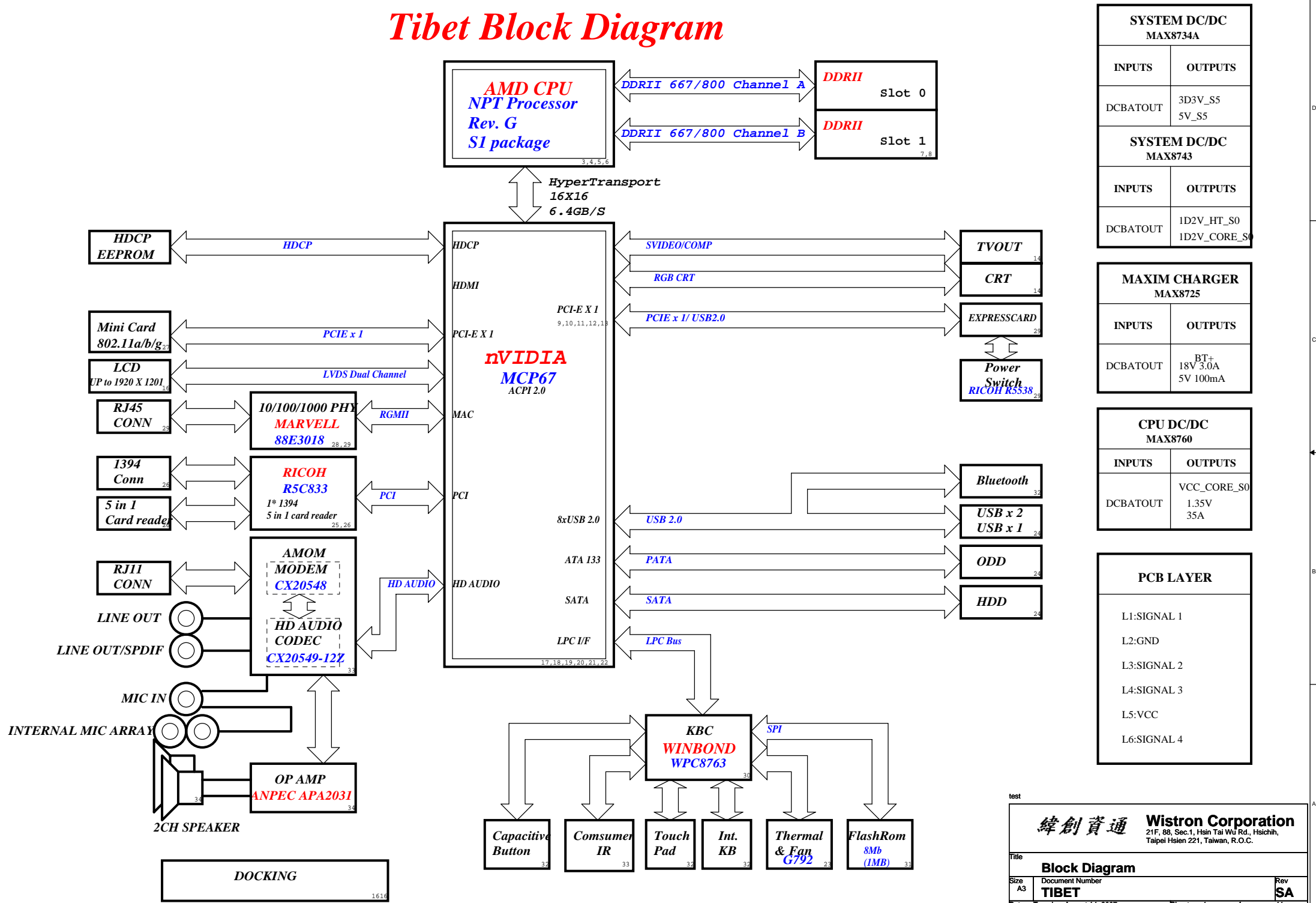


Tibet Block Diagram



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER	
L1: SIGNAL 1	
L2: GND	
L3: SIGNAL 2	
L4: SIGNAL 3	
L5: VCC	
L6: SIGNAL 4	

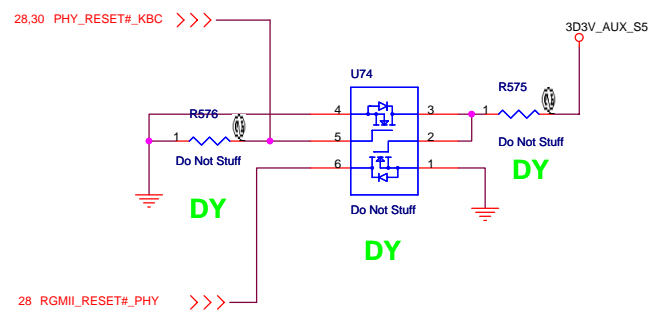
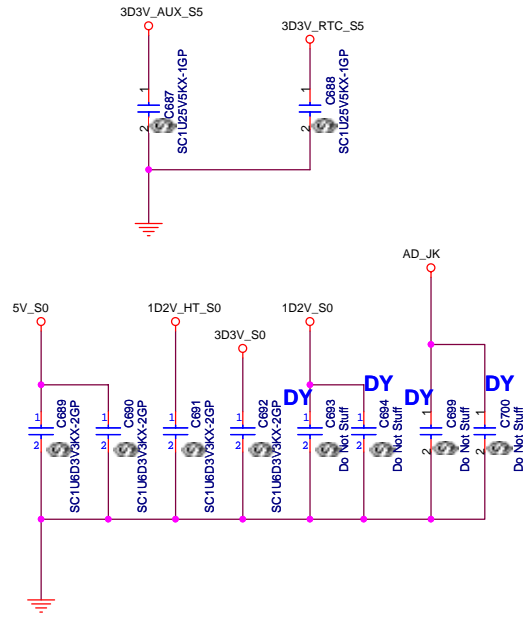
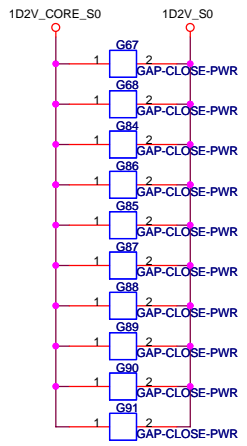
test

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 1 of 44





test

7 M_A_DQ[63..0] <<<>

<<<>

CPU1B

M_A_DQ0A12 MA_DATA63
M_A_DQ0A12 MA_DATA62
M_A_DQ0A14 MA_DATA61
M_A_DQ0A14 MA_DATA60
M_A_DQ05Y11 MA_DATA58
M_A_DQ05Y12 MA_DATA57
M_A_DQ05Y13 MA_DATA56
M_A_DQ05Y15 MA_DATA55
M_A_DQ05Y15 MA_DATA54
M_A_DQ05Y17 MA_DATA53
M_A_DQ05Y14 MA_DATA52
M_A_DQ05Y14 MA_DATA51
M_A_DQ05W14 MA_DATA50
M_A_DQ05W16 MA_DATA49
M_A_DQ05Y18 MA_DATA48
M_A_DQ05Y19 MA_DATA47
M_A_DQ05Y21 MA_DATA46
M_A_DQ05Y21 MA_DATA45
M_A_DQ05Y21 MA_DATA44
M_A_DQ05Y18 MA_DATA43
M_A_DQ05Y18 MA_DATA42
M_A_DQ05Y20 MA_DATA41
M_A_DQ05Y20 MA_DATA40
M_A_DQ05Y22 MA_DATA39
M_A_DQ05Y22 MA_DATA38
M_A_DQ05Y21 MA_DATA37
M_A_DQ05Y22 MA_DATA36
M_A_DQ05Y22 MA_DATA35
M_A_DQ05Y24 MA_DATA34
M_A_DQ05Y22 MA_DATA33
M_A_DQ05Y22 MA_DATA32
M_A_DQ05Y20 MA_DATA31
M_A_DQ05Y20 MA_DATA30
M_A_DQ05Y22 MA_DATA29
M_A_DQ05Y21 MA_DATA28
M_A_DQ05Y19 MA_DATA27
M_A_DQ05Y22 MA_DATA26
M_A_DQ05Y20 MA_DATA25
M_A_DQ05Y23 MA_DATA24
M_A_DQ05Y22 MA_DATA23
M_A_DQ05Y22 MA_DATA22
M_A_DQ05Y18 MA_DATA21
M_A_DQ05Y20 MA_DATA20
M_A_DQ05Y22 MA_DATA19
M_A_DQ05Y18 MA_DATA18
M_A_DQ05Y17 MA_DATA17
M_A_DQ05Y18 MA_DATA16
M_A_DQ05Y17 MA_DATA15
M_A_DQ05Y14 MA_DATA14
M_A_DQ05Y17 MA_DATA13
M_A_DQ05Y14 MA_DATA12
M_A_DQ05Y14 MA_DATA11
M_A_DQ05Y17 MA_DATA10
M_A_DQ05E15 MA_DATA9
M_A_DQ05H15 MA_DATA8
M_A_DQ05E13 MA_DATA7
M_A_DQ05C13 MA_DATA6
M_A_DQ05H12 MA_DATA5
M_A_DQ04H11 MA_DATA4
M_A_DQ05G14 MA_DATA3
M_A_DQ05H14 MA_DATA2
M_A_DQ05E12 MA_DATA1
M_A_DQ05G12 MA_DATA0

MA0_CLK_H2 Y16
MA0_CLK_L2 AA16
MA0_CLK_H1 E16
MA0_CLK_L1 F16

MA0_CS_L3 V19
MA0_CS_L2 J22
MA0_CS_L1 V22
MA0_CS_L0 T19

MA0_ODT1 V20
MA0_ODT0 U19

MA_CAS_L U20
MA_WE_L U21
MA_RAS_L T20

MA_BANK2 K22
MA_BANK1 R20
MA_BANK0 T22

MA_CKE1 J20
MA_CKE0 J21

MEMORY INTERFACE

MA_ADD15 K19
MA_ADD14 K20
MA_ADD13 V24
MA_ADD12 K24
MA_ADD11 L20
MA_ADD10 R19
MA_ADD9 L19
MA_ADD8 L22
MA_ADD7 L21
MA_ADD6 M19
MA_ADD5 M20
MA_ADD4 M24
MA_ADD3 M22
MA_ADD2 N22
MA_ADD1 N21
MA_ADD0 R21

MA_DQS_H7 W12
MA_DQS_L7 W13
MA_DQS_H6 W15
MA_DQS_L6 W15
MA_DQS_H5 AB19
MA_DQS_L5 AB20
MA_DQS_H4 AD23
MA_DQS_L4 AC23
MA_DQS_H3 G22
MA_DQS_L3 G22
MA_DQS_H2 C21
MA_DQS_L2 C21
MA_DQS_H1 G16
MA_DQS_L1 G15
MA_DQS_H0 G13
MA_DQS_L0 H13

M_A_CLK_DDR2# 7
M_A_CLK_DDR2# 7
M_A_CLK_DDR1# 7
M_A_CLK_DDR1# 7

M_A_CS# 7,8
M_A_CS# 7,8
M_A_CS# 7,8
M_A_CS# 7,8

M_A_ODT1 7,8
M_A_ODT0 7,8

M_A_CAS# 7,8
M_A_WE# 7,8
M_A_RAS# 7,8

M_A_BSH#2 7,8
M_A_BSH#1 7,8
M_A_BSH#0 7,8

M_A_CKE1 7,8
M_A_CKE0 7,8

M_A_A15
M_A_A14
M_A_A13
M_A_A12
M_A_A11
M_A_A10
M_A_A9
M_A_A8
M_A_A7
M_A_A6
M_A_A5
M_A_A4
M_A_A3
M_A_A2
M_A_A1
M_A_A0

M_A_A15[15..0] 7,8

M_A_DQS[7..0] 7

M_A_DQS[7..0] 7

M_A_DM7
M_A_DM6
M_A_DM5
M_A_DM4
M_A_DM3
M_A_DM2
M_A_DM1
M_A_DM0

M_A_DM7[7..0] 7

CPU1C

M_B_DQ63 AD11
M_B_DQ62 AF11
M_B_DQ61 AF14
M_B_DQ63 Y11
M_B_DQ58 AB11
M_B_DQ57 AC12
M_B_DQ56 AF13
M_B_DQ55 AF15
M_B_DQ54 AF16
M_B_DQ53 AF19
M_B_DQ52 AF19
M_B_DQ51 AD14
M_B_DQ50 AC14
M_B_DQ49 AF18
M_B_DQ48 AD18
M_B_DQ47 AD20
M_B_DQ46 AC20
M_B_DQ45 AE23
M_B_DQ44 AE24
M_B_DQ43 AF20
M_B_DQ42 AE20
M_B_DQ41 AD22
M_B_DQ40 AC22
M_B_DQ39 AE26
M_B_DQ38 AD26
M_B_DQ37 AA25
M_B_DQ36 AA26
M_B_DQ35 AE24
M_B_DQ34 AD24
M_B_DQ33 AA23
M_B_DQ32 AA24
M_B_DQ31 G24
M_B_DQ30 G23
M_B_DQ29 D26
M_B_DQ28 C26
M_B_DQ27 G26
M_B_DQ26 C25
M_B_DQ25 E24
M_B_DQ24 E23
M_B_DQ23 C24
M_B_DQ22 B24
M_B_DQ21 C20
M_B_DQ20 B20
M_B_DQ19 C25
M_B_DQ18 D24
M_B_DQ17 A21
M_B_DQ16 D20
M_B_DQ15 D18
M_B_DQ14 C18
M_B_DQ13 D14
M_B_DQ12 C14
M_B_DQ11 A20
M_B_DQ10 A19
M_B_DQ09 A16
M_B_DQ08 A15
M_B_DQ07 A13
M_B_DQ06 E11
M_B_DQ05 E11
M_B_DQ04 G11
M_B_DQ03 R14
M_B_DQ02 A14
M_B_DQ01 A11
M_B_DQ00 C11

MB_DATA63
MB_DATA62
MB_DATA61
MB_DATA60
MB_DATA59
MB_DATA58
MB_DATA57
MB_DATA56
MB_DATA55
MB_DATA54
MB_DATA53
MB_DATA52
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MB_DATA9
MB_DATA8
MB_DATA7
MB_DATA6
MB_DATA5
MB_DATA4
MB_DATA3
MB_DATA2
MB_DATA1
MB_DATA0

MEMORY INTERFACE

MB0_CLK_H2 AF18
MB0_CLK_L2 AF17
MB0_CLK_H1 A17
MB0_CLK_L1 A18

MB0_CS_L3 J24
MB0_CS_L2 W24
MB0_CS_L1 U23
MB0_CS_L0 U23

MB0_ODT1 W23
MB0_ODT0 W26

MB_CAS_L V26
MB_WE_L U22
MB_RAS_L U24

MB_BANK2 K26
MB_BANK1 T26
MB_BANK0 U26

MB_CKE1 H26
MB_CKE0 J23

MB_ADD15 J25
MB_ADD14 J26
MB_ADD13 W25
MB_ADD12 L23
MB_ADD11 L25
MB_ADD10 U25
MB_ADD9 L24
MB_ADD8 M26
MB_ADD7 L26
MB_ADD6 N23
MB_ADD5 N24
MB_ADD4 N25
MB_ADD3 N26
MB_ADD2 P24
MB_ADD1 P26
MB_ADD0 T24

M_B_A15
M_B_A14
M_B_A13
M_B_A12
M_B_A11
M_B_A10
M_B_A9
M_B_A8
M_B_A7
M_B_A6
M_B_A5
M_B_A4
M_B_A3
M_B_A2
M_B_A1
M_B_A0

M_B_DQS7
M_B_DQS#7
M_B_DQS#6
M_B_DQS#6
M_B_DQS#5
M_B_DQS#5
M_B_DQS4
M_B_DQS#4
M_B_DQS3
M_B_DQS#3
M_B_DQS2
M_B_DQS#2
M_B_DQS1
M_B_DQS#1
M_B_DQS0

M_B_DM7
M_B_DM6
M_B_DM5
M_B_DM4
M_B_DM3
M_B_DM2
M_B_DM1
M_B_DM0

M_B_CLK_DDR2# 7
M_B_CLK_DDR2# 7
M_B_CLK_DDR1# 7
M_B_CLK_DDR1# 7

M_B_CS# 7,8
M_B_CS# 7,8
M_B_CS# 7,8
M_B_CS# 7,8

M_B_ODT1 7,8
M_B_ODT0 7,8

M_B_CAS# 7,8
M_B_WE# 7,8
M_B_RAS# 7,8

M_B_BSH#2 7,8
M_B_BSH#1 7,8
M_B_BSH#0 7,8

M_B_CKE1 7,8
M_B_CKE0 7,8

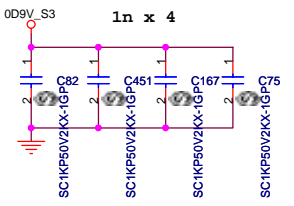
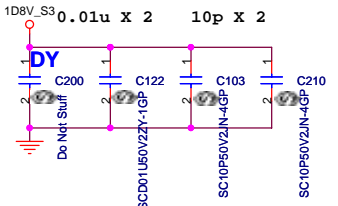
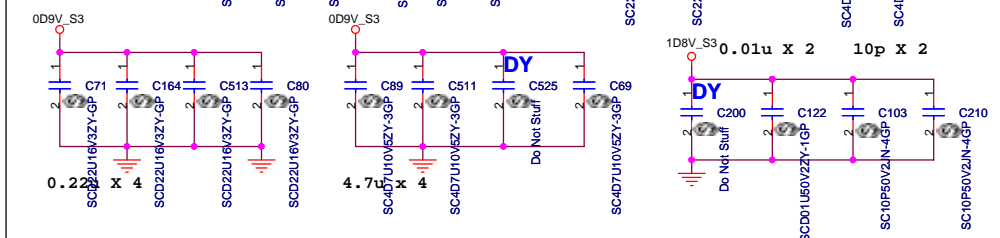
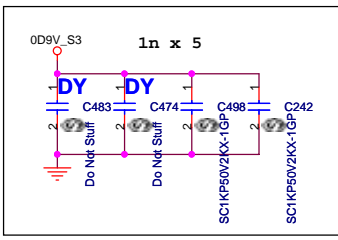
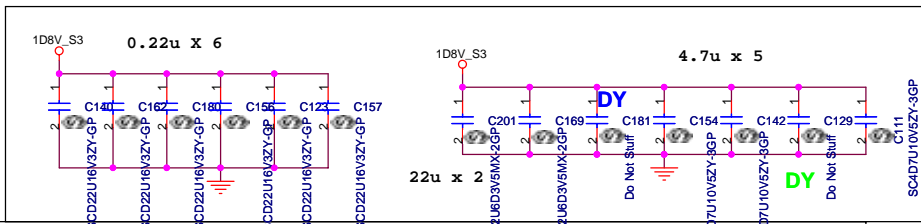
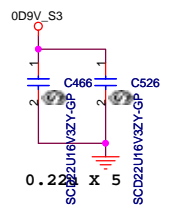
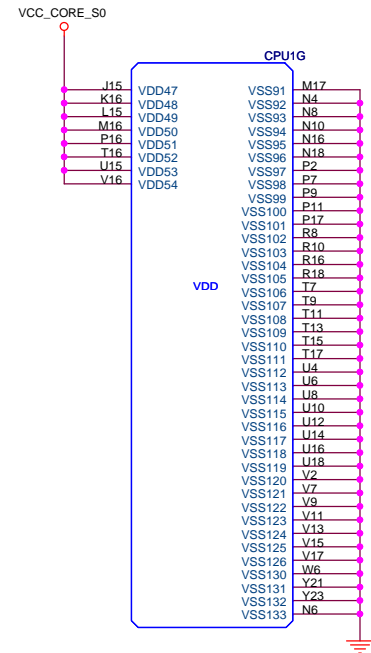
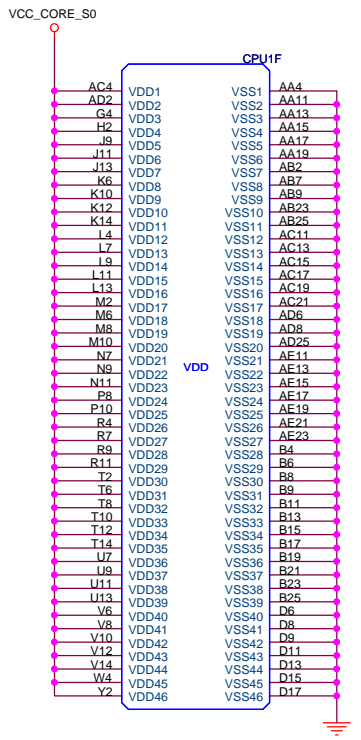
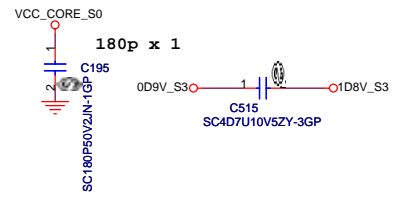
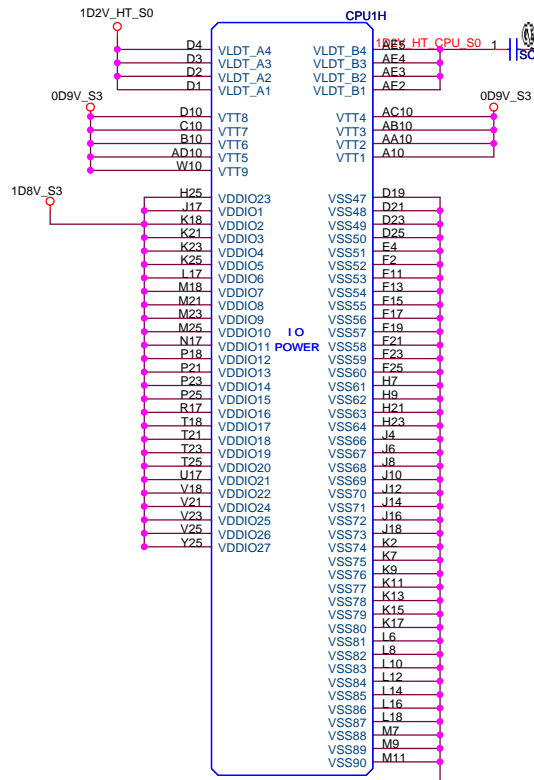
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M_B_DQS[7..0] 7

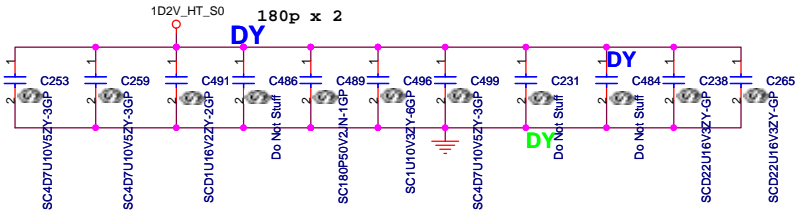
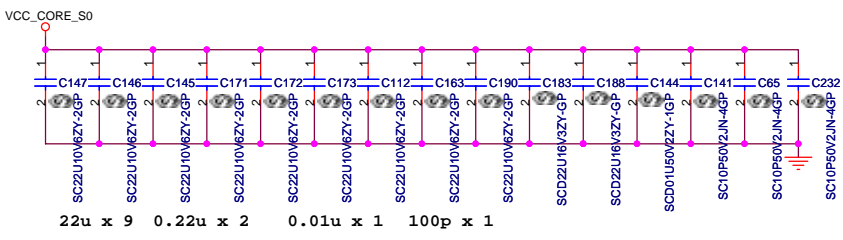
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M_B_DM[7..0] 7

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU(2/4) DDR II
TIBET
Date: Tuesday, August 14, 2007



LAYOUT: Place on backside of processor.



test

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4) POWER**

Size: A3 Document Number: TIBET Rev: SA

Date: Tuesday, August 14, 2007 Sheet 6 of 44

CPUCADOUT[15..0] 3
CPUCADOUTJ[15..0] 3

3 NB0CADOUT[15..0] 3
3 NB0CADOUTJ[15..0] 3

U55A 1 OF 8

HT

CPUCADOUT0	AF16	HT_MCP_RXD0_P	AK27	NB0CADOUT0
CPUCADOUTJ0	AG16	HT_MCP_RXD0_N	AJ27	NB0CADOUTJ0
CPUCADOUT1	AH16	HT_MCP_RXD1_P	AK26	NB0CADOUT1
CPUCADOUTJ1	AJ16	HT_MCP_RXD1_N	AL26	NB0CADOUTJ1
CPUCADOUT2	AJ15	HT_MCP_RXD2_P	AK25	NB0CADOUT2
CPUCADOUTJ2	AK15	HT_MCP_RXD2_N	AL25	NB0CADOUTJ2
CPUCADOUT3	AK16	HT_MCP_RXD3_P	AL24	NB0CADOUT3
CPUCADOUTJ3	AL16	HT_MCP_RXD3_N	AK24	NB0CADOUTJ3
CPUCADOUT4	AG17	HT_MCP_RXD4_P	AK22	NB0CADOUT4
CPUCADOUTJ4	AF17	HT_MCP_RXD4_N	AL22	NB0CADOUTJ4
CPUCADOUT5	AL17	HT_MCP_RXD5_P	AK21	NB0CADOUT5
CPUCADOUTJ5	AK17	HT_MCP_RXD5_N	AL21	NB0CADOUTJ5
CPUCADOUT6	AL18	HT_MCP_RXD6_P	AJ21	NB0CADOUT6
CPUCADOUTJ6	AK18	HT_MCP_RXD6_N	AL20	NB0CADOUTJ6
CPUCADOUT7	AJ19	HT_MCP_RXD7_P	AM20	NB0CADOUT7
CPUCADOUTJ7	AK19	HT_MCP_RXD7_N	AG27	NB0CADOUT8
CPUCADOUT8	AD14	HT_MCP_RXD8_P	AH27	NB0CADOUTJ8
CPUCADOUTJ8	AE14	HT_MCP_RXD8_N	AF25	NB0CADOUT9
CPUCADOUT9	AF14	HT_MCP_RXD9_P	AG25	NB0CADOUTJ9
CPUCADOUTJ9	AG14	HT_MCP_RXD9_N	AH25	NB0CADOUT10
CPUCADOUT10	AH14	HT_MCP_RXD10_P	AJ25	NB0CADOUTJ10
CPUCADOUTJ10	AI14	HT_MCP_RXD10_N	AE23	NB0CADOUT11
CPUCADOUT11	AL13	HT_MCP_RXD11_P	AE23	NB0CADOUTJ11
CPUCADOUTJ11	AK13	HT_MCP_RXD11_N	AD21	NB0CADOUT12
CPUCADOUT12	AC15	HT_MCP_RXD12_P	AE21	NB0CADOUTJ12
CPUCADOUTJ12	AD15	HT_MCP_RXD12_N	AE21	NB0CADOUT13
CPUCADOUT13	AD18	HT_MCP_RXD13_P	AG21	NB0CADOUTJ13
CPUCADOUTJ13	AE16	HT_MCP_RXD13_N	AC20	NB0CADOUT14
CPUCADOUT14	AE17	HT_MCP_RXD14_P	AD20	NB0CADOUTJ14
CPUCADOUTJ14	AD17	HT_MCP_RXD14_N	AE19	NB0CADOUT15
CPUCADOUT15	AB17	HT_MCP_RXD15_P	AE19	NB0CADOUTJ15
CPUCADOUTJ15	AC17	HT_MCP_RXD15_N		

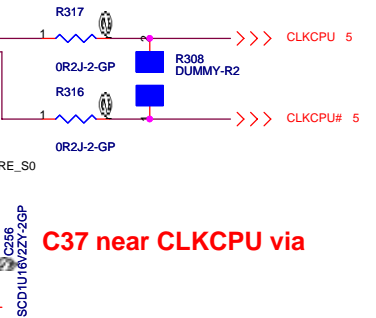
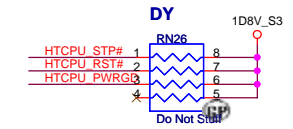
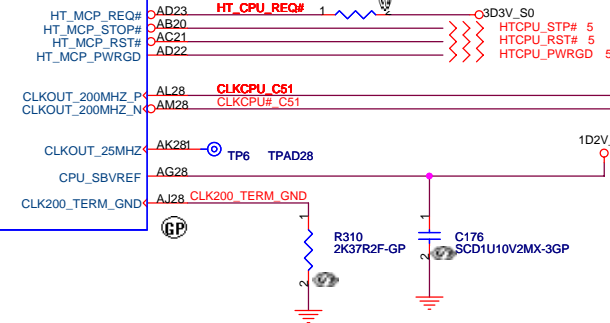
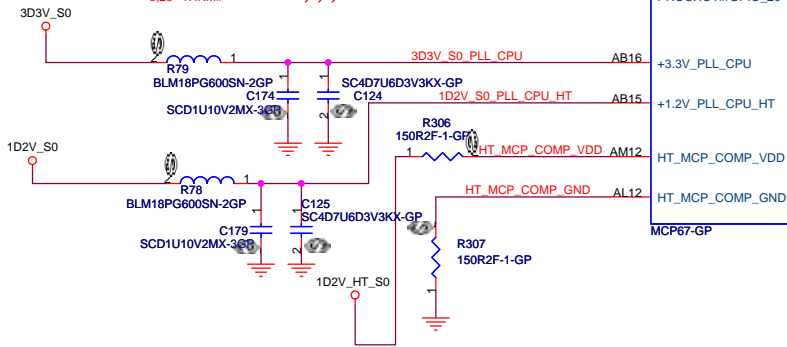
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3 CPUHTTCLKOUTJ0	>>>	CPUHTTCLKOUTJ0	AH17	HT_MCP_RX_CLK0_N
3 CPUHTTCLKOUT1	>>>	CPUHTTCLKOUT1	AL14	HT_MCP_RX_CLK1_P
3 CPUHTTCLKOUTJ1	>>>	CPUHTTCLKOUTJ1	AK14	HT_MCP_RX_CLK1_N

HT_MCP_TX_CLK0_P	AK23	NB0HTTCLKOUT0	>>>	NB0HTTCLKOUT0 3
HT_MCP_TX_CLK0_N	AJ23	NB0HTTCLKOUTJ0	>>>	NB0HTTCLKOUTJ0 3
HT_MCP_TX_CLK1_P	AG23	NB0HTTCLKOUT1	>>>	NB0HTTCLKOUT1 3
HT_MCP_TX_CLK1_N	AH23	NB0HTTCLKOUTJ1	>>>	NB0HTTCLKOUTJ1 3

3 CPUHTTCTLOUT0	>>>	CPUHTTCTLOUT0	AH19	HT_MCP_RXCTL0_P
3 CPUHTTCTLOUTJ0	>>>	CPUHTTCTLOUTJ0	AG19	HT_MCP_RXCTL0_N
			AC18	RESERVED#AC18
			AD18	RESERVED#AD18

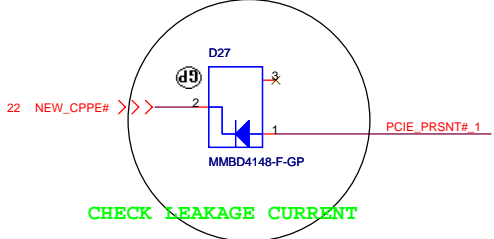
HT_MCP_TXCTL0_P	AK20	NB0HTTCTLOUT 3	>>>	NB0HTTCTLOUT 3
HT_MCP_TXCTL0_N	AJ20	NB0HTTCTLOUTJ 3	>>>	NB0HTTCTLOUTJ 3
RESERVED#AD19	AD19			
RESERVED#AC19	AC19			

5 CPU_THERMTRIP# >>> AC13 THERMTRIP#/GPIO_58
5.23 THR# >>> AB13 PROCHOT#/GPIO_20



C37 near CLKCPU via

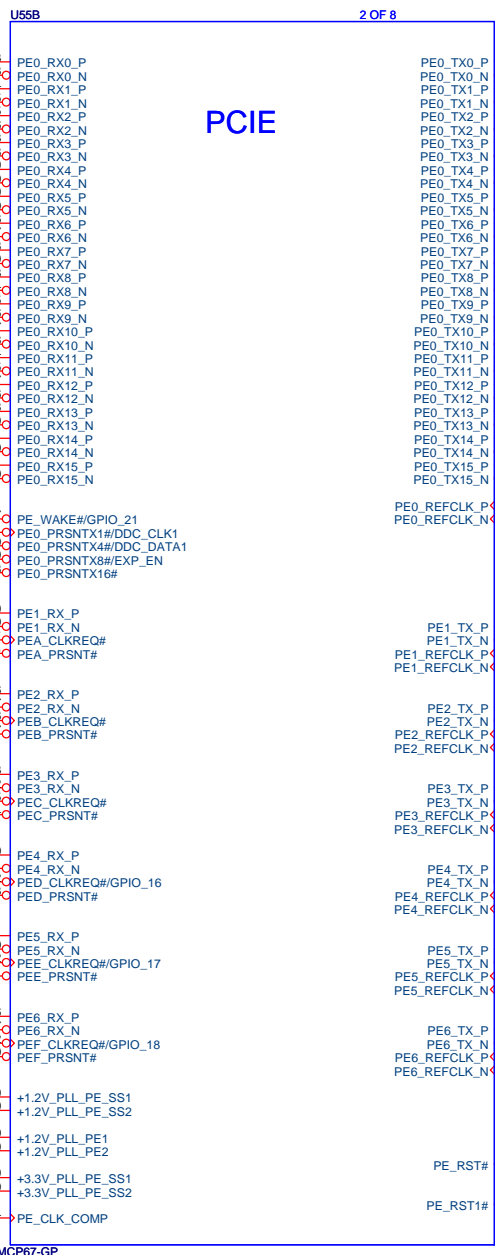
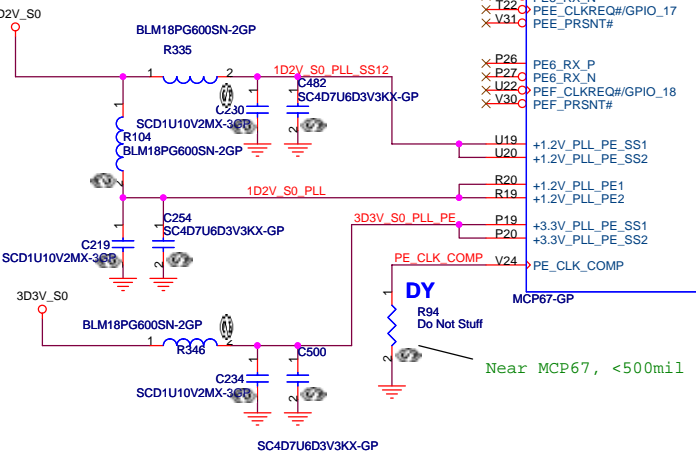
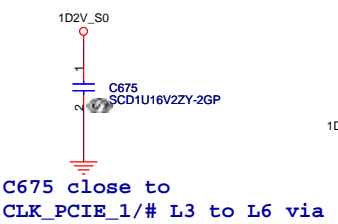
test



NEW CARD

MINI CARD1

MINI CARD2

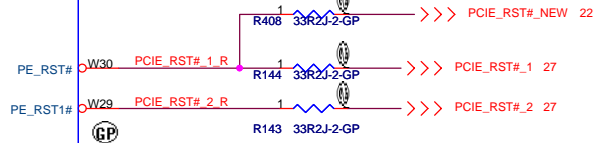
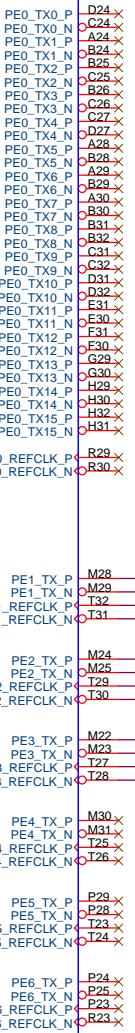


PCIE

2 OF 8

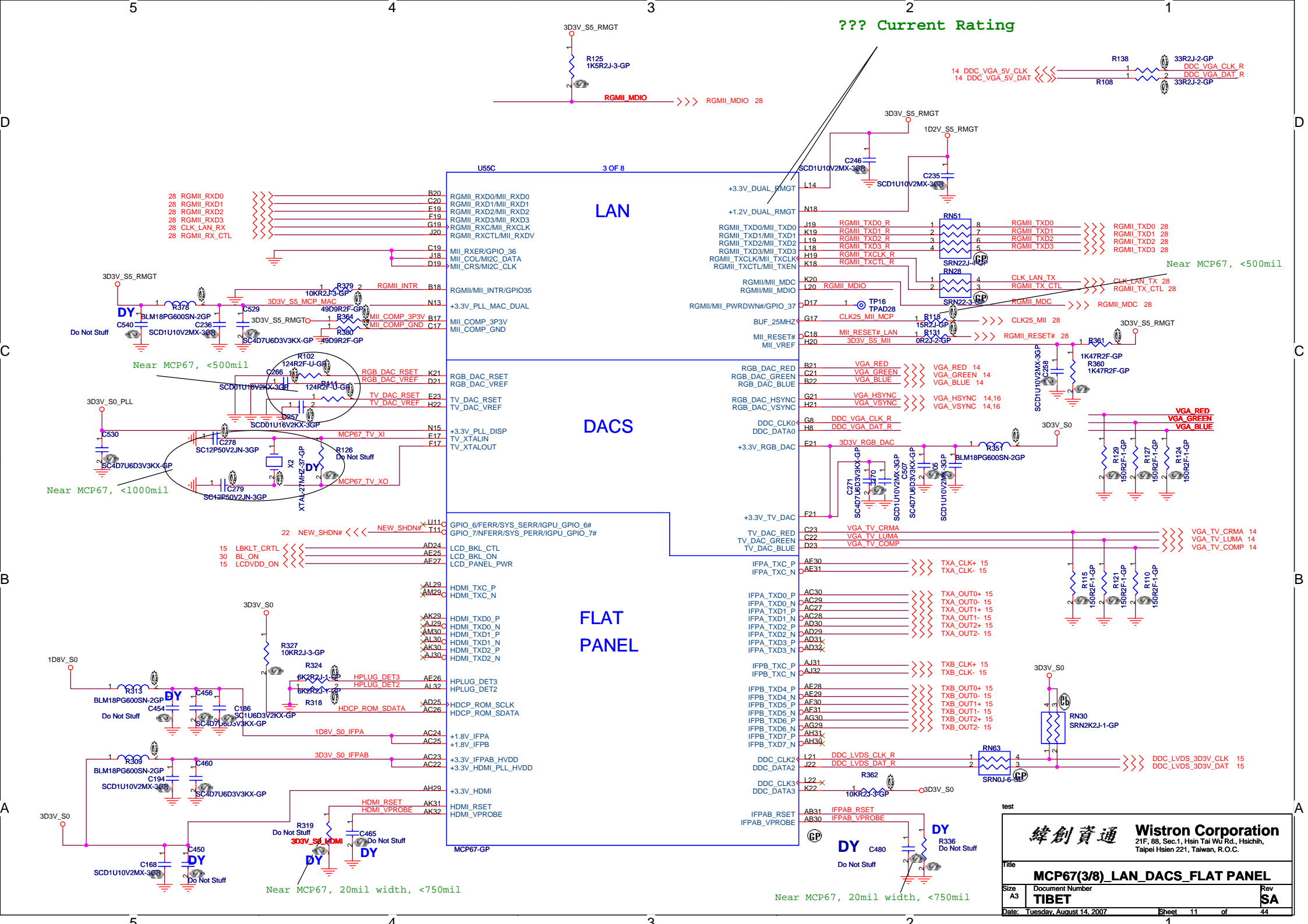
Near Connector, <500mil

For New_Card



test

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MCP67(2/8)_PCIE			
Size A3	Document Number TIBET	Rev SA	
Date: Tuesday, August 14, 2007		Sheet 10	of 44



??? Current Rating

LAN

DACS

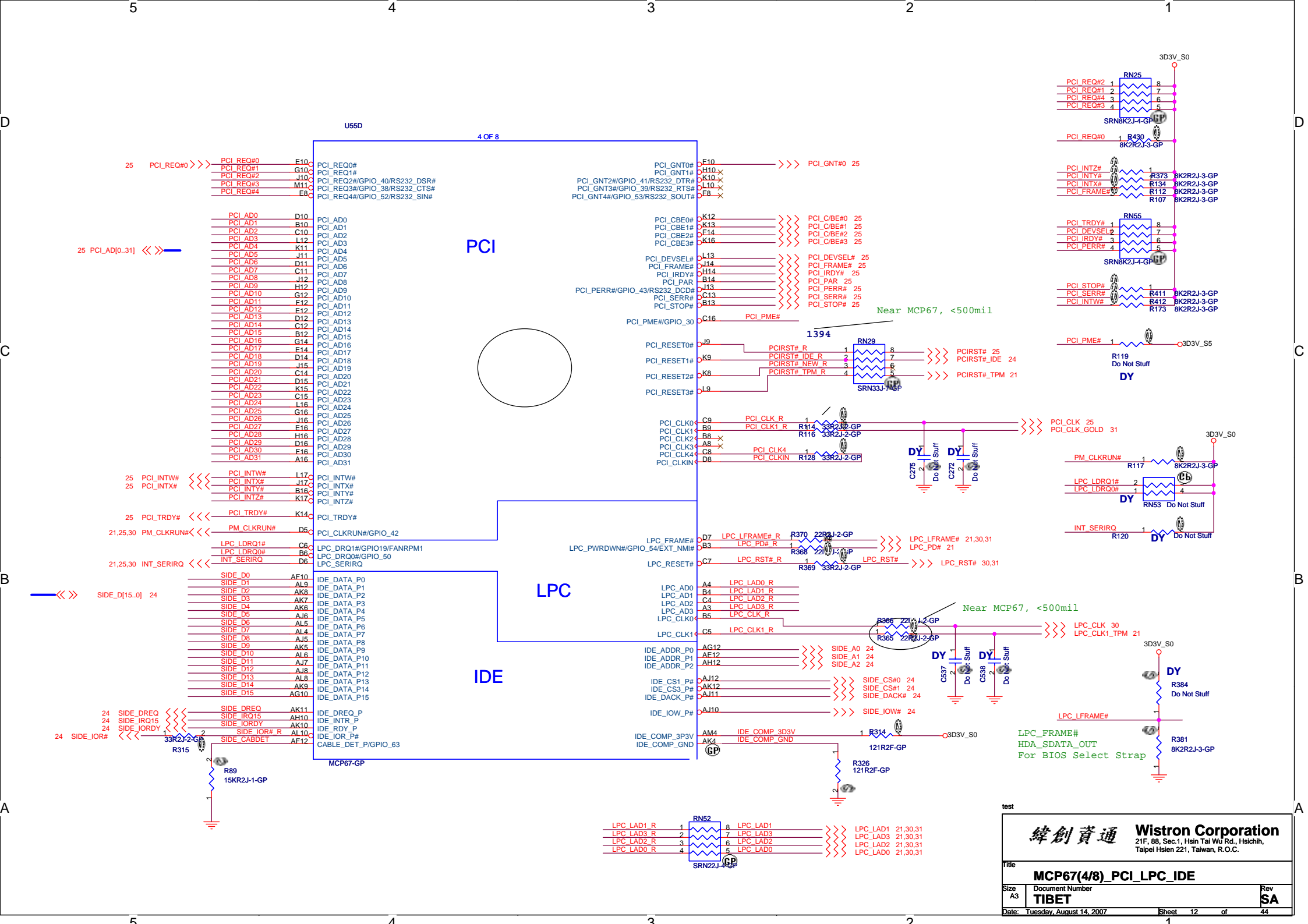
FLAT PANEL

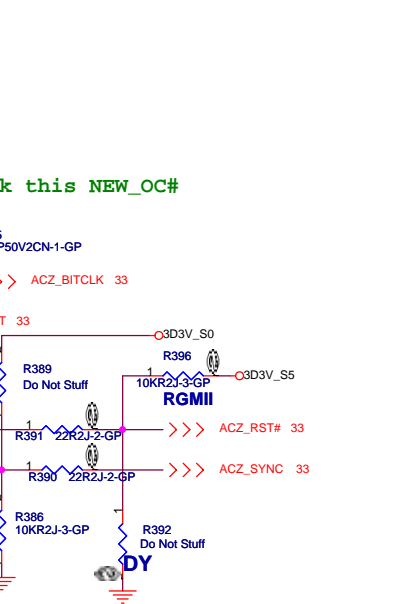
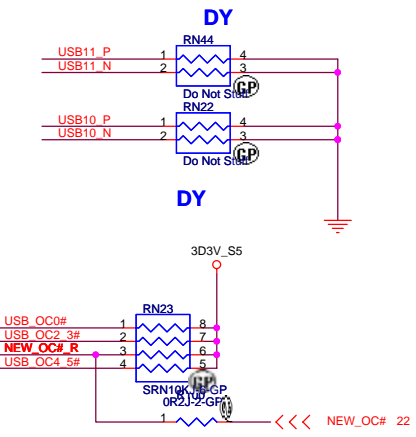
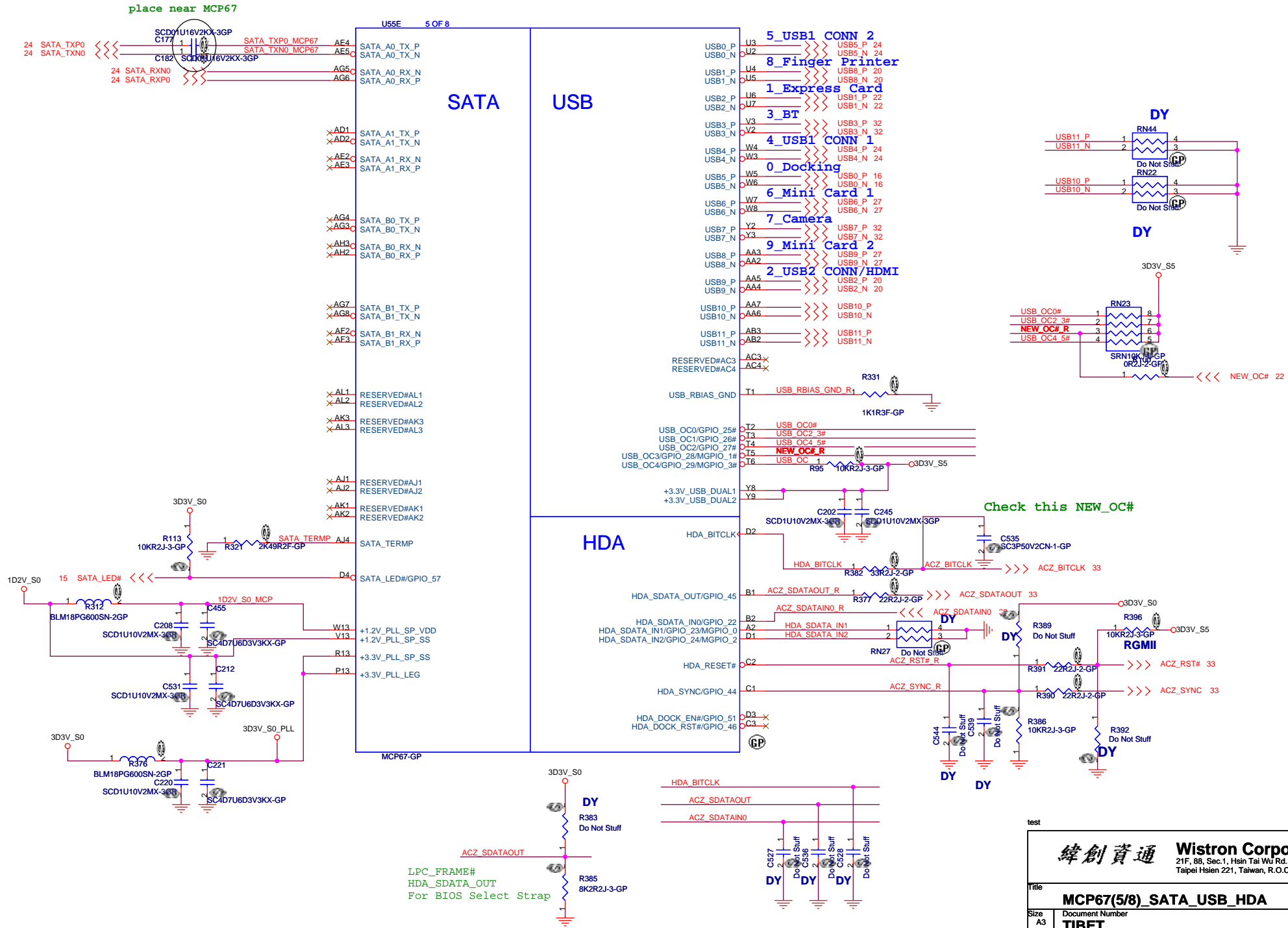
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP67(3/8)_LAN_DACS_FLAT_PANEL

Size: A3 Document Number: TIBET Rev: SA

Date: Tuesday, August 14, 2007 Sheet: 11 of 44





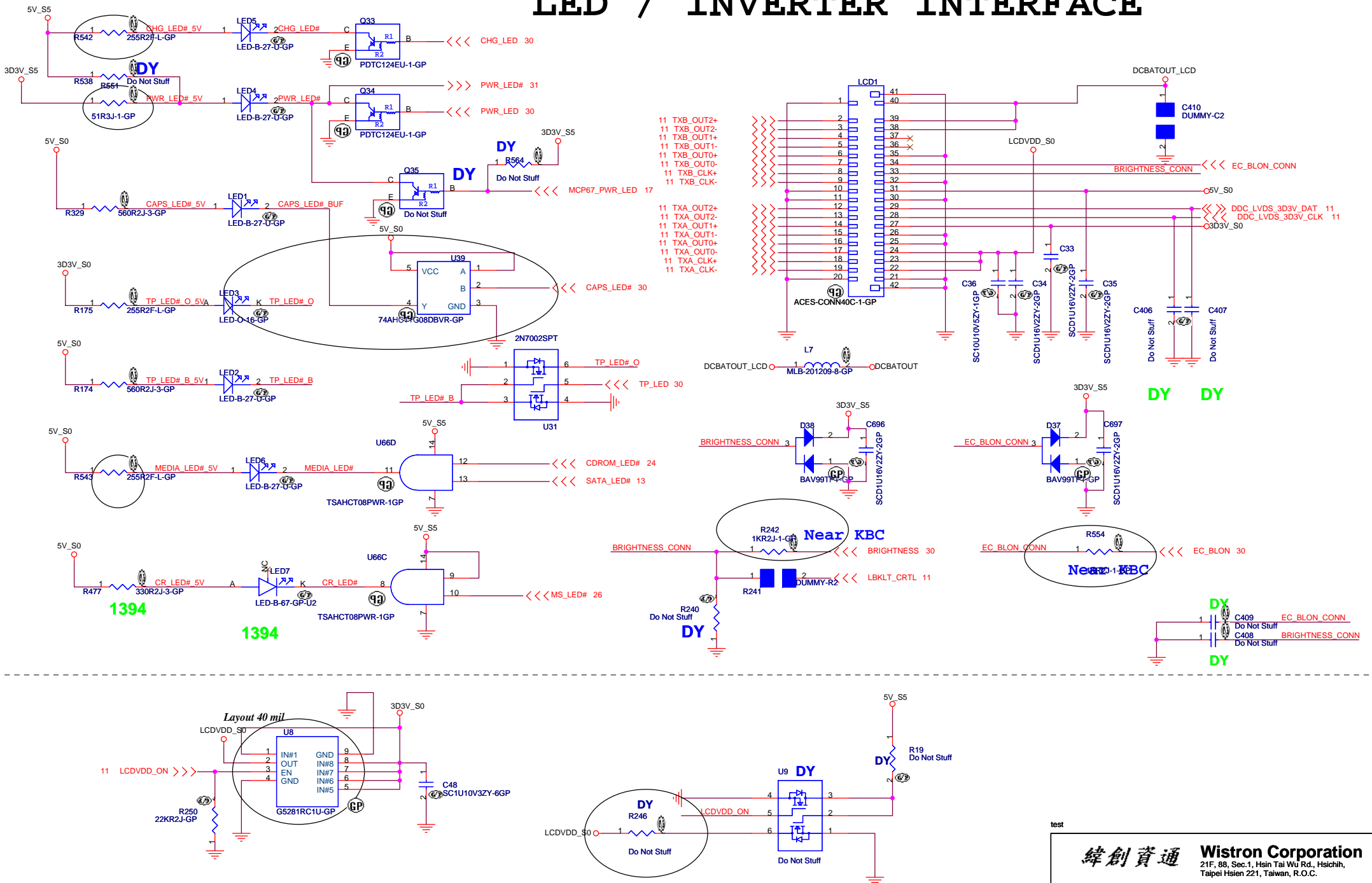
test

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(5/8)_SATA_USB_HDA**

Size: A3	Document Number: TIBET	Rev: SA
Date: Tuesday, August 14, 2007	Sheet: 13	of 44

LED / INVERTER INTERFACE

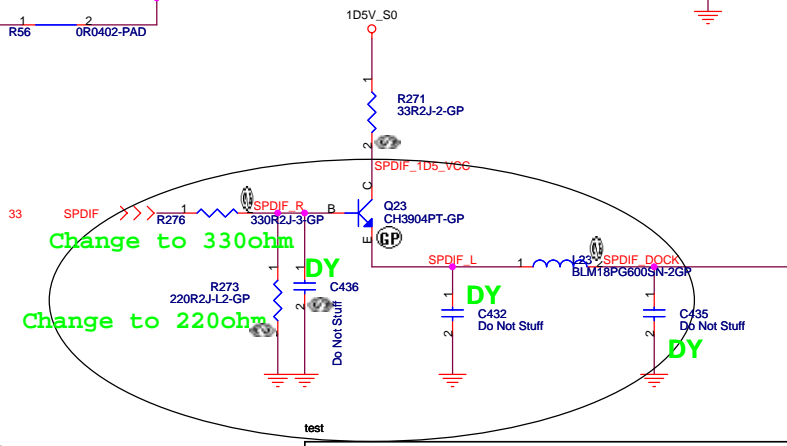
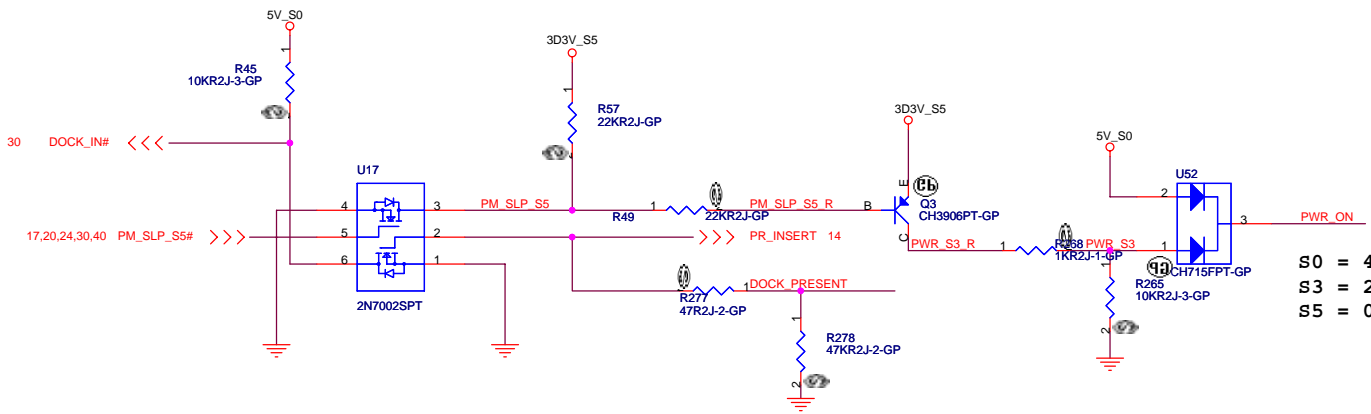
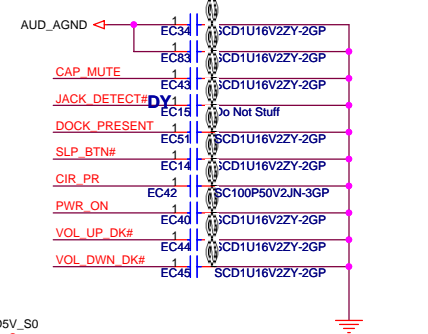
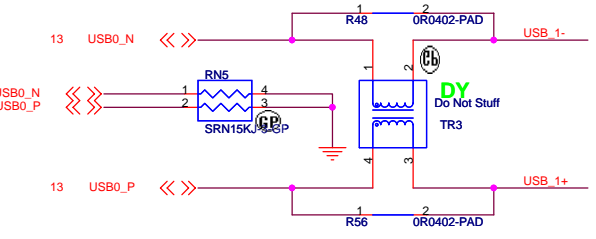
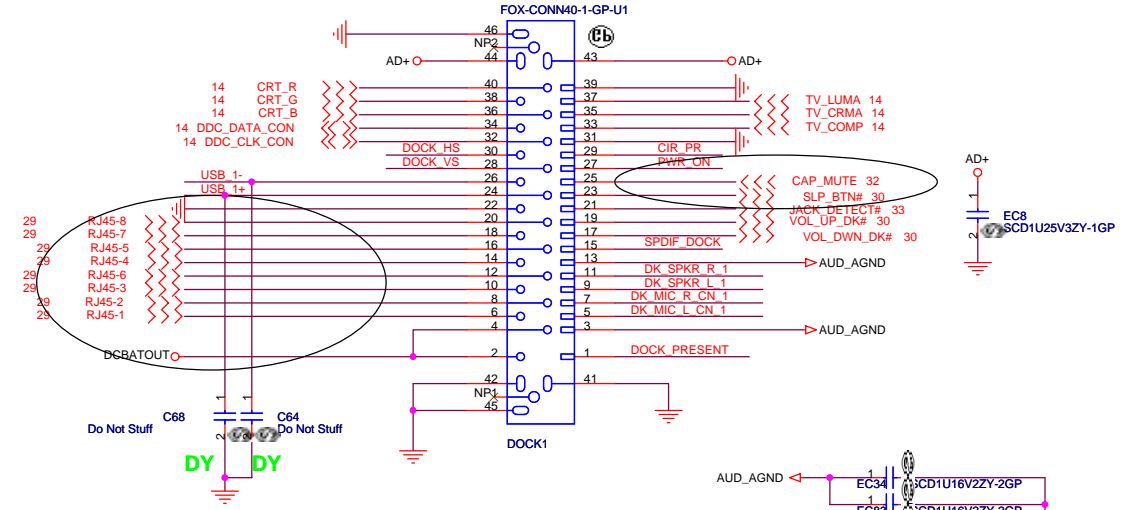
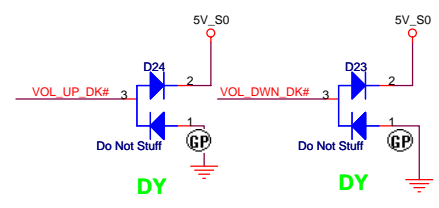
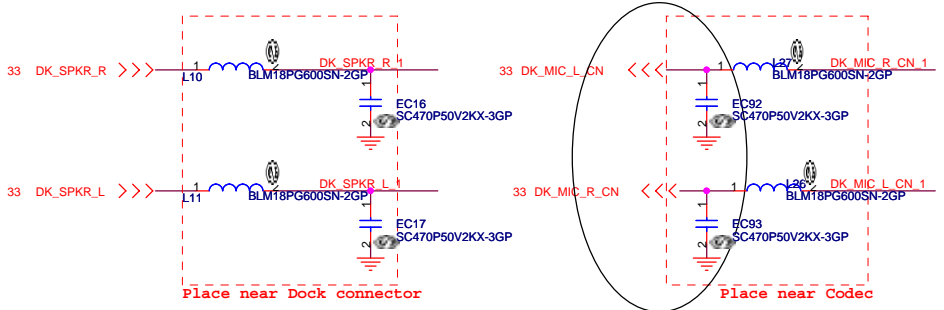
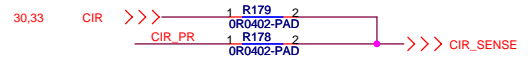
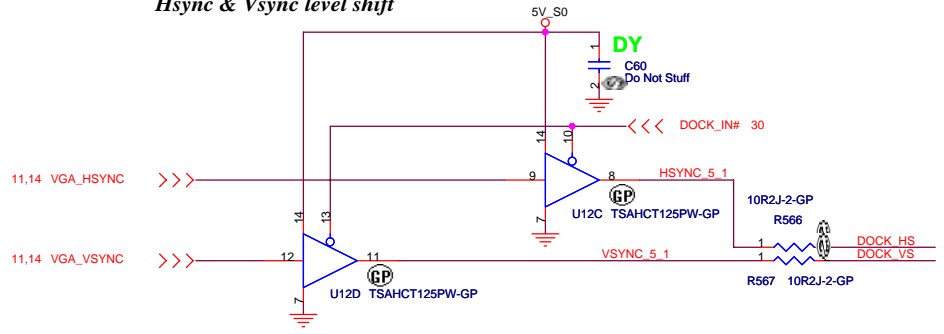


test

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD/Inverter Connector
Size Custom	Document Number
Date: Tuesday, August 14, 2007	TIBET
Sheet 15 of 44	Rev SA

Docking Connector

Hsync & Vsync level shift

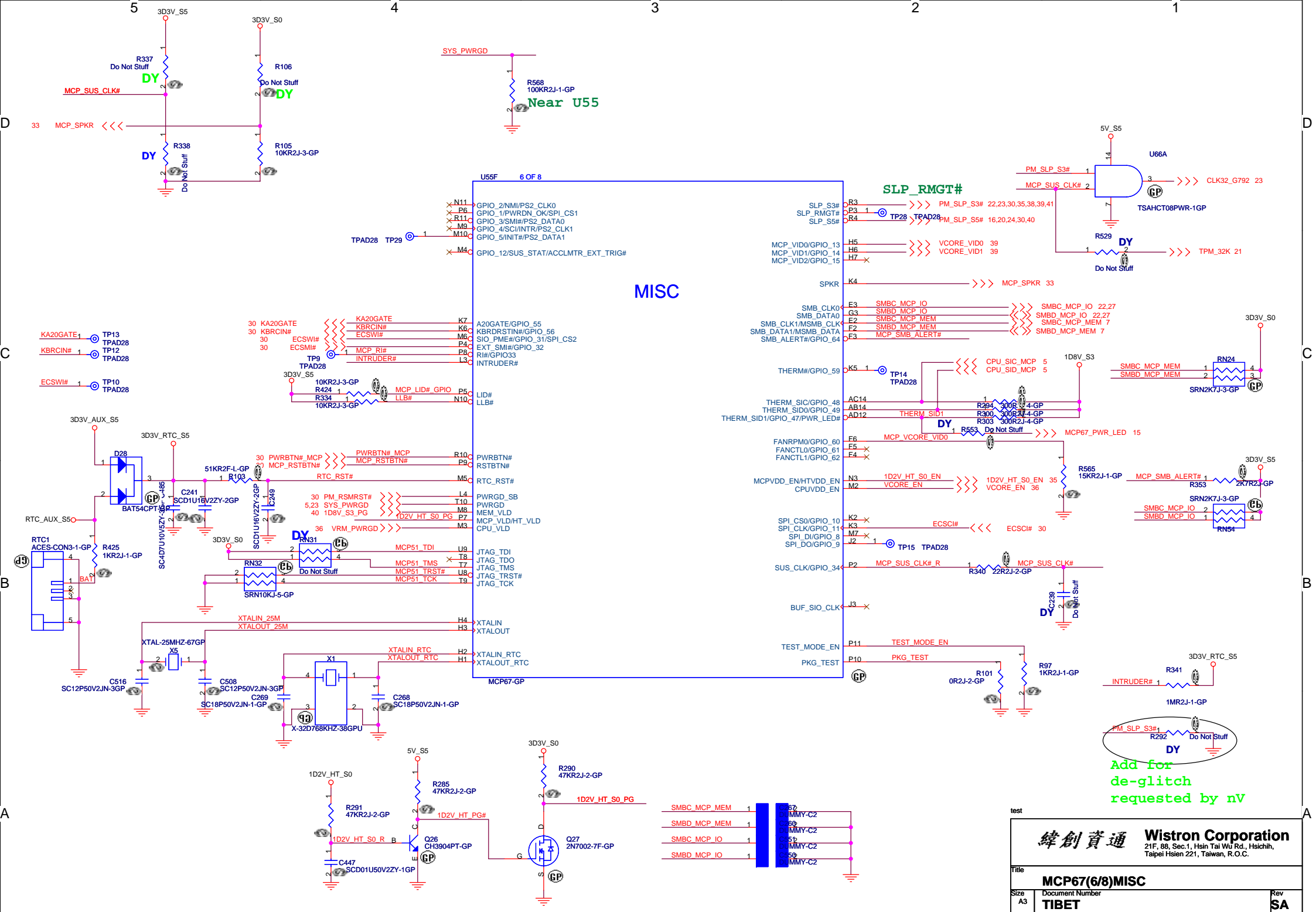


S0 = 4V
S3 = 2.5V
S5 = 0V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

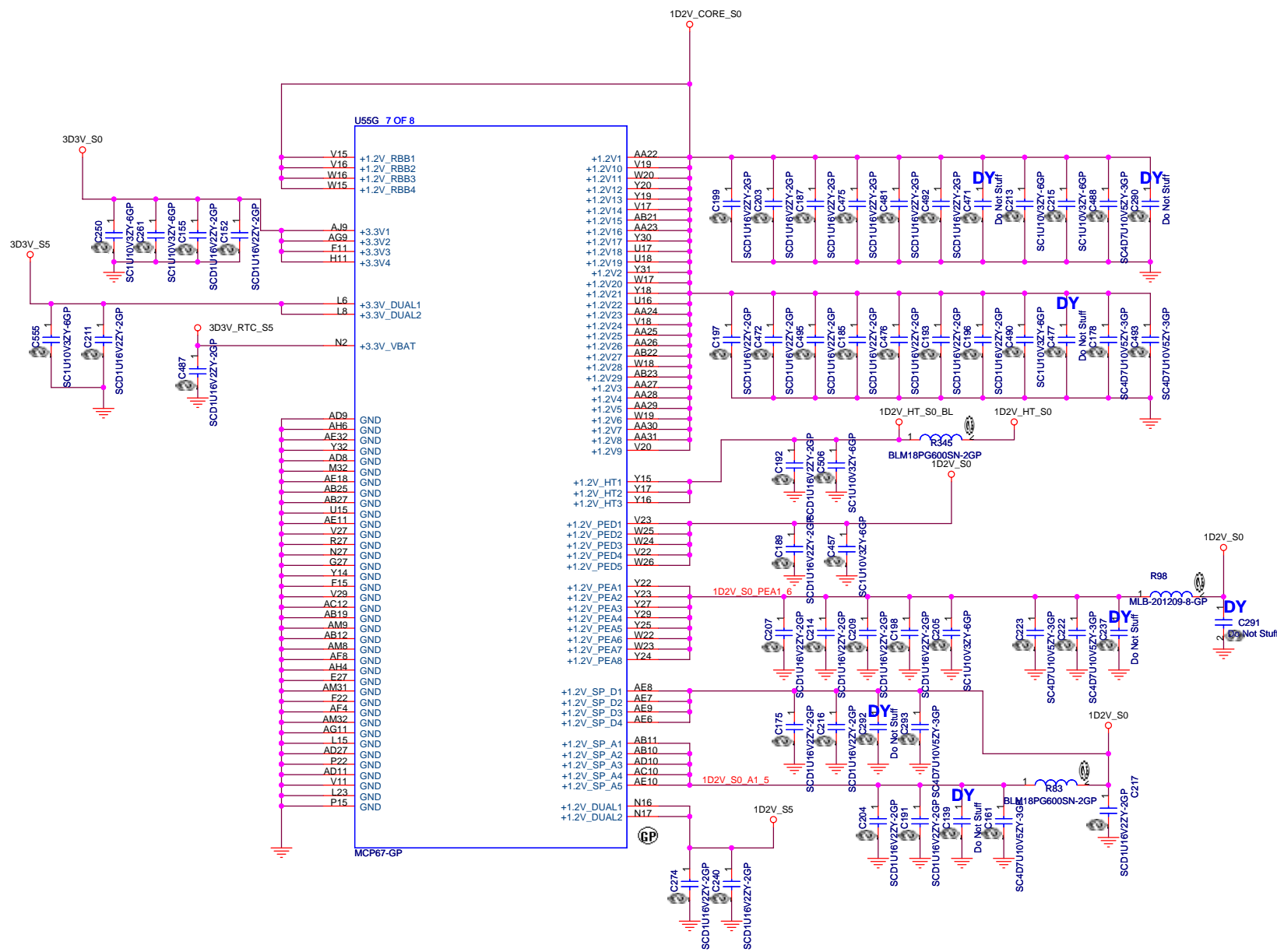
Size A3	Document Number	Rev SA
TIBET		
Date: Tuesday, August 14, 2007	Sheet 16	of 44



MISC

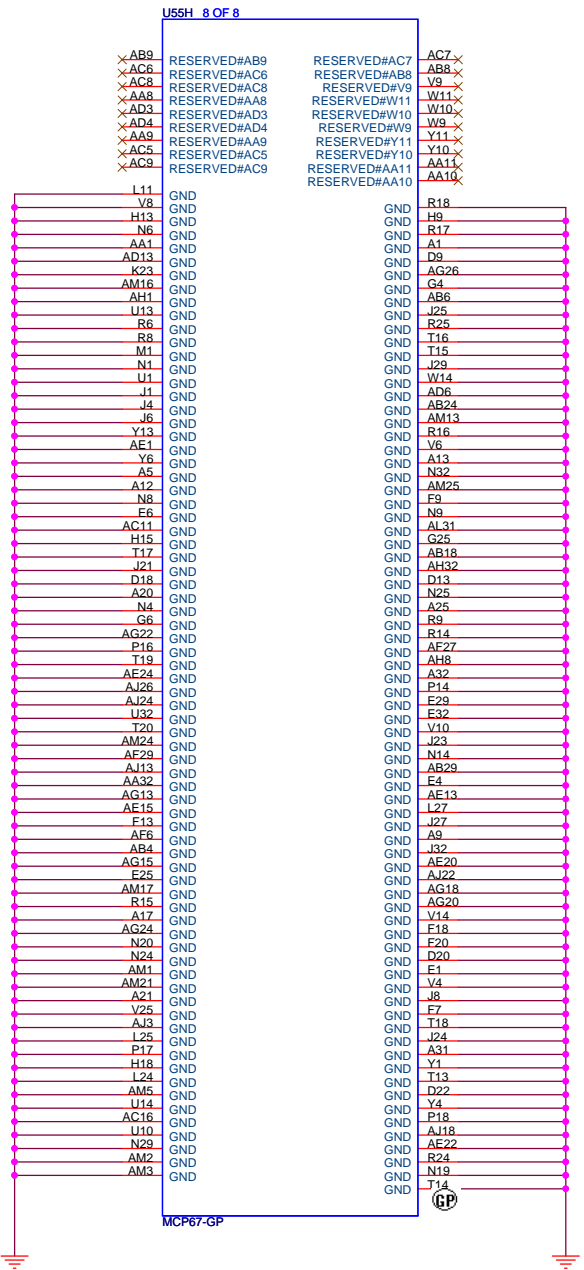
Add for de-glitch requested by nV

		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
MCP67(6/8)MISC		
Size A3	Document Number	Rev SA
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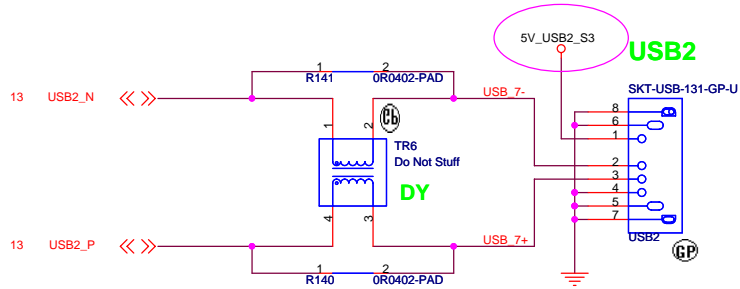
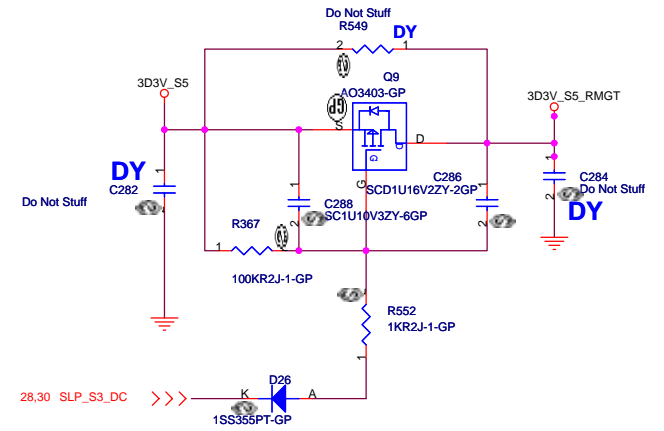
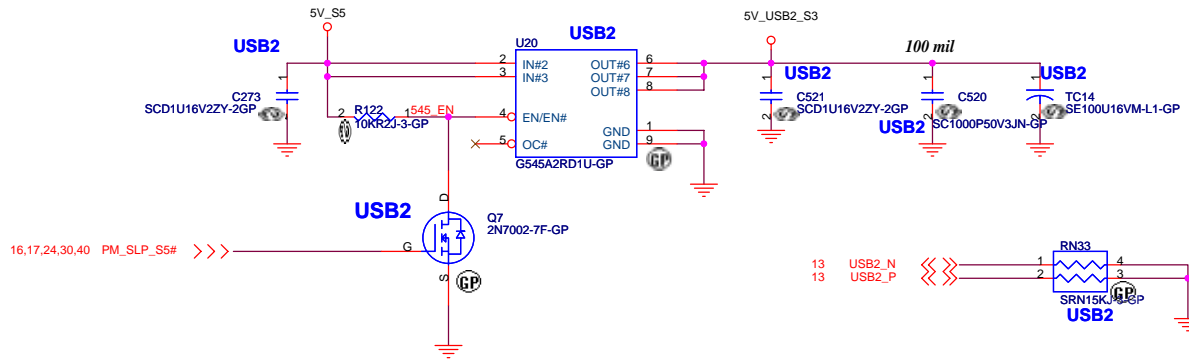
test

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MCP67(7/8)_POWER			
Size	Document Number	Rev	
A3	TIBET	SA	
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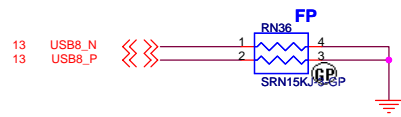
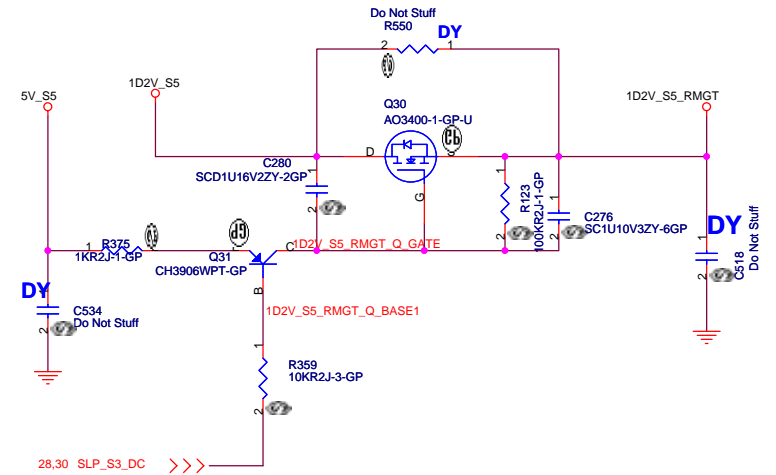


test

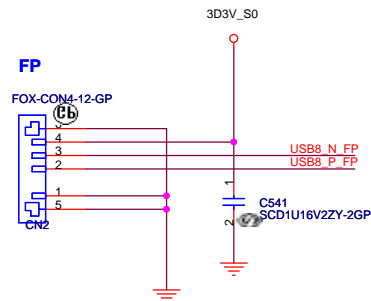
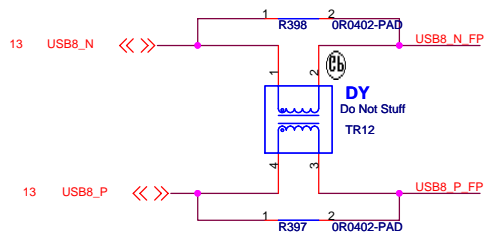
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MCP67(8/8)_GND			
Size	Document Number	Rev	
A3	TIBET	SA	
Date: Tuesday, August 14, 2007		Sheet 19	of 44



??? Current Rating



Finger Printer

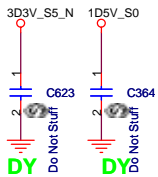


test

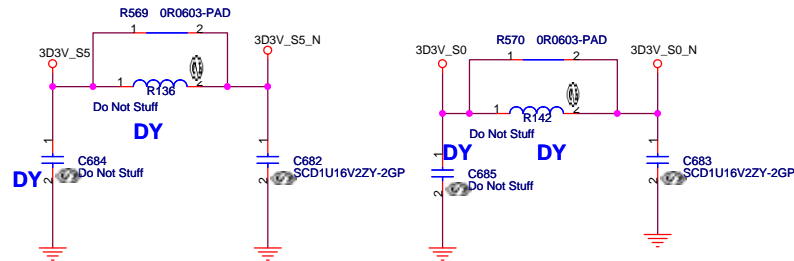
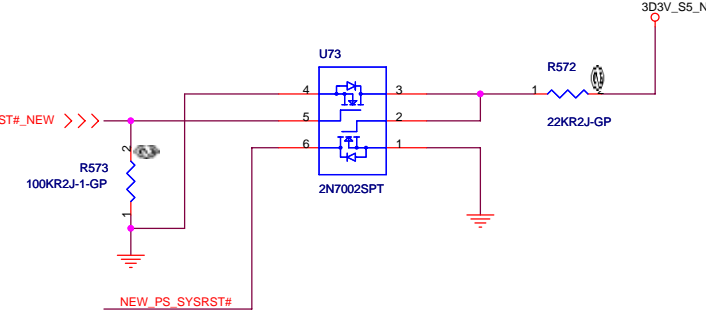
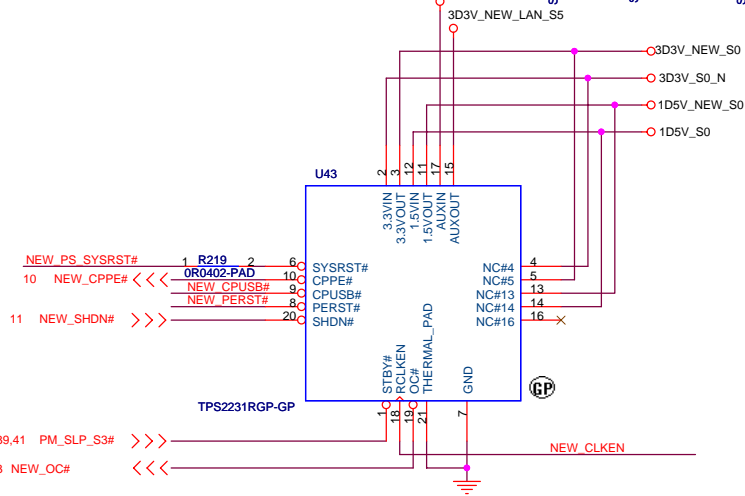
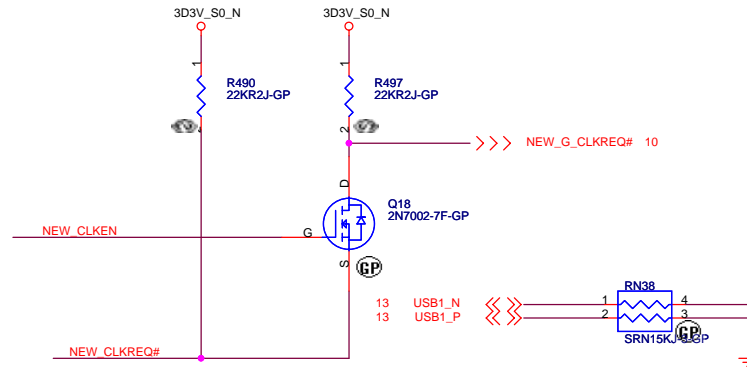
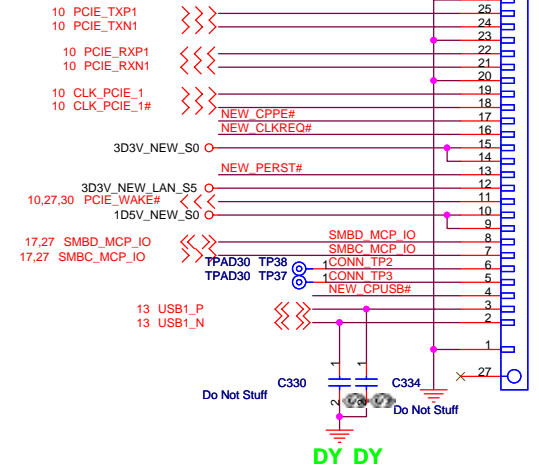
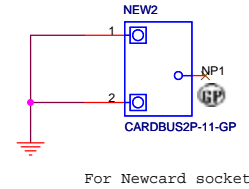
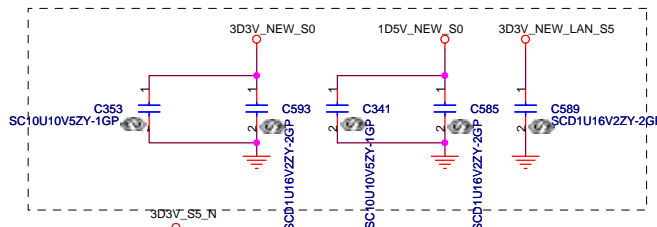
<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title HDMI/FINGER PRINTER</p>	
<p>Size A3</p>	<p>Document Number TIBET</p>
<p>Date: Tuesday, August 14, 2007</p>	<p>Sheet 20 of 44</p>
<p>Rev SA</p>	

NEWCARD Connector

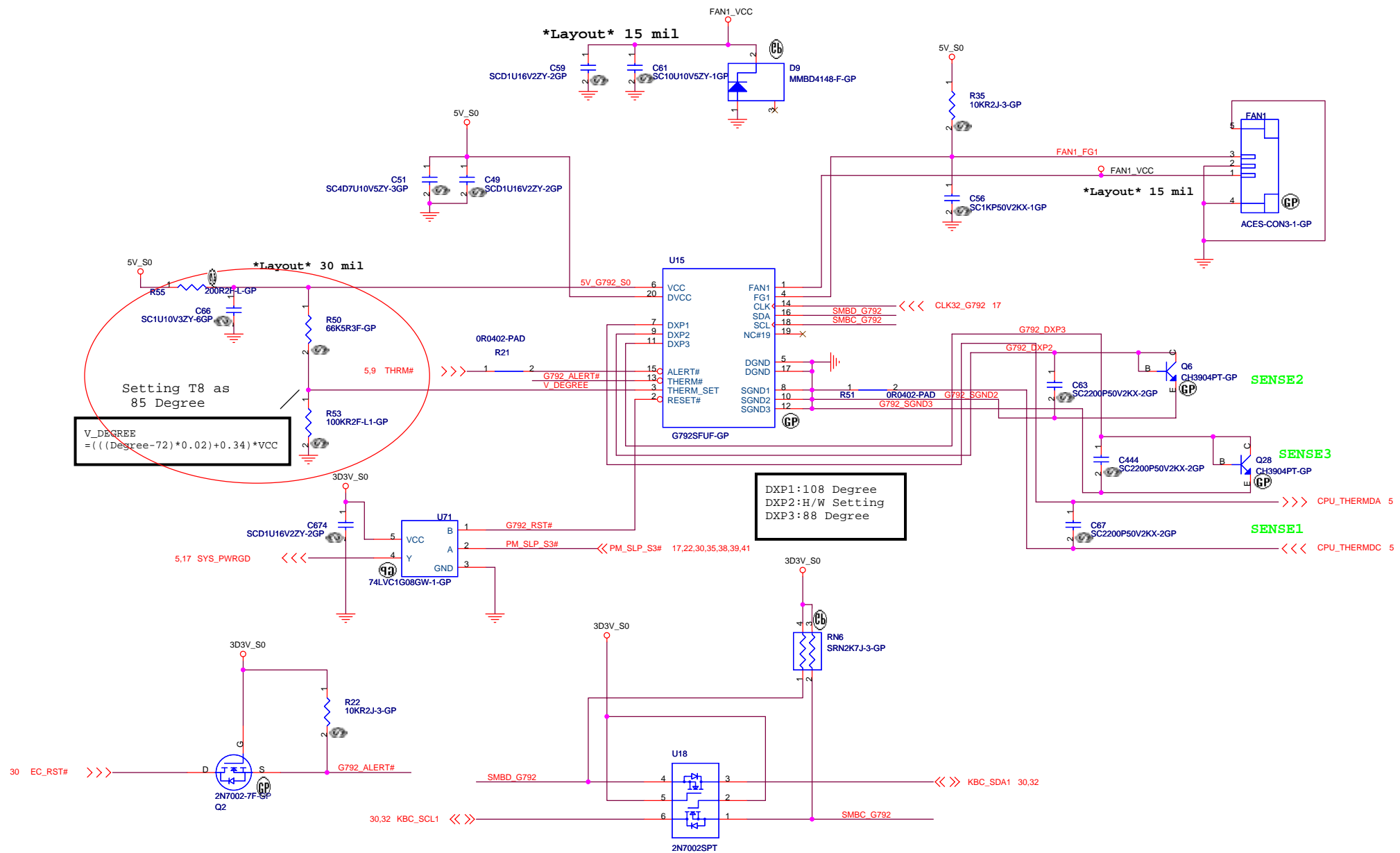
Place them Near to Chip



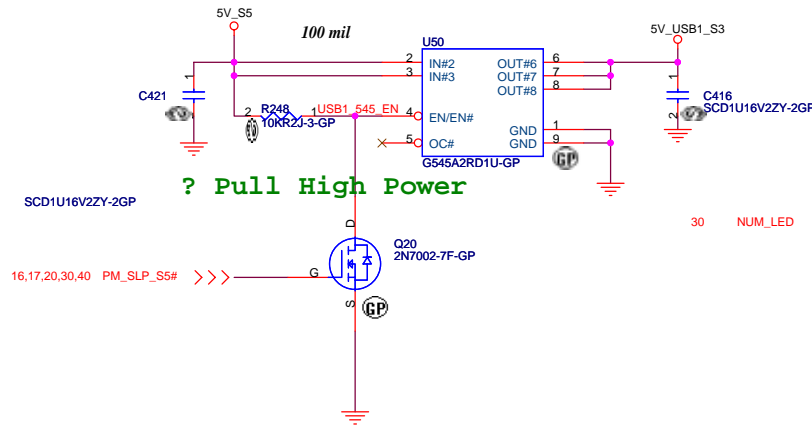
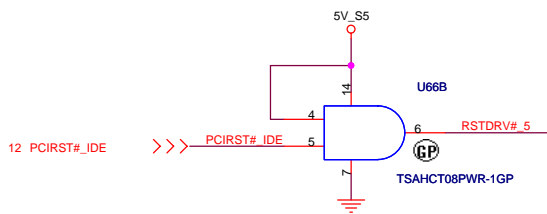
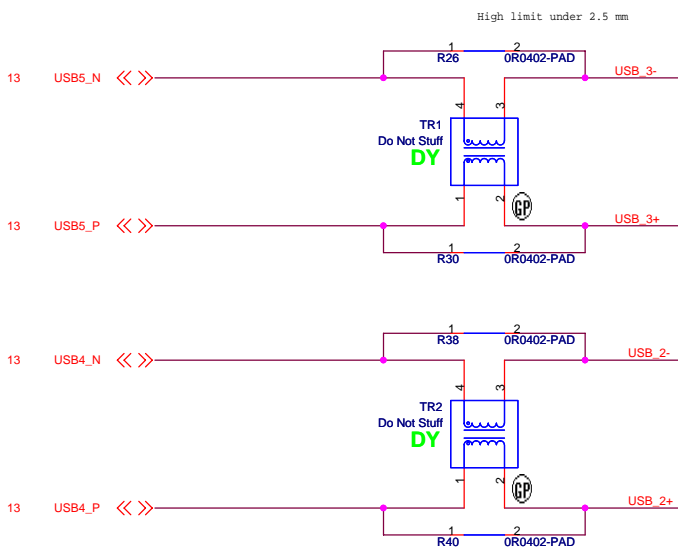
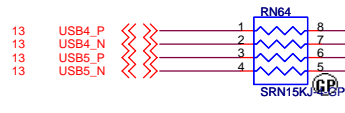
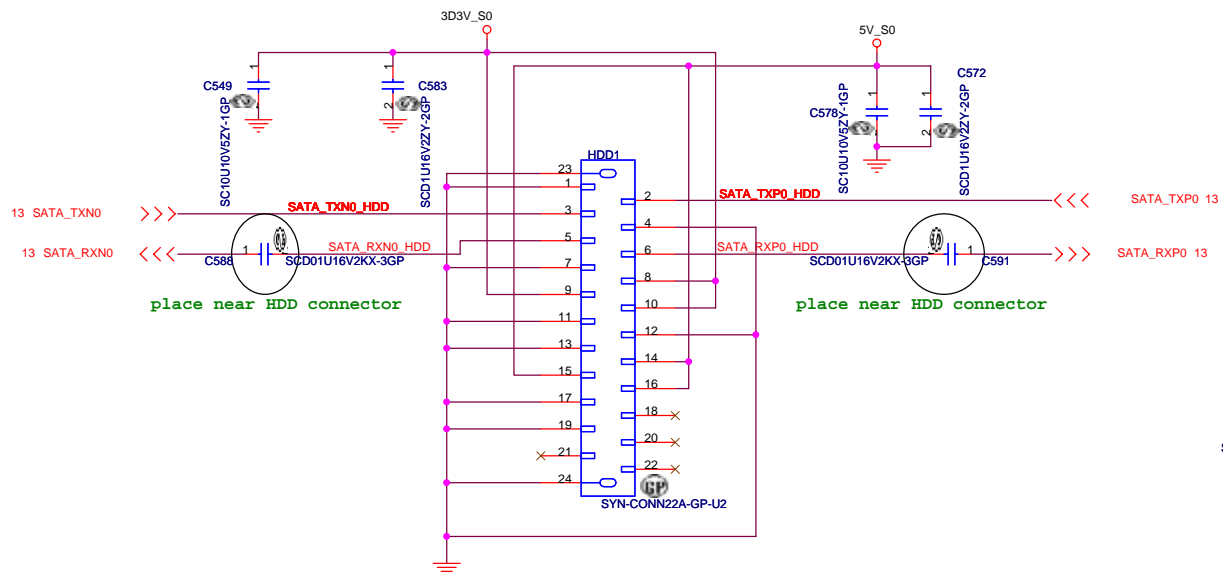
Place them Near to Connector



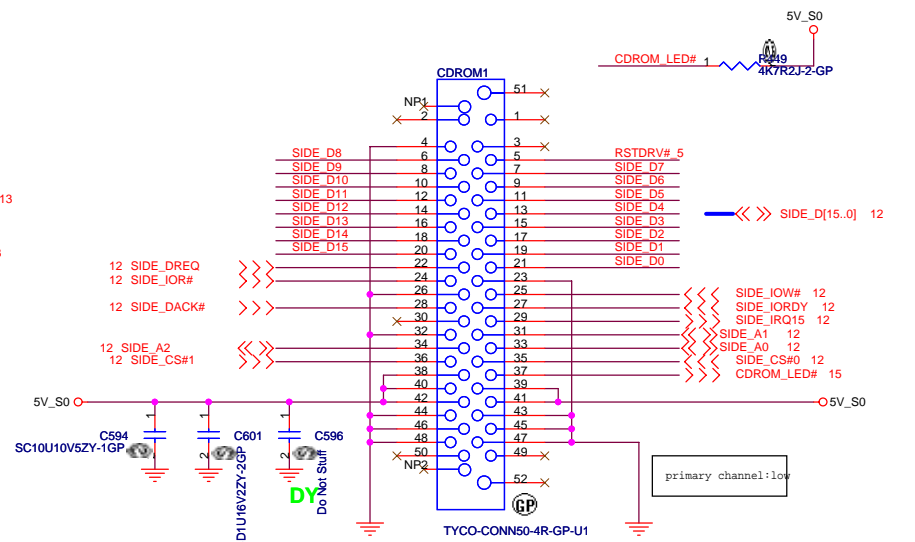
test



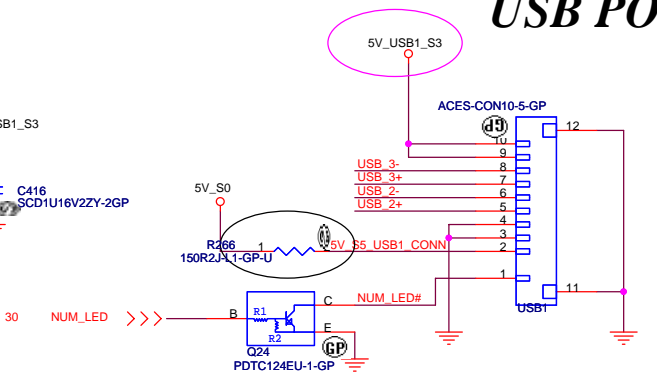
SATA HD Connector

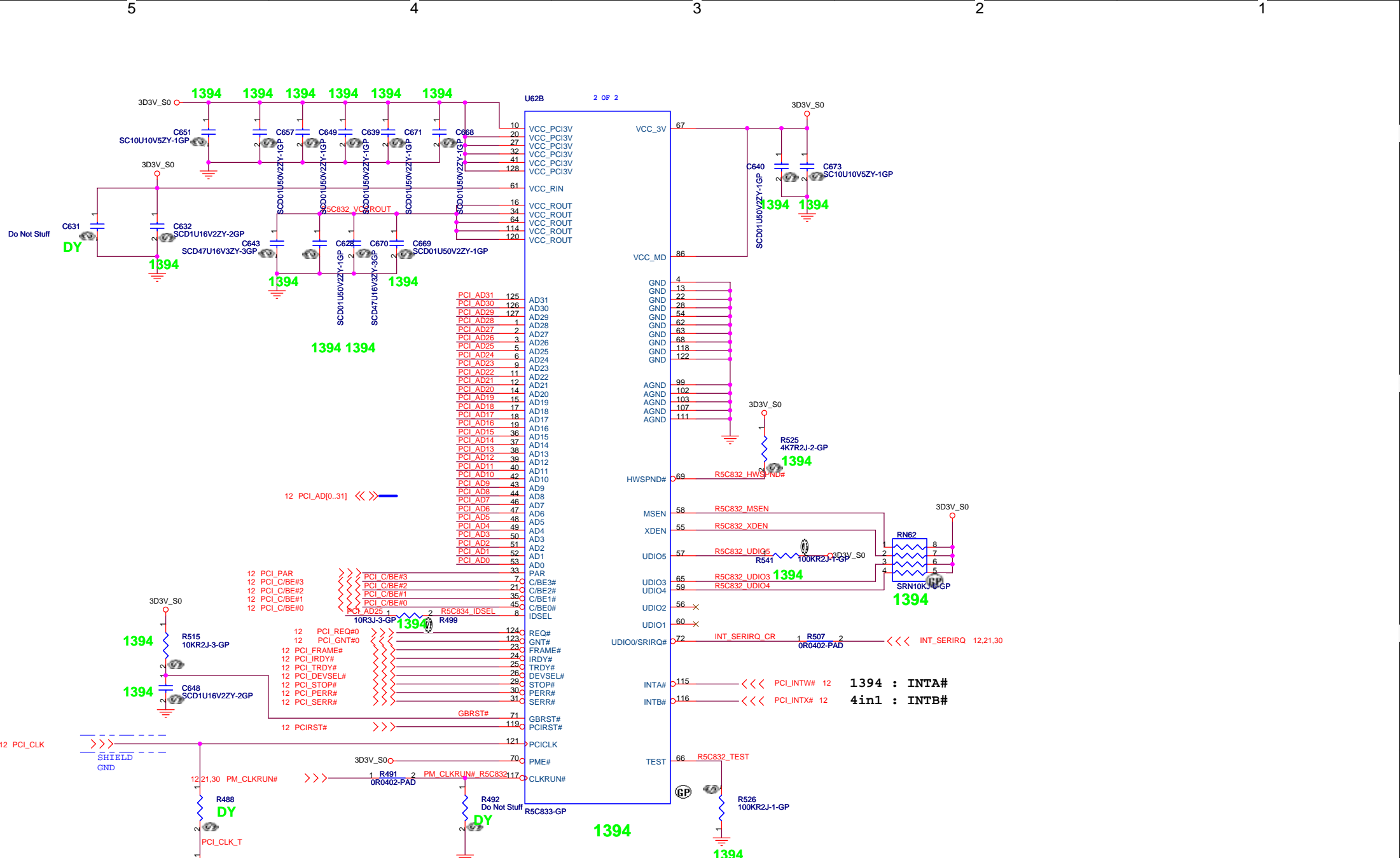


CD-ROM CONNECTOR



USB PORT



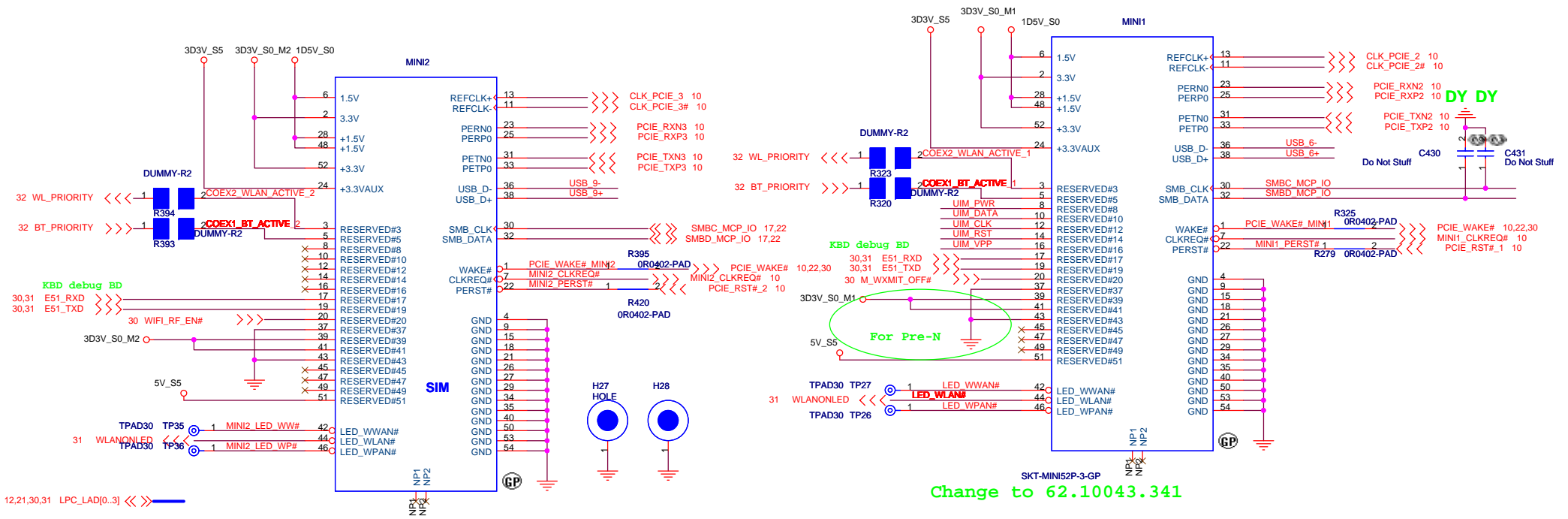


Mini Card Connector 2

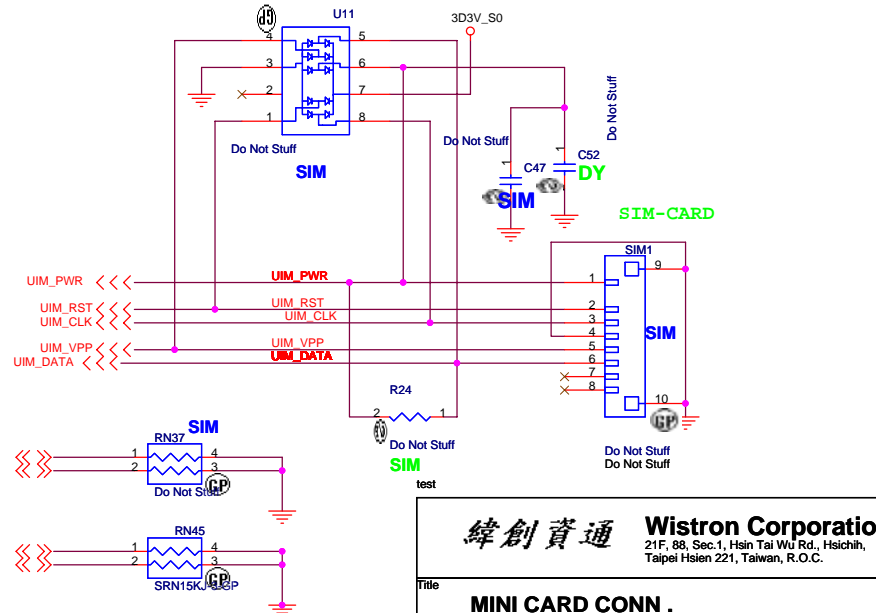
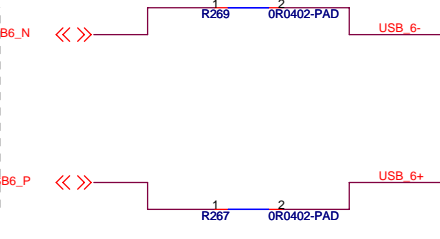
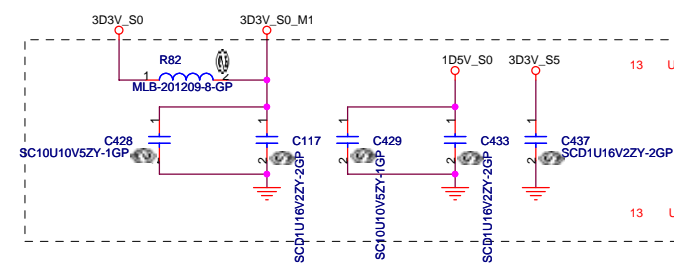
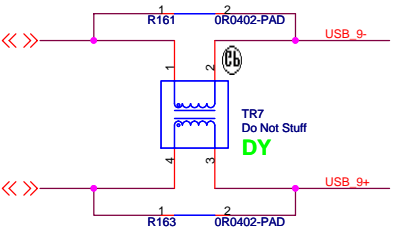
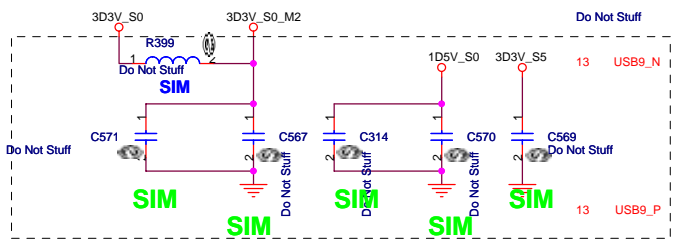
Wireless Card

Mini Card Connector 1

WWAN



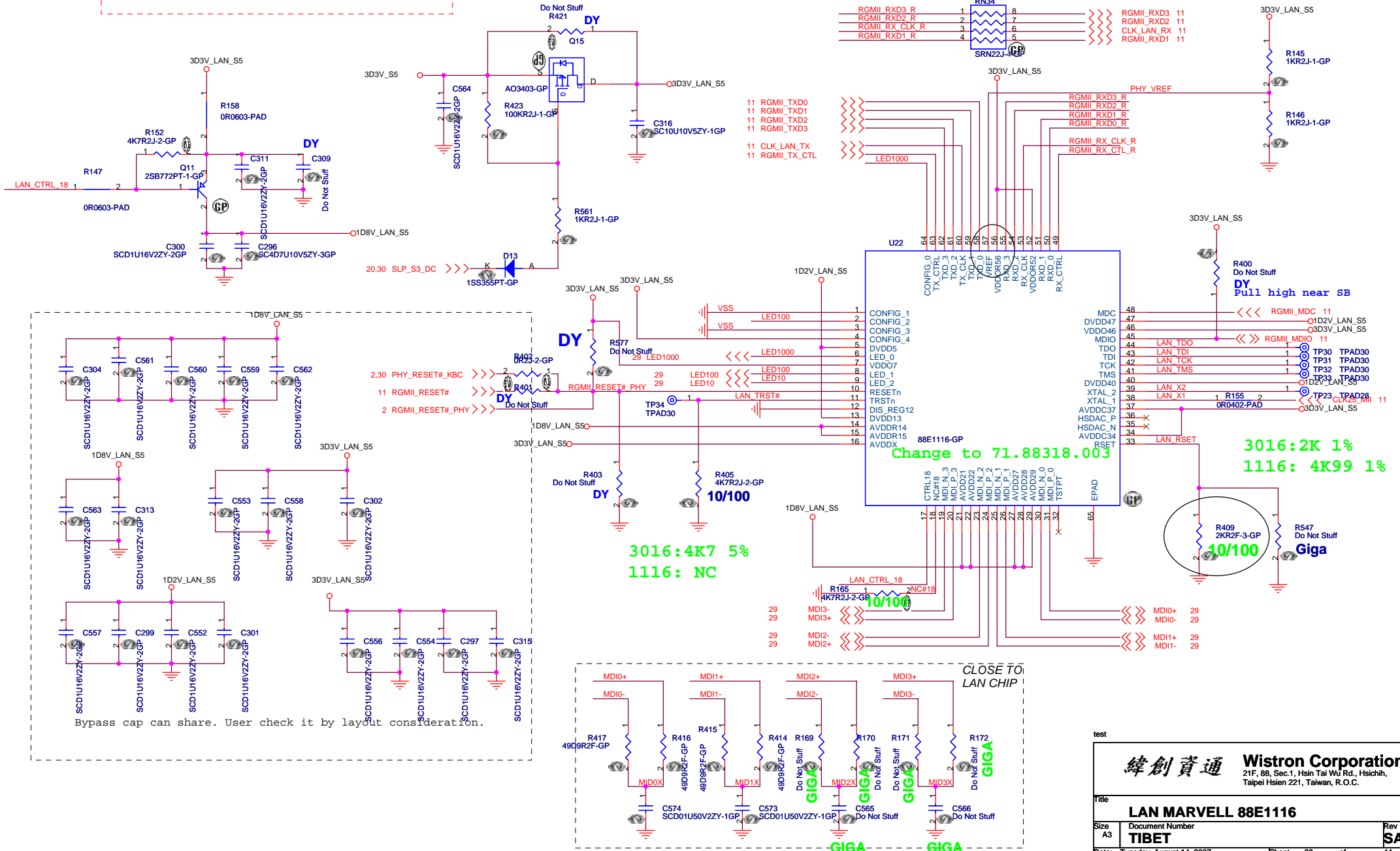
Change to 62.10043.341

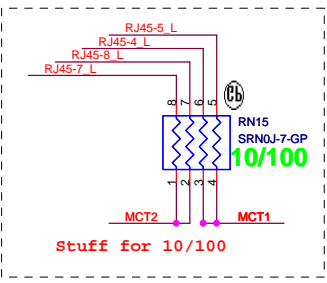
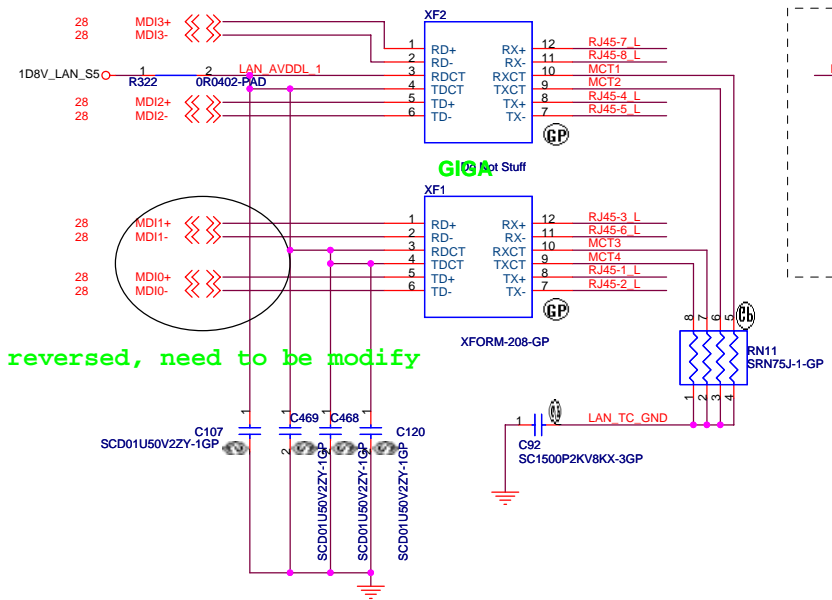


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title MINI CARD CONN.	
Size A3	Document Number TIBET
Date: Tuesday, August 14, 2007	Sheet 27 of 44
Rev SA	

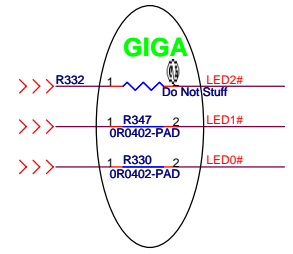
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

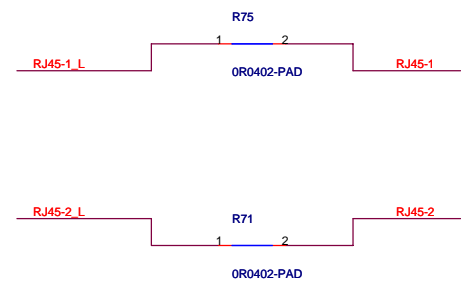
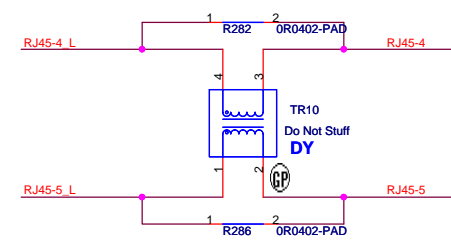
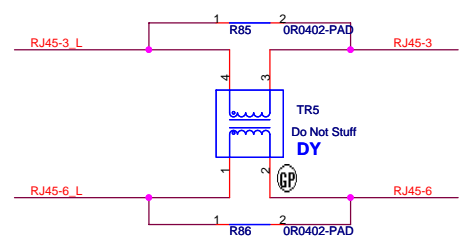
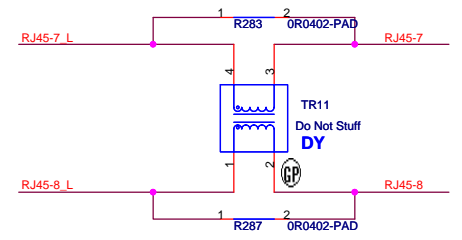
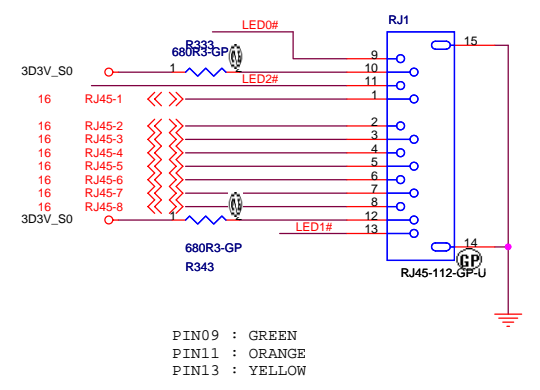




1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



GREEN: LINK 10/100 Mbps
YELLOW: TX/RX ACTIVITY
ORANGE: LINK 1000Mbps



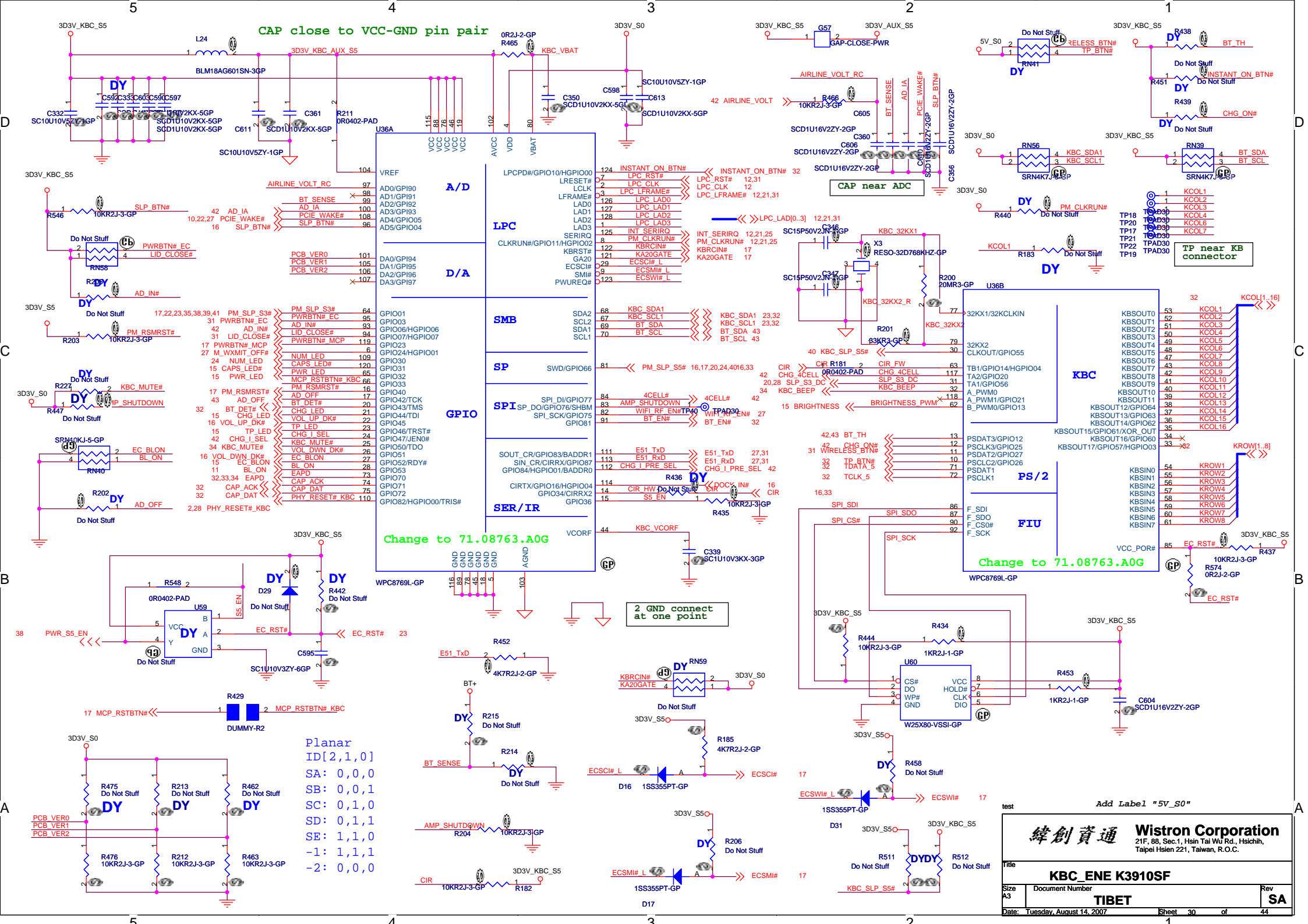
test

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size: A3 Document Number: TIBET Rev: SA

Date: Tuesday, August 14, 2007 Sheet: 29 of 44



Change to 71.08763.A0G

Change to 71.08763.A0G

2 GND connect at one point

Planar
ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,1,0
-1: 1,1,1
-2: 0,0,0

test Add Label "5V_S0"

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC_ENE K3910SF**
Size A3 Document Number: **TIBET** Rev: **SA**

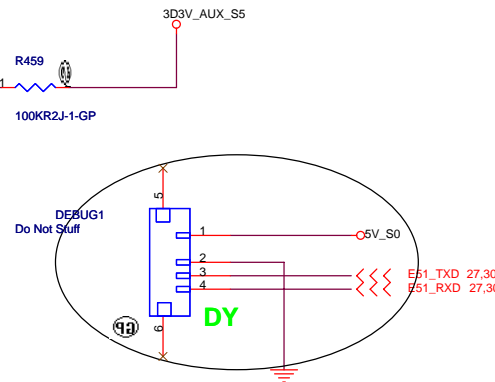
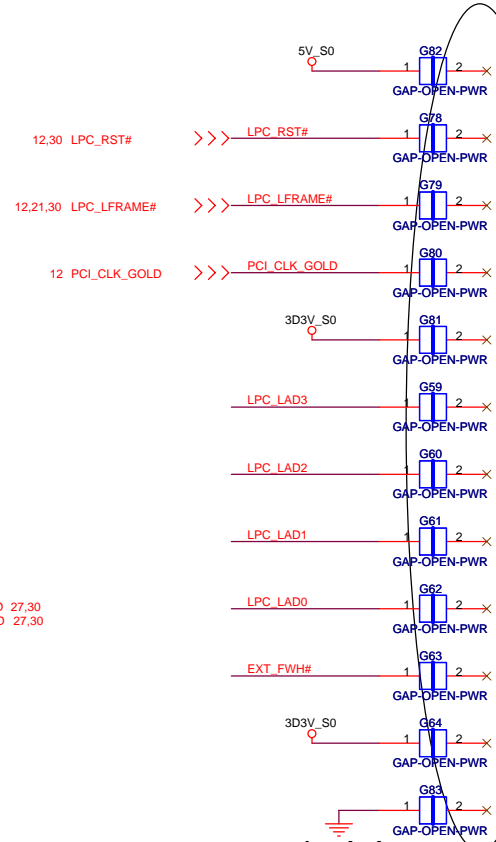
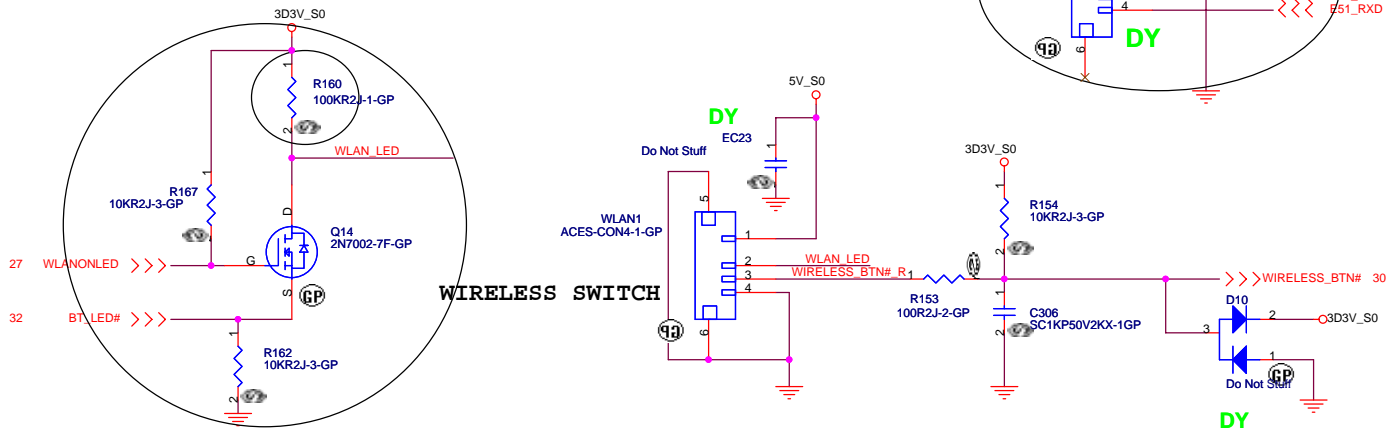
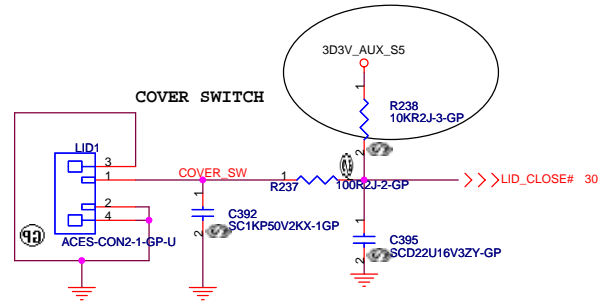
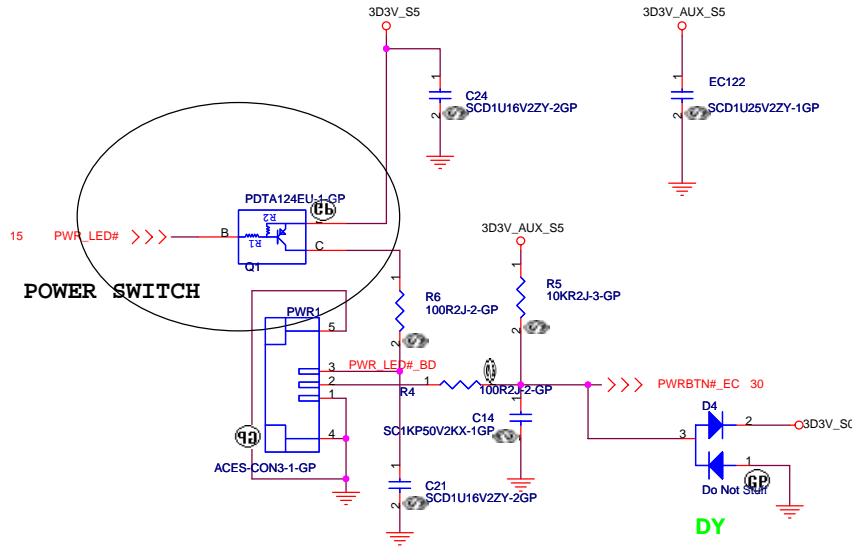
Date: Tuesday, August 14, 2007 Sheet 30 of 44

GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15 (B1)
A14 (B2)
⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)



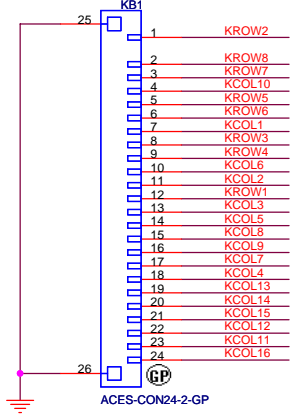
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	FLASH and Debug	
Size A3	Document Number	Rev SA
Date: Tuesday, August 14, 2007	Sheet 31 of 44	

Internal Keyboard Connector

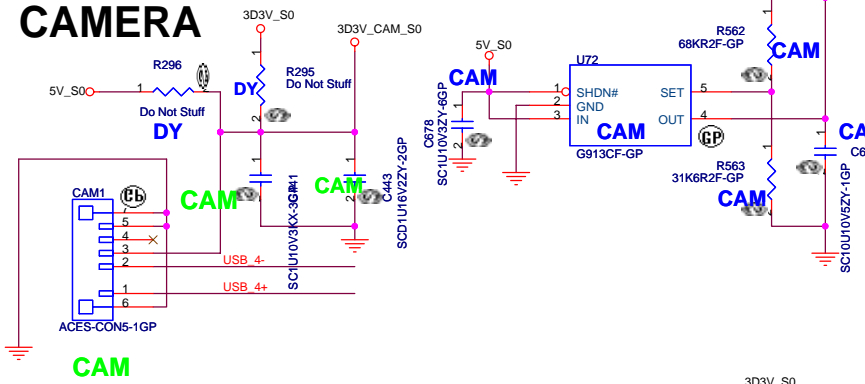
30 KROW[1..8] <<< <<< <<< <<<
 30 KCOL[1..16] <<< <<< <<< <<<

Keyboard matrix (from vendor)

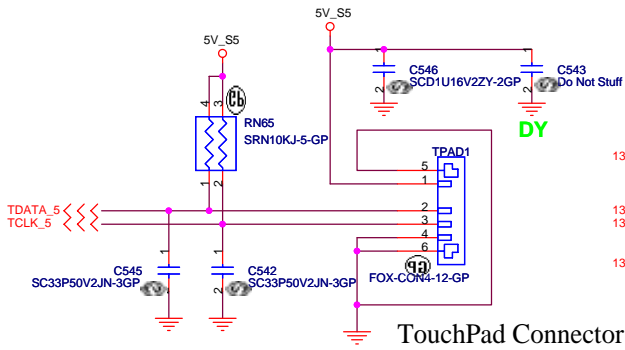
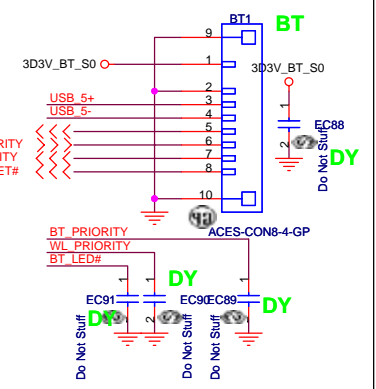
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



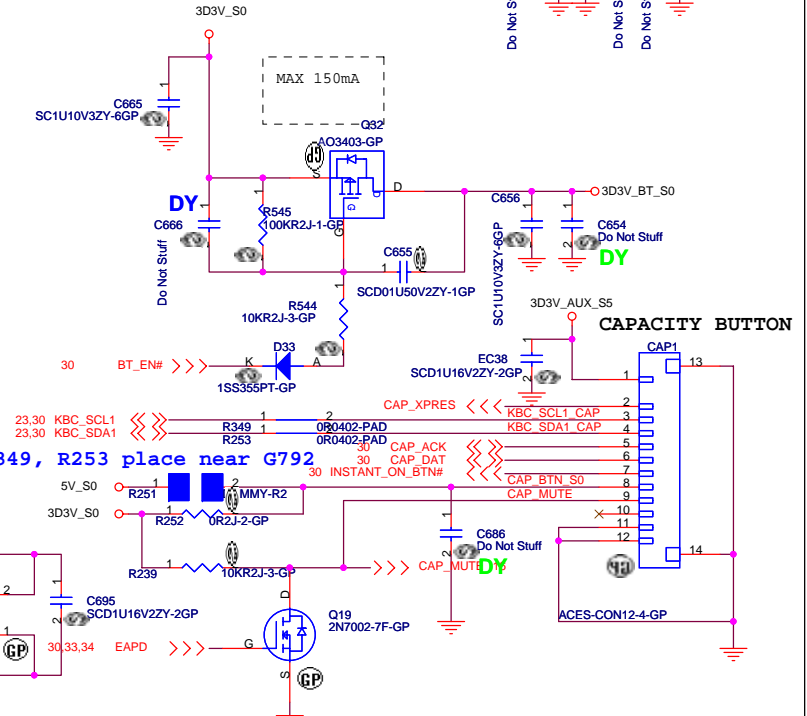
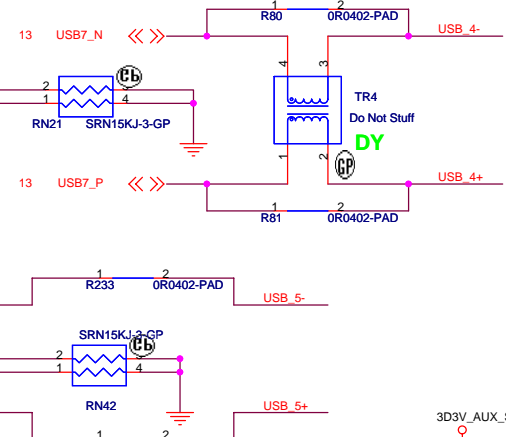
CAMERA



BT



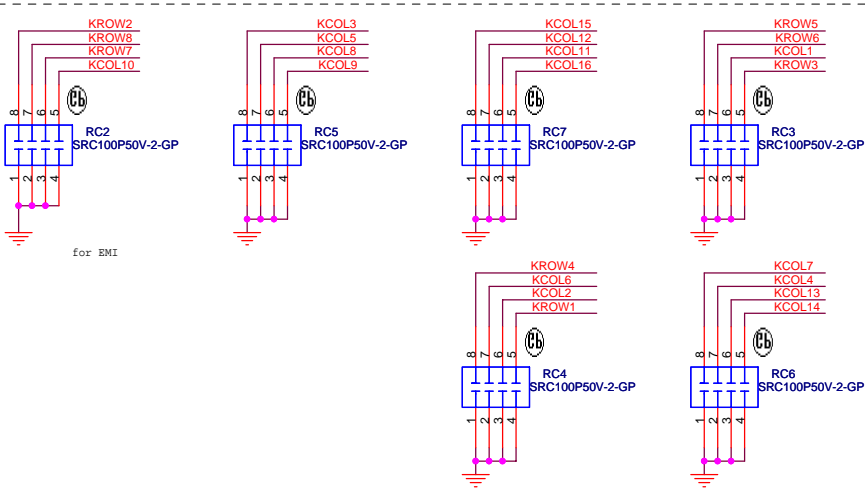
TouchPad Connector



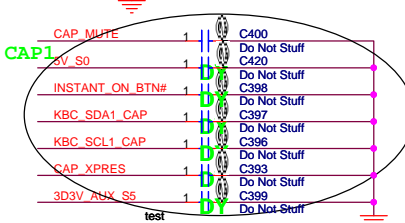
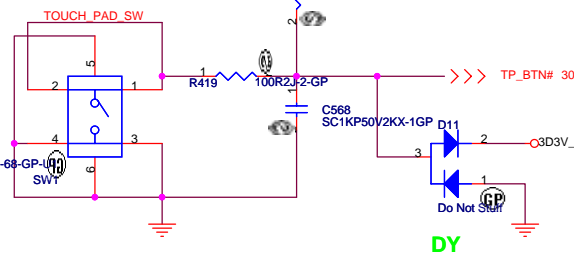
CAPACITY BUTTON

R349, R253 place near G792

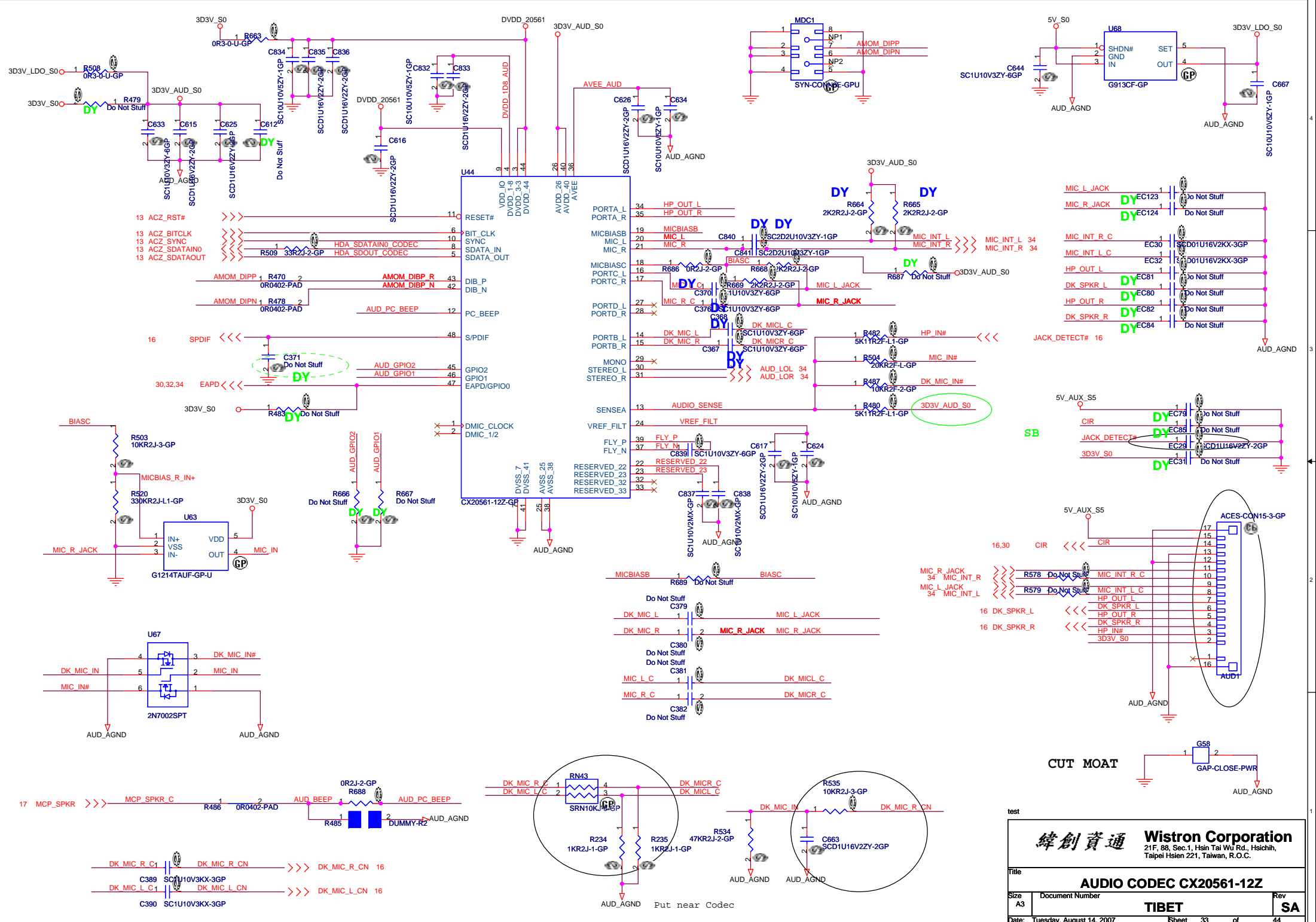
PLACE NEAR CAP1



TOUCH-PAD SWITCH



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KeyBoard-CONN	
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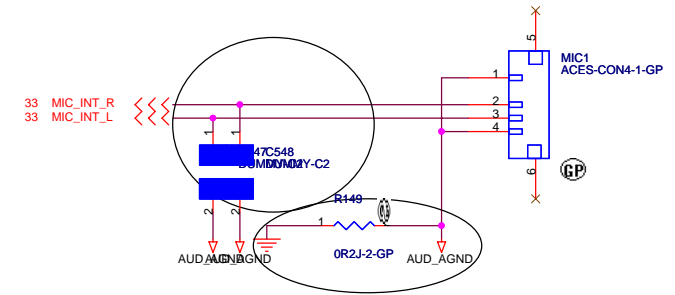
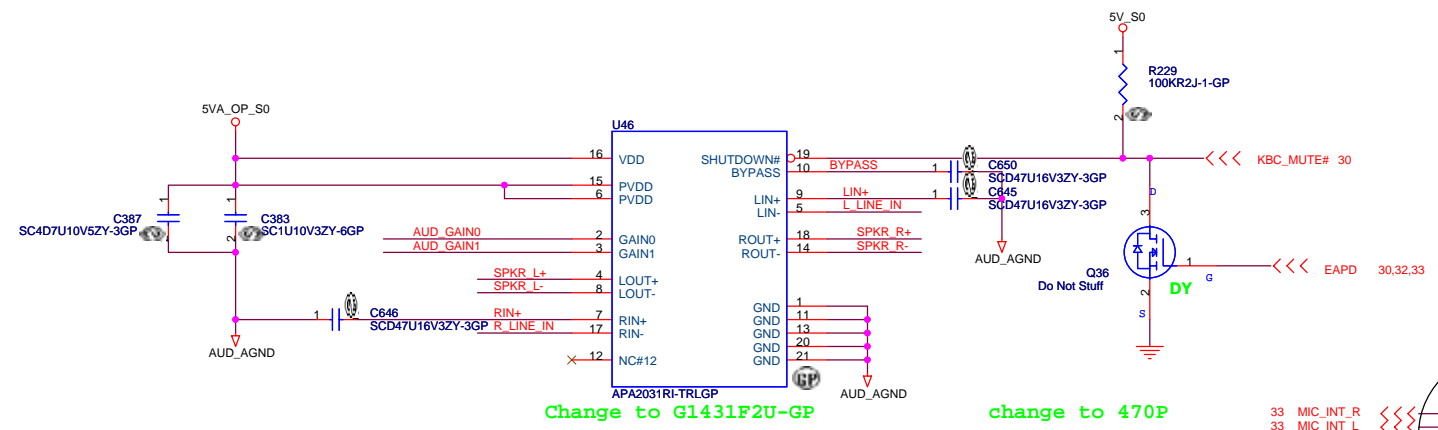
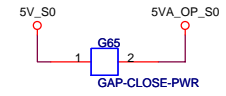
test

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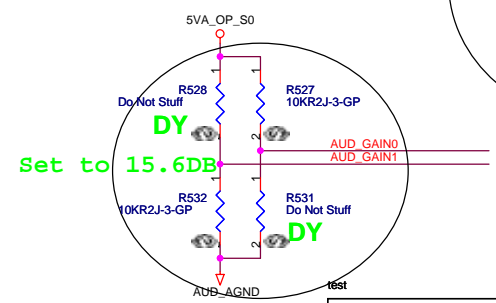
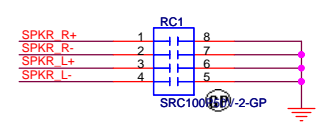
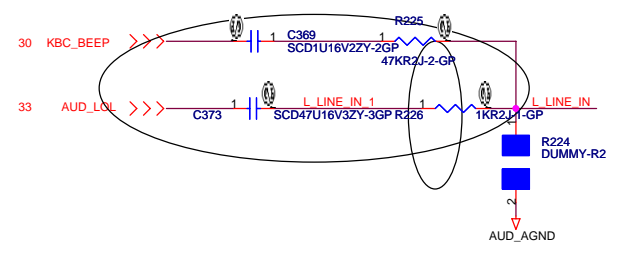
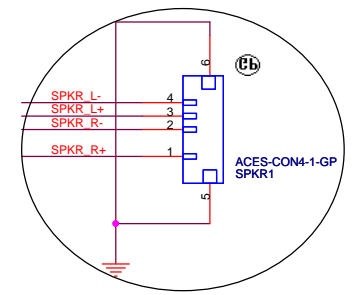
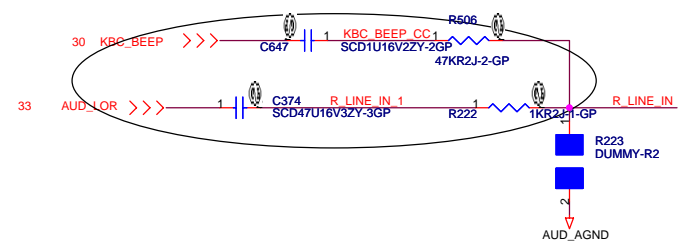
Title: **AUDIO CODEC CX20561-12Z**

Size: A3	Document Number: TIBET	Rev: SA
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Speaker



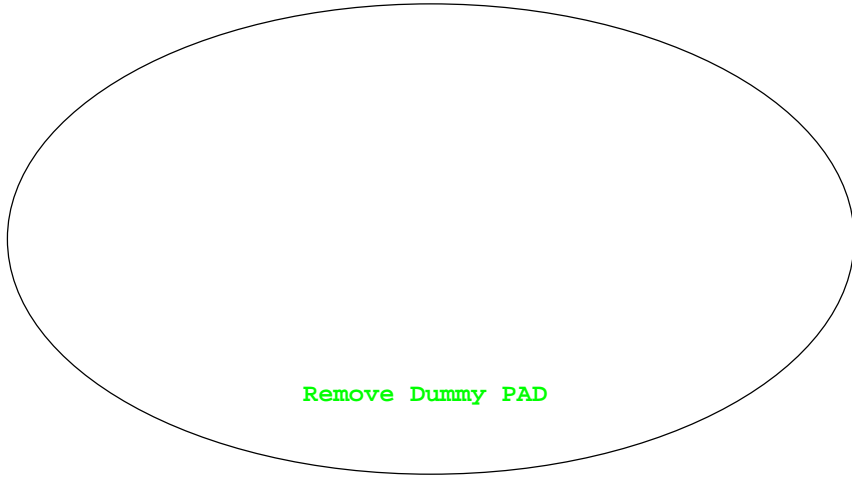
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP APA3031**

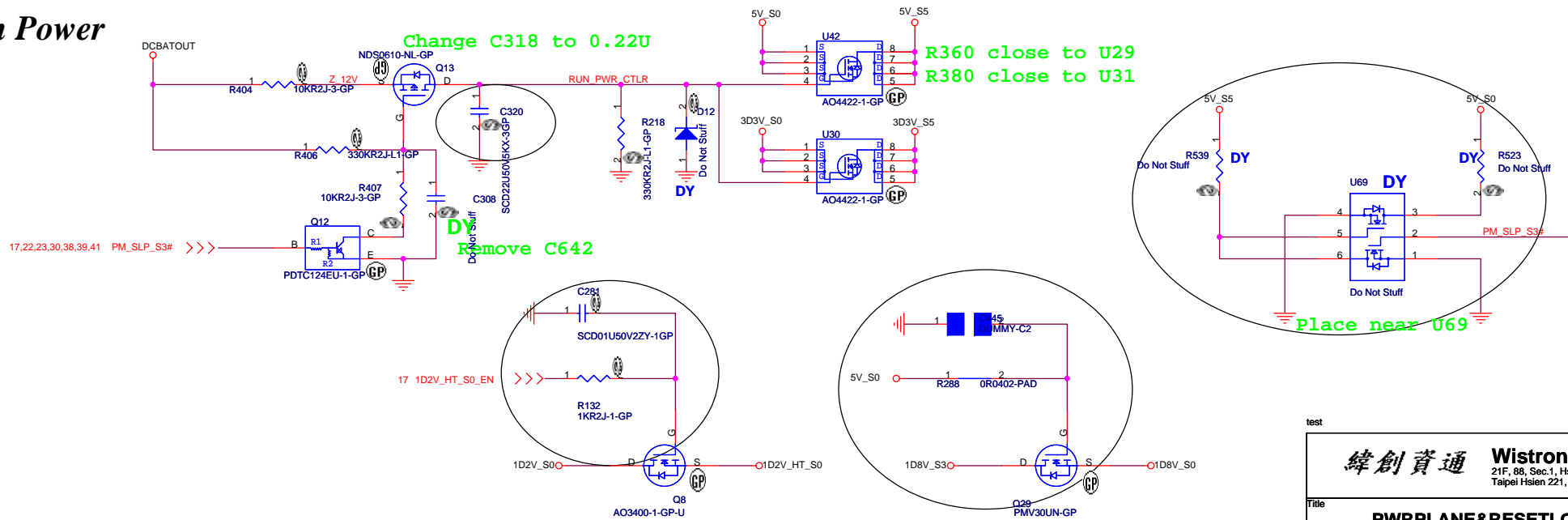
Size: A3 Document Number: **TIBET** Rev: **SA**

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Suspend Power



Run Power

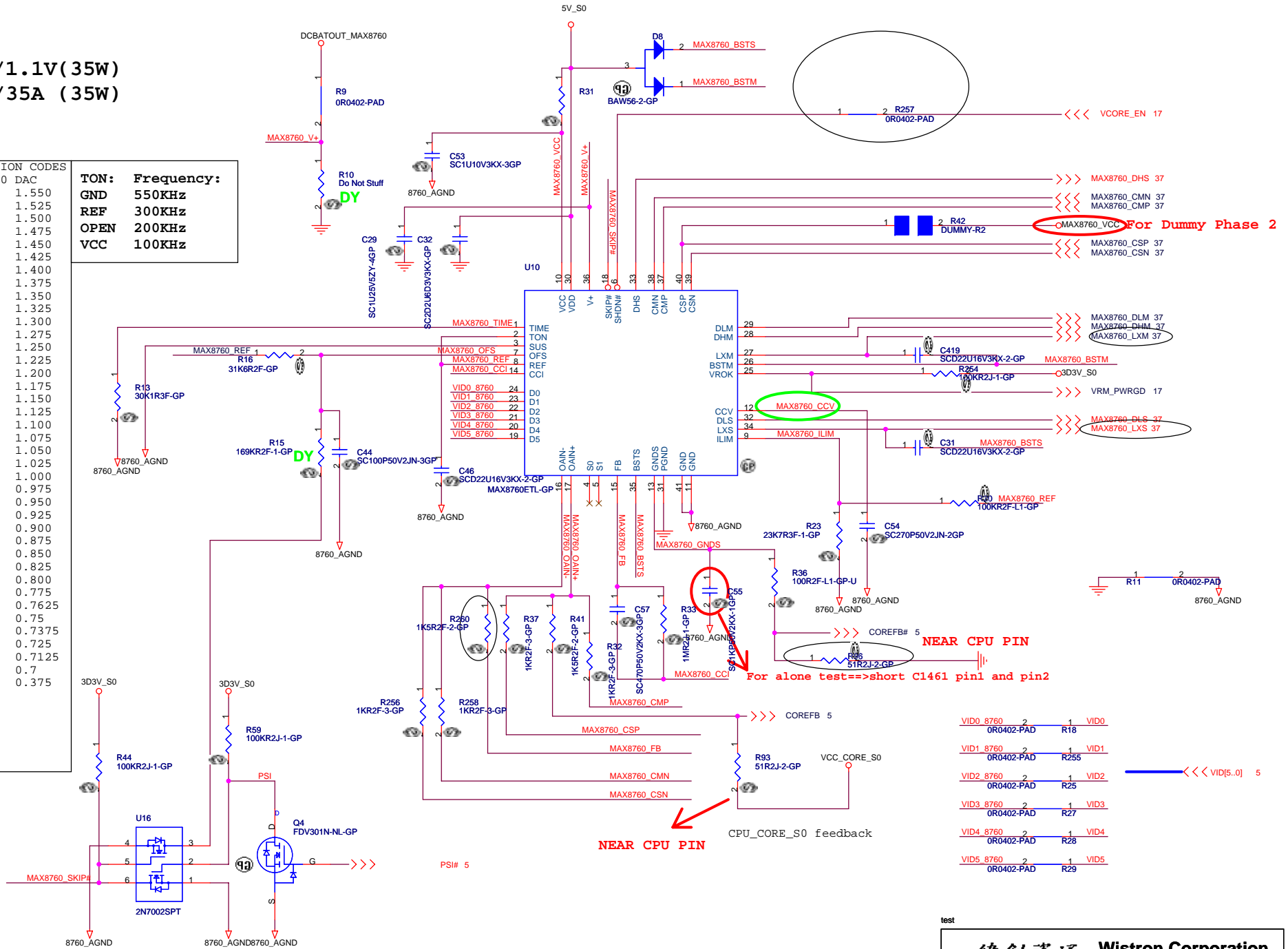


CPU_VCORE
VID=1.15V(25W)/1.1V(35W)
I_{omax}=25A(25W)/35A(35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz

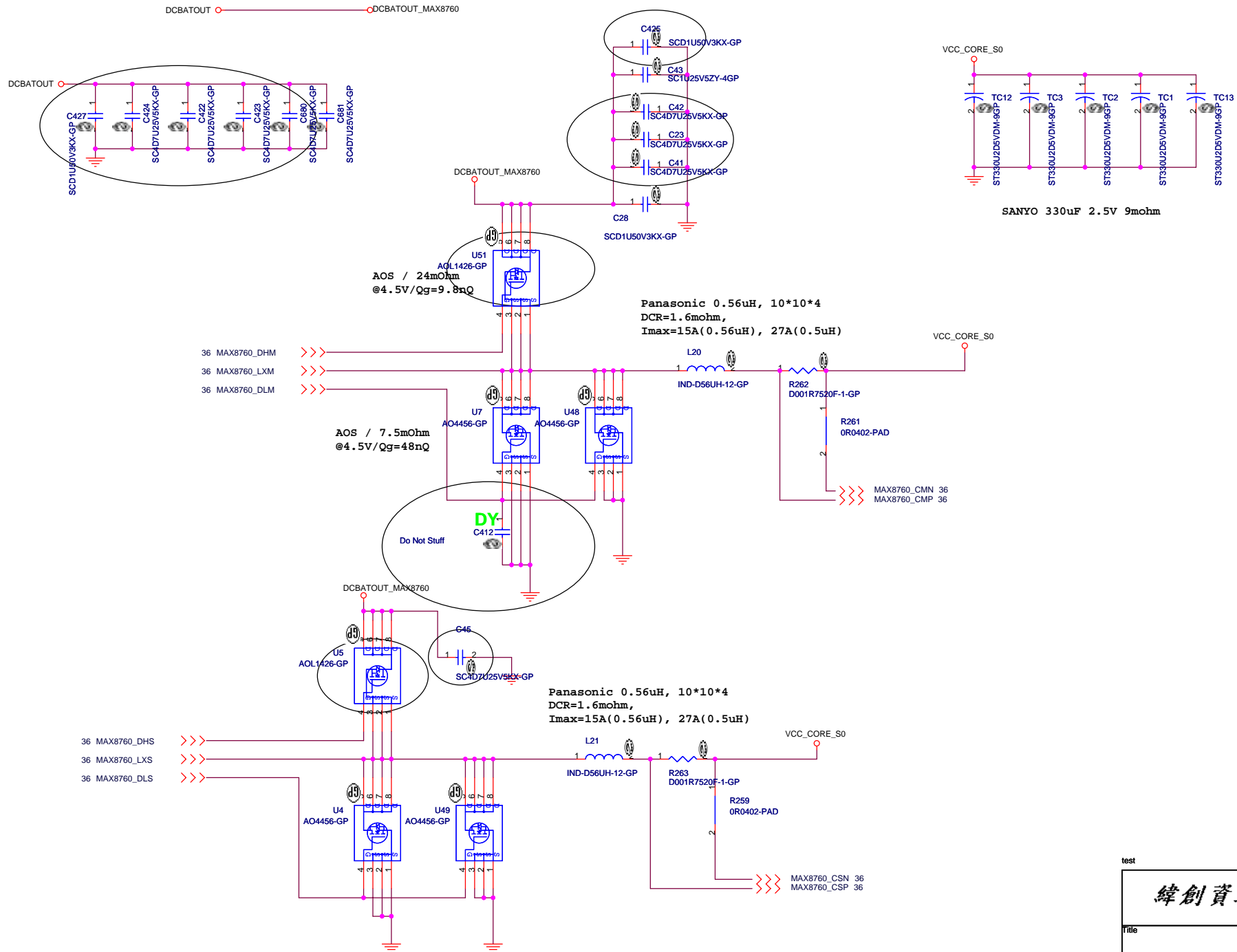


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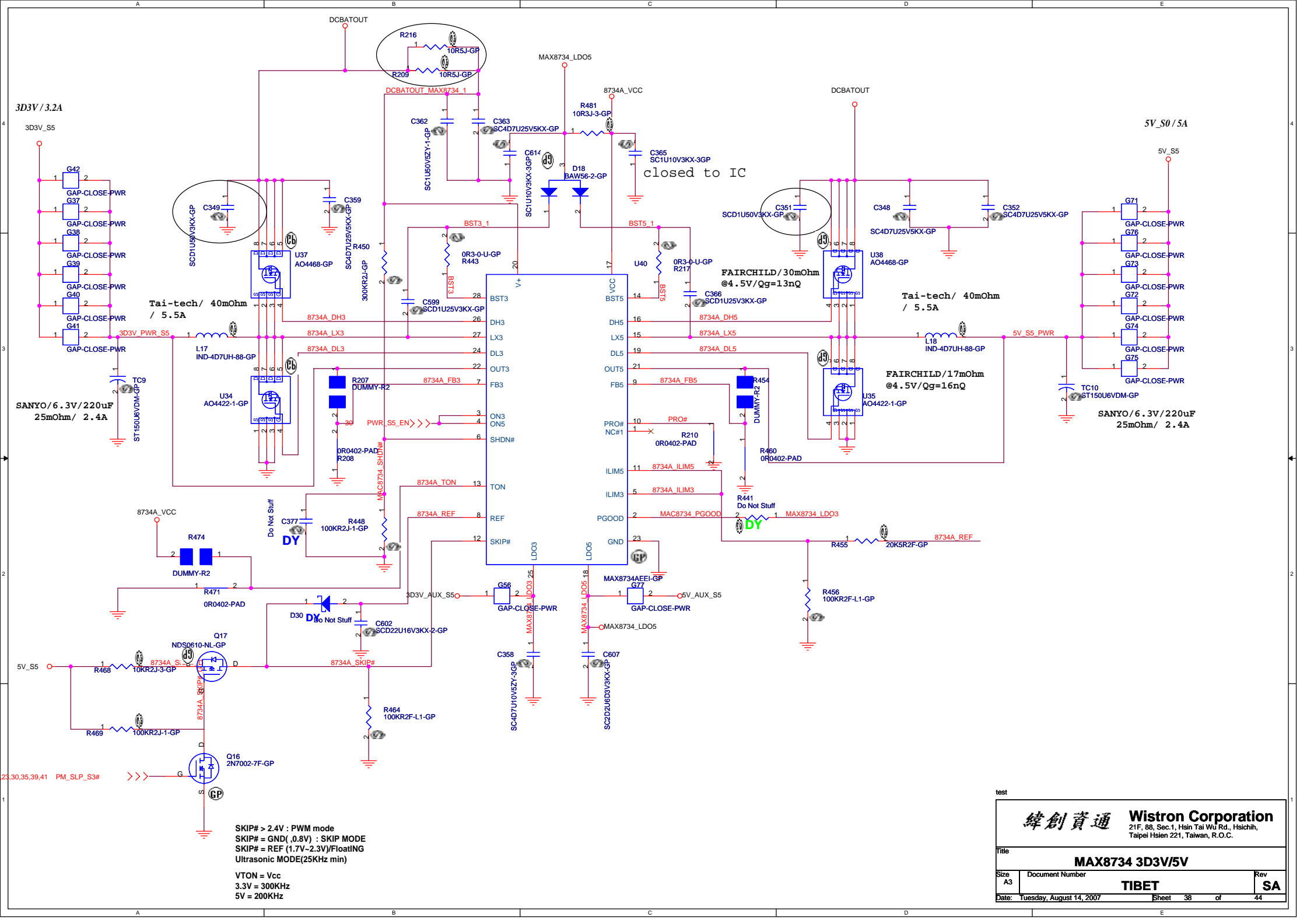
Title: **CPU CORE MAX8760(1/2)**

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(Power Team)

test	
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CPU CORE MAX8760(2/2)	
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3D3V / 3.2A

5V_S0 / 5A

SANYO / 6.3V / 220uF
25mOhm / 2.4A

SANYO / 6.3V / 220uF
25mOhm / 2.4A

23,30,35,39,41 PM_SLP_S3#

SKIP# > 2.4V : PWM mode
 SKIP# = GND(,0.8V) : SKIP MODE
 SKIP# = REF (1.7V~2.3V)/FloatNG
 Ultrasonic MODE(25KHz min)
 VTON = Vcc
 3.3V = 300KHz
 5V = 200KHz

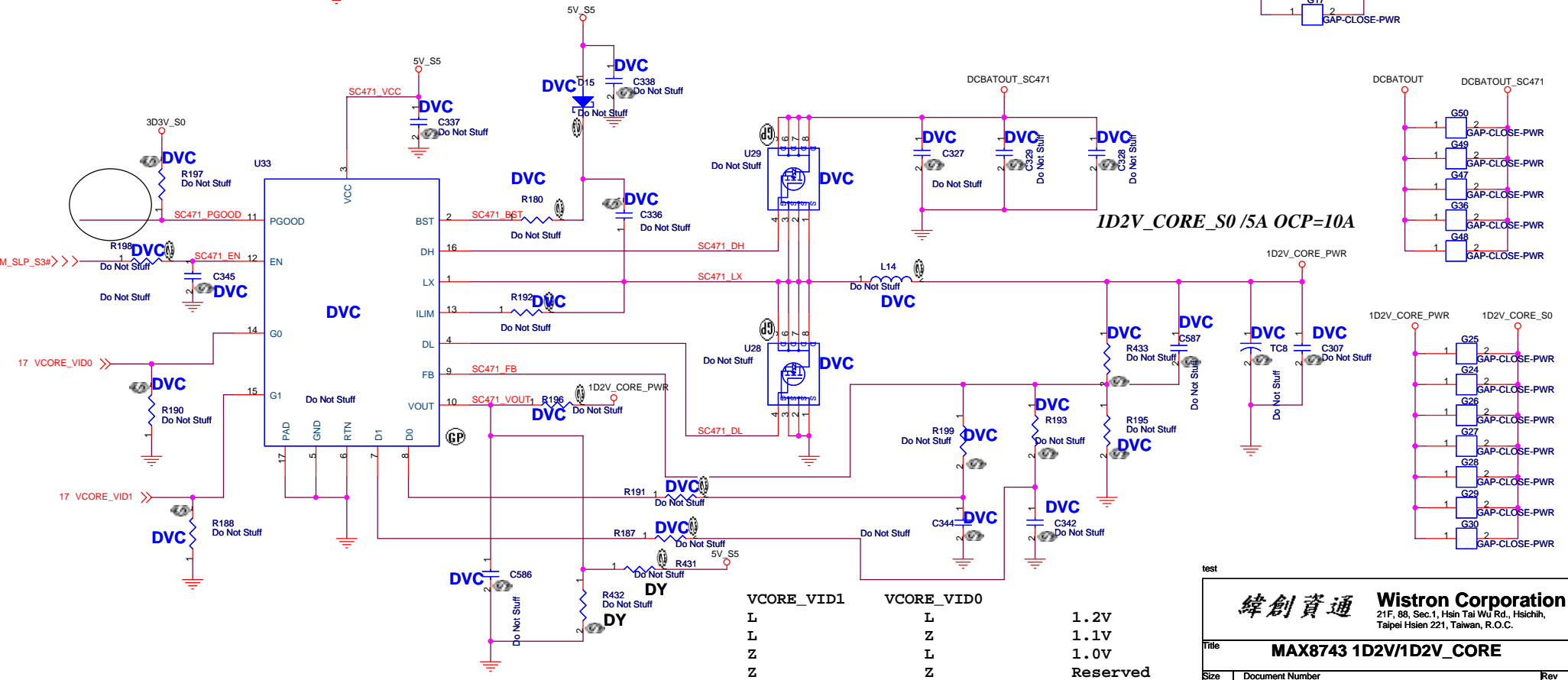
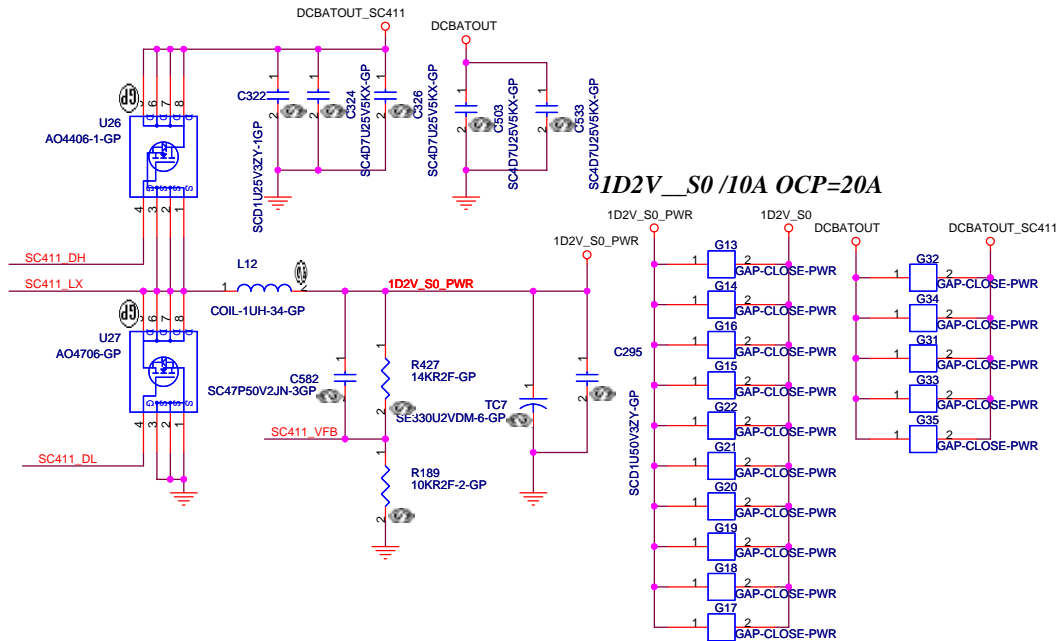
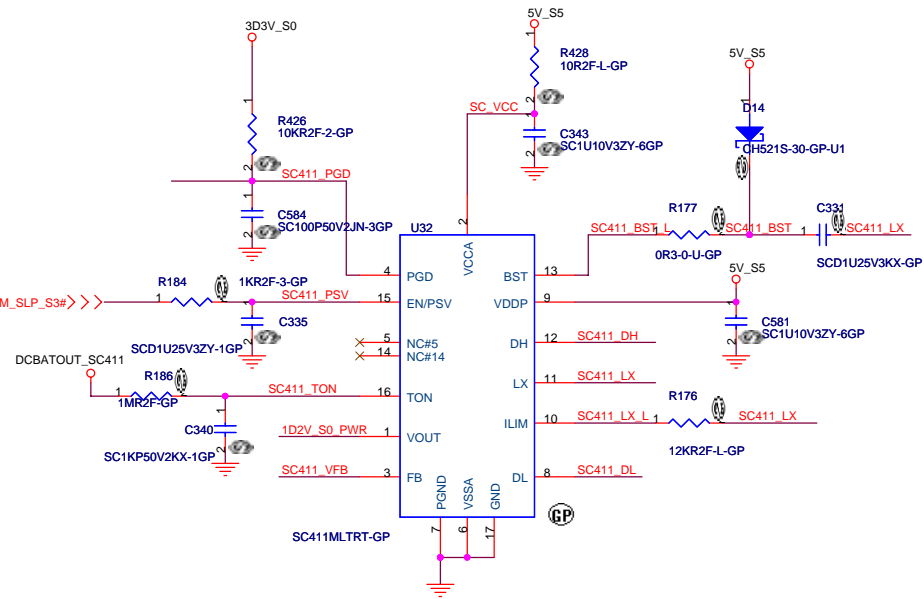
closed to IC

test

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8734 3D3V/5V**

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test

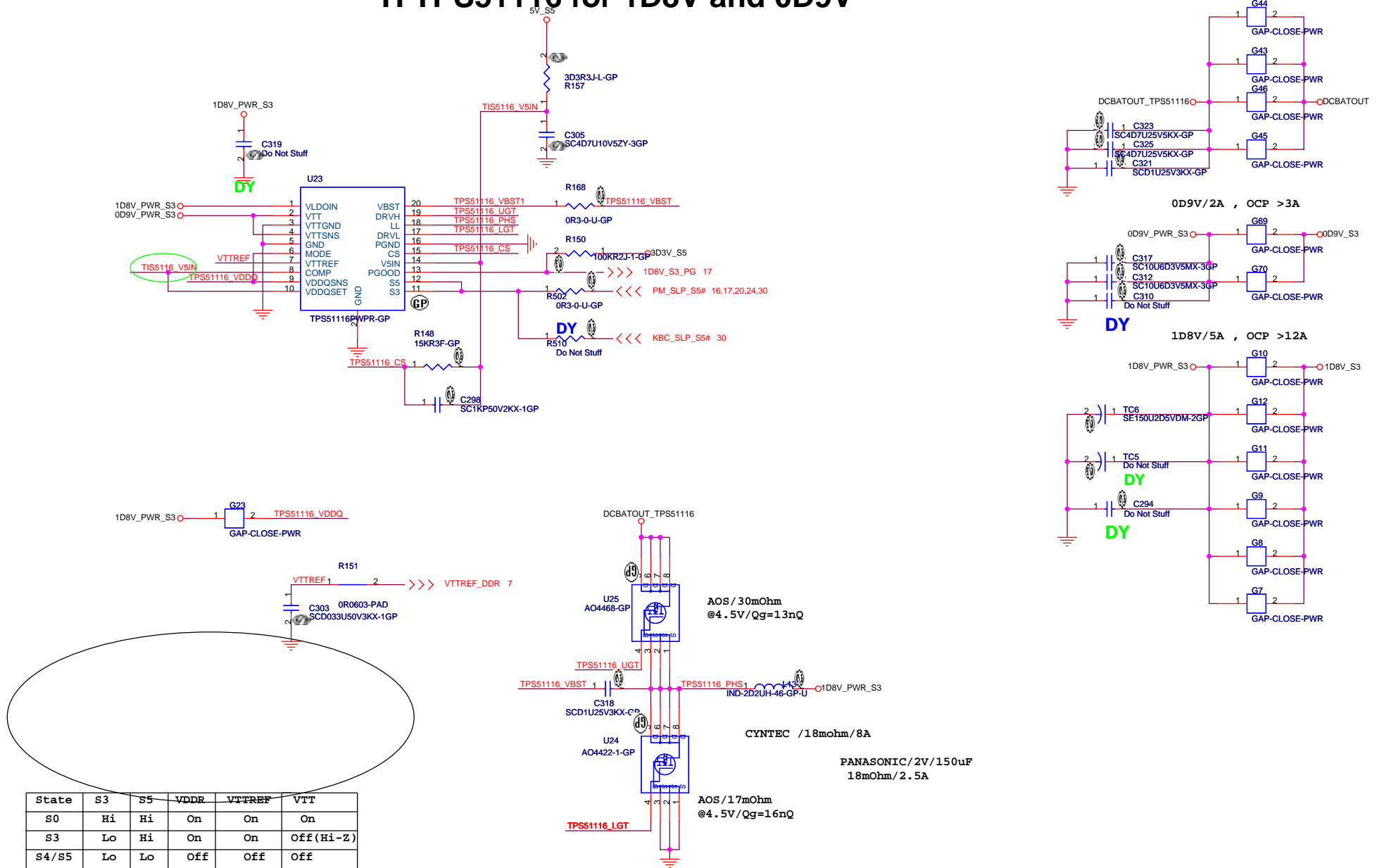
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8743 1D2V/1D2V_CORE**

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VCORE_VID1	VCORE_VID0	1.2V
L	L	1.1V
Z	Z	1.0V
Z	Z	Reserved

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

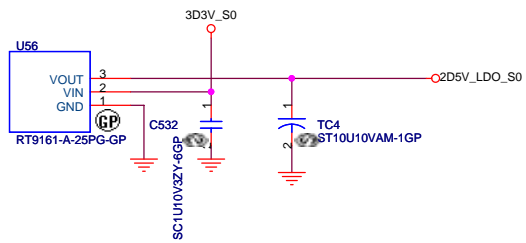
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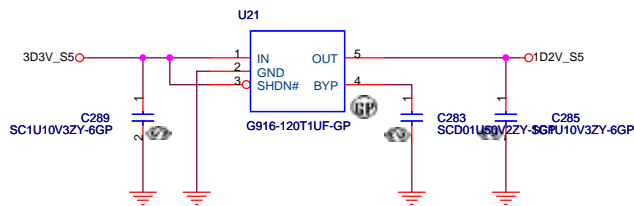
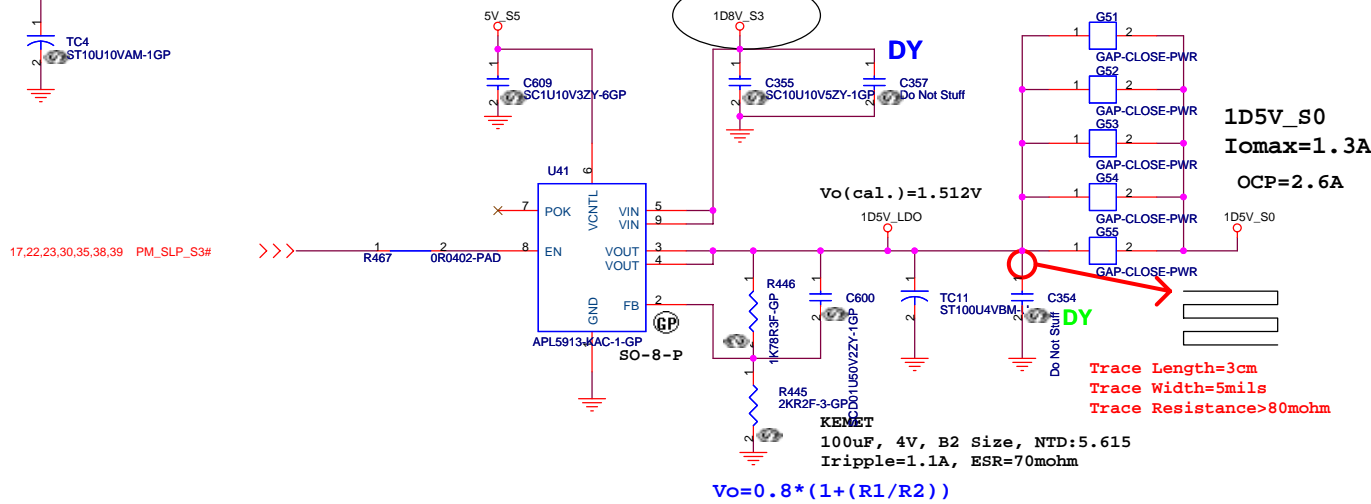
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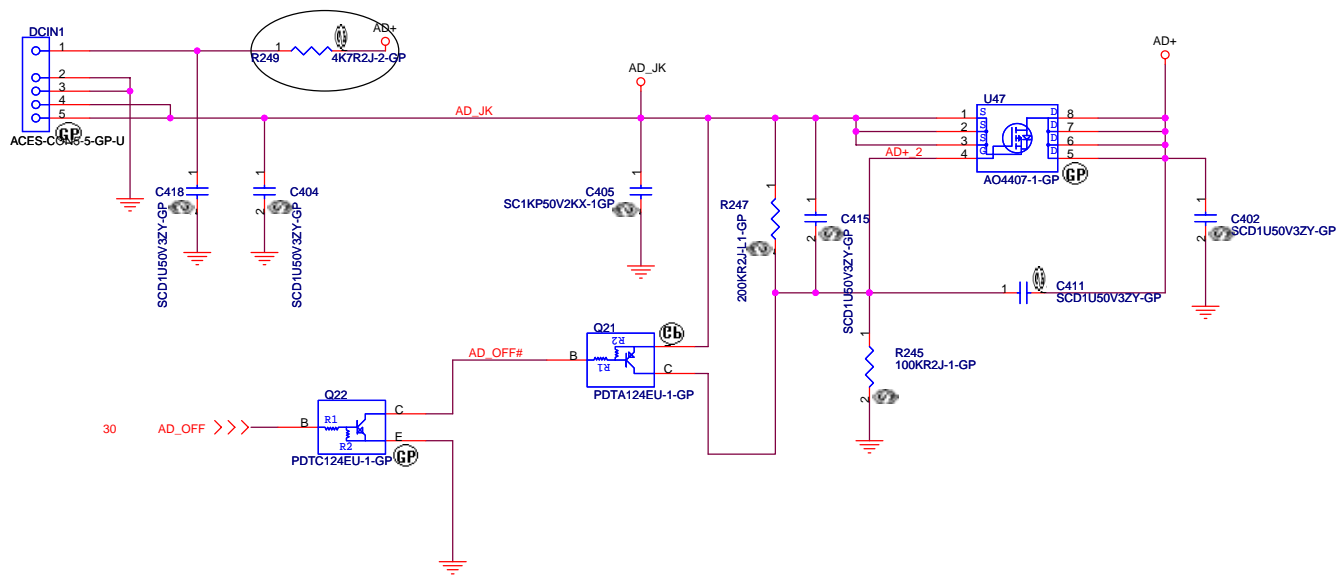


Change 3D3V_S0 to 1D8V_S3

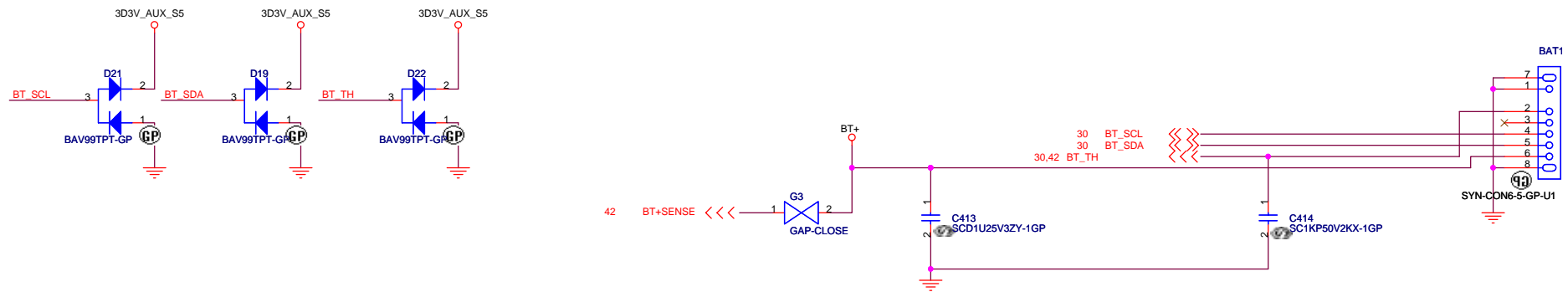


Change G914 to G916

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

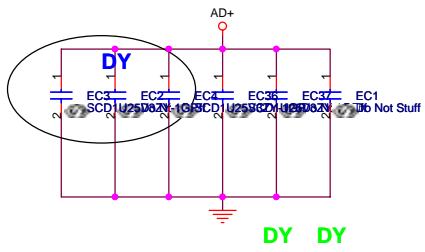


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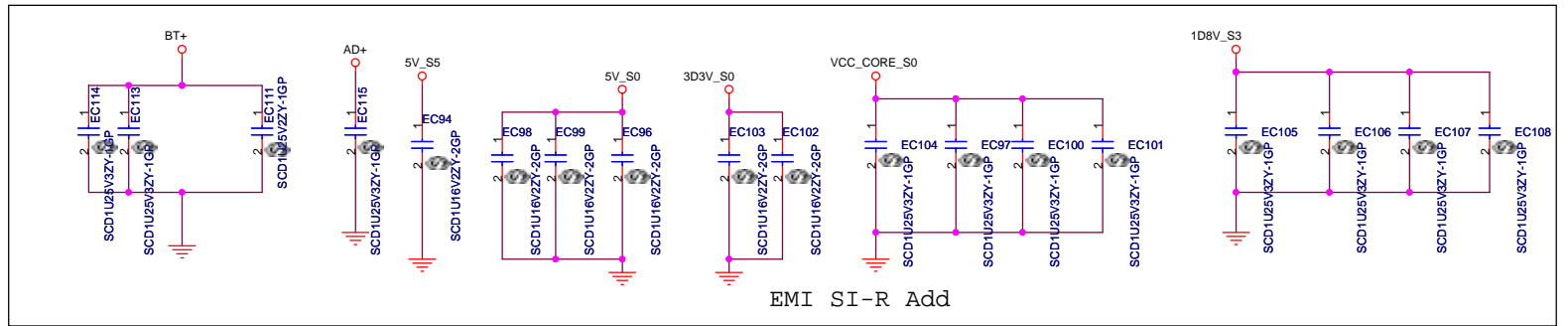
緯創資通 Wistron Corporation
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Title: **AD/BATT CONN**

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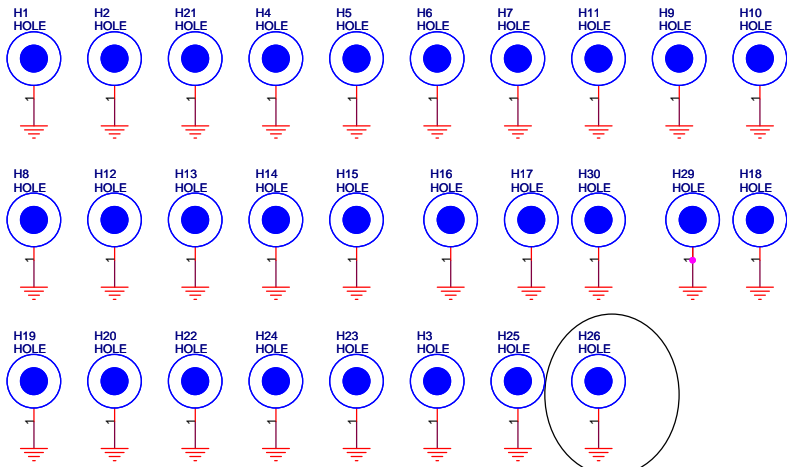
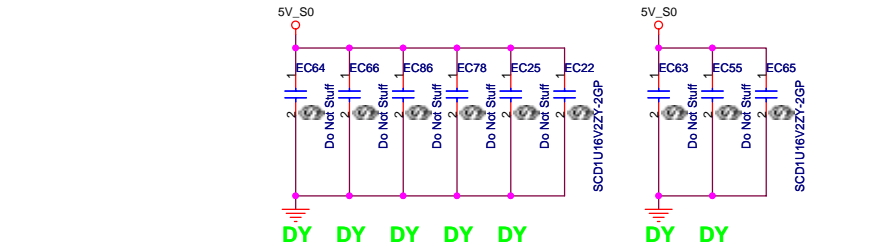
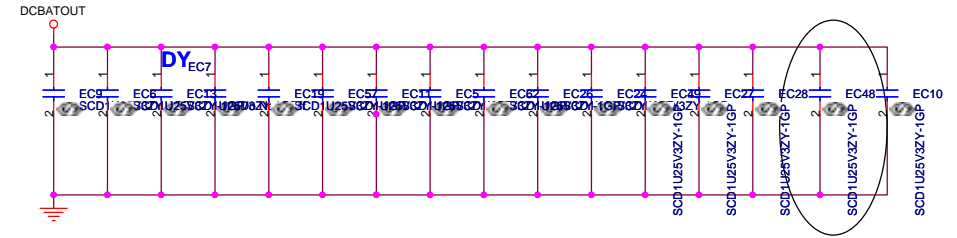
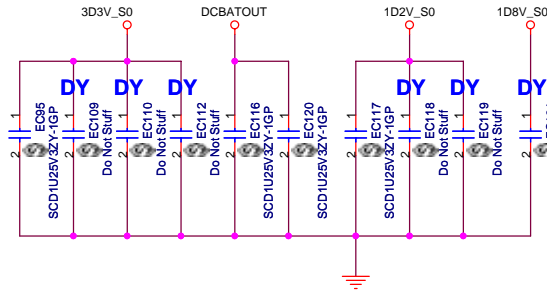


DY DY

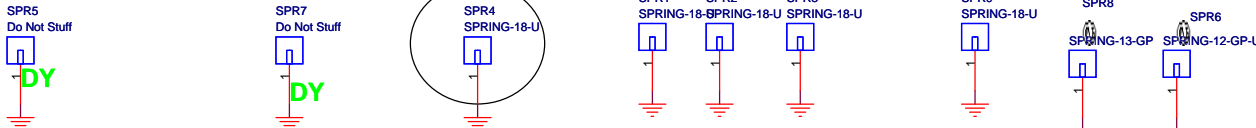


EMI SI-R Add

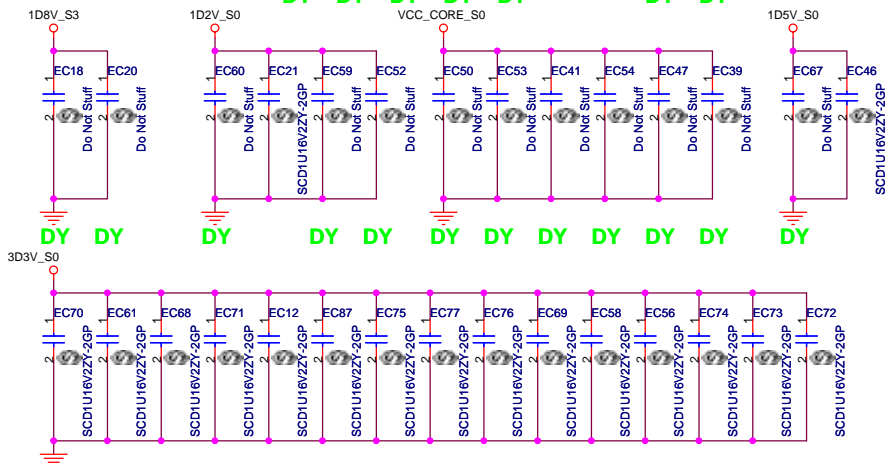
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CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



Modify SPR7 P/N manually



THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GND



test

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size A3 Document Number: **TIBET** Rev: **SA**

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