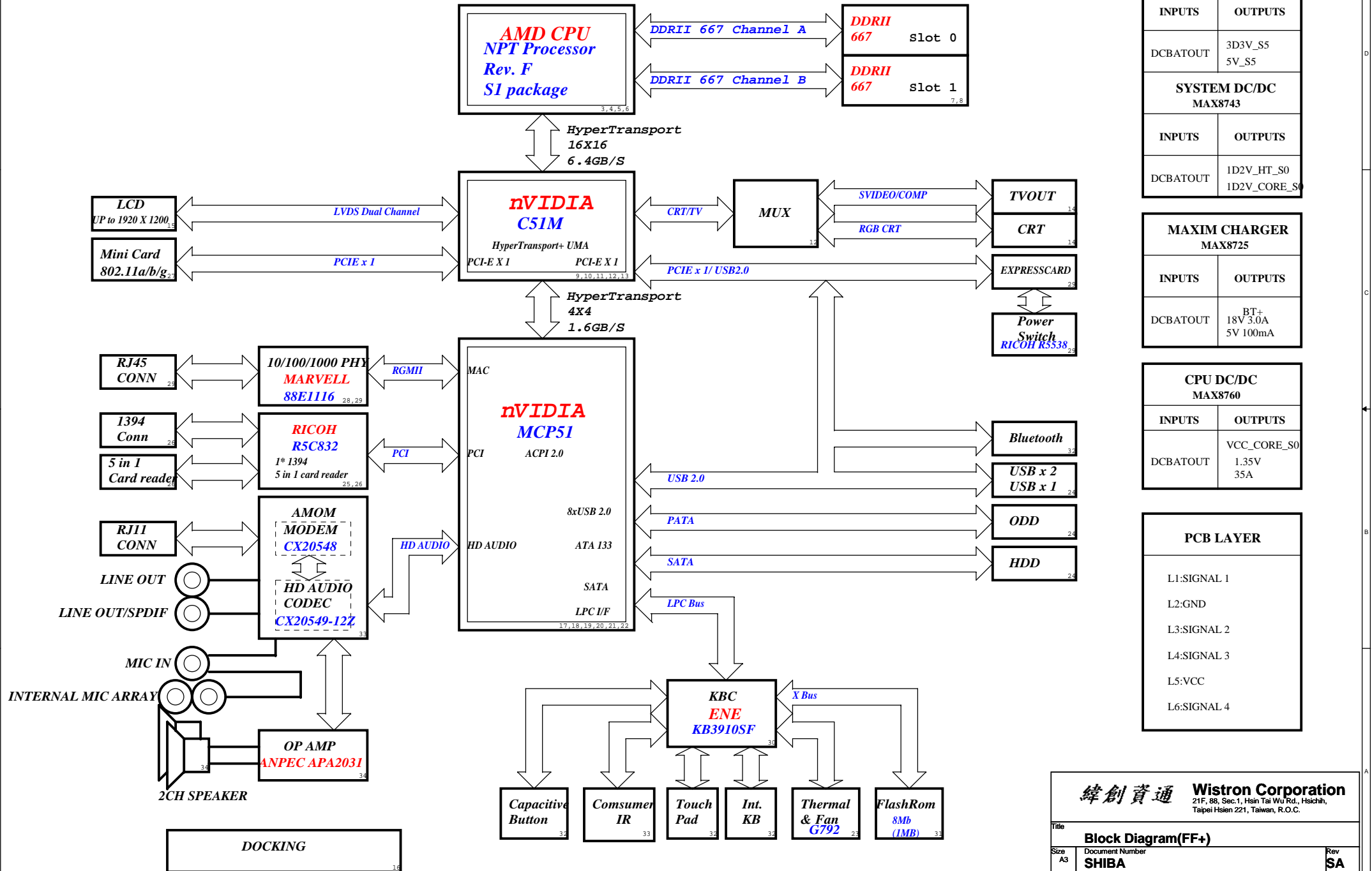


Shiba Block Diagram(FF+)

Project Code: 91.4F701.001
 Project Name: Shiba
 PCB Number: 05234

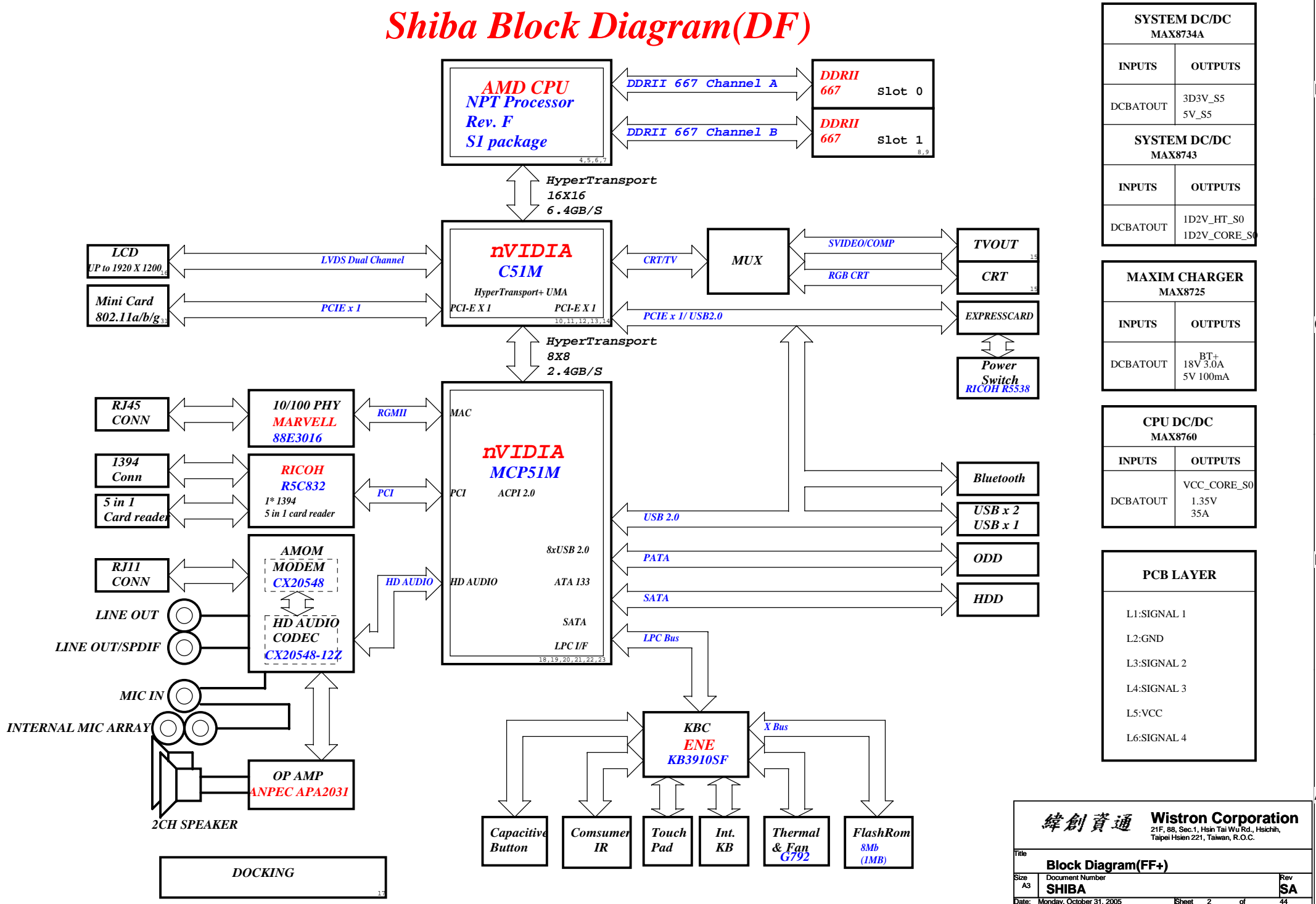


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram(FF+)**

Size: A3	Document Number: SHIBA	Rev: SA
Date: Friday, November 11, 2005	Sheet: 1 of 44	

Shiba Block Diagram(DF)



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

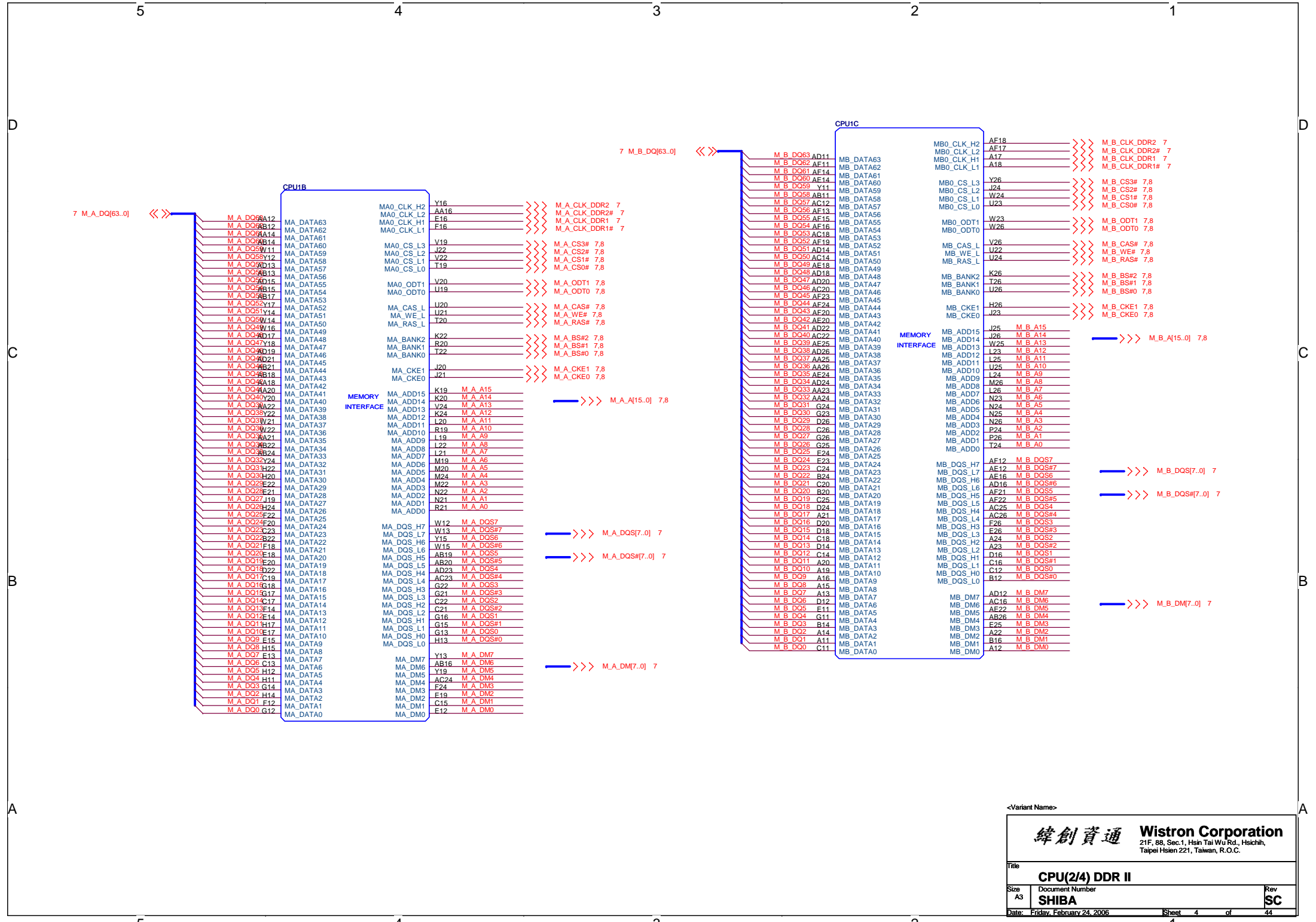
MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER	
L1: SIGNAL 1	
L2: GND	
L3: SIGNAL 2	
L4: SIGNAL 3	
L5: VCC	
L6: SIGNAL 4	

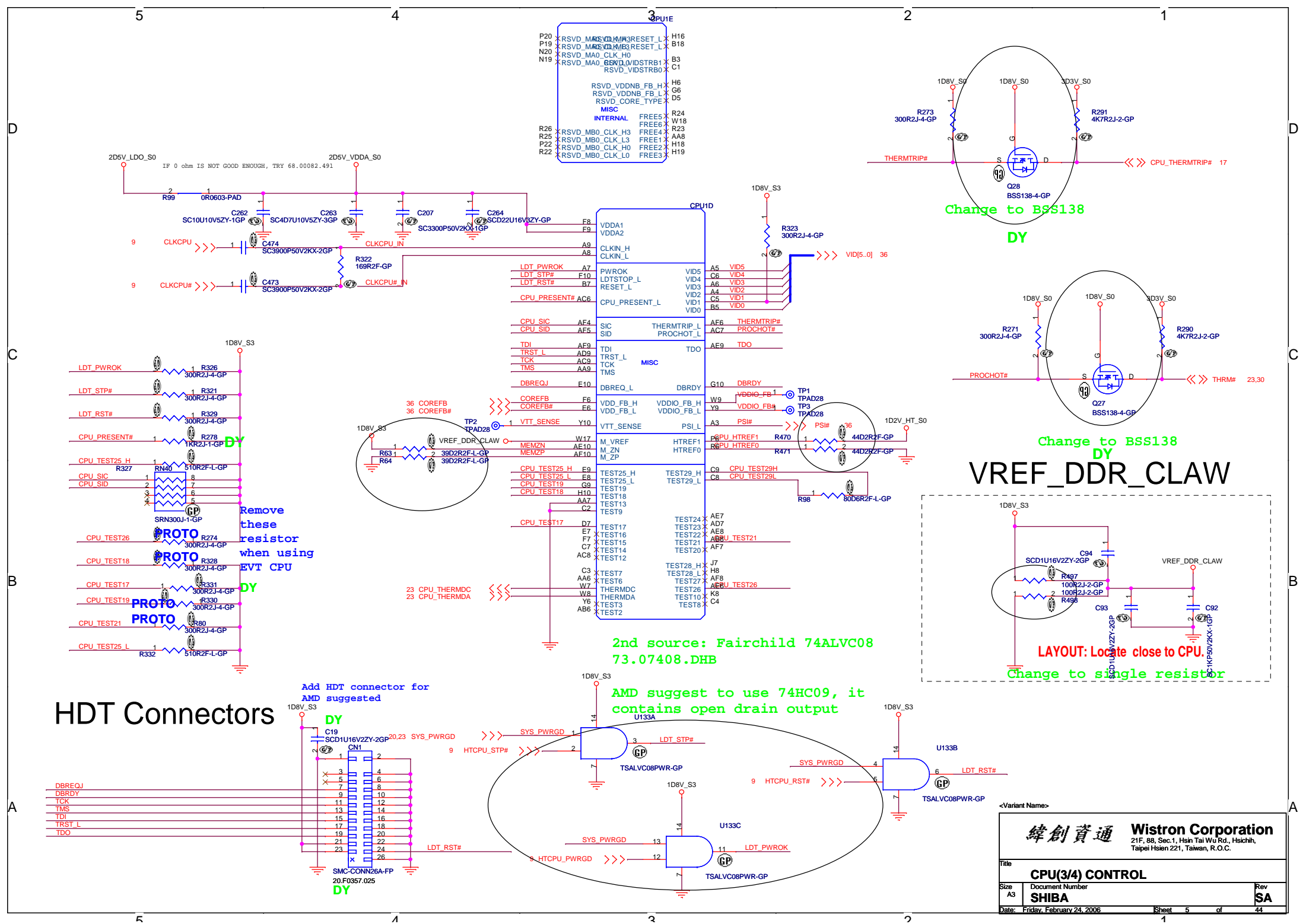
緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Block Diagram(FF+)		
Size: A3	Document Number: SHIBA	Rev: SA
Date: Monday, October 31, 2005	Sheet: 2 of 44	1





<Variant Name>

緯創資通			Wistron Corporation		
			21F, 88, Sec. 1, Hsin Tai Wu Rd., Hschih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU(2/4) DDR II					
Size	Document Number				Rev
A3	SHIBA				SC
Date:	Friday, February 24, 2006		Sheet	4	of
				1	44



Change to BSS138
DY

Change to BSS138
DY
VREF_DDR_CLAW

LAYOUT: Locate close to CPU.
Change to single resistor

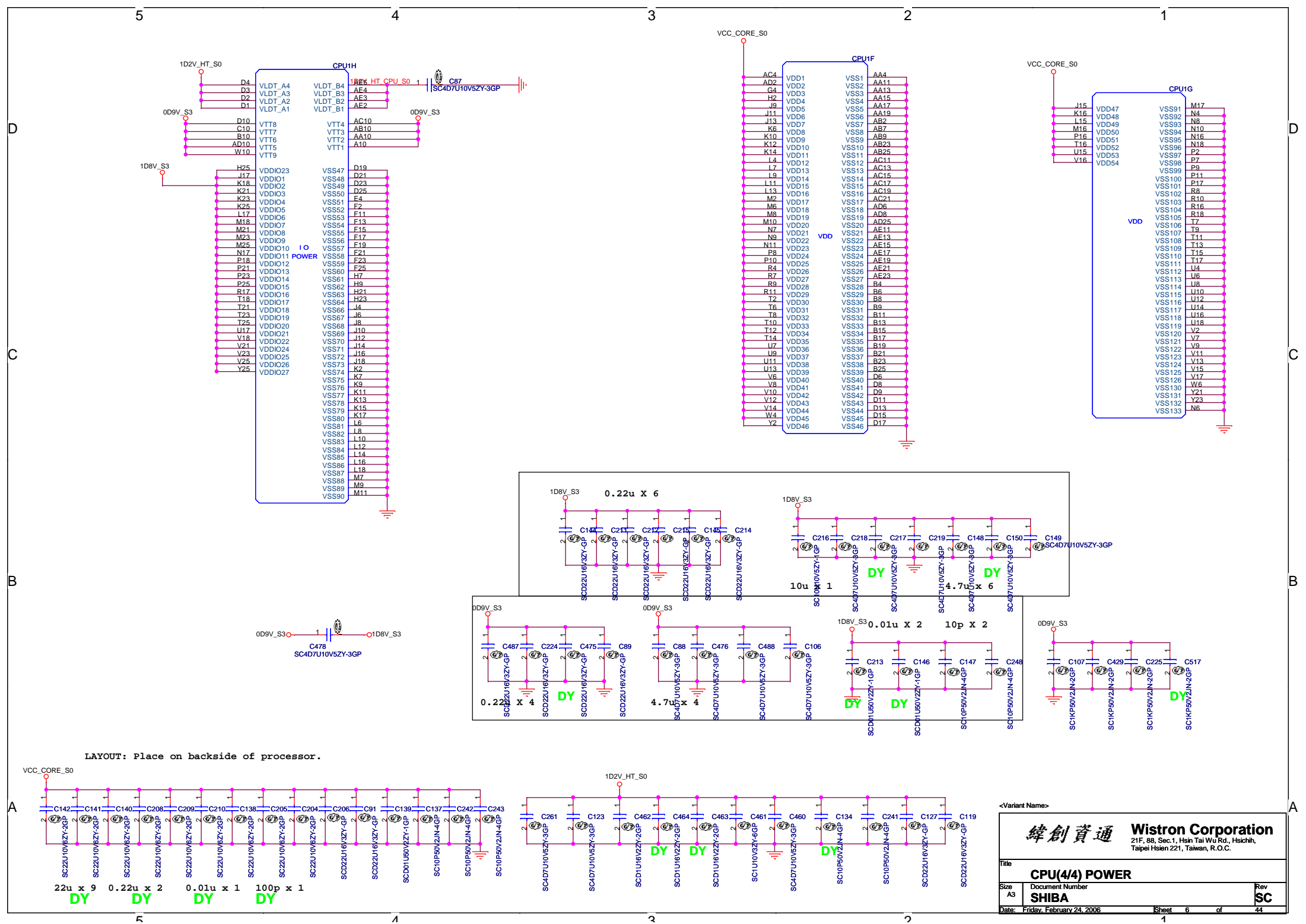
2nd source: Fairchild 74ALVC08
73.07408.DHB

AMD suggest to use 74HC09, it
contains open drain output

HDT Connectors

Add HDT connector for
AMD suggested
DY

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU(3/4) CONTROL		
Size A3	Document Number SHIBA	Rev SA
Date: Friday, February 24, 2006		Sheet 5 of 44

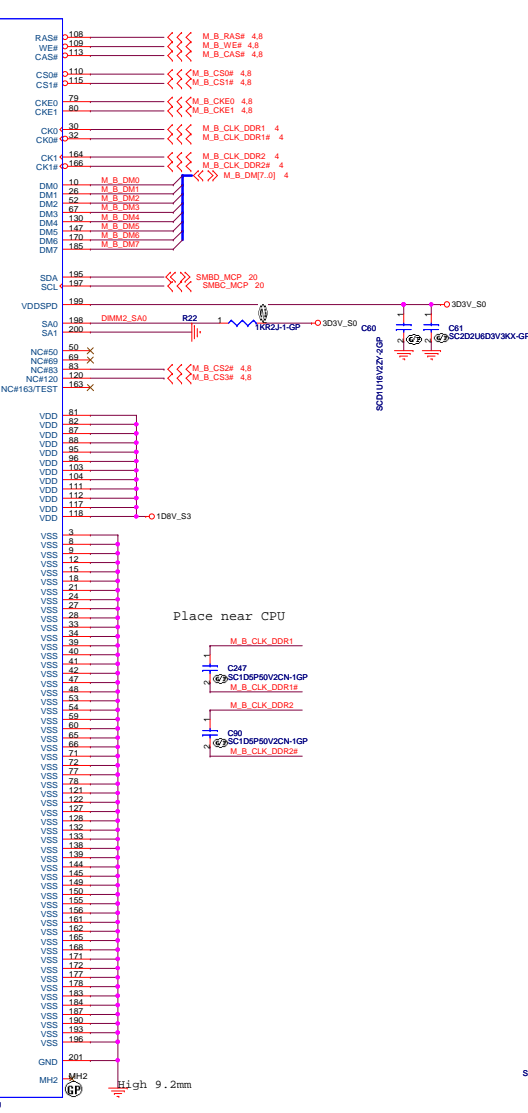
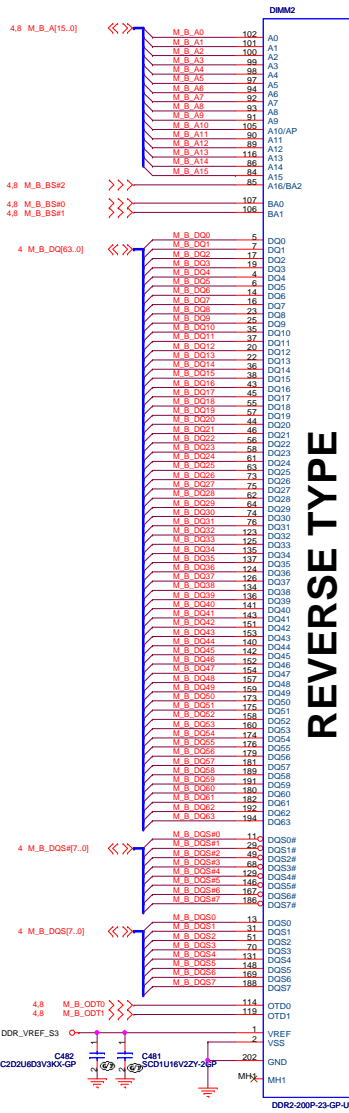


LAYOUT: Place on backside of processor.

<Variant Name>

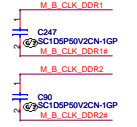
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU(4/4) POWER	
Size	Document Number	Rev	
A3	SHIBA	SC	
Date: Friday, February 24, 2006	Sheet 6	of 44	

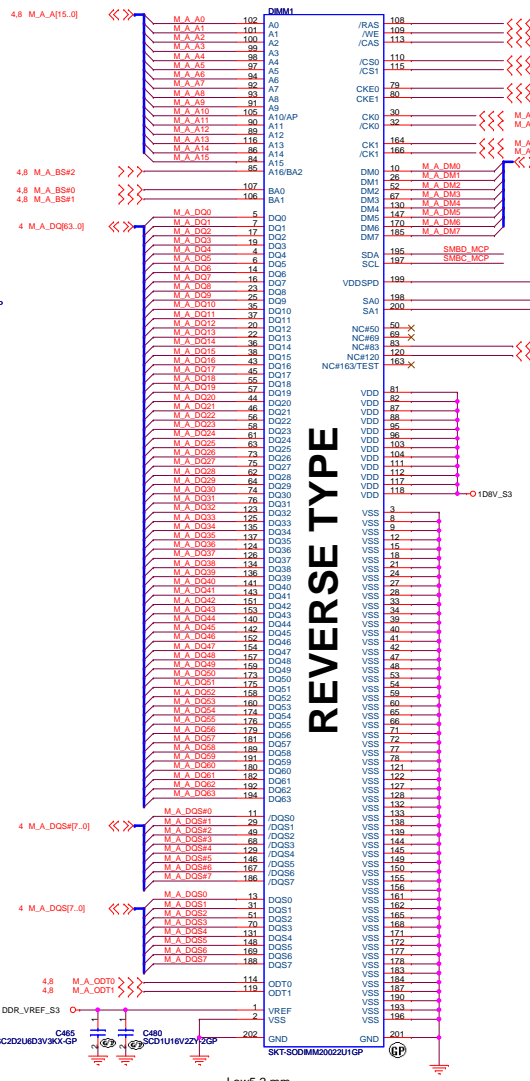


REVERSE TYPE

Place near CPU

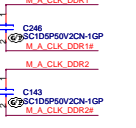


Hi 9.2 mm

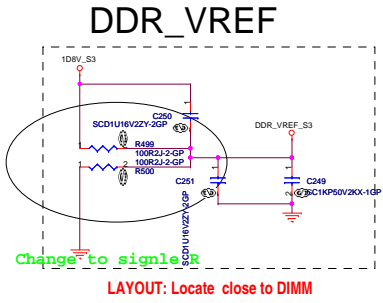


REVERSE TYPE

Place near CPU

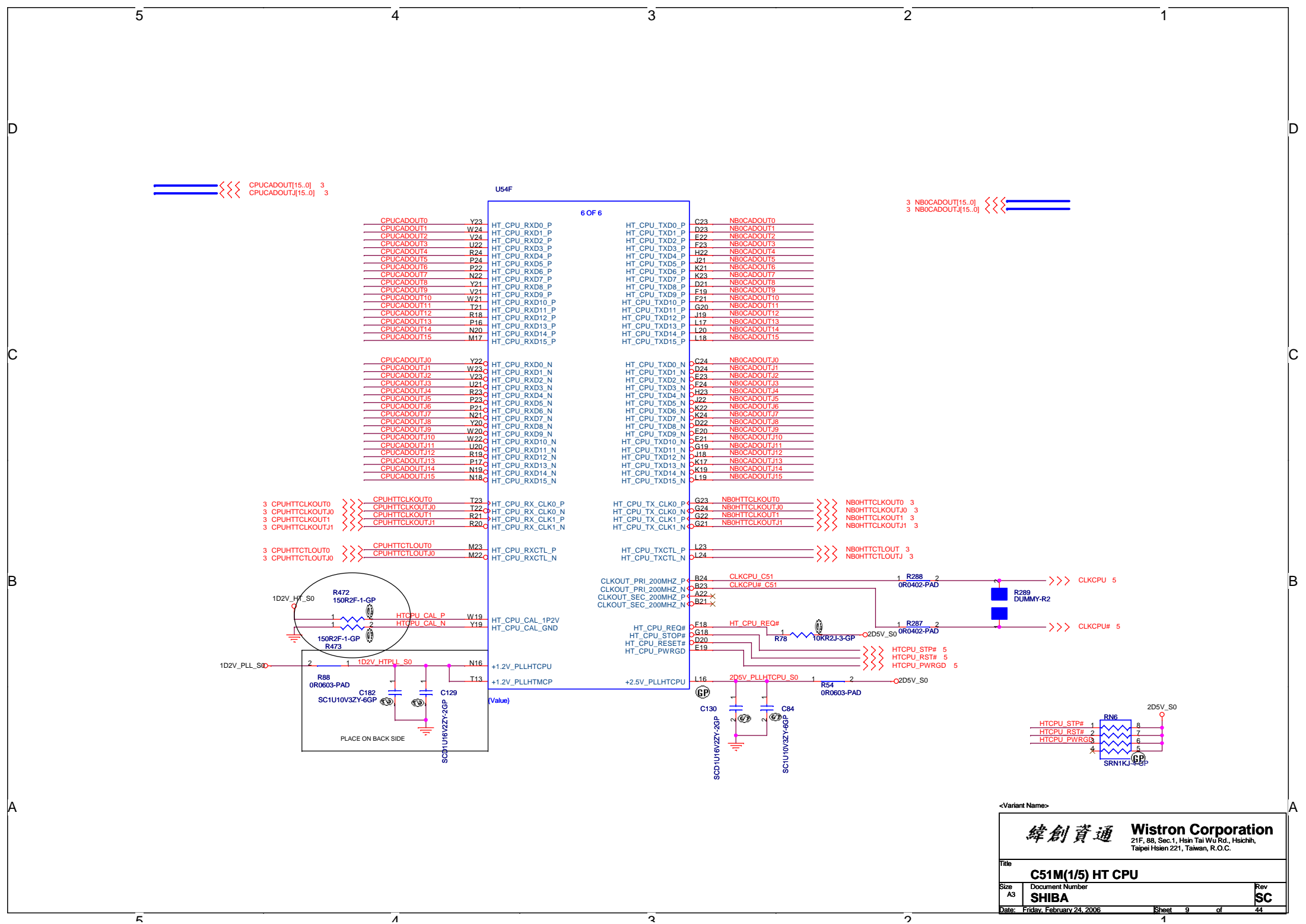


Low5.2 mm



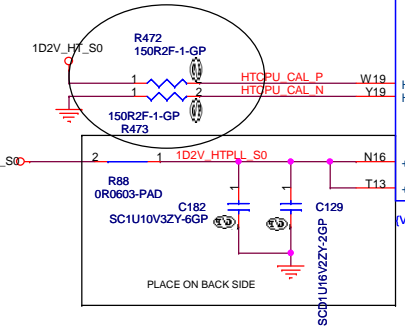
Change to singleR

LAYOUT: Locate close to DIMM



CPUCADOUT[15..0] 3
 CPUCADOUTJ[15..0] 3

NB0CADOUT[15..0] 3
 NB0CADOUTJ[15..0] 3



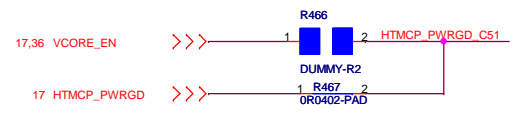
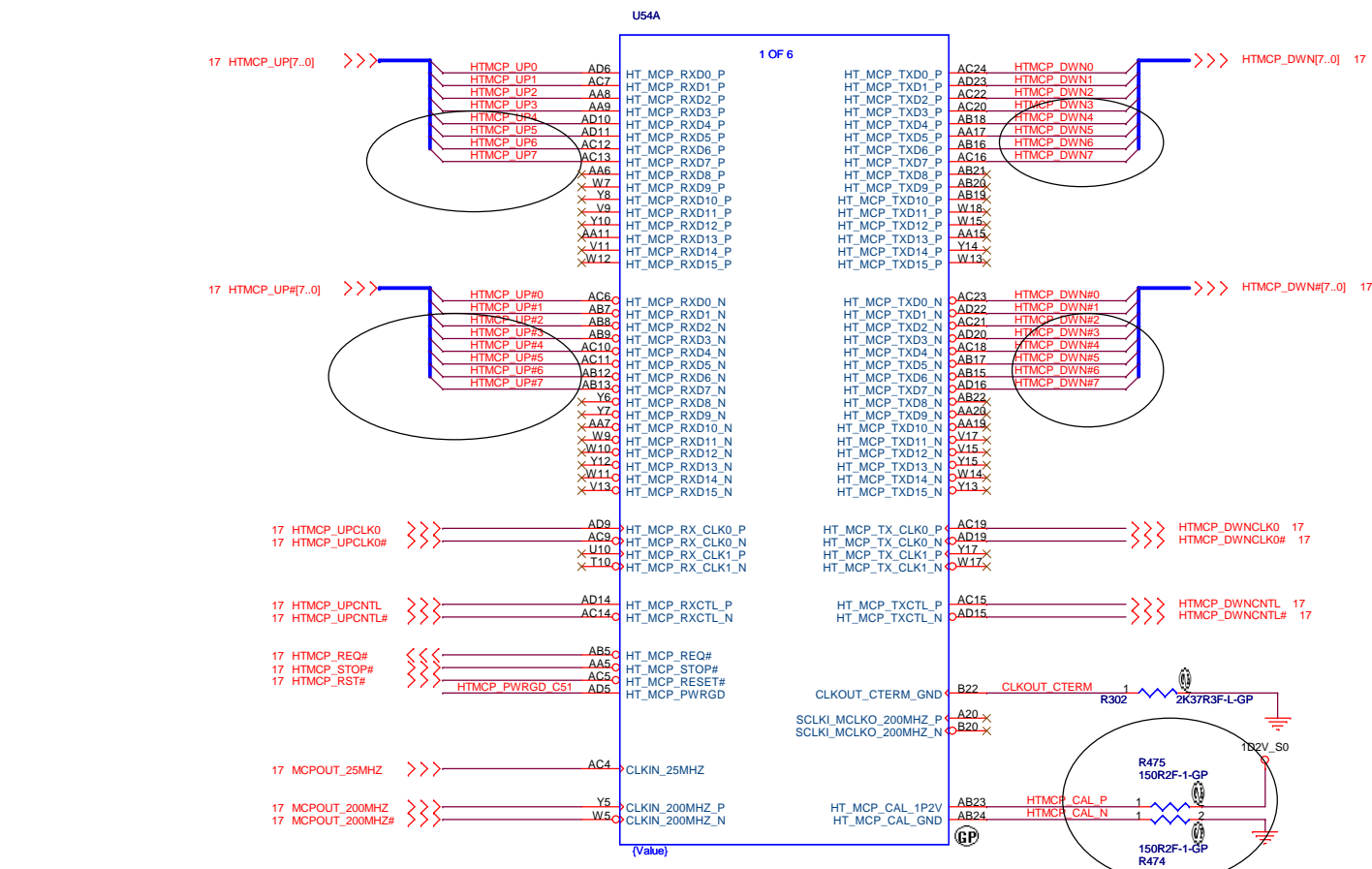
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(1/5) HT CPU**

Size	Document Number	Rev
A3	SHIBA	SC

Date: Friday, February 24, 2006 Sheet 9 of 44

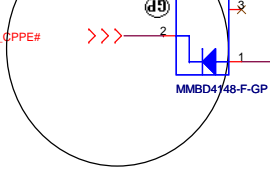


<Variant Name>

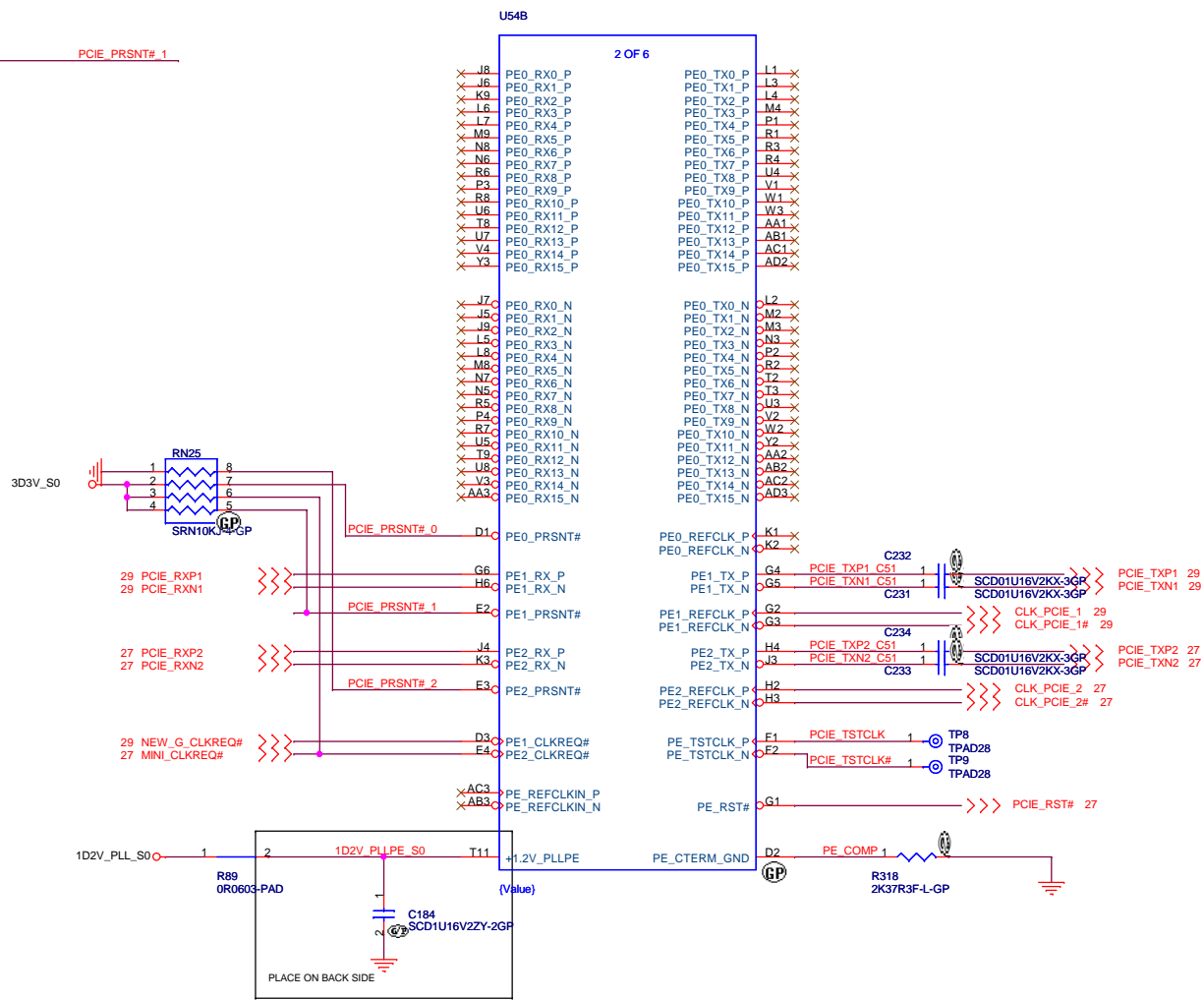
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

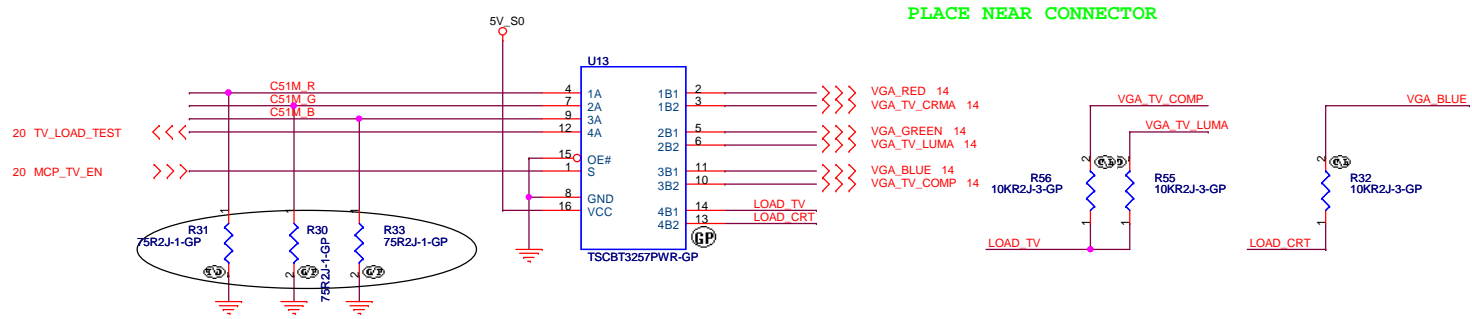
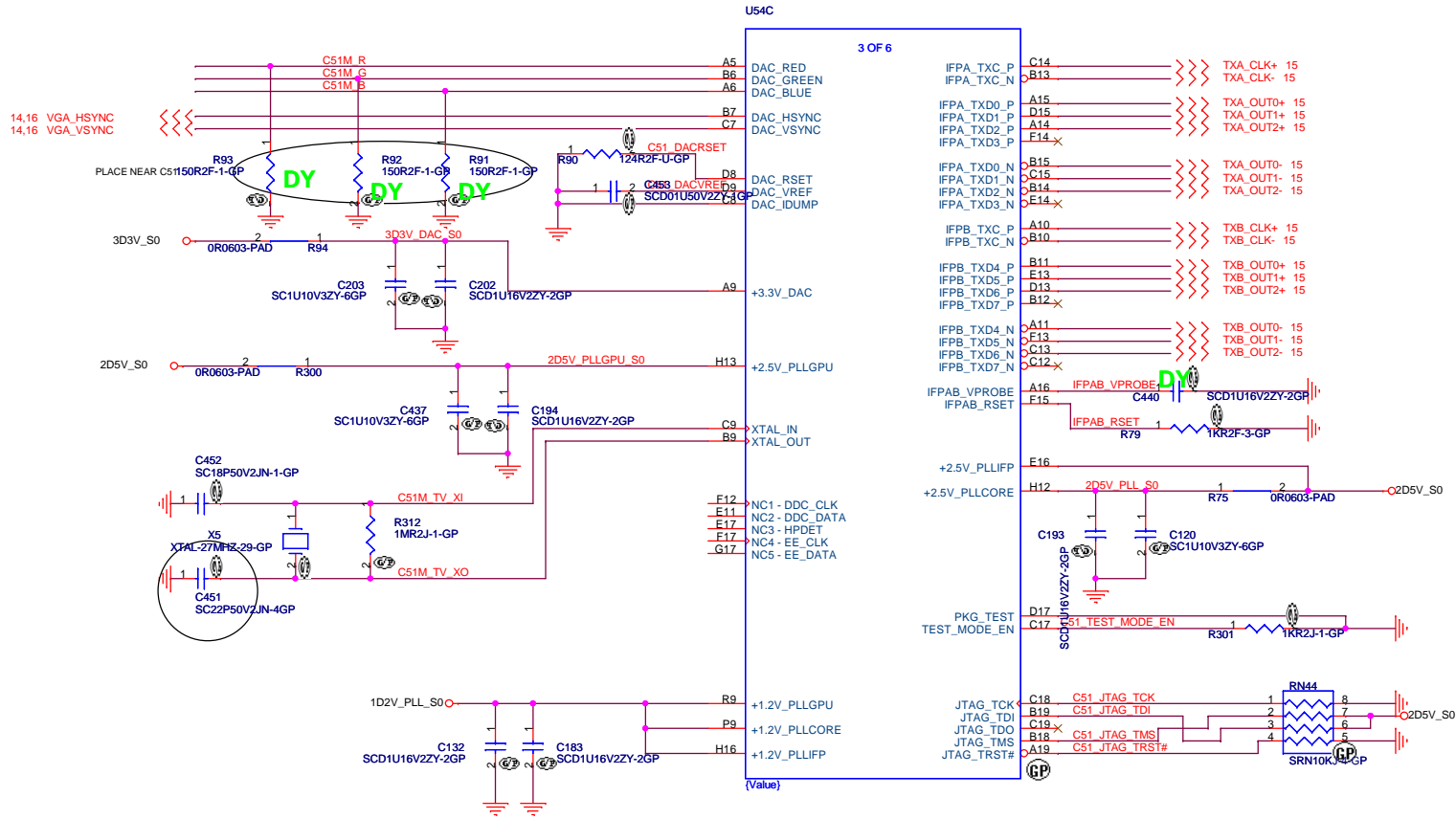
Title: **C51M(2/5)HT MCP**

Size: A3	Document Number: SHIBA	Rev: SC
Date: Friday, February 24, 2006	Sheet: 10	of 44



CHECK LEAKAGE CURRENT

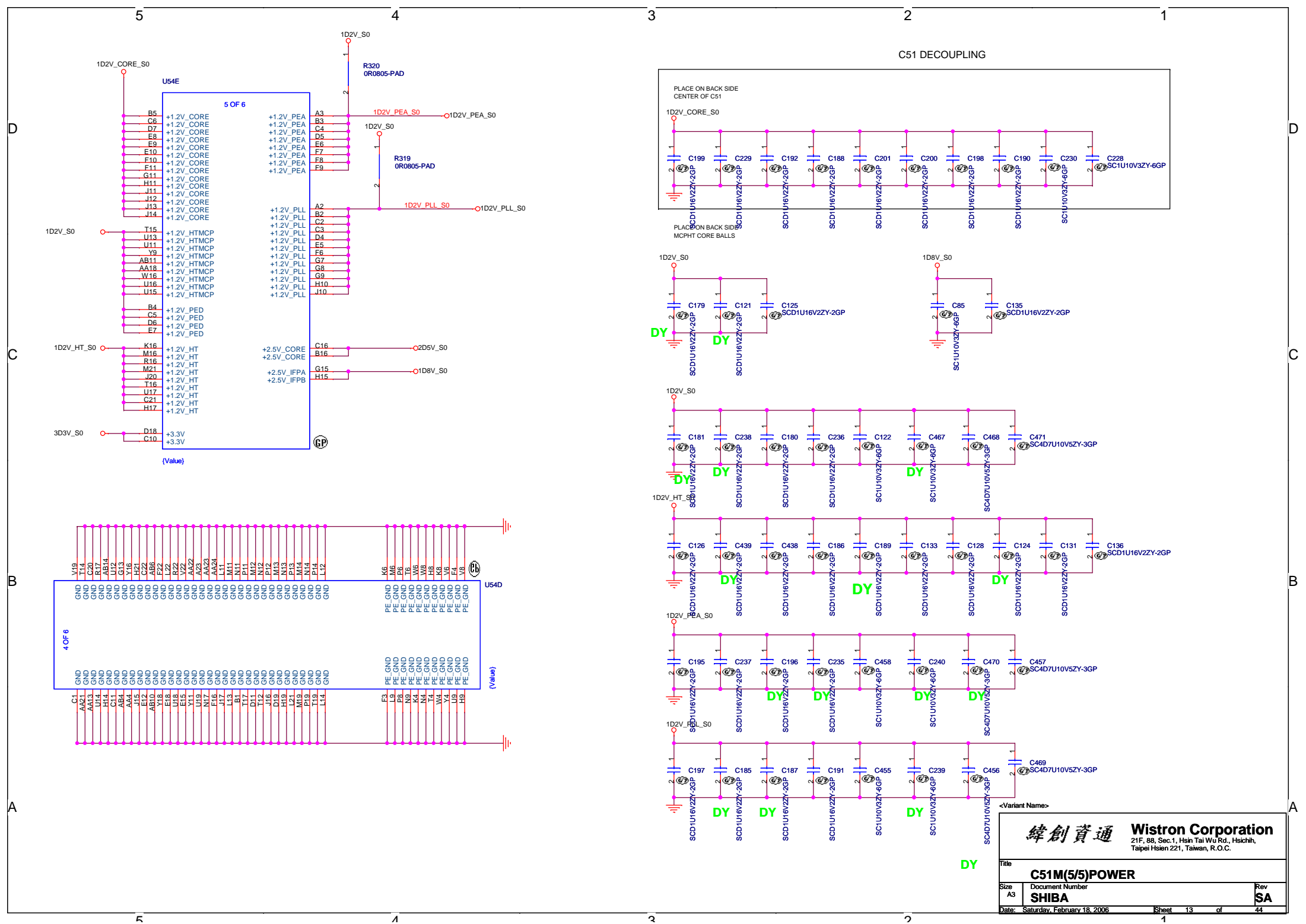




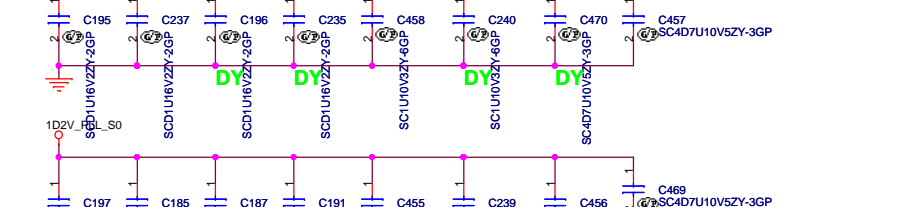
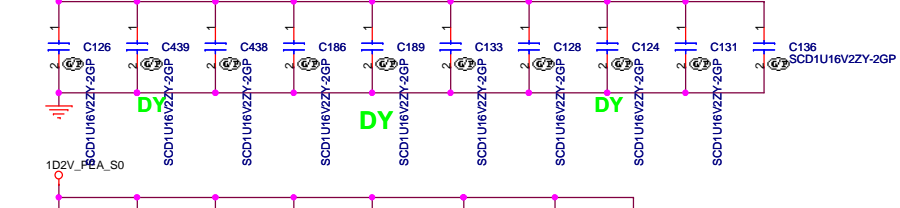
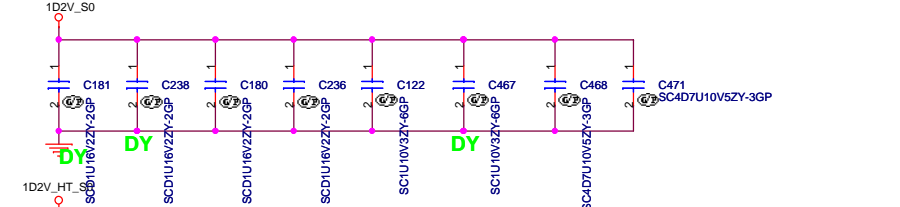
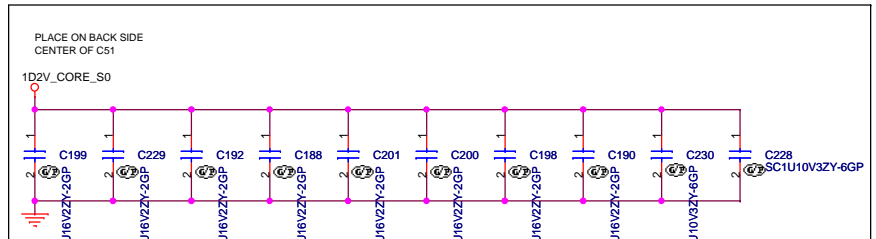
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title C51M(4/5)CRT/LVDS		
Size A3	Document Number SHIBA	Rev SA
Date: Wednesday, March 15, 2006	Sheet 12 of 44	



C51 DECOUPLING



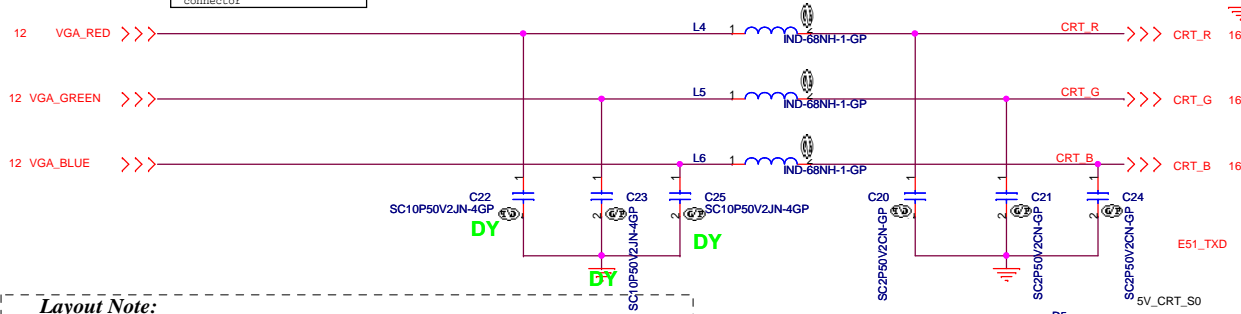
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(5/5)POWER**

Size: A3	Document Number: SHIBA	Rev: SA
Date: Saturday, February 18, 2006	Sheet: 13 of 44	

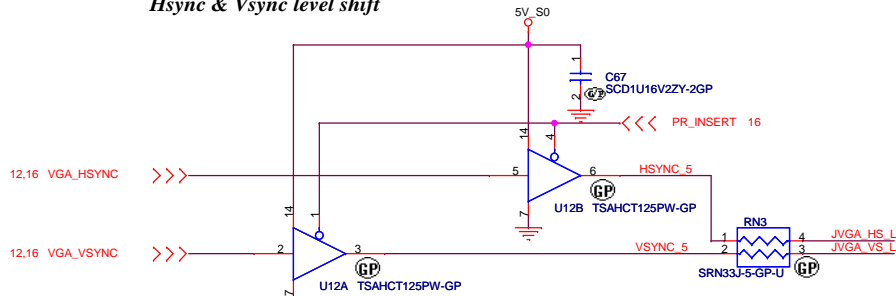
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector



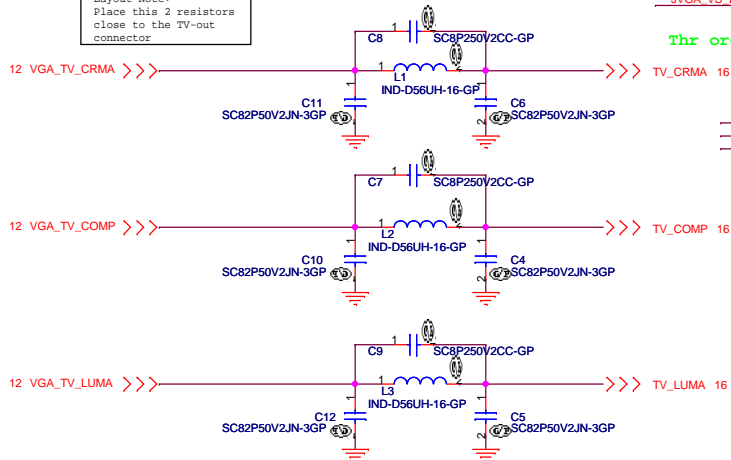
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

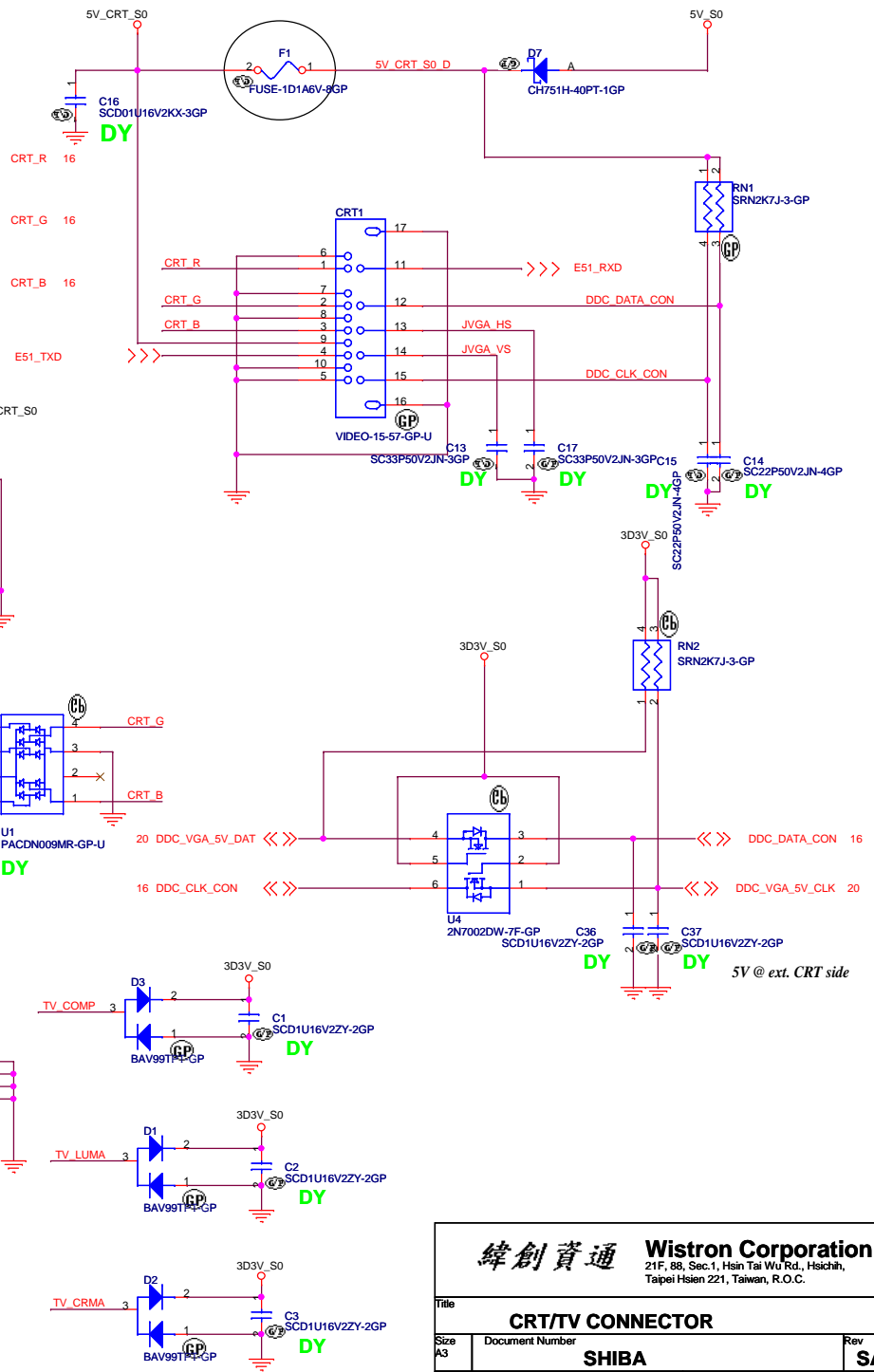
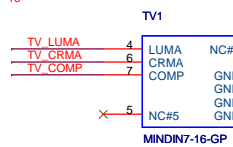


TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



Thr org part is 68.2703N.10B

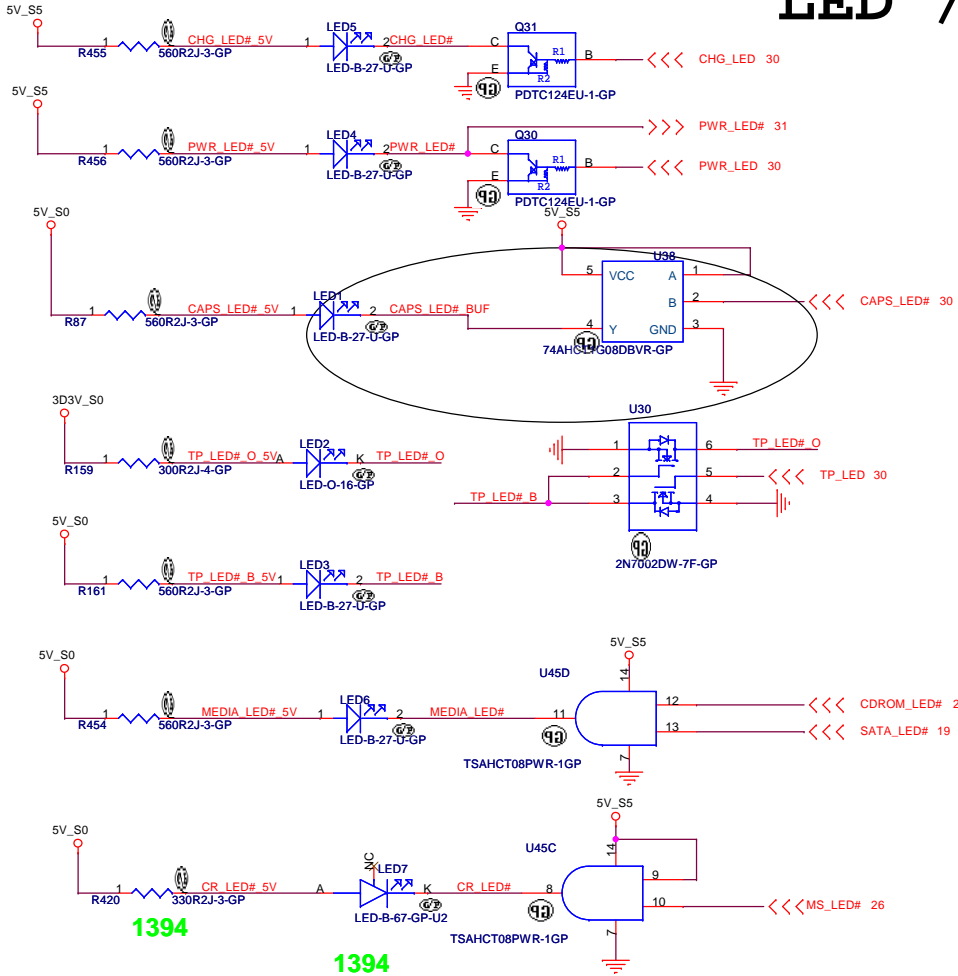


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

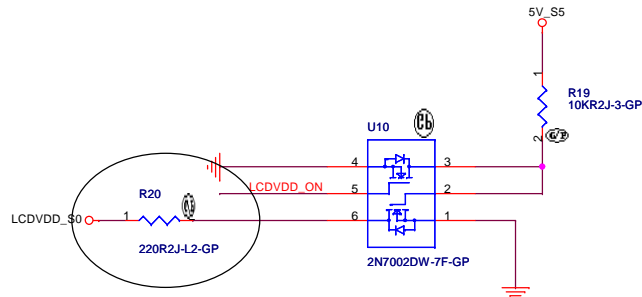
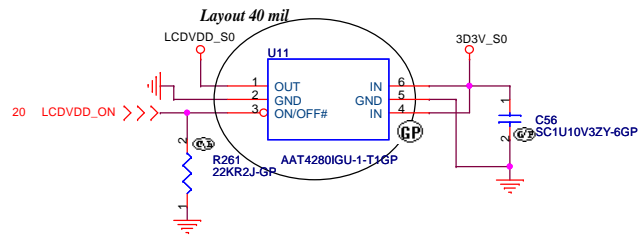
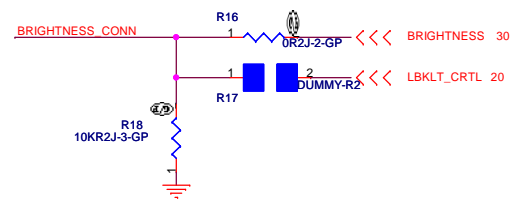
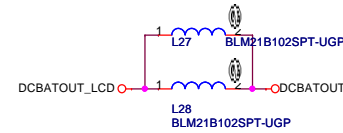
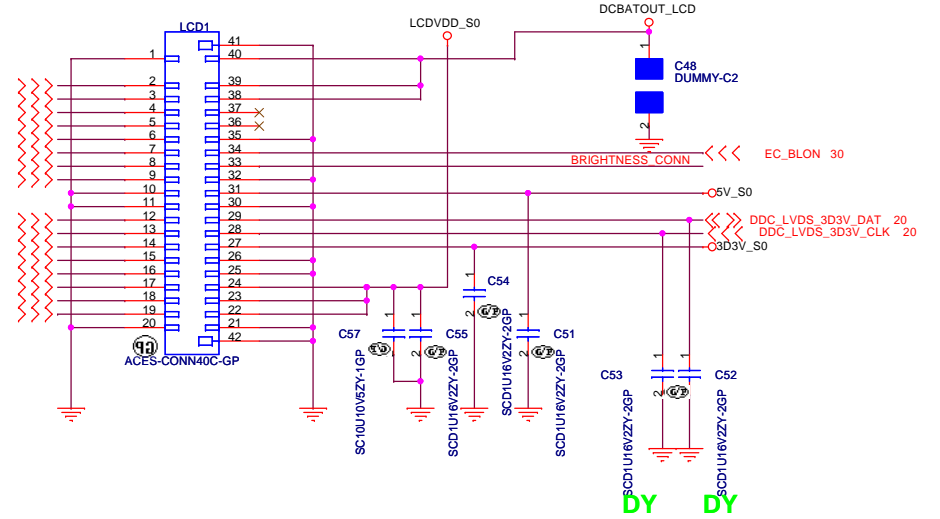
Title: **CRT/TV CONNECTOR**

Size A3	Document Number SHIBA	Rev SA
Date: Thursday, February 23, 2006	Sheet 14 of 44	

LED / INVERTER INTERFACE

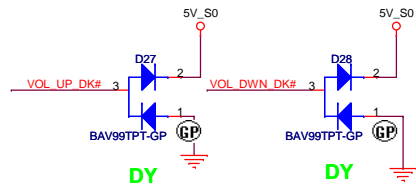


- 12 TXB_OUT2+
- 12 TXB_OUT2-
- 12 TXB_OUT1+
- 12 TXB_OUT1-
- 12 TXB_OUT0+
- 12 TXB_OUT0-
- 12 TXB_CLK+
- 12 TXB_CLK-
- 12 TXA_OUT2+
- 12 TXA_OUT2-
- 12 TXA_OUT1+
- 12 TXA_OUT1-
- 12 TXA_OUT0+
- 12 TXA_OUT0-
- 12 TXA_CLK+
- 12 TXA_CLK-

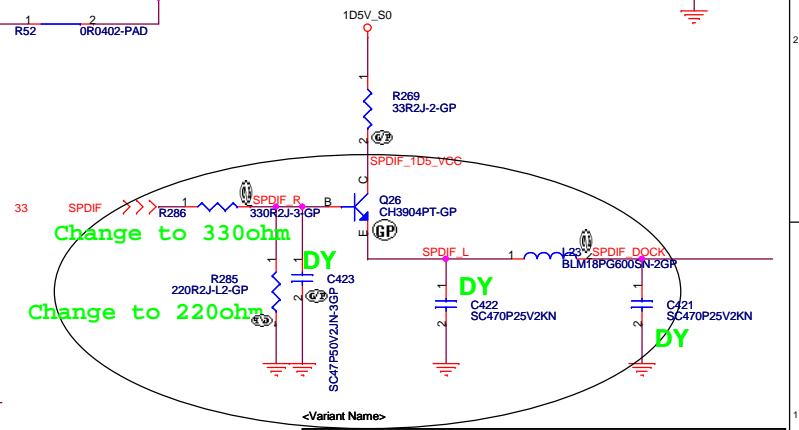
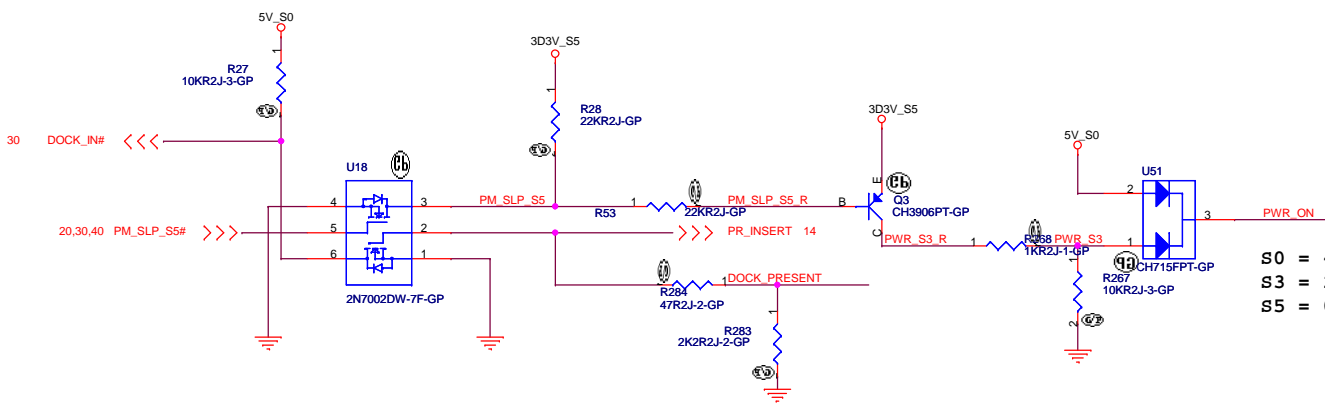
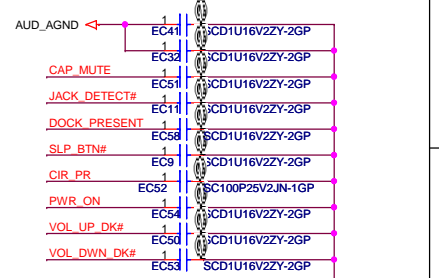
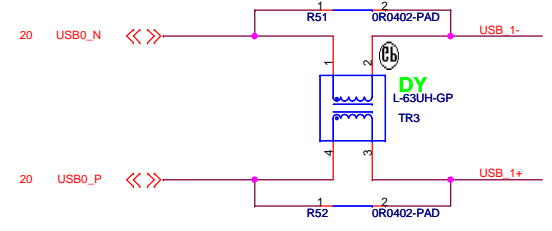
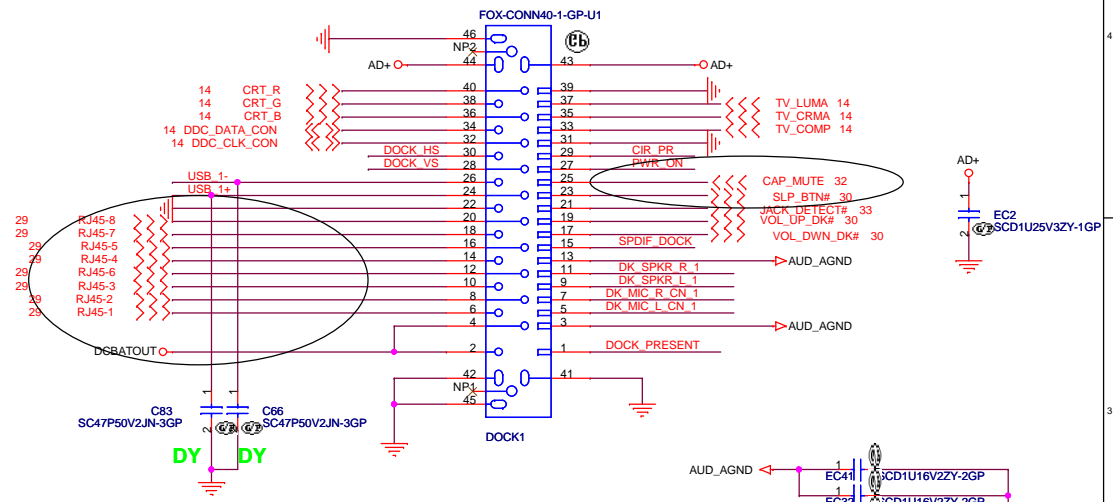
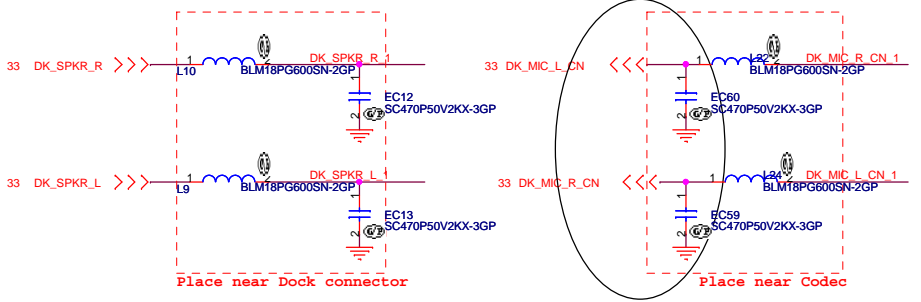
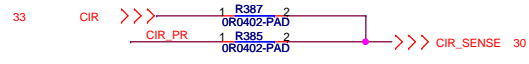
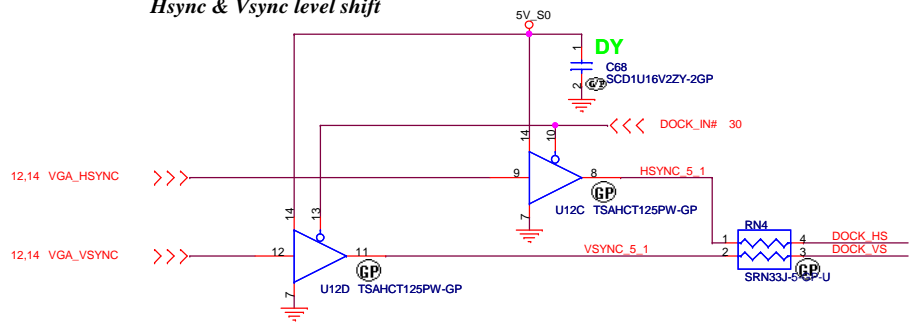


緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
LCD/Inverter Connector			
Title	Document Number	Rev	
Size Custom	SHIBA	SA	
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Docking Connector



Hsync & Vsync level shift



S0 = 4V
S3 = 2.5V
S5 = 0V

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Board to board conn/ Docking			
Title	Document Number	Rev	SA
	SHIBA		
Date: Monday, February 27, 2006	Sheet 16	of	44

D

D

C

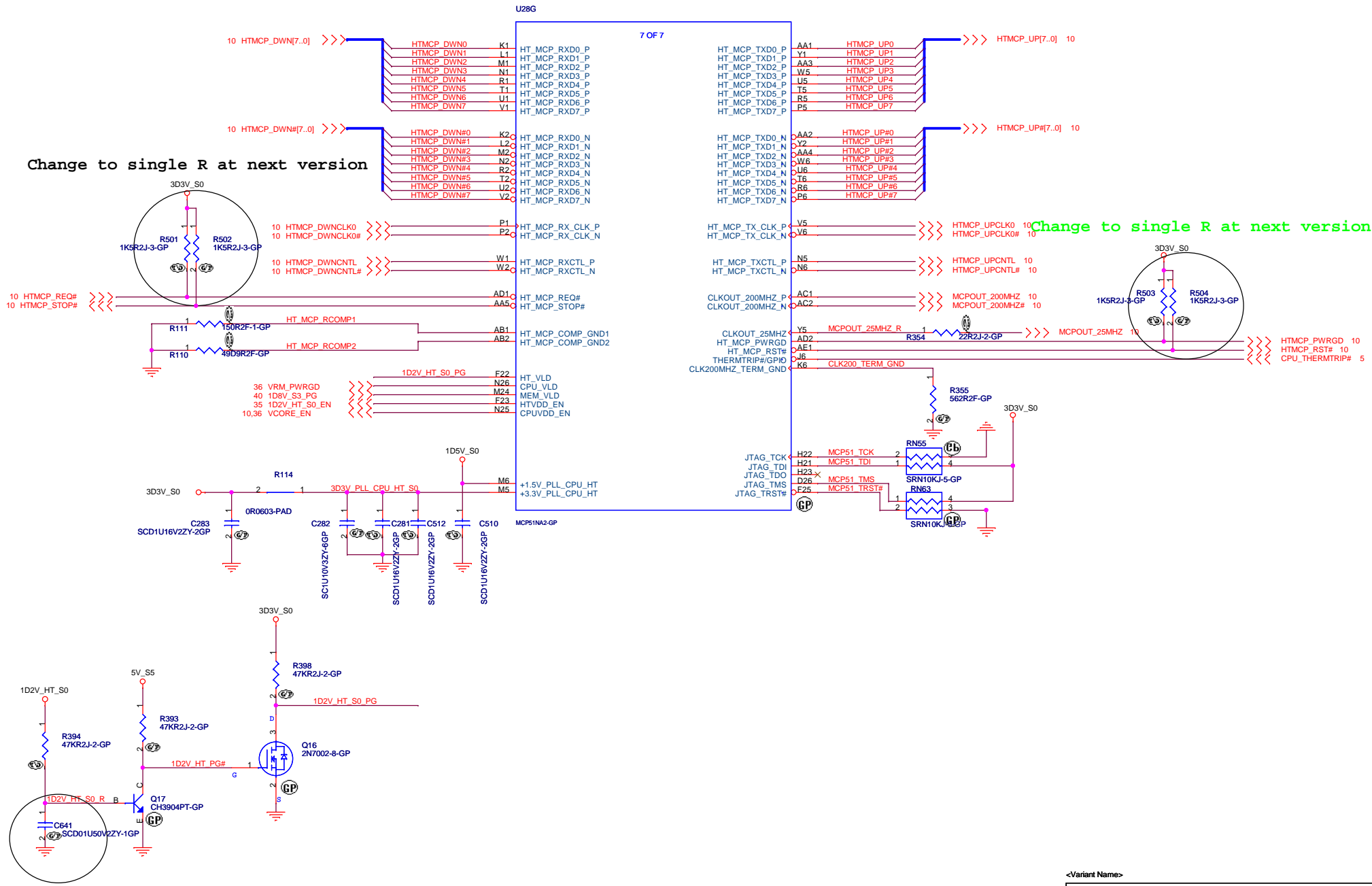
C

B

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A

A



<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(1/6)HT**

Size	Document Number	Rev
A3	SHIBA	SA
Date:	Monday, February 20, 2006	Sheet 17 of 44

D

25 PCI_AD[0..31] <<<>>>

25 PCI_C/BE#0 <<<>>> AD19 PCI_CBE#0
 25 PCI_C/BE#1 <<<>>> AB17 PCI_CBE#1
 25 PCI_C/BE#2 <<<>>> AA15 PCI_CBE#2
 25 PCI_C/BE#3 <<<>>> AA13 PCI_CBE#3

25 PCI_FRAME# <<<>>> AC15 PCI_FRAME#
 25 PCI_IRDY# <<<>>> AD15 PCI_IRDY#
 25 PCI_TRDY# <<<>>> AB16 PCI_TRDY#
 25 PCI_STOP# <<<>>> AE16 PCI_STOP#
 25 PCI_DEVSEL# <<<>>> AA16 PCI_DEVSEL#
 25 PCI_PAR <<<>>> AF16 PCI_PAR
 25 PCI_PERR# <<<>>> AF17 PCI_PERR#/GPIO
 25 PCI_SERR# <<<>>> AD11 PCI_SERR#
 25.30 PM_CLKRUN# <<<>>> AF25 PCI_CLKRUN#/GPIO

25 PCIRST# <<<>>> R388 22R2J-2-GP PCIRST# R AE25 PCI_RESET#0
 24 PCIRST#_IDE <<<>>> R389 22R2J-2-GP PCIRST#_IDE R AD24 PCI_RESET#1
 29 PCIRST#_NEW <<<>>> R167 22R2J-2-GP PCIRST#_NEW R AE26 PCI_RESET#2
 30.31 LPC_RST# <<<>>> R199 22R2J-2-GP LPC_RST# R L26 PCI_RESET#3

U28A

1 OF 7

PCI_AD0	AF19	PCI_AD0
PCI_AD1	AB21	PCI_AD1
PCI_AD2	AC19	PCI_AD2
PCI_AD3	AA20	PCI_AD3
PCI_AD4	AA19	PCI_AD4
PCI_AD5	AE20	PCI_AD5
PCI_AD6	AE19	PCI_AD6
PCI_AD7	AE20	PCI_AD7
PCI_AD8	AB20	PCI_AD8
PCI_AD9	AB19	PCI_AD9
PCI_AD10	AA18	PCI_AD10
PCI_AD11	AB18	PCI_AD11
PCI_AD12	AE18	PCI_AD12
PCI_AD13	AF18	PCI_AD13
PCI_AD14	AC17	PCI_AD14
PCI_AD15	AA17	PCI_AD15
PCI_AD16	AB15	PCI_AD16
PCI_AD17	AE15	PCI_AD17
PCI_AD18	AE15	PCI_AD18
PCI_AD19	AF14	PCI_AD19
PCI_AD20	AE14	PCI_AD20
PCI_AD21	AA14	PCI_AD21
PCI_AD22	AB14	PCI_AD22
PCI_AD23	AC13	PCI_AD23
PCI_AD24	AB13	PCI_AD24
PCI_AD25	AE13	PCI_AD25
PCI_AD26	AF13	PCI_AD26
PCI_AD27	AA12	PCI_AD27
PCI_AD28	AB12	PCI_AD28
PCI_AD29	AE12	PCI_AD29
PCI_AD30	AE12	PCI_AD30
PCI_AD31	AF11	PCI_AD31

MCP51NA2-GP

PCI_REQ#0 <<<>>> AA22 PCI_REQ#0 <<<>>> PCI_REQ#0 25
 PCI_REQ#1 <<<>>> AE22 PCI_REQ#1
 PCI_REQ#2 <<<>>> AF21 PCI_REQ#2
 PCI_REQ#3/GPIO <<<>>> AE22 PCI_REQ#3
 PCI_REQ#4/GPIO <<<>>> AE23 PCI_REQ#4

PCI_GNT#0 <<<>>> AE21 PCI_GNT#0 <<<>>> PCI_GNT#0 25
 PCI_GNT#1 <<<>>> AC21
 PCI_GNT#2 <<<>>> AA21
 PCI_GNT#3/GPIO <<<>>> AB24
 PCI_GNT#4/GPIO <<<>>> AB24

PCI_INTW# <<<>>> AE11 PCI_INTW# <<<>>> PCI_INTW# 25
 PCI_INTX# <<<>>> AB11 PCI_INTX# <<<>>> PCI_INTX# 25
 PCI_INTY# <<<>>> AC11 PCI_INTY#
 PCI_INTZ# <<<>>> AA11 PCI_INTZ#

PCI_CLK#0 <<<>>> AE24 PCI_CLK# R <<<>>> PCI_CLK# 25
 PCI_CLK1 <<<>>> AF24
 PCI_CLK2 <<<>>> AD23
 PCI_CLK3 <<<>>> AE23
 PCI_CLK4 <<<>>> AB23

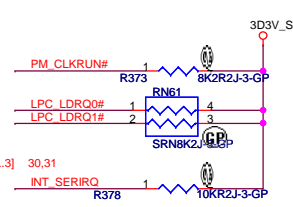
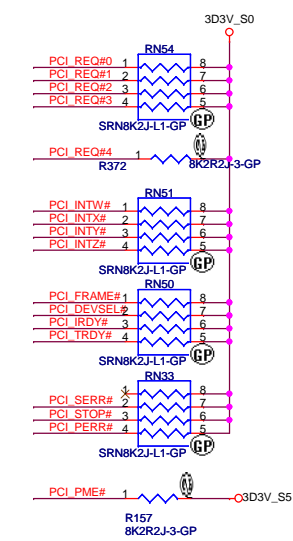
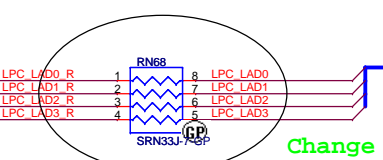
PCI_CLKIN <<<>>> AC23 PCI_CLKIN

LPC_AD0 K24 LPC_LAD0 R 1 8 LPC_LAD0 <<<>>> LPC_LAD[0..3] 30.31
 LPC_AD1 H26 LPC_LAD1 R 2 7 LPC_LAD1
 LPC_AD2 H25 LPC_LAD2 R 3 6 LPC_LAD2
 LPC_AD3 K22 LPC_LAD3 R 4 5 LPC_LAD3

LPC_FRAME# G25 LPC_LDRQ0# <<<>>> LPC_LFRAME# 30.31
 LPC_DRQ#0 K21 LPC_LDRQ1# <<<>>> INT_SERIRQ 25.30
 LPC_DRQ#1/LPC_CS# L22
 LPC_SERIRQ H24

LPC_PWRDWN#/GPIO H24

LPC_CLK#0 F26 LPC_CLK# R 1 8 LPC_CLK# 30
 LPC_CLK1 G26 PCI_CLK1# R 1 8 PCI_CLK# GOLD 31



<Variant Name>

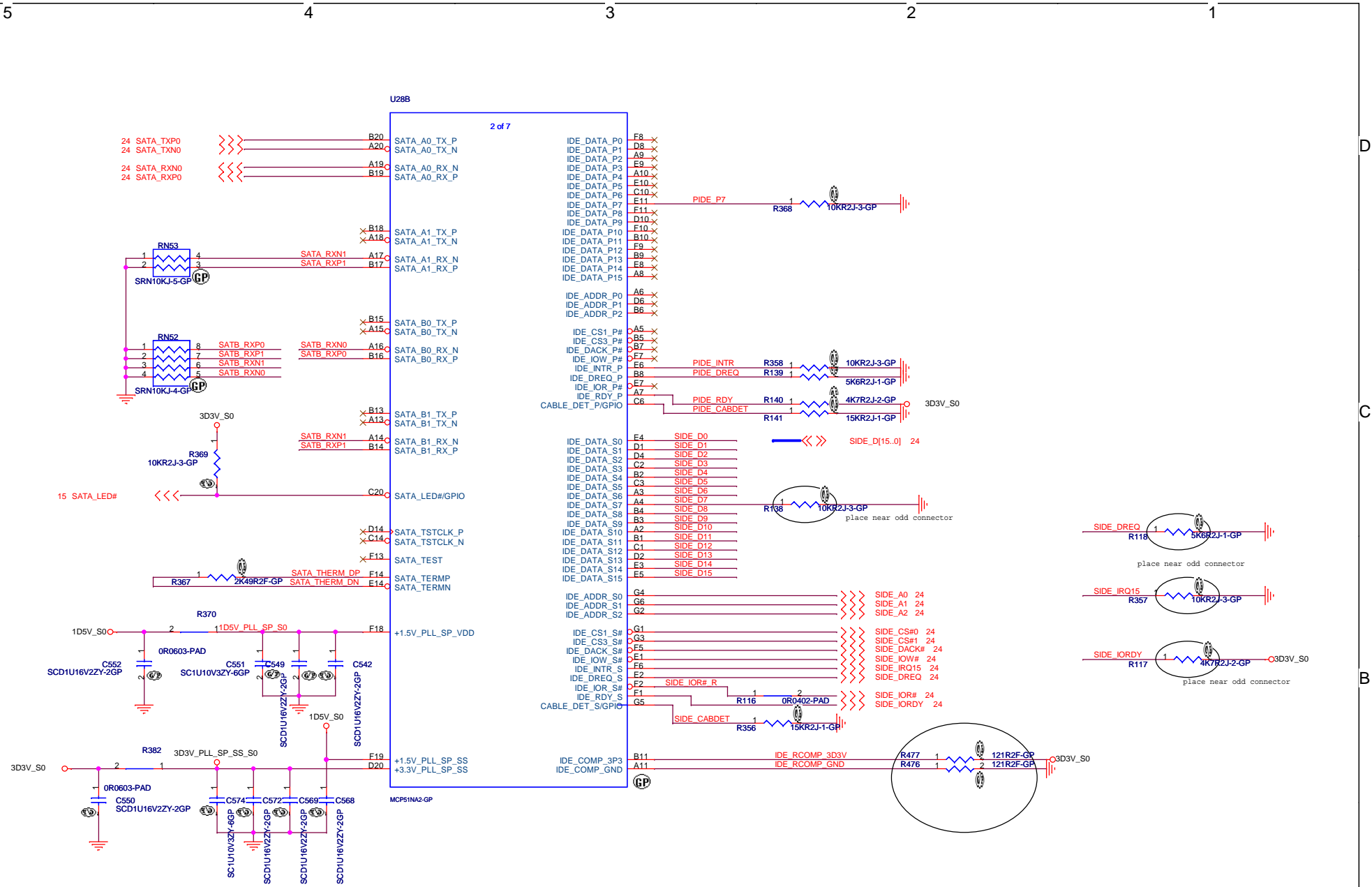
緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MCP51(2/6)PCI			
Size			
A3		Document Number	
SHIBA		Rev	
Date: Monday, February 20, 2006		SA	
Sheet 18		of 44	

D

C

B

A



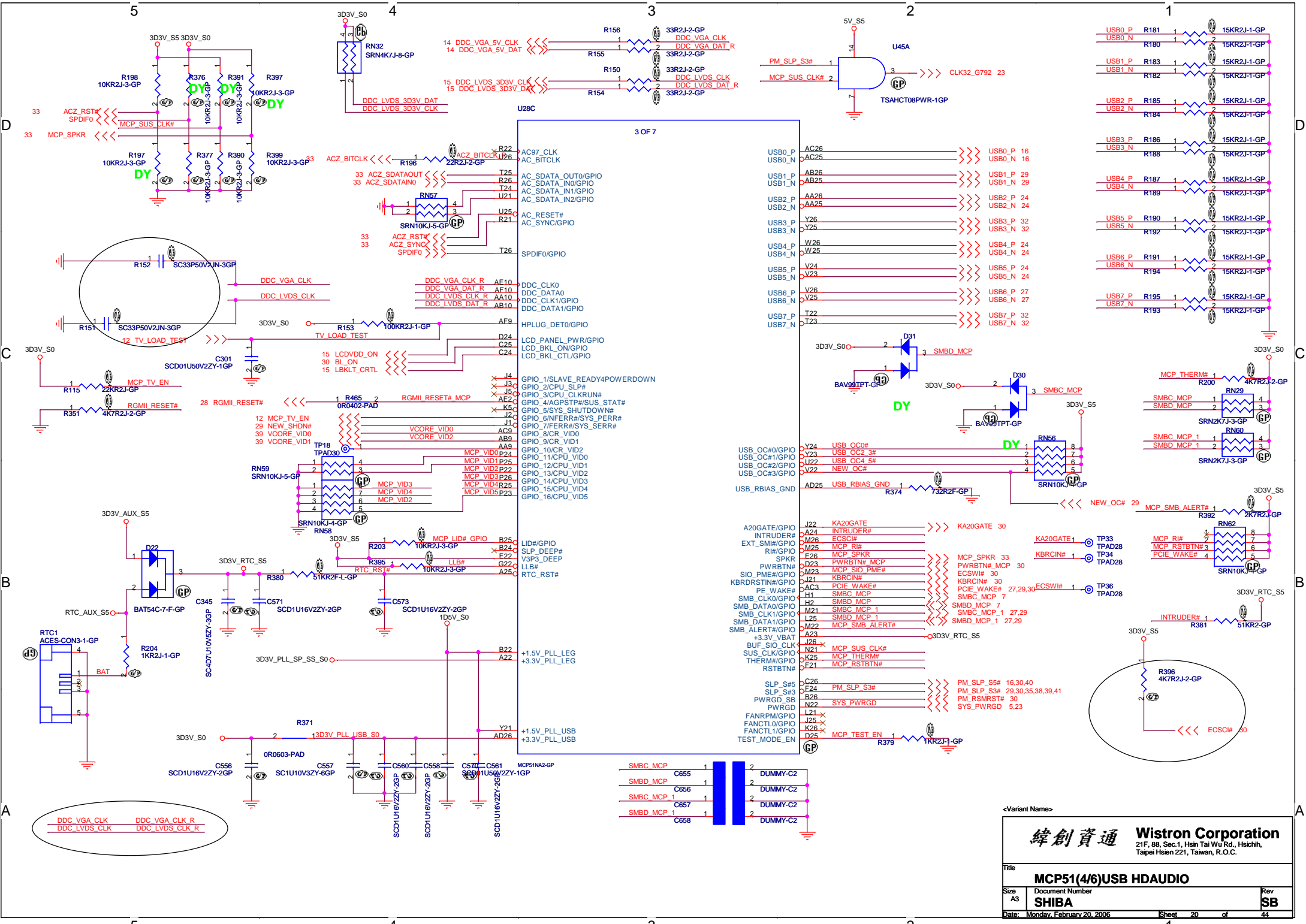
<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(3/6)SATA/PATA**

Size: A3
 Document Number: **SHIBA**
 Date: Monday, February 20, 2006

Rev: **SA**
 Sheet: 19 of 44



14 DDC_VGA_5V_CLK
14 DDC_VGA_5V_DAT
15 DDC_LVDS_3D3V_CLK
15 DDC_LVDS_3D3V_DAT

PM_SLP_S3#
MCP_SUS_CLK#
CLK32_G792 23

AC97_CLK
AC_BITCLK
AC_SDATA_OUT0/GPIO
AC_SDATA_IN0/GPIO
AC_SDATA_IN1/GPIO
AC_SDATA_IN2/GPIO
AC_RESET#
AC_SYNC/GPIO

USB0_P AC26
USB0_N AC25
USB1_P AB26
USB1_N AB25
USB2_P AA26
USB2_N AA25
USB3_P Y26
USB3_N Y25
USB4_P W26
USB4_N W25
USB5_P V24
USB5_N V23
USB6_P V26
USB6_N V25
USB7_P T22
USB7_N T23

DDC_VGA_CLK R AE10
DDC_VGA_DAT R AF10
DDC_LVDS_CLK R AA10
DDC_LVDS_DAT R AB10

USB_OC0/GPIO Y24
USB_OC1/GPIO Y23
USB_OC2/GPIO Y22
USB_OC3/GPIO Y22
NEW_OC# 29

GPIO_1/SLAVE_READY4POWERDOWN
GPIO_2/CPU_SLP#
GPIO_3/CPU_CLKRUN#
GPIO_4/AGPSTP#/SUS_STAT#
GPIO_5/SYS_SHUTDOWN#
GPIO_6/NFERR#/SYS_SERR#
GPIO_7/8CR_VID0
GPIO_8/9CR_VID0
GPIO_10/CR_VID2
GPIO_11/CPU_VID0
GPIO_12/CPU_VID1
GPIO_13/CPU_VID2
GPIO_14/CPU_VID3
GPIO_15/CPU_VID4
GPIO_16/CPU_VID5

A20GATE/GPIO Y22
INTRUDER# A24
EXT_SMI#/GPIO M26
Ri#/GPIO M25
MCP_Ri# M25
MCP_SPKR E26
PWRBTN# M23
MCP_SIO_PME# M23
KBRDRSTN#/GPIO A21
KBRClN# M23
PCIE_WAKE# H11
SMB_CLK0/GPIO H2
SMB_DATA0/GPIO M21
SMB_CLK1/GPIO M21
SMB_DATA1/GPIO L25
SMB_ALERT#/GPIO M22
MCP_SMB_ALERT# M22

LID#/GPIO B25
SLP_DEEP# B24
V3P3_DEEP E22
LLB# G22
RTC_RST# A25

KA20GATE_1 TP33
KBRClN#_1 TP34
ECSSW#_1 TP36
INTRUDER#_1 R381

+1.5V_PLL_LEG
+3.3V_PLL_LEG

PM_SLP_S5# C26
PM_SLP_S3# C24
SYS_PWRGD N22
MCP_SUS_CLK# N21
MCP_THERM# K25
MCP_RSTBTN# E21

+1.5V_PLL_USB
+3.3V_PLL_USB

FANRPM/GPIO L21
FANCTL0/GPIO J25
FANCTL1/GPIO J25
TEST_MODE_EN D25

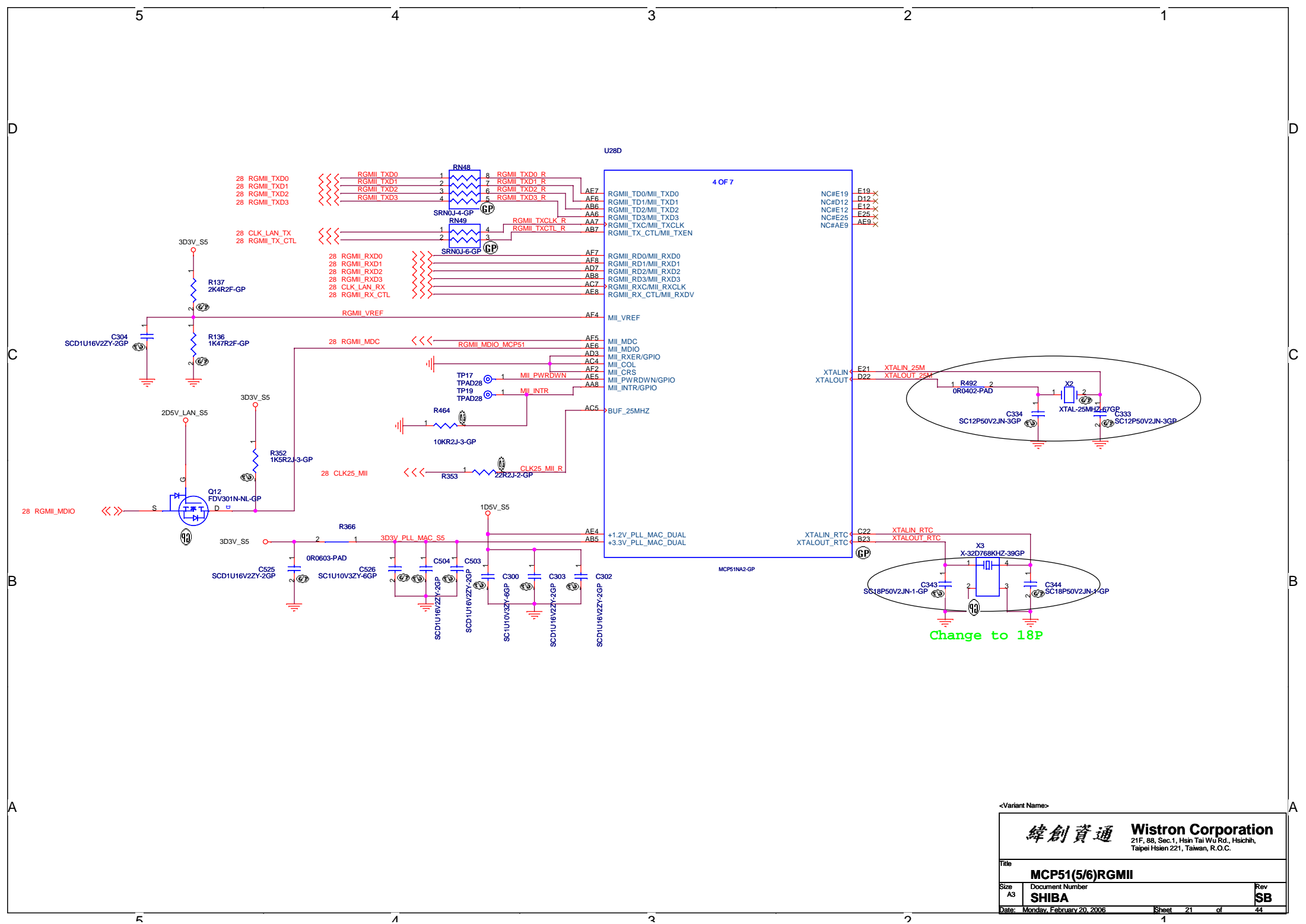
SMB_C MCP	1	2	DUMMY-C2
SMB_D MCP	1	2	DUMMY-C2
SMB_C MCP	1	2	DUMMY-C2
SMB_D MCP	1	2	DUMMY-C2

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(4/6)USB HDAUDIO**

Size: A3 Document Number: **SHIBA** Rev: **SB**

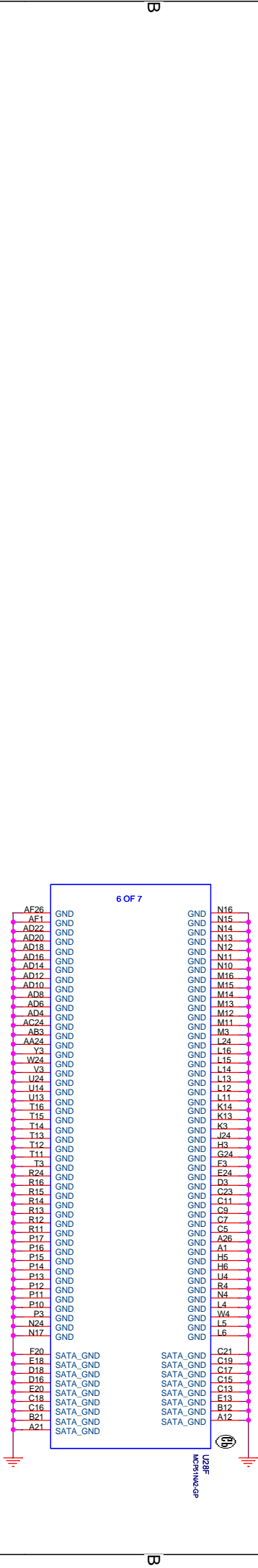
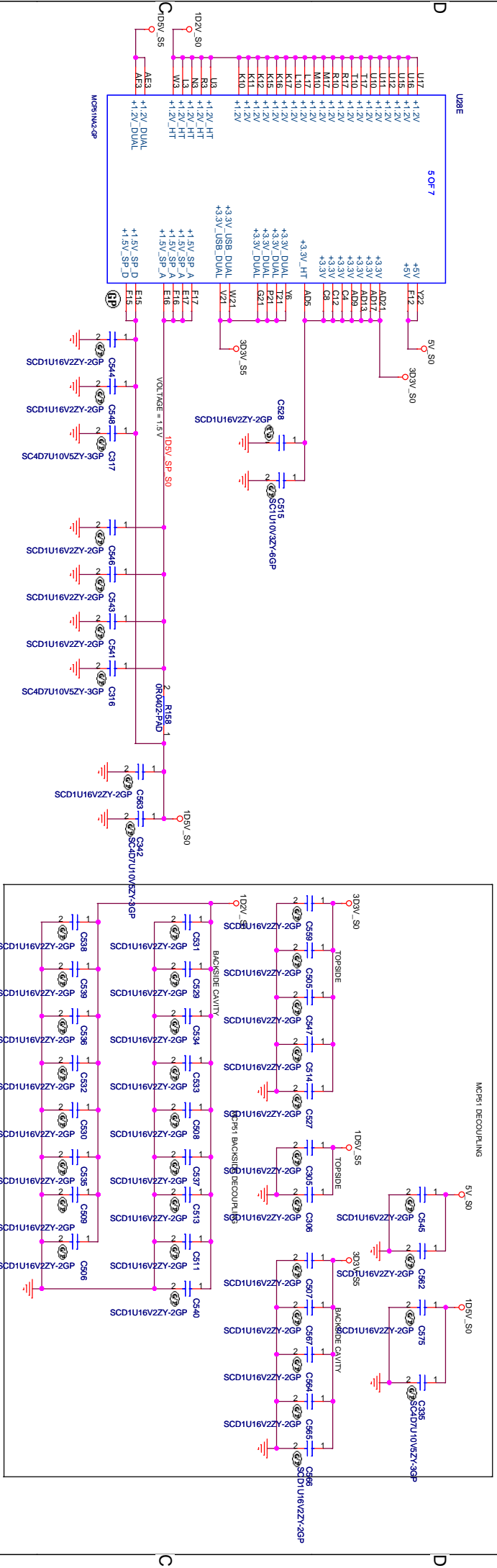
Date: Monday, February 20, 2006 Sheet: 20 of 44



<Variant Name>

緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

Title MCP51(5/6)RGMII		
Size A3	Document Number SHIBA	Rev SB
Date: Monday, February 20, 2006	Sheet 21	of 44



Wistron Corporation
 2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

偉創資通

Document Number: **MCP51(6)POWER**

Rev: **SB**

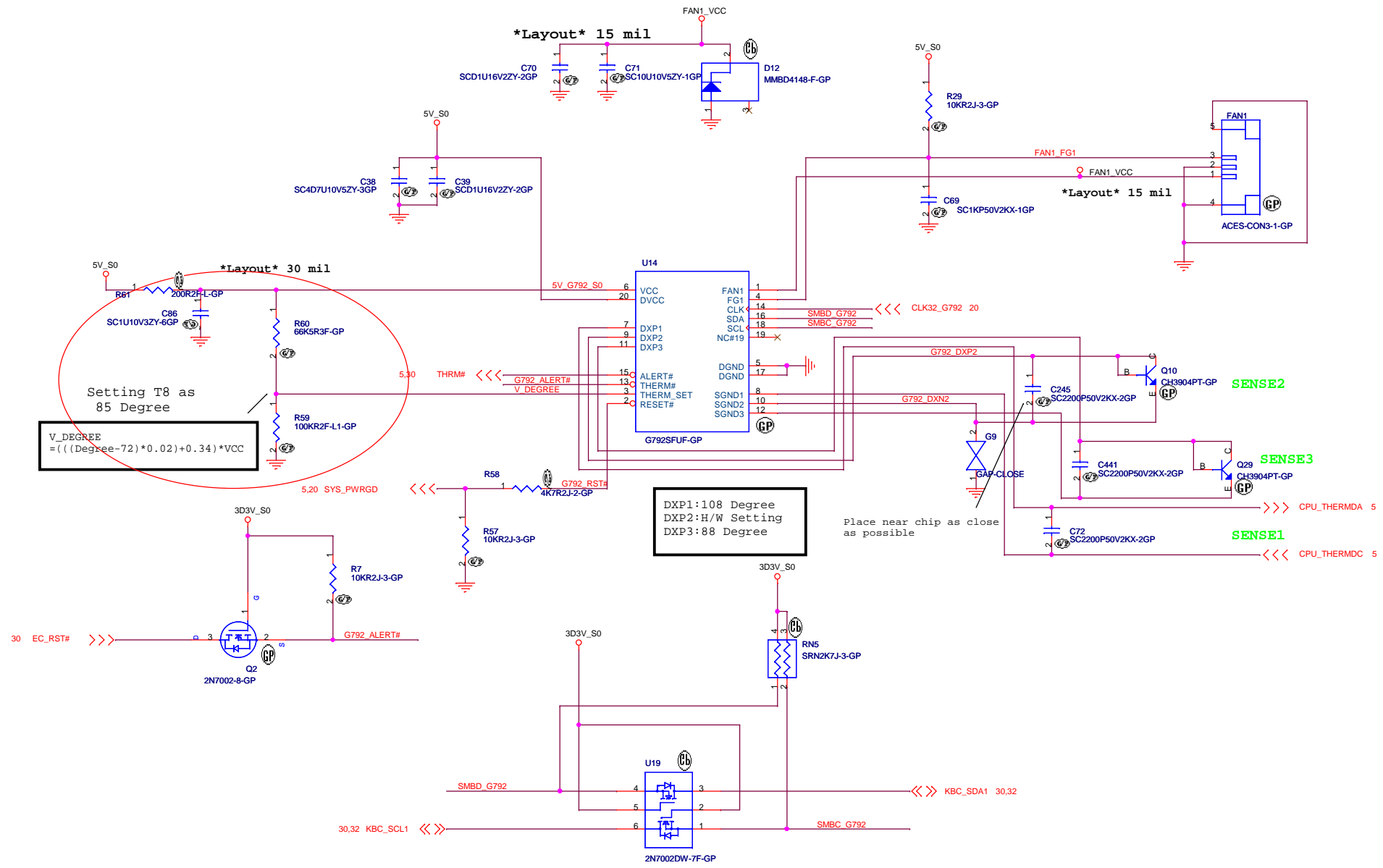
Sheet: 22 of 44

Date: Monday, February 20, 2006

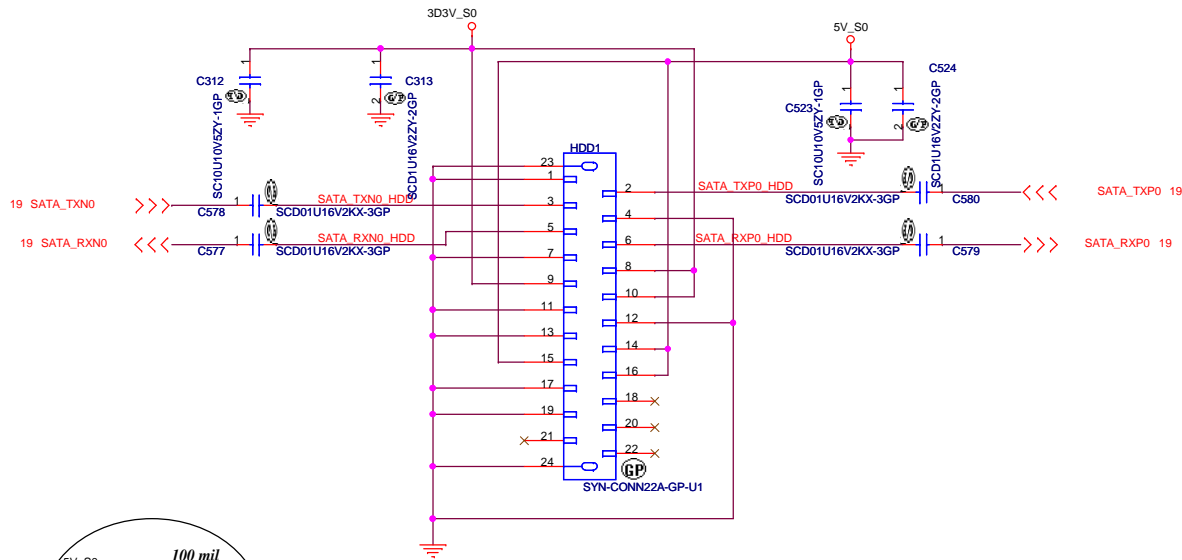
Author: X3

Title: MCP51(6)POWER

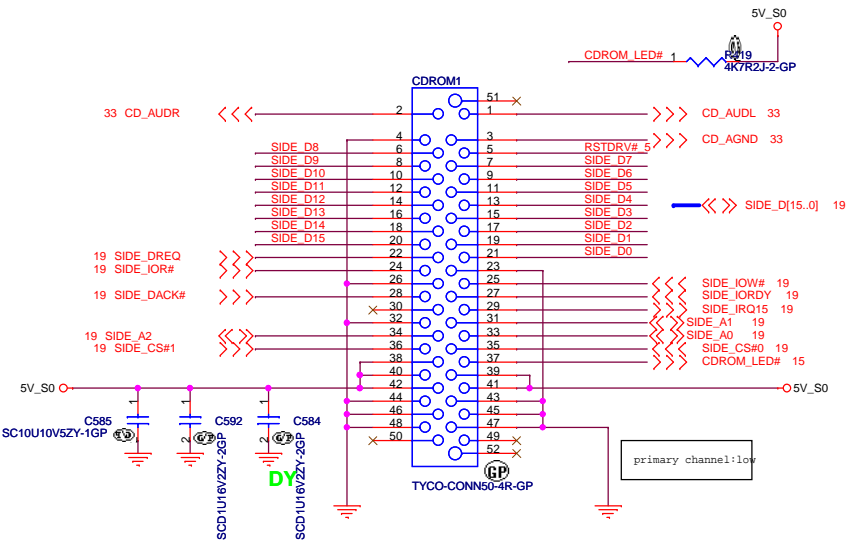
Variant Names:



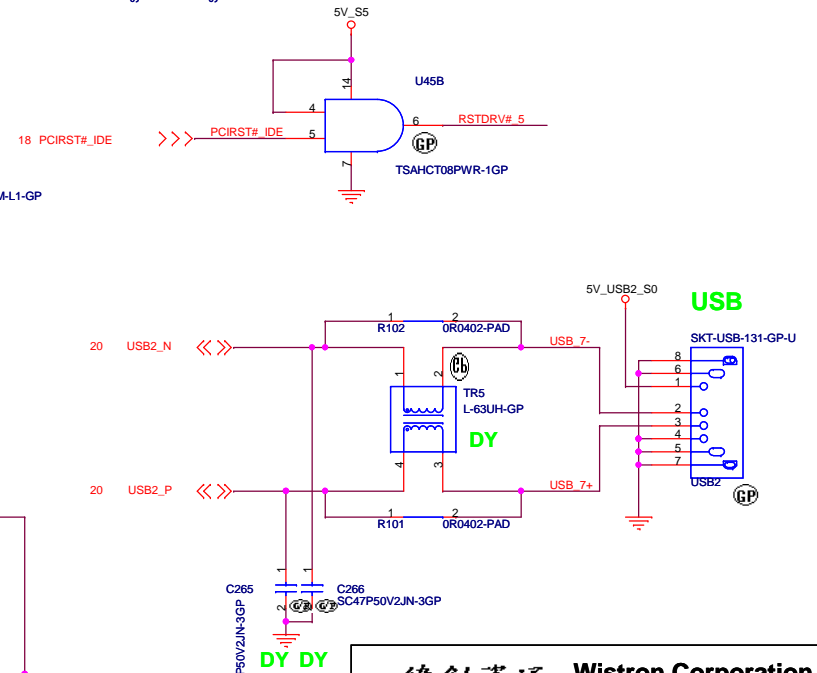
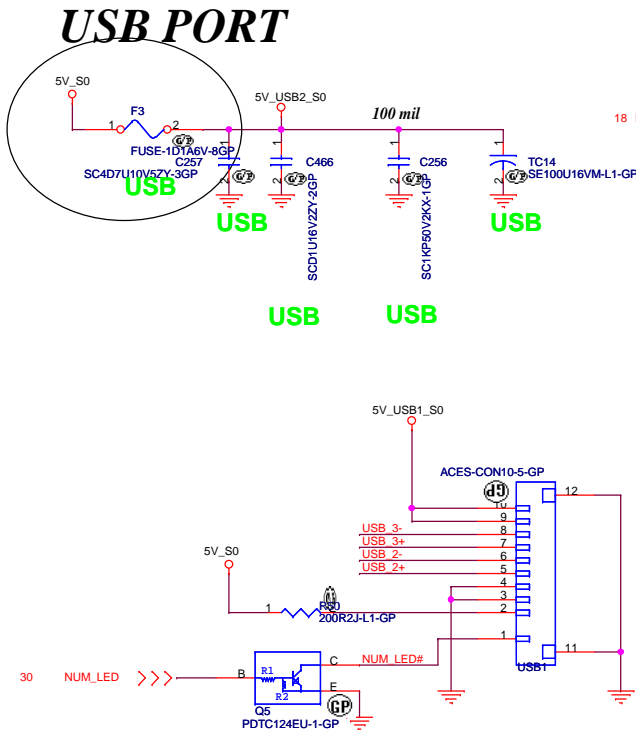
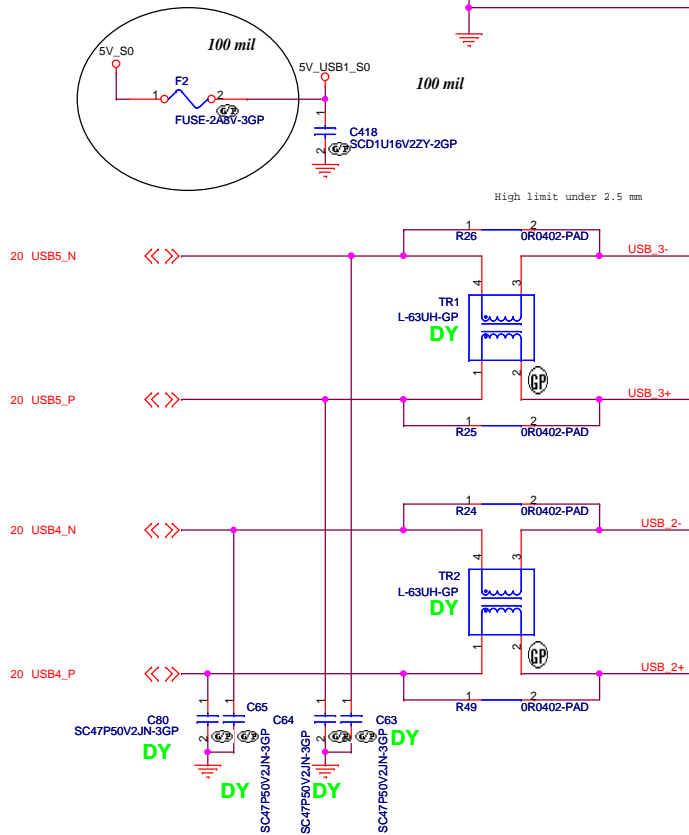
SATA HD Connector



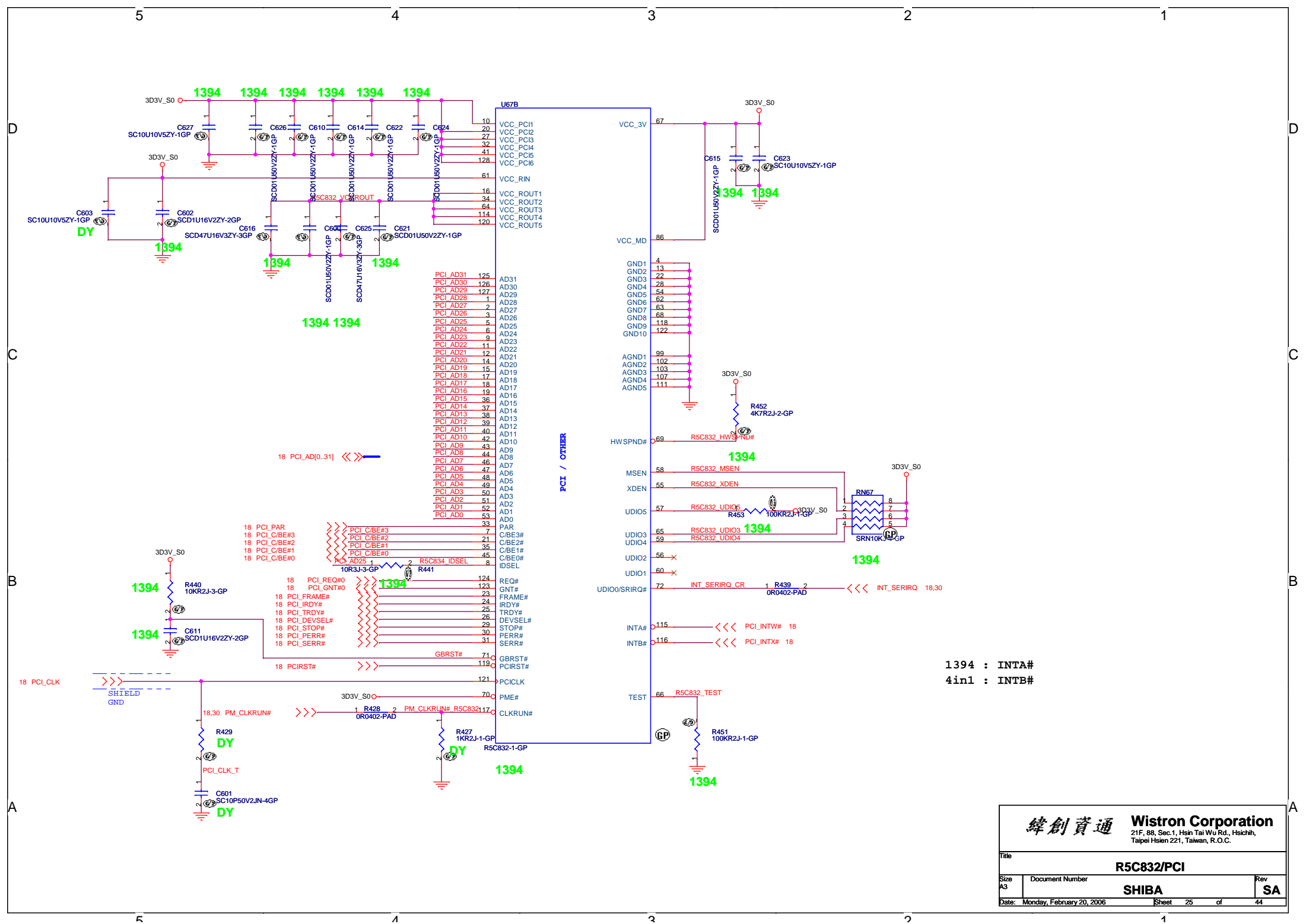
CD-ROM CONNECTOR



USB PORT

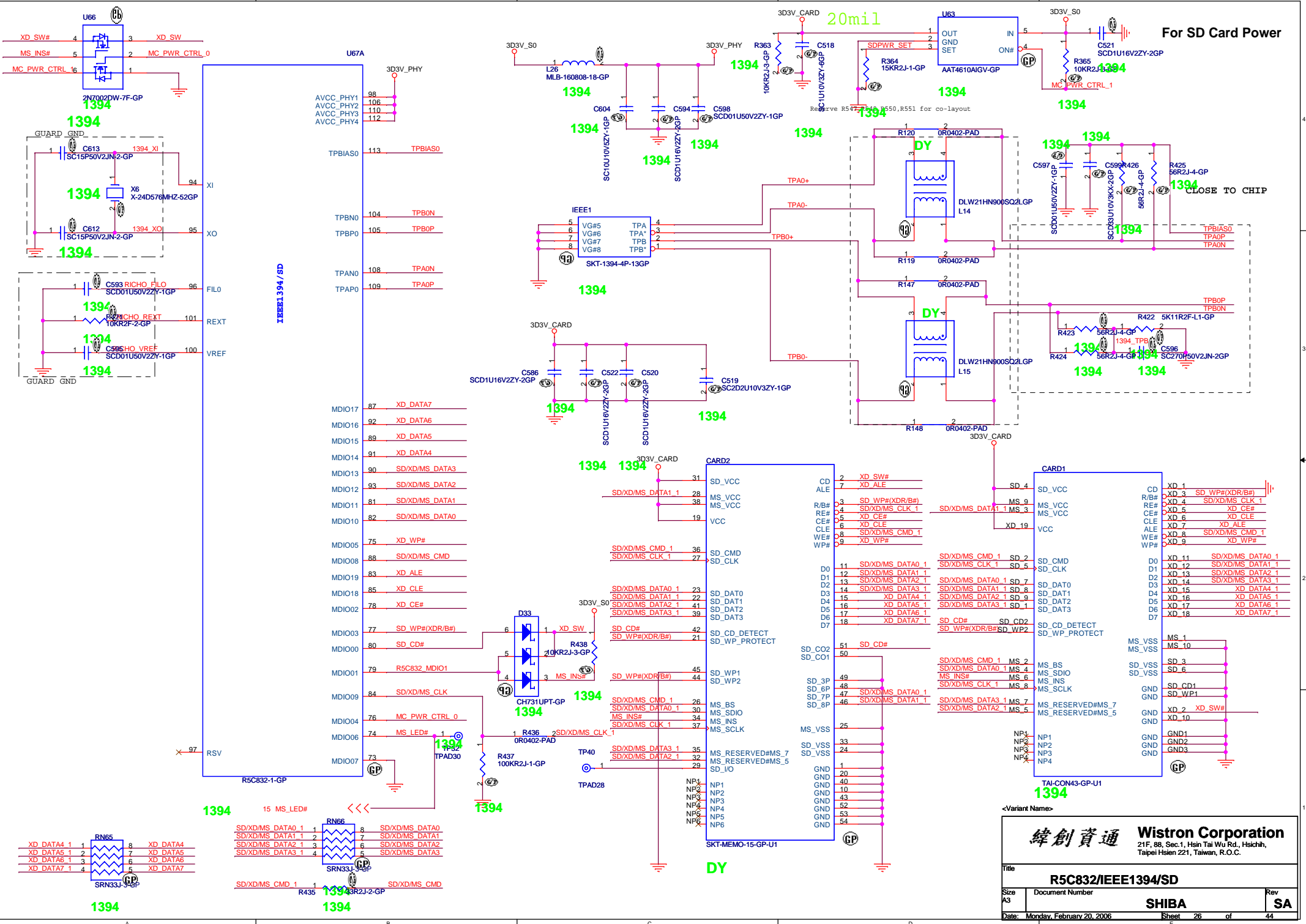


Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HD/CDROM	
Size A3	Document Number SHIBA
Date: Saturday, March 04, 2006	Sheet 24 of 44
	Rev SA



1394 : INTA#
 4in1 : INTB#

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
R5C832/PCI	
Size	Document Number
A3	SHIBA
Date:	Rev
Monday, February 20, 2006	SA
Sheet	of
25	44



For SD Card Power

CLOSE TO CHIP

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 Taipei Hsien 221, Taiwan, R.O.C.

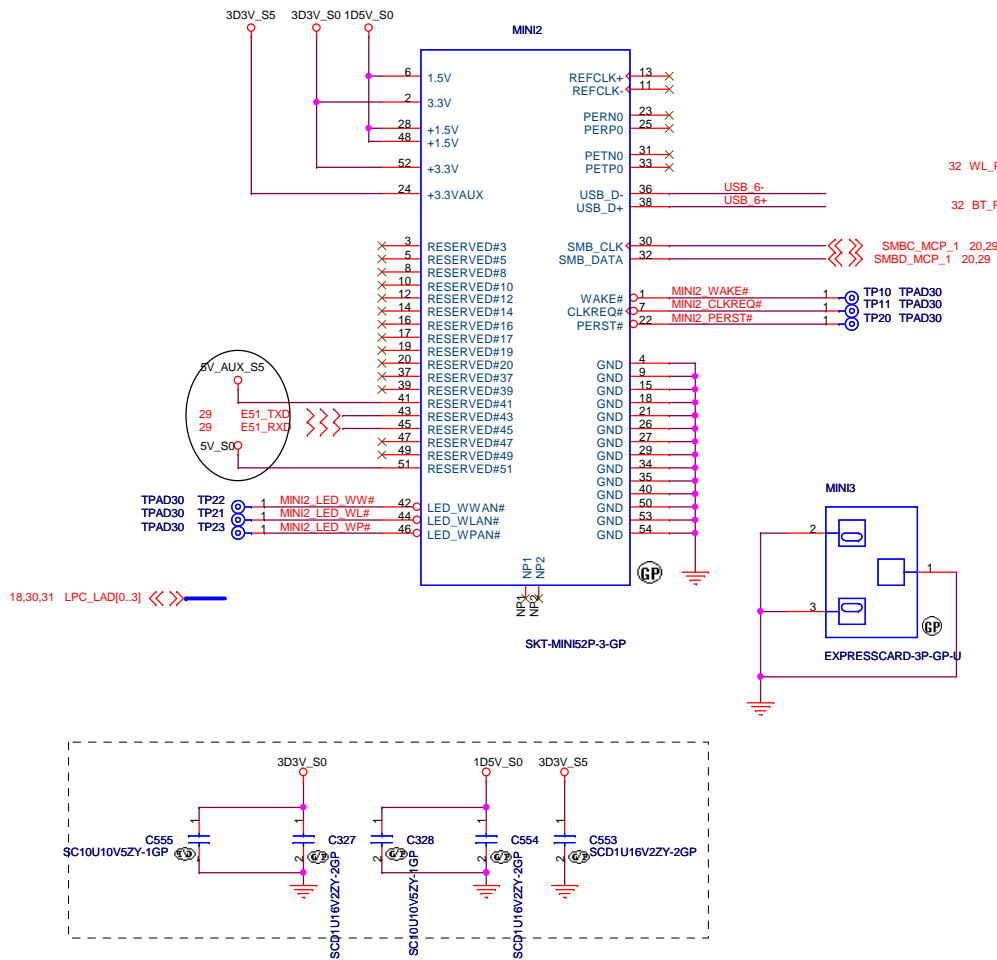
Title: **R5C832/IEEE1394/SD**

Size: A3 Document Number: **SHIBA** Rev: **SA**

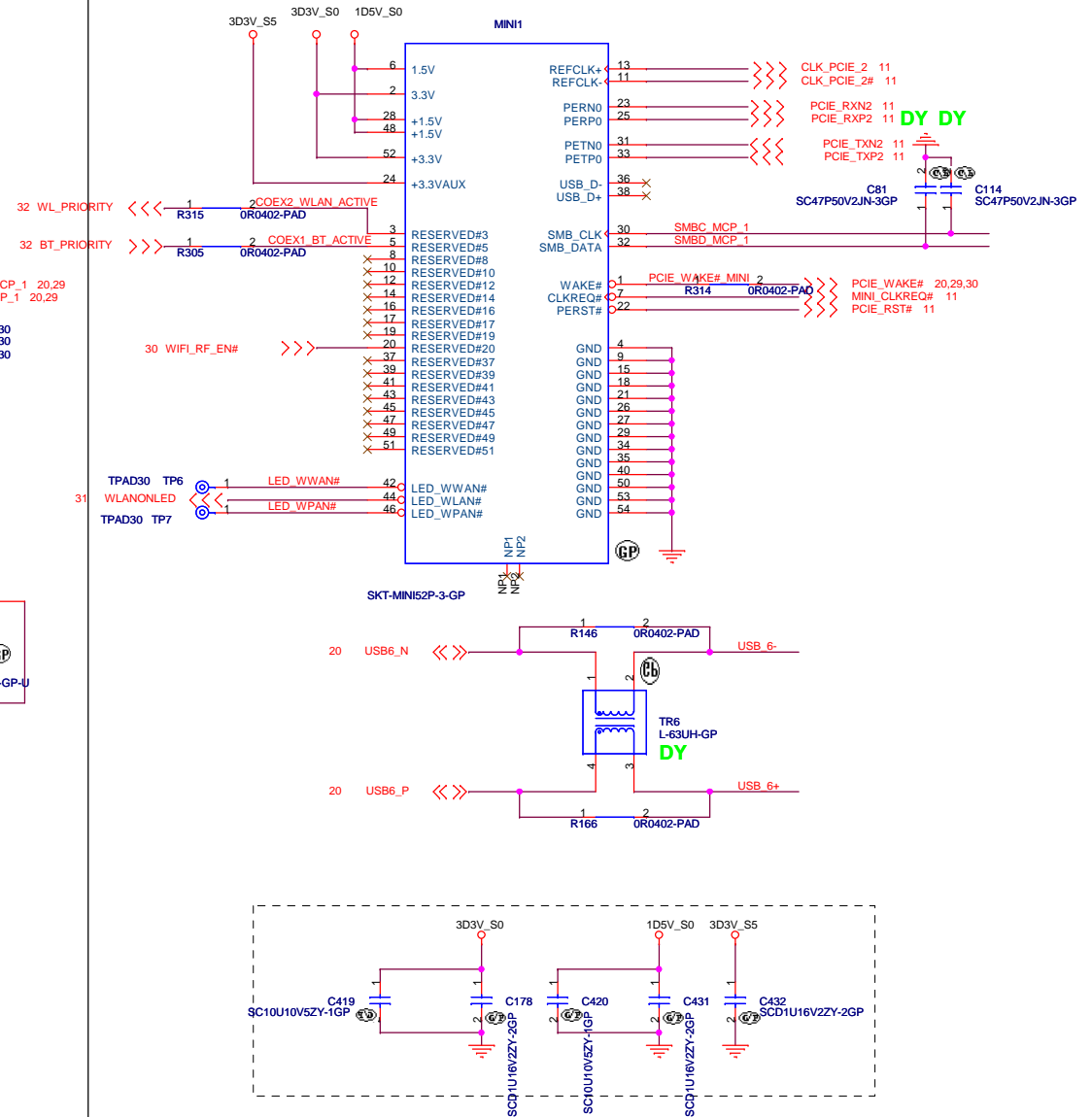
Date: Monday, February 20, 2006 Sheet 26 of 44

Mini Card Connector

Mini Card Connector 1



Mini Card Connector 2



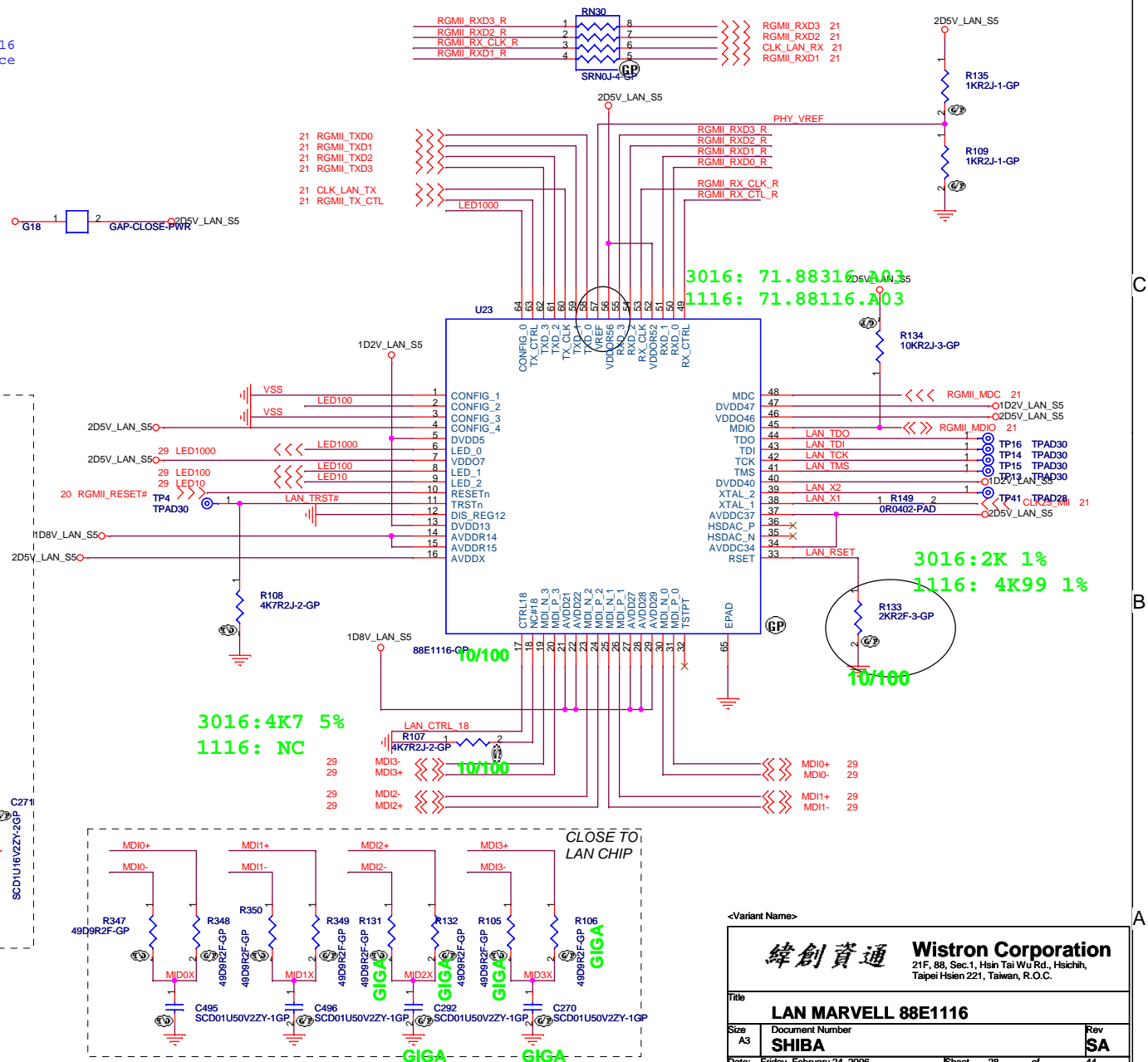
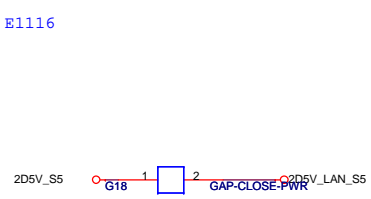
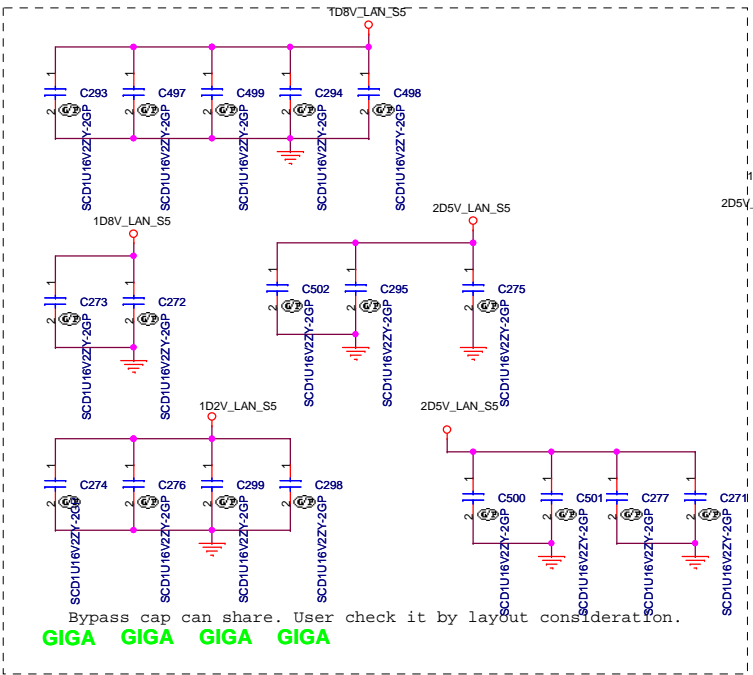
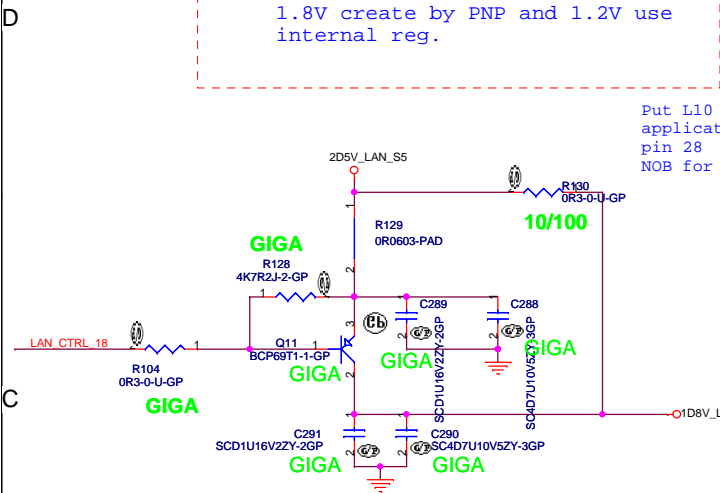
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MINI CARD CONN.			
Size: A3	Document Number: SHIBA	Rev: SA	
Date: Thursday, February 23, 2006 Sheet 27 of 44			

Hardware Configuration: See config_0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

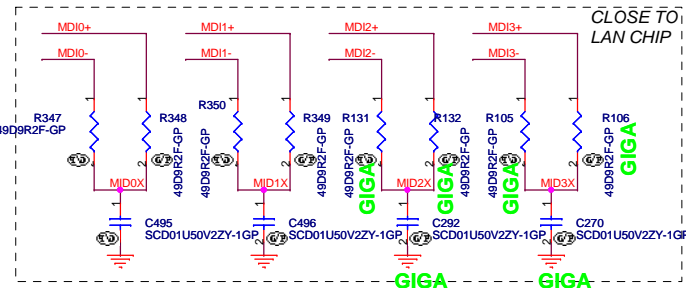
Put L10 for E3016 application since pin 28 NOB for E1116



3016: 4K7 5%
1116: NC

3016: 71.88316.A03
1116: 71.88116.A03

3016: 2K 1%
1116: 4K99 1%

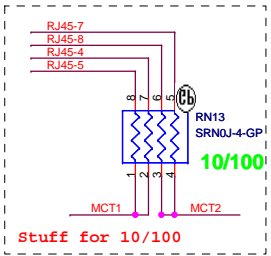
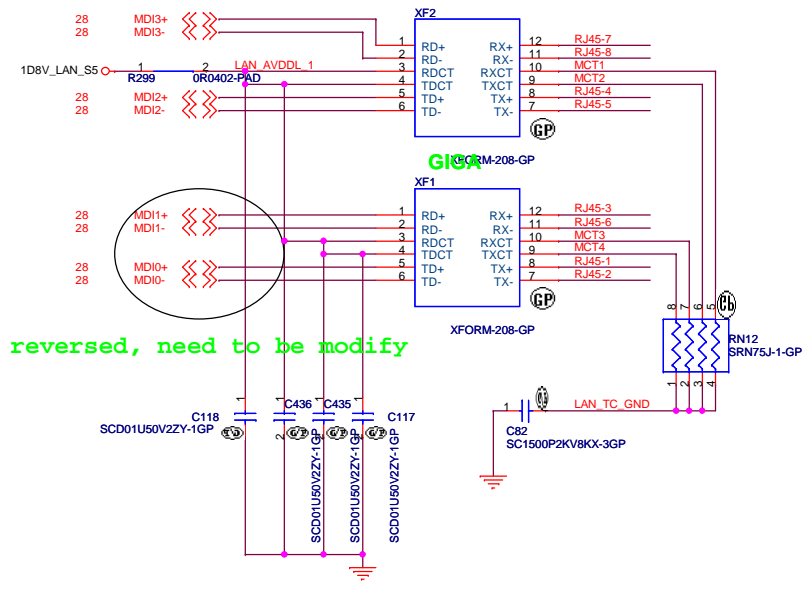


<Variant Name>

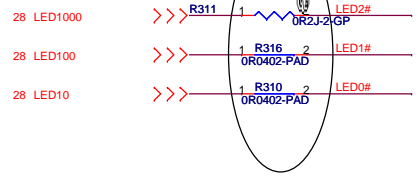
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN MARVELL 88E1116**

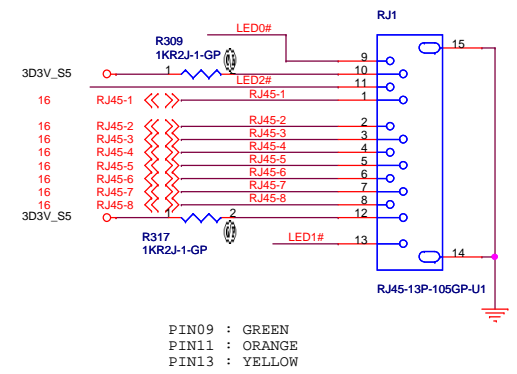
Size A3	Document Number: SHIBA	Rev: SA
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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

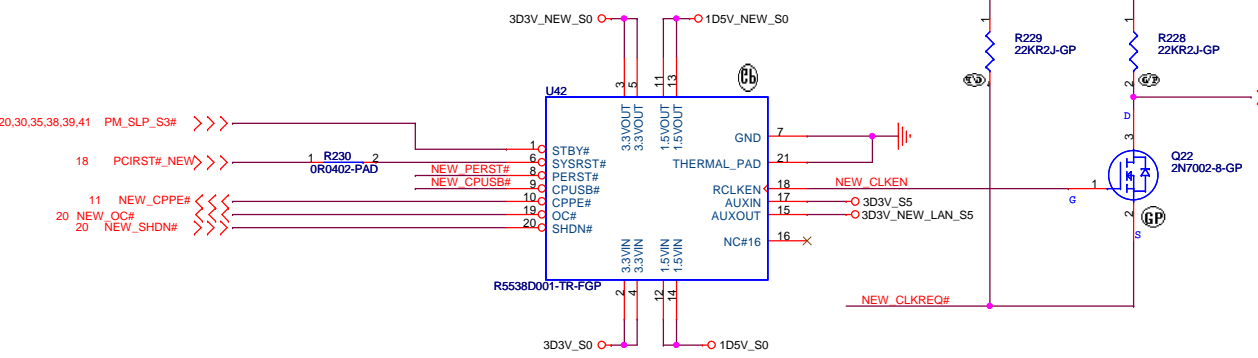
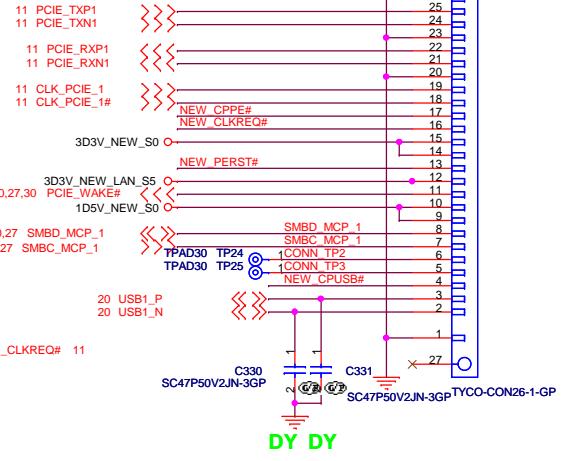
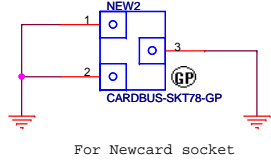
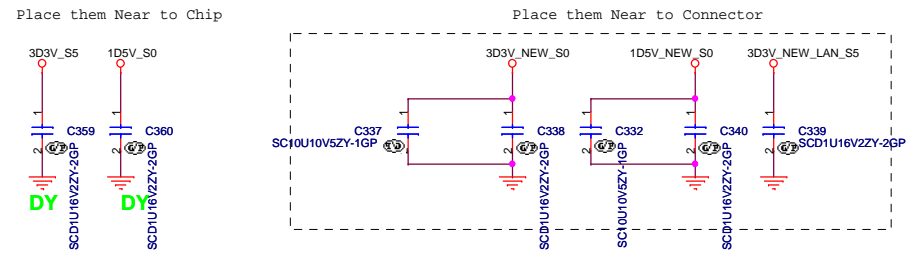


GREEN: LINK 10/100 Mbps
YELLOW: TX/RX ACTIVITY
ORANGE: LINK 1000Mbps

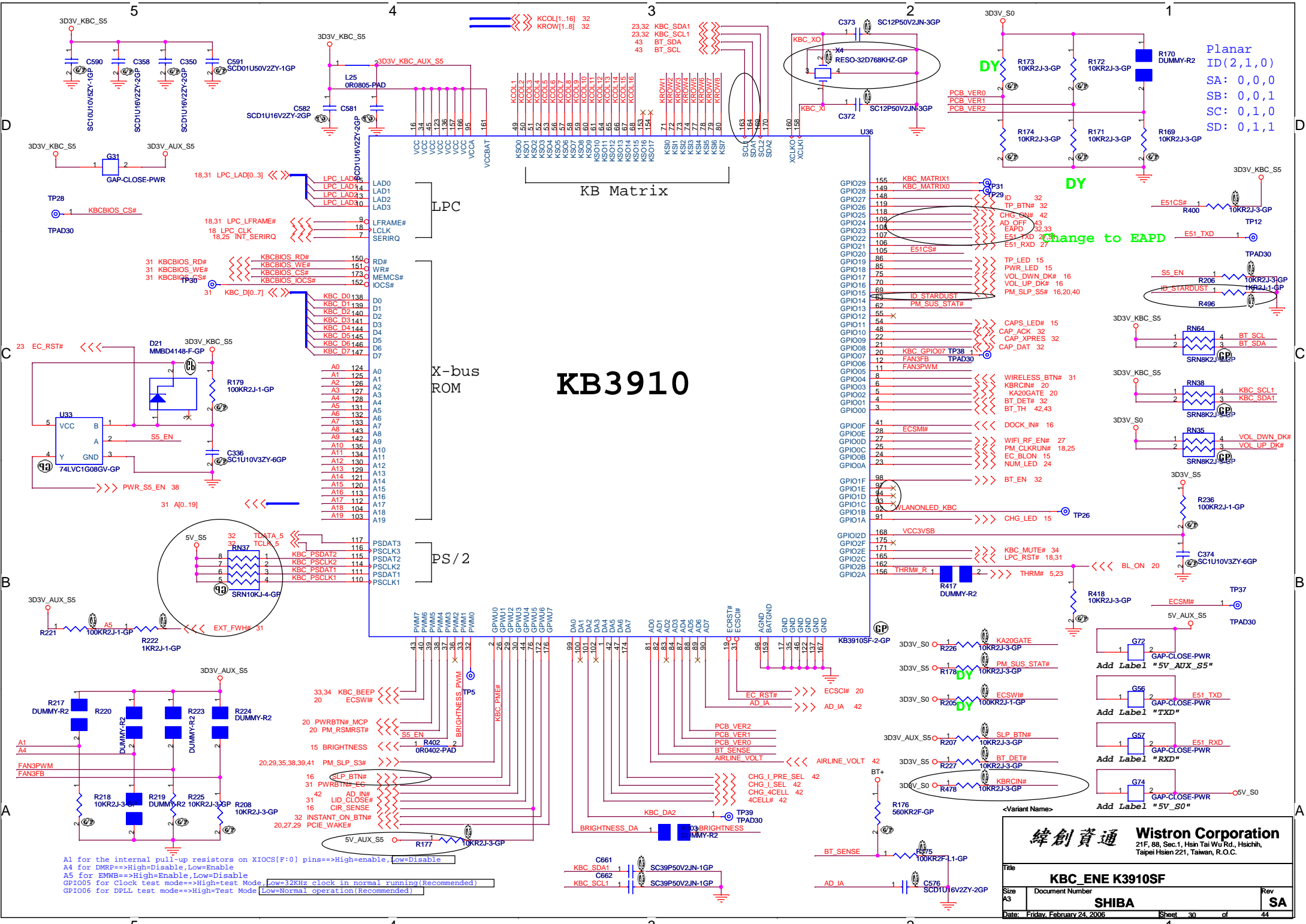


PIN09 : GREEN
 PIN11 : ORANGE
 PIN13 : YELLOW

NEWCARD Connector



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New Card			
Size A3	Document Number SHIBA	Rev SA	
Date: Monday, February 20, 2006		Sheet 29	of 44



Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1

KB3910

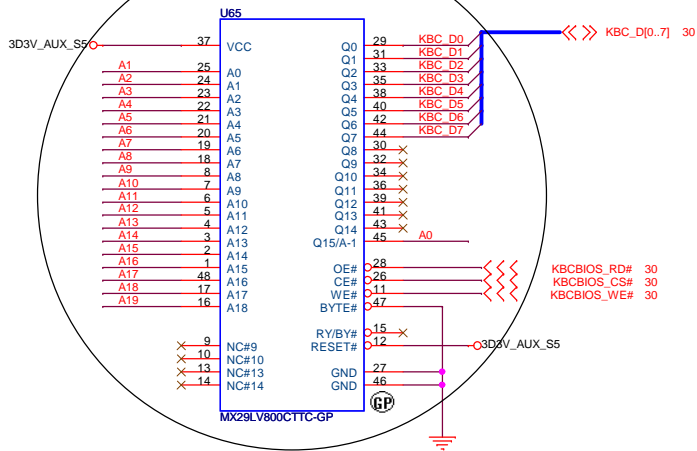
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC_ENE K3910SF**

Size: A3	Document Number: SHIBA	Rev: SA
Date: Friday, February 24, 2006	Sheet: 30	of 44

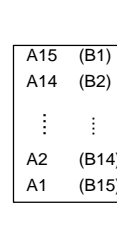
A1 for the internal pull-up resistors on XIOCS[!F:0] pins==>High=enable, Low=Disable
 A4 for DMRP==>High=Disable, Low=Enable
 A5 for EMWB==>High=Enable, Low=Disable
 GPI005 for clock test mode==>High=test Mode, Low=32KHz clock in normal running(Recommended)
 GPI006 for DPLL test mode==>High=Test Mode [Low=Normal operation(Recommended)]

30 A[0..19]



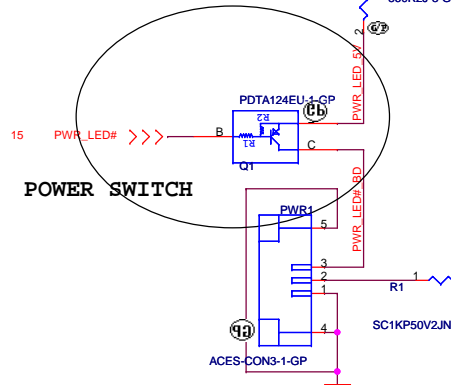
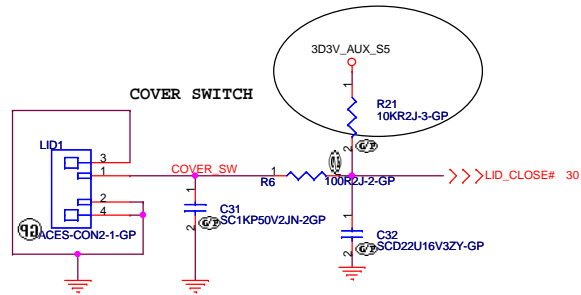
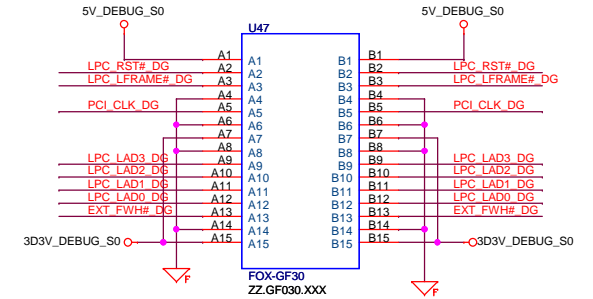
Change to MX29LV800CTTC
72.29800.0B9

TOP VIEW



(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



LPC_LAD[0..3] 18,30

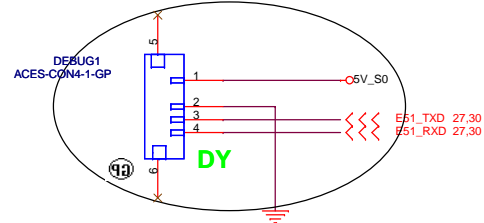
LPC_RST#

LPC_LFRAME#

PCI_CLK_GOLD

PWRBTN#_EC 30

DY

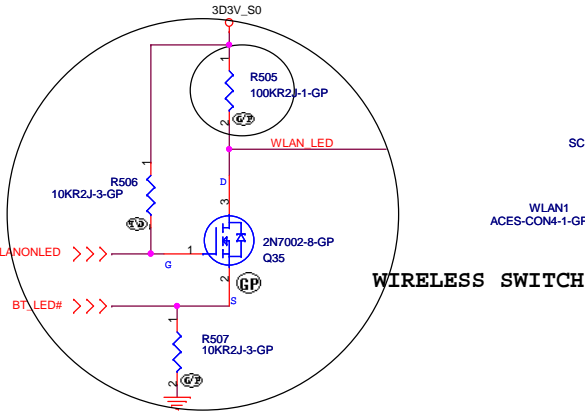


EXT_TXD 27,30

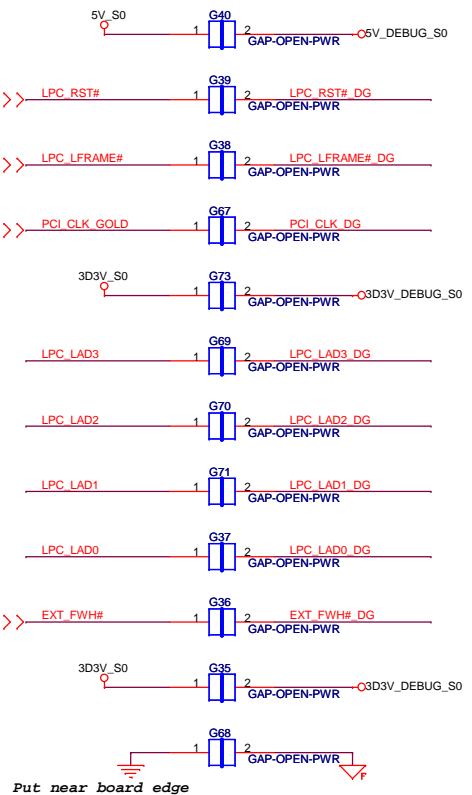
EXT_RXD 27,30

EXT_FWH#

DY



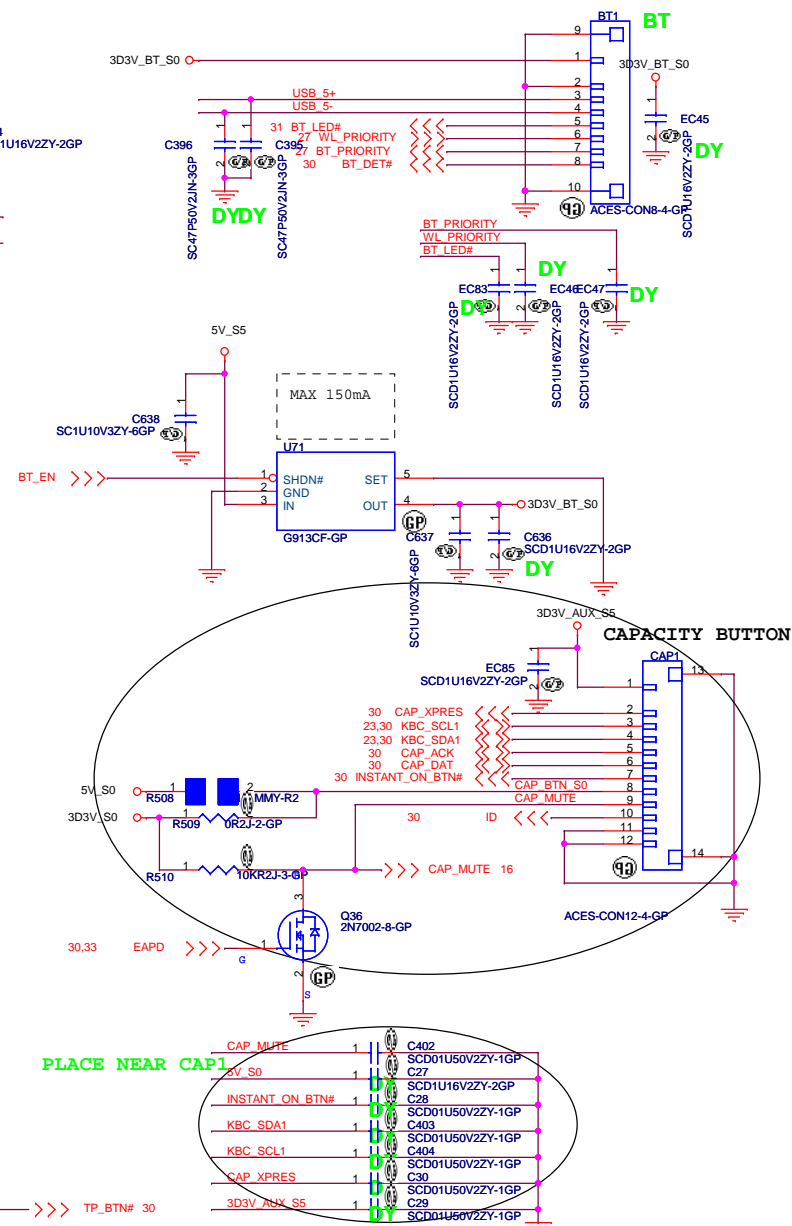
DY



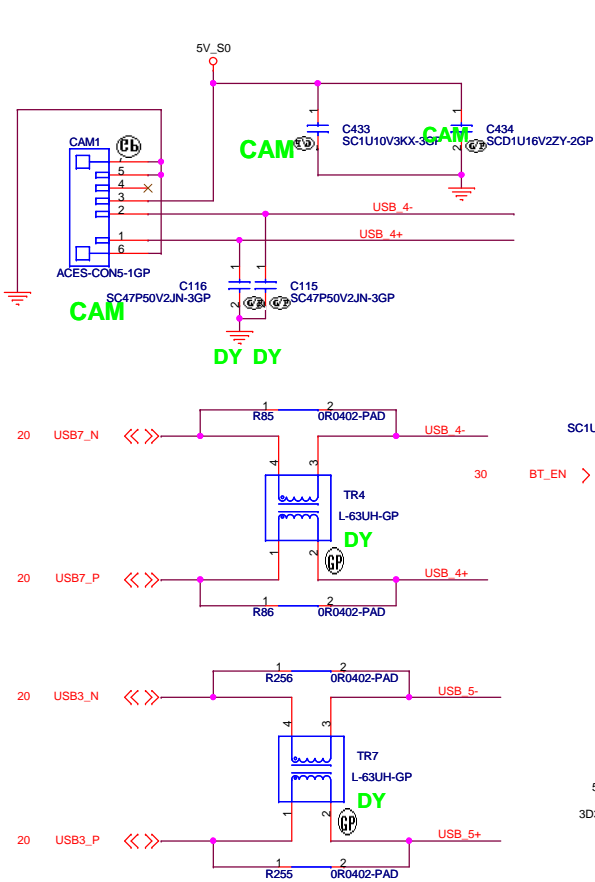
Put near board edge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
FLASH and Debug		
Title Size A3	Document Number SHIBA	Rev SA
Date: Wednesday, March 15, 2006		Sheet 31 of 44

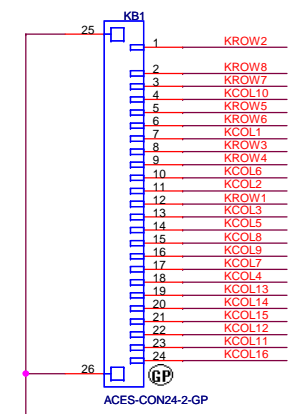
Blue thumb



CAMERA



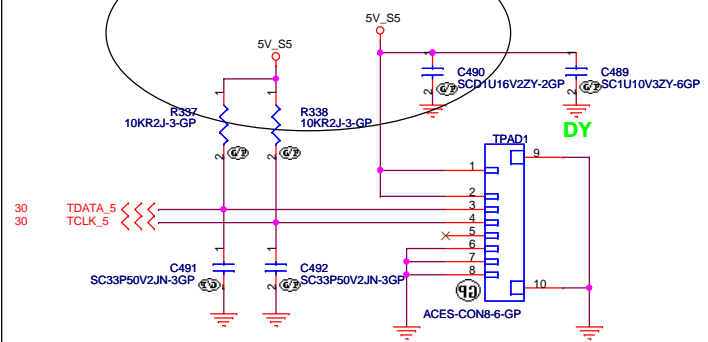
Internal KeyBoard Connector



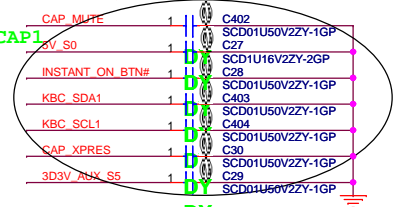
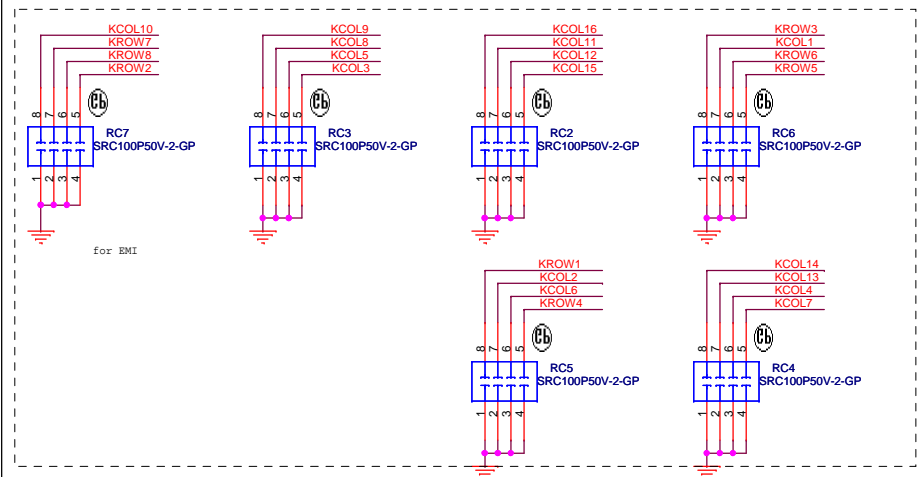
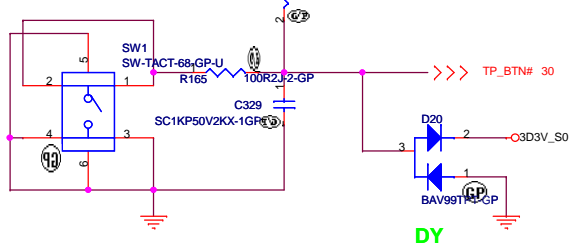
Keyboard matrix (from vendor)

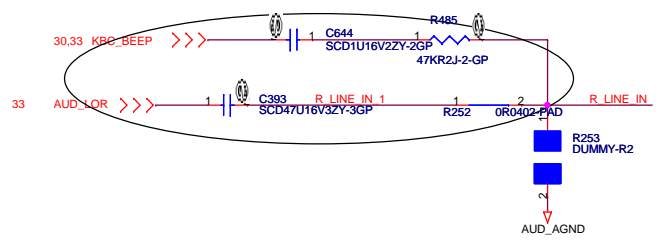
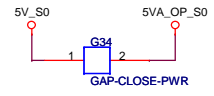
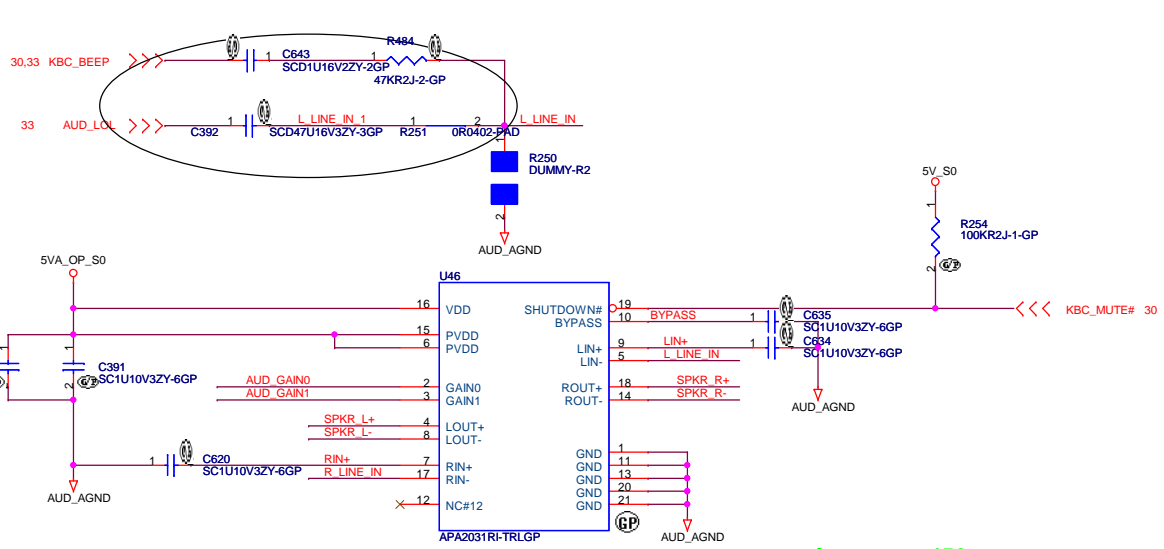
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

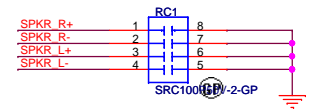
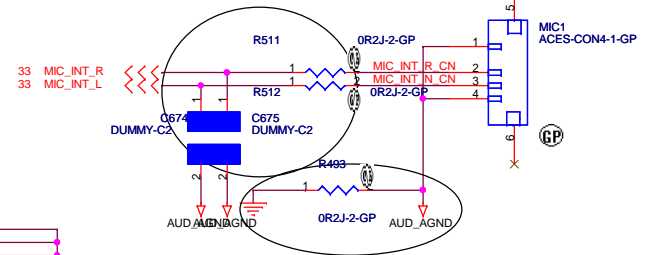


TOUCH-PAD SWITCH

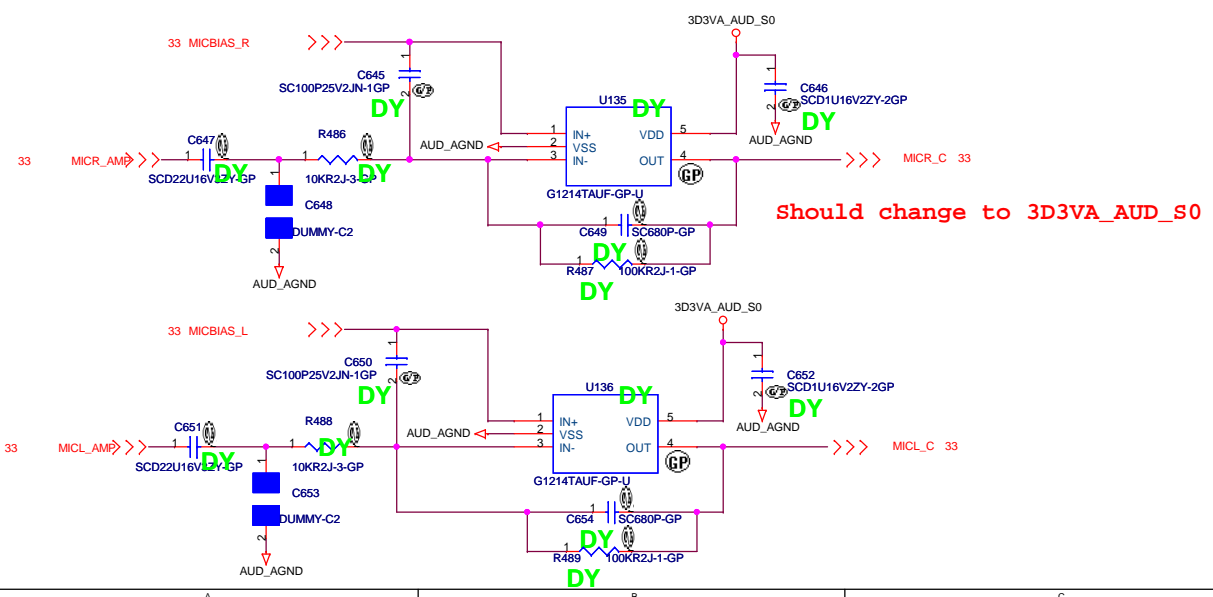
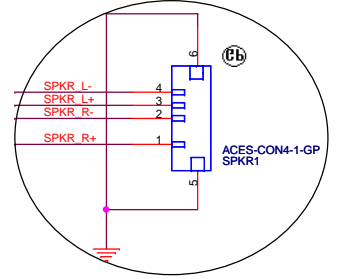




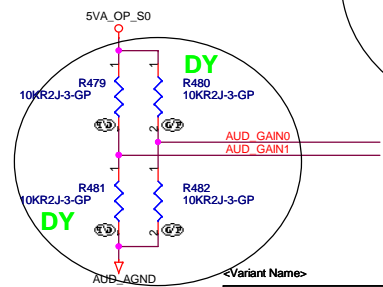
change to 470P



Speaker

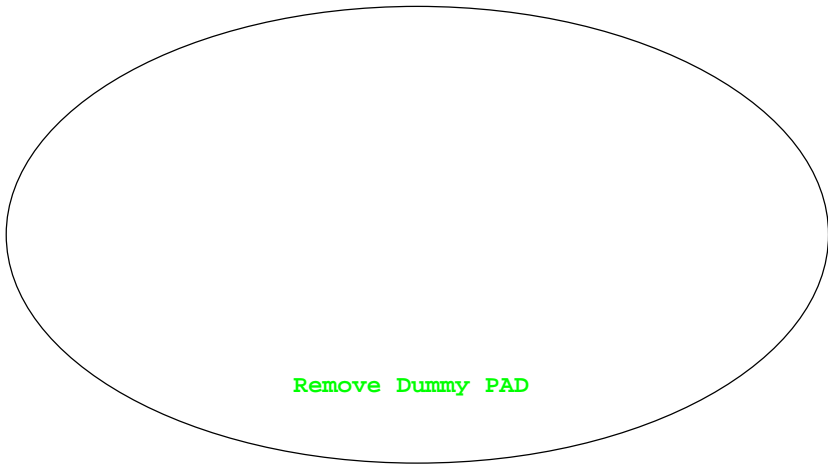


Should change to 3D3VA_AUD_S0

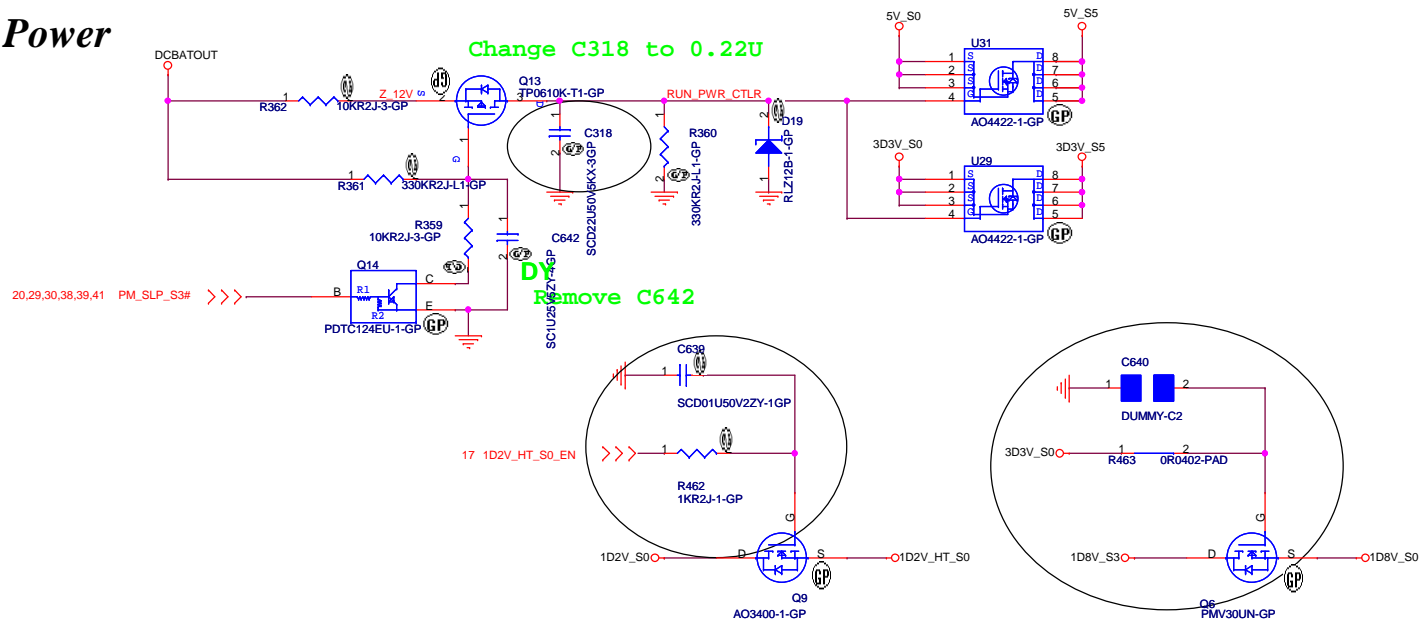


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AUDIO AMP APA3031			
Size A3	Document Number SHIBA	Rev SA	
Date: Friday, February 24, 2006	Sheet 34	of	44

Suspend Power



Run Power



CPU_VCORE

VID=1.20V(25W)/1.35V(35W)

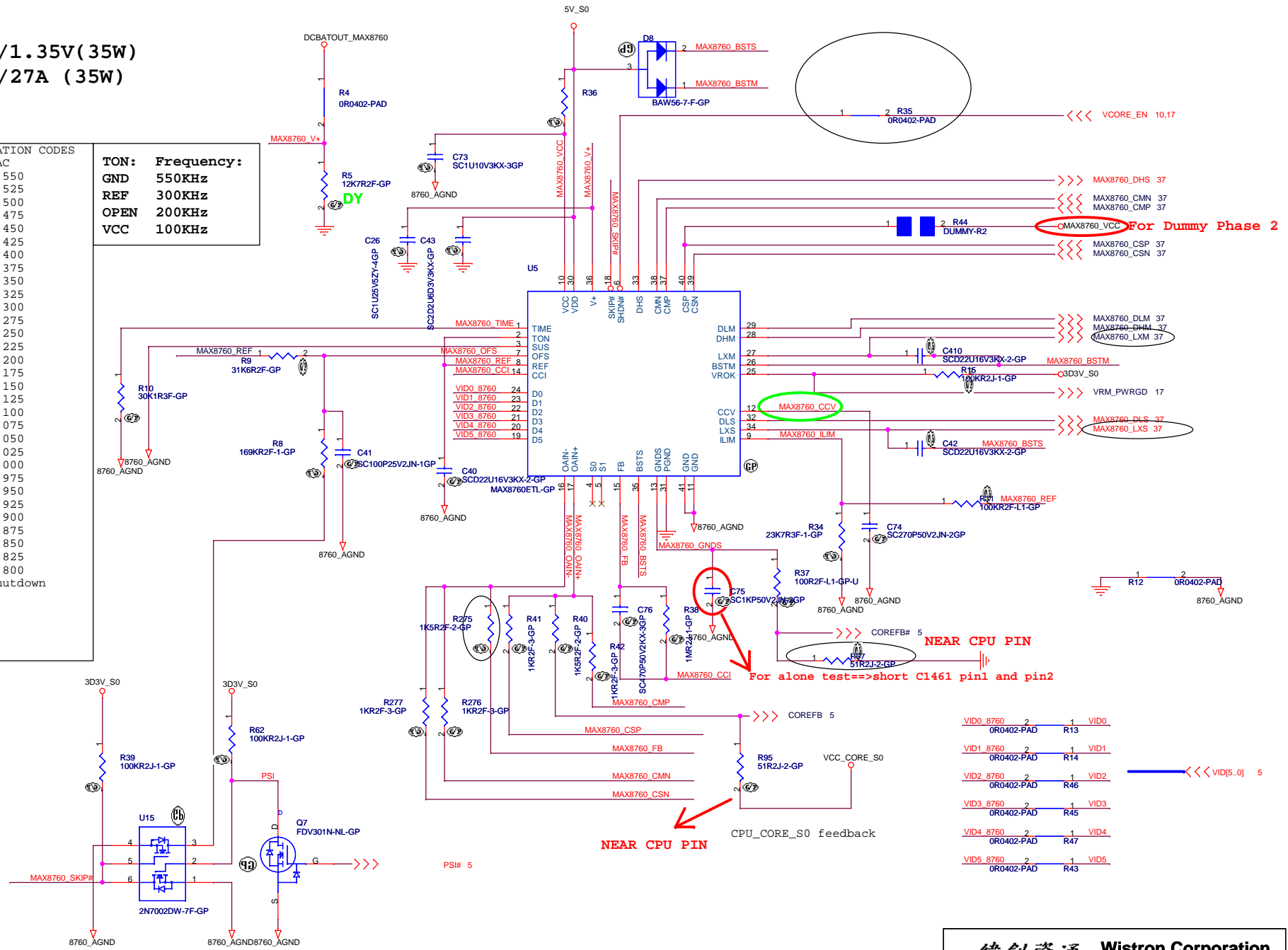
Iomax=21A(25W)/27A(35W)

OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

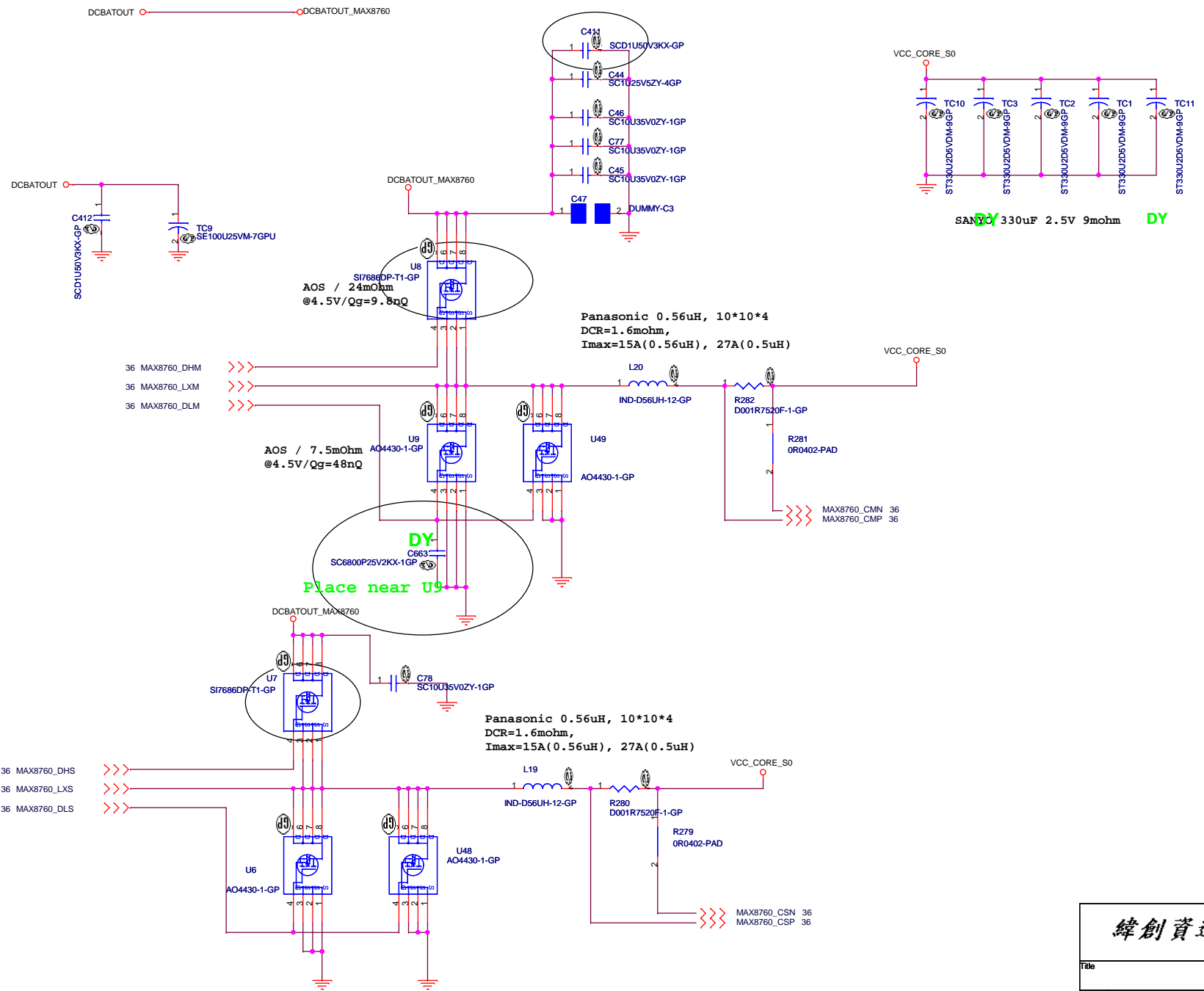
TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz



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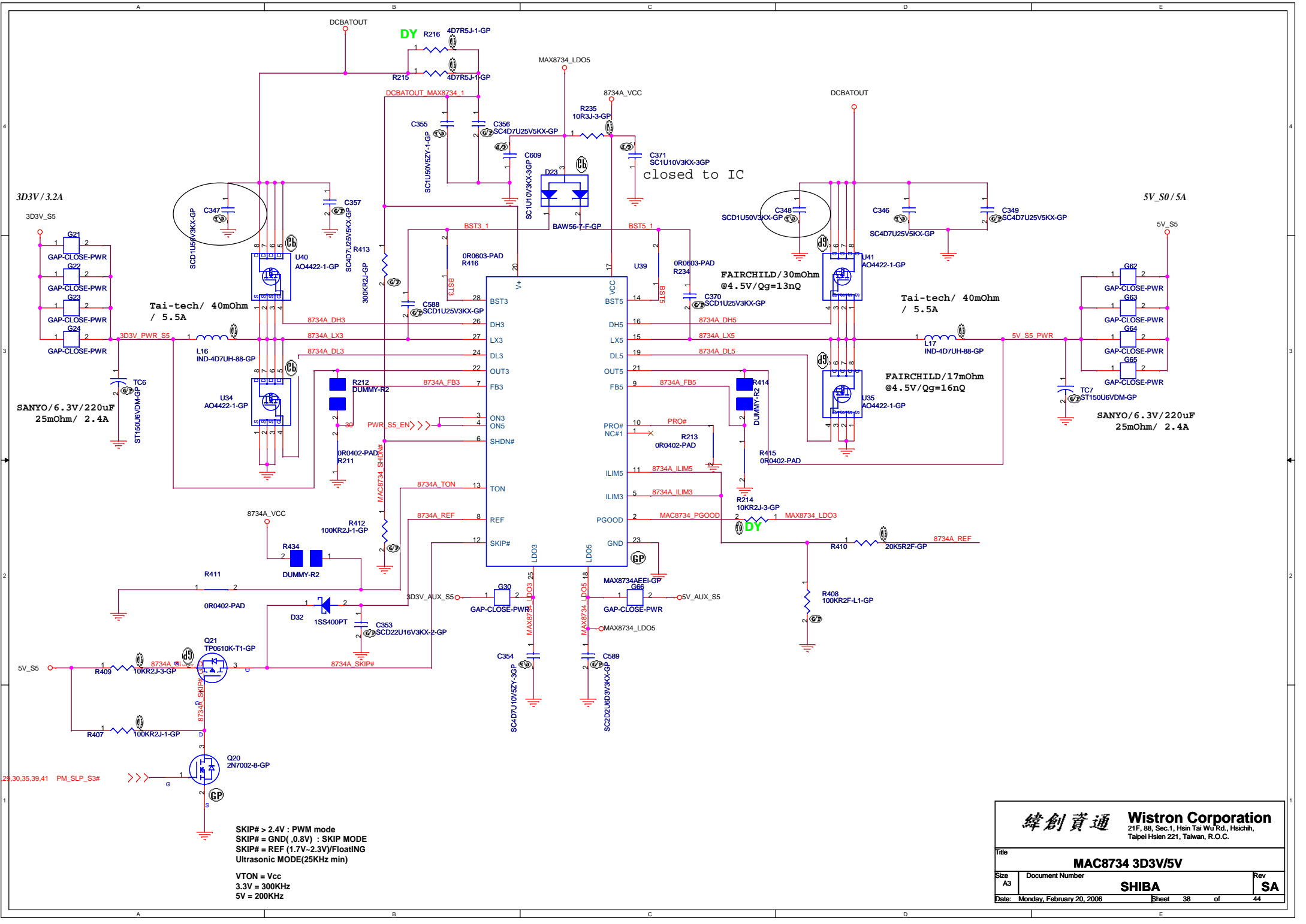
Title: **CPU CORE MAX8760(1/2)**

Size A3	Document Number	Rev SA
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Date: Wednesday, February 22, 2006	Sheet 36 of 44	



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CPU CORE MAX8760(2/2)			
File	Document Number		
Size A3	SHIBA		Rev SA
Date: Wednesday, February 22, 2006	Sheet 37	of 44	

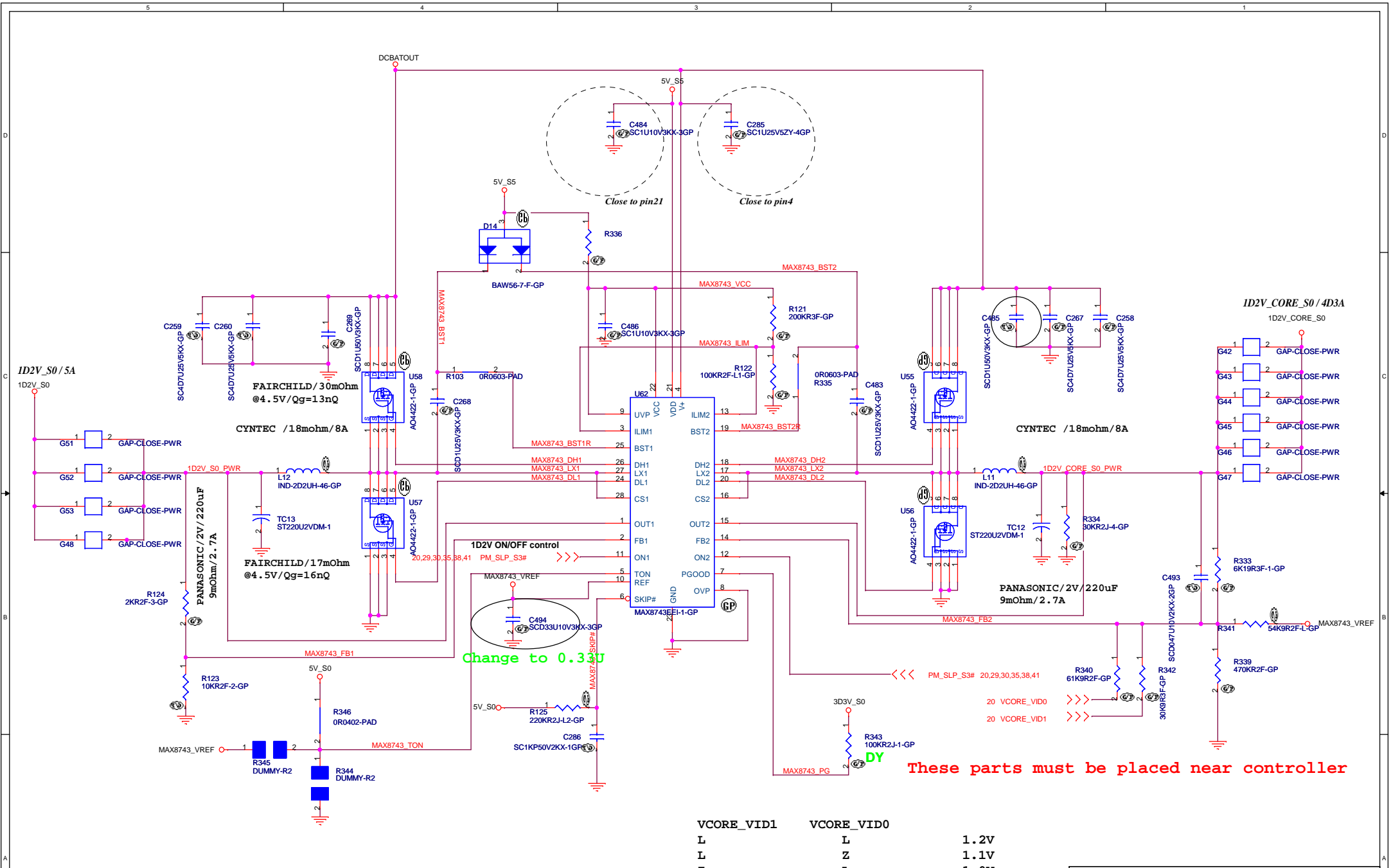
(Power Team)



SKIP# > 2.4V : PWM mode
 SKIP# = GND(.0.8V) : SKIP MODE
 SKIP# = REF (1.7V~2.3V)/FloatING
 Ultrasonic MODE(25KHz min)

 VTON = Vcc
 3.3V = 300KHz
 5V = 200KHz

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MAC8734 3D3V/5V	
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Change to 0.33u

These parts must be placed near controller

VCORE_VID1		VCORE_VID0	
L		L	1.2V
L		Z	1.1V
Z		L	1.0V
Z		Z	Reserved

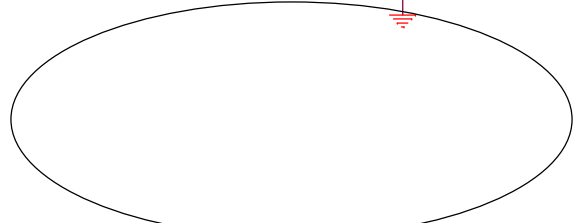
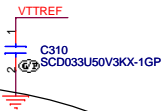
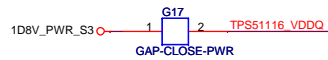
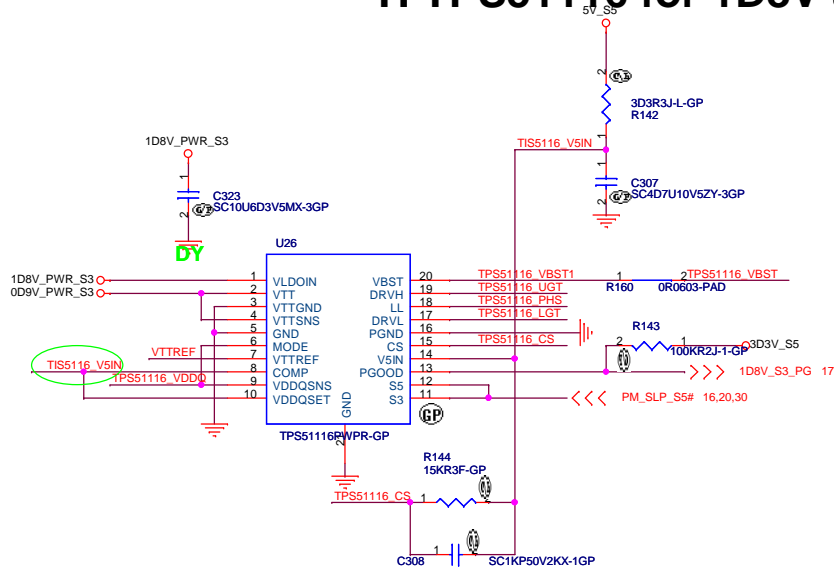
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8743 1D2V/1D2V_CORE**

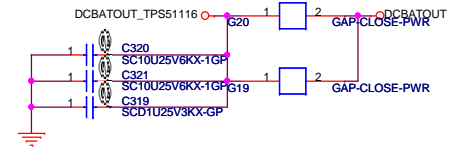
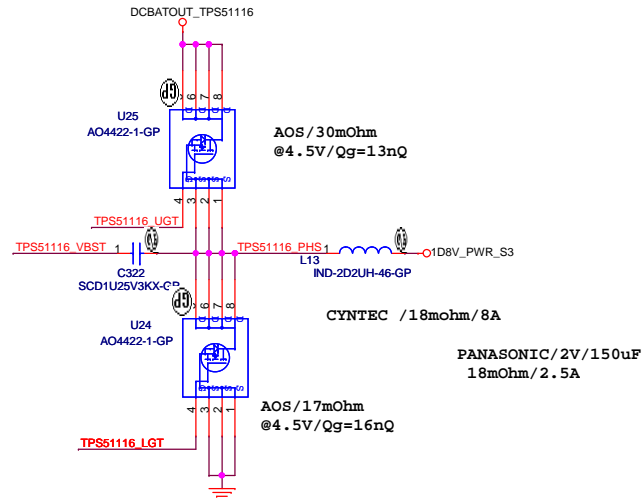
Size A3	Document Number	Rev SA
SHIBA		

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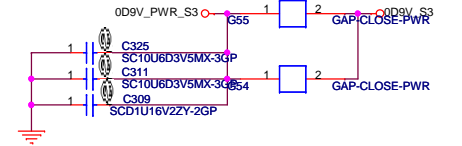
TI TPS51116 for 1D8V and 0D9V



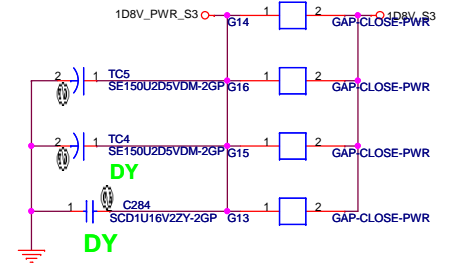
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



0D9V / 2A , OCP > 3A



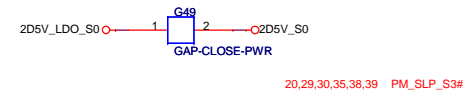
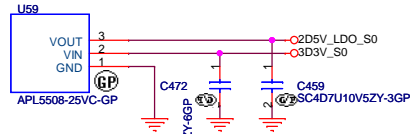
1D8V / 5A , OCP > 12A



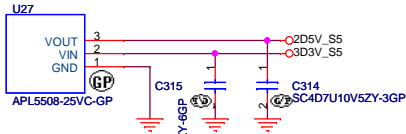
1D8V / 5A , OCP > 12A

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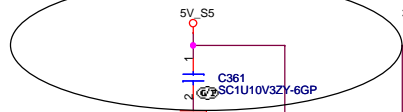
Title			TPS51116 1D8V/0D9V		
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G50



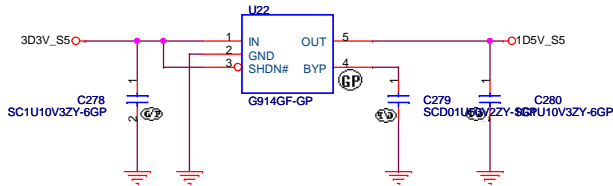
Change to S5 power plane



$$V_o(\text{cal.}) = 1.512V$$

$$V_o = 0.8 * (1 + (R1/R2))$$

KEMET
100uF, 4V, B2 Size, NTD:5.615
Iripple=1.1A, ESR=70mohm



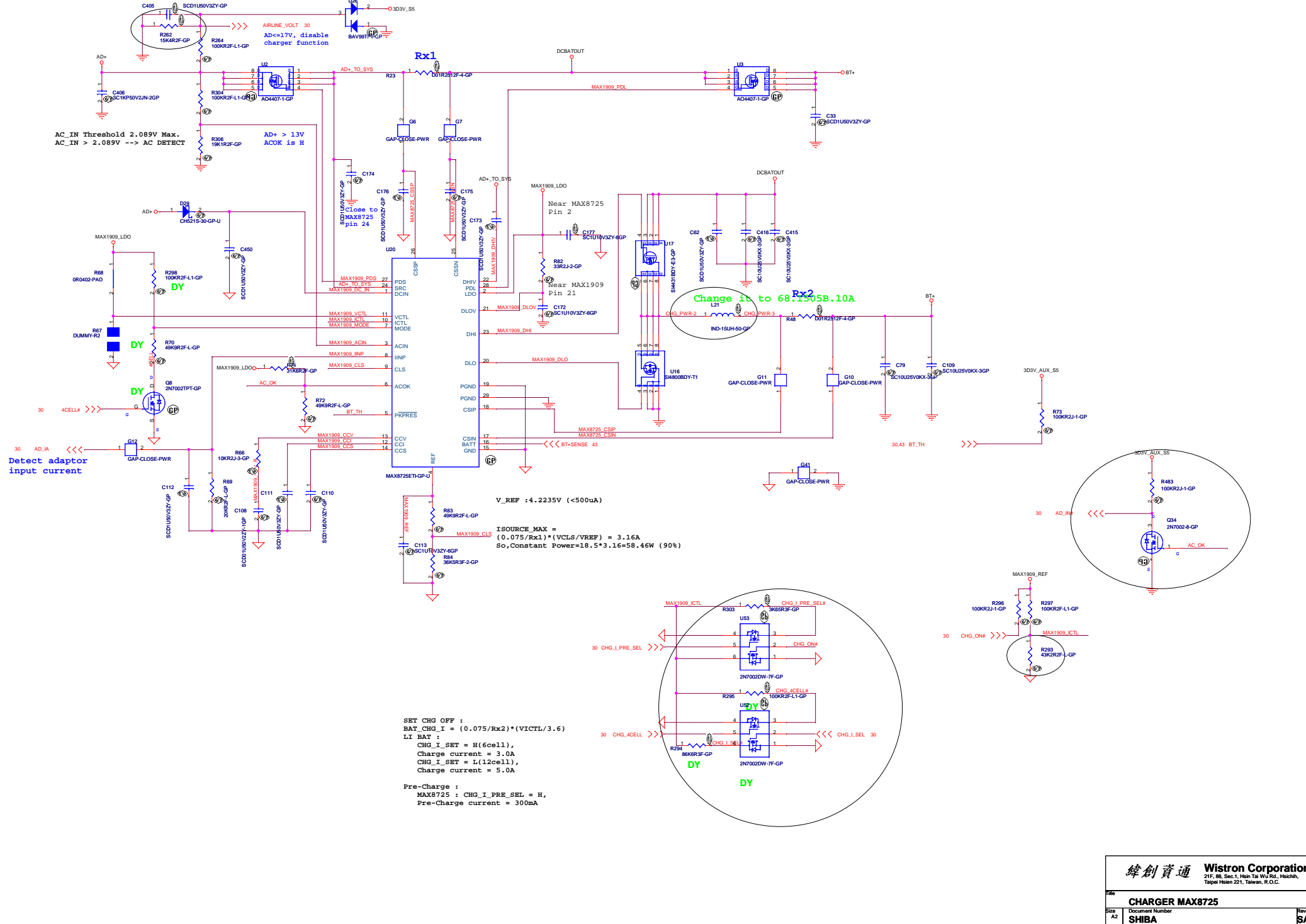
2nd source : 74.00916.D3F

1D5V_S0
Iomax=1.3A
OCP=2.6A

Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

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Title		
1D5V/2D5V/3D3V/5V_AUX		
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AC_IN Threshold 2.089V Max.
AC_IN > 2.089V -> AC DETECT

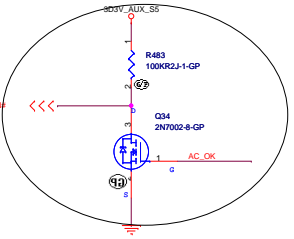
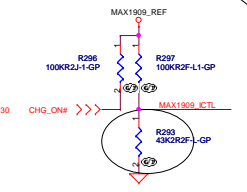
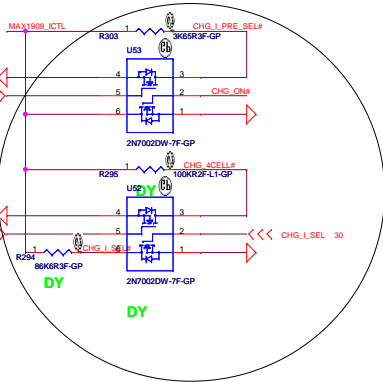
AD+ > 13V
ACOK is H

Detect adaptor
input current

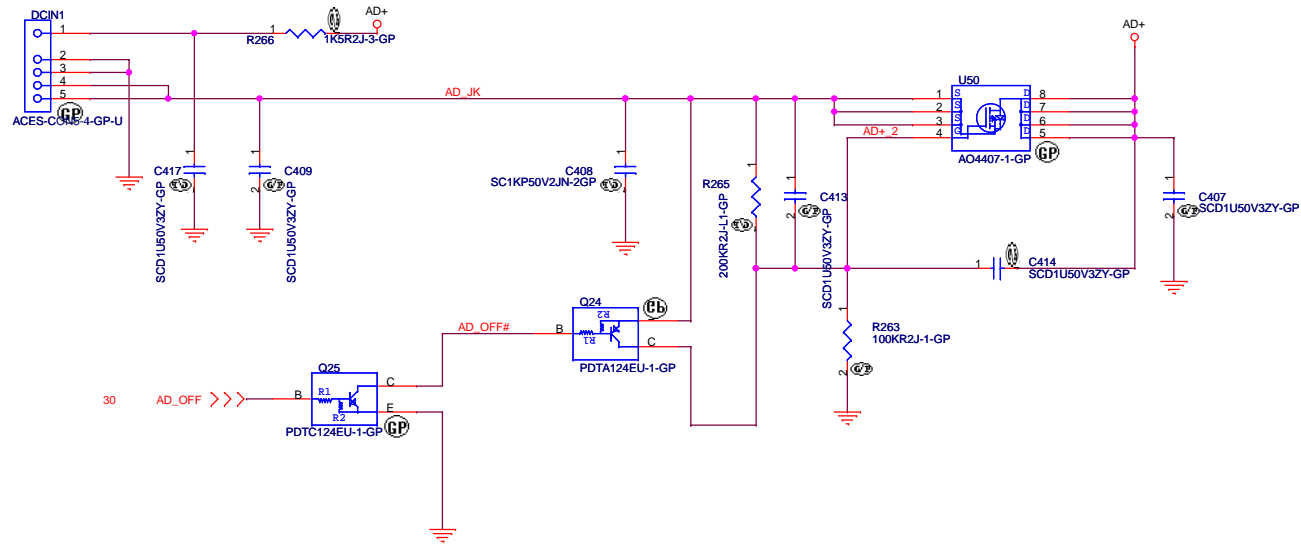
V_REF : 4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 3.16A
So, Constant Power=18.5*3.16=58.46W (90%)

SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A

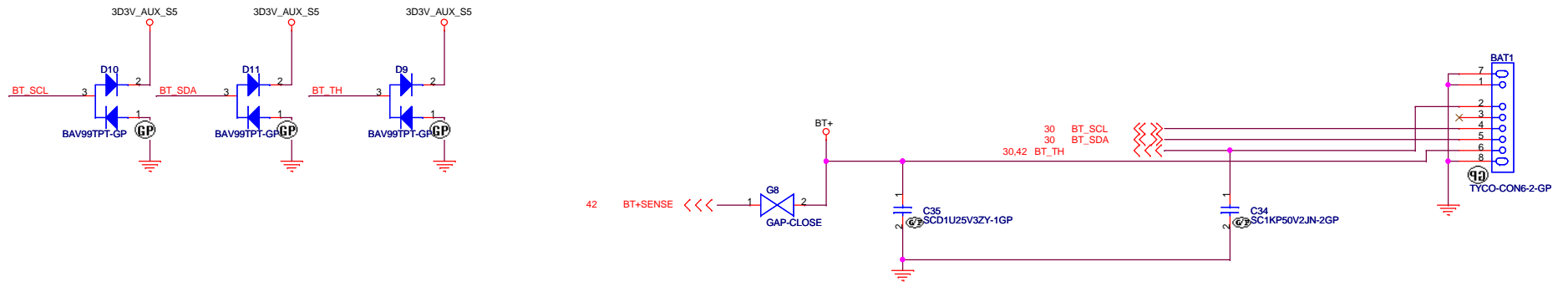
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA



Adaptor in to generate DCBATOUT



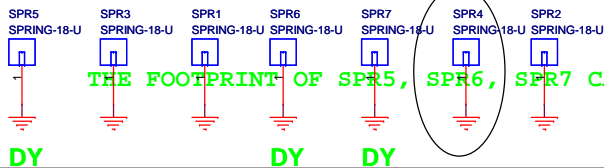
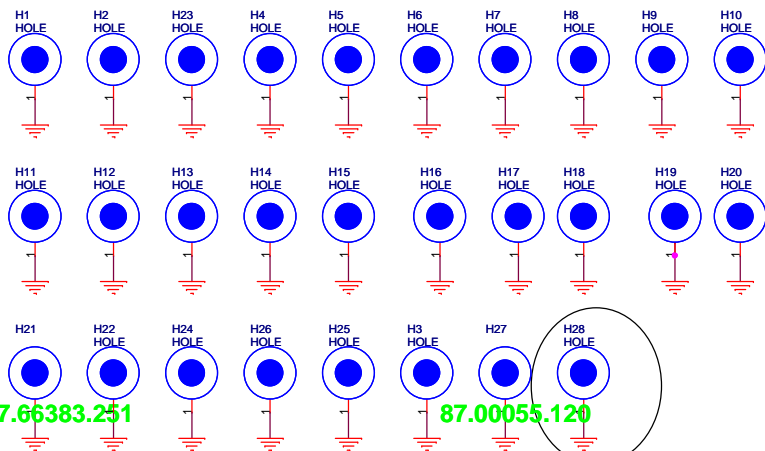
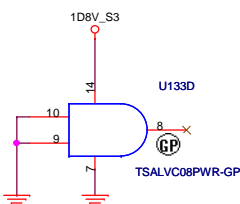
BATTERY CONNECTOR



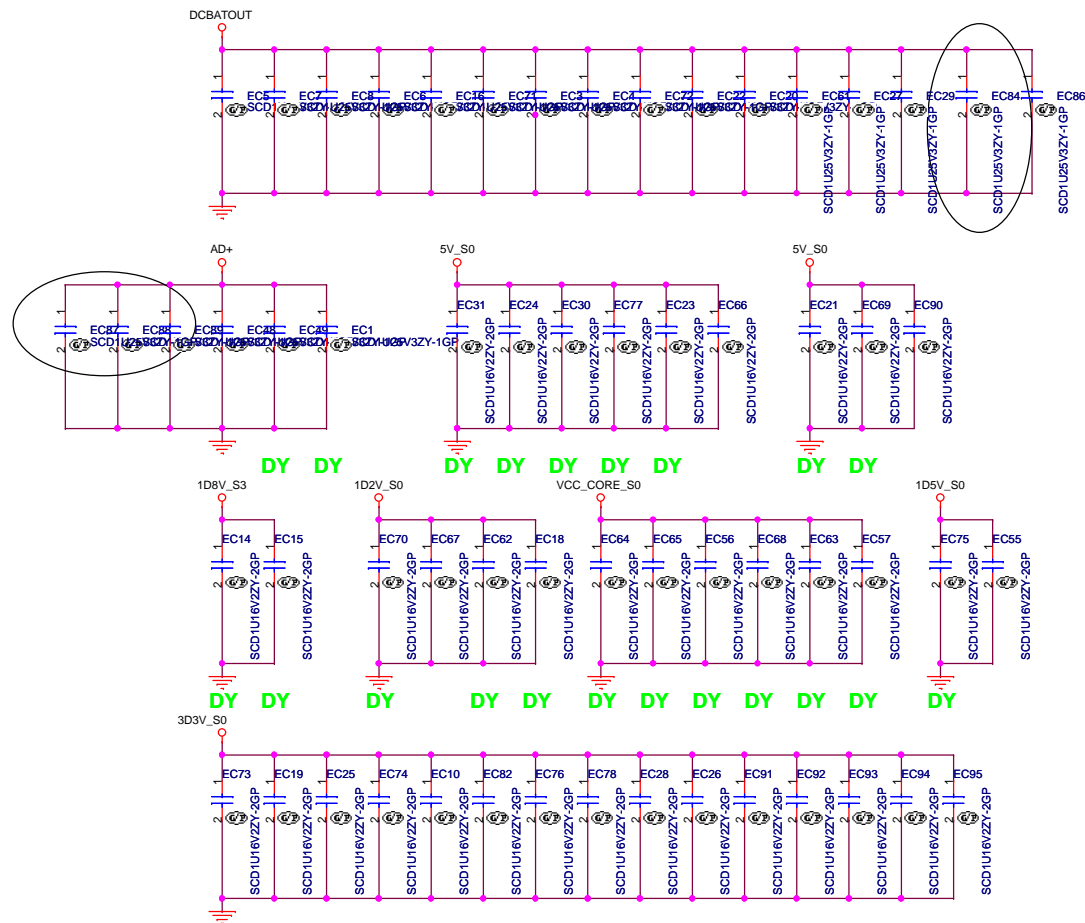
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Title		AD/BATT CONN	
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	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GND



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Title: MISC		
Size: A3	Document Number:	Rev: SA
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