

# Soyuz 2.0 SYSTEM DIAGRAM

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

**Cable Docking**

- TV\_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 32

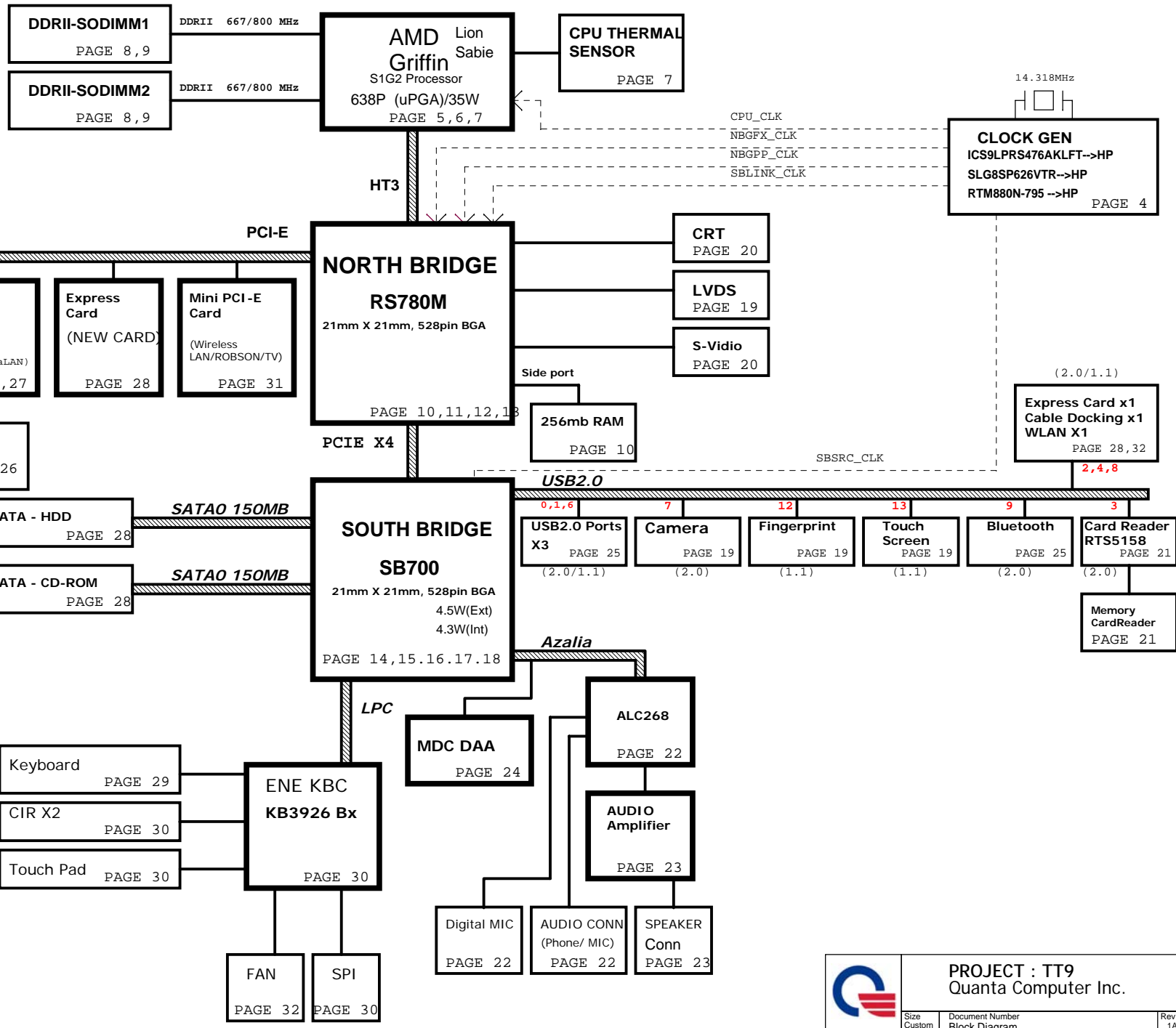
**SYSTEM CHARGER (ISL6251A)**  
PAGE 39

**SYSTEM POWER MAX1631A**  
PAGE 33

**DDR II SMDR\_VTERM 1.8V/1.8VSUS**  
PAGE 36

**VCCP +1.1V AND +1.2V (RT8204)**  
PAGE 34

**CPU CORE ISL6265A**  
PAGE 35



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Size Custom	Document Number Block Diagram	Rev 1A
Date: Wednesday, January 23, 2008   Sheet 1 of 41		

NB5/RD2/HW1

# INDEX

Pg#	Description	NOTE
1	Schematic Block Diagram	
2	System Information	
3	Power sequence chart	
4	CLOCL GENERATOR	
5-7	AMD CPU S1G2 Griffin	
8-9	DDR II SO-DIMM	
10-13	RS780M	
14-18	SB700	
19	LCD CONNECTOR / LCD PWR / LID	
20	20--CRT,TV_OUT	
21	RTS5158E & CR SOCKET	
22	Azalia ALC268	
23	JACK/AMP_TPA0312	
24	Si3080 and MDC1.5 Connector	
25	Blue Tooth / USBX3 / TPM	
26	RTL8111C/RJ45	
27	LAN Power	
28	NEW CARD/SATA ODD/SATA HDD	
29	LED/KEYBOARD/SW	
30	KB3926/ROM/TP	
31	Mini CARD/Hole	
32	CABLE DOCKING/FAN	
33	3V/5V(MAX1631A)	
34	+1.2V/+1.1V (RT8204)	
35	+CPU_CORE ISL6265	
36	+1.8VSUS/+1.8V/+2.5V	
37	+1.1V/+1.2V_S5/+1.5V	
38	DISCHARGE	
39	Charger (ISL6251)	

\* --> Un-stuff (ex. \*1K/04)  
 04-- 0402 footprint  
 06-- 0603 footprint  
 08-- 0805 footprint  
 12-- 1206 footprint  
 F-- 1% tolerance

# Power & Ground

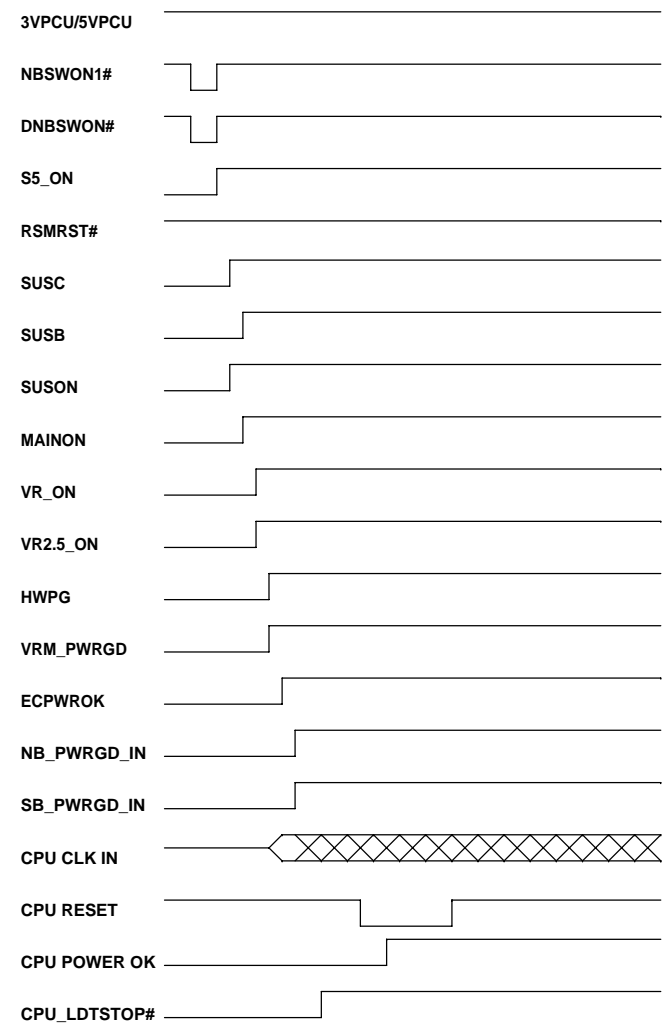
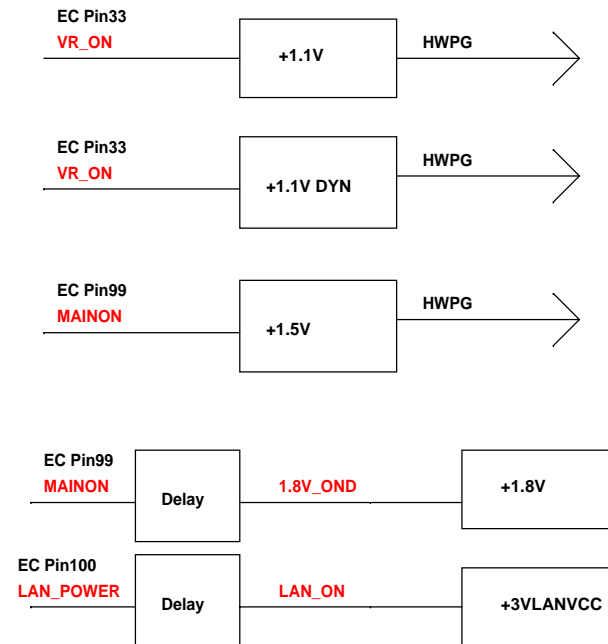
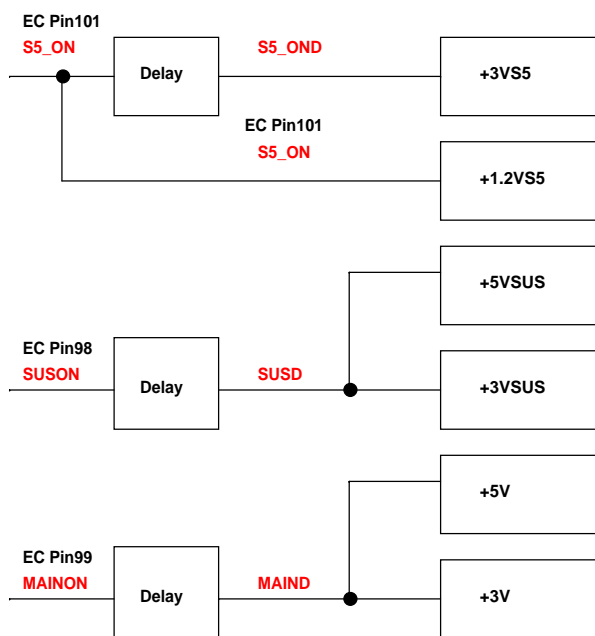
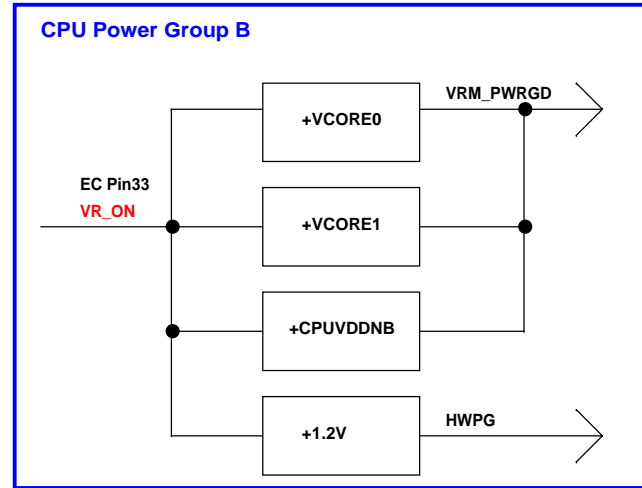
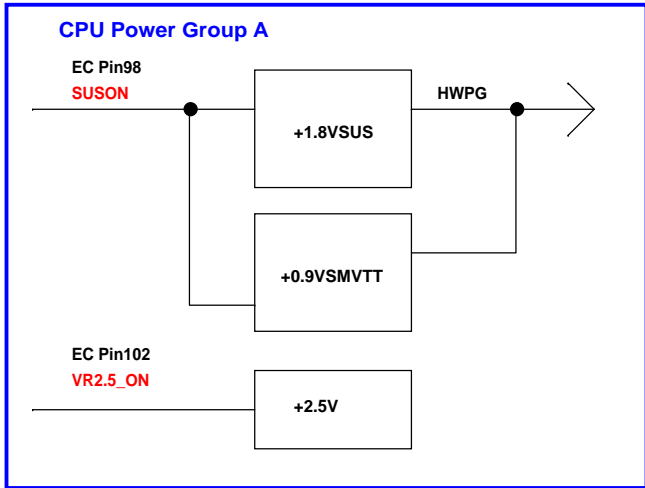
Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (18.5V)	
+BATT	S0, S3, S4, S5	MAIN BATTERY + (6.2V-8.4V)	
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3.3V)	
+12VALW	S0, S3, S4, S5	+12V	
+VCORE	S0	CPU CORE POWER (0.375-1.5V)	VRON
+CPUVDDNB	S0	CPU CORE POWER (1.375-1.5V)	VRON
+1.1V_NB	S0	+1.1 to +1.0 DYN	VRON
+1.1V	S0	+1.1V	VRON
+1.2VS5	S0, S3, S4, S5		S5_ON
+1.2V	S0	+1.2V	VRON
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
+5VSUS	S0, S3		SUSON
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+1.8V	S0		MAINON
+2.5V	S0	CPU VDDA	VR2.5_ON
+0.9VSMVTT	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
+0.9VSMVREF_DIMM	S0, S3	DDR REF POWER	SUSON
+AVDD	S0	AUDIO ANALOG POWER (5V)	MAINON
+3VLAVCC	S0, S3, S4, S5	LAN Power	LAN_ON
 GND	ALL PAGES	DIGITAL GROUND	
 AGND		AUDIO GND	

SMBUS	SMBUS function define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card (+3VS5)
SMBCLK2 SMBDAT2	New CARD (+3VS5)

# 02



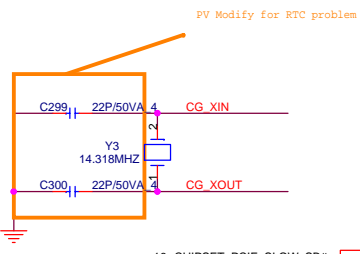
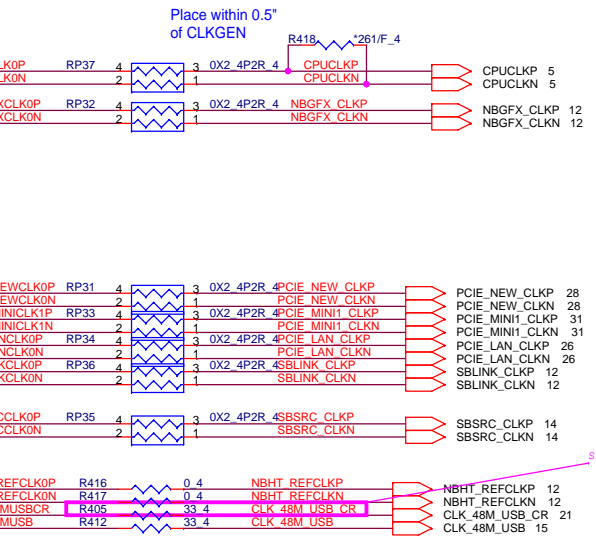
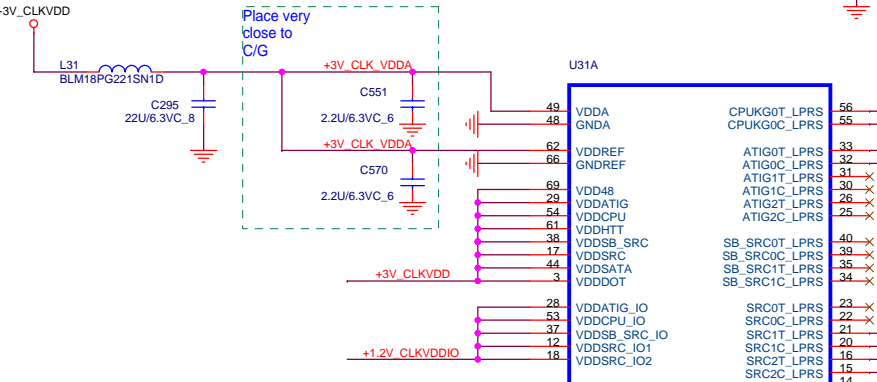
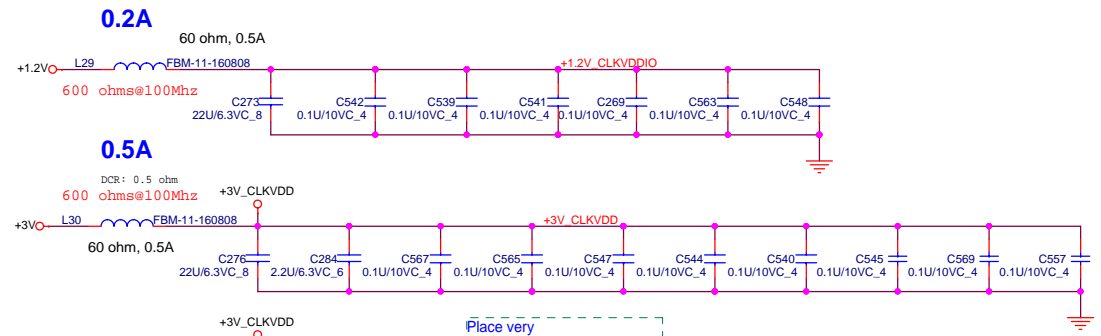
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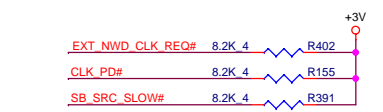
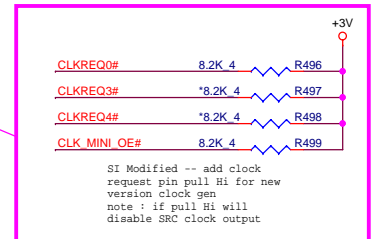
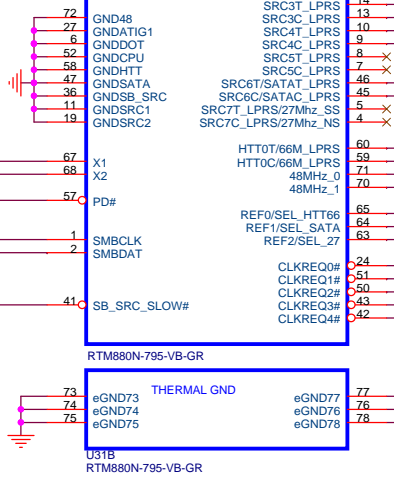
## NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



PV Modify for RTC problem



when driven low SB\_SRC clocks slow only supported with to reduced setpoint custom CG IC

\* default

SEL_HTT66	Value	Description
1	0*	66 MHz 3.3V single ended HTT clock
0*	1*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
SEL_27	0	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
SEL_27	0	100 MHz spreading differential SRC clock

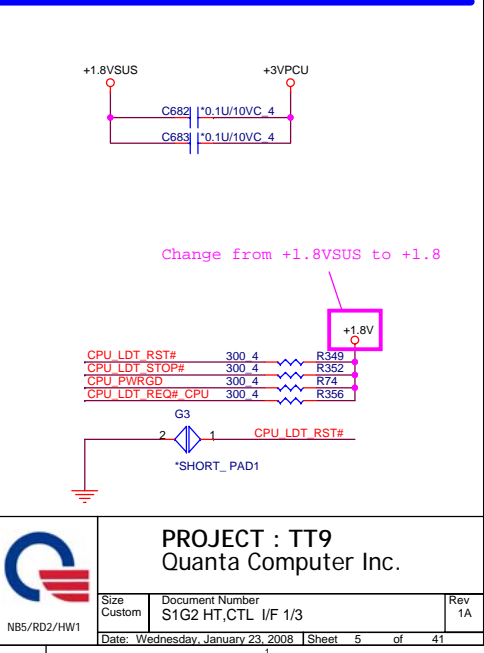
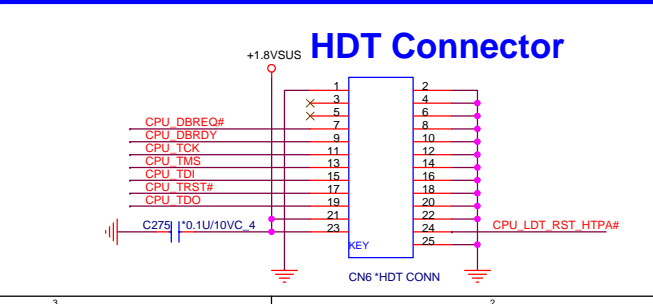
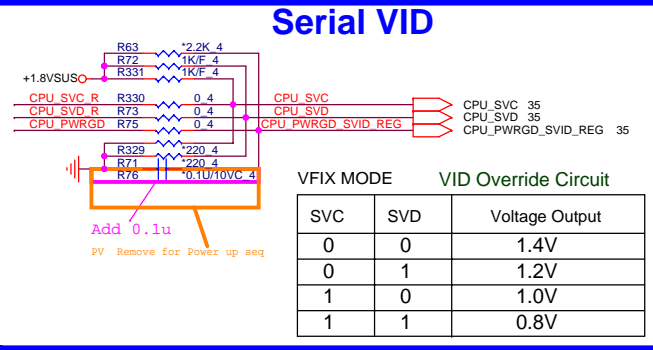
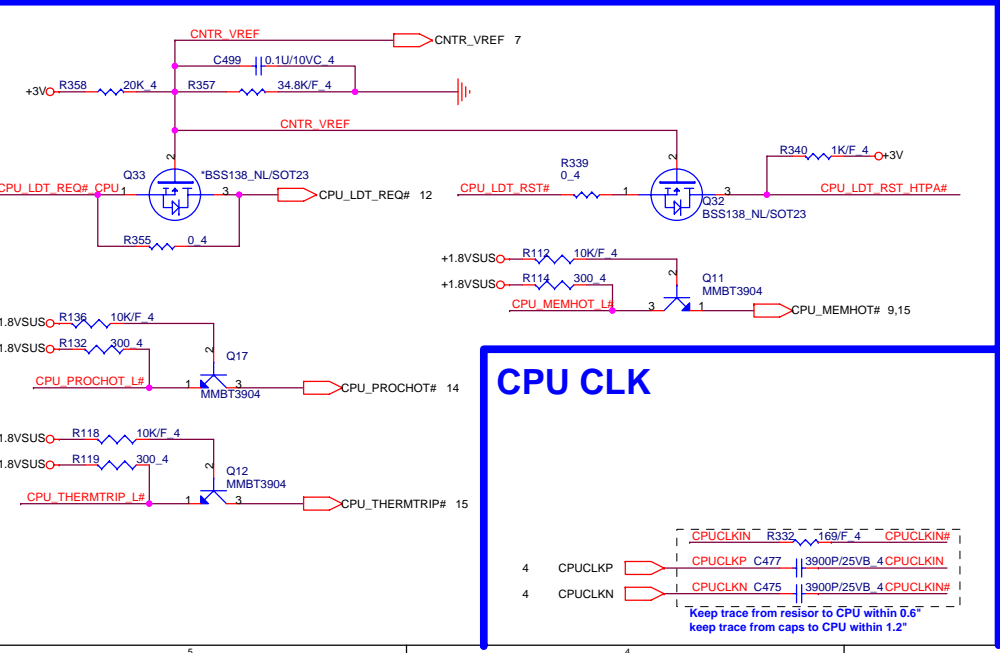
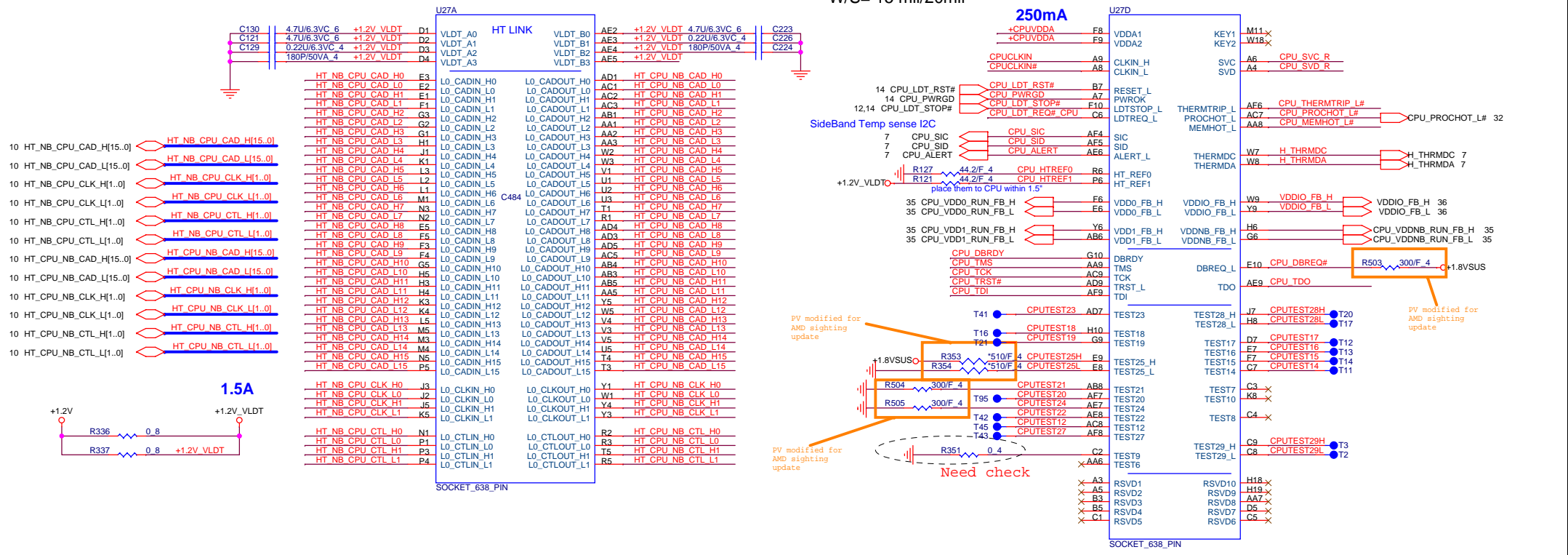
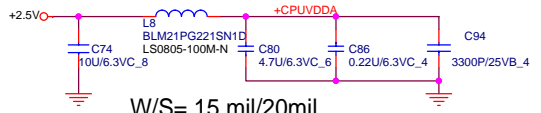
\* RS780 can be used as clock buffer to output two PCIE reference clocks. By default, chip will be configured as input mode, BIOS can program it to output mode.

- +1.2V 5,13,14,16,17,34,37
- +3V 5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38



PROJECT : TT9  
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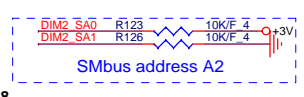
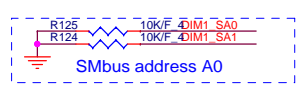
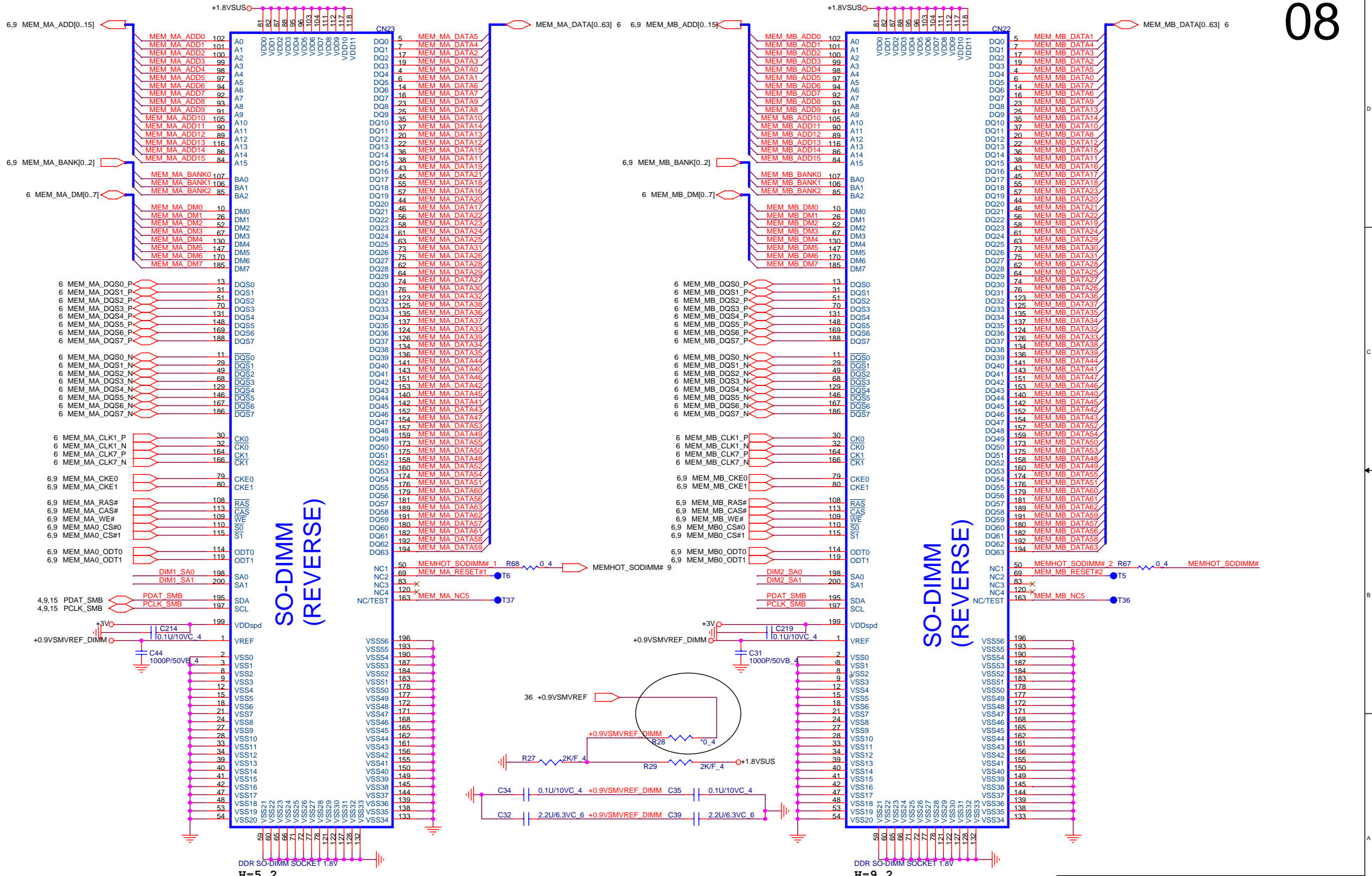
- +1.2V 4,13,14,16,17,34,37
- +1.8V 10,12,13,14,15,18,36,38
- +1.8VSUS 6,7,8,9,31,35,36,37
- +2.5V 37
- +3V 4,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38











+1.8VSUS 5,6,7,9,31,35,36,37  
 +3V 4,5,7,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

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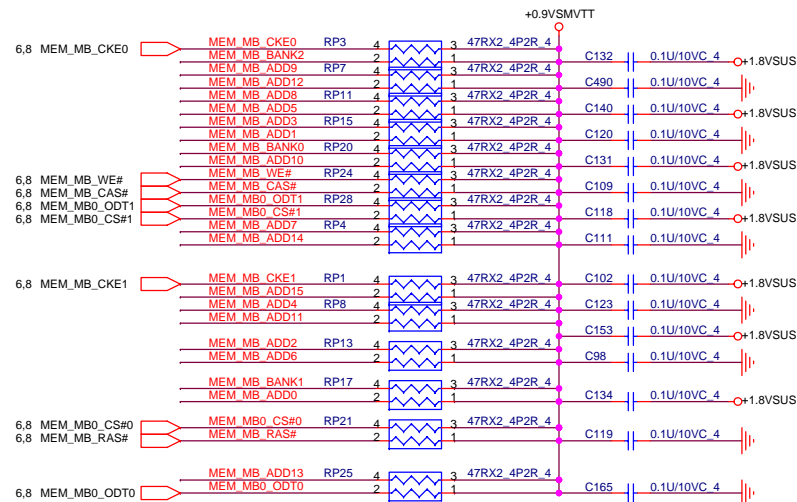
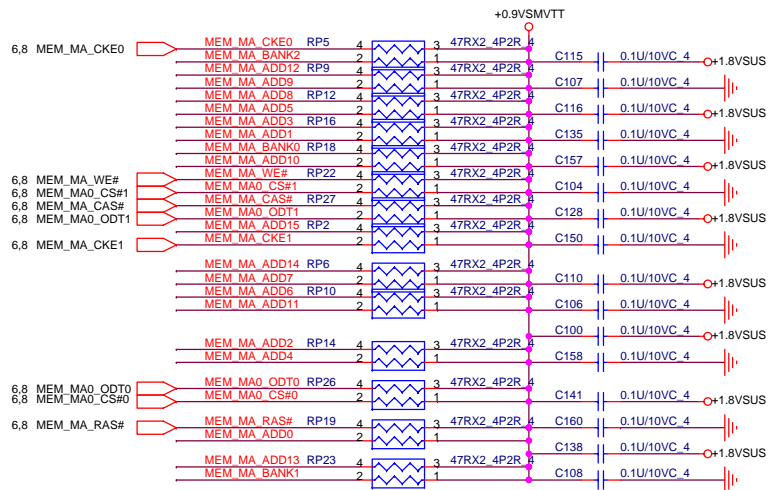
Size Custom Document Number DDR2 SODIMMS: A/B CHANNEL Rev 1A  
 Date: Wednesday, January 23, 2008 1 Sheet 8 of 41

NBS/RD2/HW1

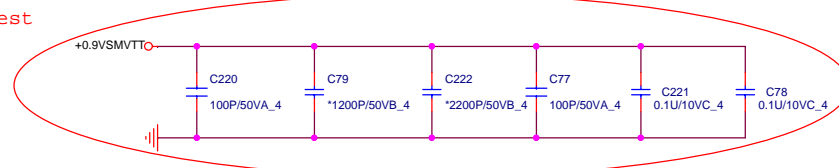


6.8 MEM\_MA\_ADD[0..15] MEM\_MA\_ADD[0..15]  
6.8 MEM\_MA\_BANK[0..2] MEM\_MA\_BANK[0..2]

6.8 MEM\_MB\_ADD[0..15] MEM\_MB\_ADD[0..15]  
6.8 MEM\_MB\_BANK[0..2] MEM\_MB\_BANK[0..2]



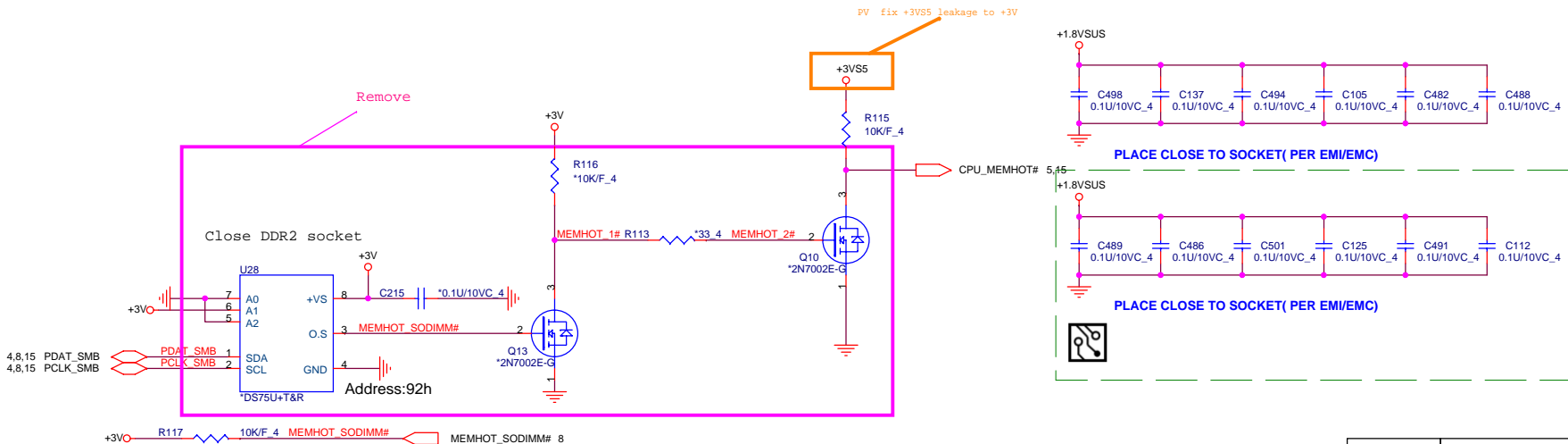
Emi request



PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



+0.9VSMVTT 6,31,36  
+1.8VSUS 5,6,7,8,31,35,36,37  
+3V 4,5,7,8,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38



PROJECT : TT9  
Quanta Computer Inc.

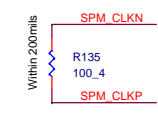
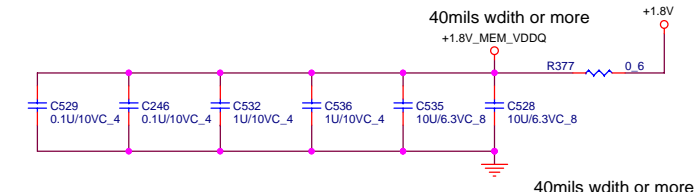
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Date: Wednesday, January 23, 2008		Sheet 9 of 41

PART 1 OF 6

HYPER TRANSPORT CPU I/F

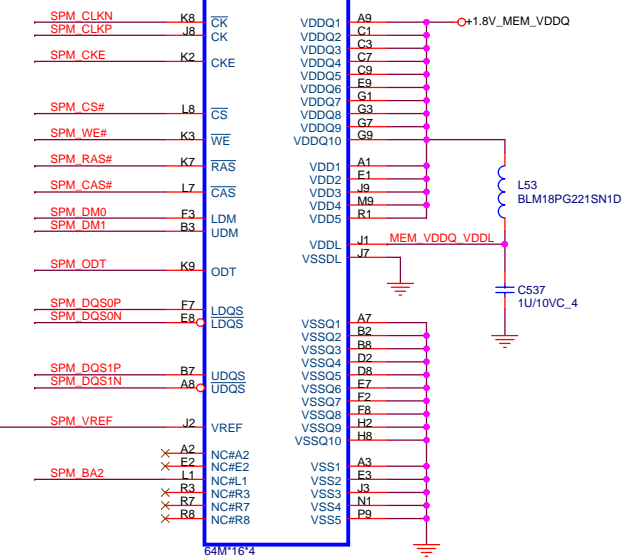
HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	E24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	E25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	E23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	E22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD9P	J20	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10P	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD10N	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11P	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	L18	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	L19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	P18	HT_NB_CPU_CTL_L1
HT_RXCALP	C23	HT_RXCALP	B24	HT_TXCALP
HT_RXCALN	A24	HT_RXCALN	B25	HT_TXCALN

HT_CPU_NB_CAD_H15_0	HT_CPU_NB_CAD_H15_0	5
HT_CPU_NB_CAD_L15_0	HT_CPU_NB_CAD_L15_0	5
HT_CPU_NB_CLK_H1_0	HT_CPU_NB_CLK_H1_0	5
HT_CPU_NB_CLK_L1_0	HT_CPU_NB_CLK_L1_0	5
HT_CPU_NB_CTL_H1_0	HT_CPU_NB_CTL_H1_0	5
HT_CPU_NB_CTL_L1_0	HT_CPU_NB_CTL_L1_0	5
HT_NB_CPU_CAD_H15_0	HT_NB_CPU_CAD_H15_0	5
HT_NB_CPU_CAD_L15_0	HT_NB_CPU_CAD_L15_0	5
HT_NB_CPU_CLK_H1_0	HT_NB_CPU_CLK_H1_0	5
HT_NB_CPU_CLK_L1_0	HT_NB_CPU_CLK_L1_0	5
HT_NB_CPU_CTL_H1_0	HT_NB_CPU_CTL_H1_0	5
HT_NB_CPU_CTL_L1_0	HT_NB_CPU_CTL_L1_0	5



Close to U23

SPM_BA0	L2	BA0	DQ15	B9	SPM_DQ15
SPM_BA1	L3	BA1	DQ14	B1	SPM_DQ14
SPM_A12	R3	A12	DQ13	D1	SPM_DQ12
SPM_A11	M7	A11	DQ11	D3	SPM_DQ8
SPM_A10	M2	A10/AP	DQ10	D7	SPM_DQ10
SPM_A9	P8	A9	DQ9	C2	SPM_DQ13
SPM_A8	P9	A8	DQ8	C8	SPM_DQ11
SPM_A7	P2	A7	DQ7	F9	SPM_DQ5
SPM_A6	N7	A6	DQ6	F1	SPM_DQ3
SPM_A5	N3	A5	DQ5	H9	SPM_DQ4
SPM_A4	N8	A4	DQ4	H1	SPM_DQ1
SPM_A3	N2	A3	DQ3	LH	SPM_DQ3
SPM_A2	M2	A2	DQ2	L2	SPM_DQ2
SPM_A1	M3	A1	DQ1	G2	SPM_DQ2
SPM_A0	M8	A0	DQ0	L8	SPM_DQ6



PV modified --  
follow AMD  
check list to  
change part  
number 300 ohm  
to 301 ohm

PV modified --  
follow AMD  
check list to  
change part  
number 300 ohm  
to 301 ohm

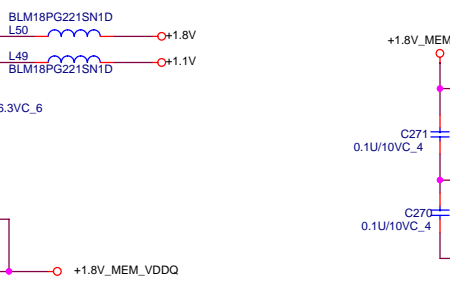
PAR 4 OF 6

SBD\_MEM/DVO\_I/F

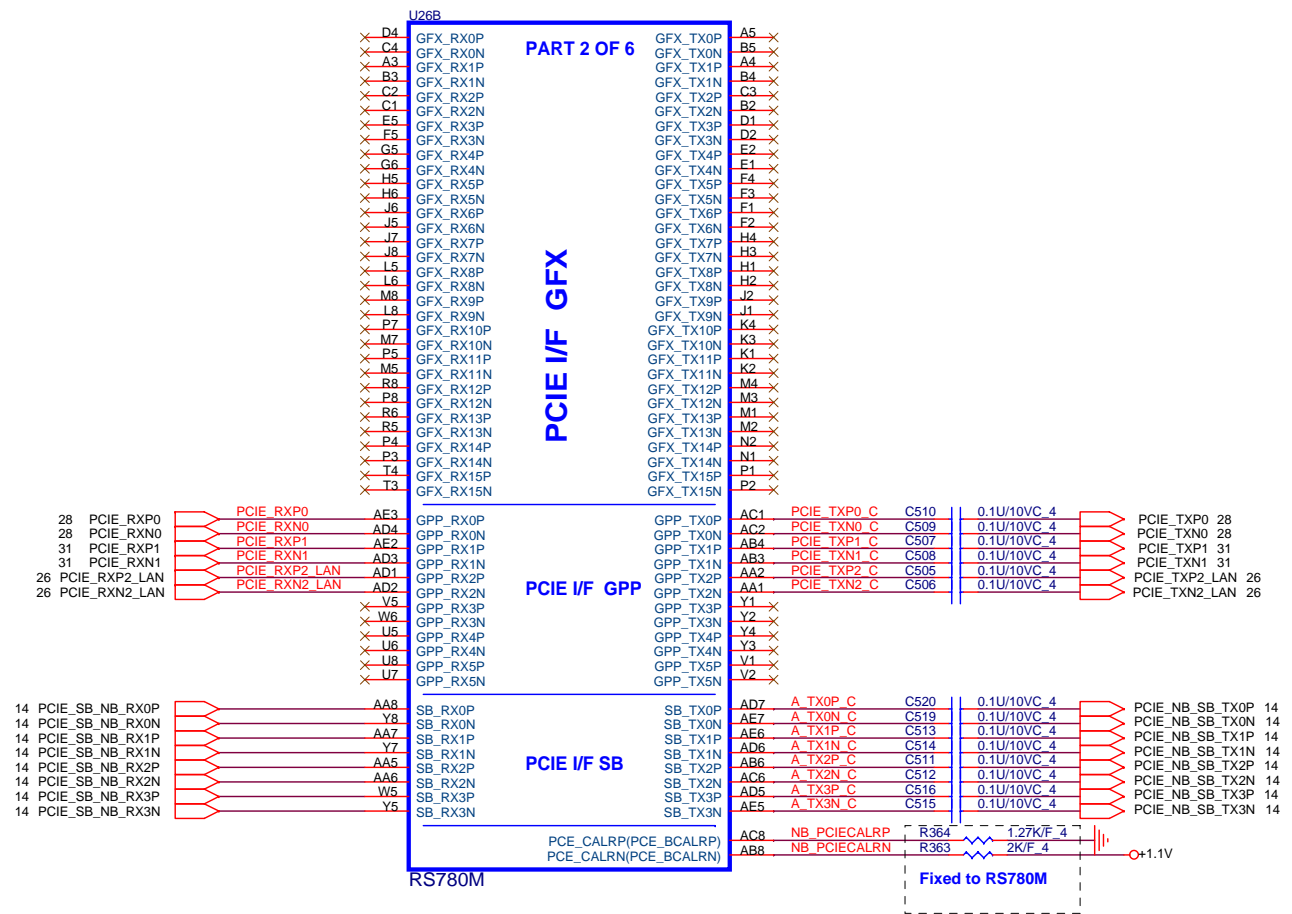
SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0(DVO_VSYNC(NC))	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1(DVO_HSYNC(NC))	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2(DVO_DE(NC))	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3(DVO_D0(NC))	V19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6(DVO_D1(NC))	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7(DVO_D2(NC))	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8(DVO_D3(NC))	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9(DVO_D5(NC))	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10(DVO_D6(NC))	AC18	SPM_DQ11
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11(DVO_D7(NC))	AB20	SPM_DQ12
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AD22	SPM_DQ13
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13(DVO_D9(NC))	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ14(DVO_D10(NC))	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)	MEM_DQ15(DVO_D11(NC))		
SPM_BA2	AD17	MEM_BA2(NC)			
SPM_RAS#	Y12C	MEM_RASb(NC)	MEM_DQS0P(DVO_IDCKP(NC))	Y17	SPM_DQS0P
SPM_CAS#	Y12C	MEM_CASb(NC)	MEM_DQS0N(DVO_IDCKN(NC))	W18	SPM_DQS0N
SPM_WE#	AD18C	MEM_WEb(NC)	MEM_DQS1P(NC)	AD20	SPM_DQS1P
SPM_CS#	AB13C	MEM_CSb(NC)	MEM_DQS1N(NC)	AE21	SPM_DQS1N
SPM_CKE	AB18C	MEM_CKE(NC)	MEM_DM0(NC)	W17	SPM_DM0
SPM_ODT	V14	MEM_ODT(NC)	MEM_DM1(DVO_D8(NC))	AE19	SPM_DM1
SPM_CLKP	W15	MEM_CKPN(NC)	IOPLLVD18(NC)	AE23	+1.8 IOPLLVD18 NB
SPM_CLKN	W14	MEM_CKN(NC)	IOPLLVD(NC)	AE24	+1.1V IOPLLVD
SPM_COMPN	AE12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18	SPM_VREF1
SPM_COMPN	AD12	MEM_COMPN(NC)			

+1.8V\_MEM\_VDDQ  
R361 40.2/F 4 SPM\_COMPN  
R362 40.2/F 4 SPM\_COMPN

All external components connected to SPME signals must be removed for RX780



+0.9VSMVTT	6,9,31,36
+1.1V	11,12,13,37
+1.8V	5,12,13,14,15,18,36,38

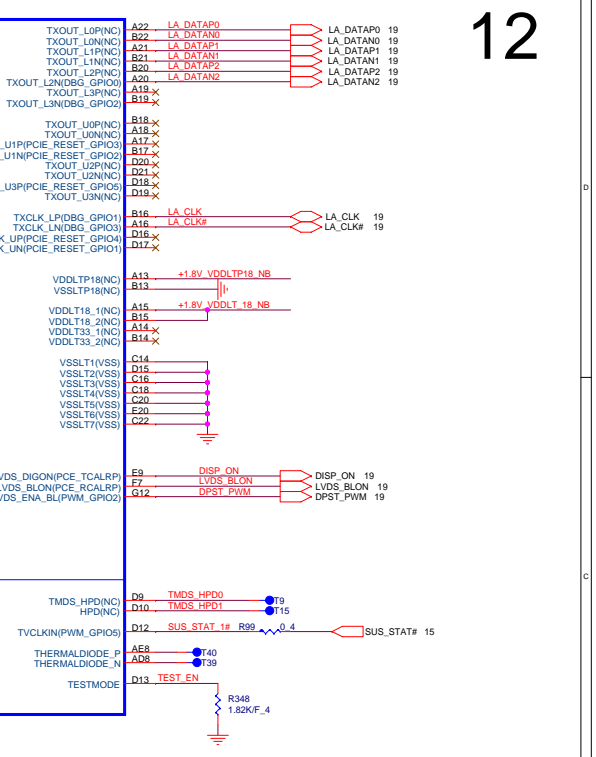
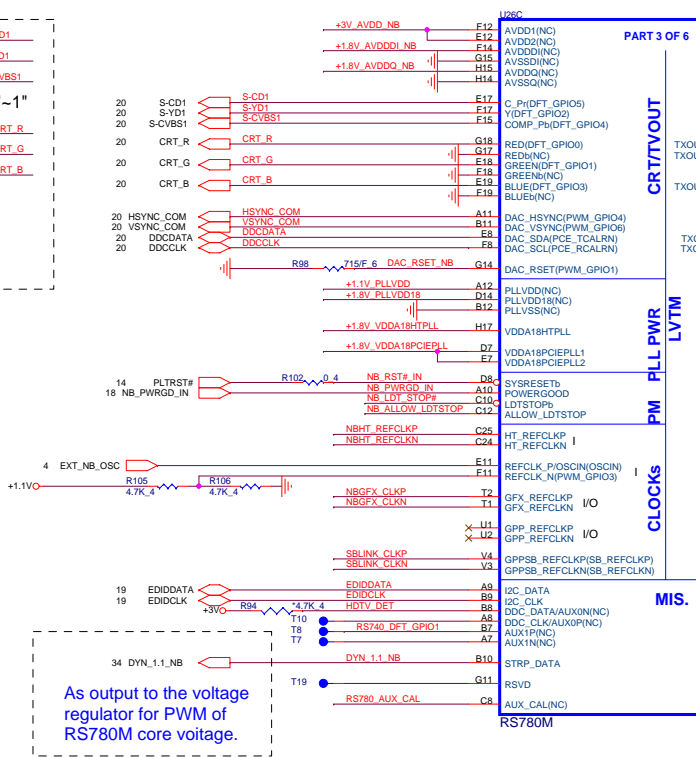
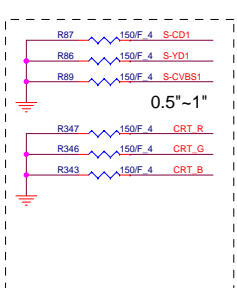
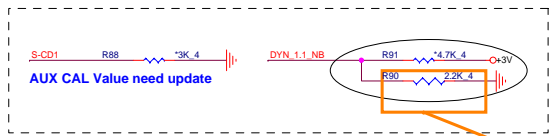
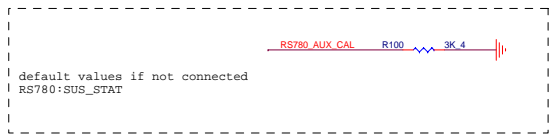
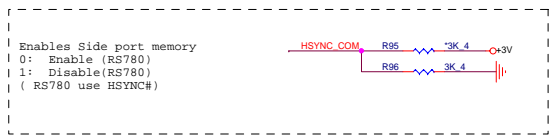


- GPP0** EXPRESS CARD (NEW CARD)
- GPP1** Wireless Lan
- GPP2** PCIE LAN(Realtek)

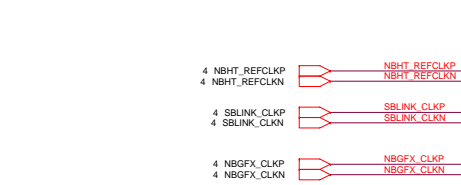
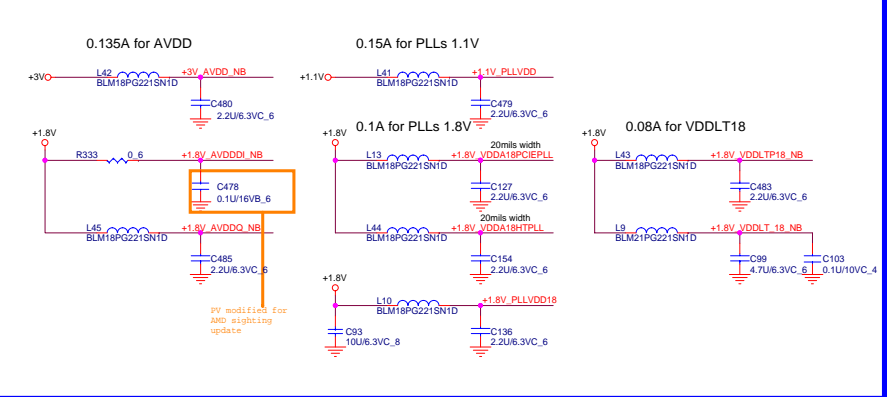
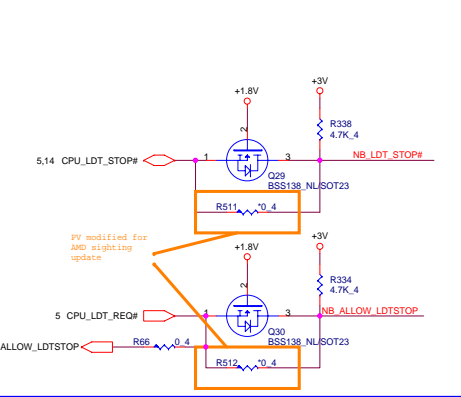


**PROJECT : TT9**  
**Quanta Computer Inc.**

Size B	Document Number RS780M-PCIE I/F 2/4	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 11 of 41		

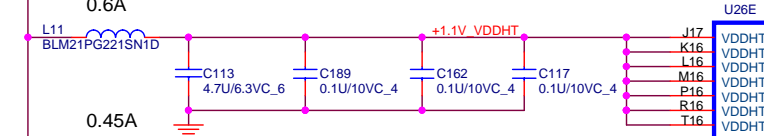


As output to the voltage regulator for PWM of RS780M core voltage.

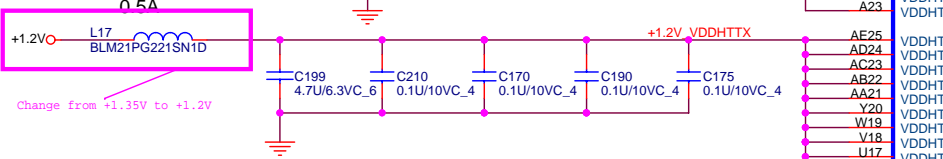


+1.1V 10,11,13,37  
+1.8V 5,10,13,14,15,18,36,38  
+3V 4,5,7,8,9,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38  
+12VALW 19,28,31,33,38

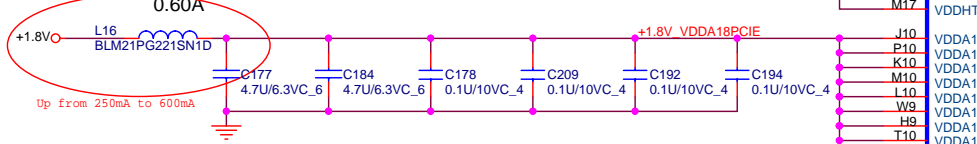
**+1.1V 2A for RS780M**



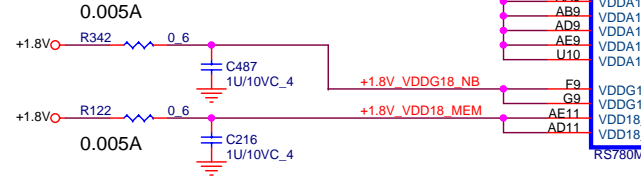
**+1.2V 2A for RS780M+SB700**



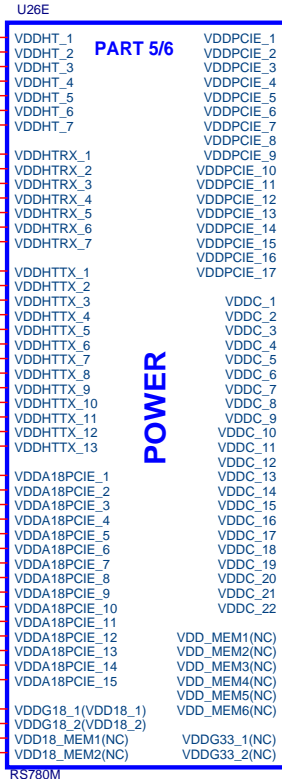
**+1.8V 1A for RS780M+SB700**



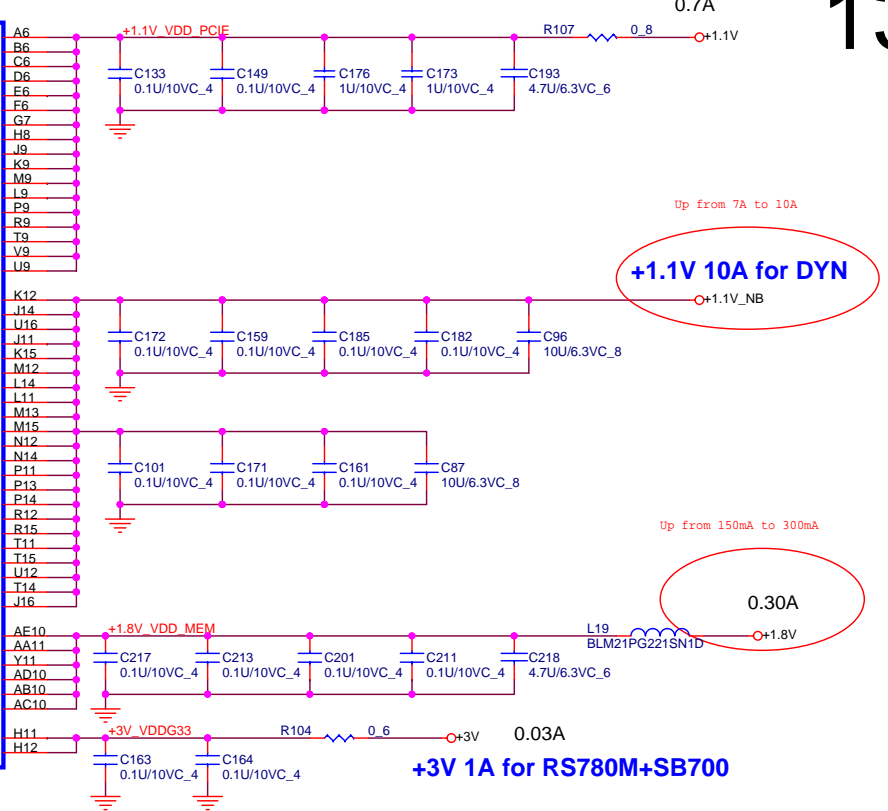
Change from +1.35V to +1.2V  
Up from 250mA to 600mA



**PART 5/6**



**POWER**

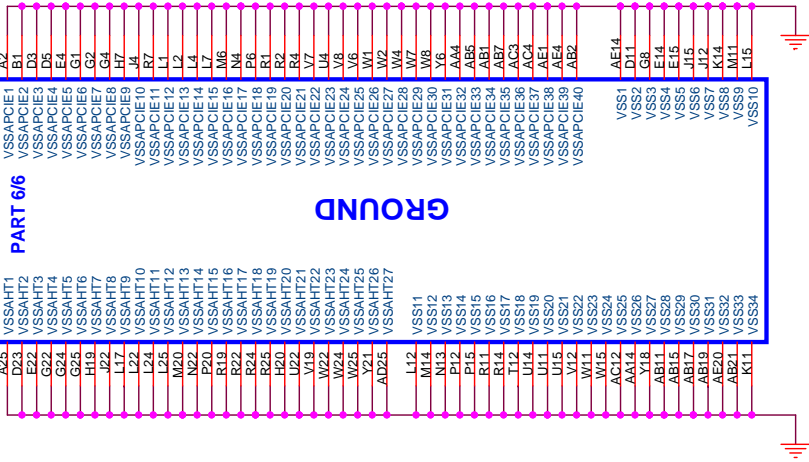


Up from 7A to 10A  
**+1.1V 10A for DYN**  
+1.1V\_NB

Up from 150mA to 300mA

0.30A

**+3V 1A for RS780M+SB700**



**GROUND**

- +1.1V NB 34
- +1.1V 10, 11, 12, 37
- +1.2V 4, 5, 14, 16, 17, 34, 37
- +1.8V 5, 10, 12, 14, 15, 18, 36, 38
- +3V 4, 5, 7, 8, 9, 12, 14, 15, 16, 17, 18, 19, 20, 22, 23, 26, 28, 29, 30, 31, 33, 34, 38



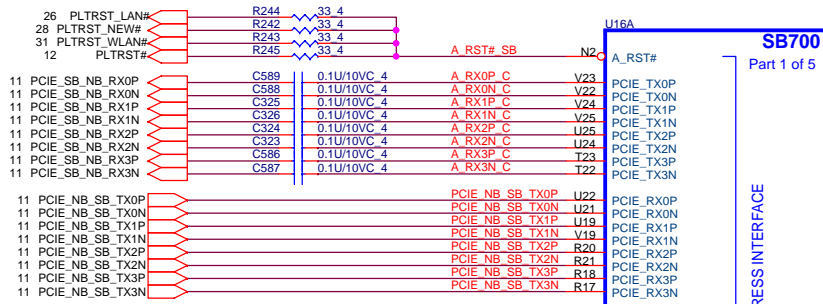
**PROJECT : TT9**  
Quanta Computer Inc.

Size B	Document Number RS780M-POWER 4/4	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 13 of 41		

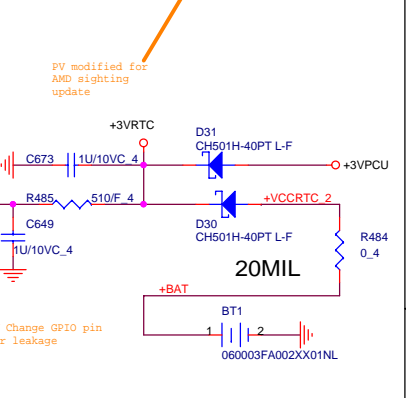
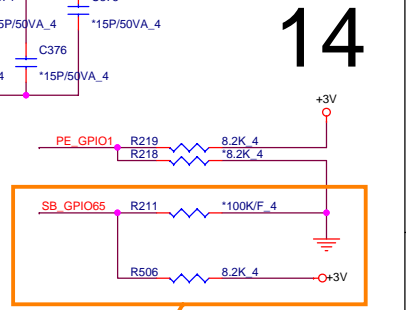
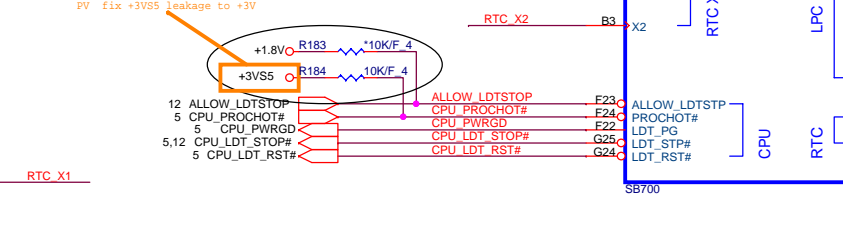
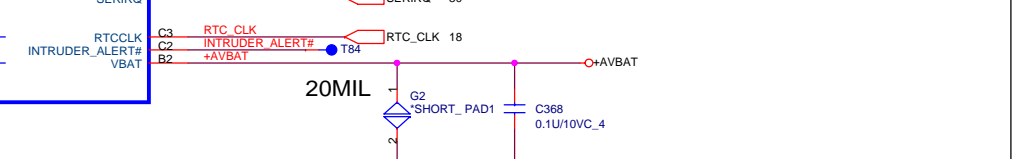
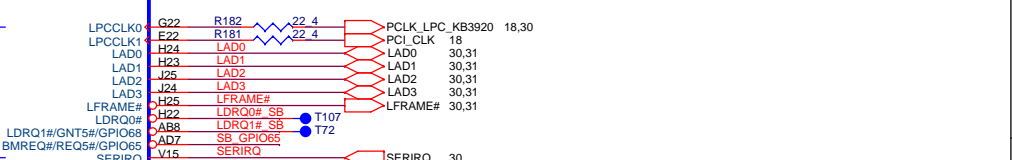
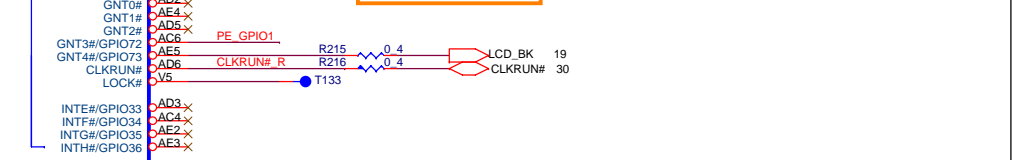
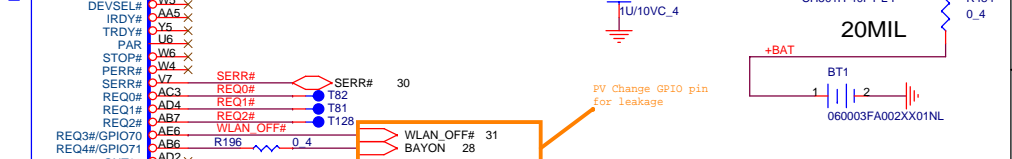
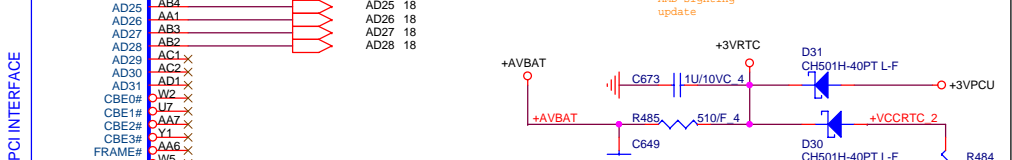
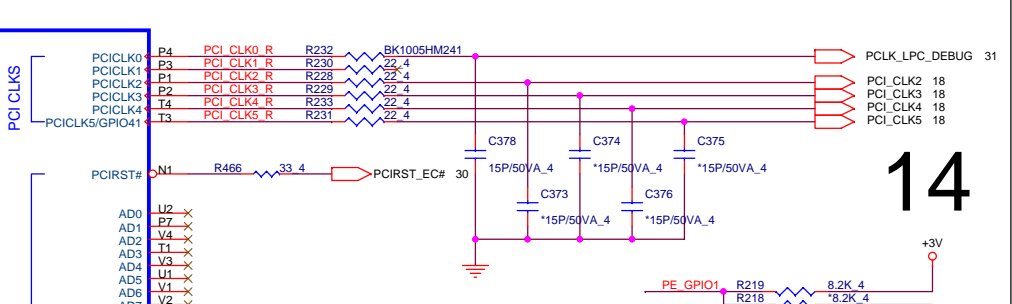
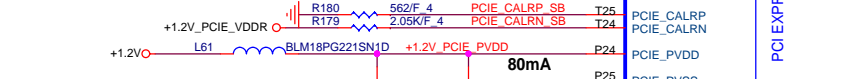
PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U600



To RS780



1. PCIe Reference Clk (Ext Clk Gen)
2. A-link Clk to North Bridge (Int Clk Gen)



14

PV modified for AMD sighting update

PV Change GPIO pin for Leakage

- +1.2V 4,5,13,16,17,34,37
- +1.8V 5,10,12,13,15,18,36,38
- +3V 4,5,7,8,9,12,13,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38
- +3VPCU 5,19,25,29,30,32,33,35,37,39

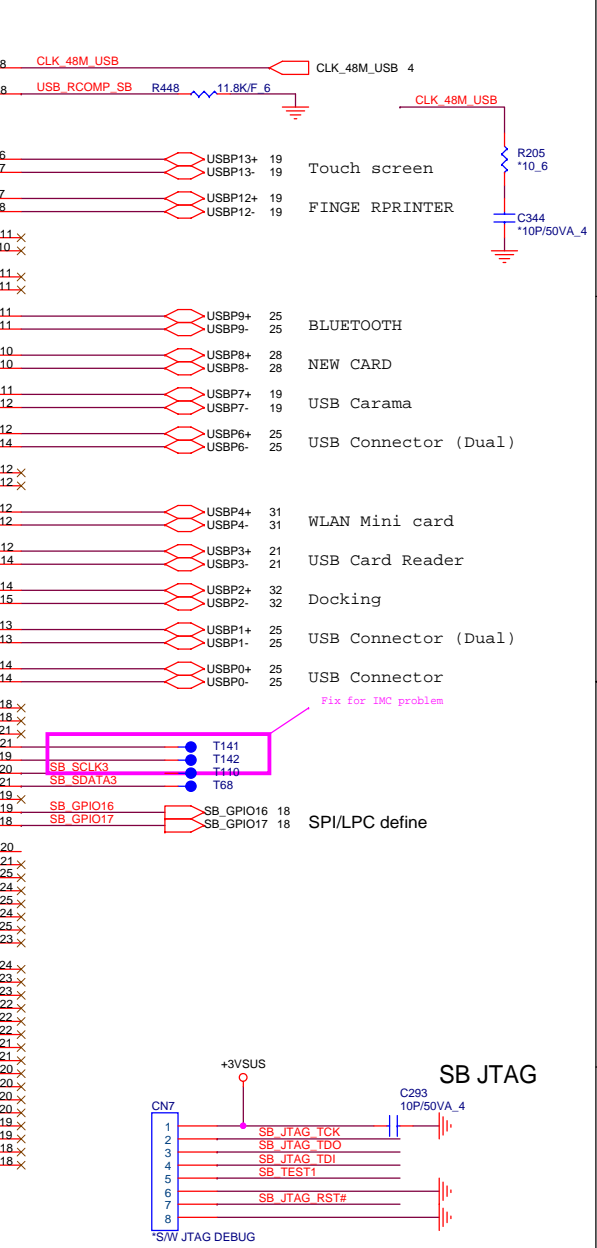
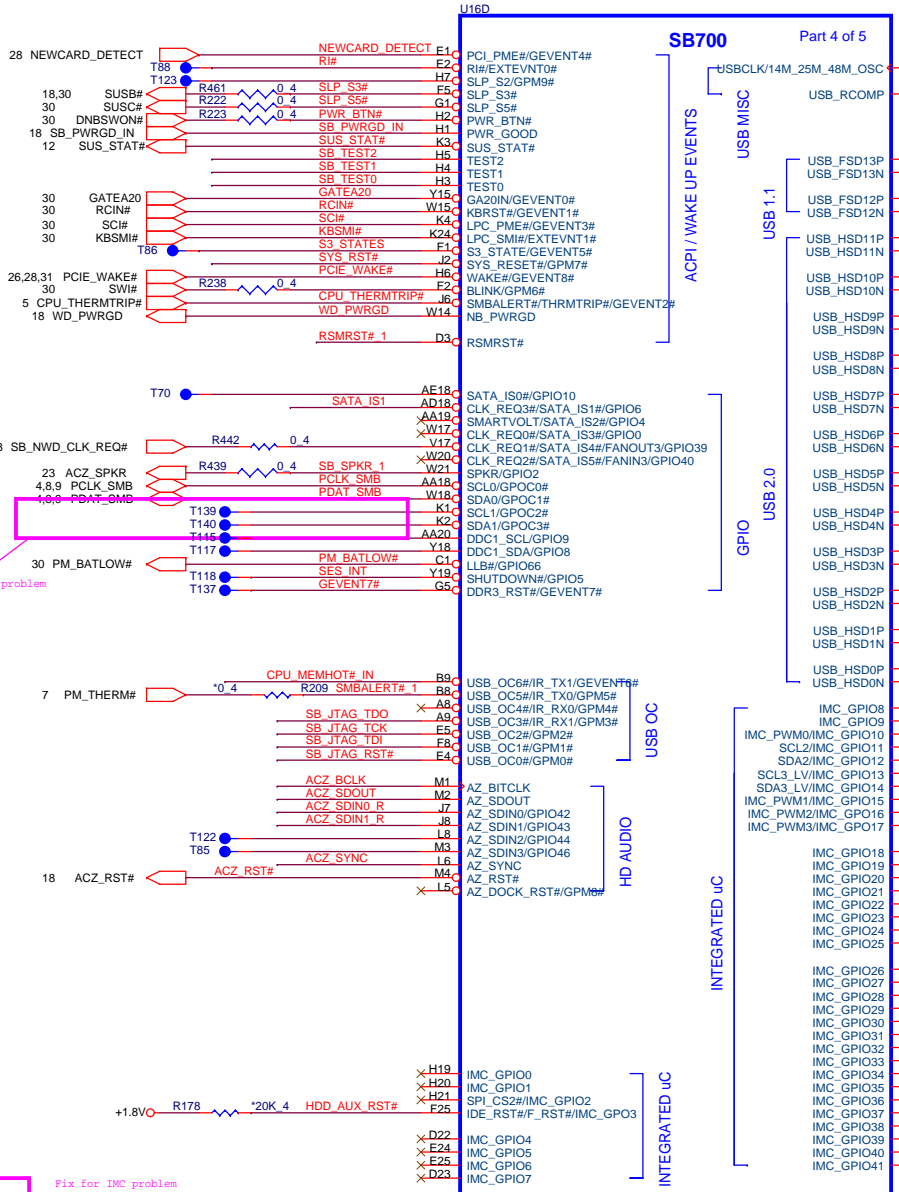
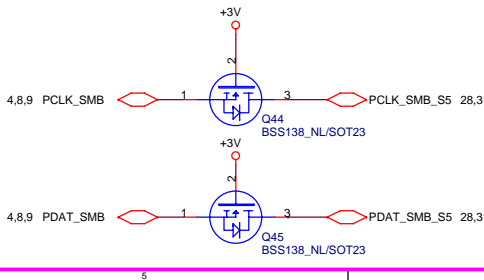
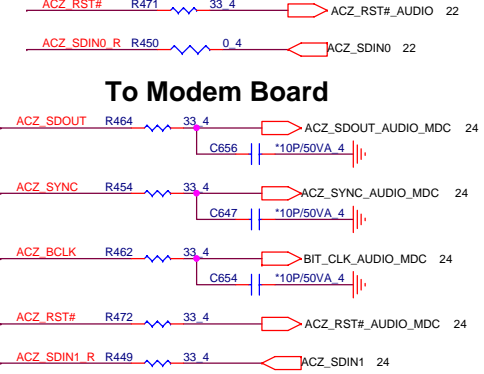
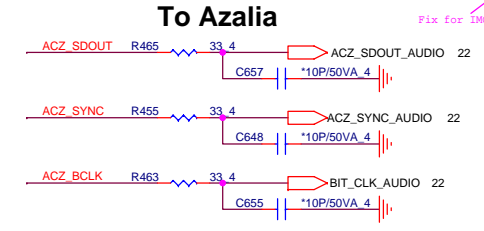
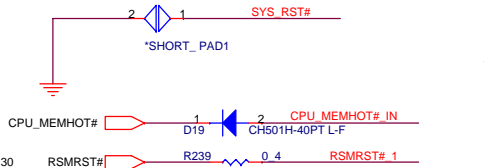
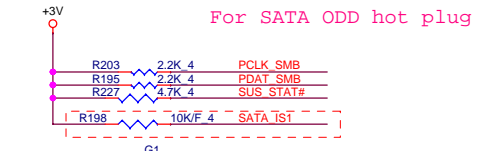
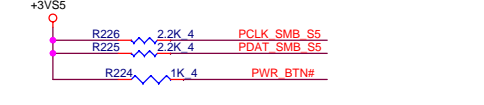
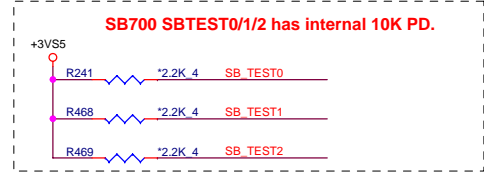


PROJECT : TT9  
Quanta Computer Inc.

Size Custom	Document Number SB700-PCIE/PCI/CPU/LPC 1/4	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 14 of 41

NB5/RD2/HW1



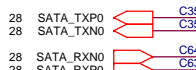


- +1.8VSUS 5,6,7,8,9,31,35,36,37
- +1.8V 10,12,13,14,18,36,38
- +3VSUS 21,22,25,29,31,33,34,35,36,38
- +3V5S 9,14,16,17,18,28,33,38
- +3V 4,5,7,8,9,12,13,14,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

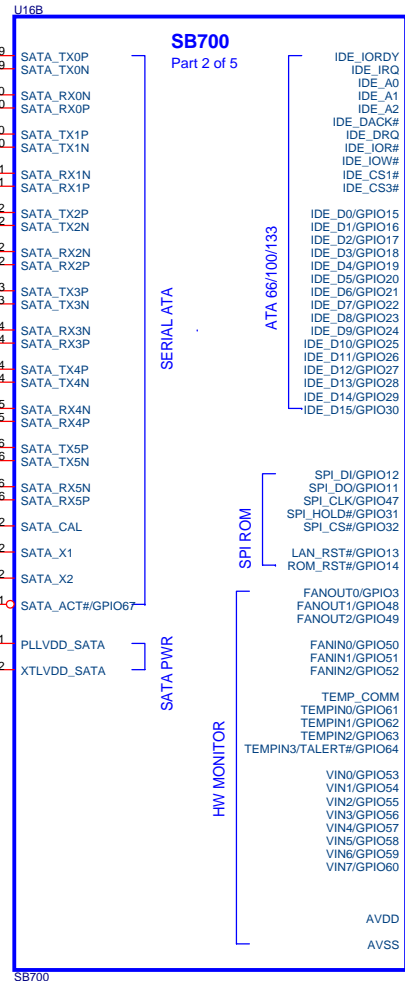
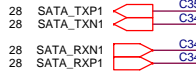


**PLACE SATA AC COUPLING CAPS CLOSE TO SB600**

### SATA1



### SATA ODD

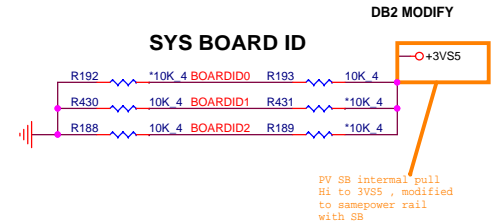
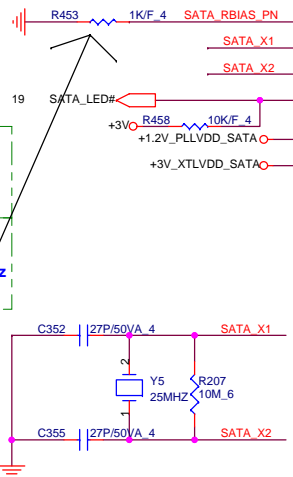


**IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY**

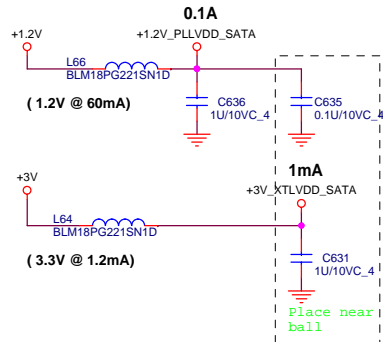
VRAM / Clock Gen	Samsung Realtek	Qimonda ICS	Hynix Silago
Board ID	(0.0.0)	(1.0.0)	(0.1.0)
BOARDID0	R192 Stuff	R193 Stuff	R192 Stuff
BOARDID1	R430 Stuff	R430 Stuff	R431 Stuff
BOARDID2	R188 Stuff	R188 Stuff	R188 Stuff

**PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U600**

**NOTE:**  
R635 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK



PV SB internal pull Hi to 3VS5, modified to samepower rail with SB



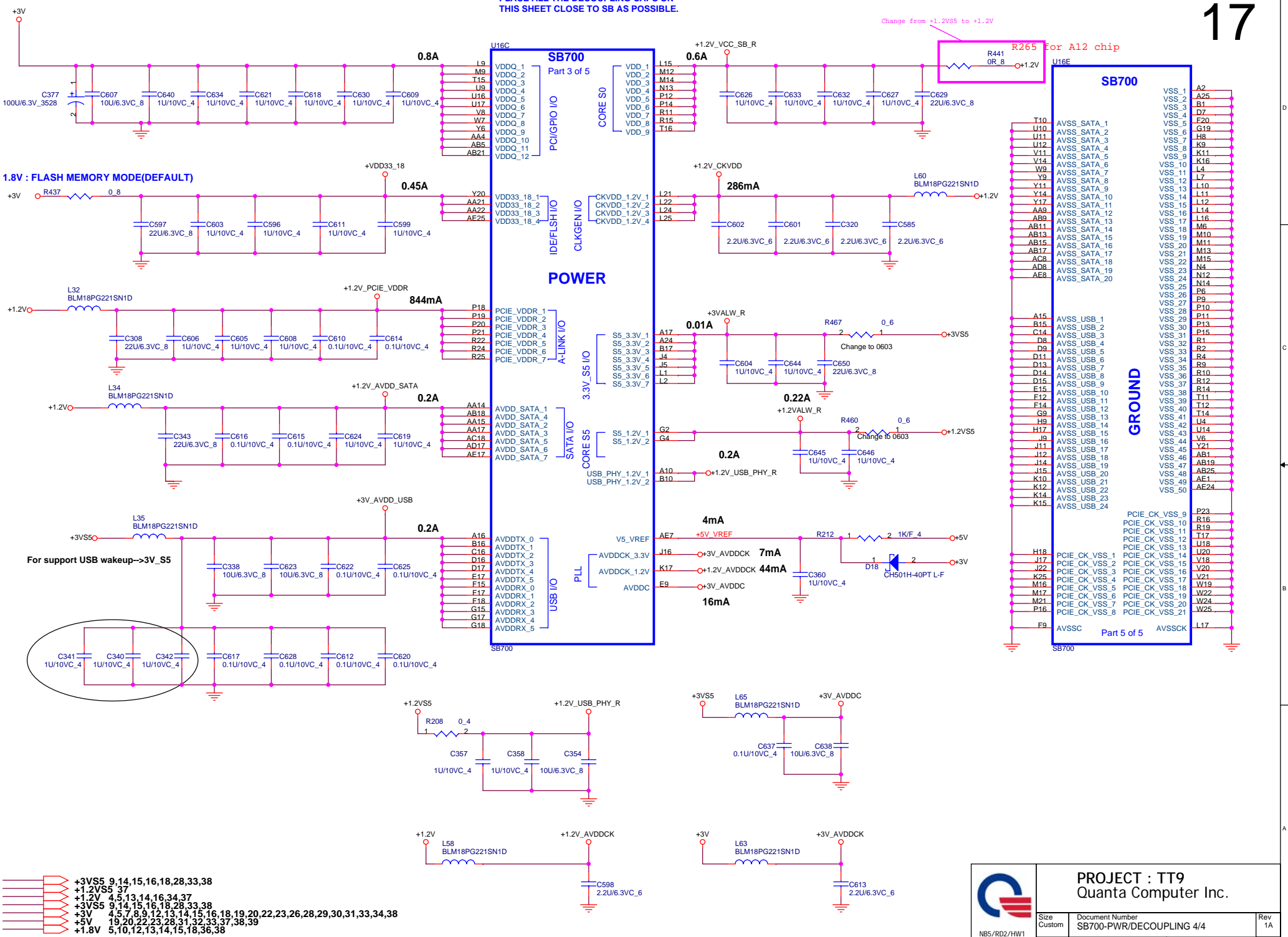
+1.2V 4,5,13,14,17,34,37  
+3V 4,5,7,8,9,12,13,14,15,17,18,19,20,22,23,26,28,29,30,31,33,34,38



**PROJECT : TT9**  
Quanta Computer Inc.

Size Custom	Document Number SB700-SATA/IDE/HWM/SPI 3/4	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 16 of 41

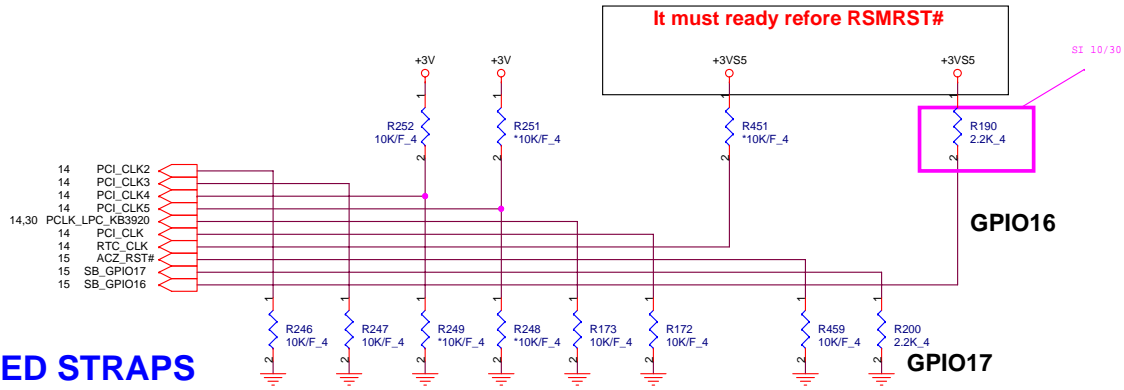
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



PROJECT : TT9  
Quanta Computer Inc.

Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 17 of 41

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

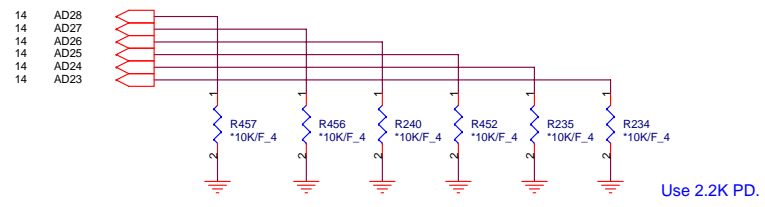


**OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.**

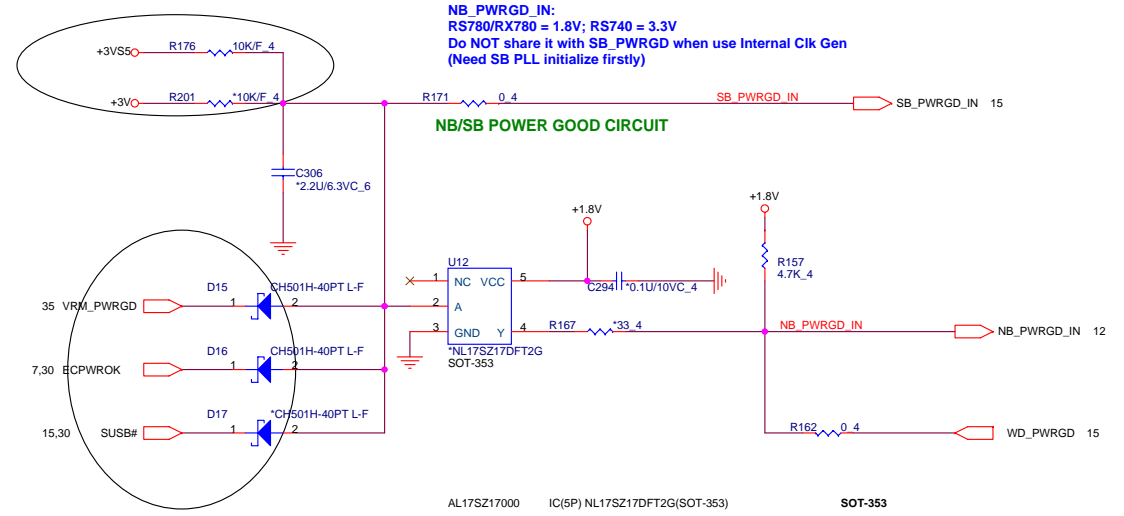
**REQUIRED STRAPS**

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCLK_LPC_KB3920	PCI_CLK	RTC_CLK	AZ_RST#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM	DEFAULT

**DEBUG STRAPS** SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM STRAPS	



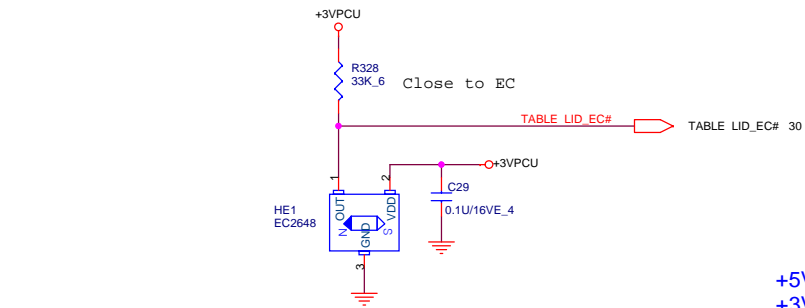
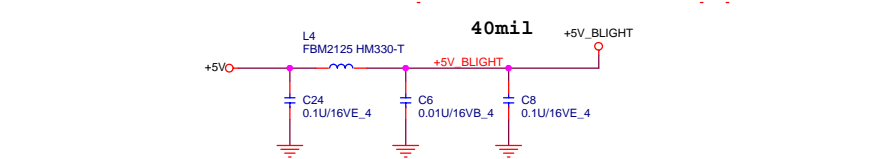
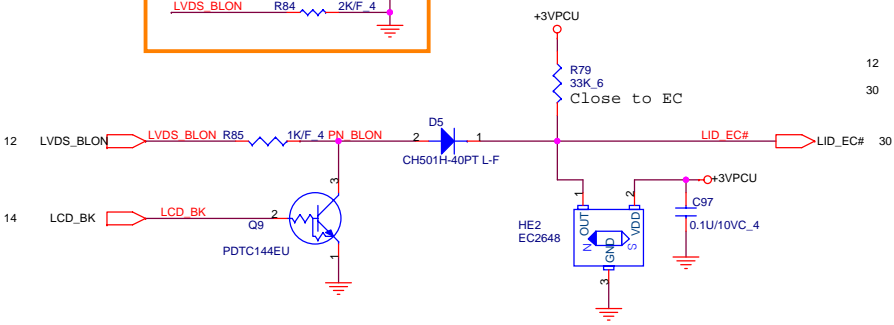
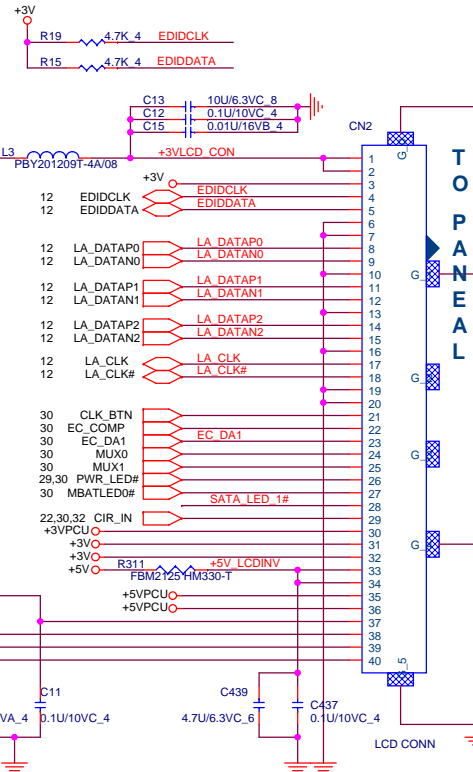
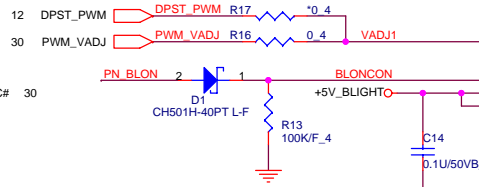
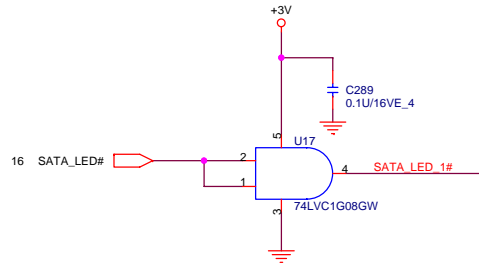
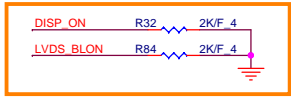
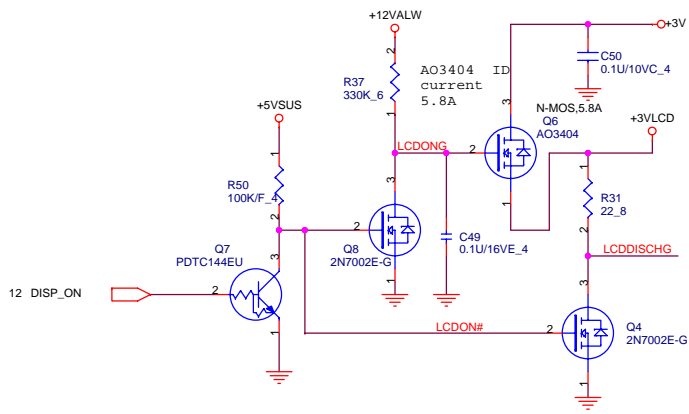
**NB\_PWRGD\_IN:**  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

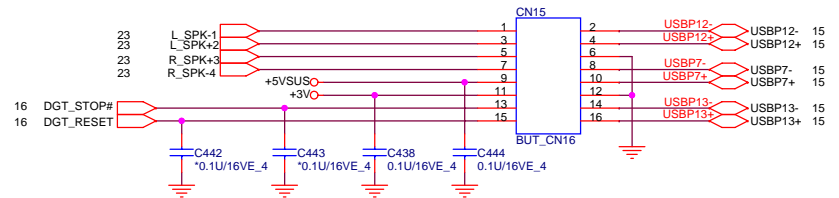
+1.8V 5,10,12,13,14,15,36,38  
+3V 4,5,7,8,9,12,13,14,15,16,17,19,20,22,23,26,28,29,30,31,33,34,36  
+3V5S 9,14,15,16,17,28,33,38

**PROJECT : TT9**  
Quanta Computer Inc.

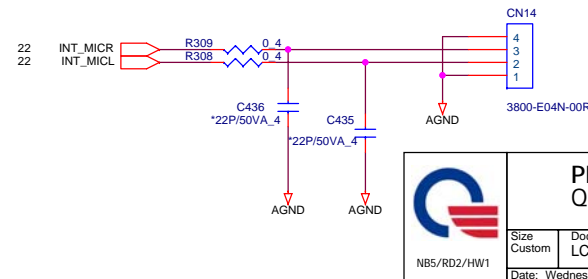
Size Custom Document Number SB700-STRAPS,PWRGD Rev 1A  
Date: Wednesday, January 23, 2008 Sheet 18 of 41




Speaker  
+5VSUS --> Camera  
+3V --> FP/Digitizer  
Digitizer control signal



Finger Printer  
Camera  
Digitizer



- +3VPCU 5,14,25,29,30,32,33,35,37,39
- +3V 4,5,7,8,9,12,13,14,15,16,17,18,20,22,23,26,28,29,30,31,33,34,38
- +3VSUS 15,21,24,25,29,31,33,34,35,36,38
- +5V 17,20,22,23,28,31,32,33,37,38,39
- +12VALW 28,31,33,38

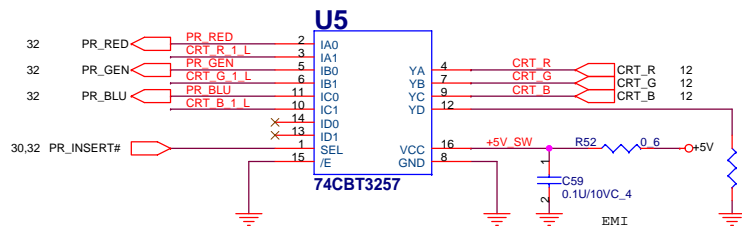


**PROJECT : TT9**  
Quanta Computer Inc.

Size Custom	Document Number LCD_CONN,HDMI_CONN	Rev 1A
Date: Wednesday, January 23, 2008   Sheet 19 of 41		

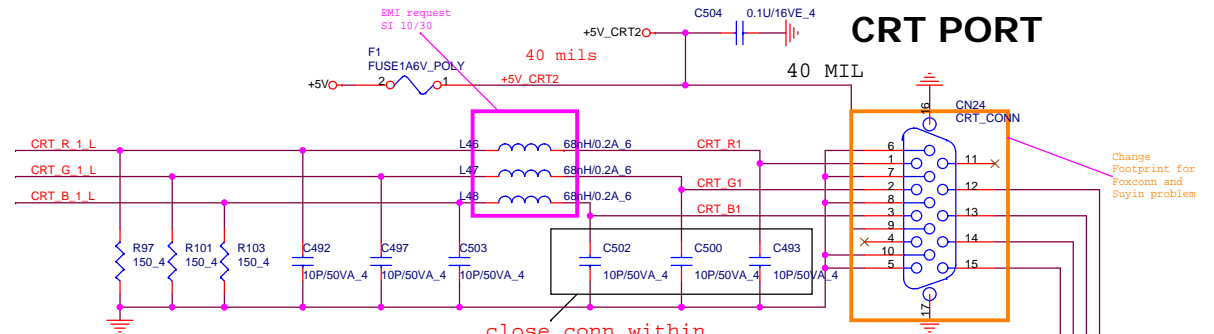
NBS/RD2/HW1

CRT SWITCH



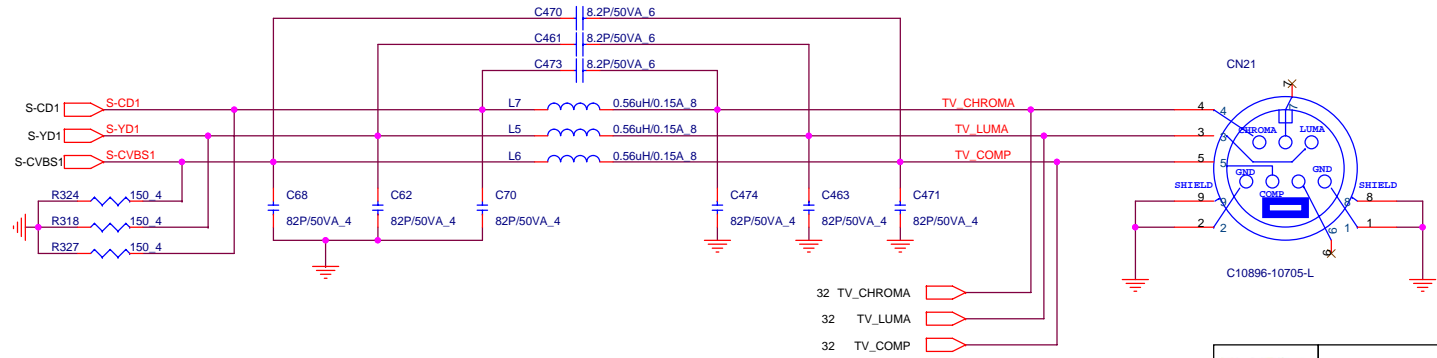
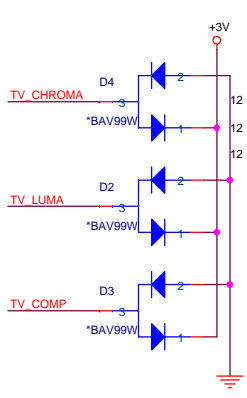
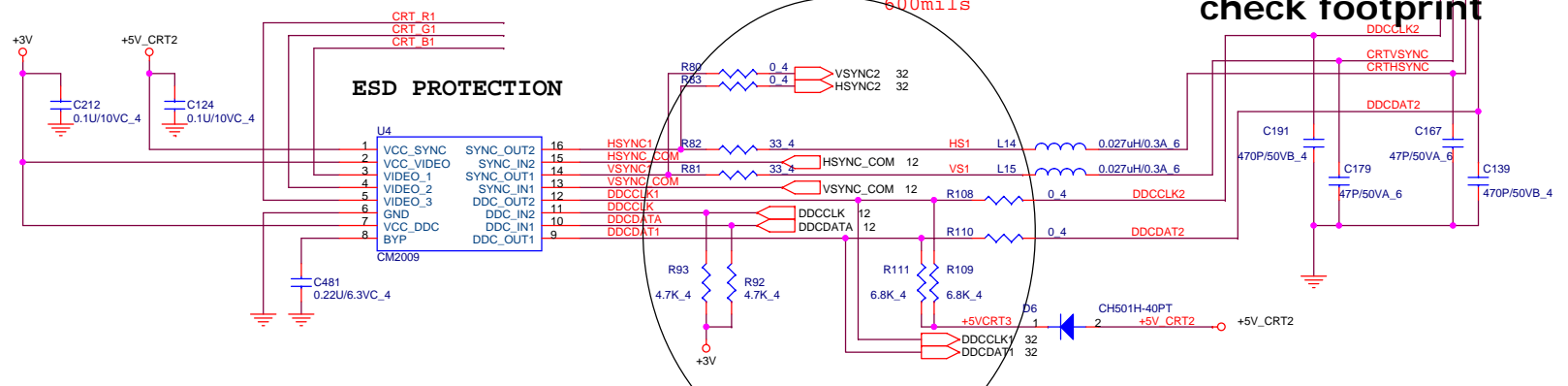
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

CRT PORT



Change Footprint for Foxconn and Suyin problem

check footprint



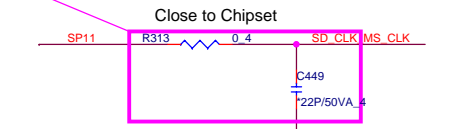
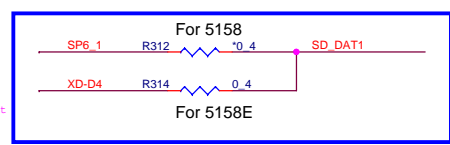
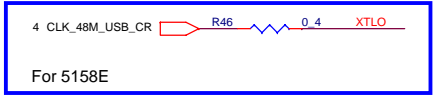
+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,22,23,26,28,29,30,31,33,34,38  
+5V 17,19,22,23,28,31,32,33,37,38,39

**PROJECT : TT9**  
Quanta Computer Inc.

Size Custom	Document Number CRT_TV_OUT	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 20 of 41		

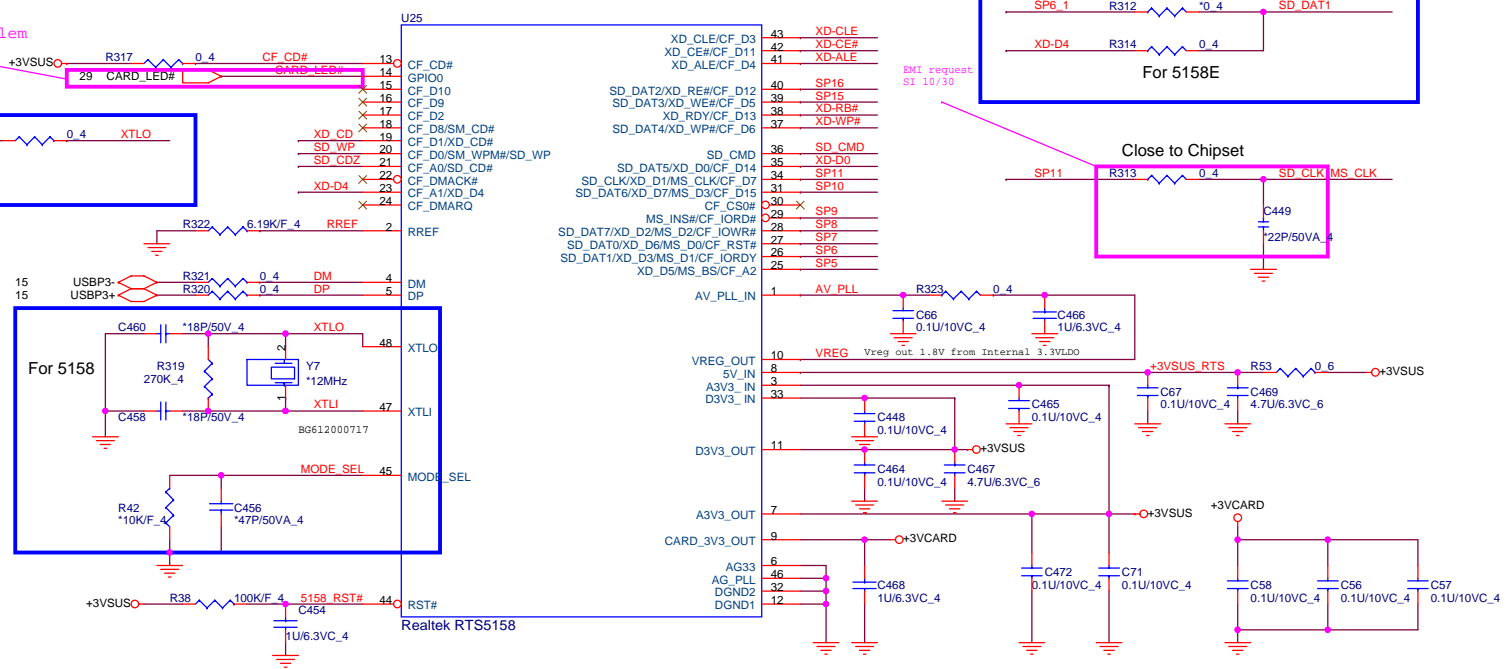


Fix card reader led problem

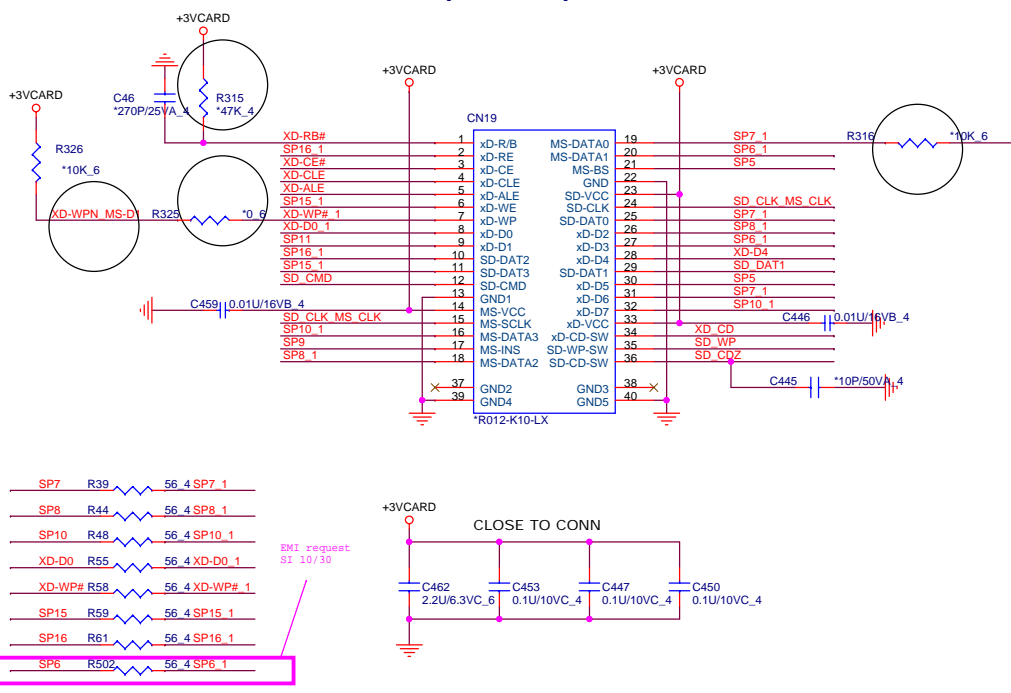


Note:

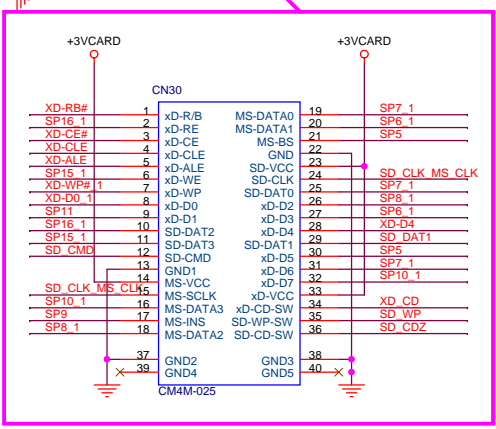
SP0	SD/MMMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE



### 4 IN1 CARD READER XD, MMC / SD, MS / MSP



Add Connector for joint

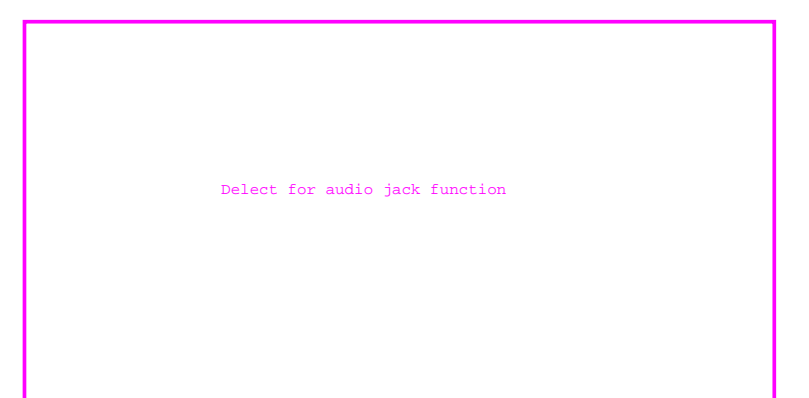
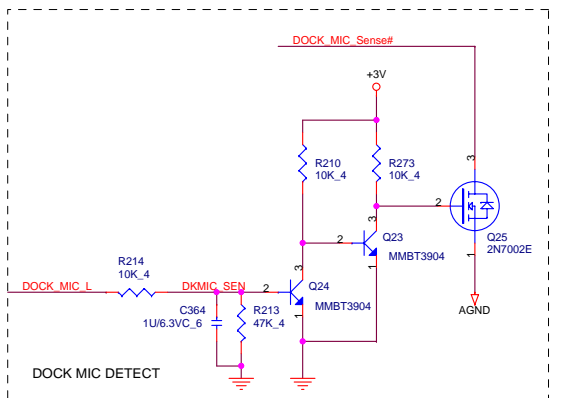
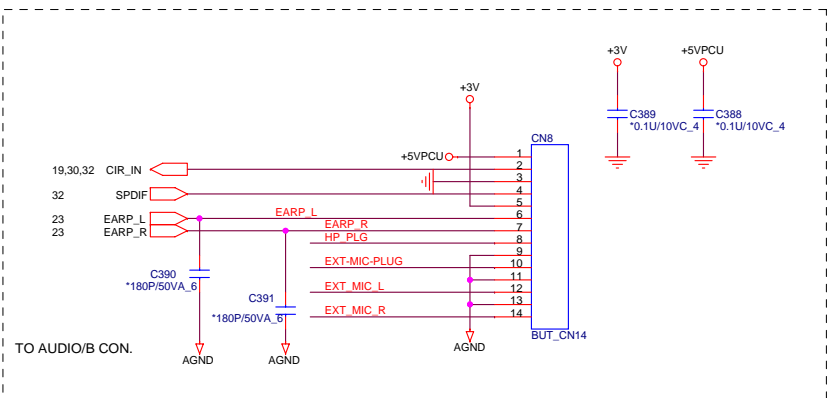
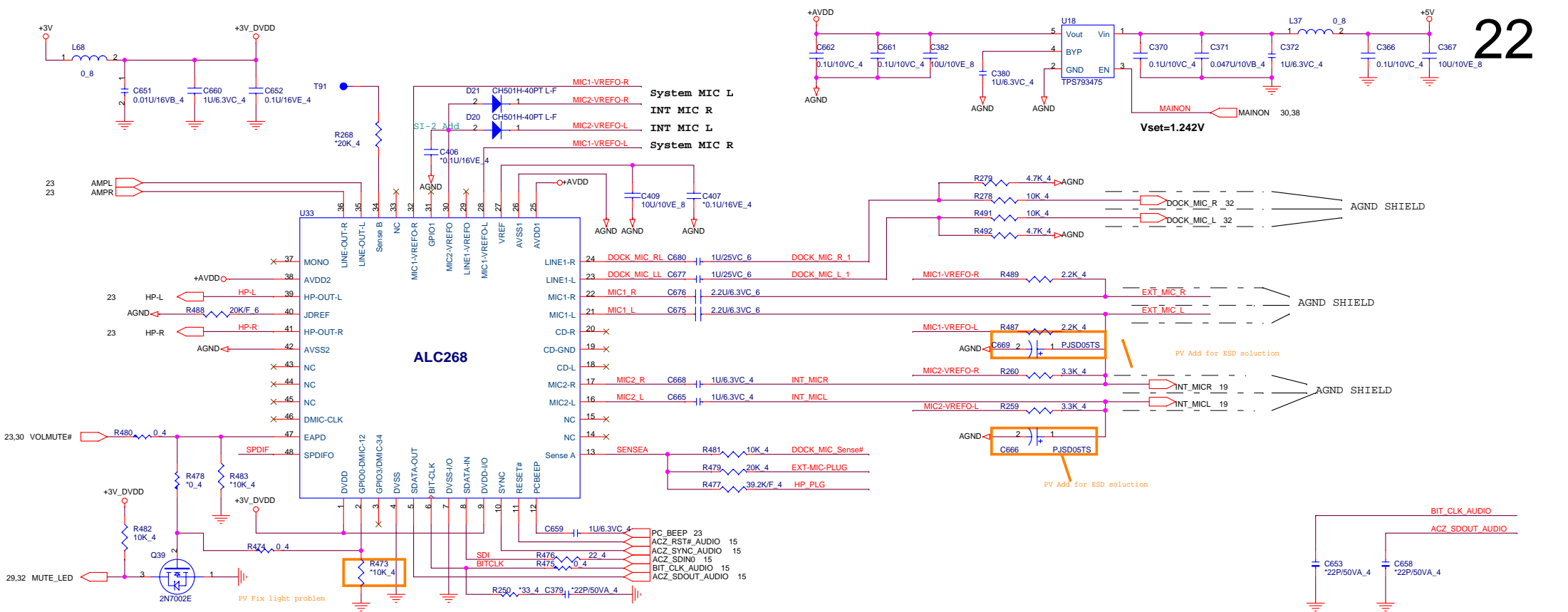


Remove Acces from HP information

+3VSUS 15,24,25,29,31,33,34,35,36,38

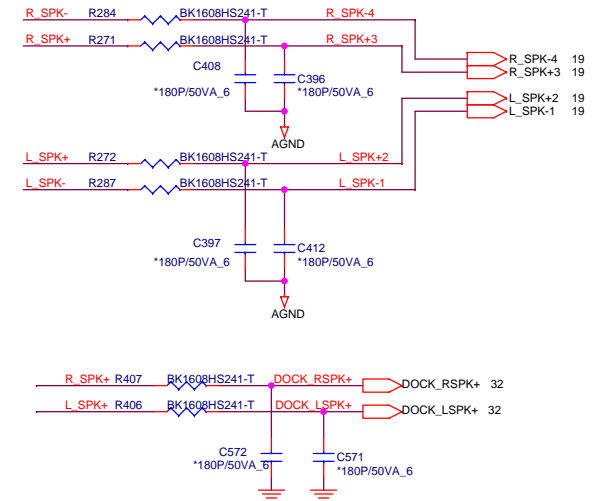


PROJECT : TT9  
Quanta Computer Inc.

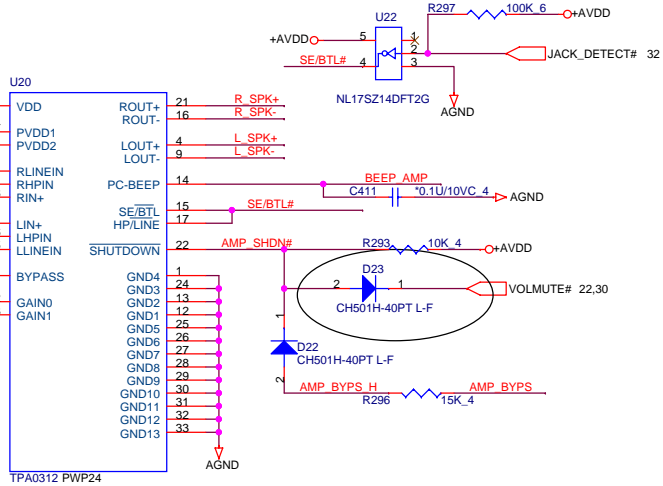


- +3V 4, 5, 7, 8, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 23, 26, 28, 29, 30, 31, 33, 34, 38
- +5V 17, 19, 20, 23, 28, 31, 32, 33, 37, 38, 39
- +AVDD 23
- +5VPCU 19, 28, 29, 30, 33, 34, 35, 36, 37

INT. SPEAKER

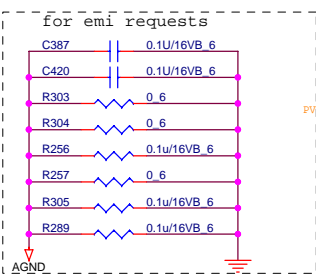


AUDIO AMPLIFIER

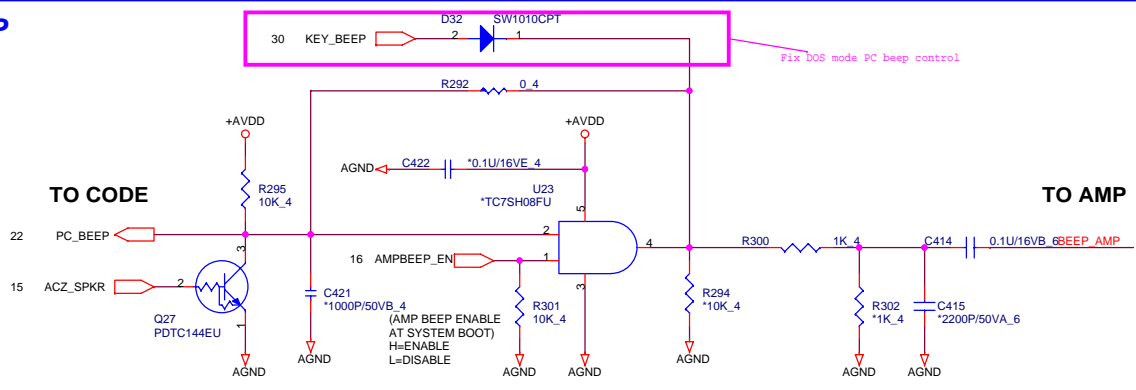


0312 Gain Table

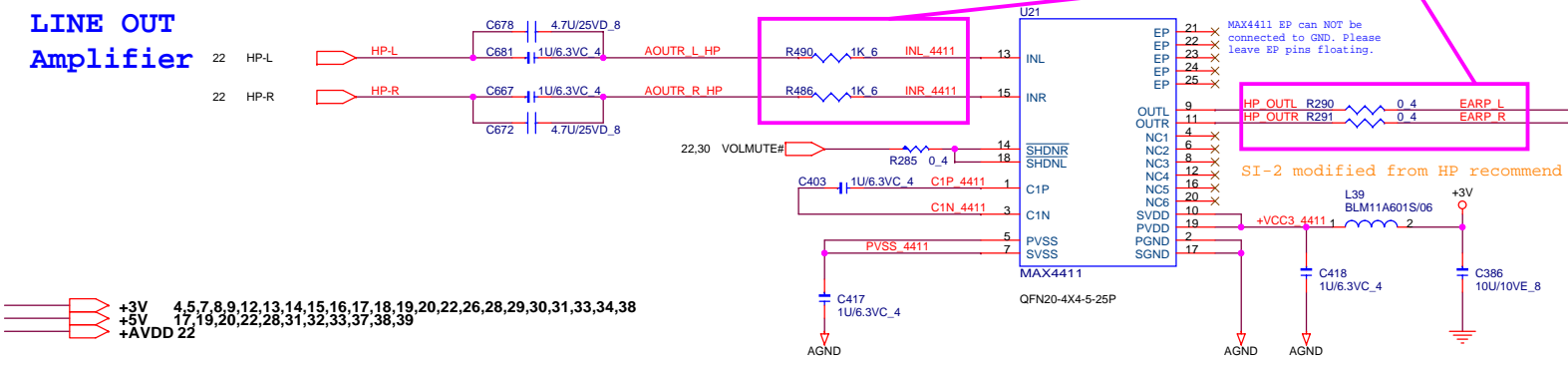
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



PCSPK BEEP



LINE OUT Amplifier



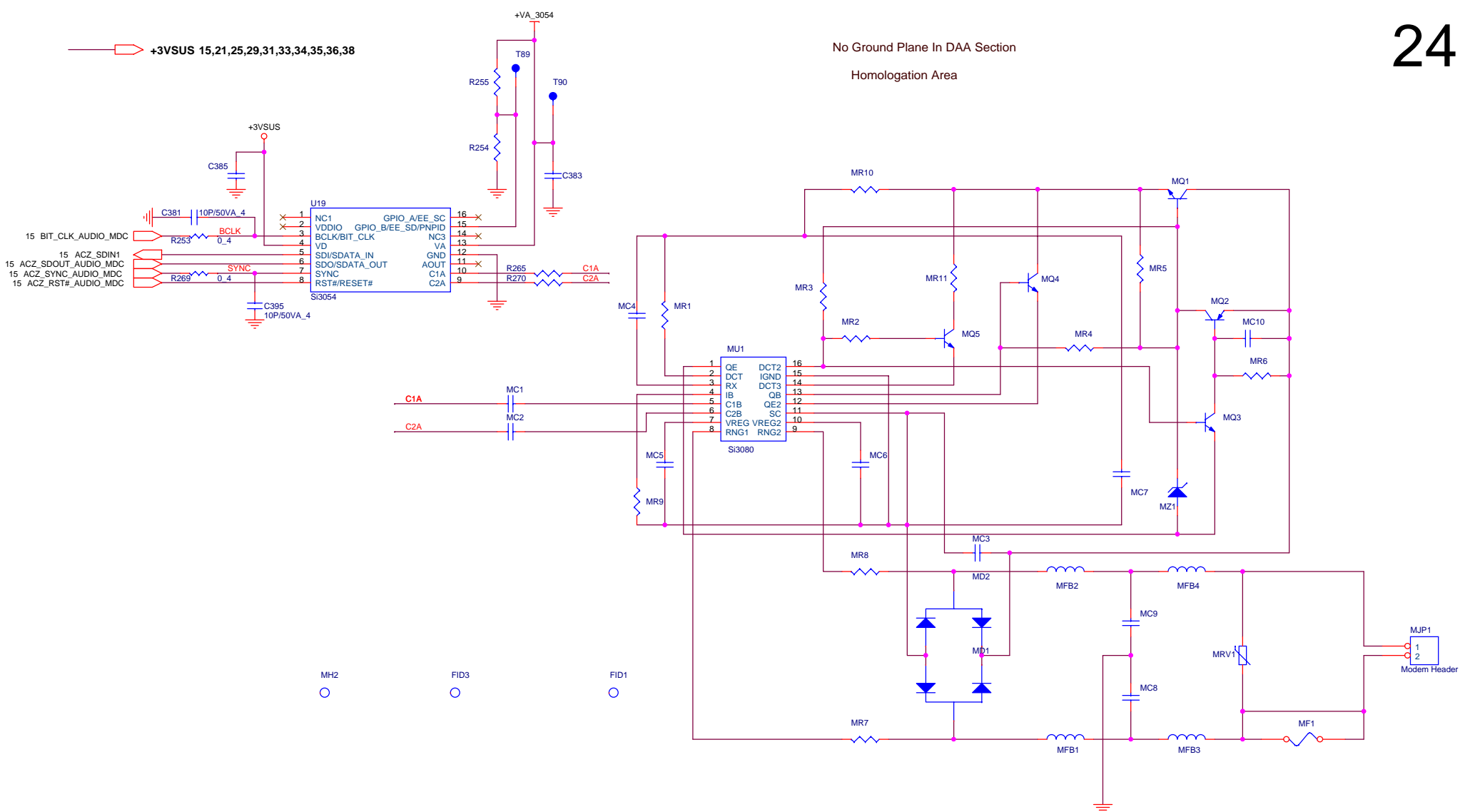
- +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,26,28,29,30,31,33,34,38
- +5V 17,19,20,22,28,31,32,33,37,38,39
- +AVDD 22

**PROJECT : TT9**  
Quanta Computer Inc.

Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 23 of 41		

No Ground Plane In DAA Section

Homologation Area

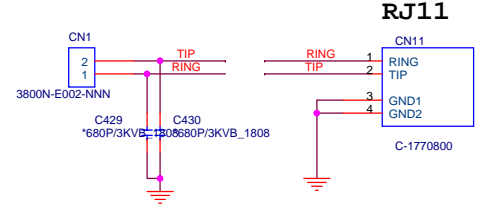



15 BIT\_CLK\_AUDIO\_MDC  
 15 ACZ\_SDIN1  
 15 ACZ\_SDOUT\_AUDIO\_MDC  
 15 ACZ\_SYNC\_AUDIO\_MDC  
 15 ACZ\_RST#\_AUDIO\_MDC

MH2  
 FID3  
 FID1

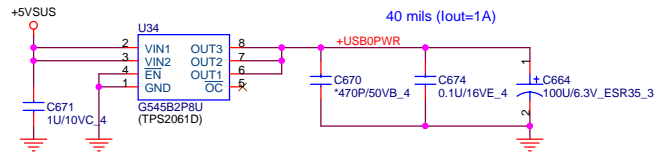
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

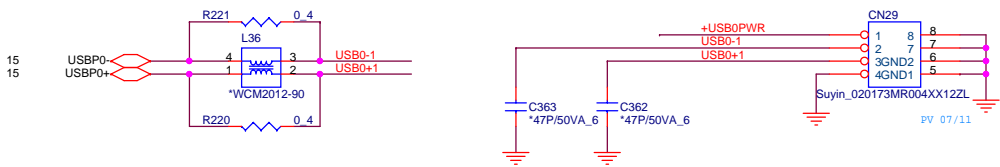


 NB5/RD2/HW1	<b>PROJECT : TT9</b> Quanta Computer Inc.		Rev 1A
	Size Custom Date: Wednesday, January 23, 2008	Document Number MODEM (DAA)	Sheet 24 of 41

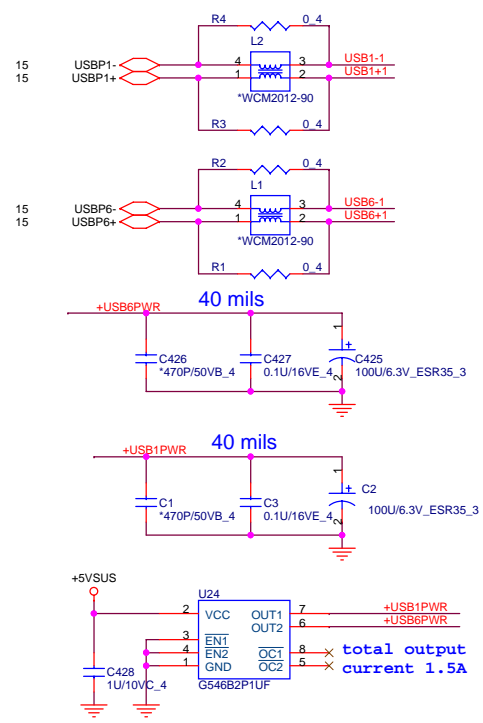
# USBX1



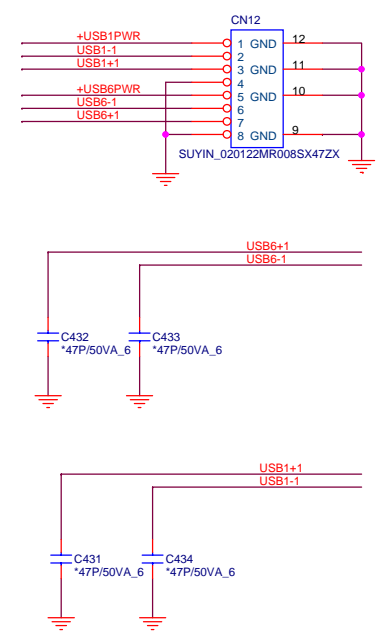
# USB 0



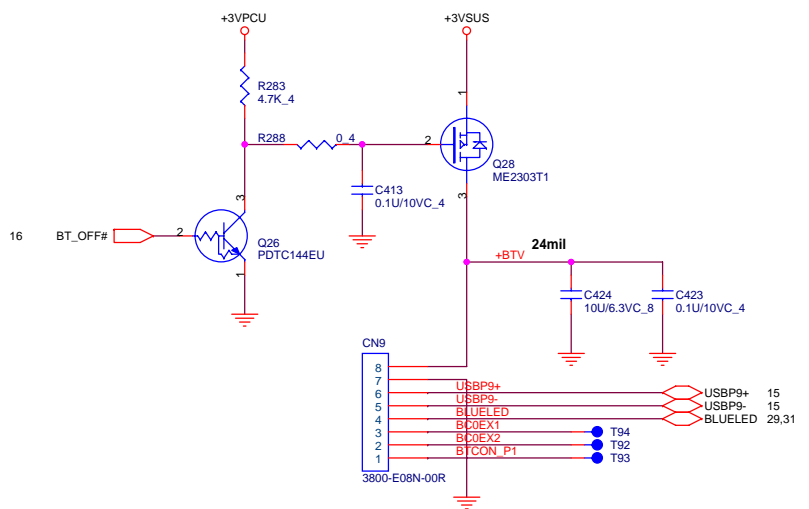
# USBX2



# USB 1 & 6



# BLUETOOTH

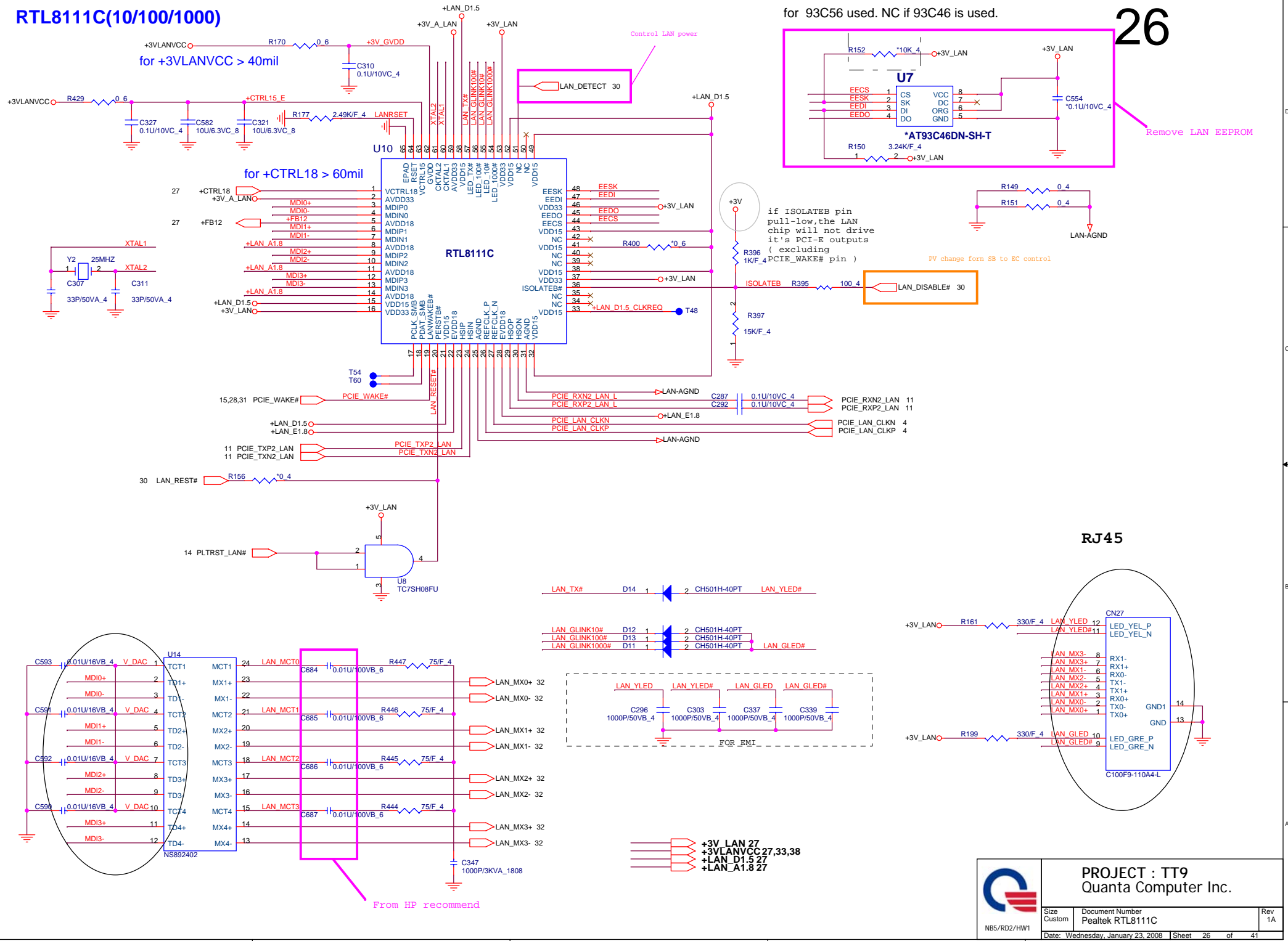


Select TPM function from HP information

- +3VPCU 5,14,19,29,30,32,33,35,37,39
- +3VSUS 15,21,24,29,31,33,34,35,36,38
- +5VSUS 19,30,32,33,38

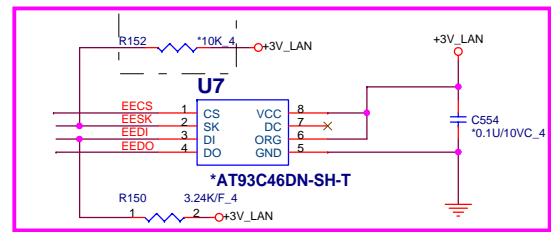
		PROJECT : TT9	
		Quanta Computer Inc.	
Size Custom	Document Number Blue Tooth/USBX3	Rev 1A	
Date: Wednesday, January 23, 2008		Sheet 25	of 41

# RTL8111C(10/100/1000)

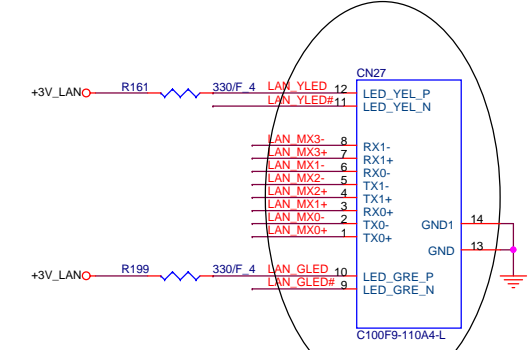


for 93C56 used. NC if 93C46 is used.

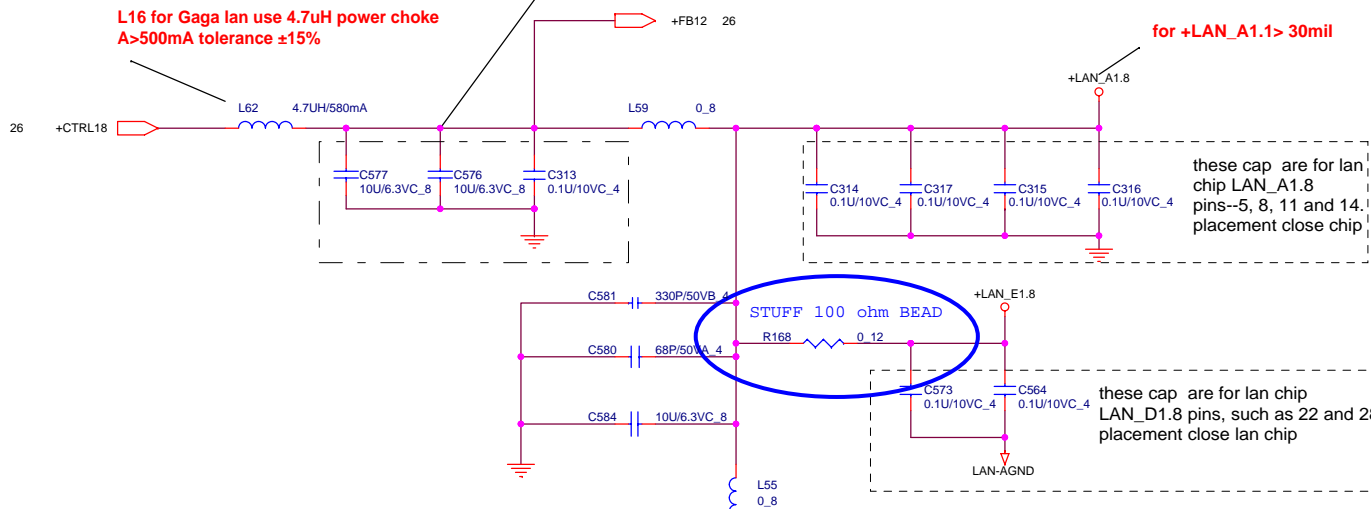
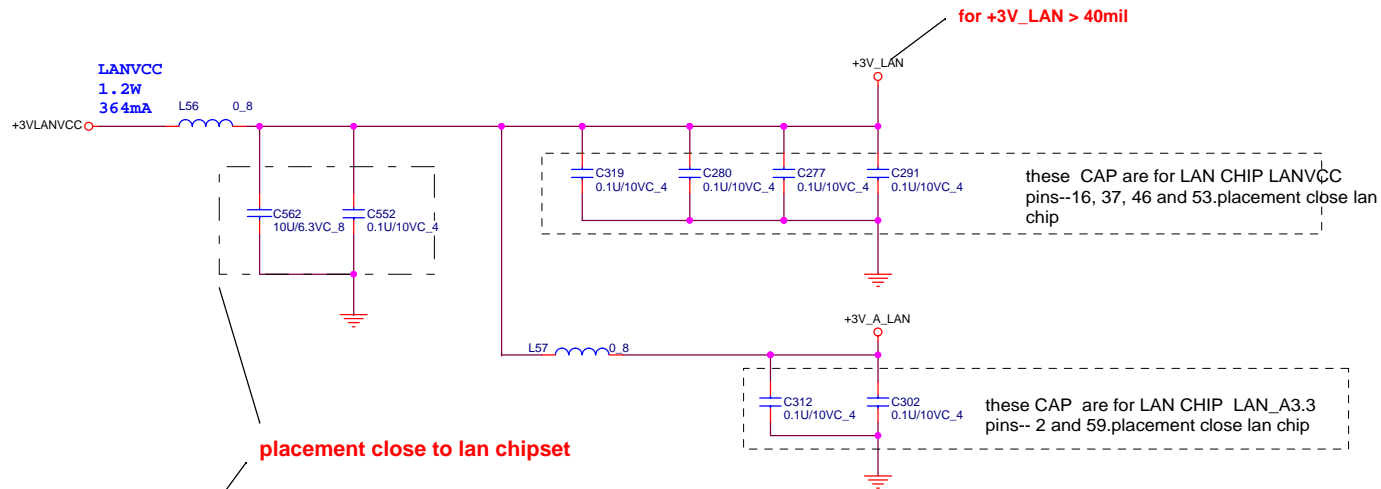
# 26



## RJ45

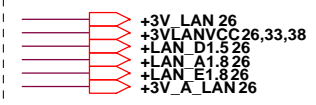
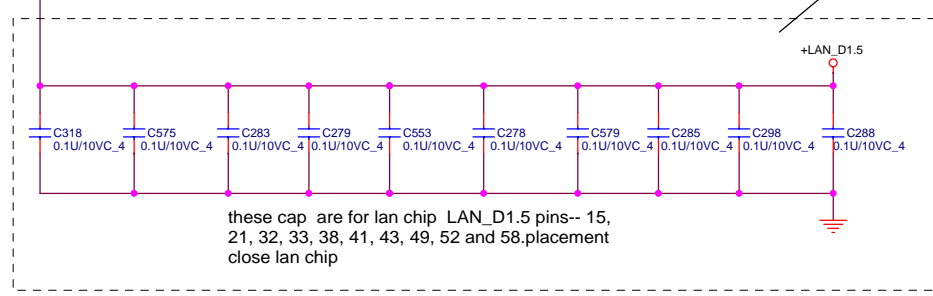






RTL8111C Power domain chart

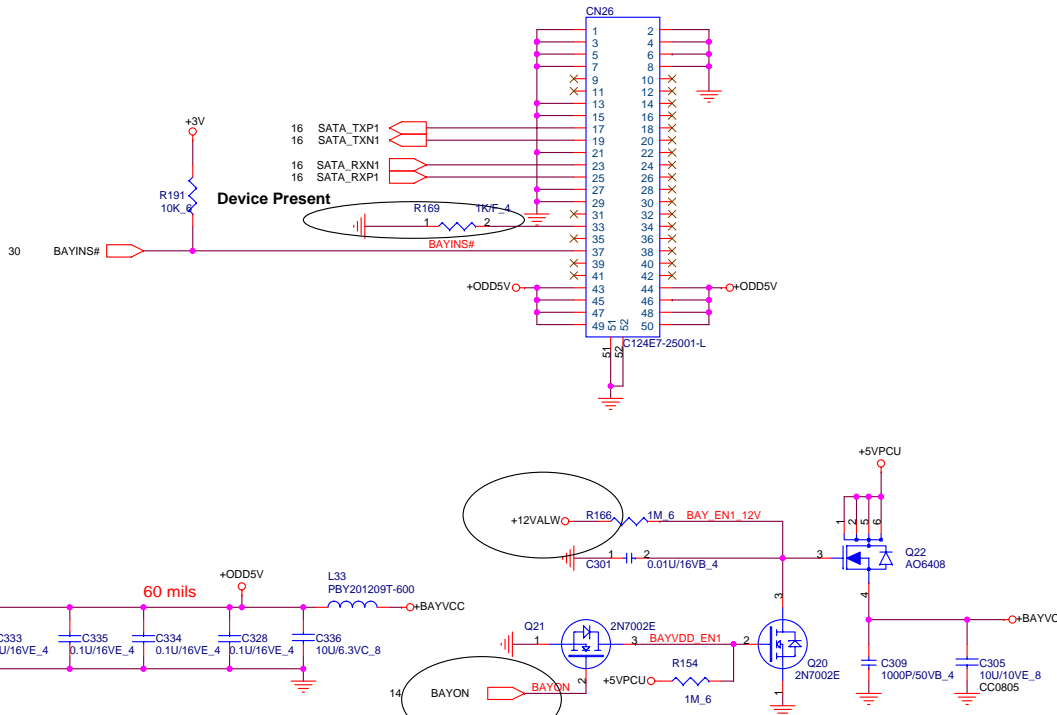
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V



PROJECT : TT9  
Quanta Computer Inc.

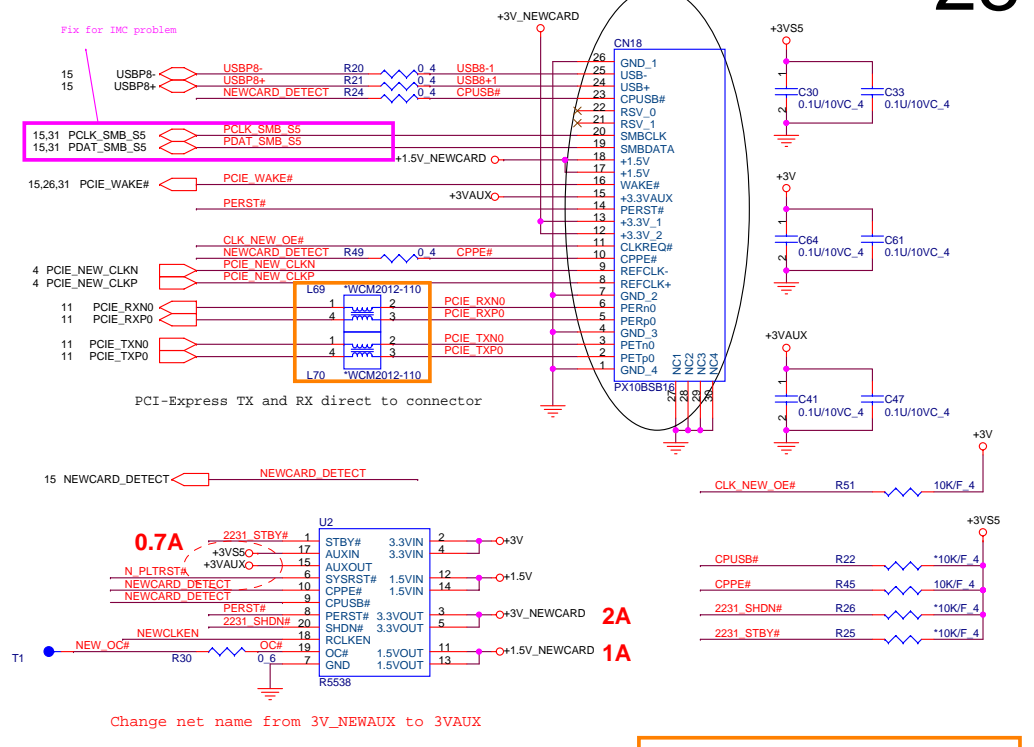
Size A3	Document Number LAN POWER	Rev 1A
Date: Wednesday, January 23, 2008   Sheet 27 of 41		

### SATA ODD

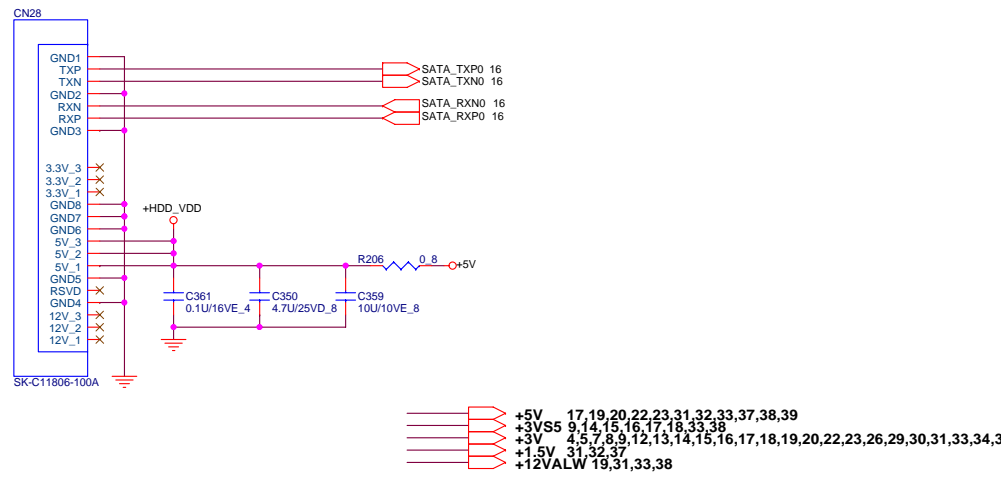


### NEWCARD

### NEWCARD (PCIEXPRESS\*1 + USB\*1)



### SATA CONNECTOR

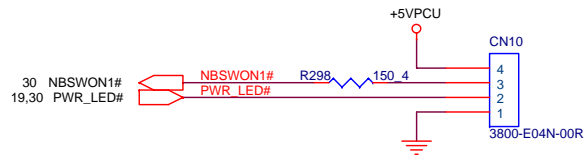


**PROJECT : TT9**  
Quanta Computer Inc.

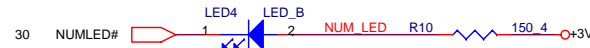
Size Custom	Document Number NEW_CARD/SATA ODD/SATA HDD	Rev 1A
Date: Wednesday, January 23, 2008   Sheet 28 of 41		

NBS/RD2/HW1

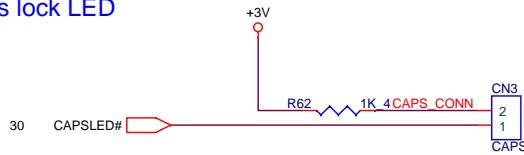
## FOR POWER ON SW BOARD



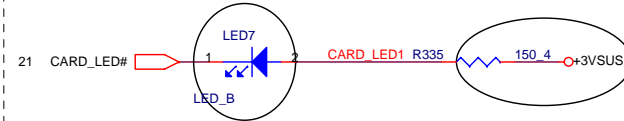
## Num lock LED



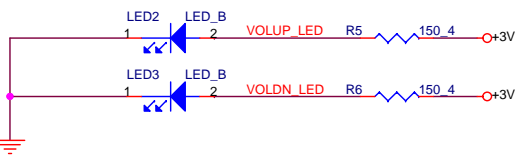
## Caps lock LED



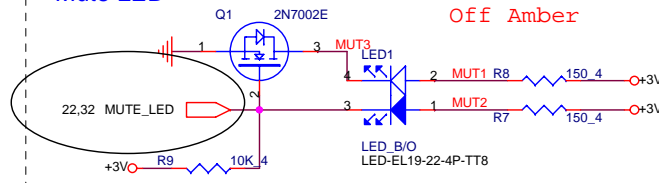
## Card Reader LED



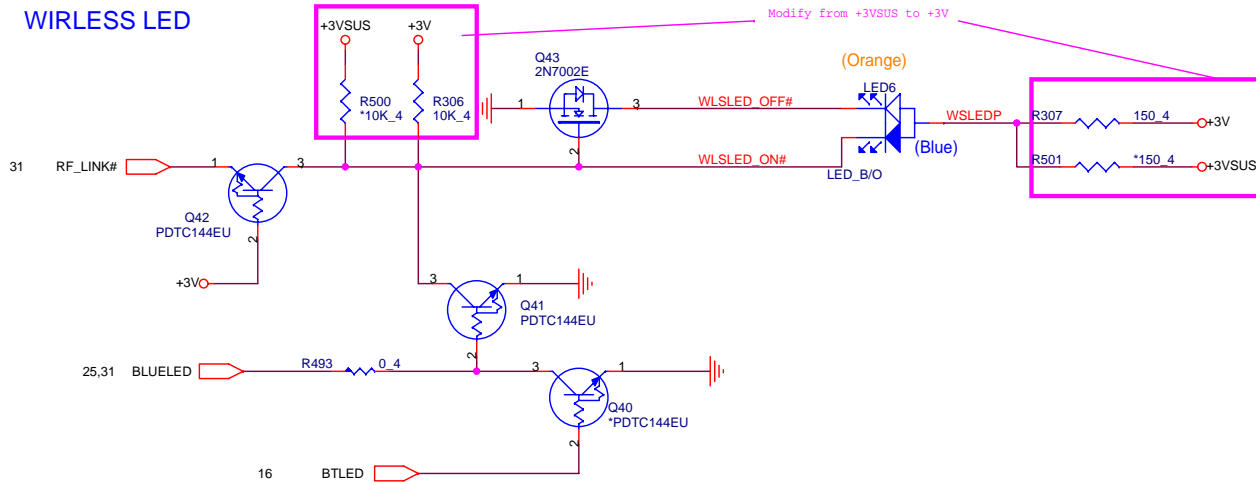
## Volume up/down LED



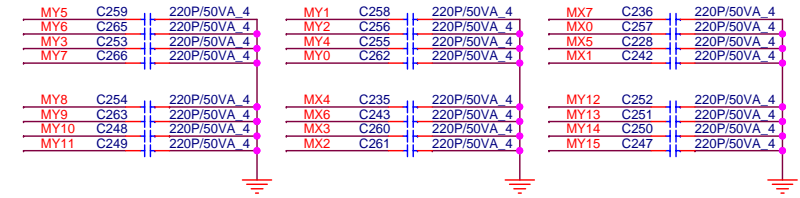
## Mute LED



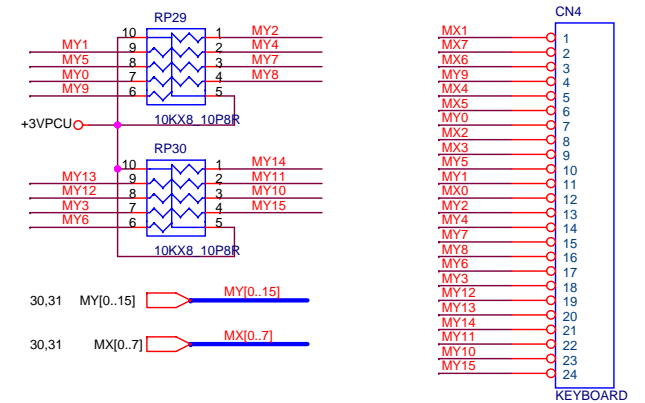
## WIRLESS LED



## Keyboard



## KEYBOARD PULL-UP

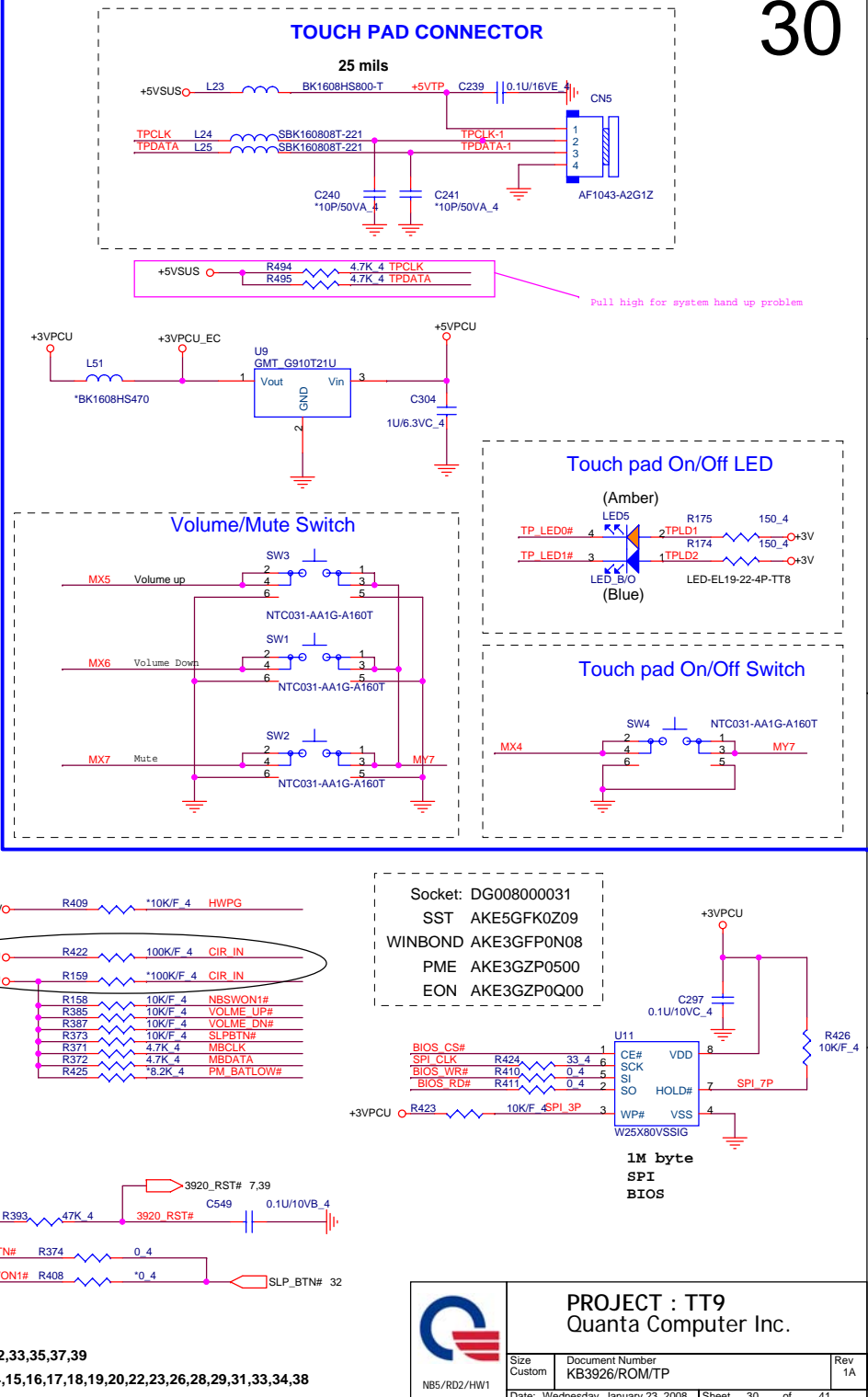
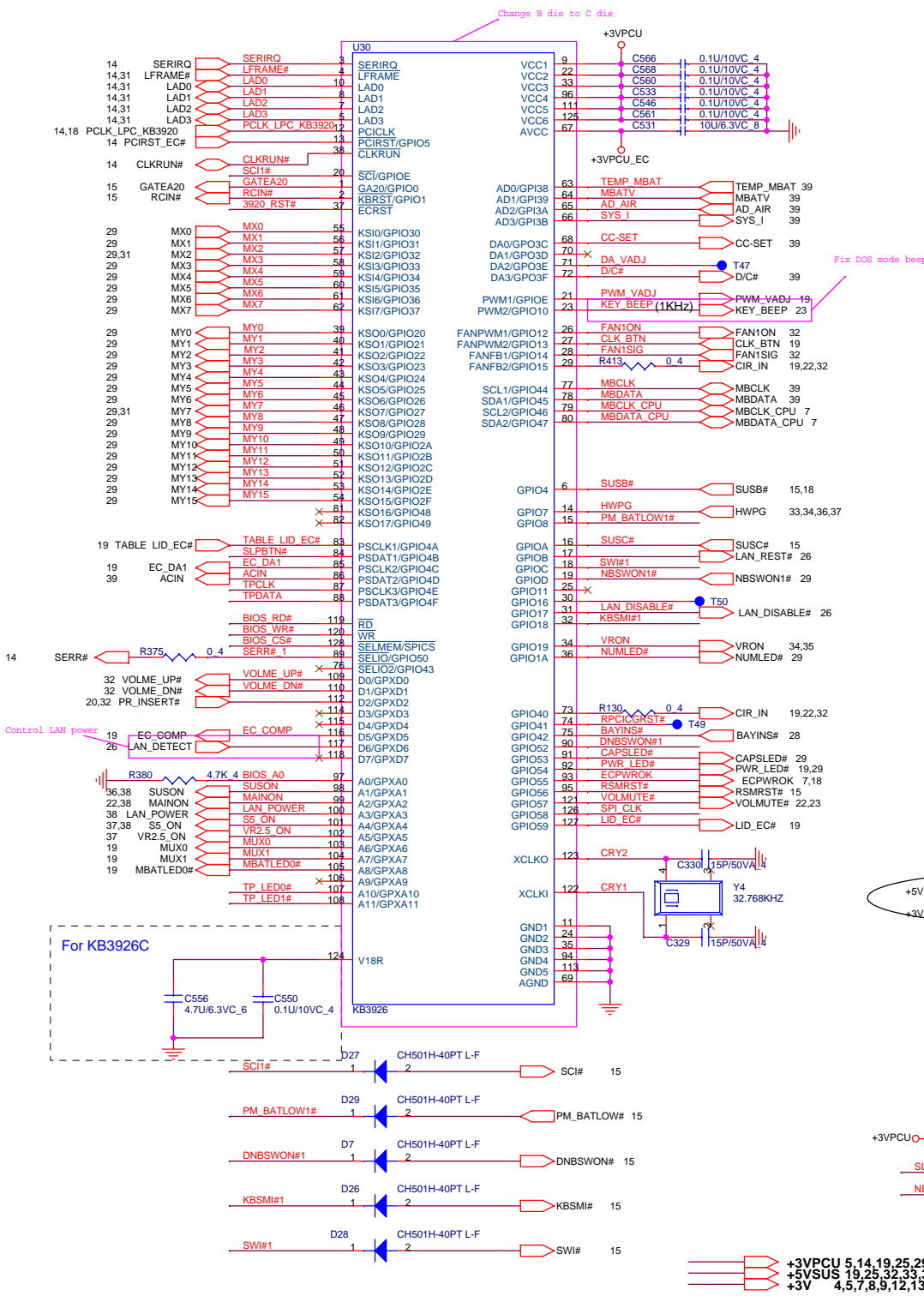


+5VPCU 19,22,28,30,33,34,35,36,37  
 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38  
 +3VSUS 15,21,24,25,31,33,34,35,36,38



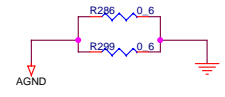
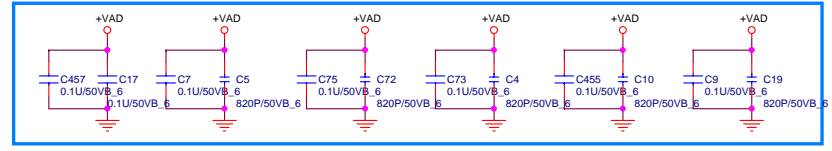
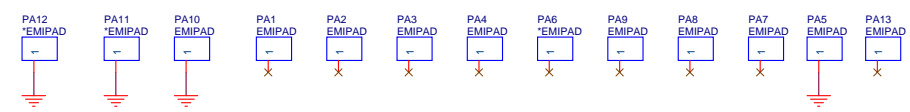
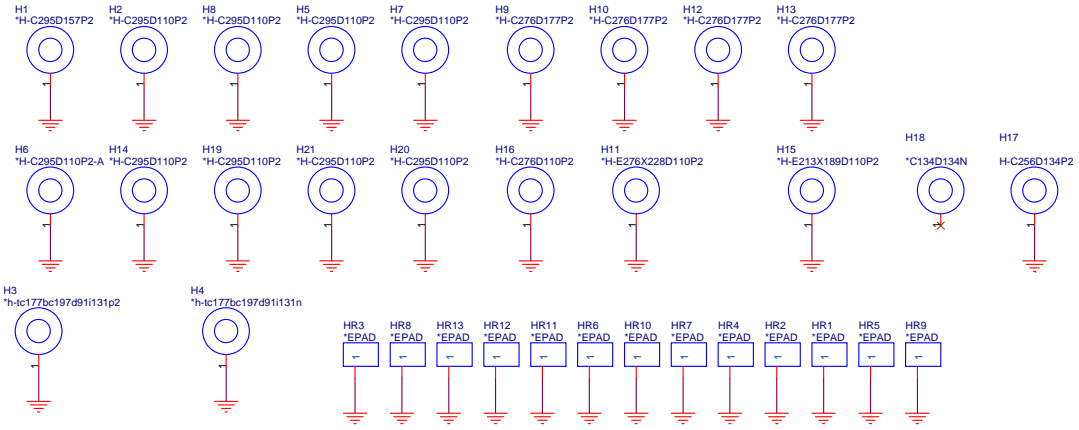
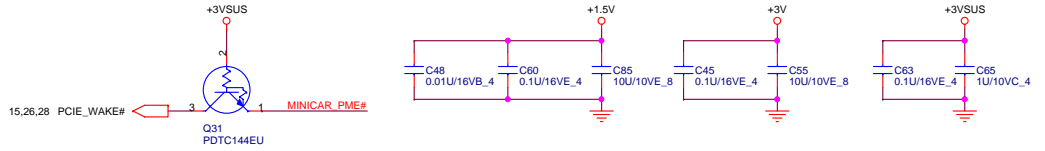
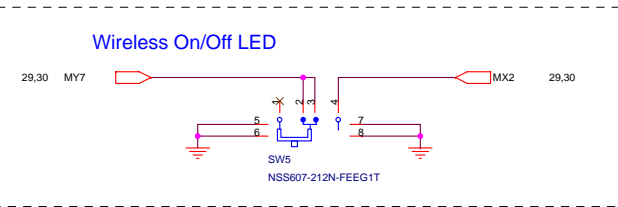
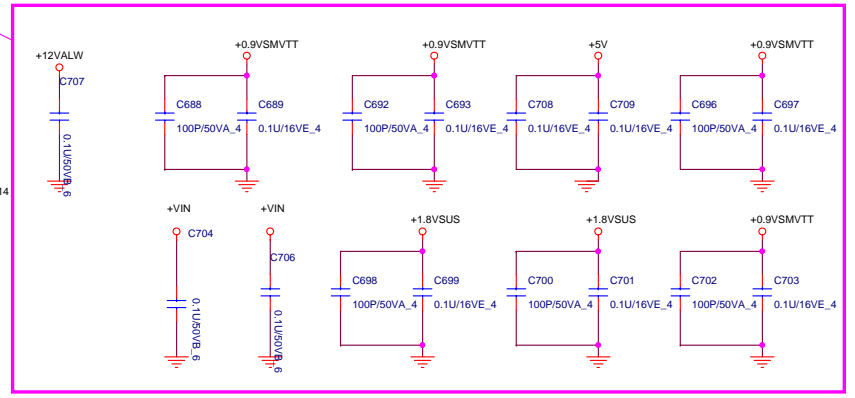
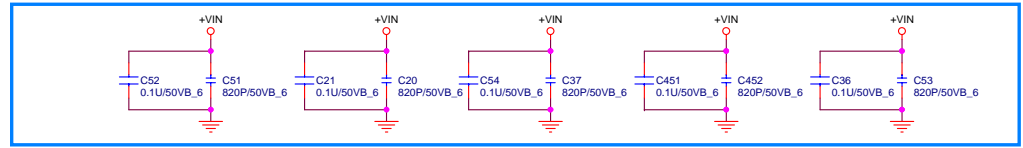
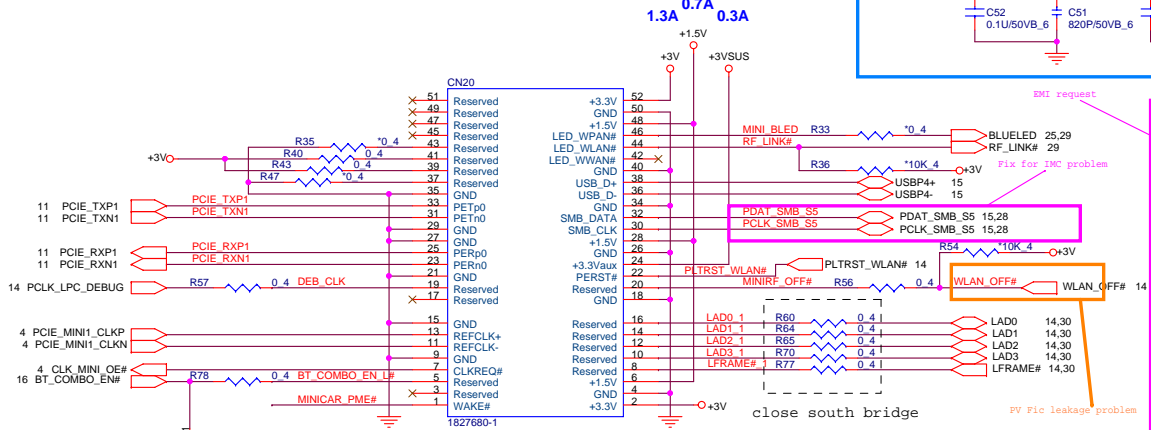
PROJECT : TT9  
Quanta Computer Inc.

Size B	Document Number LED/KEYBOARD/SW	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 29 of 41		



+1.5V 28,32,37  
+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,33,34,38  
+3VSUS 15,21,24,25,29,33,34,35,36,38  
+VIN 32,33,34,35,36,38,39

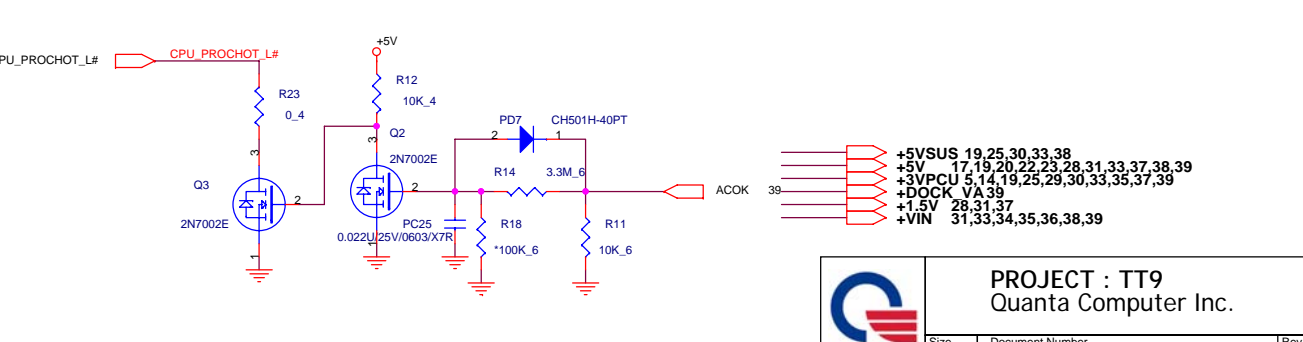
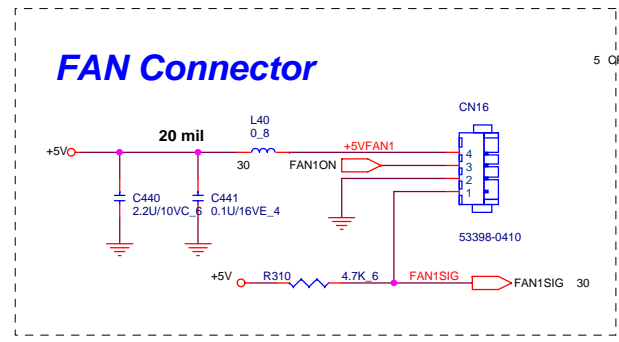
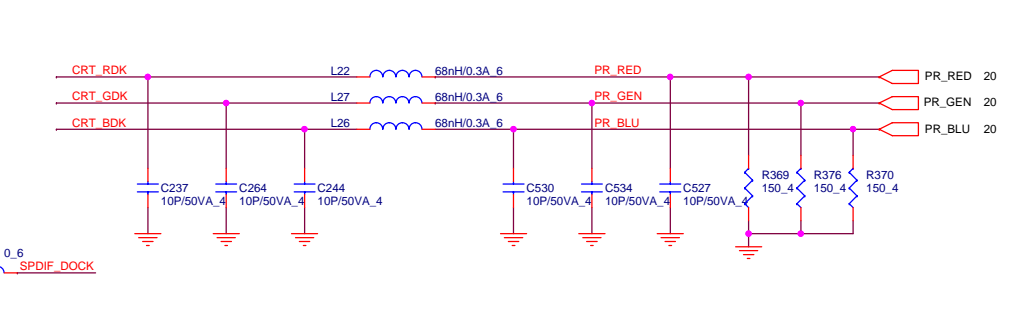
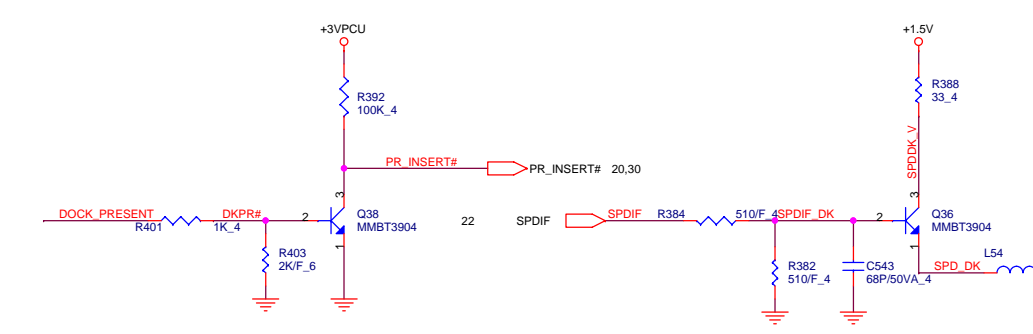
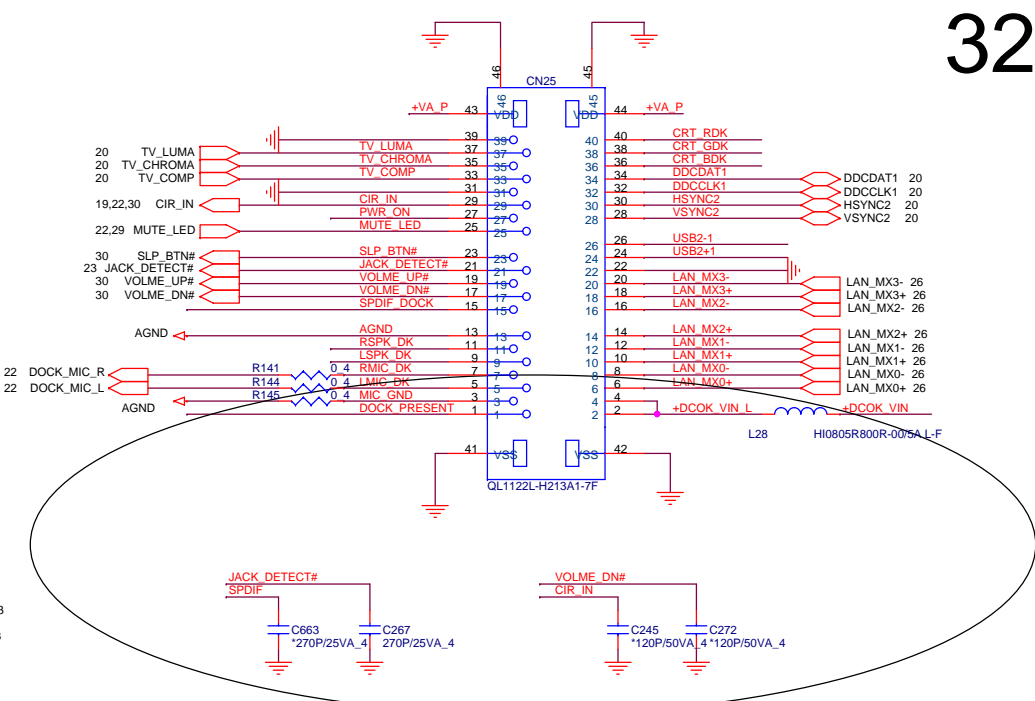
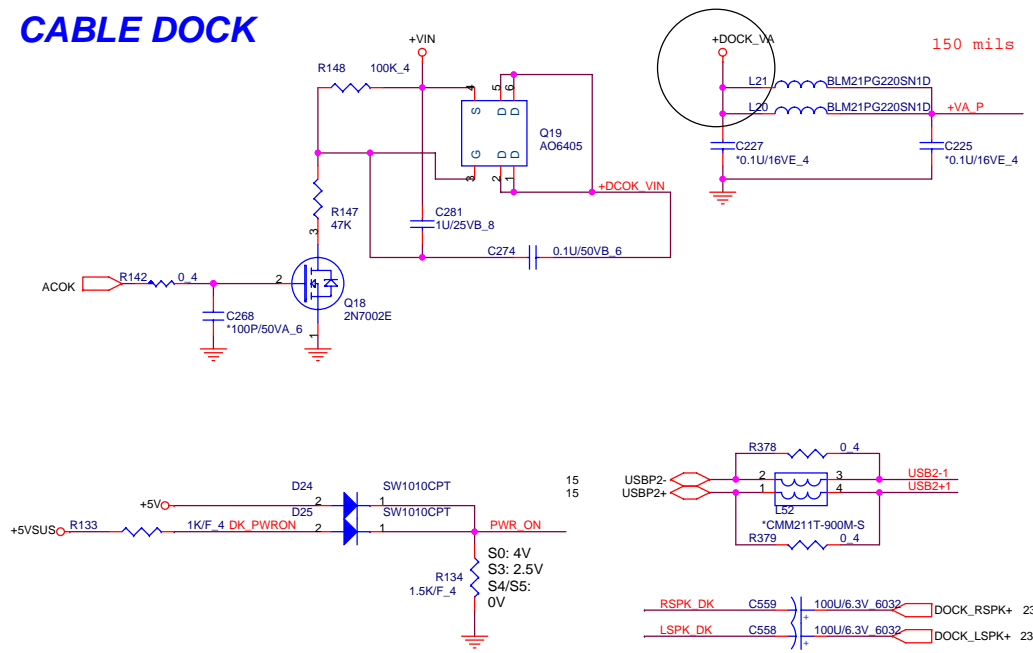
# Mini PCI-E Card 1 WLAN



**PROJECT : TT9**  
Quanta Computer Inc.

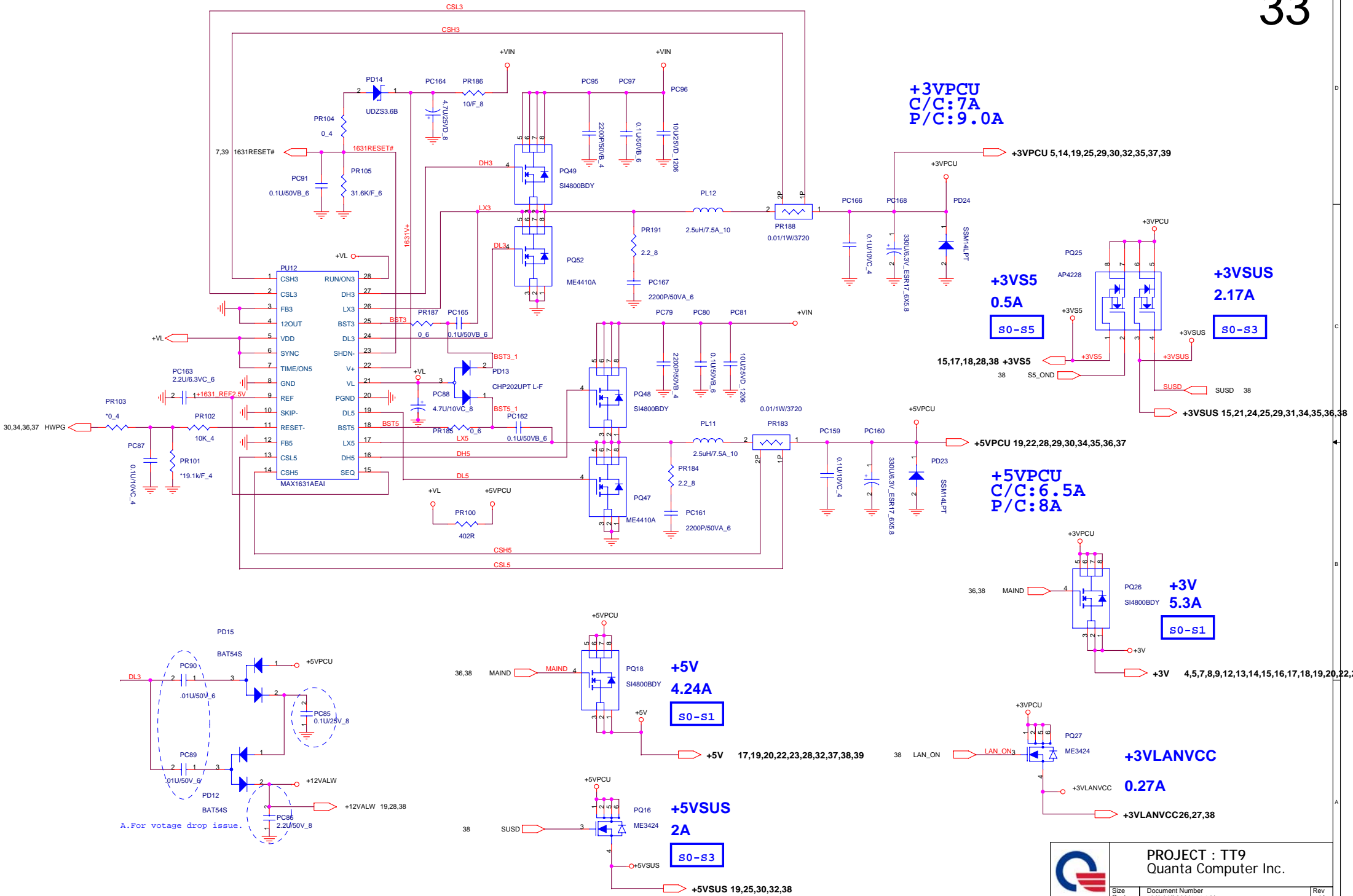
Size Custom	Document Number Mini CARD/Hole	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 31 of 41		

# CABLE DOCK



- +5VSUS 19, 25, 30, 33, 38
- +5V 17, 19, 20, 22, 23, 28, 31, 33, 37, 38, 39
- +3VPCU 5, 14, 19, 25, 29, 30, 33, 35, 37, 39
- +DOCK\_VA 39
- +1.5V 28, 31, 37
- +VIN 31, 33, 34, 35, 36, 38, 39

	PROJECT : TT9 Quanta Computer Inc.	
	Size Custom	Document Number CABLE DOCKING
NB5/RD2/HW1		Date: Wednesday, January 23, 2008 Sheet 32 of 41



**+3VPCU**  
C/C: 7A  
P/C: 9.0A

**+3VS5**  
0.5A  
S0-S5

**+3VSUS**  
2.17A  
S0-S3

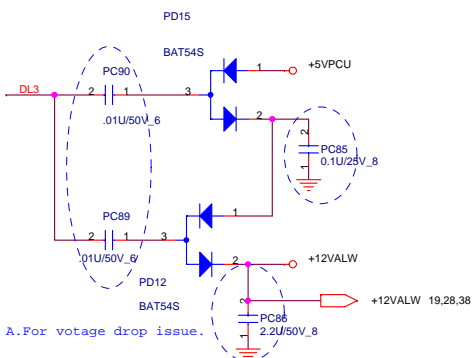
**+5VPCU**  
C/C: 6.5A  
P/C: 8A

**+3V**  
5.3A  
S0-S1

**+5V**  
4.24A  
S0-S1

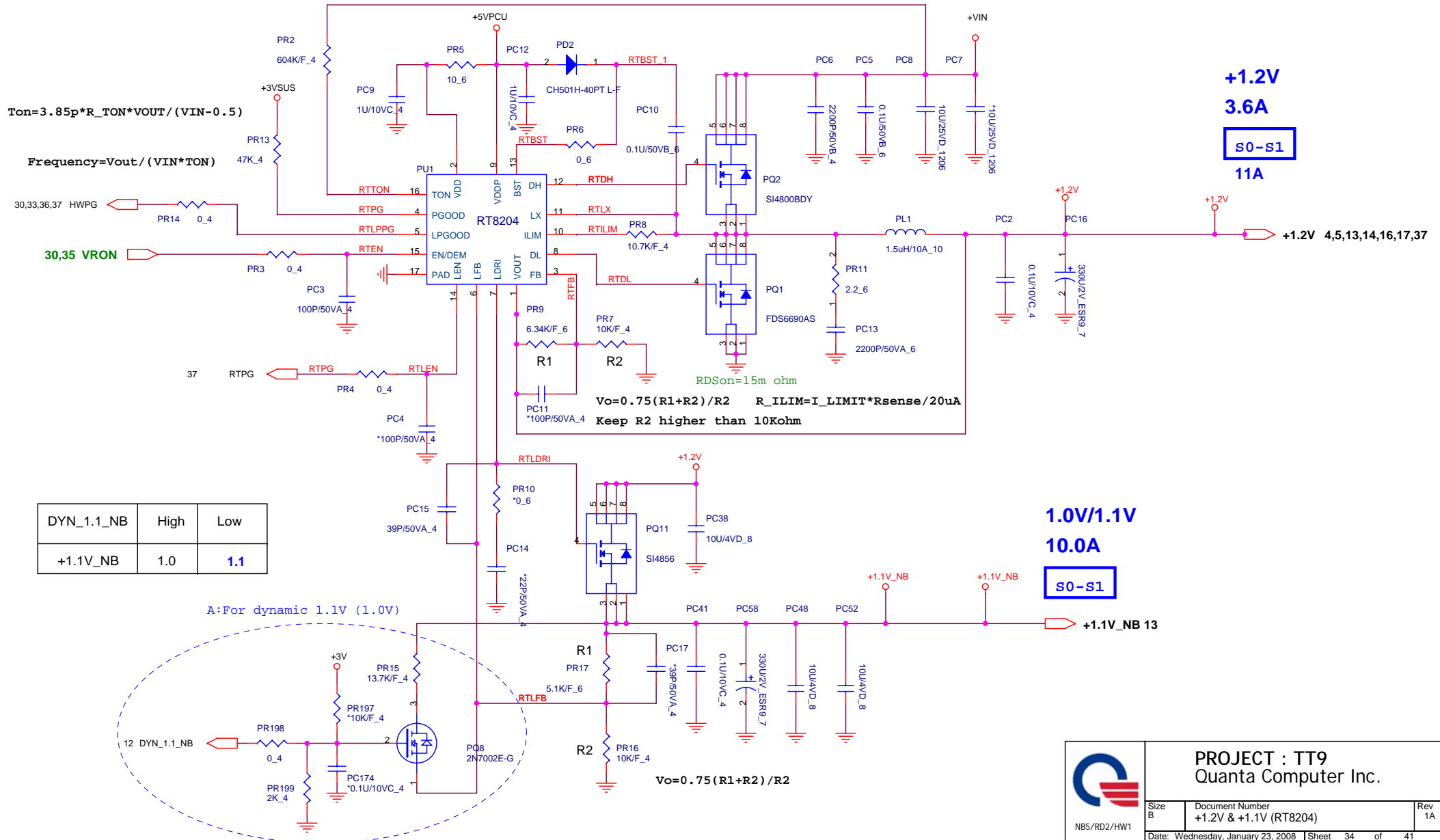
**+5VSUS**  
2A  
S0-S3


**+3VLANVCC**  
0.27A



		<b>PROJECT : TT9</b> Quanta Computer Inc.	
		Size Custom Document Number 3V/5V(MAX1631A)	Rev 1A
NBS/RD2/HW1		Date: Wednesday, January 23, 2008	Sheet 33 of 41







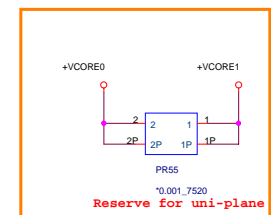
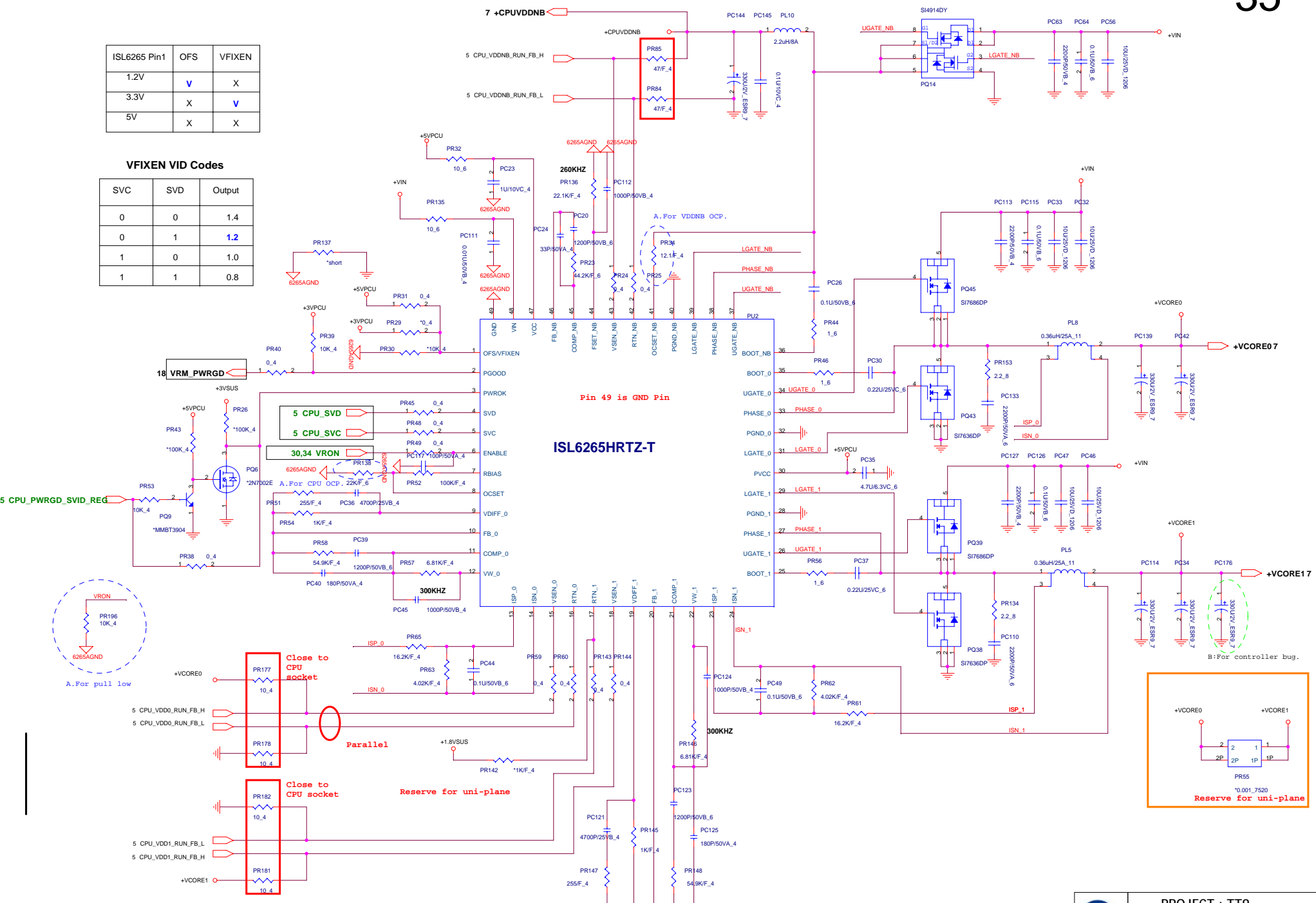
**PROJECT : TT9**  
Quanta Computer Inc.

Size B	Document Number +1.2V & +1.1V (RT8204)	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 34 of 41		

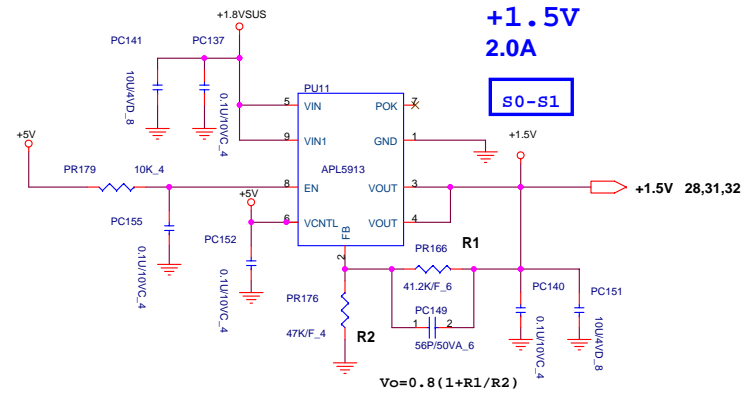
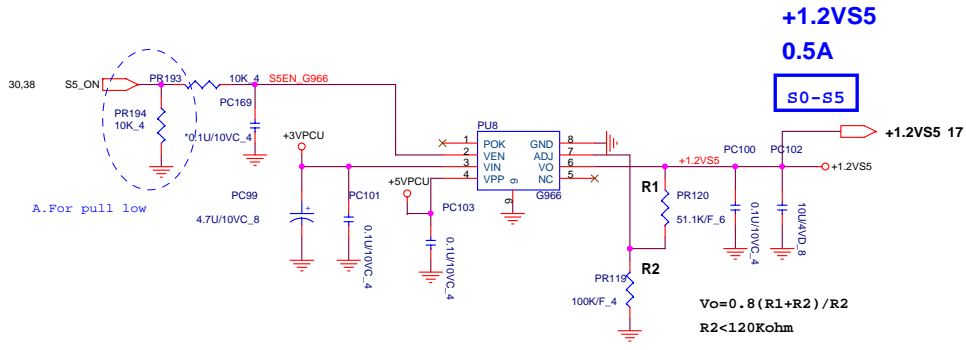
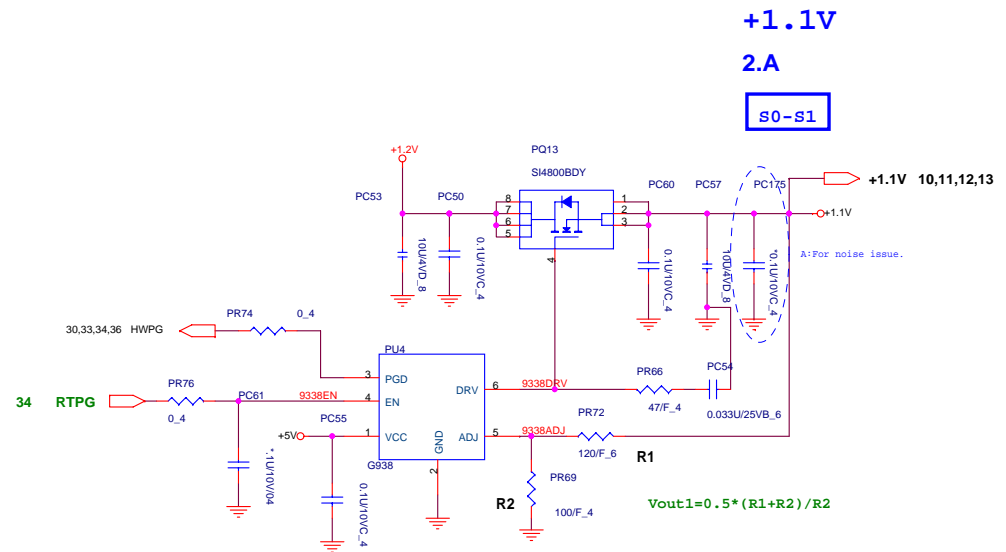
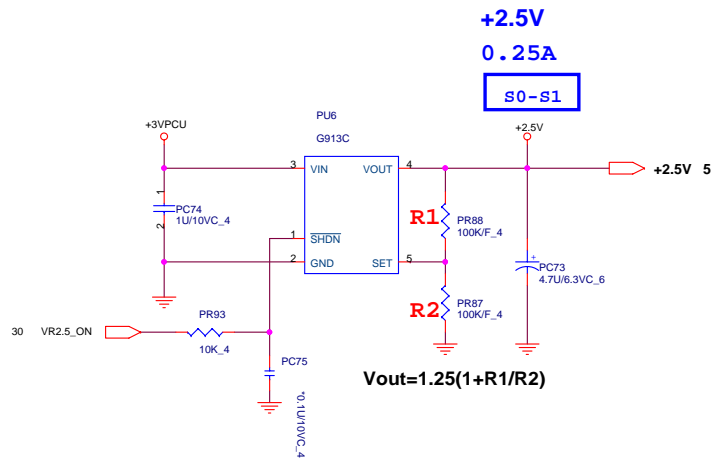
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

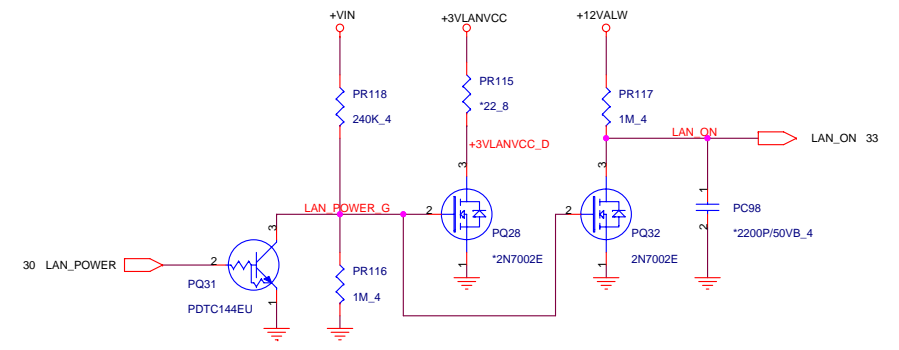
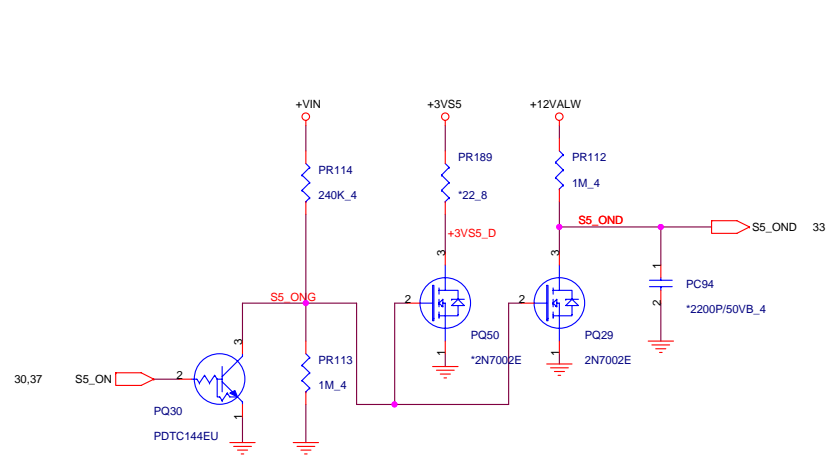
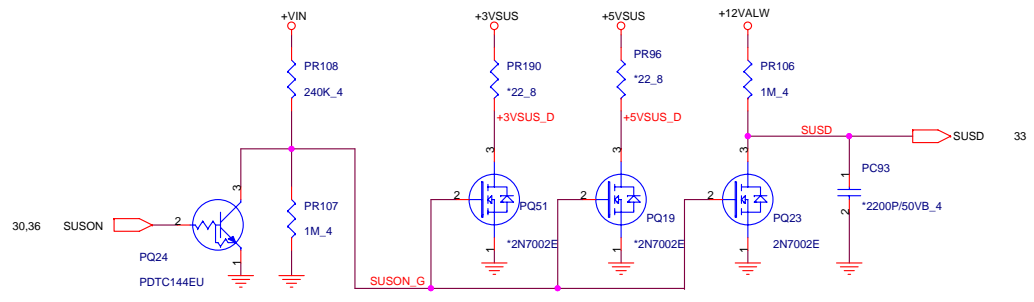
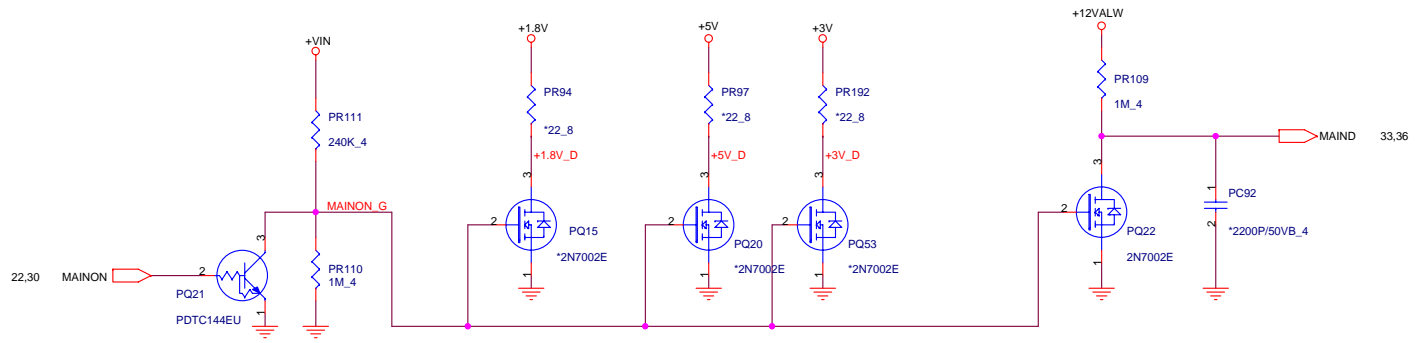
### VFIXEN VID Codes


SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



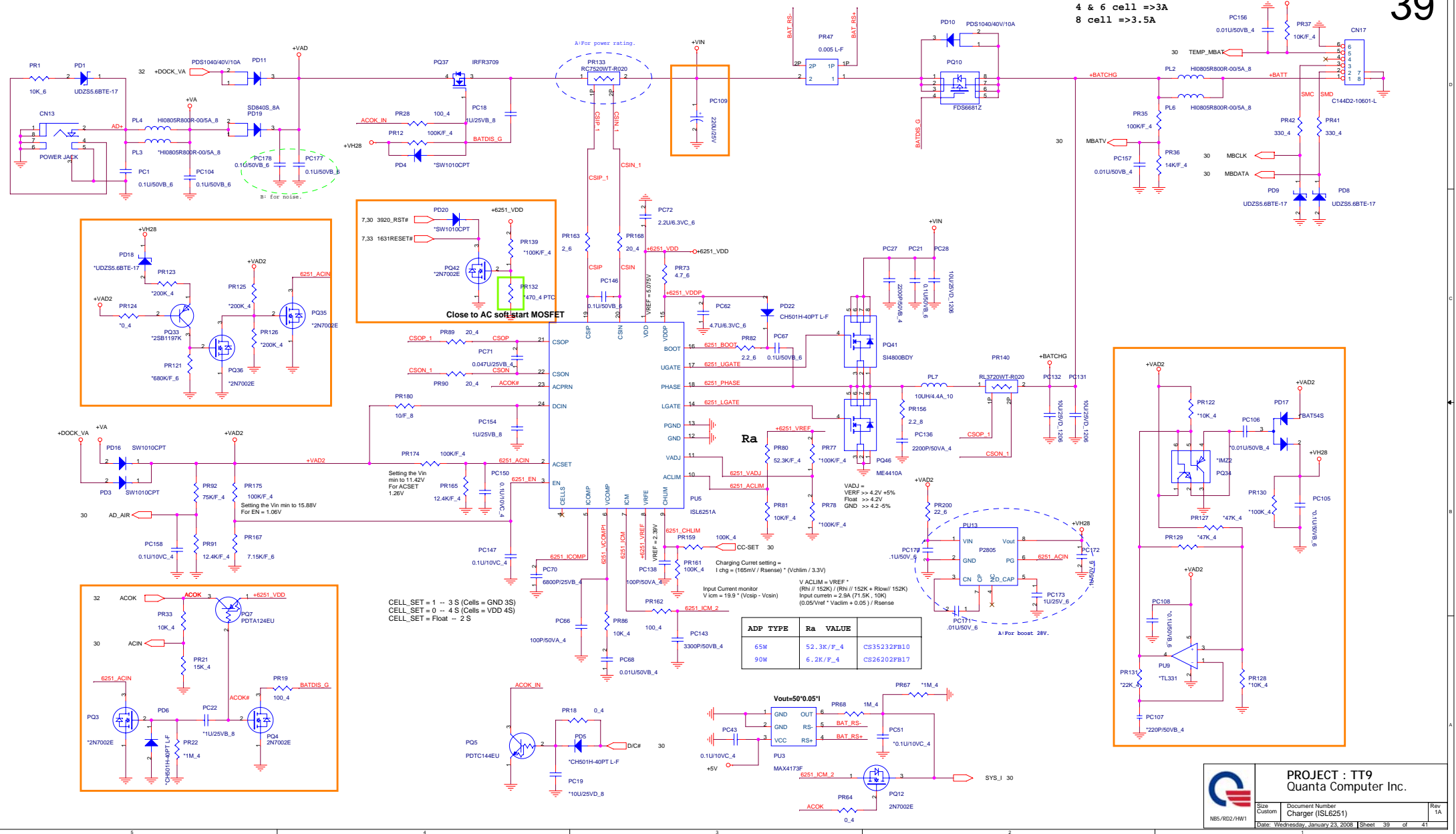






 NB5/RD2/HW1	<b>PROJECT : TT9</b> Quanta Computer Inc.	
	Size Custom Document Number DISCHARGE Date: Wednesday, January 23, 2008	Sheet 38 of 41

Charge current:  
4 & 6 cell =>3A  
8 cell =>3.5A



**PROJECT : TT9**  
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Size Custom	Document Number	Rev 1A
NBS/RDZ/RW1		Charger (ISL6251)
Date: Wednesday, January 23, 2008 Sheet 39 of 41		

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