

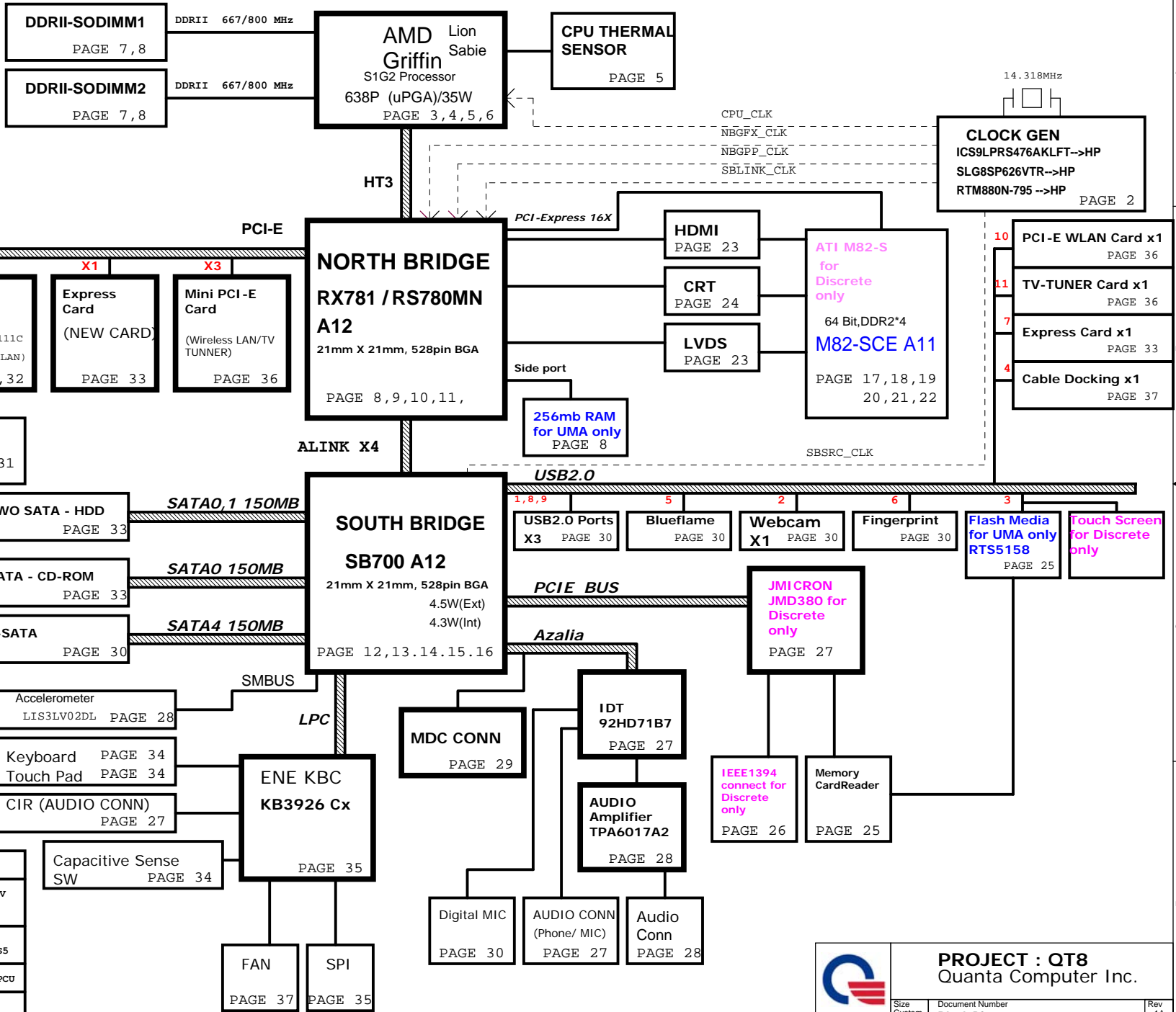
QT8 SYSTEM DIAGRAM



01

PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : IN1
 LAYER 3 : IN2
 LAYER 4 : VCC
 LAYER 5 : IN3
 LAYER 6 : BOT



Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 37

SYSTEM CHARGER(ISL6251A)
 PAGE 44

SYSTEM POWER ISL6236IRZA-T
 PAGE 38

DDR II SMD DR_VTERM 1.8V/1.8VSUS(TPS51116REGR)
 PAGE 41

VCCP +1.1V AND +1.2V(MAX8717)
 PAGE 39

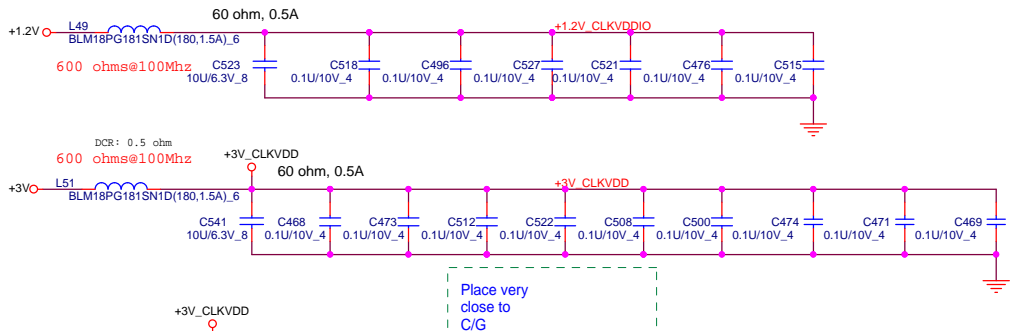
VGACORE(1.1V~1.2V)Oz8118
 PAGE 42

CPU CORE ISL6265A
 PAGE 40

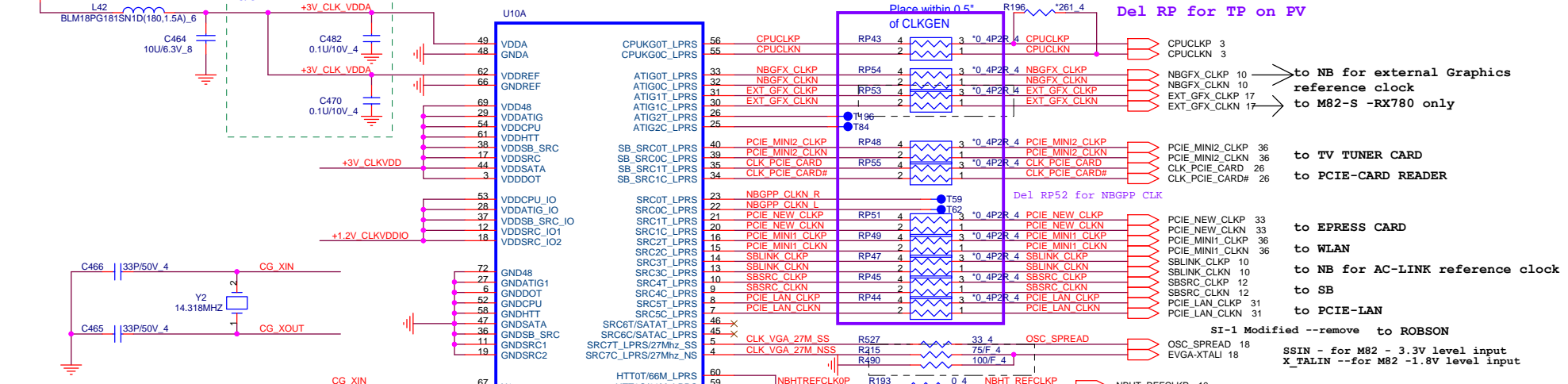
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	+3VS5
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

PROJECT : QT8
 Quanta Computer Inc.

Size Custom Document Number NBS/RD5
Block Diagram
 Date: Tuesday, February 19, 2008 Sheet 1 of 45 Rev 1A

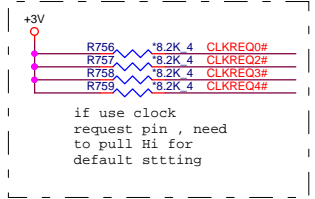
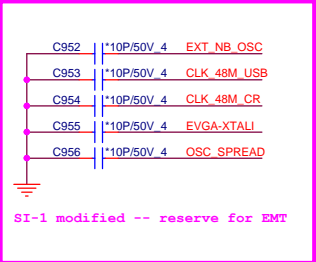


CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBPPP_CLKP NBPPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653, R656, R612 STUFF	R653, R656, R612 NC	To M82-S 27MHz - RX780 only



can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/80
power level

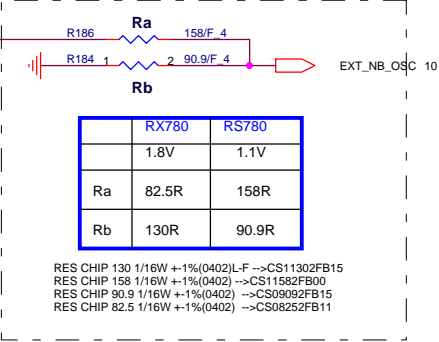
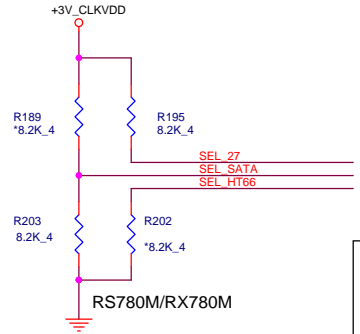
when driven low SB_SRC clocks slow only supported with
to reduced setpoint custom CG IC



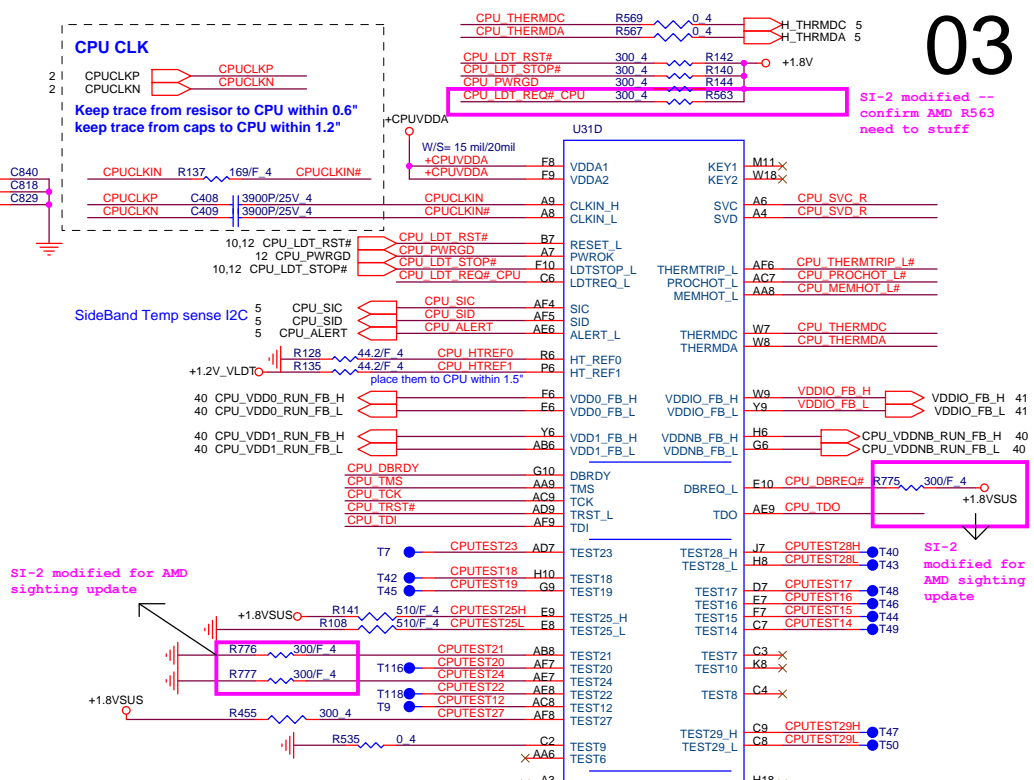
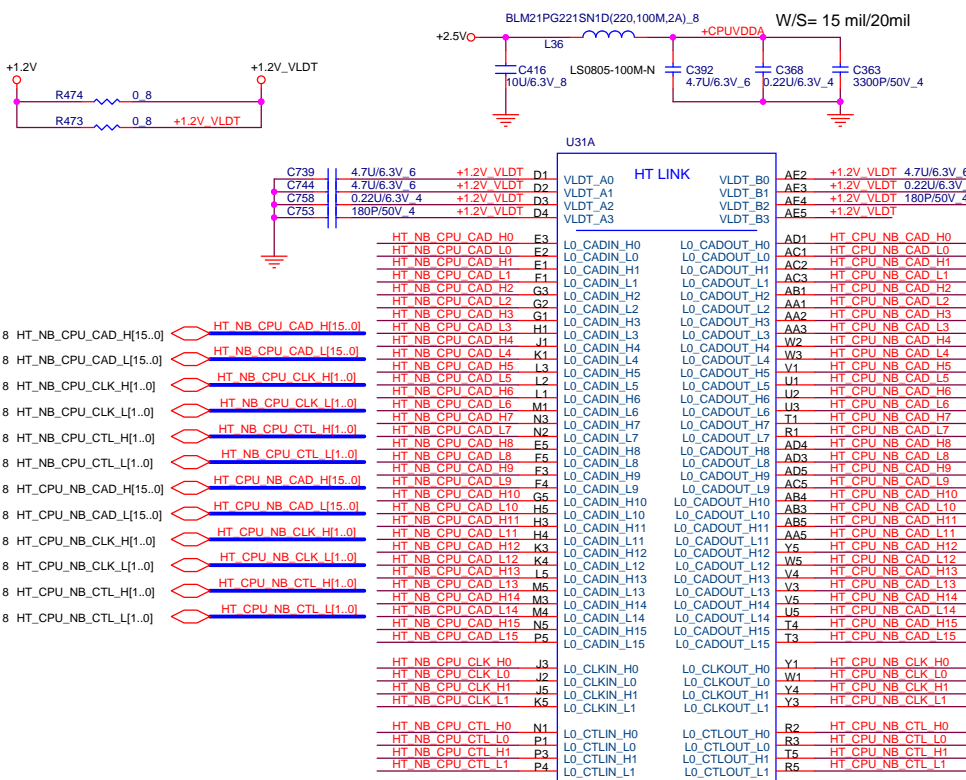
ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTL880N-795-- AJ008800000

* default	
SEL_HTT66	1
	0
SEL_SATA	1
	0
SEL_27	1
	0

Clock chip has internal serial terminations
for differential pairs, external resistors
are reserved for debug purpose.

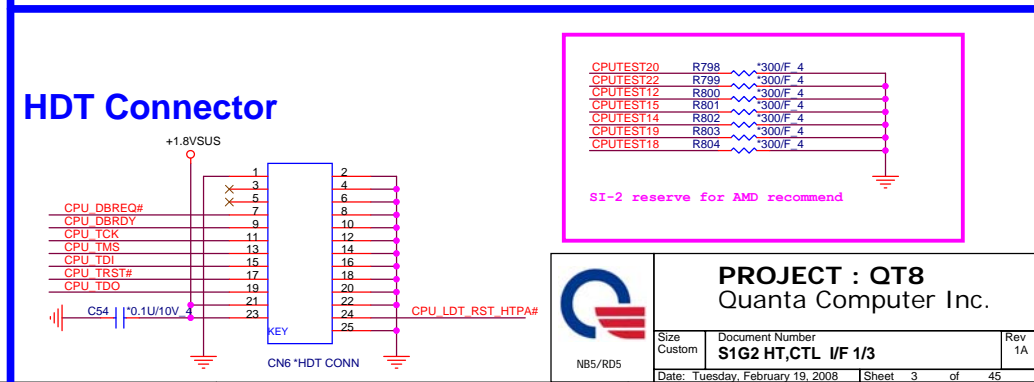
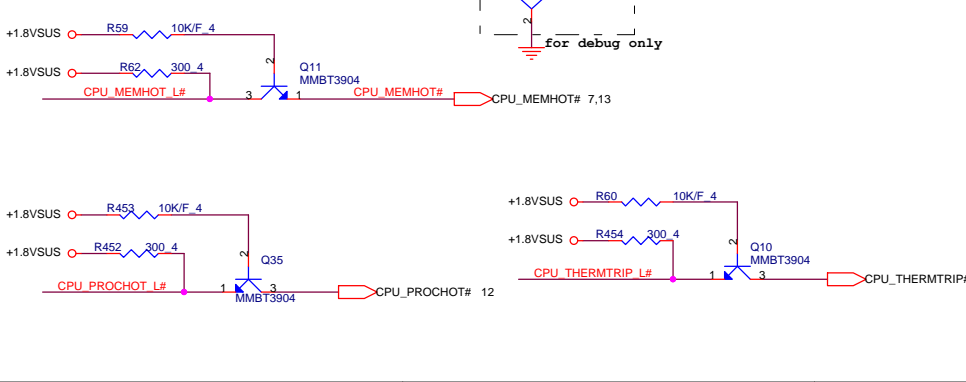
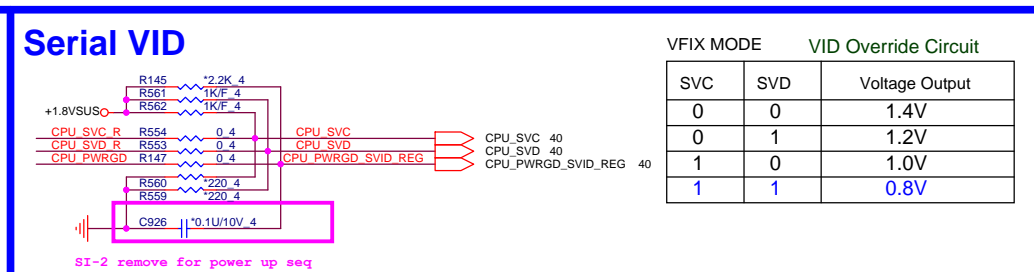
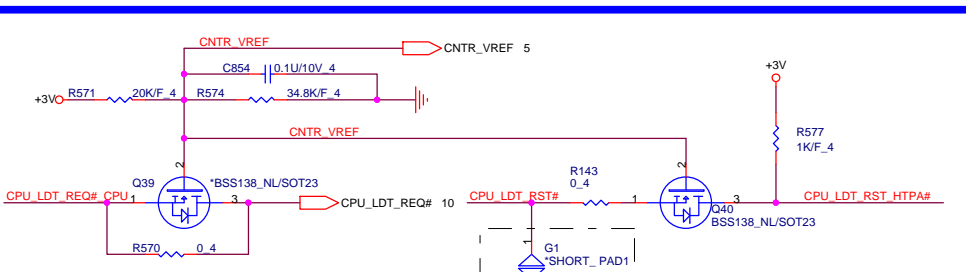
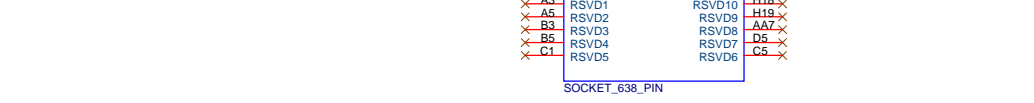


PROJECT : QT8
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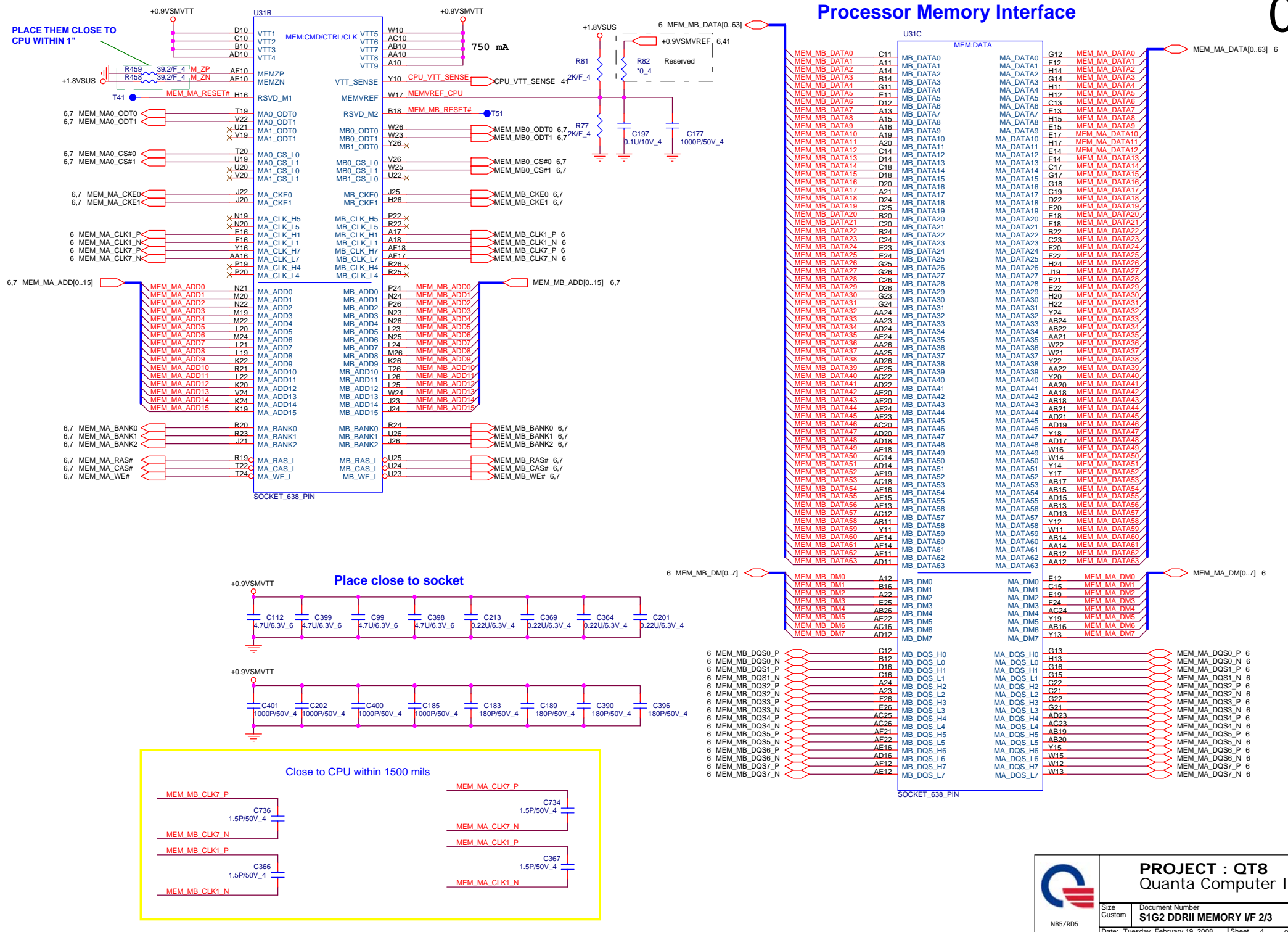


FOX PZ63826-284R-41F
 DG0*8000004 IC SOCKET SMD 638P S1 (P1.27,H3.2)
 MLX 47296-4131
 DG0*8000003 IC SOCKET SMD 638P S1 (P1.27,H3.2)
 TYC 4-1903401-2
 DG0*8000005 IC SOCKET SMD 638P S1 (P1.27,H3.2)

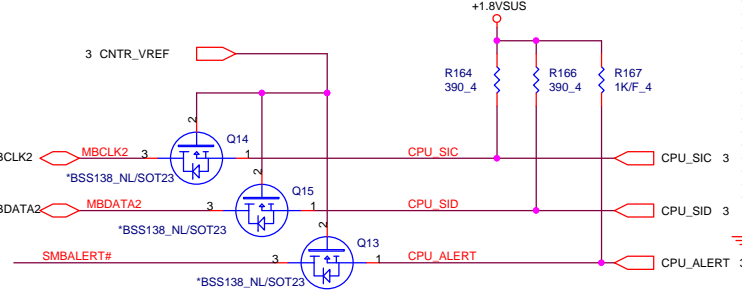
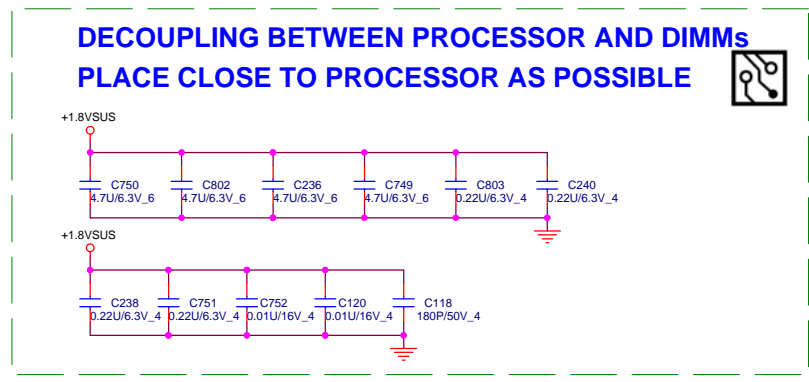
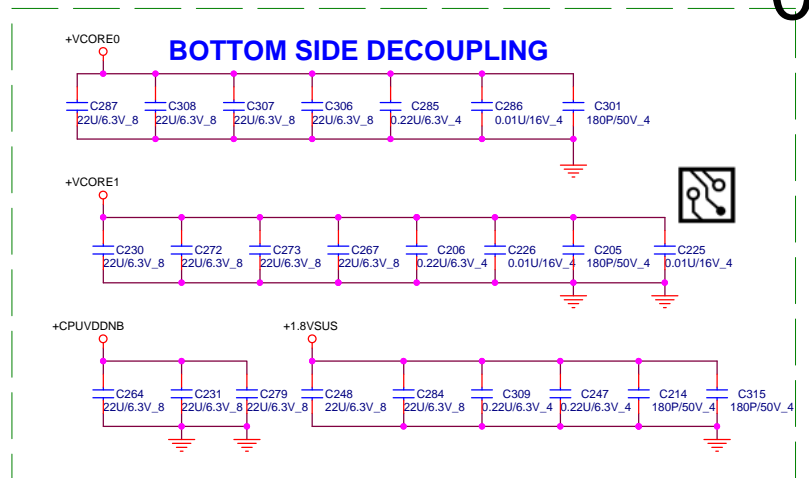
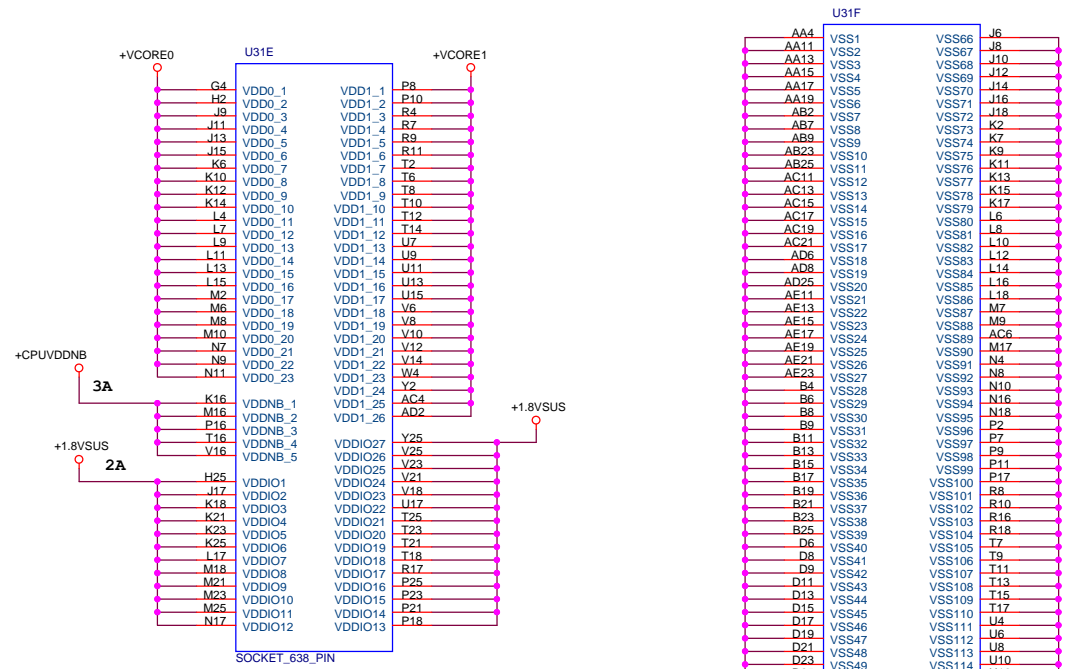
SOCKET_638_PIN



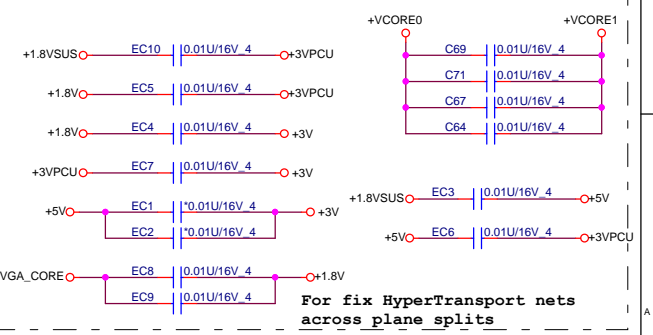
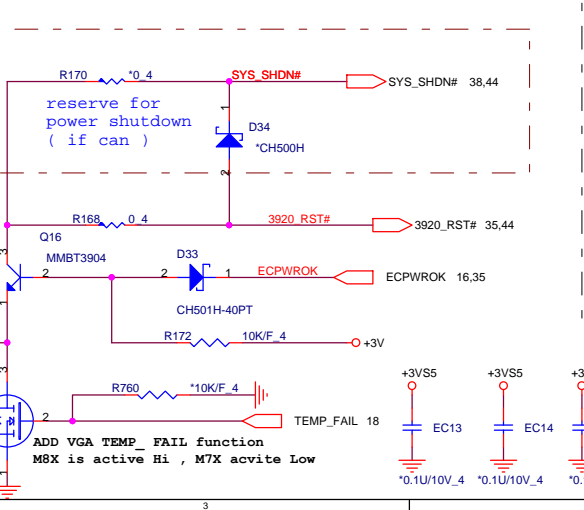
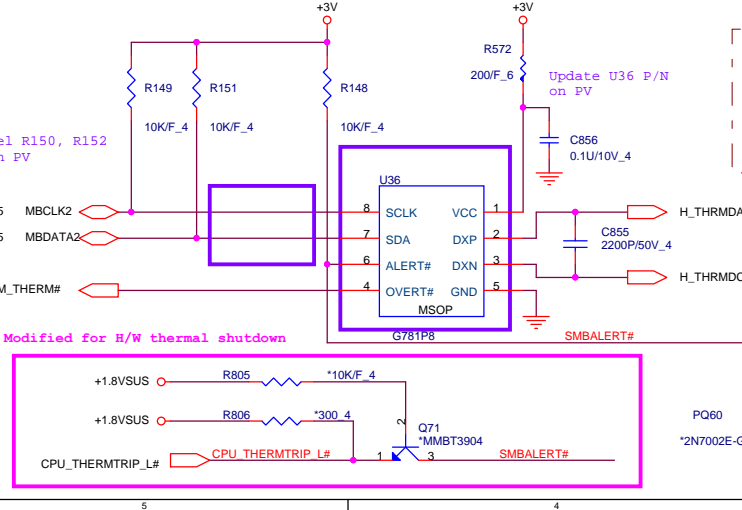
Processor Memory Interface



PROJECT : QT8
 Quanta Computer Inc.



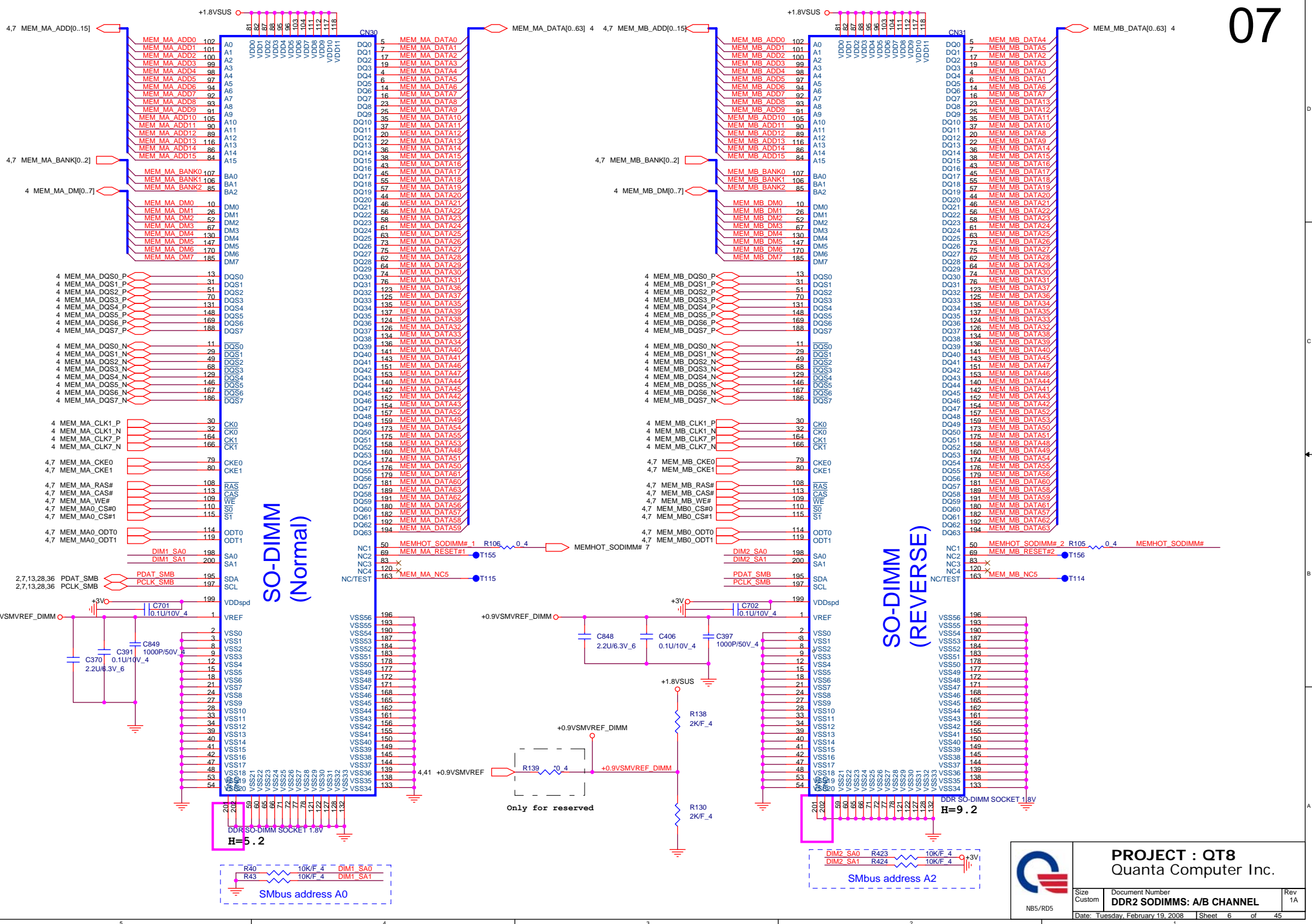
PROCESSOR POWER AND GROUND



PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number NB5/RD5
SIG2 PWR & GND 3/3 Rev 1A

Date: Tuesday, February 19, 2008 Sheet 5 of 45



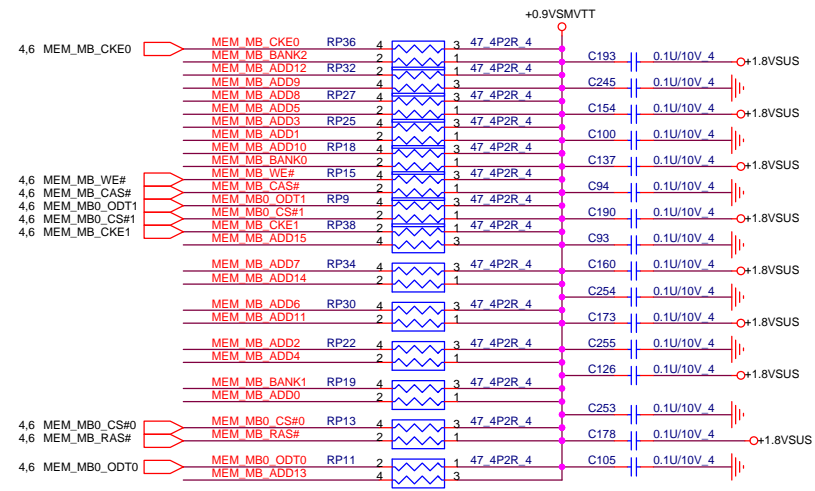
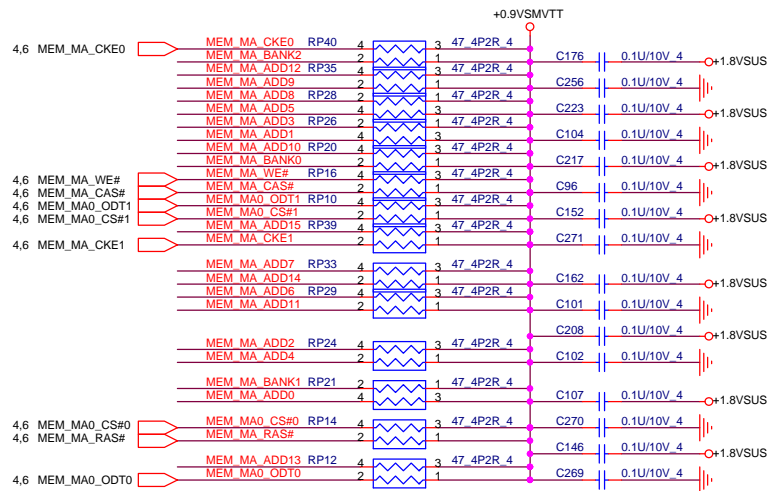
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number **DDR2 SODIMMS: A/B CHANNEL** Rev 1A
 Date: Tuesday, February 19, 2008 Sheet 6 of 45

NB5/RD5

4,6 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
 4,6 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

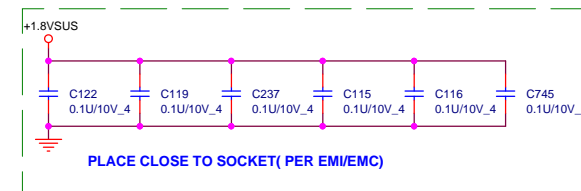
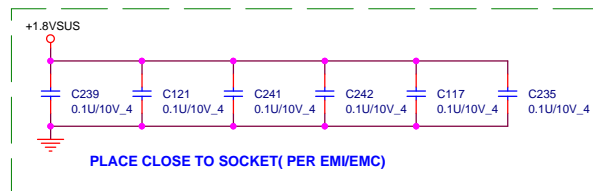
4,6 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
 4,6 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]



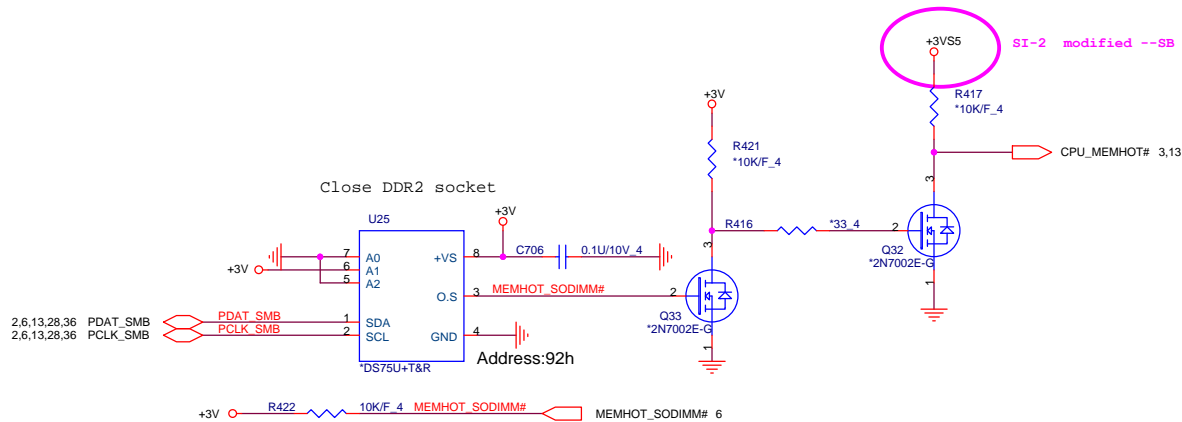
**PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH**



**PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH**



SI-2 modified --SB internal pull HI to 3vs5



	PROJECT : QT8	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
DDR2 SODIMMS TERMINATIONS		
Date: Tuesday, February 19, 2008	Sheet 7 of 45	

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	D24	HT_NB_CPU_CAD_H0	
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	D25	HT_NB_CPU_CAD_L0	
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	E24	HT_NB_CPU_CAD_H1	
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	E25	HT_NB_CPU_CAD_L1	
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	F24	HT_NB_CPU_CAD_H2	
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	F25	HT_NB_CPU_CAD_L2	
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	F23	HT_NB_CPU_CAD_H3	
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	F22	HT_NB_CPU_CAD_L3	
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	H23	HT_NB_CPU_CAD_H4	
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	H22	HT_NB_CPU_CAD_L4	
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	J25	HT_NB_CPU_CAD_H5	
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	J24	HT_NB_CPU_CAD_L5	
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	K25	HT_NB_CPU_CAD_H6	
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	K24	HT_NB_CPU_CAD_L6	
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	K23	HT_NB_CPU_CAD_H7	
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	K22	HT_NB_CPU_CAD_L7	
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	G21	HT_NB_CPU_CAD_H8	
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	G20	HT_NB_CPU_CAD_L8	
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	H21	HT_NB_CPU_CAD_H9	
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	H20	HT_NB_CPU_CAD_L9	
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	J20	HT_NB_CPU_CAD_H10	
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	J21	HT_NB_CPU_CAD_L10	
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	J18	HT_NB_CPU_CAD_H11	
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	K17	HT_NB_CPU_CAD_L11	
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	L19	HT_NB_CPU_CAD_H12	
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	J19	HT_NB_CPU_CAD_L12	
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	M19	HT_NB_CPU_CAD_H13	
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	L18	HT_NB_CPU_CAD_L13	
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	M21	HT_NB_CPU_CAD_H14	
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	P21	HT_NB_CPU_CAD_L14	
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	P18	HT_NB_CPU_CAD_H15	
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	M18	HT_NB_CPU_CAD_L15	
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	H24	HT_NB_CPU_CLK_H0	
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	H25	HT_NB_CPU_CLK_L0	
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	L21	HT_NB_CPU_CLK_H1	
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	L20	HT_NB_CPU_CLK_L1	
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	M24	HT_NB_CPU_CTL_H0	
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	M25	HT_NB_CPU_CTL_L0	
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	P19	HT_NB_CPU_CTL_H1	
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	P18	HT_NB_CPU_CTL_L1	

SI-2 modified
-- follow AMD
check list to
change part
number 300 ohm
to 301 ohm

SI-2 modified
-- follow AMD
check list to
change part
number 300 ohm
to 301 ohm

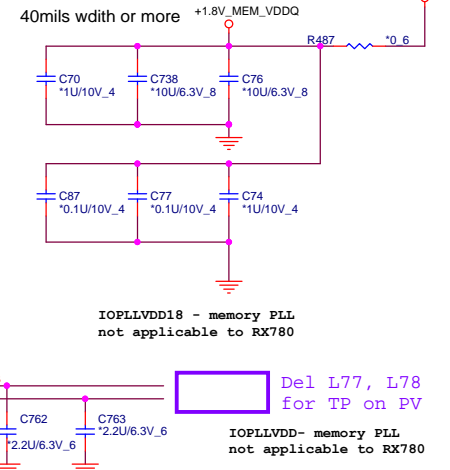
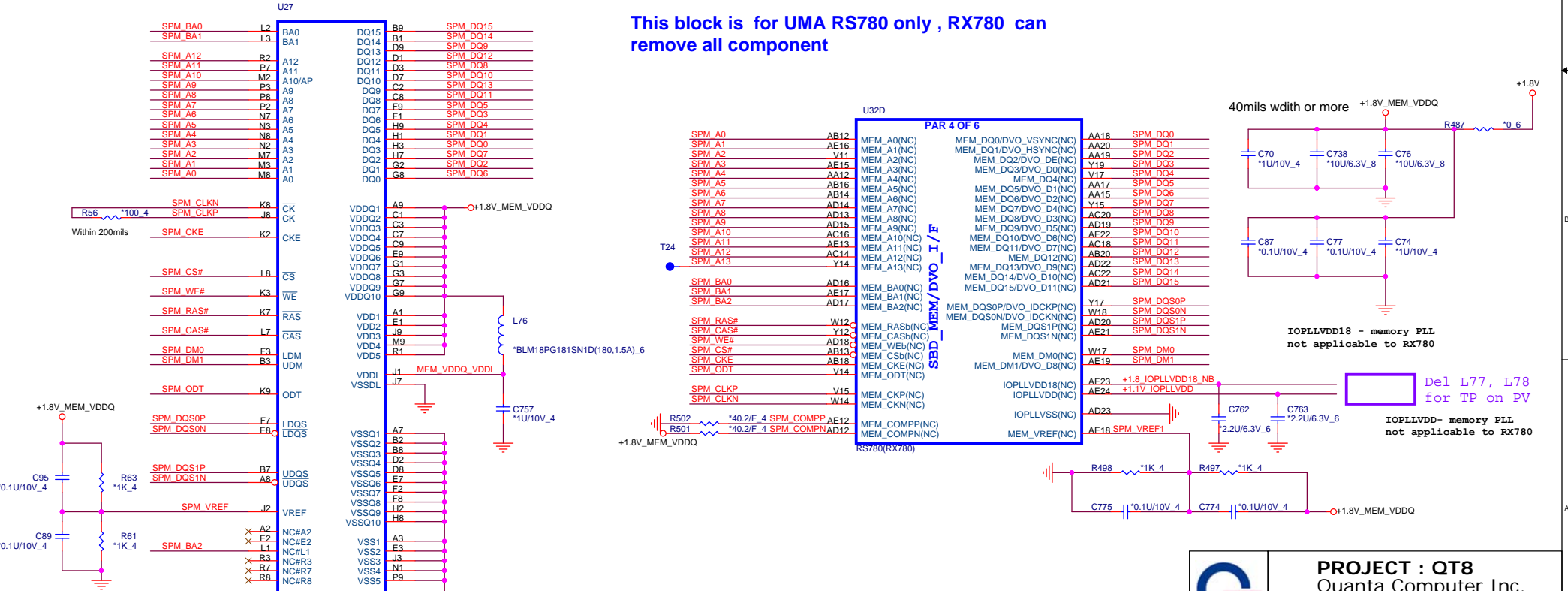


signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

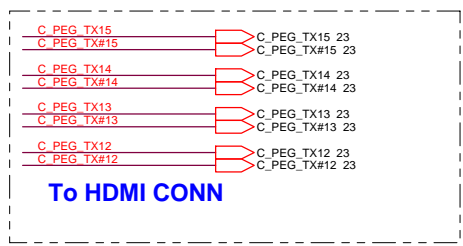
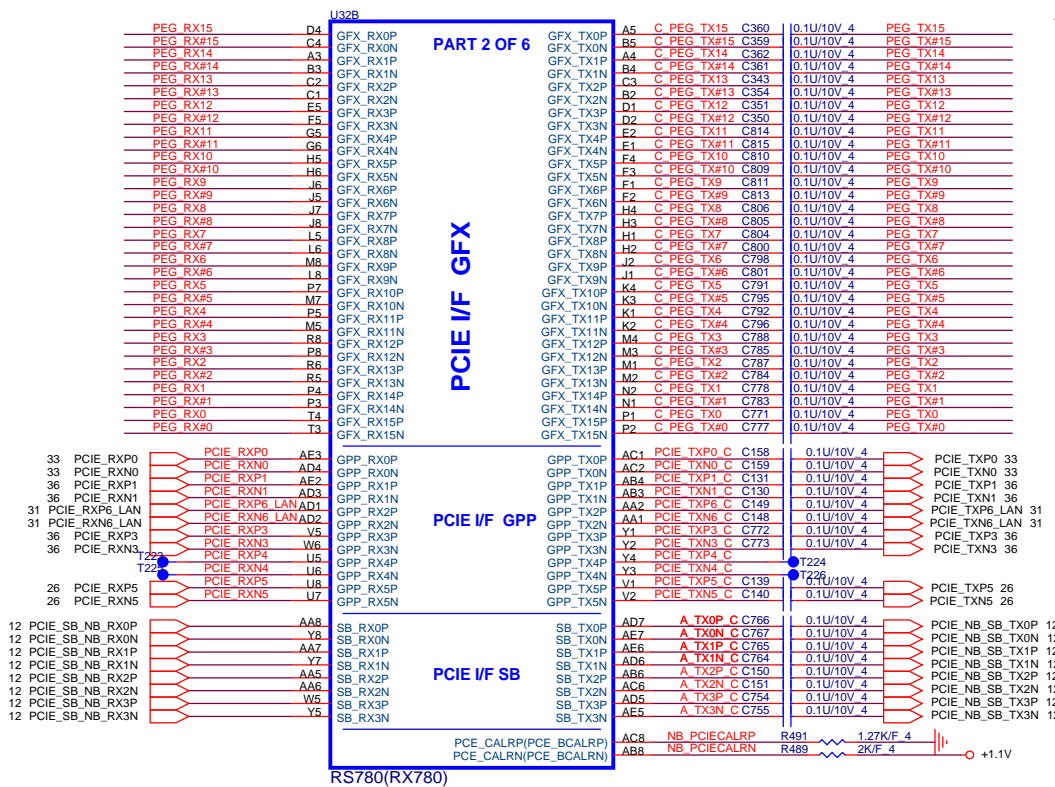
RES CHIP 1.21K 1/16W +-1% (0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1% (0402)
P/N : CS13012FB14

This block is for UMA RS780 only , RX780 can
remove all component



PROJECT : QT8
Quanta Computer Inc.



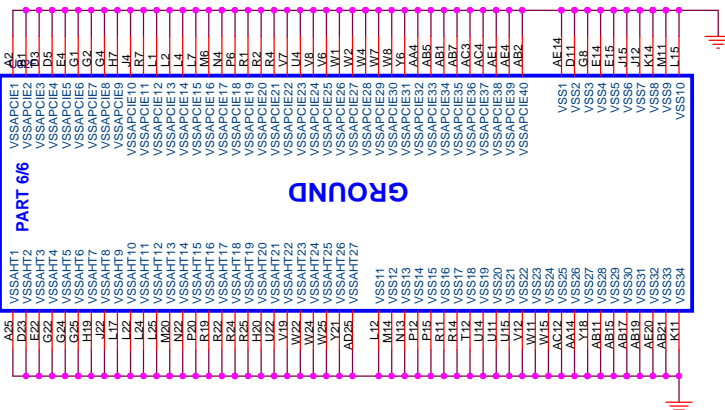
- TO EPRESS CARD**
- TO WLAN**
- TO PCIE-LAN**
- TO TV TUNNER**
- TO PCIE CARD READER**

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

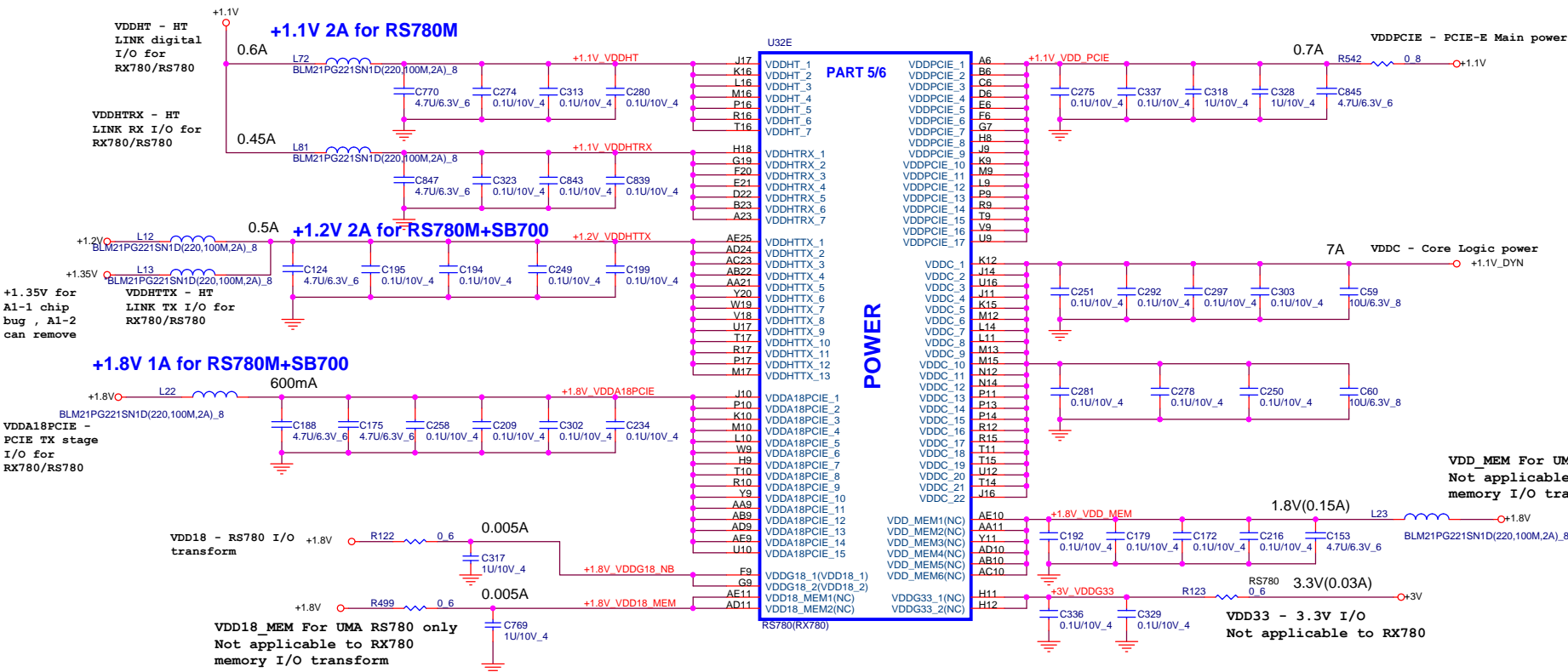
RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC

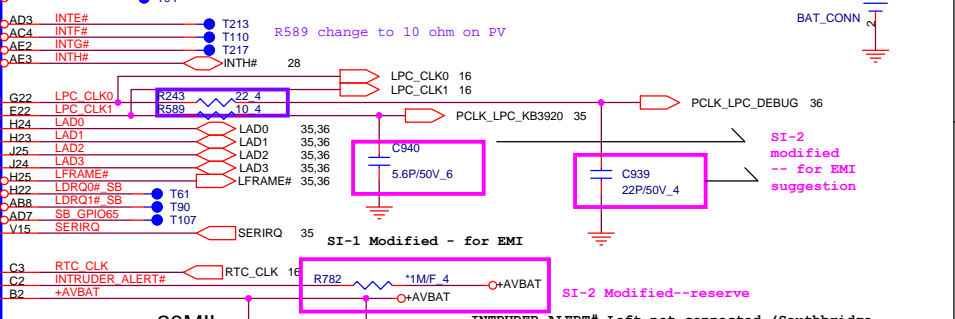
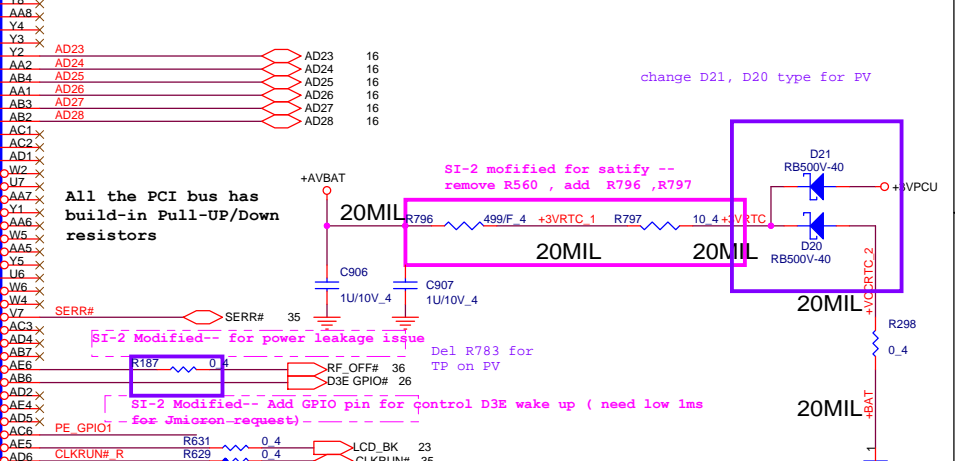
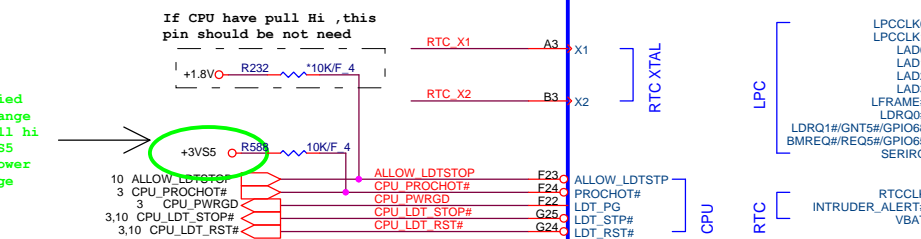
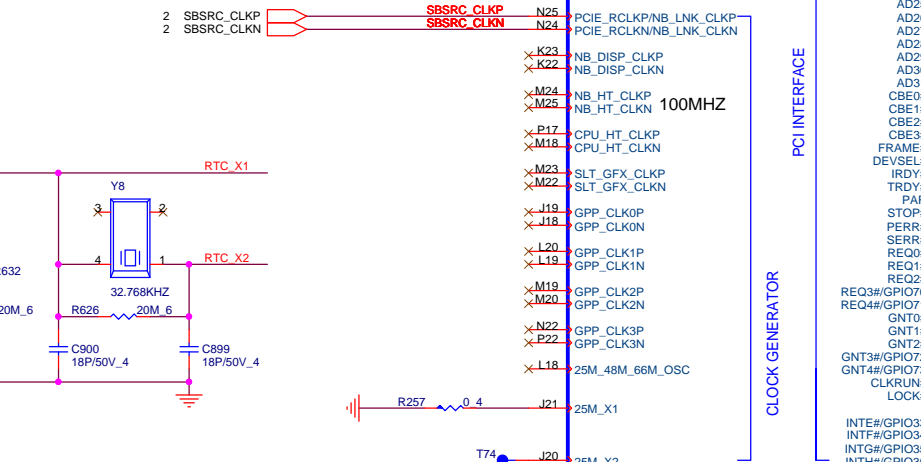
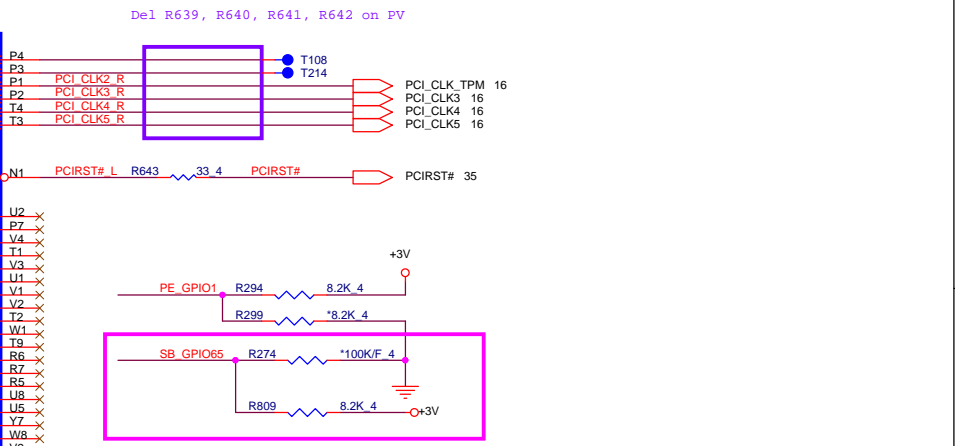
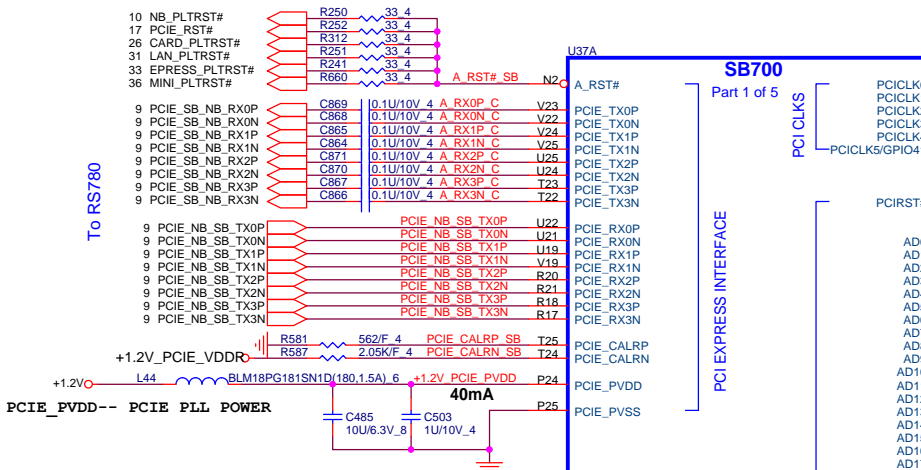


PROJECT : QT8
Quantas Computer Inc.

Size Custom	Document Number RS740/RS780-POWER5/5	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 11 of 45		

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780



PV-1 Modified -- change to pull hi to 3VS5 for power leakage issue

If CPU have pull Hi ,this pin should be not need

All the PCI bus has build-in Pull-up/Down resistors

SI-2 Modified-- for power leakage issue

SI-2 Modified-- Add GPIO pin for control D3E wake up (need low lms for Jmicron-request)

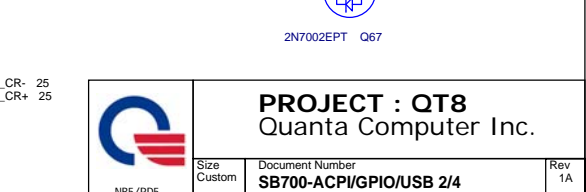
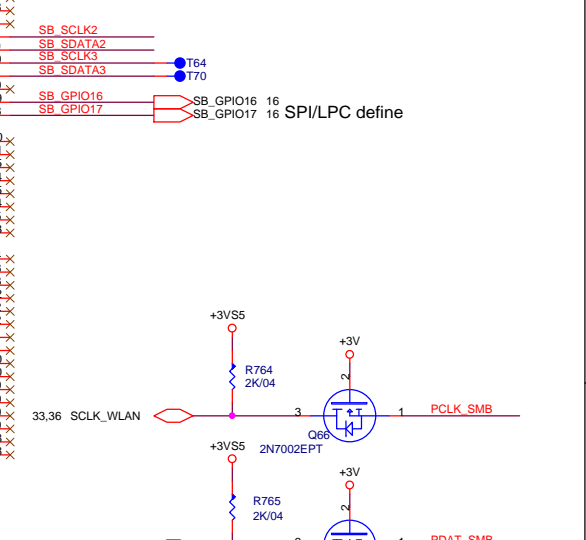
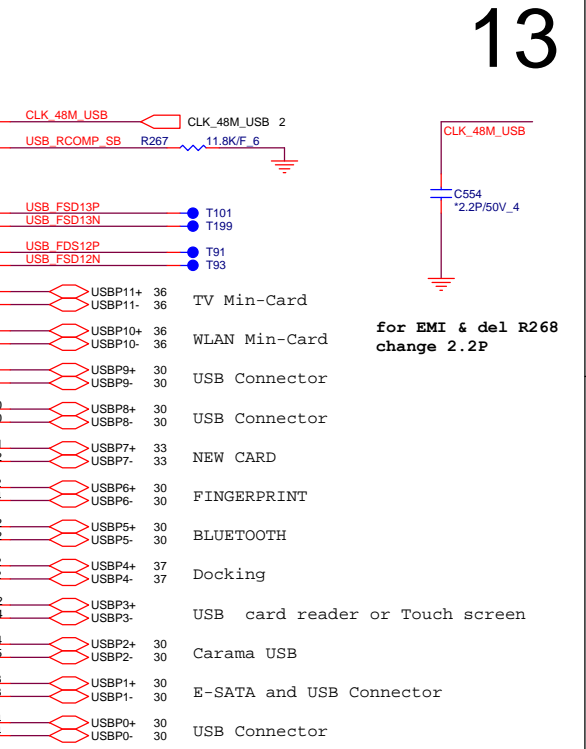
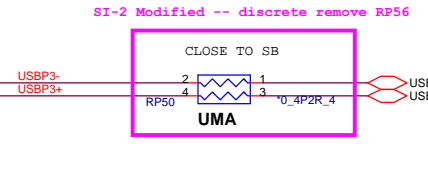
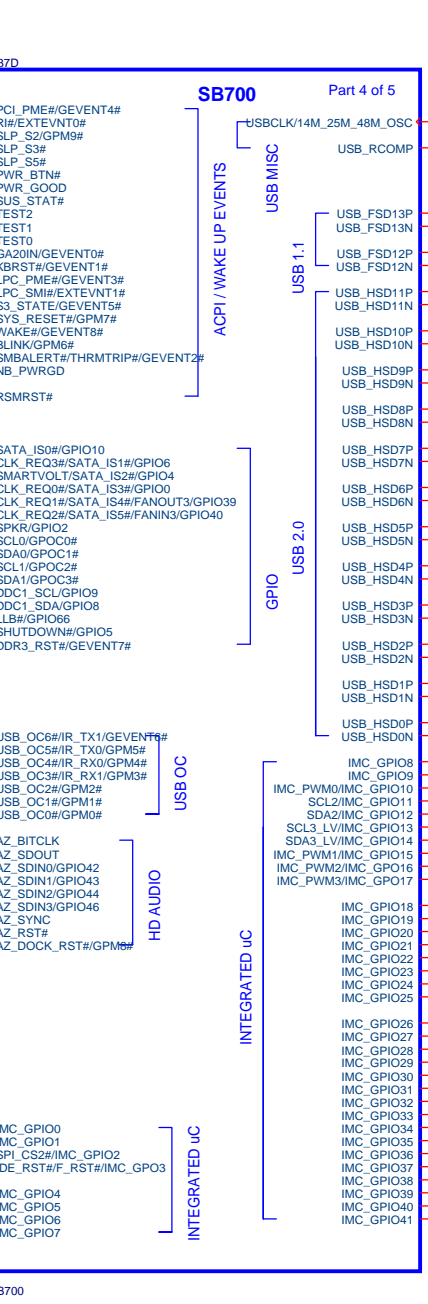
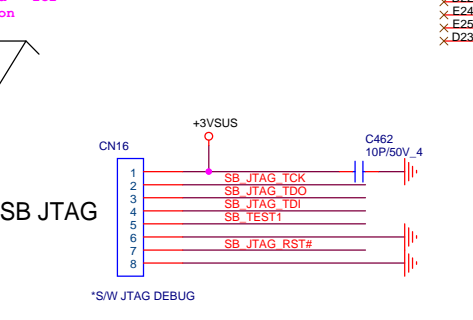
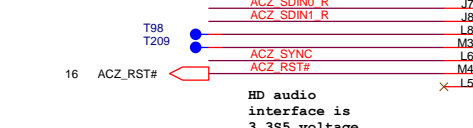
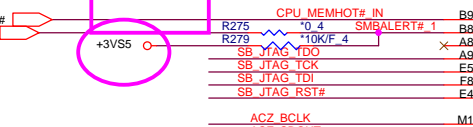
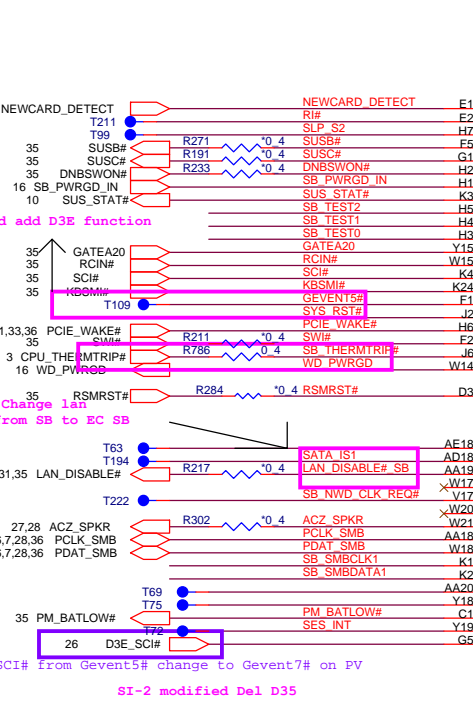
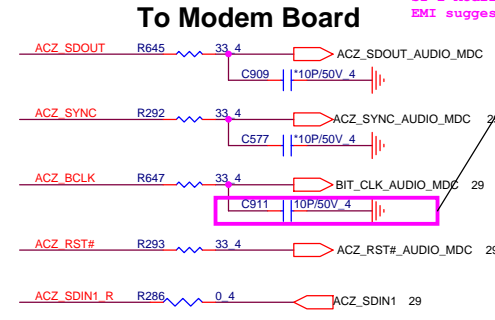
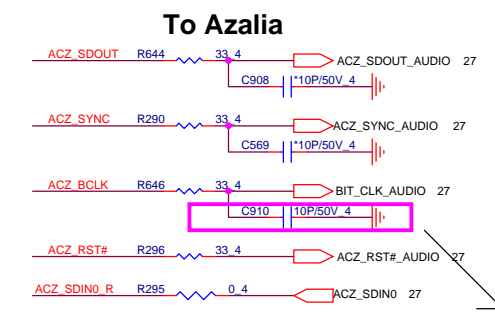
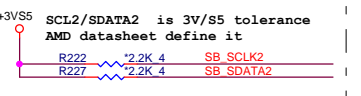
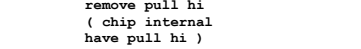
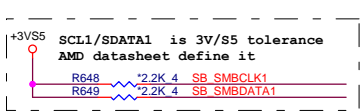
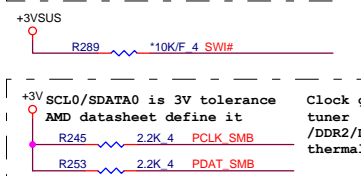
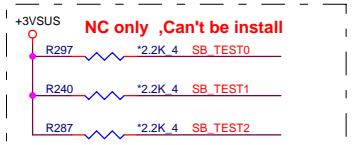
SI-1 Modified - for EMI

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number SB700-PCIE/PCU/CPU/LPC 1/4	Rev 1A
Date: Tuesday, February 19, 2008		Sheet 12 of 45



for EMI & del R268 change 2.2P

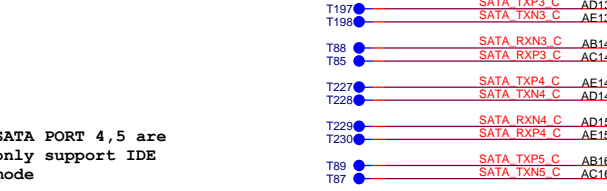
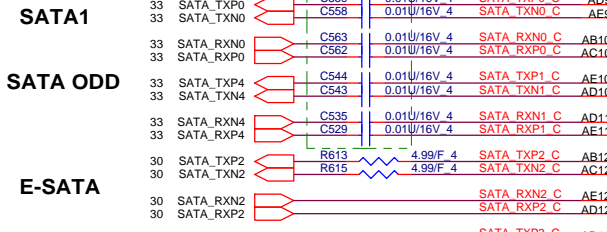
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number **SB700-ACPI/GPIO/USB 2/4** Rev 1A

Date: Tuesday, February 19, 2008 Sheet 13 of 45

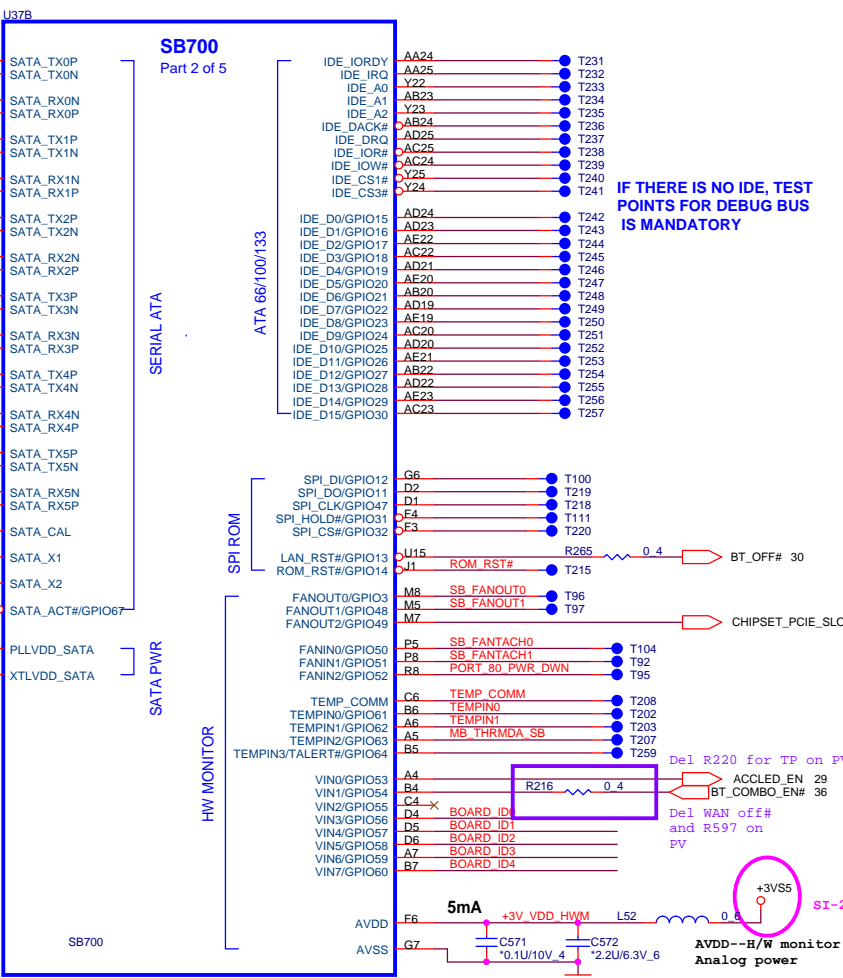
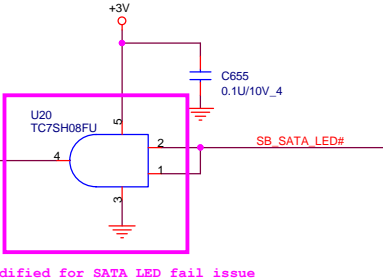
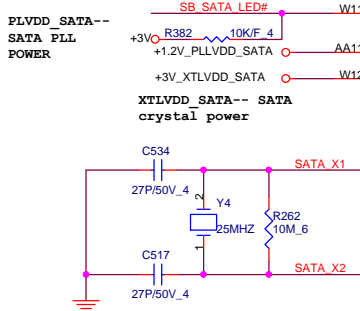
SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB600



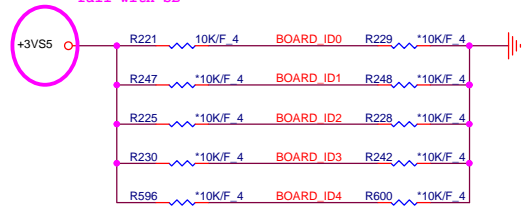
SATA PORT 4,5 are
only support IDE
mode

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

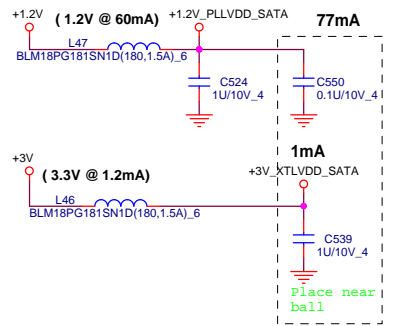


IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SI-2 modified -- SB
internal pull Hi to 3V5S
, modified to same power
rail with SB



SI-2 modified -- for fix +3V power leakage in S5 mode



ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	

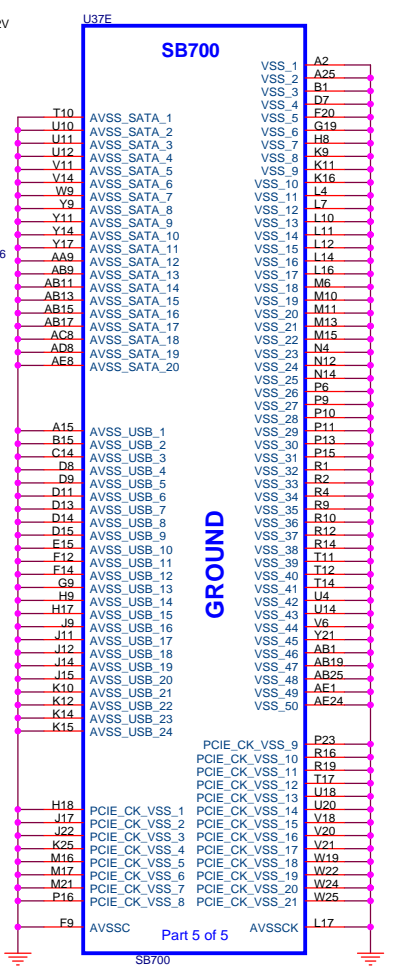
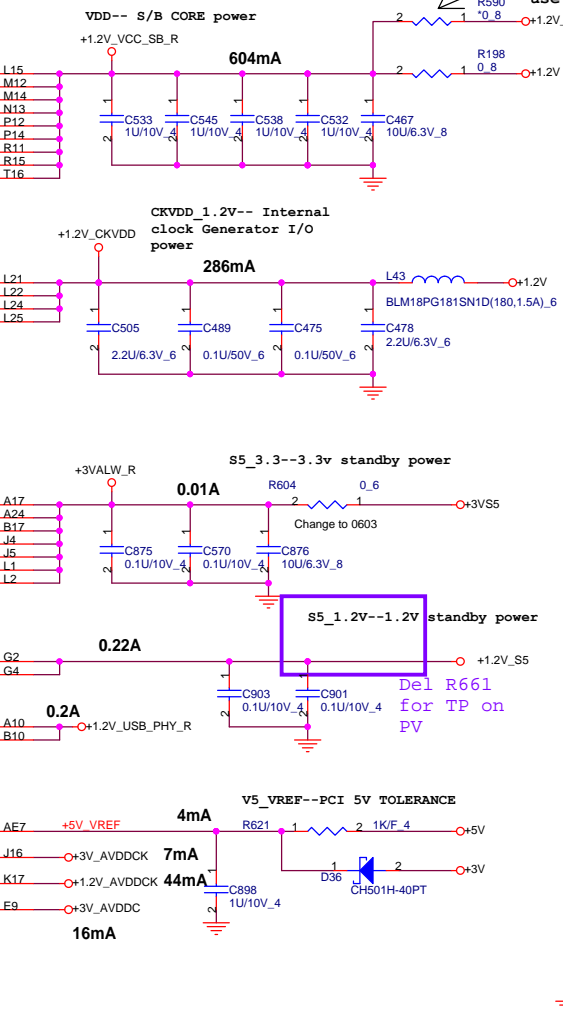
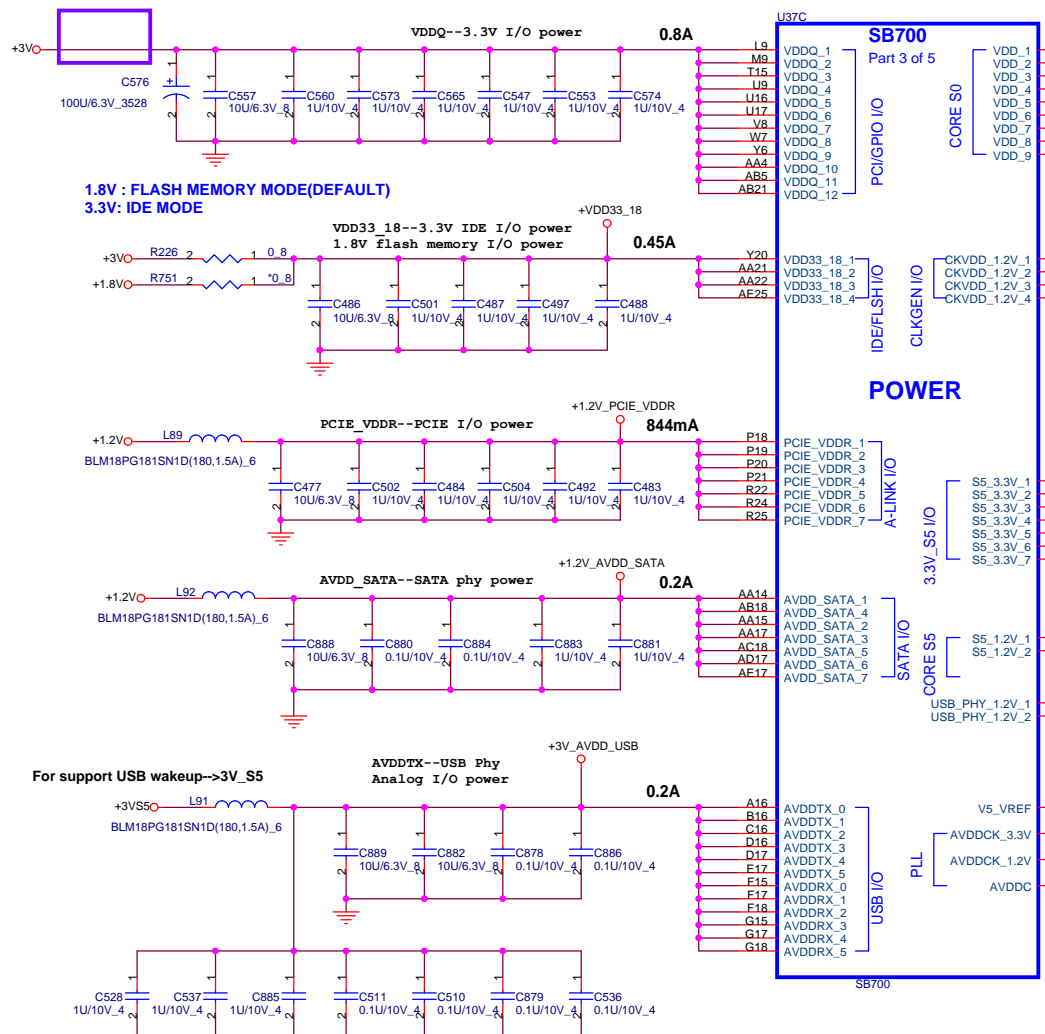


PROJECT : QT8
Quanta Computer Inc.

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

Del R285 for TP on PV



POWER

GROUND



PROJECT : QT8
Quantia Computer Inc.

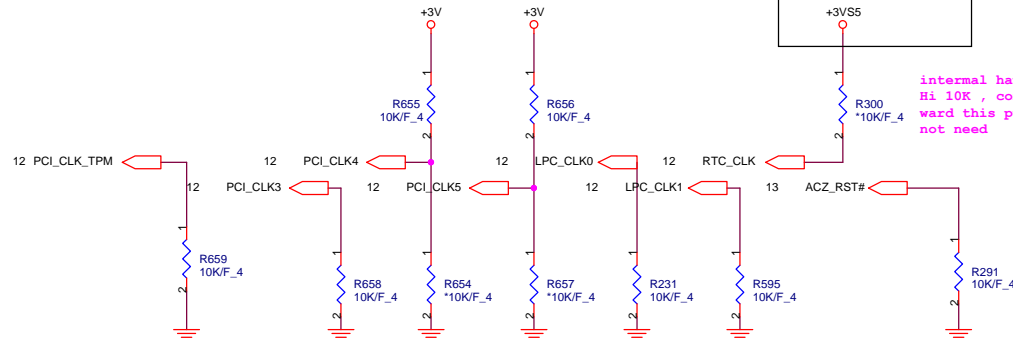
Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 15 of 45		



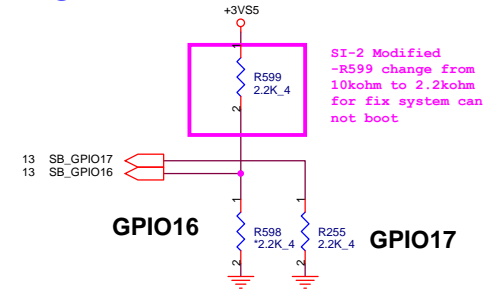
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



internal have pull Hi 10K , confirm AMD ward this pull Hi not need



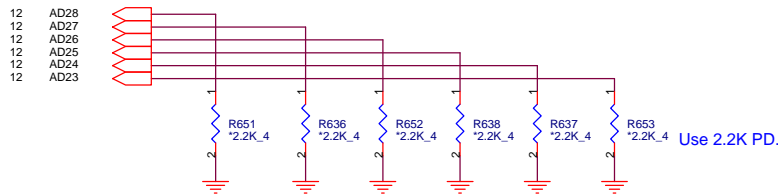
SI-2 Modified -R599 change from 10kohm to 2.2kohm for fix system can not boot

	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

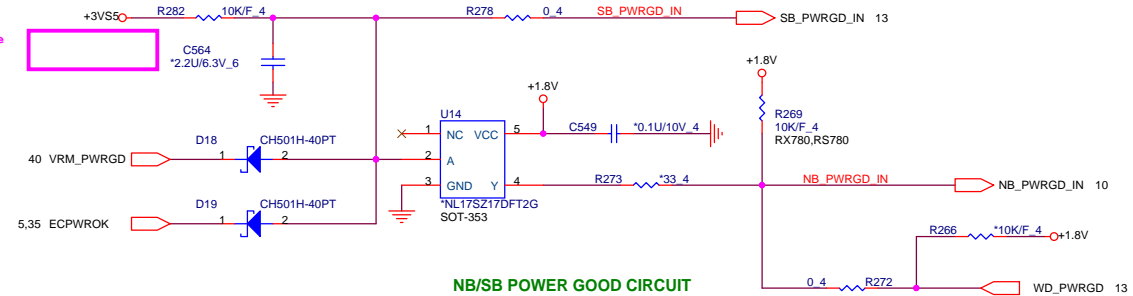


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN: RS780/RX780 = 1.8V; RS740 = 3.3V Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove +3V pull Hi resistor .



NB/SB POWER GOOD CIRCUIT

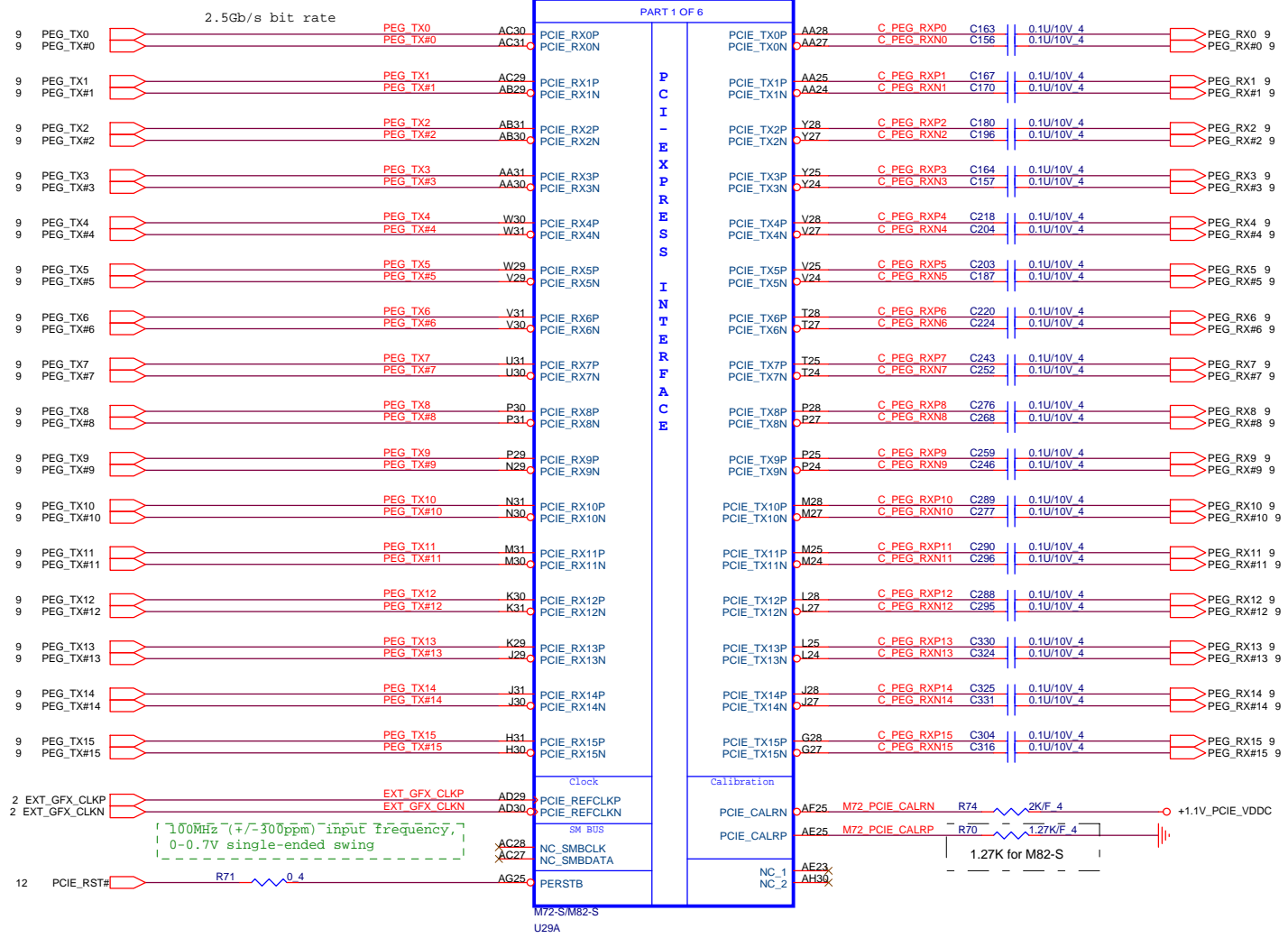
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



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Quanta Computer Inc.

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IC CTRL (632P) 216-0707001-00 (BGA)
VGA P/N : AJ070700T00

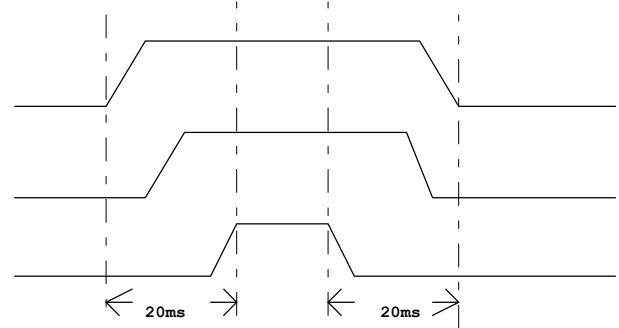


POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_COREB=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S

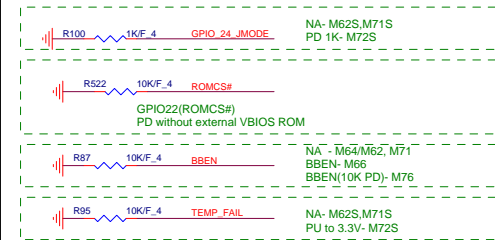
VGA Core BPP
VGA Core VDDC

+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1

3.3V_Delay VDDR3



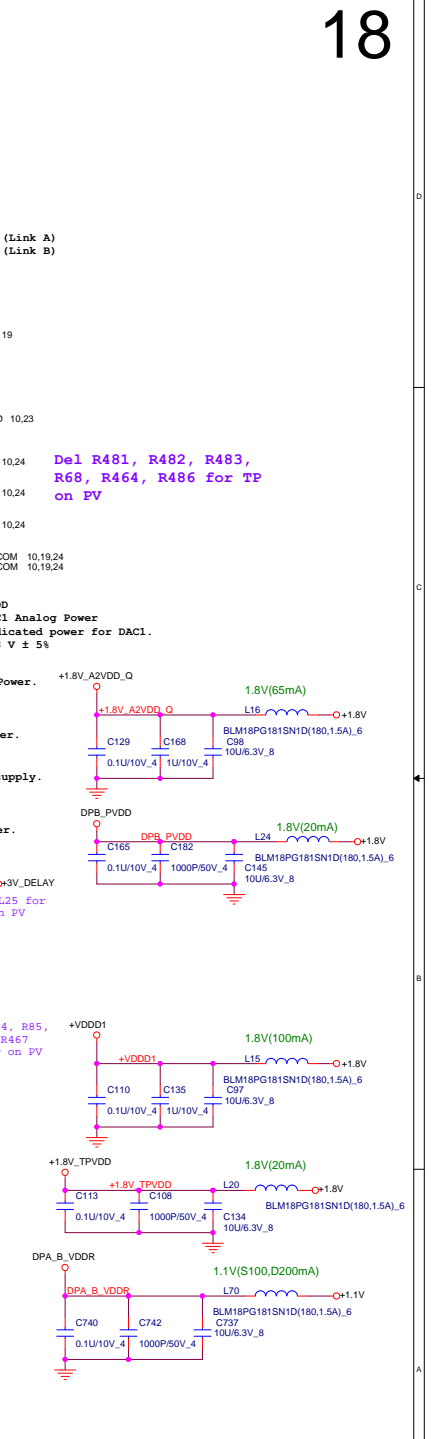
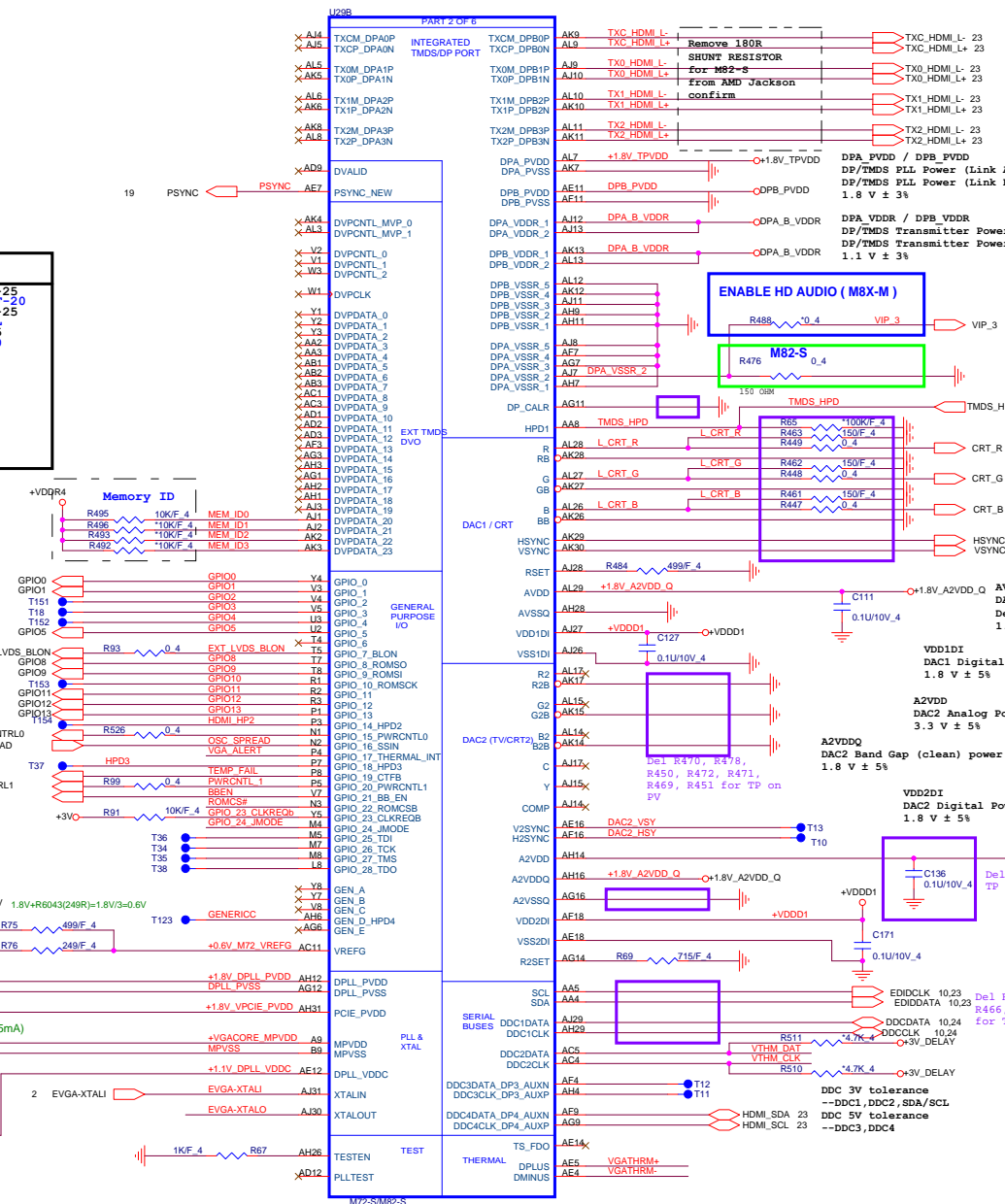
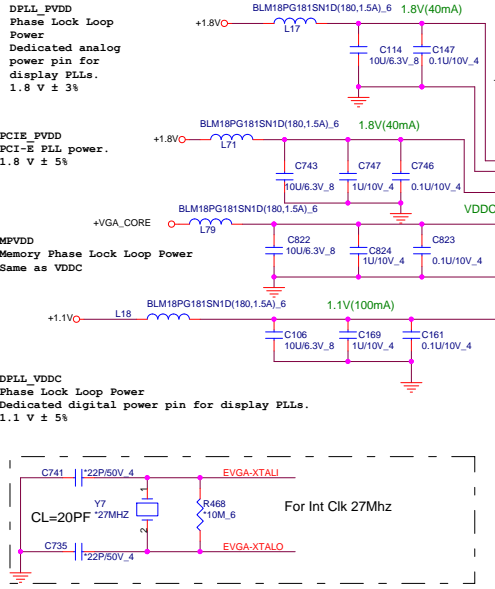
PROJECT : QT8
Quanta Computer Inc.

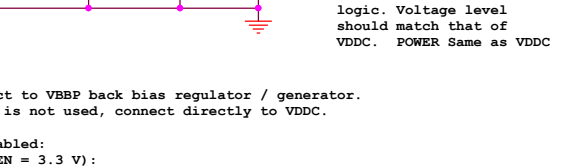
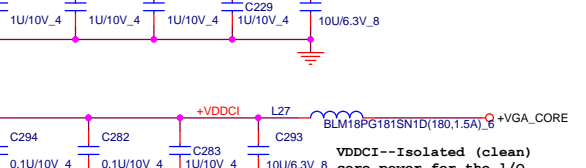
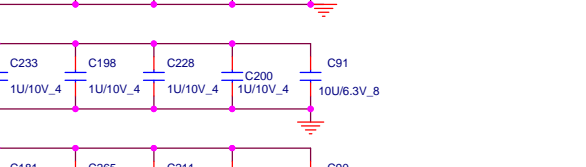
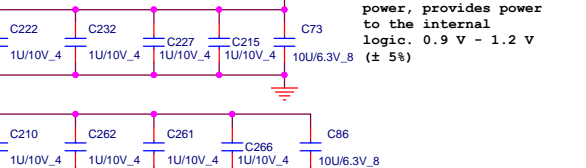
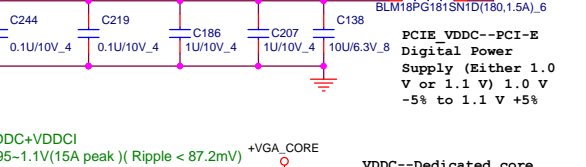
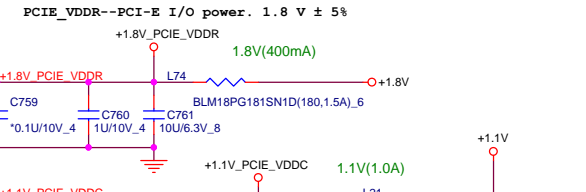
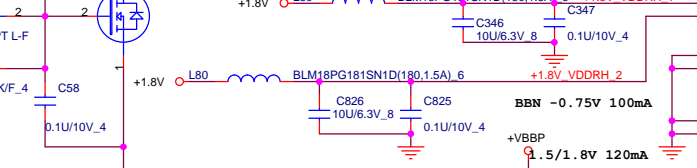
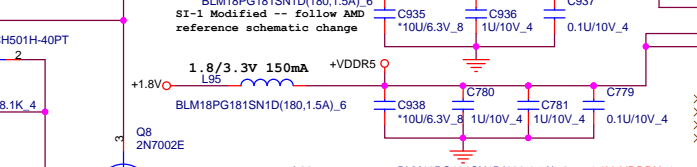
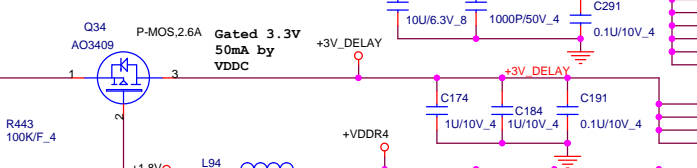
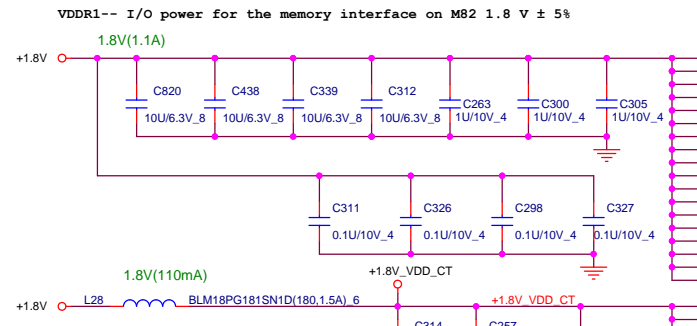
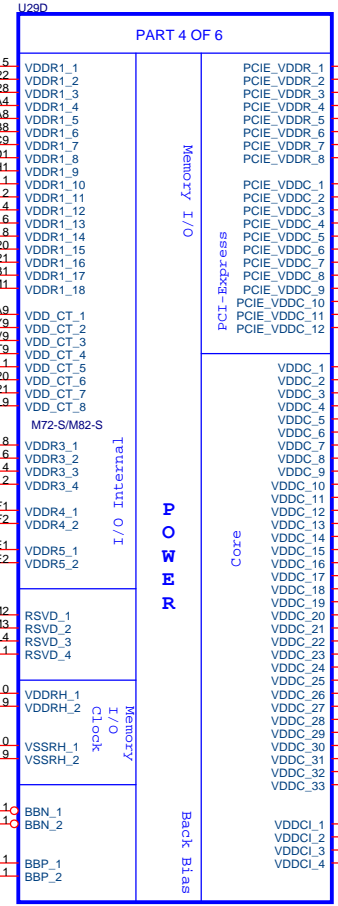


MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161B2F-25
0010	Hynix	16*16	HY5PS56162IAAF-25
0011	Hynix	32*16-500MHZ	HY5PS162IAAF-25
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-RC20
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V





BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.

Back Bias Enabled:
(GPIO_21_BB_EN = 3.3 V):
1.5 V or 1.8 V

Back Bias Disabled:
(GPIO_21_BB_EN = 0 V):
VDDC

VDD CT -- Level translation between core and I/O, excluding memory receivers. 1.8 V ± 5%

VDD R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

VDD R4 -- Power for DVPDATA [23:12] - external TMS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

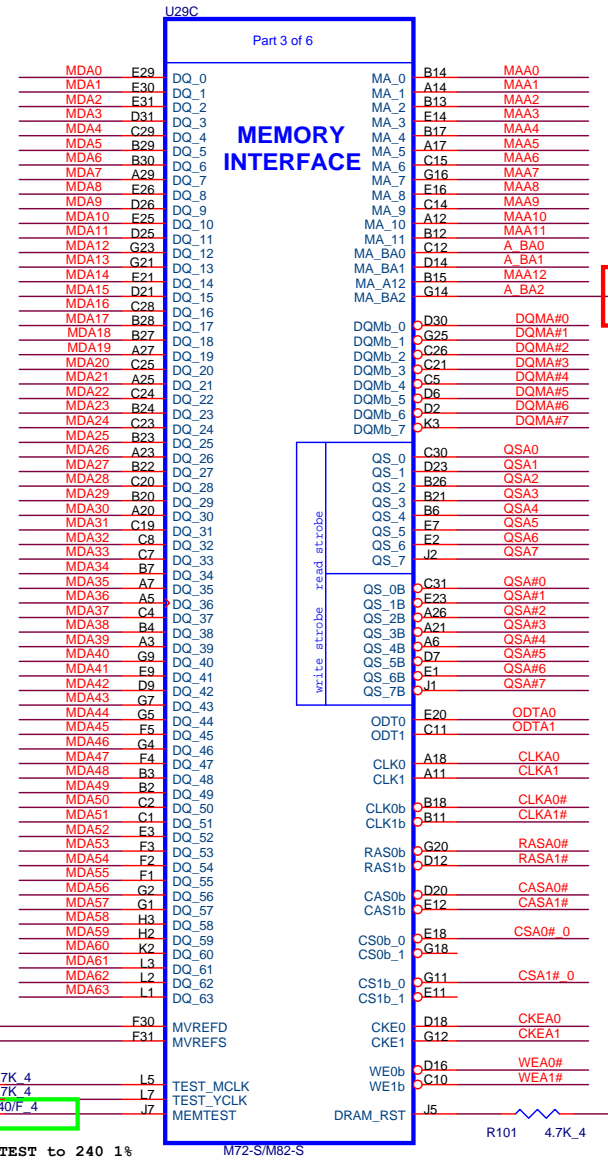
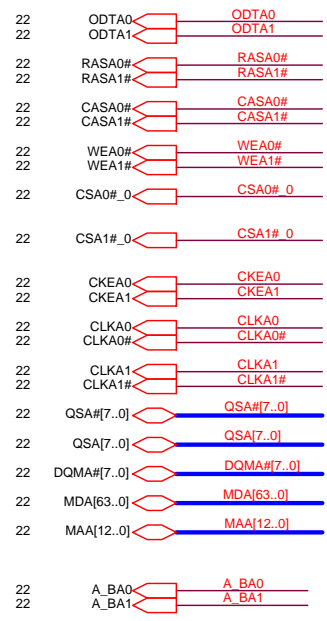
VDD R5 -- Power for DVP control pins (DVPCTRL [0-2] and DVPCLK) and DVPDATA [11:0] - external TMS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDDRH 1 & VDDRH 2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.



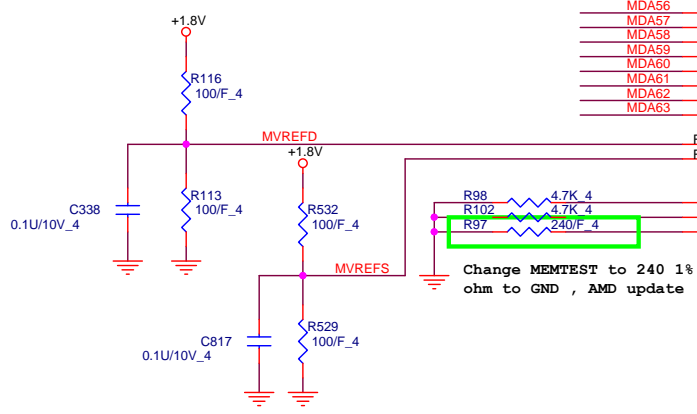
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number M7X/M8X_Power_and_NC	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 20 of 45	



A_BA2 22

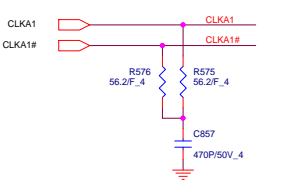
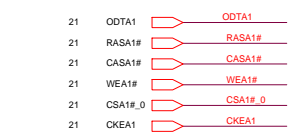
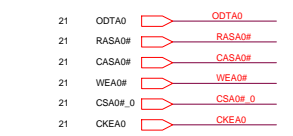
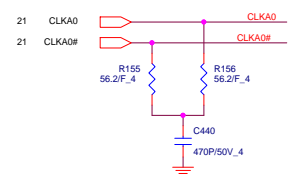
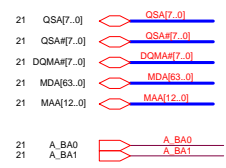
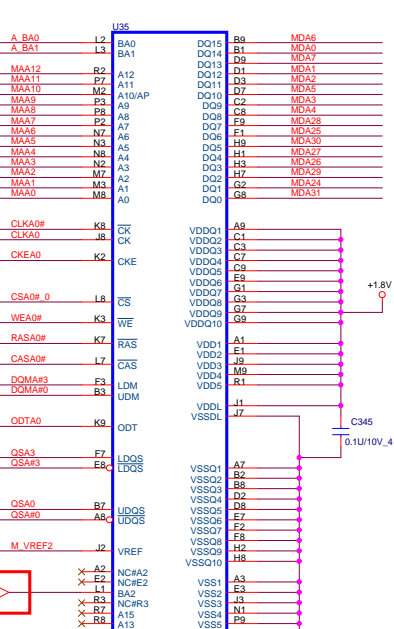
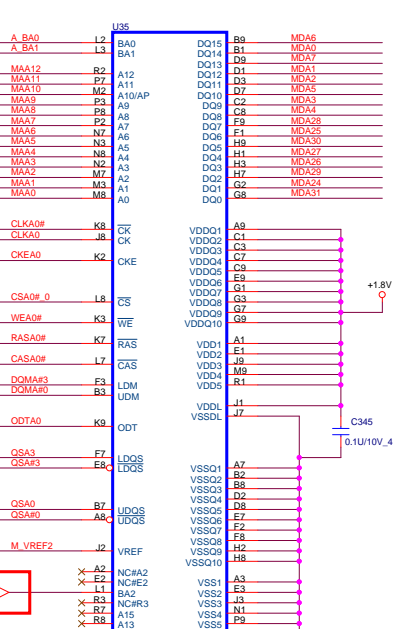
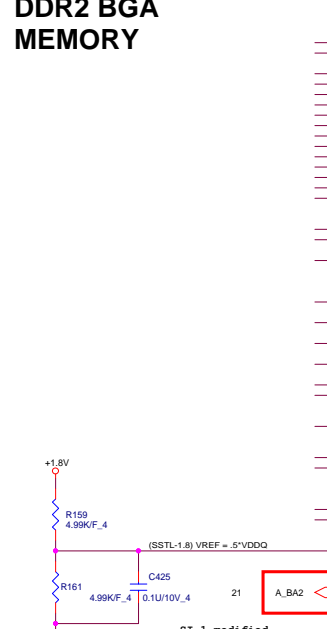
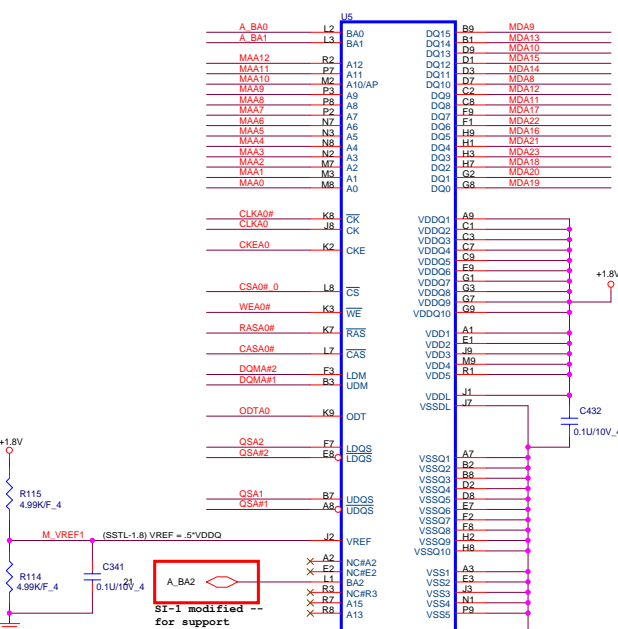
SI-1 modified --
for support
1Gbit VRAM (64M
x 16)



PROJECT : QT8
Quanta Computer Inc.

Size B	Document Number M7X/M8X/MEM_Interface	Rev 1A
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DDR2 BGA MEMORY



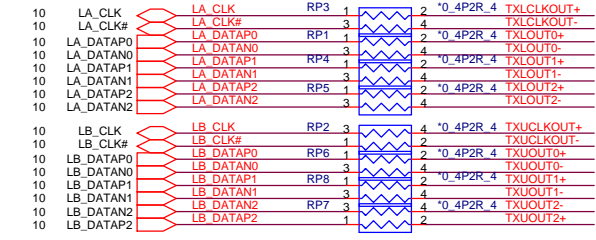
DDR2 BGA MEMORY

PROJECT : QT8
 Quanta Computer Inc.

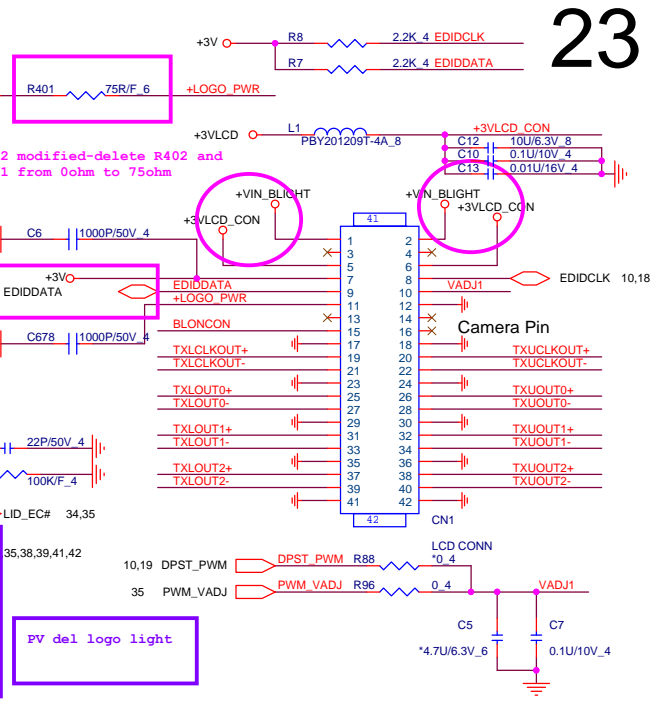
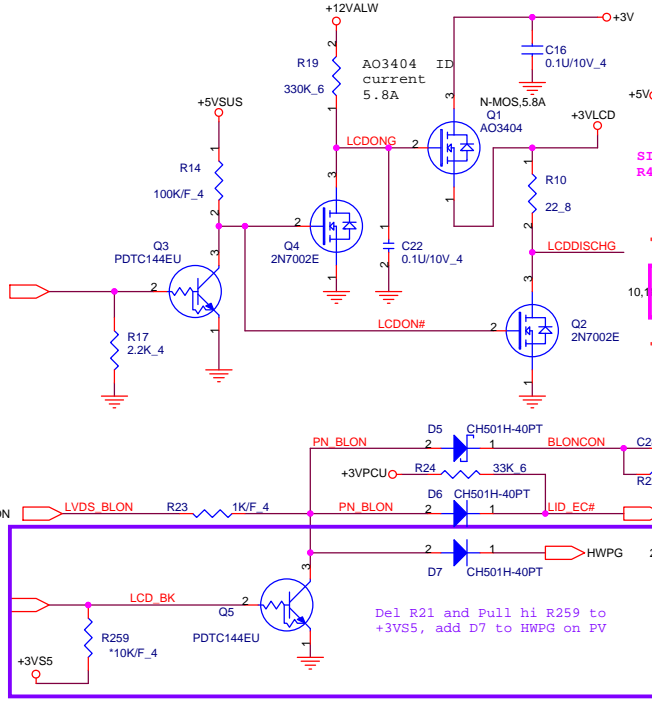
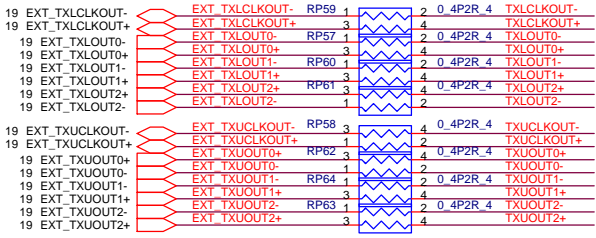
Size C Document Number **M7X/M8X/VRAM_A0,A1** Rev 1A
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

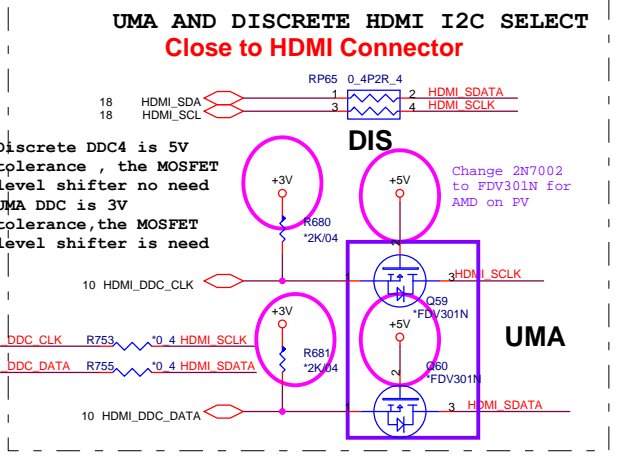
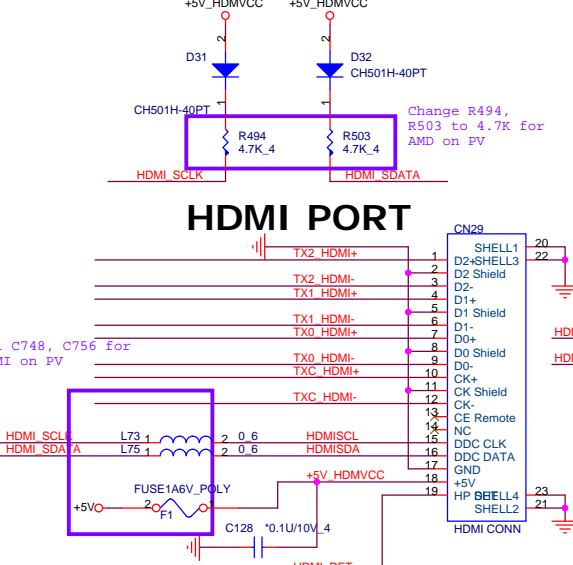
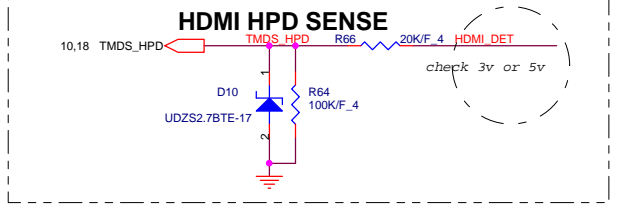
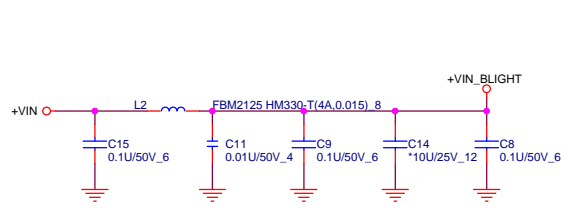
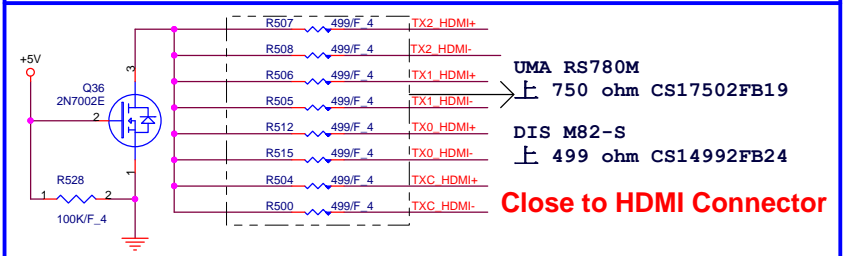
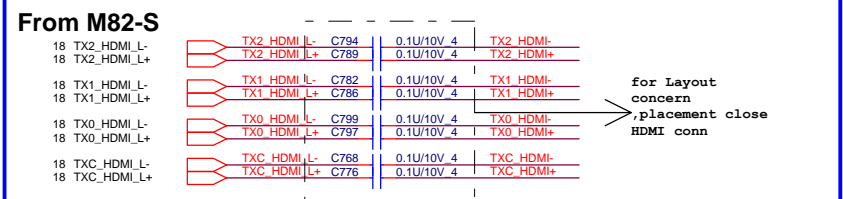
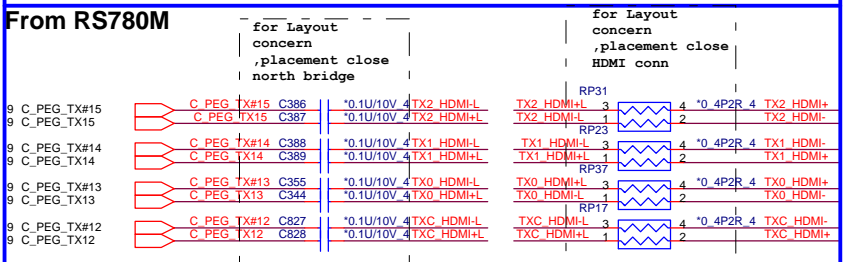
OPTION SIGNAL FROM NB to LVDS for UMA

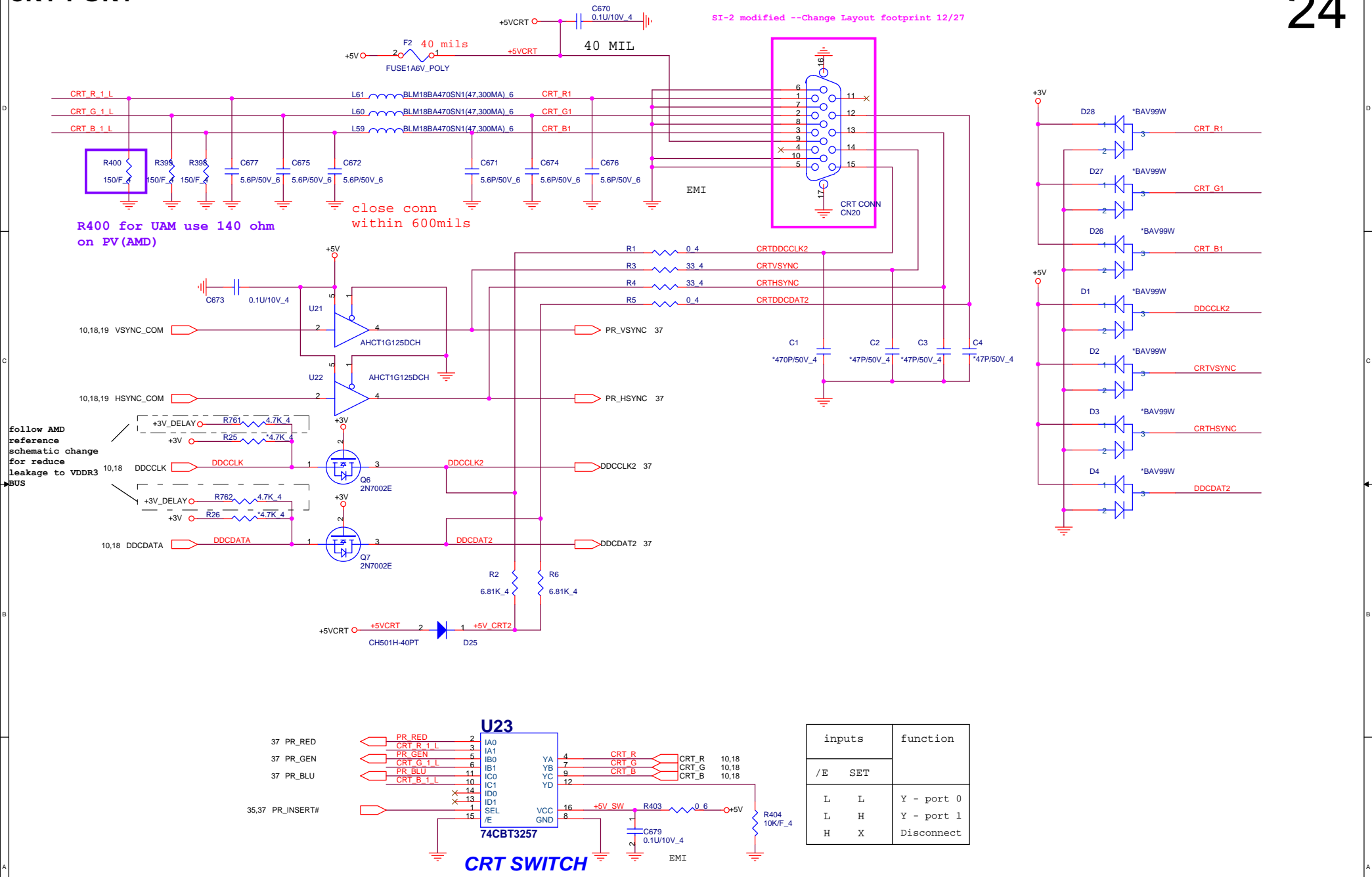


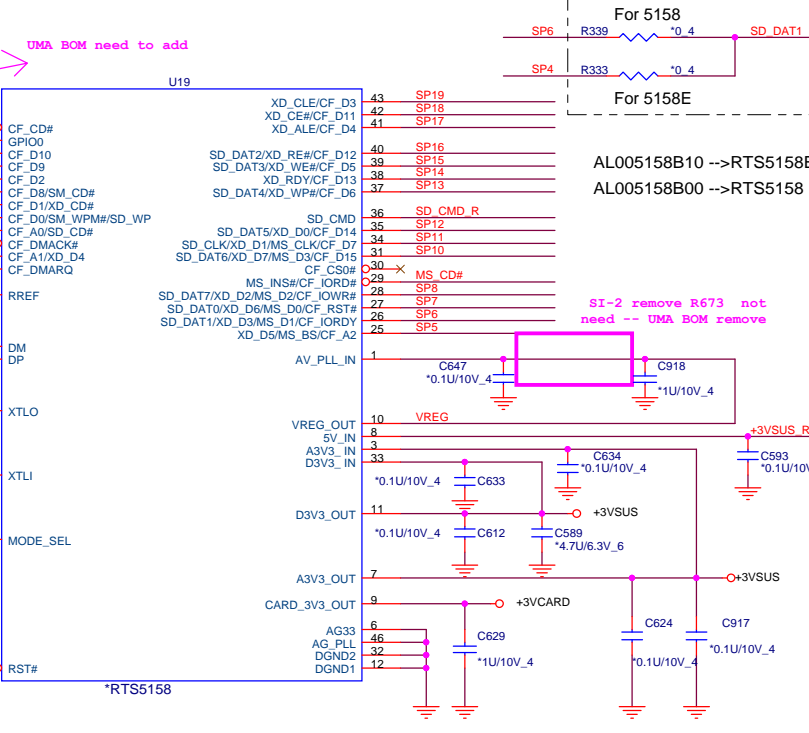
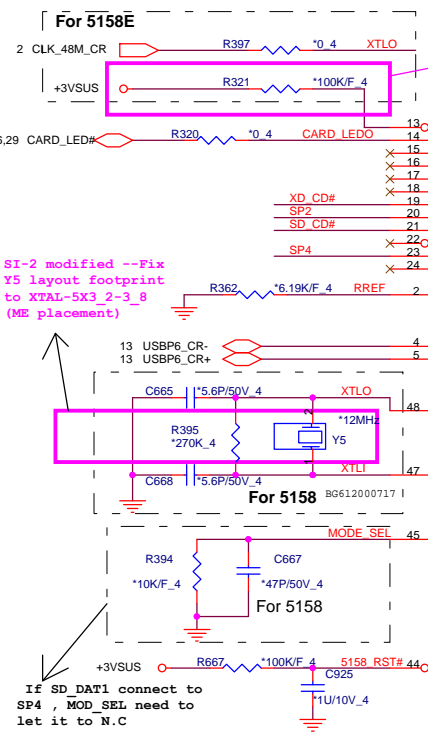
OPTION SIGNAL FROM M8X to LVDS for discrete



UMA/DISCRETE select for HDMI

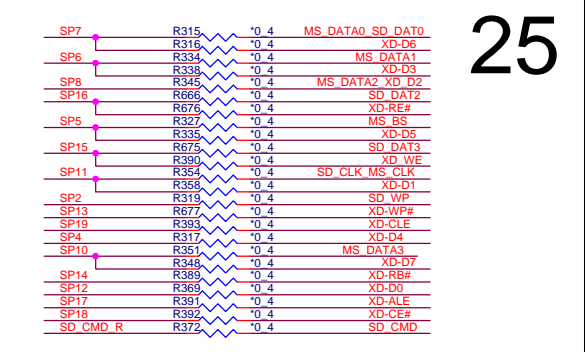






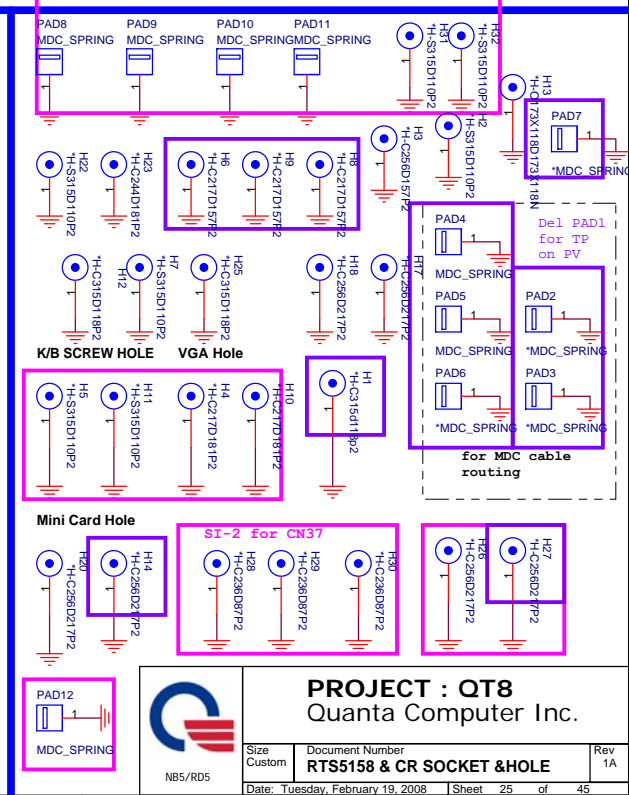
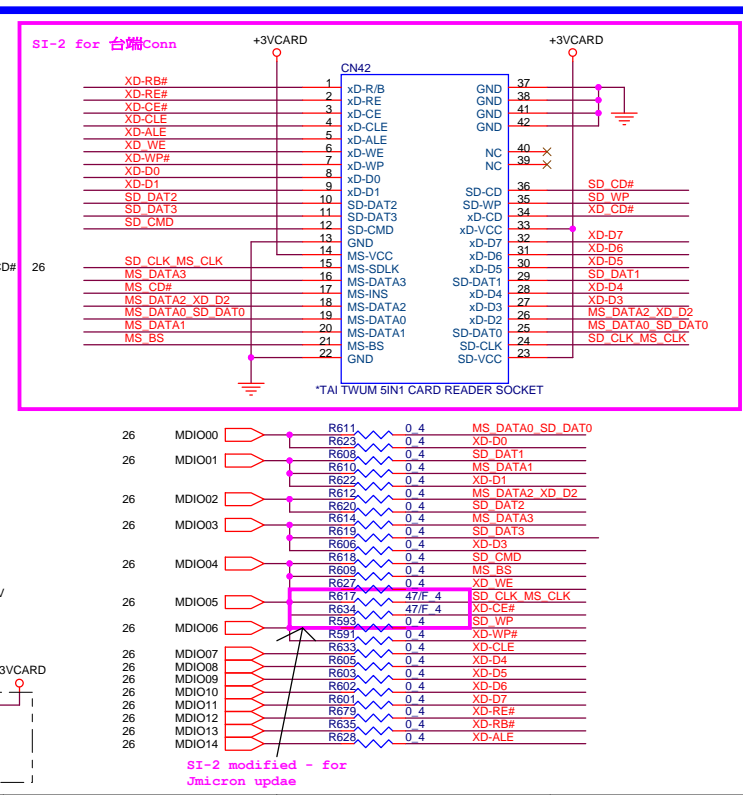
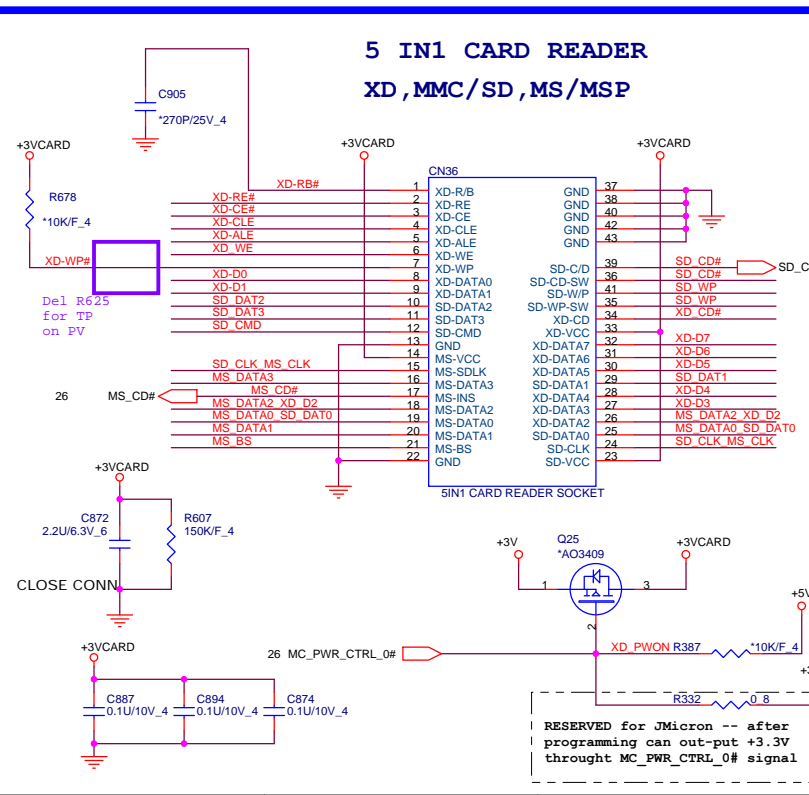
Note:

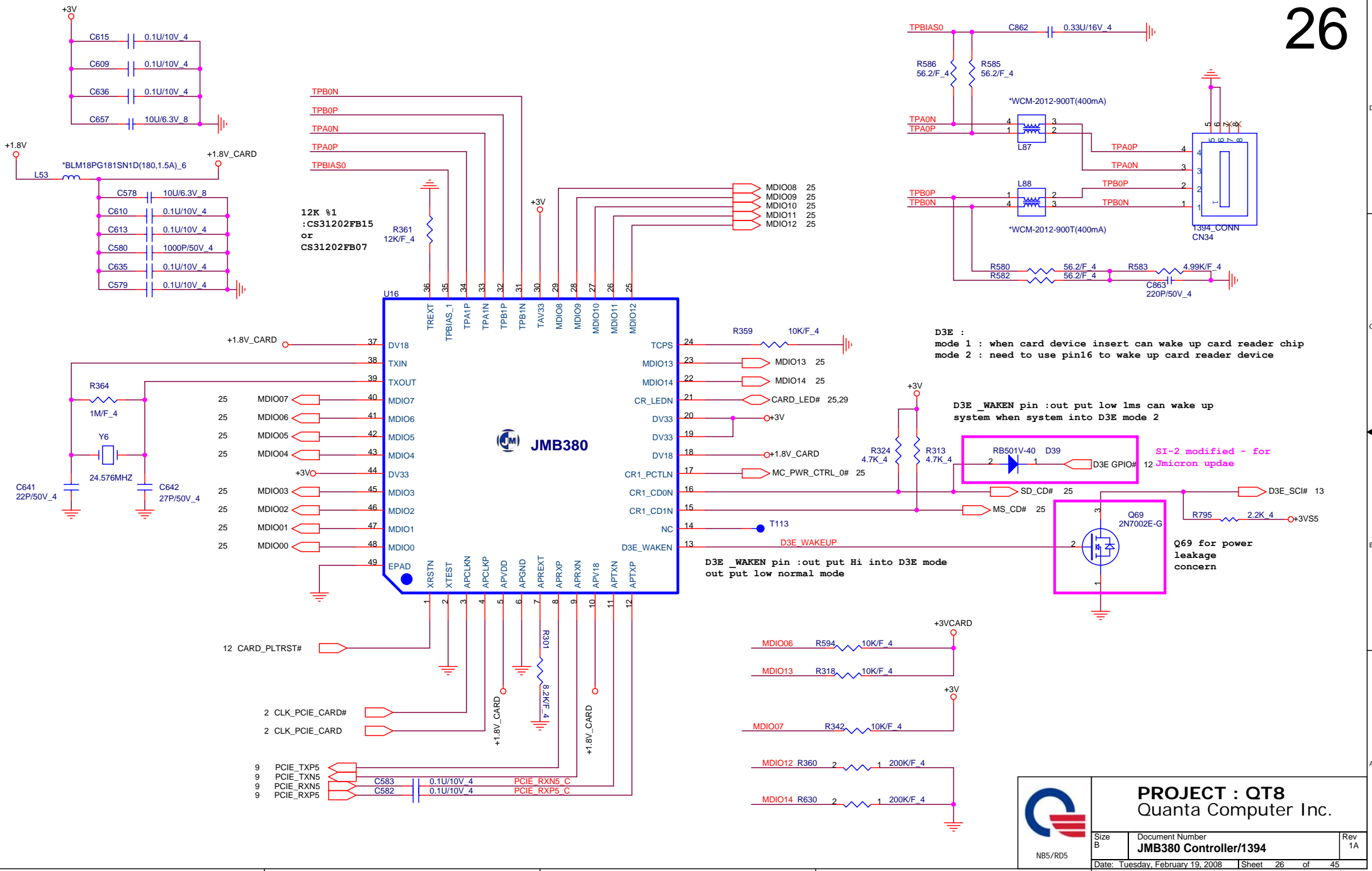
SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD_D4
SP5		XD_D5
SP6	SD_DAT1	MS_D1
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9		MS_INS#
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD_D0
SP13	SD_DAT4	XD_WP#
SP14		XD_R/#
SP15	SD_DAT3	XD_WE#
SP16	SD_DAT2	XD_RE#
SP17		XD_ALE
SP18		XD_CE#
SP19		XD_CLE



JMB 380 Note:

SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0
MDID1	SD_DAT1	MS_D1
MDID2	SD_DAT2	MS_D2
MDID3	SD_DAT3	MS_D3
MDID4	SD_CMD	MS_BS
MDID5	SD_CLK	MS_SCLK
MDID6	SD_WP	XD_WP#
MDID7		XD_CLE
MDID8	SD_DAT4	XD_D4
MDID9	SD_DAT5	XD_D5
MDID10	SD_DAT6	XD_D6
MDID11	SD_DAT7	XD_D7
MDID12		XD_RE#
MDID13		XD_R/#
MDID14		XD_ALE
CR1_LED#	SD1_LED#	MS1_LED#
CR1_PCTLN	SD1_PCTLN	MS1_PCTLN
CR1_CD0	SD1_CD#	MS1_CD#
CR1_CD1		MS1_CD#





D3E :
 mode 1 : when card device insert can wake up card reader chip
 mode 2 : need to use pin16 to wake up card reader device

D3E_WAKEN pin : out put low lms can wake up system when system into D3E mode 2

RB501V-40 D39 SI-2 modified - for Jmicron updae

Q69 2N7002E-G Q69 for power leakage concern

D3E_WAKEN pin : out put Hi into D3E mode
 out put low normal mode



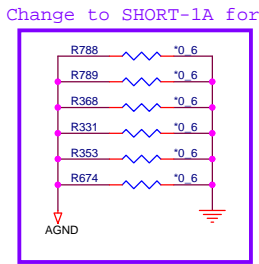
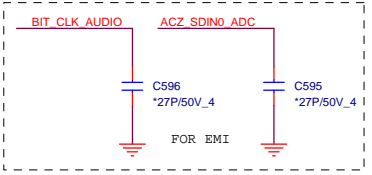
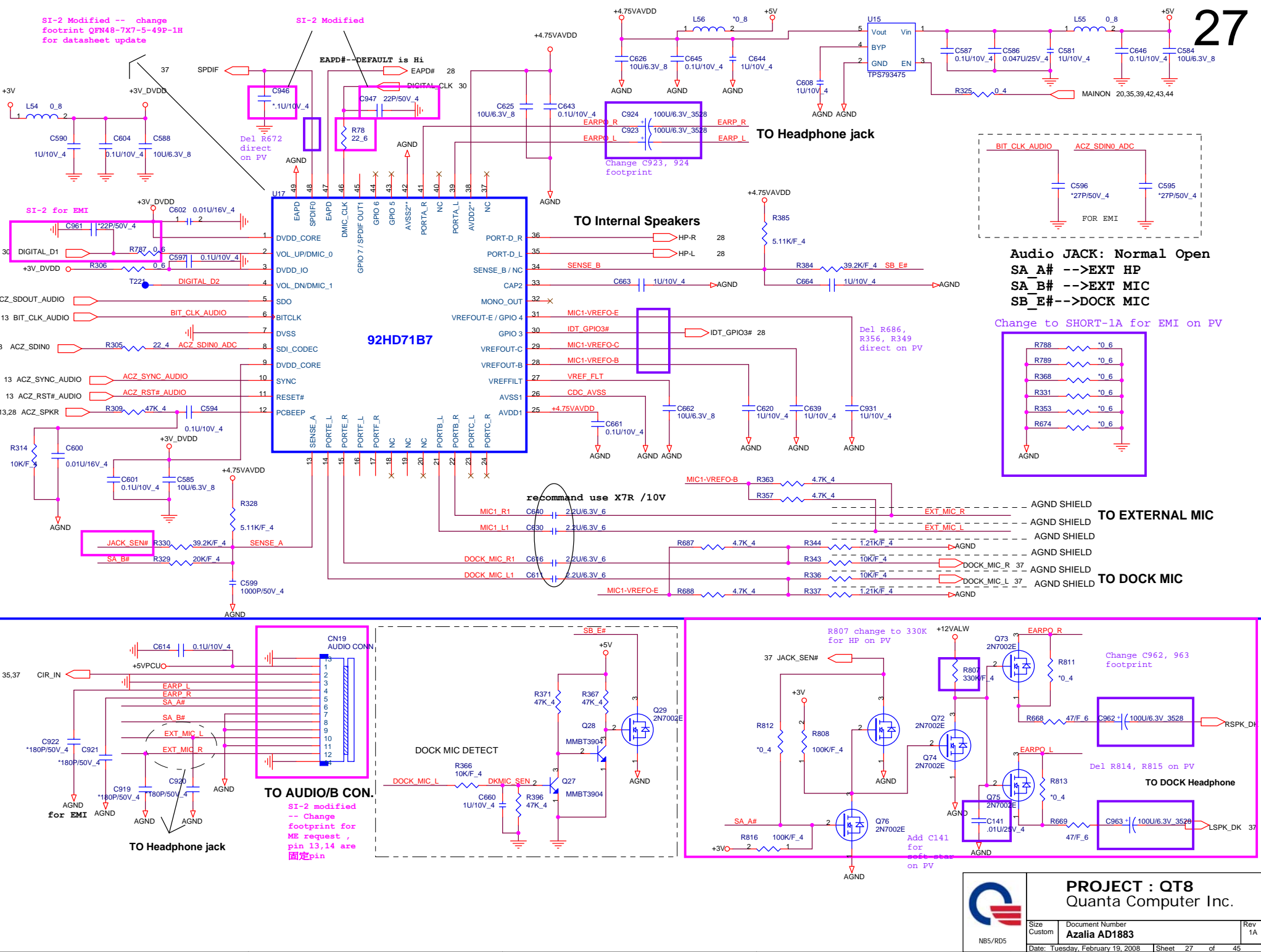
PROJECT : QT8
 Quanta Computer Inc.

Size B	Document Number JMB380 Controller/1394	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 26	of 45

NB5/RD5

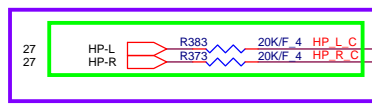
SI-2 Modified -- change footprint QFN48-7X7-5-49P-1H for datasheet update

SI-2 Modified

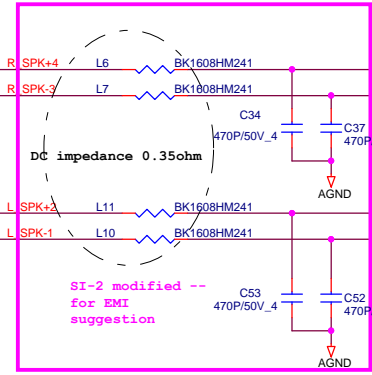
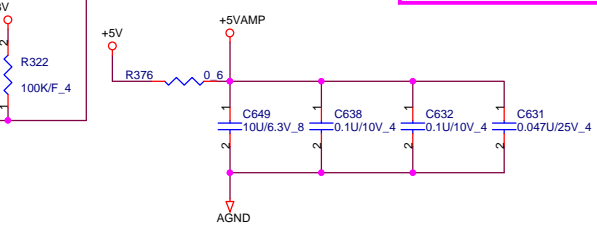
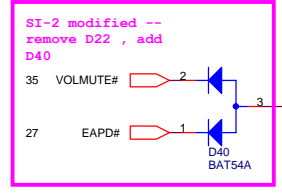
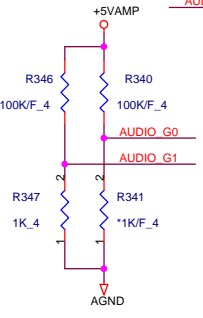


SI-2 Modified -- remove C621/C623

LIN-,RIN- and LIN+,RIN+ swap for BOBO noise on PV

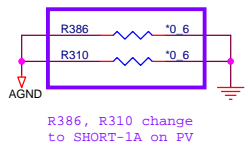


PV-1 Modified --R383 , R373 change from 20Kohm to 0 ohm for Volume too low issue



INT. SPEAKER

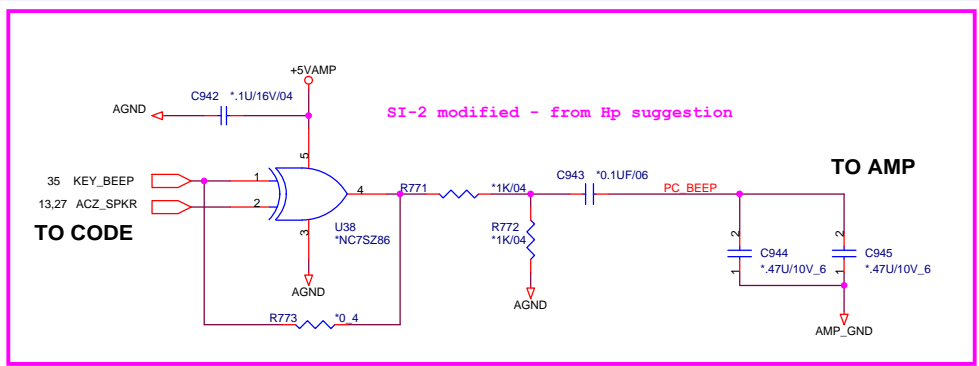
$V_{rms} = V_{pp} / 2 \sqrt{2}$
 $Power = (V_{rms})^2 / R$
 QT8 speaker -- 3.2ohm / 2W



6017A2 Gain Table

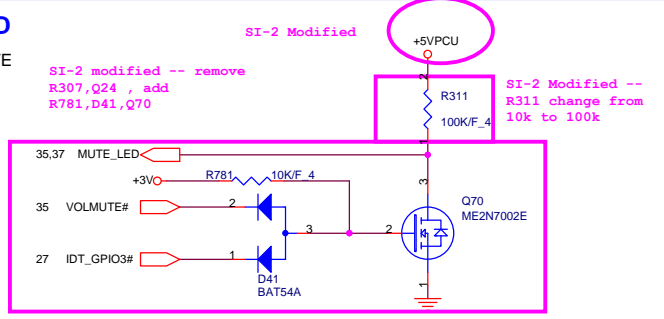
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

PC-BEEP

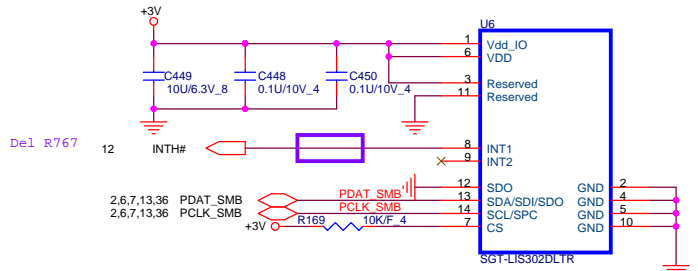


MUTE_LED

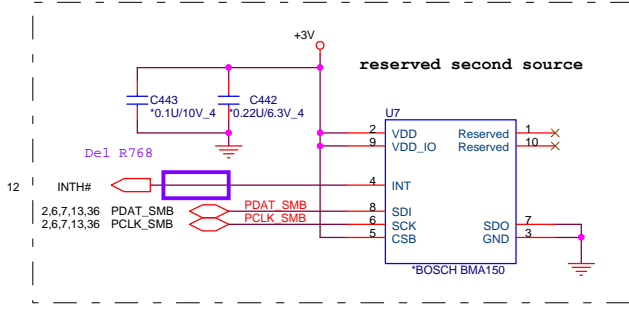
Low --> un-MUTE
 High --> Mute



Acceleration sensor

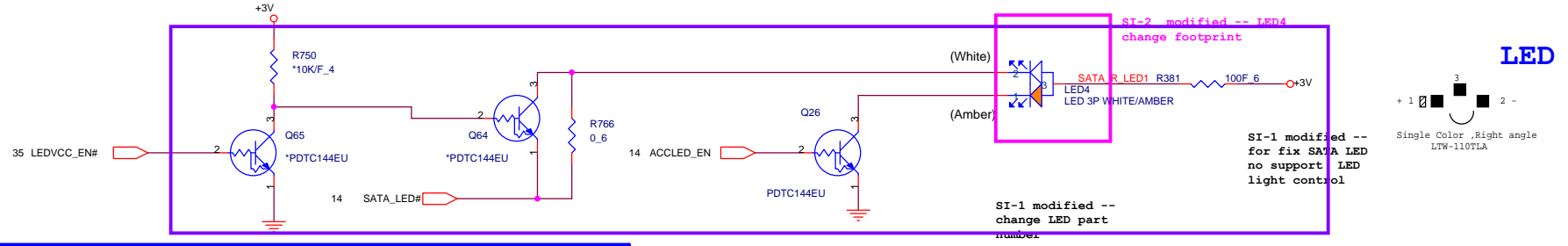
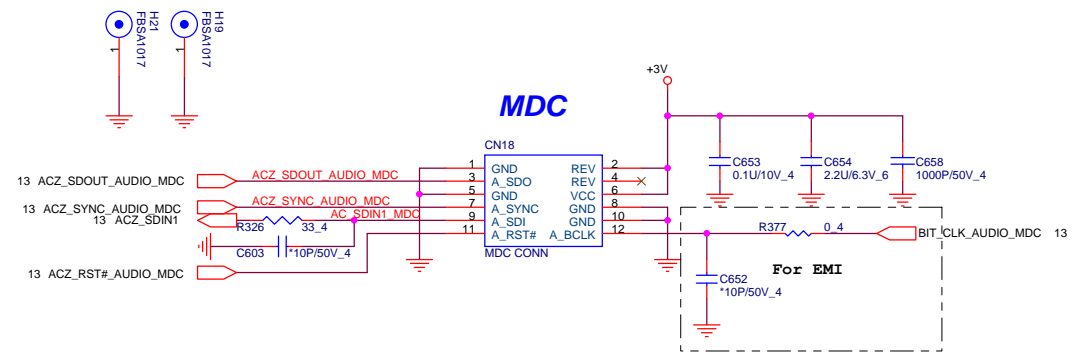


SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

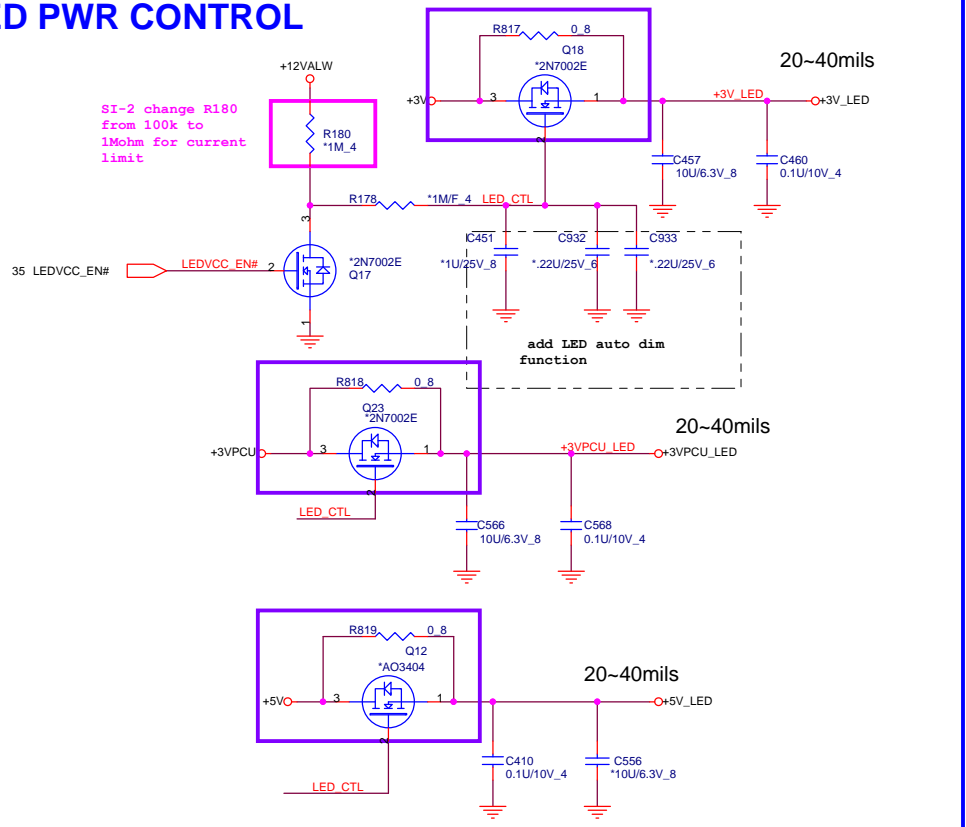


PROJECT : QT8
 Quanta Computer Inc.

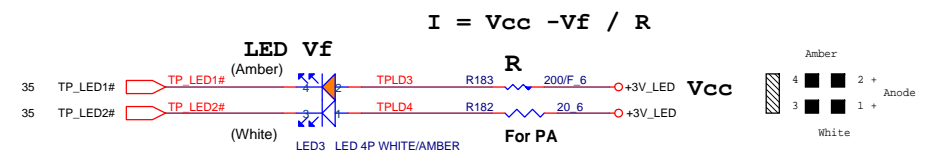
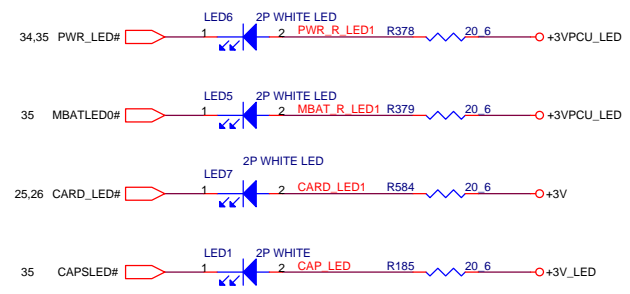
Modem CONN



LED PWR CONTROL

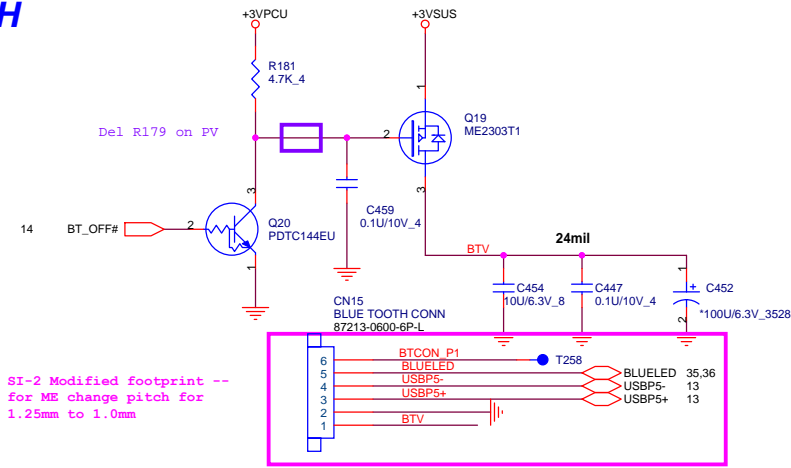


Del R380
Change R381 to 100
Add R766, R817, R818,
R819
LED PWR control no-stuff
on PV



	PROJECT : QT8 Quanta Computer Inc.		
	Size Custom Date: Tuesday, February 19, 2008	Document Number MDC1.5 Con Accelerometer/LED	Rev 1A
NBS/RD5		Sheet 29 of 45	

BLUETOOTH

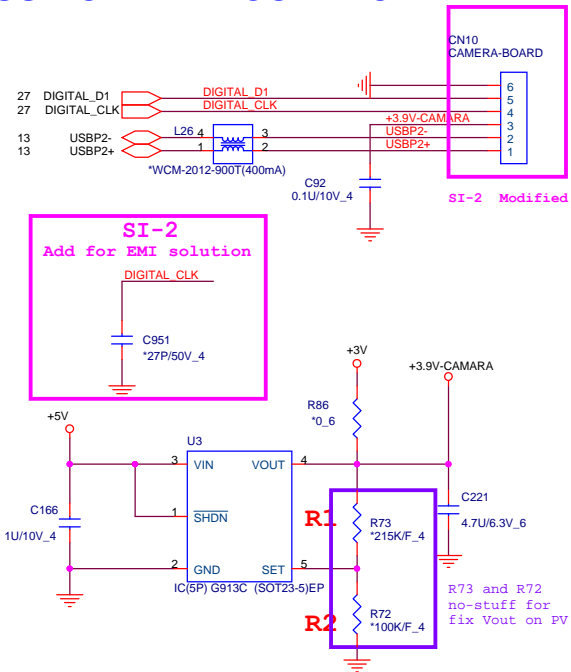


SI-2 Modified footprint --
for ME change pitch for
1.25mm to 1.0mm

For Discrete Touch-Screen



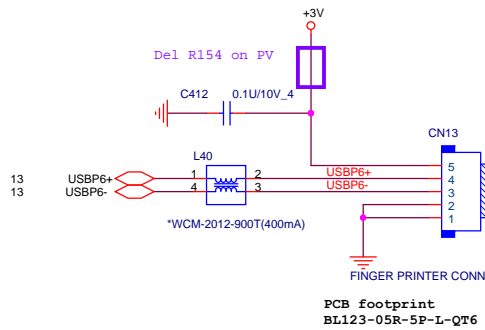
USB CAMERA CONNECT



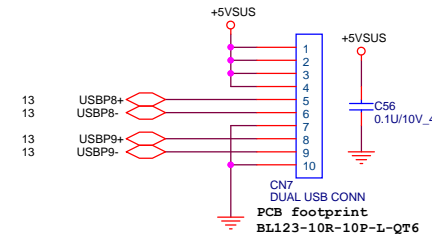
$$V_{out} = 1.25 (1 + R1/R2)$$

USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

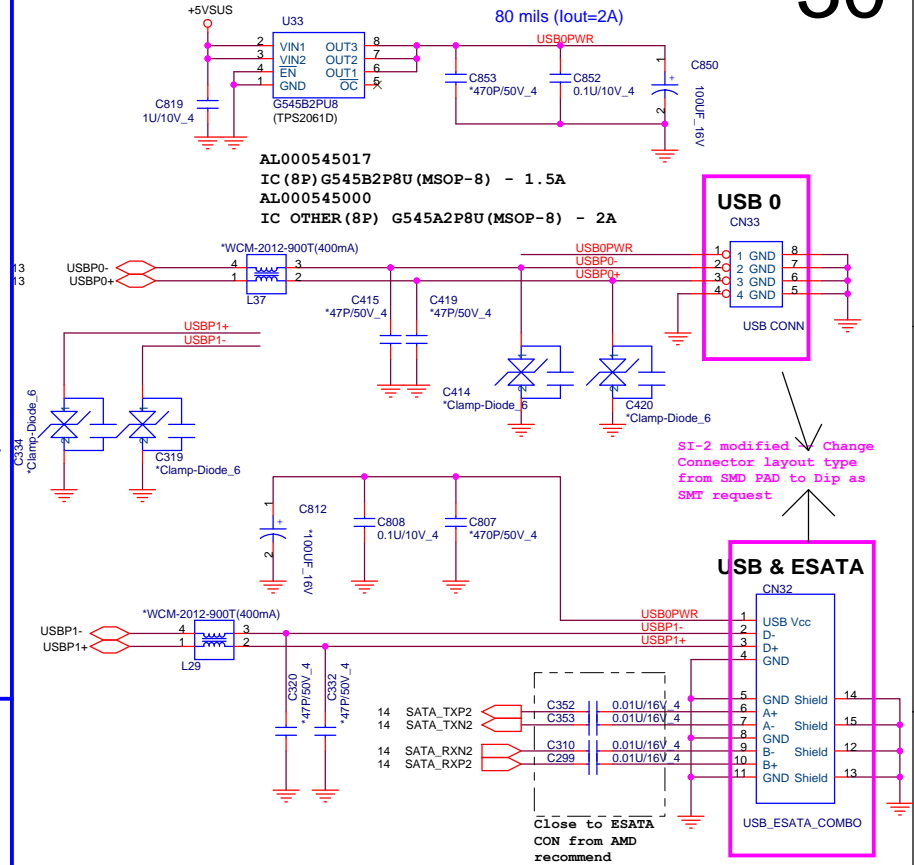


RIGHT SIDE USB2



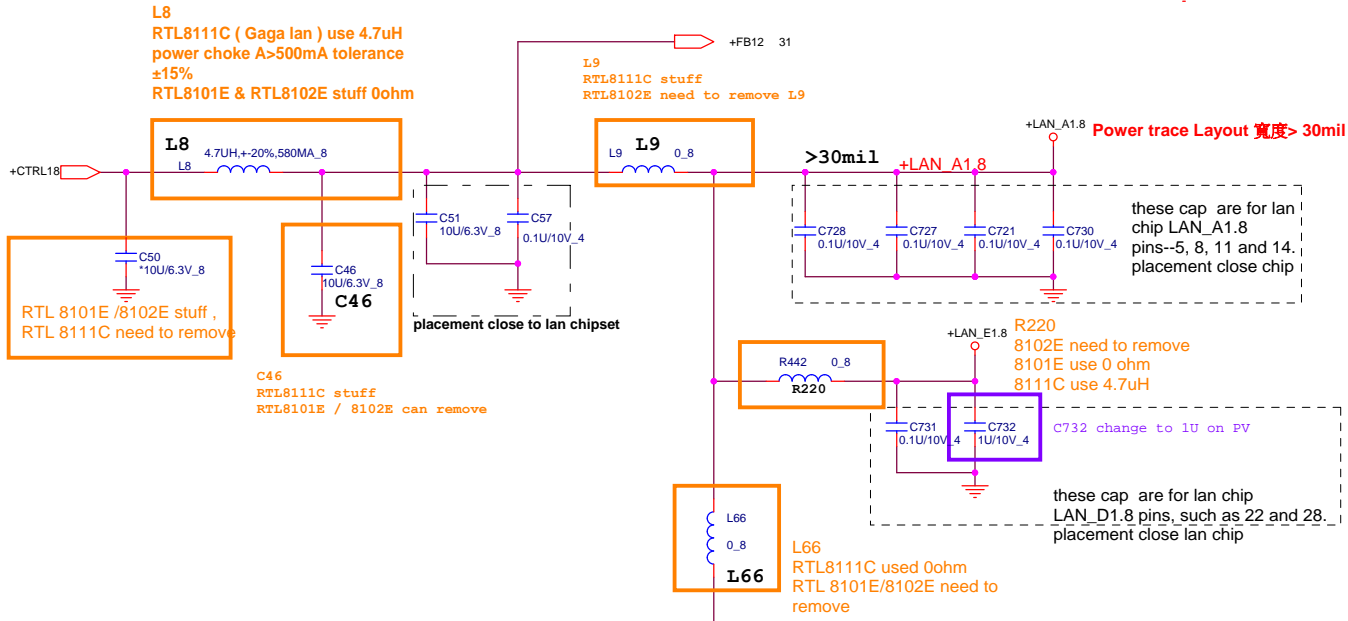
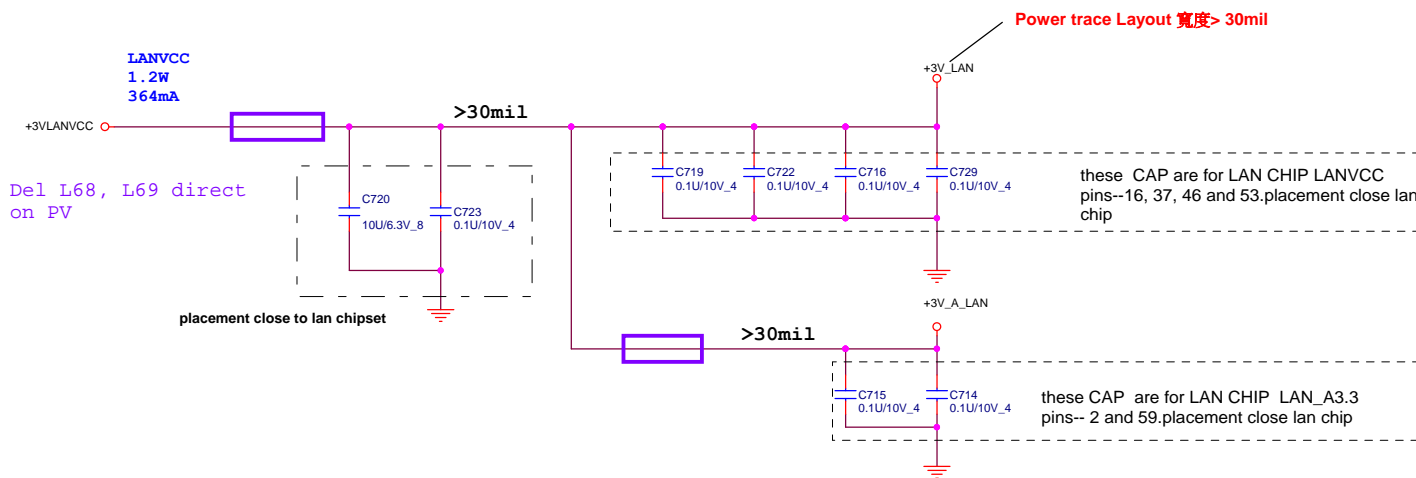
LEFT SIDE USBX1 and E-SATA/USB COMBO

30



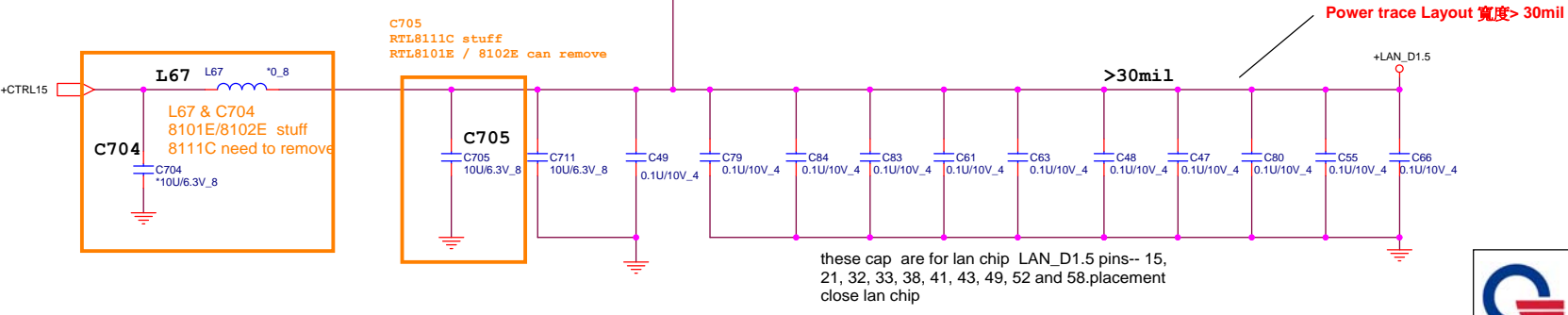
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number BT/WEBCAM/FT/USBX4/ESATA	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 30 of 45	



Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

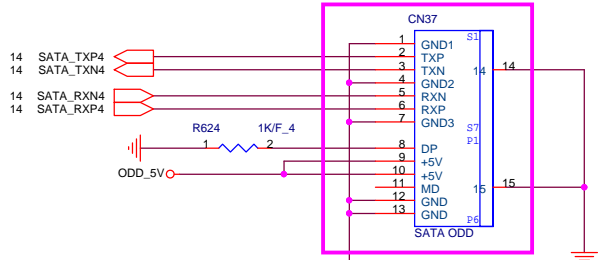


PROJECT : QT8
Quanta Computer Inc.

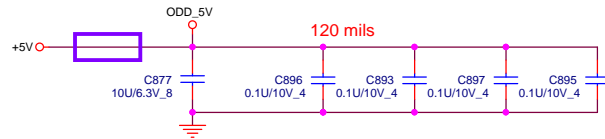
Size Custom	Document Number LAN Power	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 32 of 45		

SATA CD-ROM

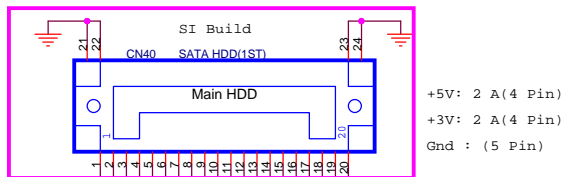
SI-2 Modified footprint -- Modify 12/27



Del L90 direct on PV

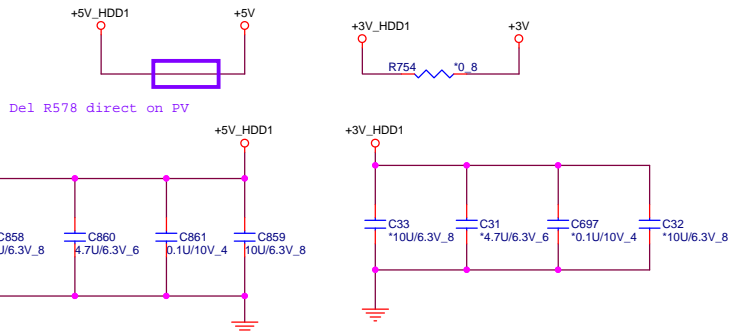


SI-2 Modified footprint -- Modify 固定孔 Size as SMT request



+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd: (5 Pin)

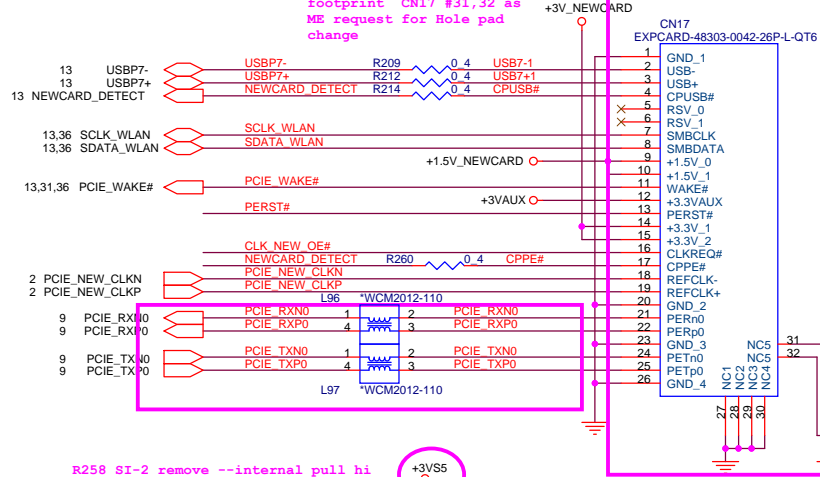
+3V_HDD1
+5V_HDD1



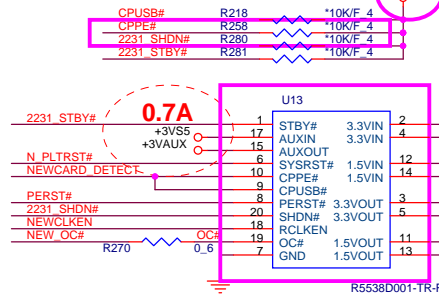
Del R578 direct on PV

NEWCARD

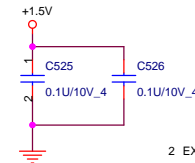
SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change



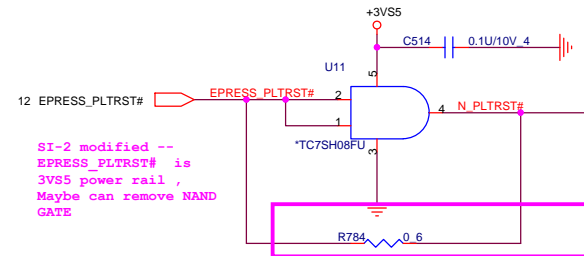
R258 SI-2 remove --internal pull hi



R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

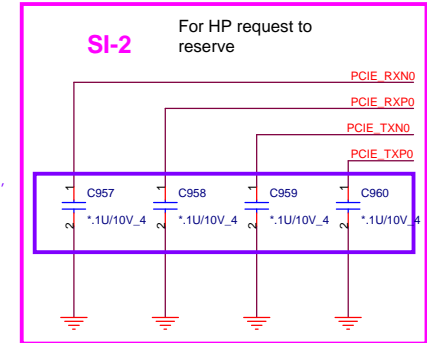
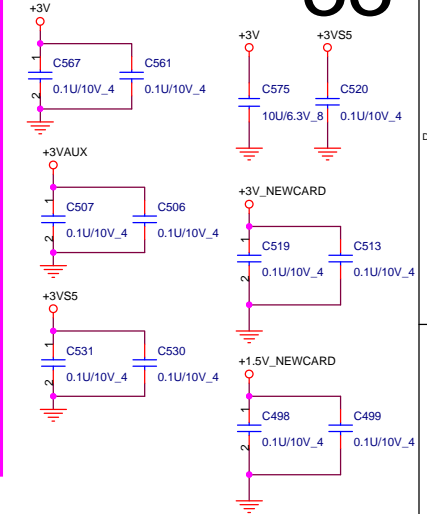


SI-2 modified -- EPRESS_PLTRST# is 3V5S power rail, Maybe can remove NAND GATE



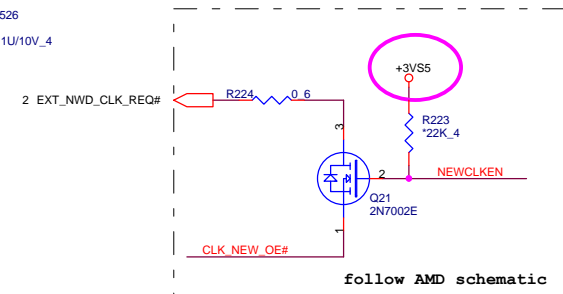
NEWCARD (PCIEXPRESS*1 + USB*1)

33



For HP request to reserve

Del R790, R791, R792, R793 for RF on PV

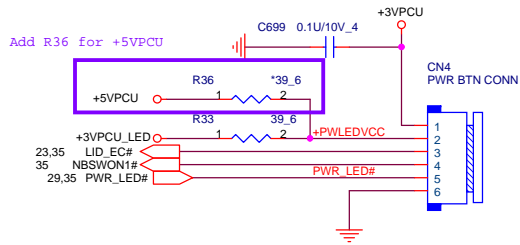


follow AMD schematic

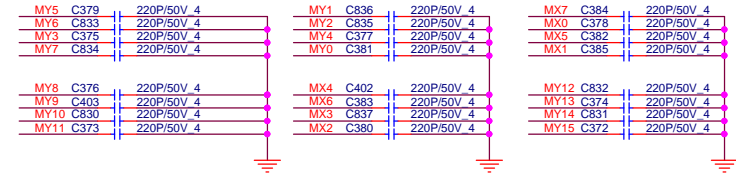
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number NEW CARD/SATA ODD/SATA HDD	Rev 1A
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POWER BUTTON CONNECT

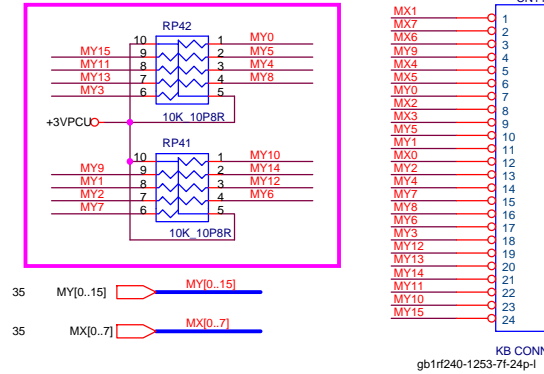


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



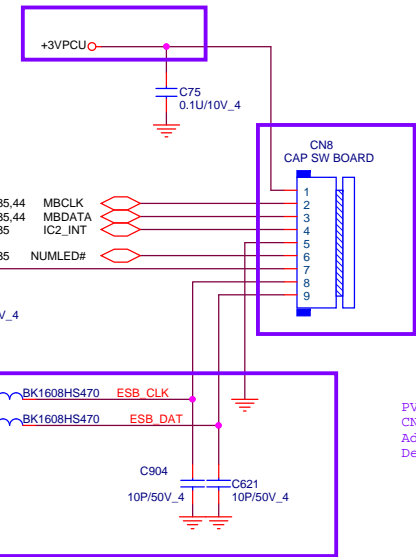
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



gb1rf240-1253-7f-24p-1

CAP SW CONNECT

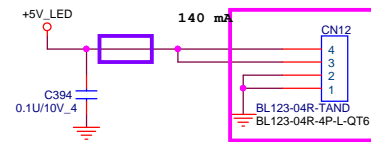


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

FV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103

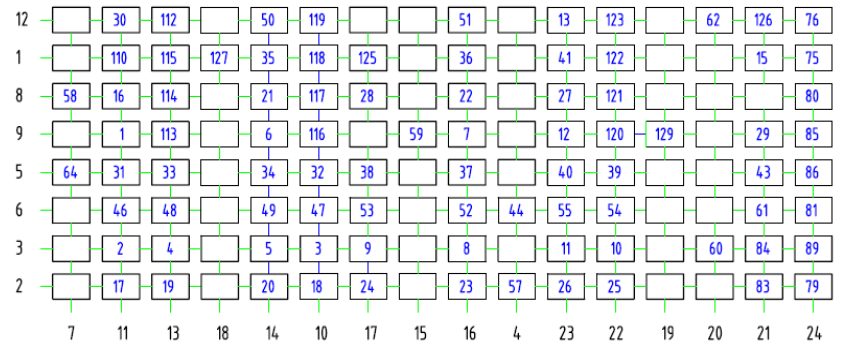
Del R770 on PV

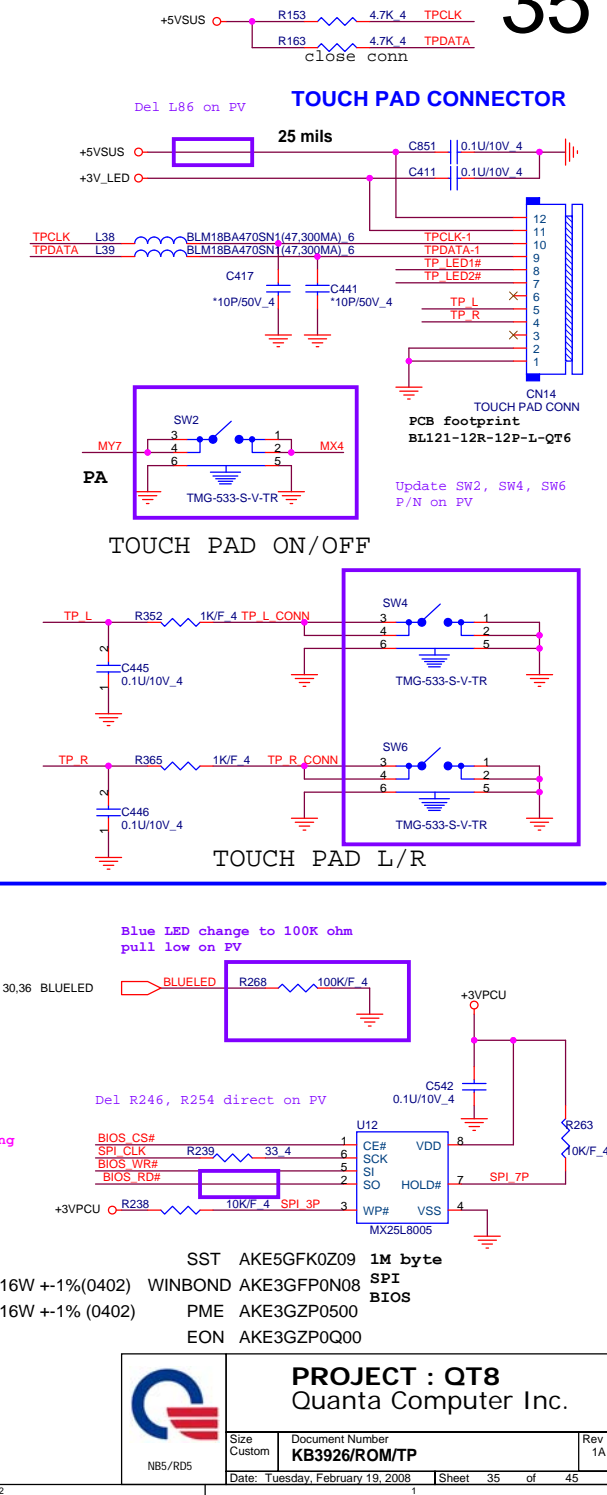
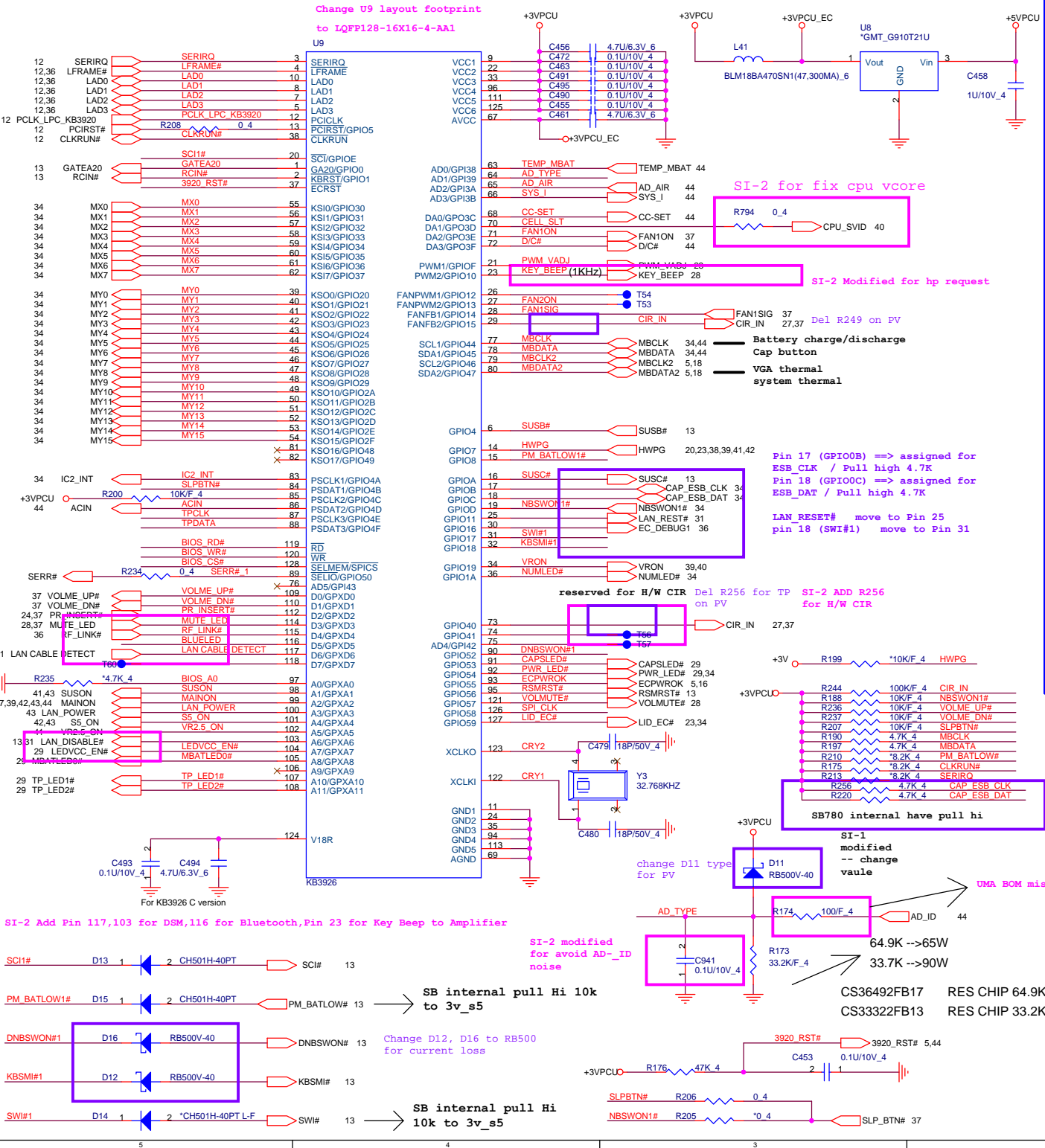
SI-2 Modified 12/27



1. LEDVCC
2. LEDVCC
3. NC
4. GND

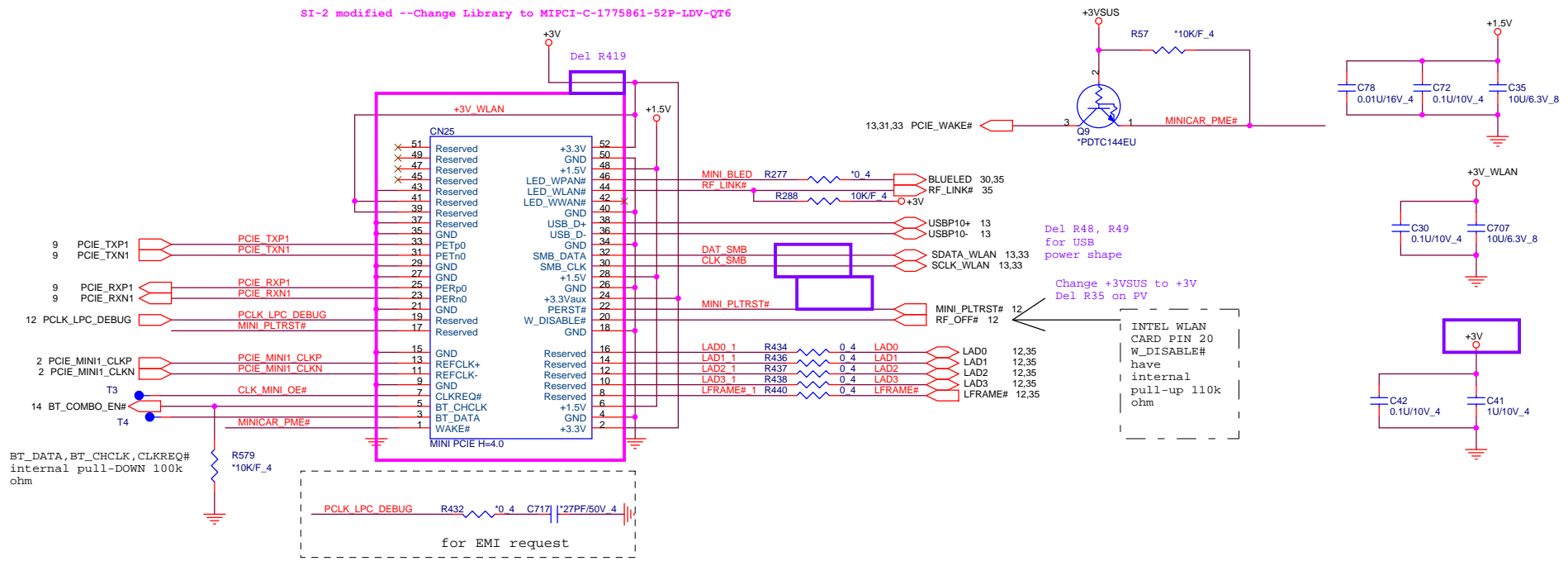
SI-2 Modified



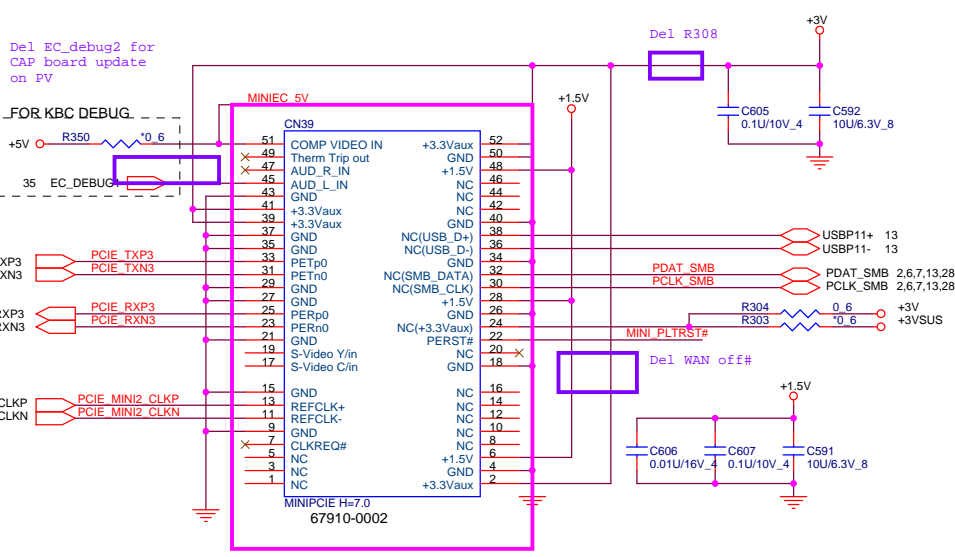


Mini PCI-E Card 1 WLAN

SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6



Mini PCI-E Card 2 TV tuner card

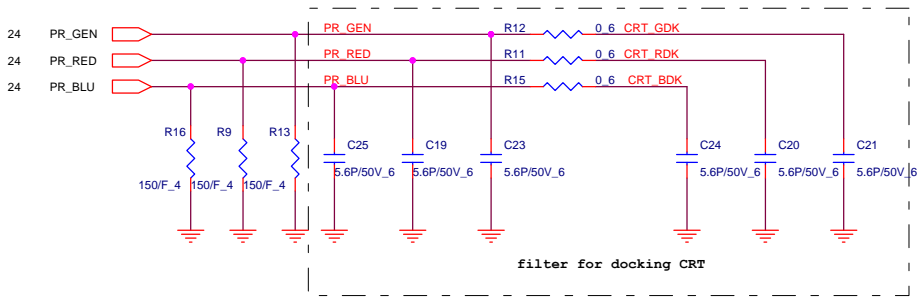
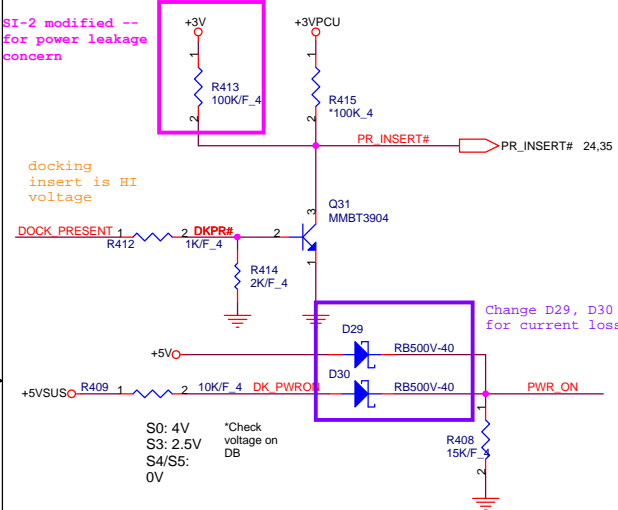
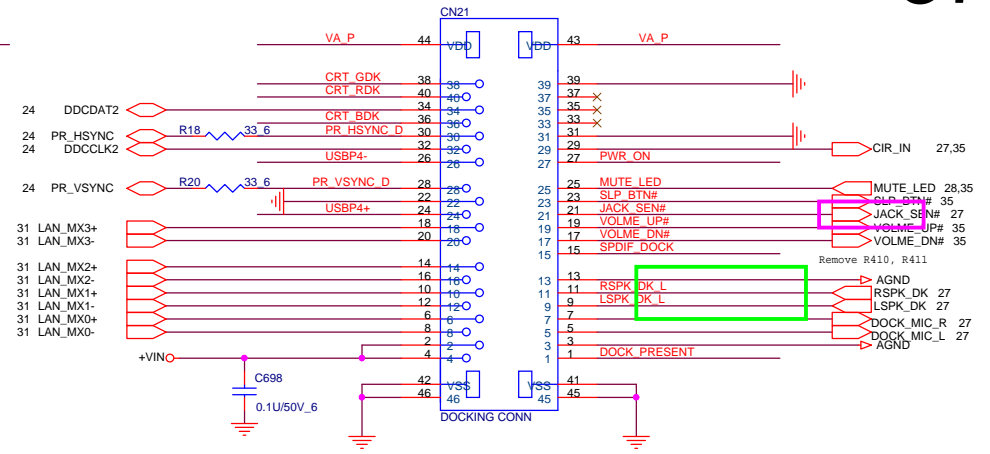
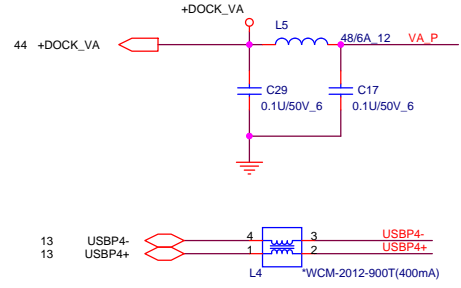
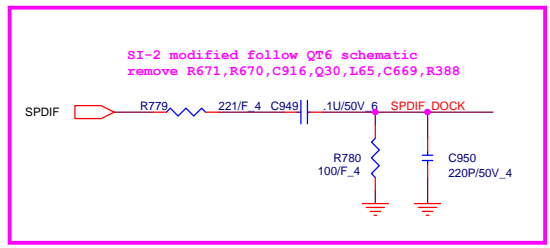


SI-2 modified --Change Library to MIPCI-P04-FJ504-170-52P-QT6

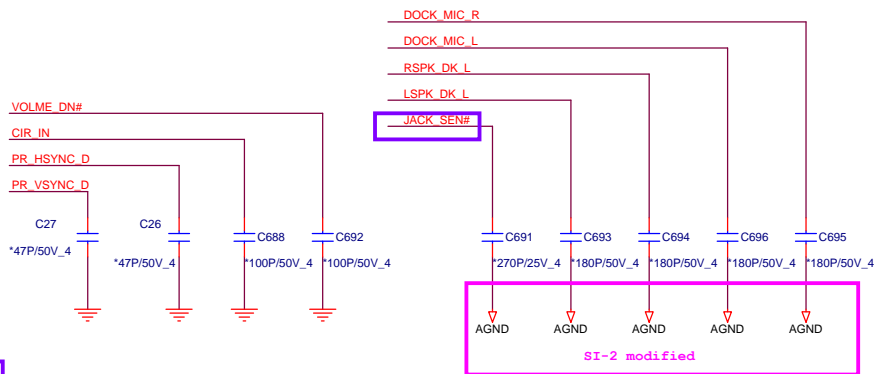
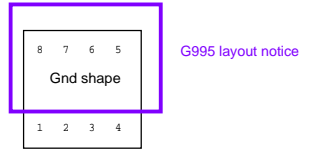
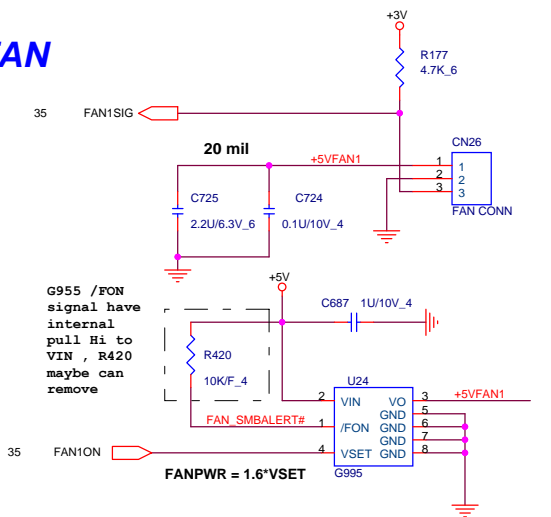
	PROJECT : QT8	
	Quanta Computer Inc.	
Size Custom	Document Number Mini CARD X 3	Rev 1A
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CABLE DOCK

support 6A 200mils
CX000480005



CPU FAN



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	Size Custom	Document Number CABLE DOCKING/FAN	
NB5/RD5		Sheet 37 of 45	

DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,18,20,23,24,25,26,27,28,29,30,31,33,35,36,37,39,43

TON: 5V / 3.3V
 GND = 400 / 500KHz
 REF = 400 / 300KHz
 VCC = 200 / 300KHz

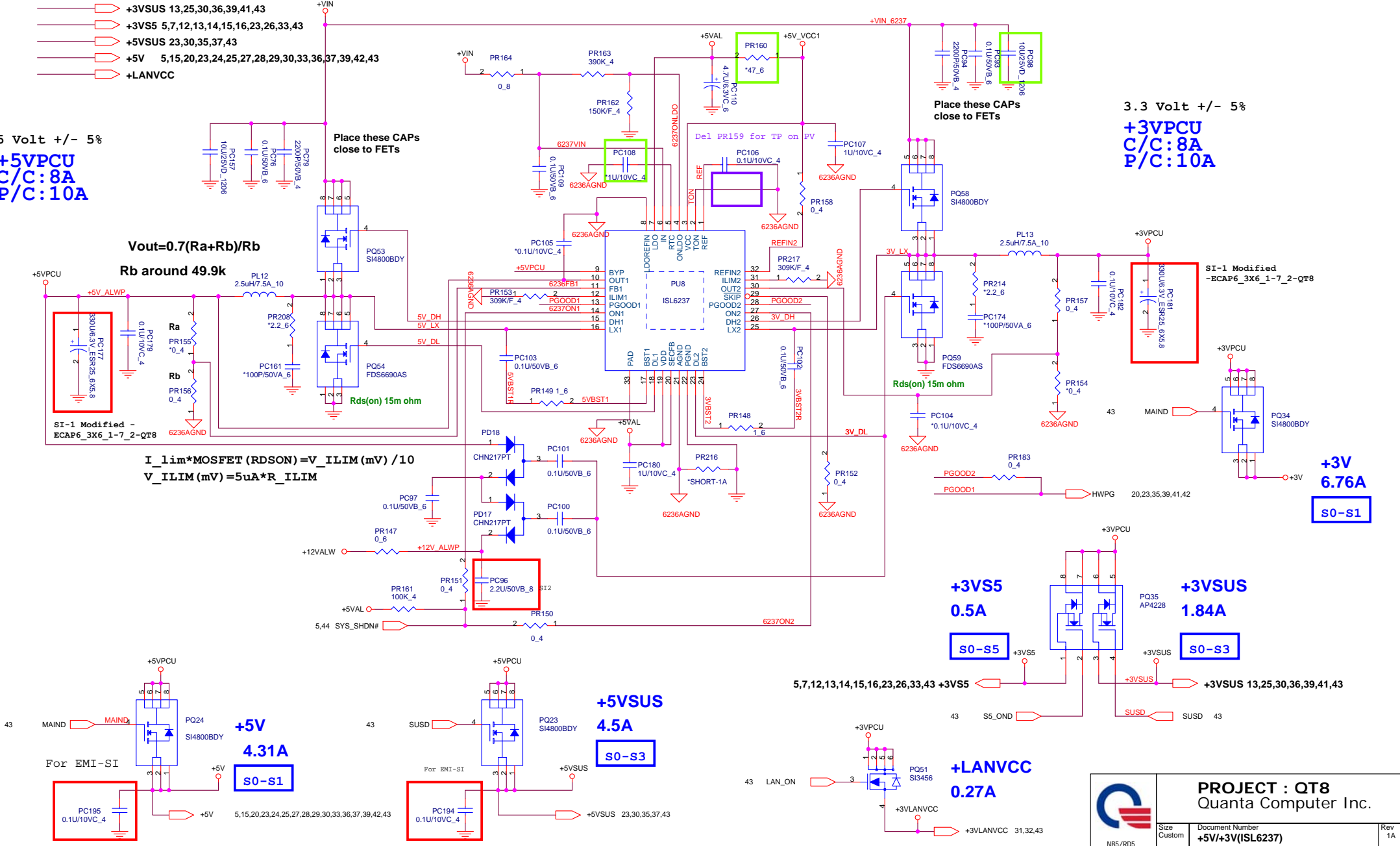
- +5VPCU 27,28,34,35,39,40,41,42,43
- +3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
- +3VSUS 13,25,30,36,39,41,43
- +3VS5 5,7,12,13,14,15,16,23,26,33,43
- +5VSUS 23,30,35,37,43
- +5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
- +LANVCC

5 Volt +/- 5%
+5VPCU
 C/C: 8A
 P/C: 10A

3.3 Volt +/- 5%
+3VPCU
 C/C: 8A
 P/C: 10A

$V_{out} = 0.7(Ra + Rb) / Rb$
 Rb around 49.9k

$I_{lim} * MOSFET (RDSON) = V_{ILIM} (mV) / 10$
 $V_{ILIM} (mV) = 5uA * R_{ILIM}$



Place these CAPs close to FETs

Place these CAPs close to FETs

SI-1 Modified - ECAP6_3X6_1-7_2-QT8

SI-1 Modified - ECAP6_3X6_1-7_2-QT8

+3V 6.76A
 S0-S1

+3VS5 0.5A
 S0-S5

+3VSUS 1.84A
 S0-S3

+5VSUS 4.5A
 S0-S3

+5V 4.31A
 S0-S1

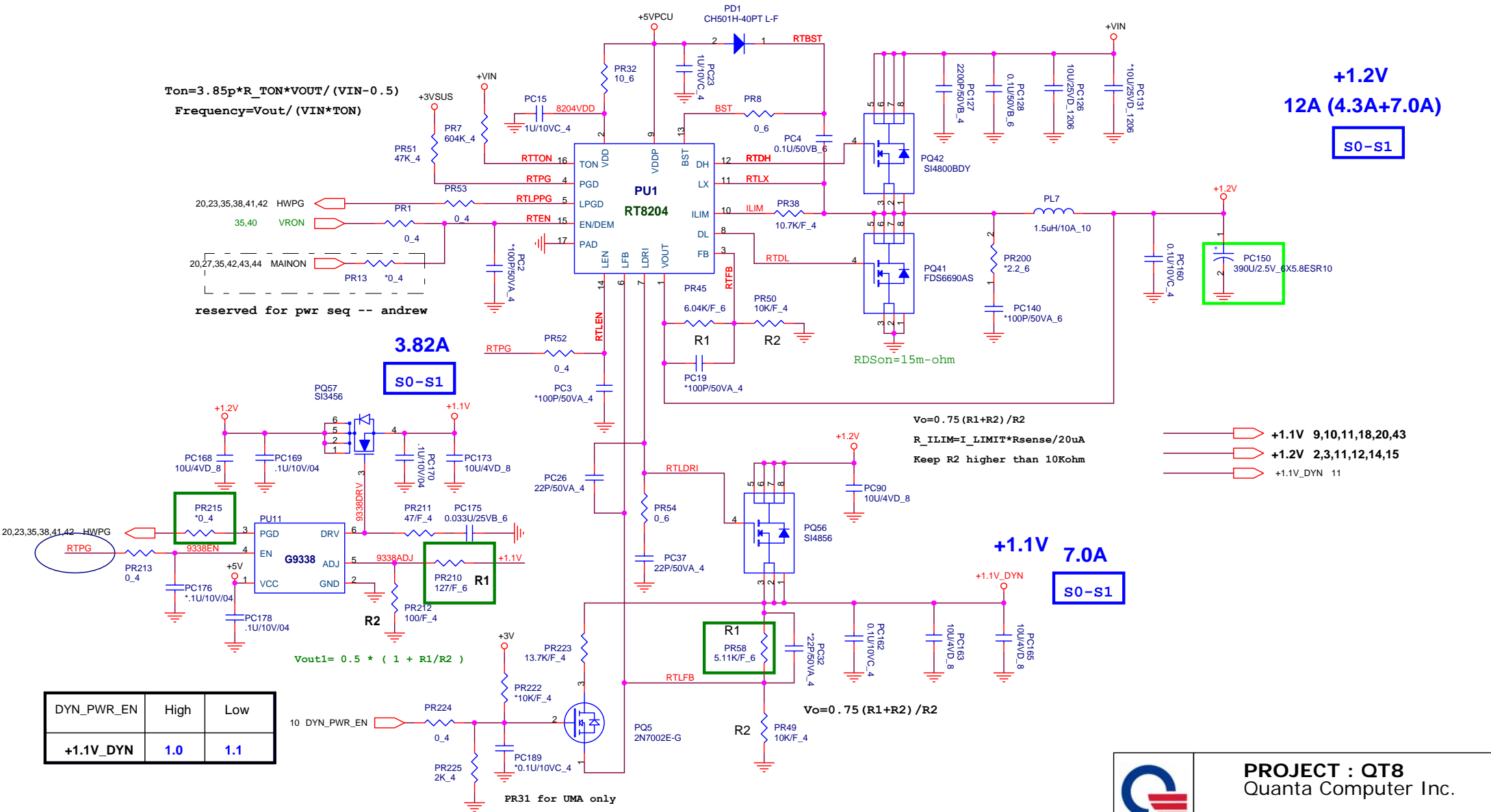
+LANVCC 0.27A

	PROJECT : QT8 Quanta Computer Inc.	
	Size Custom Document Number +5V/+3V(ISL6237) Date: Tuesday, February 19, 2008	Rev 1A Sheet 38 of 45

$$T_{on} = 3.85p * R_{TON} * V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} * TON)$$

+1.2V
12A (4.3A+7.0A)
S0-S1



reserved for pwr seq -- andrew

3.82A
S0-S1

$$V_o = 0.75 (R1 + R2) / R2$$

$$R_{ILIM} = I_{LIMIT} * R_{sense} / 20uA$$

Keep R2 higher than 10Kohm

- +1.1V 9,10,11,18,20,43
- +1.2V 2,3,11,12,14,15
- +1.1V_DYN 11

+1.1V
7.0A
S0-S1

$$V_{out1} = 0.5 * (1 + R1/R2)$$

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

PR31 for UMA only



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 Quanta Computer Inc.

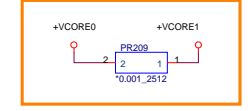
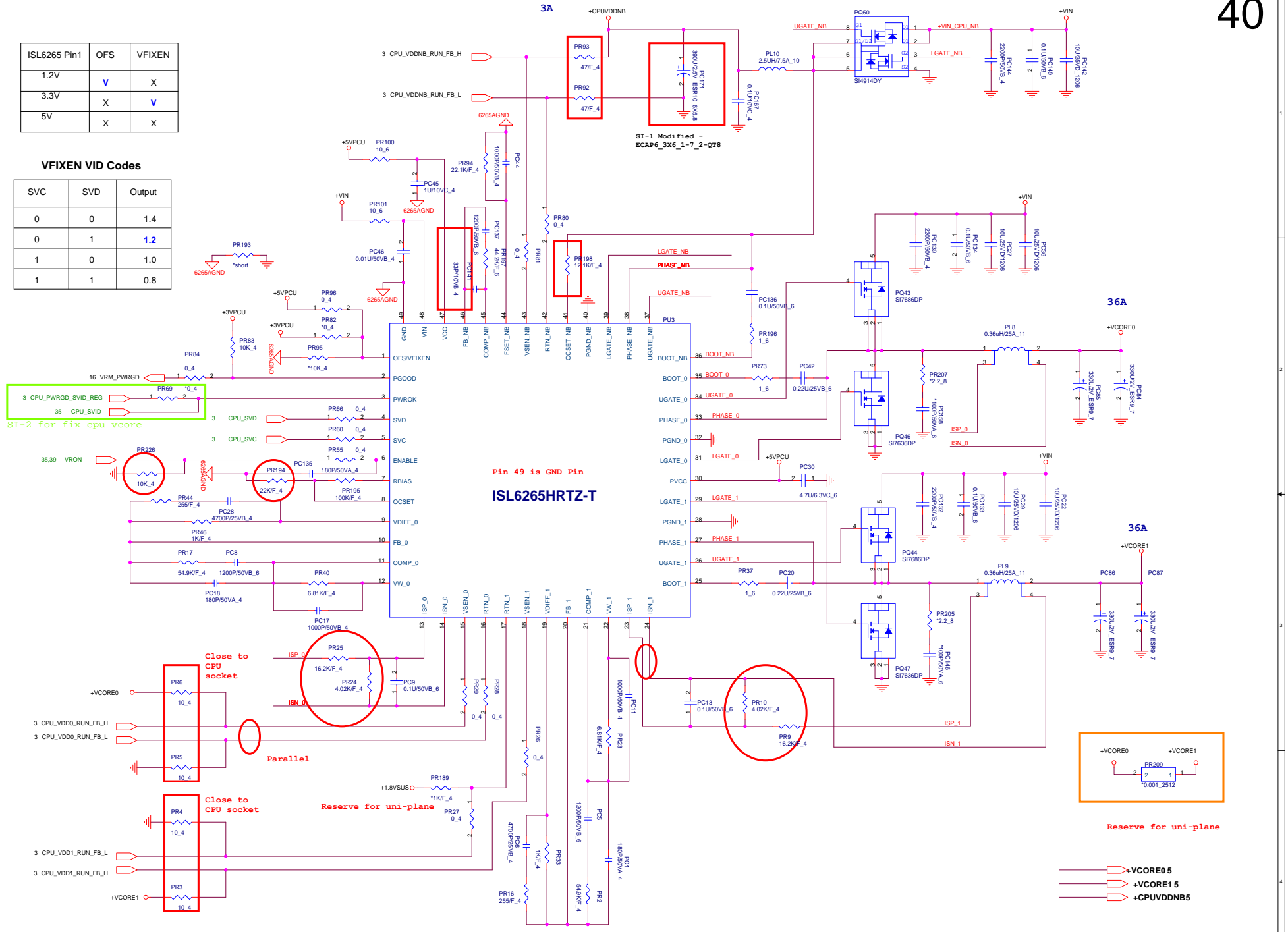
Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 1A
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

SI-2 for fix cpu vcore
 3 CPU_PWRGD_SVID_REG
 35 CPU_SVID



- +V CORE0 5
- +V CORE1 5
- +CPUVDDNB5

+2.5V 3
+1.8VSUS 3,4,5,6,7,40,42,43

+1.8VSUS
23.65A
S0~S3

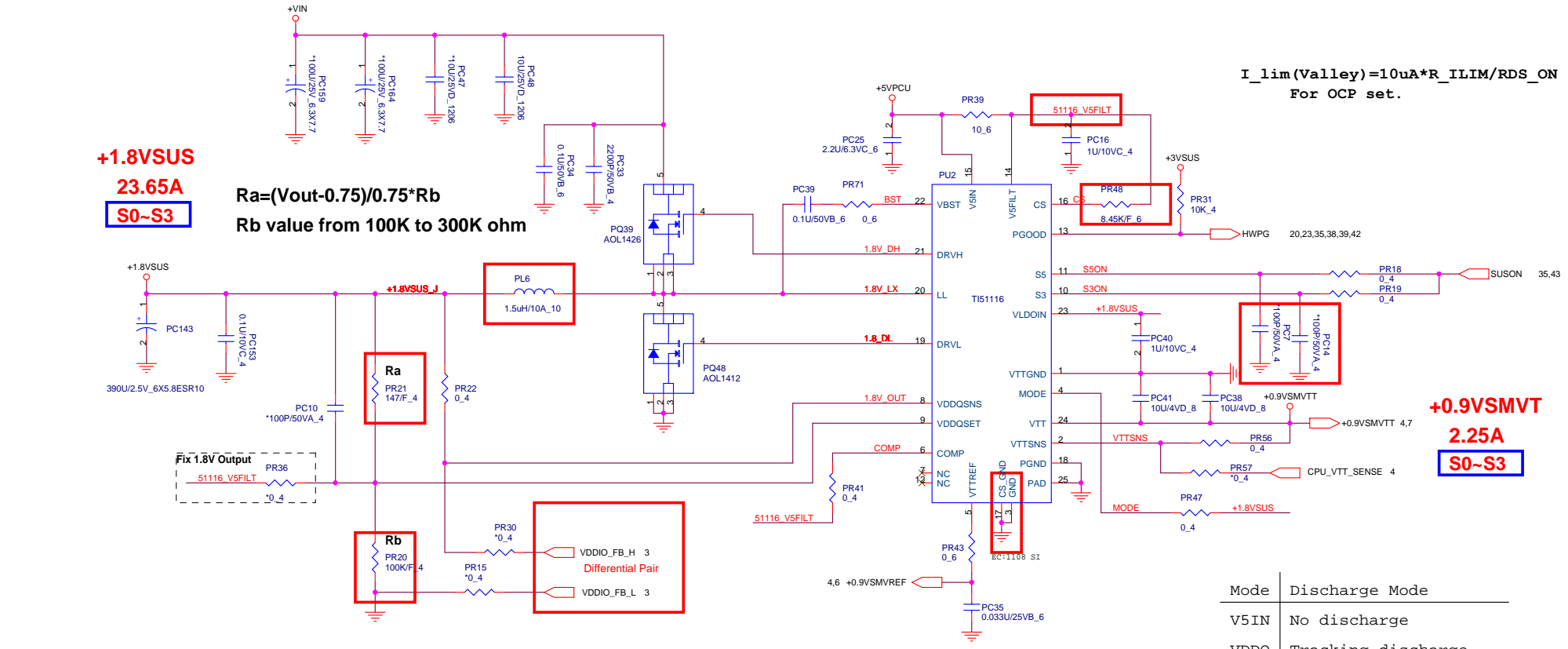
$Ra = (V_{out} - 0.75) / 0.75 * Rb$
Rb value from 100K to 300K ohm

$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS_ON}$
For OCP set.

+0.9VSMVT
2.25A
S0~S3

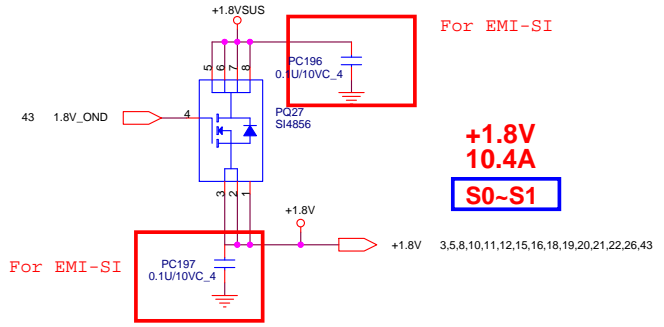
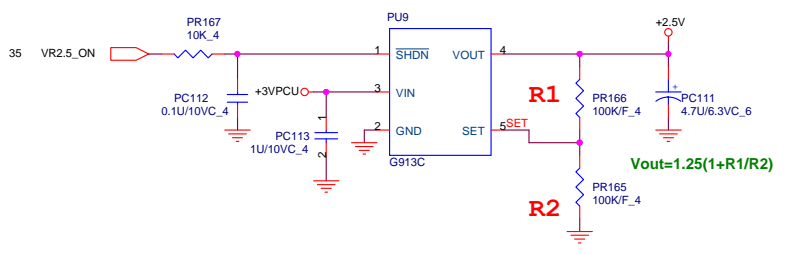
+2.5V
0.25A
S0~S1

+1.8V
10.4A
S0~S1



Fix 1.8V Output
51116_VSFILT

Close to CPU
SI power



Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge


$V_TRIP(mV) = R_TRIP(Kohm) * 10(\mu A)$
 $I_OCP = V_trip / R_{ds_on} + I_Ripple / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_vddqsns / 2$	DDR
V5IN	1.8	$V_vddqsns / 2$	DDR2
FB	adjustable	$V_VDDQSNS / 2$	$1.5V < VDDQ < 3V$

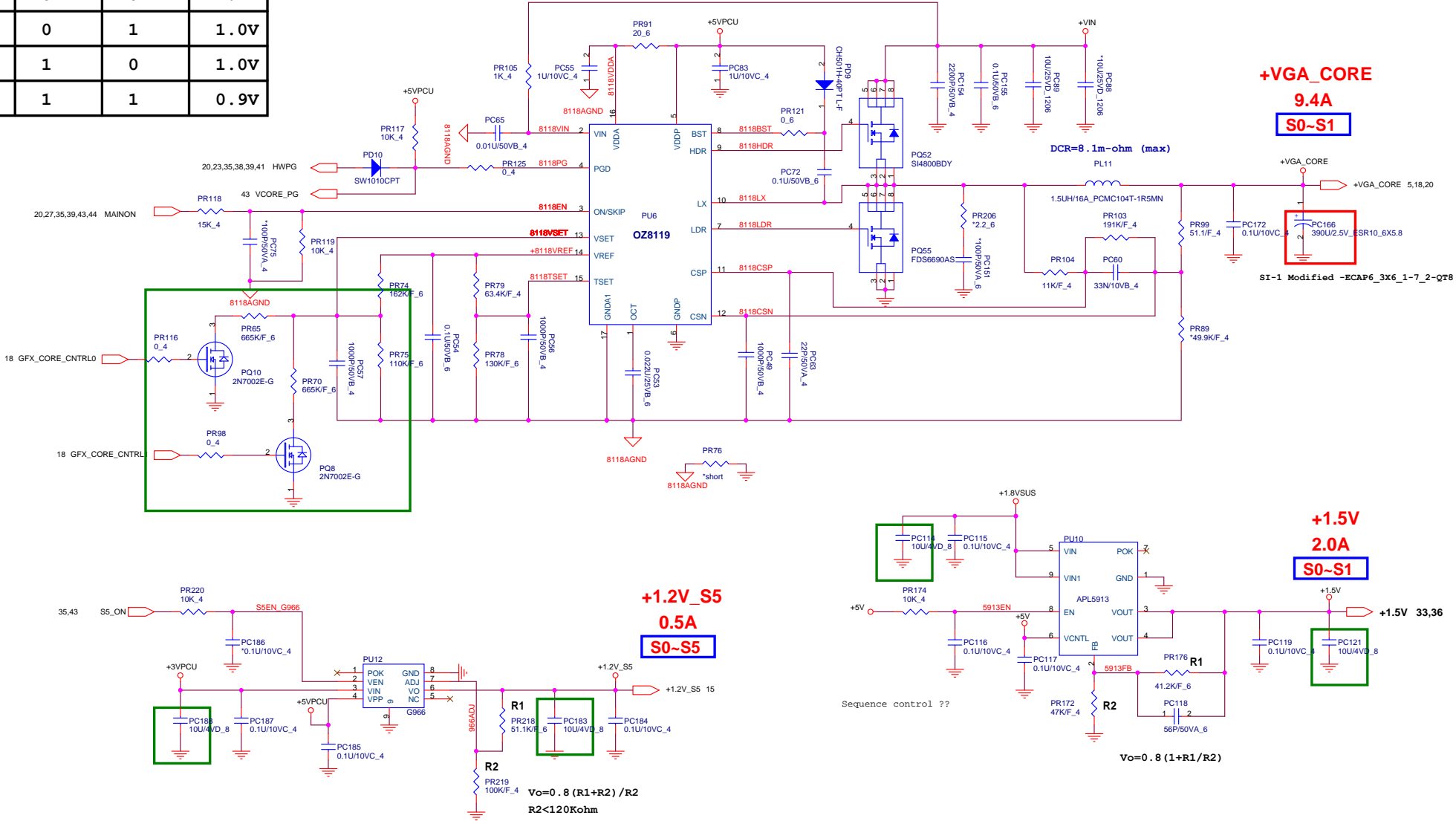
Discrete: SI4856
UMA: SI4800

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	Size Custom Document Number 1.8VSUS/DDR_VTER/+1.8V/2.5V	Rev 1A
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ATI M82-SE

-  +VGA_CORE5,18,20
-  +1.2V_S5 15
-  +1.5V 33,36

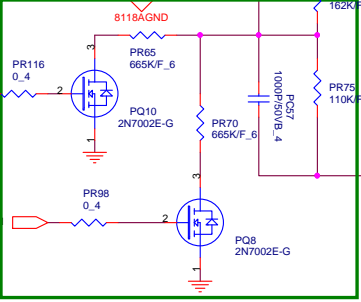
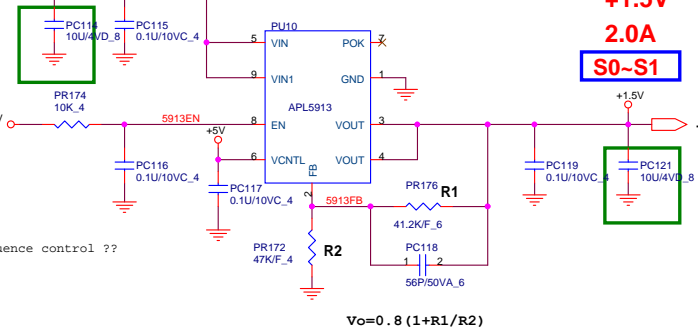
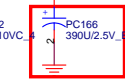
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V



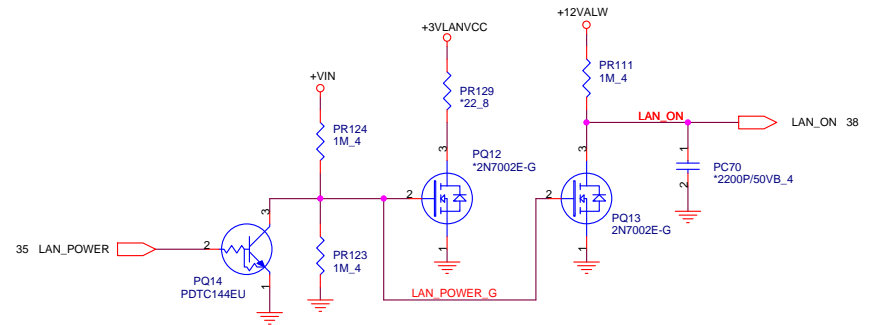
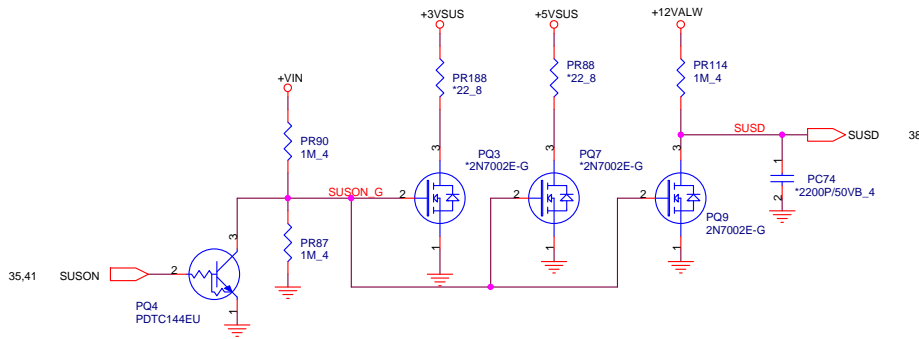
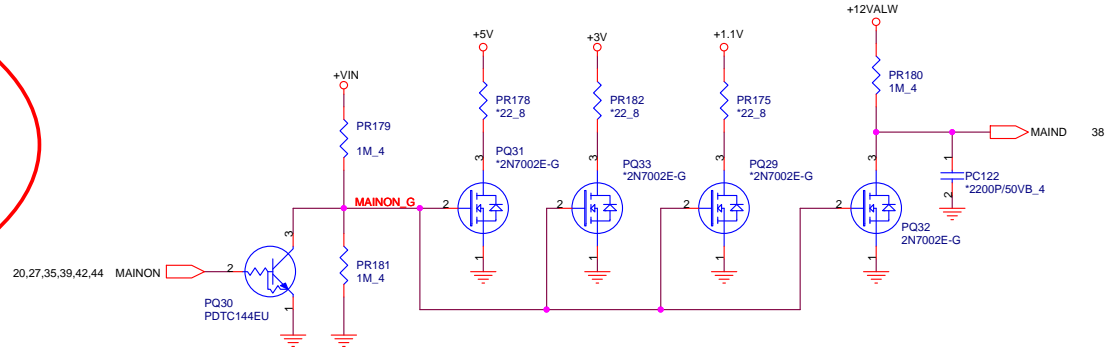
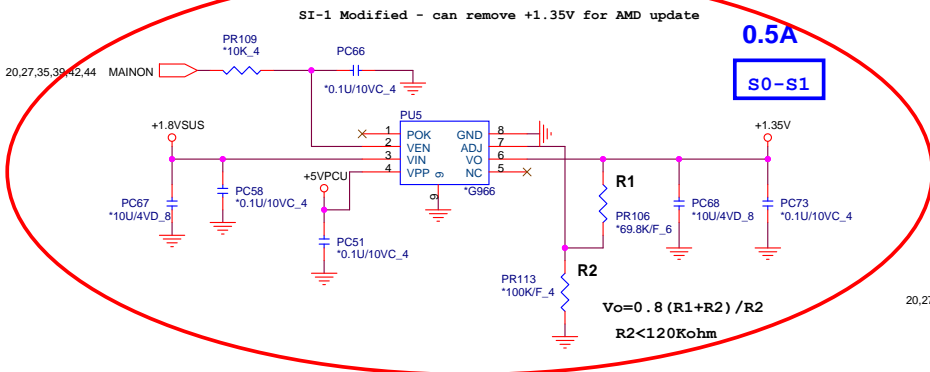
+VGA_CORE
9.4A
S0~S1

+1.5V
2.0A
S0~S1

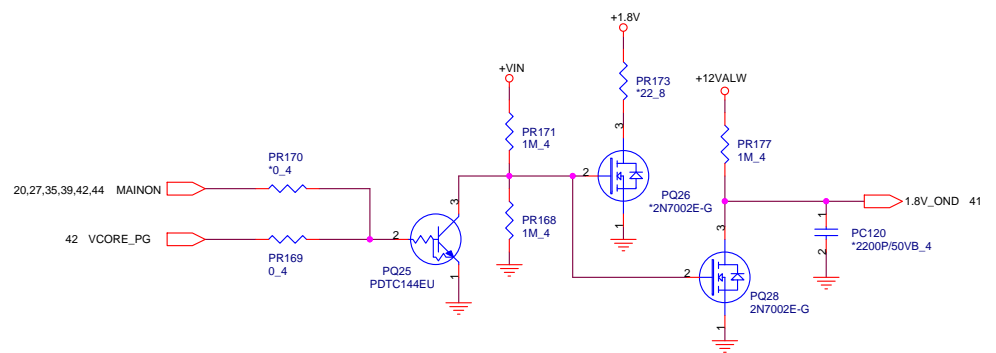
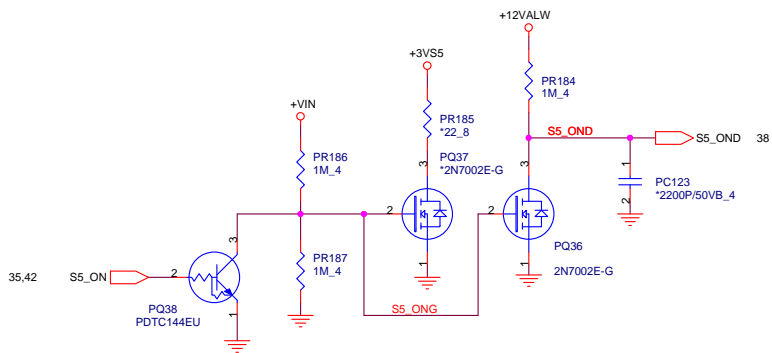
+1.2V_S5
0.5A
S0~S5

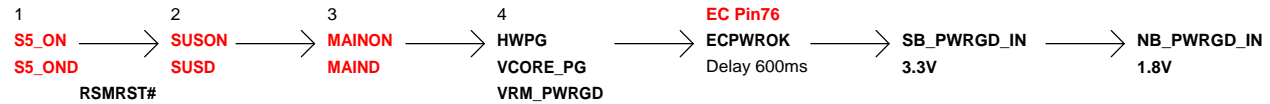
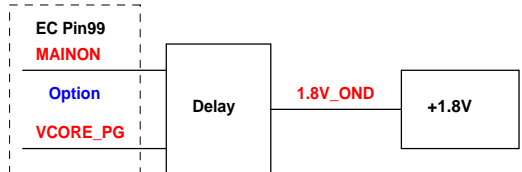
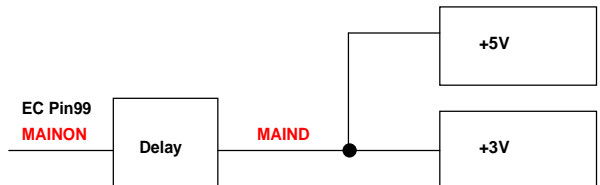
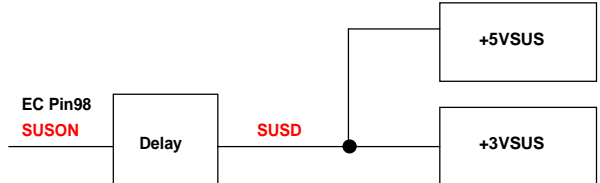
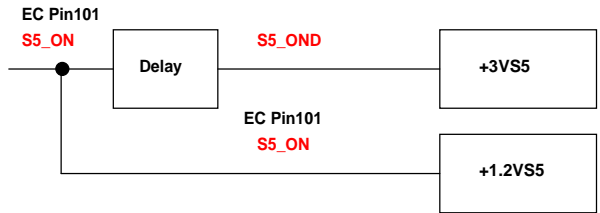
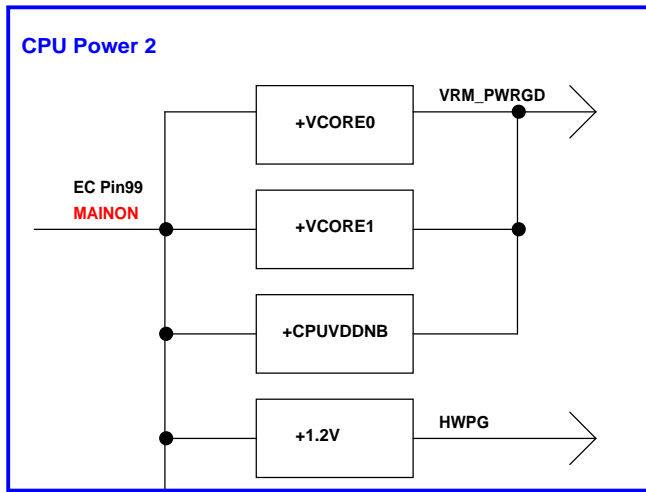
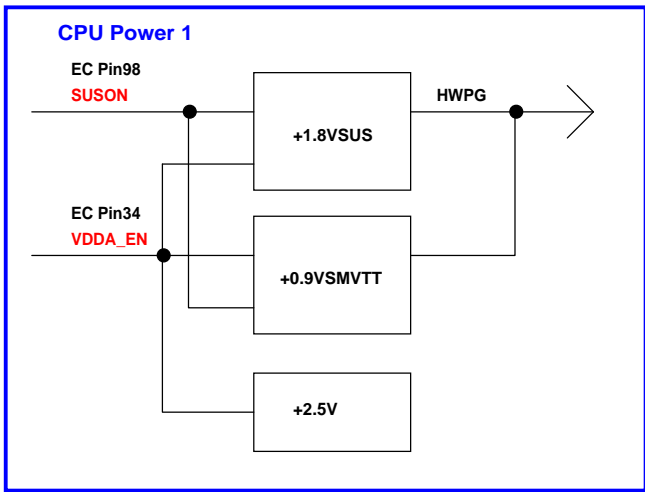


SI-1 Modified -ECAP6_3x6_1-7_2-QT8



For Discrete Only





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