

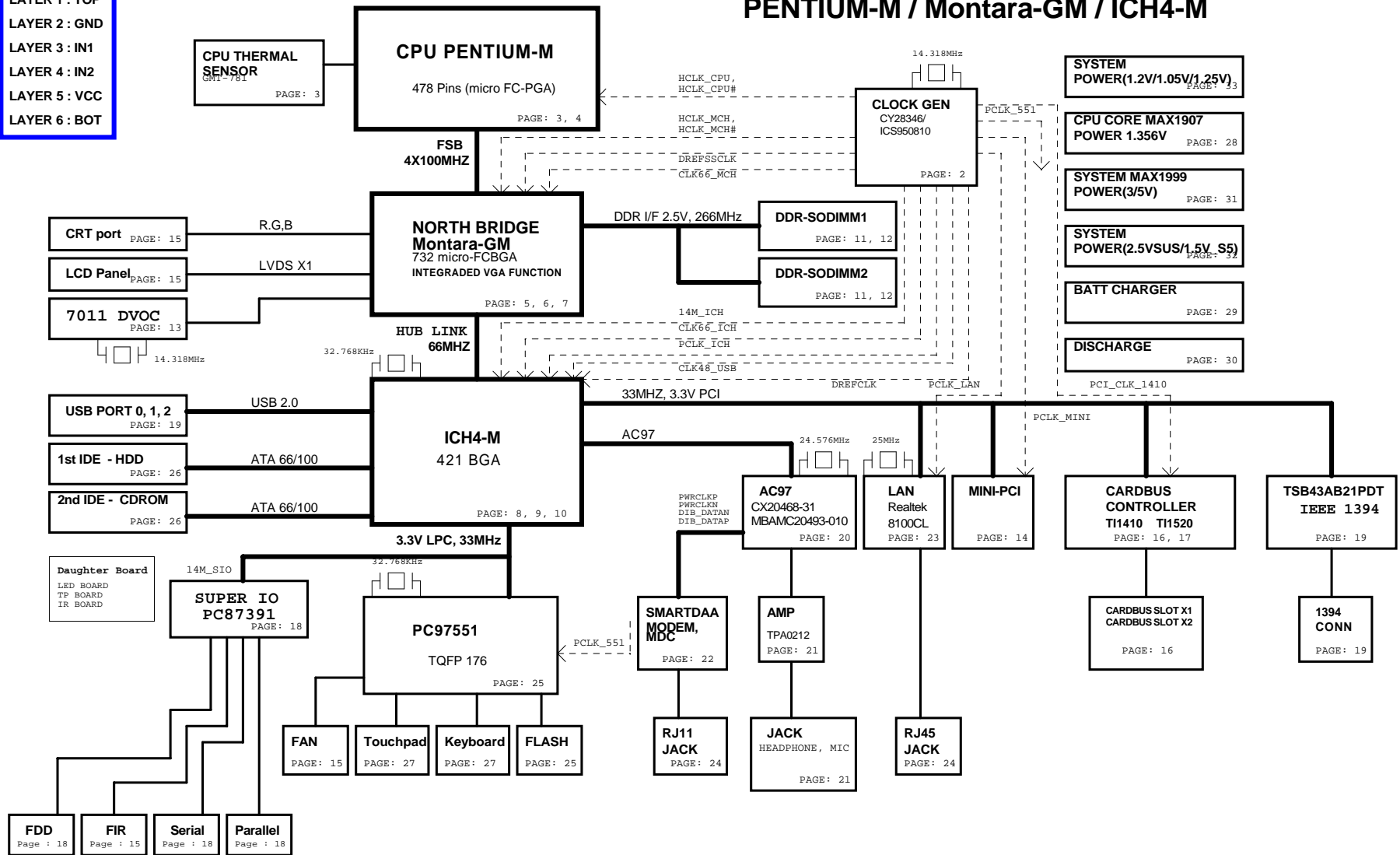
# KT2 BLOCK DIAGRAM (KT2 FF)

## PENTIUM-M / Montara-GM / ICH4-M

### PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

31KT2MB0026



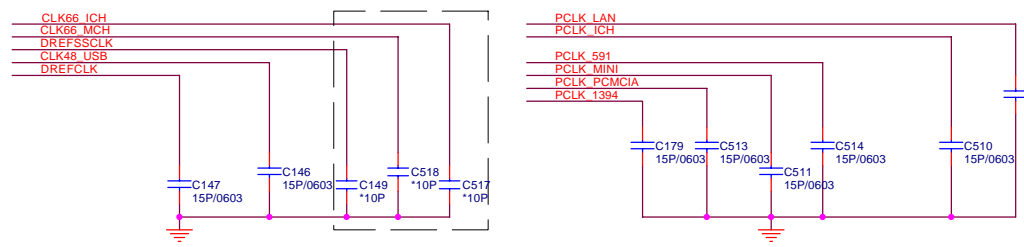
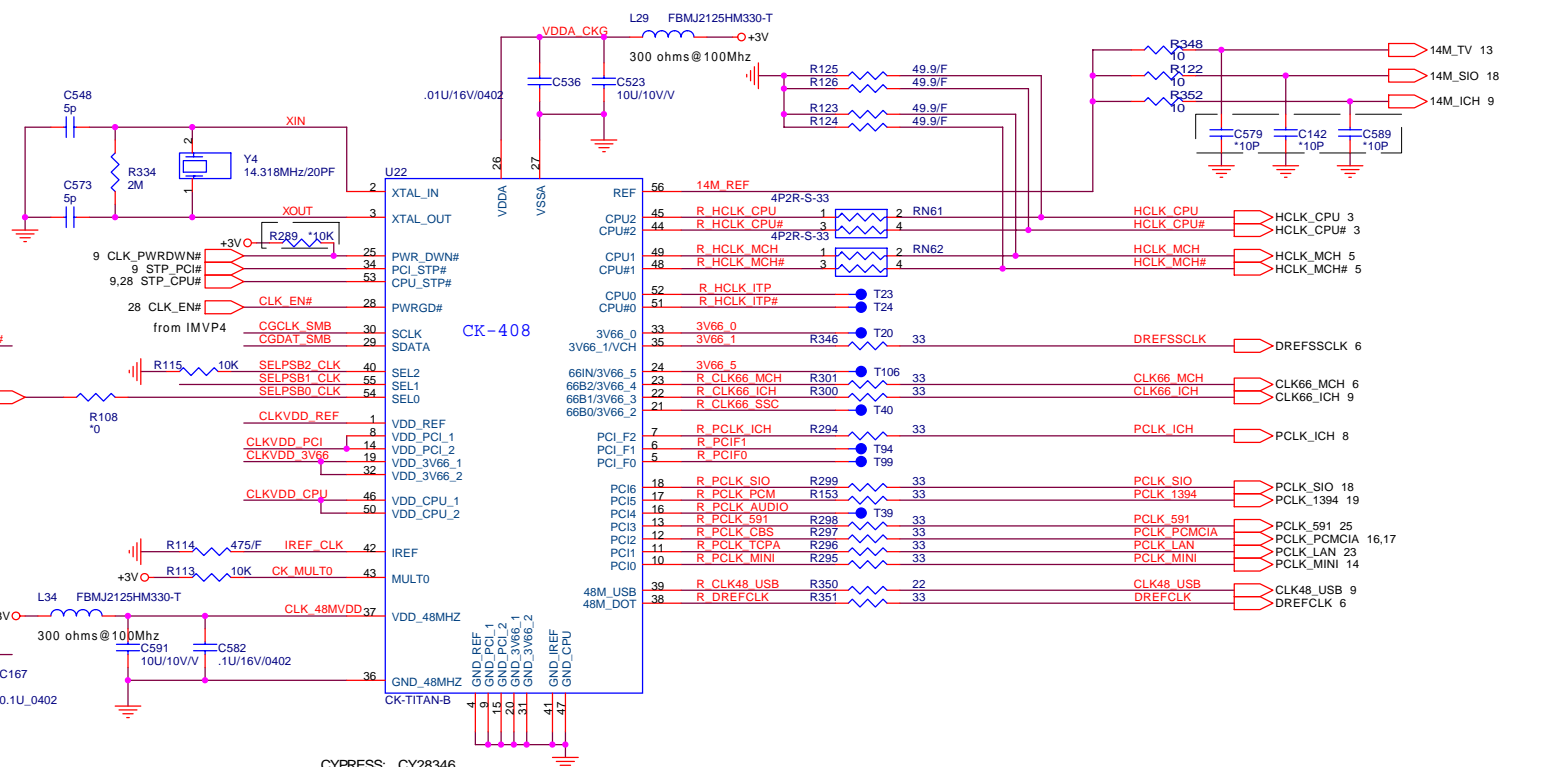
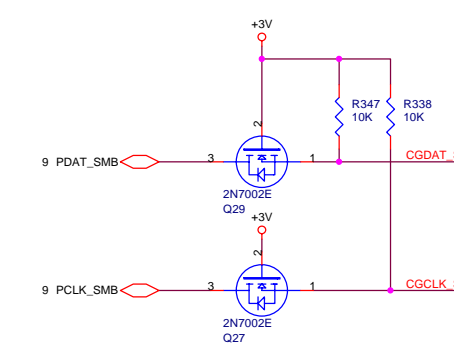
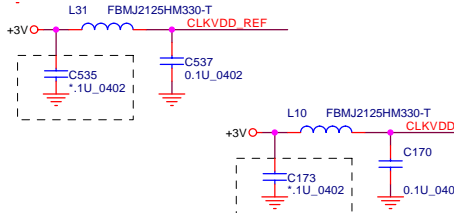
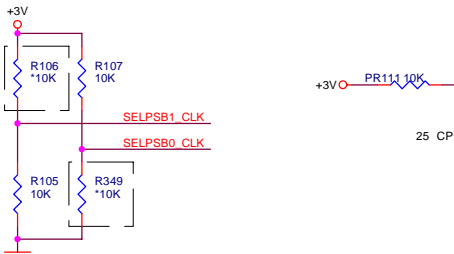
REQ0#, GNT0# : PCMCIA  
 REQ1#, GNT1# : MINIPCI  
 REQ2#, GNT2# : LAN  
 REQ3#, GNT3# : IEEE1394  
 REQ4#, GNT4# : N/A

INTA# : LAN  
 INTB# : CARDBUS 1520  
 INTC# : MINIPCI  
 INTD# : MINIPCI  
 INTE# : CARDBUS  
 INTF# : IEEE1394  
 INTG# : NC  
 INTH# : Internal USB


AD16 : RTL8100CL  
 AD17 : PCI1520  
 AD21 : PCI1410  
 AD22 : MINIPCI  
 AD23 : IEEE1394

# CLK GEN

S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input

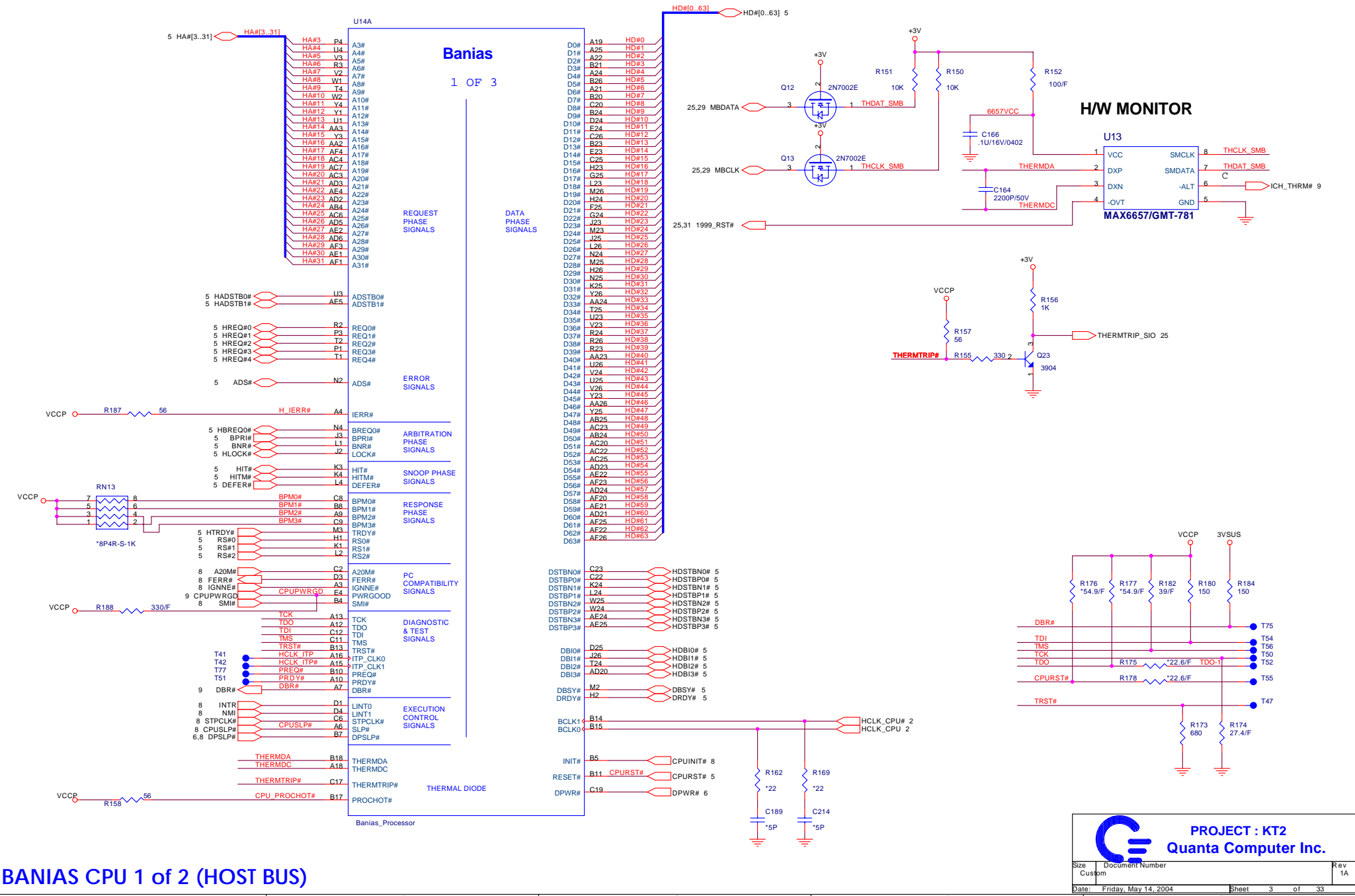


internal pull-up pin 5, FS_IN1	internal pull-down pin 4, FS_IN0MHz	SPREAD %
0	0	14M in 48M out
0	1	14M in 66M out
1	0	48M in/out, 66M in/out
1	1	48M in/out, 66M in/out



**PROJECT : KT2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A
Date:	Friday, May 14, 2004	Sheet 2 of 33



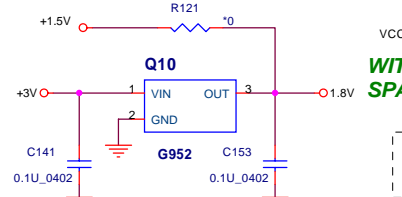
BANIAS CPU 1 of 2 (HOST BUS)

**PROJECT : KT2**  
**Quanta Computer Inc.**

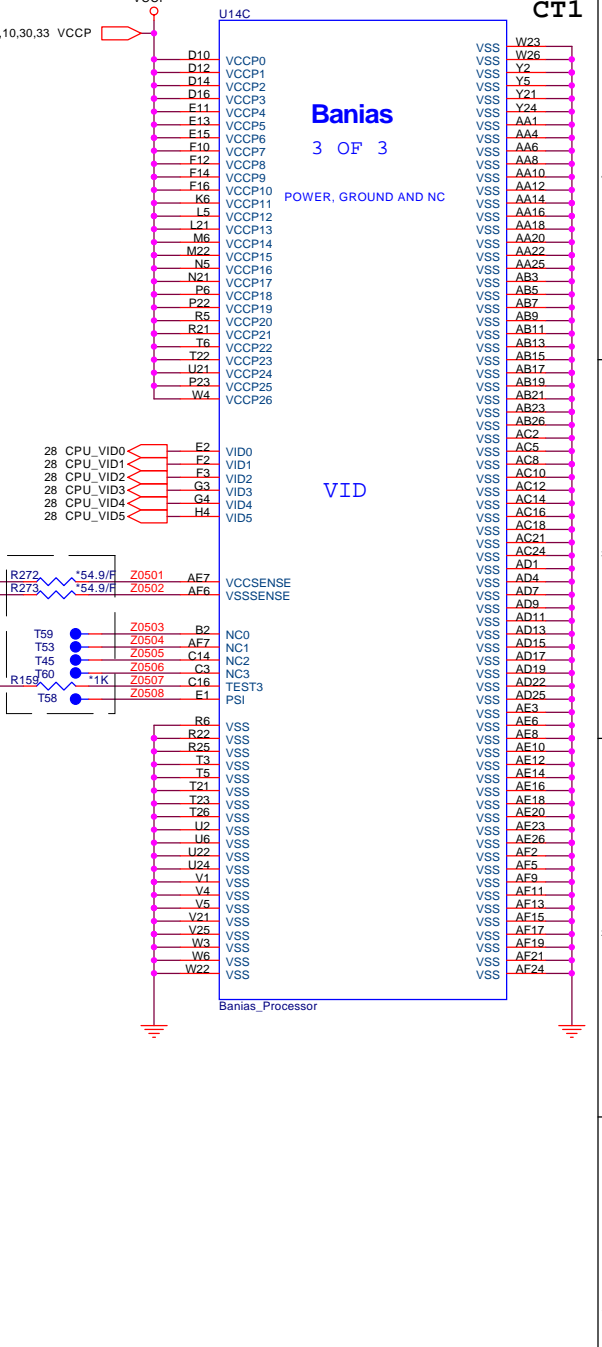
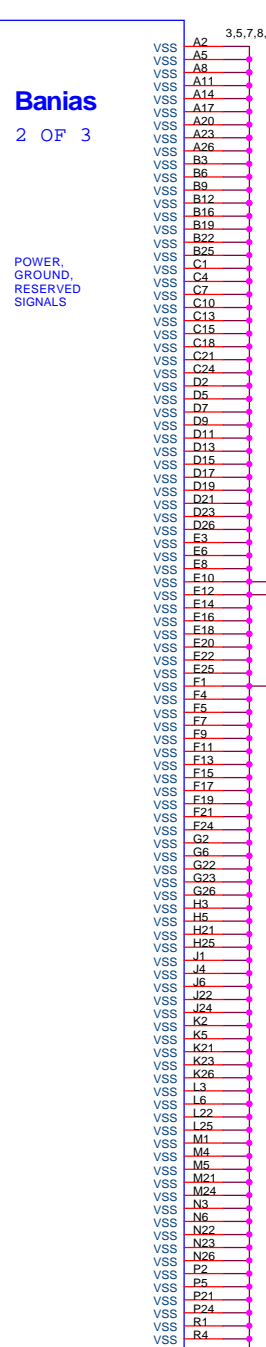
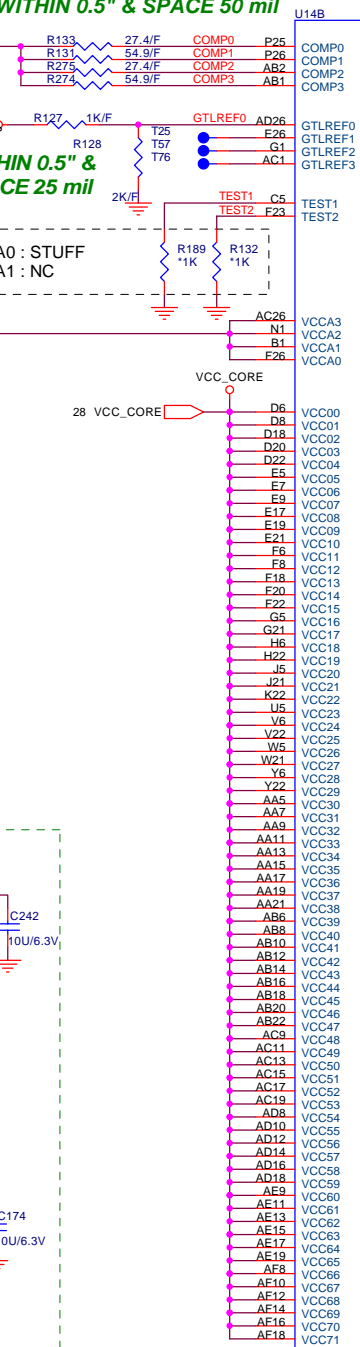
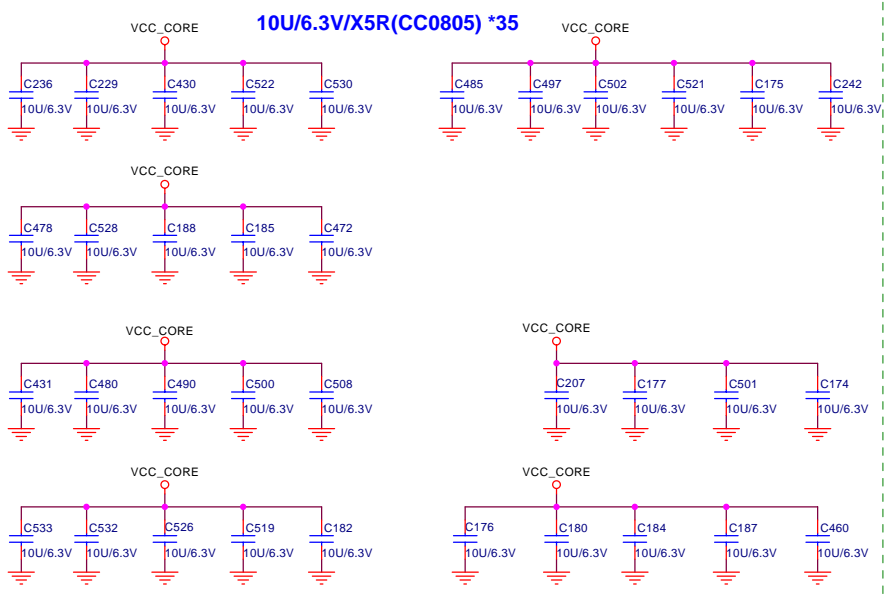
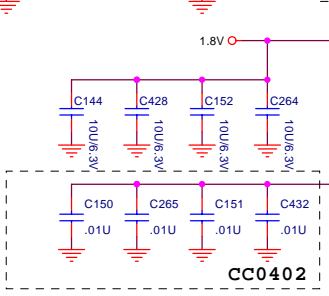
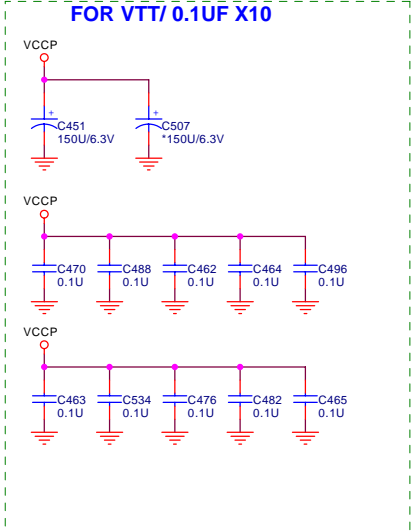
Size	Document Number	Rev
Custom		1A
Date:	Friday, May 14, 2004	Sheet 3 of 33

COMP0 & 2=> Trace Z=27.4ohm  
 COMP1 & 3=> Tracer Z=55ohm  
**WITHIN 0.5" & SPACE 50 mil**

CHANGE TO 0805



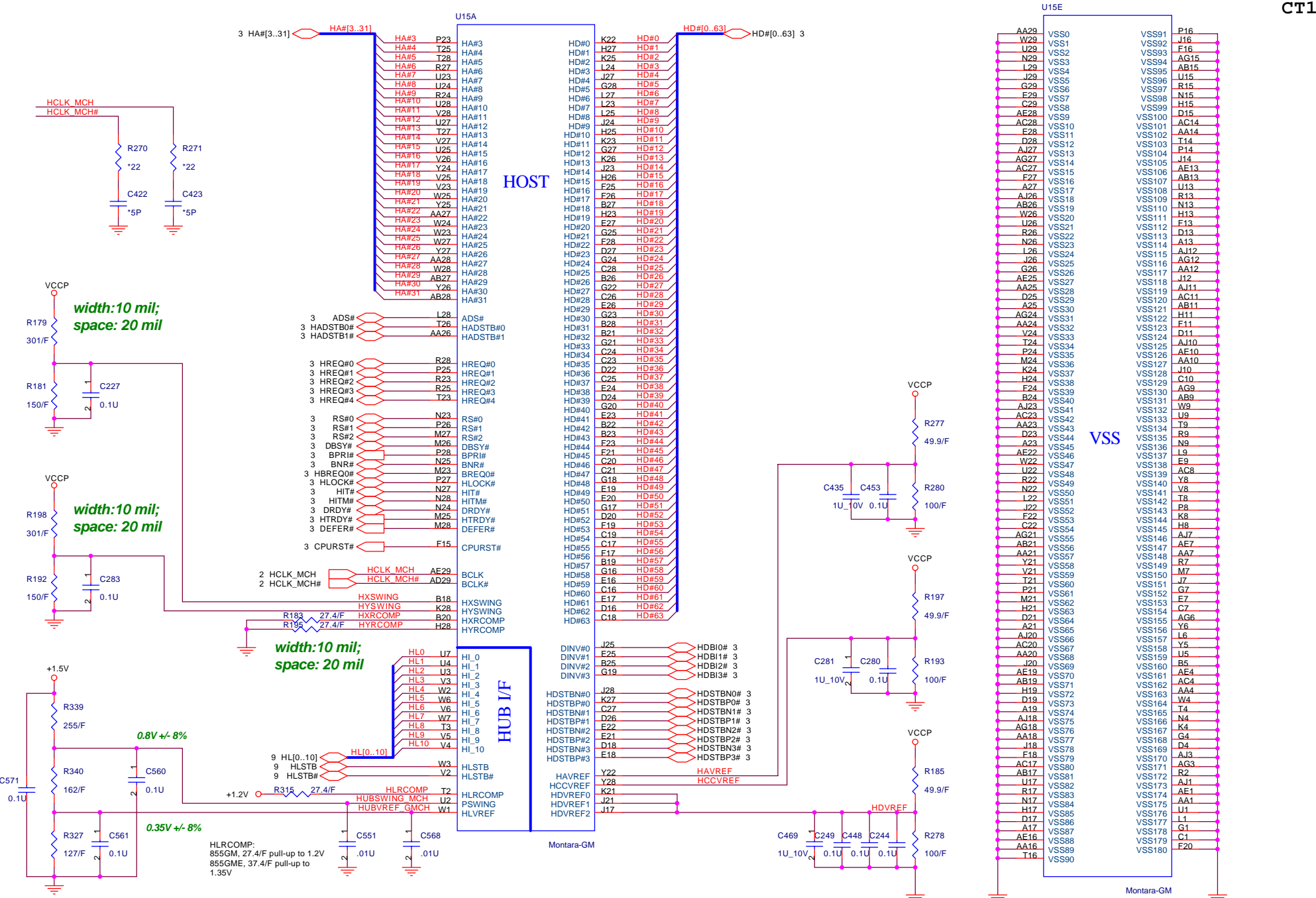
A0 : STUFF  
 A1 : NC



**PROJECT : KT2**  
**Quanta Computer Inc.**

Size B	Document Number	CPU POWER	Rev 1A
Date: Friday, May 14, 2004	Sheet 4 of 33		

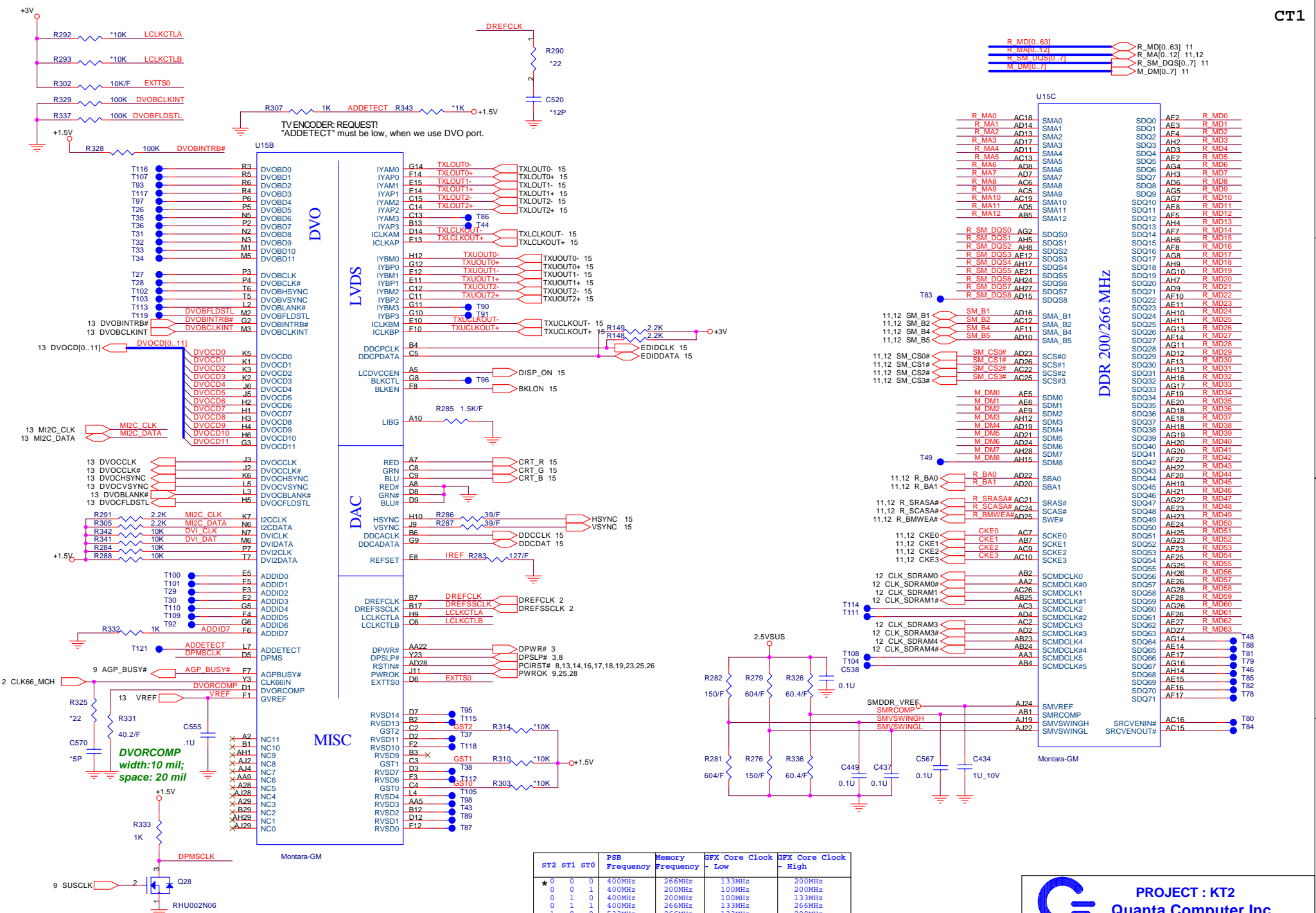
**BANIAS CPU 2 of 2 (PWR)**



MONTARA-GME/ 855GM+ 1of 3 (HOST & GND)

**PROJECT : KT2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	MontaraGM_A	1A
Date:	Friday, May 14, 2004	Sheet 5 of 33



ST2	ST1	ST0	PSB Frequency	Memory Frequency	GFX Core Clock - Low	GFX Core Clock - High
* 0	0	0	400MHz	266MHz	1.33MHz	200MHz
0	0	1	400MHz	200MHz	1.00MHz	200MHz
0	1	0	400MHz	200MHz	1.00MHz	1.33MHz
0	1	1	400MHz	266MHz	1.33MHz	266MHz
1	0	0	533MHz	266MHz	1.33MHz	200MHz
1	0	1	533MHz	266MHz	1.33MHz	266MHz
1	1	0	533MHz	333MHz	1.66MHz	266MHz
1	1	1	400MHz	333MHz	1.66MHz	250MHz

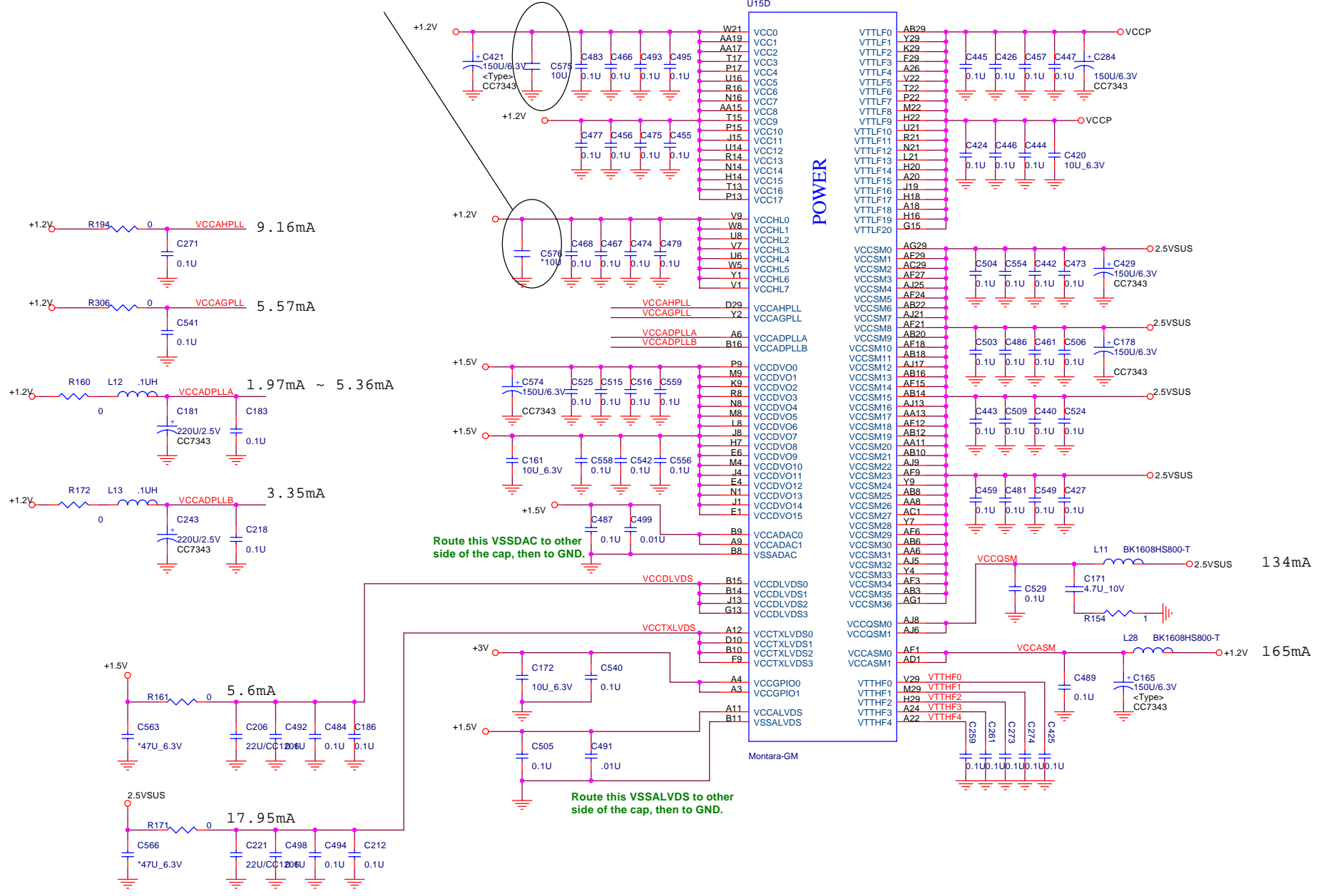
**PROJECT : KT2**  
**Quanta Computer Inc.**

Size: Cuspm Document Number: MontaraGM\_B Rev: 1A  
 Date: Friday, May 14, 2004 Sheet: 6 of 33

**MONTARA-GME/ 855GM+ 2 of 3 (DVO & DDR)**



REV:C from 1206 size change to 0805 size



change +2.5v to 2.5vsus

# MONTARA-GME/ 855GM+ 3 of 3 (POWER & CAP.)

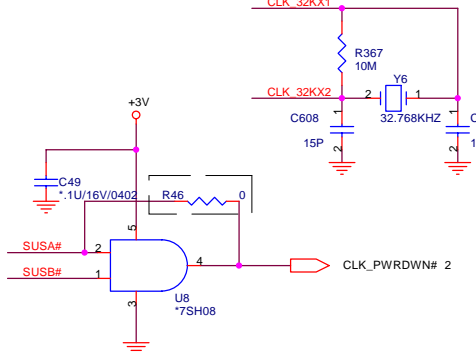
**PROJECT : KT2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Cusbm	MontaraGM_C	1A
Date:	Friday, May 14, 2004	Sheet 7 of 33

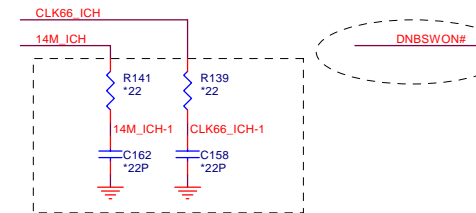




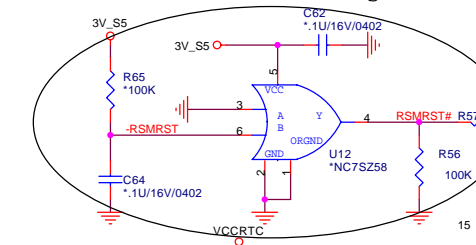
# ICH4-M



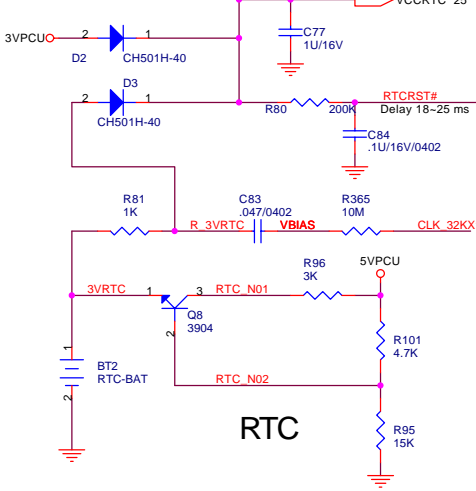
USB0~1: MB USB  
 USB2: DAUGHTER/B USB  
 USB4: CABLE DOCK  
 USB5: BLUE TIITH/  
 LCD



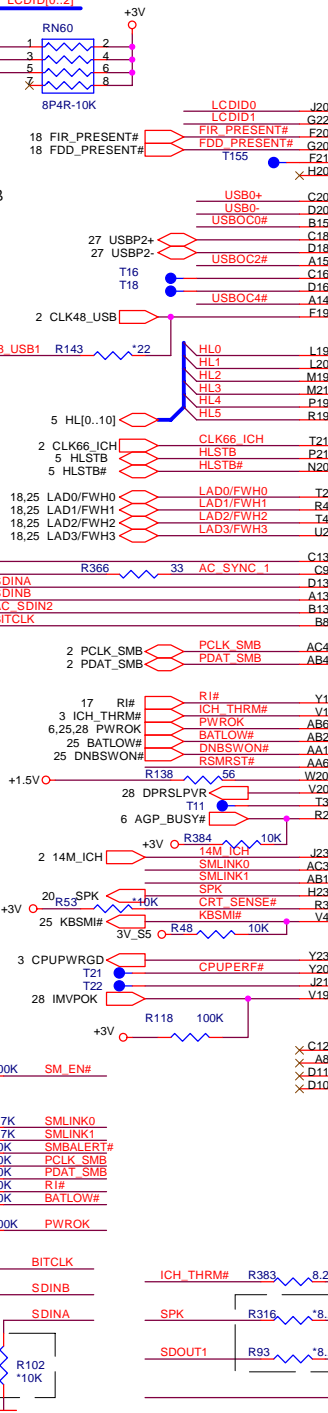
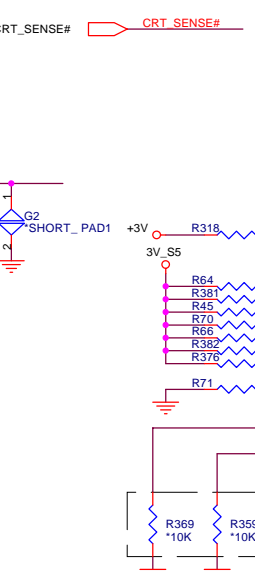
Internal pull-high  
 20K



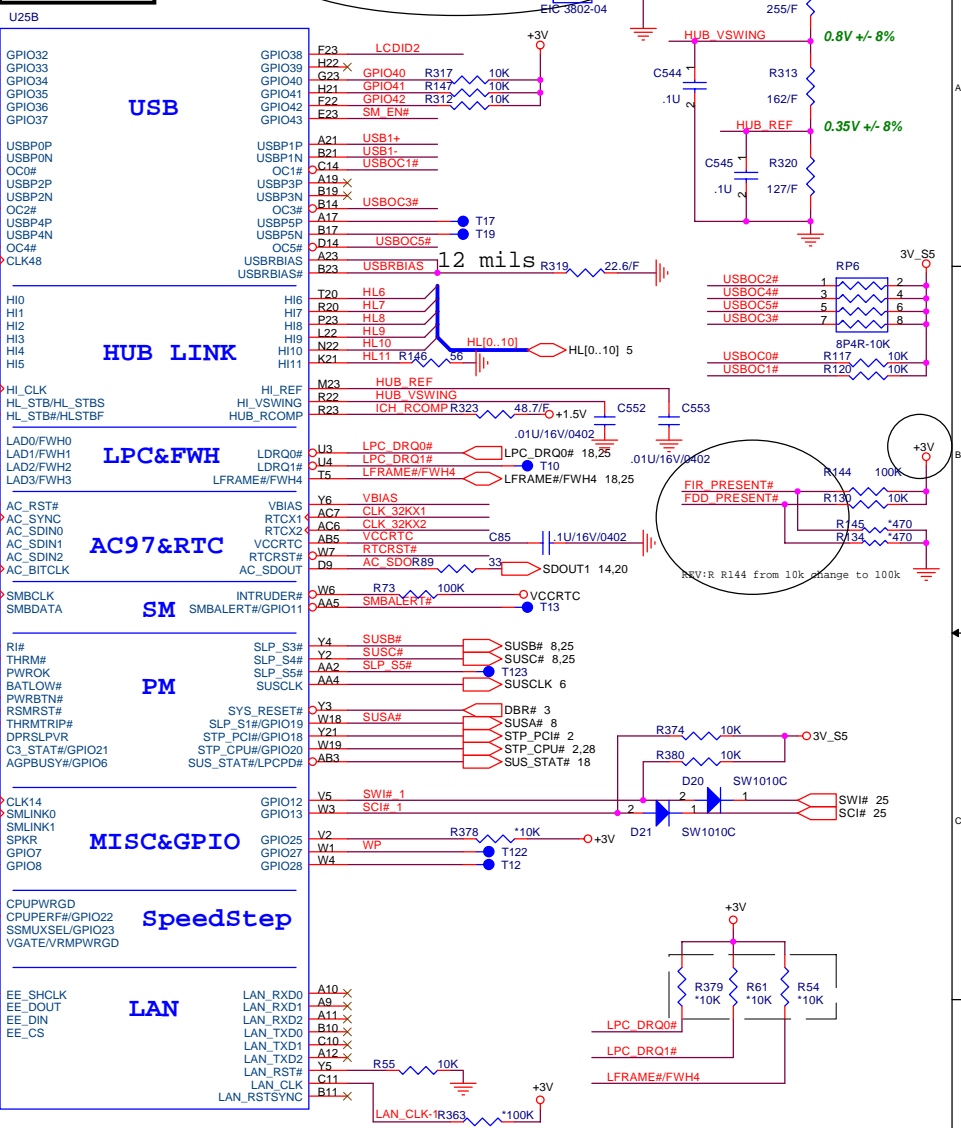
REV:B change to EC control  
 FROM EC



RTC



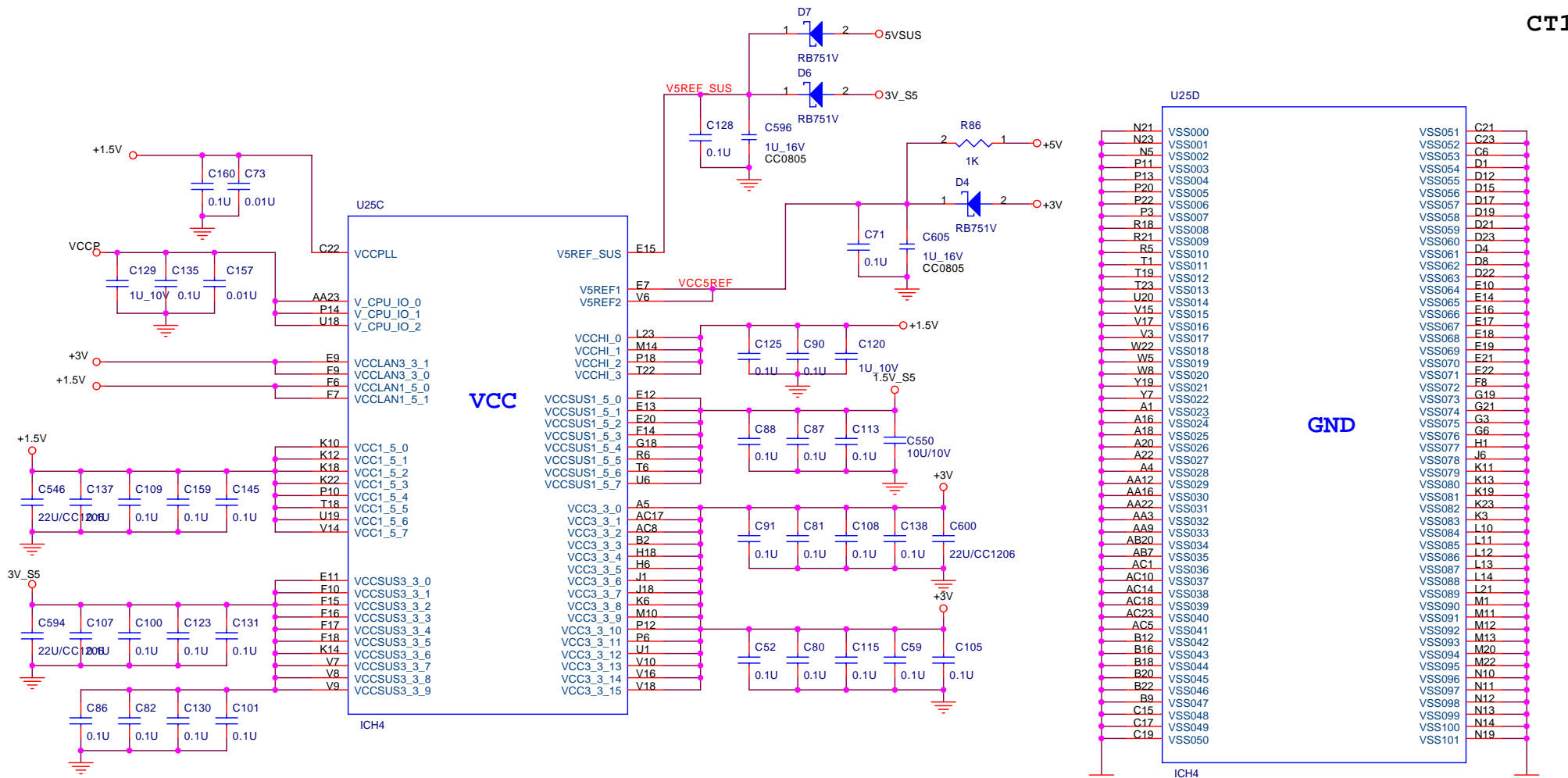
# ICH4-M



ICH4-M 2/3 (USB, HUB LINK, LPC&FWH, AC97, SM, PM, MISC&GPIO, LAN)

**PROJECT : KT2**  
**Quanta Computer Inc.**

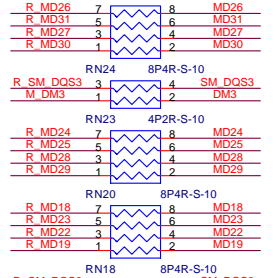
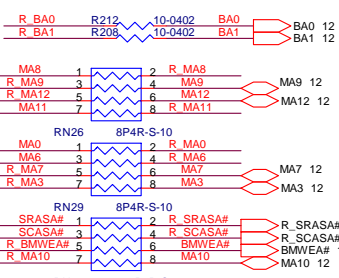
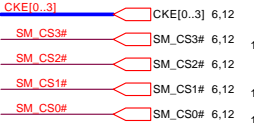
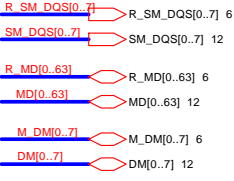
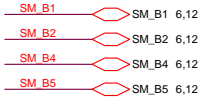
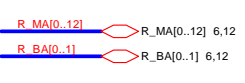
Size	Document Number	Rev
Custom	ICH4-M USB, HUB & LPC INTERFACE	1A
Date:	Friday, May 14, 2004	Sheet 9 of 33



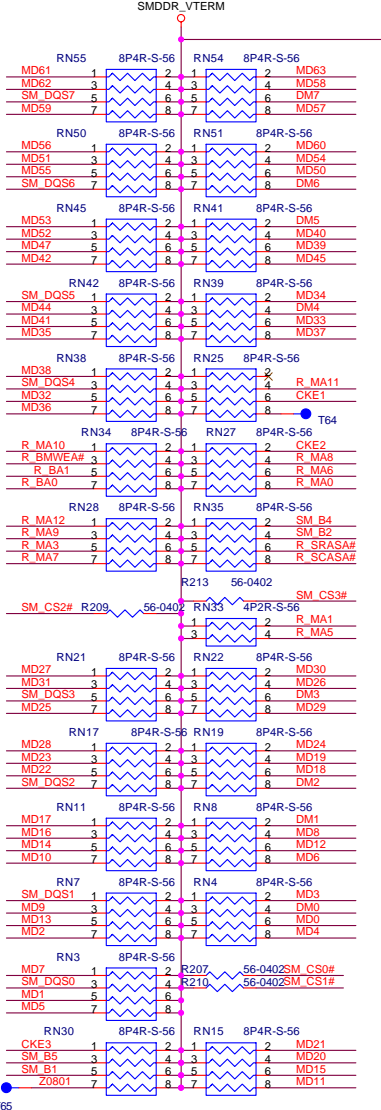
# ICH4-M 3/3 (PWR, GND)



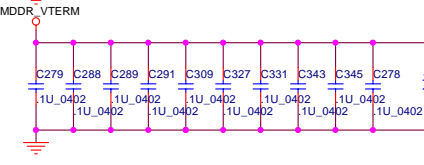
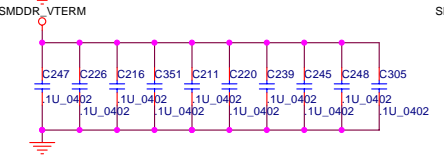
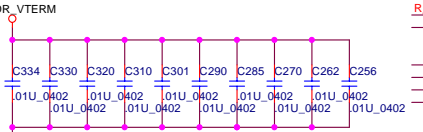
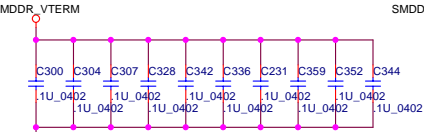
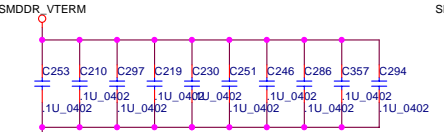
Size	Document Number	Rev
Custom	ICH4-M (POWER&GND)	1A
Date:	Friday, May 14, 2004	Sheet 10 of 33



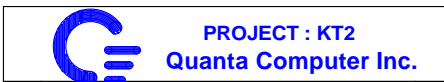
USE 8P4R-0402 package

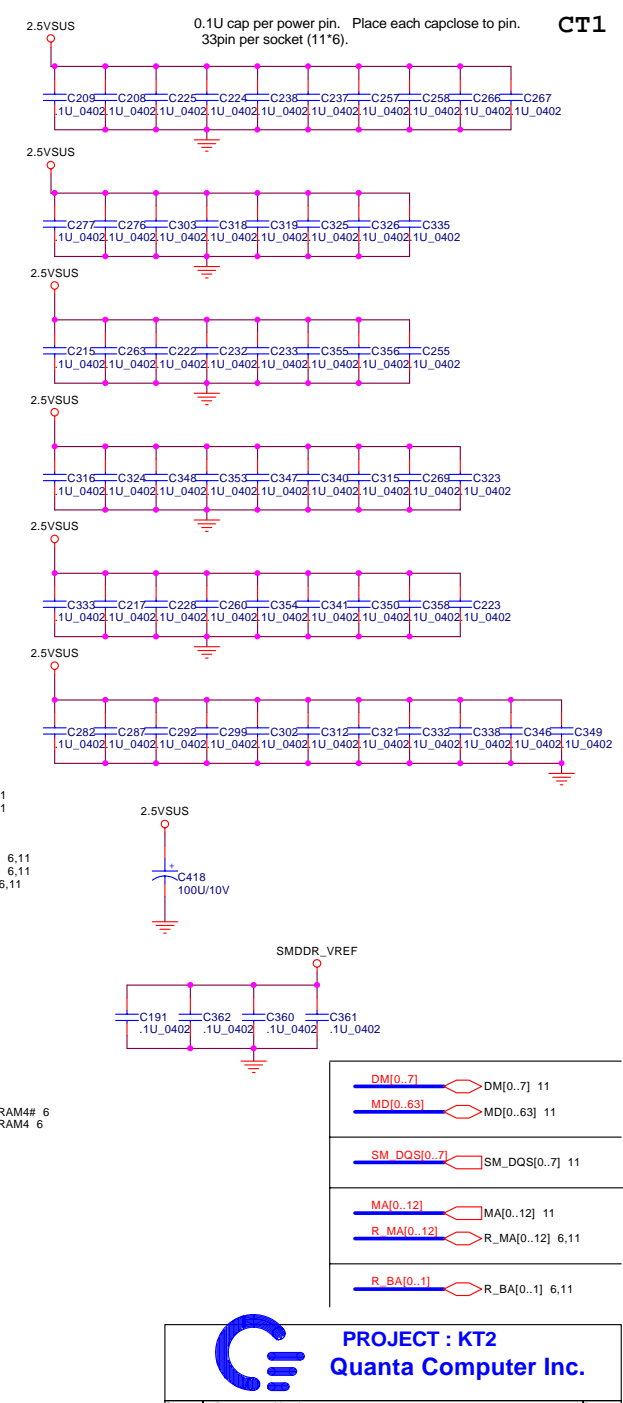
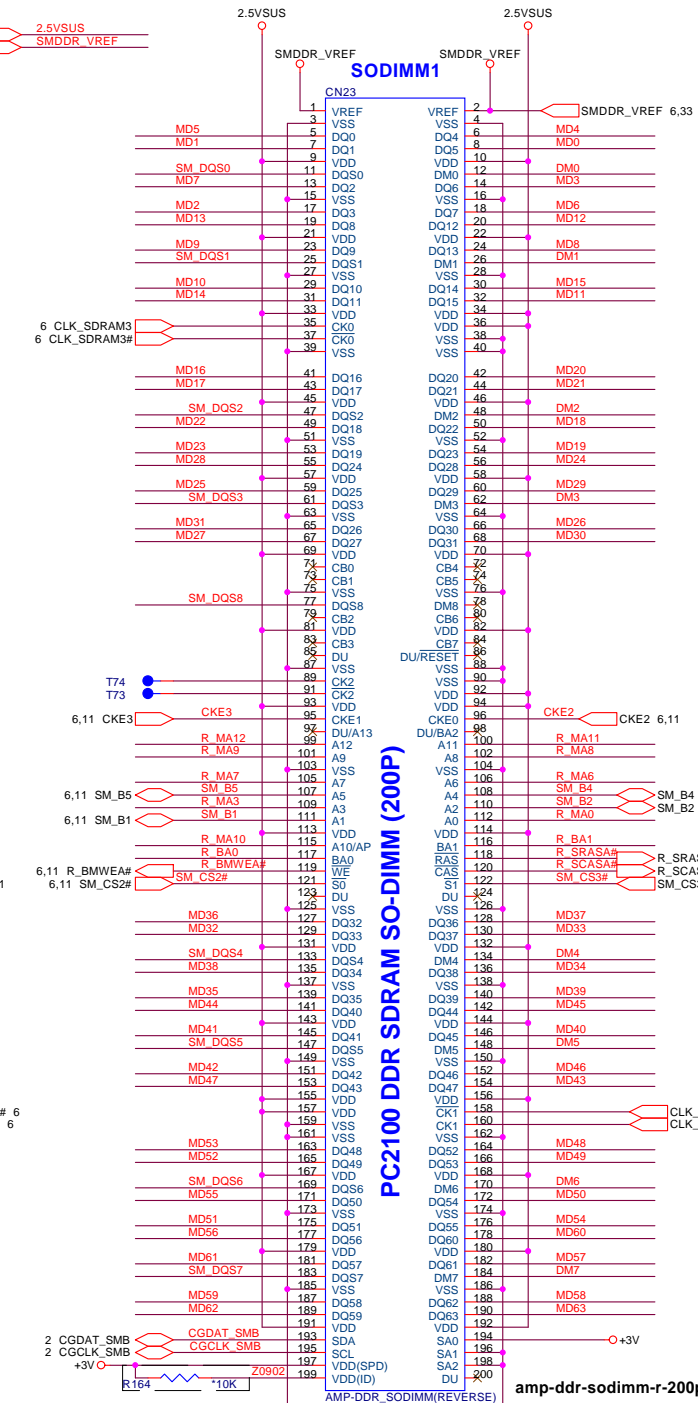
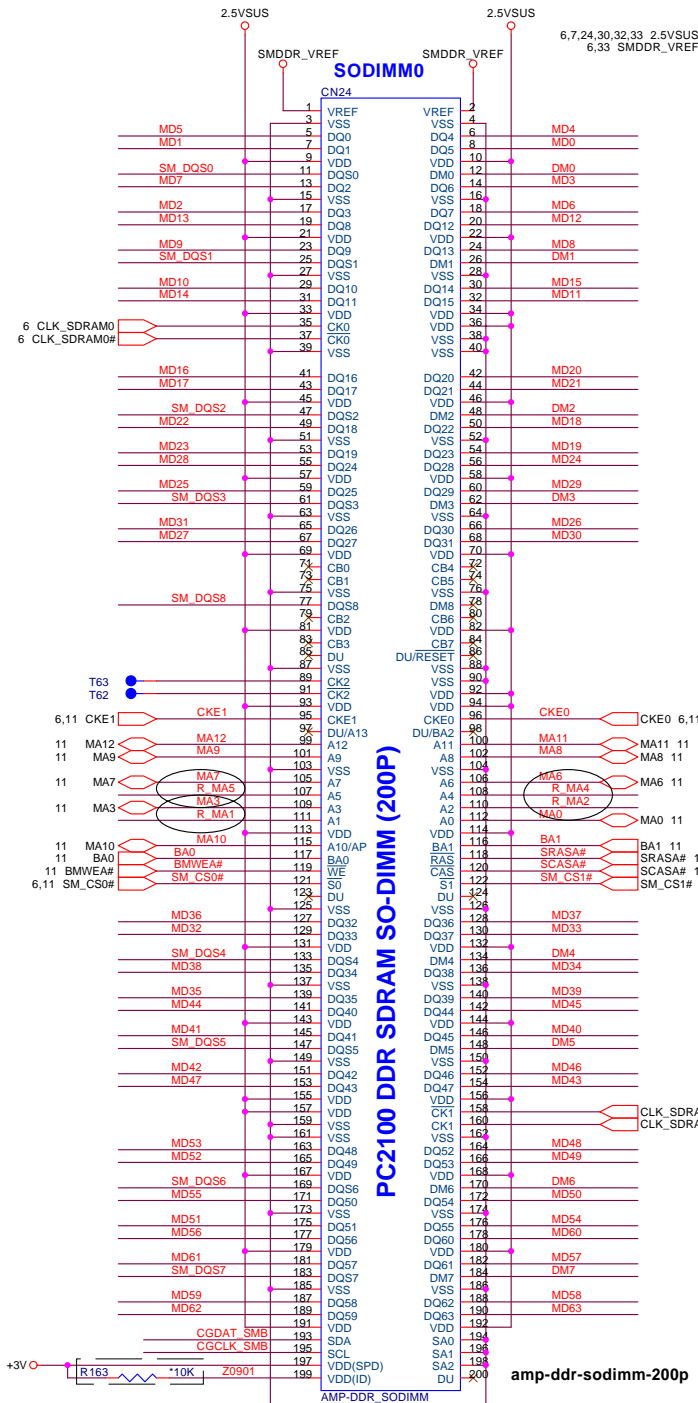


SMDR\_VTERM 30,33



Place Terms close to second DIMM

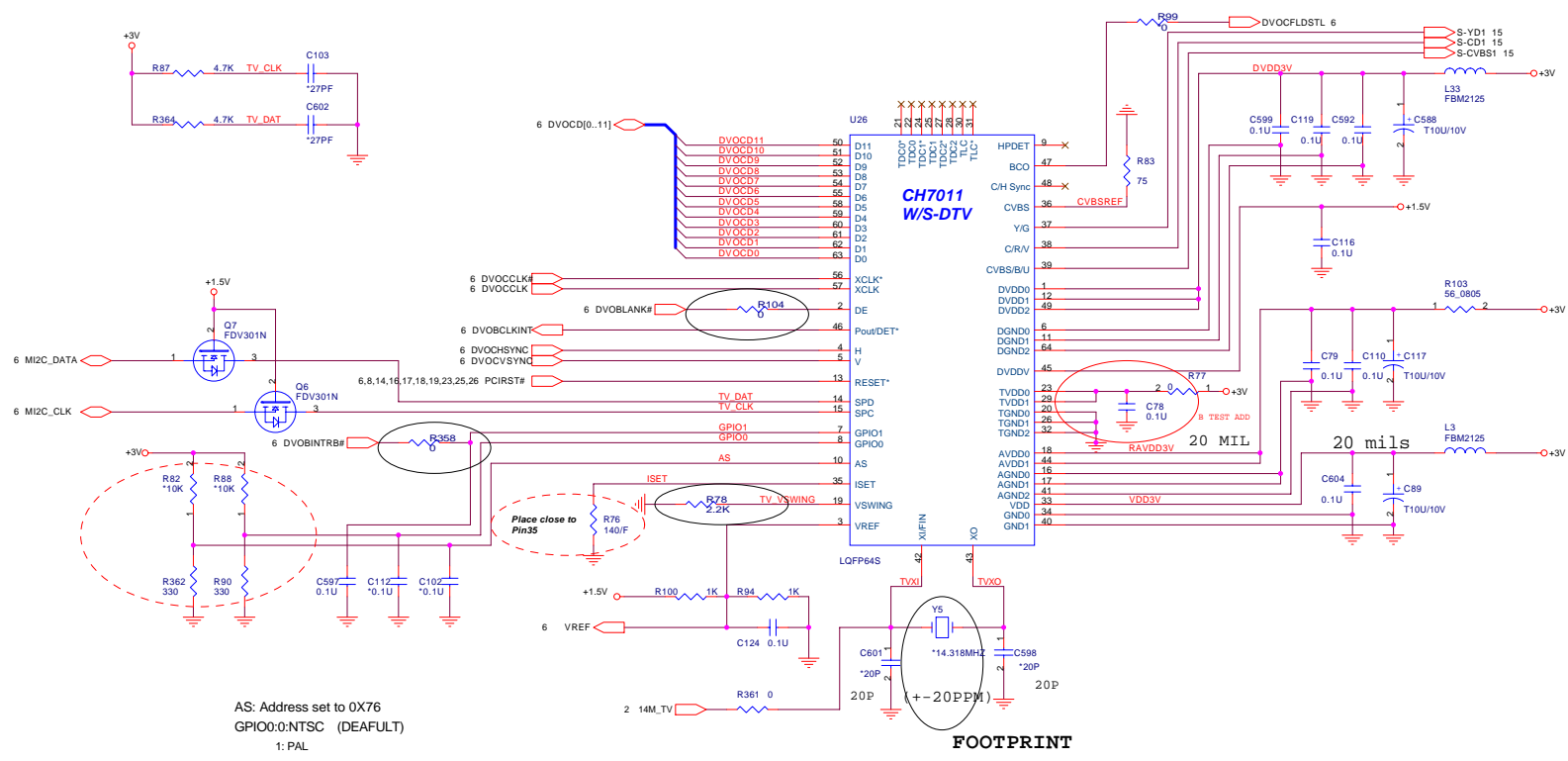




DM[0..7]	DM[0..7]	11
MD[0..63]	MD[0..63]	11
SM_DQS[0..7]	SM_DQS[0..7]	11
MA[0..12]	MA[0..12]	11
R_MA[0..12]	R_MA[0..12]	6,11
R_BA[0..1]	R_BA[0..1]	6,11

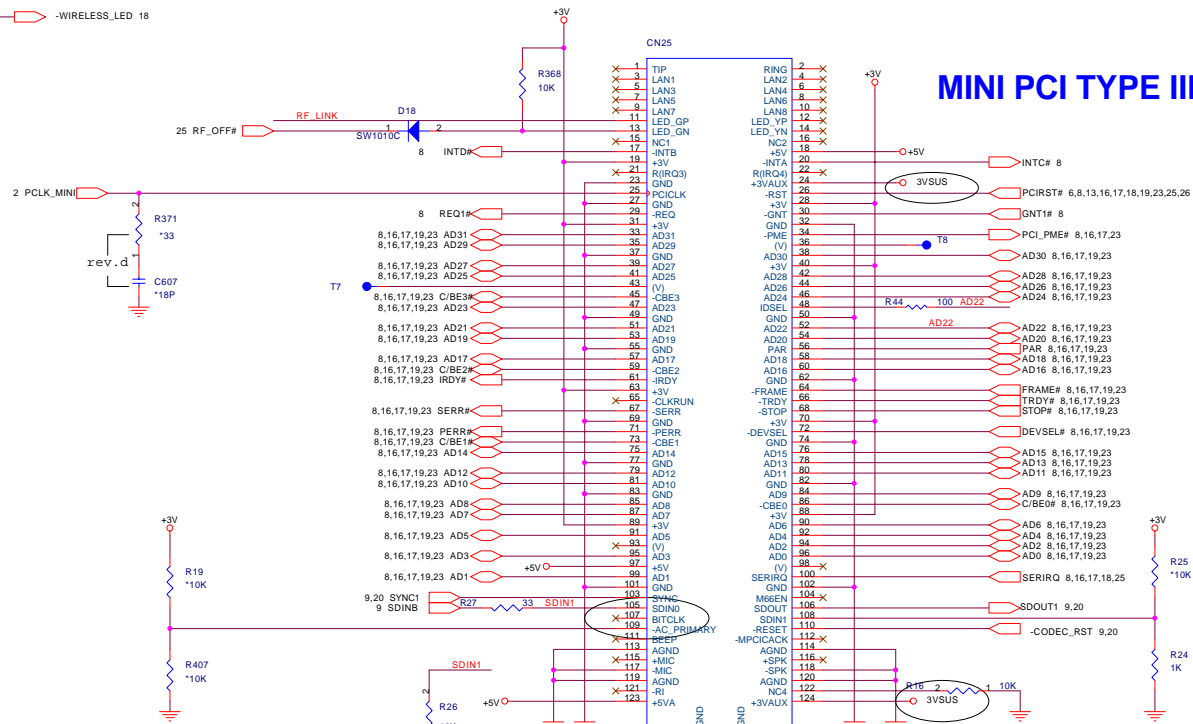
**PROJECT : KT2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
A3	12---DDR SO-DIMM(200P)	1A
Date:	Friday, May 14, 2004	Sheet 12 of 33

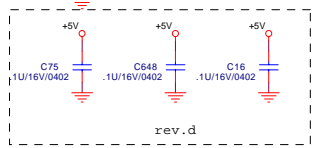


AS: Address set to 0X76  
 GPIO0:0:NTSC (DEAFULT)  
 1: PAL

FOOTPRINT



# MINI PCI TYPE III SLOT





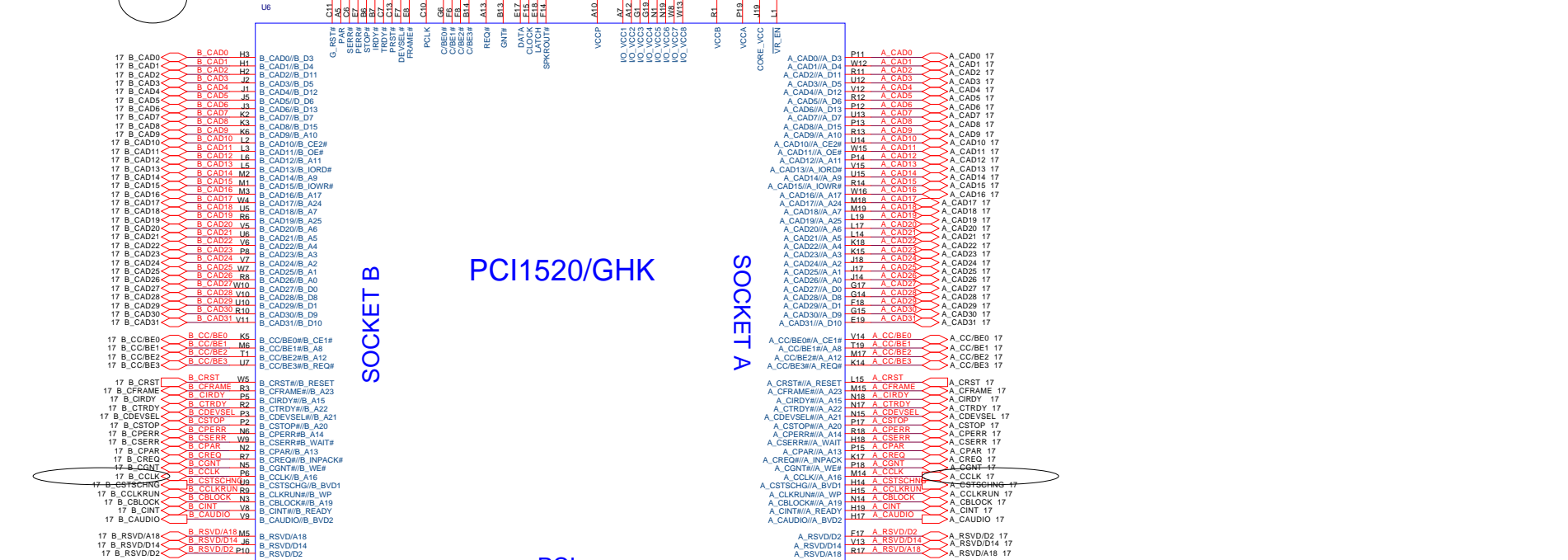
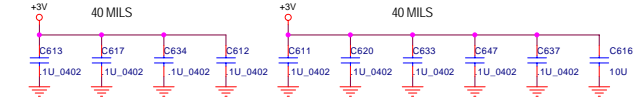


2.17 PCLK\_PCMCIA PCLK\_PCMCIA R397 PCLK\_1520

R9022 FOR 1520 INSTALL  
PLACEMENT CLOSE TO 1410

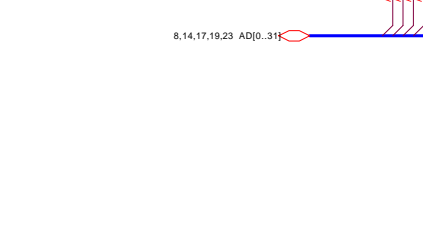
- 8.17 GNT0#
- 8.17 REQ0#
- 8.14,17,19,23 C/BE3#
- 8.14,17,19,23 C/BE2#
- 8.14,17,19,23 C/BE1#
- 8.14,17,19,23 C/BE0#
- 8.14,17,19,23 FRAME#
- 8.14,17,19,23 DEVSEL#
- 6.8,13,14,17,18,19,23,25,26 PCIRST#
- 8.14,17,19,23 TRDY#
- 8.14,17,19,23 RDY#
- 8.14,17,19,23 STOP#
- 8.14,17,19,23 PERR#
- 8.14,17,19,23 SERR#
- 8.14,17,19,23 PAR#
- 6.8,13,14,17,18,19,23,25,26 PCIRST#

- TPSDATA
- TPSCLOCK
- TPSLATCH
- PCMSPK 17,20

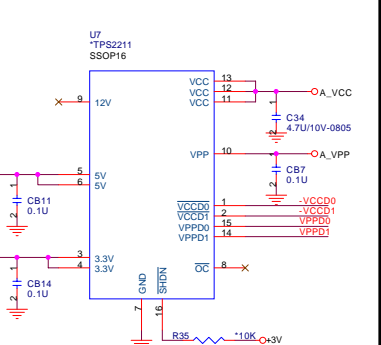
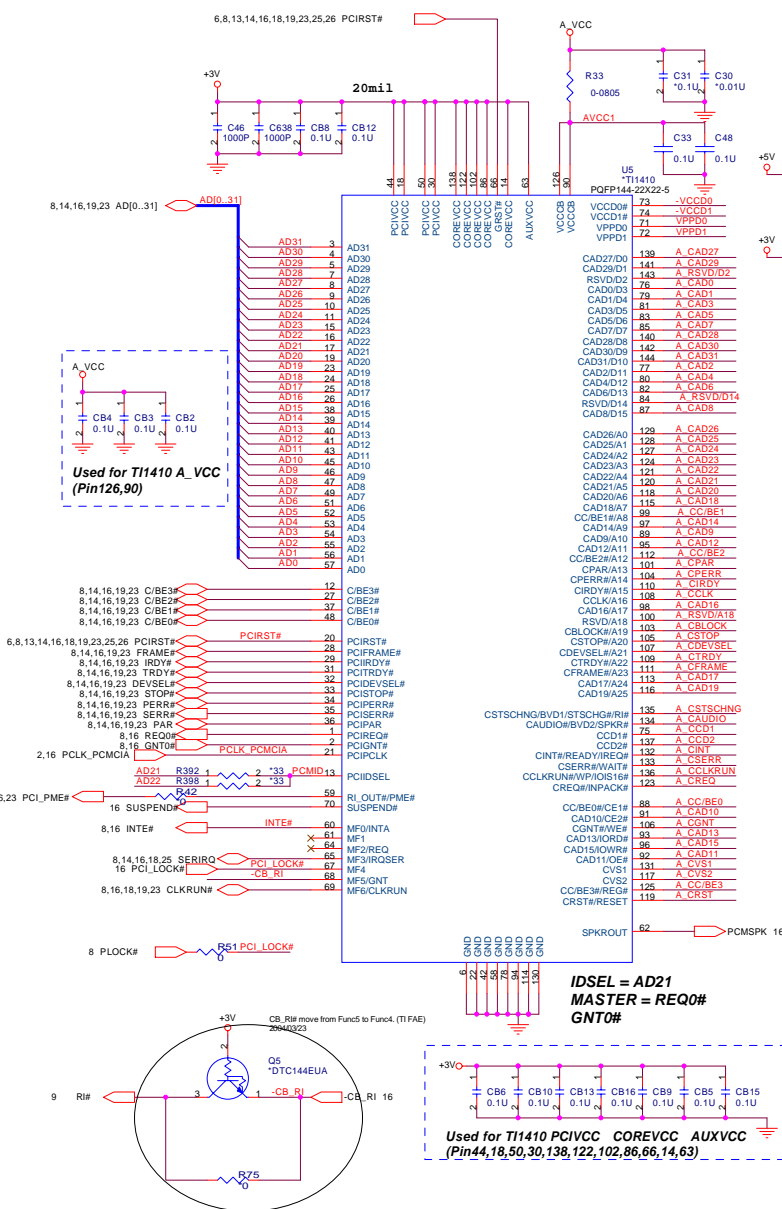


- 17 B\_CAD0# B\_CAD0# H3
- 17 B\_CAD1# B\_CAD1# H1
- 17 B\_CAD2# B\_CAD2# H2
- 17 B\_CAD3# B\_CAD3# H2
- 17 B\_CAD4# B\_CAD4# J1
- 17 B\_CAD5# B\_CAD5# J6
- 17 B\_CAD6# B\_CAD6# K2
- 17 B\_CAD7# B\_CAD7# K2
- 17 B\_CAD8# B\_CAD8# K3
- 17 B\_CAD9# B\_CAD9# L1
- 17 B\_CAD10# B\_CAD10# L2
- 17 B\_CAD11# B\_CAD11# L3
- 17 B\_CAD12# B\_CAD12# L5
- 17 B\_CAD13# B\_CAD13# M2
- 17 B\_CAD14# B\_CAD14# M1
- 17 B\_CAD15# B\_CAD15# M3
- 17 B\_CAD16# B\_CAD16# M4
- 17 B\_CAD17# B\_CAD17# U6
- 17 B\_CAD18# B\_CAD18# V5
- 17 B\_CAD19# B\_CAD19# V6
- 17 B\_CAD20# B\_CAD20# U6
- 17 B\_CAD21# B\_CAD21# V6
- 17 B\_CAD22# B\_CAD22# V6
- 17 B\_CAD23# B\_CAD23# V7
- 17 B\_CAD24# B\_CAD24# W7
- 17 B\_CAD25# B\_CAD25# W7
- 17 B\_CAD26# B\_CAD26# W7
- 17 B\_CAD27# B\_CAD27# W10
- 17 B\_CAD28# B\_CAD28# W10
- 17 B\_CAD29# B\_CAD29# W10
- 17 B\_CAD30# B\_CAD30# R10
- 17 B\_CAD31# B\_CAD31# V11

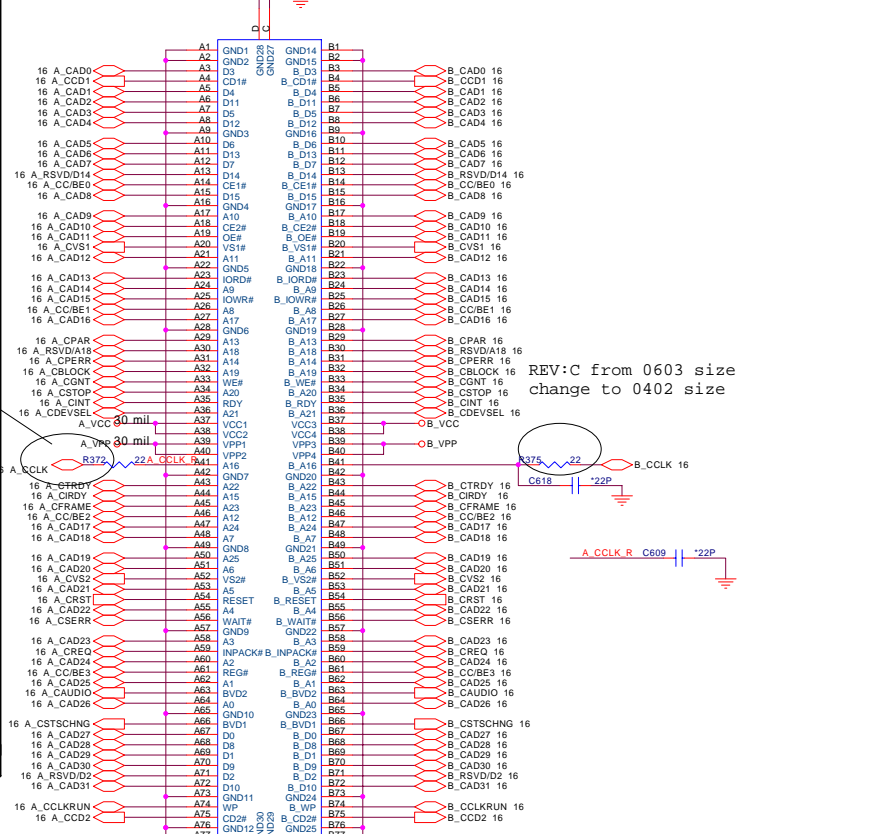
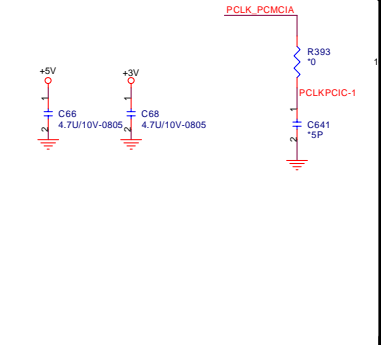
Correct module name: BCVS10, BCVS2#



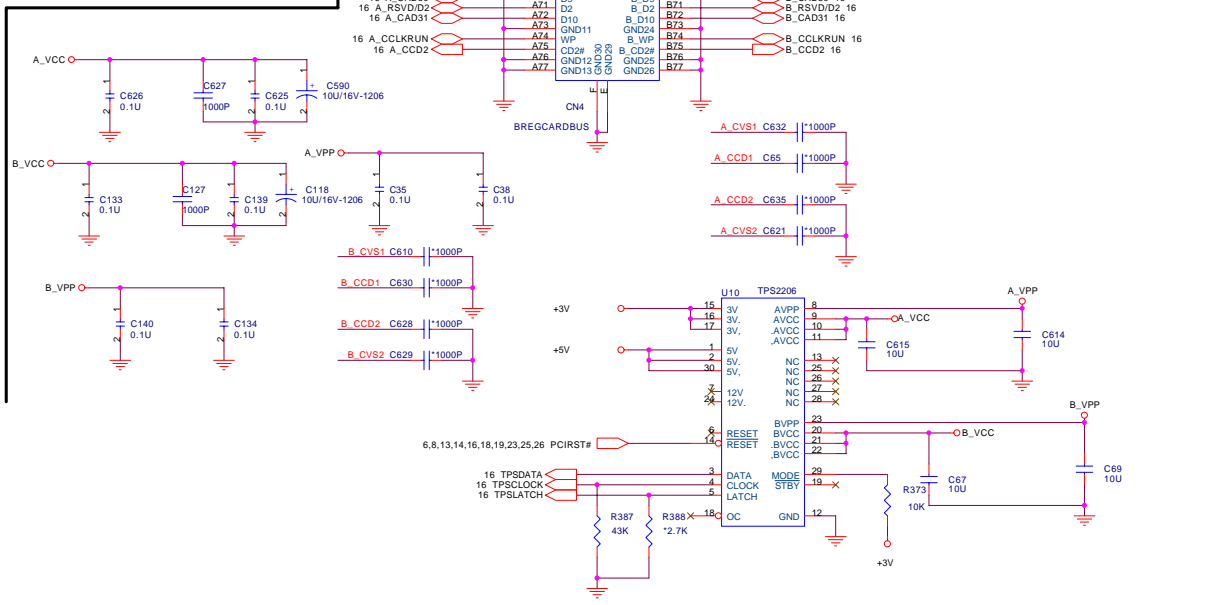
# CARDBUS PCMCIA SOCKET



REV:C from 0603 size change to 0402 size

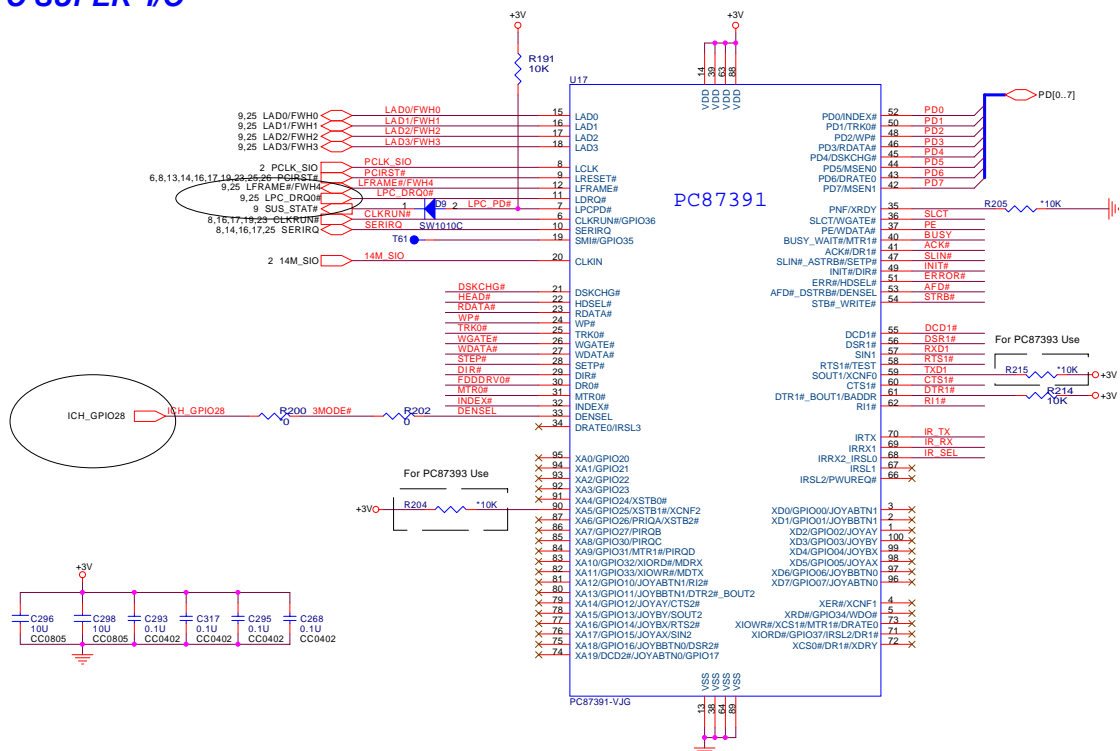


REV:C from 0603 size change to 0402 size

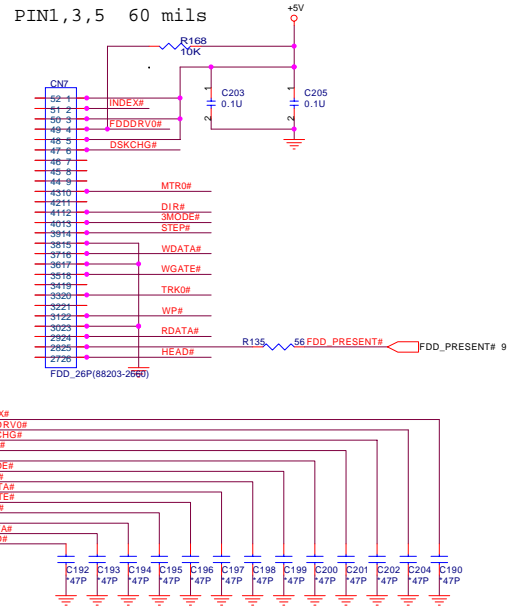


NOT SUPPORT TI1410:  
REMOVE R392, R35, U5, U7

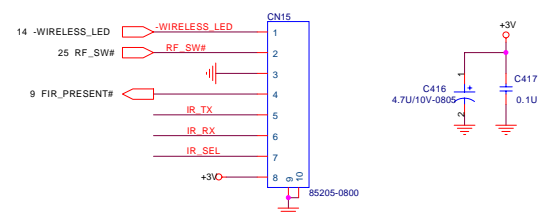
# LPC SUPER I/O



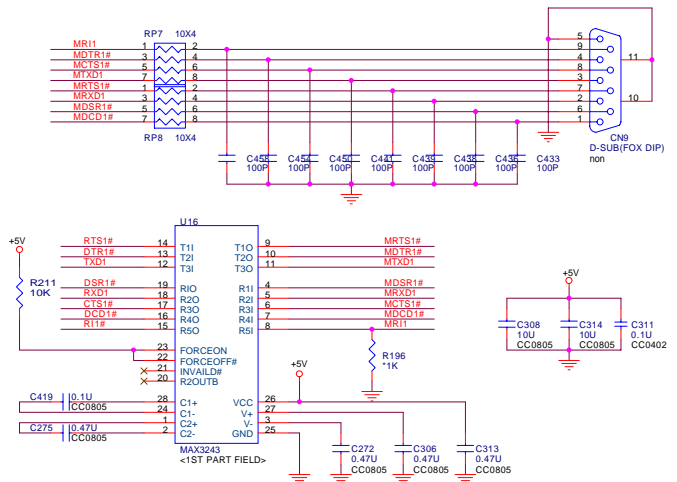
# FDD CONN



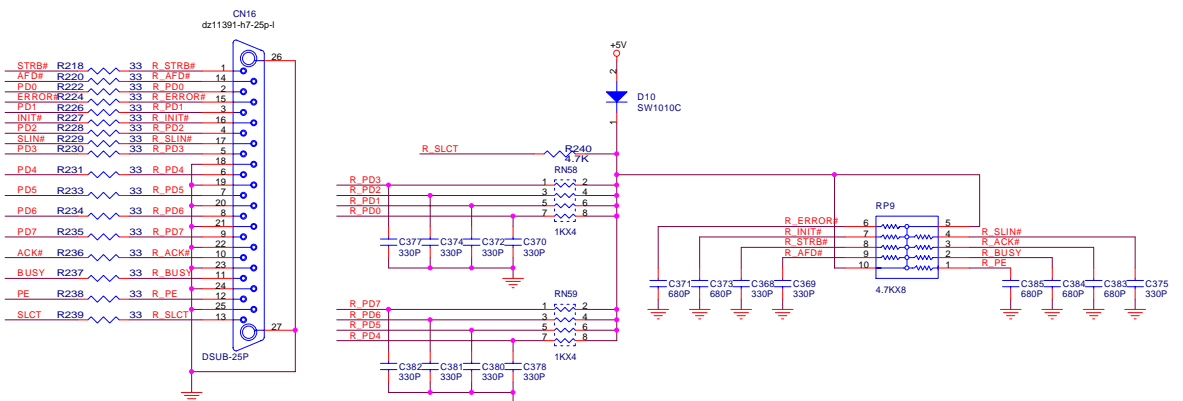
# IR BOARD CONN



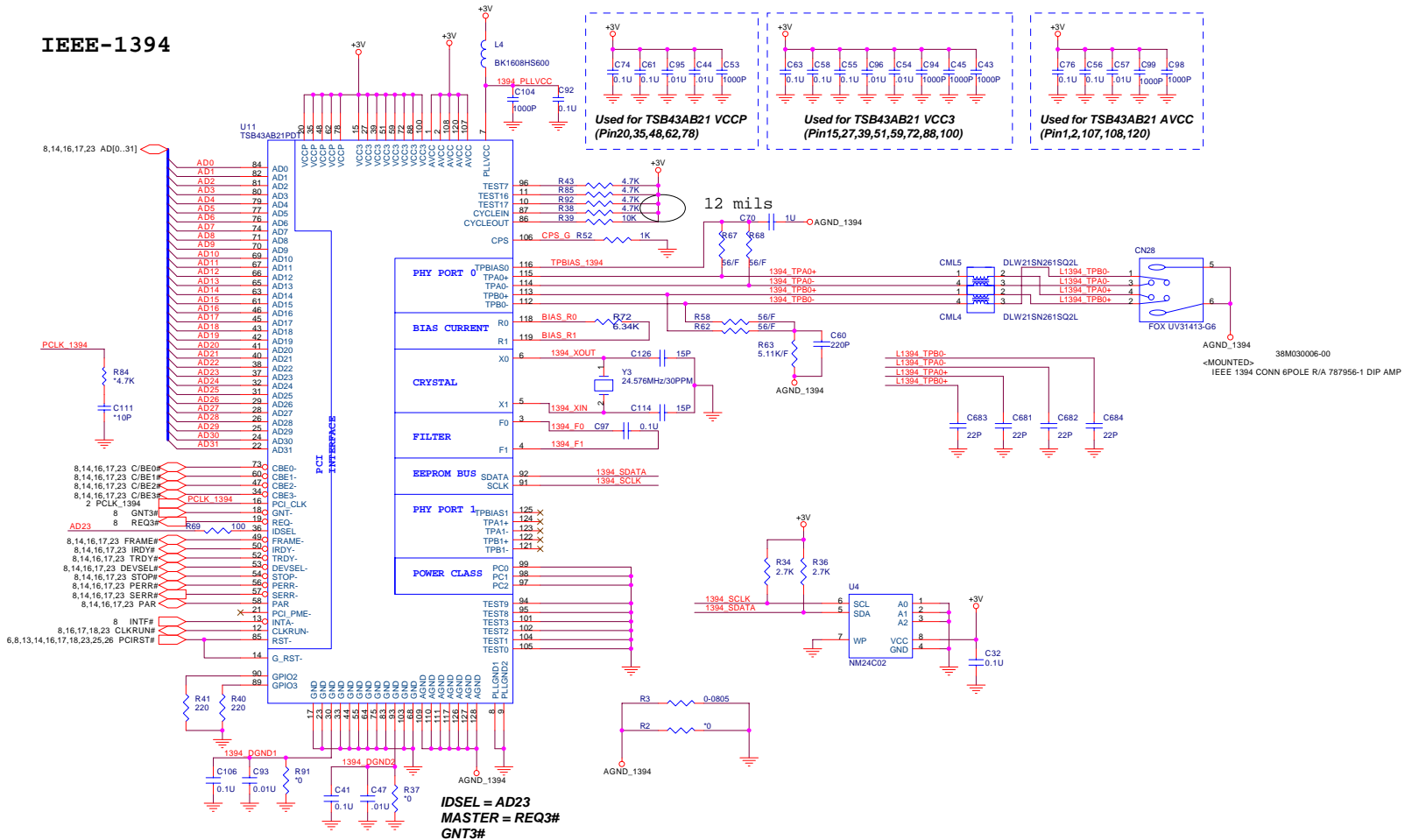
# SERIAL PORT



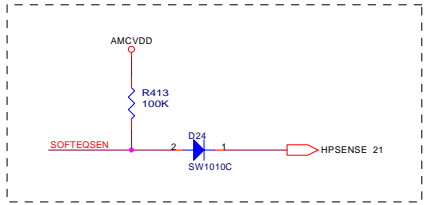
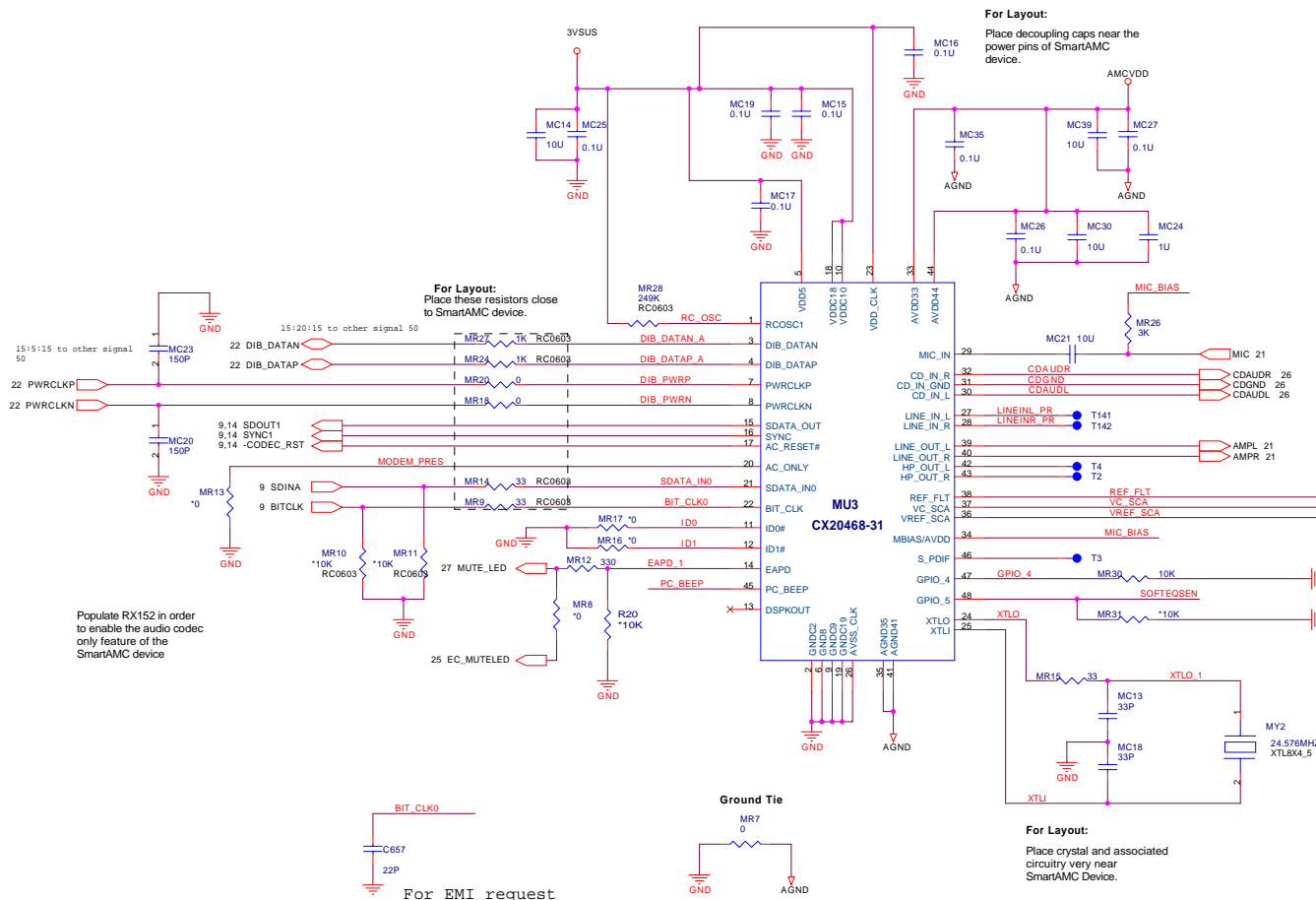
# PARALLEL PORT



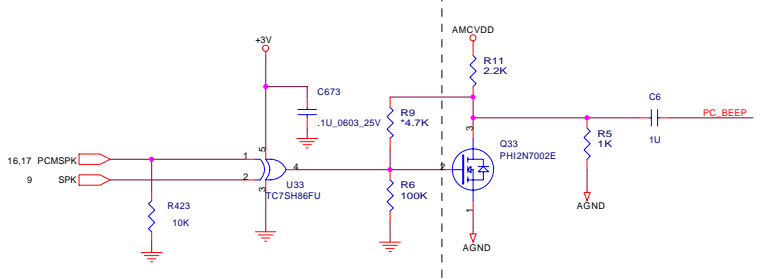
# IEEE-1394



**IDSEL = AD23**  
**MASTER = REQ3#**  
**GNT3#**



**PC SPEAKER**



CX20468-21: ADD R20, MR8  
REMOVE MR12, R413,  
D24, MR30, MR31

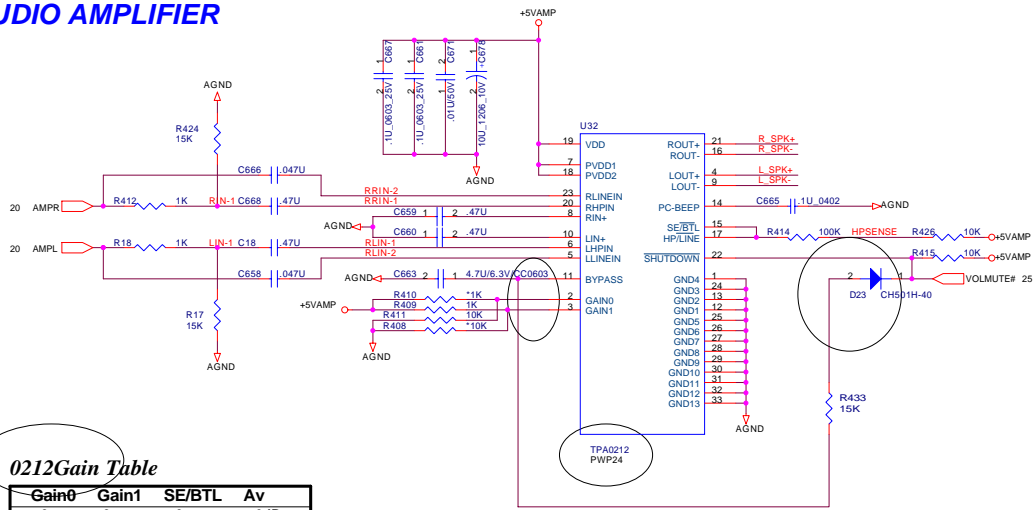
**CX20468-31:** ADD MR12, R413, D24, MR30  
REMOVE R20, MR31, MR8

CX20468-31 without software EQ:  
ADD MR12, MR31, MR30  
REMOVE R413, D24, MR8, R20

REV:B SETTING



# AUDIO AMPLIFIER

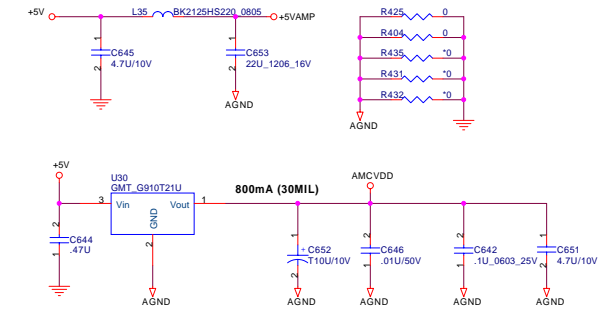
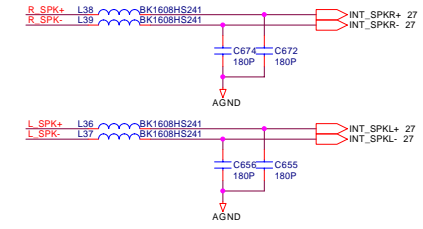


0212Gain Table

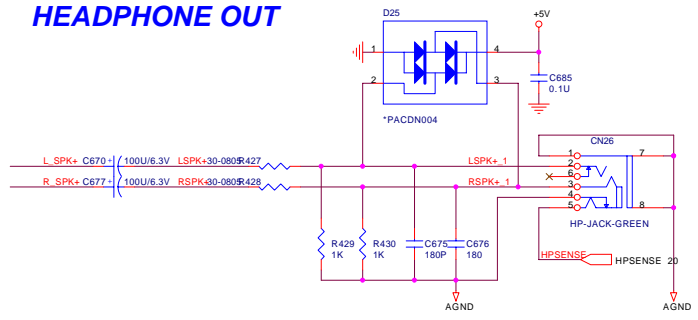
Gain0	Gain1	SE/BTL	Av
0	0	0	6dB
0	1	0	15.6dB
1	0	0	21.6dB
1	1	0	27.6dB
X	X	1	4.1dB

- Priority :
1. Port-replicator headphone is 1st priority
  2. Notebook headphone is 2nd priority
  3. Notebook internal speaker is 3rd priority
- 2004/03/20

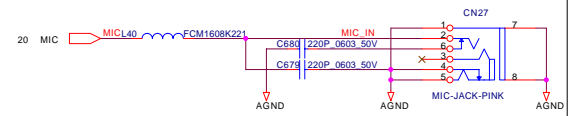
# INTERNAL SPK



# HEADPHONE OUT



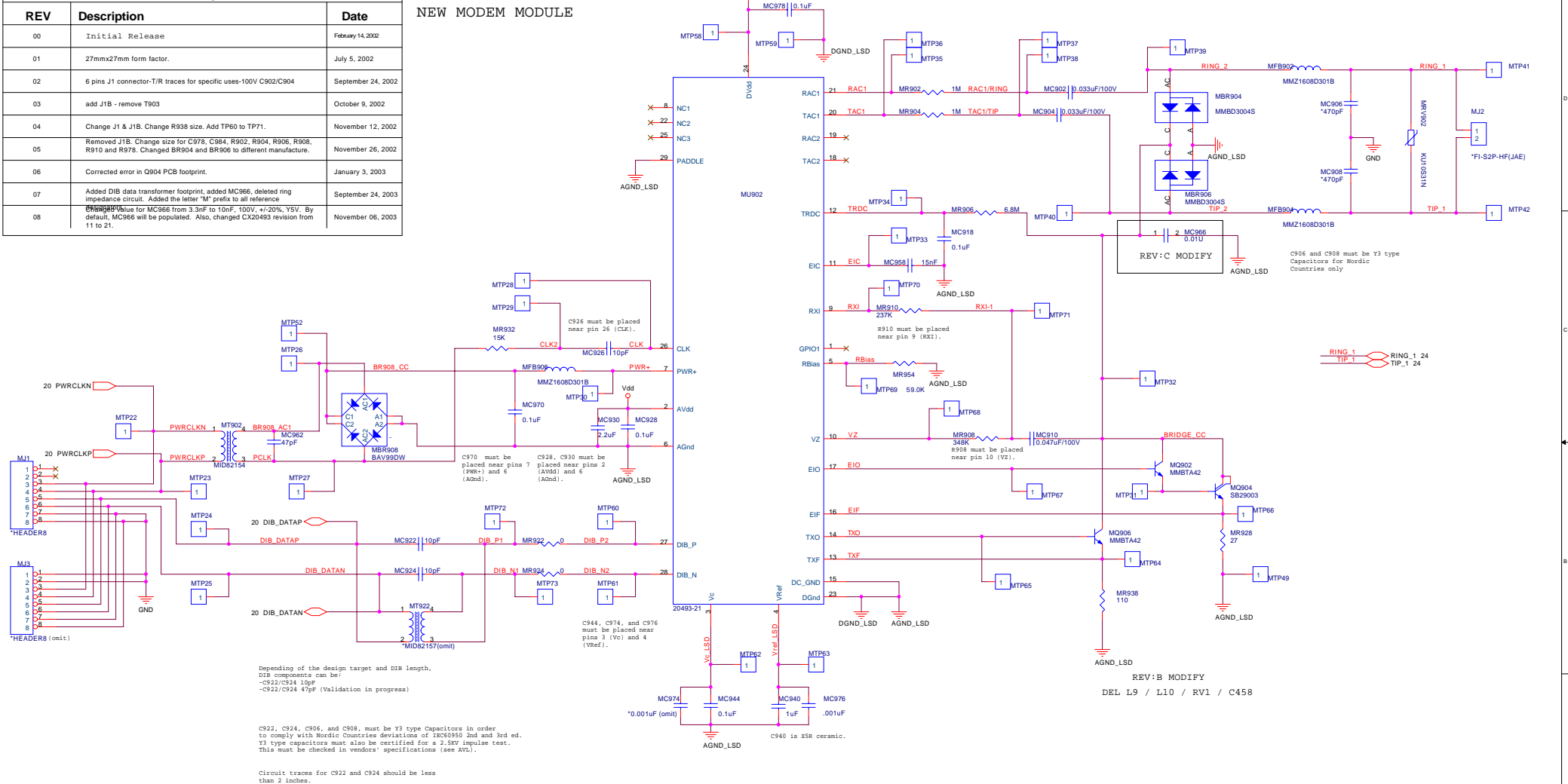
# MICROPHONE



**Revision History**

REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

**REV:B MODIFY FOR USE NEW MODEM MODULE**



Depending of the design target and DIB length, DIB components can be:  
 -C922/C924 10pF  
 -C922/C924 47pF (Validation in progress)

C922, C924, C906, and C908, must be Y3 type Capacitors in order to comply with Nordic Countries deviations of IEC60950 2nd and 3rd ed. Y3 type capacitors must also be certified for a 2.5kV impulse test. This must be checked in vendors' specifications (see AVL).

Circuit traces for C922 and C924 should be less than 2 inches.

**REV:C MODIFY**  
 1 MC966  
 0.01uF  
 AGND\_LSD

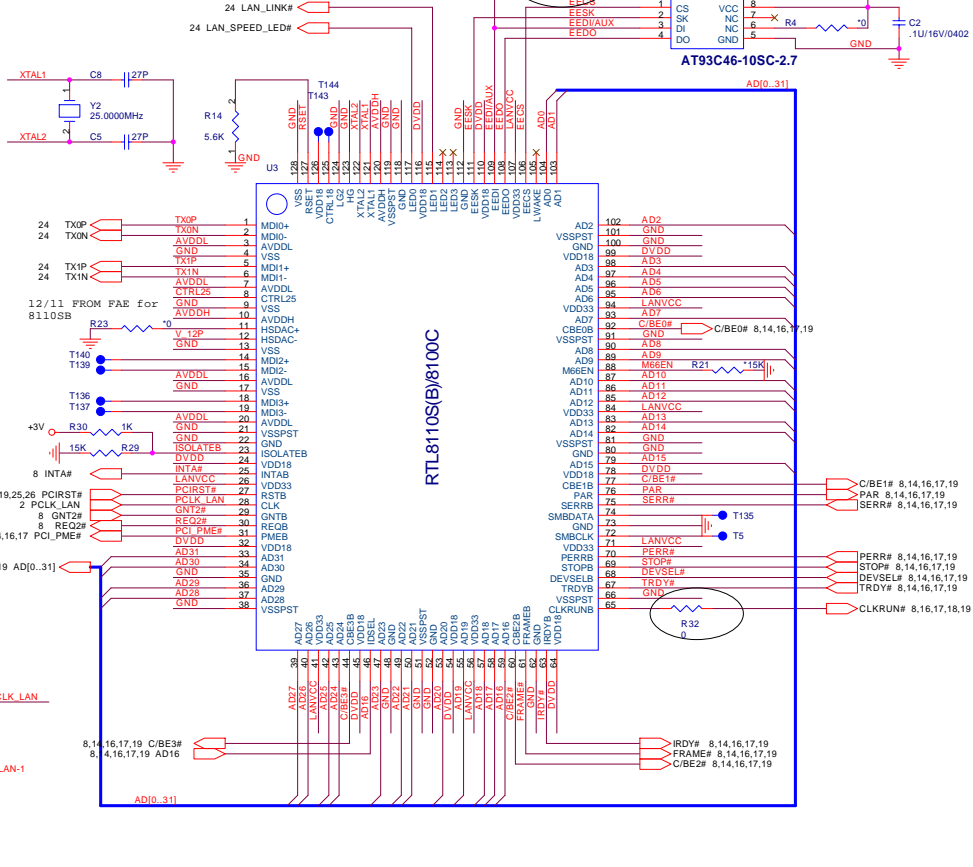
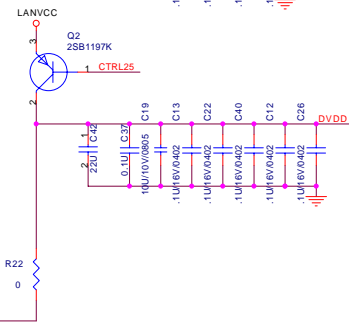
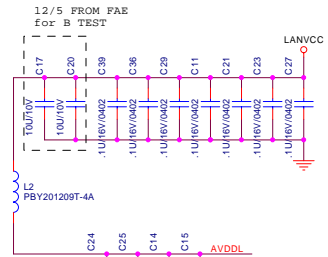
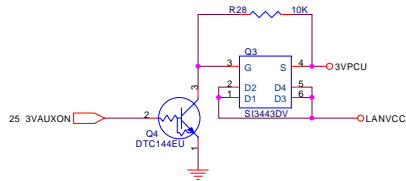
C906 and C908 must be Y3 type Capacitors for Nordic Countries only

**REV:B MODIFY**  
 DEL L9 / L10 / RV1 / C458

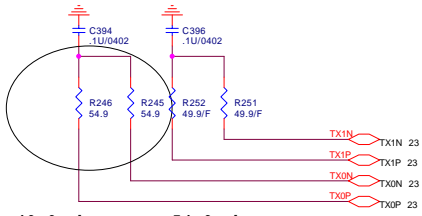
**PROJECT : KT2**  
**Quanta Computer Inc.**

Size	Document Number	REV
Custm	<b>22--MODEM (DAA)</b>	1A
Date: Friday, May 14, 2004		Sheet 22 of 33

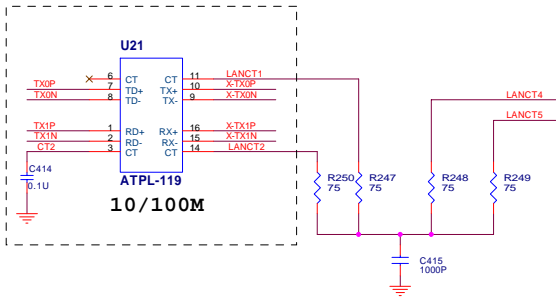
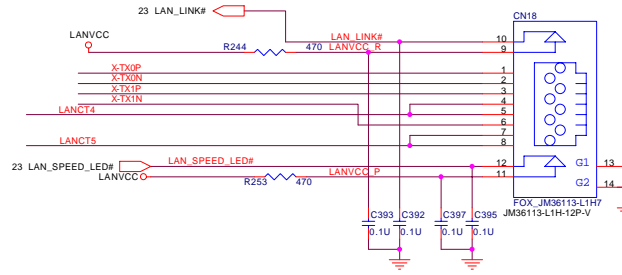
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	1.8VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120



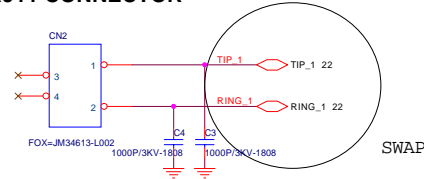
Close to Chip



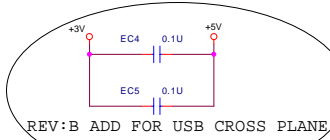
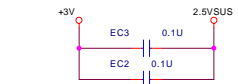
Rev: C from 49.9 change to 54.9 ohm



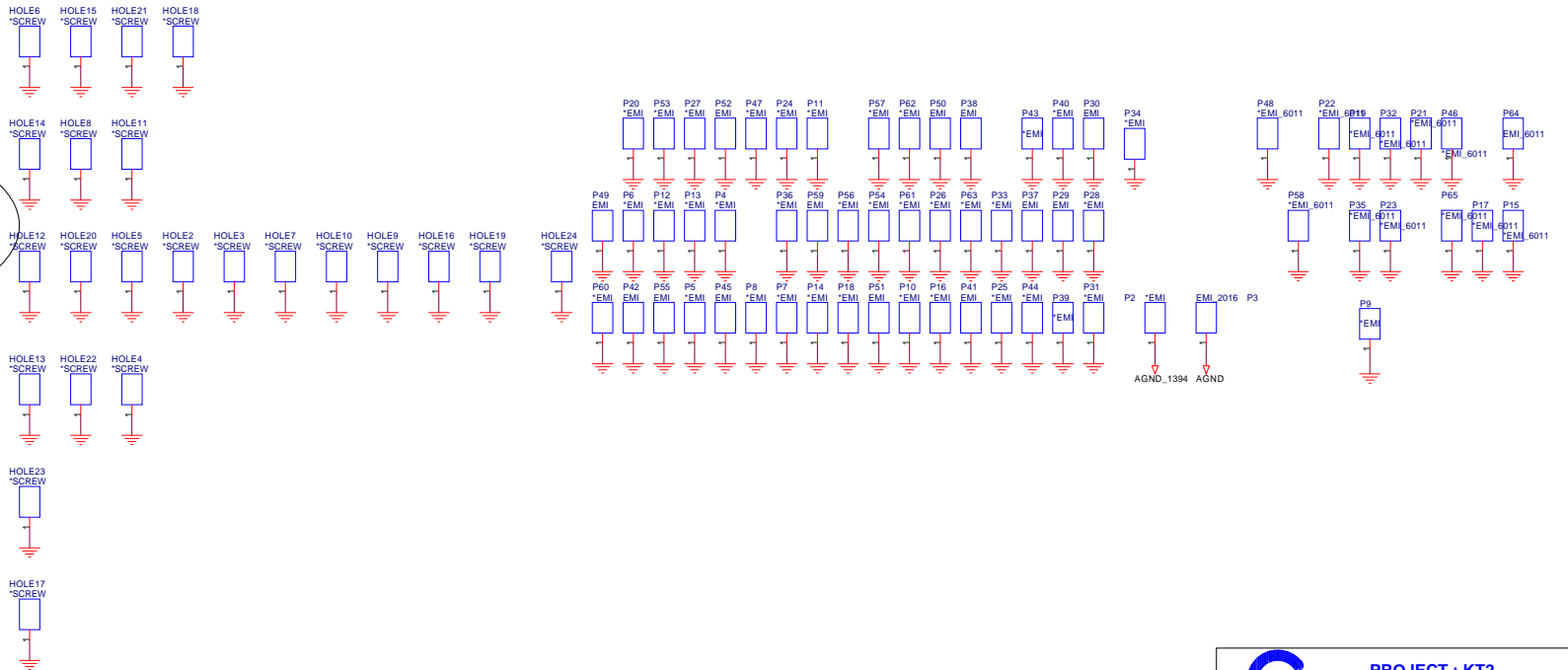
RJ11 CONNECTOR



SWAP



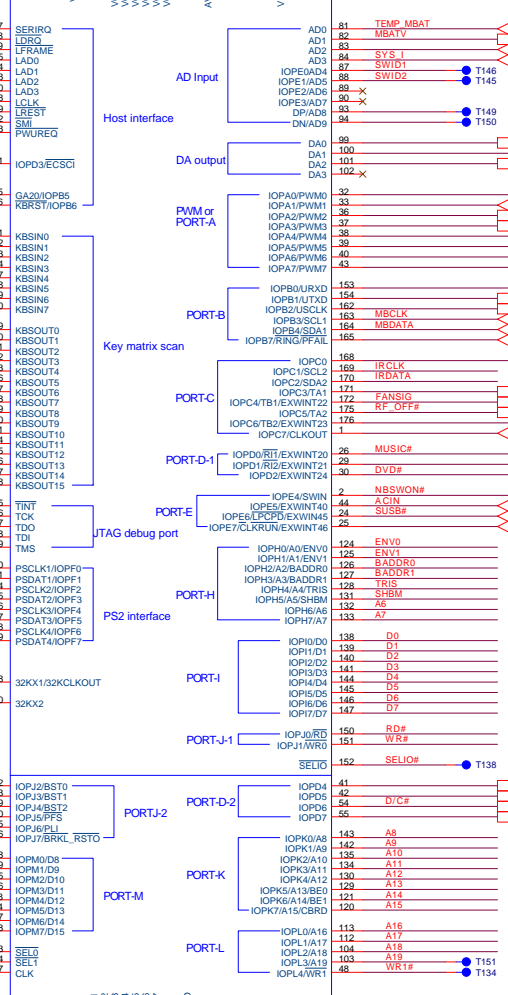
REV:B ADD FOR USB CROSS PLANE



# KBC-NS87551L

LDRQ#(pin 8) internal is no use  
 9.18 LPC\_DRQ# ← LPC\_DRQ# R385 0 DROQ#

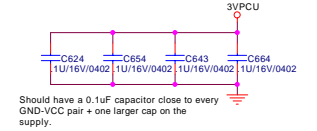
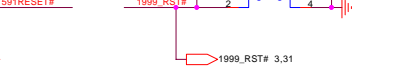
## U31



## PC97551



## REV:B



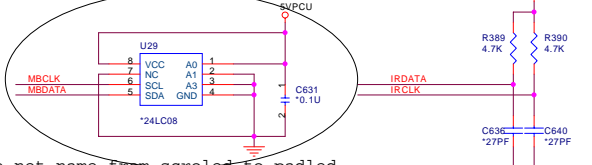
ENV1	10K	R419
BADDR0	*10K	R418
BADDR1	*10K	R417
MUSIC#	10K	R386
SBHM	10K	R416

SBBDR1-0	Index	I/O Address	Data
0 0	2E	2F	
0 1	4E	4F	
1 0	HCFGBAH, HCFGBAL	(HCFGBAH, HCFGBAL)	
1 1		Reserved	

SHBM=1. Enable shared memory with host BIOS

## REV:B u29 remove from BOM



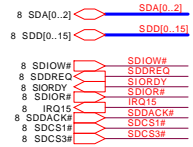
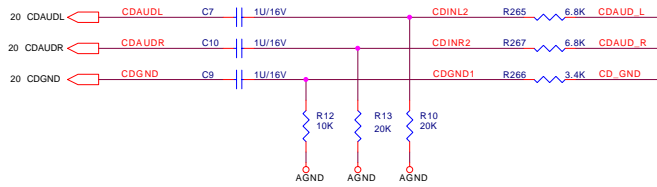
REV:B change net name from serled to padded

Pin 24 if no pull-high, will can't reboot.

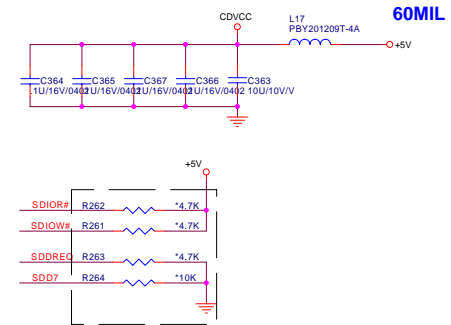
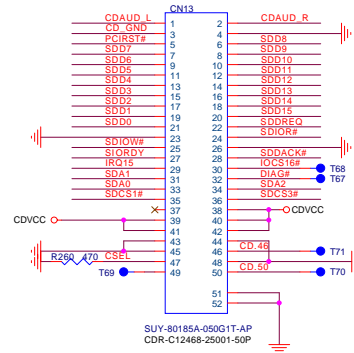
## BIOS ROM

ENV0	20	A0	D0	21	D0
ENV1	19	A1	D1	22	D1
BADDR0	18	A2	D2	23	D2
BADDR1	17	A3	D3	24	D3
TRIS	16	A4	D4	25	D4
SBHM	15	A5	D5	26	D5
AB	14	A6	D6	27	D6
A7	13	A7	D7	28	D7
A8	12	A8			
A9	11	A9			
A10	10	A10			
A11	9	A11			
A12	8	A12			
A13	7	A13			
A14	6	A14			
A15	5	A15			
A16	4	A16			
A17	3	A17			
A18	2	A18			
A19	1	A19			
A20	0	A20			
A21		A21			
A22		A22			
A23		A23			
A24		A24			
A25		A25			
A26		A26			
A27		A27			
A28		A28			
A29		A29			
A30		A30			
A31		A31			
A32		A32			
A33		A33			
A34		A34			
A35		A35			
A36		A36			
A37		A37			
A38		A38			
A39		A39			
A40		A40			
A41		A41			
A42		A42			
A43		A43			
A44		A44			
A45		A45			
A46		A46			
A47		A47			
A48		A48			
A49		A49			
A50		A50			
A51		A51			
A52		A52			
A53		A53			
A54		A54			
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A58		A58			
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A67		A67			
A68		A68			
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A70		A70			
A71		A71			
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A73		A73			
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A77		A77			
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A79		A79			
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A81		A81			
A82		A82			
A83		A83			
A84		A84			
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A93		A93			
A94		A94			
A95		A95			
A96		A96			
A97		A97			
A98		A98			
A99		A99			
A100		A100			

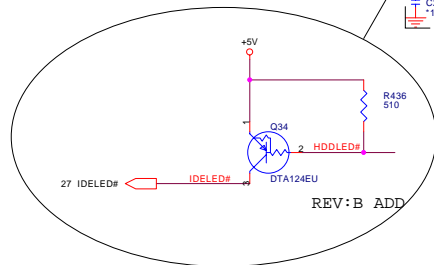
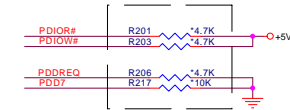
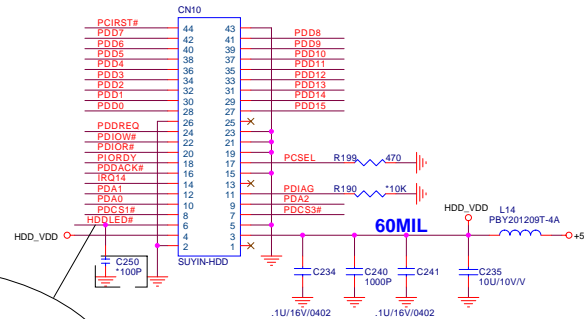
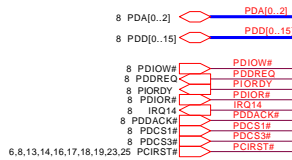
ENV0	12	A0	D0	13	D0
ENV1	11	A1	D1	14	D1
BADDR0	10	A2	D2	15	D2
BADDR1	9	A3	D3	16	D3
TRIS	8	A4	D4	17	D4
SBHM	7	A5	D5	18	D5
AB	6	A6	D6	19	D6
A7	5	A7	D7	20	D7
A8	4	A8			
A9	3	A9			
A10	2	A10			



### CD-ROM



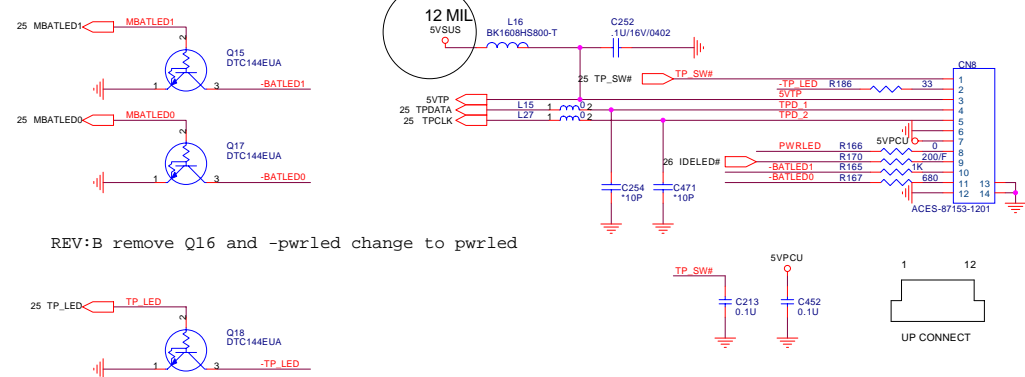
### HDD CONNECTOR



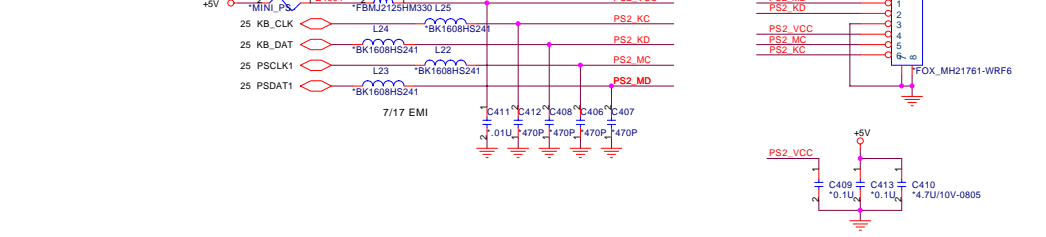
REV: B ADD



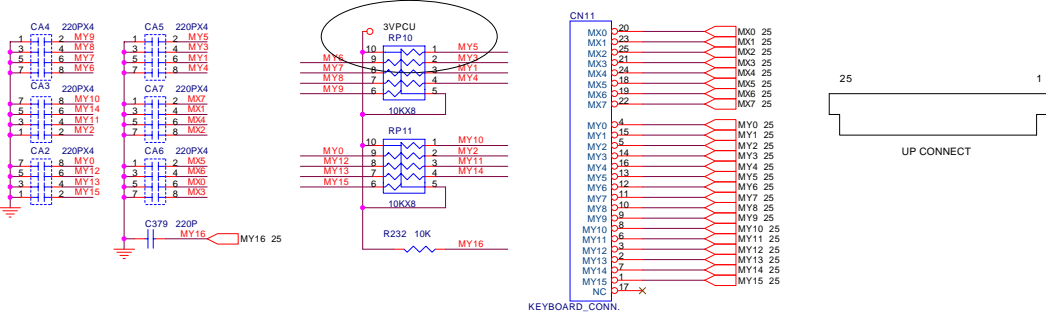
# TOUCH PAD CONNECTOR



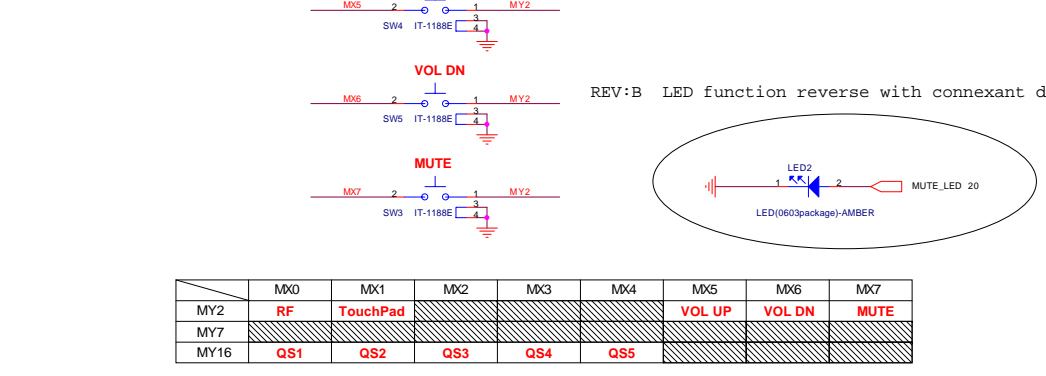
# PS/2 PORT



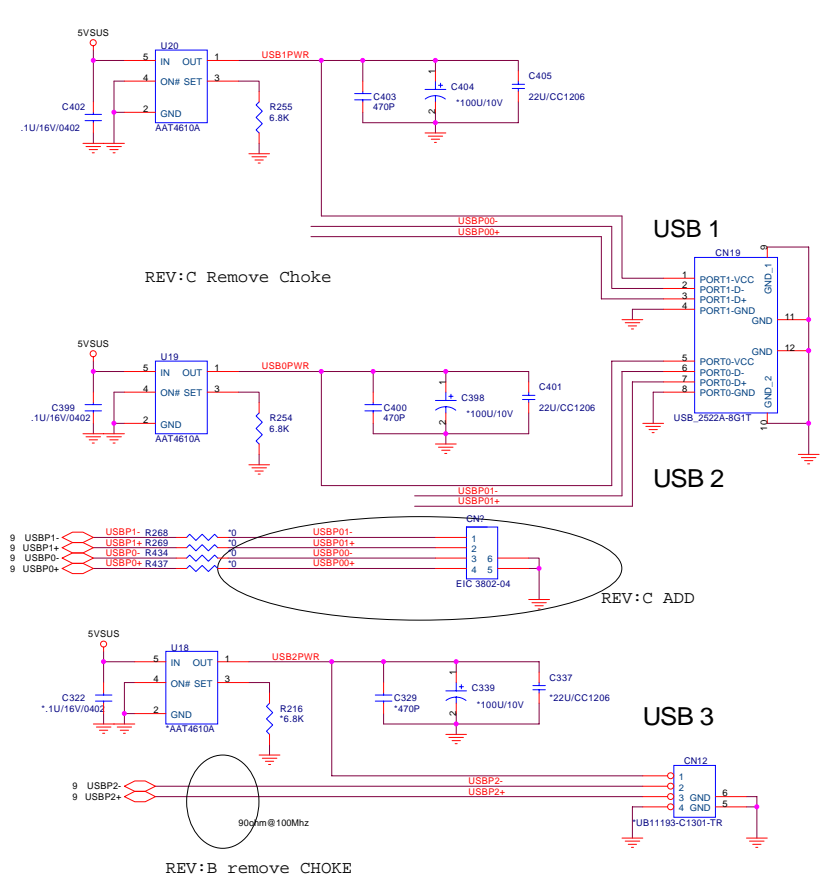
# KEYBOARD CONNECTOR



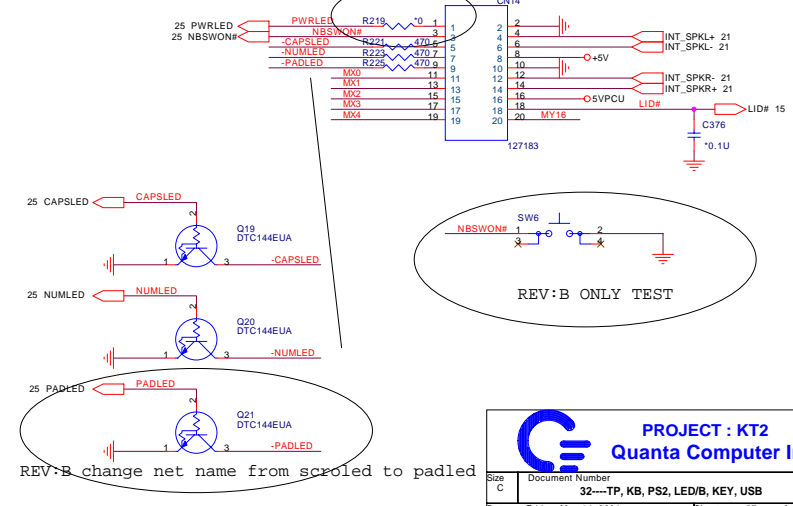
# VOLUME CONTROL

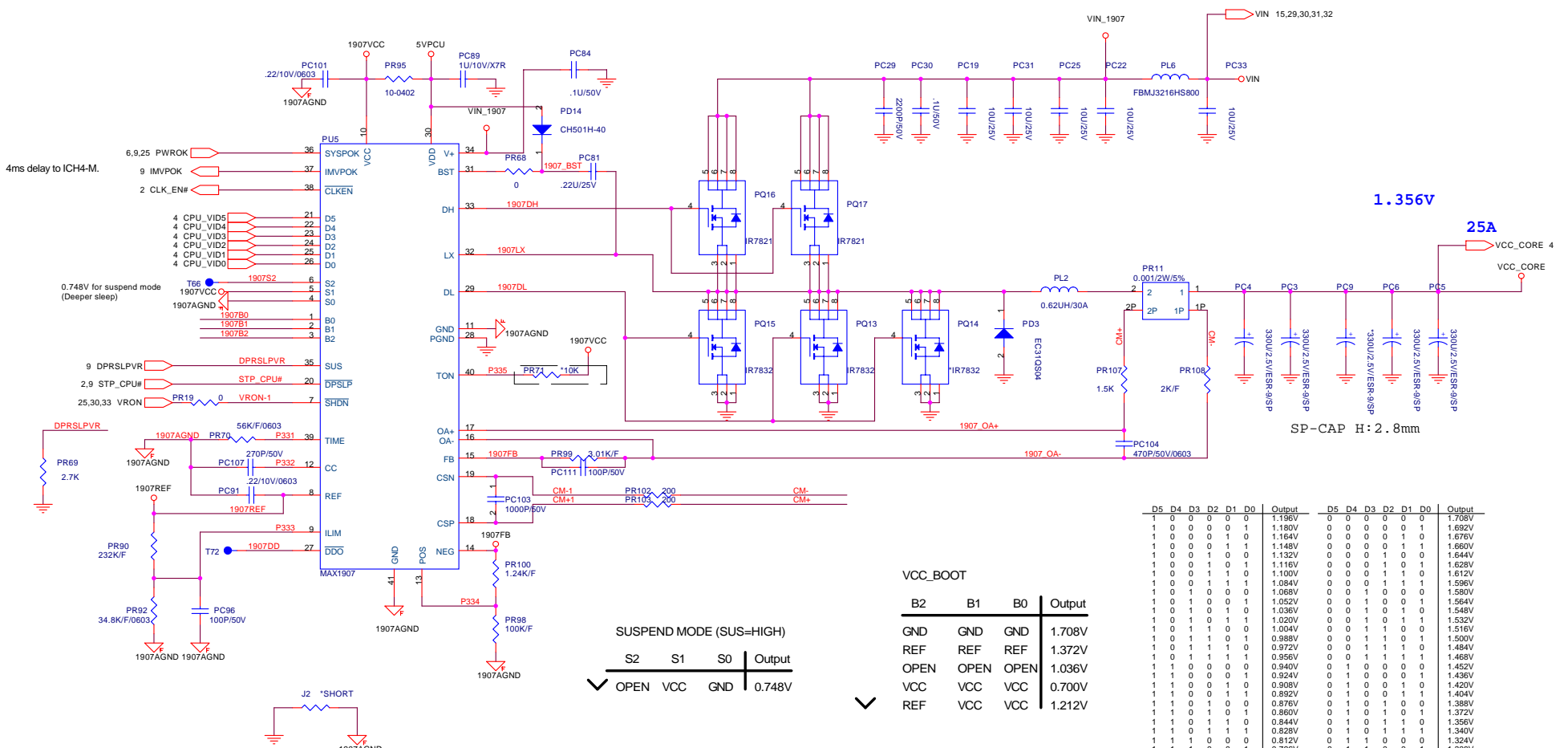


# USB PORT



# LED BOARD CON





4ms delay to ICH4-M.

0.748V for suspend mode (Deeper sleep)

1.356V

25A

VCC\_CORE 4

SP-CAP H: 2.8mm

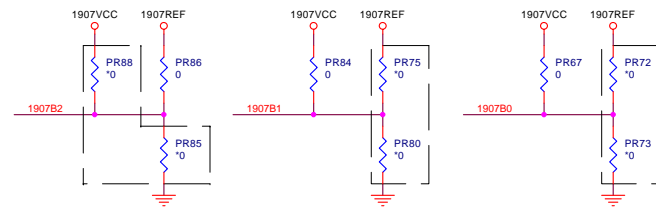
SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
✓ OPEN	VCC	GND	0.748V

VCC\_BOOT

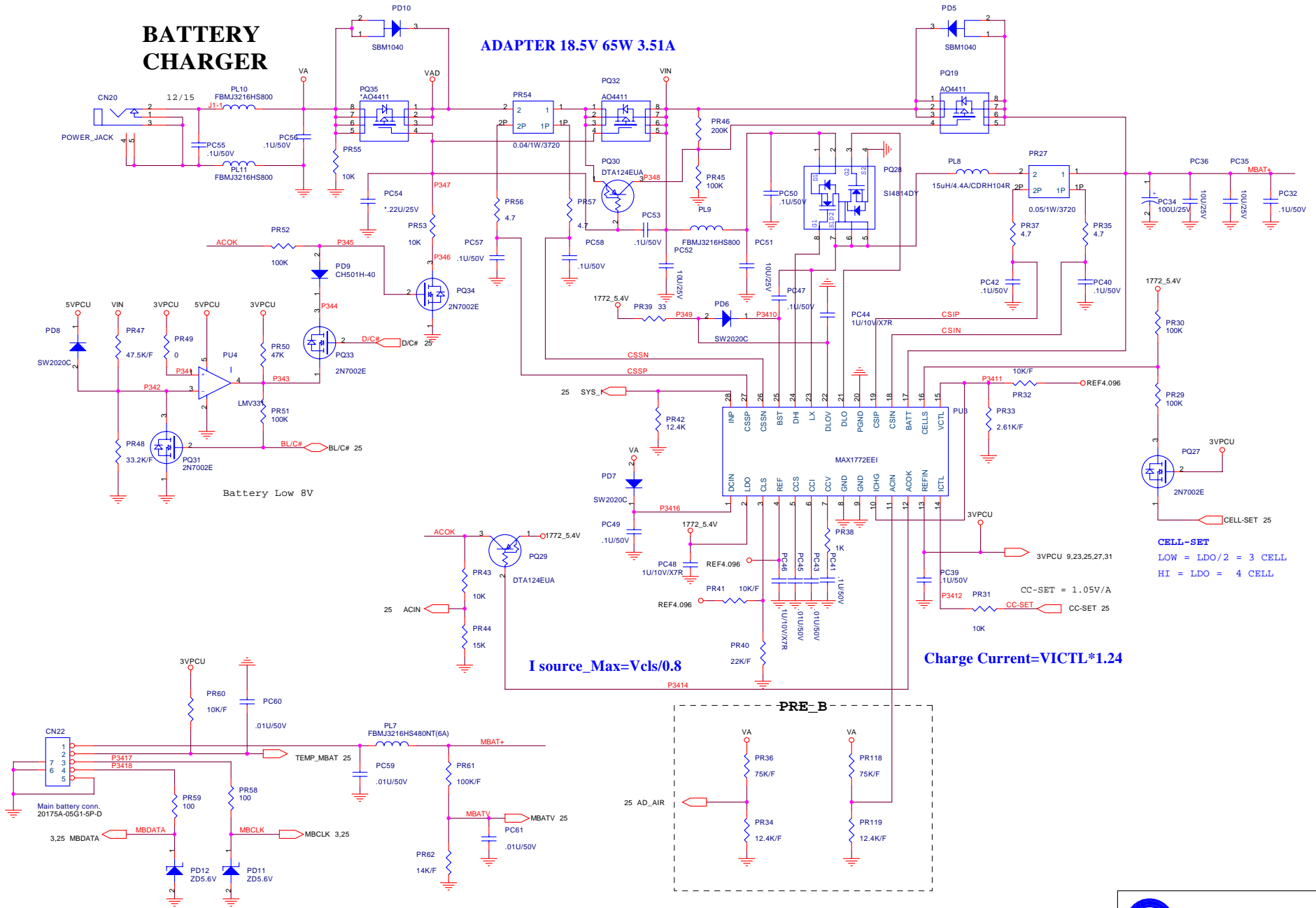
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	0	1	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	1	0	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	1	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V



# BATTERY CHARGER

## ADAPTER 18.5V 65W 3.51A



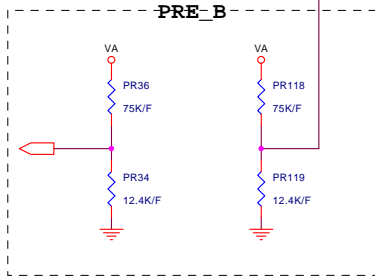
Battery Low 8V

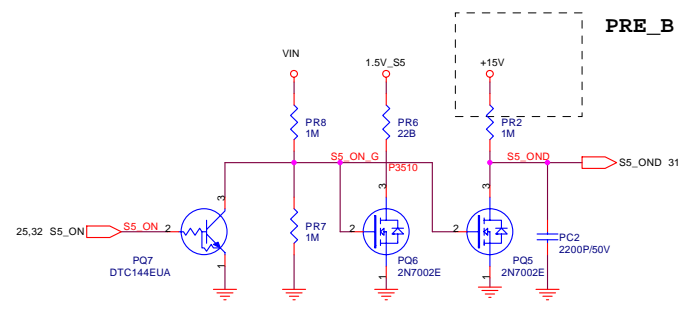
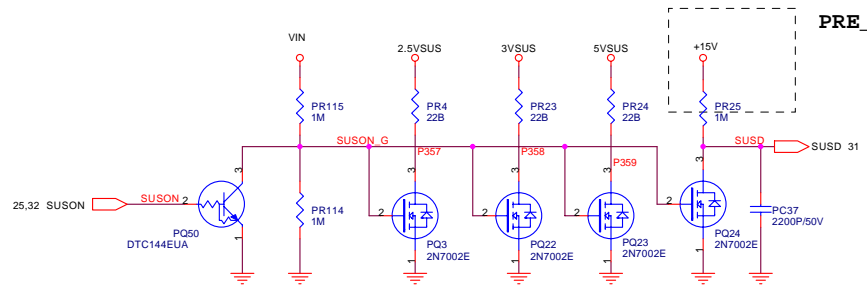
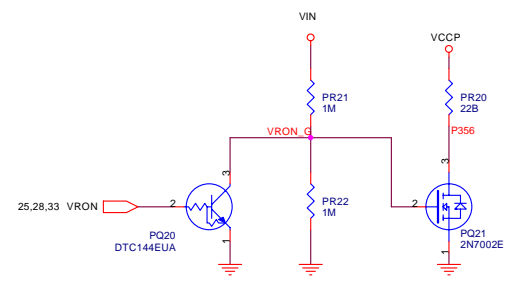
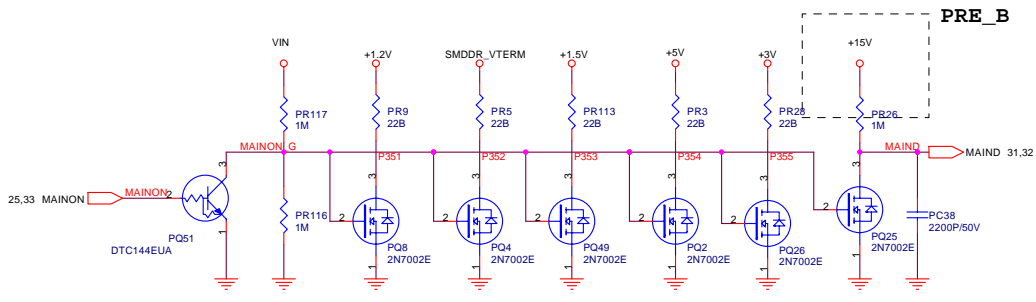
$$I_{source\_Max} = V_{cls} / 0.8$$

$$\text{Charge Current} = V_{ICTL} * 1.24$$

**CELL-SET**  
 LOW = LDO / 2 = 3 CELL  
 HI = LDO = 4 CELL

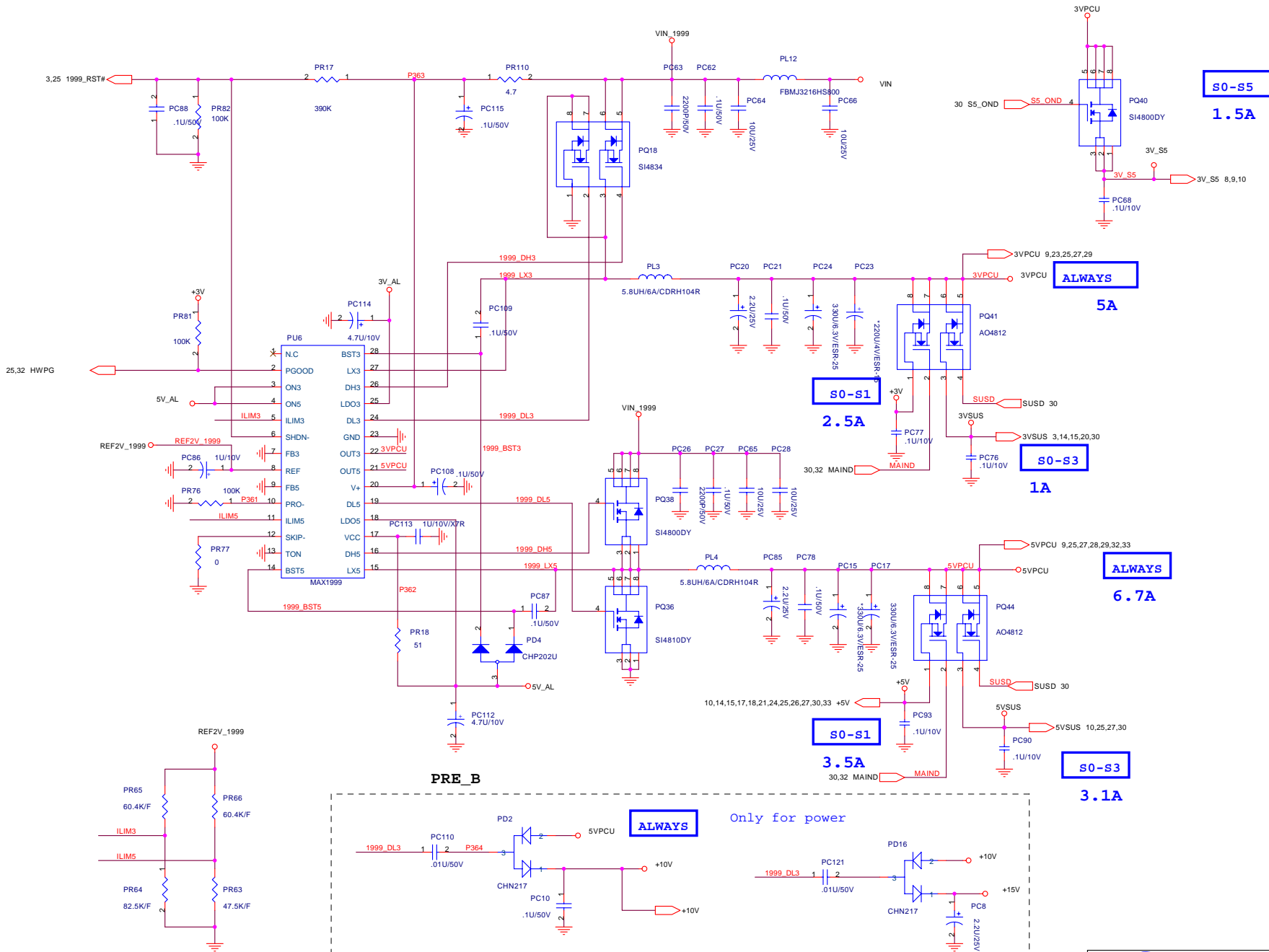
CC-SET = 1.05V/A  
 CC-SET 25





**PROJECT : KT2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	30--DISCHARGE	1A
Date:	Friday, May 14, 2004	Sheet 30 of 33



**S0-S5**  
1.5A

**ALWAYS**  
5A

**S0-S1**  
2.5A

**S0-S3**  
1A

**ALWAYS**  
6.7A

**S0-S1**  
3.5A

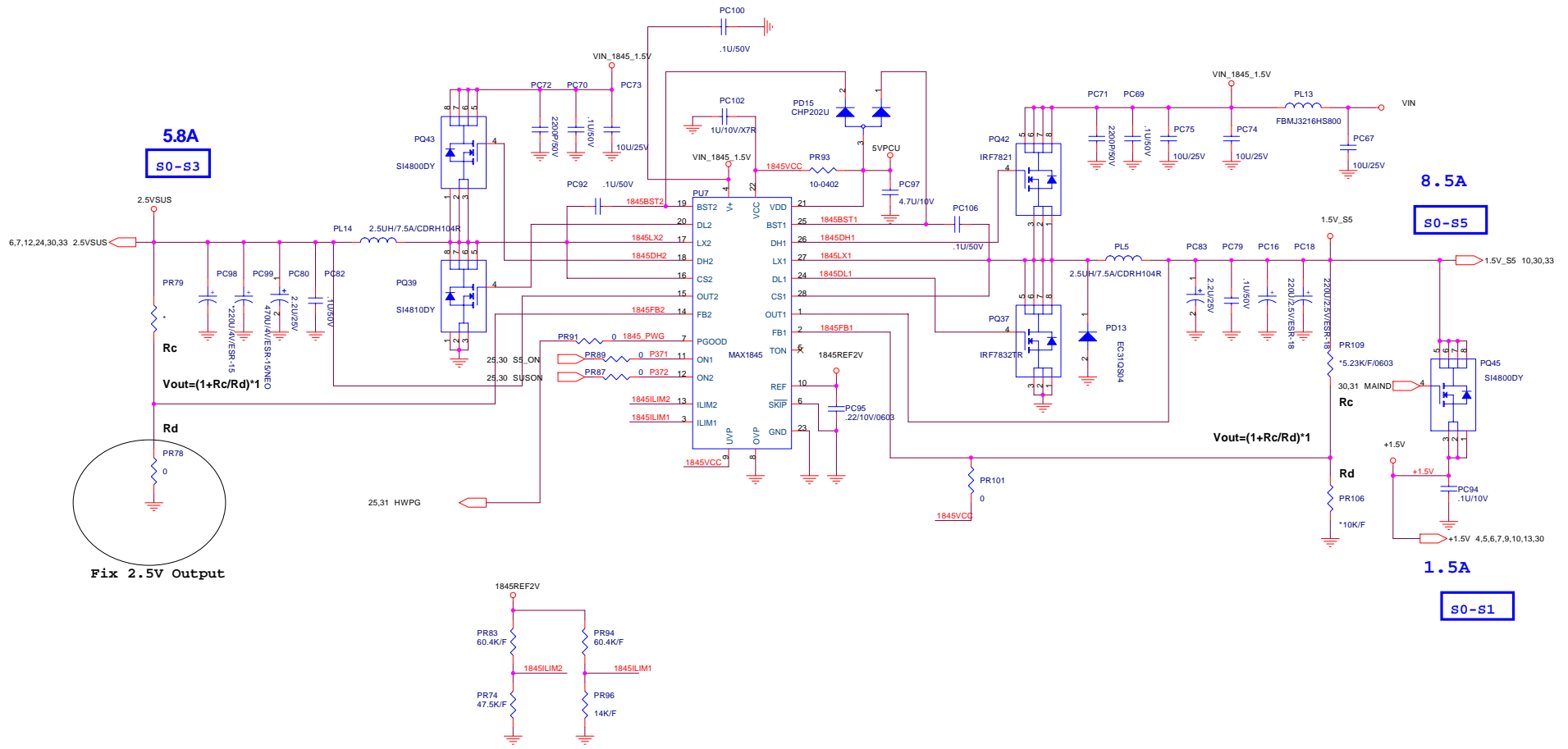
**S0-S3**  
3.1A

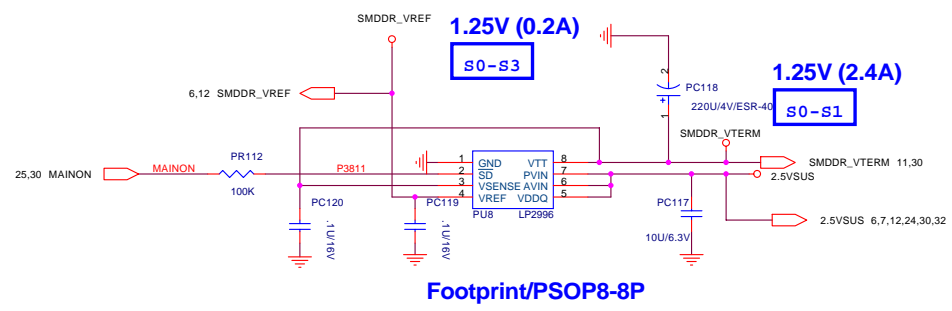
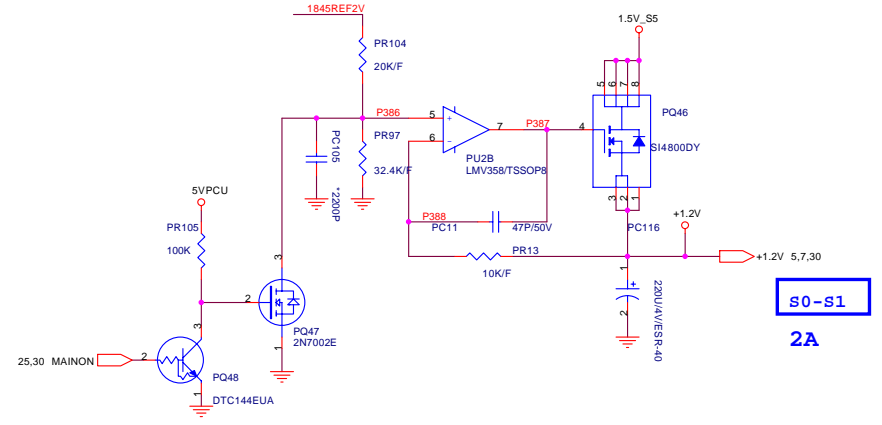
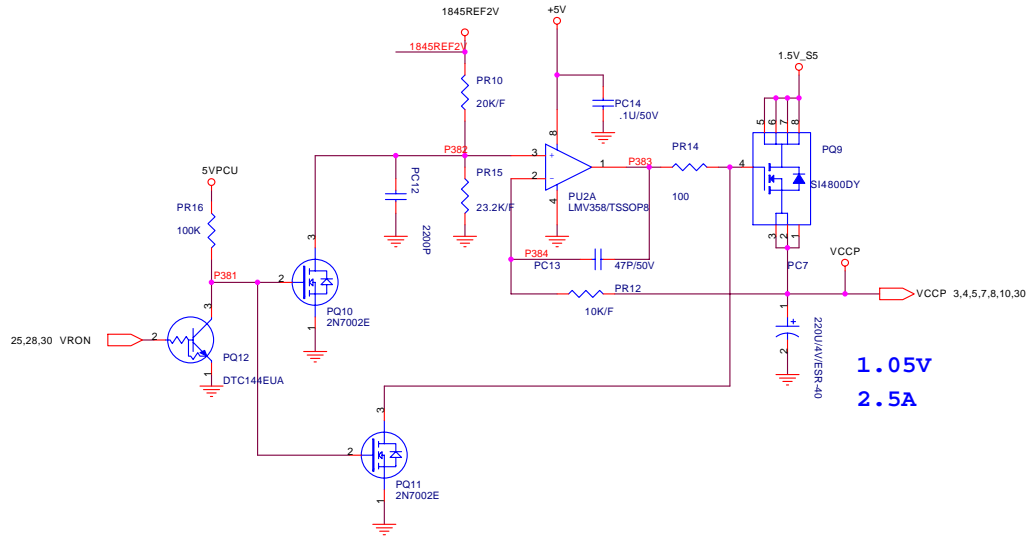
**ALWAYS**

Only for power



**PROJECT : KT2**  
**Quanta Computer Inc.**







[www.s-manuals.com](http://www.s-manuals.com)