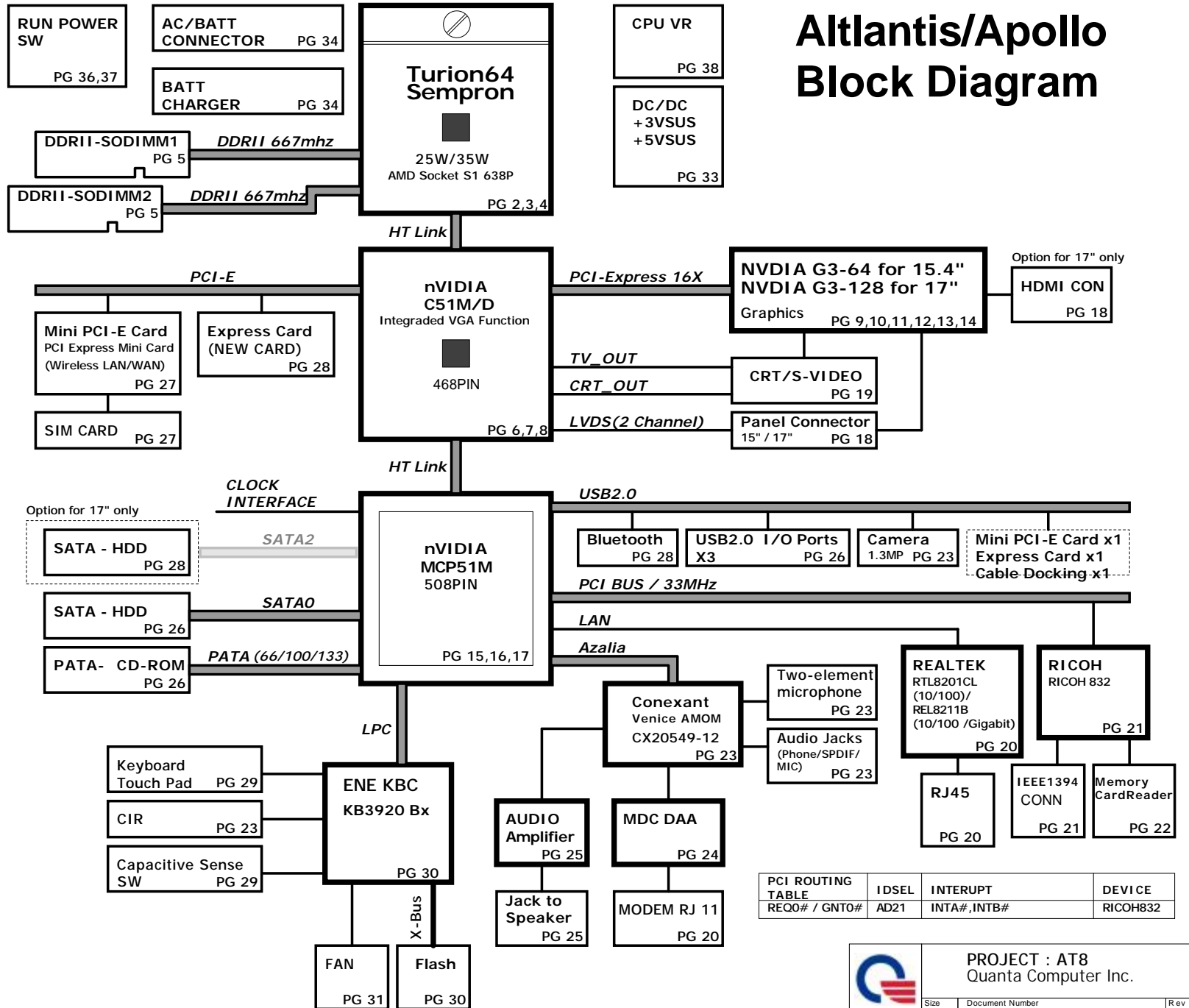


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

- Cable Docking**
- TV_OUT
 - VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PG 31

Atlantis/Apollo Block Diagram



VAULE DEFINE

A=0603,B=0805,C=1206,F=1%, OTHER IS 0402

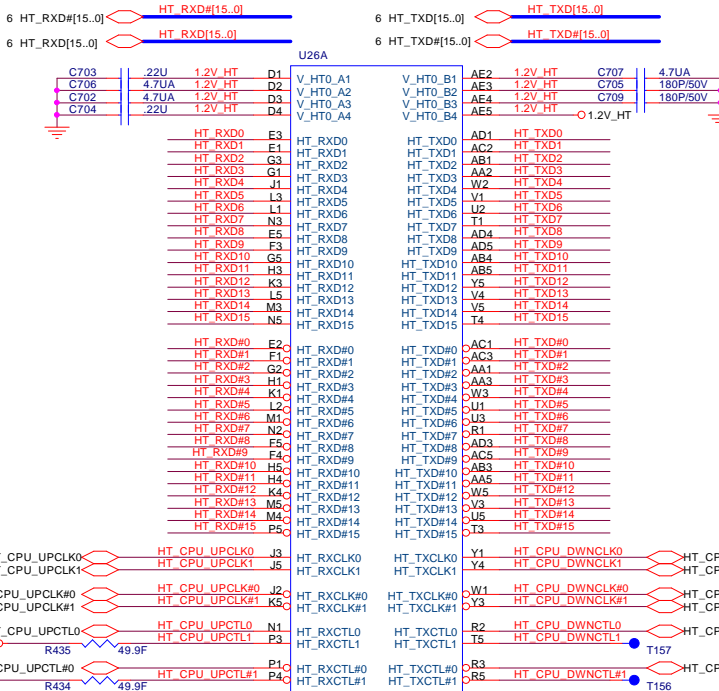
EXAMPLE
 10R=10ohm(0402)
 10A=10ohm(0603)
 10B=10ohm(0805)
 10C=10ohm(1206)
 10F=10ohm(0402 and 1%)

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

PROJECT : AT8
 Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Thursday, December 29, 2005 Sheet 1 of 38		

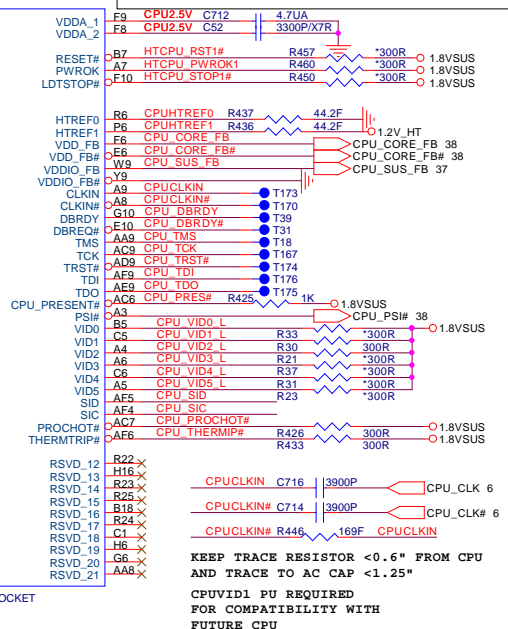
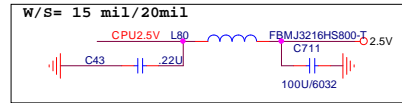
NB5/RD2/HW1



TEST PU/PL MUST FOLLOW ERRATUM 133 REVISION GUIDE FROM AMD NPT 0Fh CPU

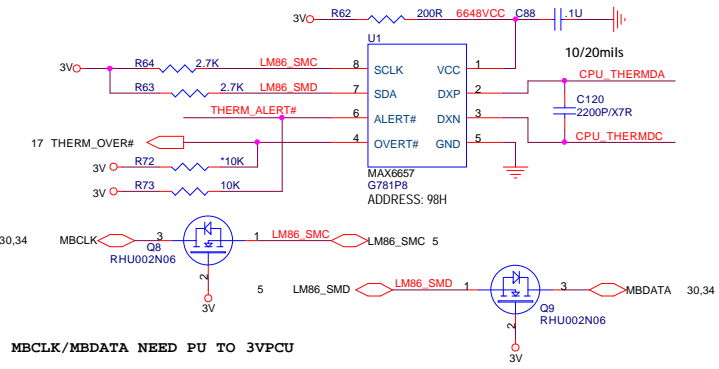
ROUTE TRACES 80OHM DIFF IMPEDENCE 8/5/20 SPACING

IF AMD SI is not used SID can be left, SIC 300ohm to Vss.

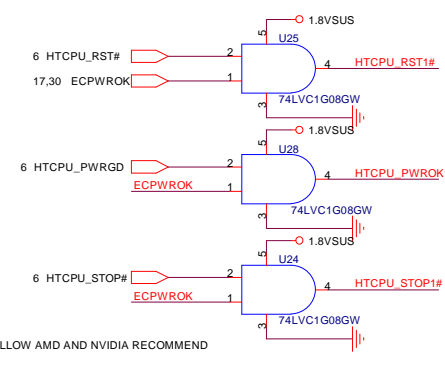


HT_RXCTL1/HT_RXCRL#1 MUST <1.5" FROM CPU PIN

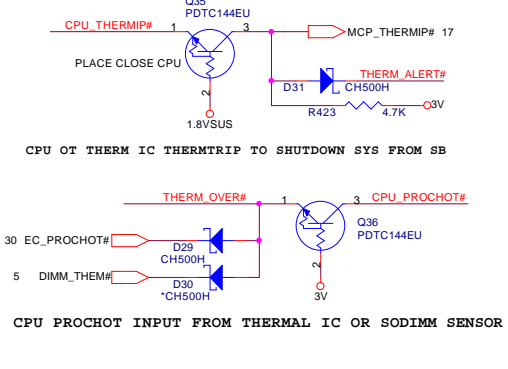
CPU THERMAL SENSOR & CONTROL



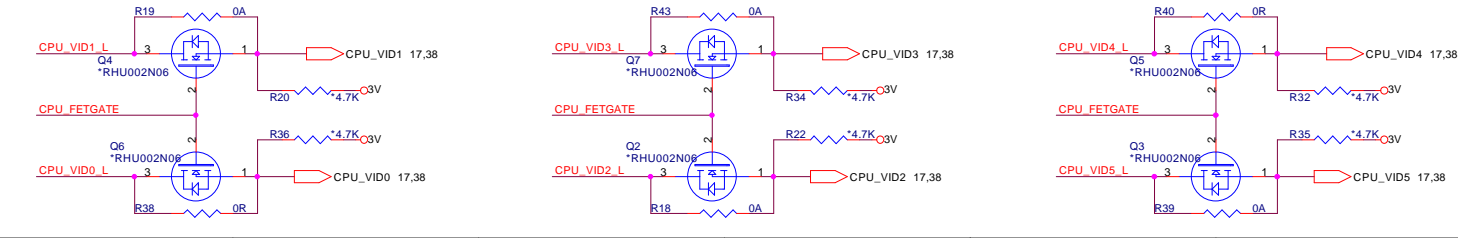
MUST KEEP LOW DURING S3-S5 TO MEET HT IO LINK SPEC HT LINK CONTROL LEVEL SHIFTER



OVER TEMP CONTROL



NEED TO CONFIRM NVIDIA FOR THE USAGE CONNECTION TO SB



PROJECT : AT8
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Size Custom	Document Number CPU(HT_LINK/CTL)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 2 of 38

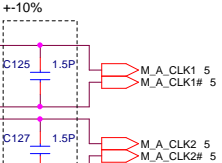
NB5/RD2/HW1

U26B	
M_A D063 AA12	MA_DATA[63]
M_A D062 AB12	MA_DATA[62]
M_A D061 AB14	MA_DATA[61]
M_A D060 AB14	MA_DATA[60]
M_A D059 W11	MA_DATA[59]
M_A D058 Y12	MA_DATA[58]
M_A D057 AD13	MA_DATA[57]
M_A D056 AB13	MA_DATA[56]
M_A D055 AD15	MA_DATA[55]
M_A D054 AB15	MA_DATA[54]
M_A D053 AB12	MA_DATA[53]
M_A D052 Y17	MA_DATA[52]
M_A D051 Y14	MA_DATA[51]
M_A D050 W14	MA_DATA[50]
M_A D049 W16	MA_DATA[49]
M_A D048 AD17	MA_DATA[48]
M_A D047 Y18	MA_DATA[47]
M_A D046 AD19	MA_DATA[46]
M_A D045 AD21	MA_DATA[45]
M_A D044 AB18	MA_DATA[44]
M_A D043 AB21	MA_DATA[43]
M_A D042 AA18	MA_DATA[42]
M_A D041 AA20	MA_DATA[41]
M_A D040 Y20	MA_DATA[40]
M_A D039 AA22	MA_DATA[39]
M_A D038 Y22	MA_DATA[38]
M_A D037 W21	MA_DATA[37]
M_A D036 Y22	MA_DATA[36]
M_A D035 AB22	MA_DATA[35]
M_A D034 AB22	MA_DATA[34]
M_A D033 AB24	MA_DATA[33]
M_A D032 Y24	MA_DATA[32]
M_A D031 H24	MA_DATA[31]
M_A D030 H20	MA_DATA[30]
M_A D029 E22	MA_DATA[29]
M_A D028 E21	MA_DATA[28]
M_A D027 H19	MA_DATA[27]
M_A D026 H24	MA_DATA[26]
M_A D025 F22	MA_DATA[25]
M_A D024 F20	MA_DATA[24]
M_A D023 C23	MA_DATA[23]
M_A D022 B22	MA_DATA[22]
M_A D021 F18	MA_DATA[21]
M_A D020 E18	MA_DATA[20]
M_A D019 E20	MA_DATA[19]
M_A D018 D22	MA_DATA[18]
M_A D017 C19	MA_DATA[17]
M_A D016 G18	MA_DATA[16]
M_A D015 G17	MA_DATA[15]
M_A D014 C17	MA_DATA[14]
M_A D013 E14	MA_DATA[13]
M_A D012 E14	MA_DATA[12]
M_A D011 H17	MA_DATA[11]
M_A D09 E16	MA_DATA[10]
M_A D08 H15	MA_DATA[9]
M_A D07 E13	MA_DATA[7]
M_A D06 C13	MA_DATA[6]
M_A D05 C12	MA_DATA[5]
M_A D04 H11	MA_DATA[4]
M_A D03 G14	MA_DATA[3]
M_A D02 H14	MA_DATA[2]
M_A D01 F12	MA_DATA[1]
M_A D00 G12	MA_DATA[0]
M_A A15 K19	MA_ADD[15]
M_A A14 K20	MA_ADD[14]
M_A A13 V24	MA_ADD[13]
M_A A12 K24	MA_ADD[12]
M_A A11 L20	MA_ADD[11]
M_A A9 L19	MA_ADD[10]
M_A A8 L22	MA_ADD[9]
M_A A7 L21	MA_ADD[8]
M_A A6 M19	MA_ADD[7]
M_A A5 M20	MA_ADD[6]
M_A A4 M24	MA_ADD[5]
M_A A3 M22	MA_ADD[4]
M_A A2 N24	MA_ADD[3]
M_A A1 N21	MA_ADD[2]
M_A A0 R21	MA_ADD[1]
	MA_ADD[0]

AMD S1 SOCKET

MA_DM[7]	Y13 M_A DOM7
MA_DM[6]	AB16 M_A DOM6
MA_DM[5]	Y19 M_A DOM5
MA_DM[4]	AC24 M_A DOM4
MA_DM[3]	F24 M_A DOM3
MA_DM[2]	E19 M_A DOM2
MA_DM[1]	C15 M_A DOM1
MA_DM[0]	E12 M_A DOM0
MA_DQS[7]	W12 M_A DQS7
MA_DQS[6]	Y15 M_A DQS6
MA_DQS[5]	AB19 M_A DQS5
MA_DQS[4]	AD23 M_A DQS4
MA_DQS[3]	G22 M_A DQS3
MA_DQS[2]	C22 M_A DQS2
MA_DQS[1]	G16 M_A DQS1
MA_DQS[0]	W13 M_A DQS0
MA_DQS#7	W15 M_A DQS#6
MA_DQS#6	AB20 M_A DQS#5
MA_DQS#5	AC23 M_A DQS#4
MA_DQS#4	G21 M_A DQS#3
MA_DQS#3	C21 M_A DQS#2
MA_DQS#2	G15 M_A DQS#1
MA_DQS#1	H13 M_A DQS#0
MA0_CLK[1]	E16 M_A CK1
MA0_CLK#1	E16 M_A CK1#
MA0_CLK[2]	Y16 M_A CK2
MA0_CLK#2	AA16 M_A CK2#
MA_BANK[2]	K22 M_A BA2
MA_BANK[1]	R20 M_A BA1
MA_BANK[0]	T22 M_A BA0
MA_RAS#	T20 M_A RAS#
MA_CAS#	U20 M_A CAS#
MA_WE#	U21 M_A WE#
MA0_CS#3	V19 M_A CS#3
MA0_CS#2	J22 M_A CS#2
MA0_CS#1	V22 M_A CS#1
MA0_CS#0	T19 M_A CS#0
MA_CKE[1]	J20 M_A CKE1
MA_CKE[0]	J21 M_A CKE0
MA0_ODT[1]	V20 M_A ODT1
MA0_ODT[0]	U19 M_A ODT0

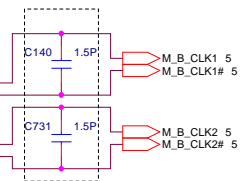
Tolerance is +/-10%



TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS

U26C	
M_B D063 AD11	MB_DATA[63]
M_B D062 AF11	MB_DATA[62]
M_B D061 AE14	MB_DATA[61]
M_B D060 AE14	MB_DATA[60]
M_B D059 Y11	MB_DATA[59]
M_B D058 AB11	MB_DATA[58]
M_B D057 AD12	MB_DATA[57]
M_B D056 AF13	MB_DATA[56]
M_B D055 AF15	MB_DATA[55]
M_B D054 AF16	MB_DATA[54]
M_B D053 AF18	MB_DATA[53]
M_B D052 AF19	MB_DATA[52]
M_B D051 AD14	MB_DATA[51]
M_B D050 AC14	MB_DATA[50]
M_B D049 AE18	MB_DATA[49]
M_B D048 AD18	MB_DATA[48]
M_B D047 AD20	MB_DATA[47]
M_B D046 AC20	MB_DATA[46]
M_B D045 AF23	MB_DATA[45]
M_B D044 AF24	MB_DATA[44]
M_B D043 AF20	MB_DATA[43]
M_B D042 AE20	MB_DATA[42]
M_B D041 AD22	MB_DATA[41]
M_B D040 AC22	MB_DATA[40]
M_B D039 AE25	MB_DATA[39]
M_B D038 AD26	MB_DATA[38]
M_B D037 AA25	MB_DATA[37]
M_B D036 AA26	MB_DATA[36]
M_B D035 AE24	MB_DATA[35]
M_B D034 AD24	MB_DATA[34]
M_B D033 AA23	MB_DATA[33]
M_B D032 AA24	MB_DATA[32]
M_B D031 G24	MB_DATA[31]
M_B D030 G23	MB_DATA[30]
M_B D029 D26	MB_DATA[29]
M_B D028 C26	MB_DATA[28]
M_B D027 C22	MB_DATA[27]
M_B D026 G25	MB_DATA[26]
M_B D025 E24	MB_DATA[25]
M_B D024 E23	MB_DATA[24]
M_B D023 C24	MB_DATA[23]
M_B D022 B24	MB_DATA[22]
M_B D021 C20	MB_DATA[21]
M_B D020 B20	MB_DATA[20]
M_B D019 C25	MB_DATA[19]
M_B D018 D24	MB_DATA[18]
M_B D017 A21	MB_DATA[17]
M_B D016 D20	MB_DATA[16]
M_B D015 D18	MB_DATA[15]
M_B D014 C18	MB_DATA[14]
M_B D013 D14	MB_DATA[13]
M_B D012 C14	MB_DATA[12]
M_B D011 A20	MB_DATA[11]
M_B D010 A19	MB_DATA[10]
M_B D09 A16	MB_DATA[9]
M_B D08 A15	MB_DATA[8]
M_B D07 A13	MB_DATA[7]
M_B D06 D12	MB_DATA[6]
M_B D05 E11	MB_DATA[5]
M_B D04 G11	MB_DATA[4]
M_B D03 B14	MB_DATA[3]
M_B D02 A14	MB_DATA[2]
M_B D01 A11	MB_DATA[1]
M_B D00 C11	MB_DATA[0]
M_B A15 J25	MB_ADD[15]
M_B A14 J26	MB_ADD[14]
M_B A13 W25	MB_ADD[13]
M_B A12 L23	MB_ADD[12]
M_B A11 L25	MB_ADD[11]
M_B A9 L24	MB_ADD[10]
M_B A8 M26	MB_ADD[9]
M_B A7 L26	MB_ADD[8]
M_B A6 N23	MB_ADD[7]
M_B A5 N24	MB_ADD[6]
M_B A4 N25	MB_ADD[5]
M_B A3 N26	MB_ADD[4]
M_B A2 P24	MB_ADD[3]
M_B A1 P26	MB_ADD[2]
M_B A0 T24	MB_ADD[1]
	MB_ADD[0]
MB_DM[7]	AD12 M_B DOM7
MB_DM[6]	AC16 M_B DOM6
MB_DM[5]	AE22 M_B DOM5
MB_DM[4]	AB26 M_B DOM4
MB_DM[3]	E25 M_B DOM3
MB_DM[2]	A22 M_B DOM2
MB_DM[1]	B16 M_B DOM1
MB_DM[0]	A12 M_B DOM0
MB_DQS[7]	AF12 M_B DQS7
MB_DQS[6]	AE16 M_B DQS6
MB_DQS[5]	AF21 M_B DQS5
MB_DQS[4]	AC25 M_B DQS4
MB_DQS[3]	F26 M_B DQS3
MB_DQS[2]	A24 M_B DQS2
MB_DQS[1]	D16 M_B DQS1
MB_DQS[0]	C12 M_B DQS0
MB_DQS#7	AE12 M_B DQS#6
MB_DQS#6	AF22 M_B DQS#5
MB_DQS#5	AC26 M_B DQS#4
MB_DQS#4	E26 M_B DQS#3
MB_DQS#3	A23 M_B DQS#2
MB_DQS#2	C16 M_B DQS#1
MB_DQS#1	B12 M_B DQS#0
MB0_CLK[1]	A17 M_B CK1
MB0_CLK#1	A18 M_B CK1#
MB0_CLK[2]	AF18 M_B CK2
MB0_CLK#2	AF17 M_B CK2#
MB_BANK[2]	K26 M_B BA2
MB_BANK[1]	T26 M_B BA1
MB_BANK[0]	U26 M_B BA0
MB_RAS#	U24 M_B RAS#
MB_CAS#	V26 M_B CAS#
MB_WE#	U22 M_B WE#
MB0_CS#3	Y26 M_B CS#3
MB0_CS#2	J24 M_B CS#2
MB0_CS#1	W24 M_B CS#1
MB0_CS#0	U23 M_B CS#0
MB_CKE[1]	H26 M_B CKE1
MB_CKE[0]	J23 M_B CKE0
MB0_ODT[1]	W23 M_B ODT1
MB0_ODT[0]	W26 M_B ODT0
VTT Sense	Y10 VTERM FB
M_VREF	W17 C51M VREF
M_ZN	AE10 MEMZNT R458
M_ZP	AF10 MEMZP R461

TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS



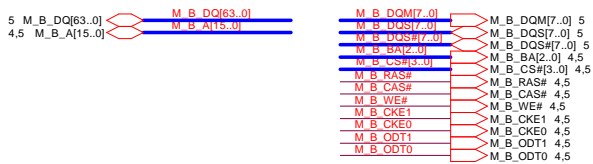
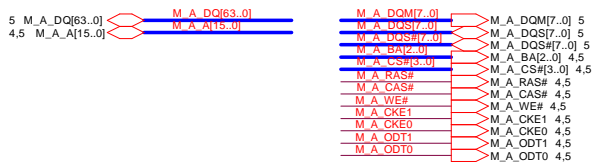
Tolerance is +/-10%

1.8VSUS

R79 2Kf

R77 2Kf

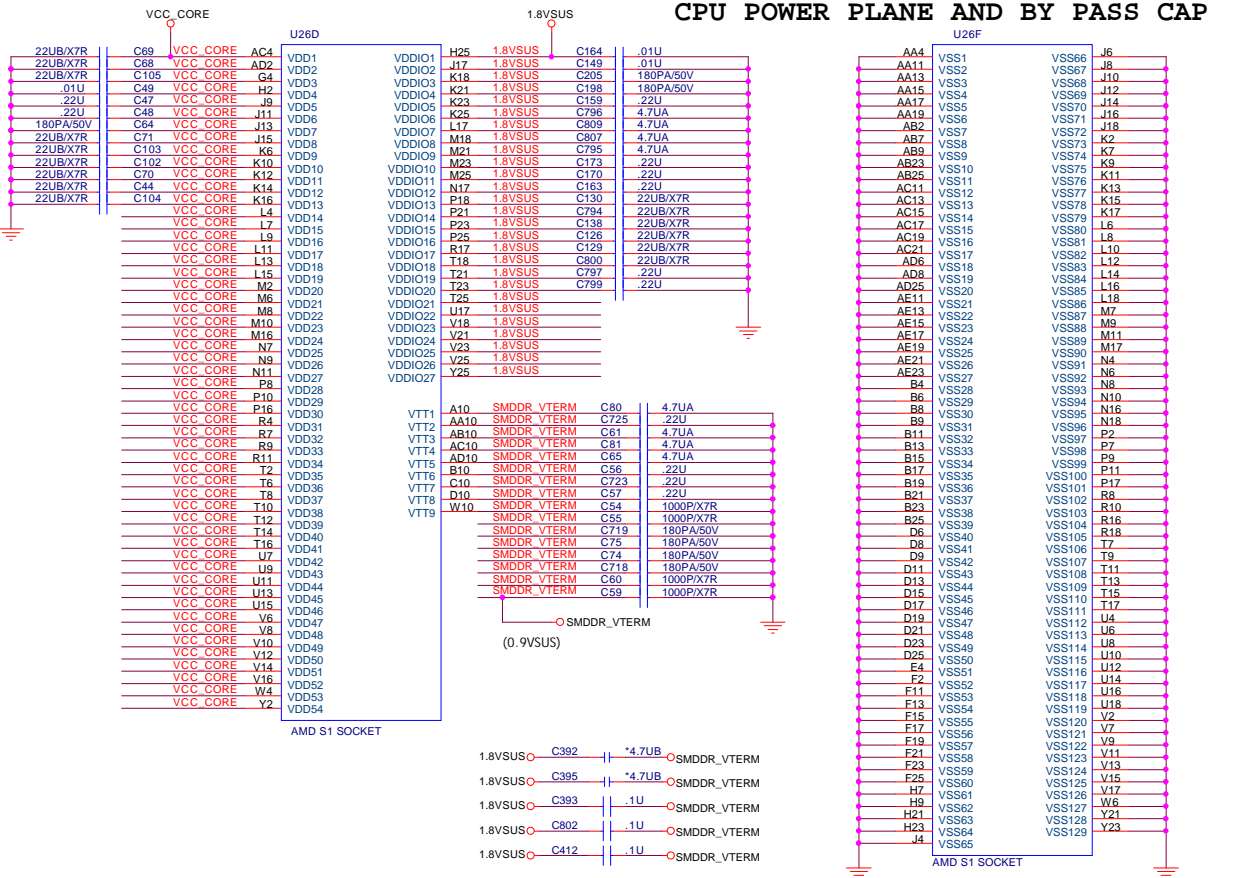
C51MVREF : W = 20MIL AND SPACE = 20MIL



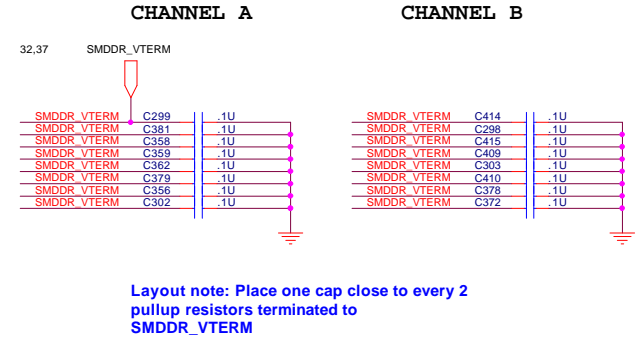
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number CPU(MEM)/F	Rev 1A
Date: Thursday, December 29, 2005 Sheet 3 of 38		

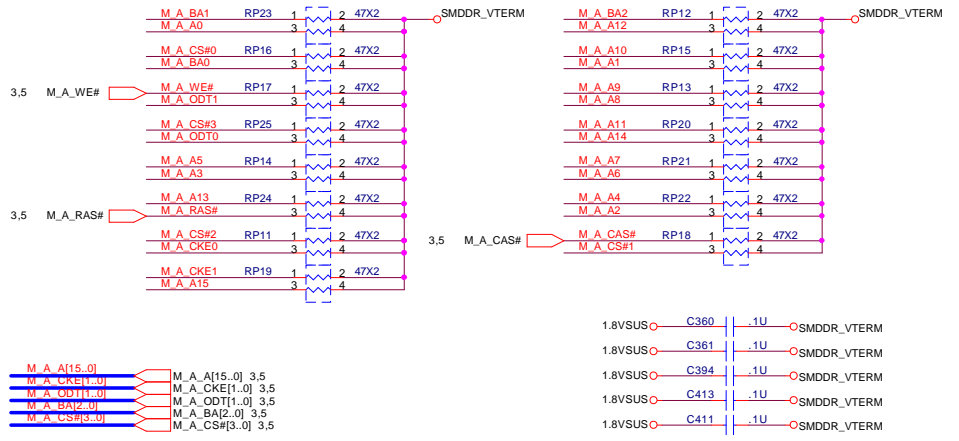
CPU POWER PLANE AND BY PASS CAP



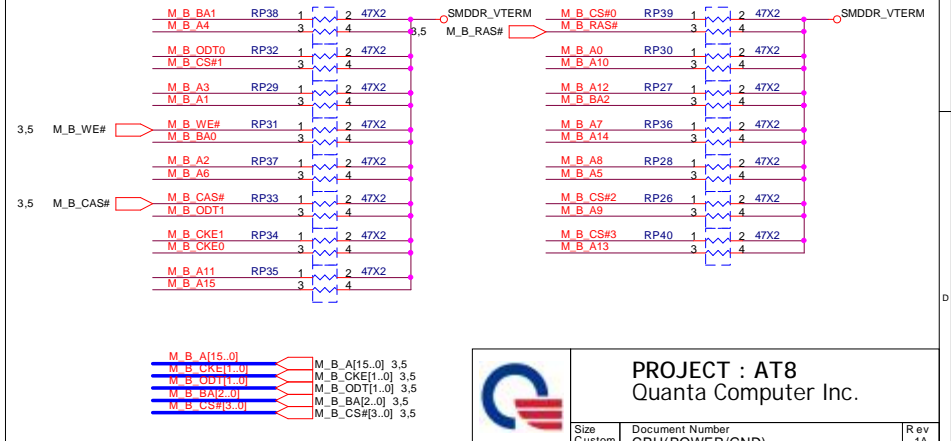
DDR2 TERMINATION BYPASS CAP



DDR1 CHANNEL A TERMINATION

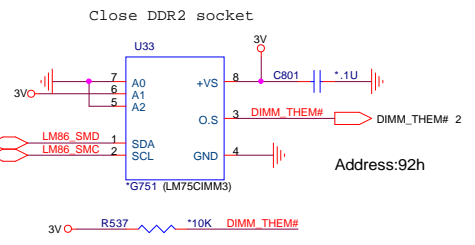
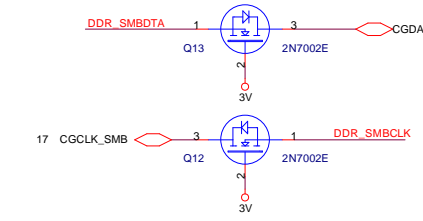
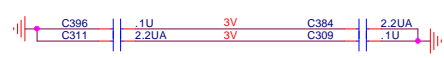
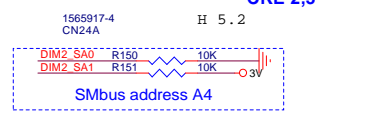
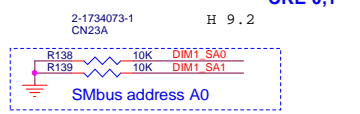
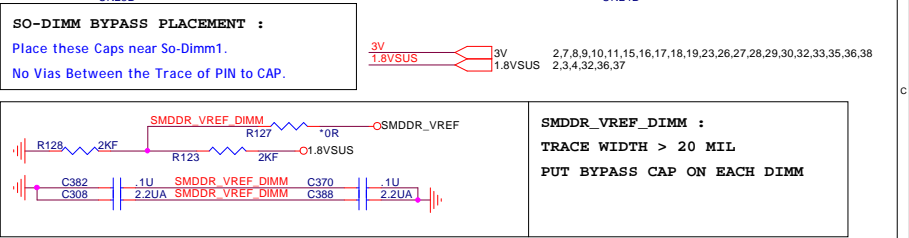
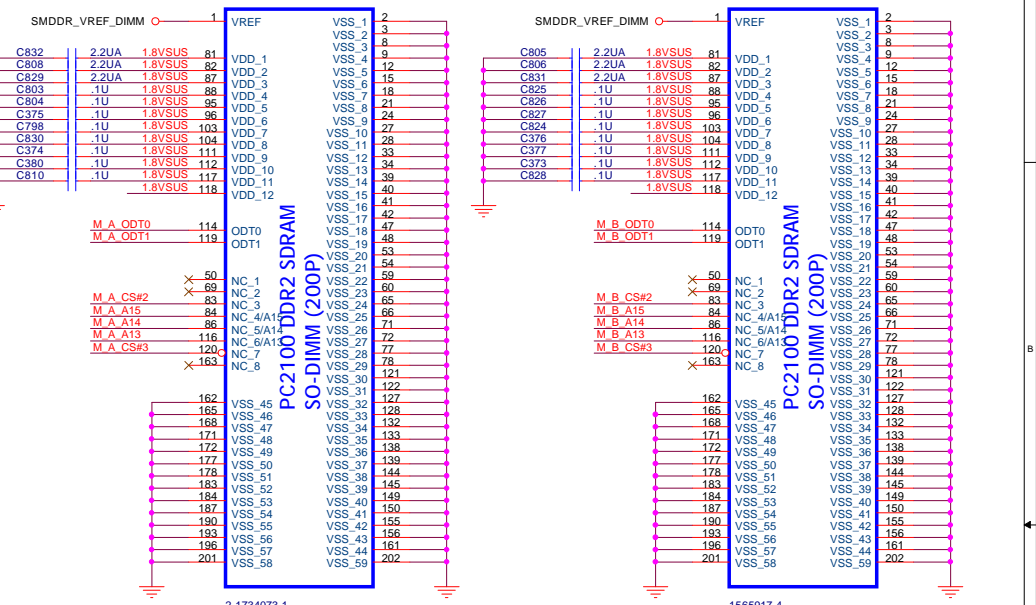
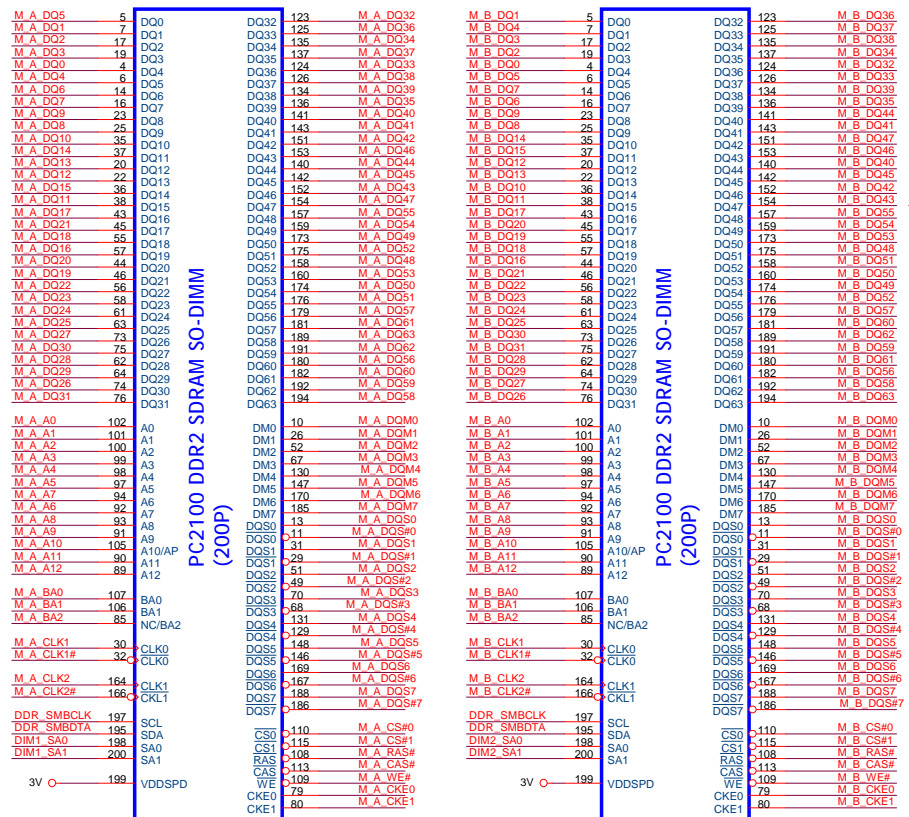
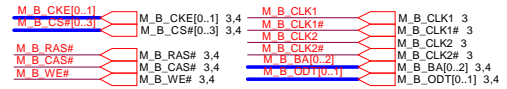
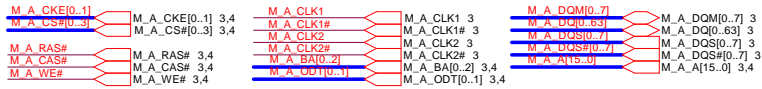


DDR1 CHANNEL B TERMINATION



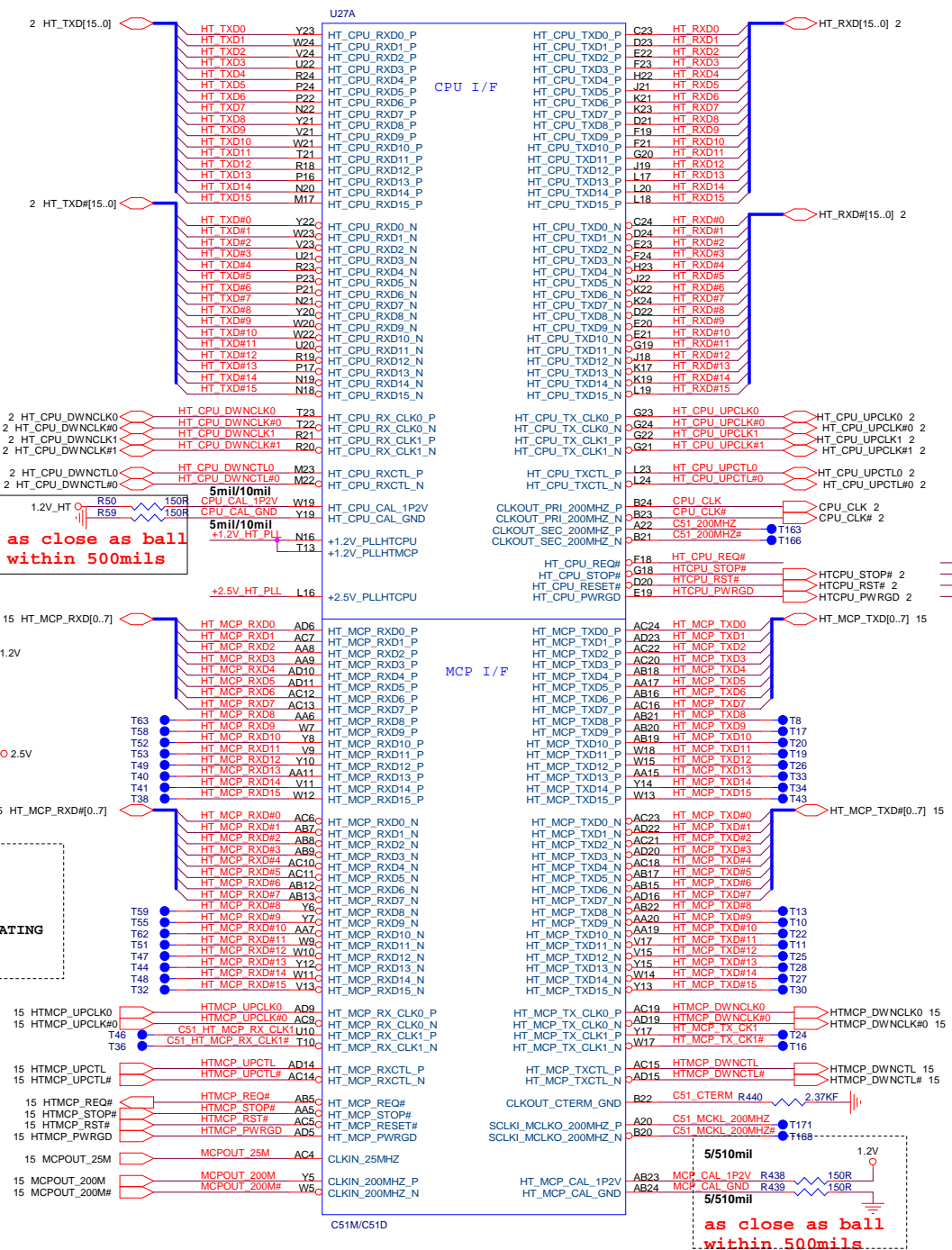
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number CPU(Power/GND)	Rev 1A
Date: Thursday, December 29, 2005	Sheet 4 of 38	



PROJECT : AT8
Quanta Computer Inc.

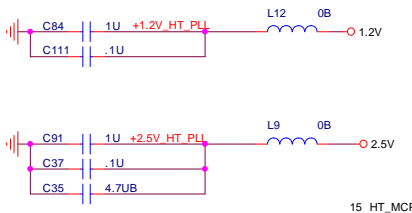
Size Custom	Document Number CPU(MEM/F)	Rev 1A
Date: Thursday, December 29, 2005 Sheet 5 of 38		



1.2V HT
R50
R59
as close as ball
within 500mils

5mil/10mil
CPU CAL 1P2V
W19
+1.2V HT PLL
N16
T13
+2.5V HT PLL
L16
+2.5V PLLHTCPU

#note from nv design guide
Pull-Hi for rise time
-0.25V

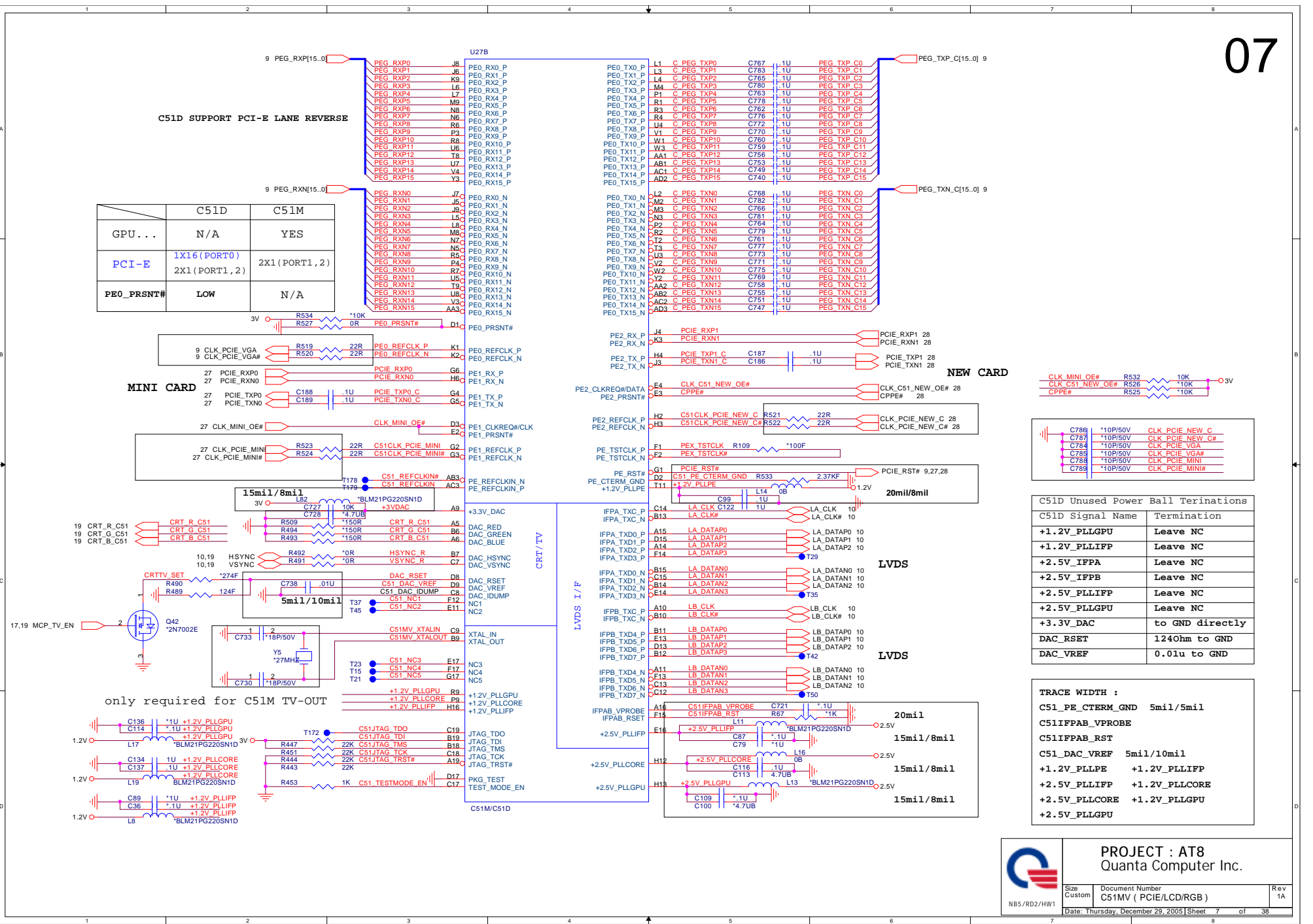


HT_MCP_RXD7 R68 *49.9F
HT_MCP_RXD#7 R70 *49.9F
STUFF : 4X4 HT LINK/UNUSED PIN FLOATING
NON-STUFF : 8X8 HT LINK(DEFAULT)

5/50mil
as close as ball
within 500mils



PROJECT : AT8 Quanta Computer Inc.		
Size Custom	Document Number C51MV (HT LINK)	Rev 1A
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	C51D	C51M
GPU...	N/A	YES
PCI-E	1X16 (PORT0) 2X1 (PORT1, 2)	2X1 (PORT1, 2)
PE0_PRSNT#	LOW	N/A

MINI CARD

NEW CARD

C51D Unused Power Ball Terminations

C51D Signal Name	Termination
+1.2V_PLLGPU	Leave NC
+1.2V_PLLIFP	Leave NC
+2.5V_IFPA	Leave NC
+2.5V_IFPB	Leave NC
+2.5V_PLLIFP	Leave NC
+2.5V_PLLGPU	Leave NC
+3.3V_DAC	to GND directly
DAC_RSET	1240hm to GND
DAC_VREF	0.01u to GND

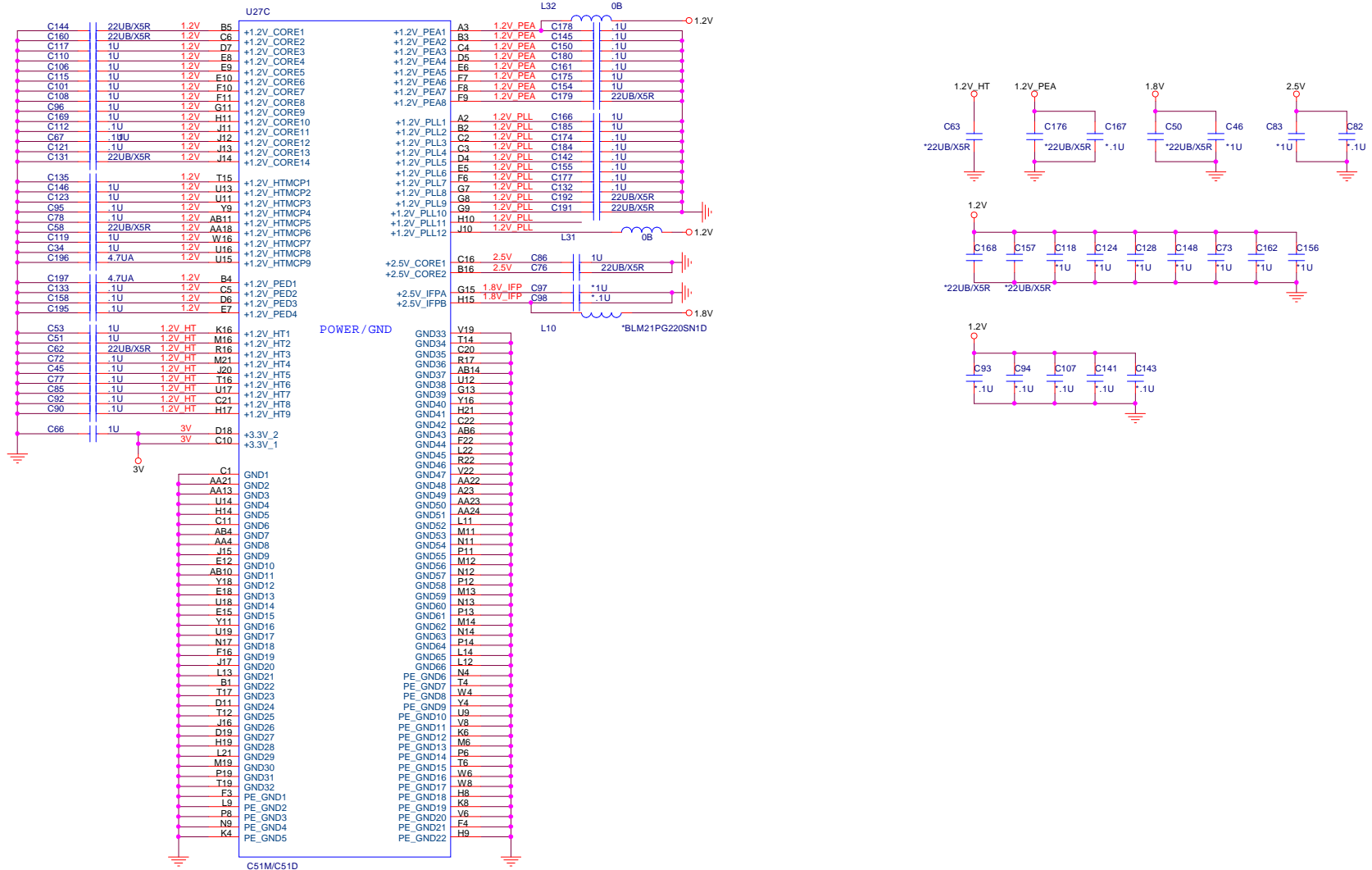
TRACE WIDTH :


C51_PE_TERM_GND	5mil/5mil
C51IFPAB_VPROBE	
C51IFPAB_RST	
C51_DAC_VREF	5mil/10mil
+1.2V_PLLPE	+1.2V_PLLIFP
+2.5V_PLLIFP	+1.2V_PLLCORE
+2.5V_PLLGPU	+1.2V_PLLGPU

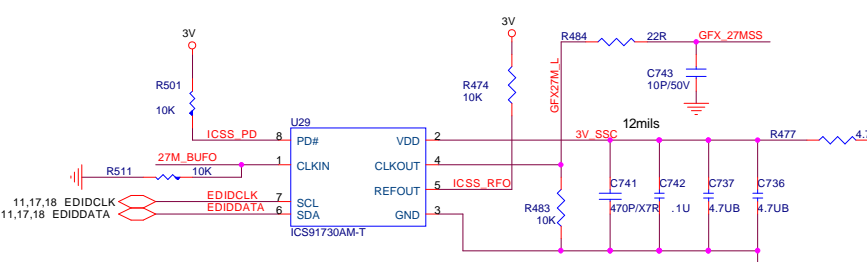
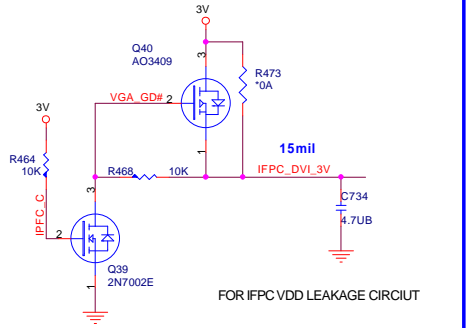
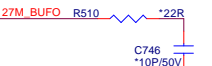
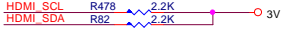
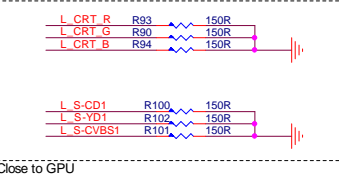
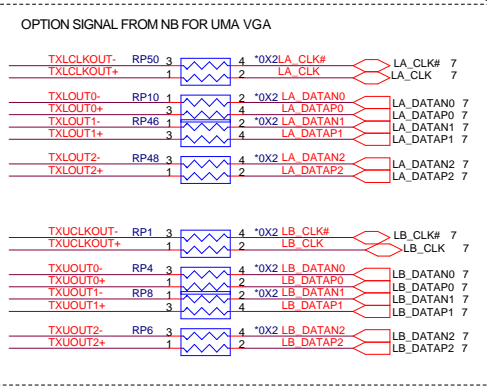
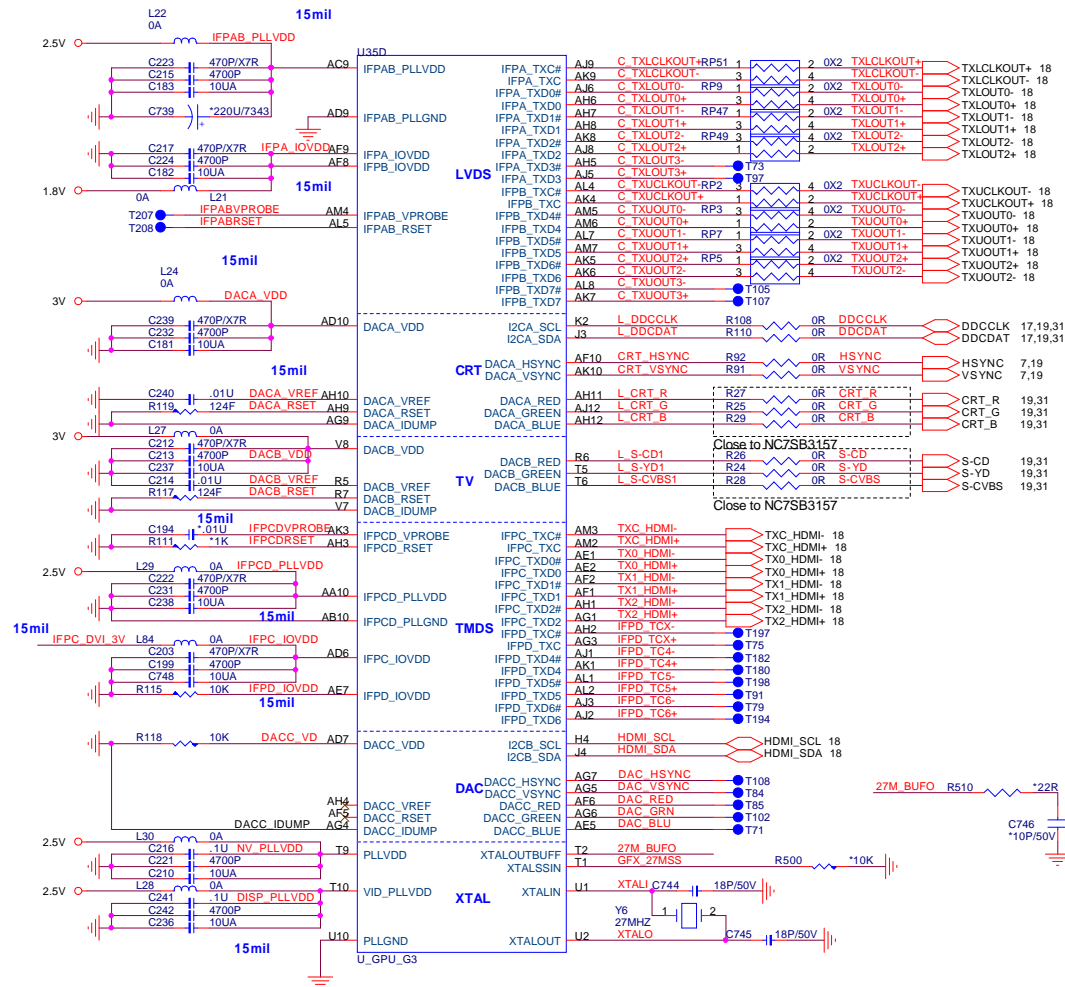
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number C51MV (PCI-E/LCD/RGB)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 7 of 38

C51M/C51D POWER PLANE/GND & BYPASS



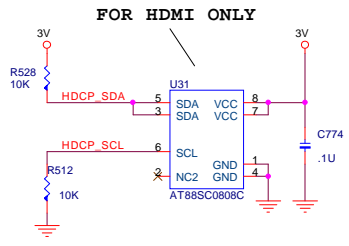
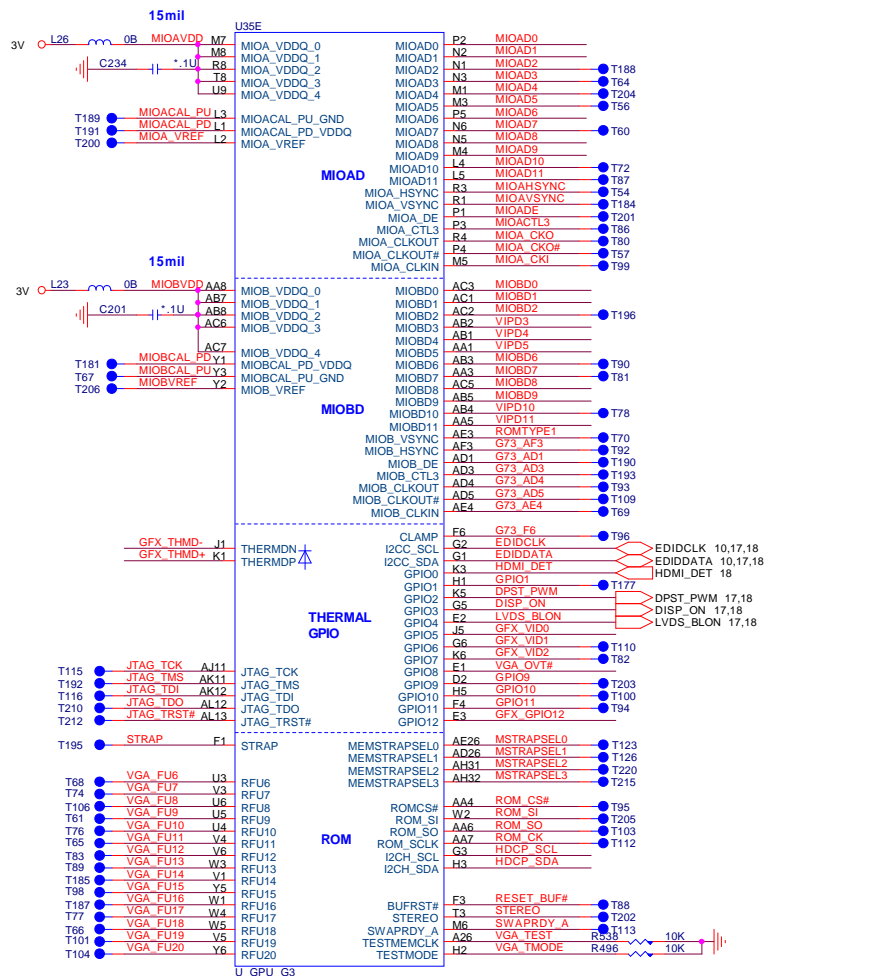
 NB5/RDZ/HW1	PROJECT : AT8 Quanta Computer Inc.		
	Size Custom	Document Number C51M (POWER/GND)	Rev 1A
	Date: Wednesday, January 11, 2006 Sheet 8 of 38		



SPREAD SPECTRUM

PROJECT : AT8
Quanta Computer Inc.

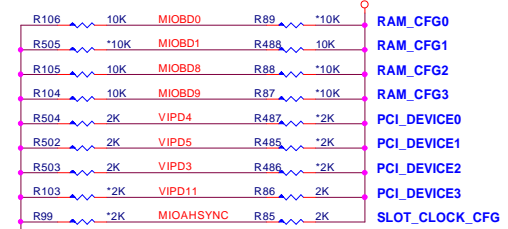
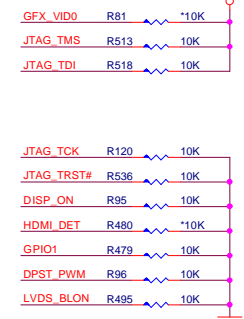
Size Custom	Document Number GFX(LVDS, CRT, TV)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 10 of 38



PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0111	G72M-V/G73M-V
others	Reserved

GFX_VID0
 L : Low Voltage
 H : Normal Voltage



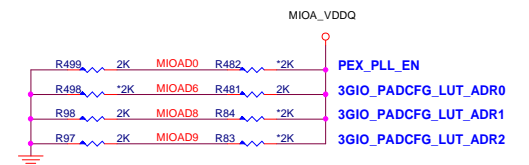
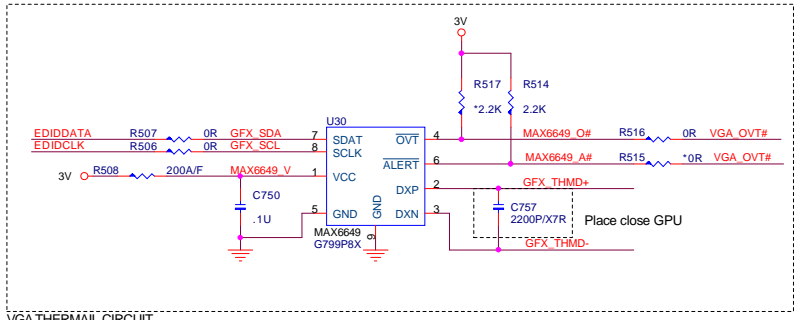
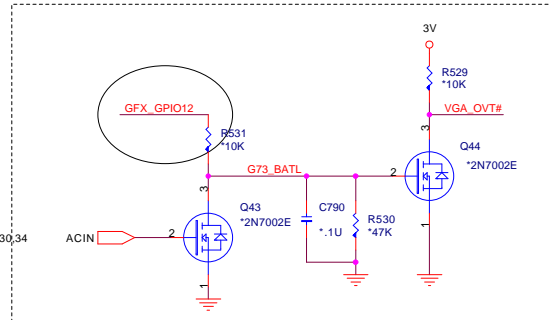
SUB_VENDOR
 SHARE M/B SYSTEM BIOS, SUB_VENDOR ID NEED PULL DOWN.

G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



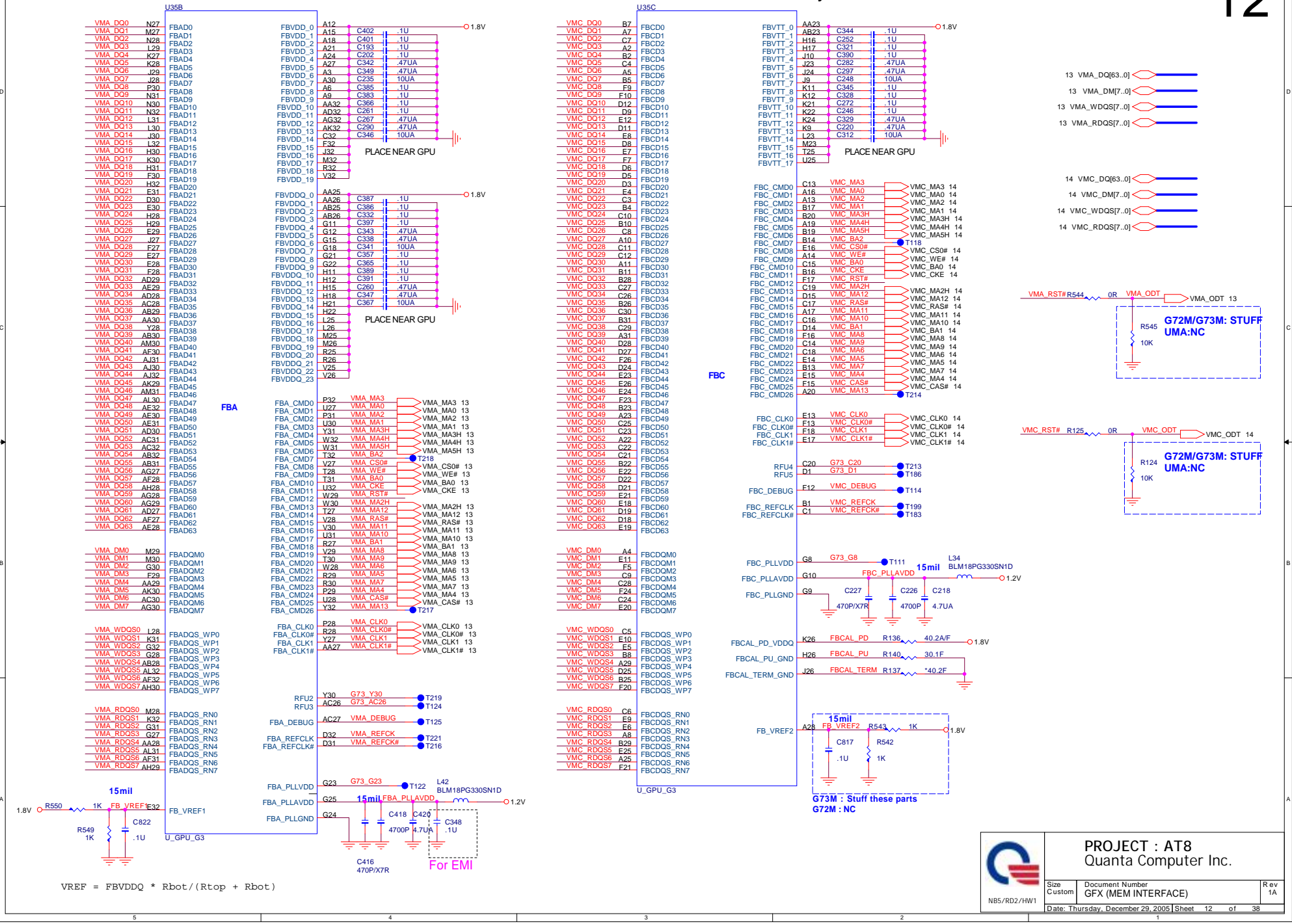
FOR BATTERY MODE FUNCTION
 GFX_GPIO12=H ENABLE
 GFX_GPIO12=L DISABLE

VGA THERMAL CIRCUIT

PROJECT : AT8
 Quanta Computer Inc.

Size Custom	Document Number GFX(ROM, GPIO, STRAP)	Rev 1A
Date: Thursday, December 29, 2005 Sheet 11 of 38		

Channel C is available on G73M only

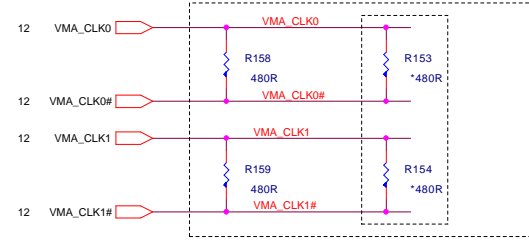
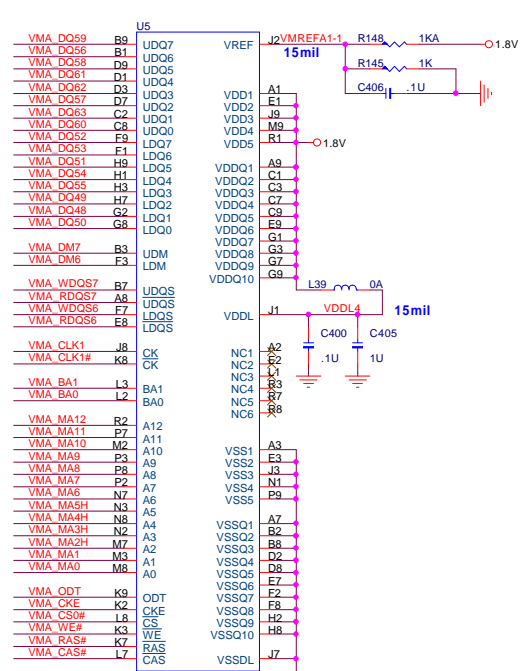
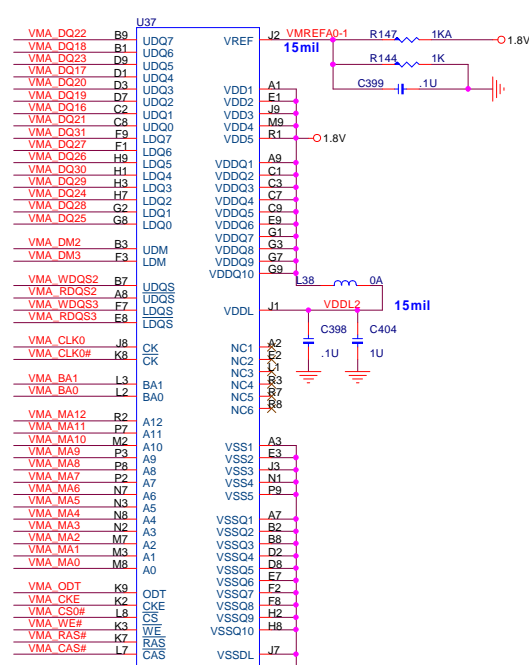
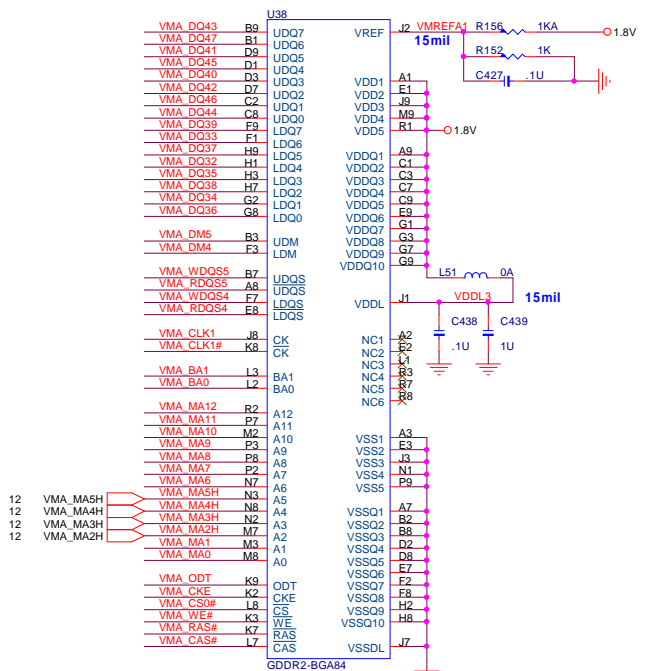
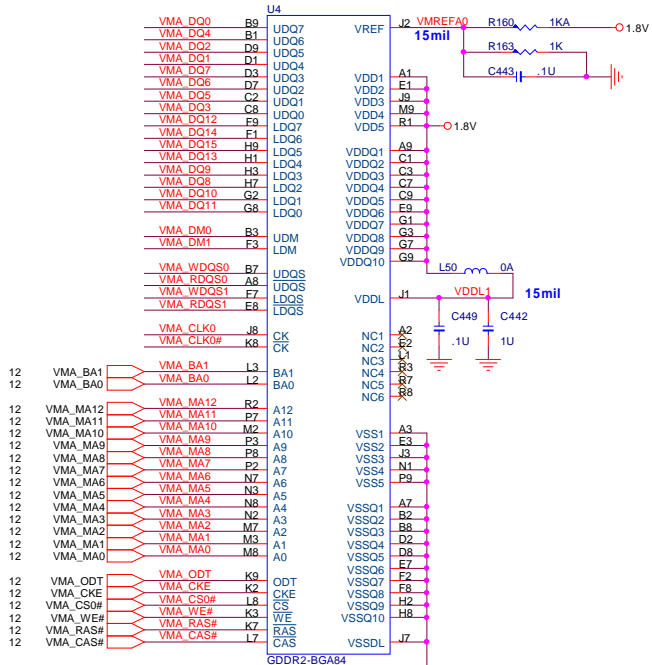


$VREF = FBVDDQ * Rbot / (Rtop + Rbot)$

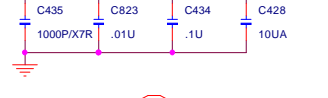
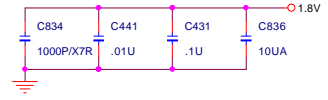
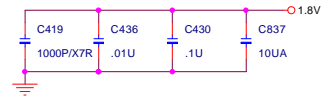
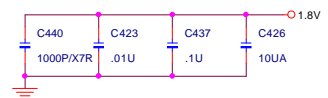
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number GFX (MEM INTERFACE)	Rev 1A
Date: Thursday, December 29, 2005 Sheet 12 of 38		

NB5/RD2/HW1




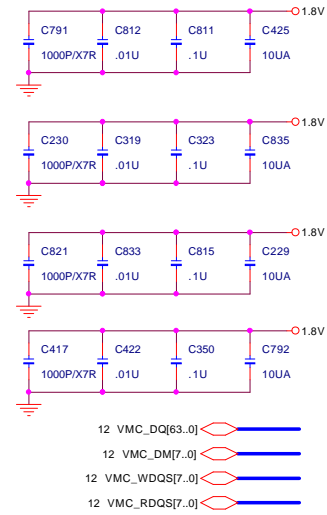
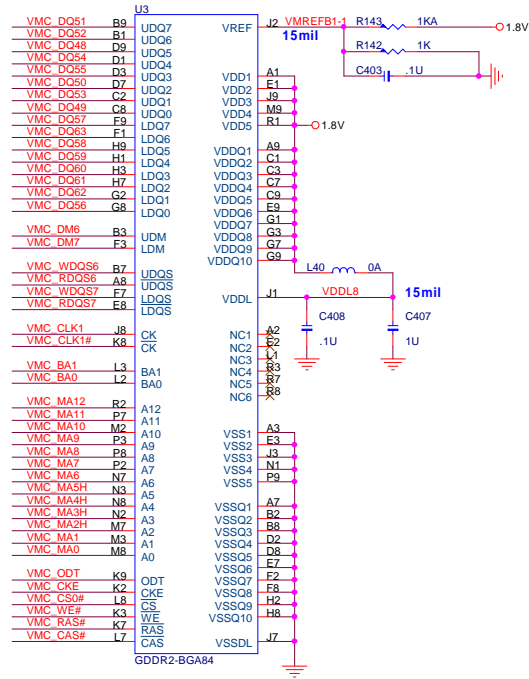
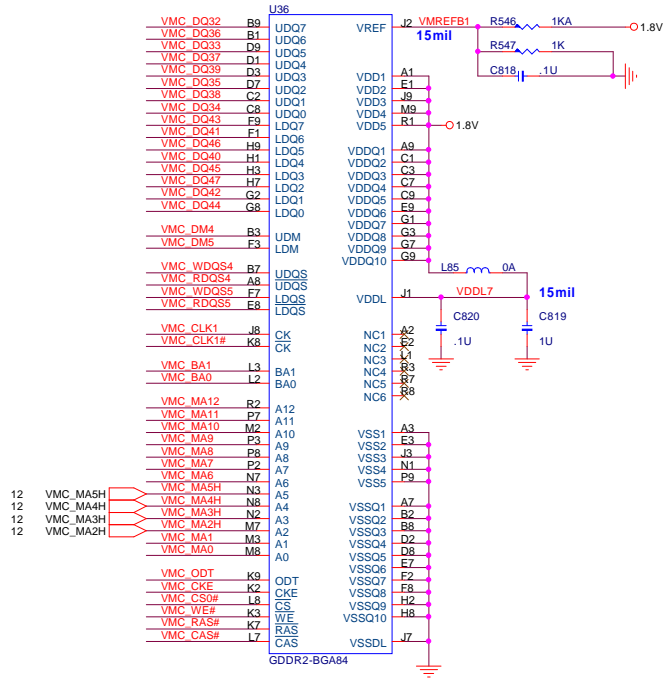
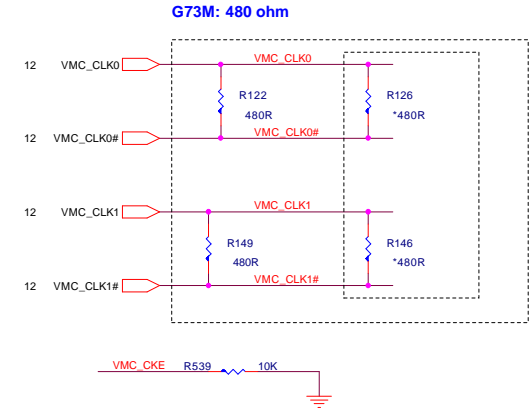
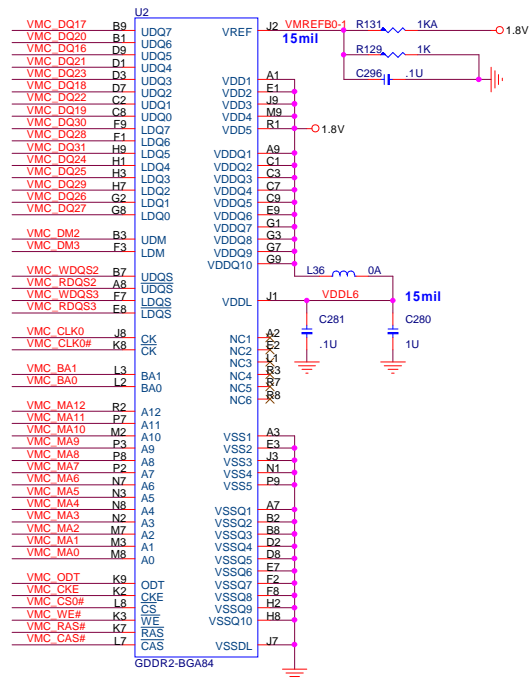
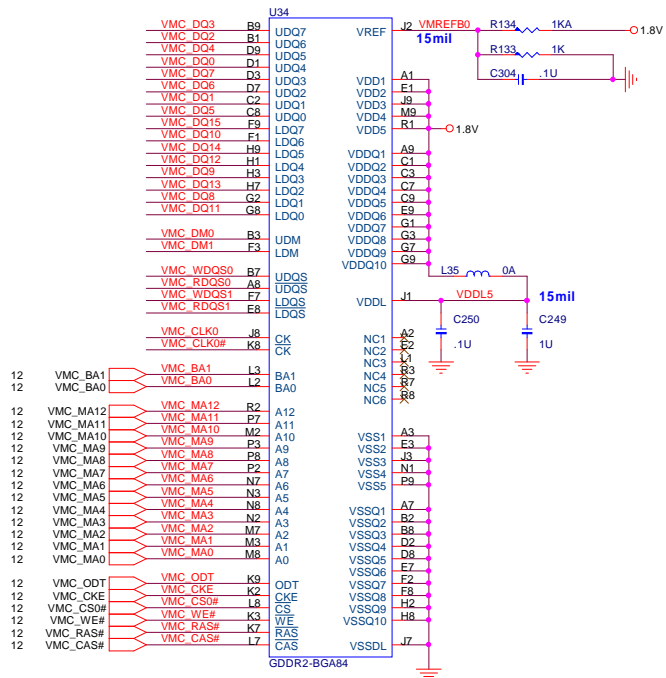
G72M: 120 ohm
G73M: 480 ohm



- 12 VMA_DQ[63..0]
- 12 VMA_DM[7..0]
- 12 VMA_WDQS[7..0]
- 12 VMA_RDQS[7..0]

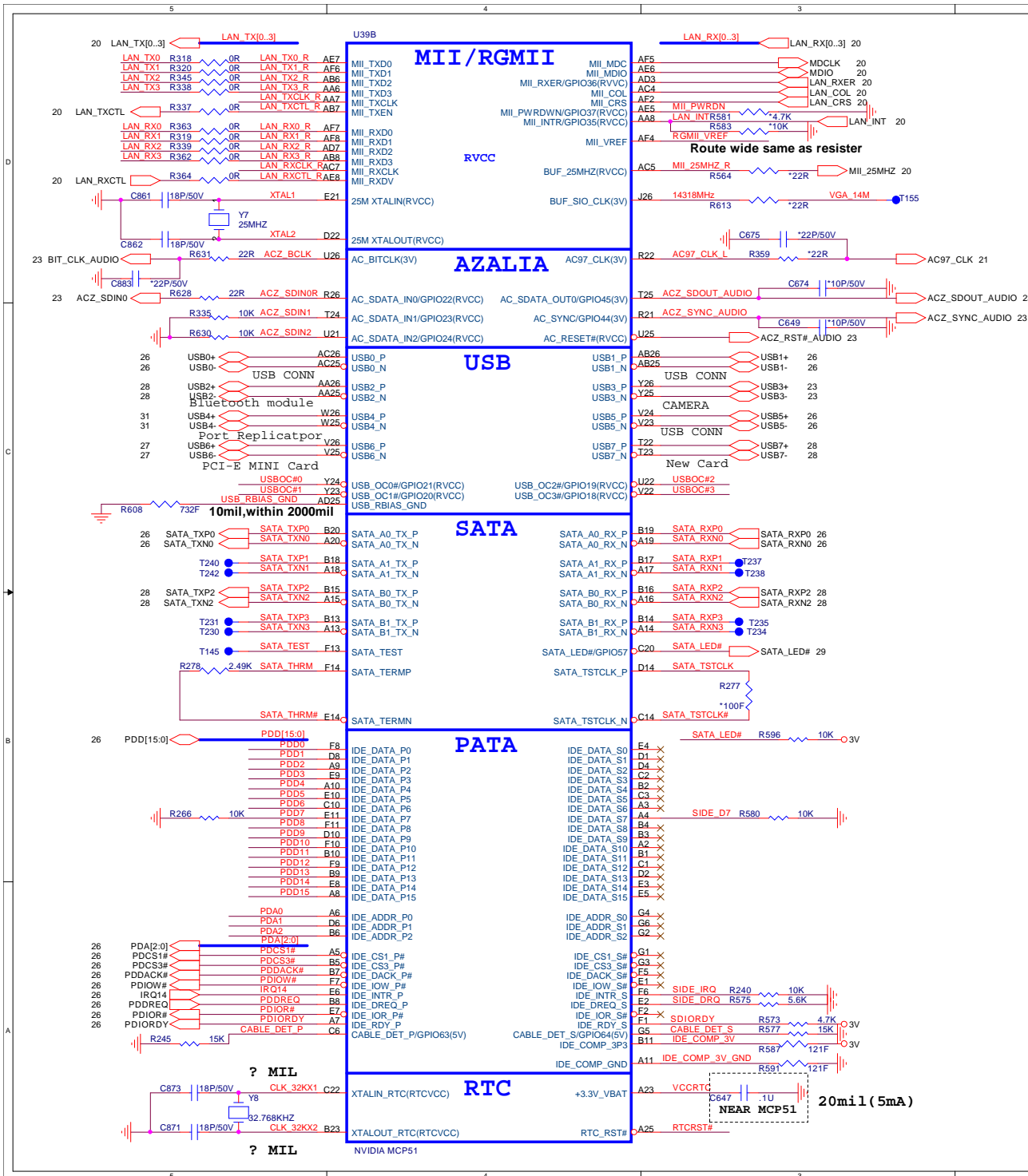
256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

 NB5/RDZ/HW1	PROJECT : AT8 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number VRAM-1 (GDDR2)	Date: Thursday, December 29, 2005



256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

	PROJECT : AT8 Quanta Computer Inc.		
	Size Custom	Document Number VRAM-2 (GDDR2)	Rev 1A
	Date: Thursday, December 29, 2005 Sheet 14 of 38		



10/100 - GIAG LAN STUFF OPTION

16

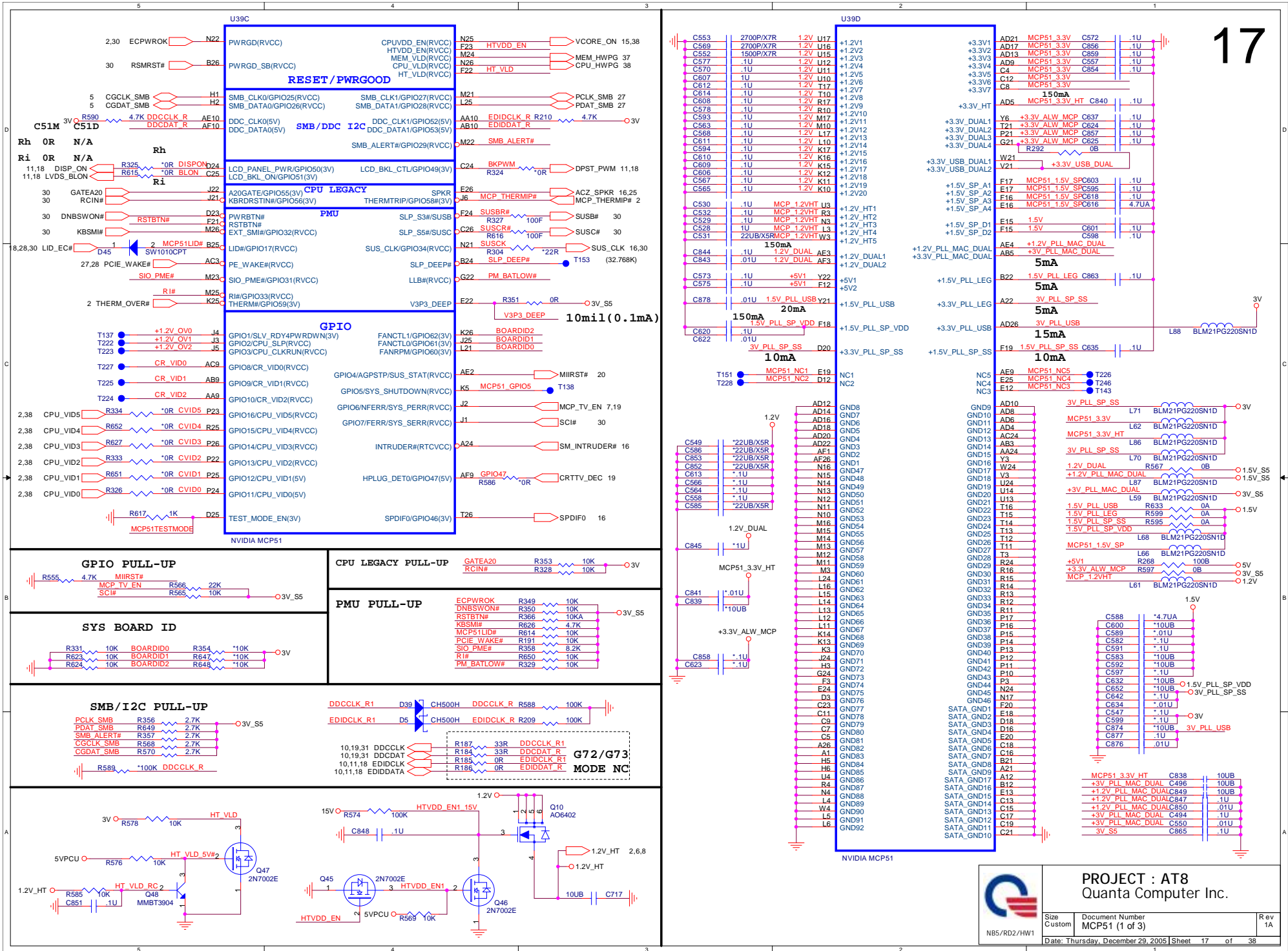
VREF	10/100	GIGA
Ra	1.25V	1.65V
Rb	2.43K/F	1K/F
Rc	1.47K/F	1K/F
Rd	0R	22R
Re	0R	0R
Rf	NC	0R
Rg	NC	0R

ACZ_SPKR STRAP (Boot MODE)	ACZ_RST# STRAP (LAN)
0 User Table	0 MII
1 Safe table	1 RGMII
*DEFAULT	*DEFAULT

SPDIF0 STRAP (SIO CLK)	SUSCLK STRAP (MCP MODE)
0 14.318MHZ	0 NORMAL
1 24.000MHZ	1 SLAVE
*DEFAULT	*DEFAULT

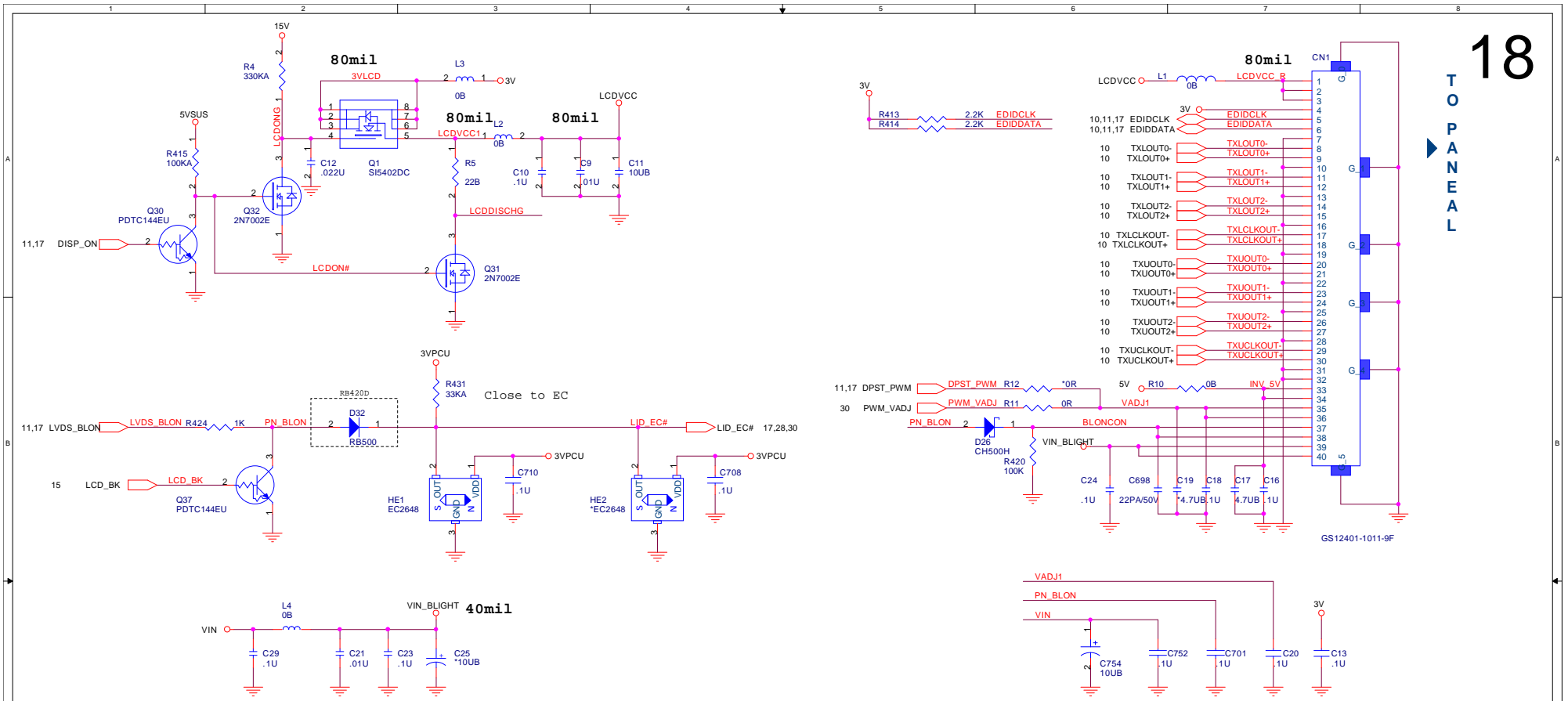
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number MCP51 (1 of 3)	Rev 1A
Date: Thursday, December 29, 2005		Sheet 16 of 38

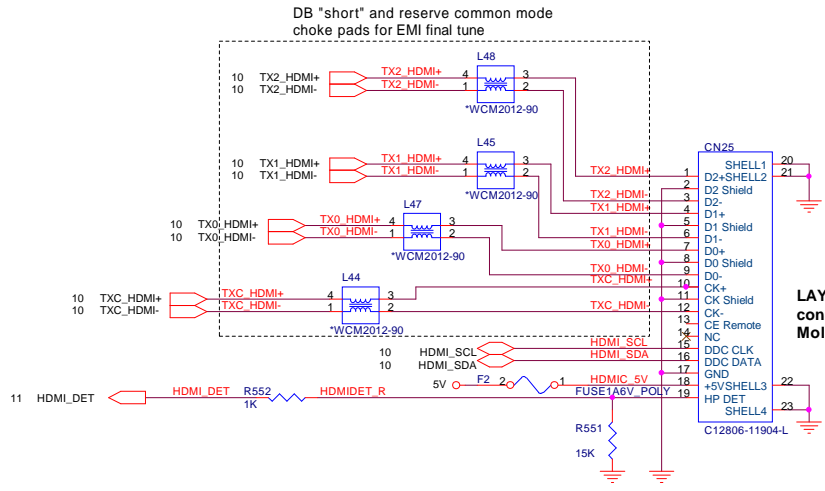


PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number MCP51 (1 of 3)	Rev 1A
Date: Thursday, December 29, 2005 Sheet 17 of 38		

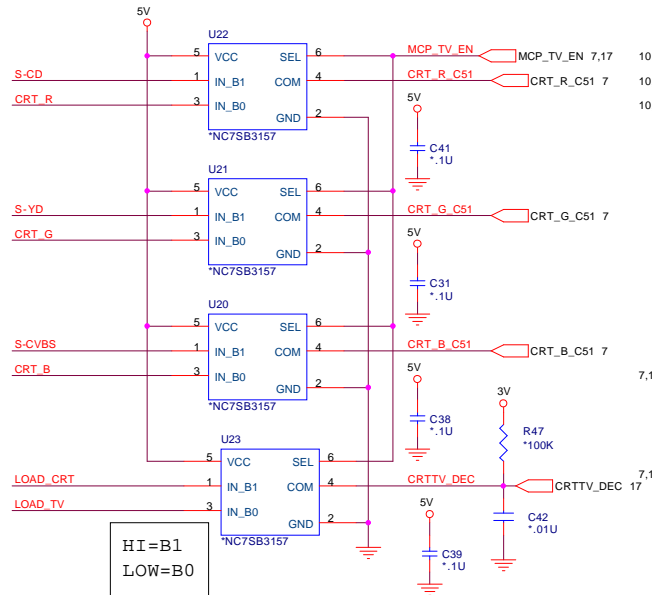


HDMI PORT

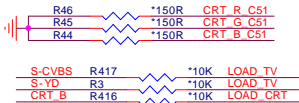


	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom	Document Number LCD CONN,HDMI CONN
Date: Thursday, December 29, 2005 Sheet 18 of 38		

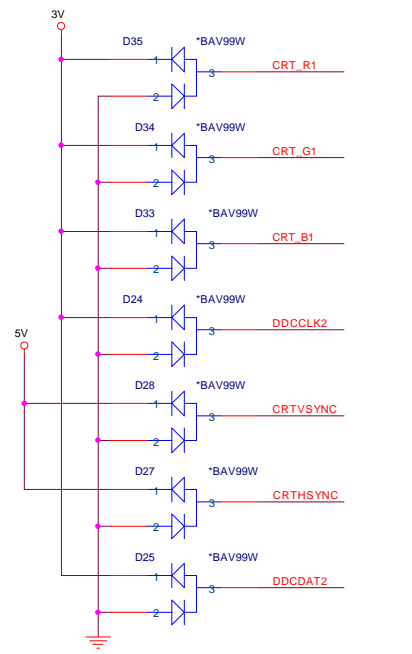
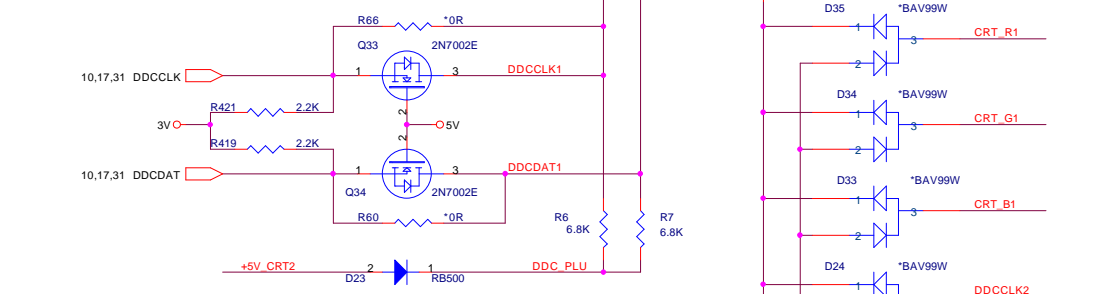
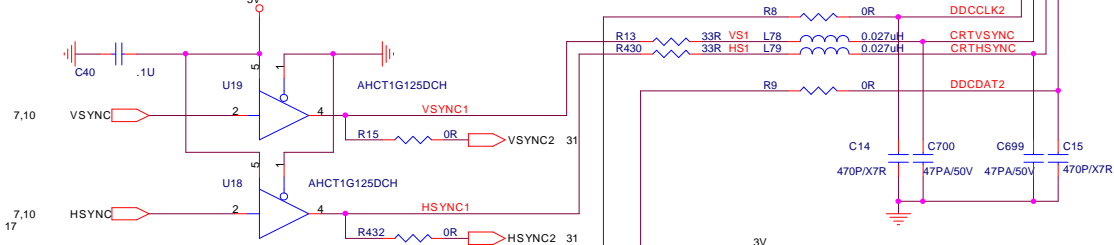
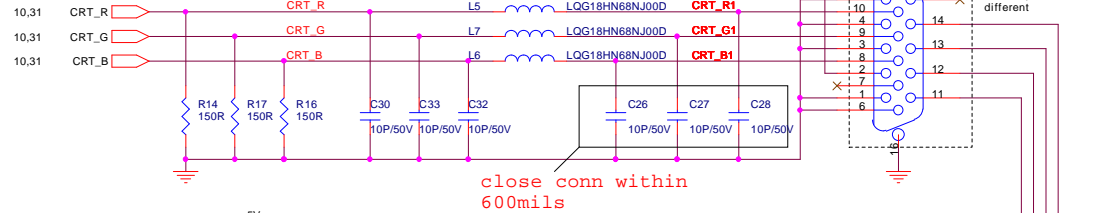
CRT PORT



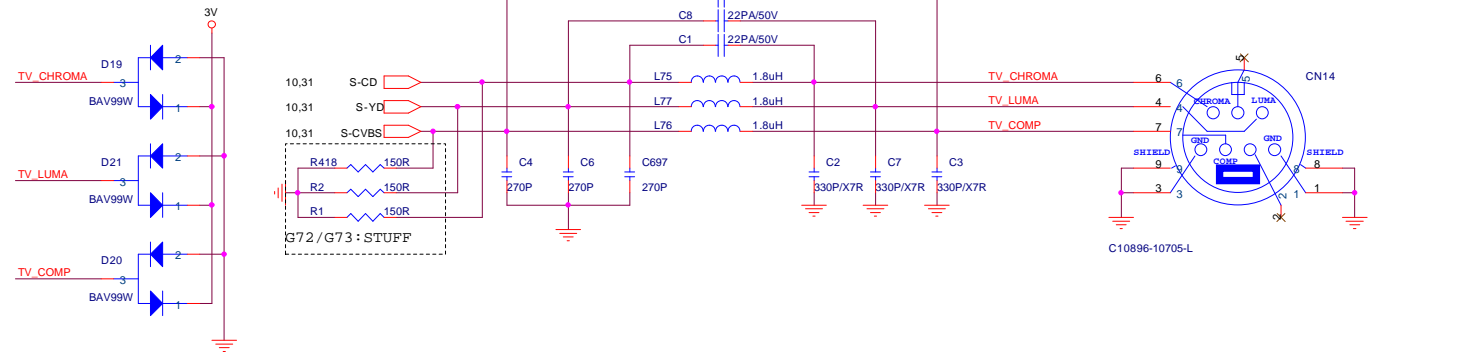
close within 600mils



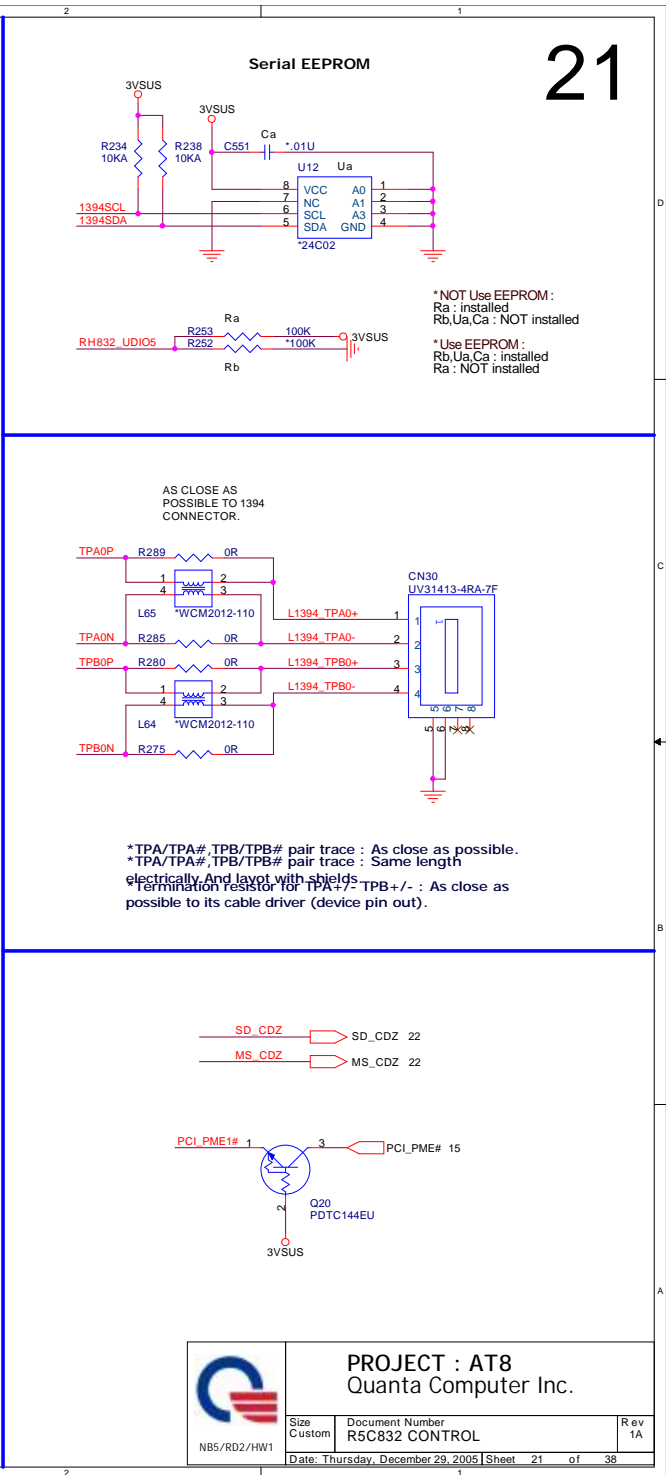
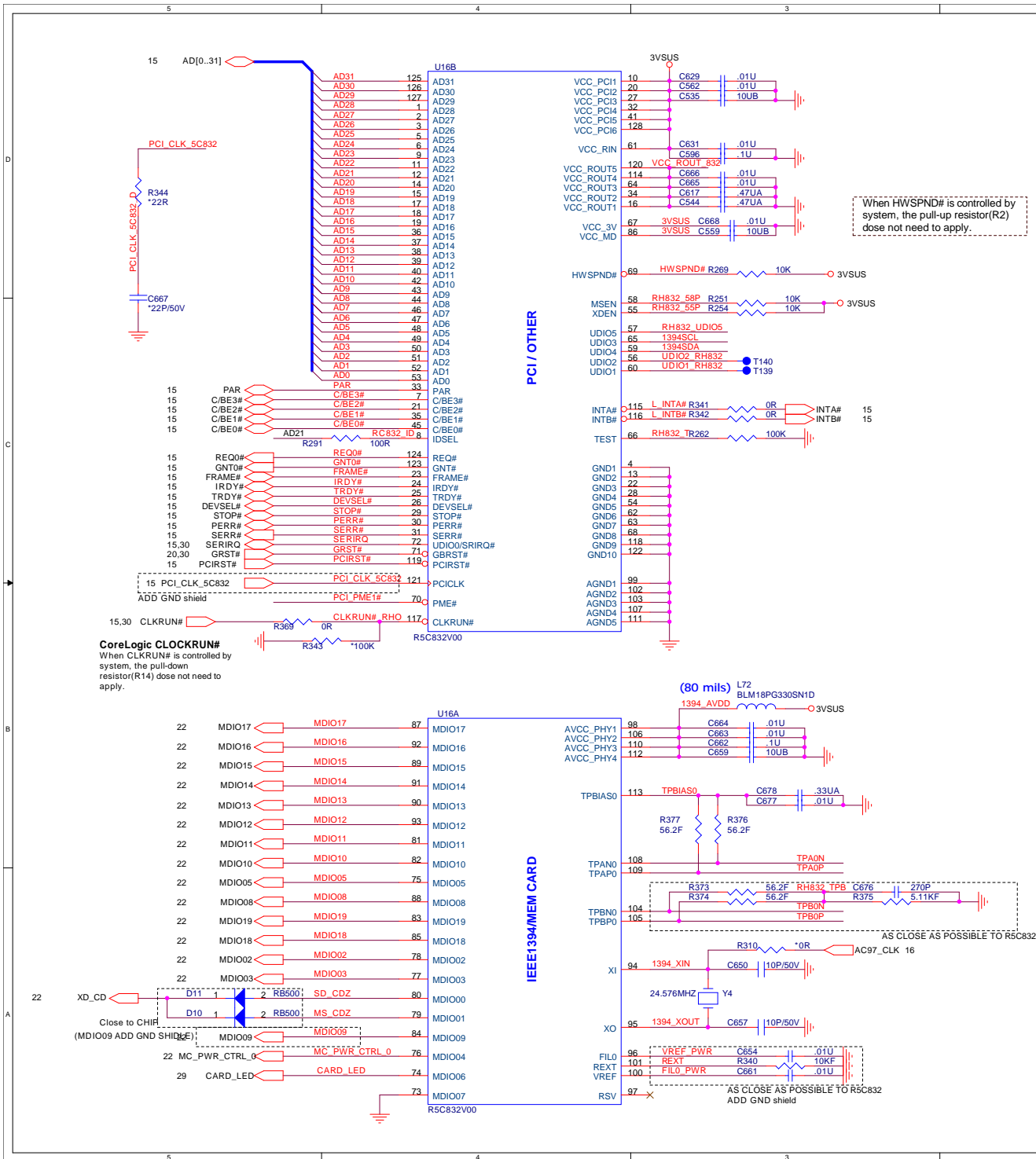
75-R as possible as closed to SB



TV_OUT

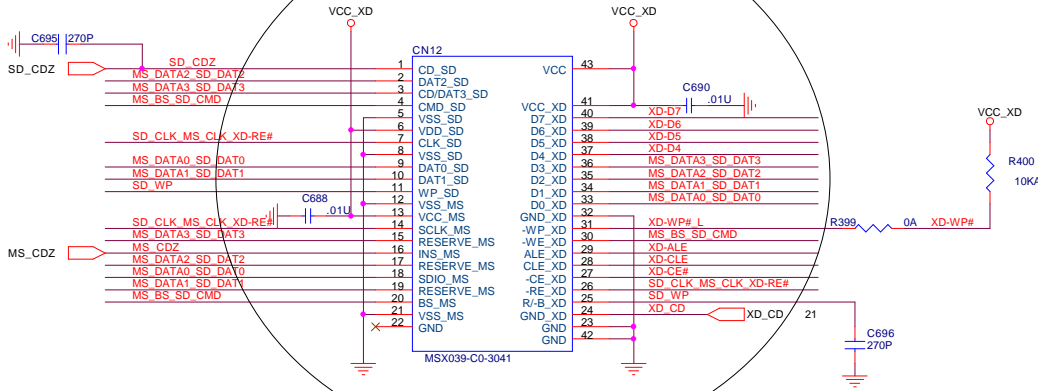


	PROJECT : AT8		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number CRT_TV_OUT	
Date: Thursday, December 29, 2005		Sheet 19 of 38	

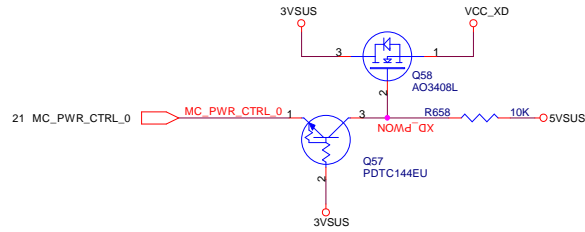
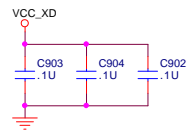
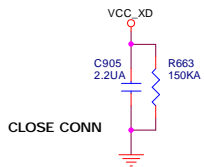


4 IN1 CARD READER
XD, MMC/SD, MS/MSP

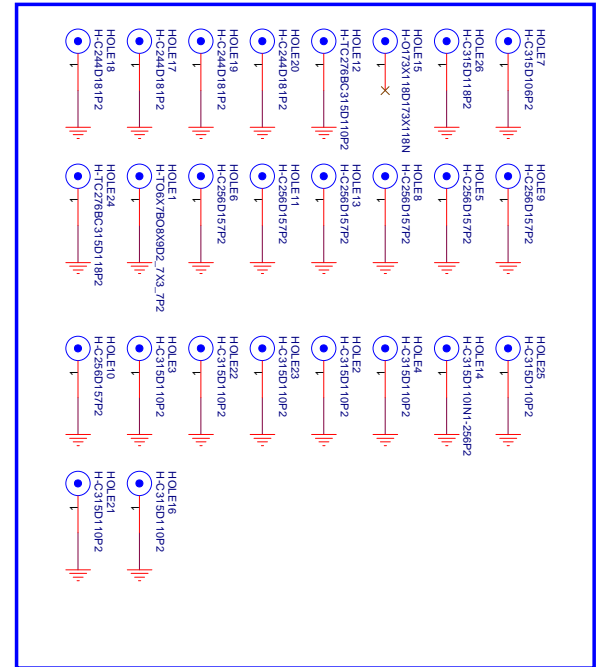
CHECK CONN.



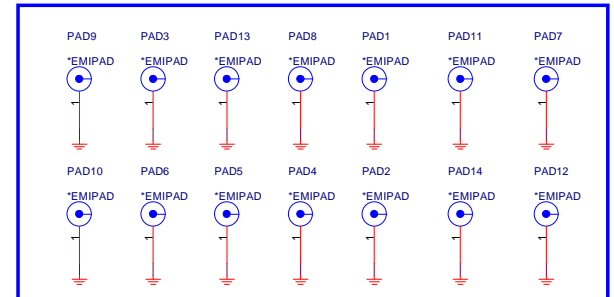
21	MDIO03	R398	56R	SD_WP
21	MDIO17	R409	56R	XD-D7
21	MDIO16	R408	56R	XD-D6
21	MDIO15	R407	56R	XD-D5
21	MDIO14	R406	56R	XD-D4
21	MDIO13	R405	56R	MS_DATA3 SD_DAT3
21	MDIO12	R404	56R	MS_DATA2 SD_DAT2
21	MDIO11	R403	56R	MS_DATA1 SD_DAT1
21	MDIO10	R402	56R	MS_DATA0 SD_DAT0
21	MDIO08	R397	56R	MS_BS SD_CMD
21	MDIO05	R401	56R	XD-WP#
21	MDIO19	R396	56R	XD-ALE
21	MDIO18	R395	56R	XD-CLE
21	MDIO02	R394	56R	XD-CE#
21	MDIO09	R393	56R	SD_CLK MS_CLK XD-RE#



SCREW HOLE



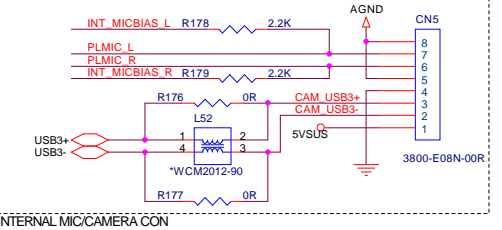
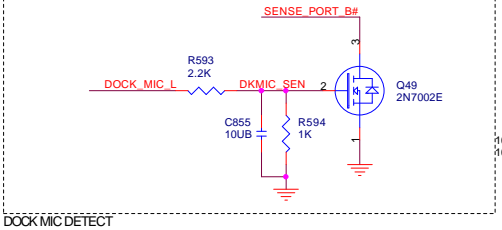
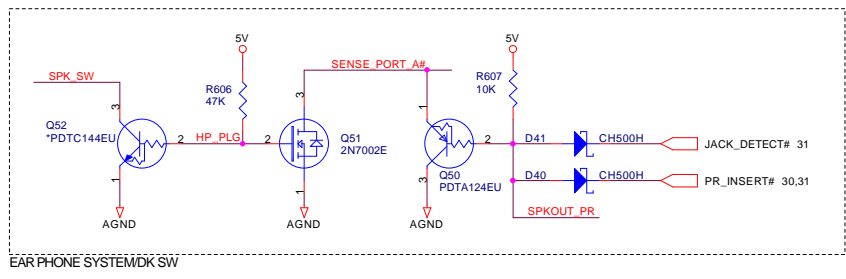
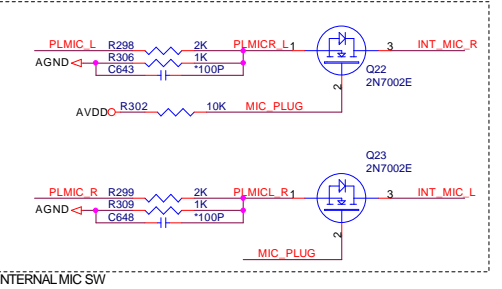
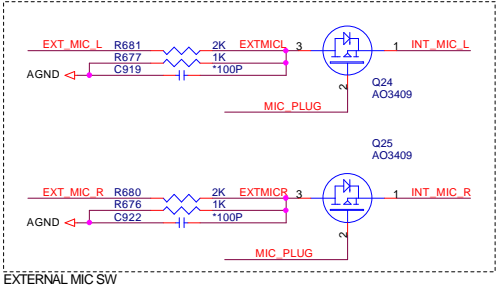
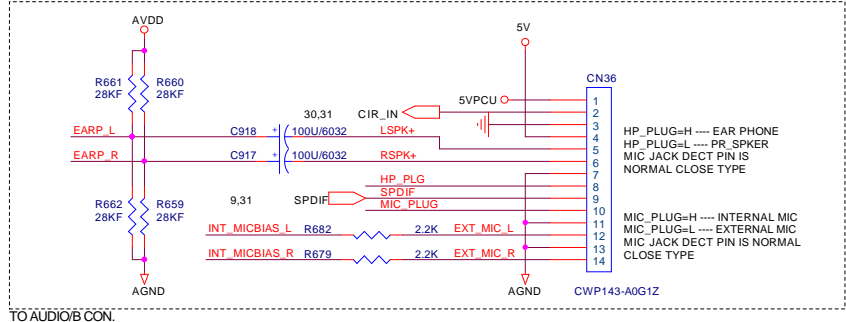
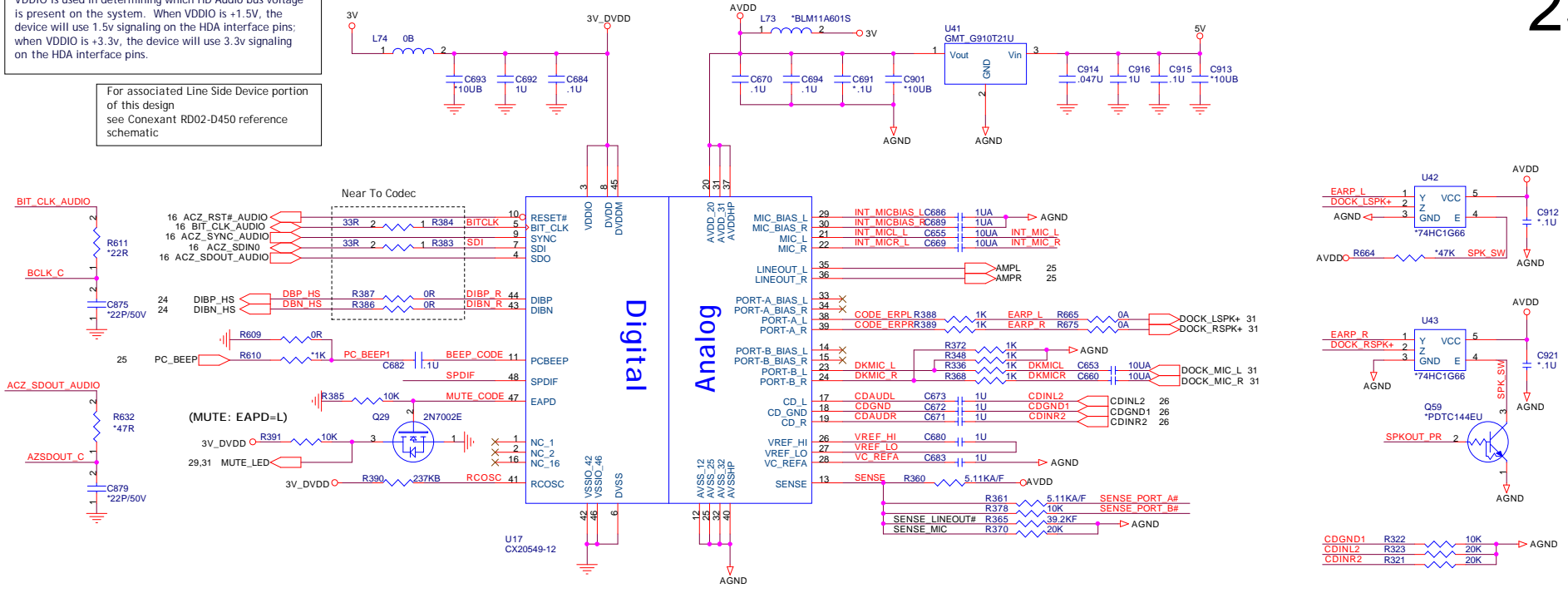
EMI PAD



	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom	Document Number CARD READER CONN
NB5/RD2/HW1	Date: Thursday, December 29, 2005	Sheet 22 of 38
		Rev 1A

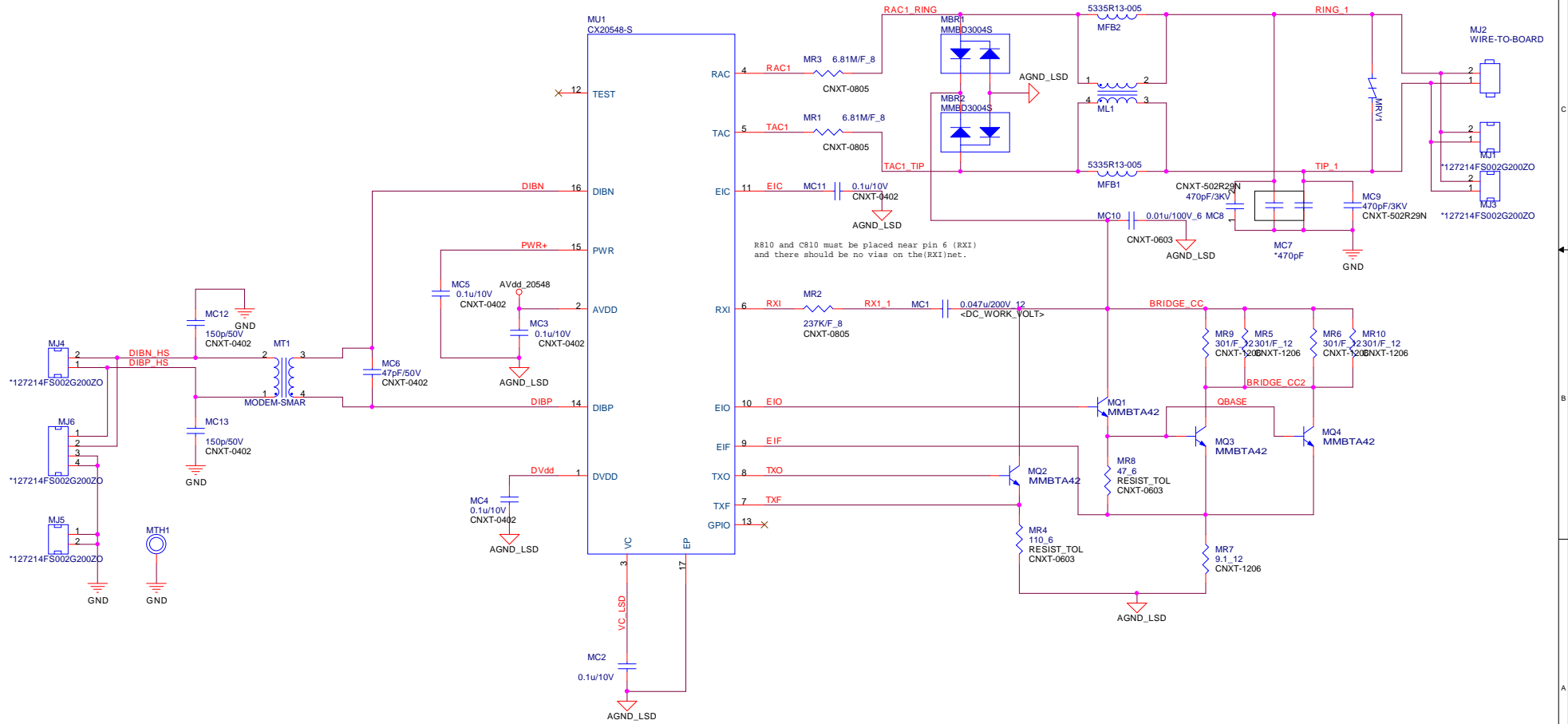
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

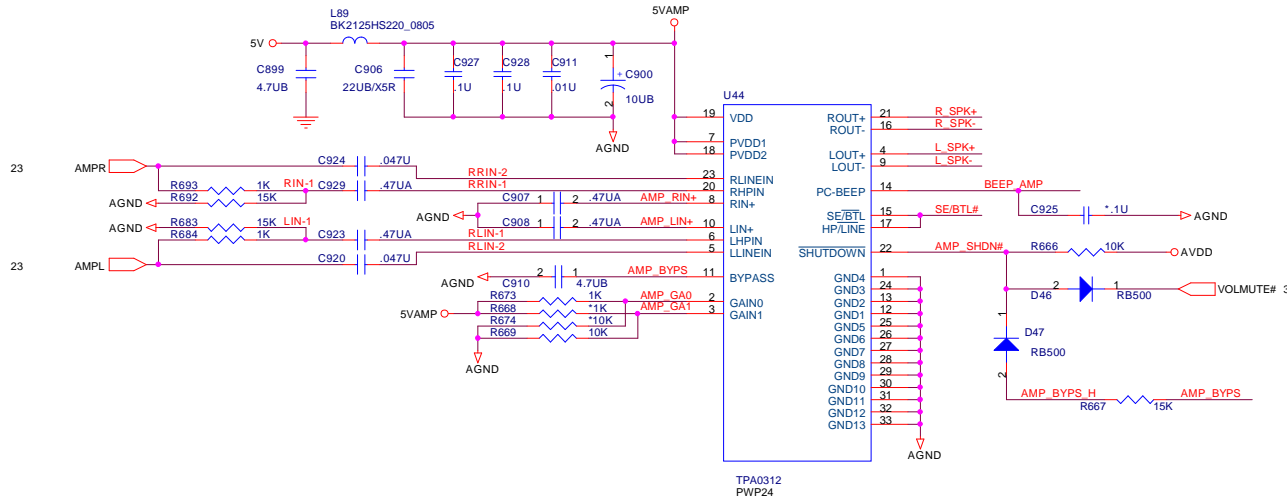


	PROJECT : AT8	
	Quanta Computer Inc.	
	Size Custom Document Number Azalia CTRL_CONEXANT20549-12 Date: Thursday, December 29, 2005	Sheet 23 of 38

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

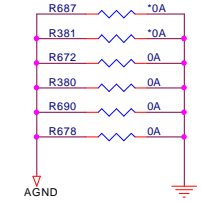


	PROJECT : AT8 Quantia Computer Inc.	
	Size Custom Document Number MODEM (DAA)	Rev 1A Date: Thursday, December 29, 2005 Sheet 24 of 38

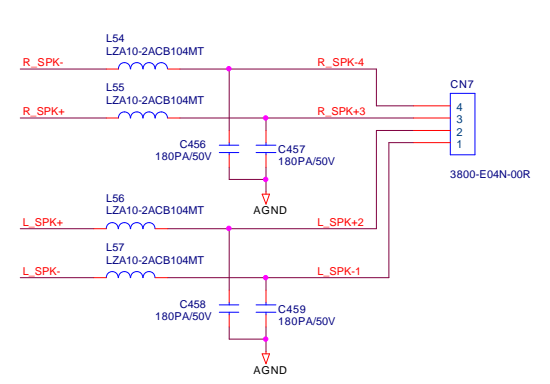


0312 Gain Table

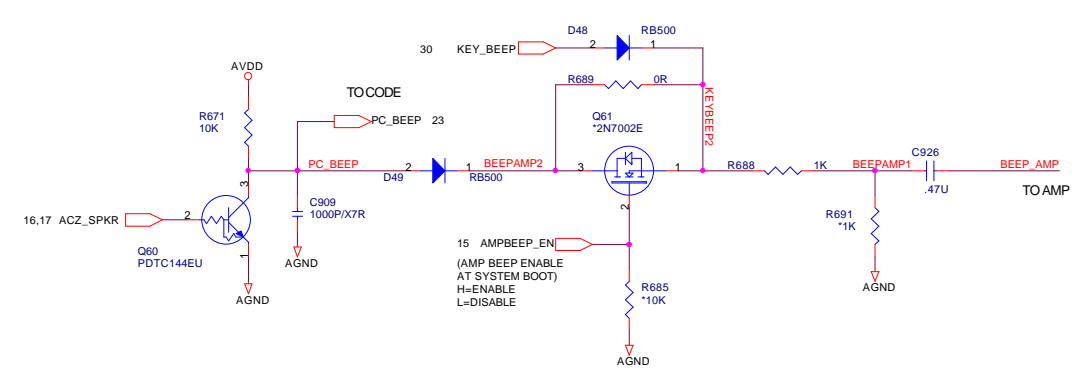
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER

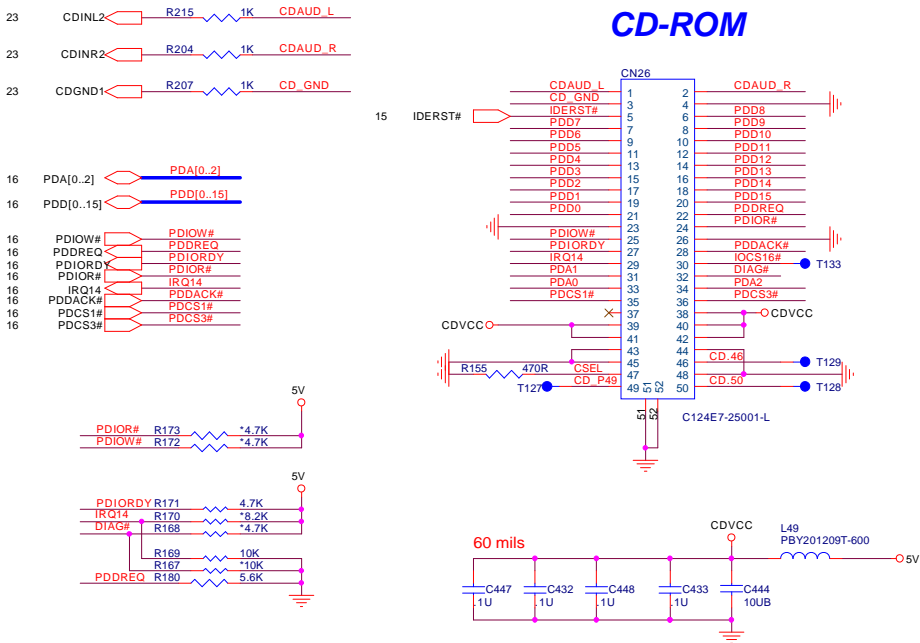


PCSPK BEEP

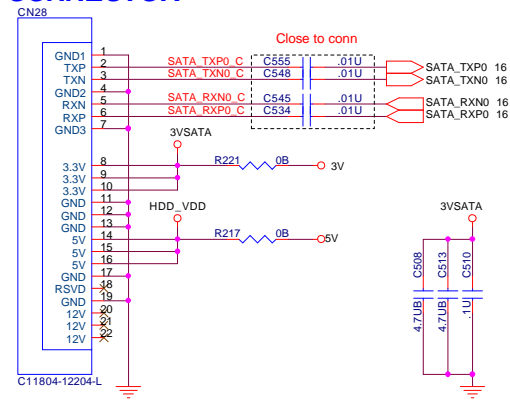


PROJECT : AT8
Quanta Computer Inc.

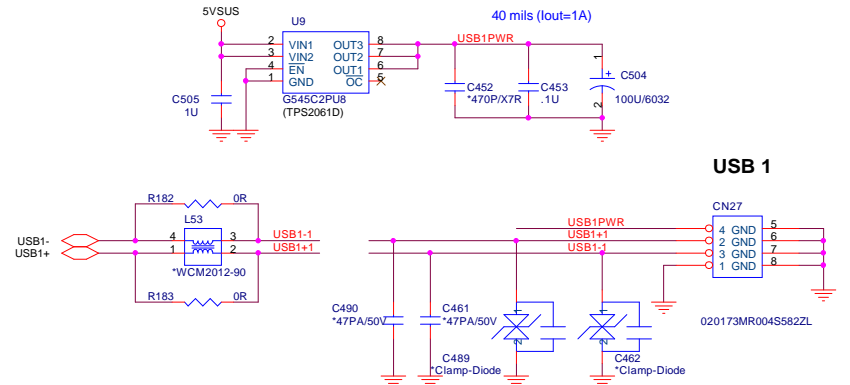
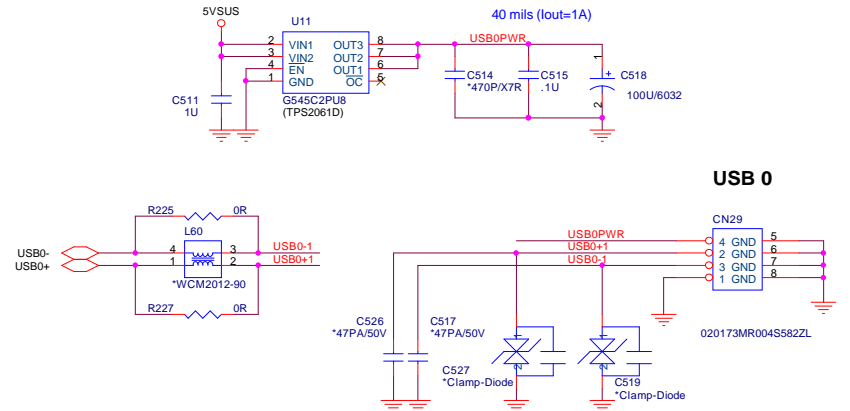
Size Custom	Document Number JACK, AMP_TPA0312	Rev 1A
Date: Thursday, December 29, 2005 Sheet 25 of 38		



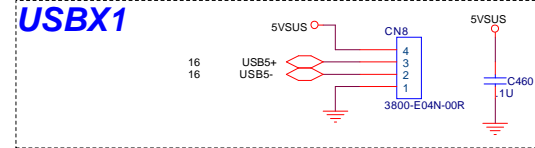
SATA 1 CONNECTOR




USBX2



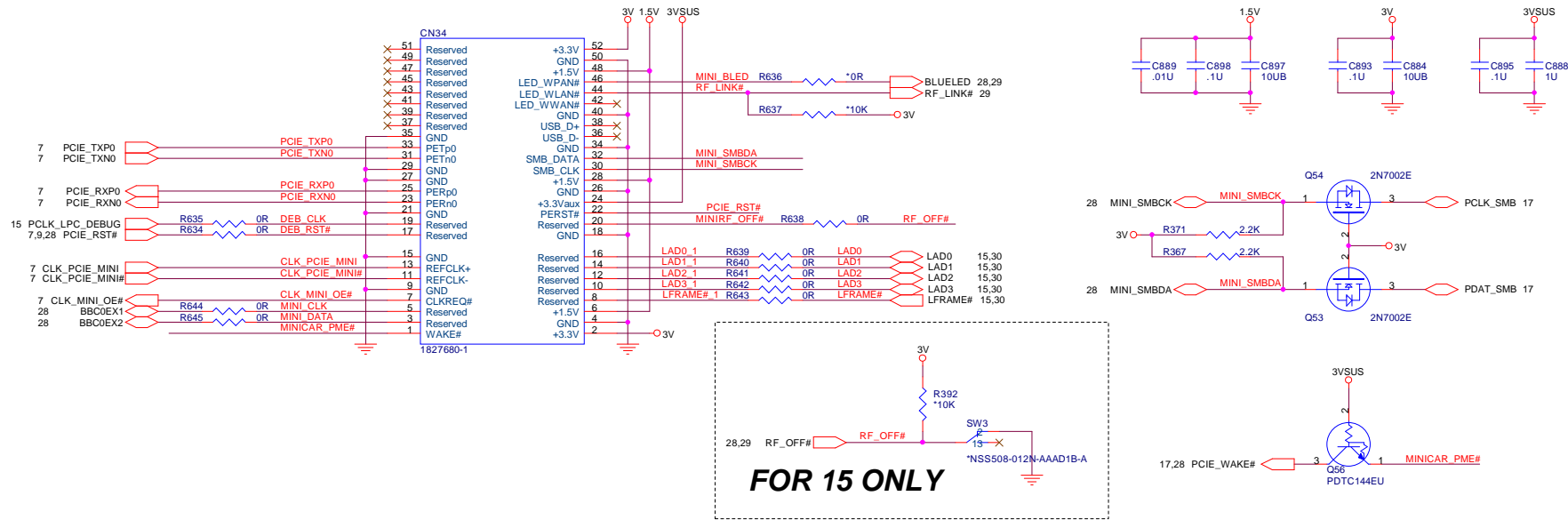
USBX1



TO AD/B

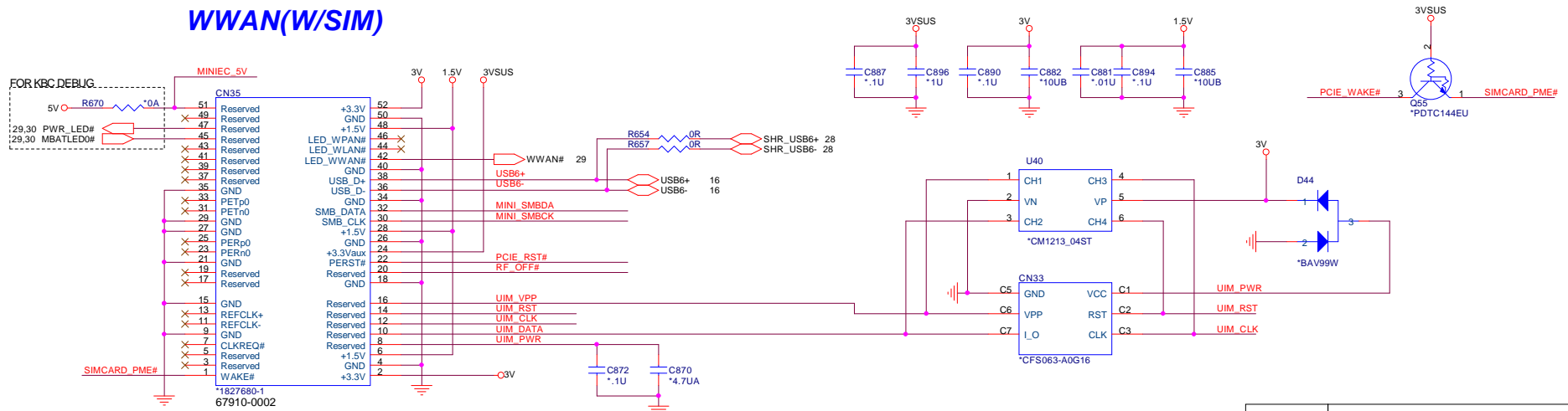
 NB5/RD2/HW1	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Document Number SATA HDD, CD-ROM, USBX2	Date: Thursday, December 29, 2005 Sheet 26 of 38


Mini PCI-E Card 1 WLAN



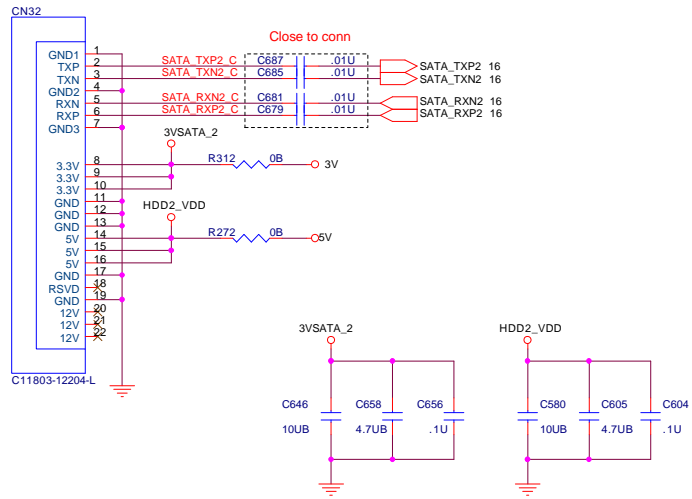
Mini PCI-E Card 2 WWAN(W/SIM)

FOR 15 ONLY

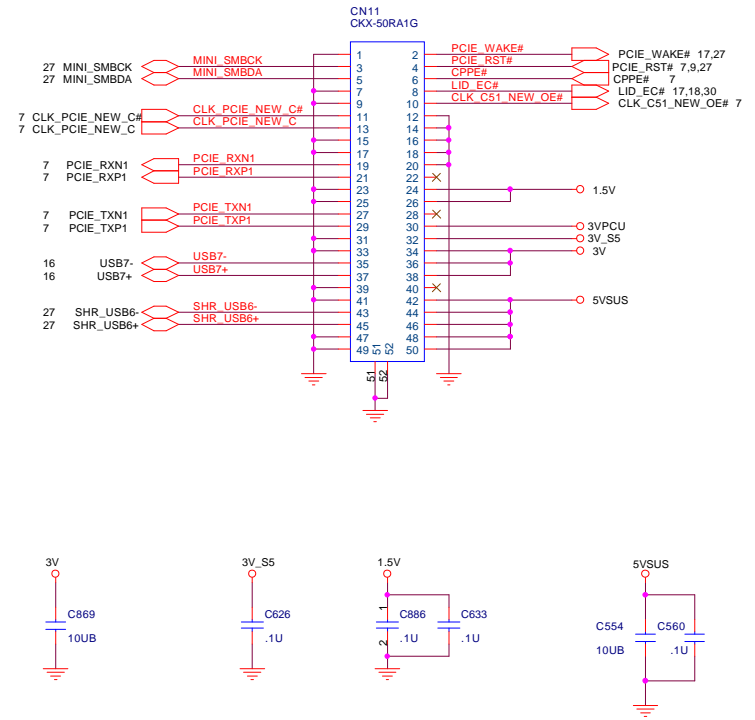


 NB5/RD2/HW1	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Date: Thursday, December 29, 2005	Document Number MINI CARD Sheet 27 of 38

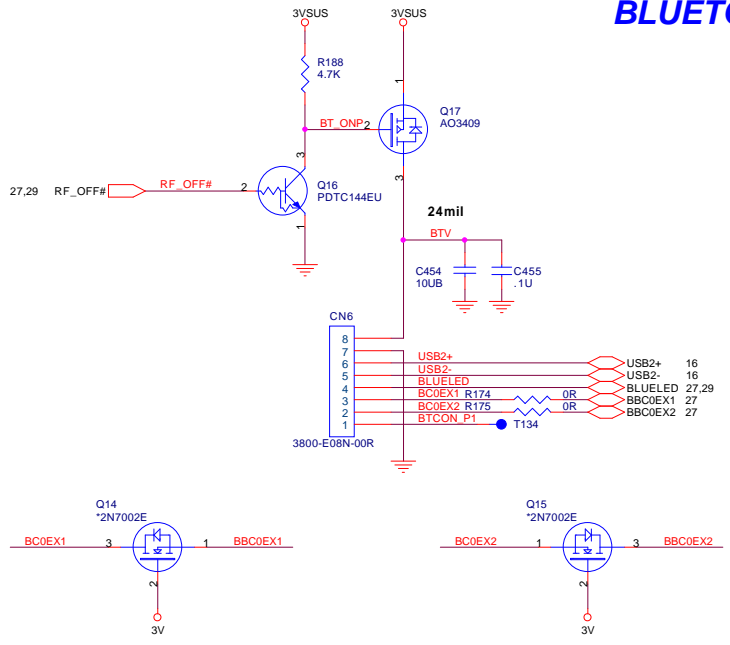
SATA_2 CONNECTOR For 17"W Second HDD



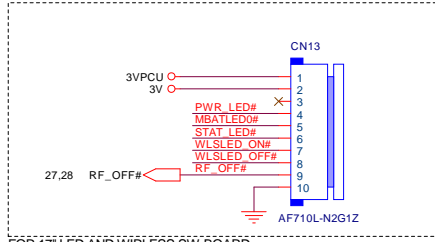
NEWCARD



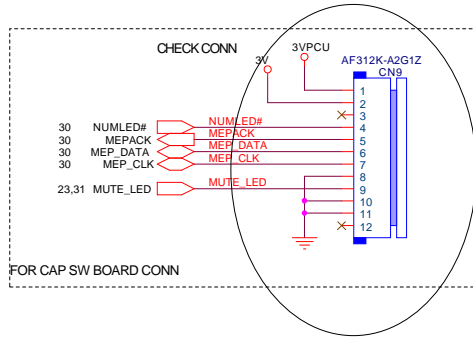
BLUETOOTH



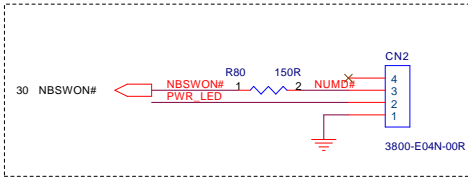
	PROJECT : AT8 Quantia Computer Inc.	
	Size Custom Document Number NEW CARD/BT Date: Thursday, December 29, 2005	Rev 1A Sheet 28 of 38



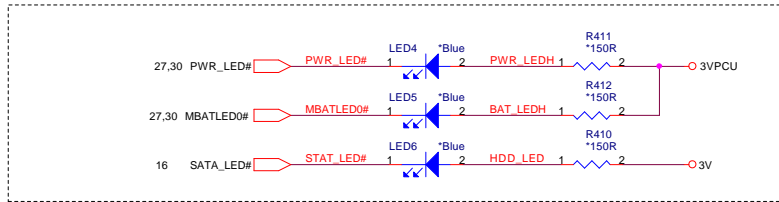
FOR 17" LED AND WIRLESS SW BOARD



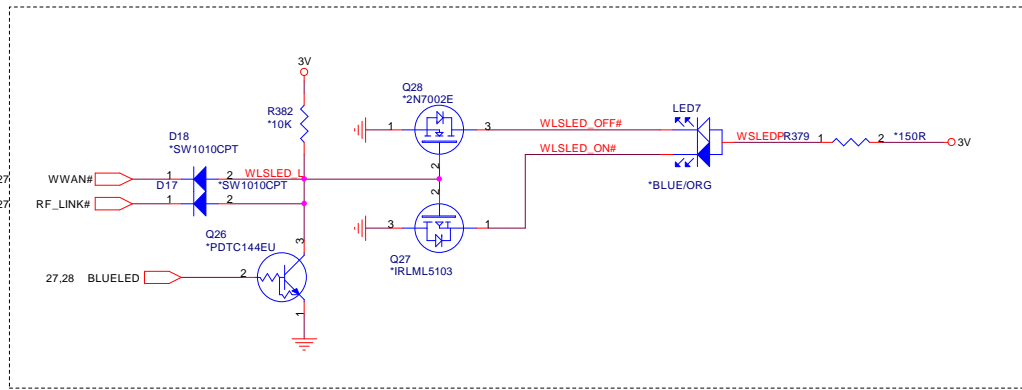
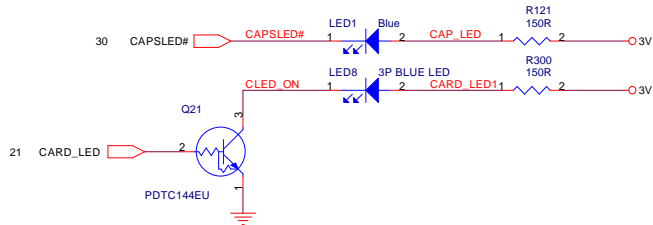
FOR CAP SW BOARD CONN



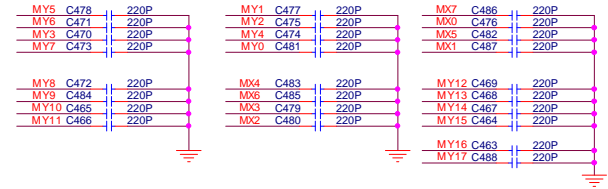
FOR POWER ON SW BOARD



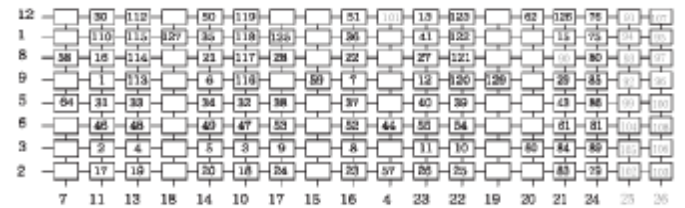
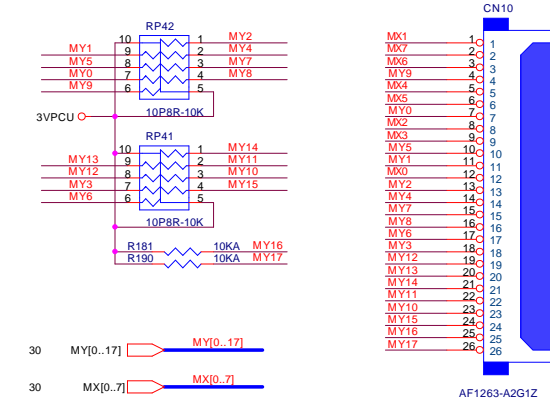
FOR 15.4" LED




FOR WIRELESS LED



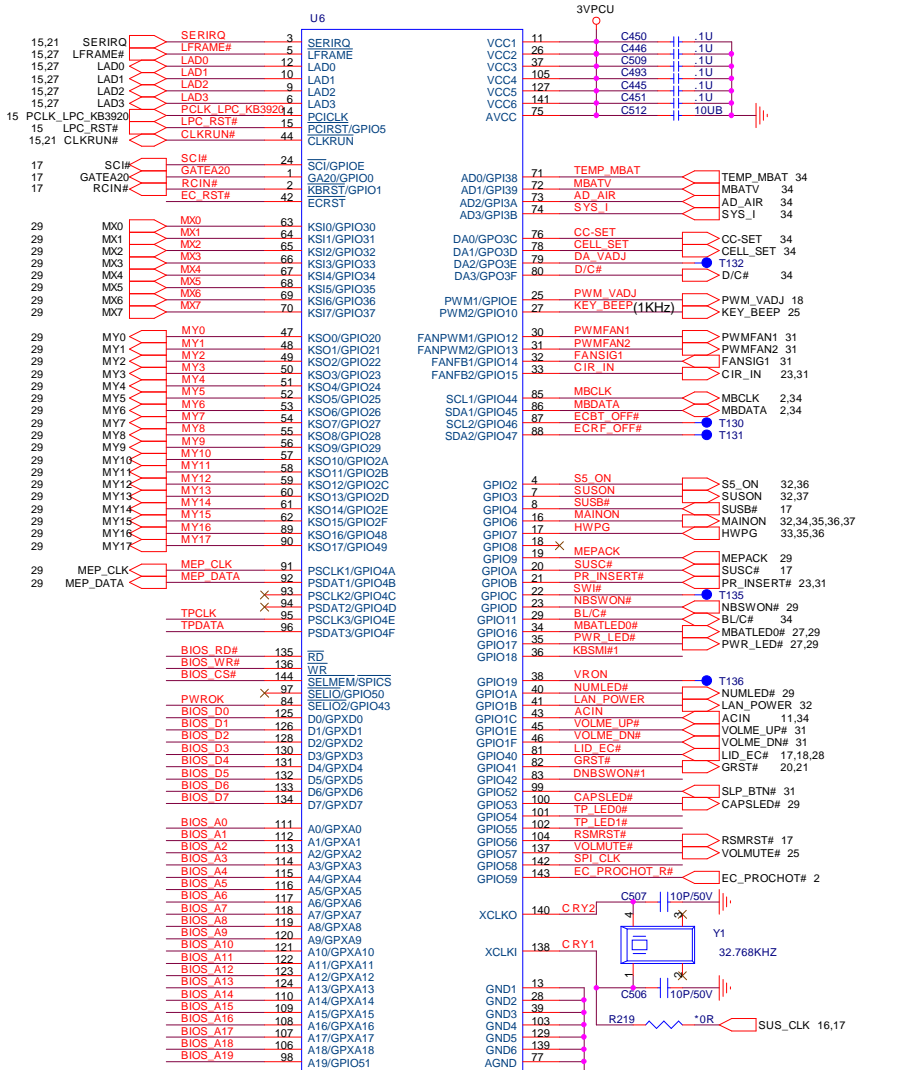
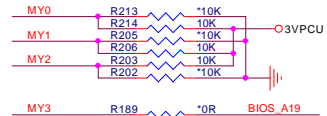
KEYBOARD PULL-UP



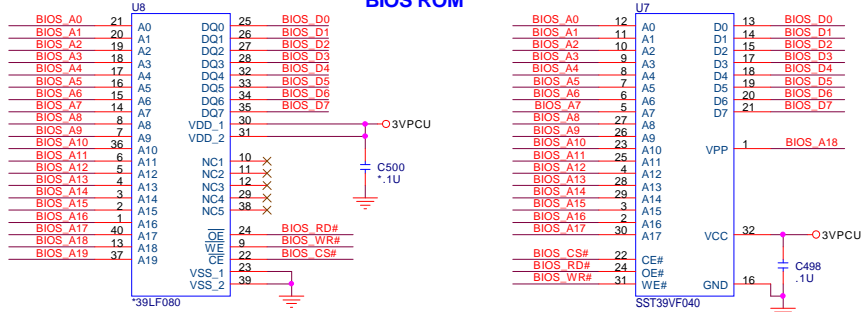
 <p>NB5/RD2/HW1</p>	<p>PROJECT : AT8 Quanta Computer Inc.</p>	
	<p>Size Custom</p>	<p>Document Number LED/KEYBOARD/TP</p>
<p>Date: Thursday, December 29, 2005 Sheet 29 of 38</p>		

STRAP PIN

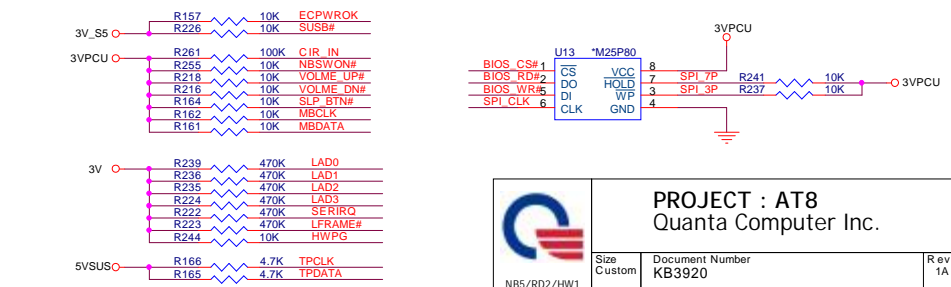
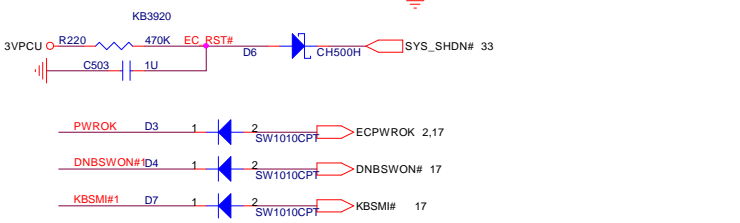
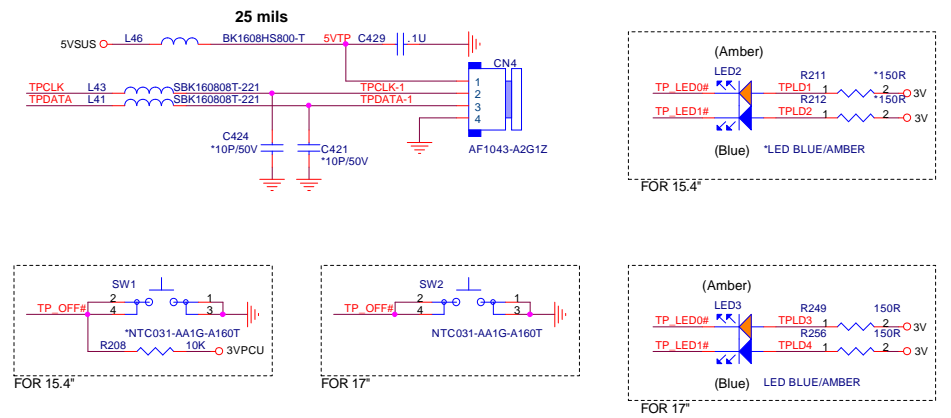
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 329KHz clock in normal running
MY1	48	TP_PLL: DRLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISH flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



BIOS ROM



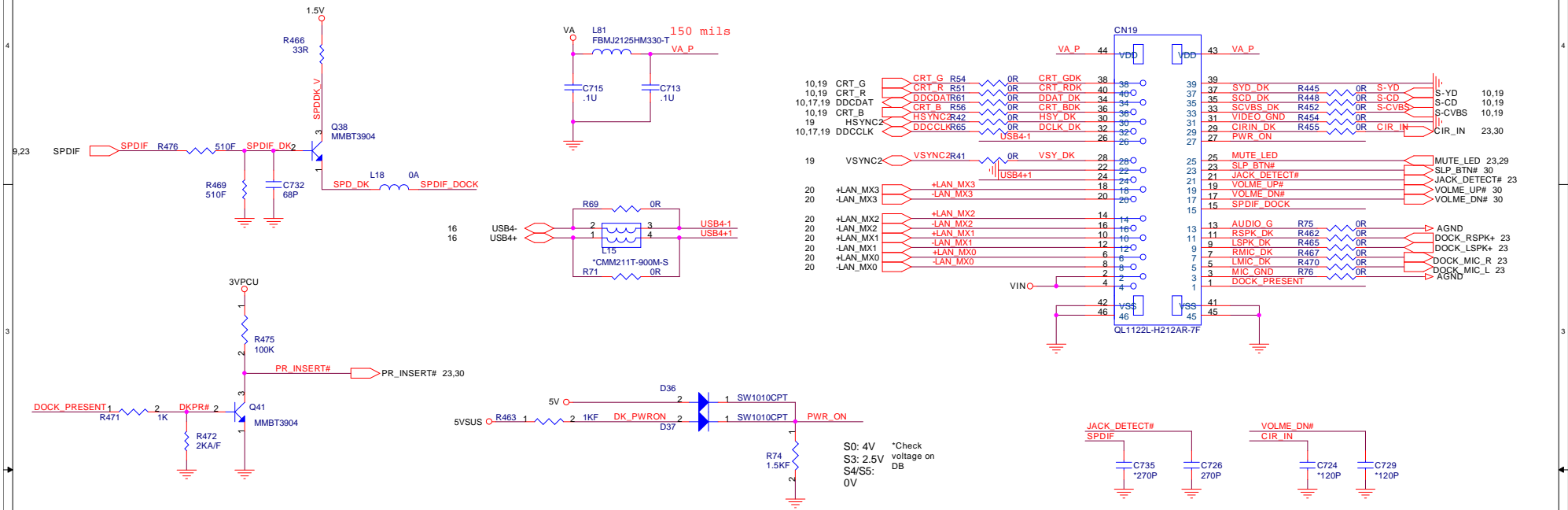
TOUCH PAD CONNECTOR



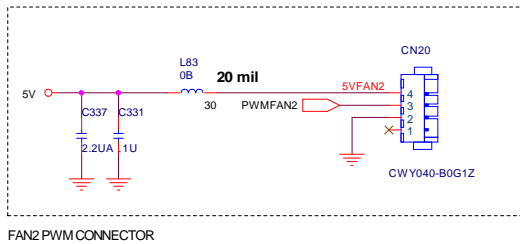
PROJECT : AT8
Quanta Computer Inc.

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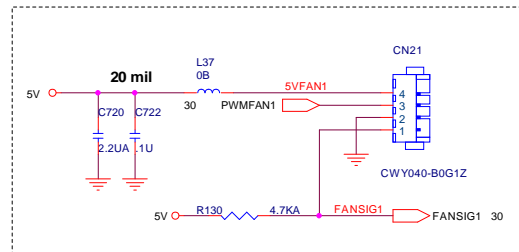
CABLE DOCK




FAN



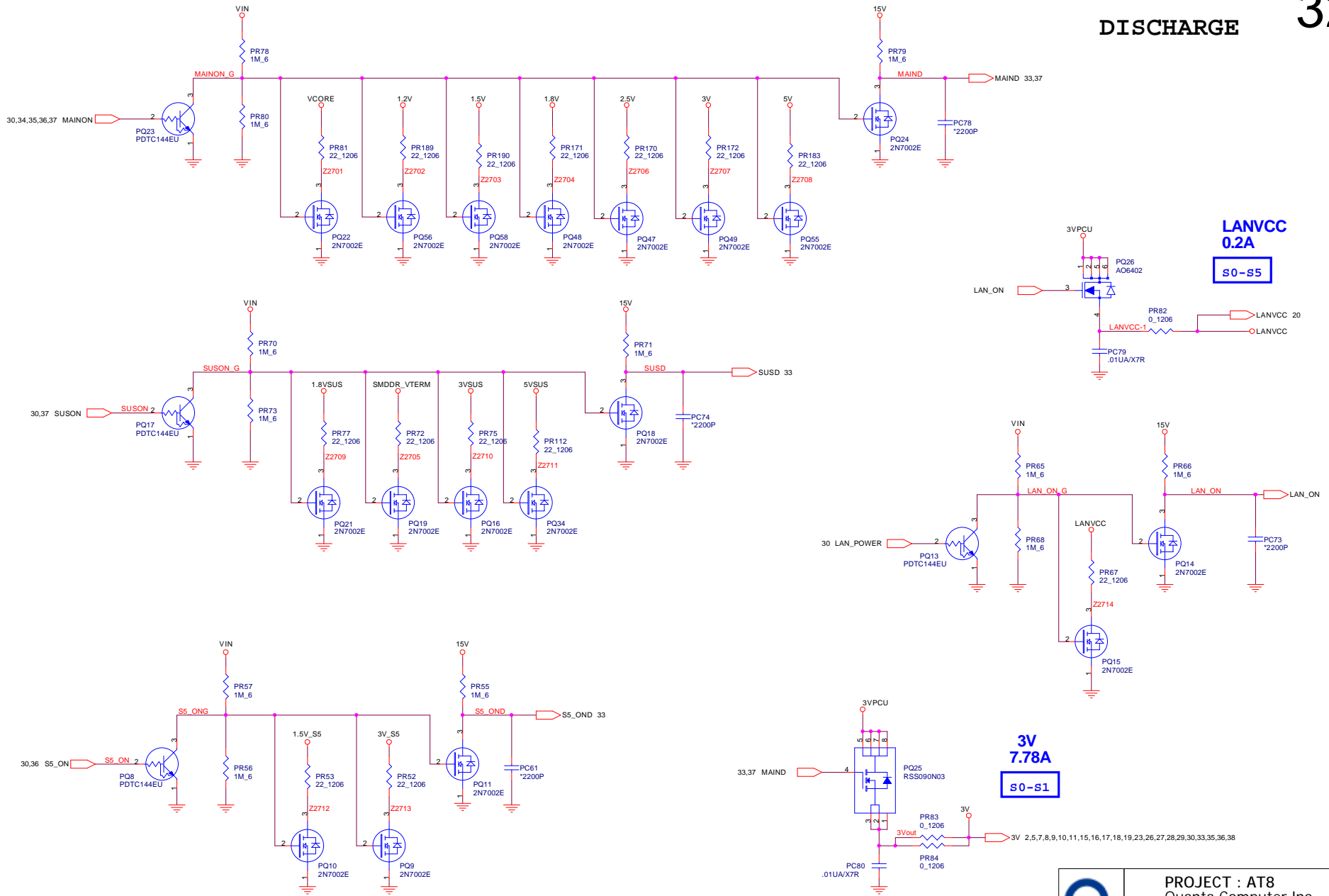
FAN2 PWM CONNECTOR




FAN1 PWM CONNECTOR

 NB5/RDZ/HW1	PROJECT : AT8 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number CABLE DOCKING	
	Date: Thursday, December 29, 2005 Sheet 31 of 38		

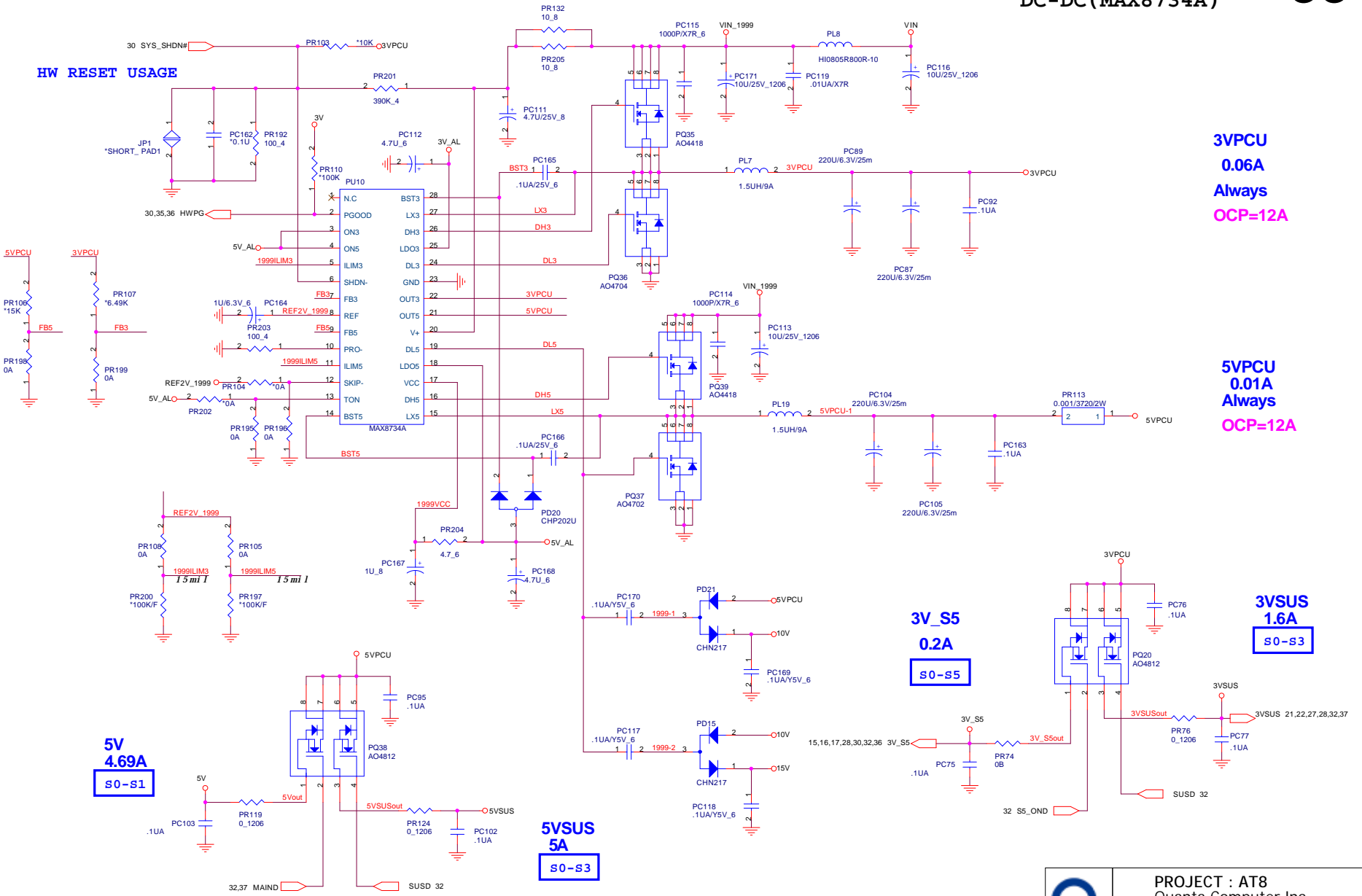
DISCHARGE



	PROJECT : AT8	
	Quantal Computer Inc.	
Size Custom	Document Number DISCHARGE	Rev 1A
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DC-DC (MAX8734A)

HW RESET USAGE



3VPCU
0.06A
Always
OCP=12A

5VPCU
0.01A
Always
OCP=12A

3V_S5
0.2A
S0-S5

3VSUS
1.6A
S0-S3

5V
4.69A
S0-S1

5VSUS
5A
S0-S3



PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number MAX8734A (3V/5V/15V)	Rev 1A
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Adapter
19V/3.4A/65W
4.75A/90W

MAX8724A

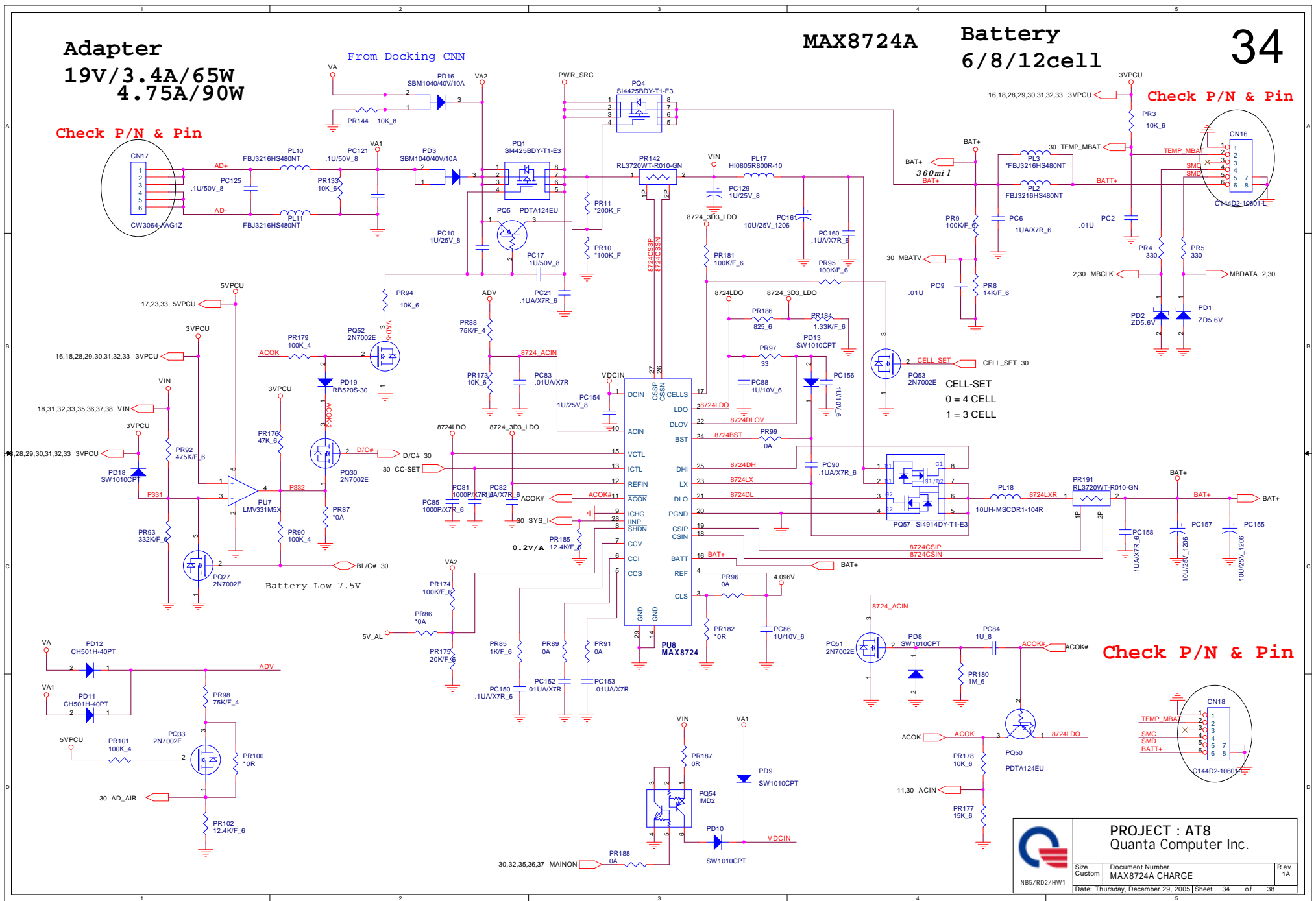
Battery
6/8/12cell


34

Check P/N & Pin

Check P/N & Pin

Check P/N & Pin

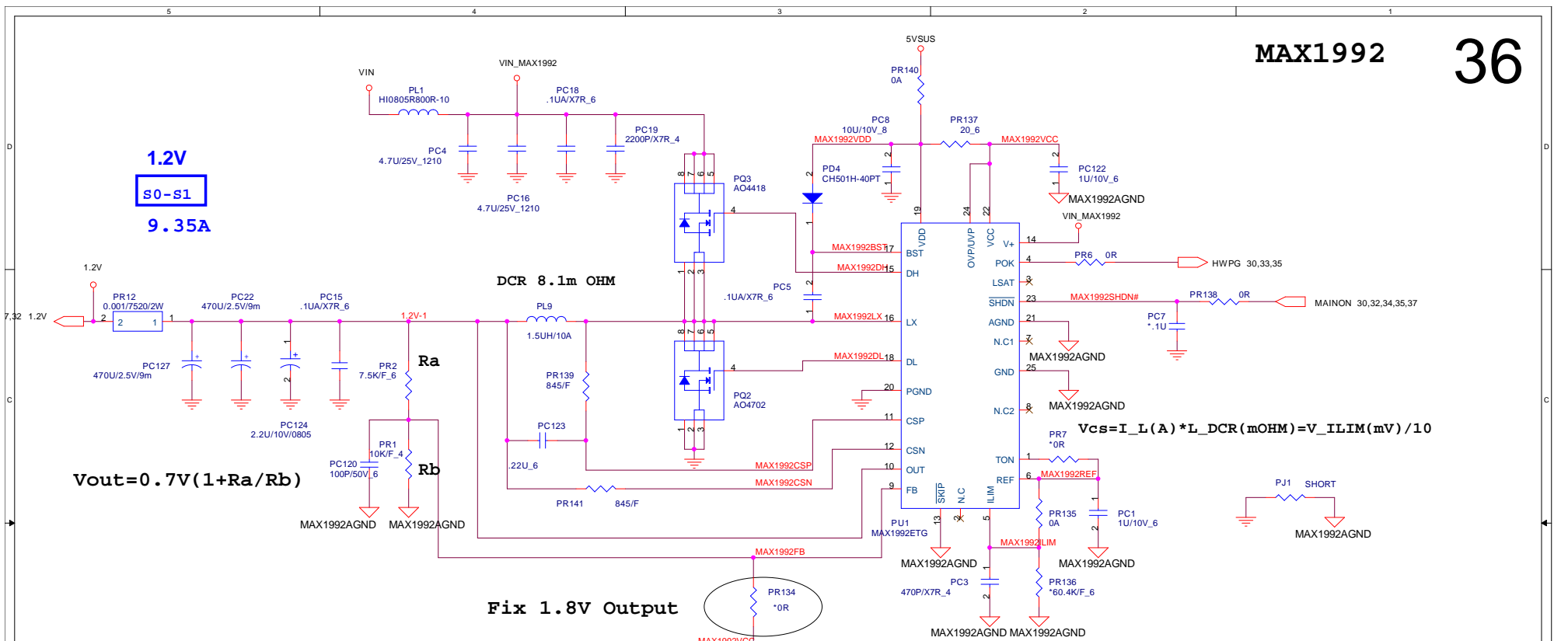


	PROJECT : AT8	
	Quanta Computer Inc.	
Size Custom	Document Number MAX8724A CHARGE	Rev 1A
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1.2V

S0-S1

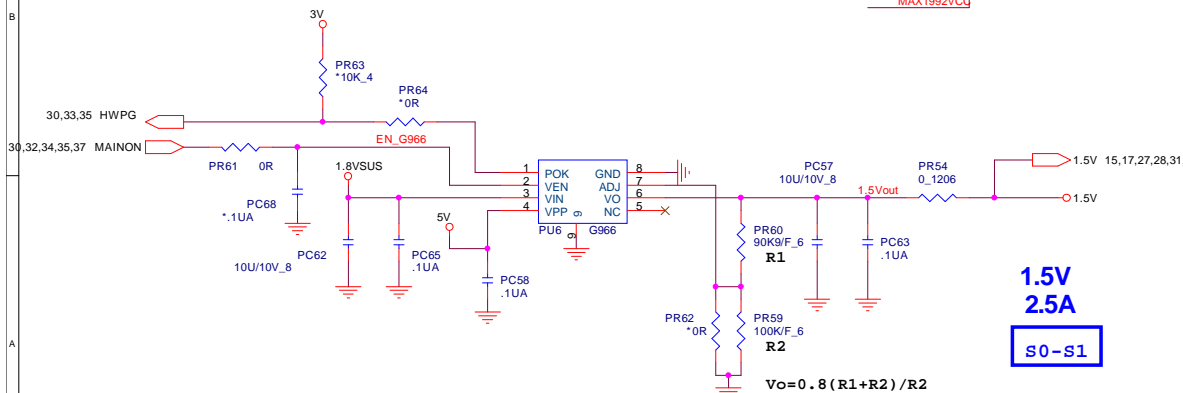
9.35A



$$V_{out} = 0.7V(1 + R_a/R_b)$$

Fix 1.8V Output

$$V_{cs} = I_L(A) * L_{DCR}(mOHM) = V_{ILIM}(mV) / 10$$



1.5V
2.5A

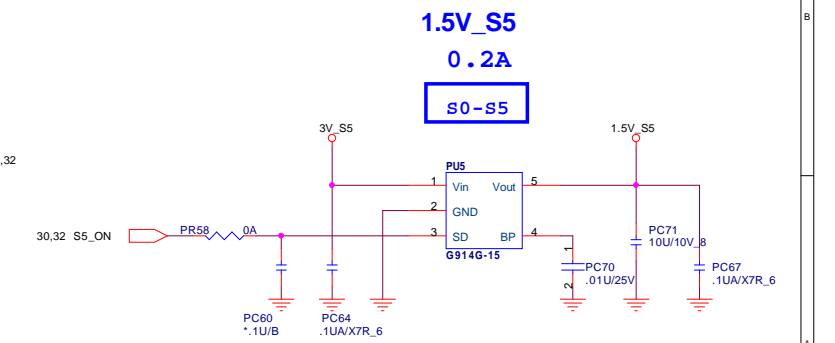
S0-S1

$$V_o = 0.8 * (R_1 + R_2) / R_2$$

1.5V_S5

0.2A

S0-S5



	PROJECT : AT8		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number MAX1992 1.5V_S5/1.5V/1.2V		
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**1.8VSUS
9.1A**
S0-S3

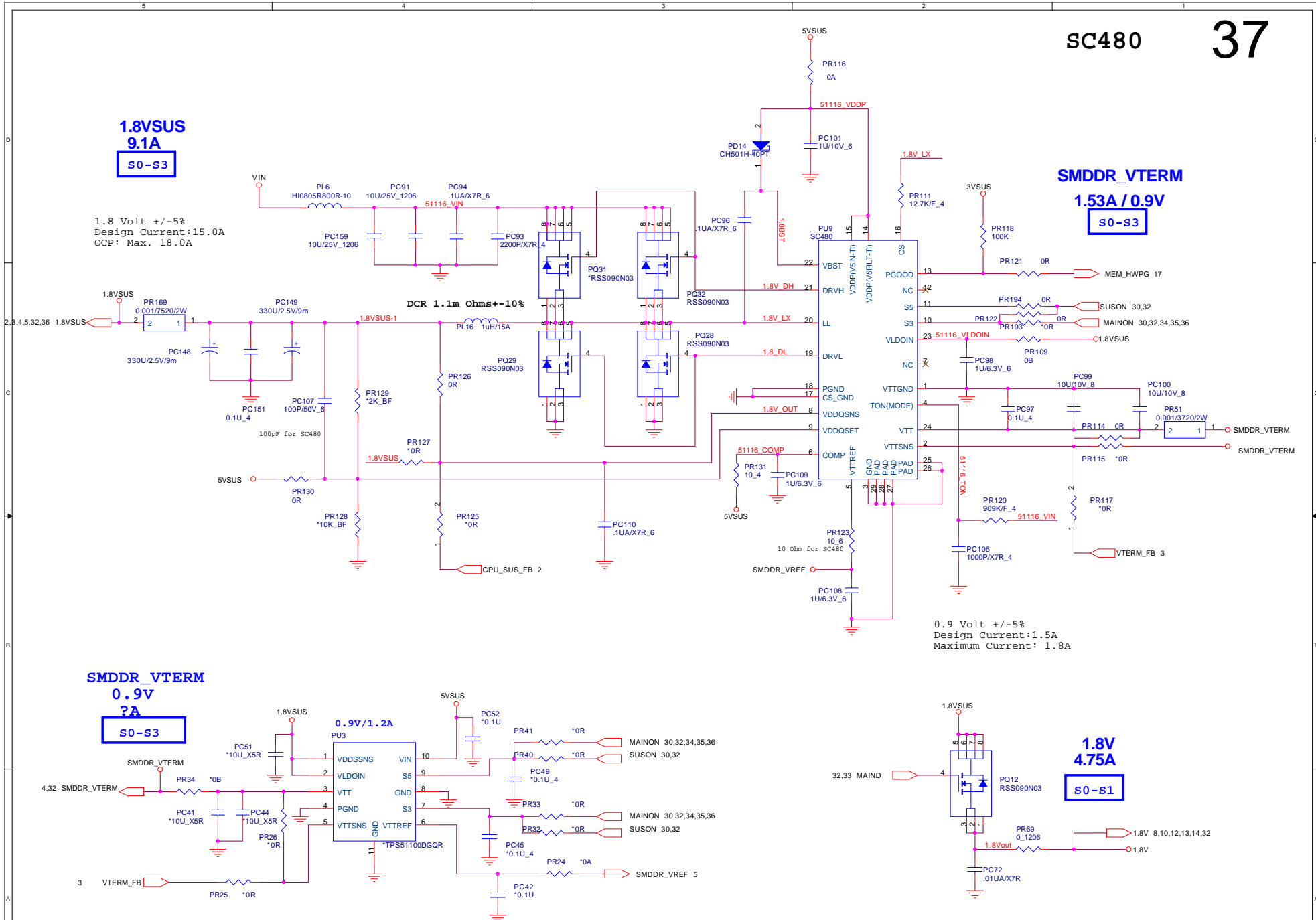
1.8 Volt +/-5%
Design Current:15.0A
OCP: Max. 18.0A


**SMDDR_VTERM
1.53A / 0.9V**
S0-S3

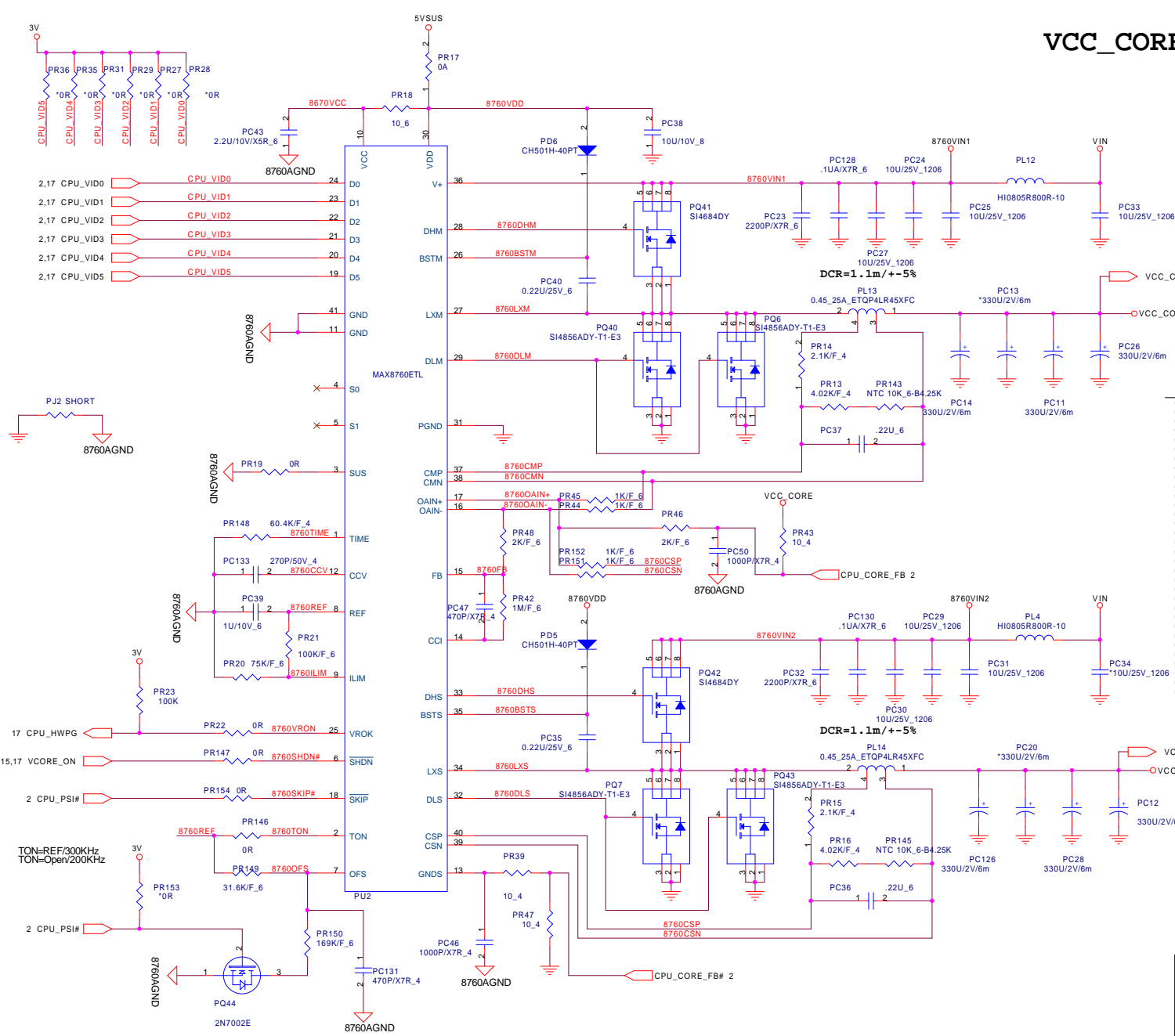
0.9 Volt +/-5%
Design Current:1.5A
Maximum Current: 1.8A

**SMDDR_VTERM
0.9V
?A**
S0-S3

**1.8V
4.75A**
S0-S1




	PROJECT : AT8 Quanta Computer Inc.	
	Size Custom Date: Thursday, December 29, 2005	Document Number SC480 1.8VSUS/1.8V/SMDDR



OCP=?A
VCC_CORE
35A / 1.05V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	1	0	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	0	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V



PROJECT : AT8
Quanta Computer Inc.

Site Custom	Document Number MAX8760 VCC_CORE	Rev 1A
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