

Compal Confidential

G400/G500 UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

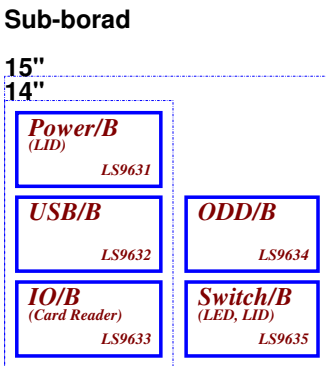
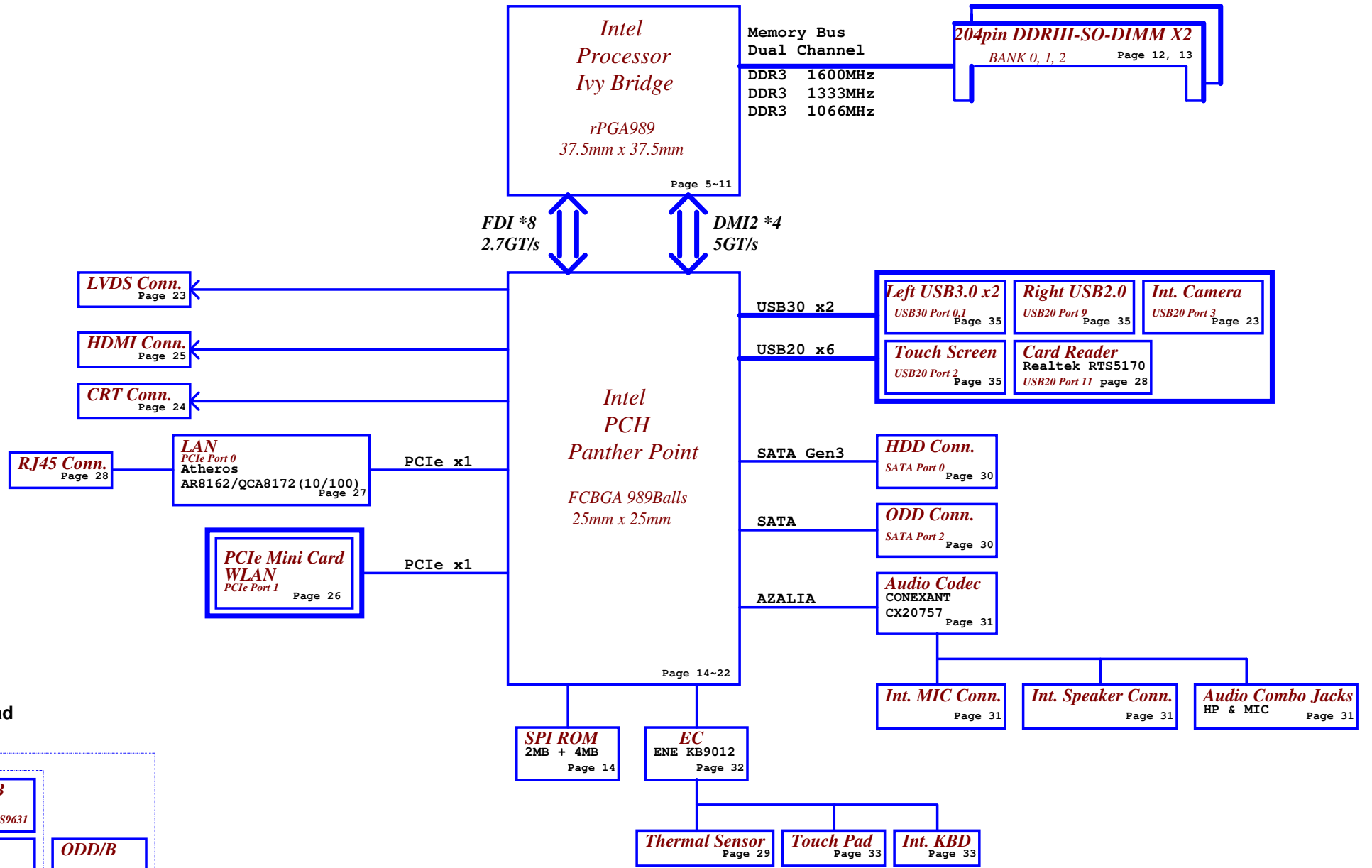
2013-02-27

LA-9632P

REV: 1.0

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Chief River



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Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
		+3VALW		+3VS
State				+1.5VS
				+V1.05S_VCCP
				+VCC_CORE
				+VGA_CORE
				+VCC_GFXCORE_AXG
				+1.8VS
				+0.75VS
				+1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	-V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V	Board ID / SKU ID Table for AD channel						
R694	100K +/- 1%	Board ID	R695	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD	
0	0	0	0 V	0 V	0 V	0 V	0x00 - 0x0B	MP
1	12K +/- 1%	1	0.347V	0.354V	0.360V	0.360V	0x0C - 0x1C	PVT
2	15K +/- 1%	2	0.423V	0.430V	0.438V	0.438V	0x1D - 0x26	DVT
3	20K +/- 1%	3	0.541V	0.550V	0.559V	0.559V	0x27 - 0x30	EVT

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011x

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

AMD-GPU SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
DDR_JDIMM2	1010 010x A4h

Device	Address
Internal thermal sensor	0100 0001 41h

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) _{USB3.0}
		1	USB Port (Left Side) _{USB3.0}
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
7			
EHCI2	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
13			

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76, HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	V	X	X	X	X	V	V
SMB_EC_DA2	+3VS	+3VGS					+3VS	+3VALW
PCH_SMBCLK	PCH	X	X	X	V	V	X	X
PCH_SMBDATA	+3VALW				+3VS	+3VS		
PCH_SMLCLK	PCH	X	X	X	X	X	X	X
PCH_SMLDATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VGS		+3VS			+3VS	

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Notes List

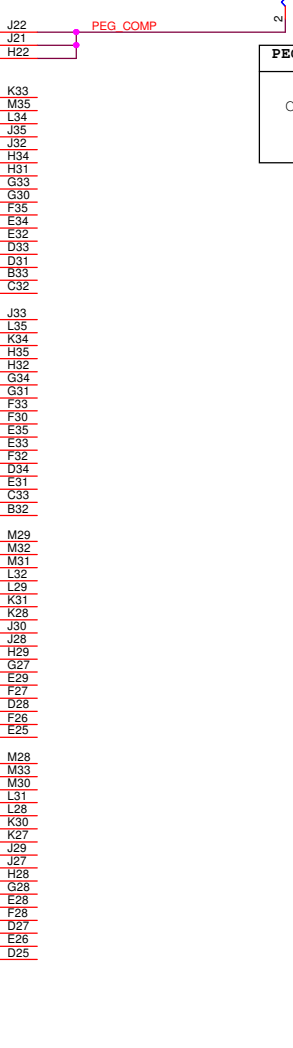
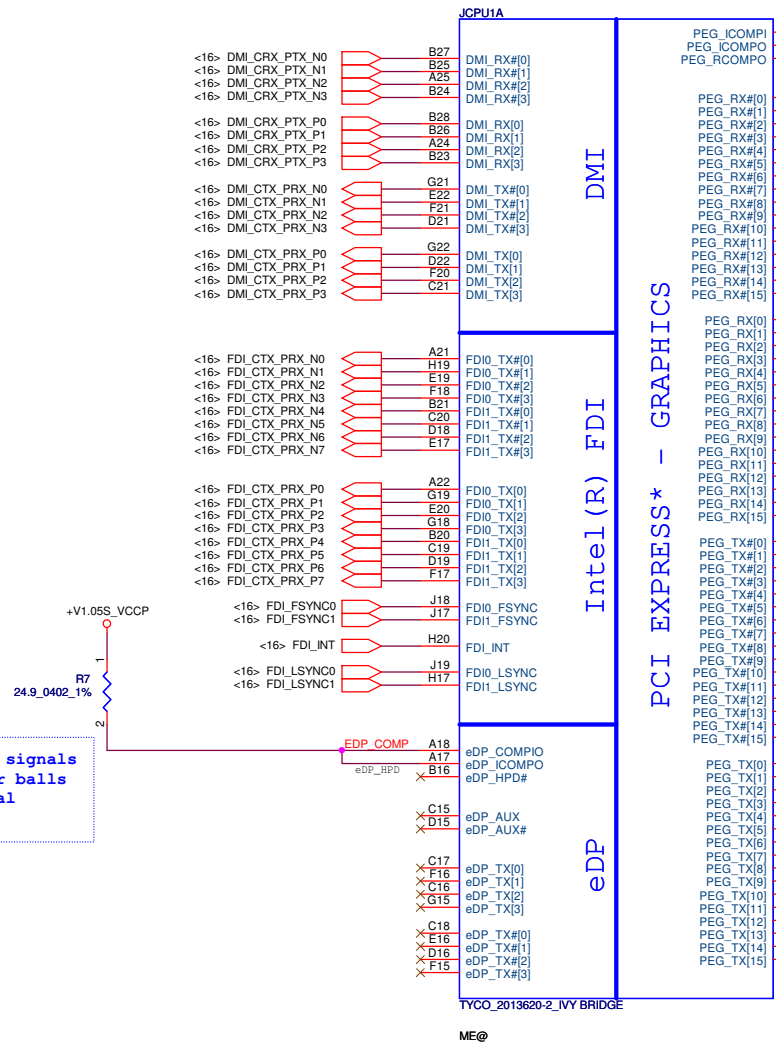
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14" UMA PCB_LA9632P
DA6000WP000
PCB 0Y0 LA-9632P REV0 MB UMA 3

15" UMA PCB_LA9632P
DA6000WP100
PCB 0Y0 LA-9632P REV0 MB UMA 5

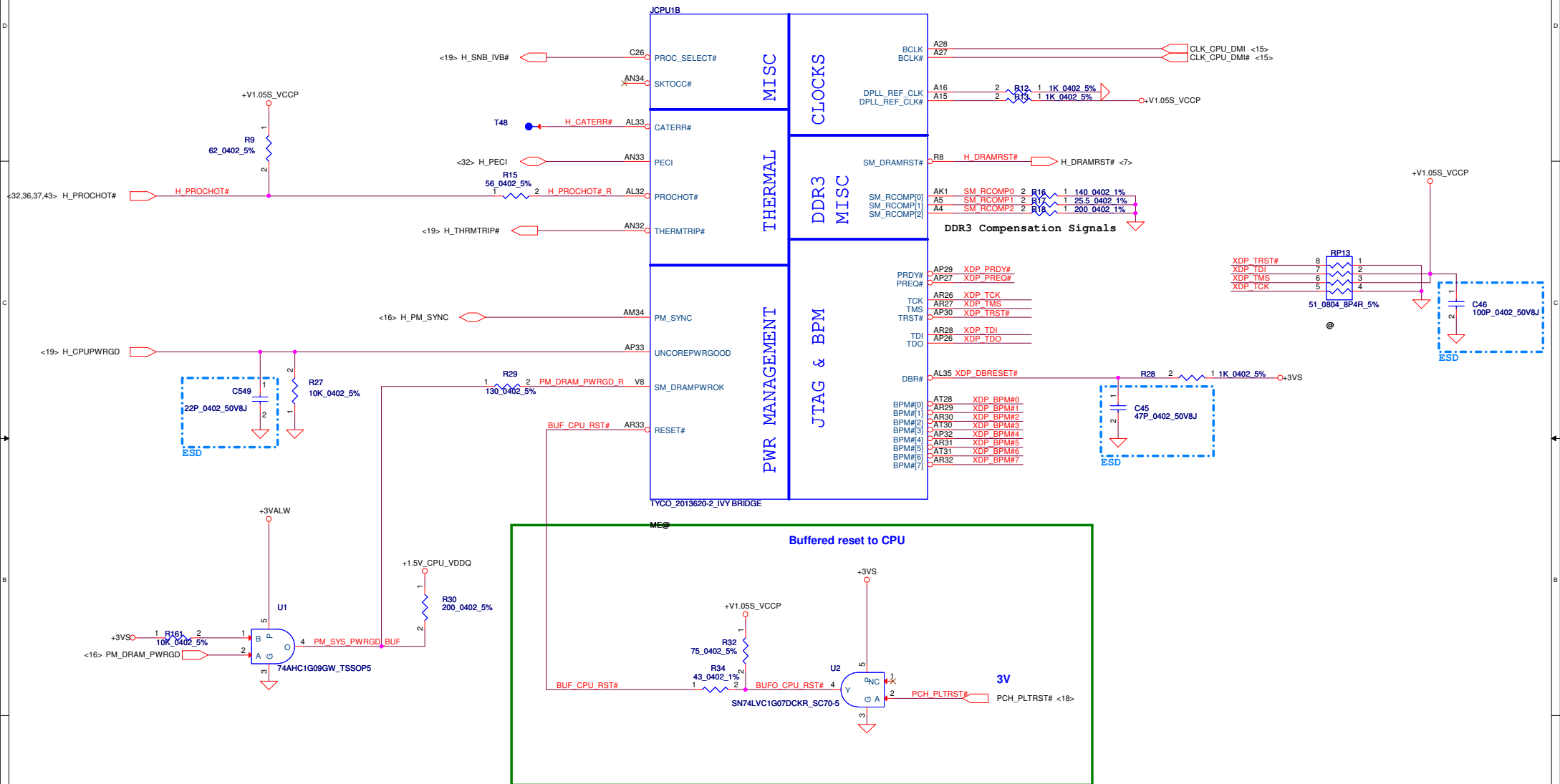
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

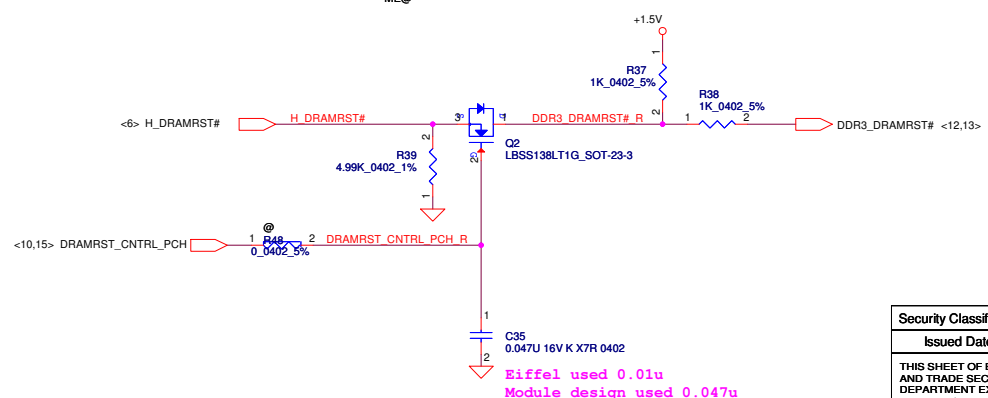
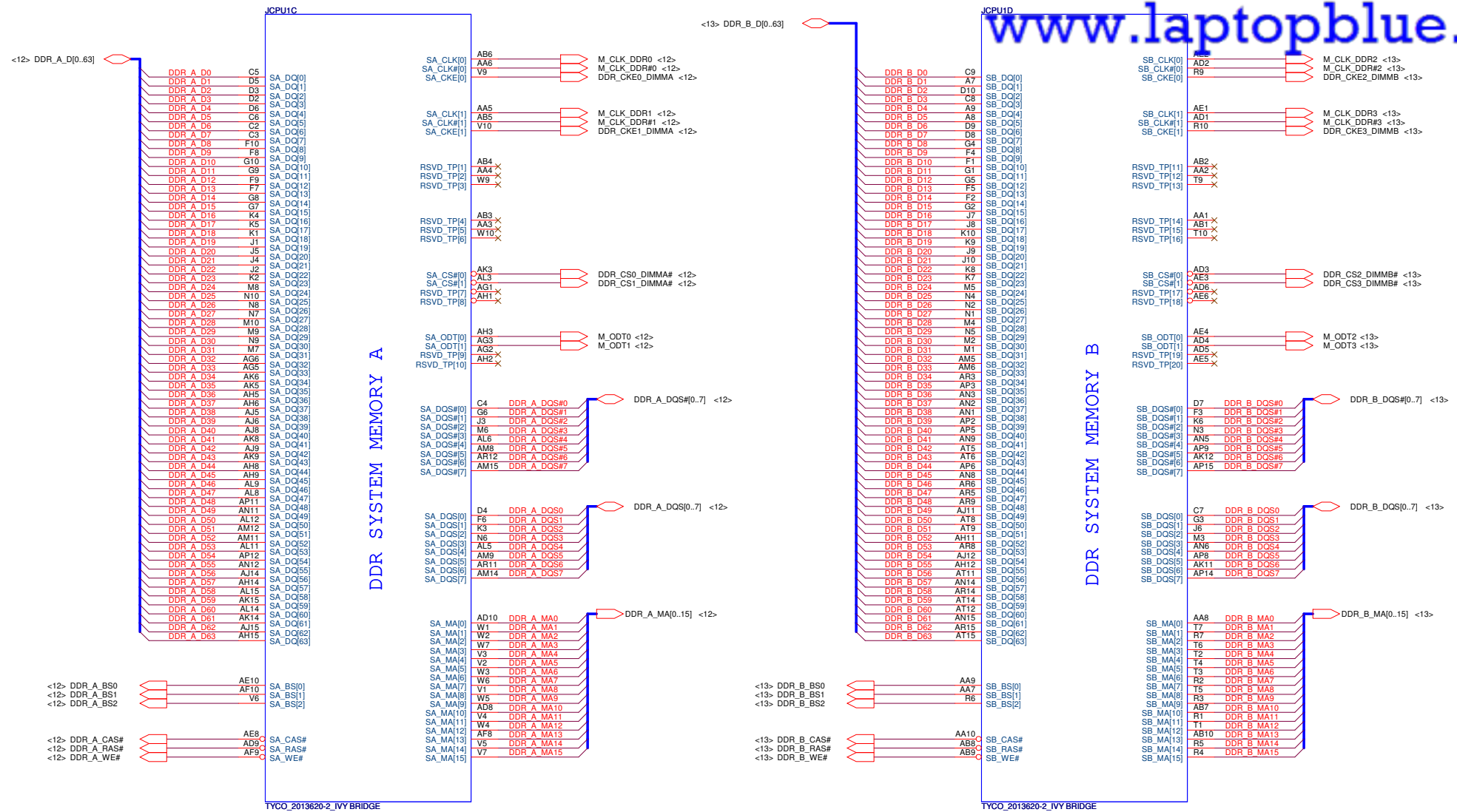


PEG Static Lane Reversal - CFG2 is for the 16x

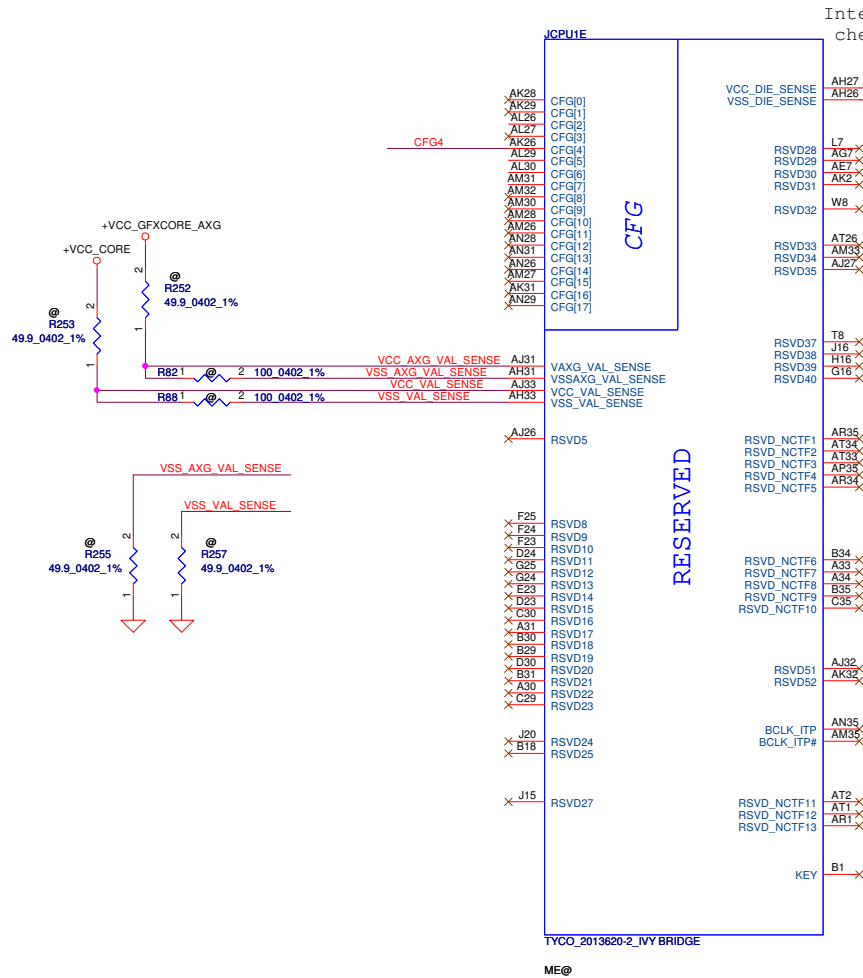
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
*	0: Lane Reversed

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms





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PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed
------	--



Display Port Presence Strap

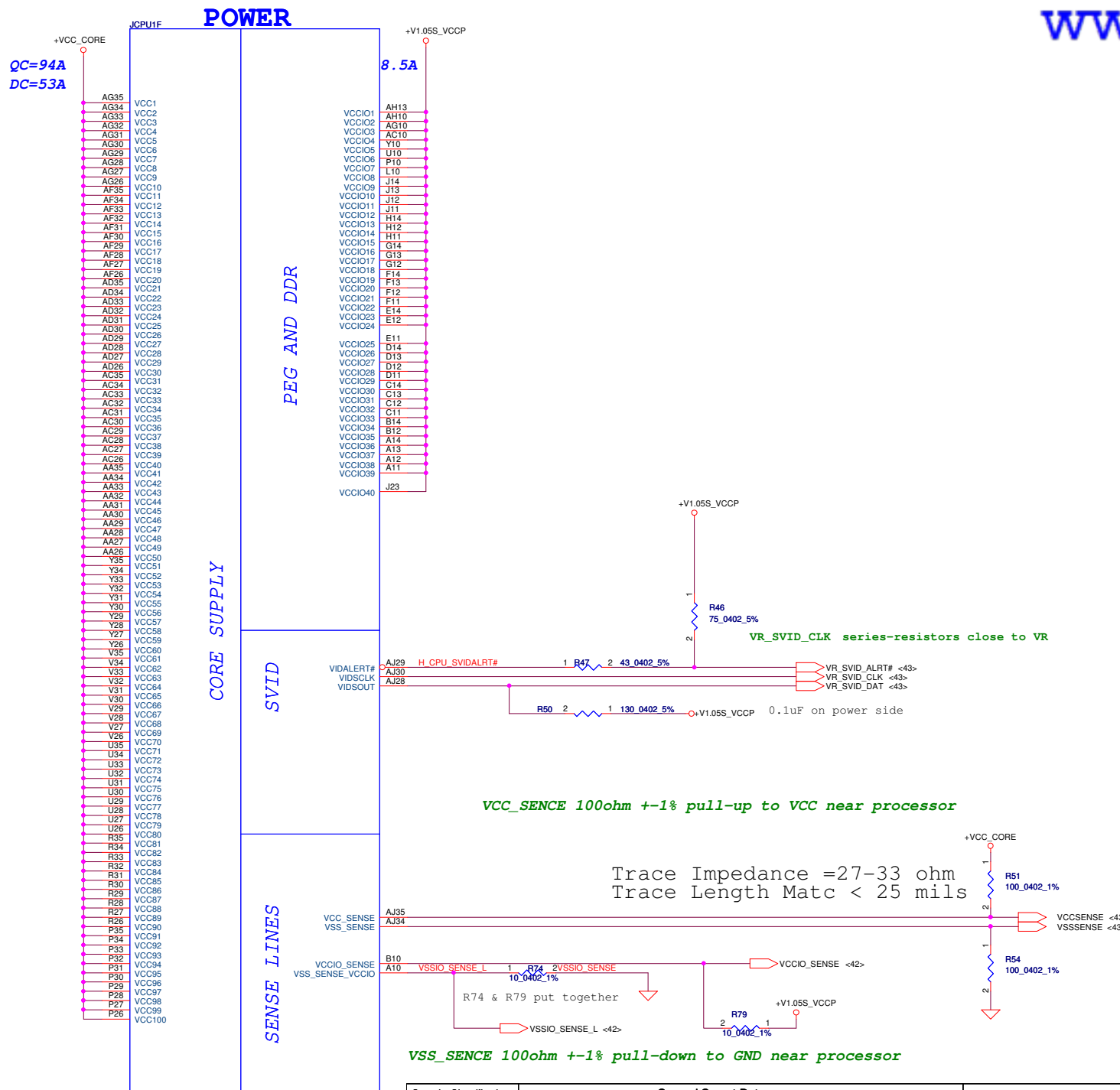
CFG4	* 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

PCIe Port Bifurcation Straps

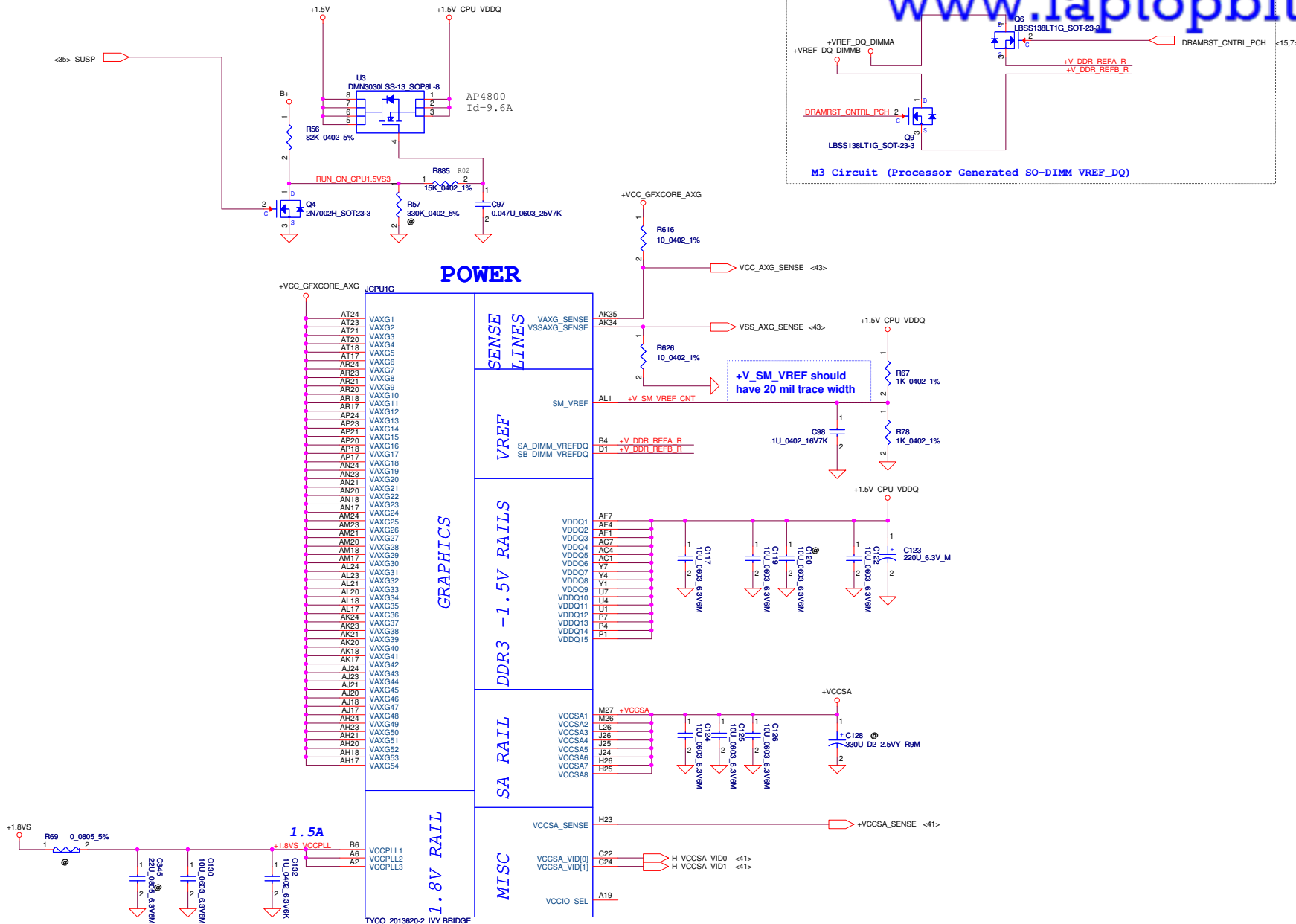
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled
----------	--

PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

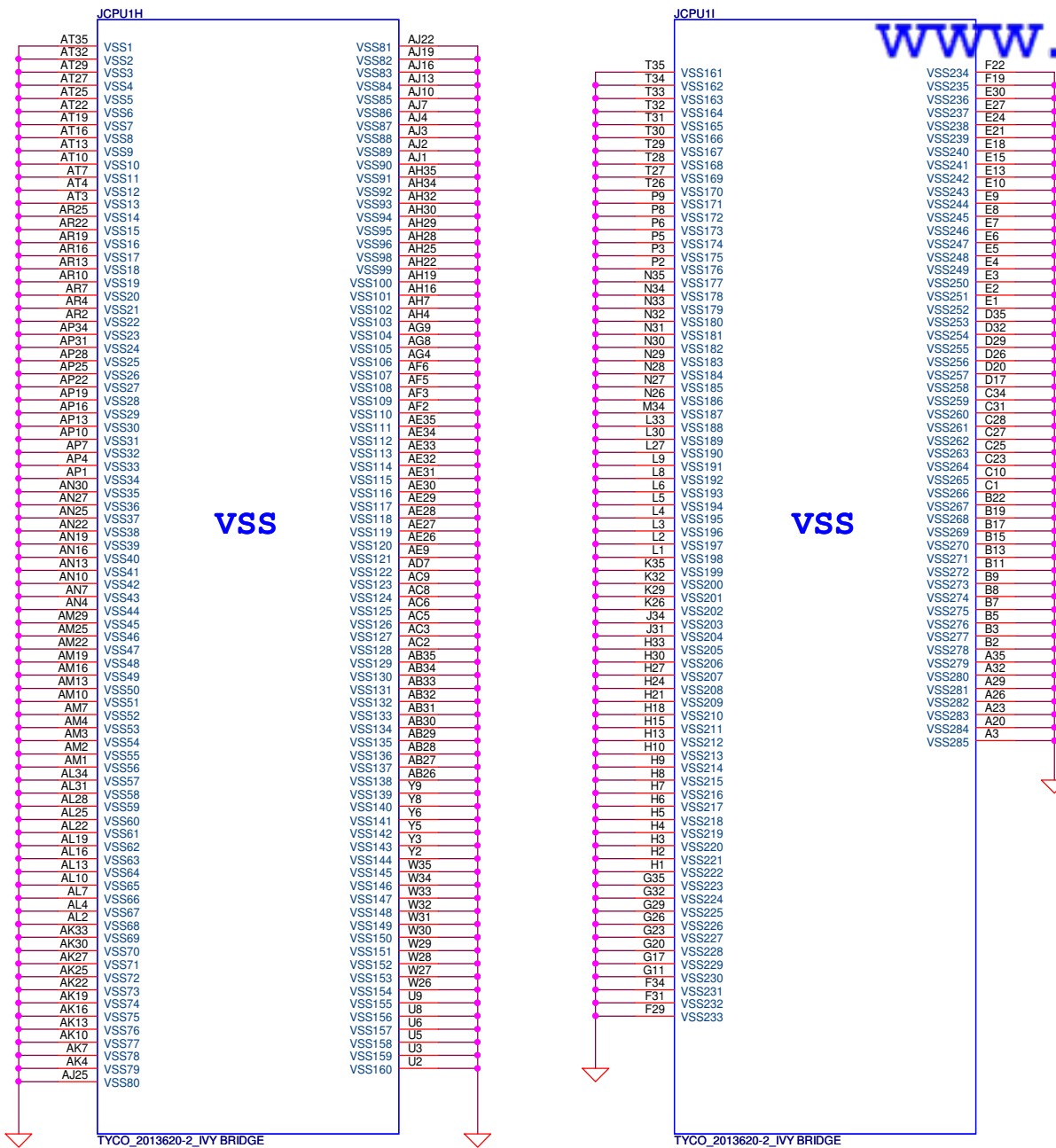


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IVY Bridge drives VCCIO_SEL low
 VCCP_PWRCTRL:0
 Sandy Bridge is NC for A19
 VCCP_PWRCTRL:1

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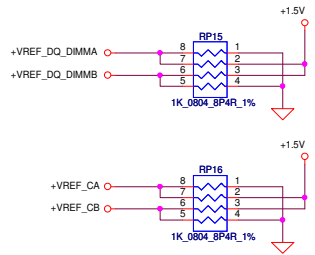
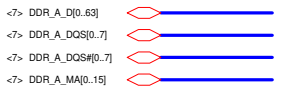
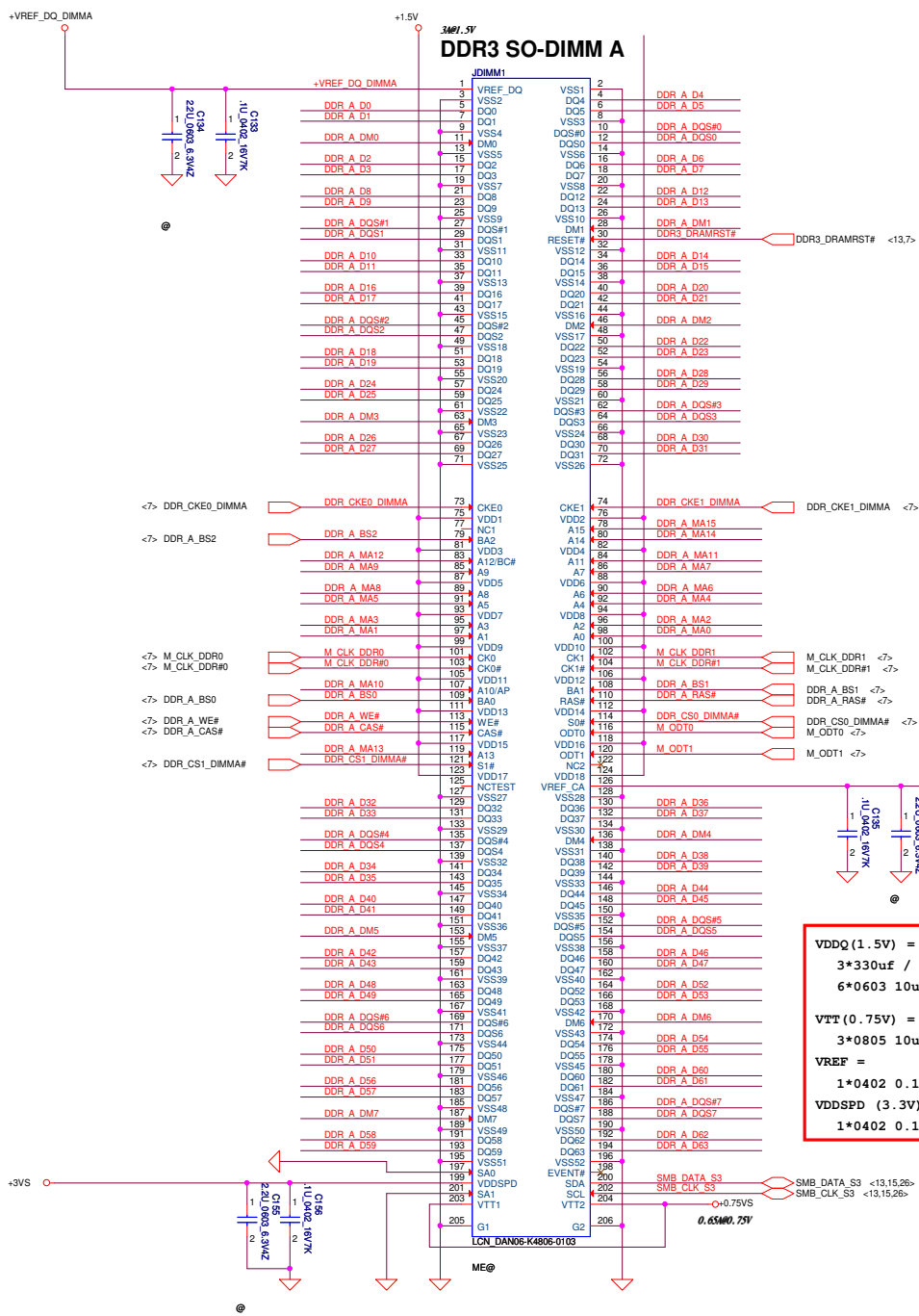
VSS

VSS

ME@

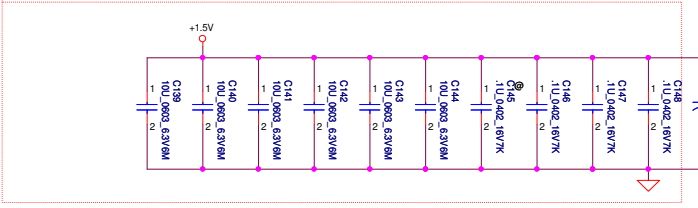
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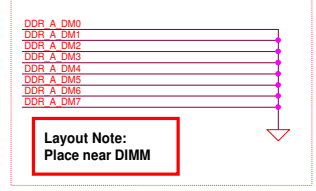
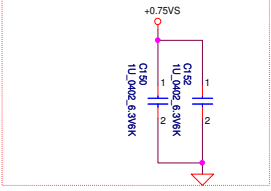
Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
 (10uF_0603_6.3V)*8
 (0.1uF_402_10V)*4



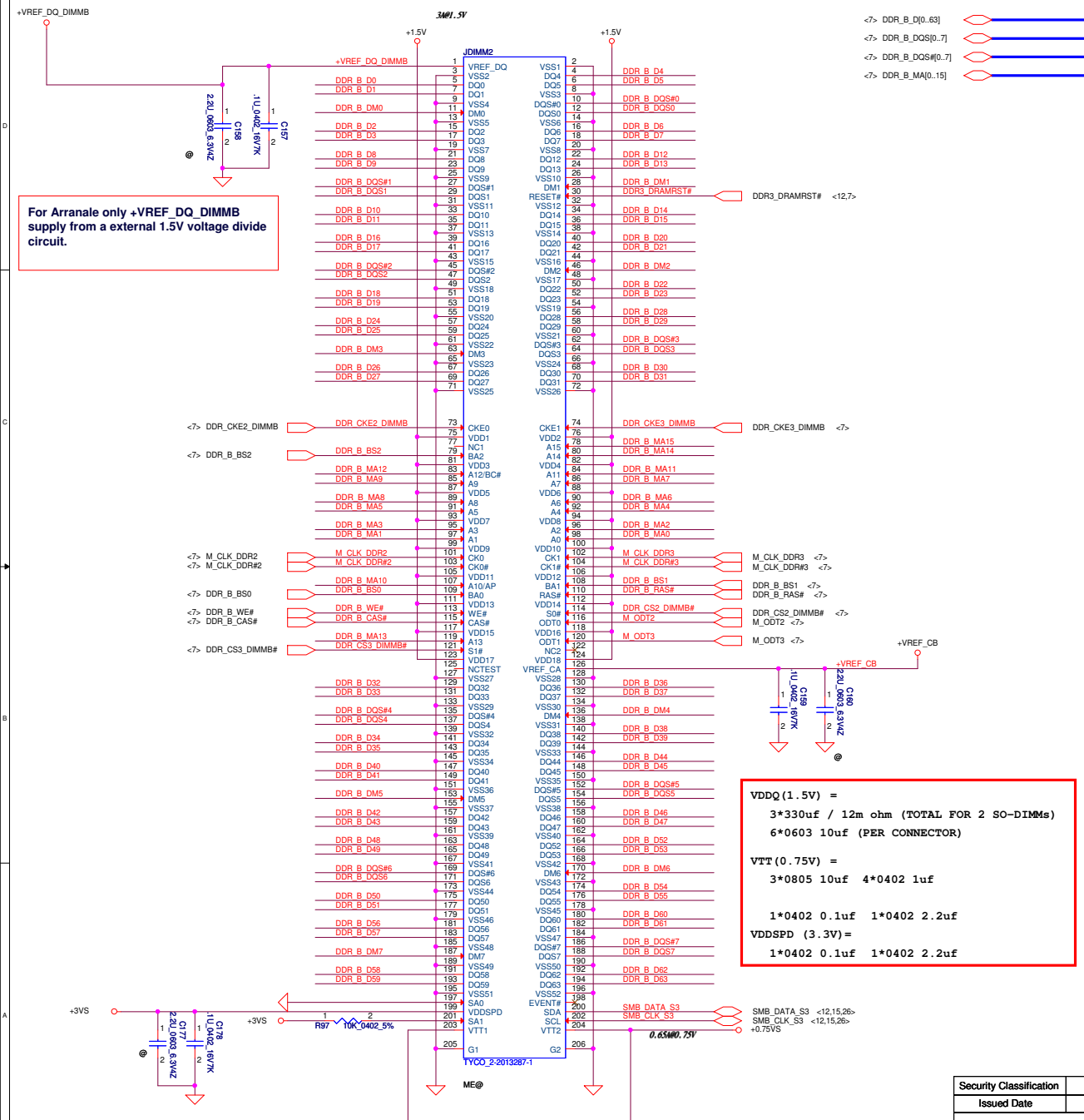
Layout Note:
Place near DIMM

7/28 Update connect GND directly



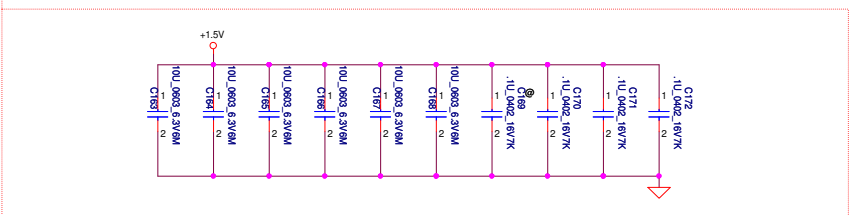
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Layout Note:
Place near DIMM

$(10\mu F_{0603_6.3V}) * 8$
 $(0.1\mu F_{402_10V}) * 4$



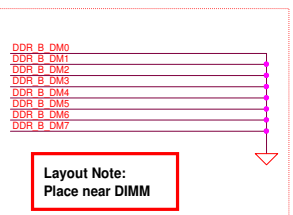
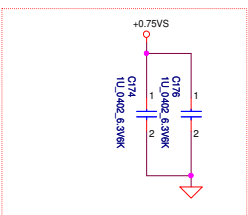
Layout Note:
Place near DIMM

VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT (0.75V) =
3*0805 10uf 4*0402 1uf

1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

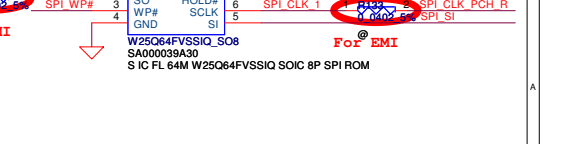
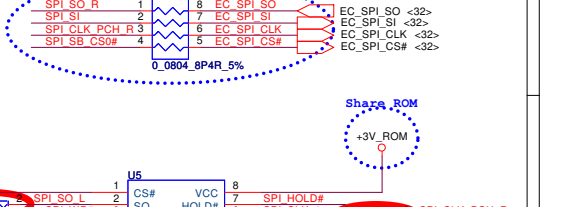
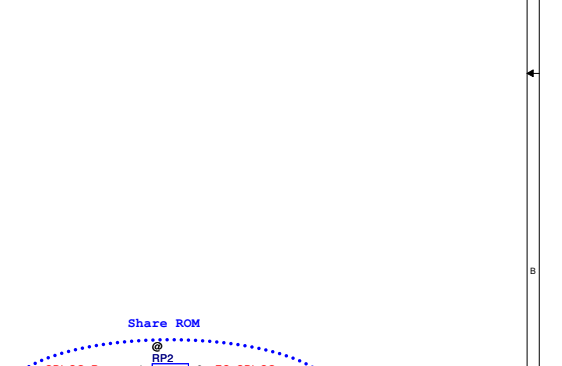
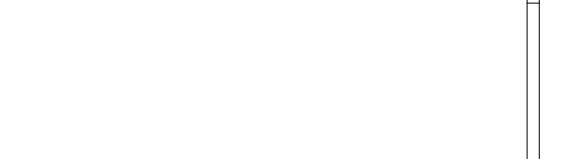
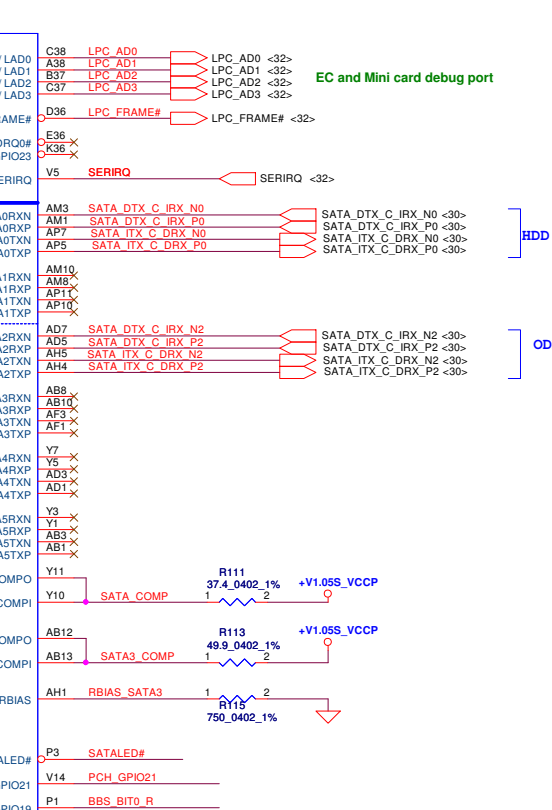
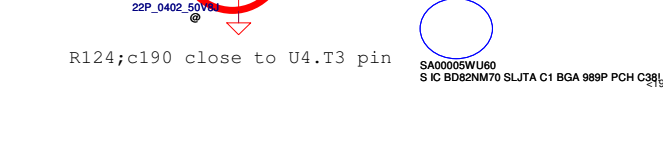
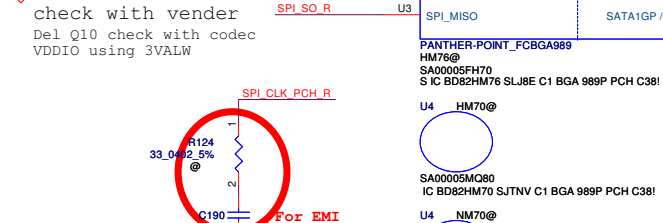
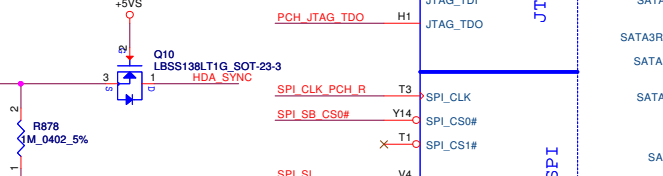
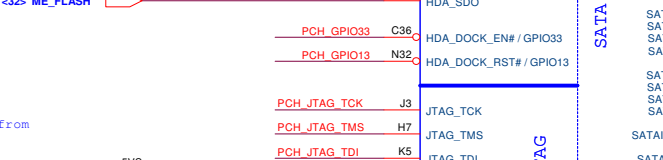
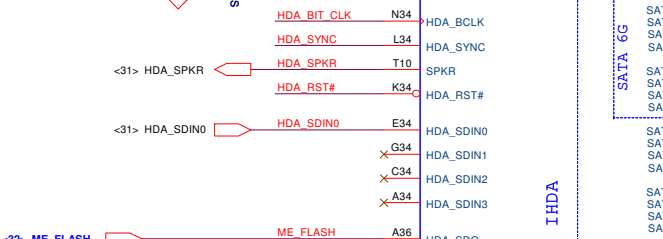
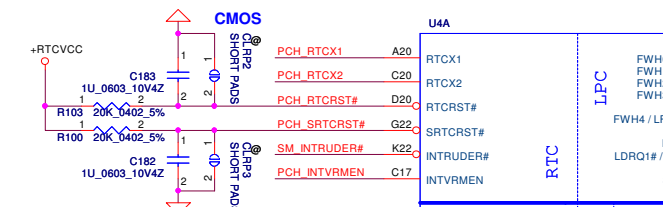
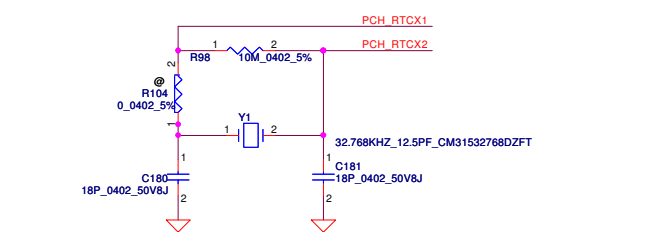
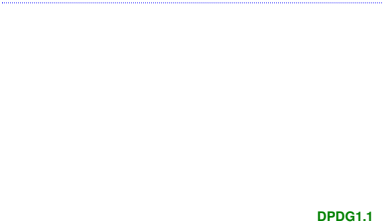
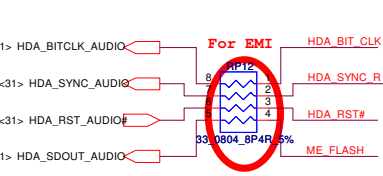
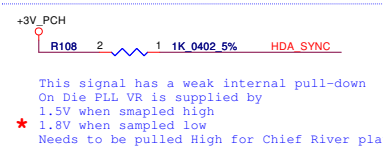
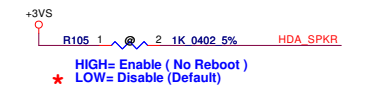
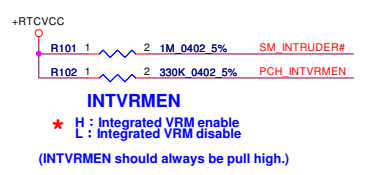
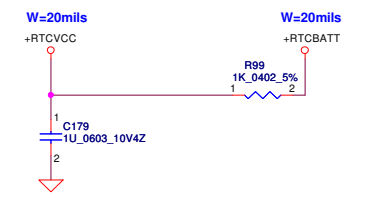


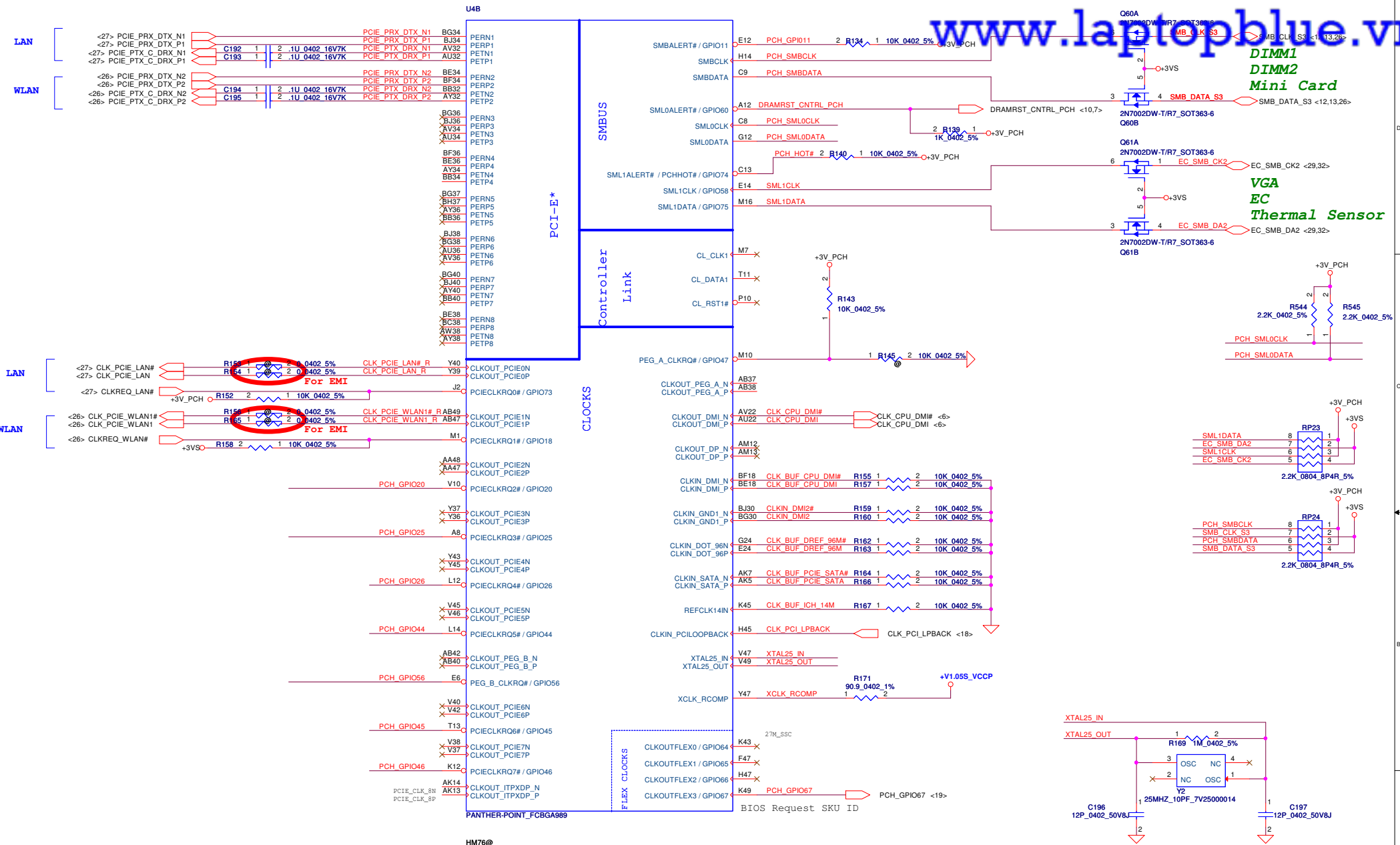
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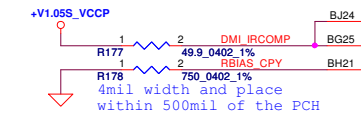
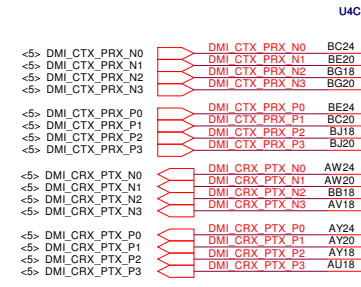
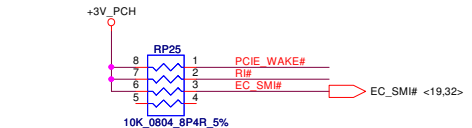
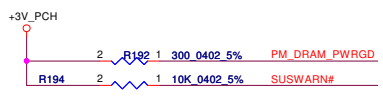
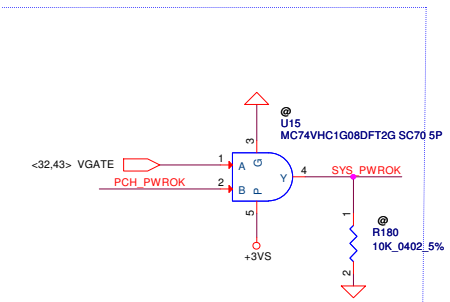
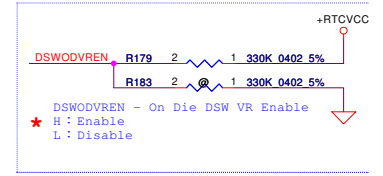
CLR2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CLR3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

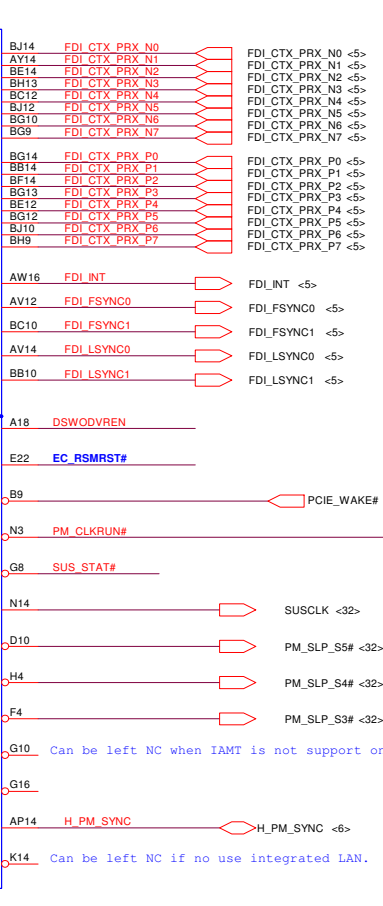
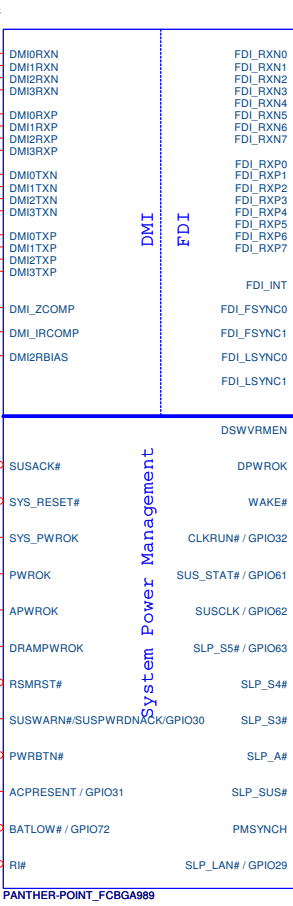
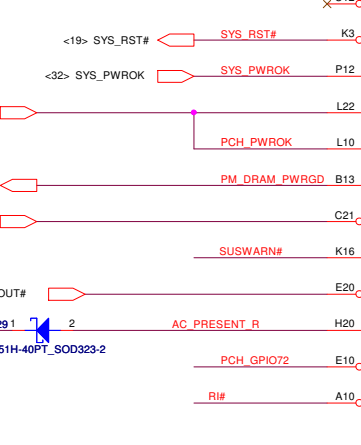




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Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (2/9) PCIE, SMBUS, CLK	
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE CUSTOMER TO ANY OTHER DIVISION OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
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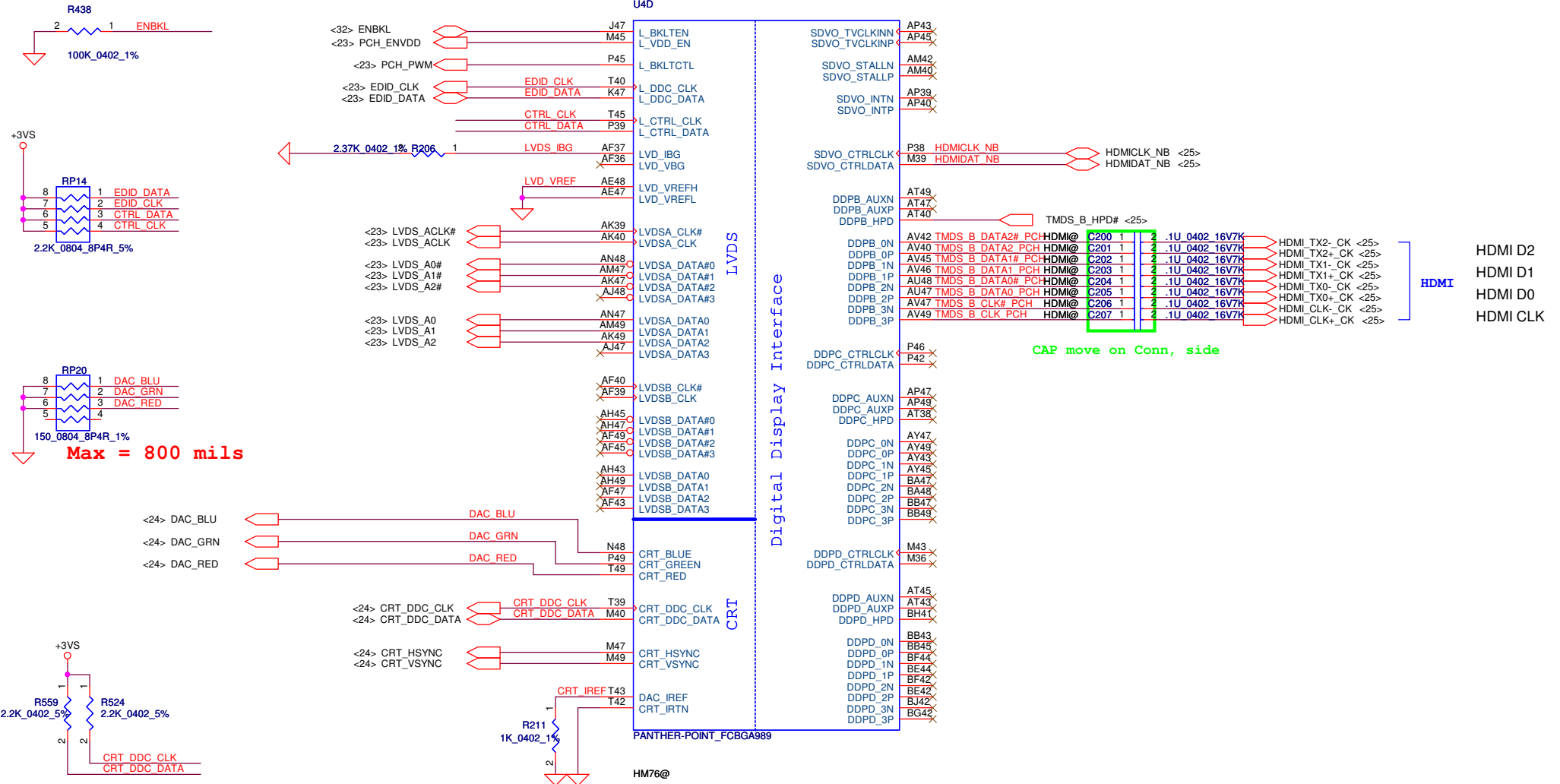


SUSACK# is only used on platform that support the Deep Sx state.

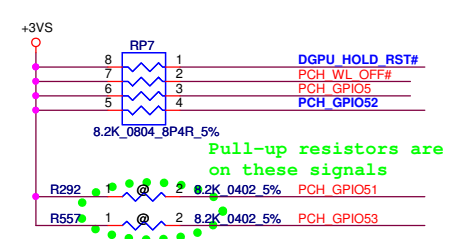
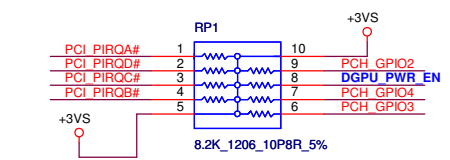


HM76@

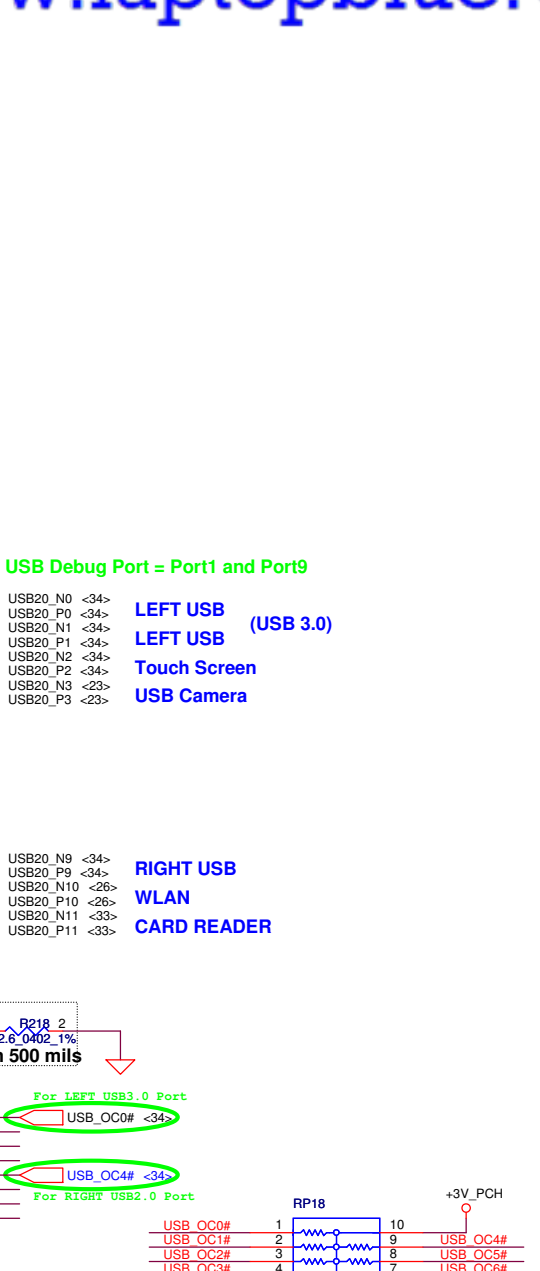
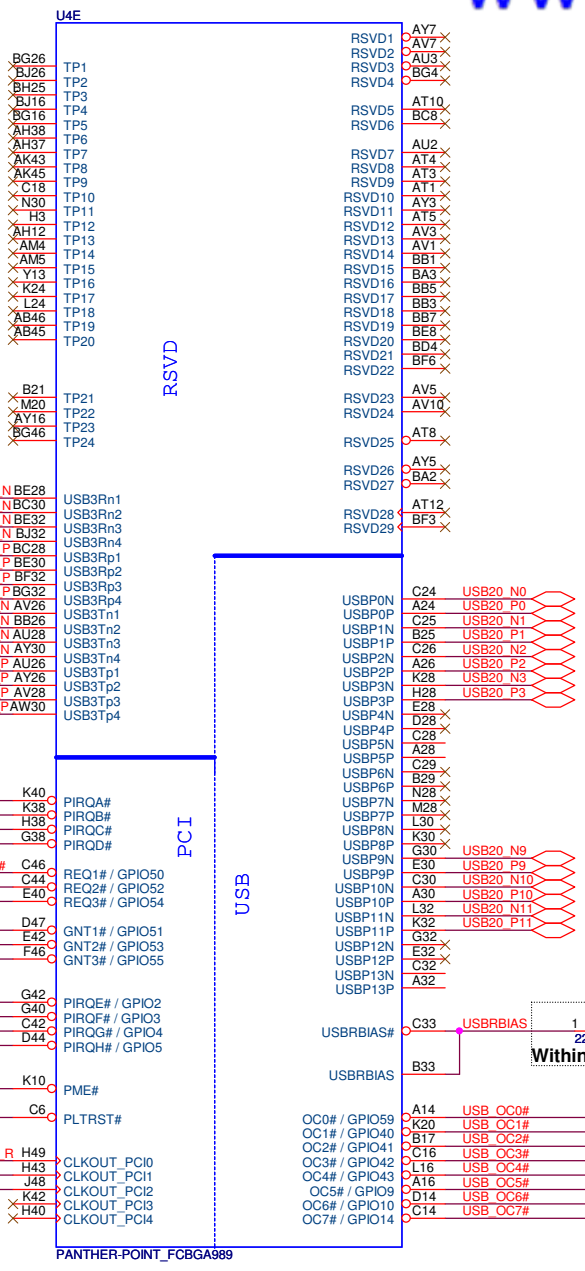
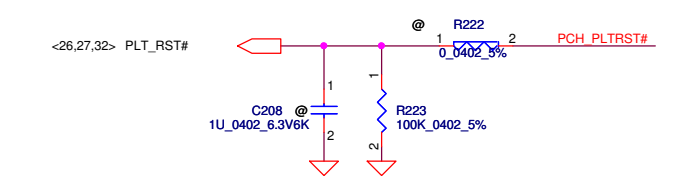
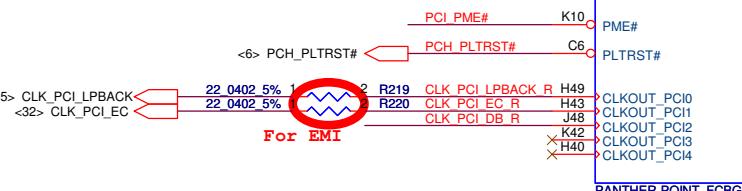
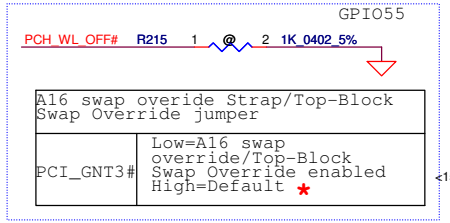
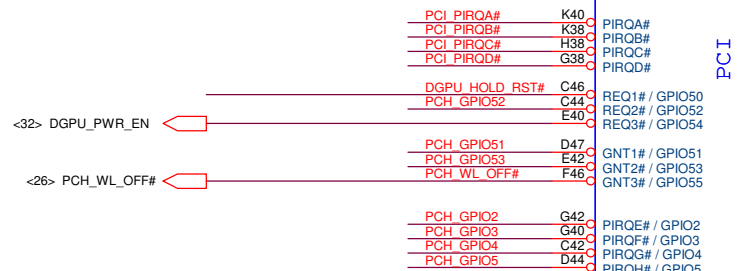
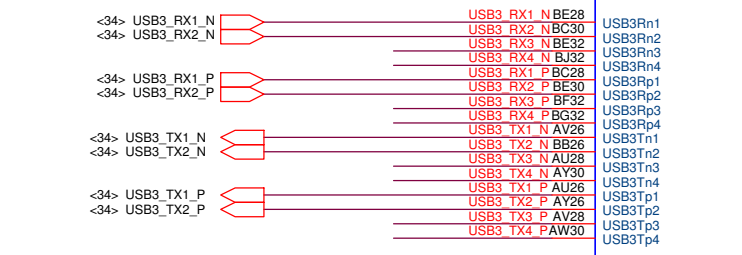
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Boot BIOS Strap bit1 BBS1		
Bit11	Bit10	Boot BIOS Destination
0	1	Reserved
1	0	Reserved
1	1	★ SPI (Default)
0	0	LPC



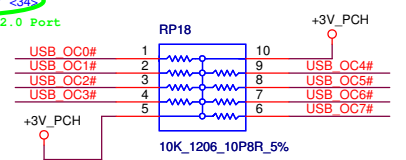
USB Debug Port = Port1 and Port9

LEFT USB (USB 3.0)
LEFT USB
Touch Screen
USB Camera

RIGHT USB
WLAN
CARD READER

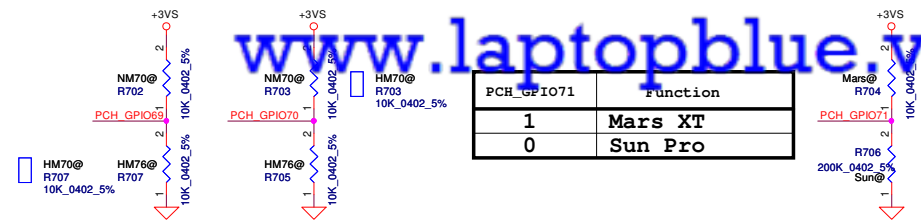
Within 500 mils

For LEFT USB3.0 Port
USB_OC0# <34>
For RIGHT USB2.0 Port
USB_OC4# <34>



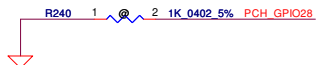
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Issued Date	2011/06/15	Deciphered Date	2012/07/11
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PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76

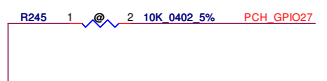


PCH_GPIO71	Function
1	Mars XT
0	Sun Pro

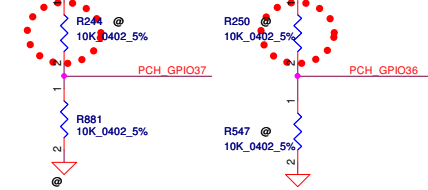
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



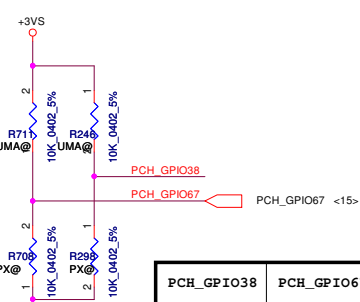
* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



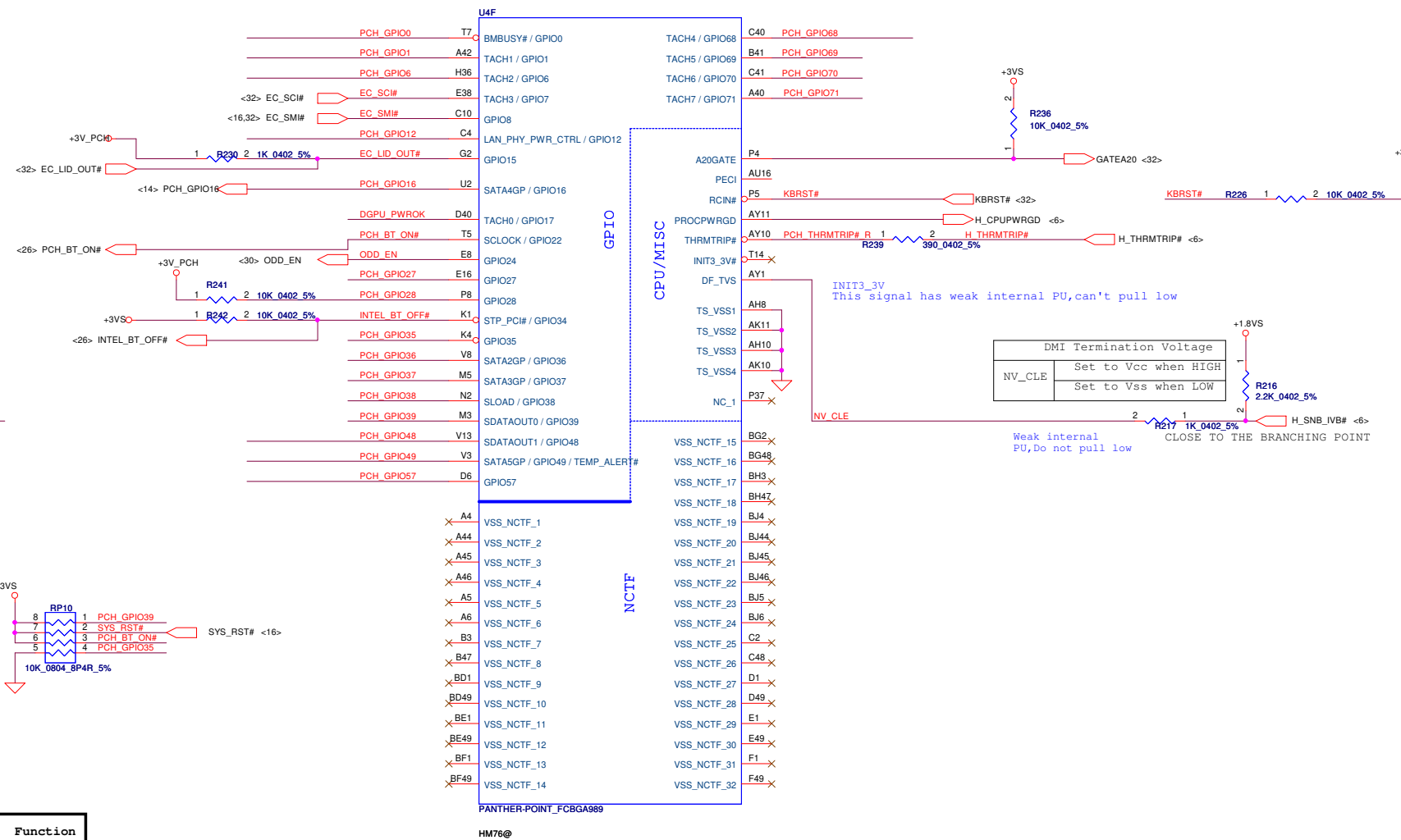
GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.



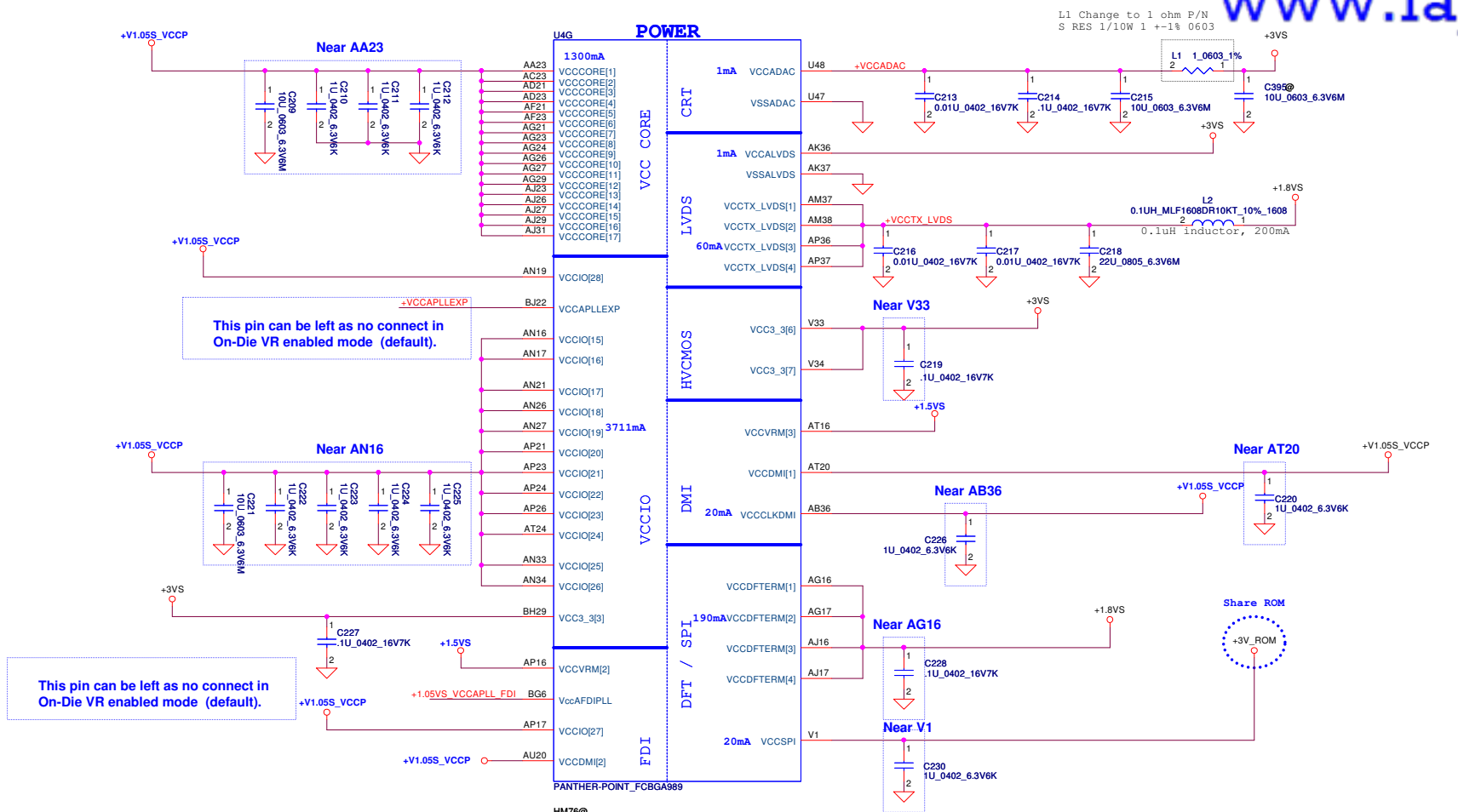
BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	SG (Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA

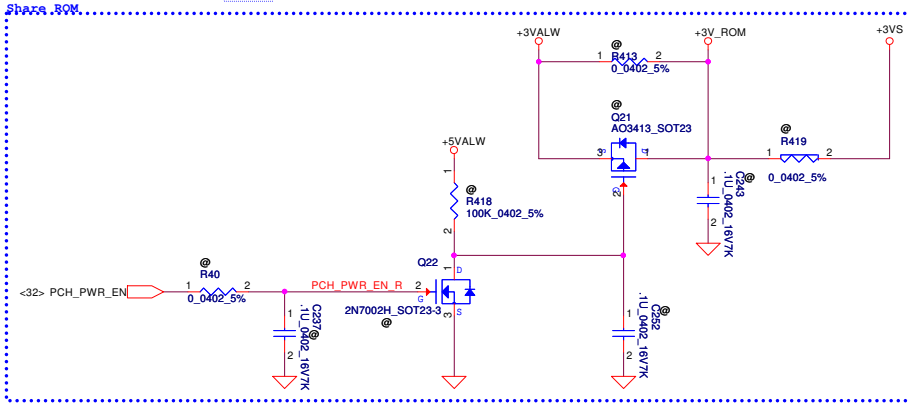


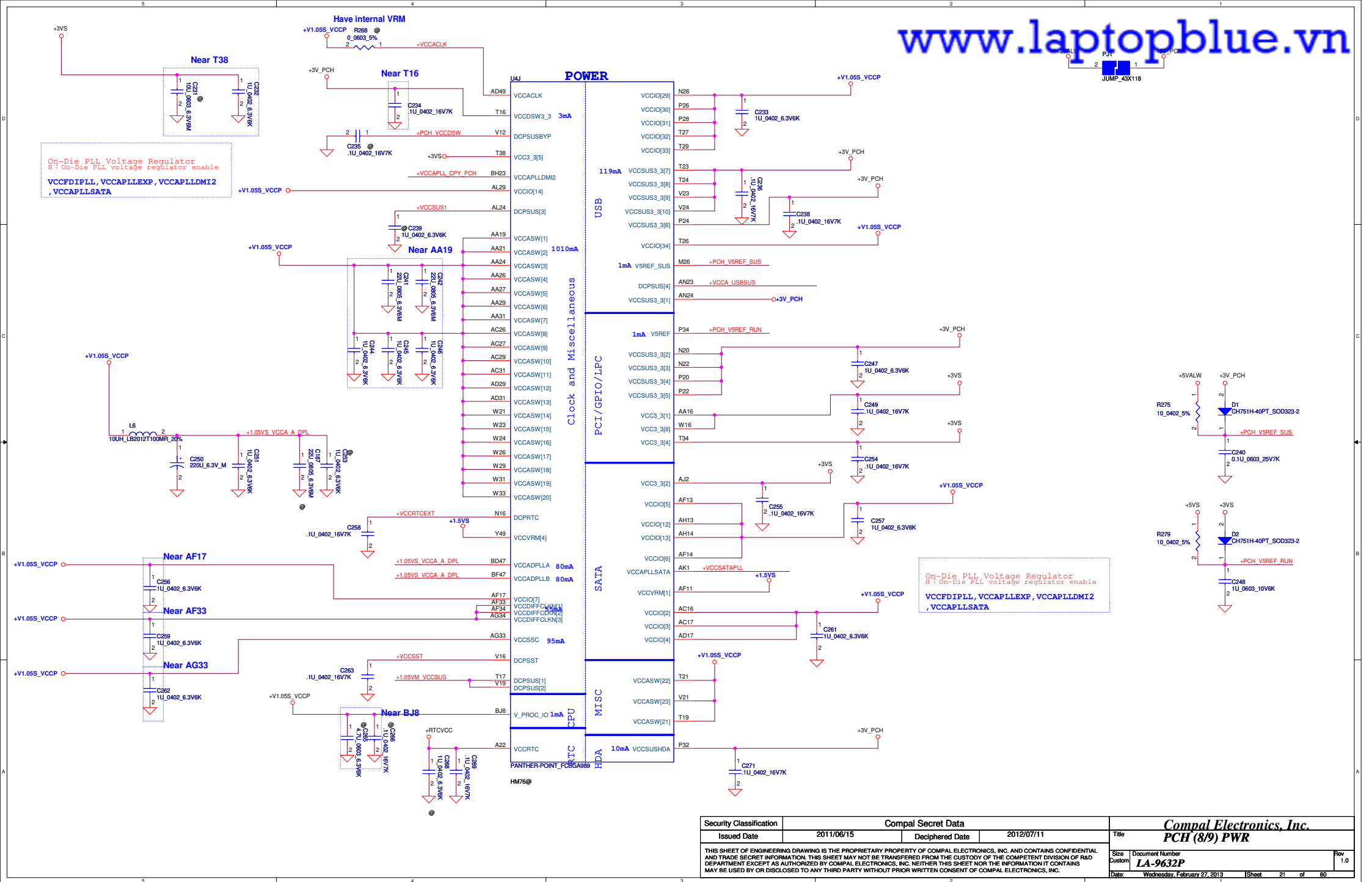
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PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLb	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

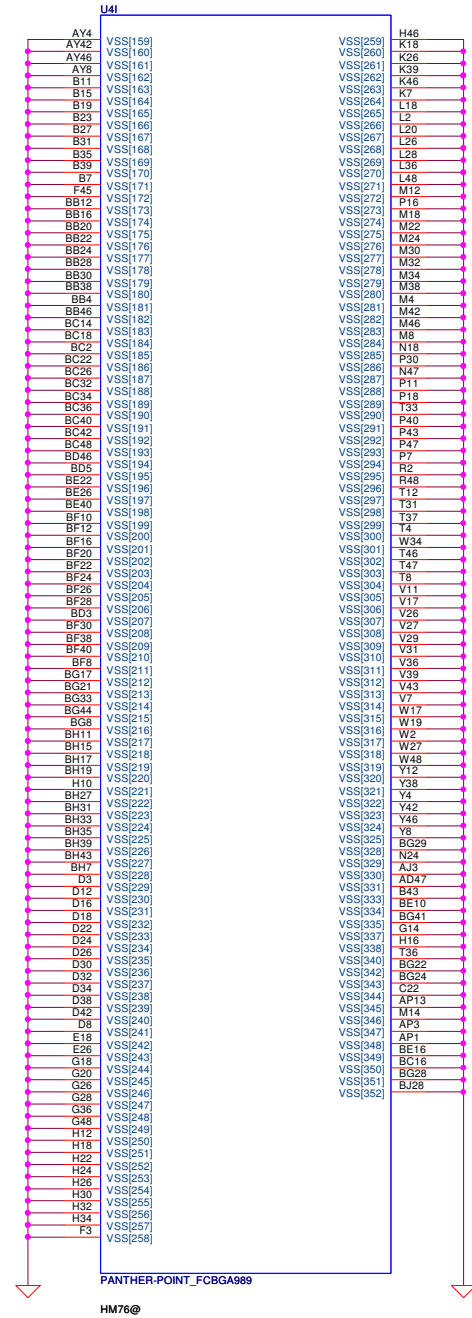
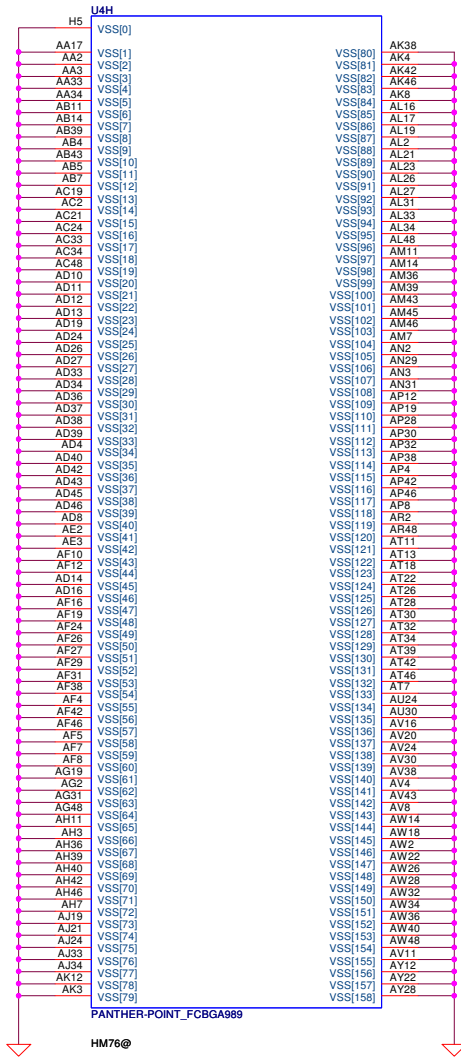




On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLEXP, VCCAPLLDMI2, VCCAPLLSATA

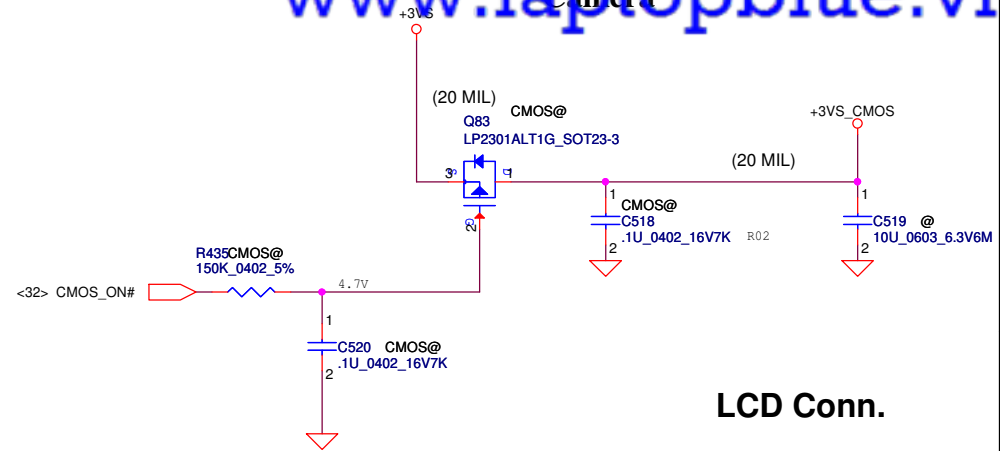
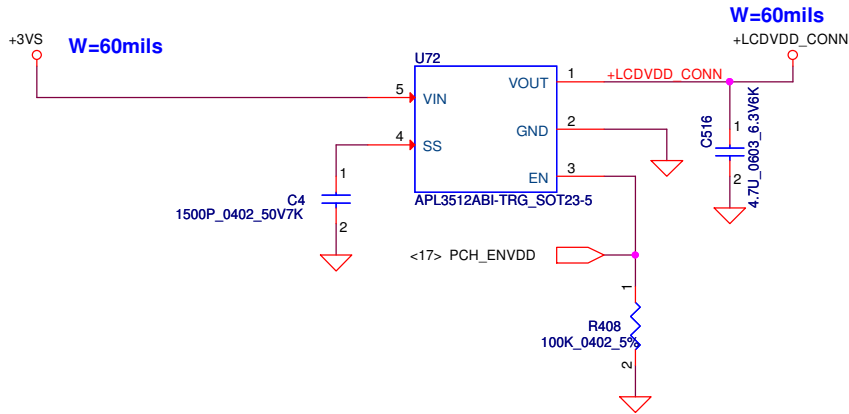
On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLEXP, VCCAPLLDMI2, VCCAPLLSATA

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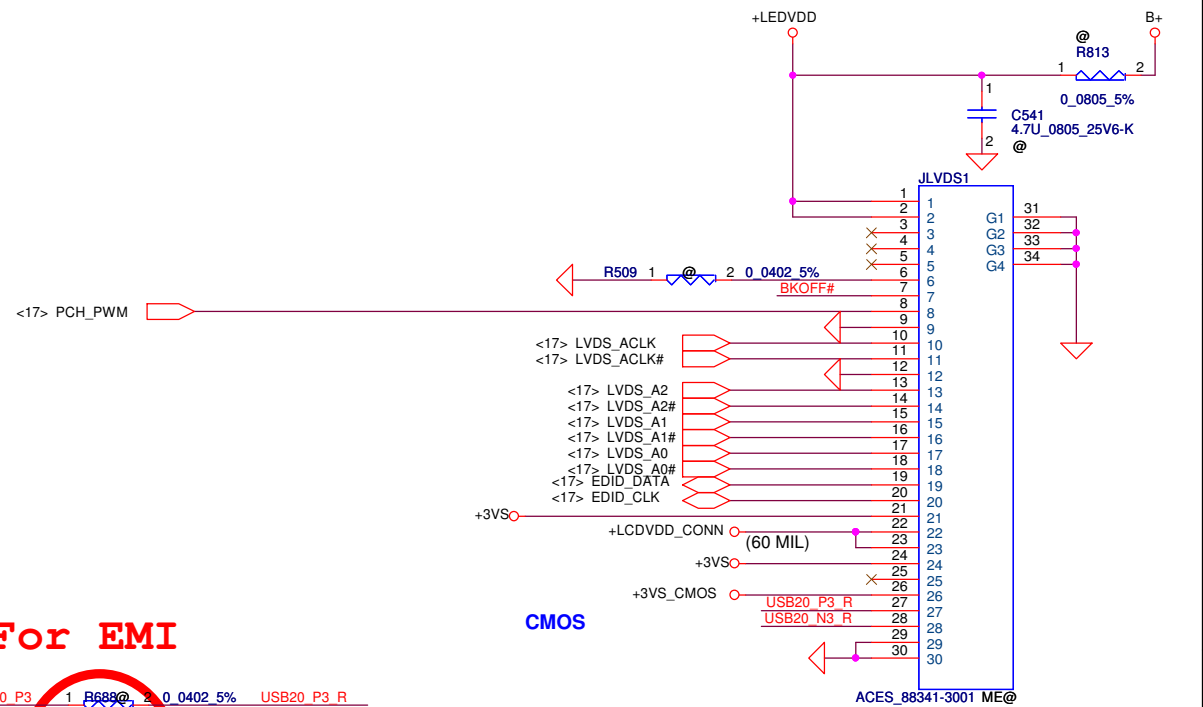


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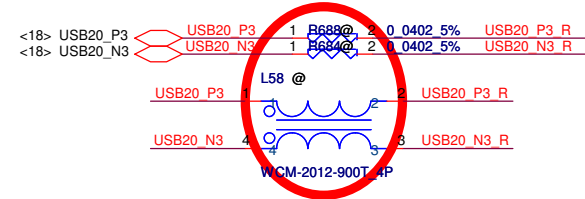
LCD POWER CIRCUIT



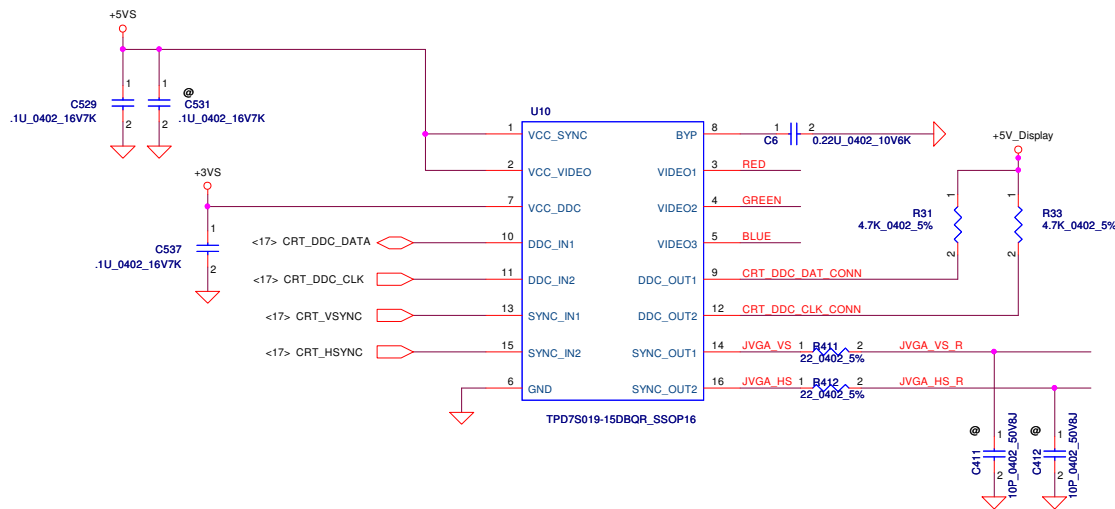
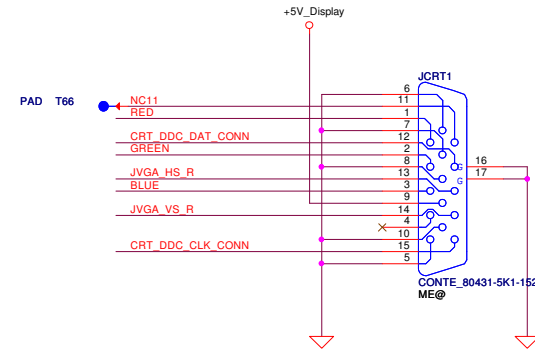
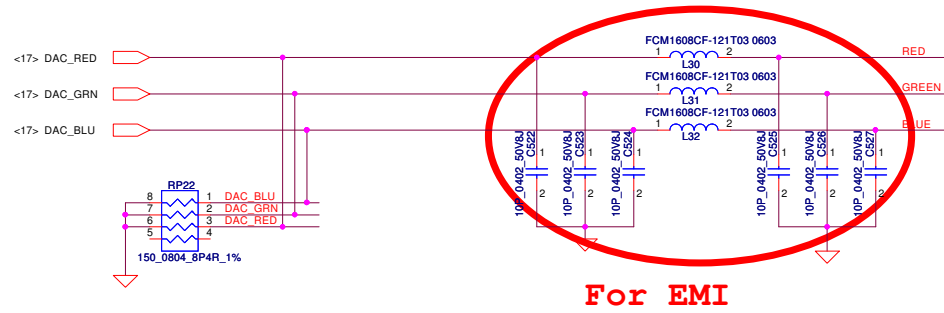
LCD Conn.



For EMI

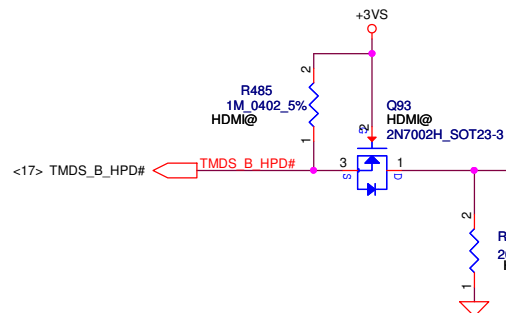
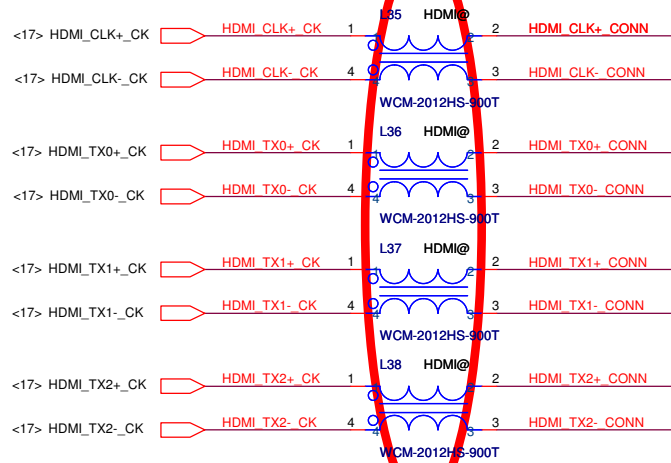


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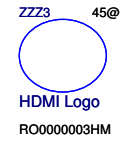


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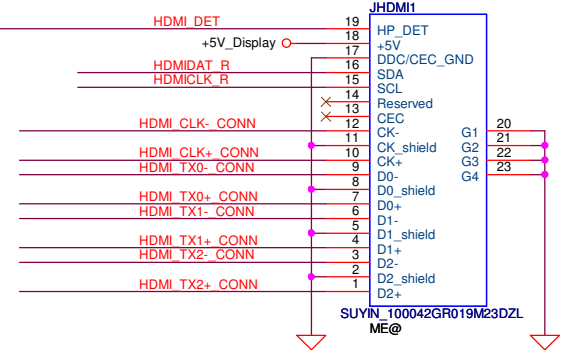
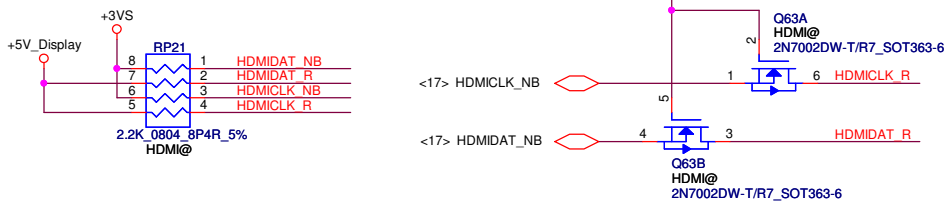
For EMI



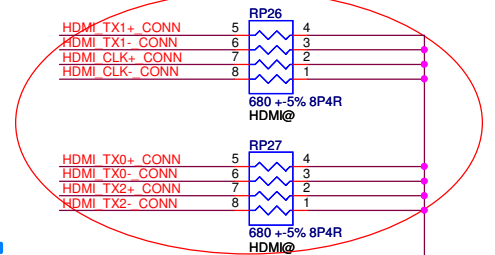
For CRT and HDMI



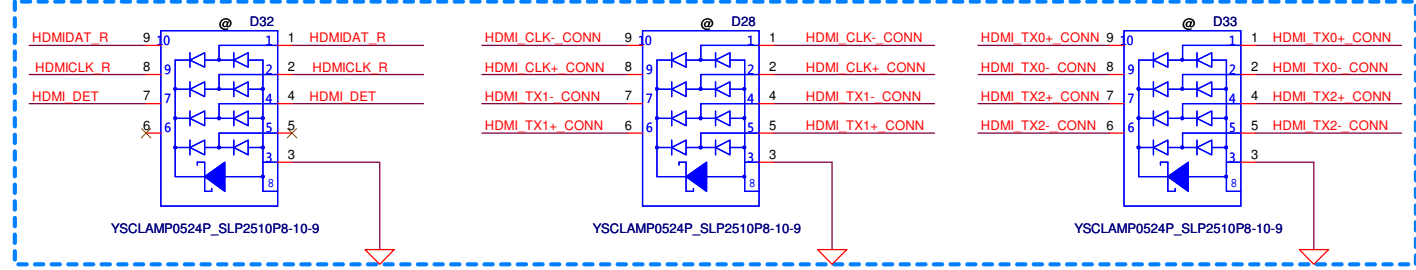
Pull up R for PCH OR VGA SIDE



DVT

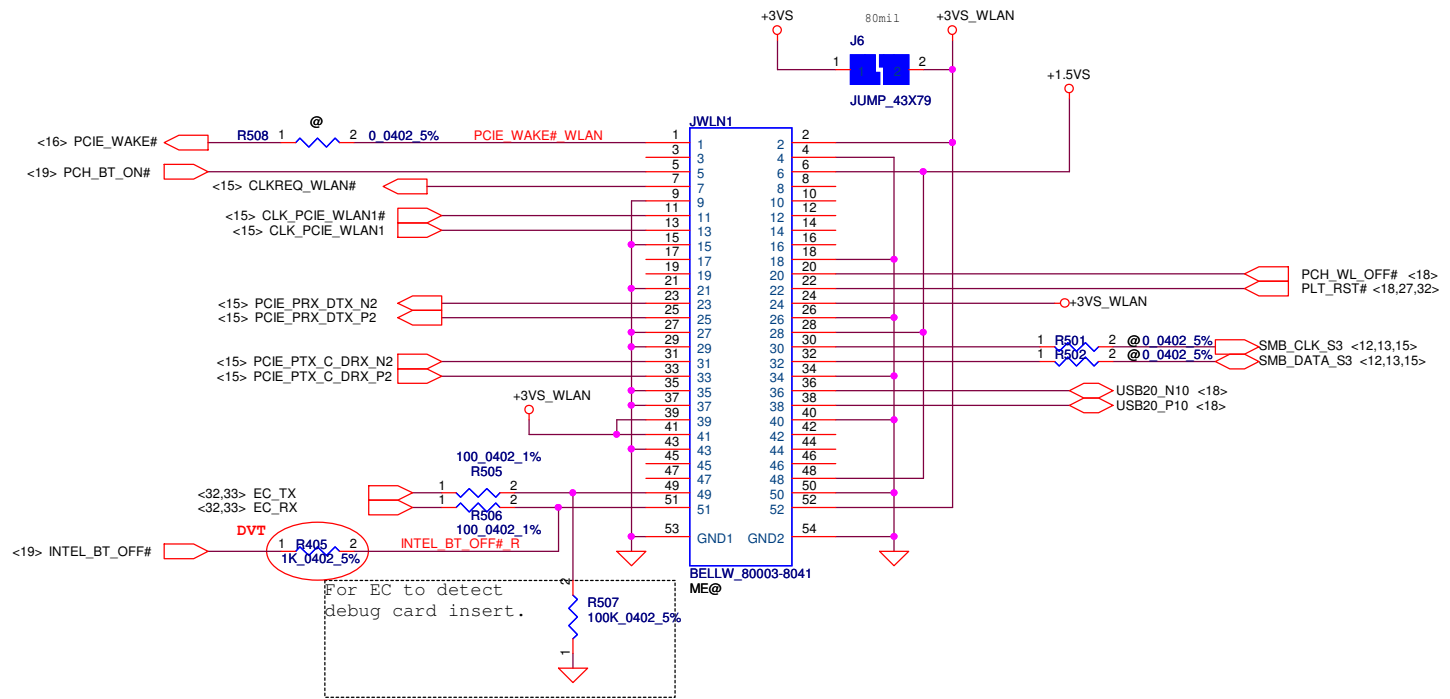


ESD



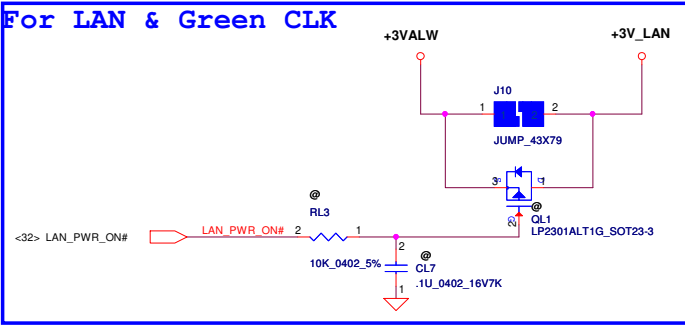
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Mini Card for WLAN/WiMAX(Half)

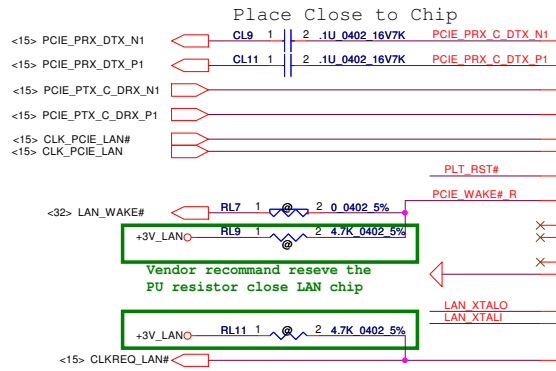
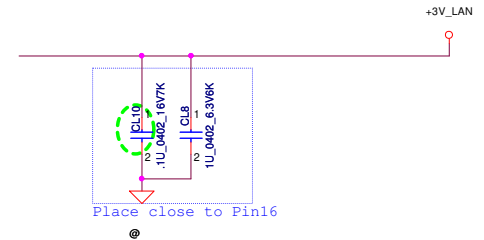
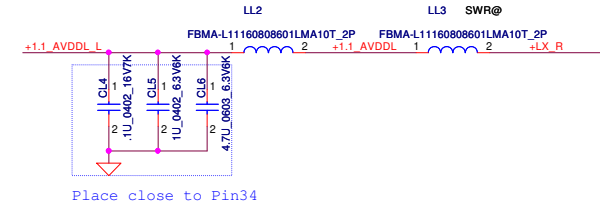
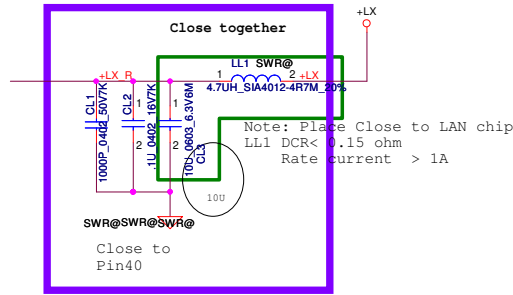
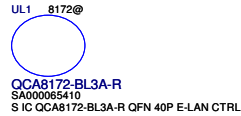
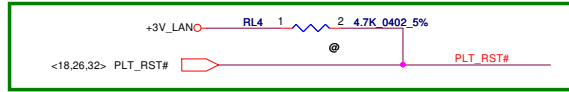


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For LAN & Green CLK

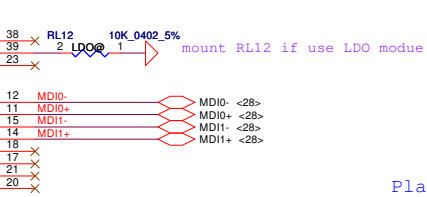
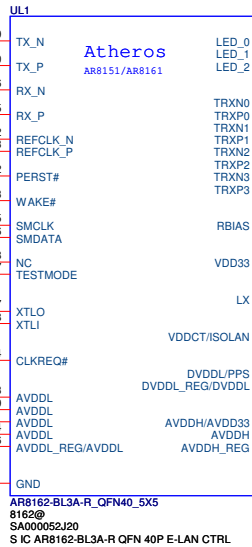


Vendor recommend reseve the PU resistor close LAN chip

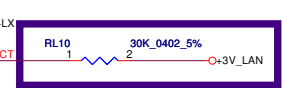


Vendor recommend reseve the PU resistor close LAN chip

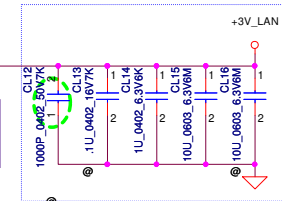
Near Pin13, Near Pin19, Near Pin31



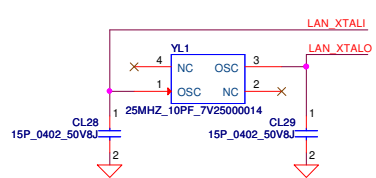
Place Close to PIN1



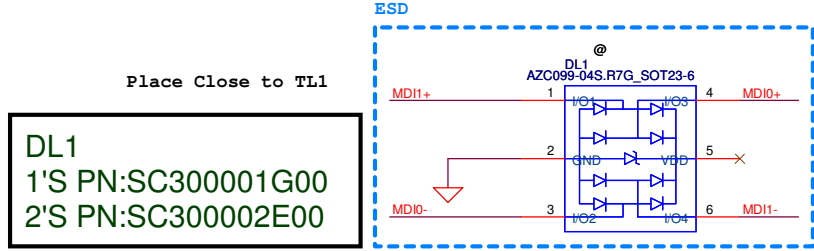
Near Pin9, Near Pin22, Near Pin37



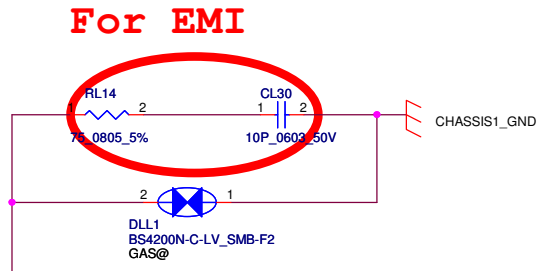
don't @ (could be B C cost done)



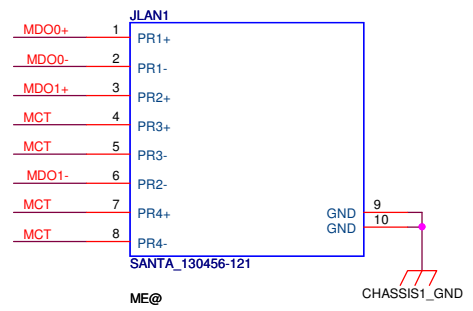
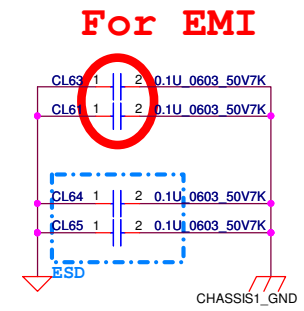
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
				LAN-AR8162/8172	
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Size	Document Number	Date		Rev	
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Date		Sheet		of	
		27		60	



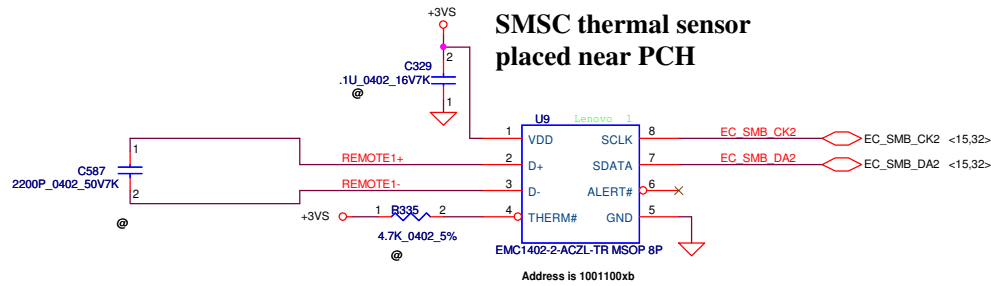
Reserve gas tube for EMI go rural solution



Place Close to TL1

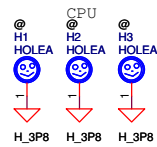
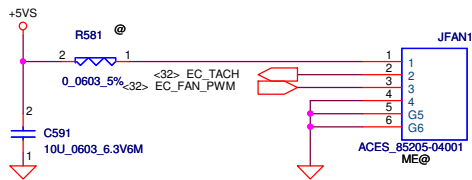


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				Date:	Wednesday, February 27, 2013
				Sheet	28 of 60



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

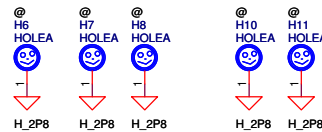
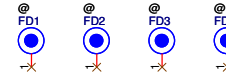
FAN1 Conn



A



C



D



E



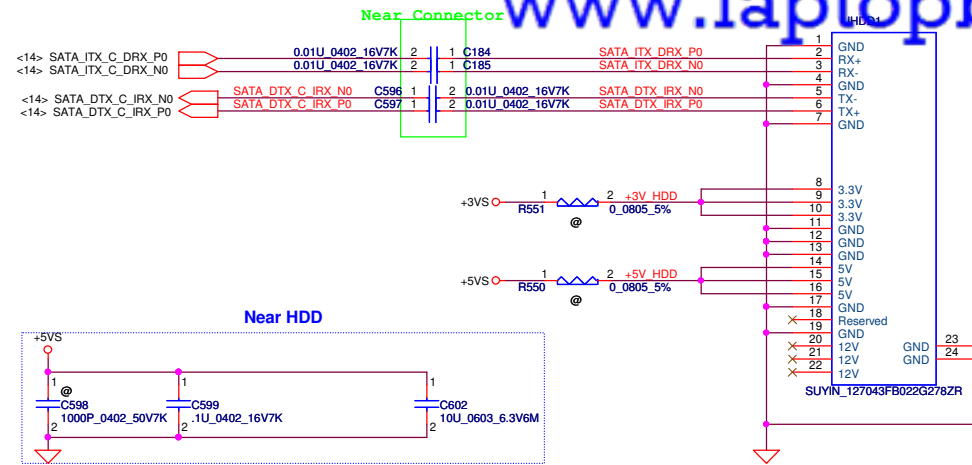
F

2P8 * 9 pcd

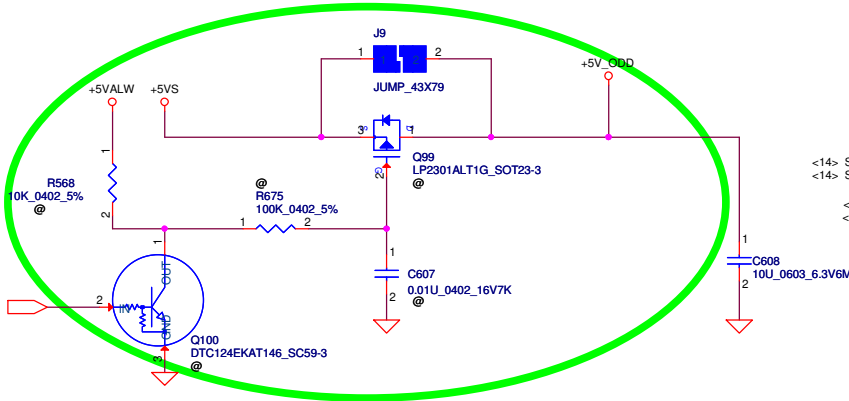
M/B 橢圓孔

M/B 圓孔

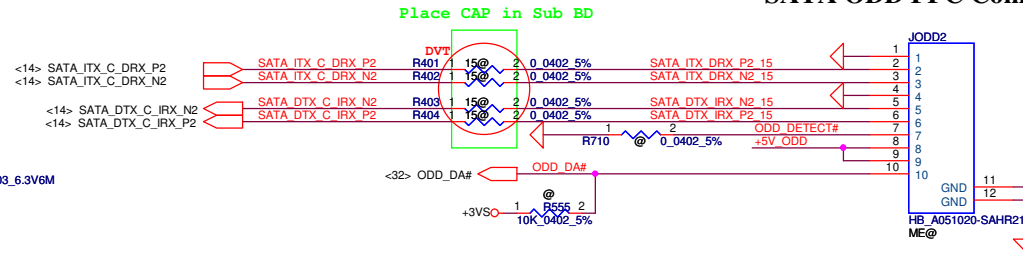
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	
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			Document Number	LA-9632P
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ODD Power Control

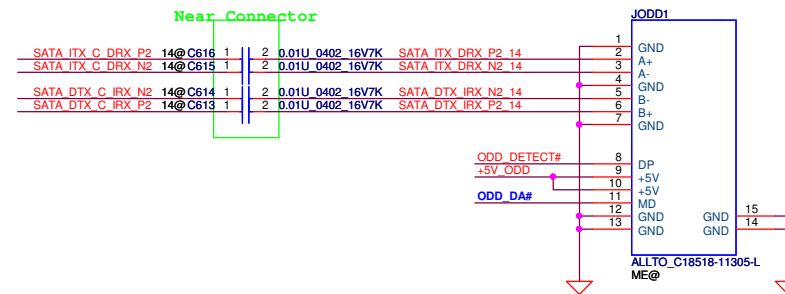


FOR 15" SATA ODD FFC Conn.



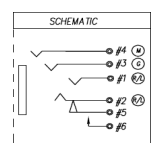
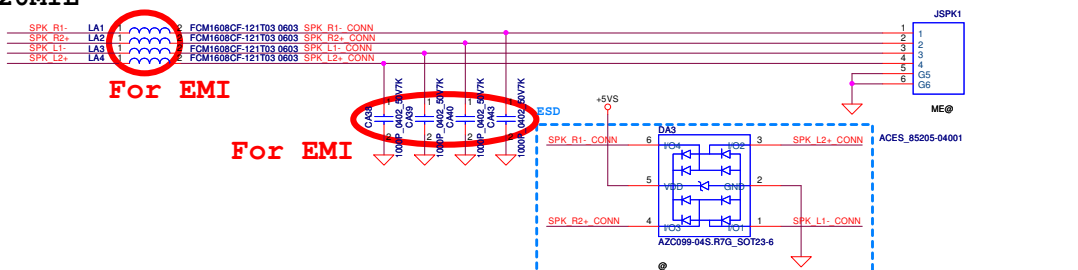
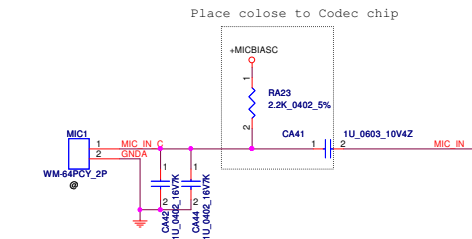
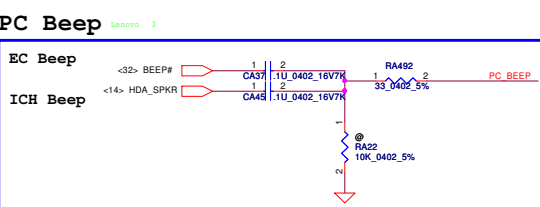
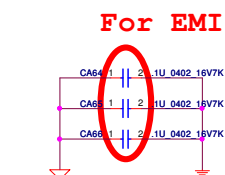
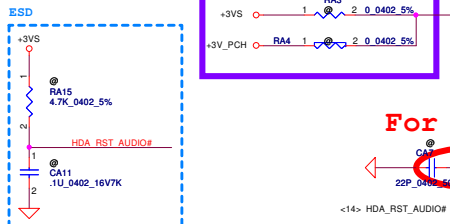
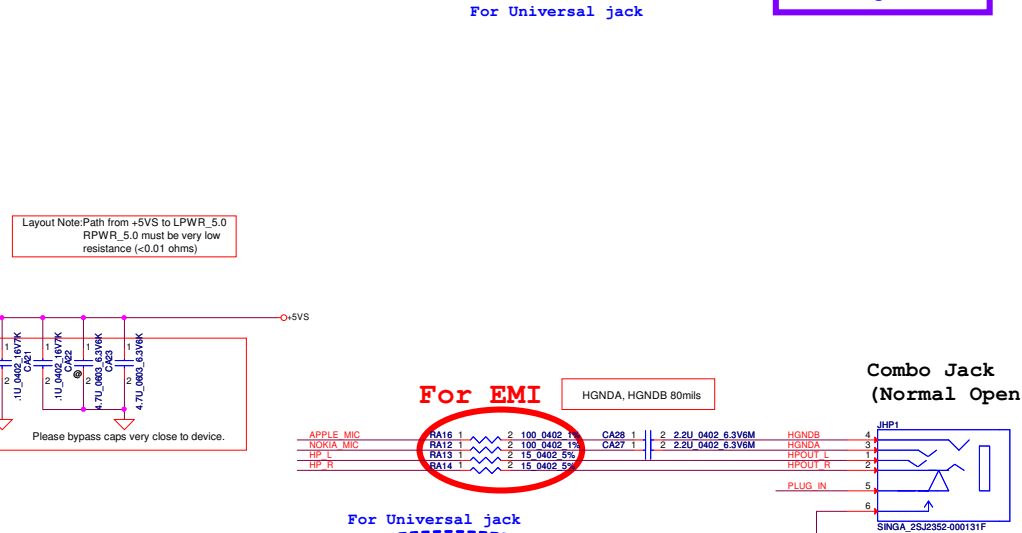
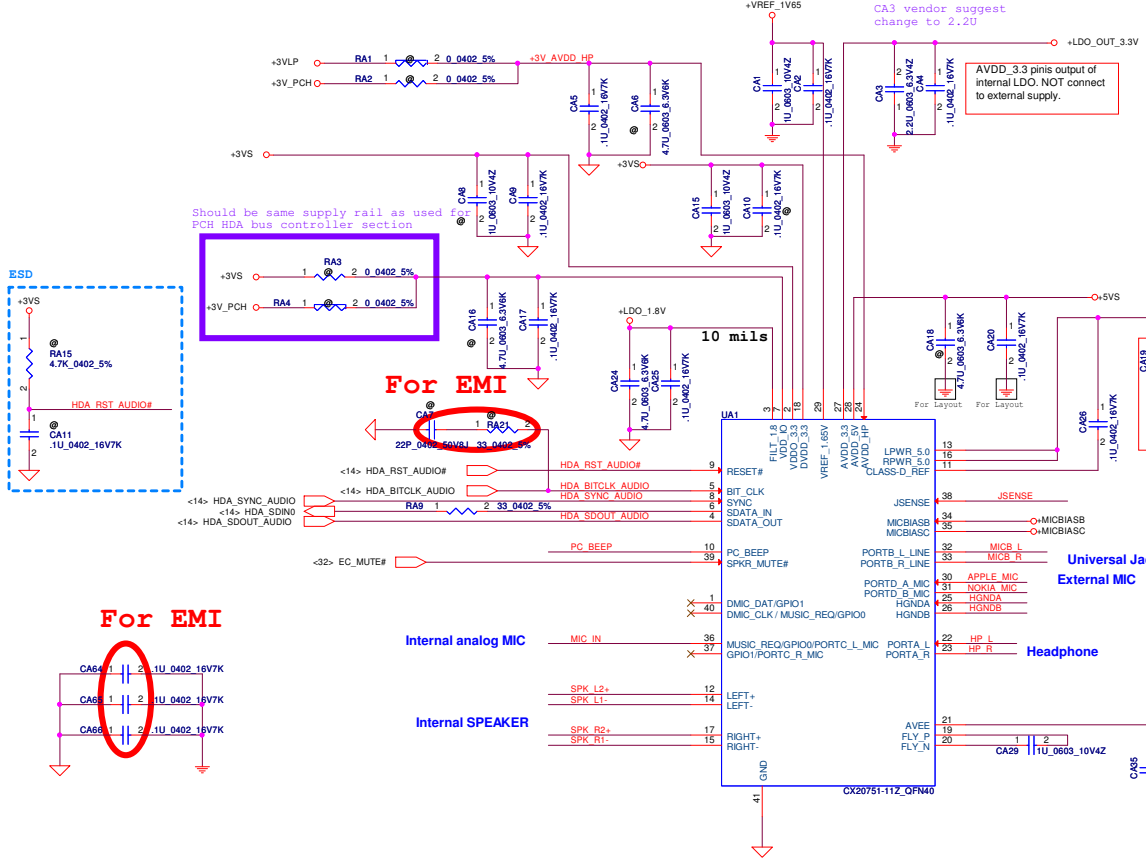
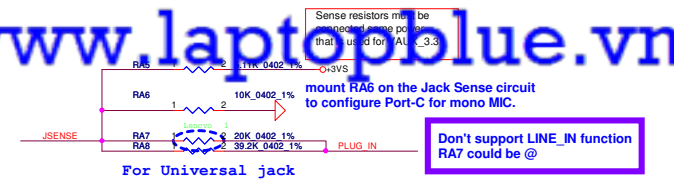
Co-lay

FOR 14" SATA ODD Conn.



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Compal Electronics, Inc. HDD/ODD/BT Connector			Size: Custom Document Number: LA-9632P Date: Wednesday, February 27, 2013	Rev: 1.0 Sheet: 30 of 60

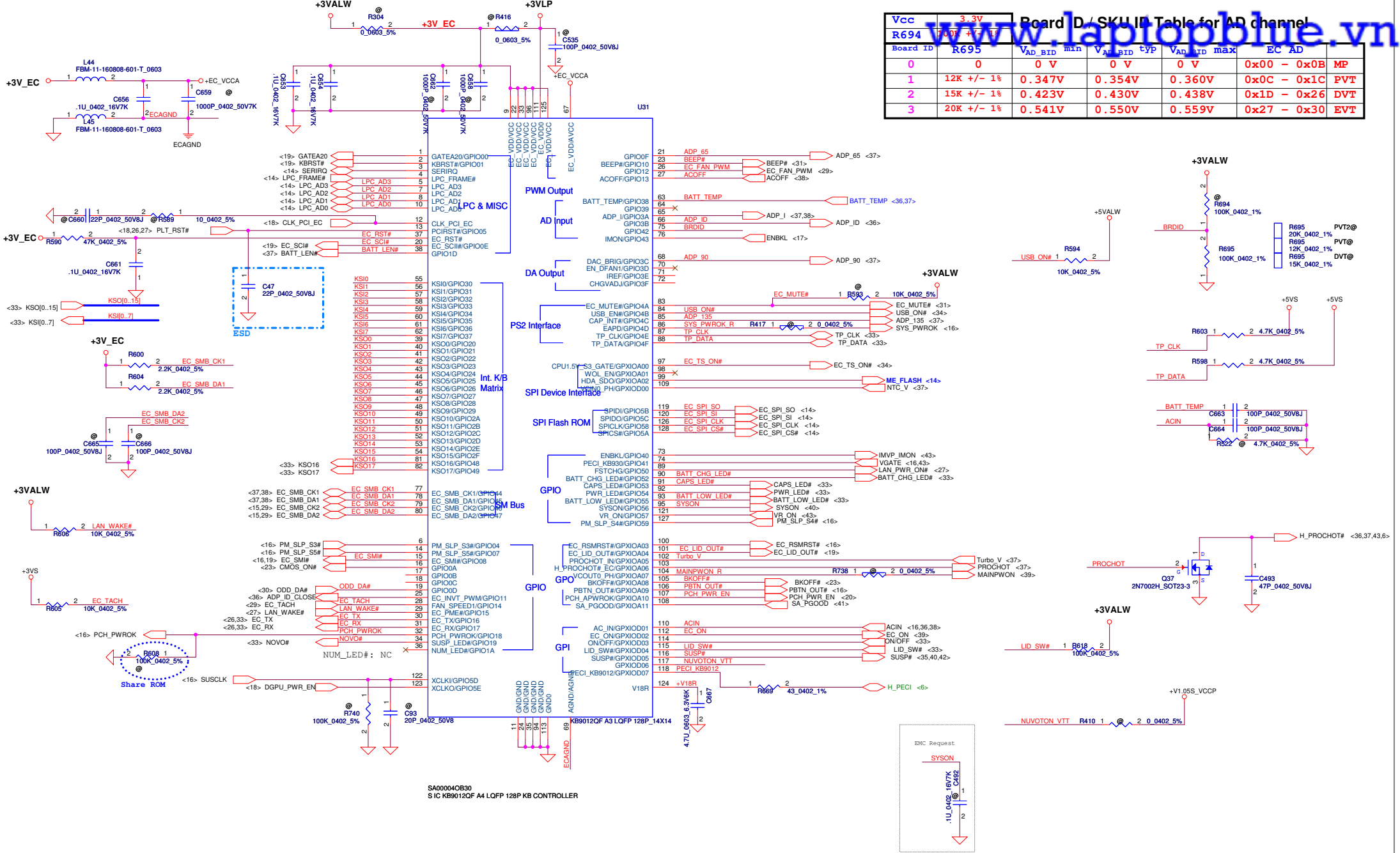
CX20751
 High Definition Audio Codec SoC
 With Integrated Class-D Stereo
 Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).



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Size	Custom	Rev	1.0	Date: Tuesday, March 05, 2013 Sheet 31 of 60

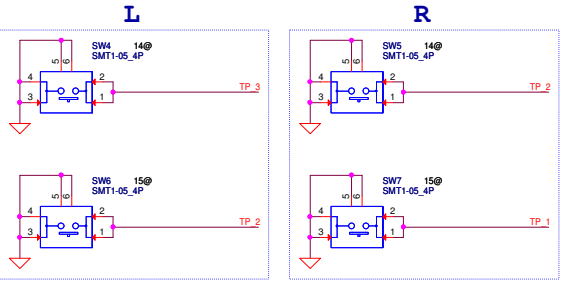
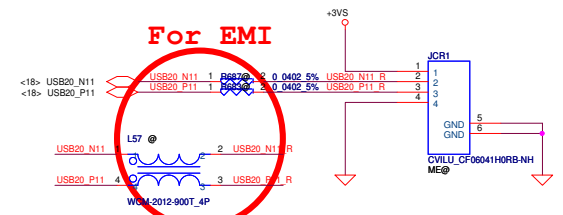
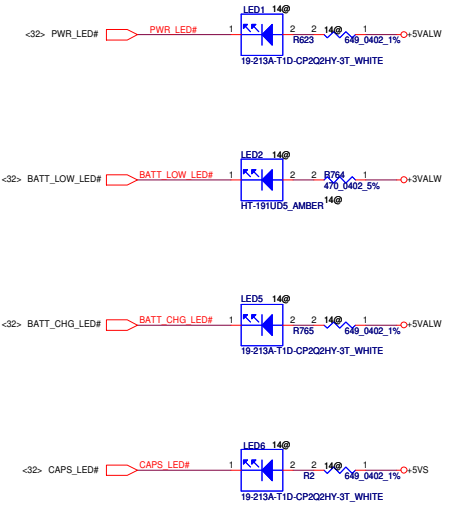
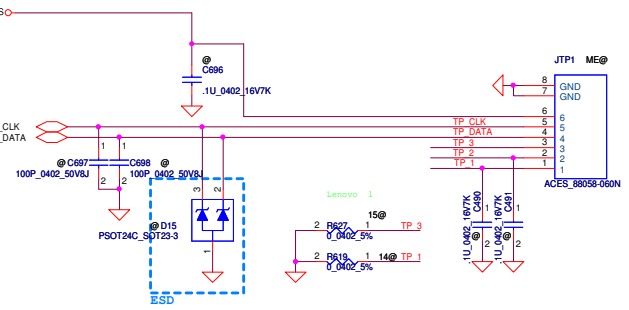
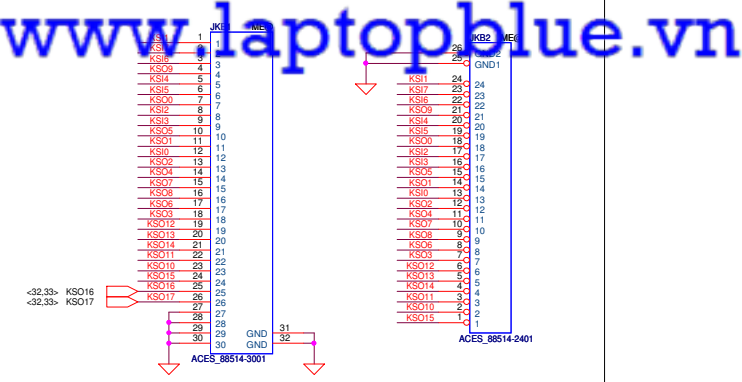
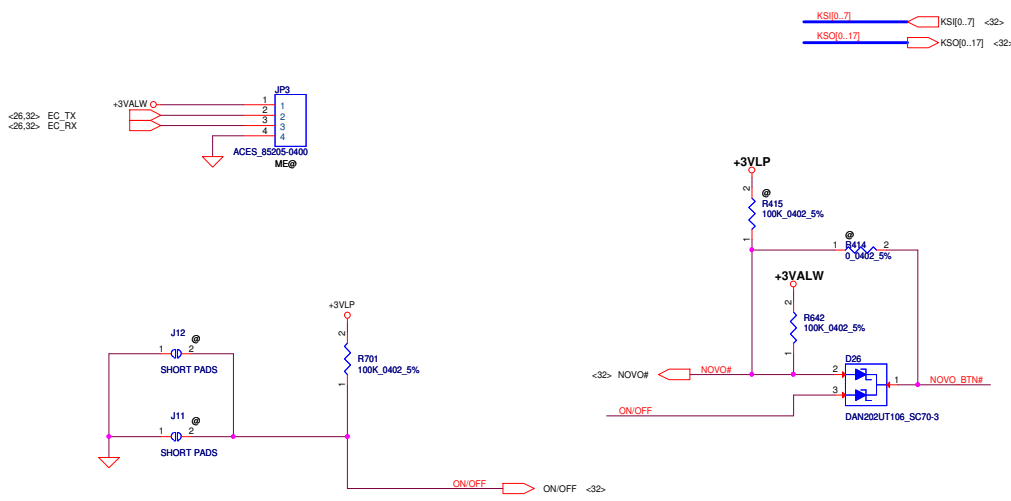
Board D / SKU ID Table for AD channel

Vcc	3.3V	Board D / SKU ID Table for AD channel				
R694	R695	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD	
0	0	0.0V	0.0V	0.0V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT

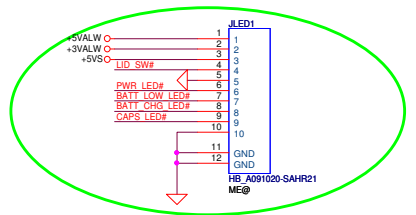
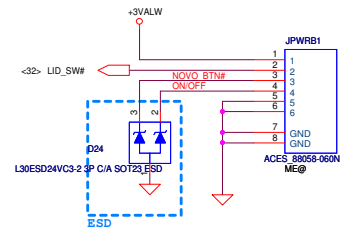


SA00004B30
S1C KB9012QF A4 LQFP 128P KB CONTROLLER

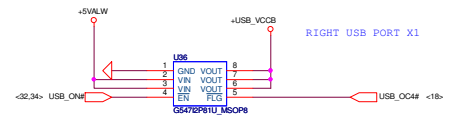
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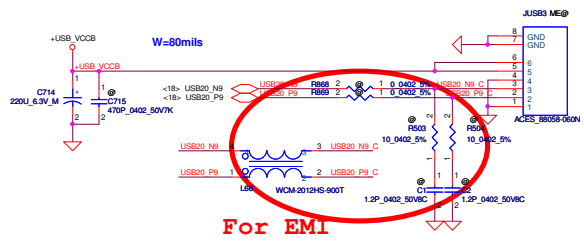
15/17"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND



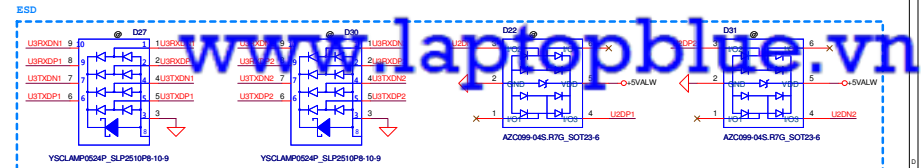
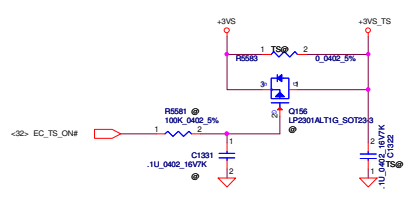
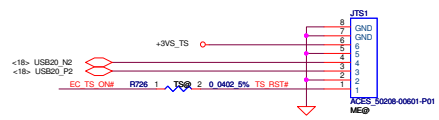
Ext. USB2.0



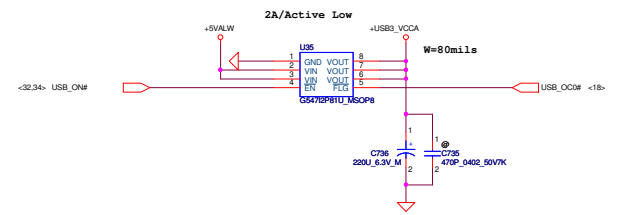
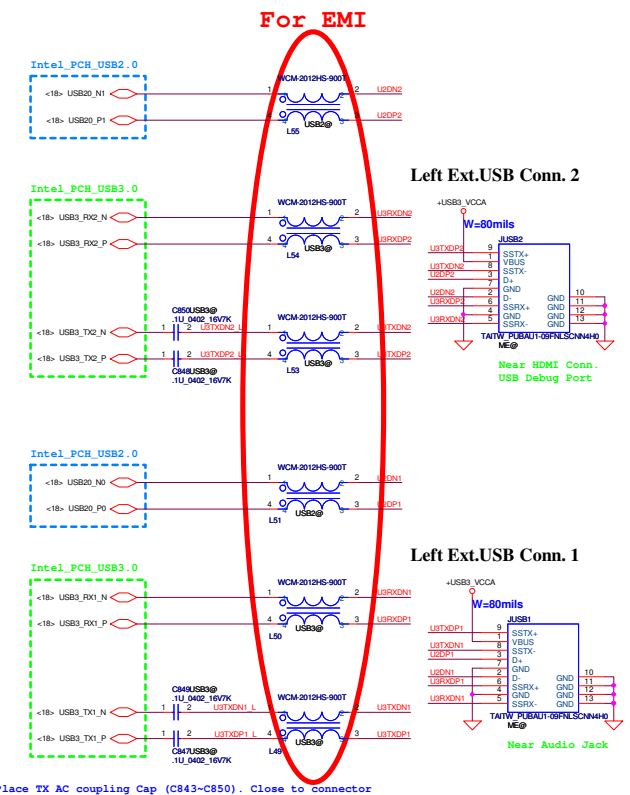
Right Ext.USB Conn.



Touch Screen

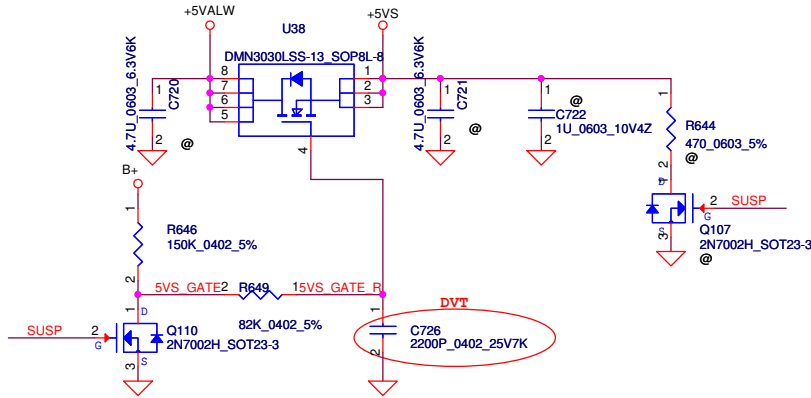


USB3.0

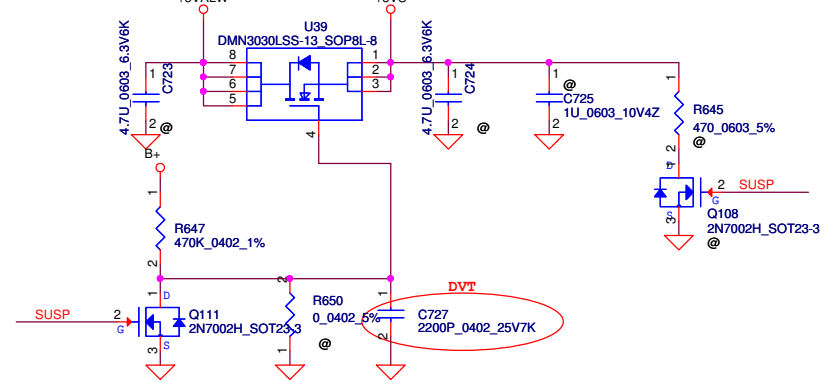


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				USB3.0/Left USB Ports
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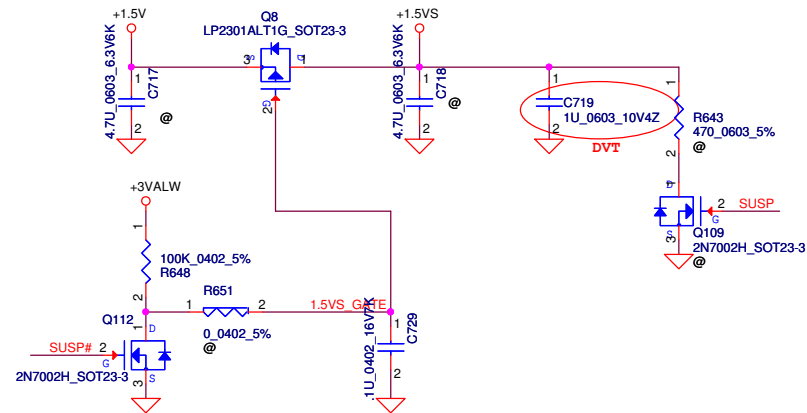
+5VALW to +5VS



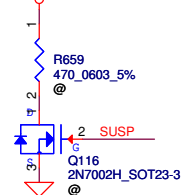
+3VALW to +3VS



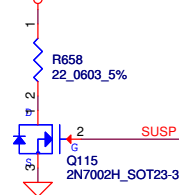
+1.5V to +1.5VS



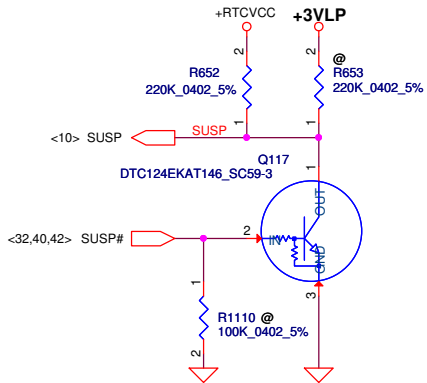
+V1.05S_VCCP



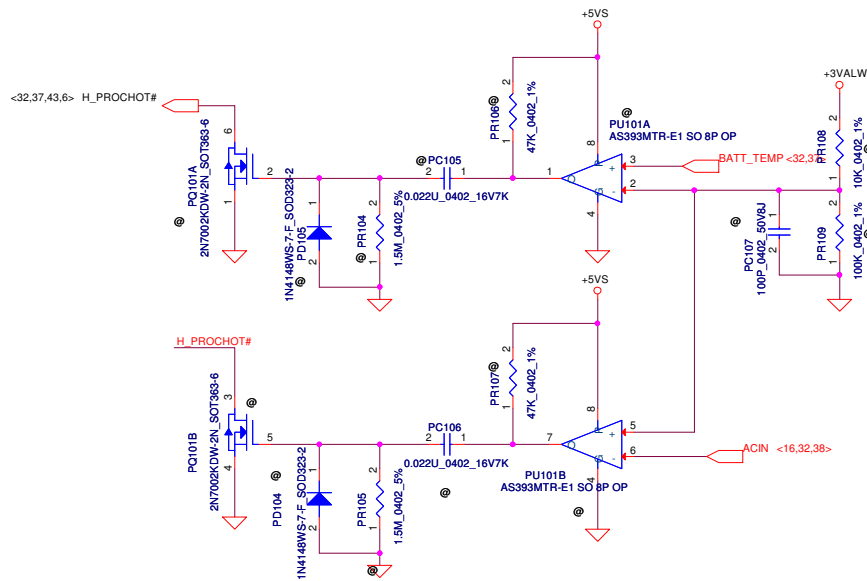
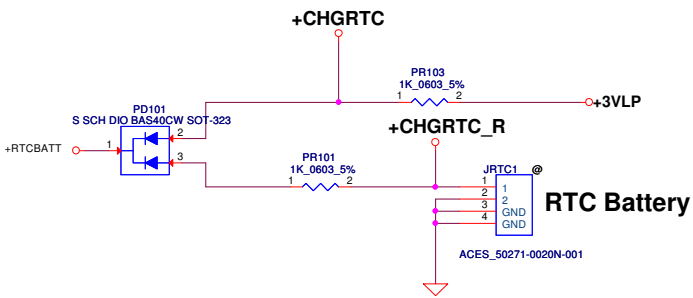
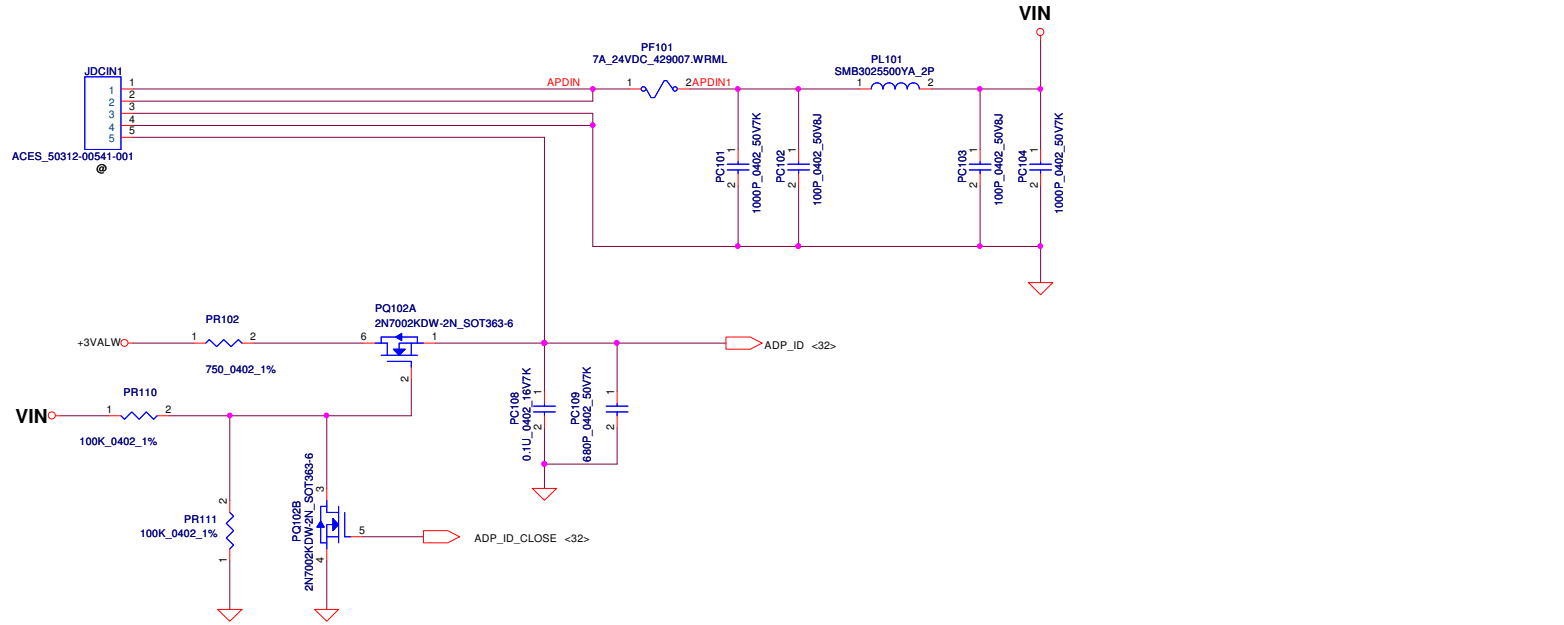
+0.75VS



+3VLP



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				Custom	1.0
				LA-9632P	
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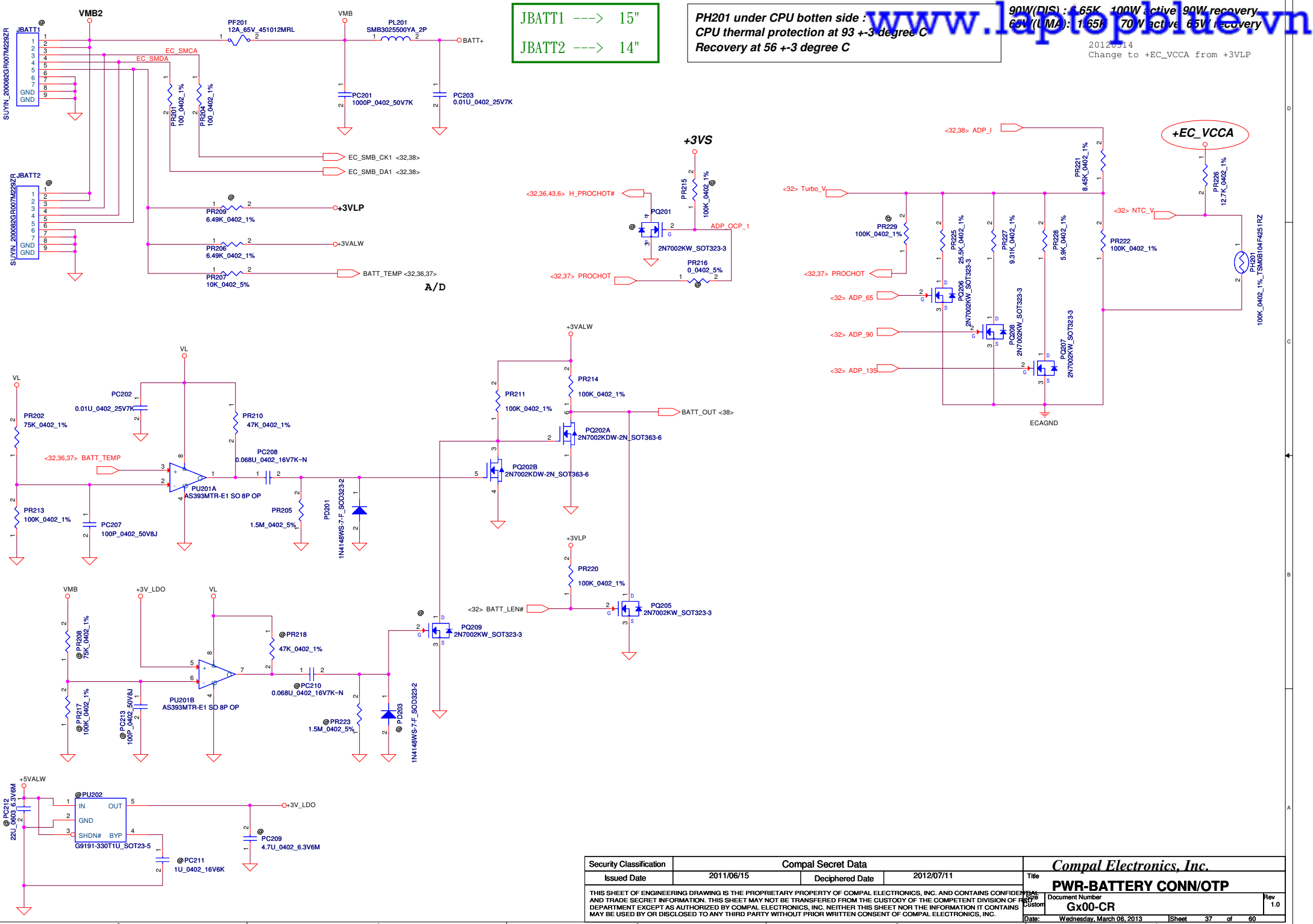


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				Rev 1.0
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PH201 under CPU bottom side :
 CPU thermal protection at 93 +3 degree C
 Recovery at 56 +3 degree C

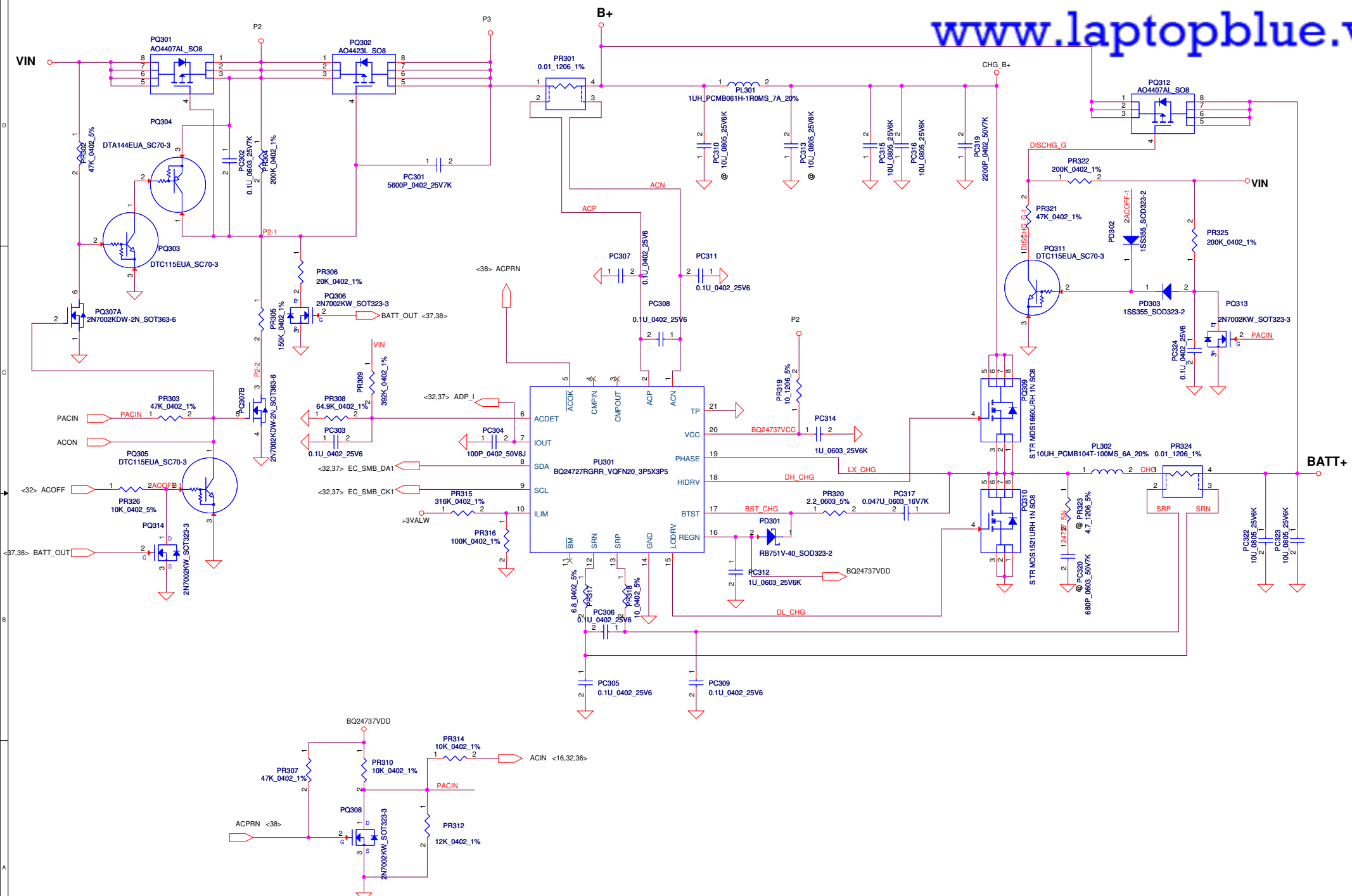
90W(DIS) : 65K 100W active 90W recovery
 65W(LMA) : 1.65I 70V active 65V recovery
 20120514
 Change to +EC_VCCA from +3VLP

JBATT1 ---> 15"
 JBATT2 ---> 14"

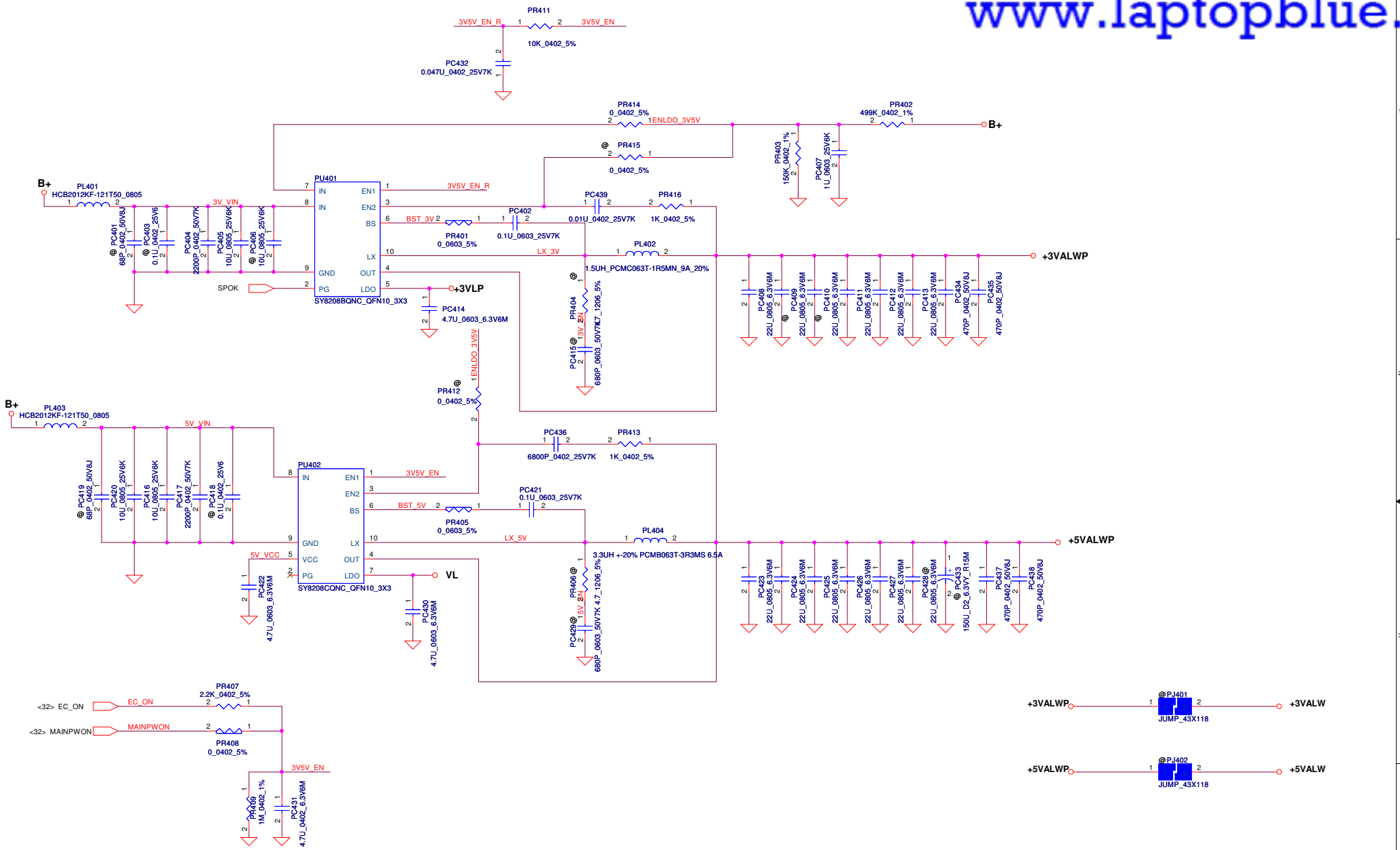


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Compal Electronics, Inc.	
PWR-BATTERY CONN/OTP	
Document Number	Rev
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Date: Wednesday, March 08, 2013	Sheet 37 of 60



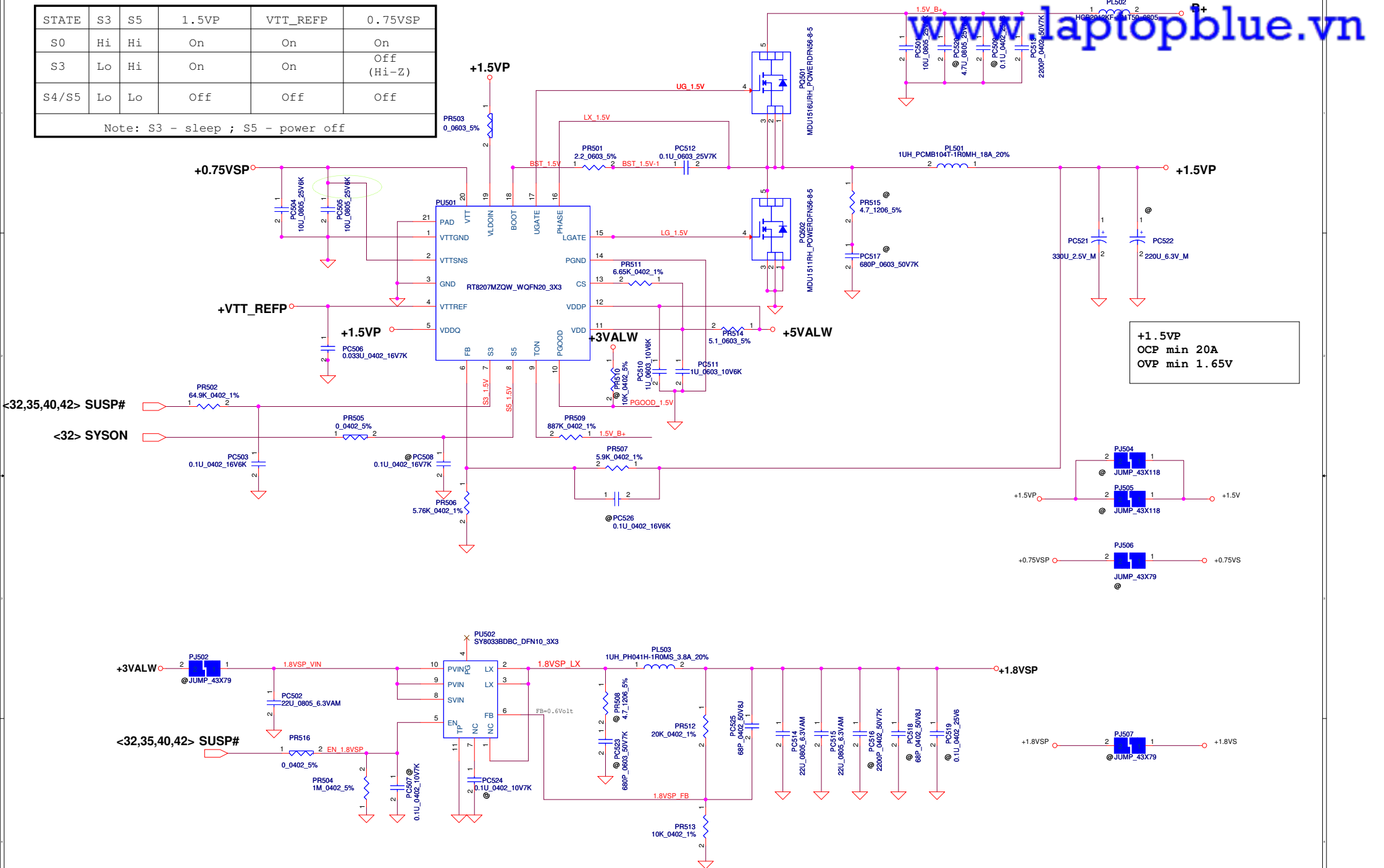
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
				CHARGER	
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



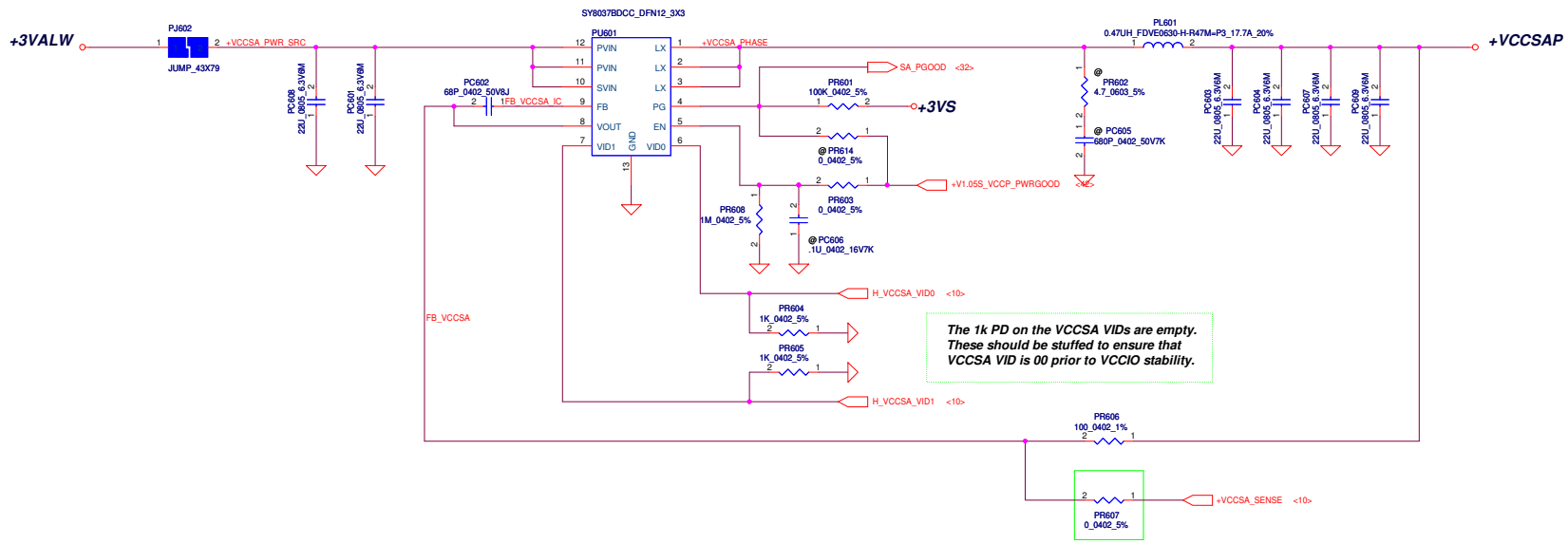
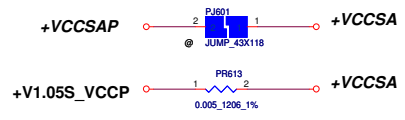
+1.5VP
 OCP min 20A
 OVP min 1.65V

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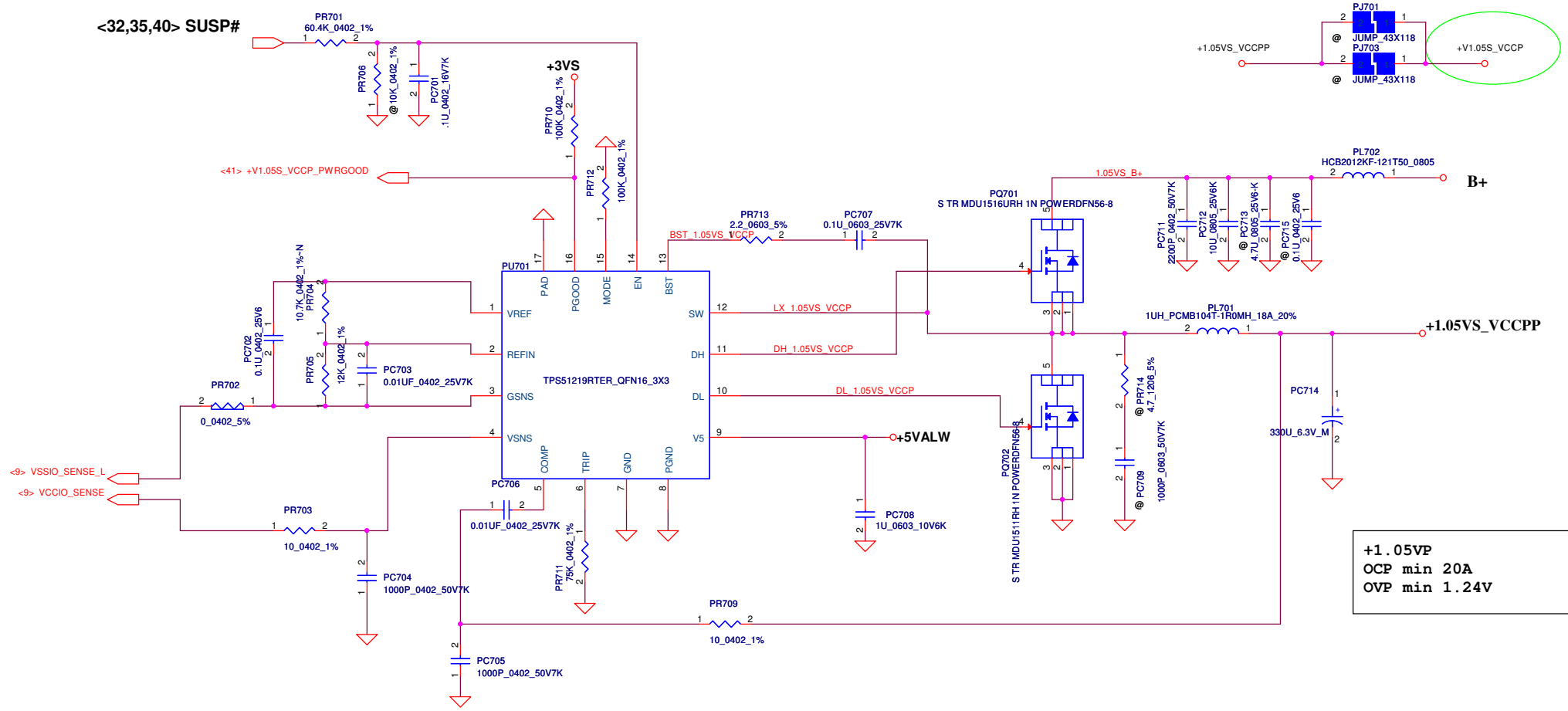
Compal Electronics, Inc.	
+1.5VP/+1.8VSP	
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

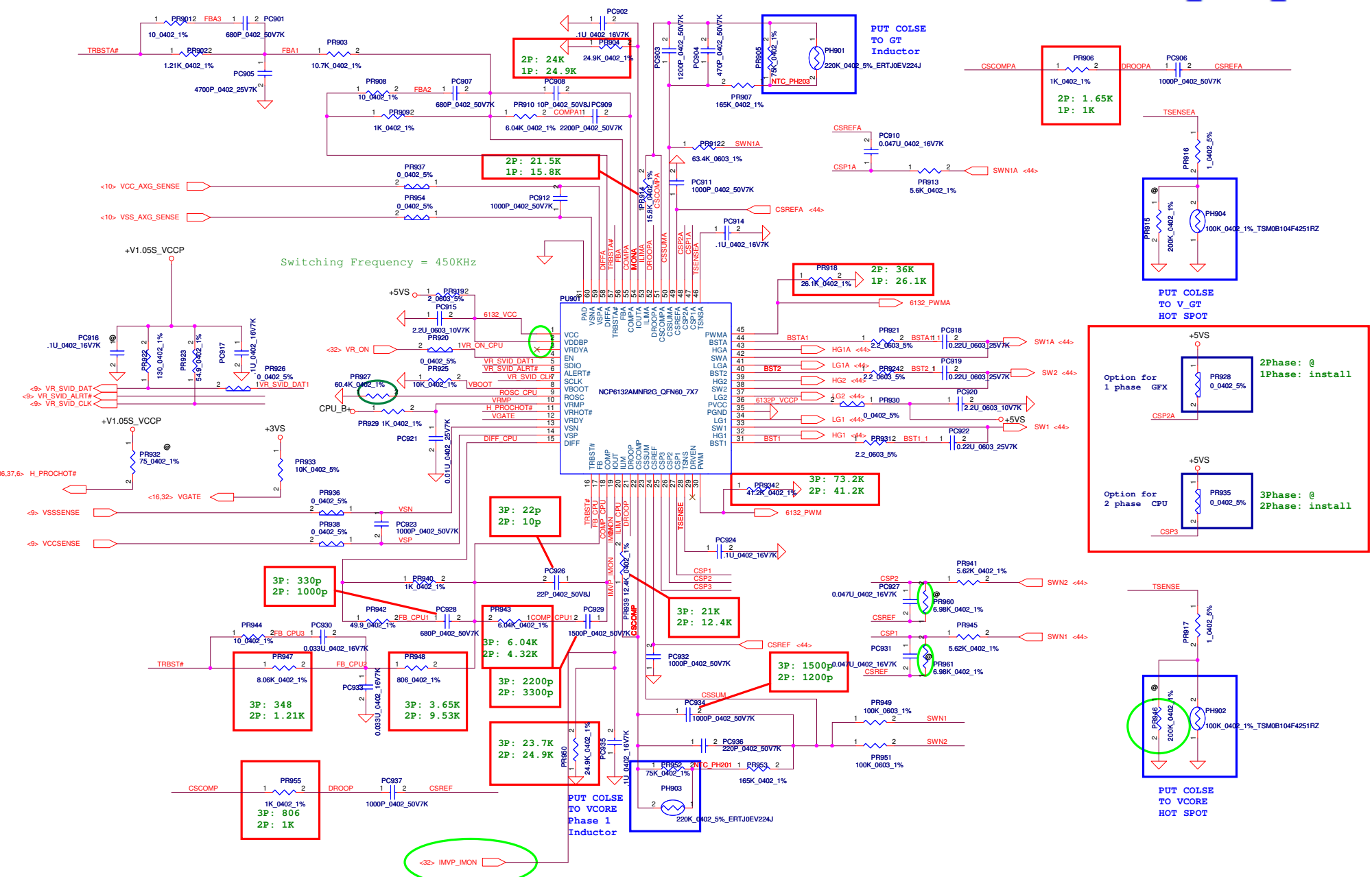
output voltage adjustable network



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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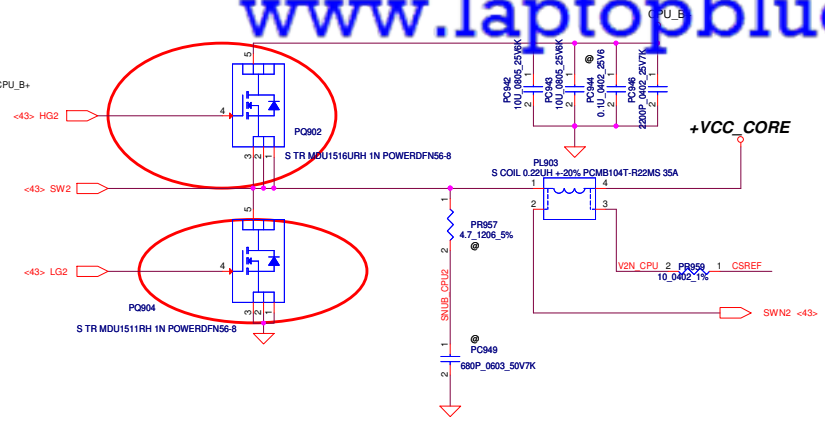
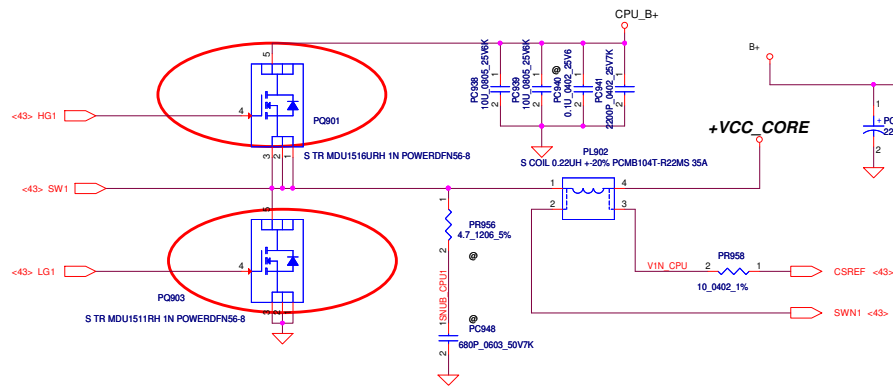


Option for 1 phase GFX
Option for 2 phase CPU

2Phase: @
1Phase: install

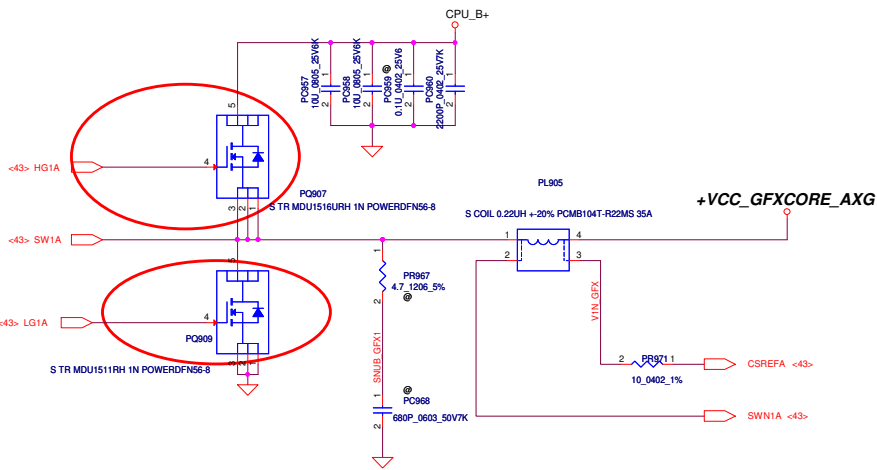
3Phase: @
2Phase: install

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QC 45W CPU
 VID1=0.9V
 IccMax=94A
 Icc_Dyn=66A
 Icc_TDC=52A
 R_LL=1.9m ohm
 OCP-110A

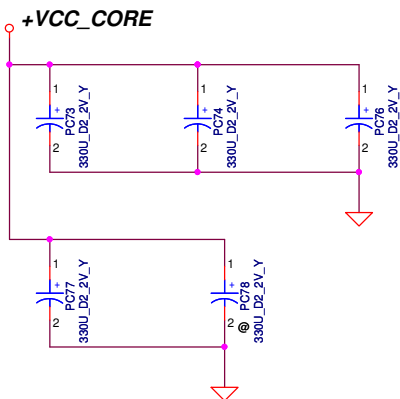
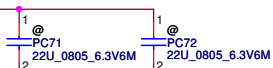
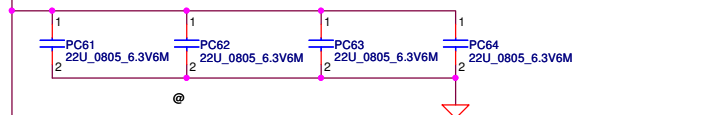
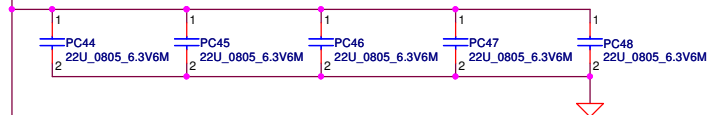
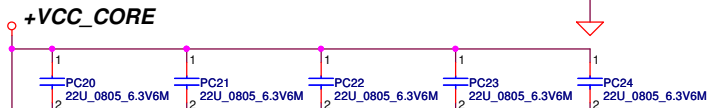
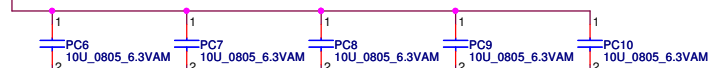
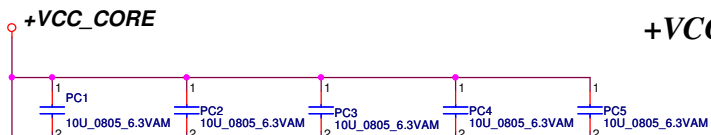
DC 35W CPU
 VID1=1.05V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP-65A



QC 45W GT2
 VID1=1.23V
 IccMax=46A
 Icc_Dyn=37A
 Icc_TDC=38A
 R_LL=3.9m ohm
 OCP-55A

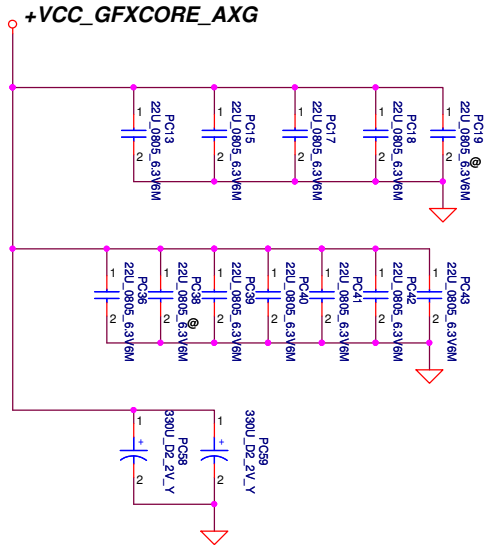
DC 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP-40A

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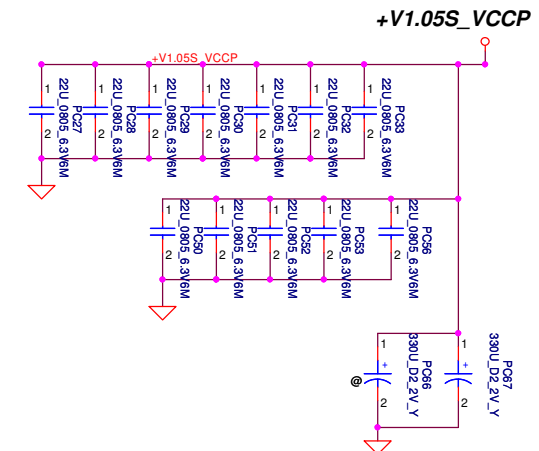
+VCC_CORE

+VCC_GFXCORE_AXG



Relwis 4.8514-GRV-PDBG-0.5 Table 5-8
www.laptopblue.vn

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

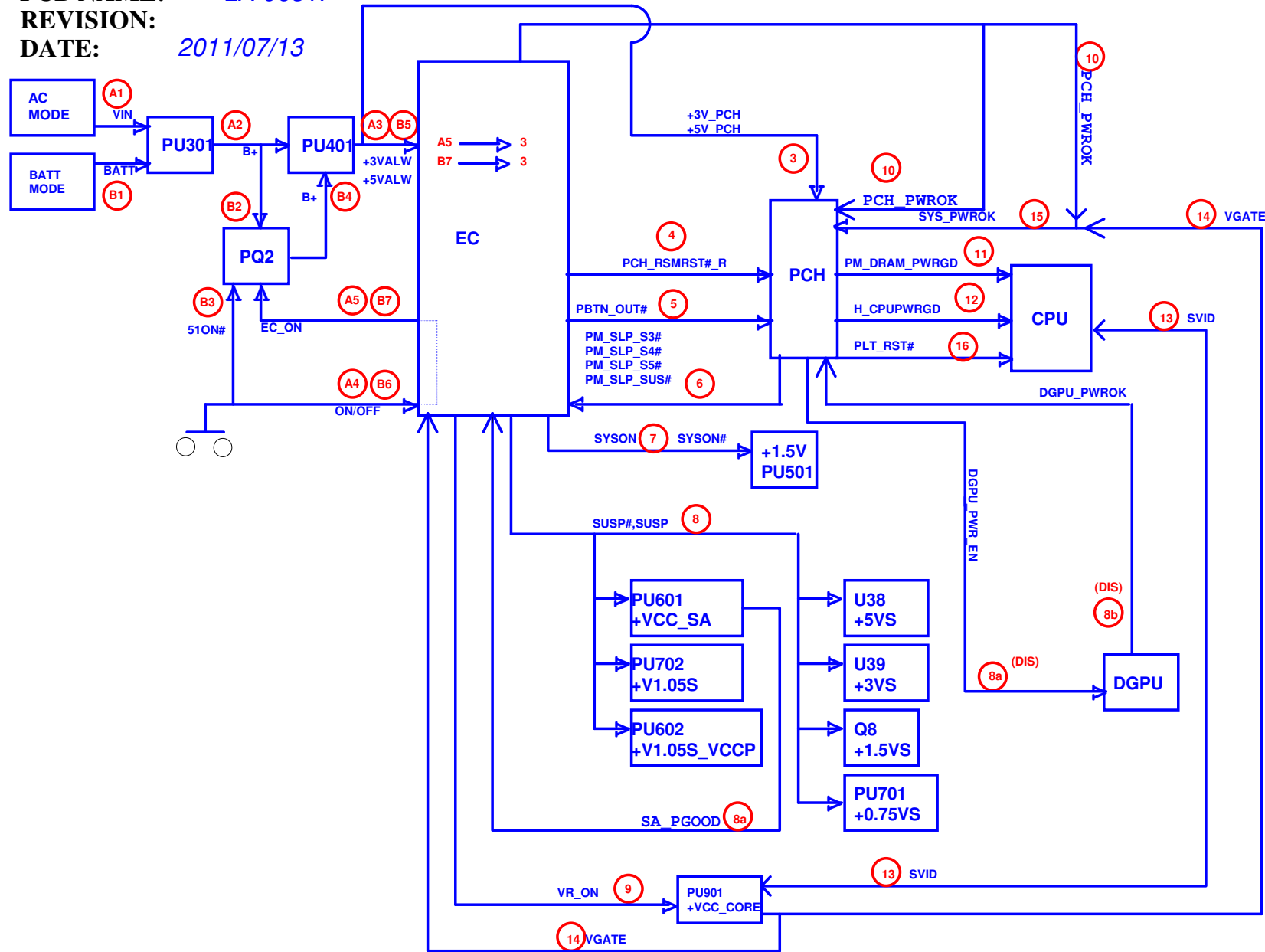


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				Size	Document Number	Rev
				LA-9632P		
Date:				Wednesday, February 27, 2013	Sheet	45 of 60

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 46	Add PR102, PC108, PC109	For ADP_ID pin detect
2	P. 47	Add PR225, PR227, PR228, PQ206, PQ207, PQ208	For protect adapter function
3	P. 49	Add PR410, PC433	For 3VALWP/5VALWP sequence
4	P. 49	Add PC434, PC435, PC436, PC437	For EMI solution
5	P. 49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple
6	P. 50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence
7	P. 51	Add PC637	For +0.95VGSP sequence
8	P. 54	Change PC907, PR912, PR927, PC928	For CPU Transient Compensation
9			
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				Custom	1.0
				C38-G series Chief River Schematic	
				Date:	Wednesday, February 27, 2013
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MODEL NAME: *Power Sequence Block Diagram*
 PCB NAME: *LA-9631P*
 REVISION:
 DATE: *2011/07/13*



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				Power sequence
				Rev 1.0
				Date: Wednesday, February 27, 2013 Sheet 47 of 60

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 36	Change C726, C727 to 2.2nF	For Sequence
2	P. 26	Add R405	For Intel Combo Card
3	P. 25	Delete RP19. Add RP26, RP27	Because ME modify MIC location
4	P. 14	Add R406, R407, R408, R409	Reserve for improvement factory processes
5	P. 32	Add EC_SPI_S0, EC_SPI_S1, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
6	P. 32	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
7	P. 32	Reserve R410	Reserve Pull-high for GPIO
8	P. 5-22	Change footprint of JCPU1, U4	For Lenovo rule
9	P. 21	Add Q21, R40, C237, R225, C243	Reserve for power consumption
10	P. 24	Add R411, R412, C411, C412	Reserve for EMI
11	P. 32	Add ADP_65 to EC Pin.21	For adapter protection
12	P. 32	Add ADP_90 to EC Pin.68	For adapter protection
13	P. 32	Add ADP_135 to EC Pin.85	For adapter protection
14	P. 32	Change EC_FAN_PWM from EC Pin. 34 to EC Pin.26	For common design
15	P. 32	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
16	P. 32	Add ADP_ID to EC Pin.66	For adapter
17	P. 32	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design
18	P. 32	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
19	P. 32	Add VGATE to EC Pin.74	Reserve for sequence
20	P. 32	Add SYS_PWROK to EC Pin.86	Reserve for sequence
21	P. 32	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design
22	P. 32	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
23	P. 32	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design

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Item	Page	MODIFICATION LIST	PURPOSE
1	P. 30	Delete R416, Add J9	No need Zero ODD Function
2	P. 26	Reserve R508	For leakage current issue of Atheros WLAN
3	P. 23	Add R509	protect BKOFF# damage
4	P. 32	Reserve R416	Reserve +3VLP power rail to EC
5	P. 32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P. 32	Change EC_SMB_CK1 & EC_SMB_DAI power rail to +3V_EC	Using power rail which the same with EC.
7	P. 14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P. 14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P. 31	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P. 32	Reserve resistance in EC for share ROM.	Follow common design
3	P. 41	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU

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				LA-9632P	1.0
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