Compal confidential

Schematics Document

Mobile Arrandale rPGA989 with Intel PCH(Ibex Peak-M) core logic

2009-10-23 Rev 1.0

機密 等級 硬體二部
產出人員
產出日期
解密日期

Security Classification	Compal Secret Data		
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Title: Cover Sheet		
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Fan conn Page 6

Calpella Consumer 14" UMA +Switchable

Mobile Arrandale
2C CPU + GMCH
Socket-rPGA989
Page 6,7,8,9,10

CK505 32QFN
Clock Generator
ICS9LRS3197AKLFT
P19

ATI M93
page 24,25,26,27,28

PCIE-Express 16X

VRAM DDR3
512MB
page 29

Dis LCD Conn. page 21
Dis MUX UMA

Dis CRT page 20
Dis MUX UMA

DDR3 1066/1333 MHz 1.5V
Dual Channel

DDR3 SO-DIMM X2
BANK 0, 1, 2, 3
P17, 18

FDI BUS
DMI X4

Intel PCH
Ibex Peak-M
FCBGA 951
Page 11,12,13,14,15,16

Dis HDMI Conn. page 23

PCI-E BUS*4

8111DL VB
8103EL
(10/100 /Giga LAN) P32

Mini-Card
WLAN P31

Mini-Card
WWAN P31

New Card
USB2.0 X1 P31

RJ45/11 CONN P32

LPC BUS

SPI

SPI ROM 16M
MX25L1605DM2I-12G P38
4M Bytes

ENE
KB926
Version D2 P38

Touch Pad CONN. P40

Int.KBD P39

SPI ROM
WIESON G6179 P38
256K bits

USB2.0 X11

Azalia

SATA Master-1

SATA Slave

Mini-Card x 2 P31

USB conn x3 P37

BT Conn P37

USB Camera P21

Finger print P37

Cardreader P33

MDC Conn P34

Audio CKT
Codec_IDT92HD80 P34

Audio Jack P35

SATA HDD Connector P30

SATA ODD Connector P30

Multi-Bay P30

e-SATA Connector P37

USB Board Conn
USB conn x2 P37

Capsense switch Conn P40

RTC CKT. P11

LED P40

ACCELEROMETER
ST P30

K/B backlight Conn P40

DC/DC Interface CKT. P41

Dock P36
USB2.0*1
RGB
RJ45
SPDIF
MIC*1
LINE-OUT*1

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Title: Block Diagram

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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
SG@ :	means stuff when Switchable graphic
PA@ :	Only For PA
OPP@ :	Only For OPP
DIS@ :	means stuff when DIS only
DEBUG@ :	means stuff when need Mini Card LPC debud card
8111DL@ :	means stuff for 8111DL
8103EL@ :	means stuff for 8103EL

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Docking
USB-4	Camera
USB-5	WLAN
USB-6	X
USB-7	X
USB-8	MiniCard(WWAN/TV)
USB-9	New card
USB-10	Cardreader
USB-11	Finger Printer
USB-12	BT

PCIe assignment:

PCIe-1	WWAN
PCIe-2	WLAN
PCIe-3	LAN
PCIe-4	New card
PCIe-5	X
PCIe-6	X

SATA assignment:

SATA0	HDD
SATA1	ODD
SATA2	X
SATA3	X
SATA4	ESATA
SATA5	Mulit-Bay

SMBUS Control Table

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK CHIP	WLAN WWAN	M93 Thermal Sensor	NB10M-GE	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	PCH	V	X	X	V	V	V	X	X	X	V	V
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
		+3VS	+5VL		+3VS	+3VS	+3VALW			+5VL	+3VALW	+3VS

M93 SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
D_EDID_DATA D_EDID_CLK	M93	V	X	X
D_CRT_DDC_DATA D_CRT_DDC_DATA	M93	X	V	X
HDMIDAT_VGA HDMICLK_VGA	M93	X	X	V

Stencil Memo:

PA: PJ1, PJP903, PJP301, PJP302, PJP303, PJP304, PJP401, PJP601, PJP602, PJP603, PJP501, PJP901, PJP902

OPP: PJ1, PJP301, PJP302, PJP303, PJP304, PJP401, PJP601, PJP602, PJP603, PJP501, PJP901, PJP902, JP303

Stand-off Location: H12, H14

PCH I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
G sensor	1D	0 0 0 1 1 1 0 1

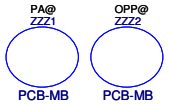
NAL70 SKUs

PCB part number

PCB DA80000GL00

PA DAZ0BI00200

OPP DAZ0BI00300



PCH version

A1 QV73 SA00002KV10

B0 QLLT SA00002KV30

B1 QMGS SA00002KV60

B3 QMNT SA00003N730

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Title: Notes List

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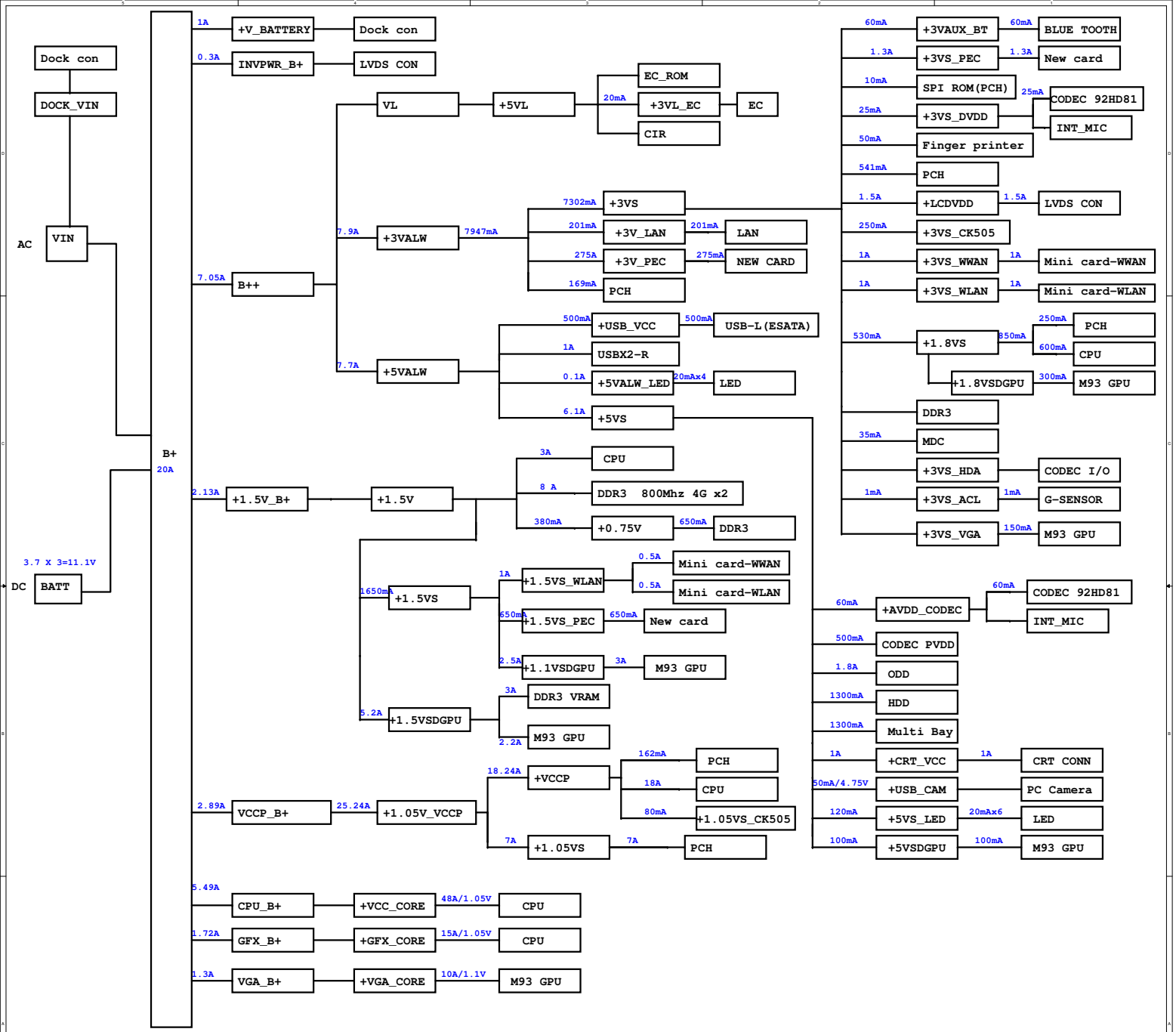

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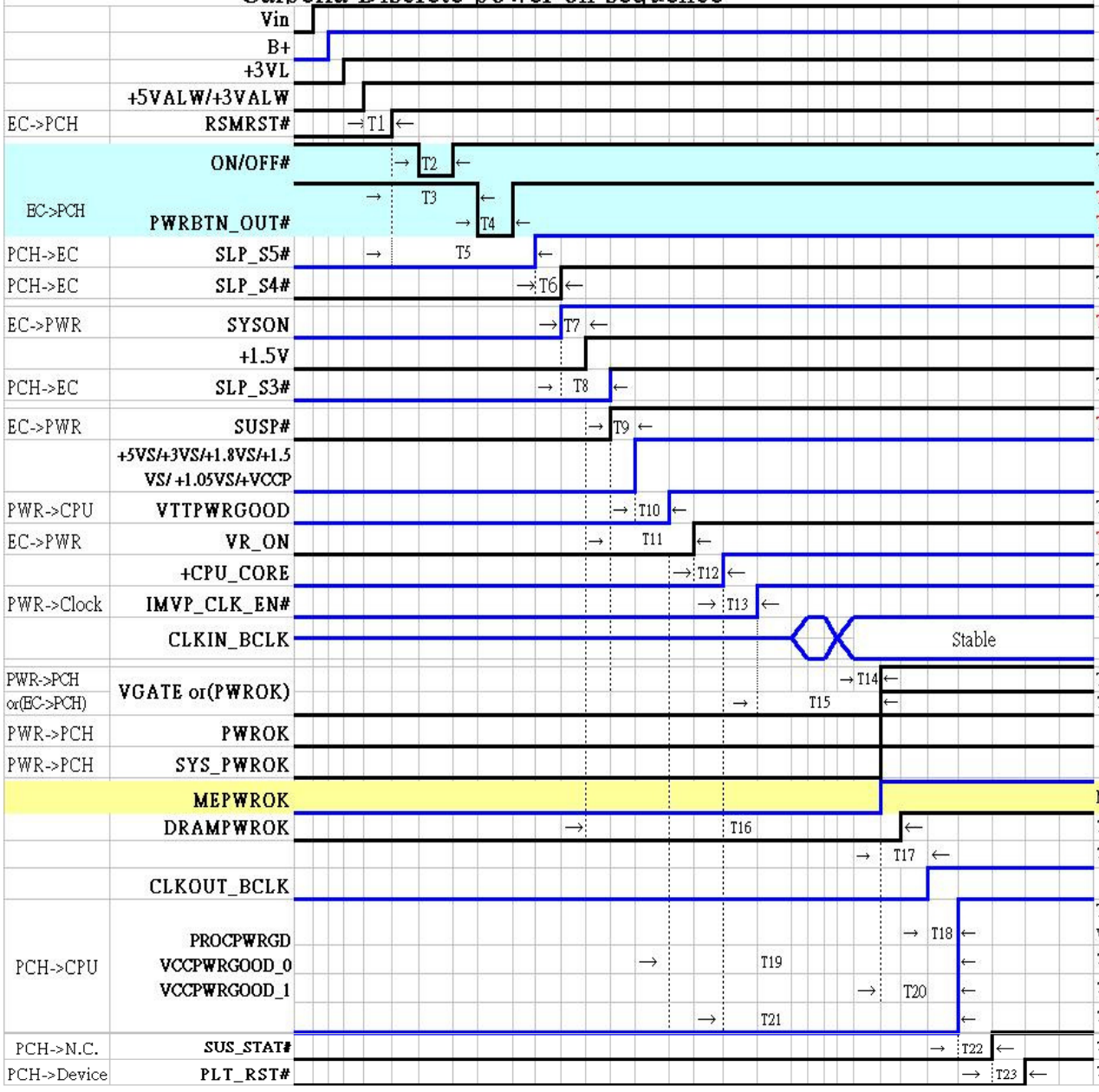
Calpella Discrete power on sequence

97.09.16.



		Spec	Intel define	min	Max
	Vin				
	B+				
	+3VL				
	+5VALW/+3VALW				
EC->PCH	RSMRST#	T1, >10ms , +3VALW to RSMRST#	T03	10 ms	-
EC->PCH	ON/OFF#	T2, User define			
EC->PCH	PWRBTN_OUT#	T3,150ms, T4,100ms			
PCH->EC	SLP_S5#	T5, >100ms,RSMRST# to SLP_S5#	T07	100 ms	-
PCH->EC	SLP_S4#	T6,>30us, SLP_S5# to SLP_S4#	T08	30 us	-
EC->PWR	SYSON	T7,10ms, SLP_S3# to SYSON			
	+1.5V				
PCH->EC	SLP_S3#	T8,>30us, SLP_S4# to SLP_S3#	T09	30 us	-
EC->PWR	SUSP#	T9,20ms, SLP_S3# to SUSP#			
	+5VS/+3VS/+1.8VS/+1.5VS/ +1.05VS/+VCCP				
PWR->CPU	VTTPWRGOOD	T10,VCCP stable to VTTPWRGOOD assertion to the processor	T13	0.0001 ms	500 ms
EC->PWR	VR_ON	T11>130ms , SLP_S3# to VR_ON	T16	99 ms	-
	+CPU_CORE	T12, Intel MVP soft start ramp-up time of +VCC_CORE	T17	-	3 ms
PWR->Clock	IMVP_CLK_EN#	T13,Duration Intel MVP V-boot, timing set by IMVP6.5	T18	10 us	100 us
	CLKIN_BCLK				
PWR->PCH	VGATE or(PWROK)	T14,CLKIN_BCLK stable to VGATE assertion	T19	1 ms	-
or(EC->PCH)		T15,IMVP_CLK_EN# to VGATE assert, Timing set by MVP6.5	T20	3 ms	20 ms
PWR->PCH	PWROK				
PWR->PCH	SYS_PWROK				
	MEPWROK	MEPWROK connecto to PWROK(iAMT disable)			
	DRAMPWROK	T16,+1.5V stable to DRAMPWROK assertion. Timing set by PCH	T22	100 ns	-
		T17,VGATE assertion to DRAMPWROK assertion, Timing set by PCH	T23	1 ms	-
	CLKOUT_BCLK				
PCH->CPU	PROCPWRGD	T18,CLKOUT_BCLK stable to VCCPWRGOOD_0 、VCCPWRGOOD_1 assertion to Processor . Timing set by	T24	10 BCKS	-
PCH->CPU	VCCPWRGOOD_0	T19,VTTPWRGD to VCCPWRGOOD assertion, Timing set by PCH	T25	1 ms	-
PCH->CPU	VCCPWRGOOD_1	T20,VGATE assertion to VCCPWRGOOD assertion, Timing by PCH	T26	1 ms	100 ms
		T21,VCORE stable to VCCPWRGOOD assertion	T27	0.05 ms	-
PCH->N.C.	SUS_STAT#	T22,VCCPWRGOOD to SUS_STAT# , timing default is 1ms	T28	0.03 ms	-
PCH->Device	PLT_RST#	T23,SUS_STAT# to PLTRST# , timing set by PCH	T29	60 us	-

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Title: **Notes List**

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Layout rule 10mil width trace length < 0.5", spacing 20mil

JCPU1B

MISC: COMP3 AT23, COMP2 AT24, COMP1 G16, COMP0 AT26, SKTOCC# AH24

THERMAL: CATERR# AK14, PECI AT15, PROCHOT# AN26, THERMTRIP# AK15

PWR MANAGEMENT: RESET_OBS# AP26, PM_SYNC AL15, VCCPWRGOOD_1 AN14, VCCPWRGOOD_0 AN27, SM_DRAMPWROK AK13, VTTPWRGOOD AM15, TAPPWRGOOD AM26, RSTIN# AL14

R1 20_0402_1% COMP3; R3 20_0402_1% COMP2; R5 49.9_0402_1% COMP1; R7 49.9_0402_1% COMP0

PAD T1 TP_SKTOCC# AH24

H_CATERR# AK14

<14> H_PECI R10 0_0402_5% H_PECI_ISO AT15

<49> H_PROCHOT# H_PROCHOT# AN26

<14,26> H_THERMTRIP# H_THERMTRIP# AK15

H_CPURST# R19 0_0402_5% H_CPURST#_R AP26

<13> H_PM_SYNC R20 0_0402_5% H_PM_SYNC_R AL15

H_CPUPWRGD R21 0_0402_5% SYS_AGENT_PWROK AN14

<14> H_CPUPWRGD R23 0_0402_5% VCCPWRGOOD_0 AN27

R1250 2K_0402_5%; <46> VTTPWRGOOD; R1249 1.5K_0402_1% AM15

H_PWRGD_XDP R25 0_0402_5% H_PWRGD_XDP_R AM26

<14> BUF_PLT_RST# R26 1.5K_0402_1% PLT_RST#_R AL14

R28 750_0402_1%

Design guide 1.11update,PLTRST series resittor 1.5K, PL resistor 750 ohm

iC;AUB_CFD_rPGA,R1P0 CONN@

CLOCKS

BCLK A16 CLK_CPU_BCLK; BCLK# B16 CLK_CPU_BCLK# — CLK_CPU_BCLK <14>, CLK_CPU_BCLK# <14>

BCLK_ITP AR30 CLK_CPU_XDP; BCLK_ITP# AT30 CLK_CPU_XDP#

PEG_CLK E16 CLK_EXP; PEG_CLK# D16 CLK_EXP# — CLK_EXP <12>, CLK_EXP# <12> OK

DPLL_REF_SSCLK A18; DPLL_REF_SSCLK# A17 — eDP

DDR3 MISC

SM_DRAMRST# F6 SM_DRAMRST#

SM_RCOMP[0] AL1 SM_RCOMP0; SM_RCOMP[1] AM1 SM_RCOMP1; SM_RCOMP[2] AN1 SM_RCOMP2

PM_EXT_TS#[0] AN15 PM_EXTTS#0; PM_EXT_TS#[1] AP15 PM_EXTTS#1 — R14 T63 PAD 0_0402_5% — PM_EXTTS#1_R <17,18> from DDR

JTAG & BPM

PRDY# AT28 XDP_PRDY#; PREQ# AP27 XDP_PREQ#

TCK AN28 XDP_TCK; TMS AP28 XDP_TMS; TRST# AT27 XDP_TRST#

TDI AT29 XDP_TDI_R; TDO AR27 XDP_TDO_R; TDI_M AR29 XDP_TDI_M; TDO_M AP29 XDP_TDO_M

DBR# AN25 XDP_DBRESET# — XDP_DBRESET# <13>

BPM#[0] AJ22 XDP_BPM#0; BPM#[1] AK22 XDP_BPM#1; BPM#[2] AK24 XDP_BPM#2; BPM#[3] AJ24 XDP_BPM#3; BPM#[4] AJ25 XDP_BPM#4; BPM#[5] AH22 XDP_BPM#5; BPM#[6] AK23 XDP_BPM#6; BPM#[7] AH23 XDP_BPM#7

+VCCP

PM_EXTTS#0 R27 10K_0402_5%

PM_EXTTS#1 R29 10K_0402_5%

2009.08.12 Remove the XDP connector

+VCCP

XDP_TDI @R2 51_0402_1%; XDP_TMS @R4 51_0402_1%; XDP_PREQ# @R6 51_0402_1%; XDP_TDO R8 51_0402_1%

This shall place near CPU

XDP_TCK @R9 51_0402_1%

+3VS

XDP_DBRESET# R603 1K_0402_5%

@ C1388 0.1U_0402_16V4Z

Processor Pullups

+VCCP

H_CATERR# R35 49.9_0402_1%

H_CPURST#_R @R36 68_0402_5%

H_PROCHOT# R11 68_0402_5%

DDR3 Compensation Signals

SM_RCOMP0 R40 100_0402_1%

SM_RCOMP1 R41 24.9_0402_1%

SM_RCOMP2 R42 130_0402_1%

Layout Note:Please these resistors near Processor

JTAG MAPPING

XDP_TDI_R R30 0_0402_5% XDP_TDI

XDP_TDO_M @R32 0_0402_5% XDP_TDO

R34 0_0402_5%

XDP_TDI_M @R37 0_0402_5%

XDP_TDO_R R38 0_0402_5%

XDP_TRST# R39 51_0402_1%

+1.5V

@R1205 0_0402_5%; R1206 1K_0402_1%

SM_DRAMRST# — Q104 BSS138_NL_SOT23-3 — DRAMRST# <17,18>

R1207 100K_0402_5%

PCH_DDR_RST <14>

C1430 470P_0402_50V7K

2009.08.17 change the Q104 to BSS138 to follow Intel's design guid.

PWM Fan Control circuit

+5VS

D56 RB751V_SOD323

C1386 4.7U_0805_10V4Z

C1387 0.1U_0402_16V4Z

JP2 ACES_88231-02001 CONN@ — GND GND

11/01 update

Change PCB Footprint from ACES_85204-02001_2P to ACES_88231-02001_2P

+FAN

<39> FAN_PWM

Q102 SI3456BDV-T1-E3_TSOP6

@D57 RLZ5.1B_LL34

1.5VSCPU_DRAM_PWRGD <47>

R1208 1.5K_0402_1%

+1.5V @R31 1.1K_0402_1%

R1209 0_0402_5%

<13> PM_DRAM_PWRGD — PM_DRAM_PWRGD — VDDPWRGOOD_R

@R33 3K_0402_1%

R1248 750_0402_1%

+3VALW

VTTPWRGOOD

U57 NC7SZ08P5X_NL_SC70-5

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Title: Auburndale(1/5)-Thermal/XDP

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Layout rule trace length < 0.5"

JCPU1A

DMI

PCI EXPRESS -- GRAPHICS Intel(R) FDI

DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]
DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]
DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]
DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]
FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]
FDI_FSYNC[0] FDI_FSYNC[1]
FDI_INT
FDI_LSYNC[0] FDI_LSYNC[1]

PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RBIAS
B26 EXP_ICOMPI R44 1 2 49.9_0402_1%
A26
B27
A25 EXP_RBIAS R45 1 2 750_0402_1%

PCIE_CRX_GTX_N[0..15] <24>
PCIE_CRX_GTX_P[0..15] <24>
PCIE_CTX_GRX_N[0..15] <24>
PCIE_CTX_GRX_P[0..15] <24>

PEG_RX#[0..15] PEG_RX[0..15] PEG_TX#[0..15] PEG_TX[0..15]

PCIE_CRX_GTX_N0 PCIE_CRX_GTX_N1 PCIE_CRX_GTX_N2 PCIE_CRX_GTX_N3 PCIE_CRX_GTX_N4 PCIE_CRX_GTX_N5 PCIE_CRX_GTX_N6 PCIE_CRX_GTX_N7 PCIE_CRX_GTX_N8 PCIE_CRX_GTX_N9 PCIE_CRX_GTX_N10 PCIE_CRX_GTX_N11 PCIE_CRX_GTX_N12 PCIE_CRX_GTX_N13 PCIE_CRX_GTX_N14 PCIE_CRX_GTX_N15
PCIE_CRX_GTX_P0 PCIE_CRX_GTX_P1 PCIE_CRX_GTX_P2 PCIE_CRX_GTX_P3 PCIE_CRX_GTX_P4 PCIE_CRX_GTX_P5 PCIE_CRX_GTX_P6 PCIE_CRX_GTX_P7 PCIE_CRX_GTX_P8 PCIE_CRX_GTX_P9 PCIE_CRX_GTX_P10 PCIE_CRX_GTX_P11 PCIE_CRX_GTX_P12 PCIE_CRX_GTX_P13 PCIE_CRX_GTX_P14 PCIE_CRX_GTX_P15

PCIE_CTX_GRX_C_N0 C4 … PCIE_CTX_GRX_C_N15 C19
PCIE_CTX_GRX_C_P0 C20 … PCIE_CTX_GRX_C_P15 C35
0.1U_0402_16V4Z

IC,AUB_CFD_rPGA,R1P0
CONN@

JCPU1E

+V_DDR_CPU_REF1 +V_DDR_CPU_REF0

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 SA_DIMM_VREF SB_DIMM_VREF RSVD11 RSVD12 RSVD13 RSVD14
RSVD32 RSVD33 RSVD34 RSVD35 RSVD36 RSVD_NCTF_37 RSVD38 RSVD39 RSVD_NCTF_40 RSVD_NCTF_41 RSVD_NCTF_42 RSVD_NCTF_43

CFG[0] CFG[1] CFG[2] CFG[3] CFG[4] CFG[5] CFG[6] CFG[7] CFG[8] CFG[9] CFG[10] CFG[11] CFG[12] CFG[13] CFG[14] CFG[15] CFG[16] CFG[17] RSVD_TP_86
RSVD45 RSVD46 RSVD47 RSVD48 RSVD49 RSVD50 RSVD51 RSVD52 RSVD53 RSVD_NCTF_54 RSVD_NCTF_55 RSVD_NCTF_56 RSVD_NCTF_57 RSVD58 RSVD_TP_59 RSVD_TP_60 KEY RSVD62 RSVD63 RSVD64 RSVD65

@R48 1 2 0_0402_5%
@R49 1 2 0_0402_5%

@R50 1 2 0_0402_5%
@R51 1 2 0_0402_5%

RSVD15 RSVD16 RSVD17 RSVD18 RSVD19 RSVD20 RSVD21 RSVD22 RSVD_NCTF_23 RSVD_NCTF_24 RSVD26 RSVD27 RSVD_NCTF_28 RSVD_NCTF_29 RSVD_NCTF_30 RSVD_NCTF_31
RSVD_TP_66 RSVD_TP_67 RSVD_TP_68 RSVD_TP_69 RSVD_TP_70 RSVD_TP_71 RSVD_TP_72 RSVD_TP_73 RSVD_TP_74 RSVD_TP_75 RSVD_TP_76 RSVD_TP_77 RSVD_TP_78 RSVD_TP_79 RSVD_TP_80 RSVD_TP_81 RSVD_TP_82 RSVD_TP_83 RSVD_TP_84 RSVD_TP_85

VSS AP34

RESERVED

IC,AUB_CFD_rPGA,R1P0
CONN@

CRB 0.9 change to GND

CFG Straps for PROCESSOR

CFG0 @R52 1 2 3.01K_0402_1%

PCI-Express Configuration Select	
CFG0	1: Single PEG ★ 0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG3 R54 1 2 3.01K_0402_1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 ->1, ... ★

CFG4 @R53 1 2 3.01K_0402_1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port ★ attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 @R55 1 2 3.01K_0402_1%

Only temporary for early CFD samples (rPGA/BGA)
Only for pre ES1 sample

CFG7
NW33 PD 3.01K on CFG7 for PCIE Jitter
NW41 don't staff

Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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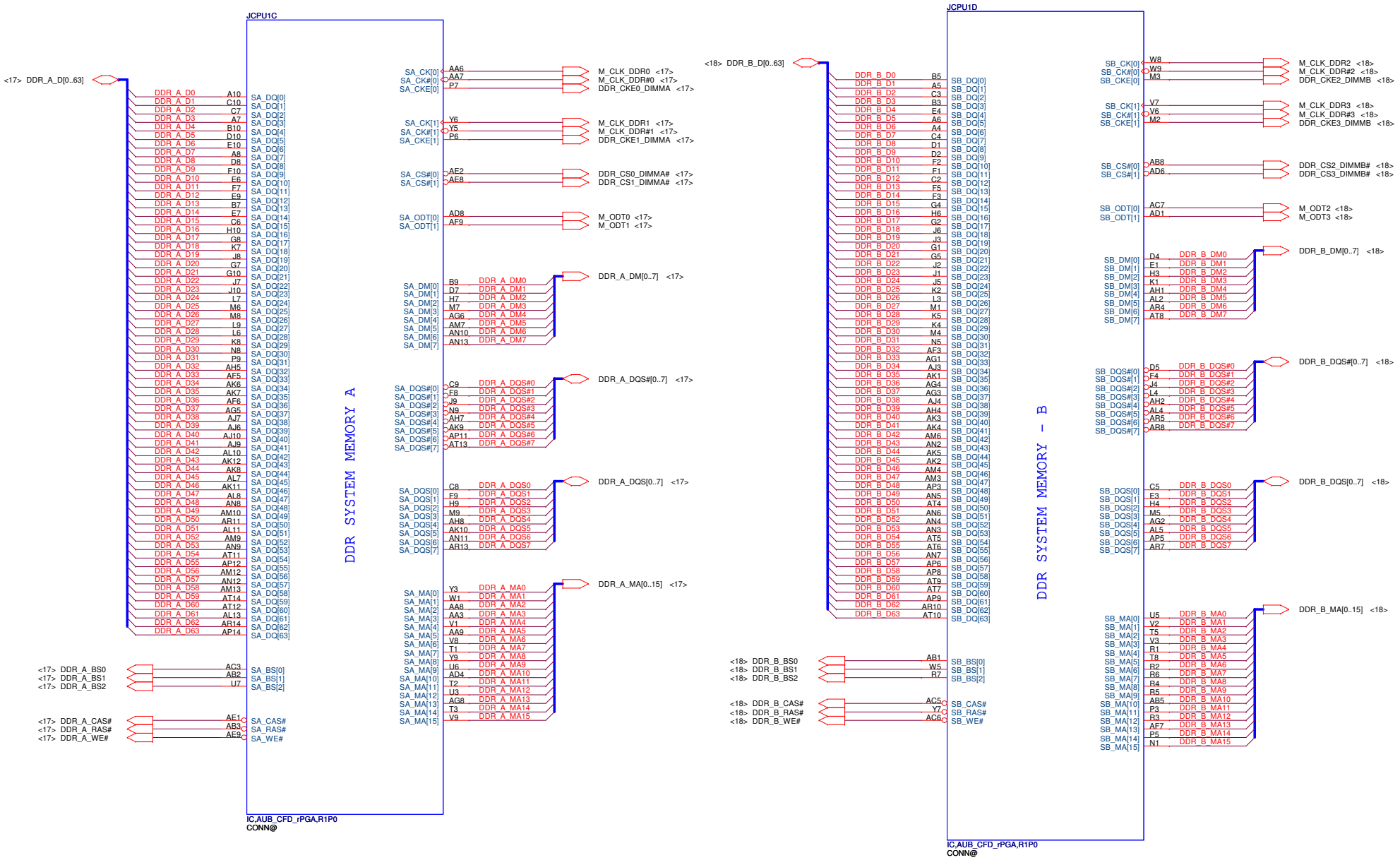
Compal Electronics, Inc.

Title: Auburndale(2/5)-DMI/PEG/FDI

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 Sheet 7 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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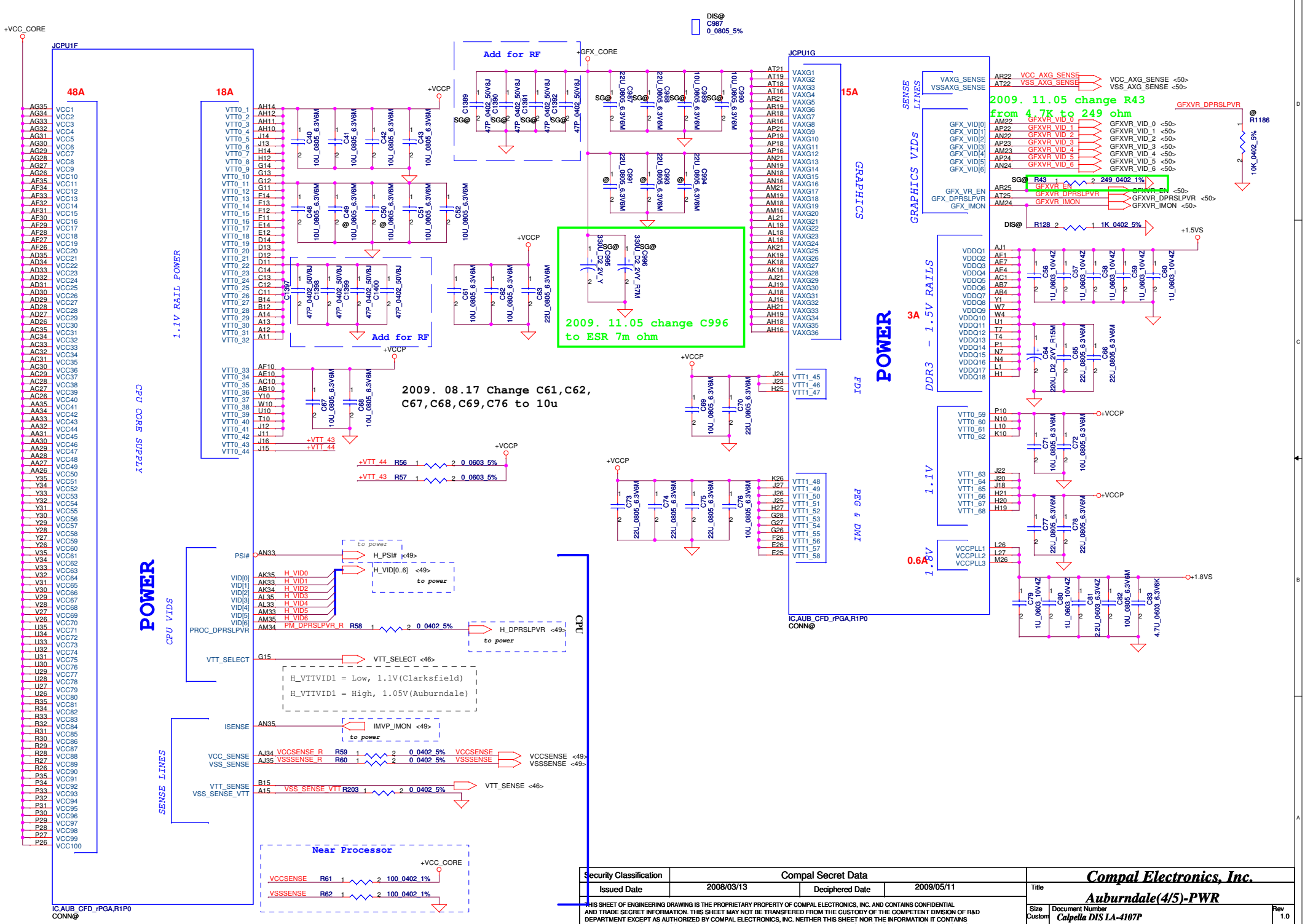
Compal Electronics, Inc.

Title: Cantiga(2/6)-DDR3 A/B CH

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 8 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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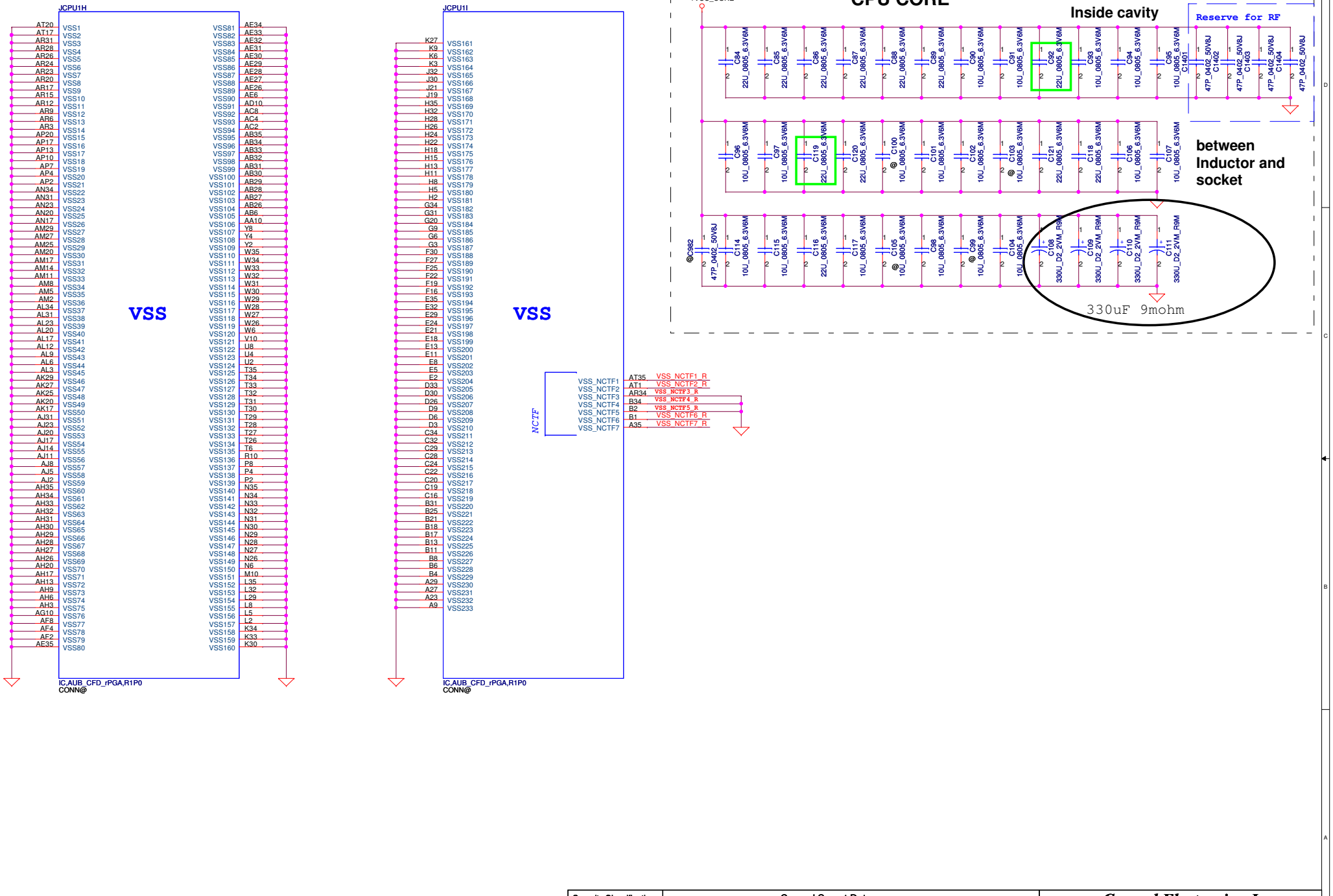
Compal Electronics, Inc.	
Title	Auburndale(4/5)-PWR
Size: Custom	Document Number: Calpella DIS LA-4107P
Rev	1.0
Date: Monday, November 09, 2009	Sheet 9 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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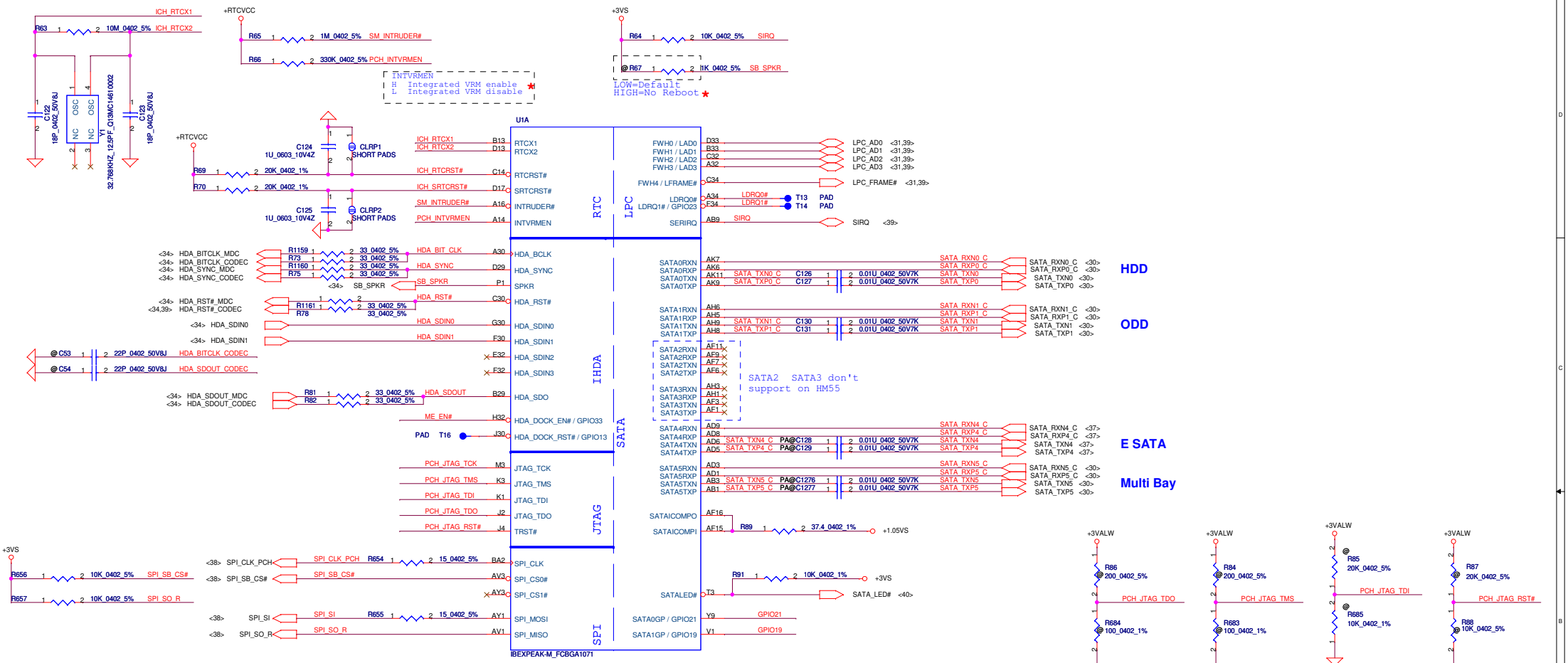
Compal Electronics, Inc.			
Title: Auburndale(5/5)-GND/Bypass			
Size: Custom	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 10 of 55		



PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable ES1	PCH JTAG Disable ES2
PCH_JTAG_TDO	R86	No Install	200ohm	No Install	No Install
	R684	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R84	200ohm	200ohm	No Install	No Install
	R683	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R85	200ohm	200ohm	20Kohm	No Install
	R685	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R90	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R87	20Kohm	20Kohm	No Install	No Install
	R88	10Kohm	10Kohm	No Install	No Install

Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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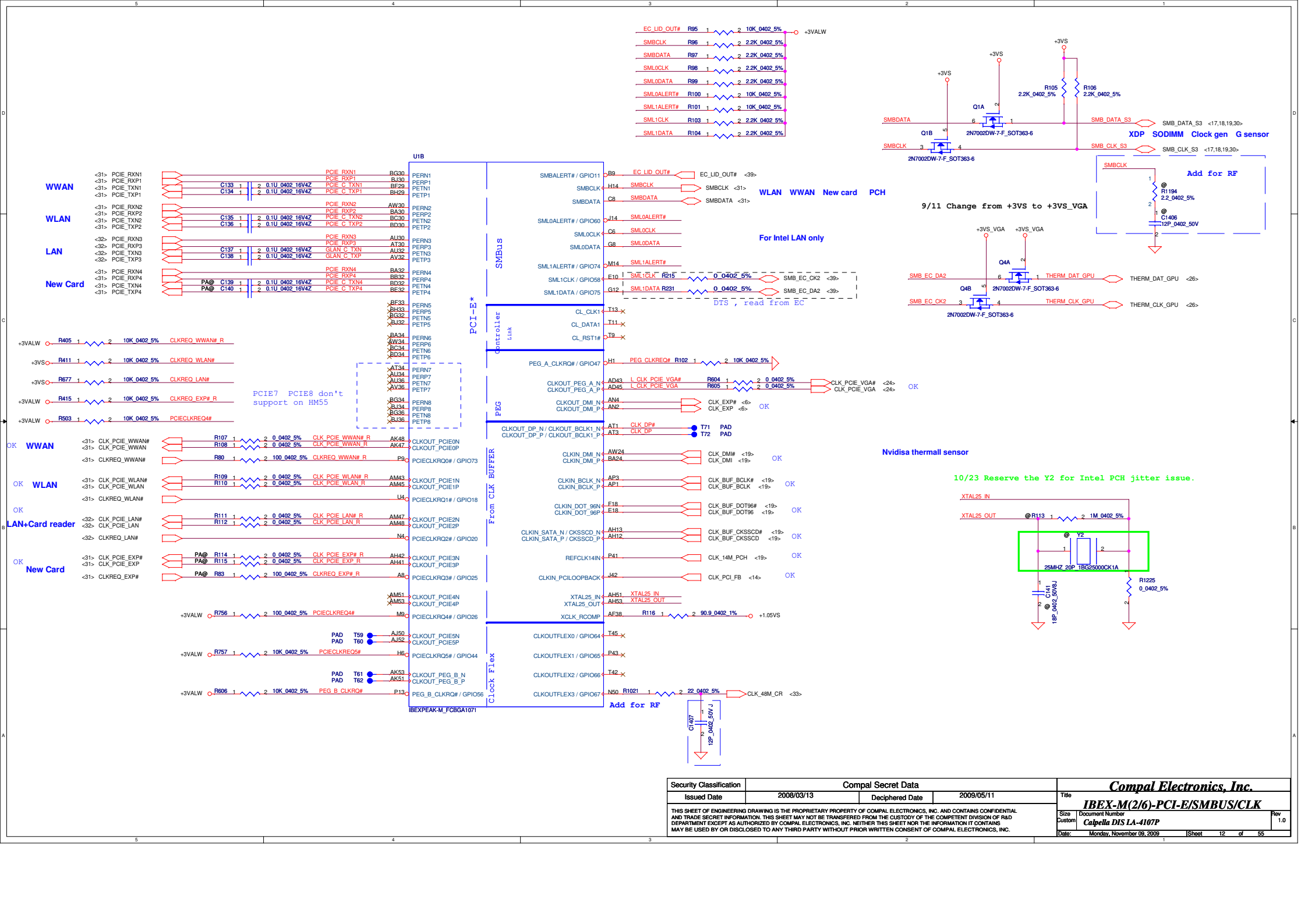
Compal Electronics, Inc.

Title: IBEX-M(1/6)-HDA/JTAG/SATA

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 Sheet 11 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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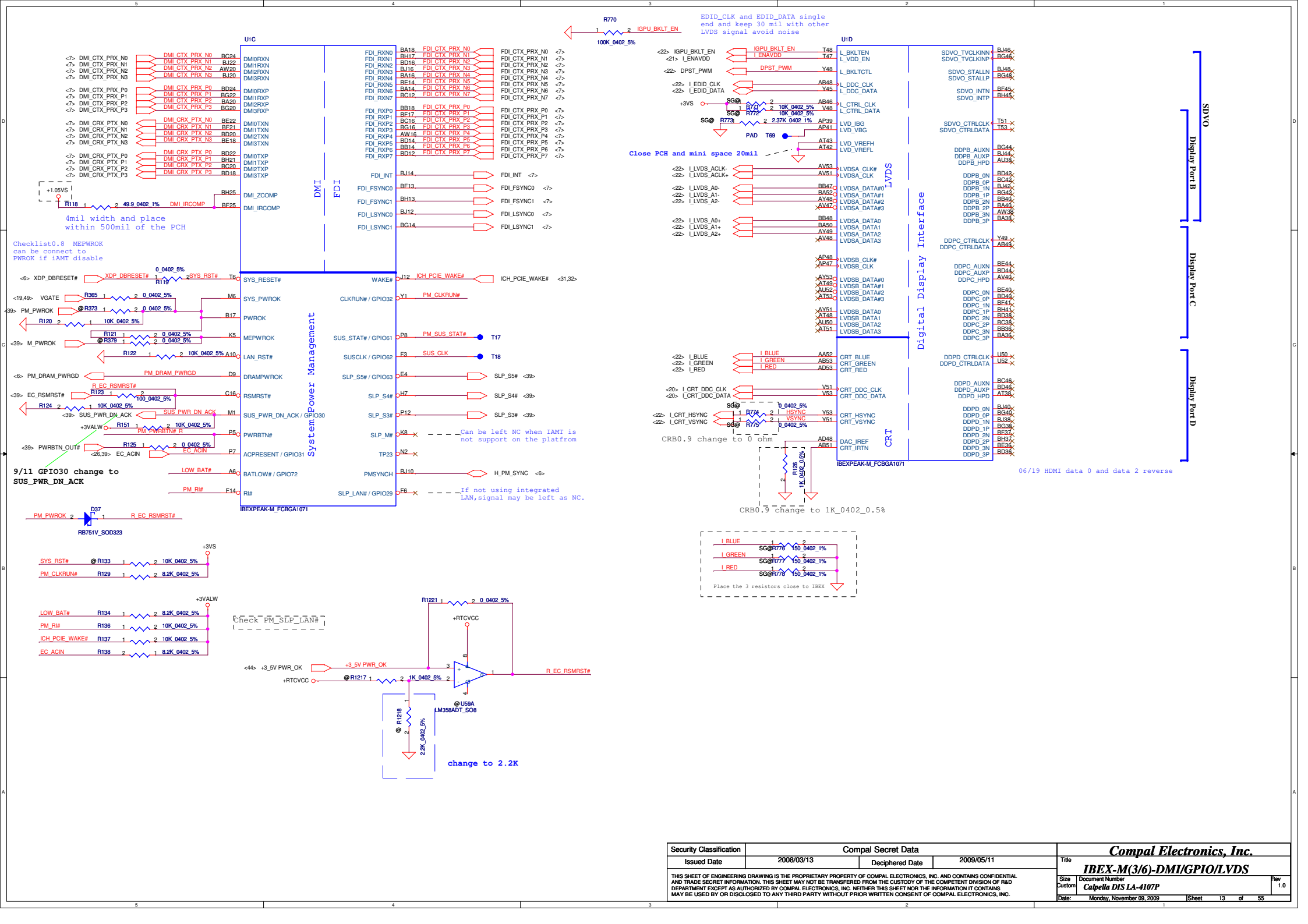
Compal Electronics, Inc.

Title: **IBEX-M(2/6)-PCI-E/SMBUS/CLK**

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 12 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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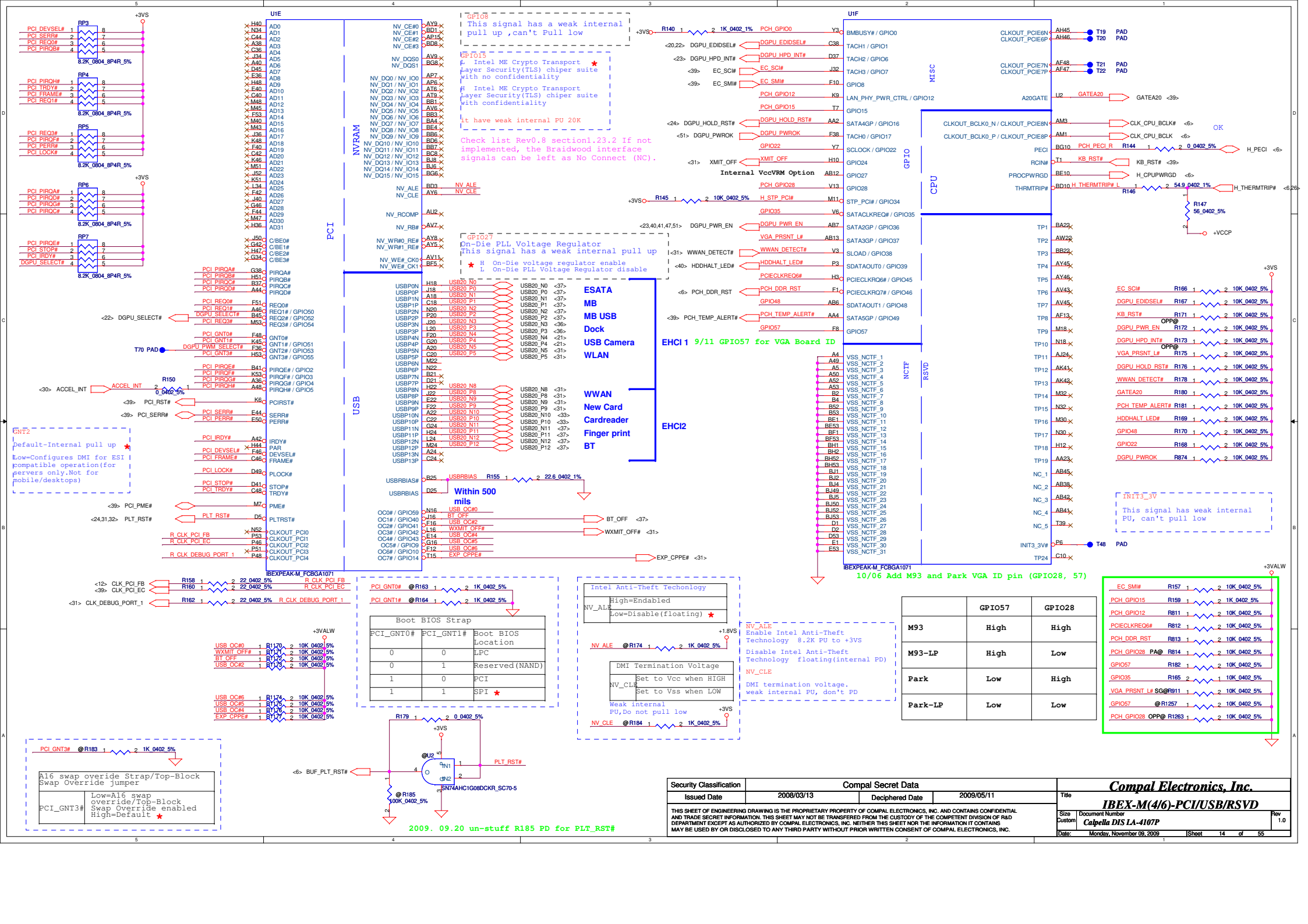
Compal Electronics, Inc.

Title: **IBEX-M(3/6)-DMI/GPIO/LVDS**

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 13 of 55



	GPIO57	GPIO28
M93	High	High
M93-LP	High	Low
Park	Low	High
Park-LP	Low	Low

Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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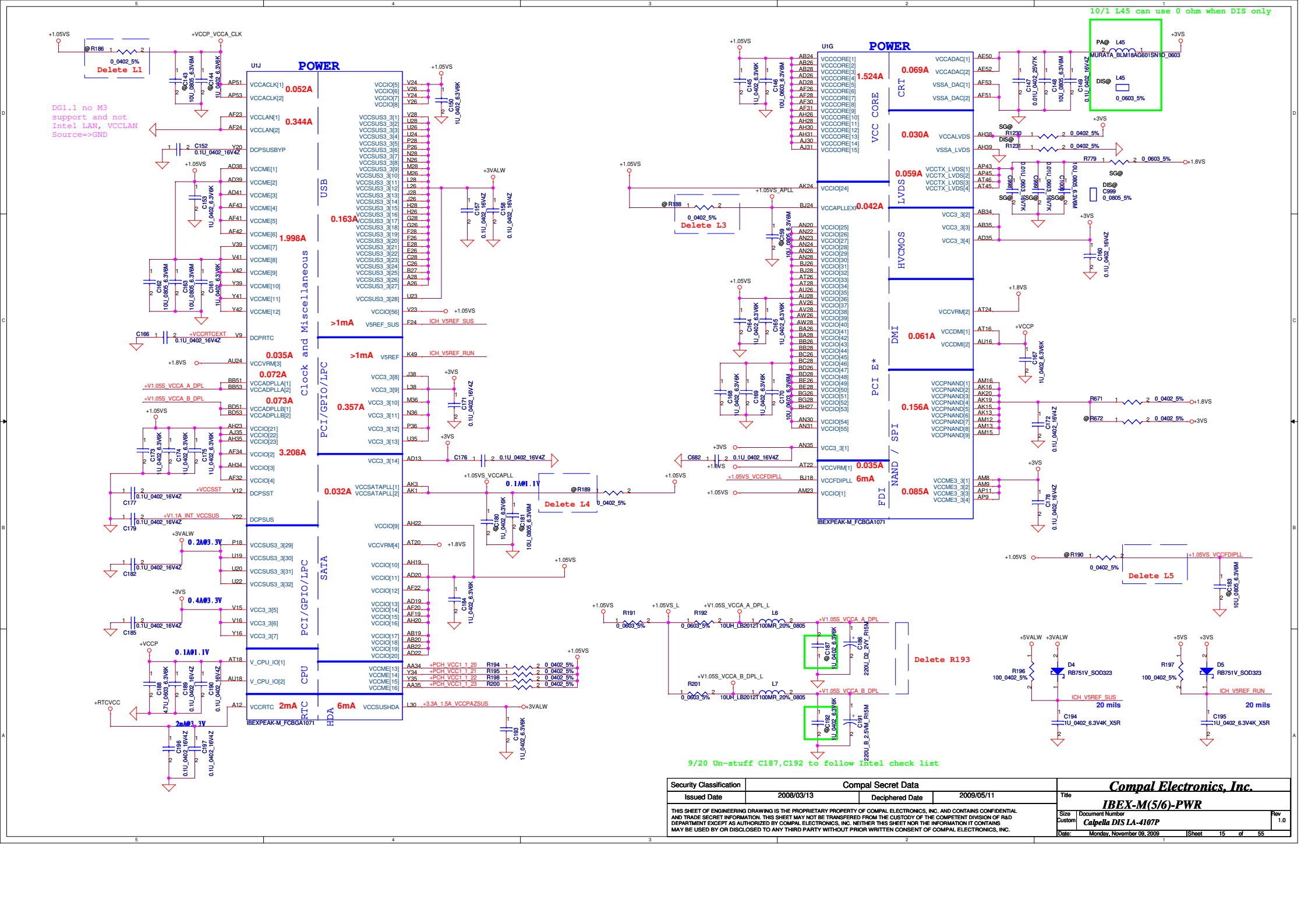
Compal Electronics, Inc.

Title: IBEX-M(4/6)-PCI/USB/RSVD

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 14 of 55


10/1 L45 can use 0 ohm when DIS only
POWER
U1J
U1G
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
SPI
NAND
FDI
DG1.1 no M3 support and not Intel LAN, VCCLAN Source=>GND
Delete L1
Delete L3
Delete L4
Delete L5
Delete R193
9/20 Un-stuff C187,C192 to follow Intel check list
IBEXPEAK-M_FCBGA1071
Security Classification
Compal Secret Data
Issued Date
2008/03/13
Deciphered Date
2009/05/11
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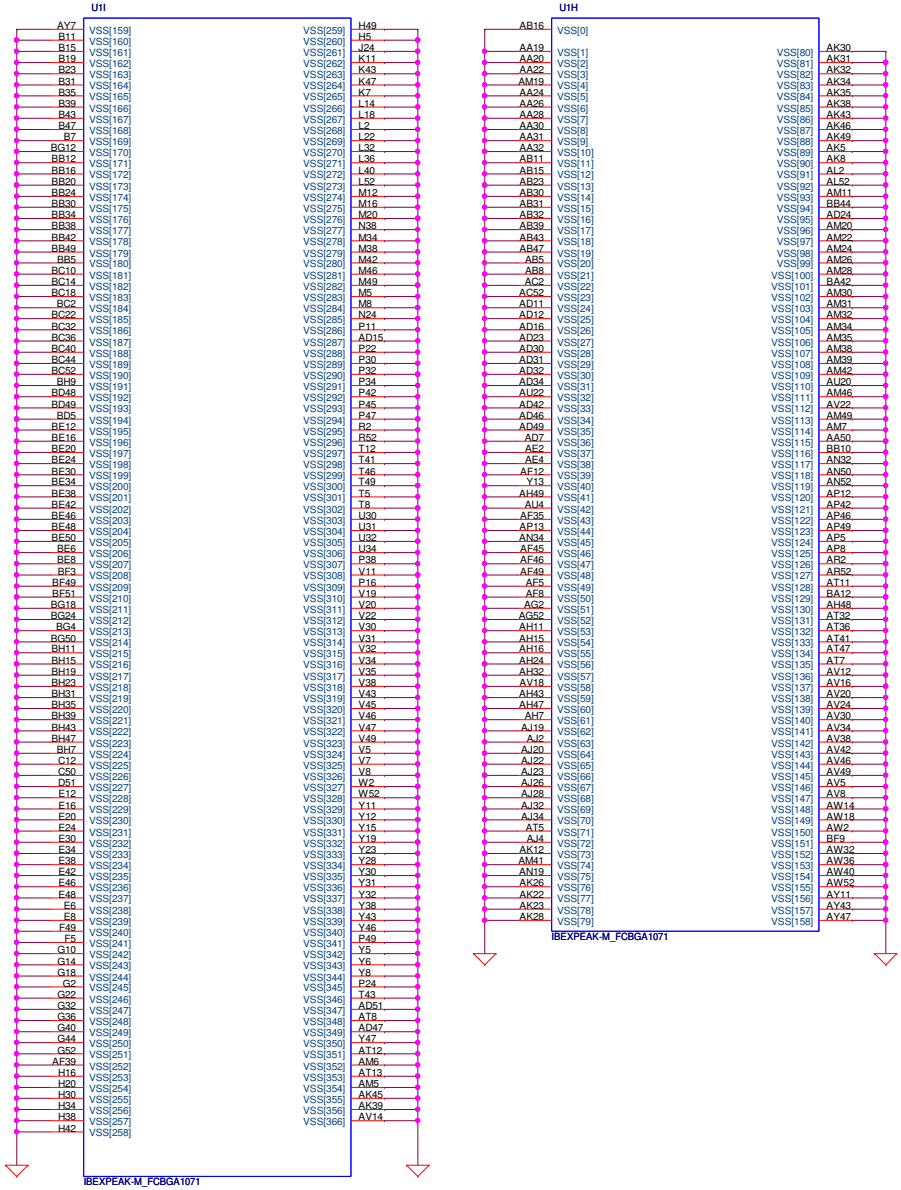
Compal Electronics, Inc.
Title
IBEX-M(5/6)-PWR
Size
Custom
Document Number
Calpella DIS LA-4107P
Rev
1.0
Date:
Monday, November 09, 2009
Sheet
15
of
55



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Issued Date	2008/03/13	Deciphered Date	2009/05/11

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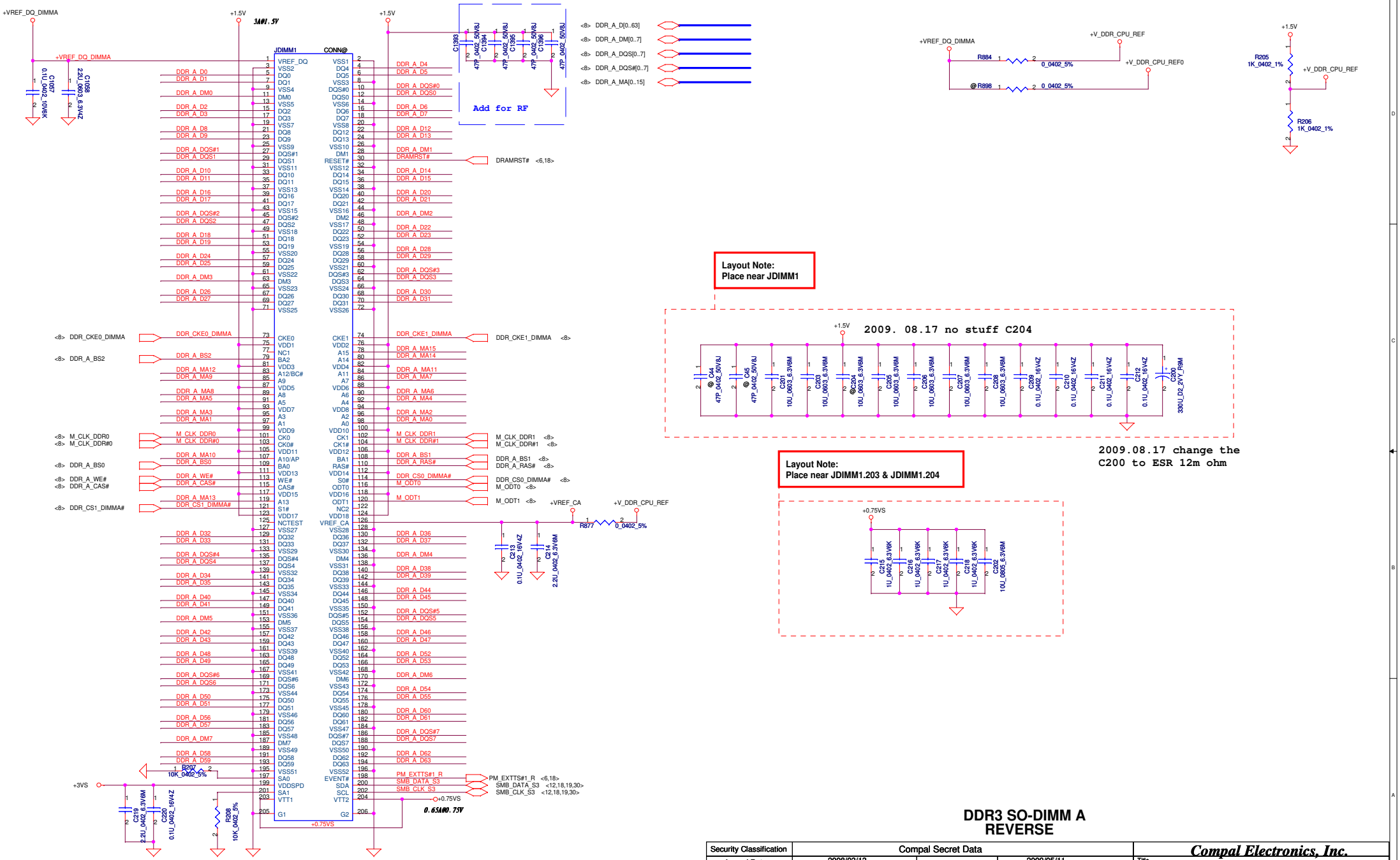
Compal Electronics, Inc.

Title: **IBEX-M(6/6)-GND**

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 16 of 55



DDR3 SO-DIMM A
REVERSE

Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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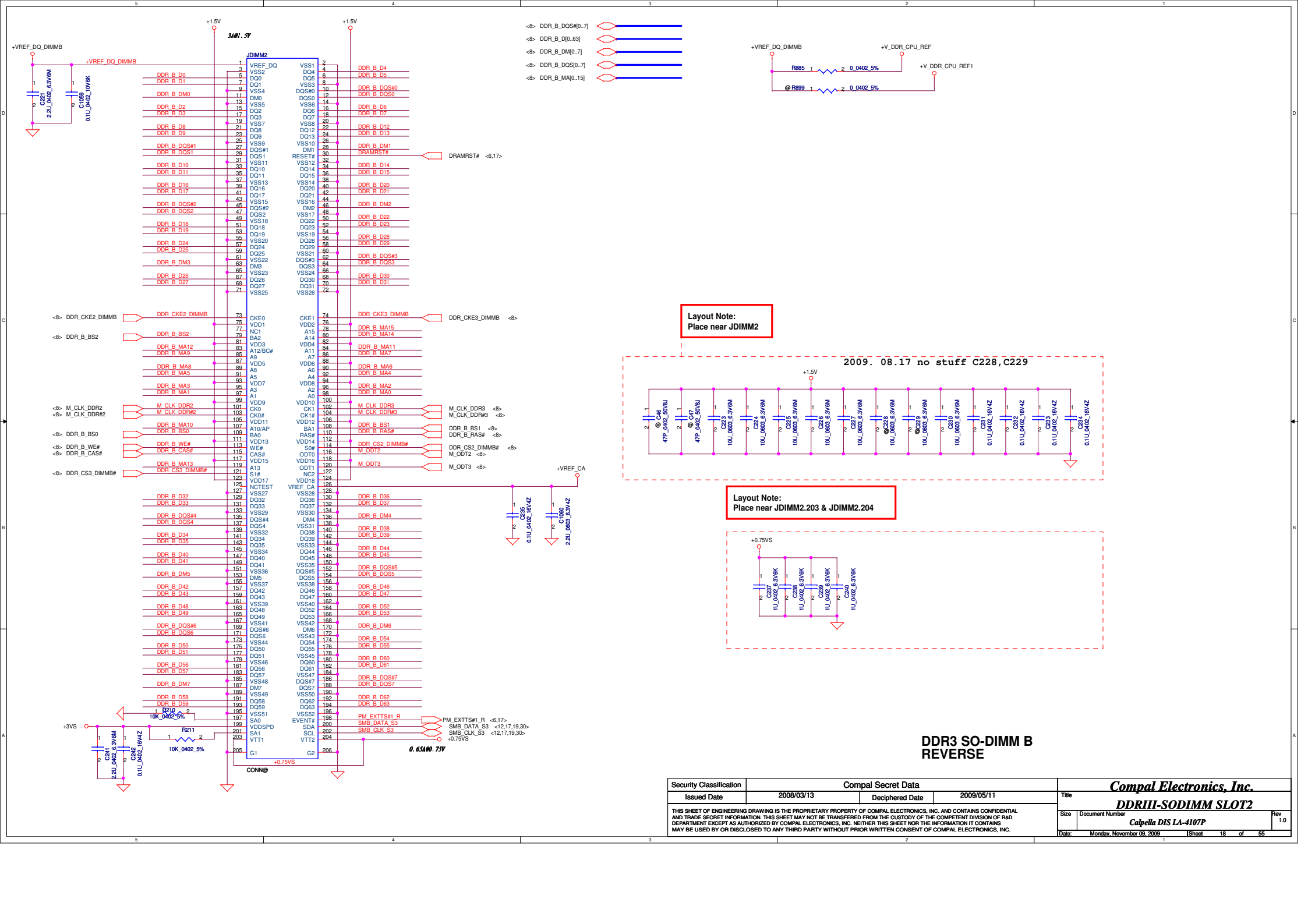
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 17 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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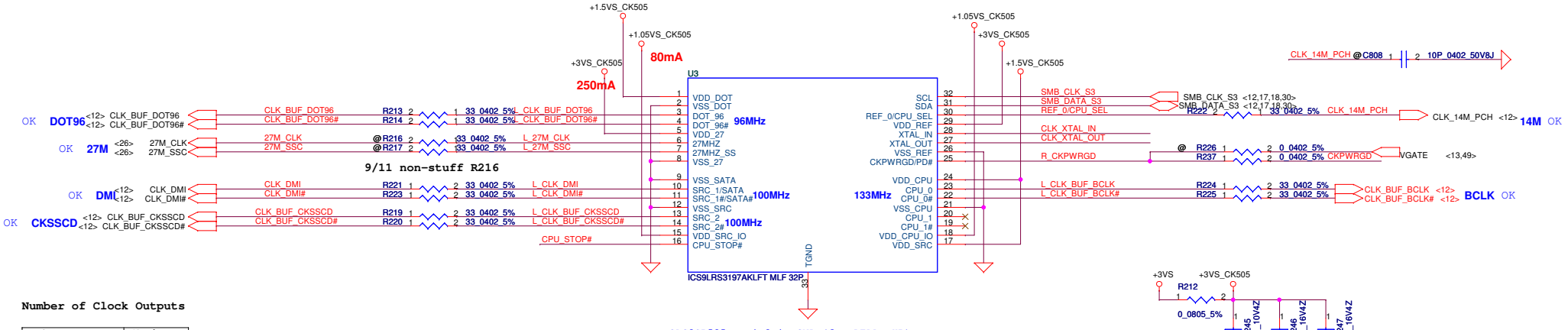
Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number		Rev
	Calpella DIS LA-4107P		1.0
Date: Monday, November 09, 2009	Sheet 18 of 55		

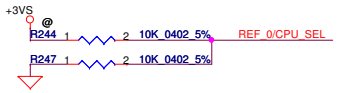


Number of Clock Outputs

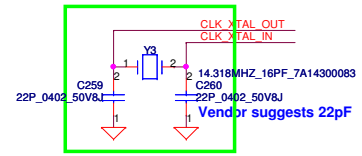
Output	Number
133MHz	2
SRC(100MHz_SS)	1
SRC/SATA(100MHz)	1
REF(14.318MHz)	1
DOT_CLK(96MHz)	1
27MHz	1
27MHz_SS	1

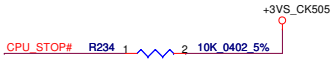
PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1	100MHz	100MHz

CPU_SEL During CK_PEWGD Latch Pin1



2009.10.21 change the C259, C260 to 22P



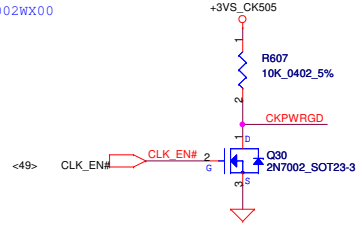


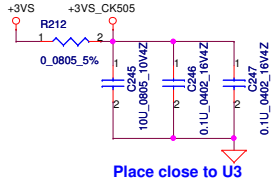
SLG8SP585 pin8 is GND (for DELL HP)
SLG8SP587 pin8 is 48MHz (For ABO or 030)

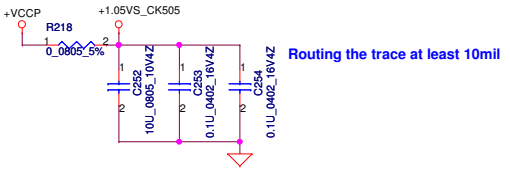
Realtek SA00002Y010

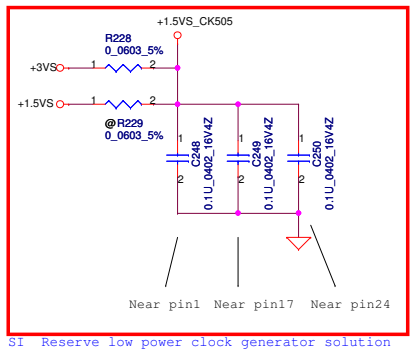
* IDT SA00002Y500

IDT SA00002WX00









SI Reserve low power clock generator solution

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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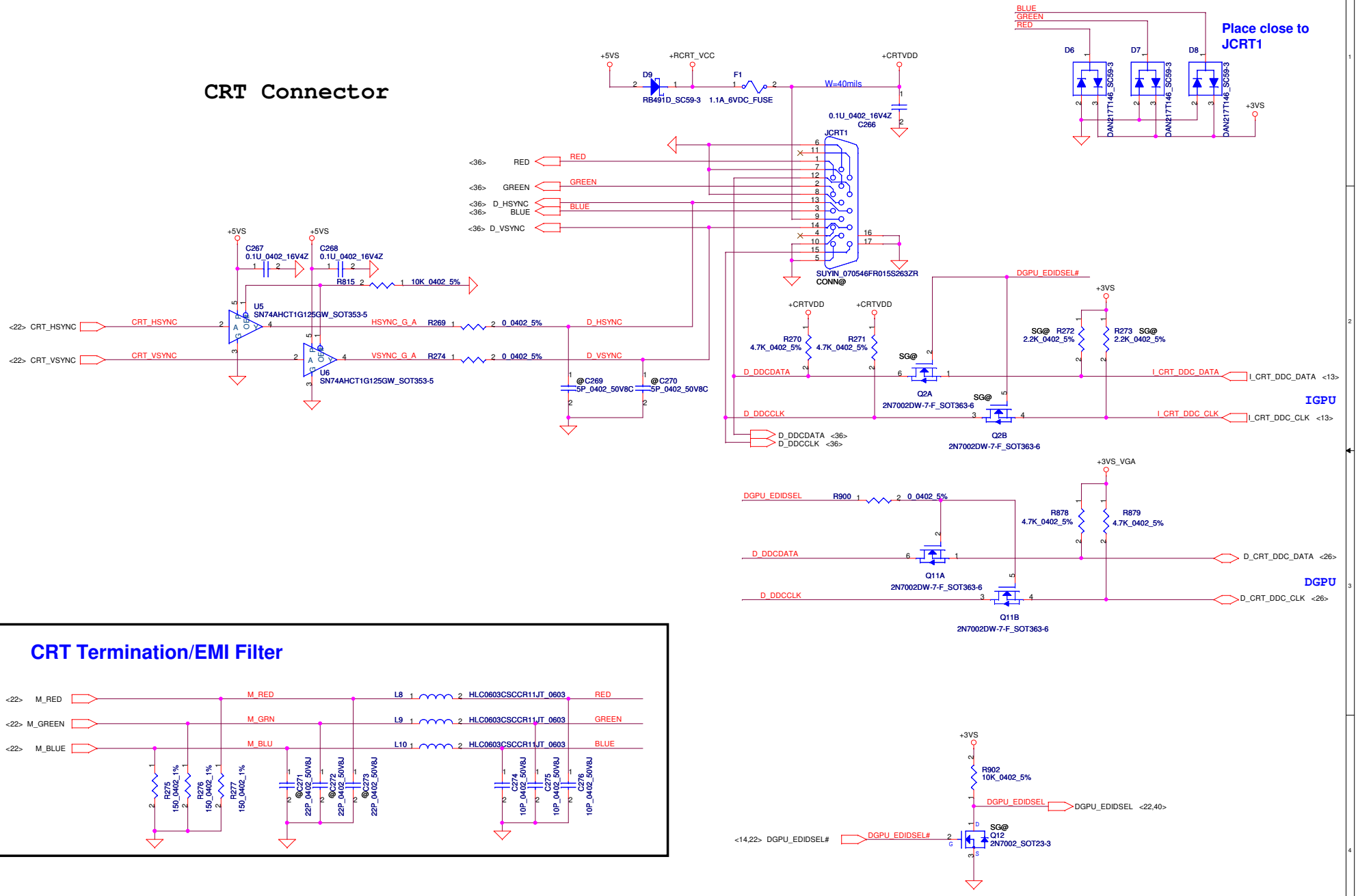
Compal Electronics, Inc.	
Title	Clock Generator CK505
Size	Document Number: Calpella DIS LA-4107P
Rev	1.0
Date: Monday, November 09, 2009	Sheet 19 of 55

CRT Connector



CRT Termination/EMI Filter

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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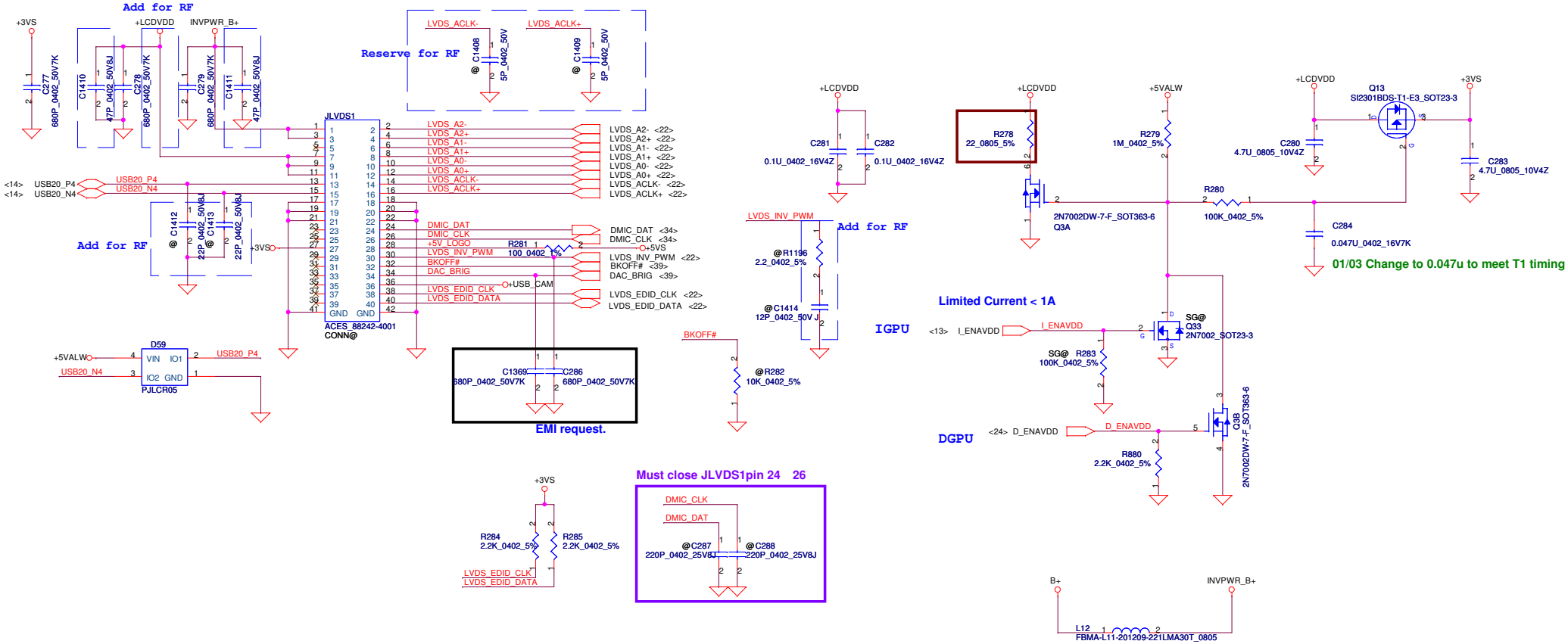
Compal Electronics, Inc.			
Title: CRT Connector			
Size	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 20 of 55		

LVDS CONN & USB Camera + Dig Mic



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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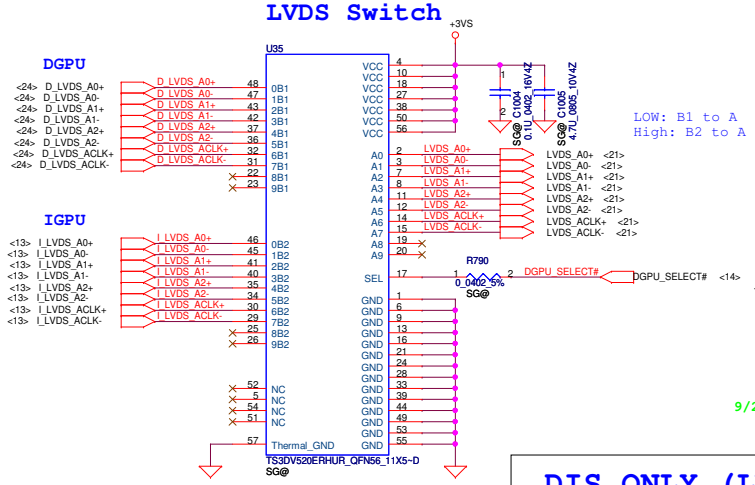
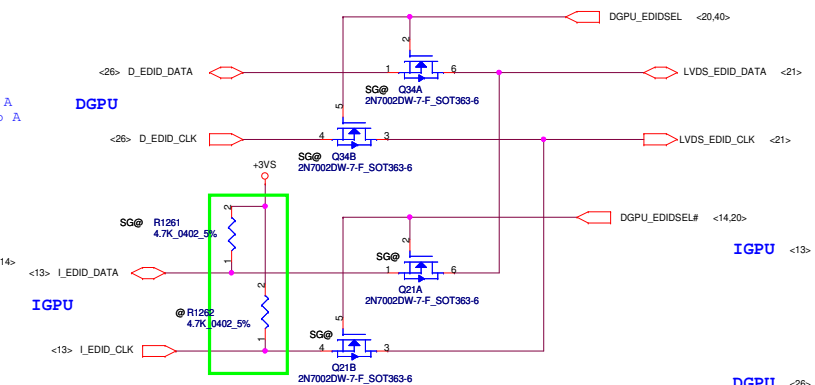
Compal Electronics, Inc.			
Title: LCD CONN.			
Size	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 21 of 55		

LVDS Switch

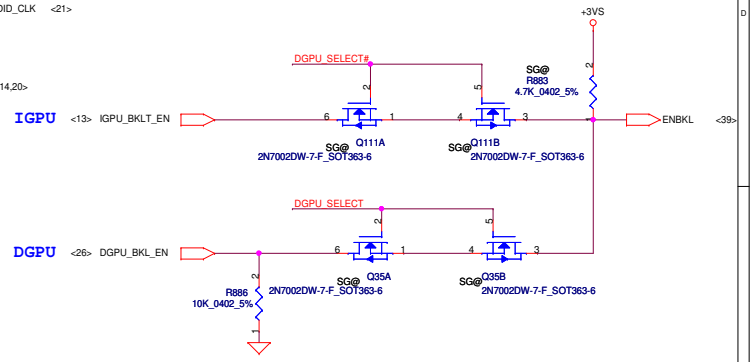


LVDS I2C switch

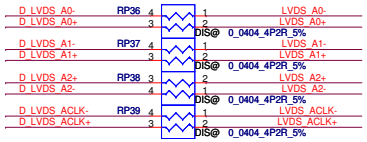


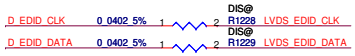
9/20 Follow Intel check list to add PU resistors for EDID signals

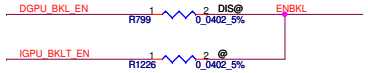
Backlight Enable



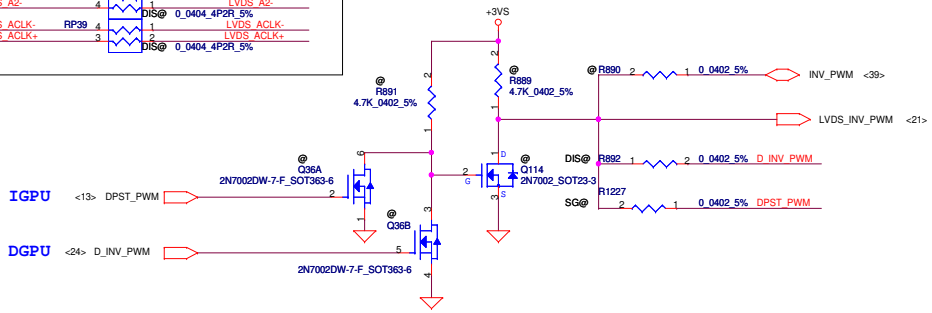
DIS ONLY (LVDS)



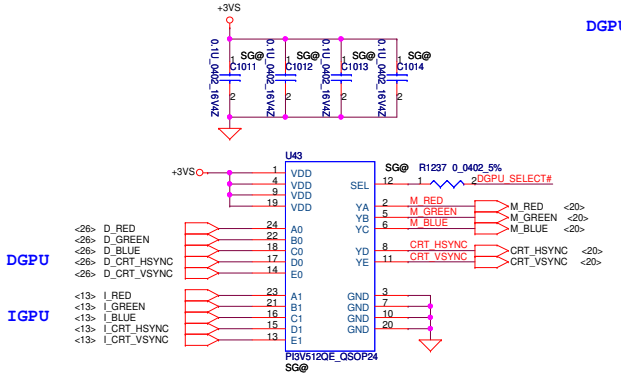




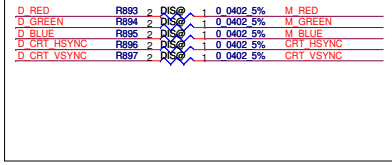
LVDS PWM switch

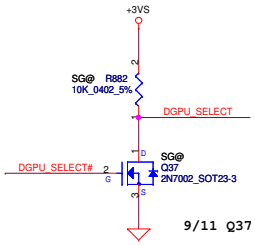


CRT Switch



DIS ONLY (CRT)





9/11 Q37 change to single package

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Issued Date	2007/09/29	Deciphered Date	2007/09/29

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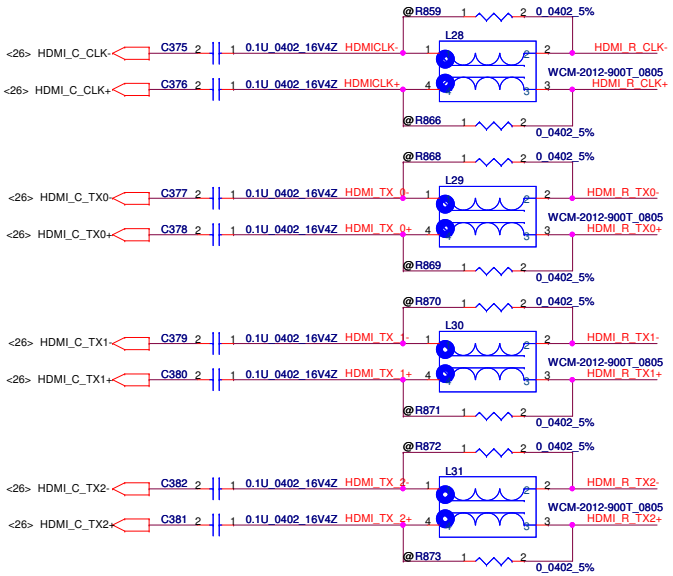
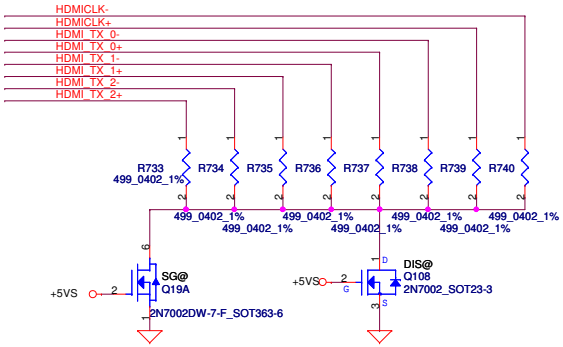
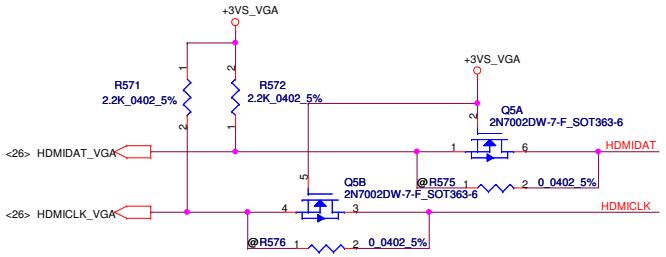
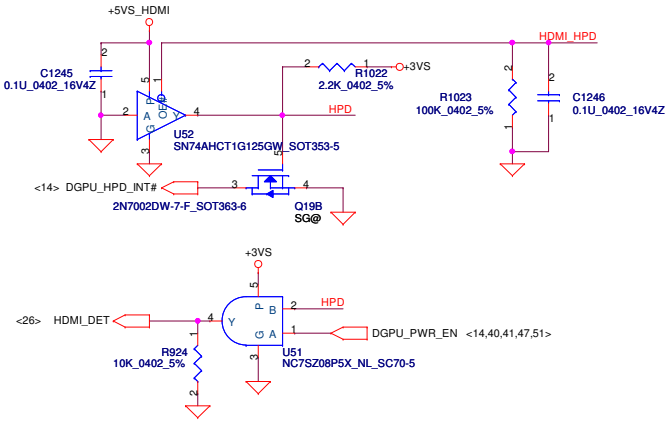
Compal Electronics, Inc.			
Title: LVDS Switch			
Size: Custom	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 22 of 55		

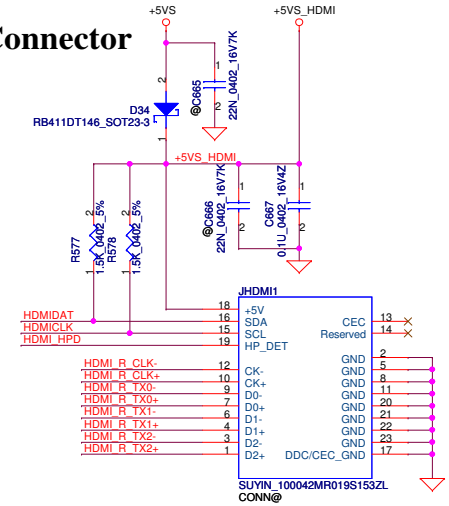
HDMI Connector











Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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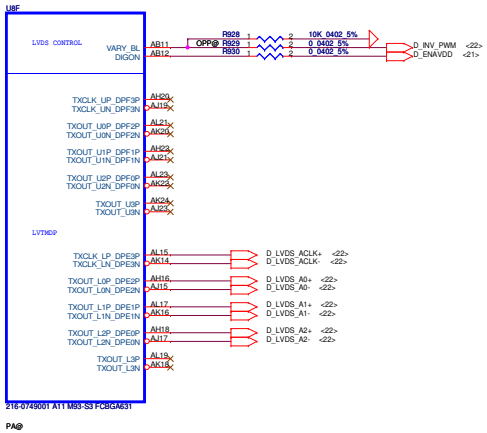
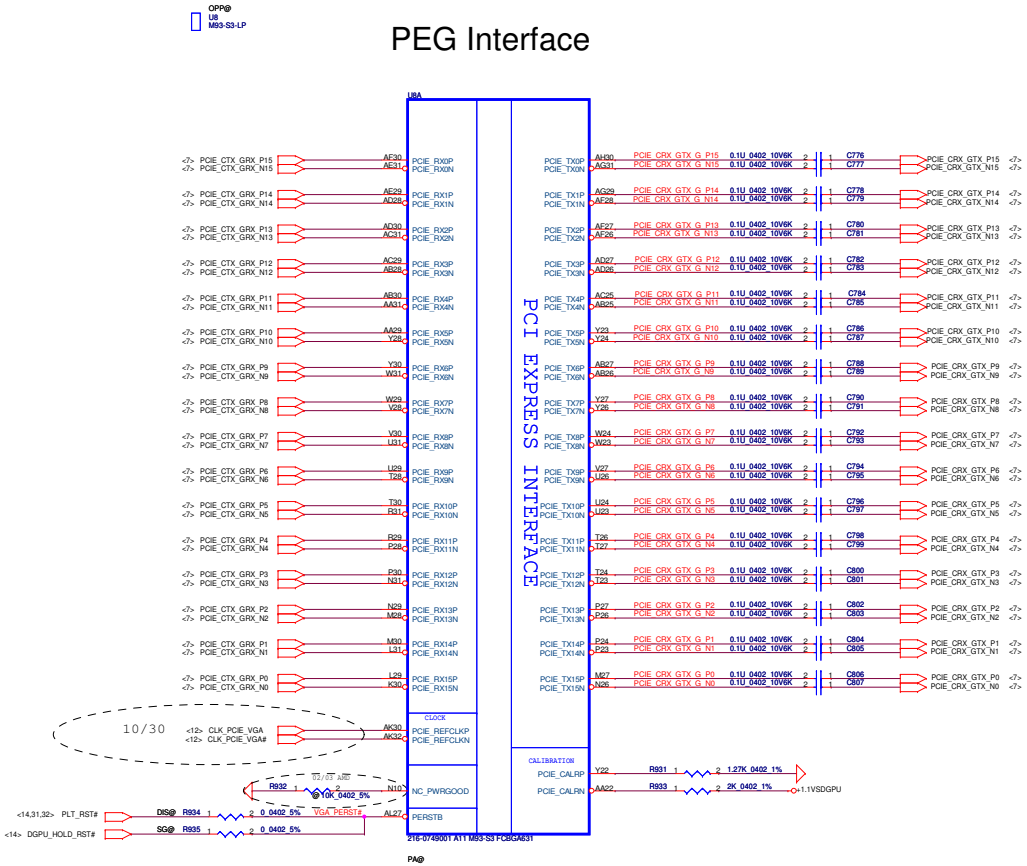
Compal Electronics, Inc.			
Title: HDMI LS & Conn.			
Size: Custom	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 23 of 55		

LVDS Interface



PEG Interface



Security Classification	Compal Secret Data		
Issued Date	2009/03/31	Deciphered Date	2010/03/31

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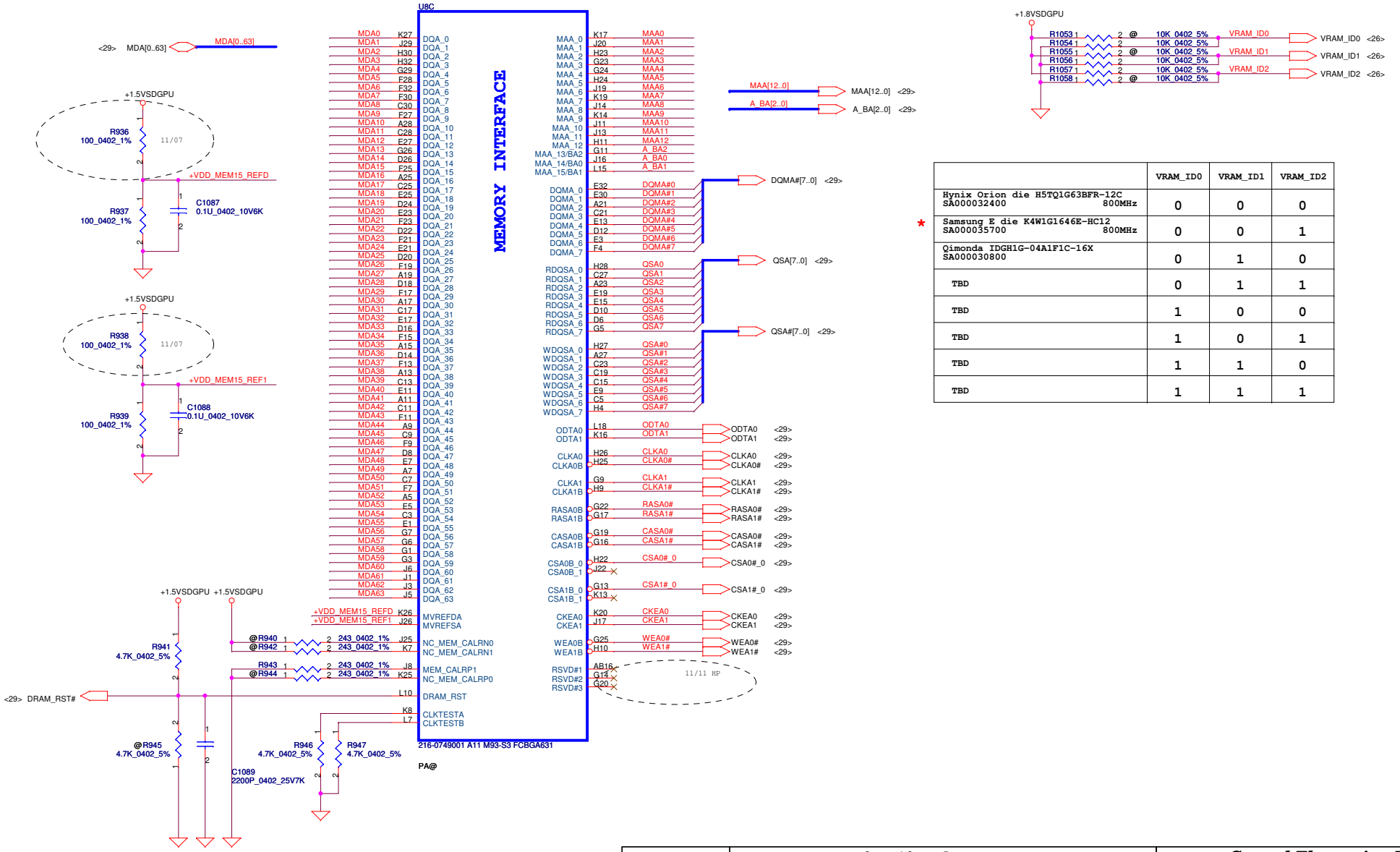
Compal Electronics, Inc.			
Title: PEG & LVDS			
Size: Custom	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 24 of 55		



*

	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix Orion die H5TQ1G63BFR-12C SA000032400 800MHz	0	0	0
Samsung E die K4W1G1646E-HC12 SA000035700 800MHz	0	0	1
Qimonda IDGH1G-04A1F1C-16X SA000030800	0	1	0
TBD	0	1	1
TBD	1	0	0
TBD	1	0	1
TBD	1	1	0
TBD	1	1	1

Security Classification	Compal Secret Data		
Issued Date	2009/03/31	Deciphered Date	2010/03/31

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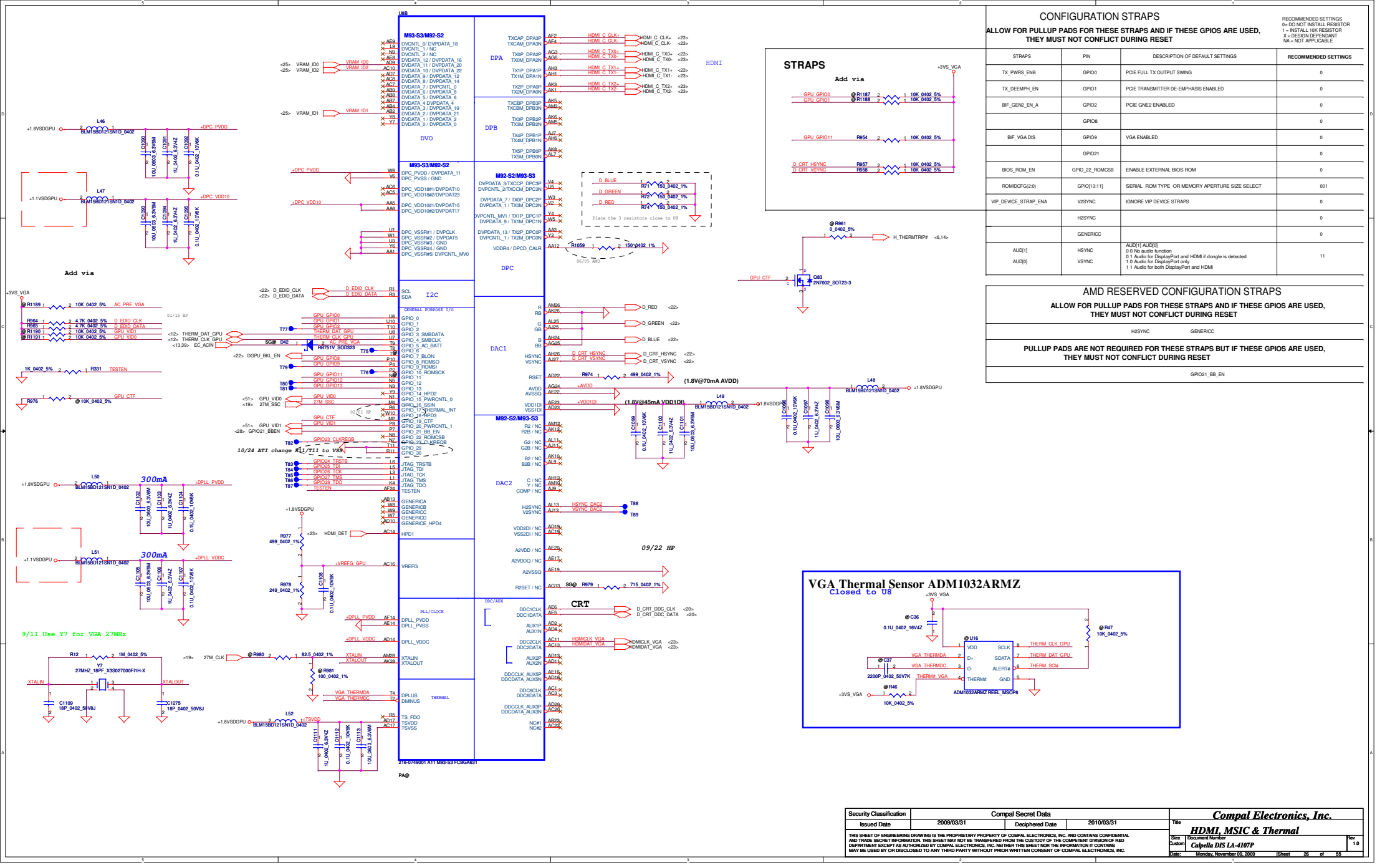
Compal Electronics, Inc.

Title: Memory Interface

Size: Custom | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 25 of 55



Security Classification	Compal Secret Data		
Issued Date	2009/03/31	Deciphered Date	2010/03/31

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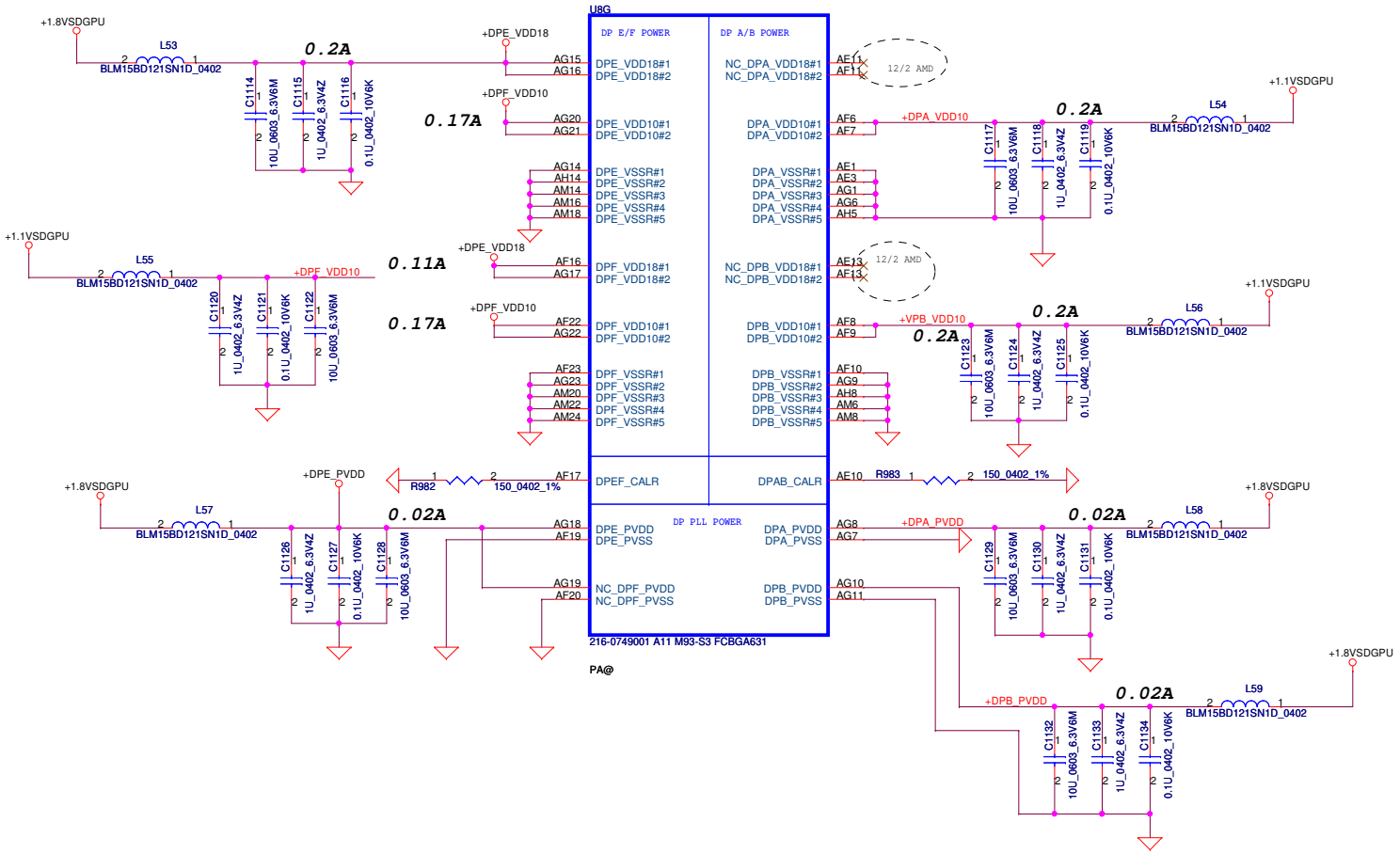
Compal Electronics, Inc.

Title: HDMI, MSIC & Thermal

Size: Custom | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 26 of 55



Security Classification	Compal Secret Data		
Issued Date	2009/03/31	Deciphered Date	2010/03/31

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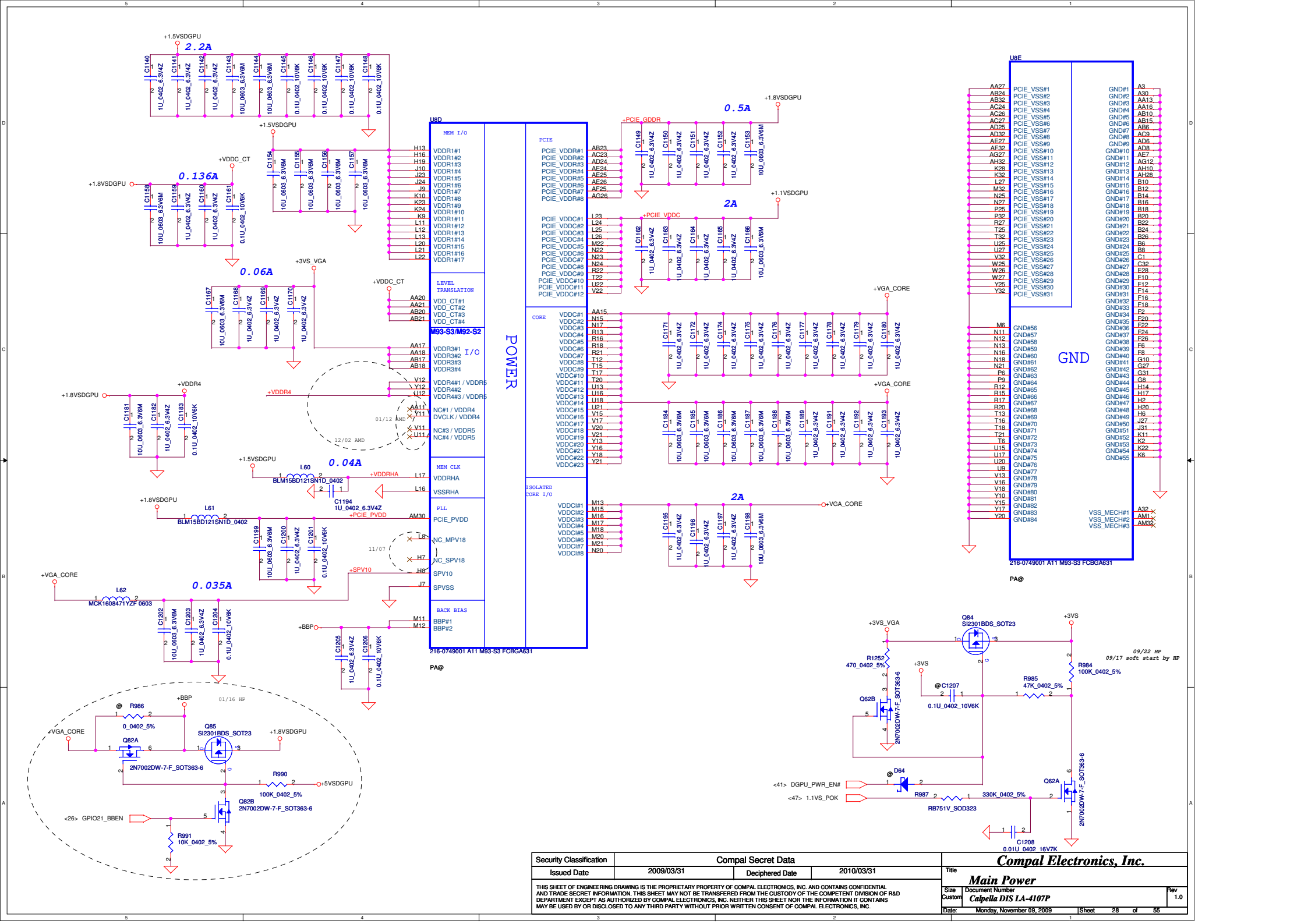
Compal Electronics, Inc.

Title: DPX POWER

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 27 of 55



Security Classification	Compal Secret Data		
Issued Date	2009/03/31	Deciphered Date	2010/03/31

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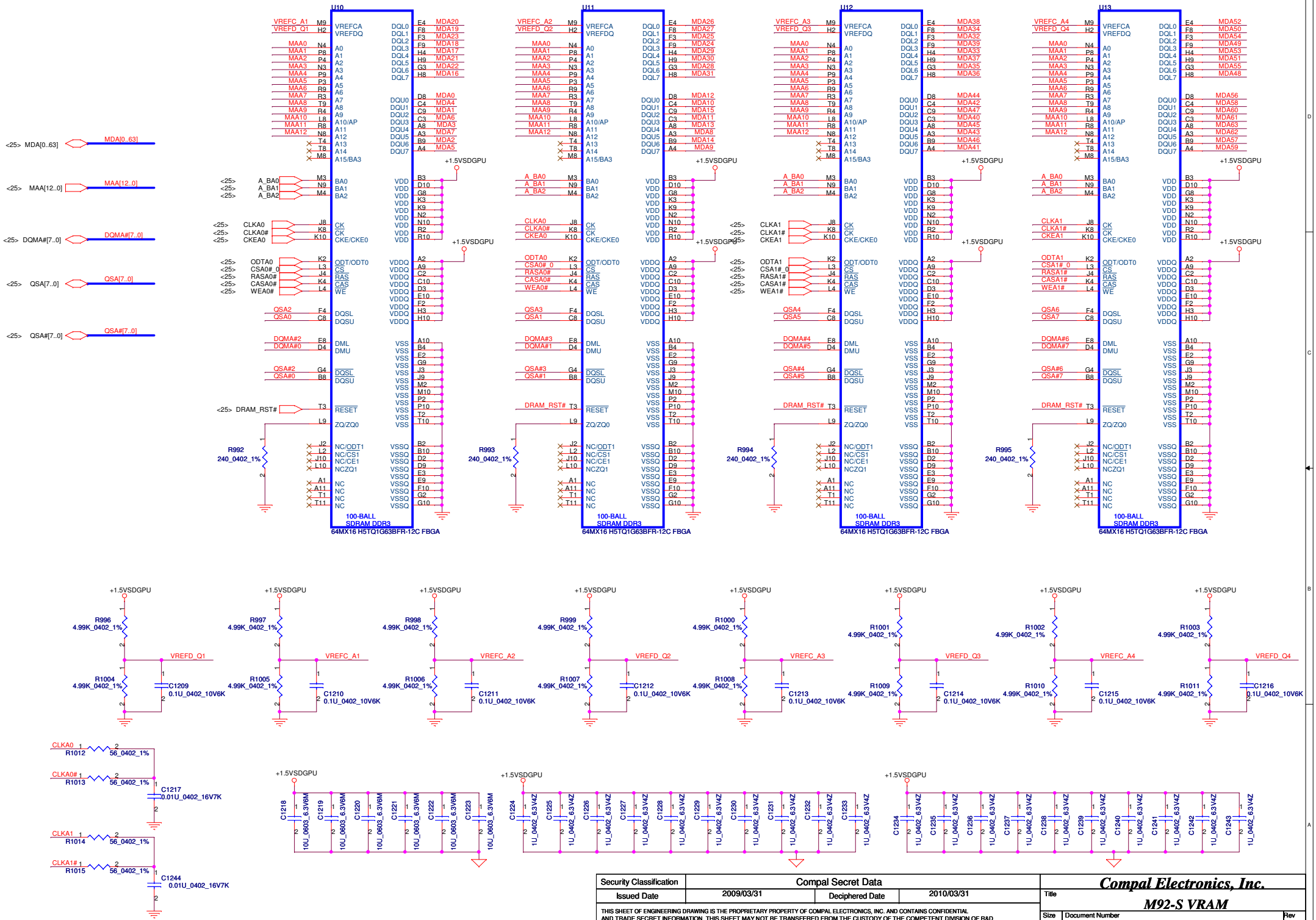
Compal Electronics, Inc.

Title: **Main Power**

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 28 of 55



Security Classification	Compal Secret Data		
Issued Date	2009/03/31	Deciphered Date	2010/03/31

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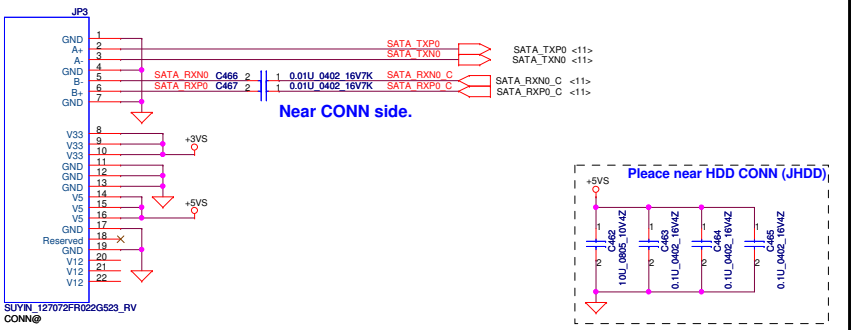
Compal Electronics, Inc.

Title: **M92-S VRAM**

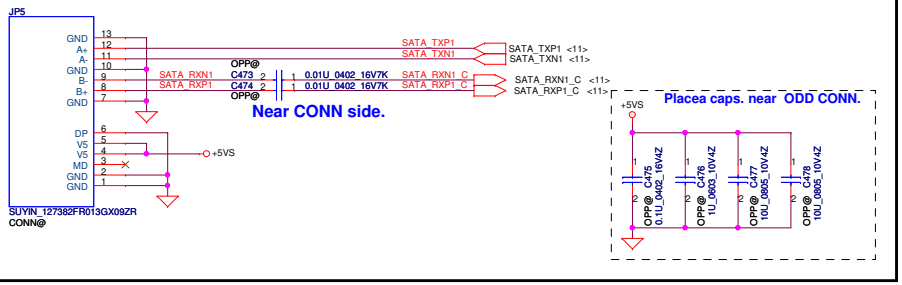
Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 Sheet 29 of 55

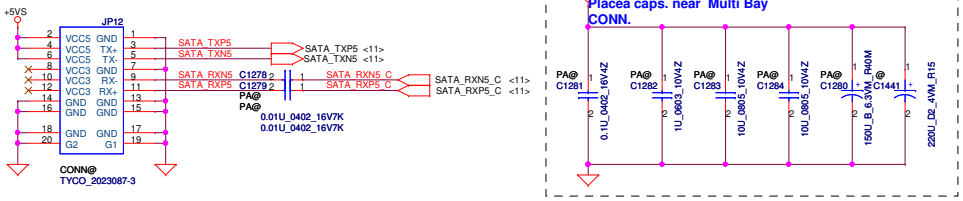
HDD Connector



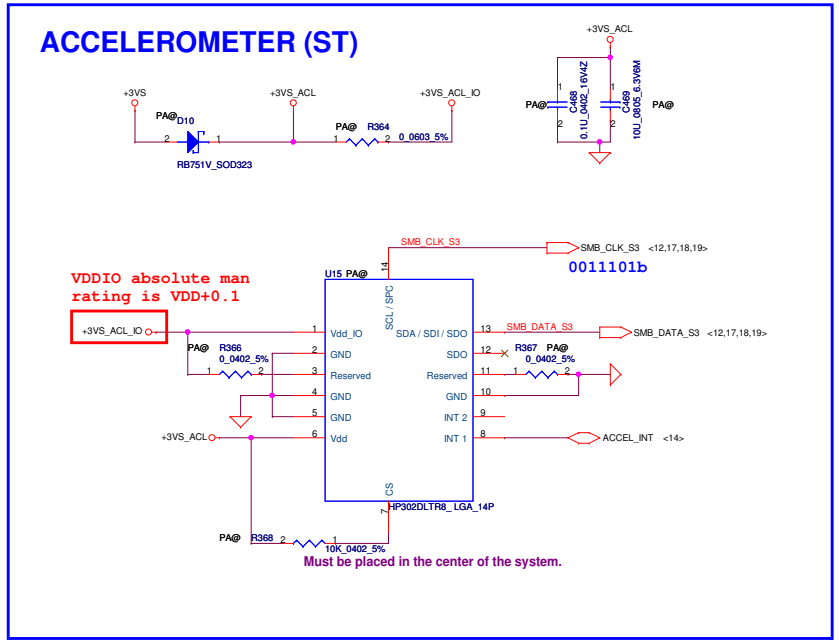
CD-ROM Connector



Multi Bay



ACCELEROMETER (ST)



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

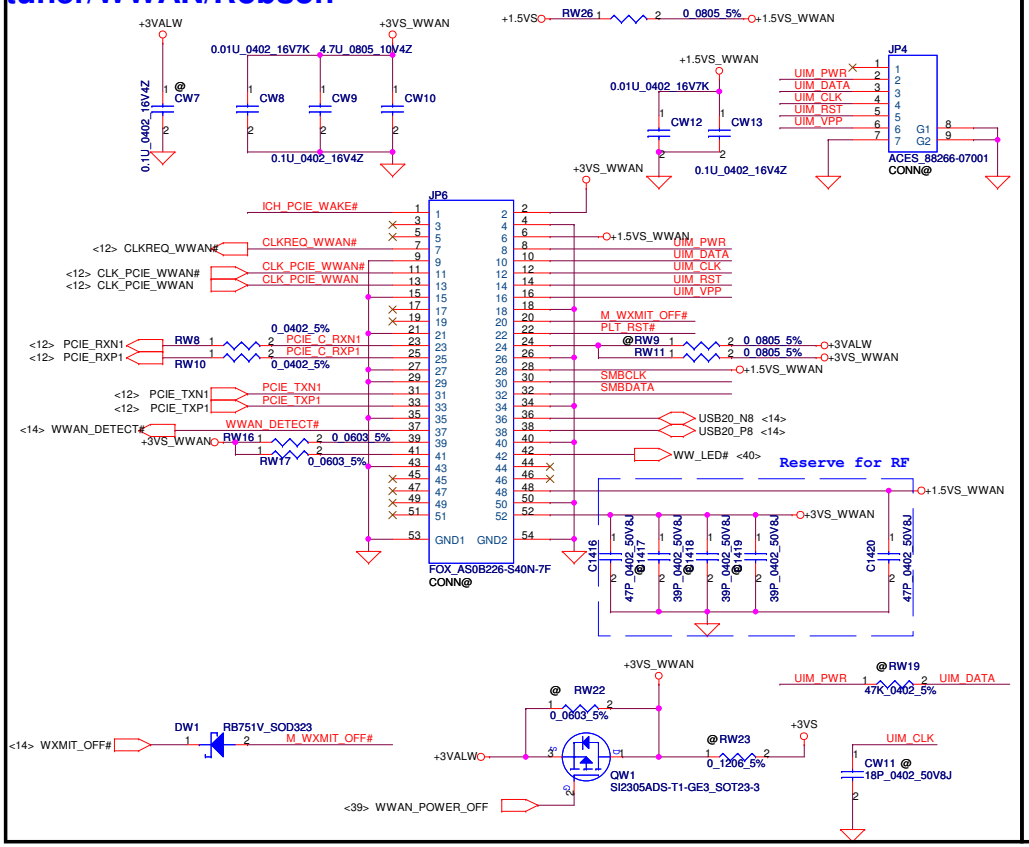
Title: **HDD & CDROM**

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

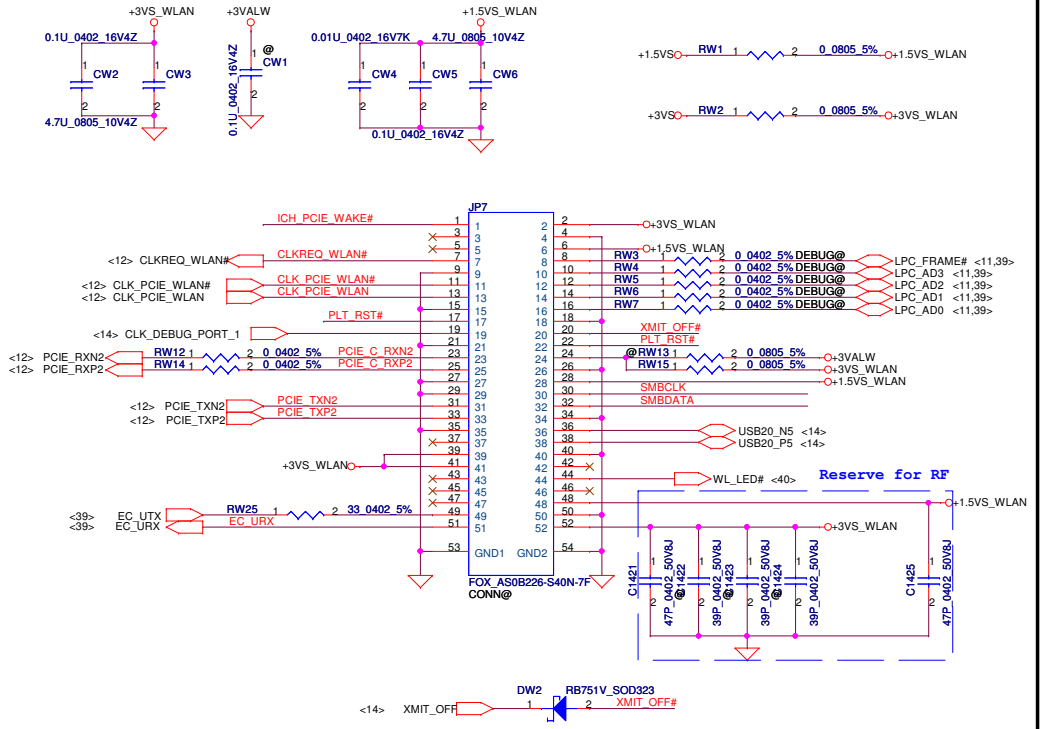
Date: Monday, November 09, 2009 Sheet 30 of 55

Mini Card 0--TV tuner/WWAN/Robson

SIM card Connector

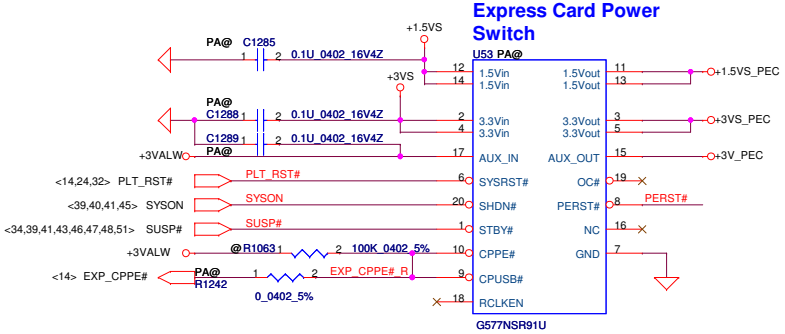


Mini Card 2---WLAN



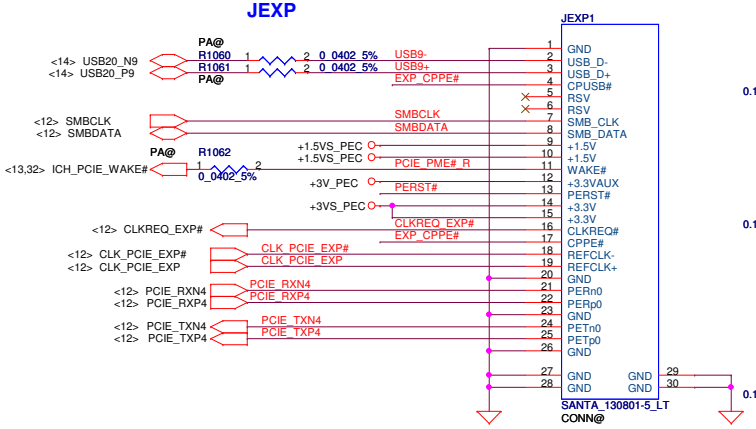
New Card

Express Card Power Switch

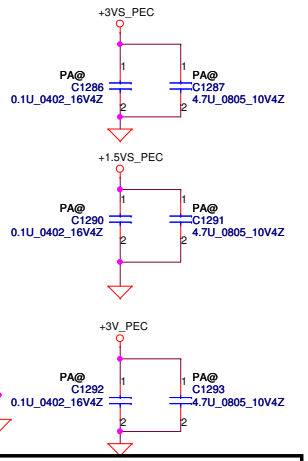


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Close to JEXP



Near to Express Card slot.



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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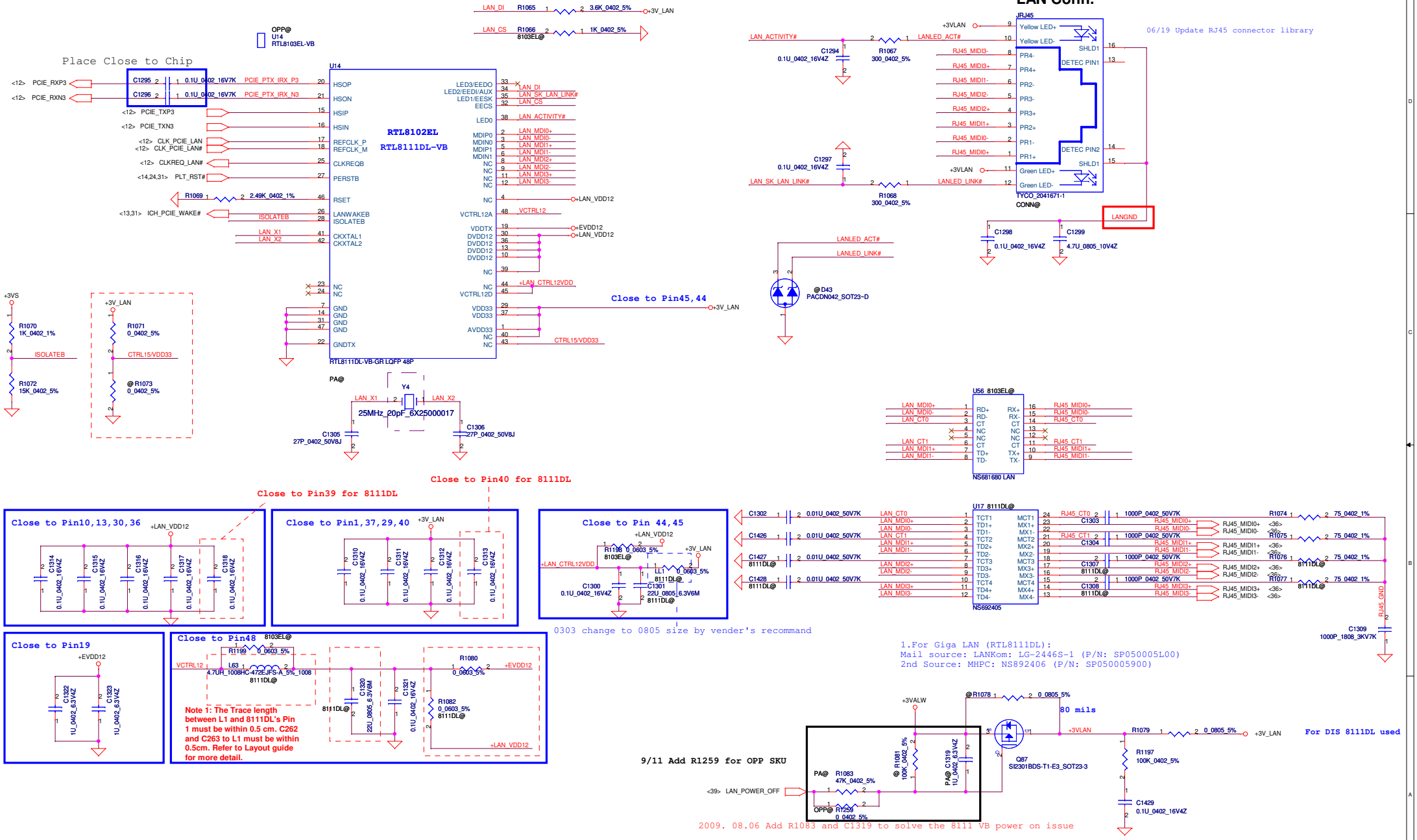
Compal Electronics, Inc.			
Title	WLAN, WWAN, New Card		
Size	Document Number	Calpella DIS LA-4107P	Rev 1.0
Date: Monday, November 09, 2009	Sheet 31 of 55		

LAN Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

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Compal Electronics, Inc.

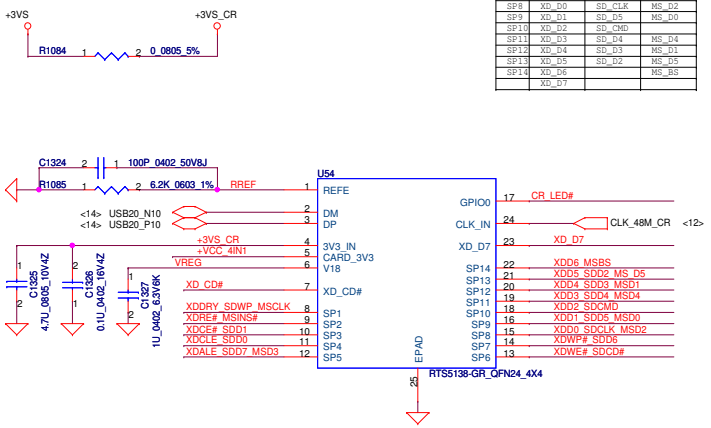
Title: USB CardReader&CONN

Size: Custom | Document Number: Calpella DIS LA-4107P | Rev: 1.0

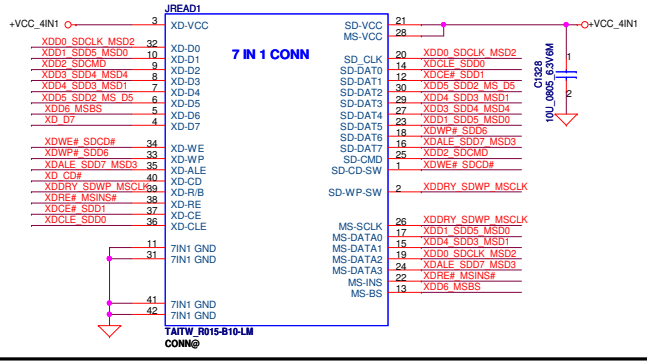
Date: Monday, November 09, 2009 | Sheet 32 of 55

RTS5138 ==>For DIS

	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

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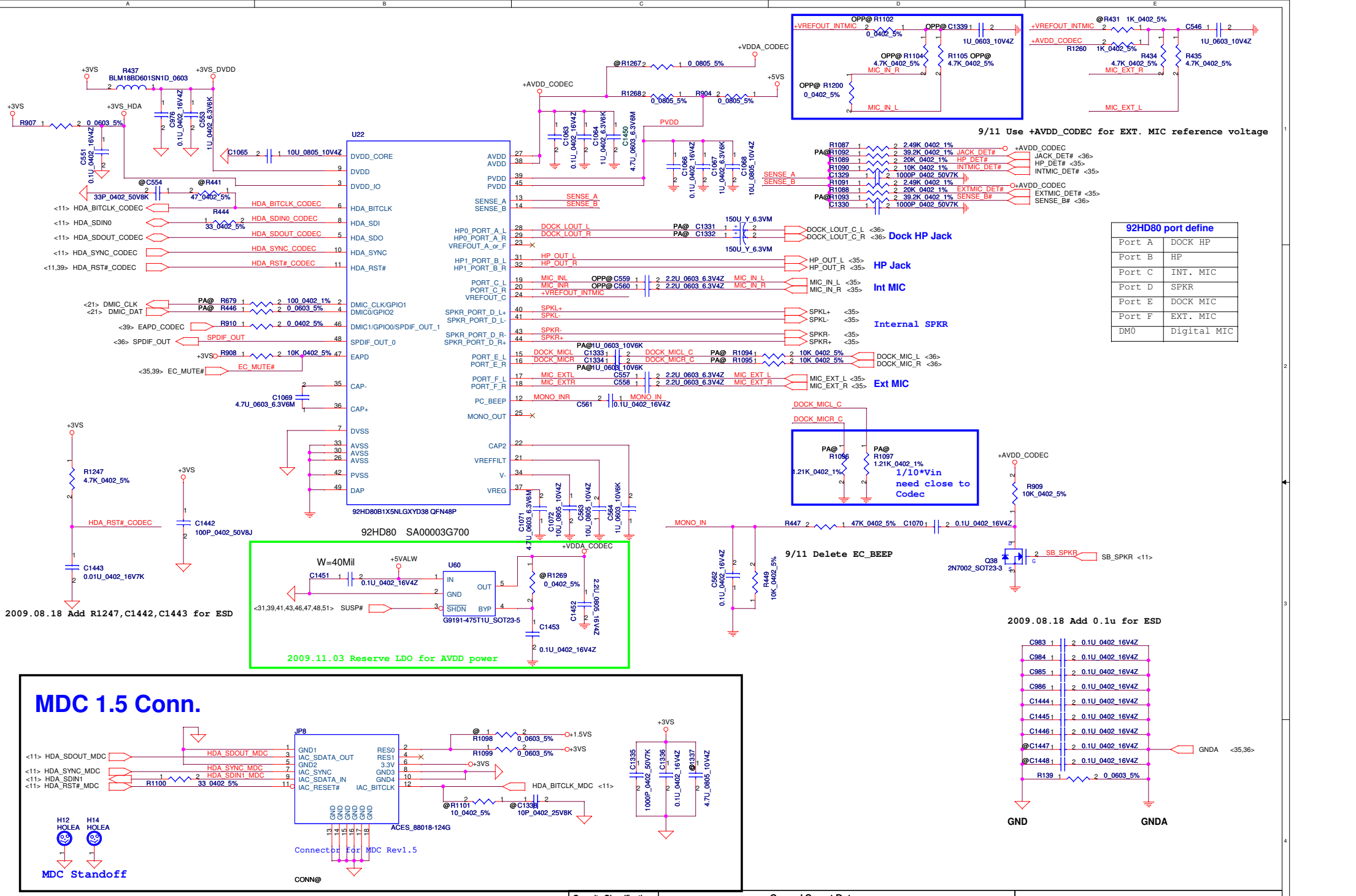
Compal Electronics, Inc.

Title: **USB CardReader&CONN**

Size: Custom | Document Number: **Calpella DIS LA-4107P** | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 33 of 55



92HD80 port define	
Port A	DOCK HP
Port B	HP
Port C	INT. MIC
Port D	SPKR
Port E	DOCK MIC
Port F	EXT. MIC
DMO	Digital MIC

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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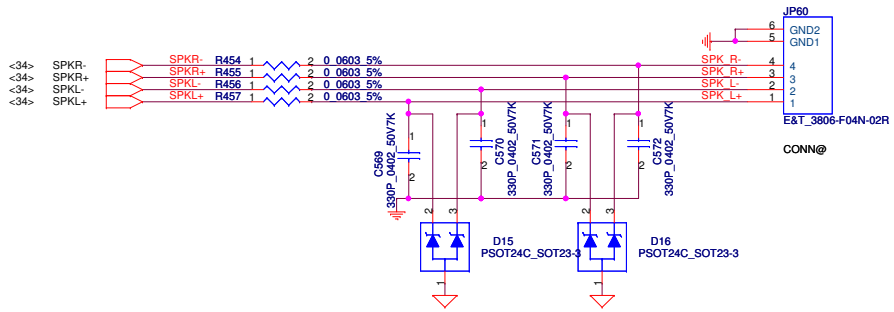
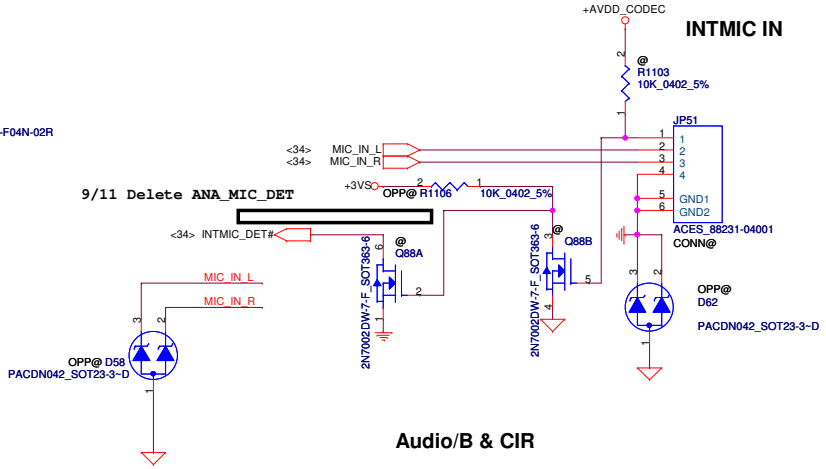
Title	Codec_IDT92HD80		
Size: Custom	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 34 of 55		

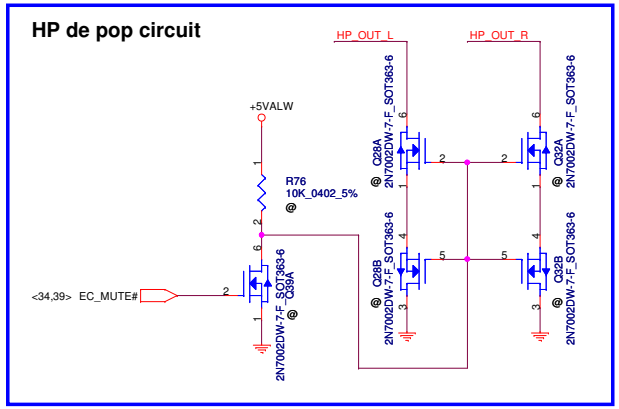
SPEAKER



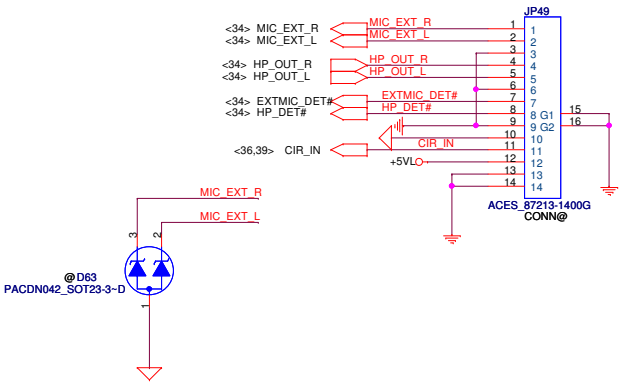
9/11 Delete ANA_MIC_DET



HP de pop circuit



Audio/B & CIR



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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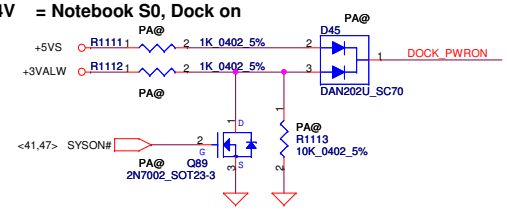
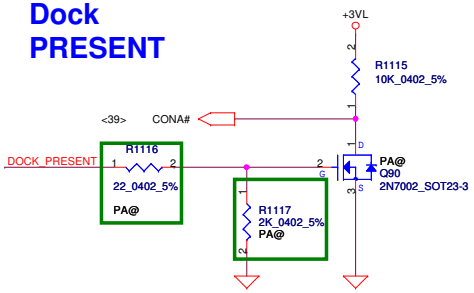
Title	AMP & Audio Jack		
Size Custom	Document Number	Calpella DIS LA-4107P	Rev 1.0
Date: Monday, November 09, 2009	Sheet 35 of 55		

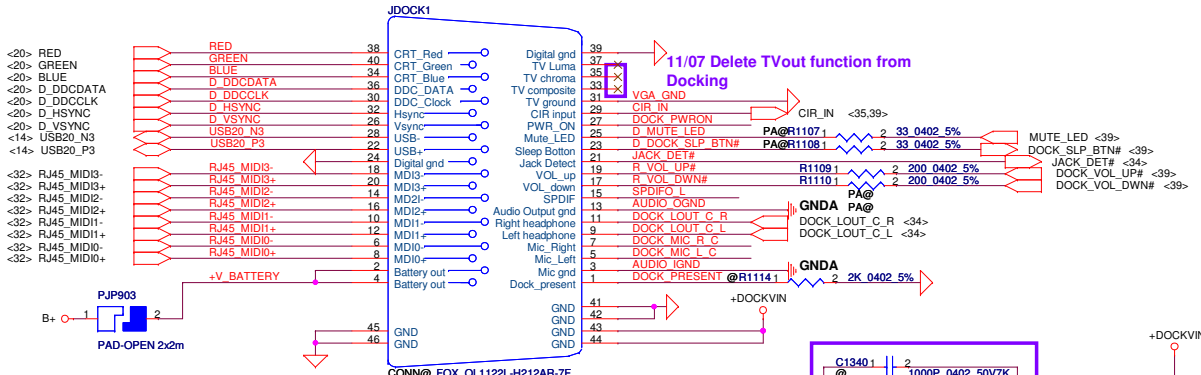
Atlas/ Saturn Dock

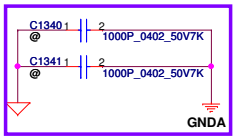
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



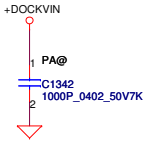
Dock PRESENT





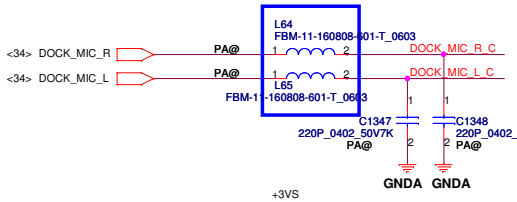


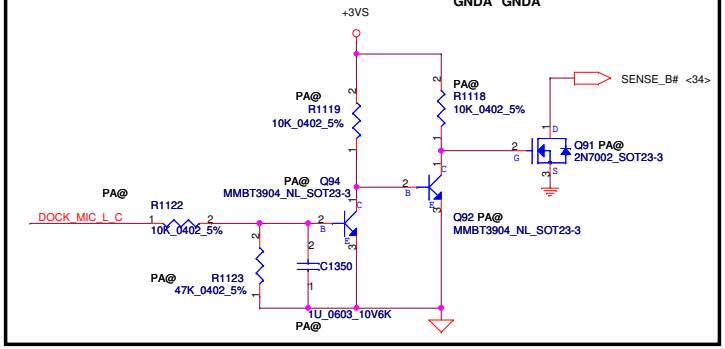
11/17 Reserve

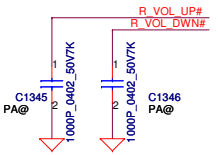


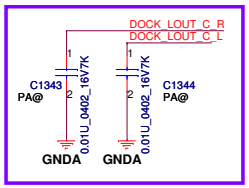
MIC_Dock

Need 600 Ohm 500 mA

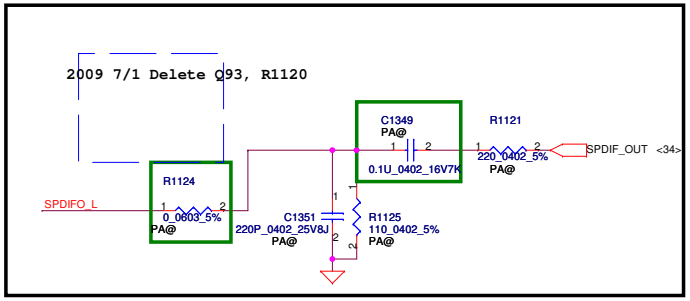








11/17 Recommend



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Issued Date	2007/08/28	Deciphered Date	2006/03/10

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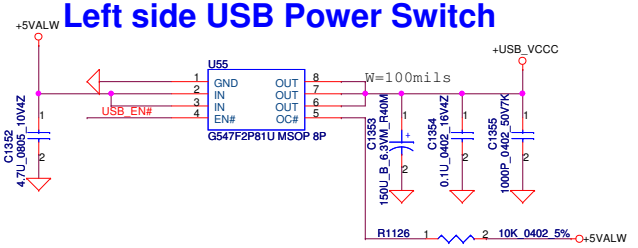
Compal Electronics, Inc.

Title: DOCK CONN.

Size	Document Number	Rev
Custom	Calpella DIS LA-4107P	1.0

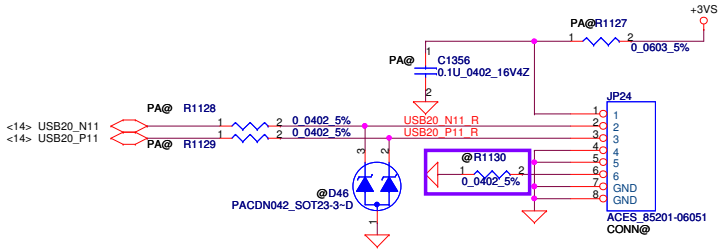
Date: Monday, November 09, 2009 Sheet 36 of 55

Left side USB Power Switch

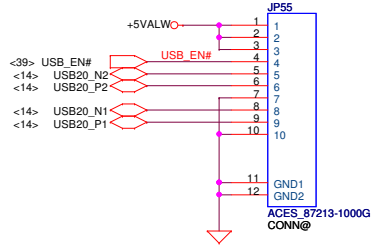


Finger printer

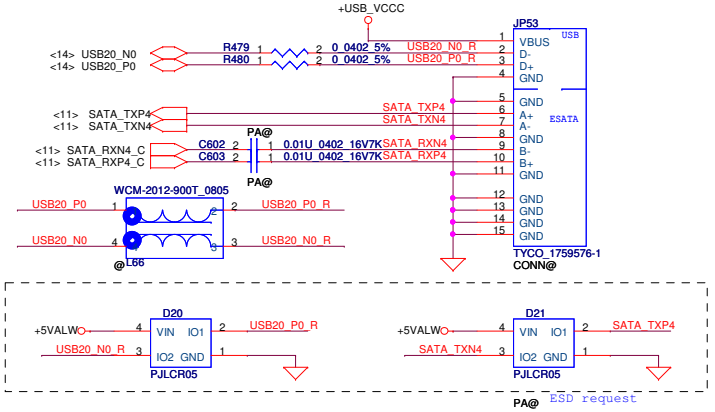
Change Finger printer from USB port7 to USB port 11



USB cable connector for Right side

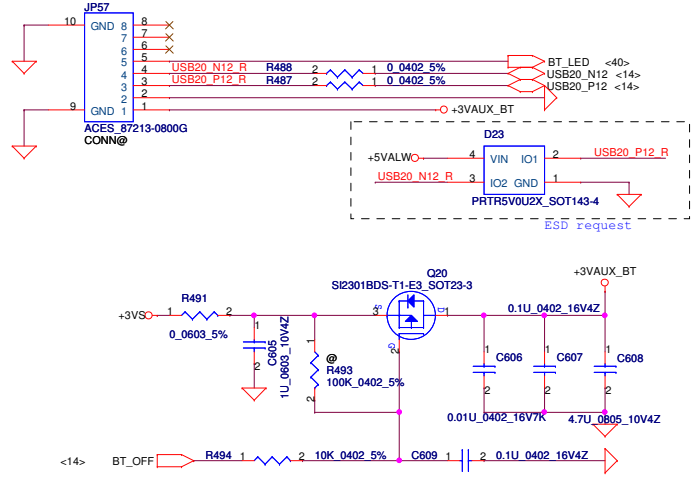


Left\ side ESATA/USB combination Connector



BT Connector (SoftBreeze) Need change to New version

Change Bluetooth from USB port 6 to USB port 12



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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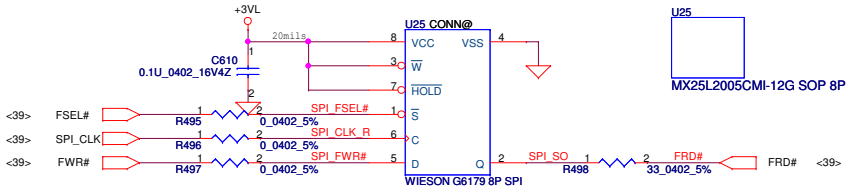
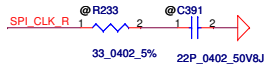
Compal Electronics, Inc.			
Title: USB, BT, eSATA			
Size	Document Number: Calpella DIS LA-4107P		Rev: 1.0
Date: Monday, November 09, 2009	Sheet 37 of 55		

SPI ROM => 256K (EC code)

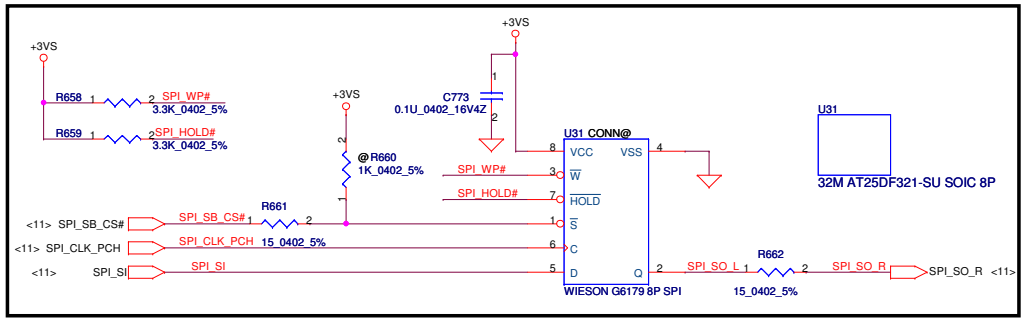


SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P

* SA00003GK00 S IC FL 2M MX25L2005CMI-12G SOP 8P (MXIC)
SA00003GM00 S IC FL 2M W25X20AVSNIG SOIC 8P (WINBOND)



SPI ROM on PCH => 4M (ME code + System BIOS)



PA/OPP SA000031Q00 S IC FL 32M AT25DF321-SU SOIC 8P

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: BIOS ROM

Size | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 38 of 55

VCC	3.3V+/-5%
Ra	100K+/-5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
Blade UMA	0	0V	0V	0V
Blade SG	8.2K+/-5%	0.216V	0.250V	0.289V
Bee UMA	18K+/-5%	0.436V	0.503V	0.538V
Bee DIS	33K+/-5%	0.712V	0.819V	0.875V

Ra

Board ID pin change to Pin75

Rb

EMI solution

EC DEBUG port

2009.08.17 R526 PU change the connection from +3VL to +3VALW

9/11 Cap. sensor board change to +3VL

10/26 Add R1265 for ATE test jig

9/11 Pin26 change to ME_EN

9/11 Pin 76 change to SUS_PWR_DN_ACK

PV check BOM structure

11/09 don't stuff when use C0

PV PWROK sequence issue

For C Revision

For EMI

14" INT_KBD CONN.(TYPE "D" KB)

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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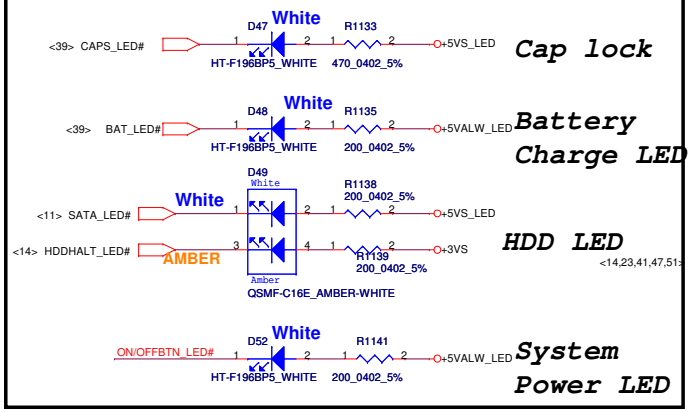
Compal Electronics, Inc.

Title: EC KB926/KB Conn.

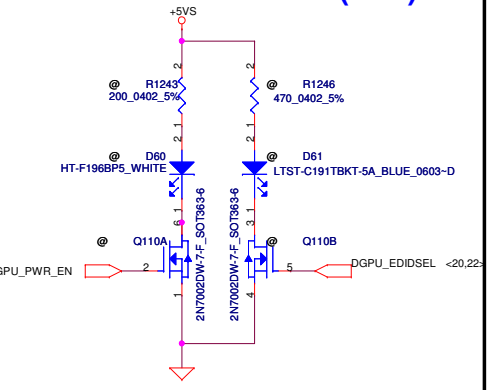
Size: | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 39 of 55

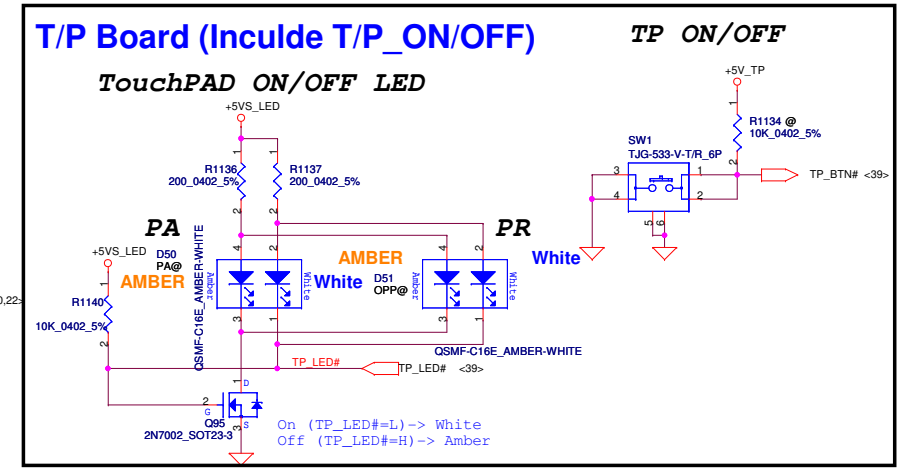
System & Caps-Lock LED



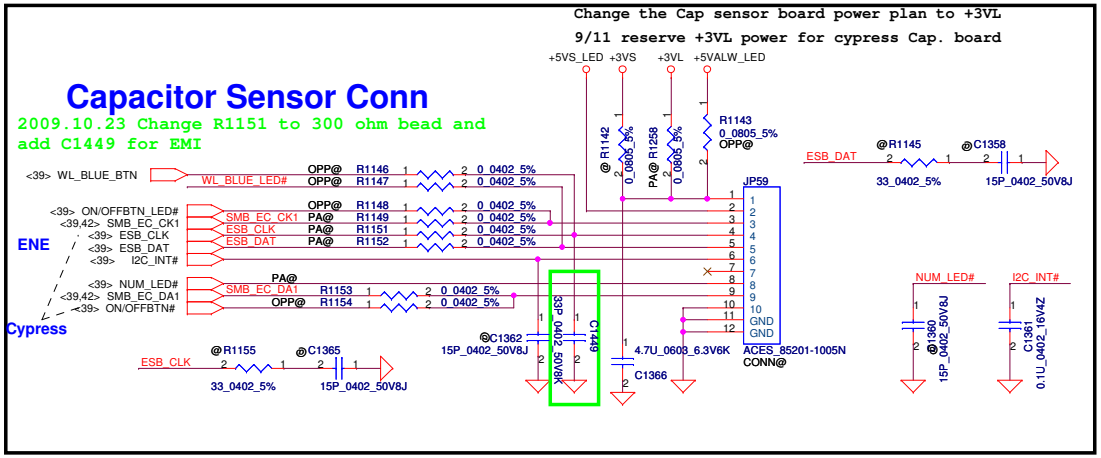
Switch function LED(test)



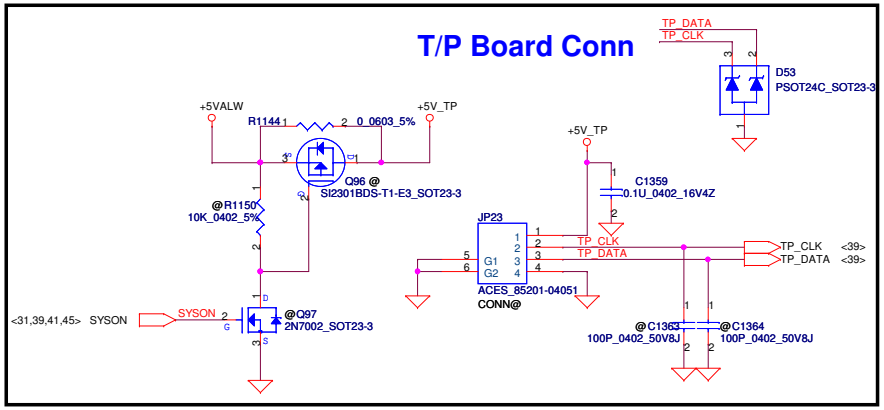
T/P Board (Inculde T/P_ON/OFF)



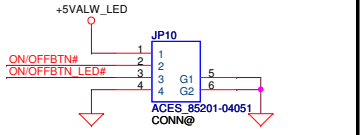
Capacitor Sensor Conn



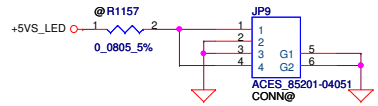
T/P Board Conn



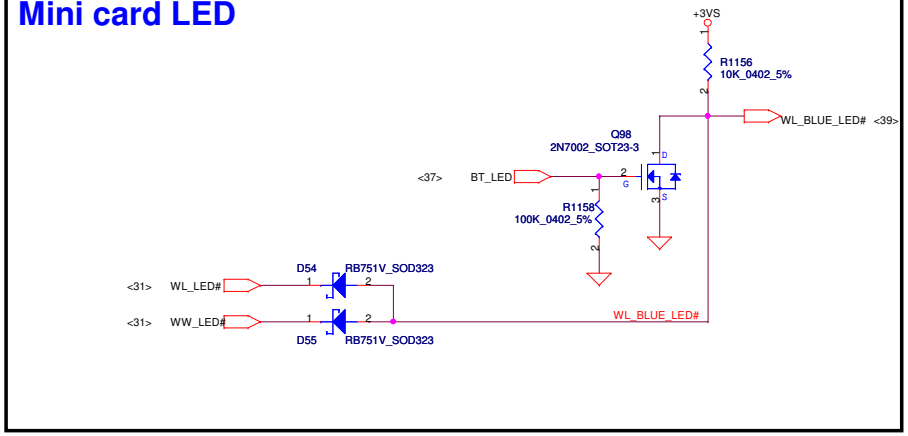
ON/OFF Button Connector



Keyboard backlight Conn

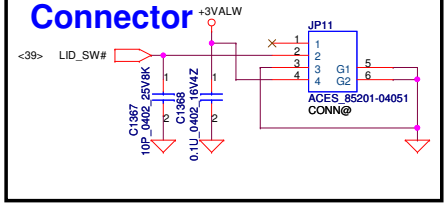


Mini card LED



Lid Switch Connector

Change the Lid switch power plan to +3VALW



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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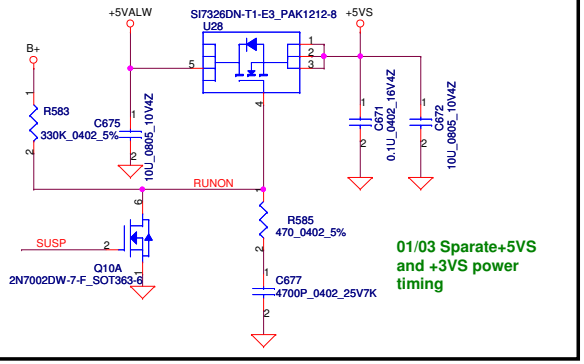
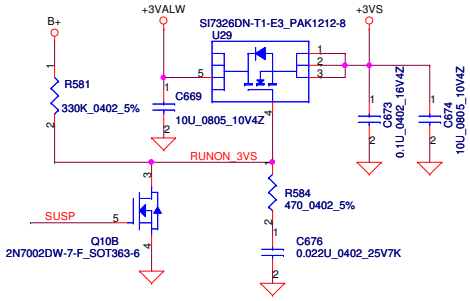
Compal Electronics, Inc.			
Title	KBD, ON/OFF, SW, CIR		
Size	Document Number	Rev	
	Calpella DIS LA-4107P	1.0	
Date: Monday, November 09, 2009	Sheet 40 of 55		

+5VALW to +5VS Transfer



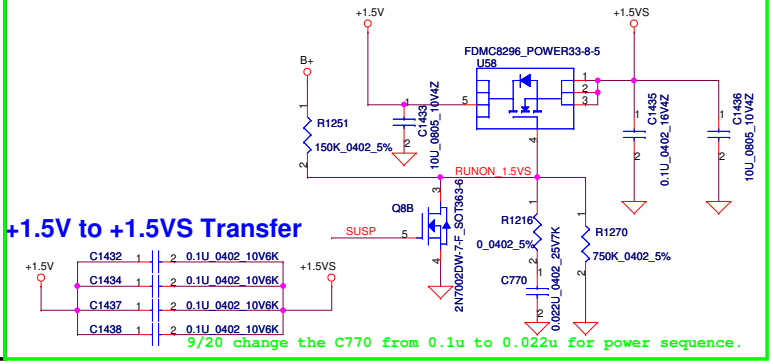
01/03 Sparate+5VS and +3VS power timing

+3VALW to +3VS Transfer



9/20 change the C676 from 0.1u to 0.022u for power sequence.

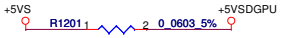
+1.5V to +1.5VS Transfer



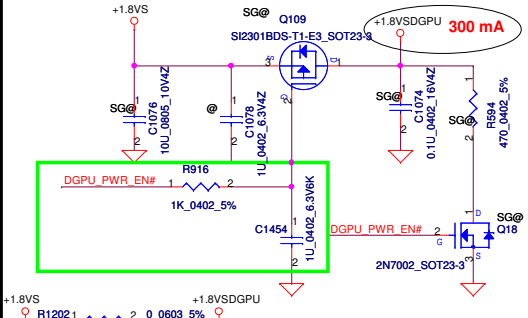
+1.5V to +1.5VS Transfer

9/20 change the C770 from 0.1u to 0.022u for power sequence.

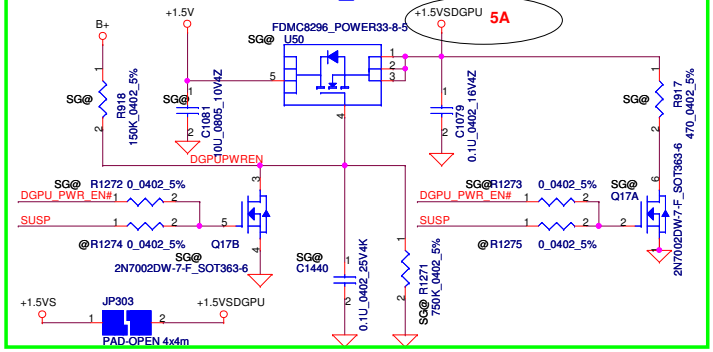
+5VS to +5VSDGPU Transfer



+1.8VS to +1.8VSDGPU Transfer

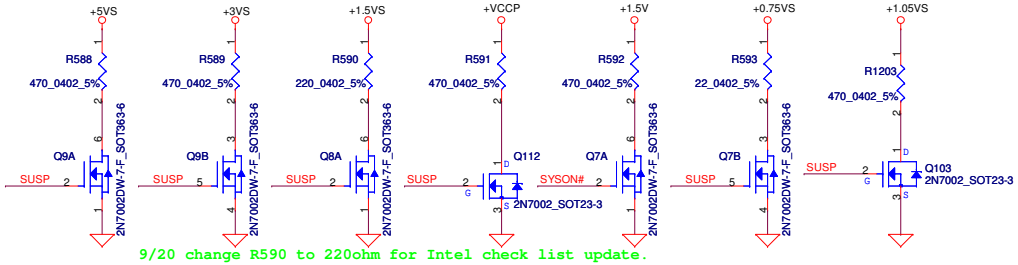


+1.5V to +1.5VS_NV Transfer



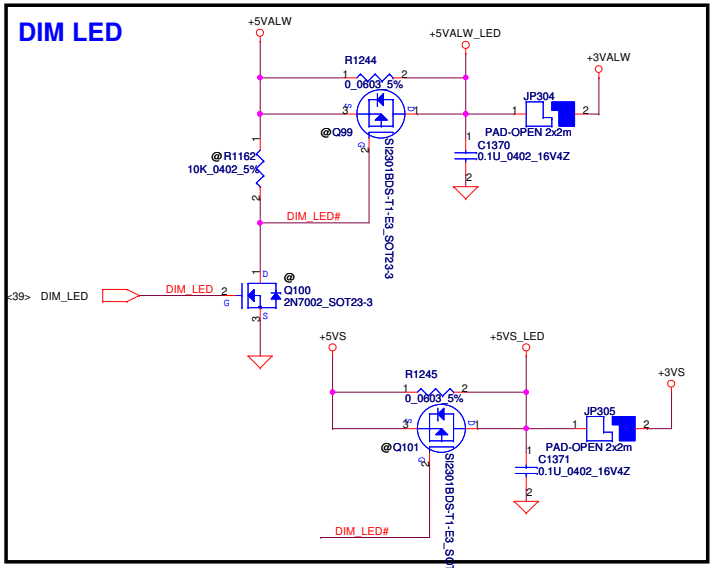
Discharge circuit

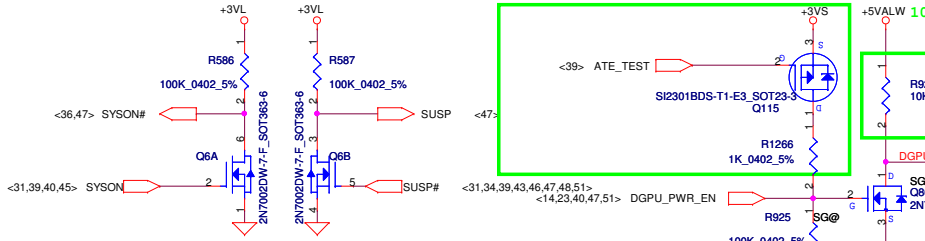
9/20 change R593 to 22ohm for Intel check list update.

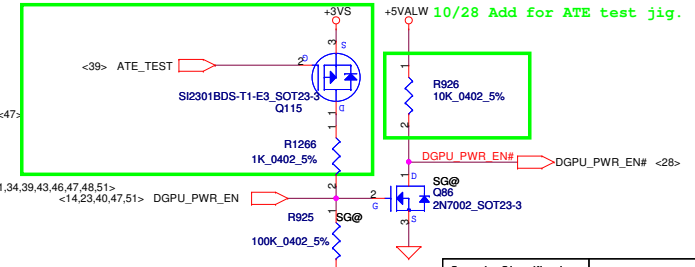


9/20 change R590 to 220ohm for Intel check list update.

DIM LED







+5VALW 10/28 Add for ATE test jig.

H1 HOLEA, H3 HOLEA, H13 HOLEC, H4 HOLEA, H5 HOLEA, H6 HOLEA, H7 HOLEA, H8 HOLEA, H9 HOLEA, H10 HOLEA, H15 HOLEA, H16 HOLEA, H17 HOLEA, H18 HOLEA, H19 HOLEC, H20 HOLEC, H11 HOLEA, FM1, FM2, FM3, FM4

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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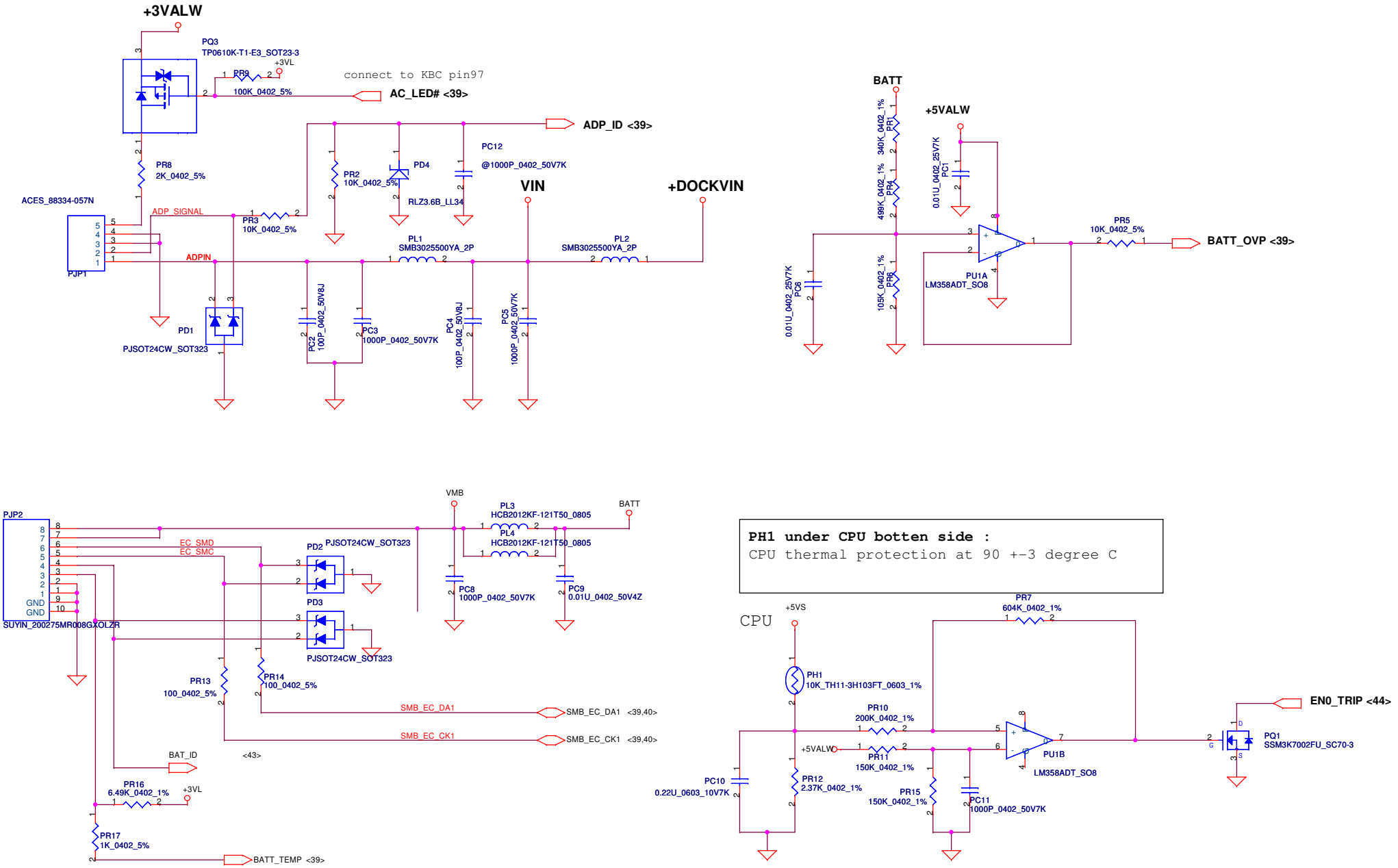
Compal Electronics, Inc.			
Title	DC/DC Interface		
Size	Document Number	Rev	
	Calpella DIS LA-4107P	1.0	
Date: Monday, November 09, 2009	Sheet 41 of 55		



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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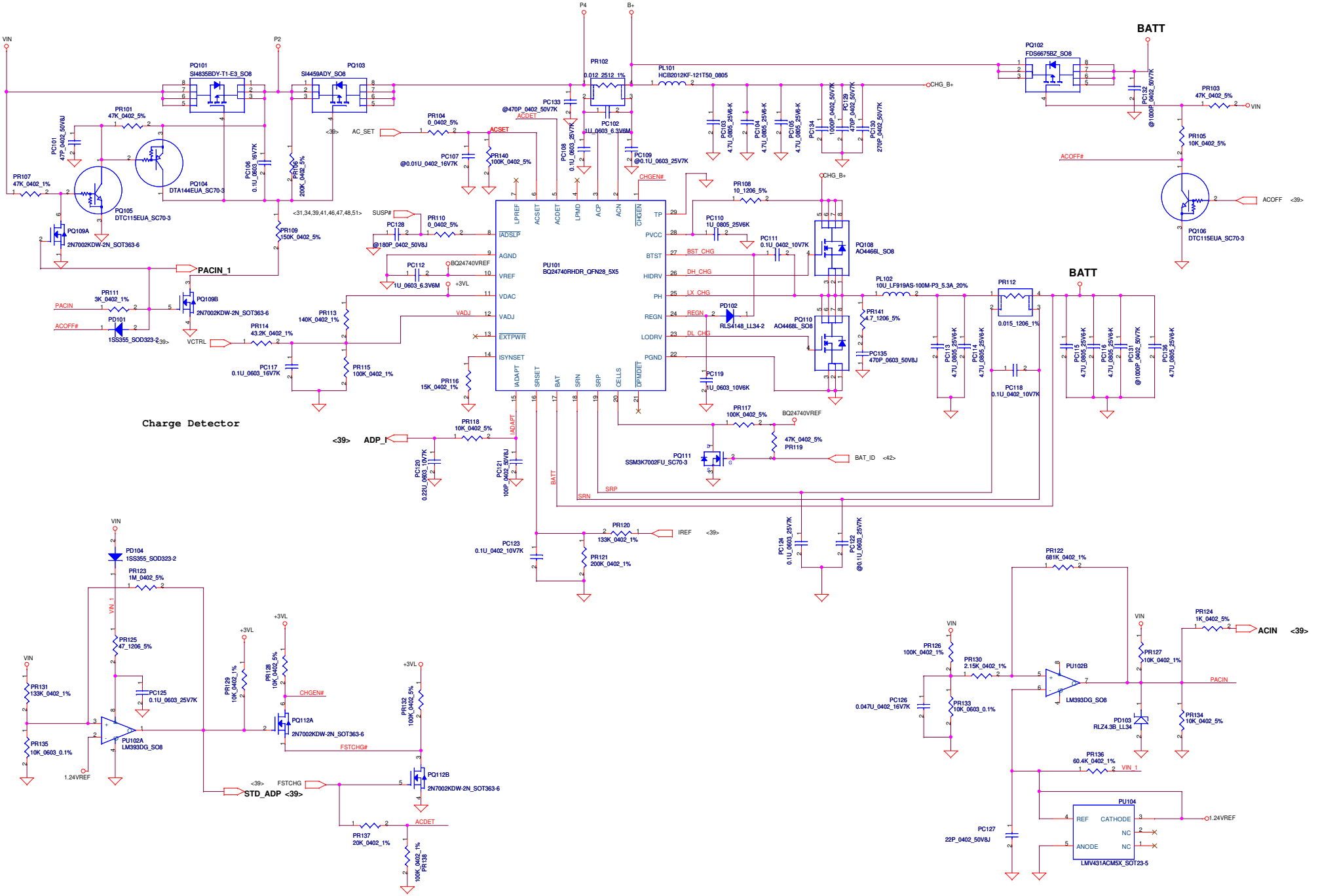
Compal Electronics, Inc.			
Title	DC Connector/CPU_OTP		
Size	Document Number	Rev	
	Calpella DIS LA-4107P	1.0	
Date: Monday, November 09, 2009	Sheet 42 of 55		



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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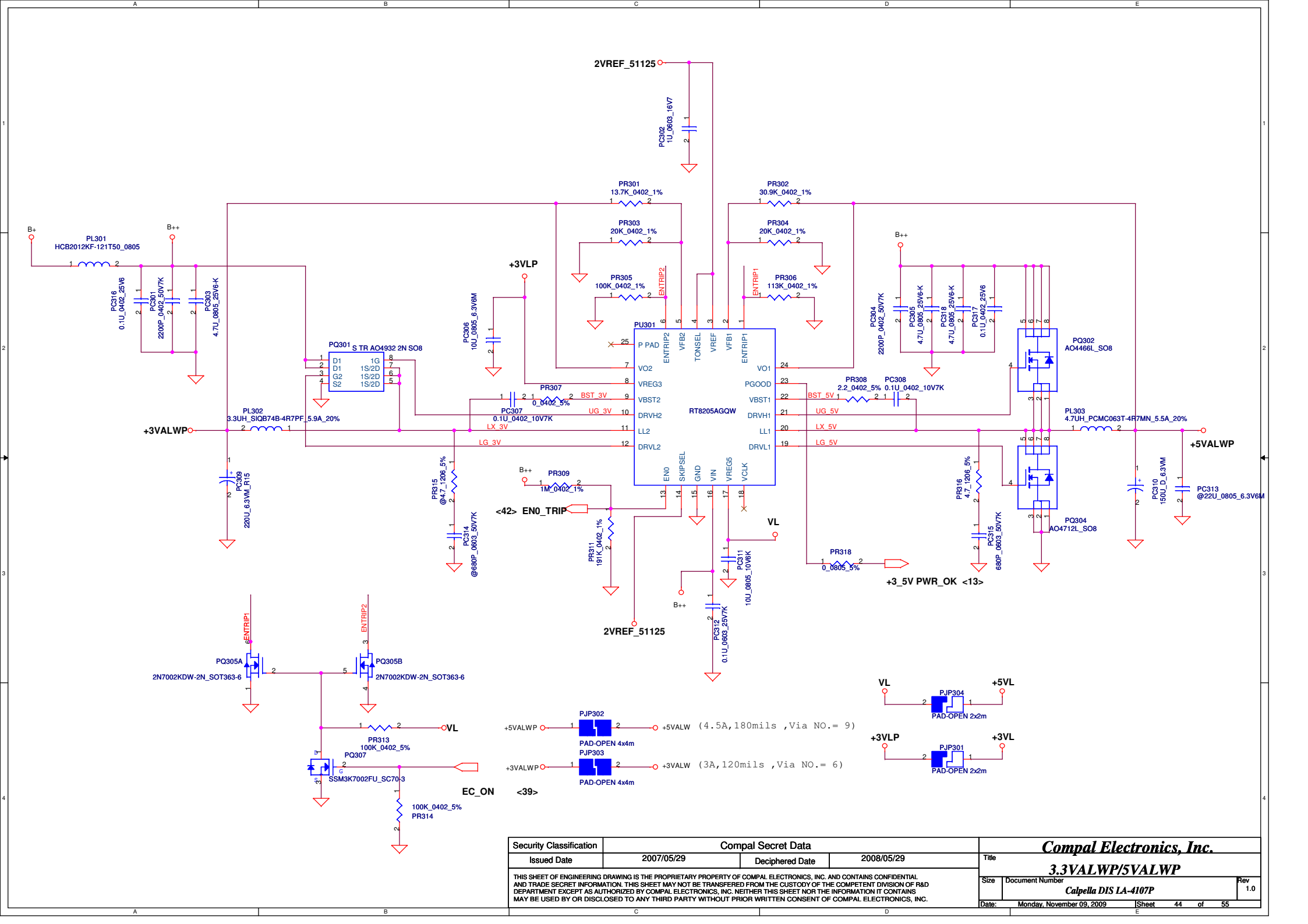
Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 43 of 55



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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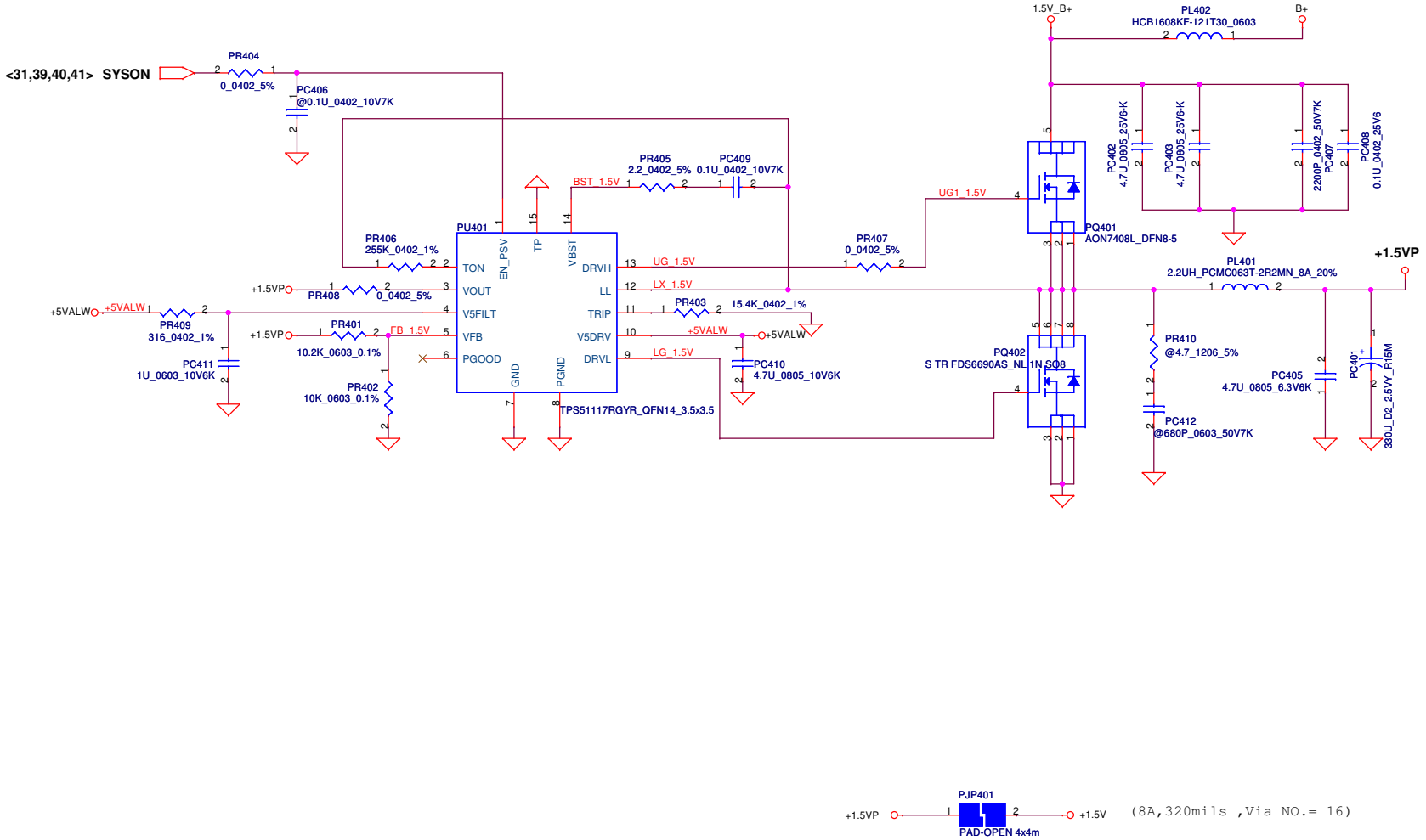
Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 Sheet 44 of 55



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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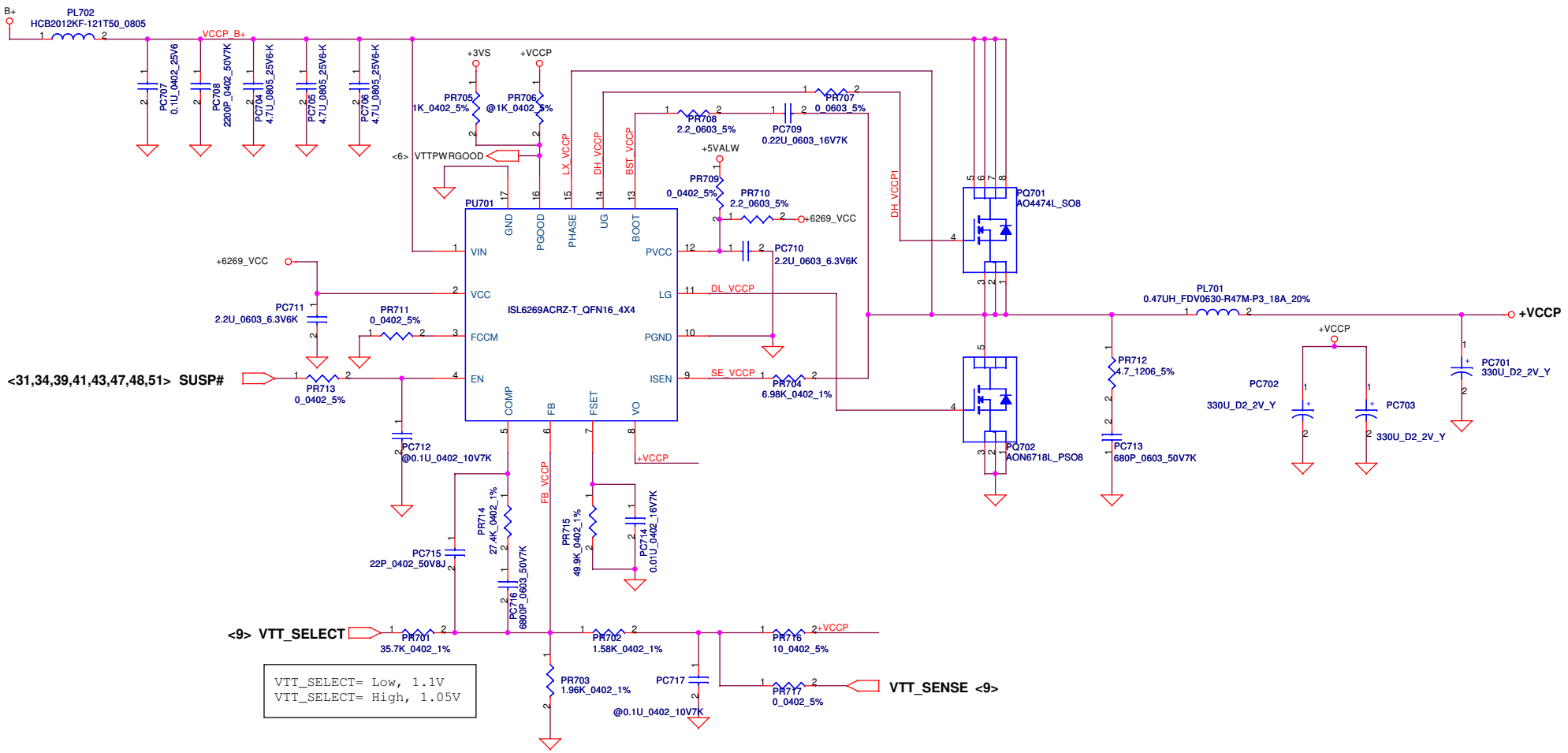
Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 45 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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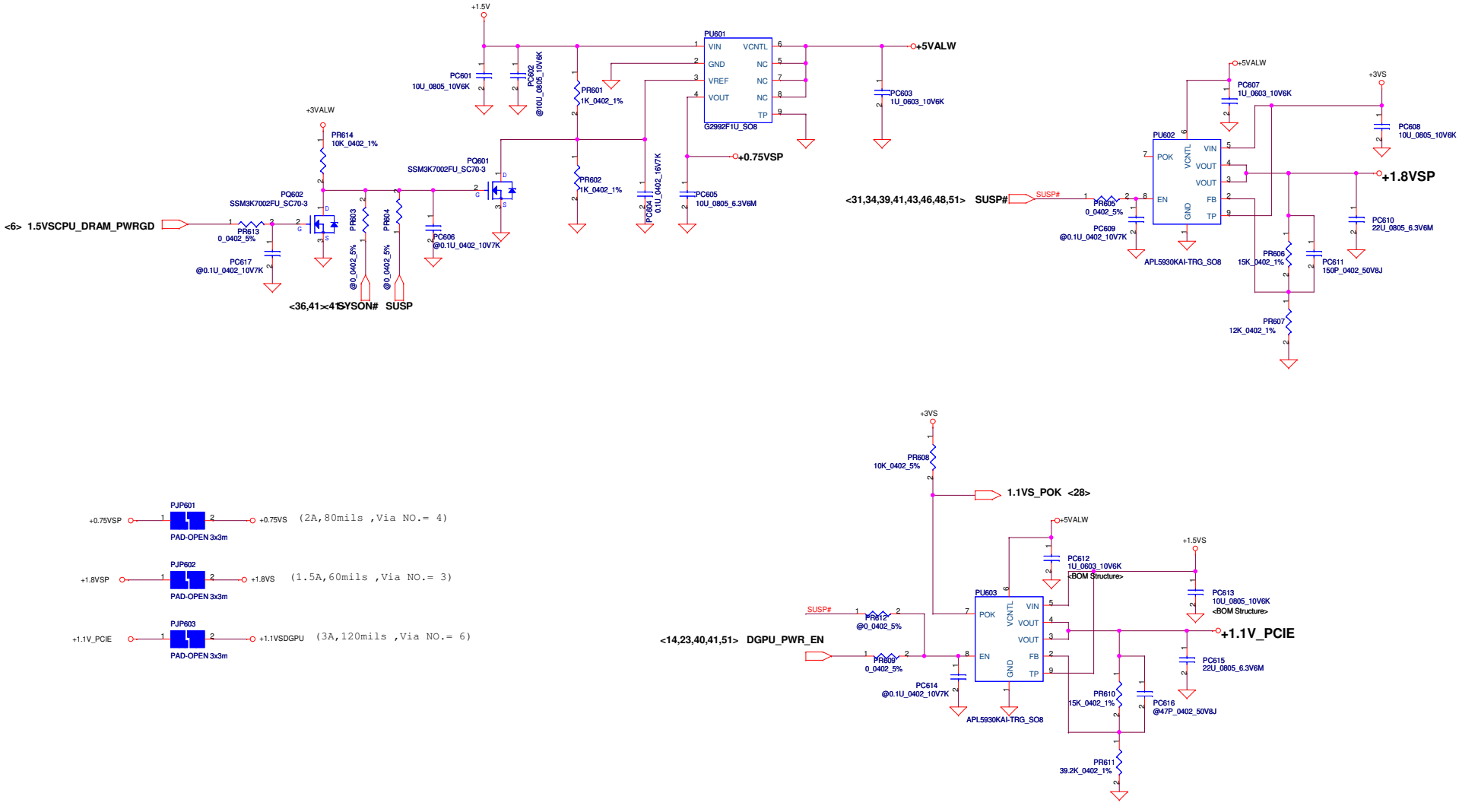
Compal Electronics, Inc.

Title: **1.05V_VCCP**

Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 46 of 55



Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

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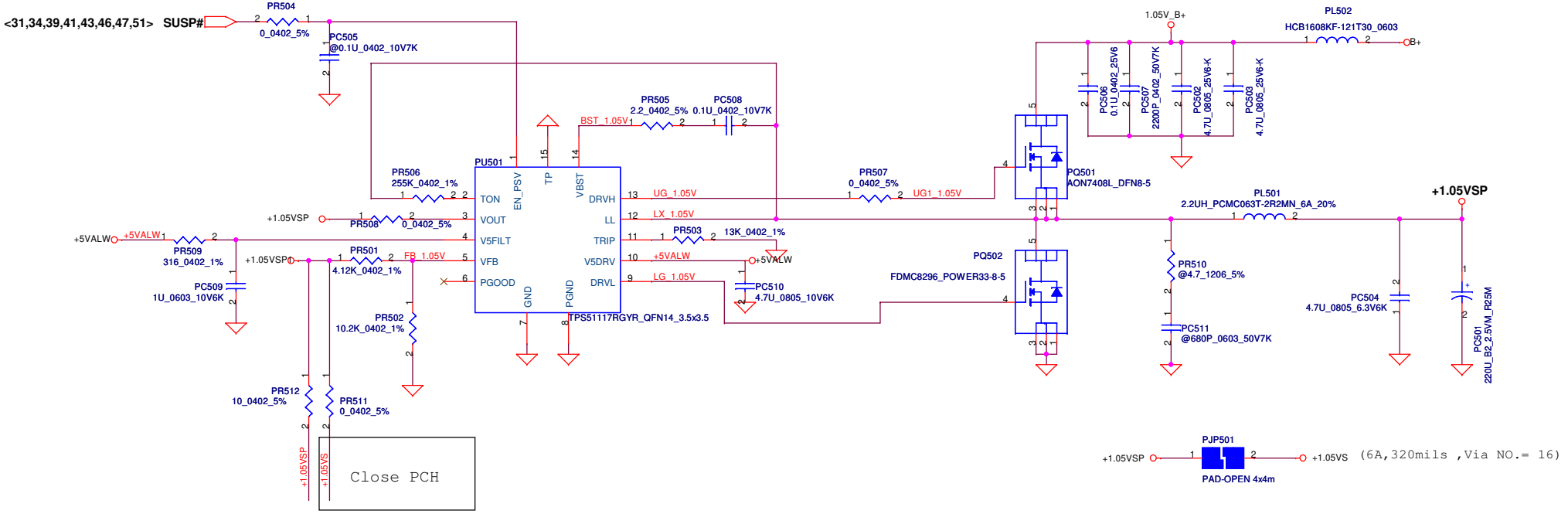
Compal Electronics, Inc.

Title: **0.75VP/1.8VSP/1.1V_PCIE**

Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 47 of 55



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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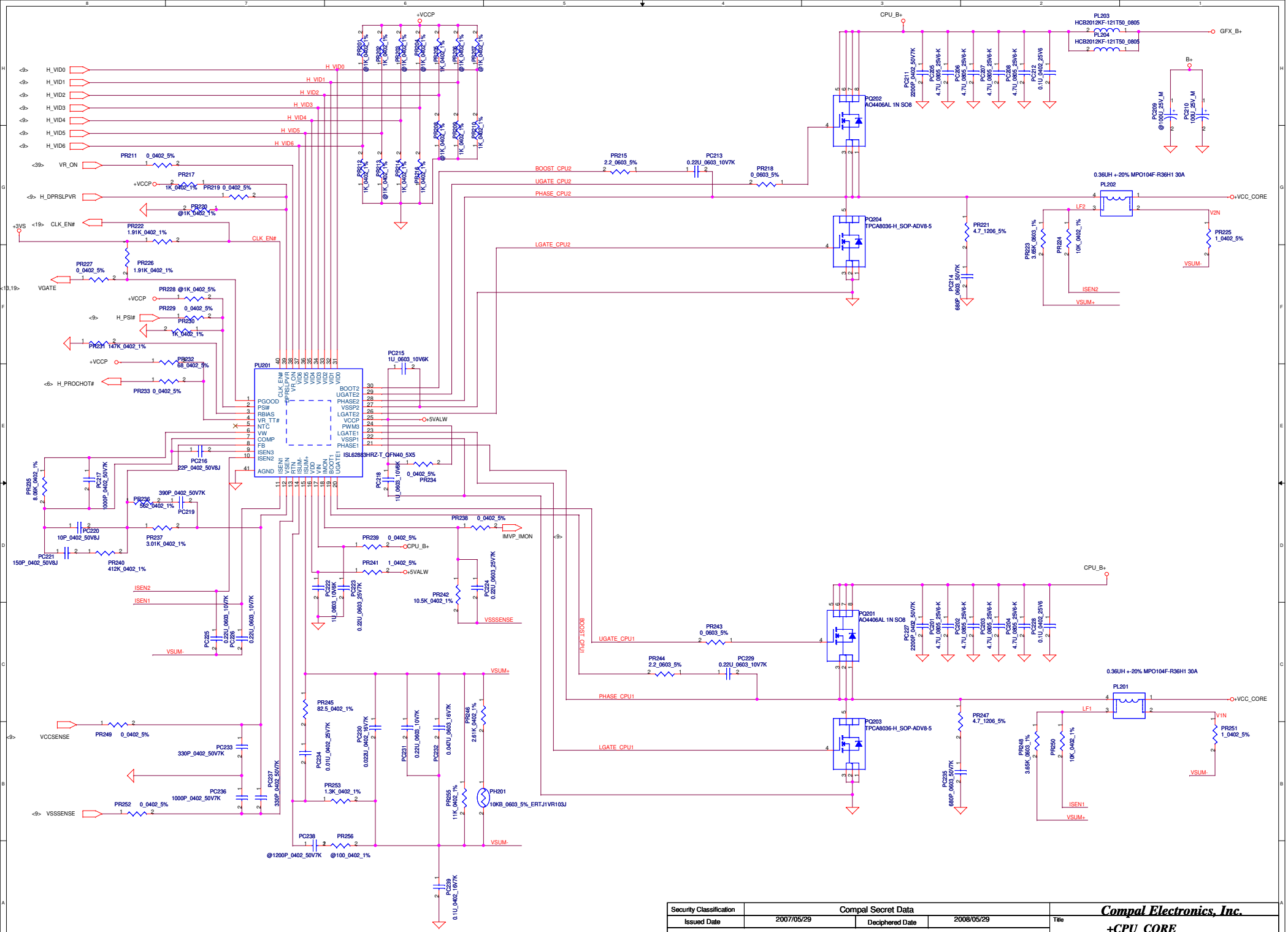
Compal Electronics, Inc.

Title: **1.05VSP**

Size	Document Number	Rev
	Calpella DIS LA-4107P	1.0

Date: Monday, November 09, 2009 | Sheet 48 of 55



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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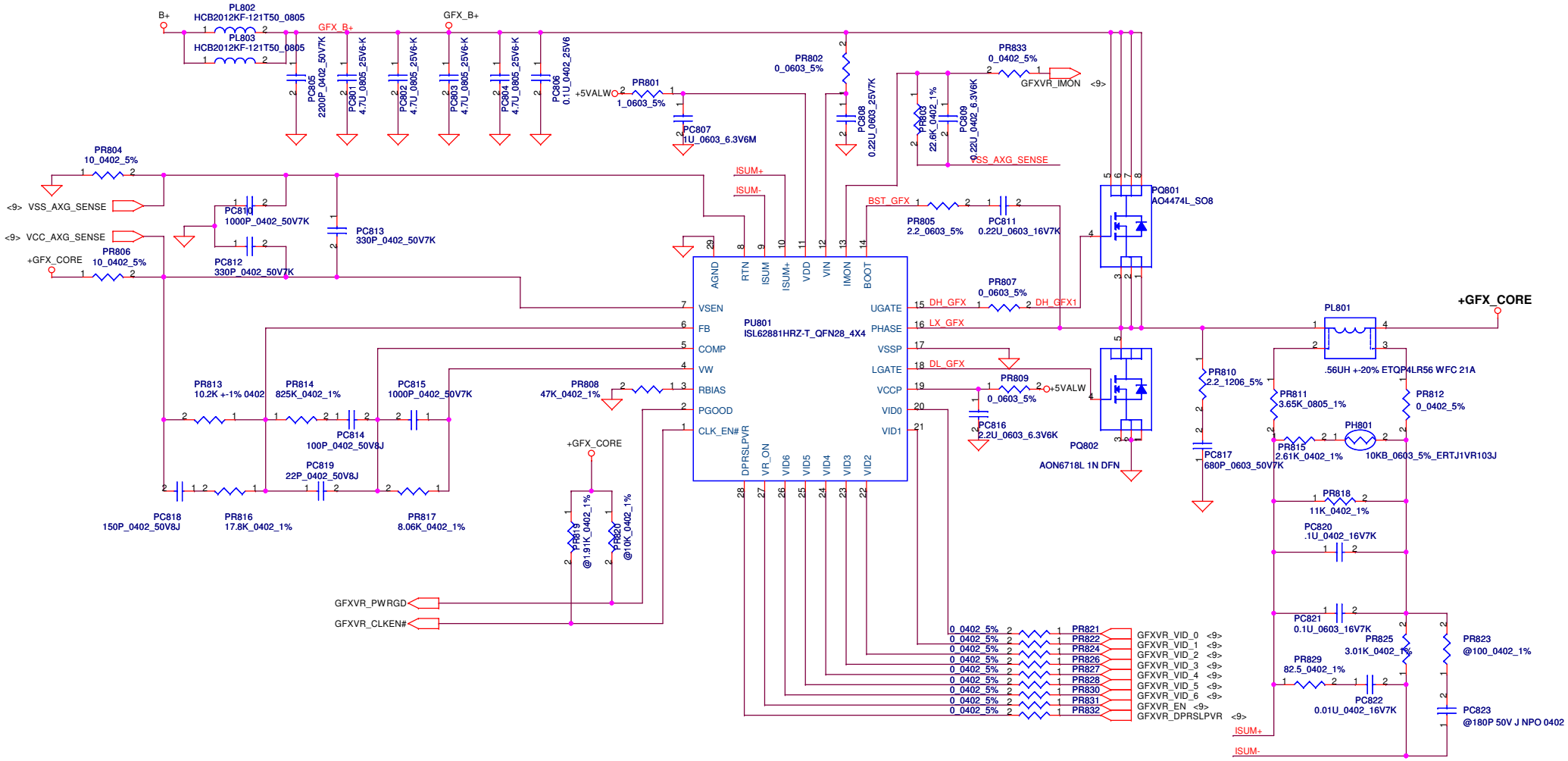
Compal Electronics, Inc.			
Title	+CPU_CORE		
Size	Document Number	Rev	
	Calpella DIS LA-4107P	1.0	
Date: Monday, November 09, 2009	Sheet 49 of 55		



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

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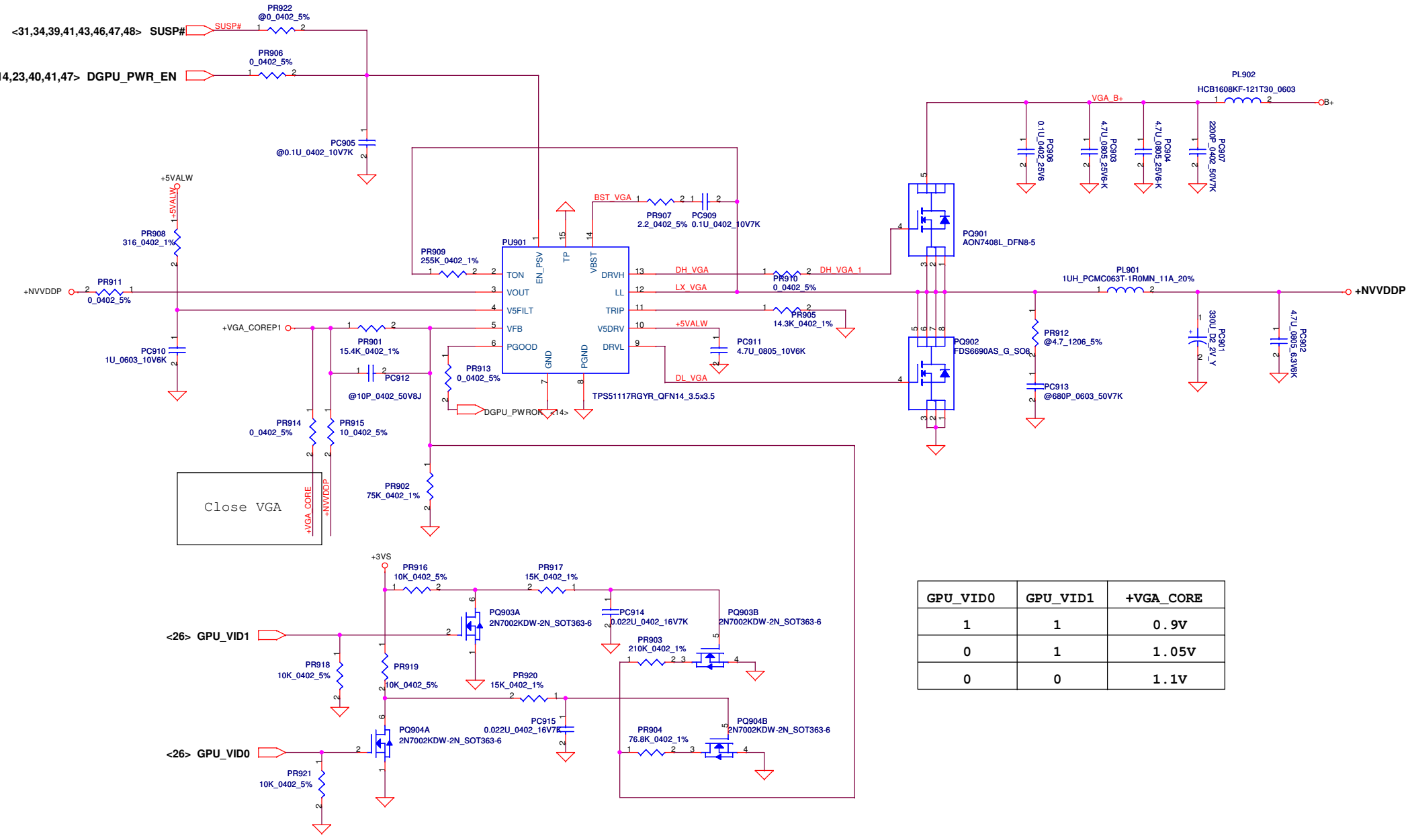
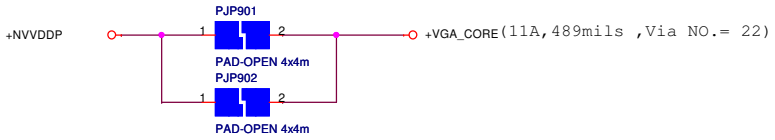
Compal Electronics, Inc.		
Title: VCCGFX		
Size: Custom	Document Number: Calpella DIS LA-4107P	Rev:
Date: Monday, November 09, 2009	Sheet 50 of 55	



GPU_VID0	GPU_VID1	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

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Compal Electronics, Inc.

Title: VGA_CORE

Size | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 51 of 55

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	PLT_RST# need a PD resistor	14	Add R185 PD for PLT_RST#	08/6	PV
2	Remove MUX in CRT DDC circuit of SG design	20	Change to MOS design	08/6	PV
3	Remove MUX in LVDS ENAVDD circuit of SG design	21	Change to MOS design	08/6	PV
4	LCD panel will fail in OPP SKU	21	Add one 0 ohm resistor (R1238) for OPP SKU	08/6	PV
5	Remove MUX in LVDS I2C circuit of SG design	22	Change to MOS design	08/6	PV
6	OPP SKU: M93 and VRAM may have leakage in S3 mode	41	Change the power plan to +1.5VS of JP303	08/6	PV
7	8111VB power on timing issue	32	Add R1083 and C1319 to fine tune the power on timing	08/10	PV
8	Blade 2.0 need Board ID	39	Use EC GPIO48 for ID pin(Add R1239, R1240)	08/12	PV
9	EC GPIO17 will be used for debug card	39	LAN_POWER_OFF signal change to EC GPXID4(Pin 115)	08/12	PV
10	Cap. sensor board need to change the power source.	40	Change the power source of Cap. sensor baord to +3VS	08/13	PV
11	Lid switch need to change the power source.	40	Change the power source of Lid switch to +3VALW and R526 PU to +3VALW.	08/13	PV
12	Change +1.8VS to +1.8VSDGPU Transfer design for cost down	41	Change the power MOS(U49) to 2301 PMOS(Q109).	08/13	PV
13	BIOS team doesn't need XDP connector	6	Remove the XDP connector	08/13	PV
14	Change +5VS to +5VSDGPU Transfer design for cost down	41	Use 0 ohm to contact +5VS and +5VSDGPU	08/13	PV
15	PCH_DDR_RST need use PCH GPIO46 to control	6	PCH_DDR_RST MOS gate control signal change from EC to PCH GPIO46	08/13	PV
16	Remove the 27MHz crystal of VGA	26	Use clock gen 27MHz source and stuff R216	08/14	PV
17	Q104 need change to low Vgs type	6	Change the Q104 to BSS138 P/N:SB501380020	08/18	PV
18	Cost down plan	9	Change the C995,C996 330u to ESR=9m ohm	08/14	PV
19	Cost down plan	9	Change the C64 from 330u to 220u	08/14	PV
20	Cost down plan	9	Change the C61,C62,C67,C68,C69,C76,C82 from 22u to 10u	08/14	PV
21	Cost down plan	9	Change the C200 330u to ESR=9m ohm	08/14	PV
22	Cost down plan	9	Un-stuff C204,C228 and C229	08/14	PV
23	Docking no sound when play music	34	Need to stuff R910	08/14	PV
24	Audio new Mapping	34	Exchange the port A and port F	08/14	PV
25	We won't have DIM_LED function	41	Un-stuff Q99,Q101 and add two 0 ohm(R1244,R1245) resistors for LED power source.	08/14	PV
26	ESD issue	34	Add R1247,C1442,C1443 and change the C983~C986, C1444~C1446 to 0.1u	08/18	PV
27	Black light issue(will see the garbage when boot)	22	Change the black light enable schematic design.	08/18	PV
28	CPU leakage issue	6	Change the design for Intel's power leakage issue when go into S3 mode	08/19	PV

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: PIR-HW

Size | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 52 of 55

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	INT.MIC ESD issue	35	Add D58 and D62 for ESD issue	08/18	PV
30	EXT.MIC ESD issue	35	Reserve D63 for Ext. MIC	08/18	PV
31	Reserve PU resistors to +3VL for ESB BUS	39	Reserve R1253,R1254 for ESB bus	08/21	PV
32	Make sure power sequence is correct	6,47	Use 1.5VSCPU_DRAM_PWRGD to enable 0.75VS power	09/11	PV2
33	Add ME_EN# for PCH GPIO33	11	Add inverter circuit for ME_EN signal	09/11	PV2
34	+3VS_VGA will have leakage when switch to IGPU mode	12	Change Q4 pin2 and pin5 to +3VS_VGA	09/11	PV2
35	Need contact SUS_PWR_DN_ACK between EC and PCH	13	Use PCH GPIO30 and EC pin76 for SUS_PWR_DN_ACK	09/11	PV2
36	Need add VGA ID pin for M93 and M93 LP	14	Use PCH GPIO57 for VGA ID pin	09/11	PV2
37	Change 27MHz clock source of VGA to Y7	19,26	non-stuff R216	09/11	PV2
38	Q37 dual package will have floating isse	22	Change Q37 to single package	09/11	PV2
39	Fix 8103 BOM isse	32	Add R1259 for 8103EL LAN chip	09/11	PV2
40	Fix EXT. MIC reference voltage issue	34	Change the reference voltage to +AVDD_CODEC	09/11	PV2
41	Remove EC_BEEP function	34	Delete EC_BEEP function	09/11	PV2
42	Remove Analog MIC detect function	35,39	Delete ANA_MIC_DET signal from EC and codec	09/11	PV2
43	EMI need to add chock for ESATA/USB port	37	Add L66 for ESATA/USB port	09/11	PV2
44	HM55 PCH will disable USB port6 and port7	37	Change Finger printer from USB port7 to USB port 11	09/11	PV2
45	HM55 PCH will disable USB port6 and port7	37	Change Bluetooth from USB port 6 to USB port 12	09/11	PV2
45	Remove EC_BEEP function	39	Change Pin 26 from EC_BEEP to ME_EN	09/11	PV2
46	Fix PV phase Board ID issue	39	Exchange TP_BTN# and Board_ID pin	09/11	PV2
47	Cypress Cap. sensor board need use +3VL power	40	Change Cap. sensor board power to +3VL	09/11	PV2
48	Adjust +3VS / +1.5VS power sequence	41	Change C676,C770 from 0.1u to 0.022u	09/12	PV2
49	PLT_RST# don't need PD resistor	14	Un-stuff R185	09/20	MV
50	Follow Intel to adjust +0.75VS discharge timing	41	Change R593 from 470ohm to 22ohm	09/20	MV
51	Follow Intel to adjust +1.5VS discharge timing	41	Change R590 from 470ohm to 220ohm	09/20	MV
52	Follow Intel Check list 2.0	15	Un-stuff C187 and C192	09/20	MV
53	EDID signal need to add PU resistor	22	Add R1261 for EDID DATA	09/20	MV
54	VCCADAC dosen't need LC filter when DIS only	15	Change L45 to 0 ohm resistor for OPP SKU	10/01	MV
55	GFX core power transient fail	9	Change C996 to 330u 7m ohm	10/21	MV

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Compal Electronics, Inc.

Title: PIR-HW

Size | Document Number: Calpella DIS LA-4107P | Rev: 1.0

Date: Monday, November 09, 2009 | Sheet 53 of 55

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
56	Add M93 / M93LP / Park / Park LP ID pin	14	Use PCH GPIO28 and GPIO57 for VGA ID pin	10/21	MV
57	RTC timing fast / slow issue	19	Change C259, C260 to 22P	10/21	MV
58	ESB CLK can't pass EMI test.	40	Change R1151 to 300 ohm bead and add C1449	10/21	MV
59	Intel PCH CLK jitter issue	12	Reserve Y2 for this issue.	10/23	MV
60	ATE test jig issue(M/B will shutdown when no CPU)	39	Add R1265 for ATE jig test	10/23	MV
61	ATE test jig issue (need to turn on +VGA_CORE when no CPU)	41	Add R1266 and reserve Q115 for ATE jig test	10/29	MV
62	Ext. MIC record noise issue	34	Reserve LDO circuit for this issue.	11/03	MV
63	Intel CPU GFX overshoot issue	09	Follow Intel suggestion to change the R43 to 249 ohm	11/05	MV
64	+1.8VSDGPU power up/down timing issue	41	Change R916 to 1K and R926 to 10K then add C1454 to fine tune timing	11/05	MV
65	+1.5VSDGPU / +1.5VS power quality issue	41	Change U50 and U58 to low RDSON NMOS	11/05	MV

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Compal Electronics, Inc.		
Title: PIR-HW		
Size	Document Number: Calpella DIS LA-4107P	Rev: 1.0
Date: Monday, November 09, 2009	Sheet 54 of 55	

Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Note
1	44	PWR-3.3VALWP/5VALWP	8/12	PWR	all cap no more than 0805	Add PC318,PC305 from 1206 to 0805 and parallel with PC318	DB to PV1
2	49	PWR-CPU_CORE	8/13	PWR	OCP & IMON ajustment and Fixed LL to match INTEL Spec	Change PR253 from 1.1K to 1.3K,Change PR242 from 8.25K to 10.5K Change PR237 from 2.43K to 3.01K	DB to PV1
3	49	PWR-CPU_CORE	8/17	PWR	RF Solution	Change PQ201 PQ202 from AO4474L to AO4406AL,PR215 PR244 from 0 to 2.2	DB to PV1
4	47	PWR-0.75VP/1.8VSP	8/20	PWR	Cost Down plan	Change PU602 from APL5915 to APL5930	DB to PV1
5	43	PWR-Charger	8/20	PWR	Smart Charger	Change PR113 from 143K to 140K, Change PC117 from 1u to 0.1u, Add PR114	DB to PV1
6	49	PWR-CPU_CORE	8/20	PWR	Avoide DFX interfere	Delete PC209 and add PC210	DB to PV1
7	46	PWR-1.05V_VCCP	8/24	PWR	Follow HW Suggestion Pull-up resistor connect to 3VS	Add PR705 connect to 3VS, remove PR706	DB to PV1
8	45	PWR-1.5VP	8/24	PWR	PU401 second source solution	PR403 from 13.7K to 15.4K	DB to PV1
9	46	PWR-1.05V_VCCP	8/24	PWR	PU701 second source solution	PR703 from 8.06K to 6.98K	DB to PV1
10	49	PWR-CPU-CORE	8/28	PWR	Improve transient response	Add PC230	DB to PV1
11	46	PWR-1.05V_VCCP	9/2	PWR	Cost down plan	Change PC701 PC702 PC703 from 330u 6m ohm to 330u 9m ohm	DB to PV1
12	46	PWR-1.05V_VCCP	9/3	PWR	Improve VCCP Ripple	Del PC717	DB to PV1
13	50	GFX_CORE	9/11	PWR	Let GFX IMON measure easily	Add PR833 connect to GFRXVR_IMON and PU801 pin 13	PV1 to PV2
14	47	PWR-0.75VP/1.8VSP	9/11	PWR	For HW requirement add 1.5VSCPU_DRAM_PWRGD	Add 1.5VSCPU_DRAM_PWRGD add PR613 connect to PQ601 pin 2 and Delet PR604	PV1 to PV2

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