Compal confidential

JBK00 LA-4093P Schematics Document

Mobile AMD S1G2 CPU with ATI RX781 & SB700 core logic with M86-M

2009-03-25

REV:1.0

機密	等級	硬體二部
		產出人員
		產出日期
		解密日期

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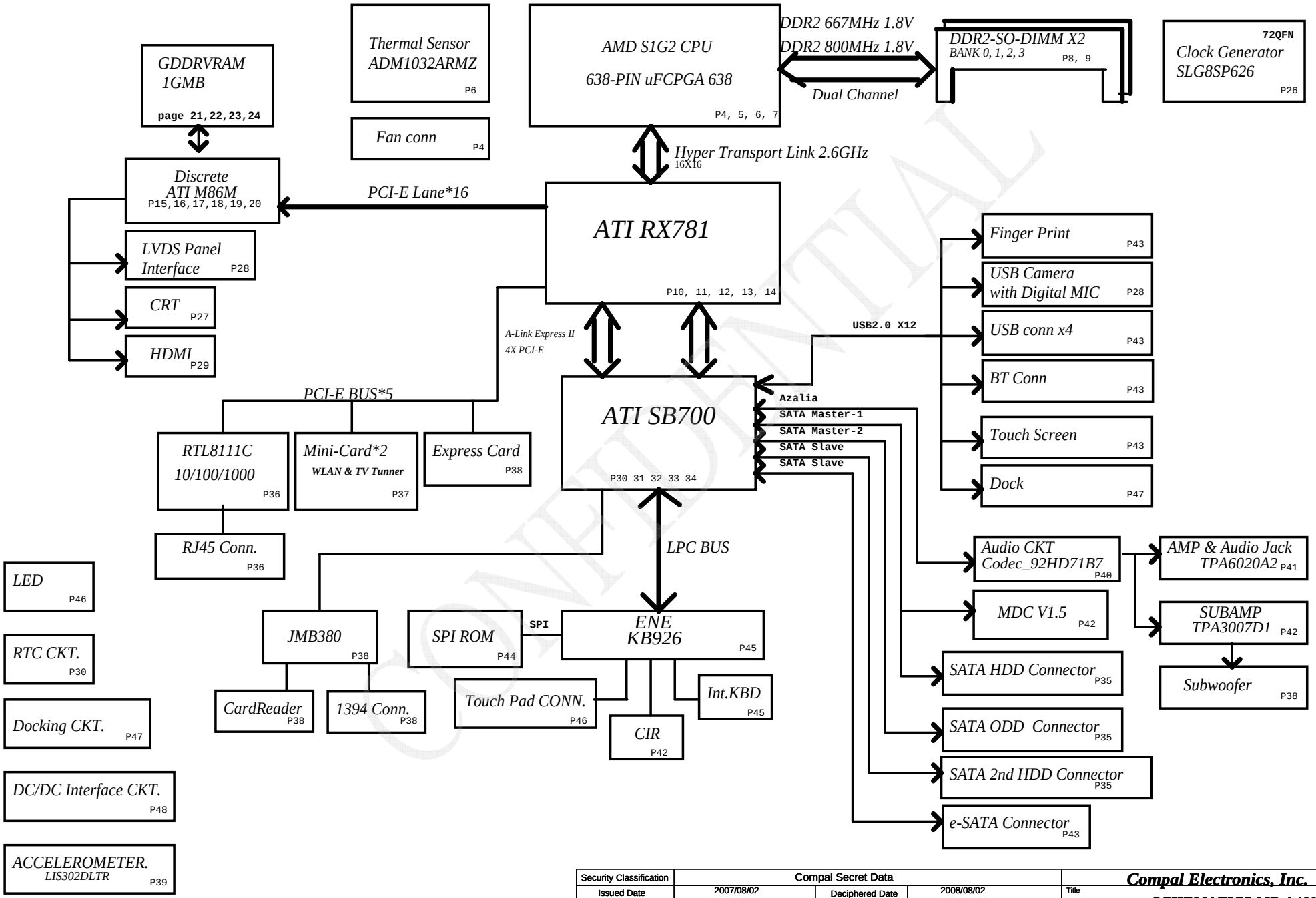
Consumer AMD Discrete 17"



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Voltage Rails

power plane / State	+B +3VL +5VL	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON X MEANS OFF

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

Layout Notes

@ : means just reserve , no build
45@ : means need be mounted when 45 level assy or rework stage.
RX781R1@ : means just reserve for R1 FRU BOM
SBR1 @ : means just reserve for R1 FRU BOM
M86R1@ : means just reserve for R1 FRU BOM

M86M — U5 — M86M R1 / M86R3@

RX781 — U3 — RX781 R1 / RX781R3@

SB700 — U15 — SB700 R1 / SBR3@

PCB — ZZZ — PCB LA-4093P REV1.0 M/B

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
24C16	A0H	1010 000X b
CPU SIC interface	98H	1001 100X b

EC SM Bus2 address

Device	HEX	Address
ADI1032-2 CPU	9AH	1001 101X b
ADI1032-1 VGA	98H	1001 100X b

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	V
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

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10 H_CADIP[0..15] H_CADIP[0..15]
10 H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] 10
H_CADON[0..15] H_CADON[0..15] 10

+1.2V_HT

VLDT=500mA

JP1A

HT LINK

	D1	VLDT_A0	VLDT_B0	AE2	+VLDT_B
	D2	VLDT_A1	VLDT_B1	AE3	
	D3	VLDT_A2	VLDT_B2	AE4	
	D4	VLDT_A3	VLDT_B3	AE5	
H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	E3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15
10 H_CLKIP0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	H_CLKOP0 10
10 H_CLKIN0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	H_CLKON0 10
10 H_CLKIP1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	H_CLKOP1 10
10 H_CLKIN1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	H_CLKON1 10
10 H_CTLIP0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	H_CTLOP0 10
10 H_CTLIN0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	H_CTLON0 10
10 H_CTLIP1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	H_CTLOP1 10
10 H_CTLIN1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	H_CTLON1 10

C7 4.7U_0805_10V4Z

6090022100G_B

CONN@

VLDT CAP.

+1.2V_HT

250 mil

C1 4.7U_0805_10V4Z
C2 4.7U_0805_10V4Z
C3 0.22U_0603_16V4Z
C4 0.22U_0603_16V4Z
C5 180P_0402_50V8J
C6 180P_0402_50V8J

Near CPU Socket

PWM Fan Control circuit

+5VS

D1 CH751H-40PT_SOD323-2

C8 4.7U_0805_10V4Z

C9 @0.1U_0402_16V4Z

JP2 ACES_88231-02001 CONN@

GND GND

+VCC_FAN

Q1 SI3456BDV-T1-E3_TSOP6

@D2 RLZ5.1B_LL34

45 FAN_PWM

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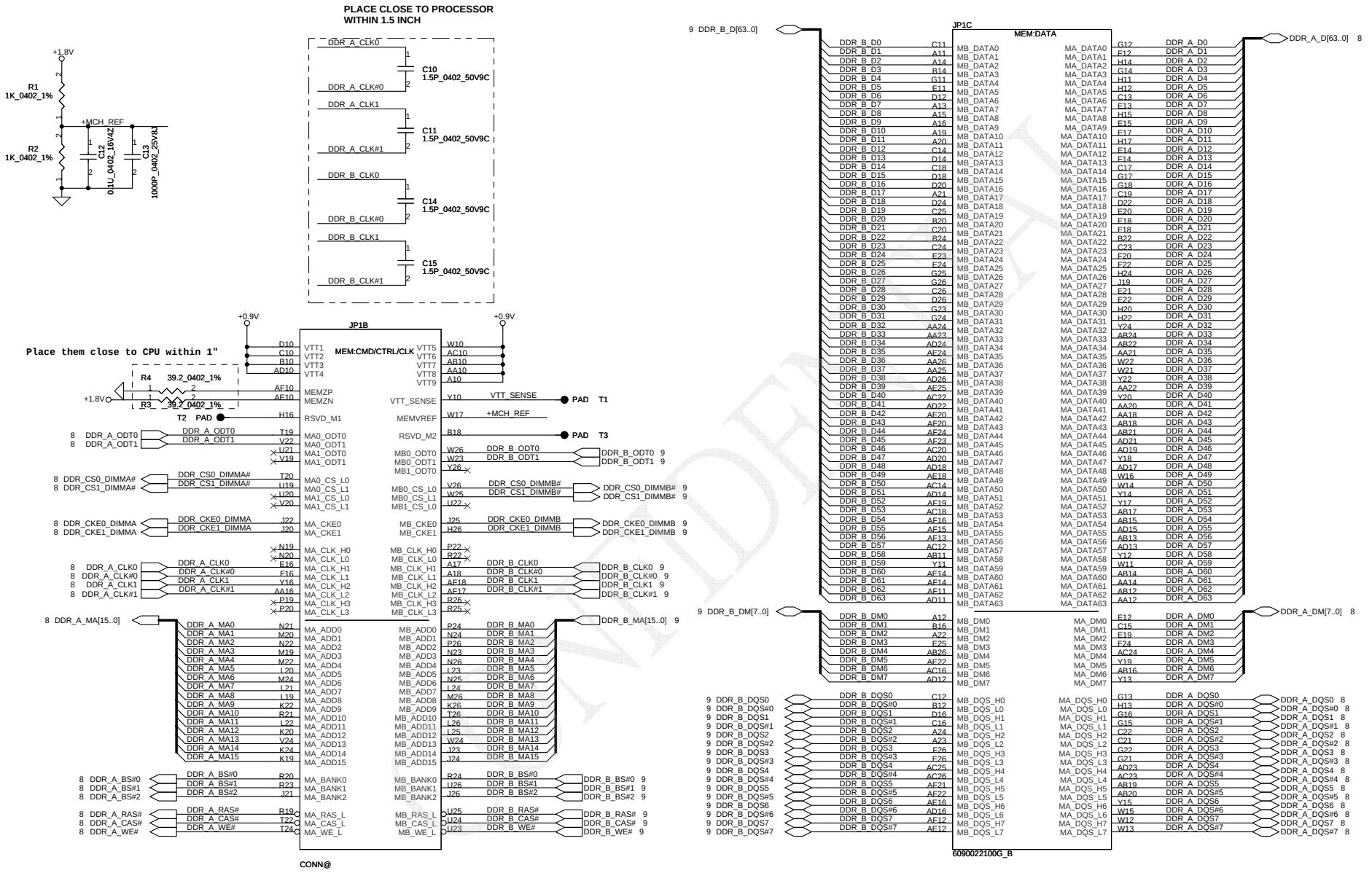
Processor DDR2 Memory Interface



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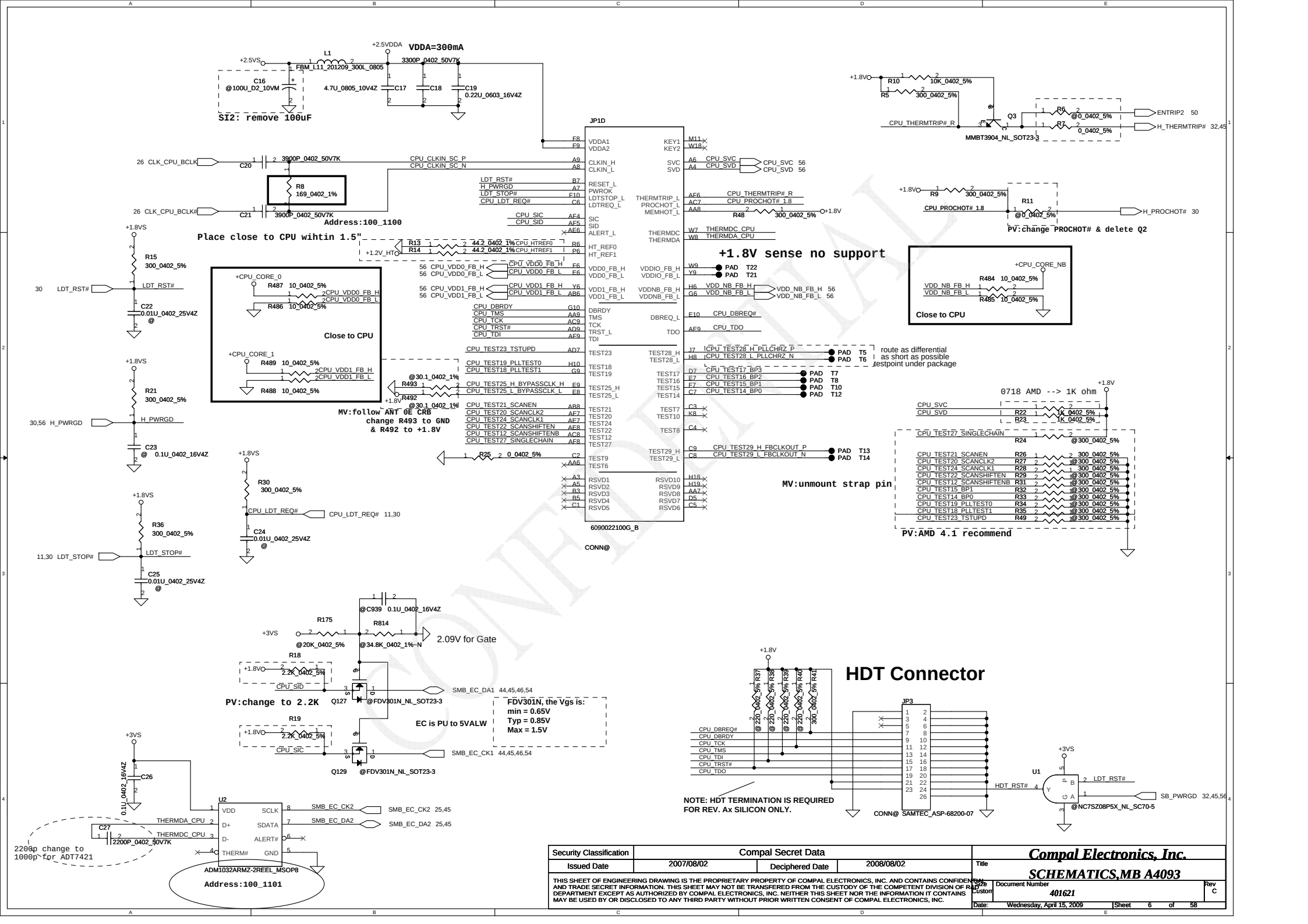

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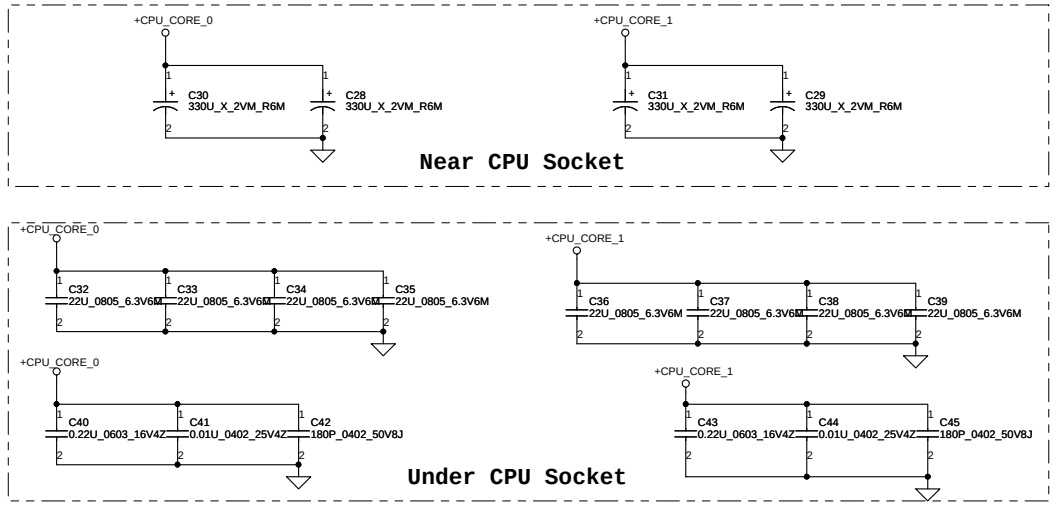
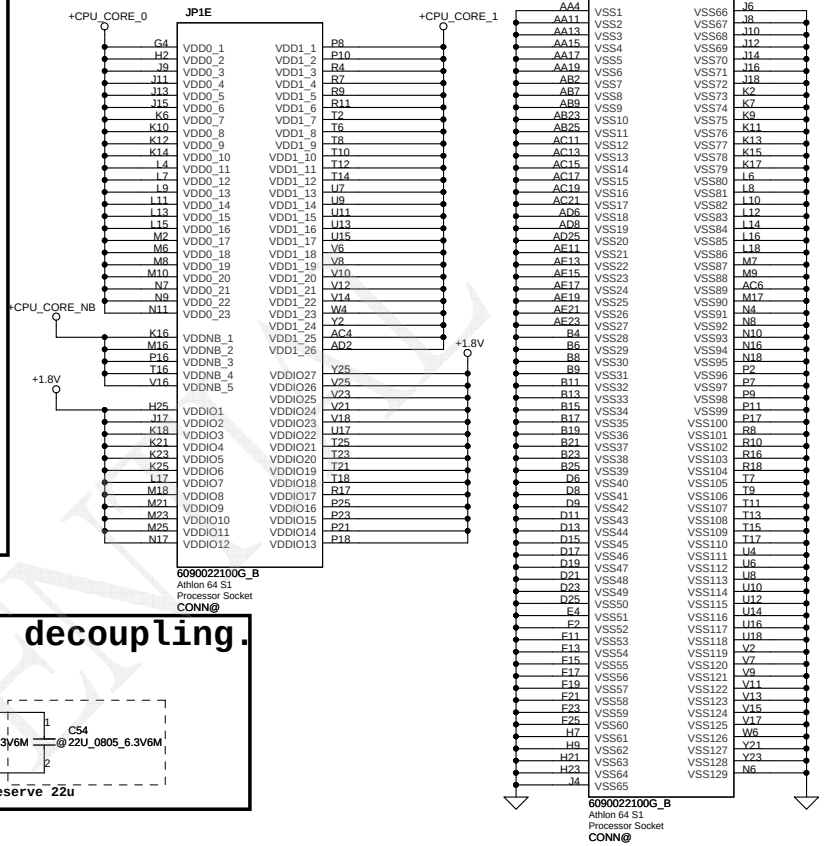
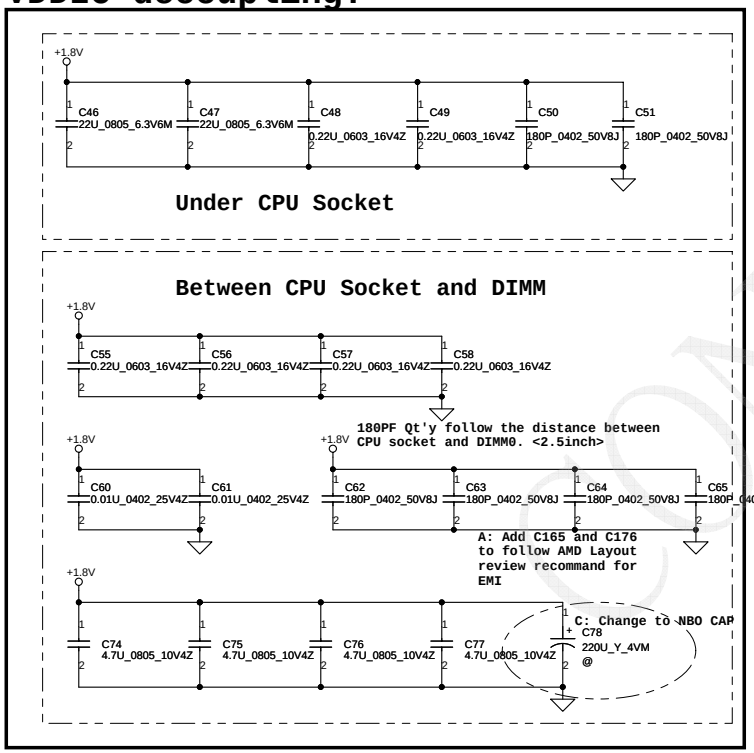
VDD(+CPU_CORE) decoupling.

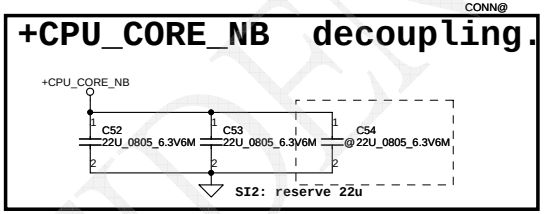




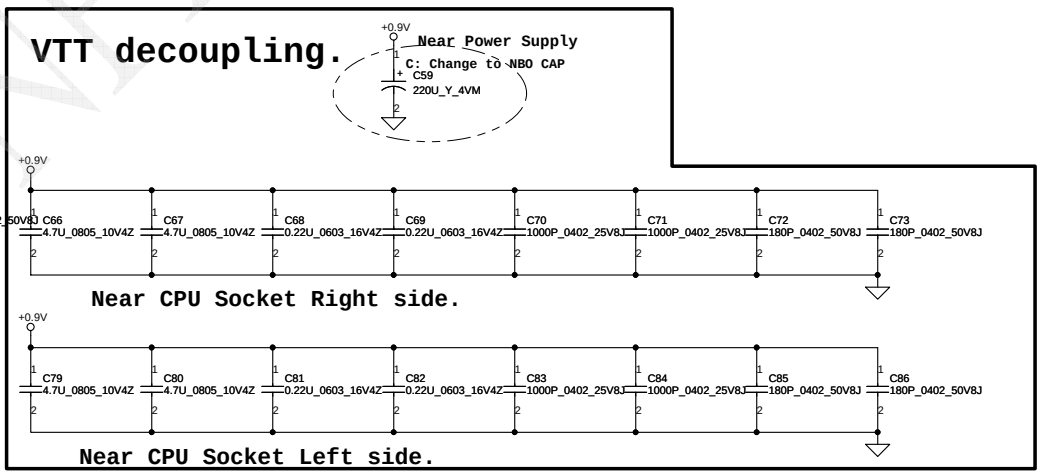
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



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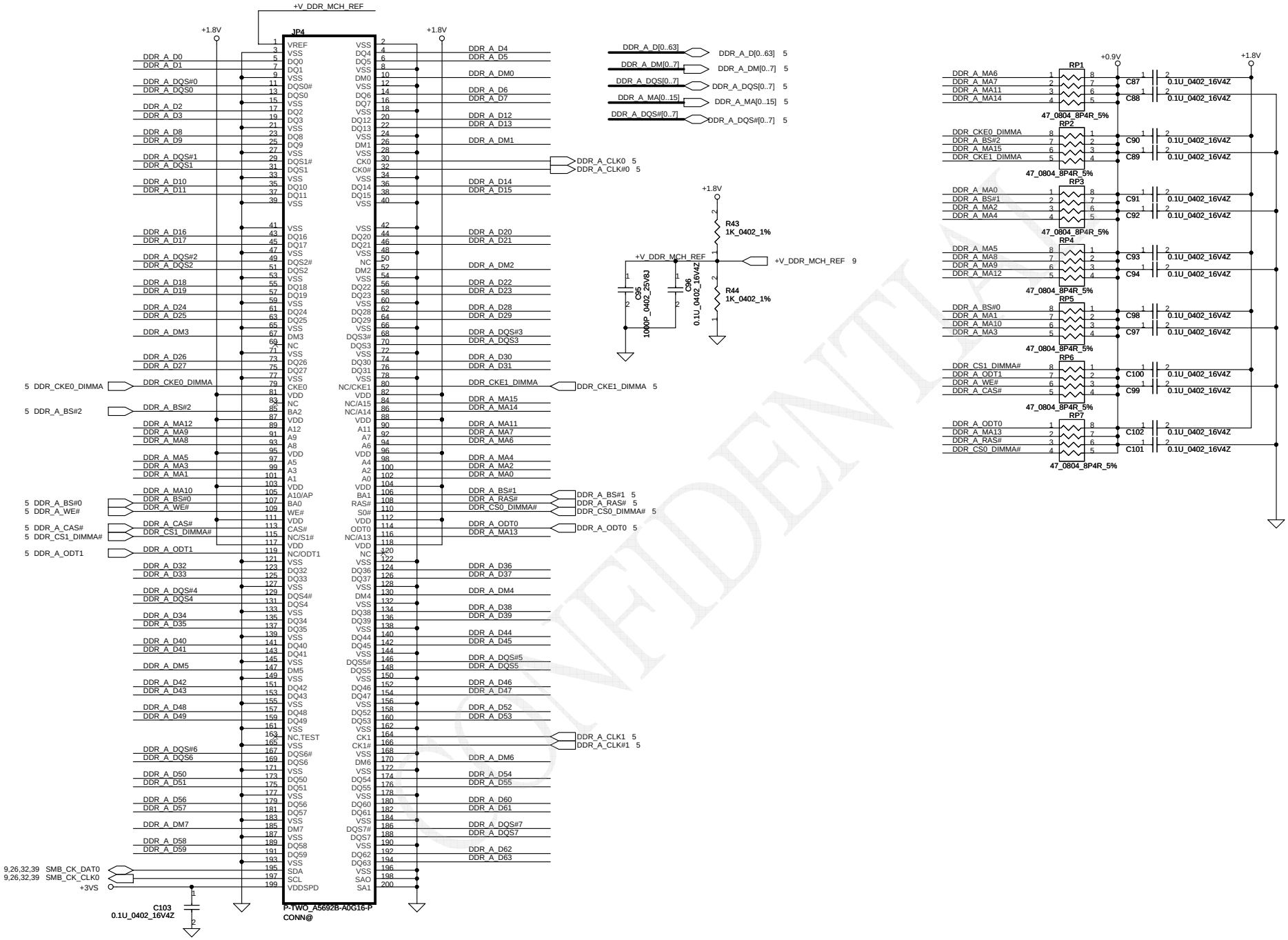

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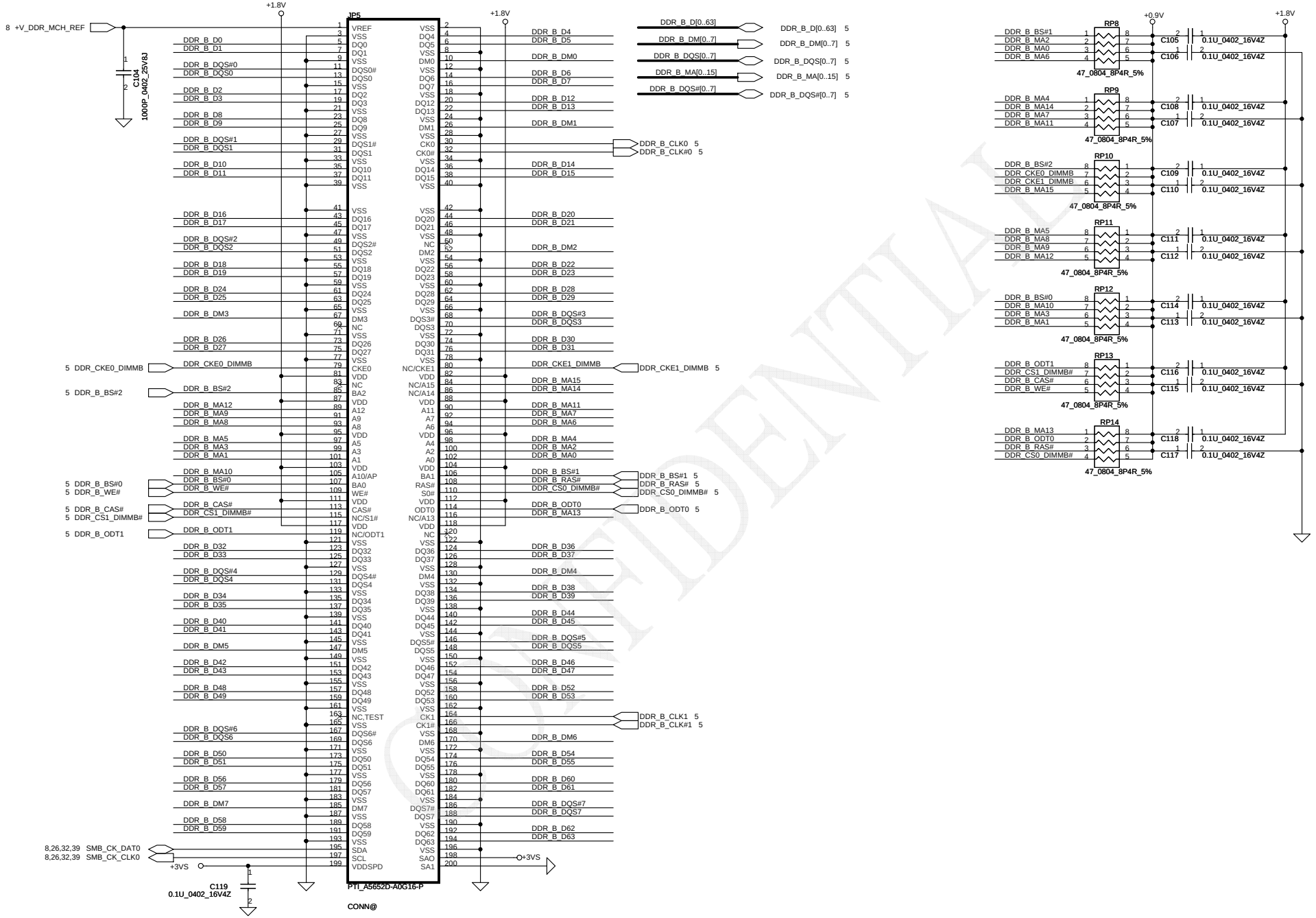

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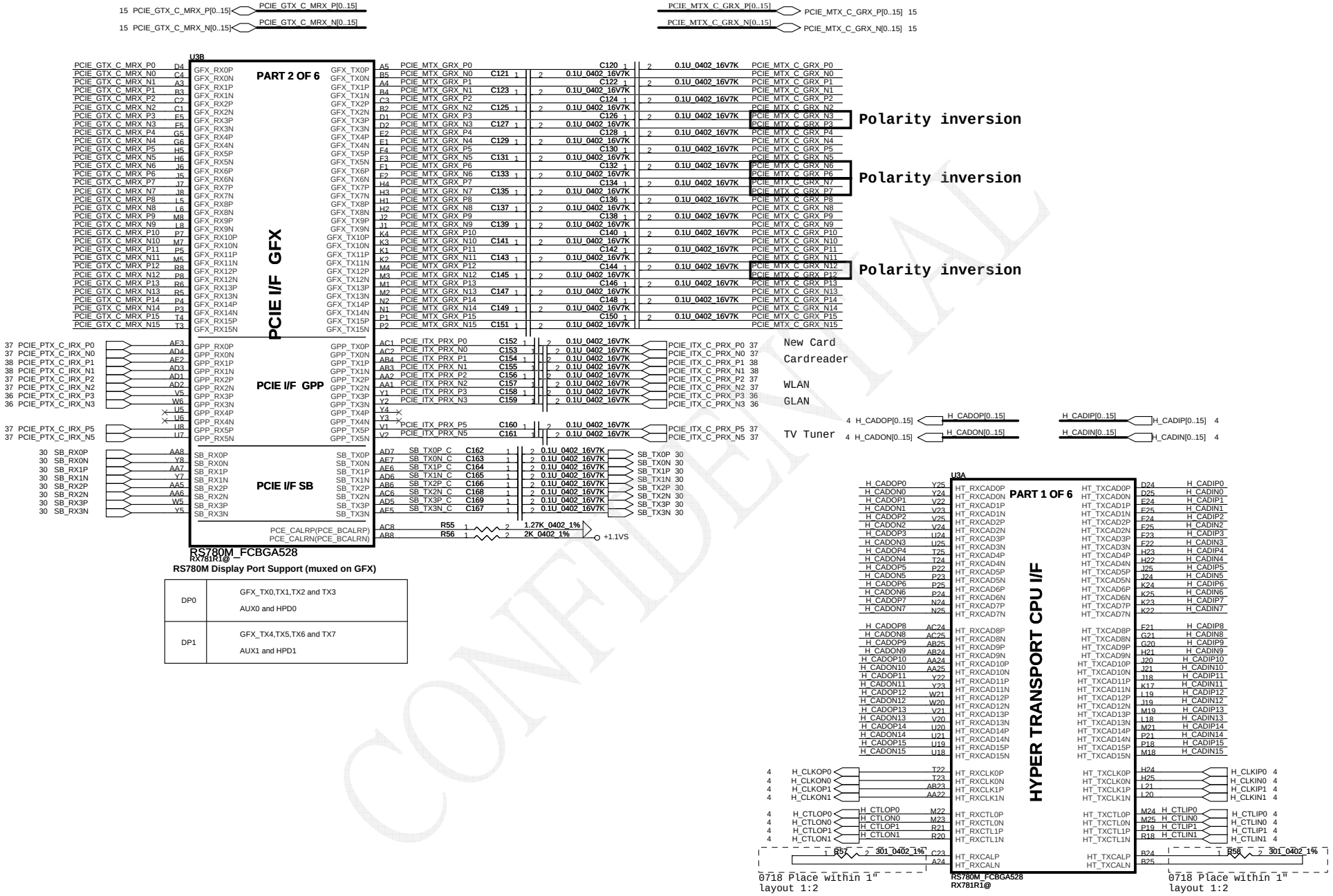

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NEED CHECK R68 & R69 WITH AMD

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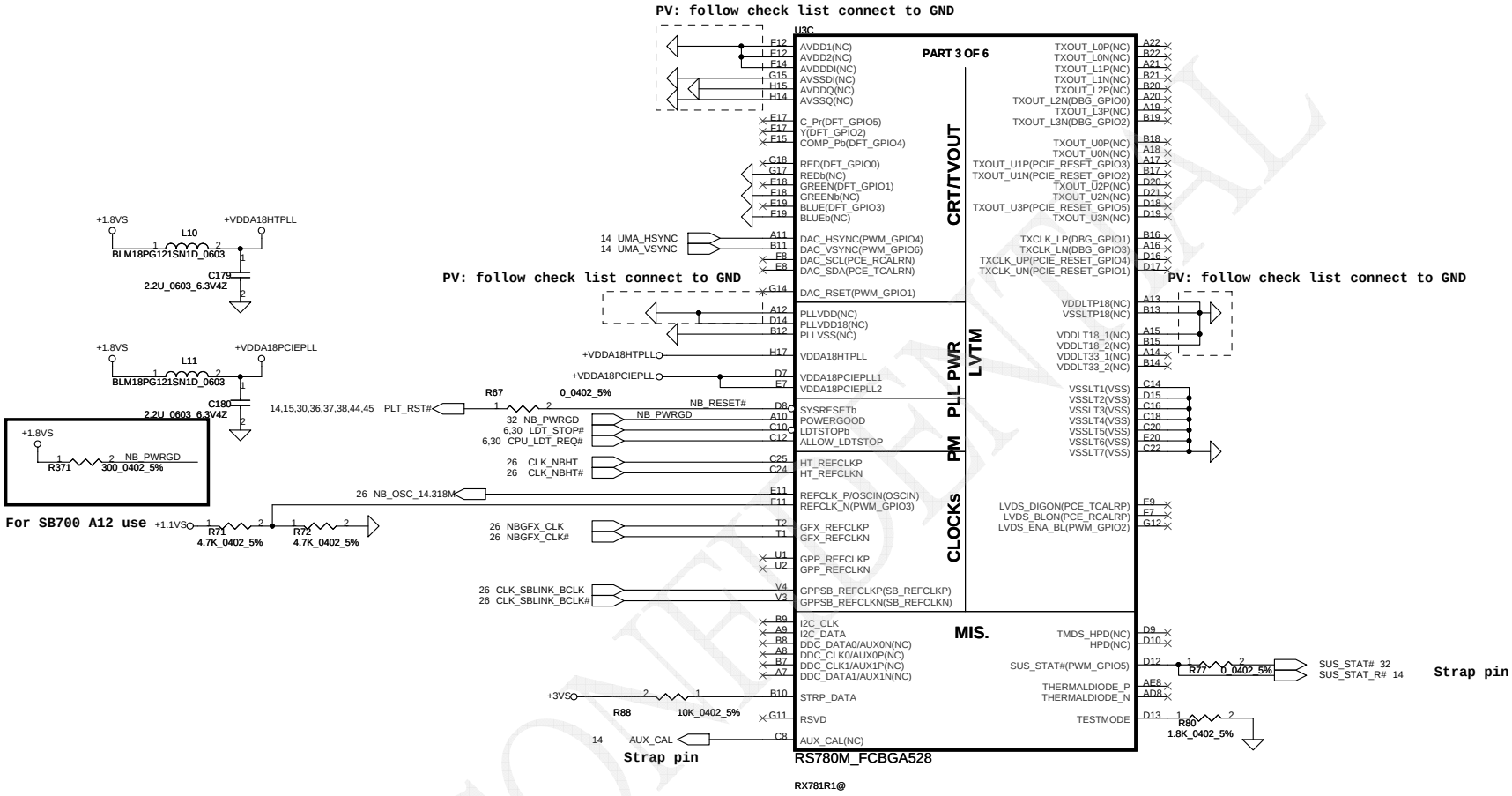

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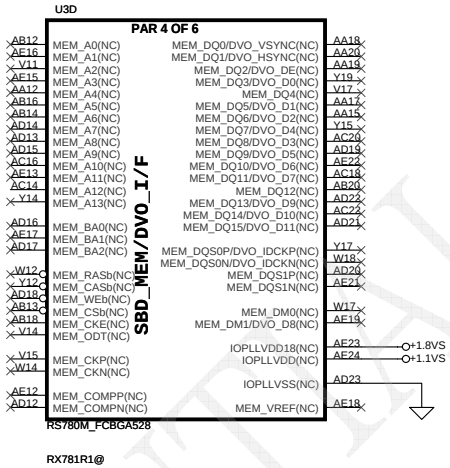

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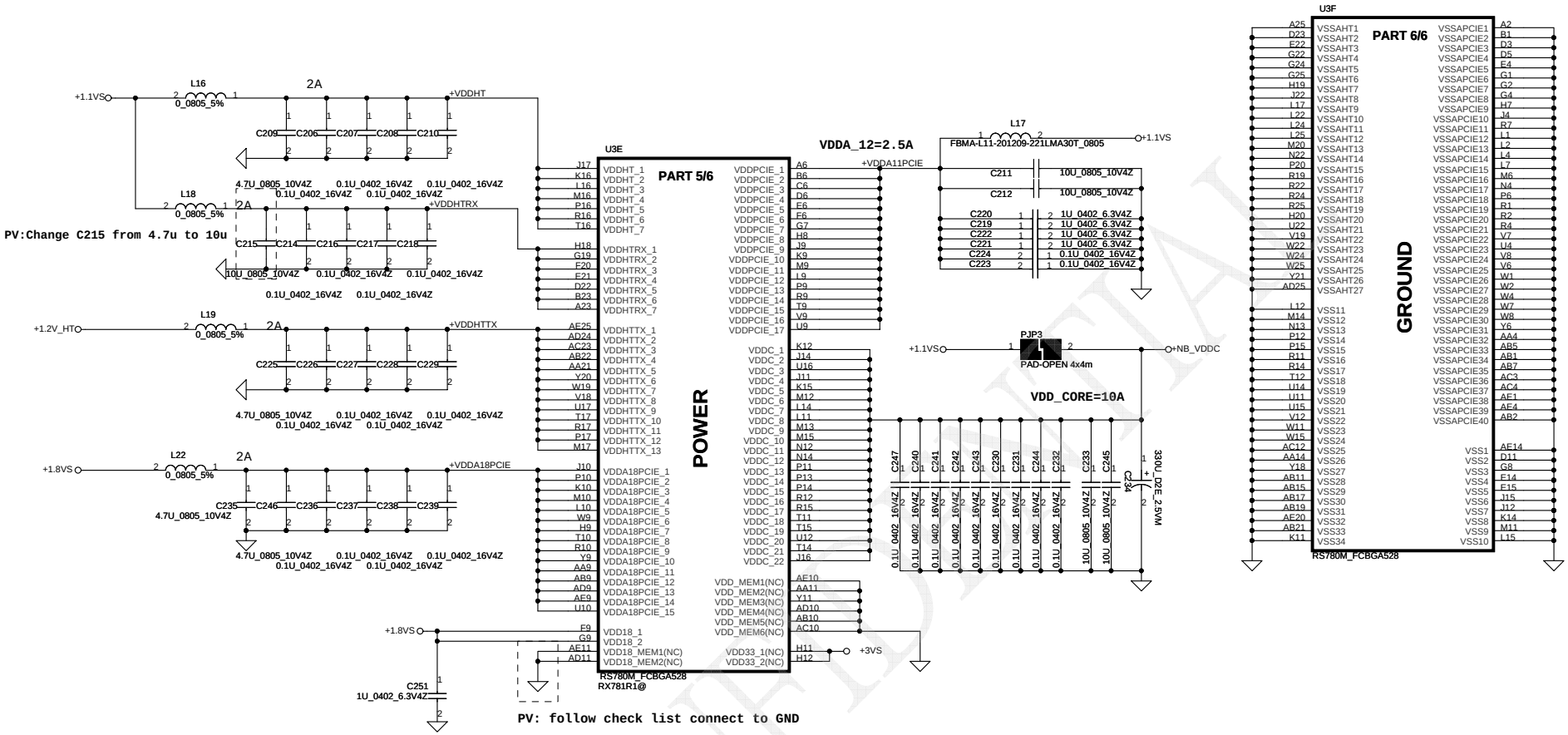

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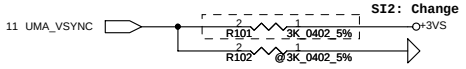
RS780 DFT_GPIO5 mux at CRT_VSYNC pull high to 3K

SI2: Change to 3K pull high



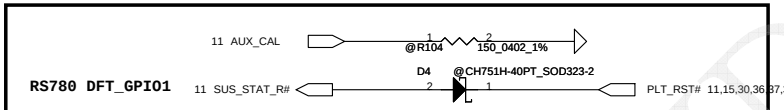
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#
```

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```

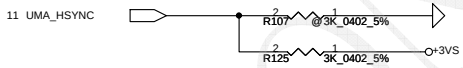


RX780 DFT_GPIO1 mux at GREEN(Ball E18) and change pull low form 150 to 3K.

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```

RS780 use HSYNC to enable SIDE PORT (internal pull high)



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS780)
0 : Enable (RS780)
```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10 PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]

10 PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

10 PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]

10 PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]

Close to connector

U5A

PART 1 OF 7

PCIE_MTX_C_GRX_P15	AK33	PCIE_RX0P		PCIE_TX0P	AG31	PCIE_GTX_MRX_P15	CV9	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P15
PCIE_MTX_C_GRX_N15	AJ33	PCIE_RX0N		PCIE_TX0N	AG30	PCIE_GTX_MRX_N15	CV10	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N15
PCIE_MTX_C_GRX_P14	AJ35	PCIE_RX1P		PCIE_TX1P	AF31	PCIE_GTX_MRX_P14	CV11	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P14
PCIE_MTX_C_GRX_N14	AJ34	PCIE_RX1N		PCIE_TX1N	AF30	PCIE_GTX_MRX_N14	CV12	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N14
PCIE_MTX_C_GRX_P13	AH35	PCIE_RX2P		PCIE_TX2P	AF28	PCIE_GTX_MRX_P13	CV13	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P13
PCIE_MTX_C_GRX_N13	AH34	PCIE_RX2N		PCIE_TX2N	AF27	PCIE_GTX_MRX_N13	CV14	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N13
PCIE_MTX_C_GRX_P12	AG35	PCIE_RX3P		PCIE_TX3P	AD31	PCIE_GTX_MRX_P12	CV15	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P12
PCIE_MTX_C_GRX_N12	AG34	PCIE_RX3N		PCIE_TX3N	AD30	PCIE_GTX_MRX_N12	CV16	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N12
PCIE_MTX_C_GRX_P11	AE33	PCIE_RX4P		PCIE_TX4P	AD28	PCIE_GTX_MRX_P11	CV17	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P11
PCIE_MTX_C_GRX_N11	AE33	PCIE_RX4N		PCIE_TX4N	AD27	PCIE_GTX_MRX_N11	CV18	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N11
PCIE_MTX_C_GRX_P10	AE35	PCIE_RX5P		PCIE_TX5P	AB31	PCIE_GTX_MRX_P10	CV19	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P10
PCIE_MTX_C_GRX_N10	AE34	PCIE_RX5N		PCIE_TX5N	AB30	PCIE_GTX_MRX_N10	CV20	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N10
PCIE_MTX_C_GRX_P9	AD35	PCIE_RX6P		PCIE_TX6P	AB28	PCIE_GTX_MRX_P9	CV21	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P9
PCIE_MTX_C_GRX_N9	AD34	PCIE_RX6N		PCIE_TX6N	AB27	PCIE_GTX_MRX_N9	CV22	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N9
PCIE_MTX_C_GRX_P8	AC35	PCIE_RX7P		PCIE_TX7P	AA31	PCIE_GTX_MRX_P8	CV23	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P8
PCIE_MTX_C_GRX_N8	AC34	PCIE_RX7N		PCIE_TX7N	AA30	PCIE_GTX_MRX_N8	CV24	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N8
PCIE_MTX_C_GRX_P7	AB33	PCIE_RX8P		PCIE_TX8P	AA28	PCIE_GTX_MRX_P7	CV25	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P7
PCIE_MTX_C_GRX_N7	AA33	PCIE_RX8N		PCIE_TX8N	AA27	PCIE_GTX_MRX_N7	CV26	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N7
PCIE_MTX_C_GRX_P6	AA35	PCIE_RX9P		PCIE_TX9P	W31	PCIE_GTX_MRX_P6	CV27	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P6
PCIE_MTX_C_GRX_N6	AA34	PCIE_RX9N		PCIE_TX9N	W30	PCIE_GTX_MRX_N6	CV28	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N6
PCIE_MTX_C_GRX_P5	Y35	PCIE_RX10P		PCIE_TX10P	W28	PCIE_GTX_MRX_P5	CV29	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P5
PCIE_MTX_C_GRX_N5	Y34	PCIE_RX10N		PCIE_TX10N	W27	PCIE_GTX_MRX_N5	CV30	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N5
PCIE_MTX_C_GRX_P4	W35	PCIE_RX11P		PCIE_TX11P	V31	PCIE_GTX_MRX_P4	CV31	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P4
PCIE_MTX_C_GRX_N4	W34	PCIE_RX11N		PCIE_TX11N	V30	PCIE_GTX_MRX_N4	CV32	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N4
PCIE_MTX_C_GRX_P3	V33	PCIE_RX12P		PCIE_TX12P	V28	PCIE_GTX_MRX_P3	CV33	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P3
PCIE_MTX_C_GRX_N3	U33	PCIE_RX12N		PCIE_TX12N	V27	PCIE_GTX_MRX_N3	CV34	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N3
PCIE_MTX_C_GRX_P2	U35	PCIE_RX13P		PCIE_TX13P	U31	PCIE_GTX_MRX_P2	CV35	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P2
PCIE_MTX_C_GRX_N2	U34	PCIE_RX13N		PCIE_TX13N	U30	PCIE_GTX_MRX_N2	CV36	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N2
PCIE_MTX_C_GRX_P1	T35	PCIE_RX14P		PCIE_TX14P	U28	PCIE_GTX_MRX_P1	CV37	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P1
PCIE_MTX_C_GRX_N1	T34	PCIE_RX14N		PCIE_TX14N	U27	PCIE_GTX_MRX_N1	CV38	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N1
PCIE_MTX_C_GRX_P0	R35	PCIE_RX15P		PCIE_TX15P	R31	PCIE_GTX_MRX_P0	CV39	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_P0
PCIE_MTX_C_GRX_N0	R34	PCIE_RX15N		PCIE_TX15N	R30	PCIE_GTX_MRX_N0	CV40	1 2	0.1U_0402_10V7K PCIE_GTX_C_MRX_N0

P C I - E X P R E S S I N T E R F A C E

Clock

26 CLK_PCIE_VGA	AJ31	PCIE_REFCLKP	
26 CLK_PCIE_VGA#	AJ30	PCIE_REFCLKN	

SM Bus

	AK35	NC_SMB_DATA	
	AK34	NC_SMBCLK	
11,14,30,36,37,38,44,45 PLT_RST#	AM32	PERSTB	

Calibration

	AG26	PCIE_CALRN	RV5 2K_0402_1% 1 2 +PCIE_VDDC
	AJ27	PCIE_CALRP	RV6 1.27K_0402_1% 1 2
	AF3	NC_DRAM_0	
	AG9	NC_DRAM_1	
	AK29	NC_AC_BATT	
	AK14	NC_FAN_TACH	

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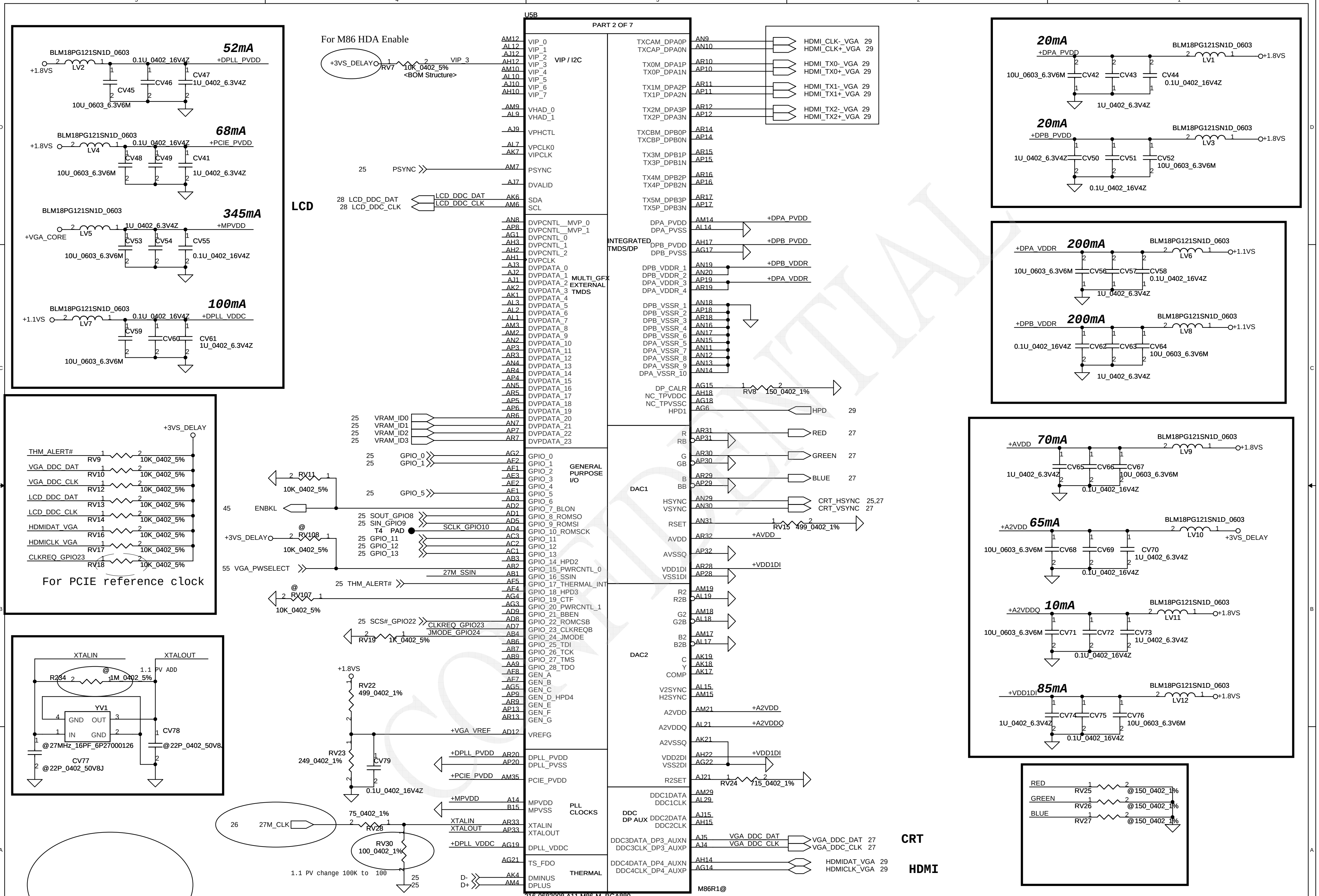

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Issued Date	2006/09/25	Deciphered Date	2006/09/25	Title: SCHEMATICS,MB A4093

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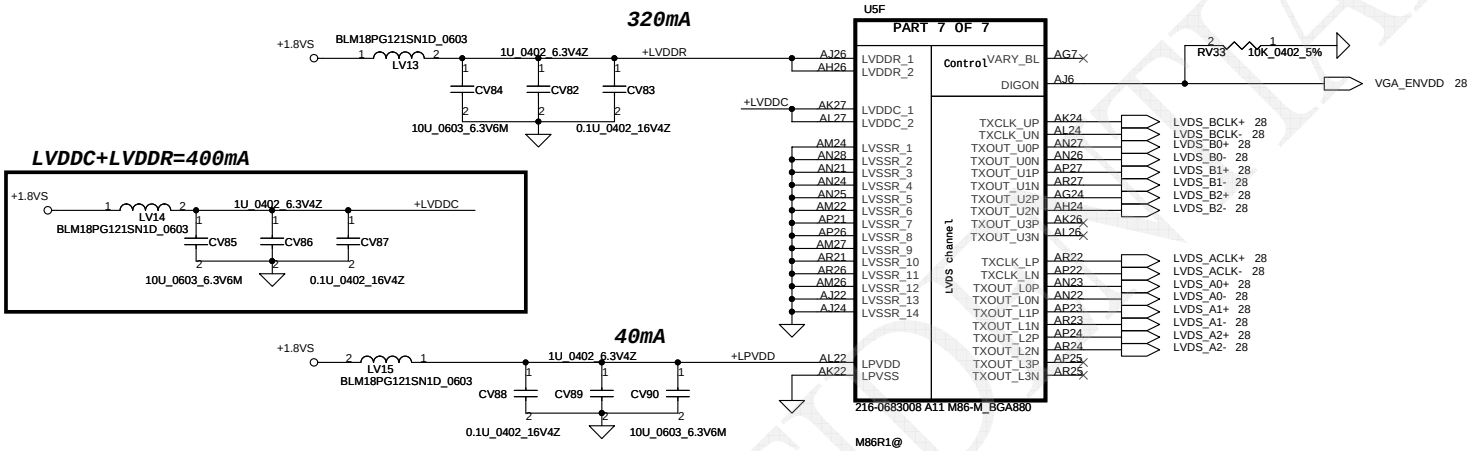

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	401621	C

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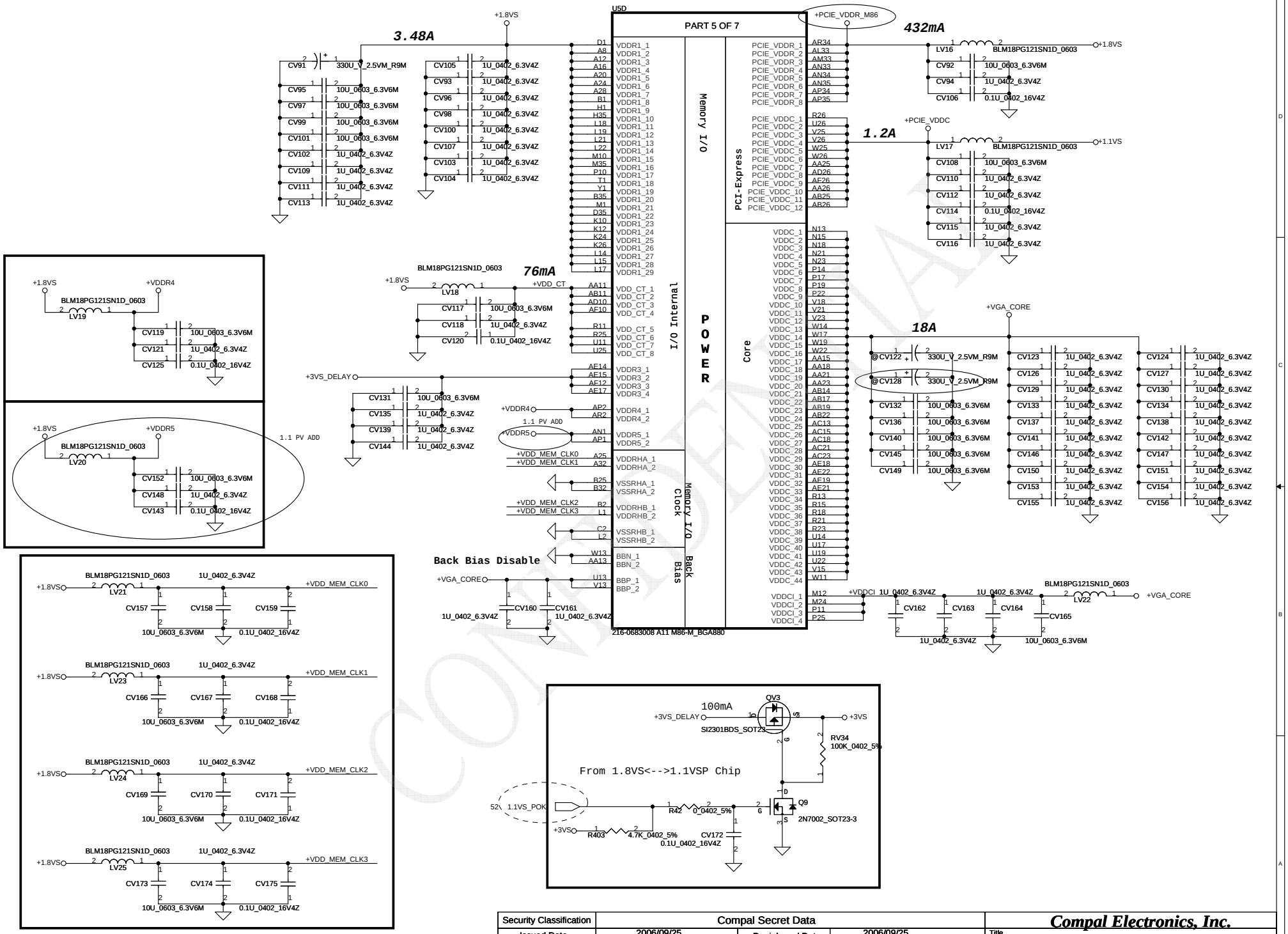

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Size	Document Number	Rev
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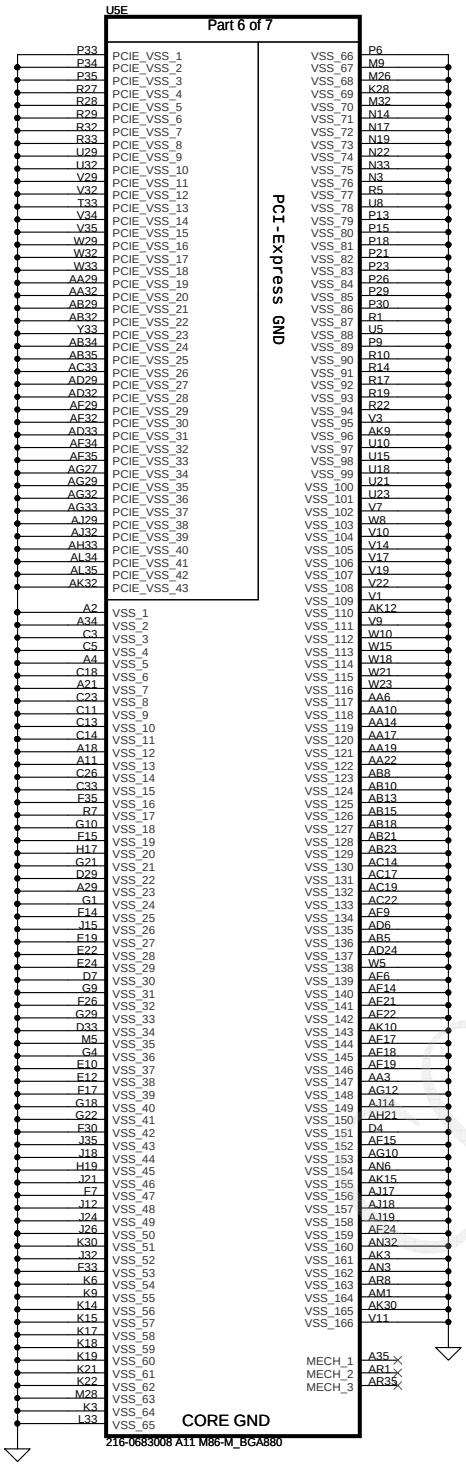

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DQMA#[7..0] — DQMA#[7..0] 21,22
QSA[7..0] — QSA[7..0] 21,22
QSA#[7..0] — QSA#[7..0] 21,22
MAA[12..0] — MAA[12..0] 21,22
BA[2..0] — BA[2..0] 21,22
MDA[63..0] — MDA[63..0] 21,22

MDB[63..0] — MDB[63..0] 23,24
MAB[12..0] — MAB[12..0] 23,24
BB[2..0] — BB[2..0] 23,24
DQMB#[7..0] — DQMB#[7..0] 23,24
QSB[7..0] — QSB[7..0] 23,24
QSB#[7..0] — QSB[7..0] 23,24

Close to pin N34, N35

+1.8VS
RV36 100_0402_1% — +MVREFDA — CV177 0.1U_0402_16V4Z
RV39 100_0402_1%
+1.8VS
RV37 100_0402_1% — +MVREFSA — CV176 0.1U_0402_16V4Z
RV38 100_0402_1%

Close to pin A13, B14

+1.8VS
RV40 100_0402_1% — +MVREFDB — CV178 0.1U_0402_16V4Z
RV42 100_0402_1%
+1.8VS
RV41 100_0402_1% — +MVREFSB — CV179 0.1U_0402_16V4Z
RV43 100_0402_1%

U5C

Part 3 of 7

MEMORY INTERFACE A

MDA0	P27	DQA_0	MAA_0	C27	MAA0
MDA1	P28	DQA_1	MAA_1	B28	MAA1
MDA2	P31	DQA_2	MAA_2	B27	MAA2
MDA3	P32	DQA_3	MAA_3	G26	MAA3
MDA4	M27	DQA_4	MAA_4	F27	MAA4
MDA5	K29	DQA_5	MAA_5	E27	MAA5
MDA6	K31	DQA_6	MAA_6	D27	MAA6
MDA7	K32	DQA_7	MAA_7	J27	MAA7
MDA8	M33	DQA_8	MAA_8	F29	MAA8
MDA9	M34	DQA_9	MAA_9	C30	MAA9
MDA10	L34	DQA_10	MAA_10	E26	MAA10
MDA11	L35	DQA_11	MAA_11	A27	MAA11
MDA12	J33	DQA_12	MAA_A12	G27	MAA12
MDA13	J34	DQA_13	MAA_BA2	D26	BA2
MDA14	H33	DQA_14	MAA_BA0	C28	BA0
MDA15	H34	DQA_15	MAA_BA1	B29	BA1
MDA16	K27	DQA_16			
MDA17	J29	DQA_17	DQMAb_0	M29	DQMA#0
MDA18	J30	DQA_18	DQMAb_1	K33	DQMA#1
MDA19	J31	DQA_19	DQMAb_2	G30	DQMA#2
MDA20	F29	DQA_20	DQMAb_3	E33	DQMA#3
MDA21	F32	DQA_21	DQMAb_4	C22	DQMA#4
MDA22	D30	DQA_22	DQMAb_5	H21	DQMA#5
MDA23	D32	DQA_23	DQMAb_6	C17	DQMA#6
MDA24	G33	DQA_24	DQMAb_7	G17	DQMA#7
MDA25	G34	DQA_25			
MDA26	G35	DQA_26	QSA_0	M30	QSA0
MDA27	F34	DQA_27	QSA_1	K34	QSA1
MDA28	D34	DQA_28	QSA_2	G31	QSA2
MDA29	C34	DQA_29	QSA_3	E34	QSA3
MDA30	C35	DQA_30	QSA_4	B22	QSA4
MDA31	B34	DQA_31	QSA_5	F21	QSA5
MDA32	C24	DQA_32	QSA_6	B17	QSA6
MDA33	B24	DQA_33	QSA_7	D17	QSA7
MDA34	B23	DQA_34			
MDA35	A23	DQA_35	QSA_0B	M31	QSA#0
MDA36	C21	DQA_36	QSA_1B	K35	QSA#1
MDA37	B21	DQA_37	QSA_2B	G32	QSA#2
MDA38	C20	DQA_38	QSA_3B	E35	QSA#3
MDA39	B20	DQA_39	QSA_4B	A22	QSA#4
MDA40	J22	DQA_40	QSA_5B	E21	QSA#5
MDA41	H22	DQA_41	QSA_6B	A17	QSA#6
MDA42	F22	DQA_42	QSA_7B	E17	QSA#7
MDA43	D21	DQA_43			
MDA44	J19	DQA_44	ODTA0	C31	ODTA0 21
MDA45	G19	DQA_45	ODTA1	C25	ODTA1 22
MDA46	F19	DQA_46			
MDA47	D19	DQA_47	CLKA0	A33	CLKA0 21
MDA48	C19	DQA_48	CLKA1	A26	CLKA1 22
MDA49	B19	DQA_49			
MDA50	A19	DQA_50	CLKA0b	B33	CLKA0# 21
MDA51	B18	DQA_51	CLKA1b	B26	CLKA1# 22
MDA52	C16	DQA_52			
MDA53	B16	DQA_53	RASA0b	A31	RASA#0 21
MDA54	C15	DQA_54	RASA1b	D24	RASA#1 22
MDA55	A15	DQA_55			
MDA56	H18	DQA_56	CASA0b	C32	CASA#0 21
MDA57	F18	DQA_57	CASA1b	H26	CASA#1 22
MDA58	F18	DQA_58			
MDA59	D18	DQA_59	CSA0b_0	A30	CSA0# 21
MDA60	J17	DQA_60	CSA0b_1	B30	
MDA61	G15	DQA_61			
MDA62	E15	DQA_62	CSA1b_0	G24	CSA1# 22
MDA63	D15	DQA_63	CSA1b_1	H24	
+MVREFDA	N35	MVREFDA	CKEA0	B31	CKEA0 21
+MVREFSA	N34	MVREFSA	CKEA1	F24	CKEA1 22
	AM34	NC_1	WEA0b	C29	WEA#0 21
			WEA1b	D22	WEA#1 22

read strobe
write strobe

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U5G

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MEMORY INTERFACE B

MDB0	H15	DQB_0	MAB_0	H2	MAB0
MDB1	G14	DQB_1	MAB_1	H3	MAB1
MDB2	E14	DQB_2	MAB_2	J3	MAB2
MDB3	D14	DQB_3	MAB_3	J5	MAB3
MDB4	H12	DQB_4	MAB_4	J4	MAB4
MDB5	G12	DQB_5	MAB_5	J6	MAB5
MDB6	F12	DQB_6	MAB_6	G5	MAB6
MDB7	D10	DQB_7	MAB_7	J9	MAB7
MDB8	B13	DQB_8	MAB_8	F3	MAB8
MDB9	C12	DQB_9	MAB_9	F4	MAB9
MDB10	B12	DQB_10	MAB_10	J1	MAB10
MDB11	B11	DQB_11	MAB_11	J2	MAB11
MDB12	C9	DQB_12	MAB_A12	J7	MAB12
MDB13	B9	DQB_13	MAB_BA2	F1	BB2
MDB14	A9	DQB_14	MAB_BA0	G2	BB0
MDB15	B8	DQB_15	MAB_BA1	G3	BB1
MDB16	J10	DQB_16			
MDB17	H10	DQB_17	DQMBb_0	D12	DQMB#0
MDB18	F10	DQB_18	DQMBb_1	C10	DQMB#1
MDB19	D9	DQB_19	DQMBb_2	E7	DQMB#2
MDB20	G7	DQB_20	DQMBb_3	C6	DQMB#3
MDB21	G6	DQB_21	DQMBb_4	P3	DQMB#4
MDB22	F6	DQB_22	DQMBb_5	R4	DQMB#5
MDB23	D6	DQB_23	DQMBb_6	W3	DQMB#6
MDB24	C8	DQB_24	DQMBb_7	V8	DQMB#7
MDB25	C7	DQB_25			
MDB26	B7	DQB_26	QSB_0	J14	QSB0
MDB27	A7	DQB_27	QSB_1	B10	QSB1
MDB28	B5	DQB_28	QSB_2	F9	QSB2
MDB29	A5	DQB_29	QSB_3	B6	QSB3
MDB30	C4	DQB_30	QSB_4	P2	QSB4
MDB31	B4	DQB_31	QSB_5	P8	QSB5
MDB32	M3	DQB_32	QSB_6	W2	QSB6
MDB33	M2	DQB_33	QSB_7	V6	QSB7
MDB34	N2	DQB_34			
MDB35	N1	DQB_35	QSB_0B	H14	QSB#0
MDB36	R3	DQB_36	QSB_1B	A10	QSB#1
MDB37	R2	DQB_37	QSB_2B	F9	QSB#2
MDB38	T3	DQB_38	QSB_3B	A6	QSB#3
MDB39	T2	DQB_39	QSB_4B	P1	QSB#4
MDB40	M8	DQB_40	QSB_5B	P7	QSB#5
MDB41	M7	DQB_41	QSB_6B	W1	QSB#6
MDB42	P5	DQB_42	QSB_7B	V5	QSB#7
MDB43	P4	DQB_43			
MDB44	R9	DQB_44	ODTB0	D2	ODTB0 23
MDB45	R8	DQB_45	ODTB1	K5	ODTB1 24
MDB46	R6	DQB_46			
MDB47	U4	DQB_47	CLKB0	A3	CLKB0 23
MDB48	U3	DQB_48	CLKB1	K1	CLKB1 24
MDB49	U2	DQB_49			
MDB50	U1	DQB_50	CLKB0b	B3	CLKB0# 23
MDB51	V2	DQB_51	CLKB1b	K2	CLKB1# 24
MDB52	Y3	DQB_52			
MDB53	Y2	DQB_53	RASB0b	D3	RASB#0 23
MDB54	AA2	DQB_54	RASB1b	K7	RASB#1 24
MDB55	AA1	DQB_55			
MDB56	U9	DQB_56	CASB0b	C1	CASB#0 23
MDB57	U7	DQB_57	CASB1b	K4	CASB#1 24
MDB58	U6	DQB_58			
MDB59	V4	DQB_59	CSB0b_0	E1	CSB0# 23
MDB60	W9	DQB_60	CSB0b_1	E2	
MDB61	W7	DQB_61			
MDB62	W6	DQB_62	CSB1b_0	L3	CSB1# 24
MDB63	W4	DQB_63	CSB1b_1	M4	
+MVREFDB	B14		CKEB0	E3	CKEB0 23
+MVREFSB	A13		CKEB1	K8	CKEB1 24
MVREFDB			WEB0b	E2	WEB#0 23
MVREFSB			WEB1b	M6	WEB#1 24
TESTEN		AM30			
TEST_MCLK		AA8			
TEST_YCLK		AA7			
MEMTEST		AA5	DRAM_RST	AA4	
PLLTEST		AH19			

RV44 1K_0402_5%
RV45 4.7K_0402_5%
RV46 4.7K_0402_5%
RV47 240_0402_1%

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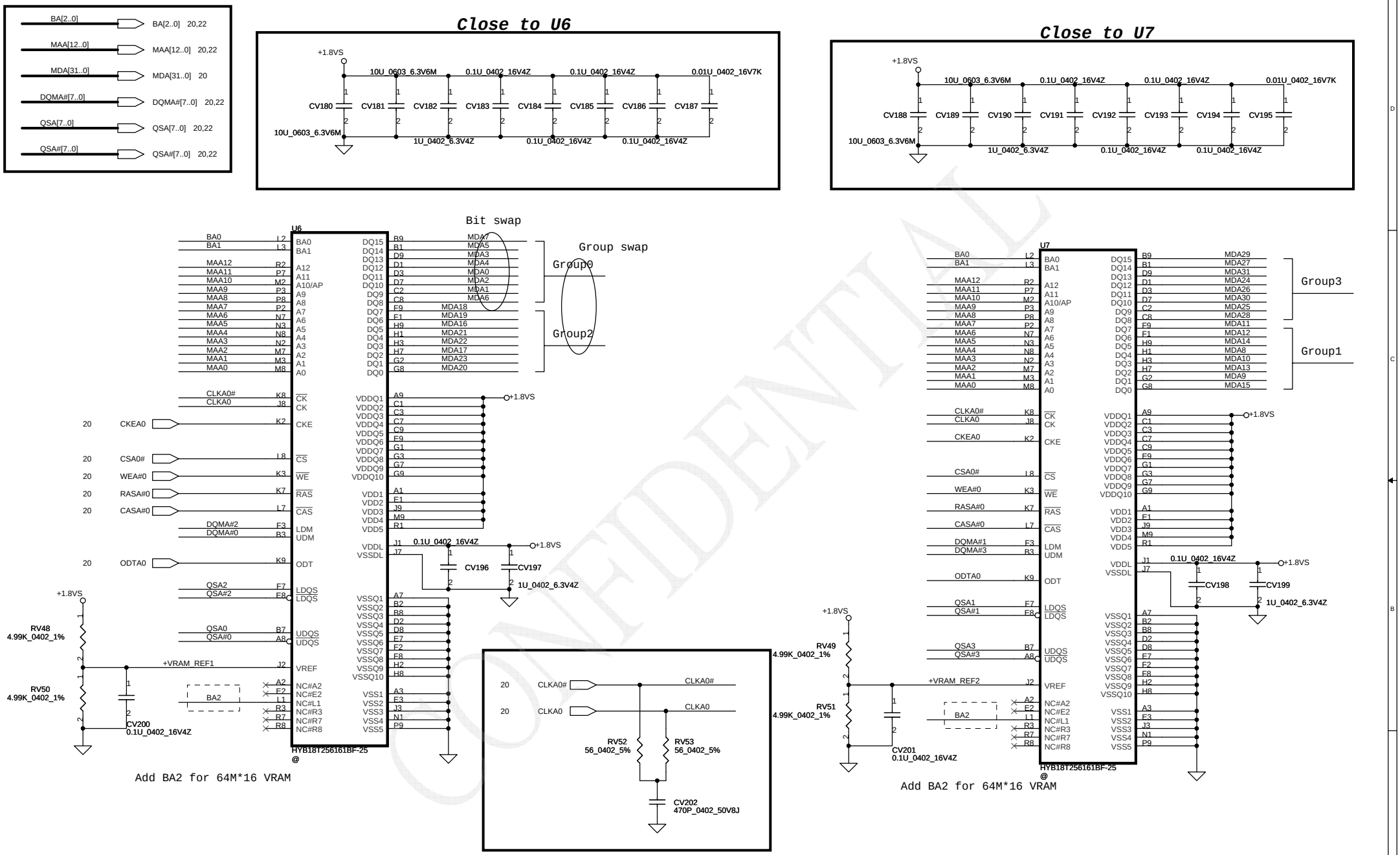

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MDA[63..32] MDA[63..32] 20
DQMA#[7..0] DQMA#[7..0] 20,21
QSA[7..0] QSA[7..0] 20,21
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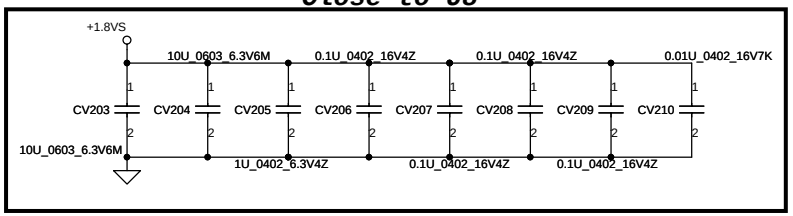
Close to U8



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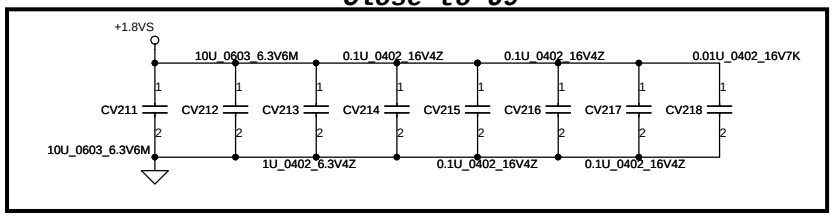

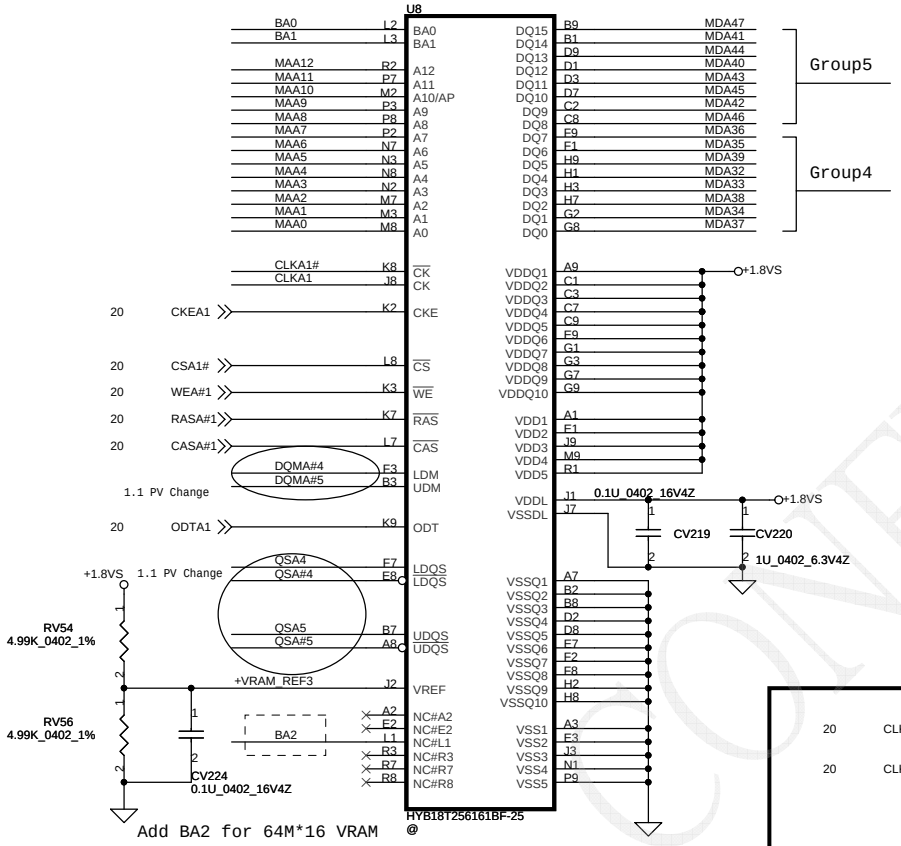

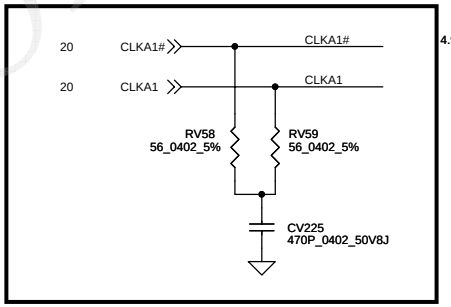

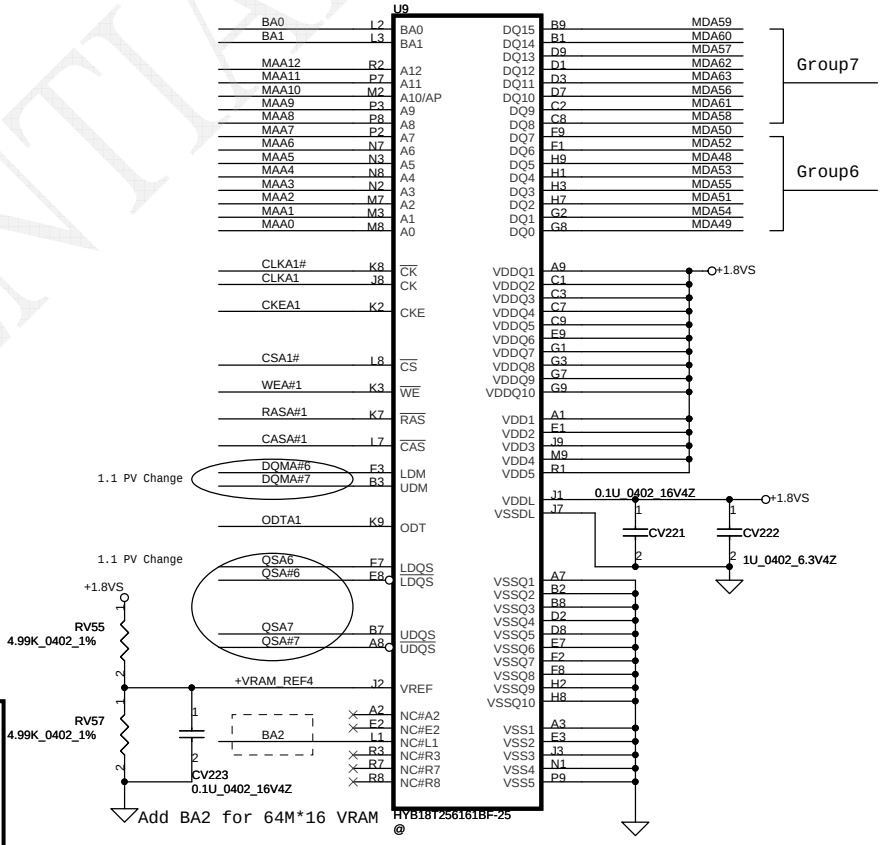

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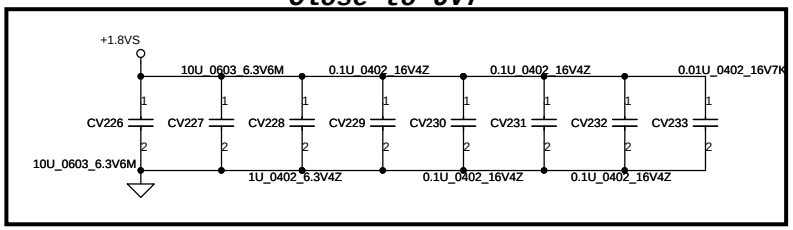
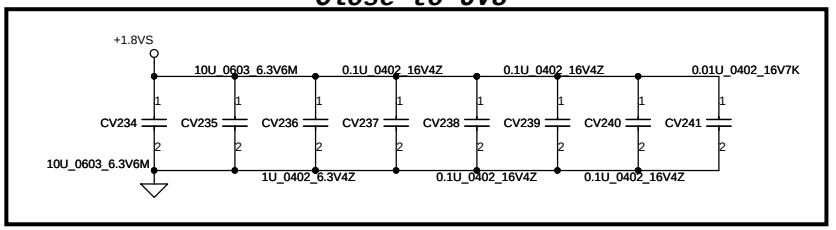
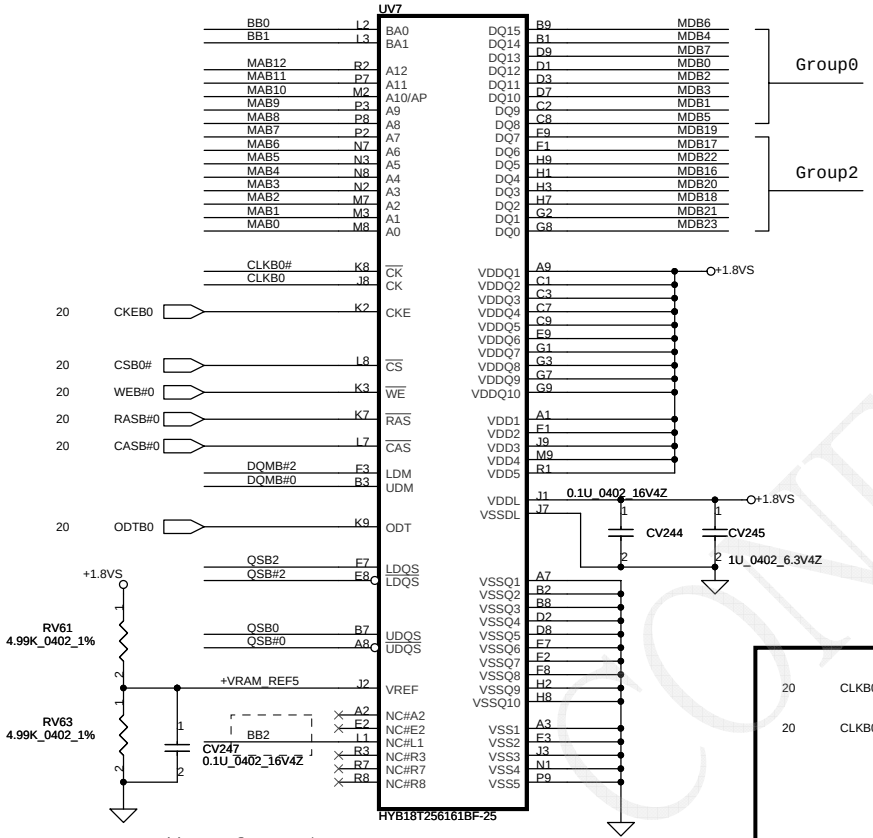
BB[2..0] BB[2..0] 20,24
MAB[12..0] MAB[12..0] 20,24
MDB[31..0] MDB[31..0] 20
DQMB#[7..0] DQMB#[7..0] 20,24
QSB[7..0] QSB[7..0] 20,24
QSB#[7..0] QSB#[7..0] 20,24

Close to UV7

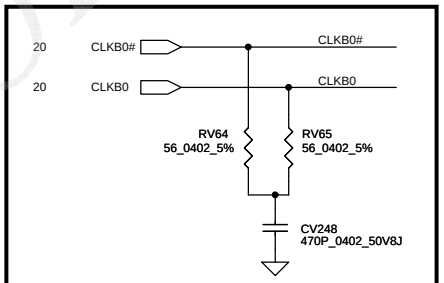


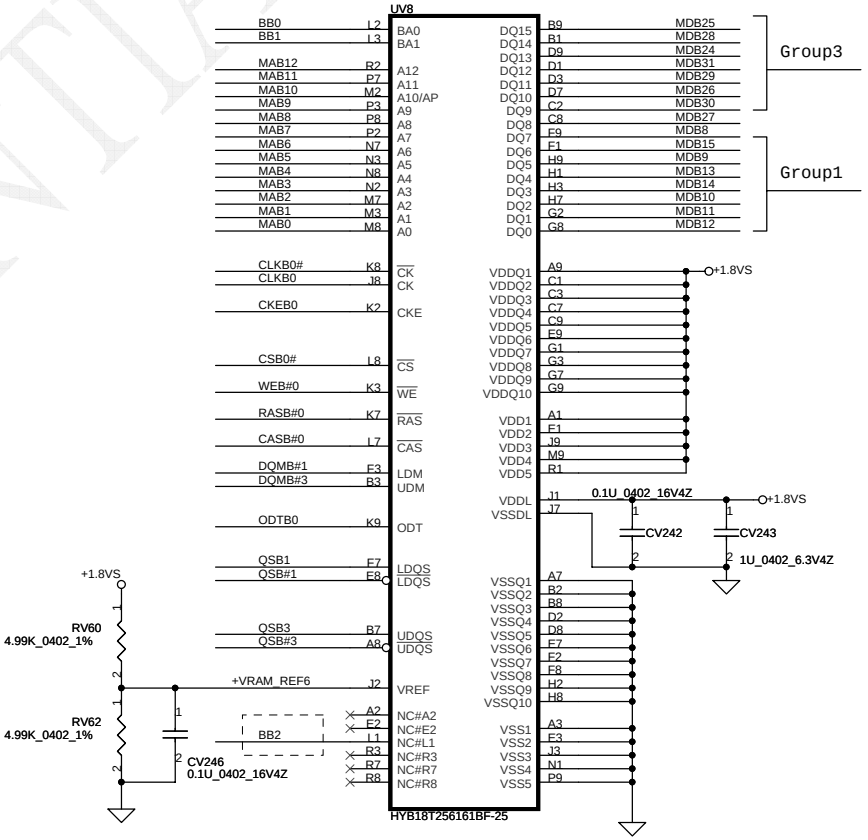
Close to UV8





Add BA2 for 64M*16 VRAM





Add BA2 for 64M*16 VRAM

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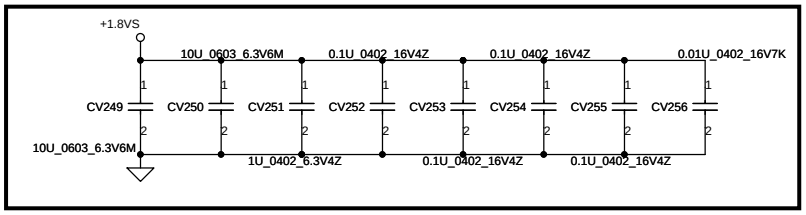
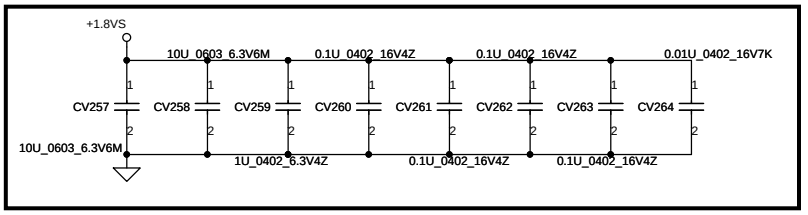
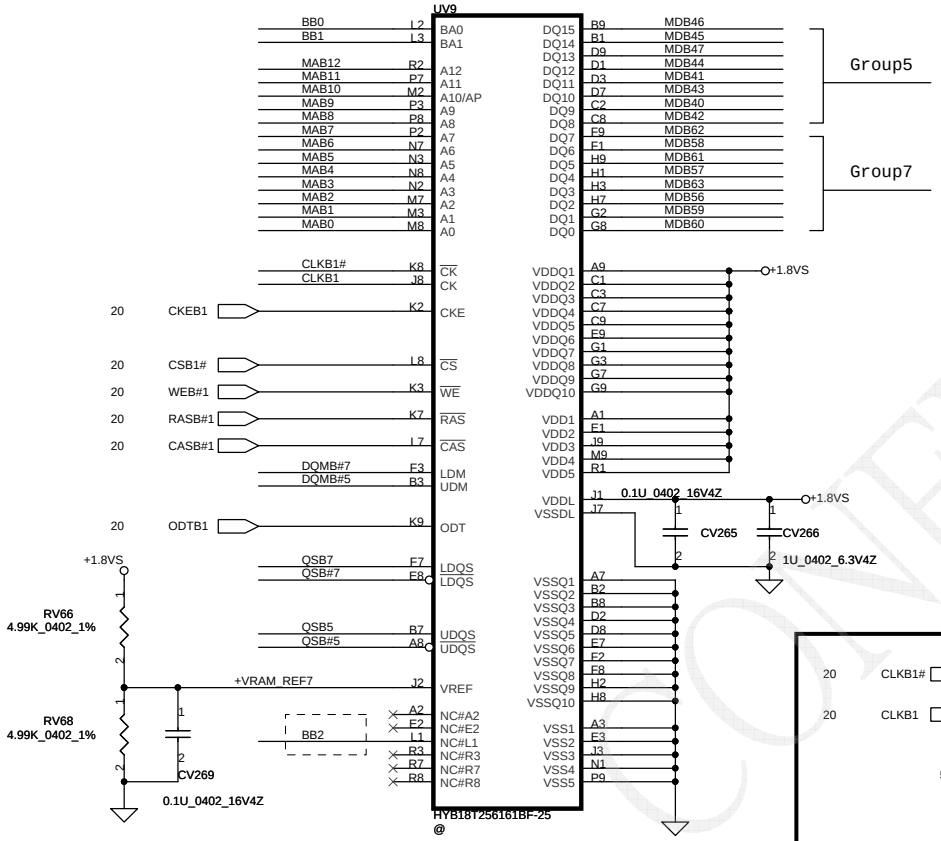
BB[2..0] BB[2..0] 20,23
MAB[12..0] MAB[12..0] 20,23
MDB[63..32] MDB[63..32] 20
DQMB#[7..0] DQMB#[7..0] 20,23
QSB[7..0] QSB[7..0] 20,23
QSB#[7..0] QSB#[7..0] 20,23

Close to UV9

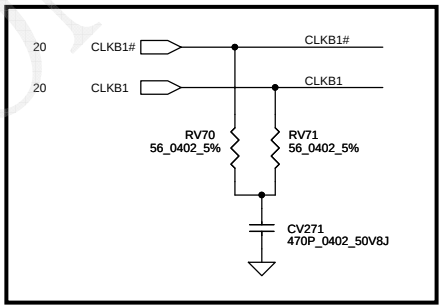


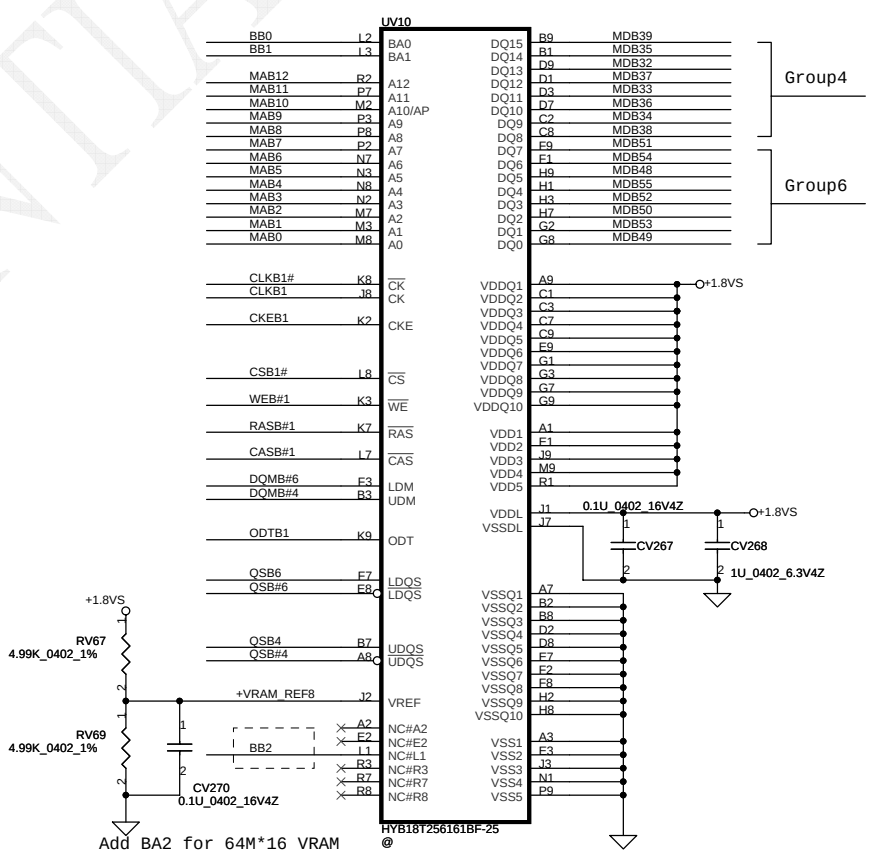
Close to UV10





Add BA2 for 64M*16 VRAM





Add BA2 for 64M*16 VRAM

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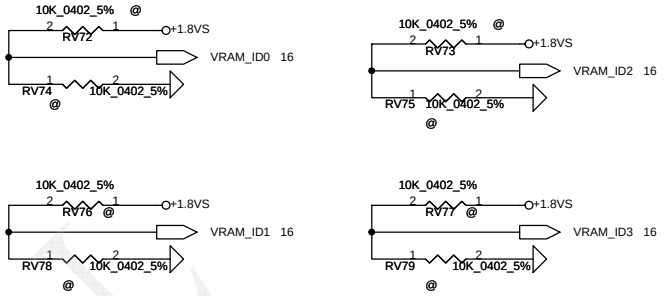
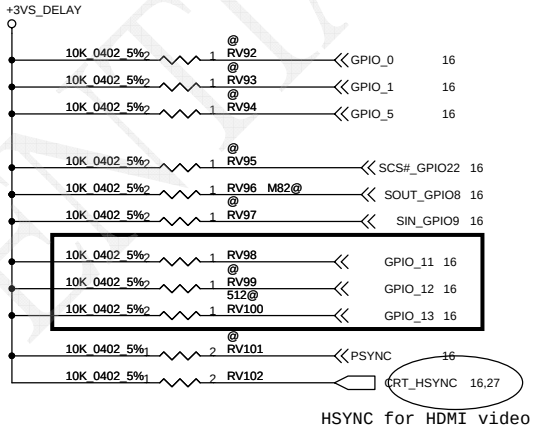
STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M82M-XT	JBK00 1.0a	512M(x4)	Samsung 64Mx16 1.8V	SA00002MD00	0 0 0 0
			JBK00 1.0	256M(X4)	Samsung 32Mx16 1.8V	SA00002AJ10	0 0 0 1
				512M(x4)	Hynix 64Mx16 1.8V		0 0 1 0
			JBK00 1.0	256M(X4)	Hynix 32Mx16 1.8V	SA00002DL00	0 0 1 1
			JBK00 1.0	256M(X4)	Qimonda 32Mx16 1.8V	SA00002A600	0 1 0 0
			JBK00 1.0a	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00	0 1 0 1
		M86M	JBK00 1.1	512M(x8)	Samsung 32Mx16 1.8V	SA00002AJ10	0 1 1 0
			JBK00 1.1	512M(x8)	Hynix 32Mx16 1.8V	SA00002DL00	0 1 1 1
			JBK00 1.1	512M(x8)	Qimonda 32Mx16 1.8V	SA00002A600	1 0 0 0
				1G(x8)	Samsung 64Mx16 1.8V	SA00002MD00	1 0 0 1
				1G(x8)	Hynix 64Mx16 1.8V		1 0 1 0
				1G(x8)	Qimonda 64Mx16 1.8V	SA00002MF00	1 0 1 1



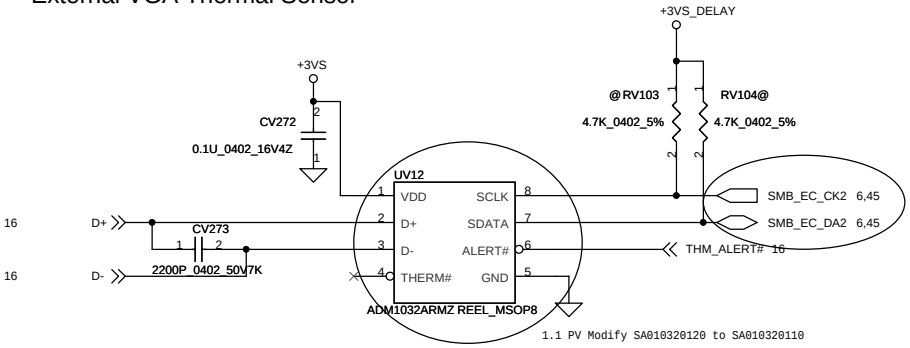
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO ***M86-M ONLY***	
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO ***M82-M ONLY***	
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 0 1
BIF_VGA_DIS	PSYNC	VGA ENABLED===0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1



HSYNC for HDMI video

GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	MEMORY SIZE
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

External VGA Thermal Sensor



1.1 PV Modify SA010320120 to SA010320110

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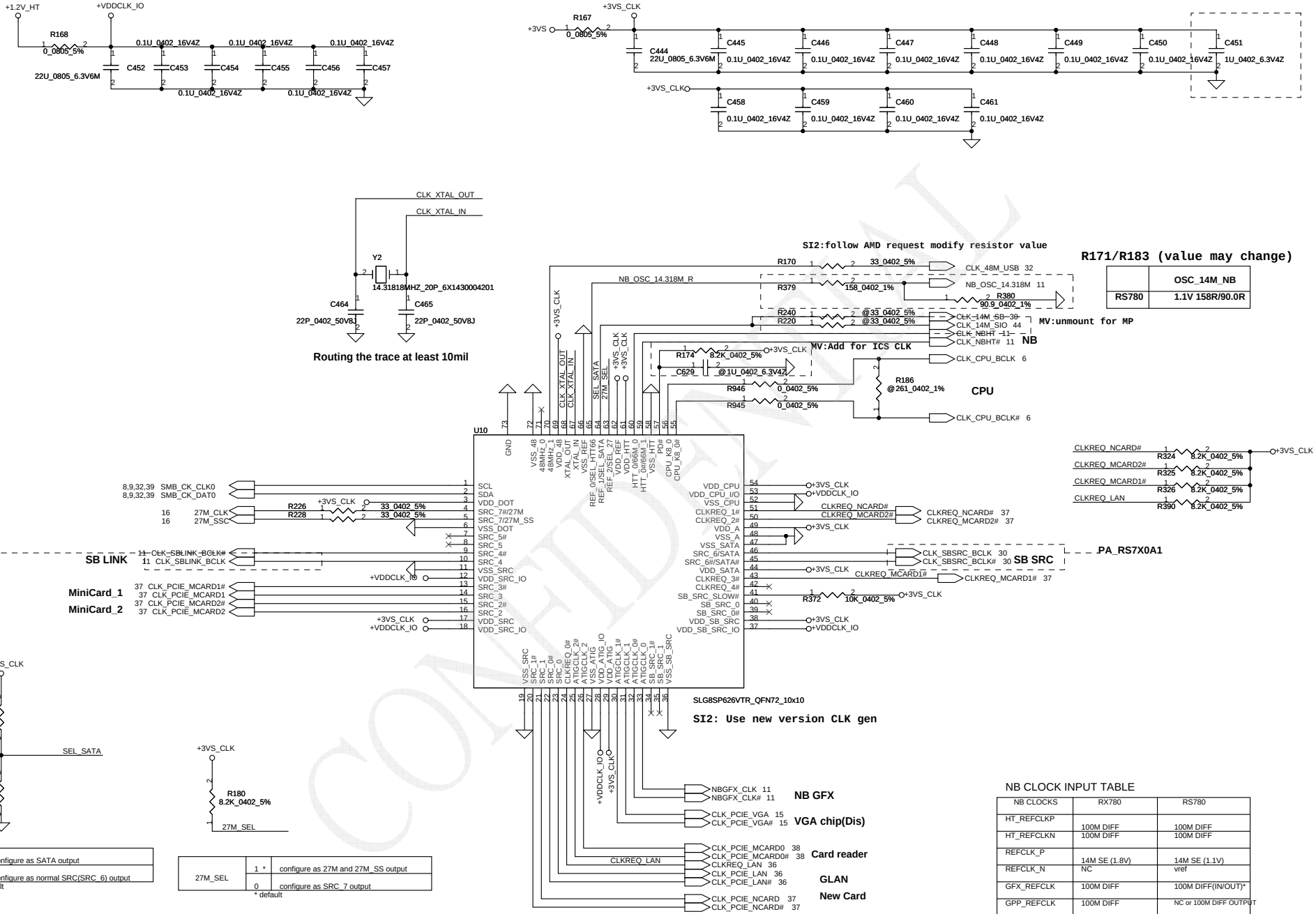

SEL_SATA		
	1	configure as SATA output
	0 *	configure as normal SRC(SRC_6) output

* default

27M_SEL		
	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M		
	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output

* default

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

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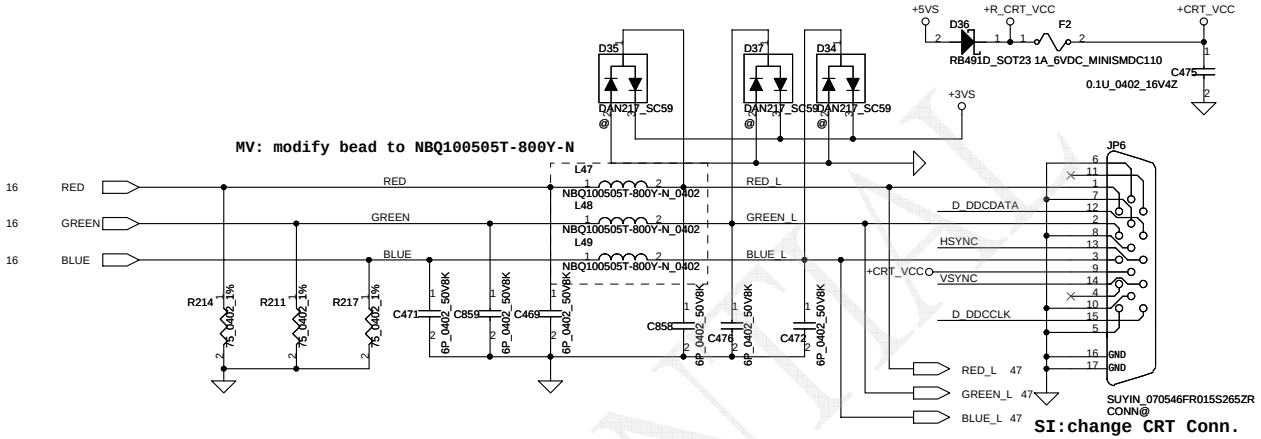
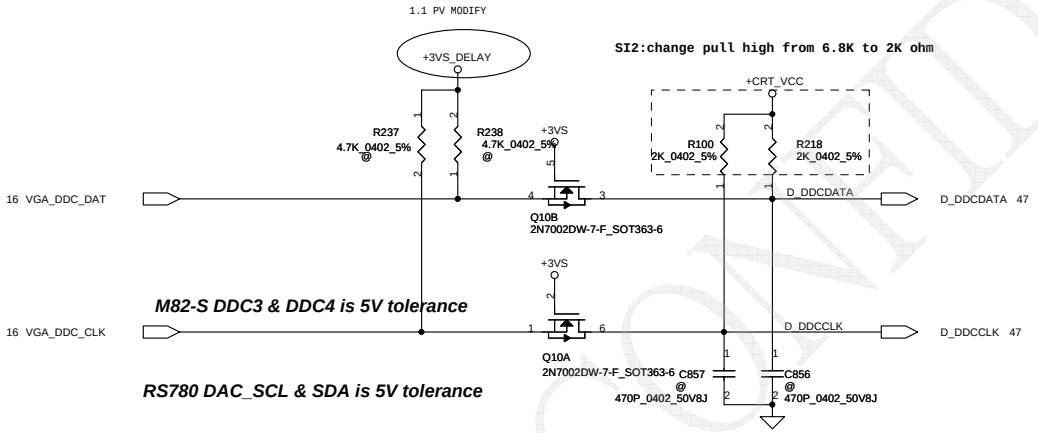
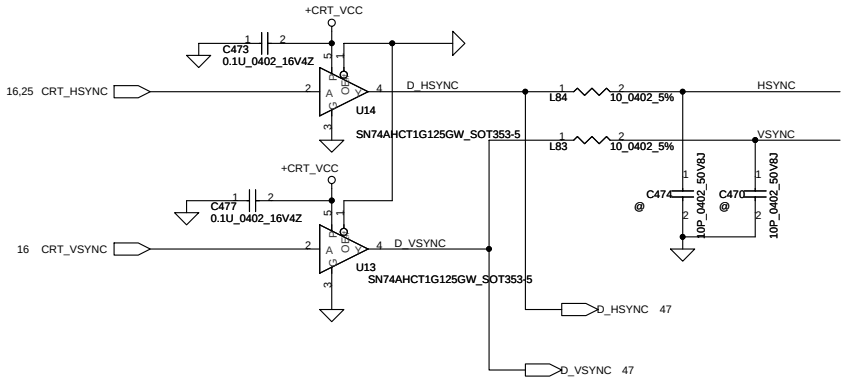
CRT CONNECTOR







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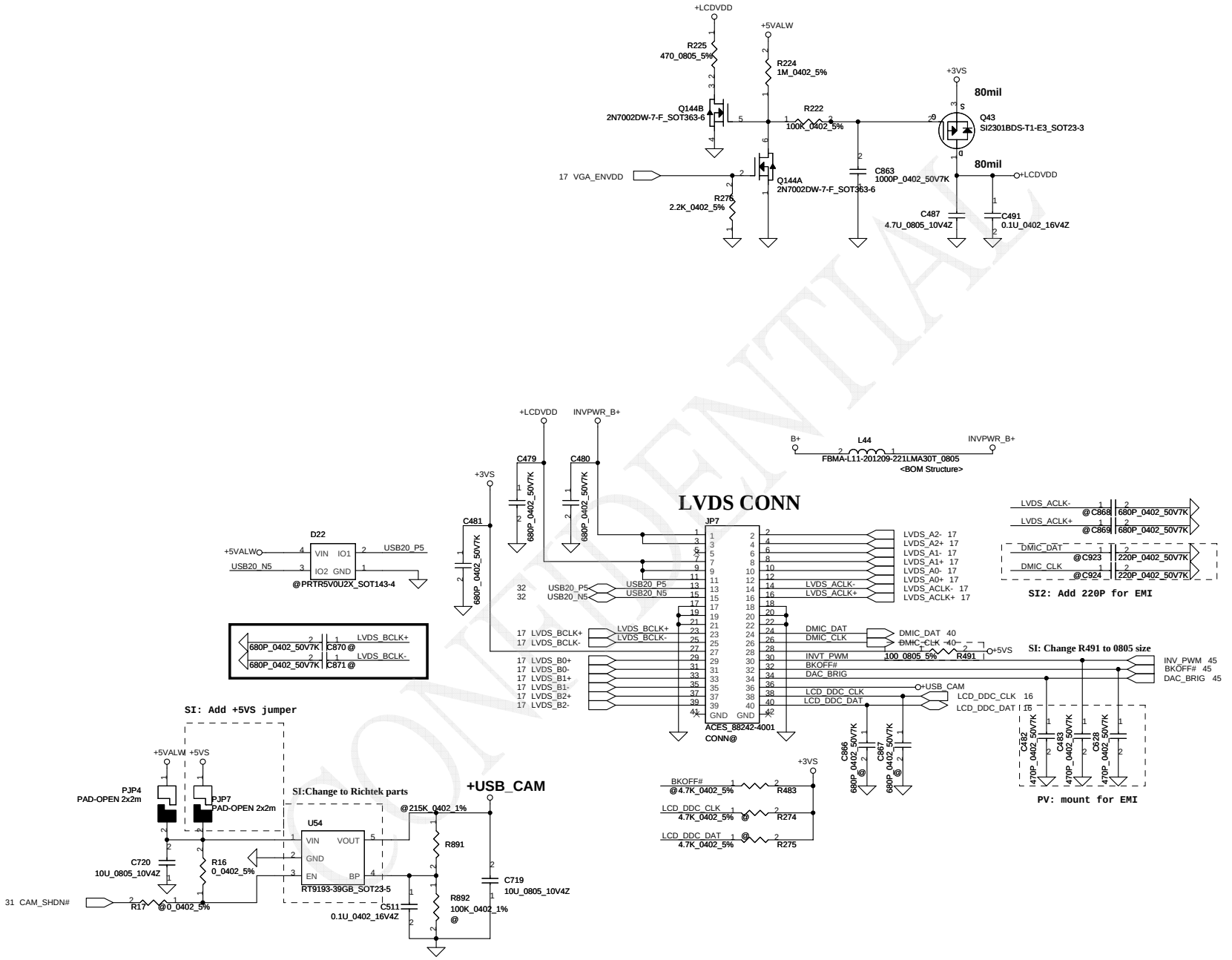

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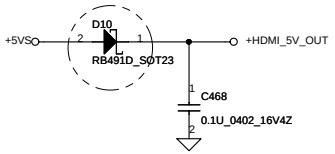
1.1 PV MODIFY

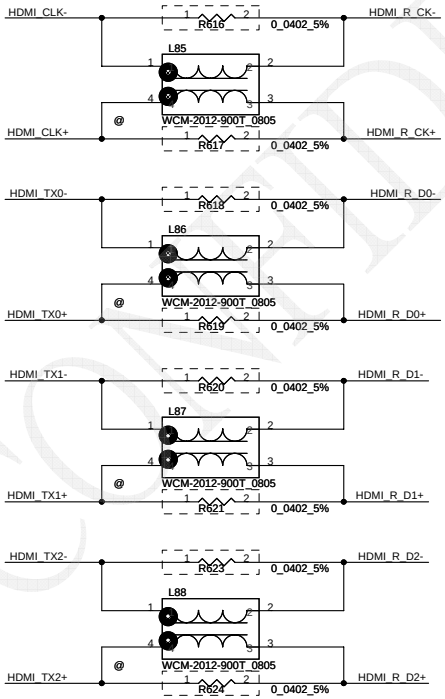
SI2:change pull high from 6.8K to 2K ohm

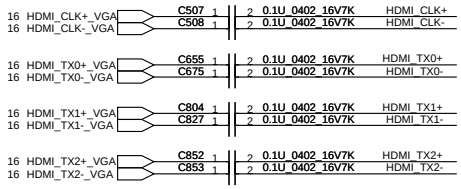
C:Chg. PN to SB770020010.

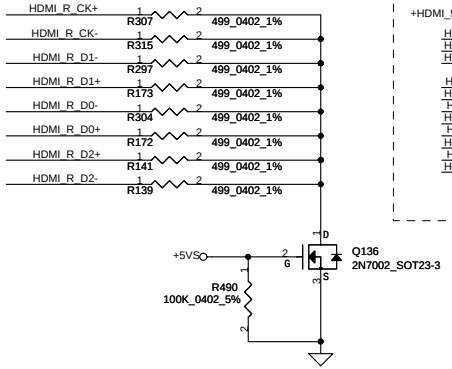
MP:Update D10 to meet HDMI.



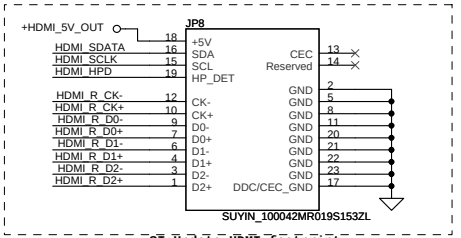
SI:Add R6161~R624 for EMI requset







HDMI Connector



SI:Update HDMI footprint

CONN@

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Check AMD need pull low or not

R300 1 2 NB_RST# R @8.2K_0402_5%

U15A

SB700

Part 1 of 5

NB_RST# R → N2 A_RST#

SB_RX0P 10 → C492 0.1U_0402_16V7K → SB_RX0P_C → V23 PCIE_TX0P
SB_RX0N 10 → C493 0.1U_0402_16V7K → SB_RX0N_C → V22 PCIE_TX0N
SB_RX1P 10 → C494 0.1U_0402_16V7K → SB_RX1P_C → V24 PCIE_TX1P
SB_RX1N 10 → C495 0.1U_0402_16V7K → SB_RX1N_C → V25 PCIE_TX1N
SB_RX2P 10 → C496 0.1U_0402_16V7K → SB_RX2P_C → U25 PCIE_TX2P
SB_RX2N 10 → C497 0.1U_0402_16V7K → SB_RX2N_C → U24 PCIE_TX2N
SB_RX3P 10 → C498 0.1U_0402_16V7K → SB_RX3P_C → T23 PCIE_TX3P
SB_RX3N 10 → C499 0.1U_0402_16V7K → SB_RX3N_C → T22 PCIE_TX3N

SB_TX0P 10 → U22 PCIE_RX0P
SB_TX0N 10 → U21 PCIE_RX0N
SB_TX1P 10 → U19 PCIE_RX1P
SB_TX1N 10 → V19 PCIE_RX1N
SB_TX2P 10 → R20 PCIE_RX2P
SB_TX2N 10 → R21 PCIE_RX2N
SB_TX3P 10 → R18 PCIE_RX3P
SB_TX3N 10 → R17 PCIE_RX3N

R305 562_0402_1% / R306 2.05K_0402_1% → T25 PCIE_CALRP, T24 PCIE_CALRN

+PCIE_VDDR → L33 BLM18PG121SN1D_0603 → +SB_PCIEVDD → P24 PCIE_PVDD, P25 PCIE_PVSS
+1.2V_HT

C504 10U_0805_10V4Z, C505 1U_0402_6.3V4Z

Close to SB

PCI EXPRESS INTERFACE

PCICLK0 P4, PCICLK1 P3, PCICLK2 P1, PCICLK3 P2, PCICLK4 T4, PCICLK5/GPIO41 T3 → PCI CLKS

PCI_CLK2 34
PCI_CLK3 34
PCI_CLK4 34
PCI_CLK5 34

PCIRST# → N1

AD0 U2, AD1 P7, AD2 V4, AD3 T1, AD4 V3, AD5 U1, AD6 V1, AD7 V2, AD8 T2, AD9 W1, AD10 T9, AD11 R6, AD12 R7, AD13 R5, AD14 U8, AD15 U5, AD16 Y7, AD17 W8, AD18 V9, AD19 Y8, AD20 AA8, AD21 Y4, AD22 V3, AD23 Y2, AD24 AA2, AD25 AB4, AD26 AA1, AD27 AB3, AD28 AB2, AD29 AC1, AD30 AC2, AD31 AD1

AD23 PCI_AD23 34
AD24 PCI_AD24 34
AD25 PCI_AD25 34
AD26 PCI_AD26 34
AD27 PCI_AD27 34
AD28 PCI_AD28 34

CBE0# W2, CBE1# U7, CBE2# AA7, CBE3# Y1, FRAME# AA6, DEVSEL# W5, IRDY# AA5, TRDY# Y5, PAR U6, STOP# W6, PERR# W4, SERR# V7 → PCI_SERR# 45, REQ0# AC3, REQ1# AD4, REQ2# AB7, REQ3#/GPIO70 AE6, REQ4#/GPIO71 AB6 → PAD T15, GNT0# AD2, GNT1# AE4, GNT2# AD5, GNT3#/GPIO72 AC6, GNT4#/GPIO73 AE5 → PAD T16, CLKRUN# AD6 → PAD T17, LOCK# V5

INTE#/GPIO33 AD3, INTF#/GPIO34 AC4, INTG#/GPIO35 AE2, INTH#/GPIO36 AF3 → PCI_PIRQH# → R967 0_0402_5% → ACCEL_INT 39

08/29 new add

PCI INTERFACE

26 CLK_SBSRC_BCLK → N25 PCIE_RCLKP/NB_LNK_CLKP
26 CLK_SBSRC_BCLK# → N24 PCIE_RCLKN/NB_LNK_CLKN

K23 NB_DISP_CLKP, K22 NB_DISP_CLKN
M24 NB_HT_CLKP, M25 NB_HT_CLKN
P17 CPU_HT_CLKP, M18 CPU_HT_CLKN
M23 SLT_GFX_CLKP, M22 SLT_GFX_CLKN
J19 GPP_CLK0P, J18 GPP_CLK0N
L20 GPP_CLK1P, L19 GPP_CLK1N
M19 GPP_CLK2P, M20 GPP_CLK2N
N22 GPP_CLK3P, P22 GPP_CLK3N
L18 25M_48M_66M_OSC

CLOCK GENERATOR

@R314 20M_0402_5%
C643 18P_0402_50V8J
R389 20M_0603_5%
C652 18P_0402_50V8J
Y3 32.768KHZ_12.5P_1TJS125BJ4A421P
SB_32KHI, SB_32KHO

Close to SB

26 CLK_14M_SB → J21 25M_X1
R241 0_0402_5% → J20 25M_X2

SB_32KHI → A3 X1
SB_32KHO → B3 X2

RTC XTAL

CLK_PCI_EC → R303 @100_0402_5% → C501 @100P_0402_25V8K
CLK_PCI_SIO → R369 @100_0402_5% → C503 @100P_0402_25V8K

LPCCLK0 G22, LPCCLK1 E22 → R308 22_0402_5% CLK_PCI_EC, R309 22_0402_5% CLK_PCI_SIO, R310 @22_0402_5%
→ CLK_PCI_EC 34,45
→ CLK_PCI_SIO 34,44
→ CLK_PCI_SIO2 44

LAD0 H24 → LPC_AD0 44,45
LAD1 H23 → LPC_AD1 44,45
LAD2 J25 → LPC_AD2 44,45
LAD3 J24 → LPC_AD3 44,45
LFRAME# H25 → LPC_FRAME# 44,45
LDRQ0# H22
LDRQ1#/GNT5#/GPIO68 AB8 → LPC_DRQ1# 44
BMREQ#/REQ5#/GPIO65 AD7
SERIRQ V15 → SIRQ 44,45

LPC

RTCCLK C3 → RTC_CLK 34 **STRAP PIN**
INTRUDER_ALERT# C2
VBAT B2 → +SB_VBAT

RTC

+3VS → R319 10K_0402_5% → H_PROCHOT#

6,11 CPU_LDT_REQ# → CPU_LDT_REQ# F23 ALLOW_LDTSTP
6 H_PROCHOT# → H_PROCHOT# F24 PROCHOT#
6,56 H_PWRGD → H_PWRGD F22 LDT_PG
6,11 LDT_STOP# → G25 LDT_STP#
6 LDT_RST# → G24 LDT_RST#

CPU

218S7EALA11FG_BGA528_SB700
SBR1@

+SB_VBAT → R316 120_0402_5% → +RTCVCC_R → R317 120_0402_5% → +RTCVCC
W=20mils

D42 DAN202U_SC70
+3VL → R876 1K_0402_5% → +RTCBATT
W=20mils

JBATT1 ACES_85205-02001 CONN@ (1 2 3 4 GND GND)

C509 0.1U_0402_16V4Z, C510 1U_0402_6.3V4Z

J1 @JUMP_43X39

+3VALW → C506 @0.1U_0402_16V4Z

U16 @NC7SZ08P5X_NL_SC70-5
NB_RST# R → PLT_RST# → PLT_RST# 11,14,15,36,37,38,44,45
R312 33_0402_5%

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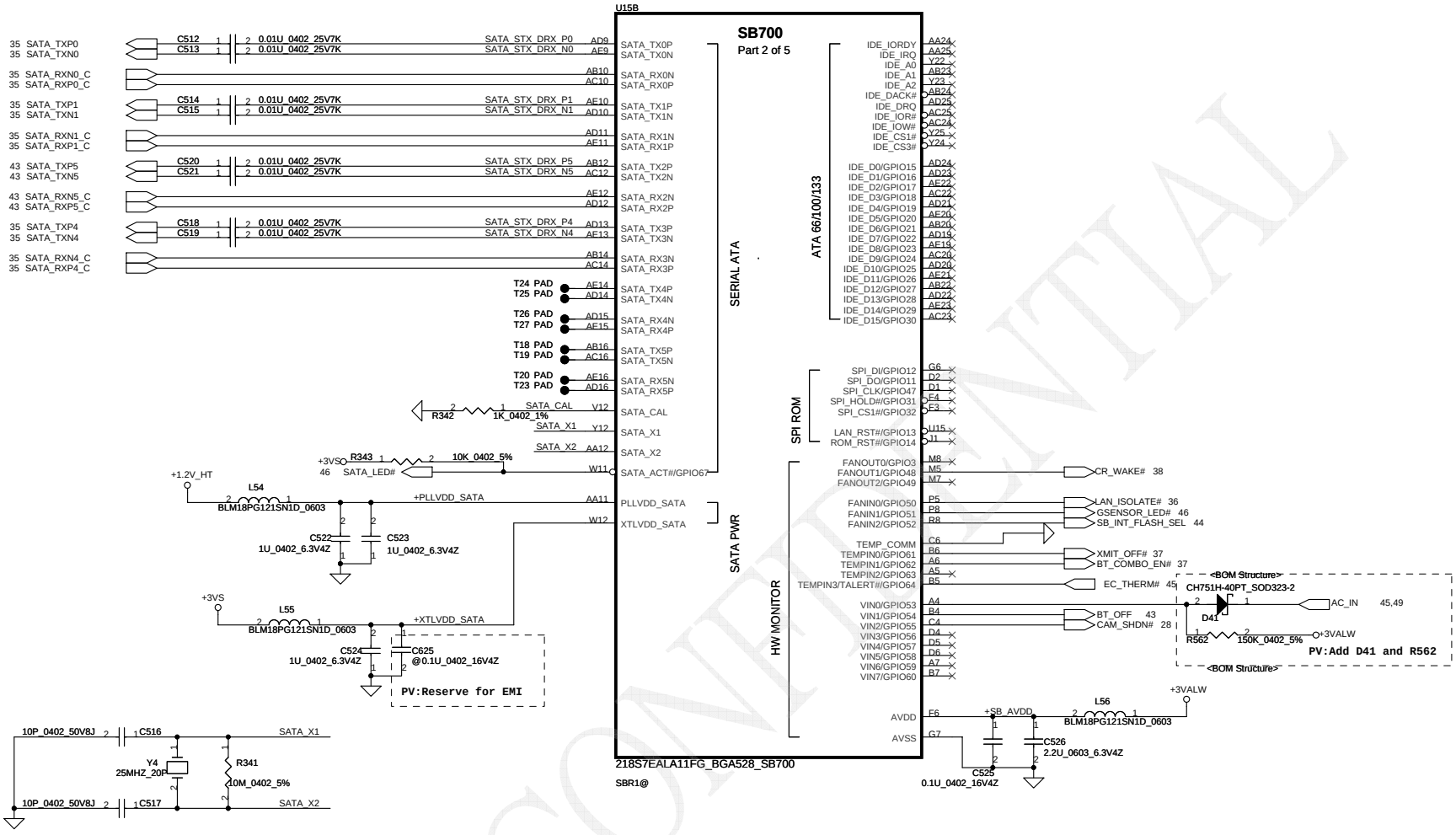

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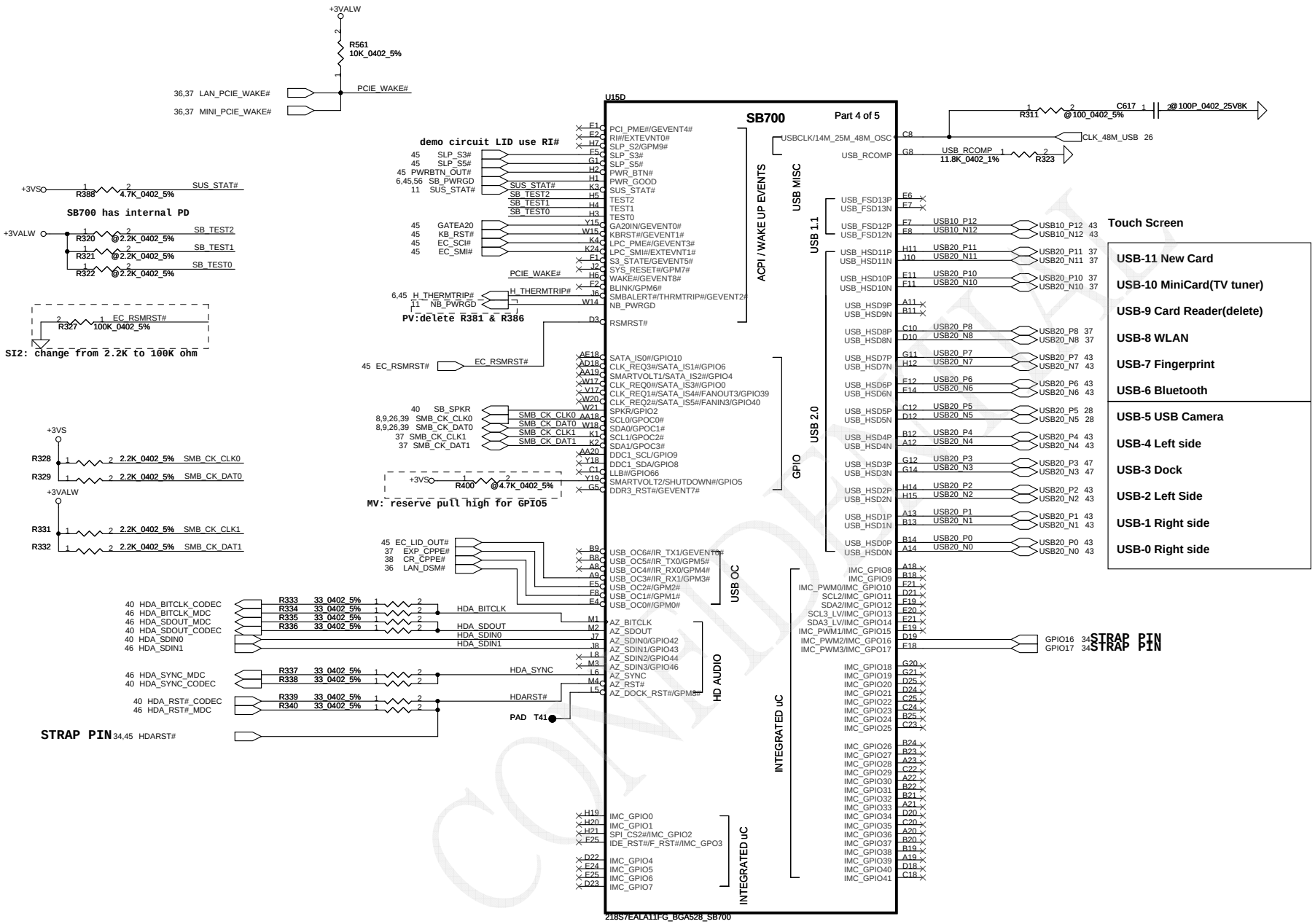

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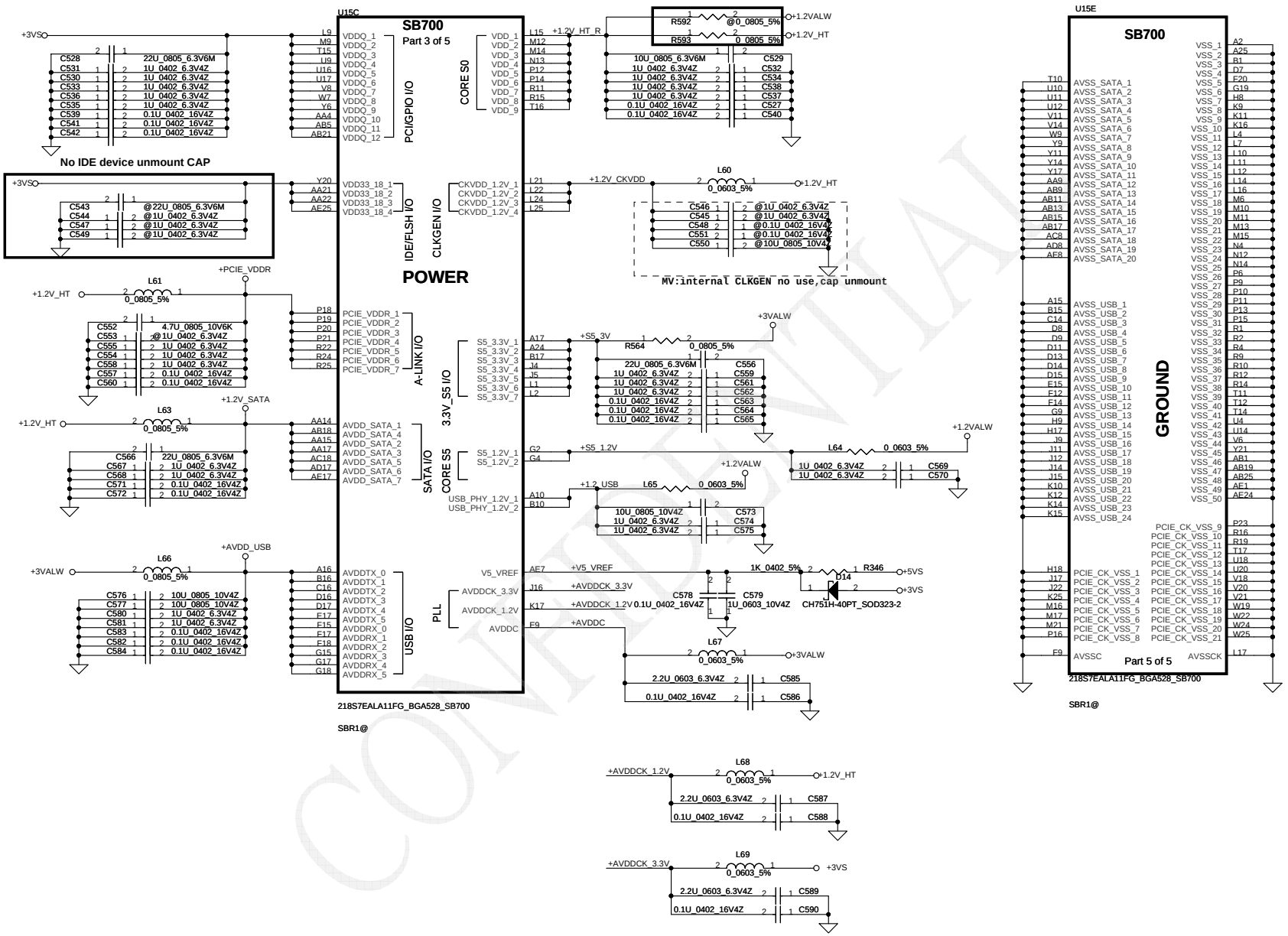

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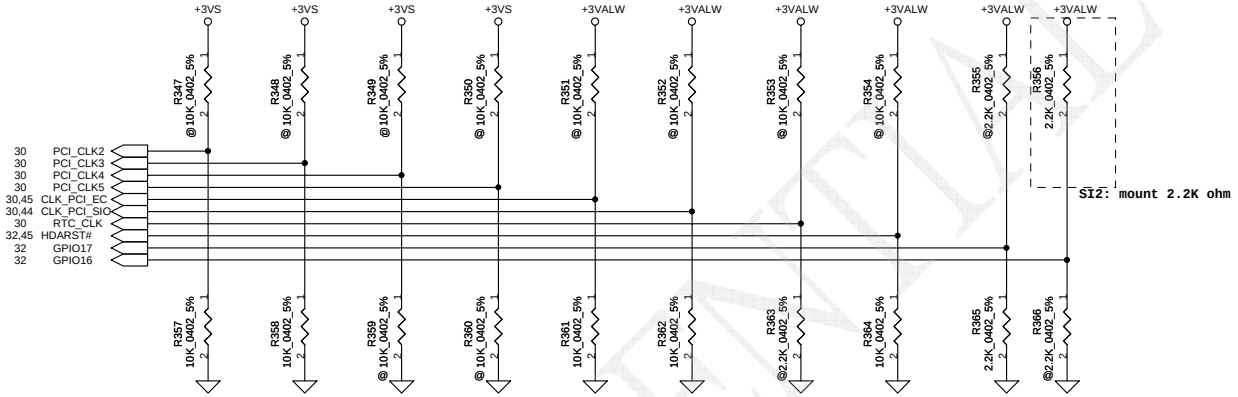
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

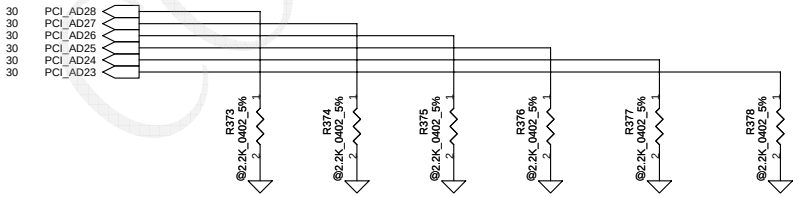
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



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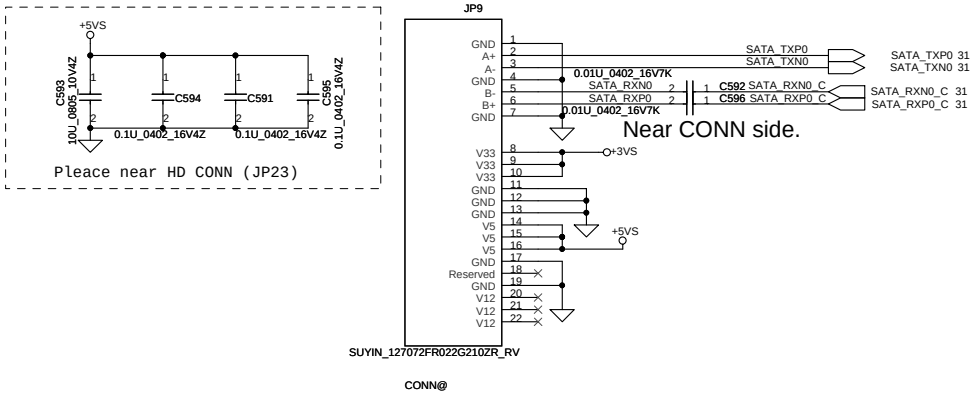
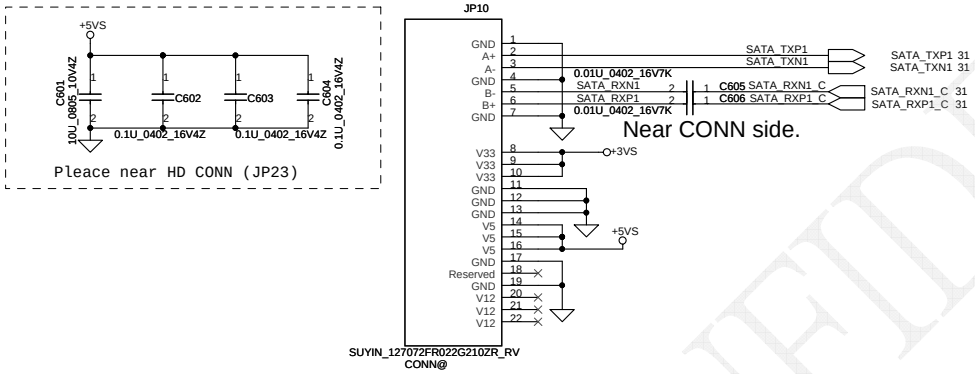
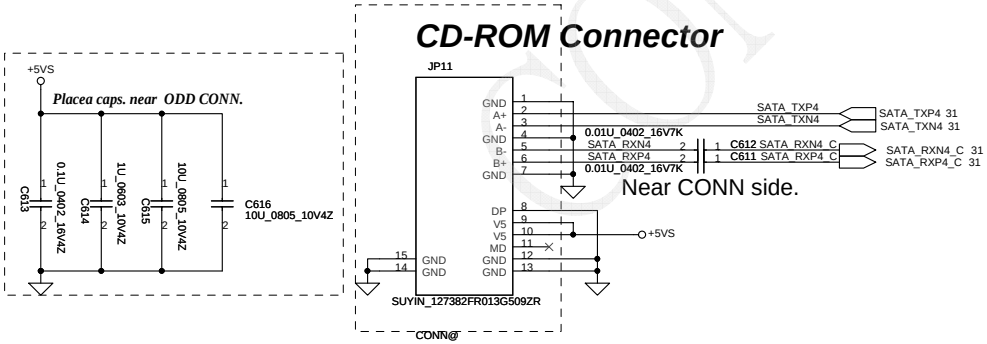
HDD Connector



2nd HDD Connector-option



CD-ROM Connector



SI: Update ODD footprint to fix pin reverse issue

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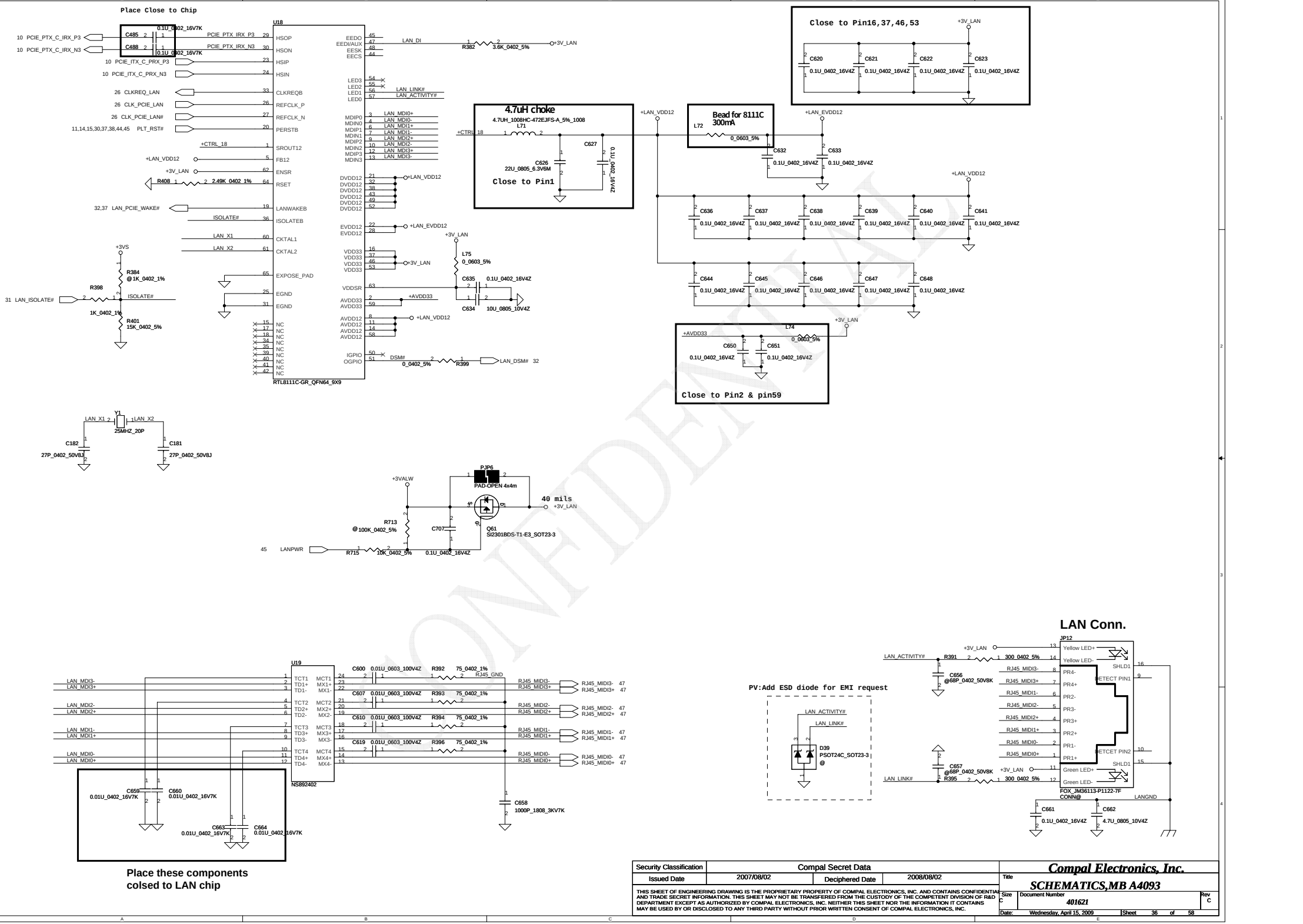

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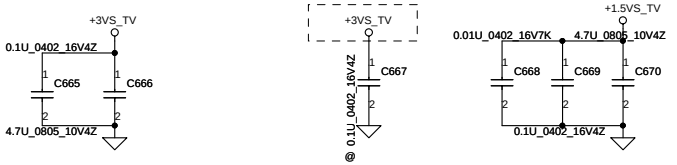
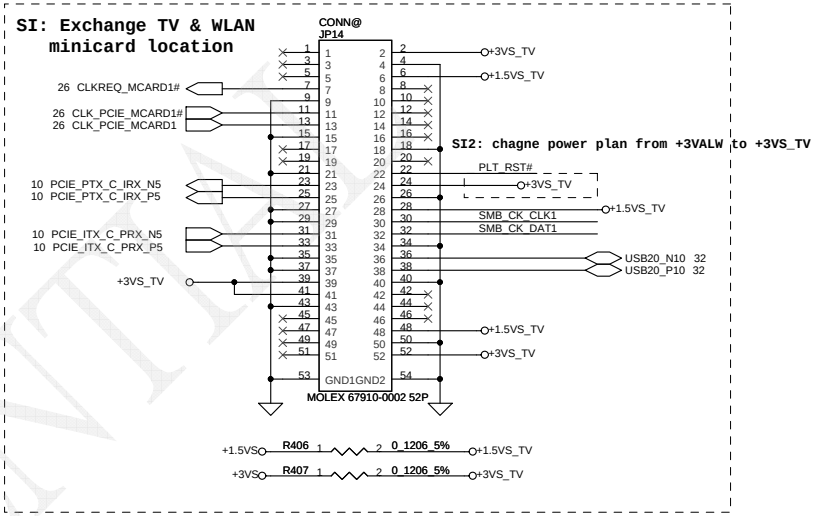
Mini Card---TV tuner

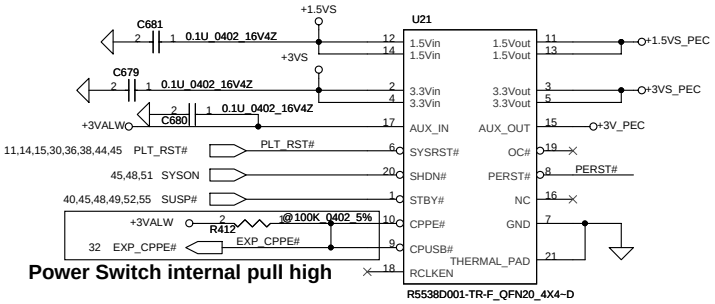
SI2: chagne power plan from +3VALW to +3VS_TV



SI: Exchange TV & WLAN minicard location



New Card

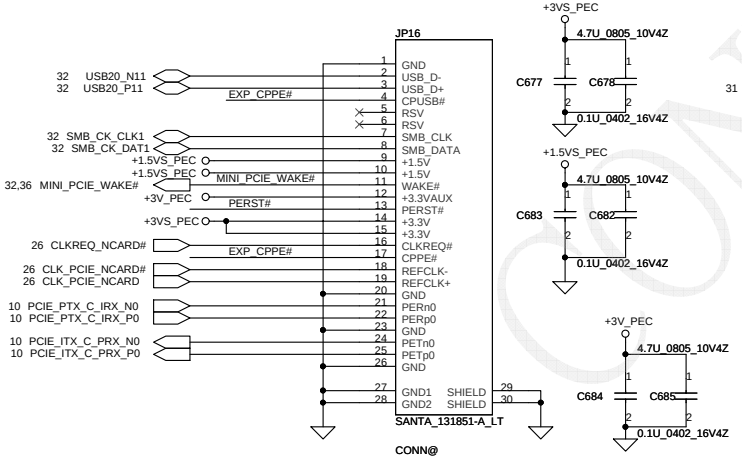


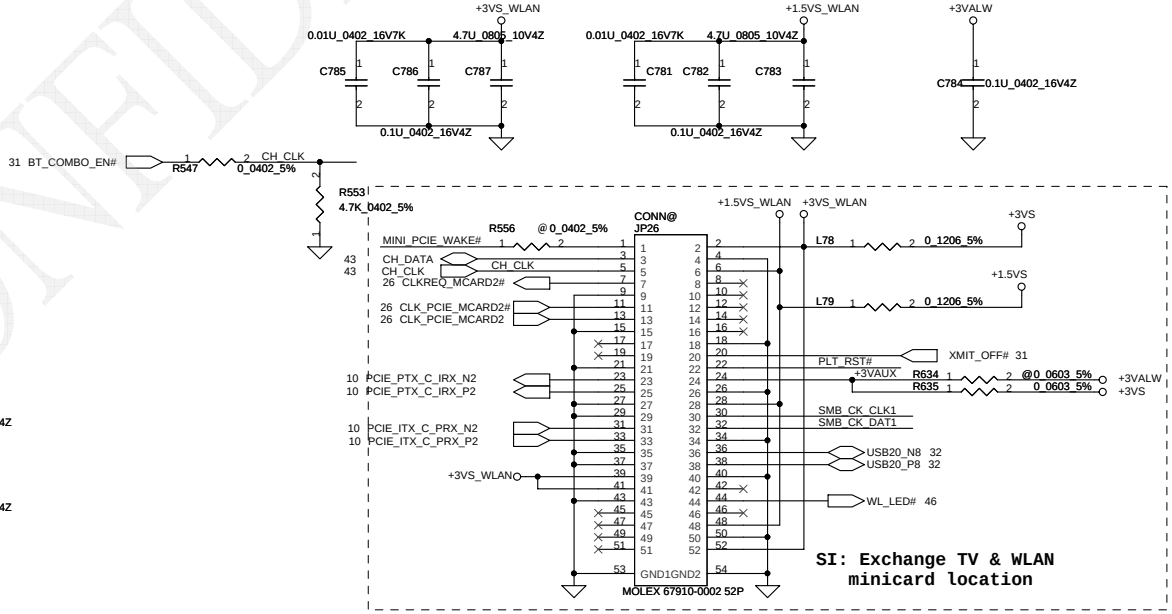
Power Switch internal pull high

USE TI TPS2231MRGPR

Mini-Express Card---WLAN

Near to Express Card slot.





SI: Exchange TV & WLAN minicard location

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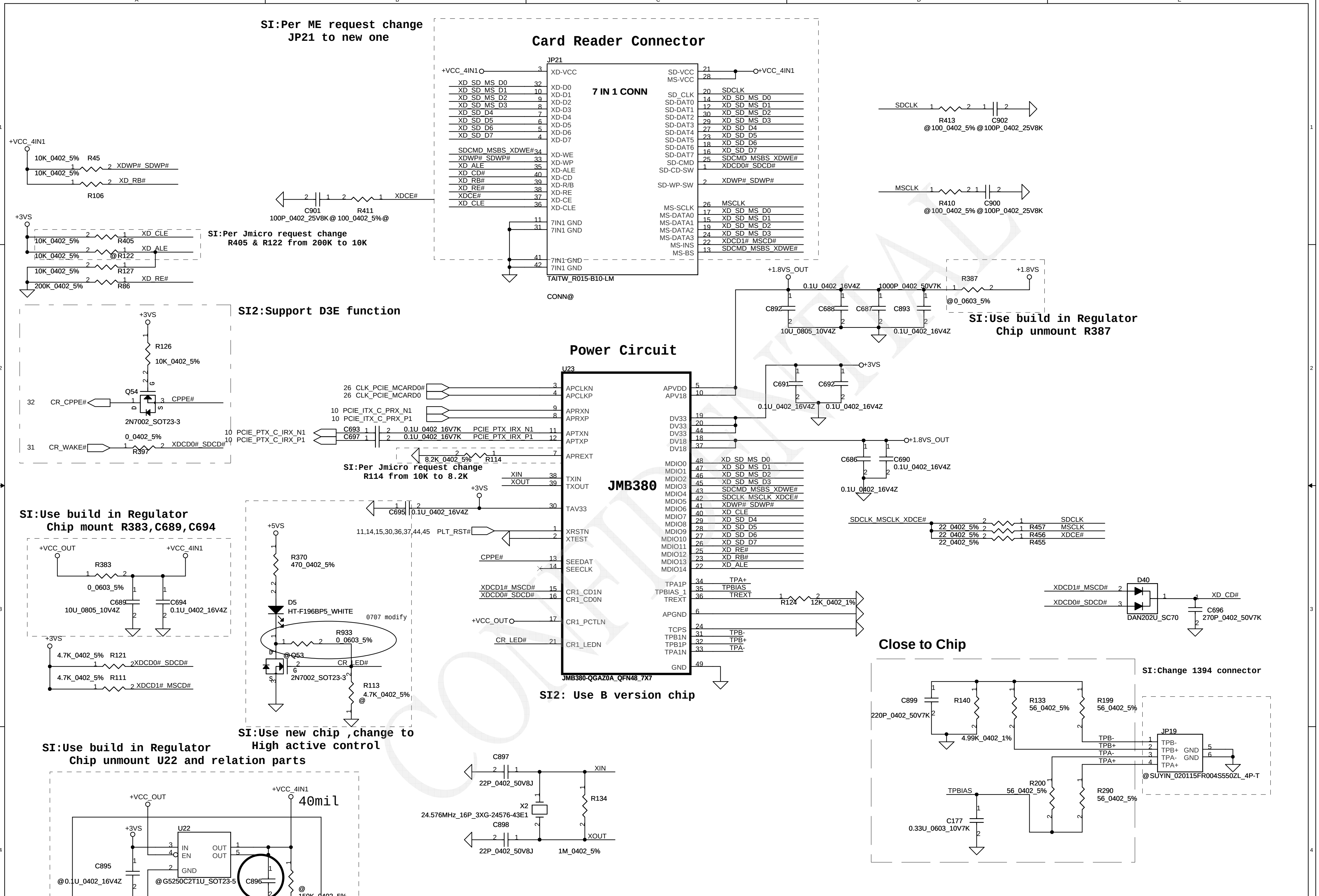

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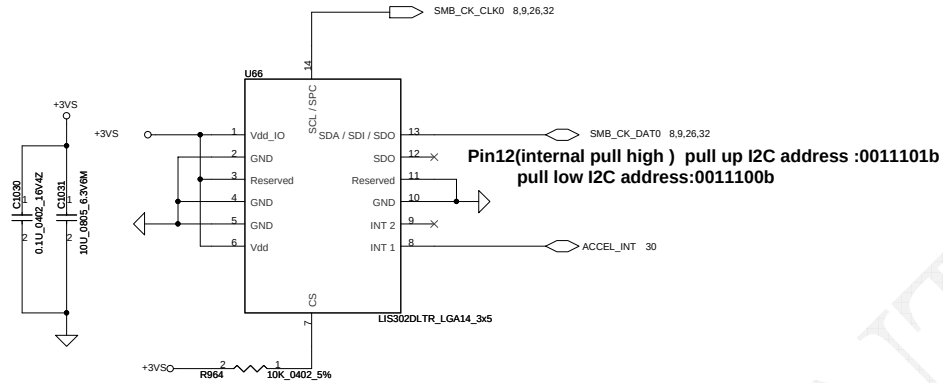
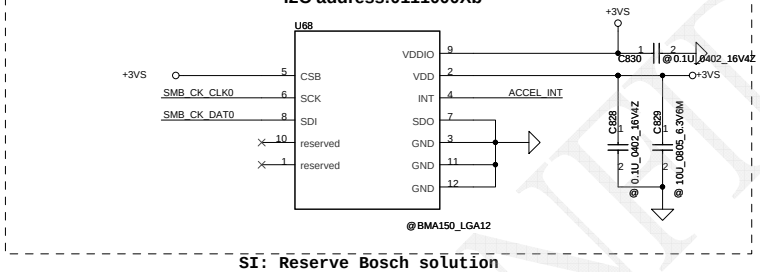
ACCELEROMETER



Pin12(internal pull high) pull up I2C address :0011101b
pull low I2C address:0011100b

I2C address:0111000Xb



SI: Reserve Bosch solution

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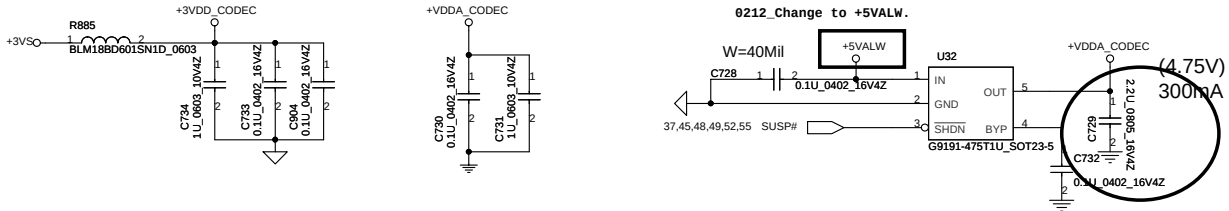
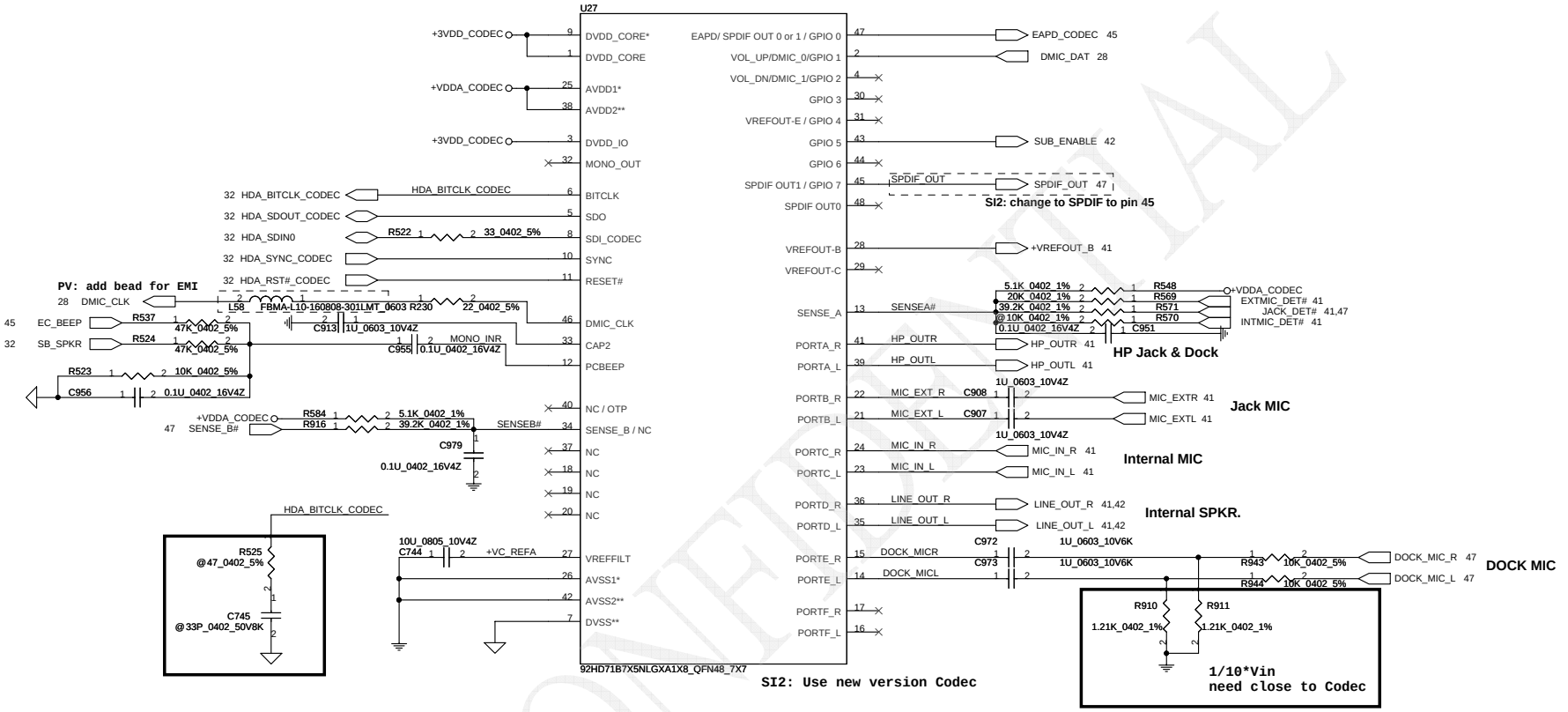
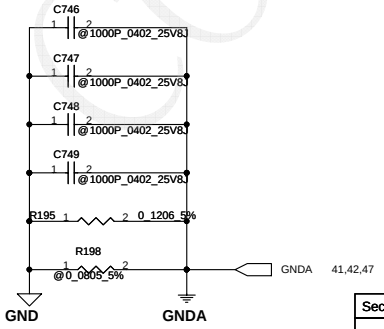
CODEC POWER





SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0(LOW)	0(LOW)	OFF	ON	ON	Disable
0(LOW)	NC	OFF	ON	OFF	Disable
NC	0(LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

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SI2:change from 12.7K to 7.5K

SI2:change from 0.047u to 0.1u

Keep 10 mil width

SI2:change from 10u to 1u for PA PA sound issue

TPA6020A2RGWR_QFN20_5x5

PV:change cap form 100uF to 150uF

HP OUT For M/B

SI: change 2n7002 to dual package

SI2: Add cap & 44.2 ohm for dock

PV:change cap form 100uF to 150uF

HP OUT For Docking

Analog MIC

SP02000D000 S W-CONN ACES 85204-04001 4P P1.25

SPEAKER

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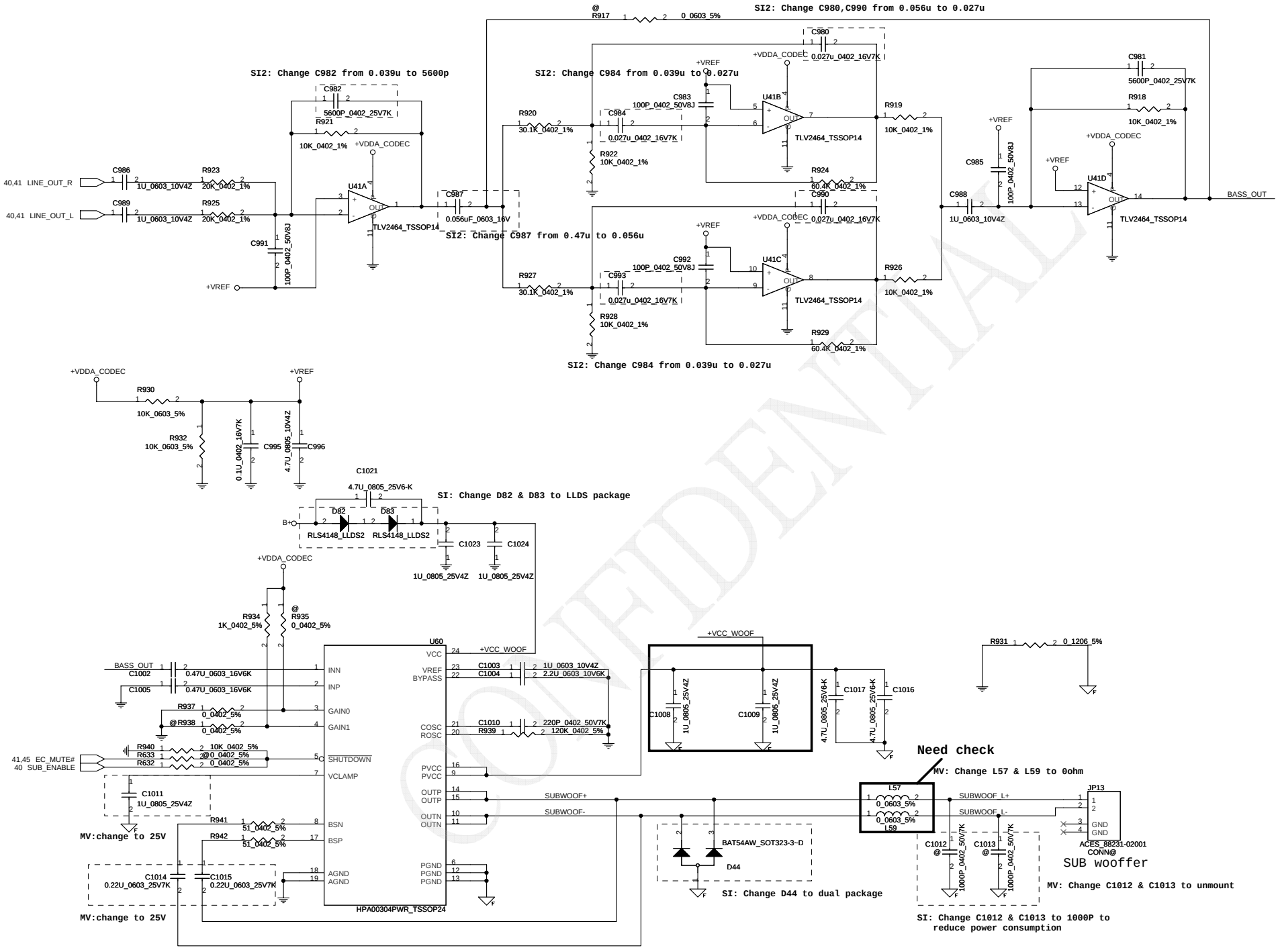

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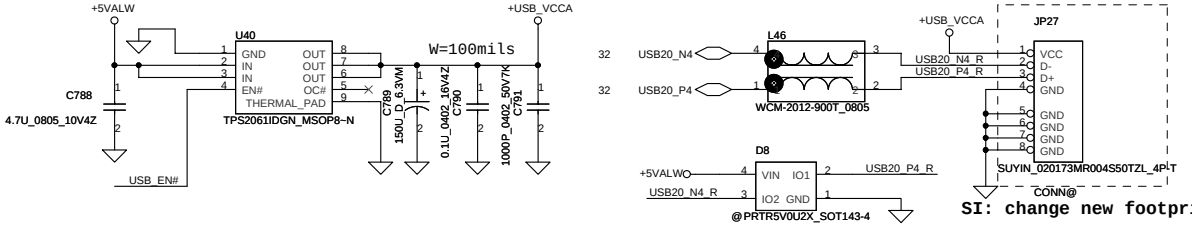
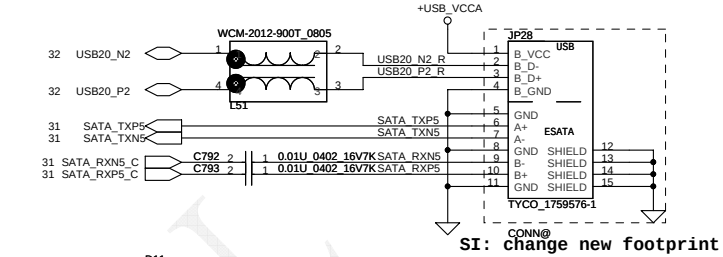
Left side USB CONNECTOR 0



SI: change new footprint

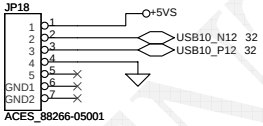
Left side ESATA/USB combination Connector



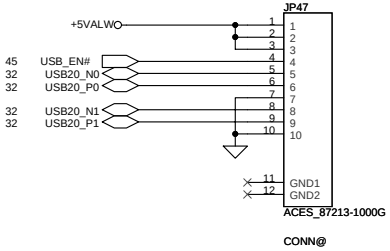
SI: change new footprint

SI: new add for ESD

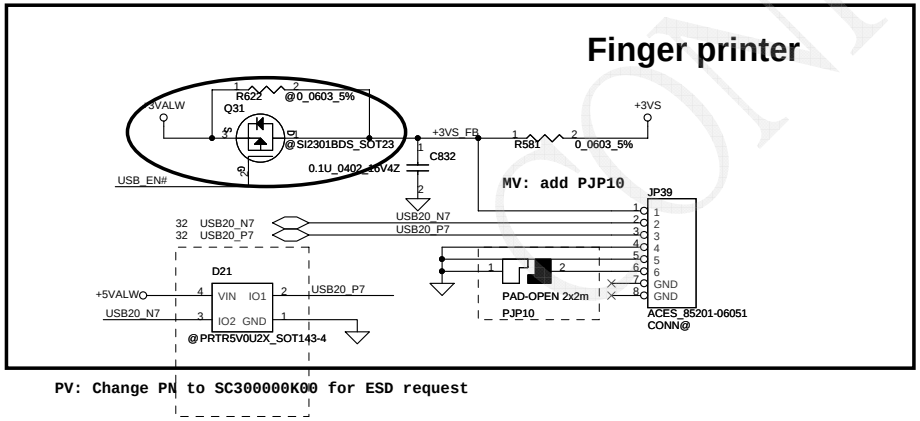
Touch screen



USB Board Conn

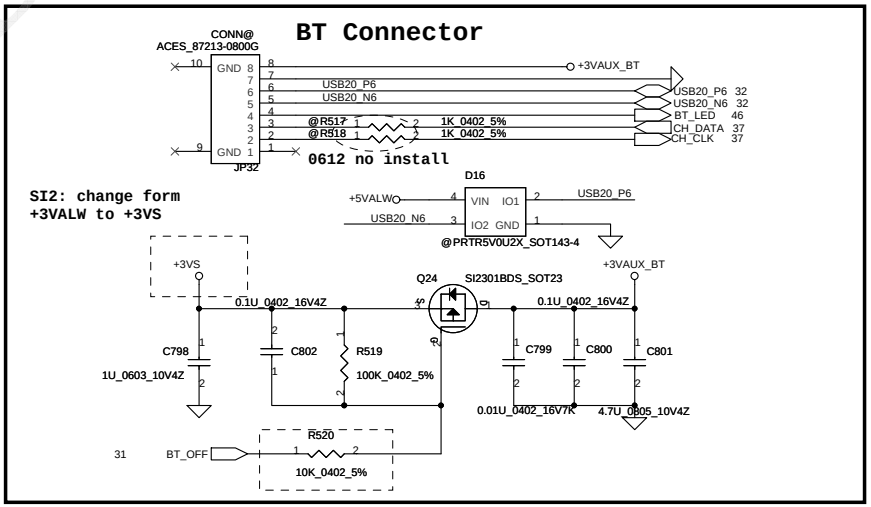


Finger printer



PV: Change PN to SC300000K00 for ESD request

BT Connector



SI: change to 10K ohm to make sure MOS can turn on

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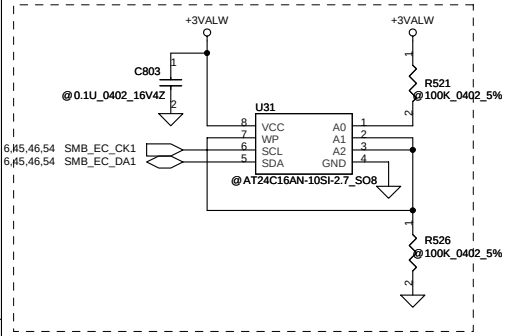
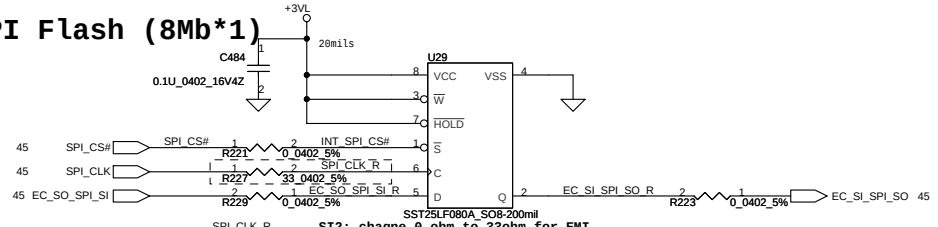
SI2: Change from +3VL to +3VALW and unmount this EEPROM

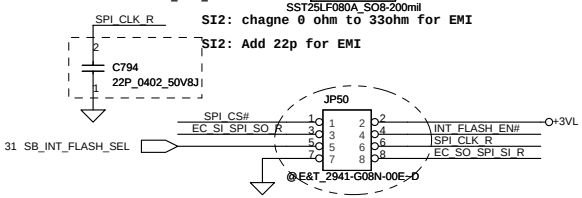


SPI Flash (8Mb*1)



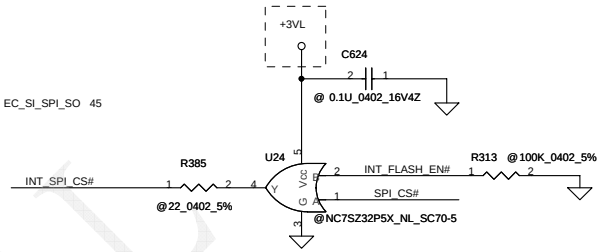
SI2: chagne 0 ohm to 33ohm for EMI

SI2: Add 22p for EMI

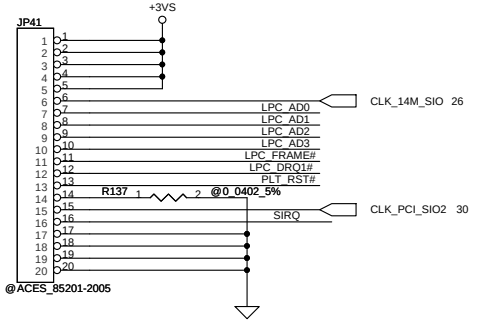


C:Chg. PN to LTC00000200

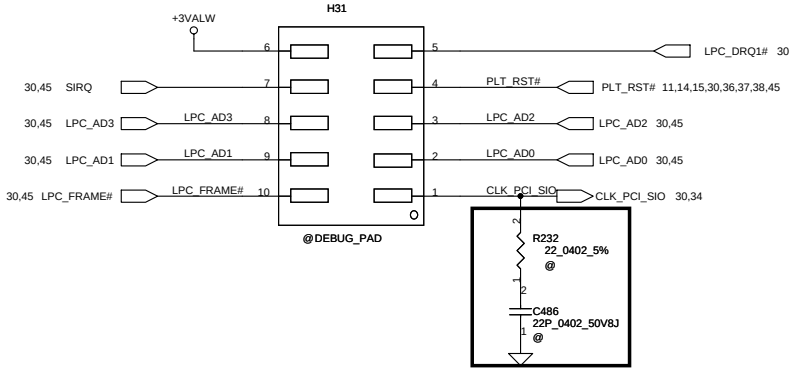
SI2: Change from +3VALW to +3VL



LPC Debug Port



LPC Debug Port



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SI2: Change keyboard conn

PV: change to BEAD for EMI request

SI2: Change from +5VL to +3VL

SI2: Change from 10K to 100K

0205_Add Pull down
R402 for SUSP#.

PV:Add for AC_LED function

PV: Change from +3VALW to +3VL

SI: Mount C814 for KB926C

PV: change to BEAD for EMI request

KB926QFC0_LQFP128_14X14

KBD CONN

CONN@ JP33

ACES_85201-26051

For EMI

KB Back Light Conn

JP48 ACES_85201-0405N

CONN@

EC DEBUG port

@ JP34 ACES_85205-0400

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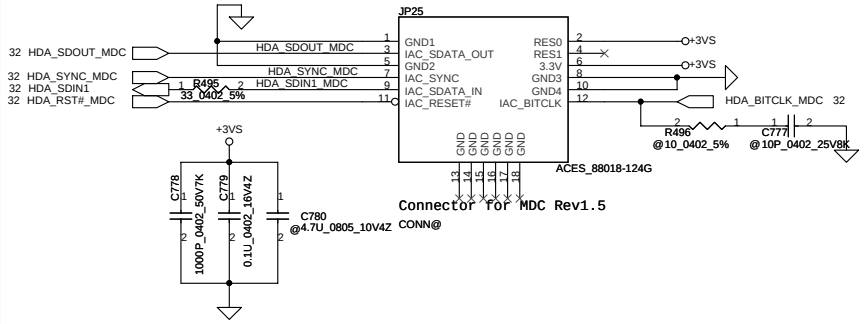
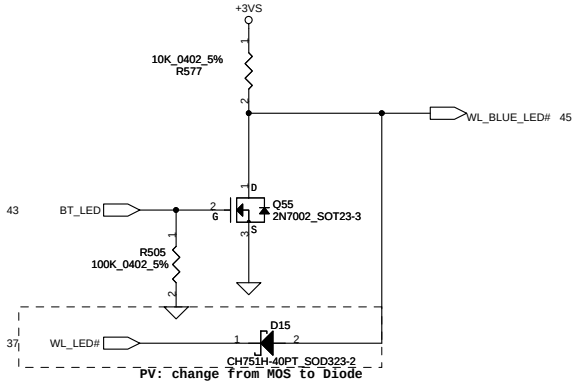
MDC 1.5 Conn.

Change type 4/25

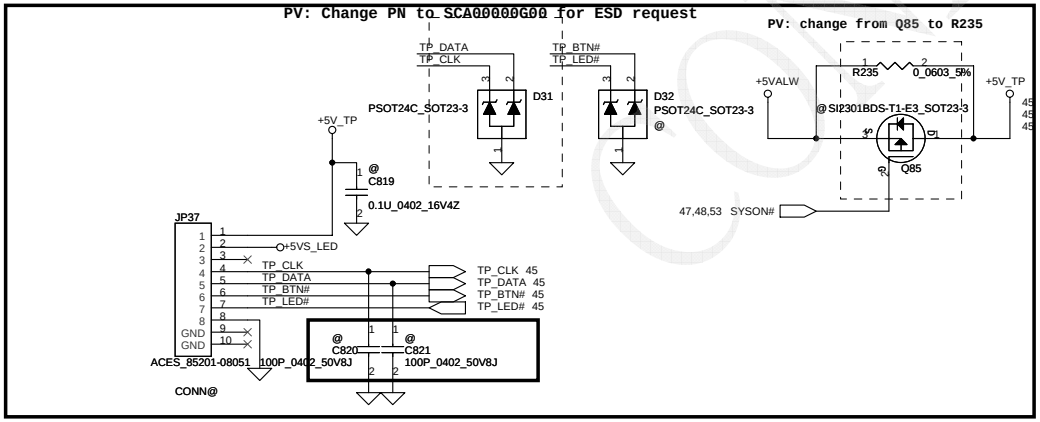


Connector for MDC Rev1.5



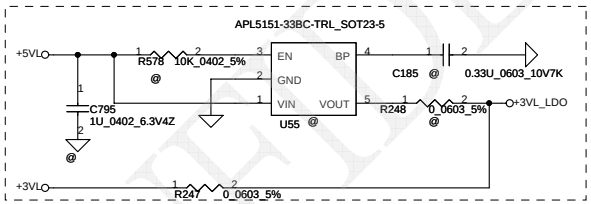
PV: change from MOS to Diode

T/P Board (Inculde T/P_ON/OFF)

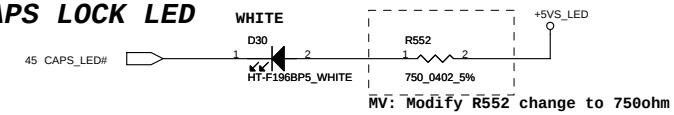


PV: change from Q85 to R235

PV: Add LDO for ENE cap board

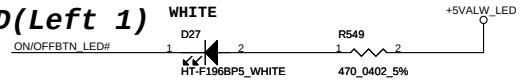


CAPS LOCK LED

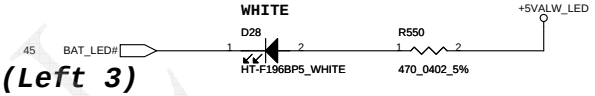


MV: Modify R552 change to 750ohm

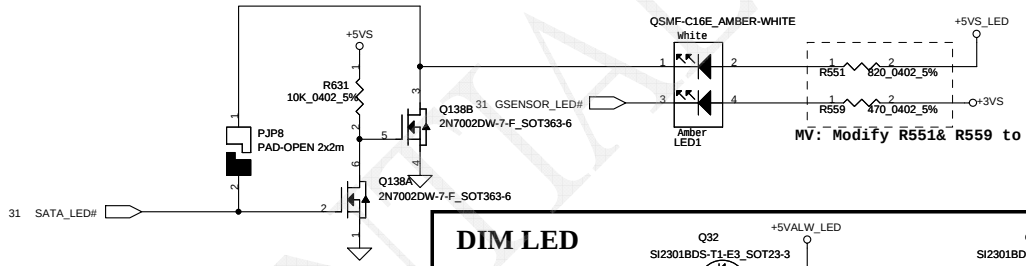
POWER LED(Left 1)



Battery Charge LED(Left 2)

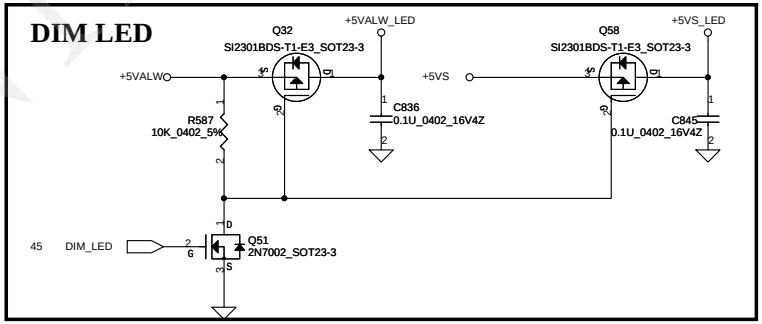


HDD LED(Left 3)



MV: Modify R551& R559 to 470 ohm

DIM LED



SI: Change to +3VL to support Qplay bottom boot in BATT mode

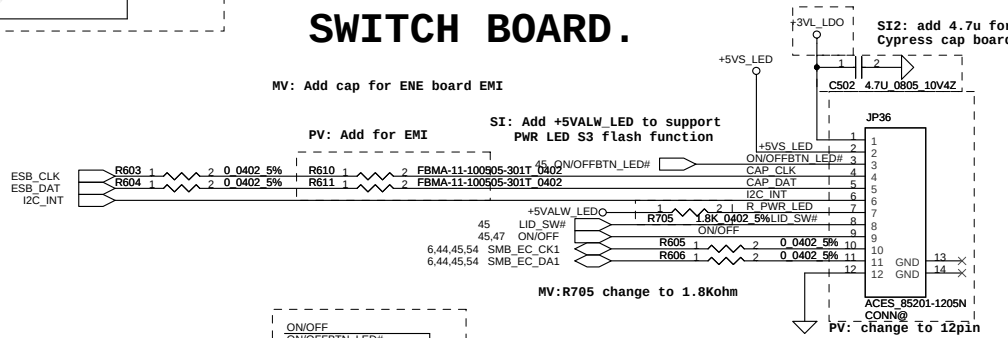
SWITCH BOARD.

MV: Add cap for ENE board EMI

PV: Add for EMI

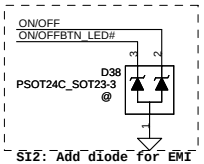
SI: Add +5VALW_LED to support PWR LED S3 flash function

SI2: add 4.7u for Cypress cap board

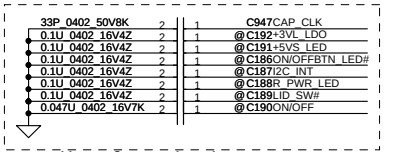


MV:R705 change to 1.8Kohm

PV: change to 12pin



SI2: Add diode for EMI



MV: Add cap for ENE board EMI

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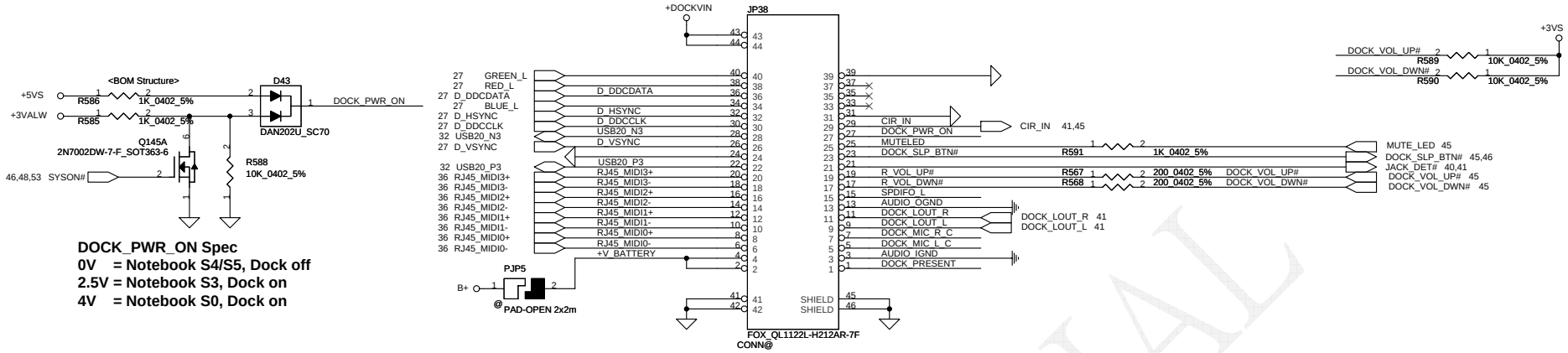
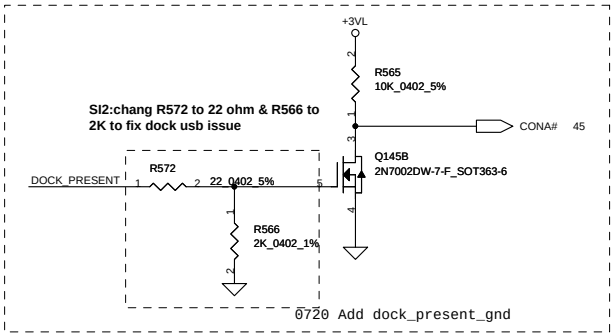
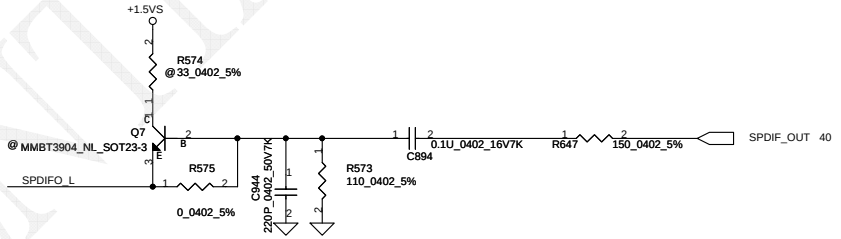
Atlas/ Saturn Dock

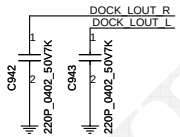


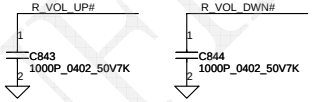
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

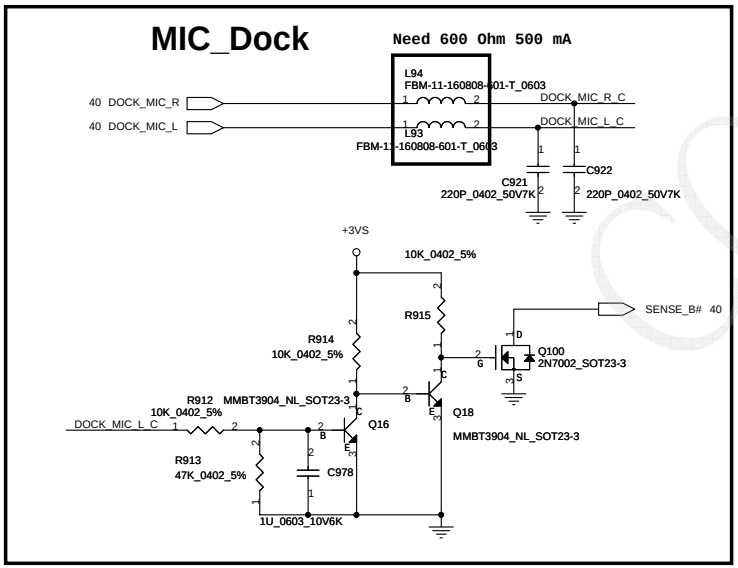
need change to reverse type connector











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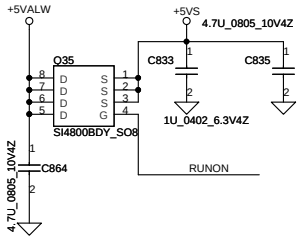
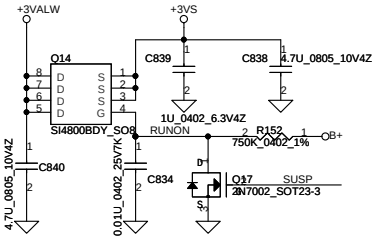
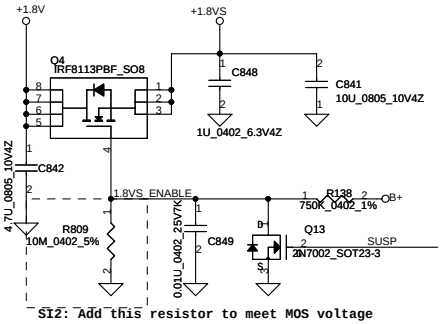
+5VALW TO +5VS



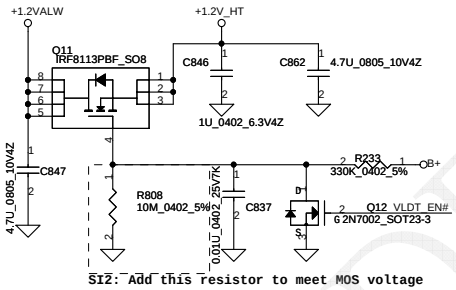
+3VALW TO +3VS

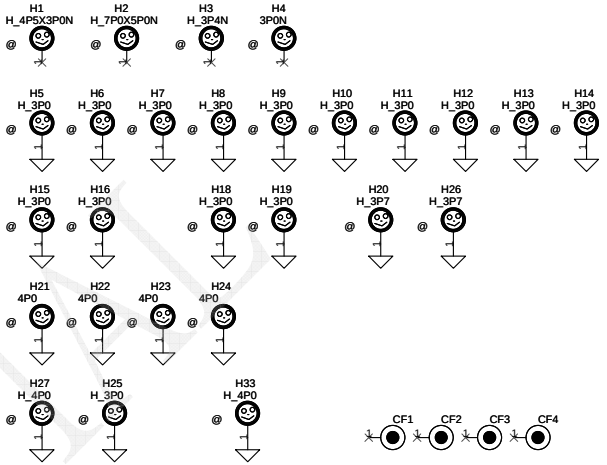


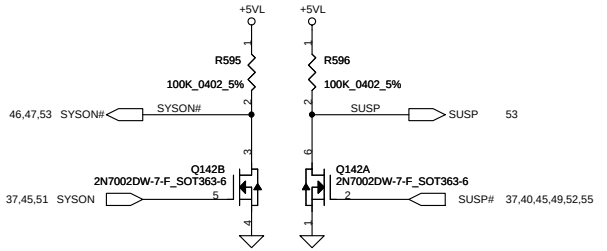
+1.8V TO +1.8VS



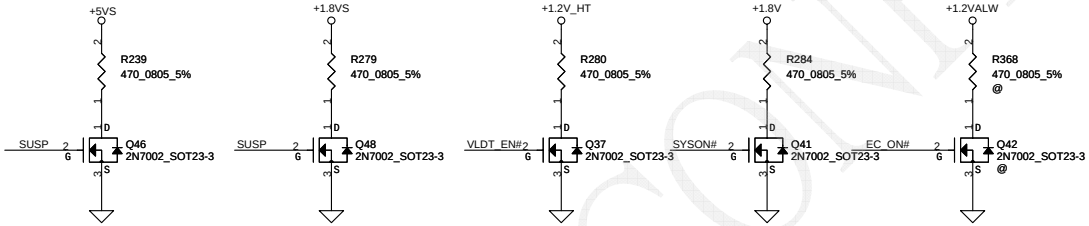
+1.2VALW TO +1.2V_HT

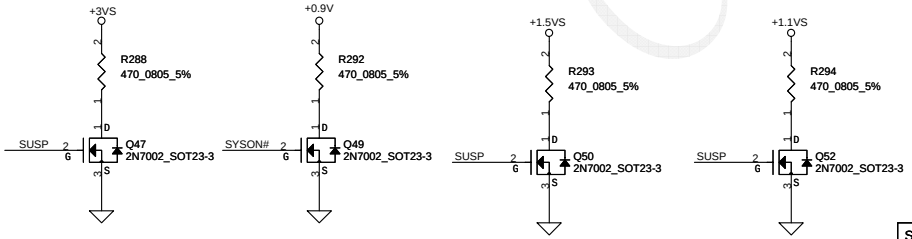


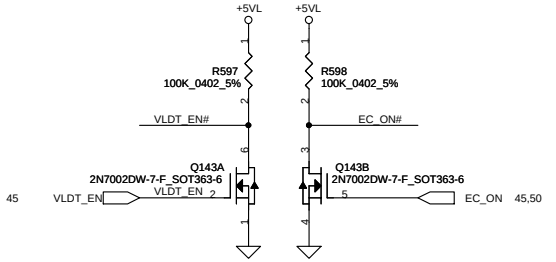




Discharge circuit







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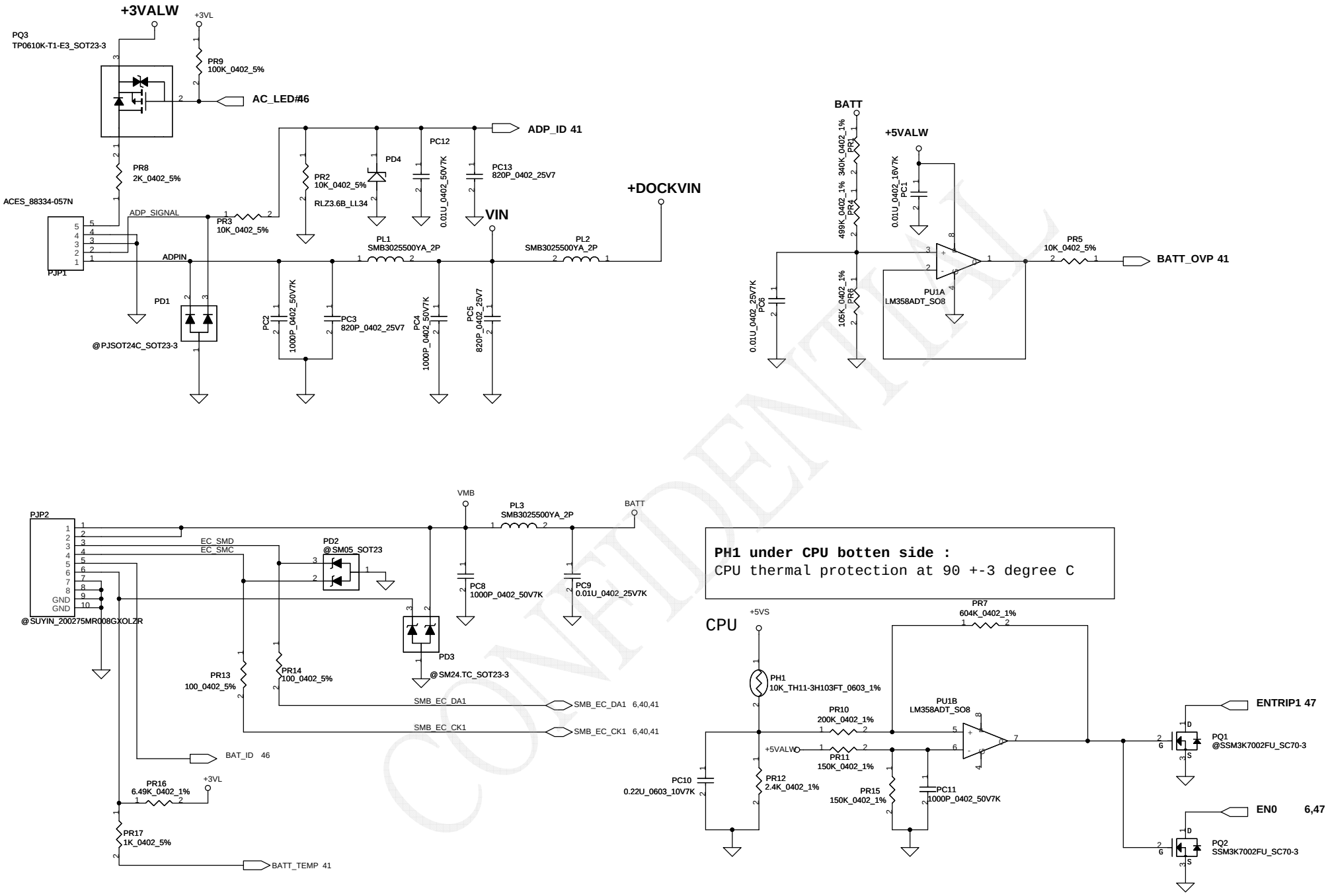

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Compal Electronics, Inc.			
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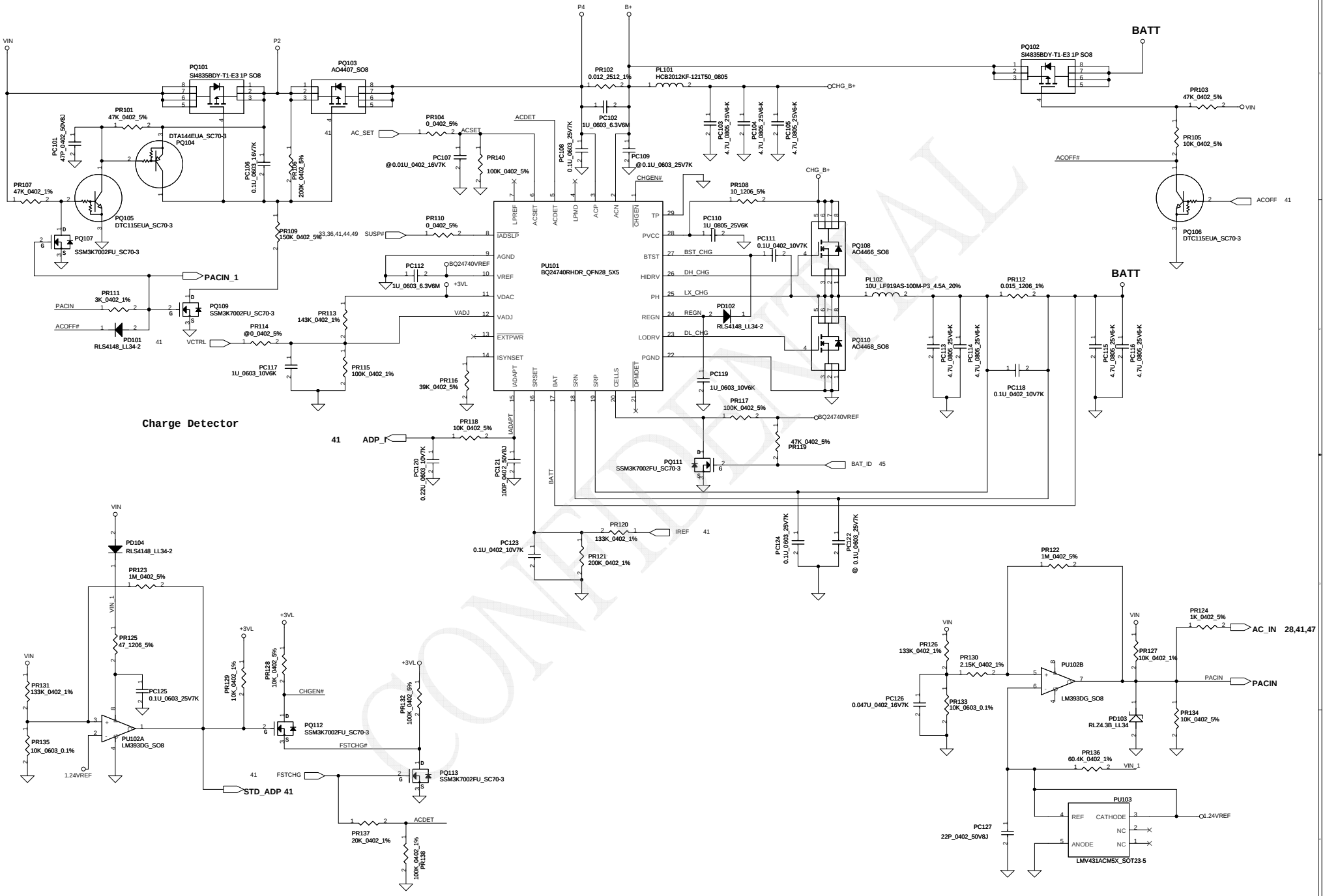

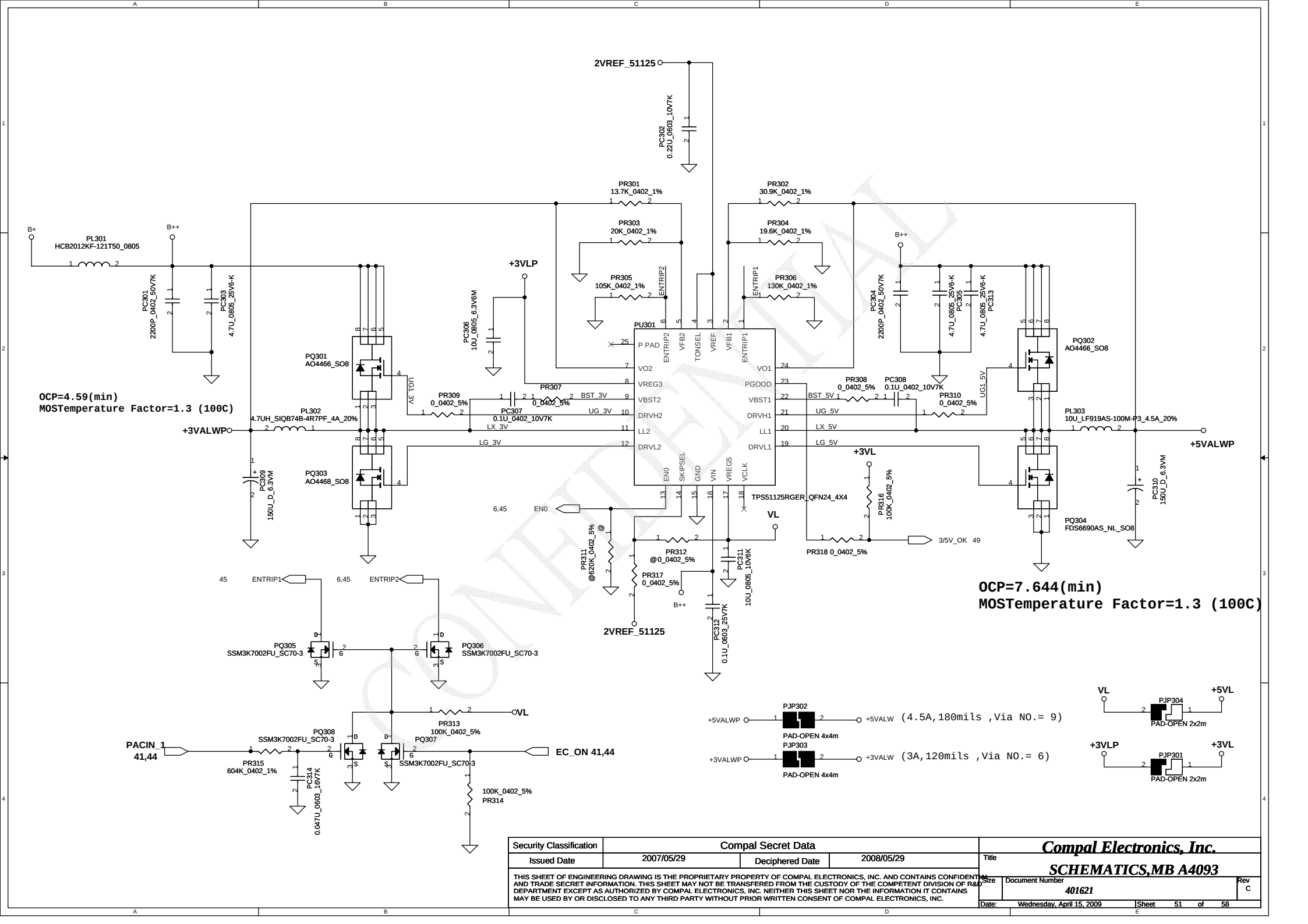

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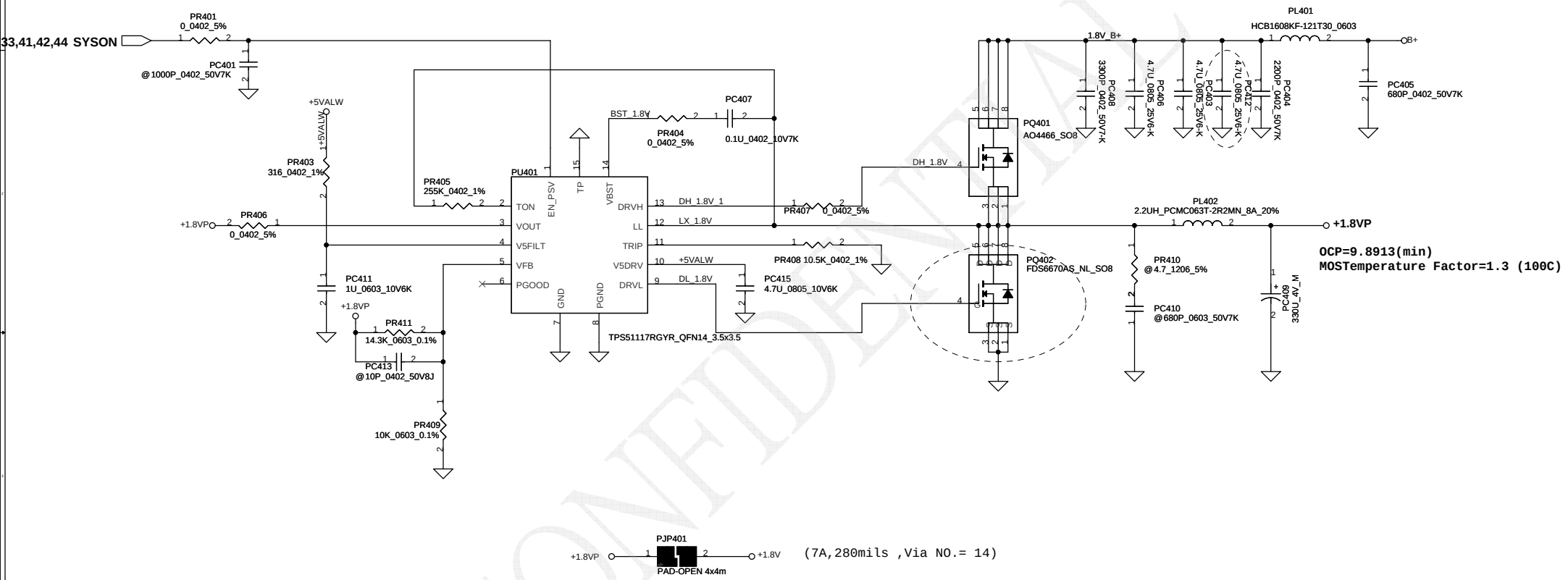

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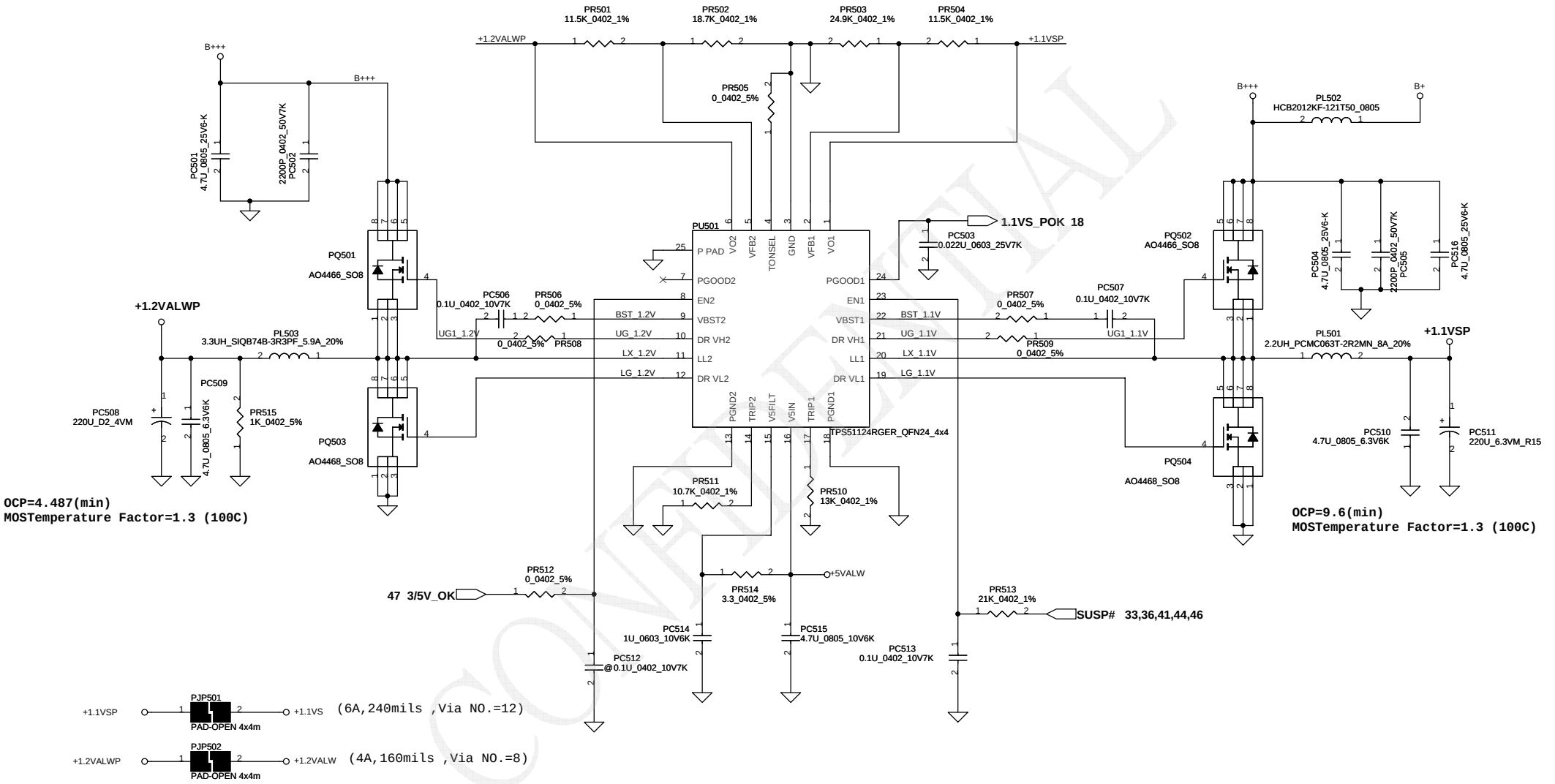

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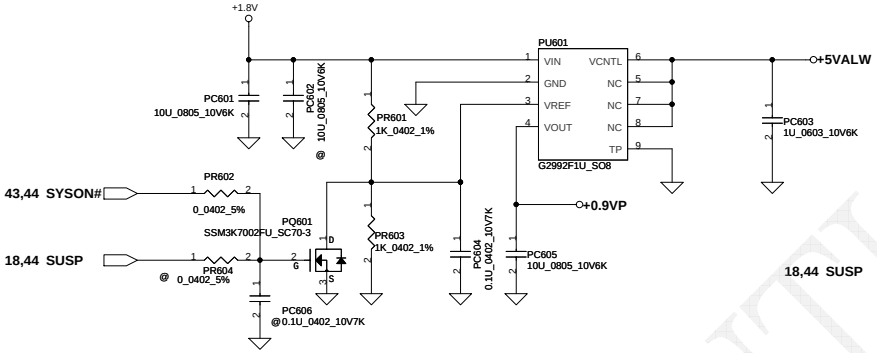

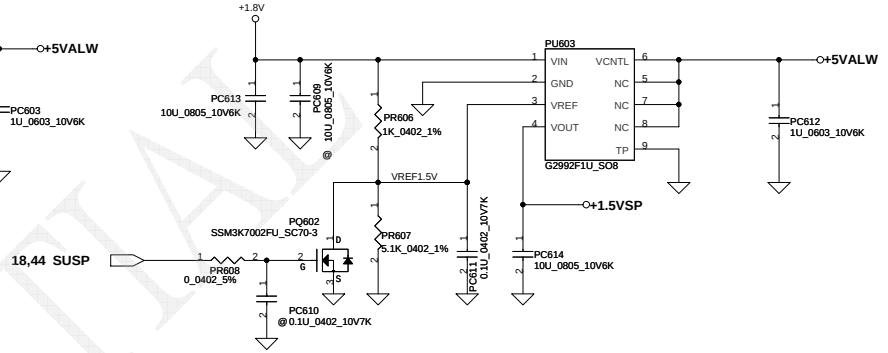

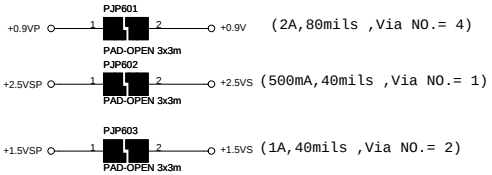

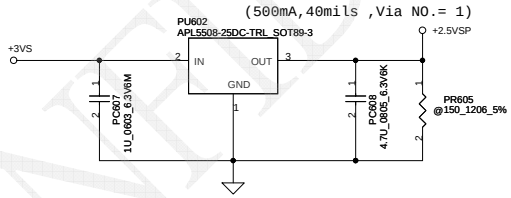

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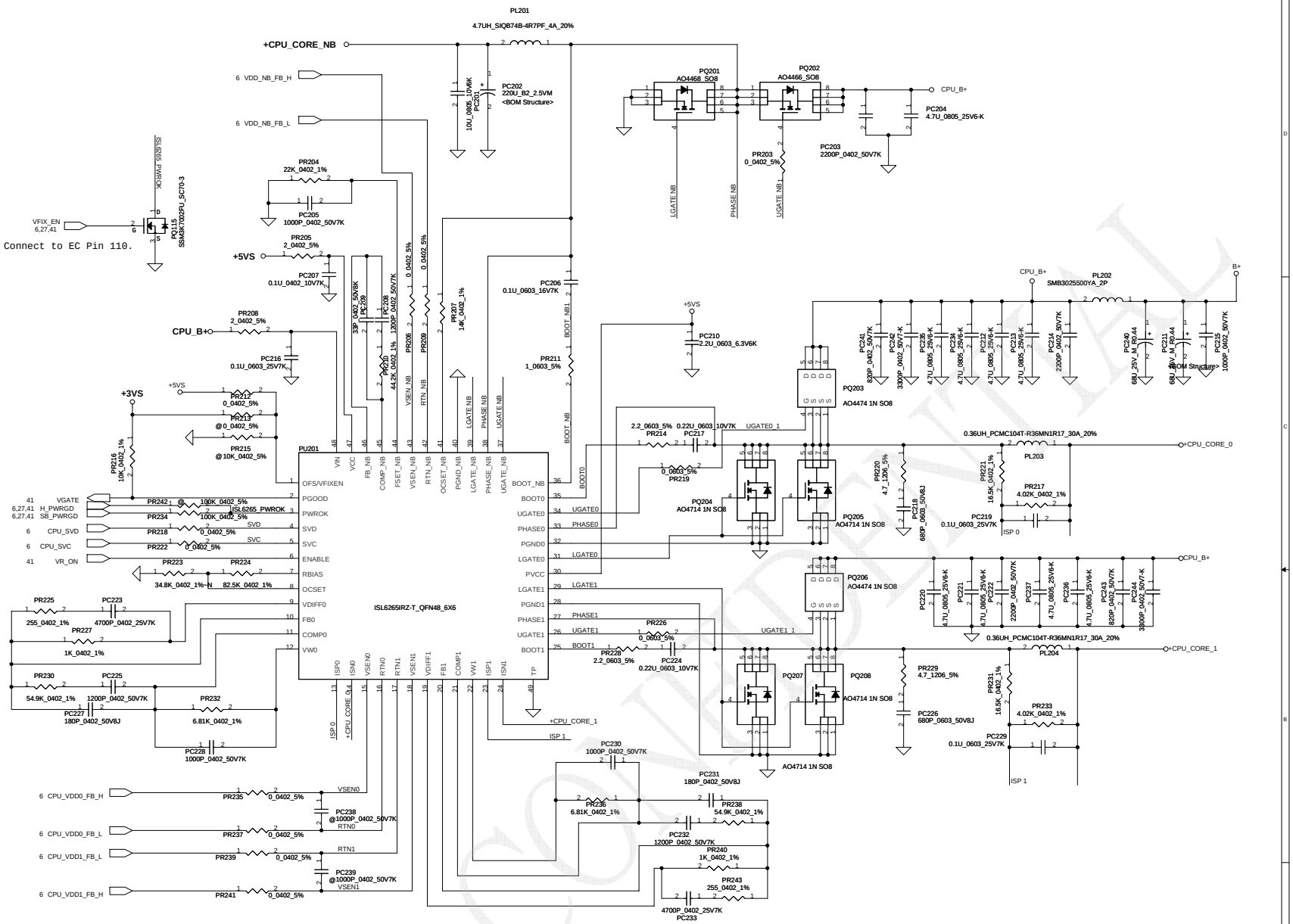

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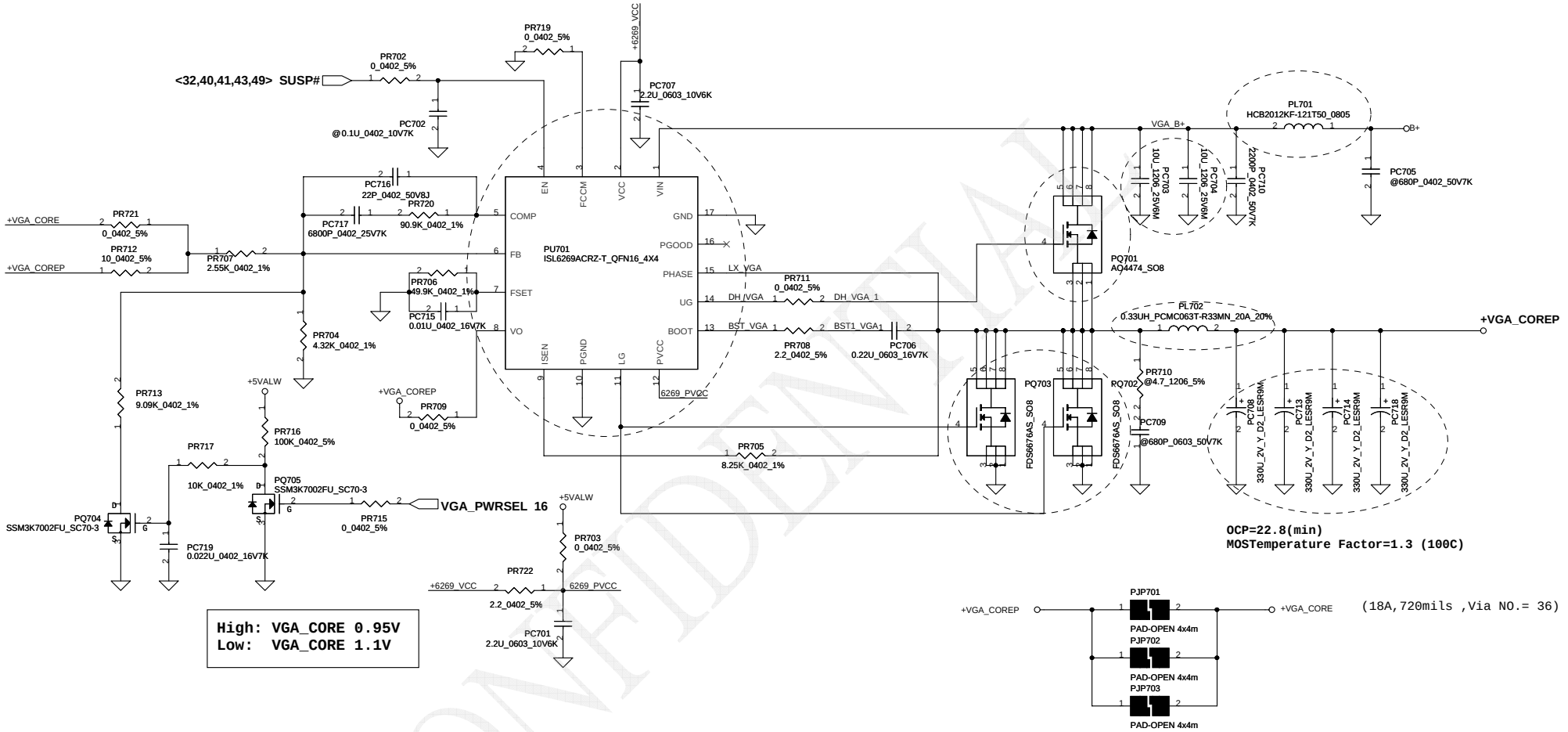

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Item	Modify List	PAGE	Fixed Issue and change item	M.B. Ver.
1	Remove Q23 (2N7002)	41	HP OUT For Docking	1.1
2	ADD R936 R937 (0 ohm)	41	HP OUT For Docking	1.1
3	Remove U5 (M82-S)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
4	Remove U54	15,16,17 18,19,20,21	change M82S TO M86M	1.1
5	Remove Q8(SI2301BDS)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
6	Remove Q9(2N7002)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
7	Remove R149 (240 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
8	Remove L32,L33 (0 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
9	Remove R42,R625,R630 (0 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
10	Remove R189 (100 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
11	Remove R131,R142 (1K ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
12	Remove R120,R130,R190,R197,R243,R244,R245,R246(10K ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
13	Remove R151 (10Kohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
14	Remove R145,R146,R147,R241,R242,R403 (4.7Kohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
15	Remove R159,R160,R165,R166(56 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
16	Remove R143,R144,R148,R150 (100 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
17	Remove R109 (1.27K ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
18	Remove R112 (150 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
19	Remove R108 (2K ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
18	Remove R1136 (249 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
20	Remove R119,R132 (499 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
21	Remove R155,R156,R157,R158,R161,R162,R163,R164 (4.99Kohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
22	Remove R135 (715 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
23	Remove R177 (75 ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
24	Remove C254,C255,C256,C257,C258,C259,C260,C261,C262,C263,C264,C265,C266,C267,C268,C269,C270,C271,C272,C273,C274,C275,C276,C277,C278,C279,C280,C281,C282,C283,C284,C285 (0.1U)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
25	Remove C478 (220U)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
26	Remove L23,L24,L25,L26,L27,L28,L29,L30,L31,L34,L35,L36,L37,L38,L39,L40,L41,R110,R115 (BLM18PG121SN1D)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
27	Remove C294,C295,C298,C299,C302,C303,C305,C307,C310,C315,C318,C319,C322,C330,C331,C332,C336,C337,C341,C351,C356,C359,C364,C368,C373,C380,C386,C390,C392,C395,C405,C406,C413,C414,C428,C429,C436,C437,C599 (10 U)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
28	Remove C287,C288,C290,C292,C297,C306,C308,C308,C311,C314,C317,C320,C323,C325,C328,C329,C339,C344,C358,C382,C391,C394,C397,C398,C400,C402,C403,C408,C409,C410,C411,C416,C417,C418,C419,C421,C423, C425,C426,C431,C432,C433,C434,C439,C440,C441,C442,C598 (0.1 U)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
29	Remove C286,C312,C338,C340,C342,C343,C345,C346,C352,C353,C354,C355,C360,C361,C362,C363,C369,C370,C371,C372,C374,C375,C376,C377,C387,C388,C393,C396,C289,C291,C293 C296,C301,C304,C309,C313,C316,C321,C324,C333,C334,C335,C347,C348,C349,C350,C357,C365,C366,C367,C378,C379,C381,C383,C384,C385,C389,C399,C401,C407,C415,C422,C424,C430,C438,C597(1U)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
30	Remove U12 (ADM1032ARMZ)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
31	Remove R330(4.7K ohm)	15,16,17 18,19,20,21	change M82S TO M86M	1.1
32	Remove C466 (0.1U)	38	Fix CR_LED	1.1
33	Remove C467 (2200P)	38	Fix CR_LED	1.1
34	Remove Q53(2N7002)	38	Fix XD_ALE	
35	ADD R933(0 ohm)			
36	ADD R127(10Kohm)			

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Item	Modify List	PAGE	Fixed Issue and change item	M.B. Ver.
1	ADD ":U6,UV7,U7,UV8,U8,UV9,U9,UV10 "(MEMARY)	P15~P25	change M82S TO M86M	1.1
2	ADDQ9 (2N7002)	P15~P25	change M82S TO M86M	1.1
3	ADD QV3(SI2301BDS)	P15~P25	change M82S TO M86M	1.1
4	ADD RV47(240 ohm)	P15~P25	change M82S TO M86M	1.1
5	ADD R42(0 ohm)	P15~P25	change M82S TO M86M	1.1
6	ADD RV19,RV44 (1K ohm)	P15~P25	change M82S TO M86M	1.1
7	ADD RV96,RV100,RV72,RV73,RV74,RV75,RV76,RV77,RV78,RV79,RV92,RV93,RV94,RV95,RV97,RV99,RV101,RV107,RV108,RV7,RV9,RV10,RV11,RV12,RV13,RV14,RV16,RV17,RV18,RV33,RV98,RV102(10K ohm)	P15~P25	change M82S TO M86M	1.1
8	ADD RV30,RV34(100K ohm)	P15~P25	change M82S TO M86M	1.1
9	ADD RV103,RV104,RV45,RV46,R403(4.7K ohm)	P15~P25	change M82S TO M86M	1.1
10	ADD RV36,RV37,RV38,RV39,RV40,RV41,RV42,RV43(100 ohm)	P15~P25	change M82S TO M86M	1.1
11	ADD RV6 (1.27Kohm)	P15~P25	change M82S TO M86M	1.1
12	ADD RV25,RV26,RV27,RV8(150 ohm)	P15~P25	change M82S TO M86M	1.1
13	ADD RV5(2K ohm)	P15~P25	change M82S TO M86M	1.1
14	ADD RV23,RV15,RV22(499 ohm)	P15~P25	change M82S TO M86M	1.1
15	ADD RV60,RV61,RV62,RV63,RV66,RV67,RV68,RV69,RV54,RV55,RV56,RV57,RV48,RV49,RV50,RV51(4.99K ohm)	P15~P25	change M82S TO M86M	1.1
16	ADD RV24(715 ohm)	P15~P25	change M82S TO M86M	1.1
17	ADD RV28(75 ohm)	P15~P25	change M82S TO M86M	1.1
18	ADD YV1(CRYSTAL 27MHZ)	P15~P25	change M82S TO M86M	1.1
19	ADD RV103,RV104,RV45,RV46,R403(4.7K ohm)	P15~P25	change M82S TO M86M	1.1
20	ADD LV1,LV2,LV3,LV4,LV5,LV6,LV7,LV8,LV9,LV10,LV11,LV12,LV13,LV14,LV15,LV16,LV17,LV18,LV19,LV21,LV22,LV23,LV24,LV25 (MURATA BLM18PG121SN1D)	P15~P25	change M82S TO M86M	1.1
21	ADDCV226,CV227,CV234,CV235,CV249,CV250,CV257,CV258,CV203,CV204,CV211,CV212,CV180,CV181,CV188,CV189,CV42,CV45,CV48,CV52,CV53,CV56,CV59,CV64,CV67,CV68,CV71,CV76,CV84,CV85,CV90,CV92,CV95,CV97,CV99,CV101,CV108, CV117,CV119,CV131,CV132,CV136,CV140,CV145,CV149,CV157,CV165,CV166,CV169,CV173(10u)	P15~P25	change M82S TO M86M	1.1
22	ADD CV80,CV244,CV229,CV230,CV231,CV232,CV237,CV238,CV239,CV240,CV242,CV246,CV247,CV252,CV253,CV254,CV255,CV260,CV261,CV262,CV263,CV265,CV267,CV269,CV270,CV206,CV207,CV208,CV209,CV214,CV215,CV216, CV217,CV219,CV221,CV223,CV224,CV196,CV183,CV184,CV185,CV186,CV191,CV192,CV193,CV194,CV198,CV200,CV201,CV44,CV46,CV49,CV50,CV55,CV58,CV60,CV62,CV66,CV69,CV72,CV75,CV79,CV83, CV87,CV88,CV106,CV114,CV120,CV125,CV159,CV168,CV171,CV172,CV175,CV176,CV177,CV178,CV179,CV272(0.1u)	P15~P25	change M82S TO M86M change M82S TO M86M	1.1 1.1
23	ADD CV77,CV78(22P)	P15~P25	change M82S TO M86M	1.1
24	ADD CV273 (2200P)	P15~P25	change M82S TO M86M	1.1
25	ADDCV233,CV241,CV256,CV264,CV210,CV218,CV187,CV195(0.01U)	P15~P25	change M82S TO M86M	1.1
26	ADD CV245,CV228,CV236,CV243,CV251,CV259,CV266,CV268,CV205,CV213,CV220,CV222,CV197,CV182,CV190,CV199,CV41,CV43,CV47,CV51,CV57,CV63,CV65,CV70,CV73,CV74,CV82,CV86,CV89,CV93,CV96,CV98,CV100,CV103,CV104, CV105,CV107,CV109,CV111,CV113,CV118,CV121,CV135,CV139,CV144,CV162,CV163,CV164,CV54,CV61,CV94,CV102,CV110,CV112,CV115,CV116,CV123,CV124,CV126,CV127,CV129,CV130,CV133,CV134,CV137,CV138,CV141,CV142, CV146,CV147,CV150,CV151,CV153,CV154,CV155,CV156,CV158,CV160,CV161,CV167,CV170,CV174(75 ohm) ADD RV28(1U)	P15~P25	change M82S TO M86M change M82S TO M86M	1.1 1.1
27	ADD CV9,CV10,CV11,CV12,CV13,CV14,CV15,CV16,CV17,CV18,CV19,CV20,CV21,CV22,CV23,CV24,CV25,CV26,CV27,CV28,CV29,CV30,CV31,CV32,CV33,CV34,CV35,CV36,CV37,CV38,CV39,CV40 (0.1U)	P15~P25	change M82S TO M86M	1.1
28	ADD CV122,CV91,CV128(330U)	P15~P25	change M82S TO M86M	1.1
PV				
1	Change RV30 100K to 100 ohm	P16	About GBU 27MHz	
2	Change PR702 4.7K to 0 ohm	P55	About GBU 3V delay time	
3	del PC702 0.1 U	P55	About GBU 3V delay time	
4	change NET DQMA#4 TO U8 F3 Pin	P22	about GBU A chanel VRAM	
5	change NET DQMA#5 TO U8 B3 Pin	P22	about GBU A chanel VRAM	
6	Change NET QSA4 QSA#4 TO U8 F7,E8 PIN	P22	about GBU A chanel VRAM	
7	Change NET QSA5 QSA#5TO U8 B7,A8 PIN	P22	about GBU A chanel VRAM	
8	change NET DQMA#7 TO U8 F3 Pin	P22	about GBU A chanel VRAM	
9	change NET DQMA#6 TO U8 B3 Pin	P22	about GBU A chanel VRAM	
10	Change NET QSA7 QSA#7TO U8 F7,E8 PIN	P22	about GBU A chanel VRAM	
11	Change NET QSA6 QSA#6 TO U8 B7,A8 PIN	P22	about GBU A chanel VRAM	
12	Change UV12 BOM SA010320120 to SA010320110	P25	about GBU Thermal Sensor	
13	Modify R237,R238,R176,R209 PULL +3VS TO +3VS_DELAY	P27 P29	Change power plan	
14	ADD LV20,CV152,CV148,CV143	P18	ADD M86M +VDDR5 POWER	

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