

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

2007-08-02

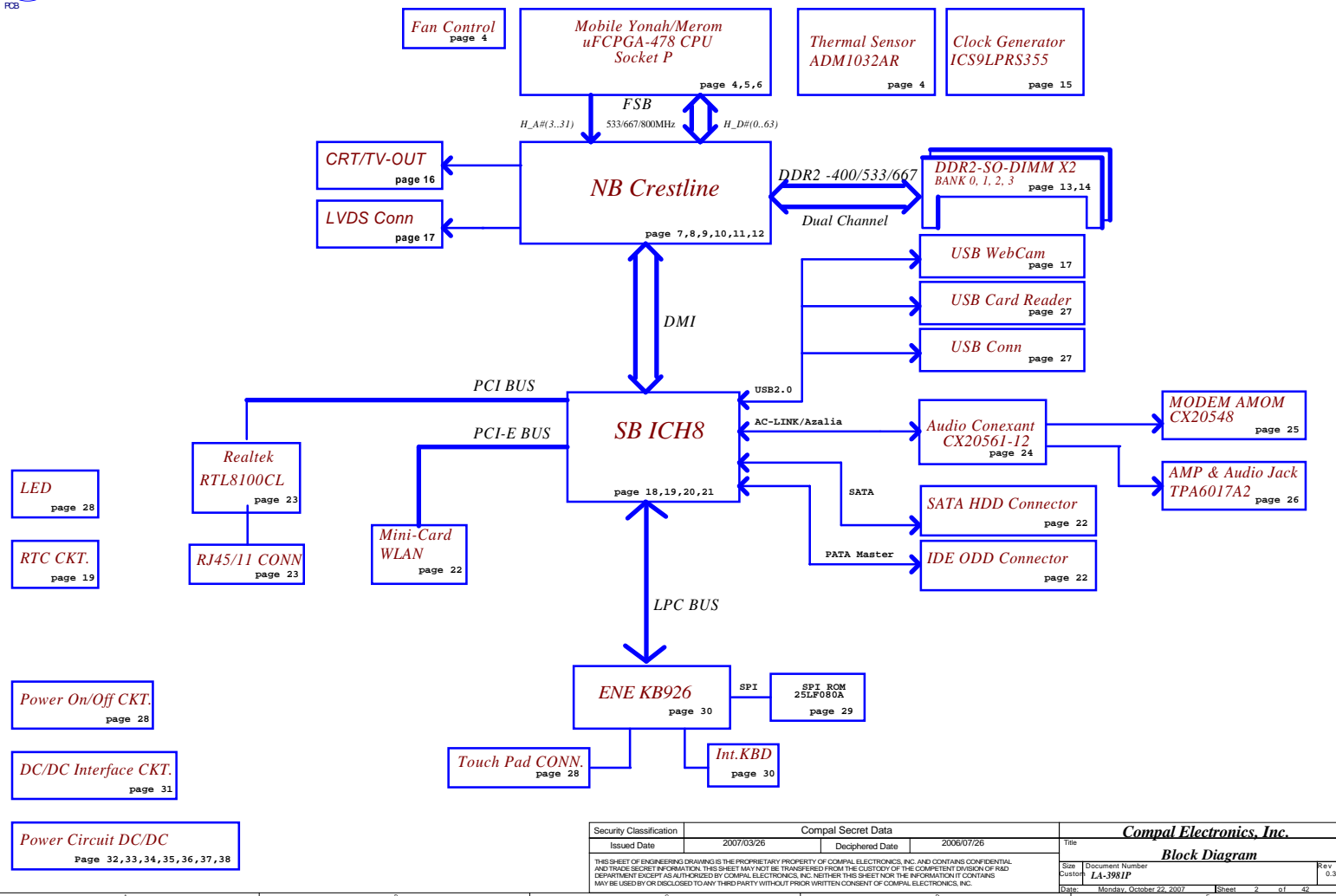
REV: 0.2

Security Classification	Compal Secret Data		Title		<i>Compal Electronics, Inc.</i>	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	Cover Sheet		
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LEON 1.0 (Merom +Crestline+ICH8)



PCB



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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
s0	O	O	O	O
s1	O	O	O	O
s3	O	O	O	X
s5 s4/AC	O	O	X	X
s5 s4/ Battery only	O	X	X	X
s5 s4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

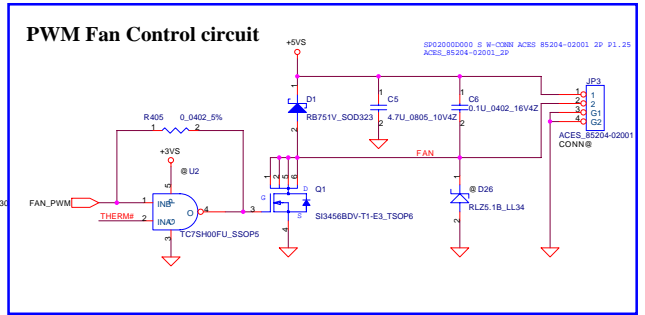
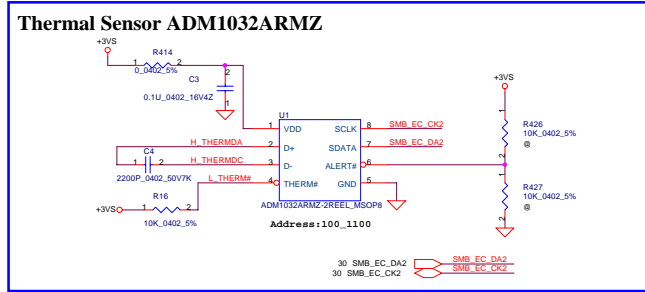
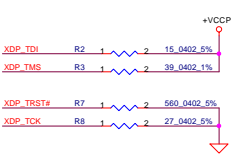
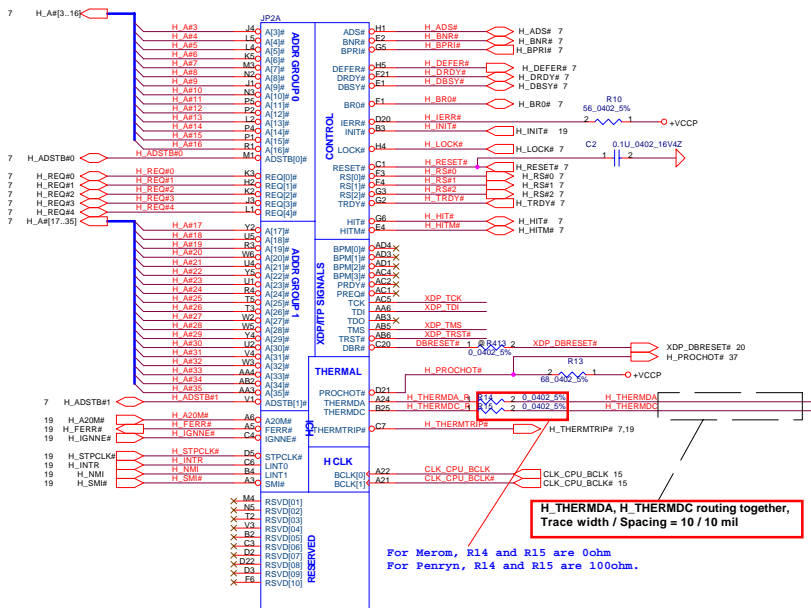
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADML022	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43151732L01(965GM) & 443151732L02(960GML) with card reader

BOM: 43151732L03(965GM) & 43151732L04(960GML) without card reader

Jump-Short: PJP?

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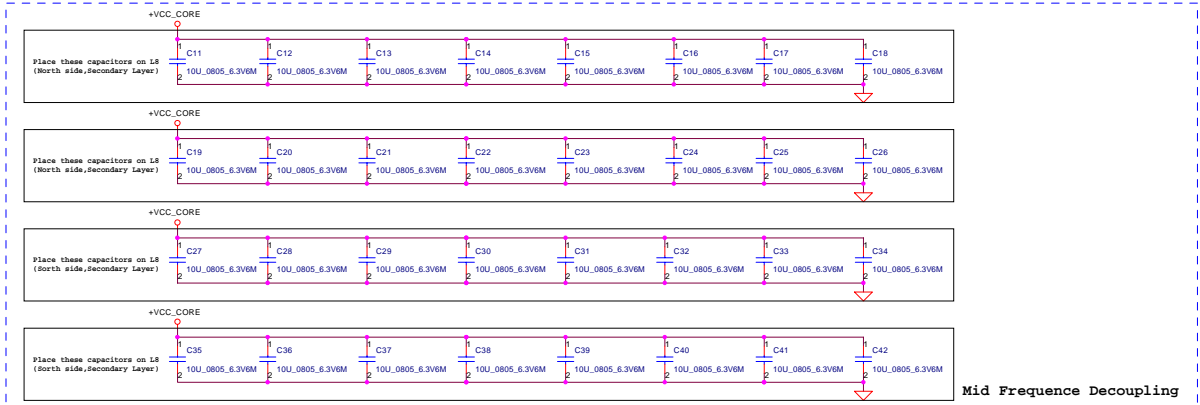


**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

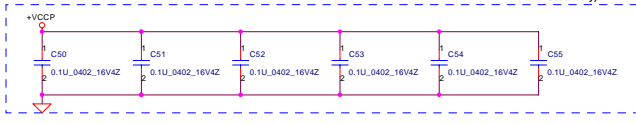
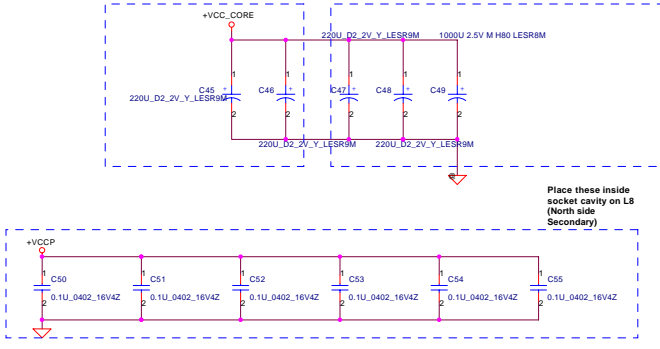
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JP2D			
A4	VSS1001	VSS1080	P8
A5	VSS1002	VSS1081	P21
A6	VSS1003	VSS1082	P22
A11	VSS1004	VSS1083	B2
A14	VSS1005	VSS1084	B22
A16	VSS1006	VSS1085	B22
A19	VSS1007	VSS1086	B22
A22	VSS1008	VSS1087	T1
AF2	VSS1009	VSS1088	T1
BB	VSS1010	VSS1089	T2
BB	VSS1011	VSS1090	T2
B11	VSS1012	VSS1091	T26
B13	VSS1013	VSS1092	T26
B16	VSS1014	VSS1093	L16
B19	VSS1015	VSS1094	L16
B21	VSS1016	VSS1095	L24
B24	VSS1017	VSS1096	L24
C2	VSS1018	VSS1097	U5
C3	VSS1019	VSS1098	U22
C14	VSS1020	VSS1099	U22
C19	VSS1021	VSS1100	W4
C16	VSS1022	VSS1101	W4
C19	VSS1023	VSS1102	W22
C2	VSS1024	VSS1103	W22
C22	VSS1025	VSS1104	V3
C22	VSS1026	VSS1105	V3
D4	VSS1027	VSS1106	V24
D8	VSS1028	VSS1107	V24
D11	VSS1029	VSS1108	A2
D13	VSS1030	VSS1109	A2
D18	VSS1031	VSS1110	AA1
D19	VSS1032	VSS1111	AA1
D23	VSS1033	VSS1112	AA14
D23	VSS1034	VSS1113	AA16
D28	VSS1035	VSS1114	AA19
E3	VSS1036	VSS1115	AA22
E8	VSS1037	VSS1116	AA25
E8	VSS1038	VSS1117	AA25
E11	VSS1039	VSS1118	AB1
E16	VSS1040	VSS1119	AB4
E16	VSS1041	VSS1120	AB4
E19	VSS1042	VSS1121	AB11
E21	VSS1043	VSS1122	AB13
E24	VSS1044	VSS1123	AB16
F4	VSS1045	VSS1124	AB19
F8	VSS1046	VSS1125	AB26
F8	VSS1047	VSS1126	AB26
F13	VSS1048	VSS1127	AC2
F16	VSS1049	VSS1128	AC2
F19	VSS1050	VSS1129	AC11
F22	VSS1051	VSS1130	AC14
F22	VSS1052	VSS1131	AC16
F25	VSS1053	VSS1132	AC19
G4	VSS1054	VSS1133	AC21
G1	VSS1055	VSS1134	AC24
G3	VSS1056	VSS1135	AD2
G28	VSS1057	VSS1136	AD5
H8	VSS1058	VSS1137	AD8
H8	VSS1059	VSS1138	AD11
H21	VSS1060	VSS1139	AD13
H24	VSS1061	VSS1140	AD16
J2	VSS1062	VSS1141	AD19
J2	VSS1063	VSS1142	AD22
J22	VSS1064	VSS1143	AD25
J5	VSS1065	VSS1144	AE1
K1	VSS1066	VSS1145	AE4
K23	VSS1067	VSS1146	AE8
K28	VSS1068	VSS1147	AE11
L3	VSS1069	VSS1148	AE14
L6	VSS1070	VSS1149	AE16
L1	VSS1071	VSS1150	AE19
L24	VSS1072	VSS1151	AE23
M2	VSS1073	VSS1152	AE26
M2	VSS1074	VSS1153	AE26
M22	VSS1075	VSS1154	AF2
M28	VSS1076	VSS1155	AF5
N1	VSS1077	VSS1156	AF11
N4	VSS1078	VSS1157	AF13
N23	VSS1079	VSS1158	AF16
N23	VSS1080	VSS1159	AF19
P1	VSS1081	VSS1160	AF21
	VSS1081	VSS1160	A22
	VSS1081	VSS1160	A22
	VSS1081	VSS1160	AE26

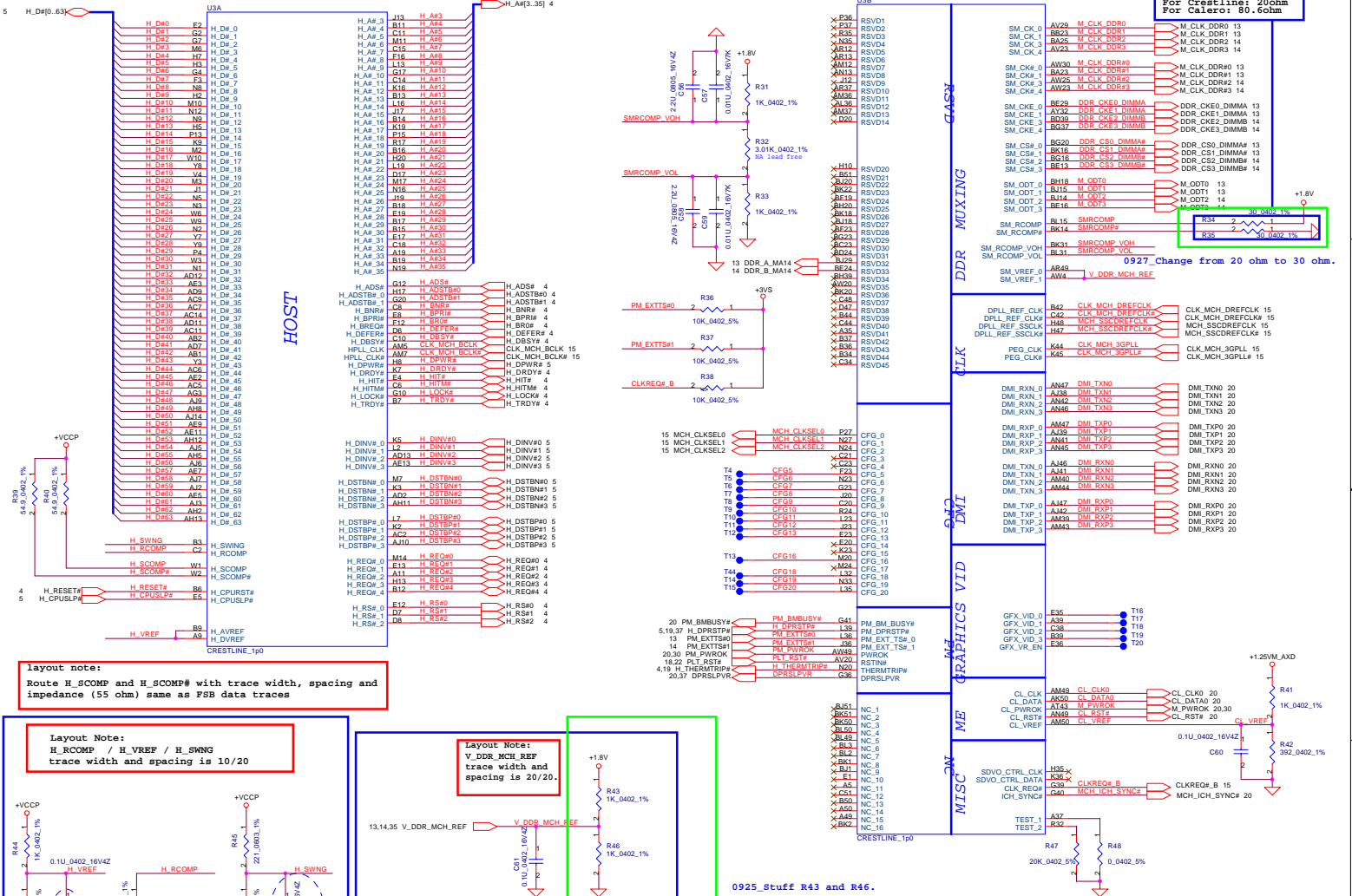


Mid Frequency Decoupling

Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



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For Crestline: 20ohm
For Calero: 80, 60ohm

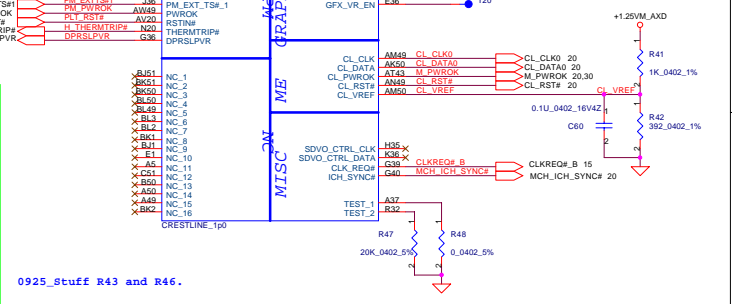
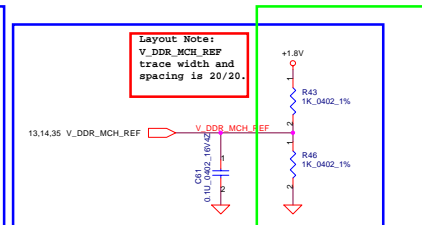
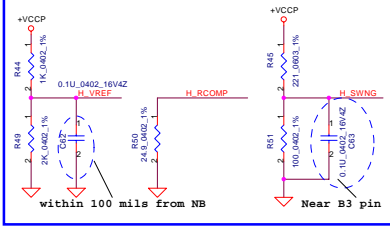
0927_Change from 20 ohm to 30 ohm.

layout note:
Route H_SCOMP and H_SCMP# with trace width, spacing and impedance (55 ohm) same as #8 data traces

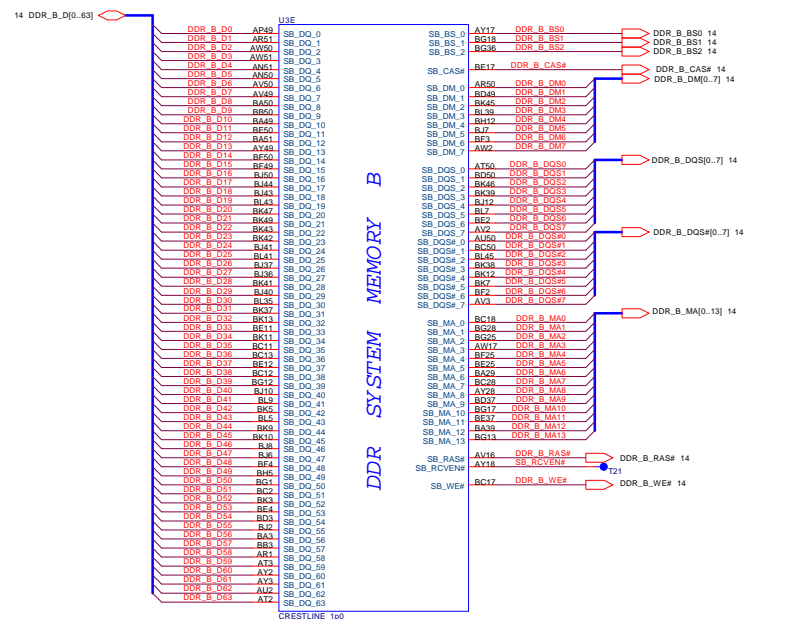
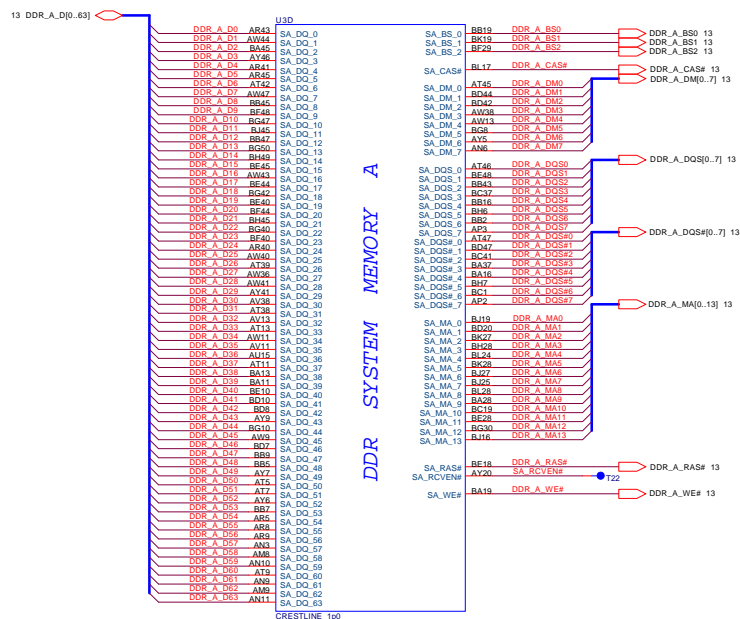
Layout Note:
H_RCMP / H_VREF / H_SWNG trace width and spacing is 10/20

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.

0925_Stuff R43 and R46.



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CRESTLINE_1p0

CRESTLINE_1p0

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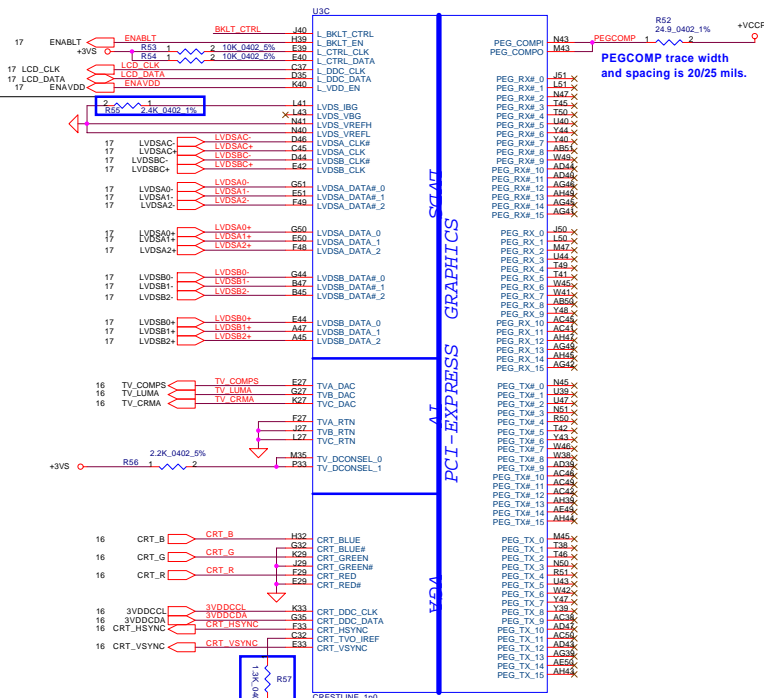
Compal Electronics, Inc.
CRESTLINE((2/6)-DDR2 A/B CH
 LA-3901P
 Monday, October 22, 2007

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

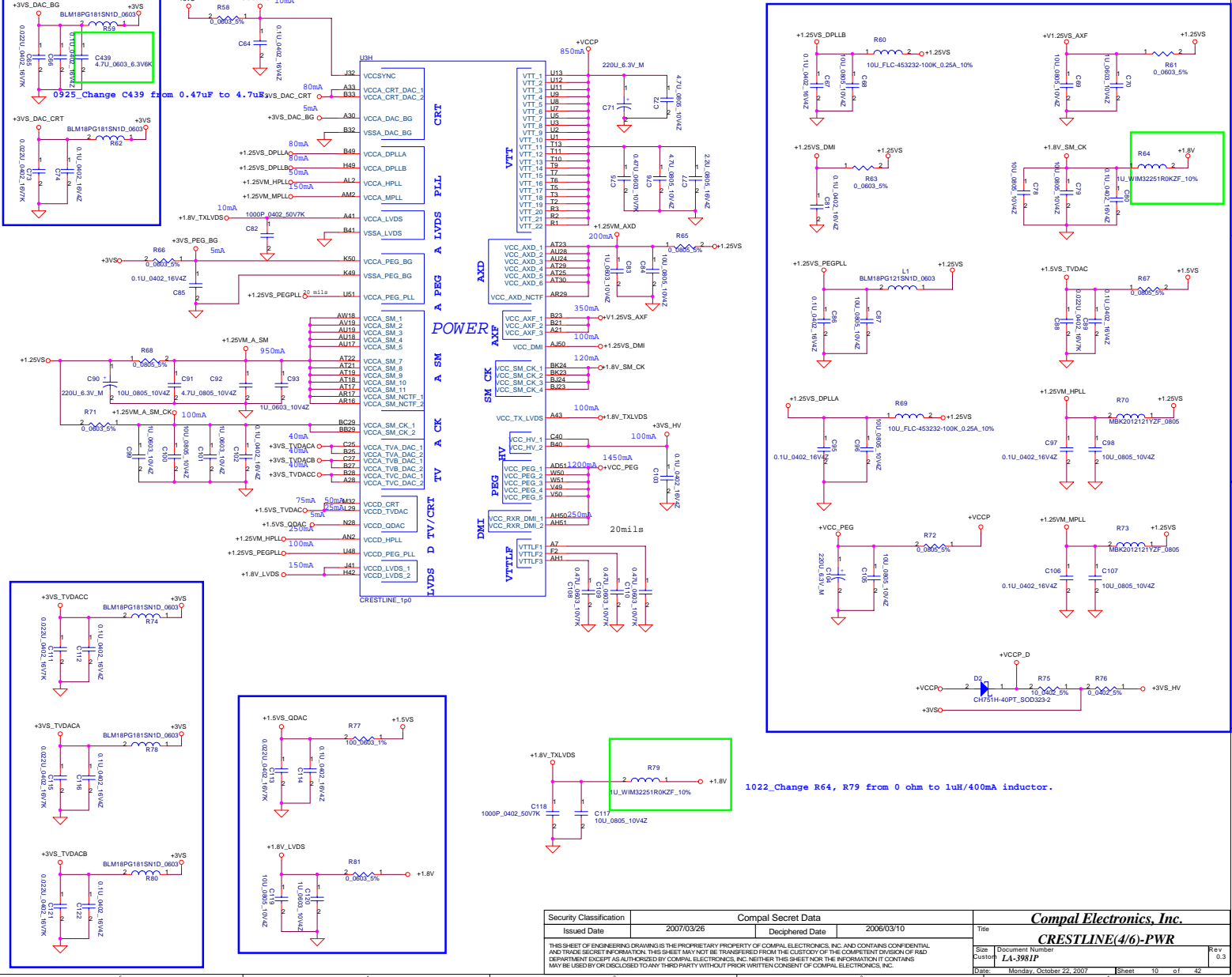
CFG[17:13] have internal pull up
CFG[19:18] have internal pull down

For Crestline: 2.4kohm
For Calero: 1.5kohm

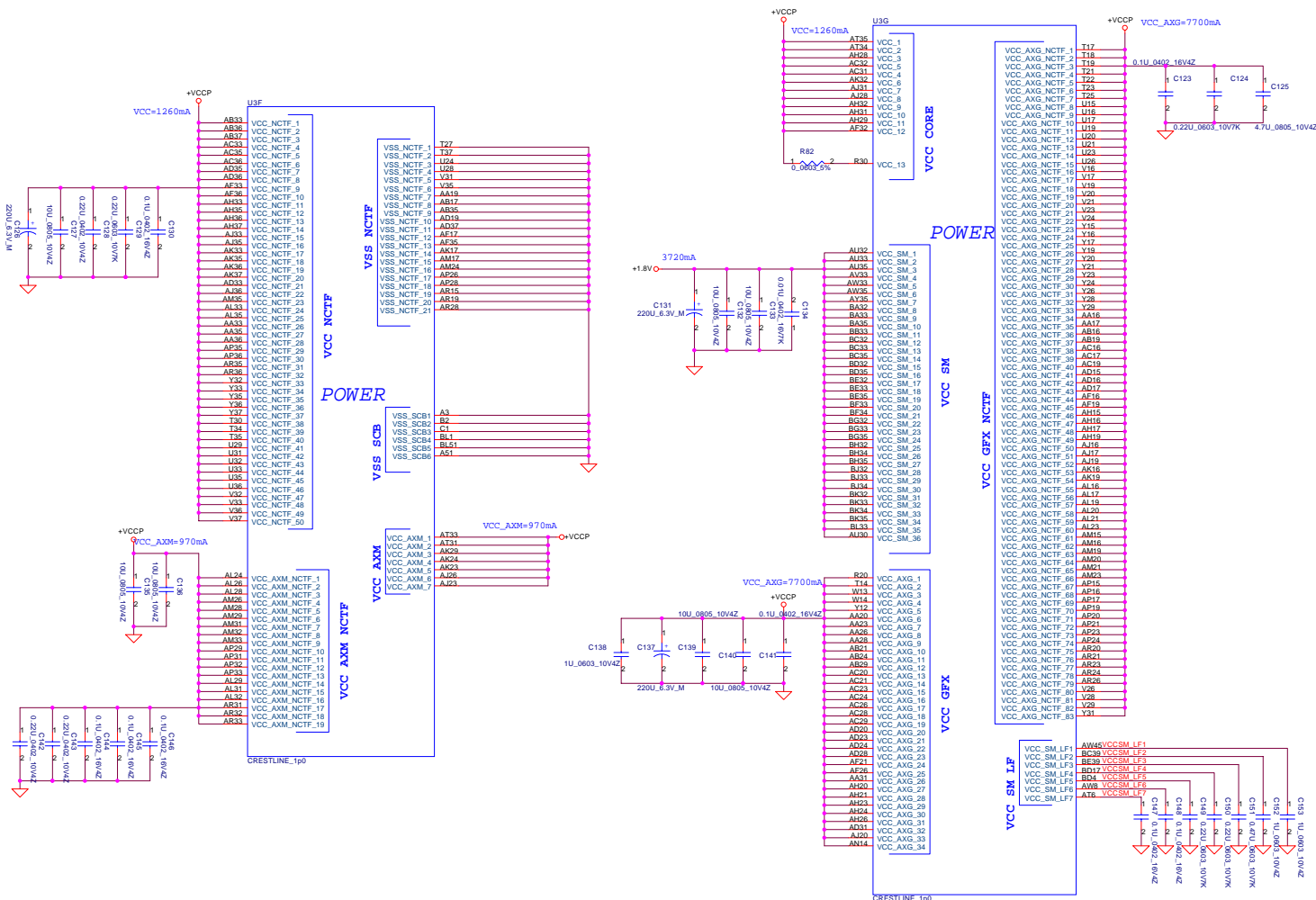


For Crestline: 1.3kohm
For Calero: 255ohm

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Compal Electronics, Inc.
CRESTLINE((5/6)-PWR/GND

Rev 0.3

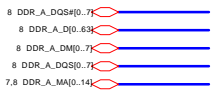
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A13	VSS_1	AW24	
A15	VSS_2	AW29	
A17	VSS_3	AW32	
A2	VSS_4	AW5	
AA21	VSS_5	AW7	
AA24	VSS_6	AY10	
AA25	VSS_7	AY24	
AB20	VSS_8	AY37	
AB23	VSS_9	AY42	
AB26	VSS_10	AY43	
AB28	VSS_11	AY45	
AB31	VSS_12	AY47	
AC10	VSS_13	AY50	
AC13	VSS_14	B0	
AC1	VSS_15	B20	
AC2	VSS_16	B29	
AC43	VSS_17	B29	
AC47	VSS_18	B32	
AD1	VSS_19	B33	
AD21	VSS_20	B38	
AD26	VSS_21	B40	
AD29	VSS_22	B46	
AD3	VSS_23	B47	
AD41	VSS_24	B8	
AD49	VSS_25	VSS_124	
AD5	VSS_26	VSS_125	
AD50	VSS_27	VSS_128	
AE10	VSS_28	VSS_127	
AE3	VSS_29	BA24	
AE14	VSS_30	BB12	
AE1	VSS_31	BB25	
AE2	VSS_32	BB40	
AF20	VSS_33	BB44	
AF23	VSS_34	BB48	
AF24	VSS_35	BB8	
AF31	VSS_36	BC16	
AG2	VSS_37	BC24	
AG38	VSS_38	BC25	
AG43	VSS_39	BC36	
AG47	VSS_40	BC40	
AH3	VSS_41	CA	
AH9	VSS_42	BD13	
AH41	VSS_43	BD2	
AH41	VSS_44	BD28	
AH7	VSS_45	BD45	
AI9	VSS_46	BD58	
AJ11	VSS_47	BD6	
AJ13	VSS_48	BE1	
AJ21	VSS_49	BE19	
AJ24	VSS_50	BE2	
AJ29	VSS_51	BE30	
AJ32	VSS_52	BE47	
AJ43	VSS_53	BE51	
AJ45	VSS_54	BE5	
AJ55	VSS_55	BE12	
AK20	VSS_56	BE16	
AK21	VSS_57	BE36	
AK28	VSS_58	BE19	
AK29	VSS_59	BE5	
AK31	VSS_60	BE54	
AL1	VSS_61	BG3	
AL1	VSS_62	BG39	
AM11	VSS_63	BG48	
AM13	VSS_64	BG5	
AM4	VSS_65	BG51	
AM41	VSS_66	BH17	
AM5	VSS_67	BH30	
AN1	VSS_68	BH46	
AN38	VSS_69	BH5	
AN38	VSS_70	BH11	
AN43	VSS_71	BH13	
AN5	VSS_72	BH3	
AN7	VSS_73	B4	
AN7	VSS_74	B42	
AP48	VSS_75	B46	
AP50	VSS_76	BK15	
AR1	VSS_77	BK17	
AR2	VSS_78	BK25	
AR2	VSS_79	BK29	
AR44	VSS_80	BK36	
AR7	VSS_81	BK40	
AR7	VSS_82	BK44	
AT10	VSS_83	BK5	
AT14	VSS_84	BL1	
AT14	VSS_85	BL13	
AT41	VSS_86	BL11	
AT56	VSS_87	BL13	
AU1	VSS_88	BL19	
AU23	VSS_89	BL27	
AU3	VSS_90	BL22	
AU36	VSS_91	BL1	
AU36	VSS_92	BL1	
AU49	VSS_93	C16	
AU51	VSS_94	C15	
AV38	VSS_95	C28	
AV48	VSS_96	C29	
AW1	VSS_97	C33	
AW12	VSS_98	C36	
AW16	VSS_99	C41	

VSS

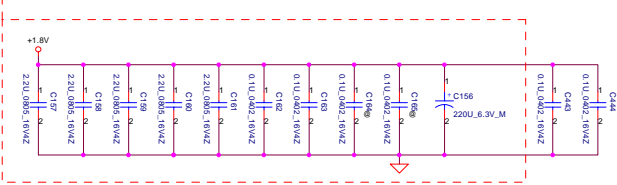
J31			
C46	VSS_199	W11	
C50	VSS_200	W39	
C7	VSS_201	W43	
D13	VSS_202	W47	
D24	VSS_203	W5	
D3	VSS_204	W7	
D32	VSS_205	W13	
D39	VSS_206	Y2	
D45	VSS_207	Y41	
D49	VSS_208	Y46	
E10	VSS_209	Y49	
E14	VSS_210	Y50	
E24	VSS_211	Y50	
E28	VSS_212	Y50	
E47	VSS_214	T29	
F19	VSS_215	T31	
F36	VSS_216	T33	
F4	VSS_217	T35	
F40	VSS_218	R28	
F50	VSS_219		
G1	VSS_220		
G13	VSS_221	VSS_306	AA32
G16	VSS_222	VSS_307	AD32
G19	VSS_223	VSS_308	AF28
G24	VSS_224	VSS_309	AF29
G28	VSS_225	VSS_310	AV27
G28	VSS_226	VSS_311	AV28
G30	VSS_227	VSS_312	AV28
G42	VSS_228	VSS_313	H50
G46	VSS_229		
G48	VSS_230		
H1	VSS_231		
H24	VSS_232		
H28	VSS_233		
H4	VSS_234		
H45	VSS_235		
H11	VSS_236		
J16	VSS_237		
J2	VSS_238		
J24	VSS_239		
J33	VSS_240		
J35	VSS_241		
J35	VSS_242		
J39	VSS_243		
K12	VSS_245		
K47	VSS_246		
L1	VSS_247		
L17	VSS_248		
L20	VSS_249		
L24	VSS_250		
L24	VSS_251		
L28	VSS_252		
L3	VSS_253		
L33	VSS_254		
L48	VSS_255		
M28	VSS_256		
M42	VSS_257		
M48	VSS_258		
M49	VSS_259		
M5	VSS_260		
M50	VSS_261		
M9	VSS_262		
N14	VSS_263		
N17	VSS_264		
N26	VSS_265		
N32	VSS_266		
N32	VSS_267		
N39	VSS_268		
N44	VSS_269		
N49	VSS_270		
N7	VSS_271		
P13	VSS_272		
P2	VSS_273		
P23	VSS_274		
P23	VSS_275		
P3	VSS_276		
P39	VSS_277		
P49	VSS_278		
P59	VSS_279		
T43	VSS_280		
T47	VSS_281		
T47	VSS_282		
U41	VSS_283		
U50	VSS_284		
U55	VSS_285		
V2	VSS_286		
V3	VSS_286		

VSS

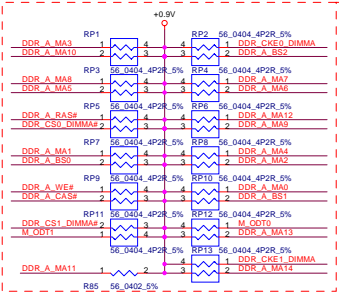
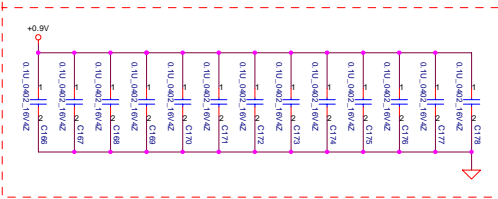
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title
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				LA-3901P
				Rev 0.3
				Date: Monday, October 22, 2007
				Sheet 12 of 42



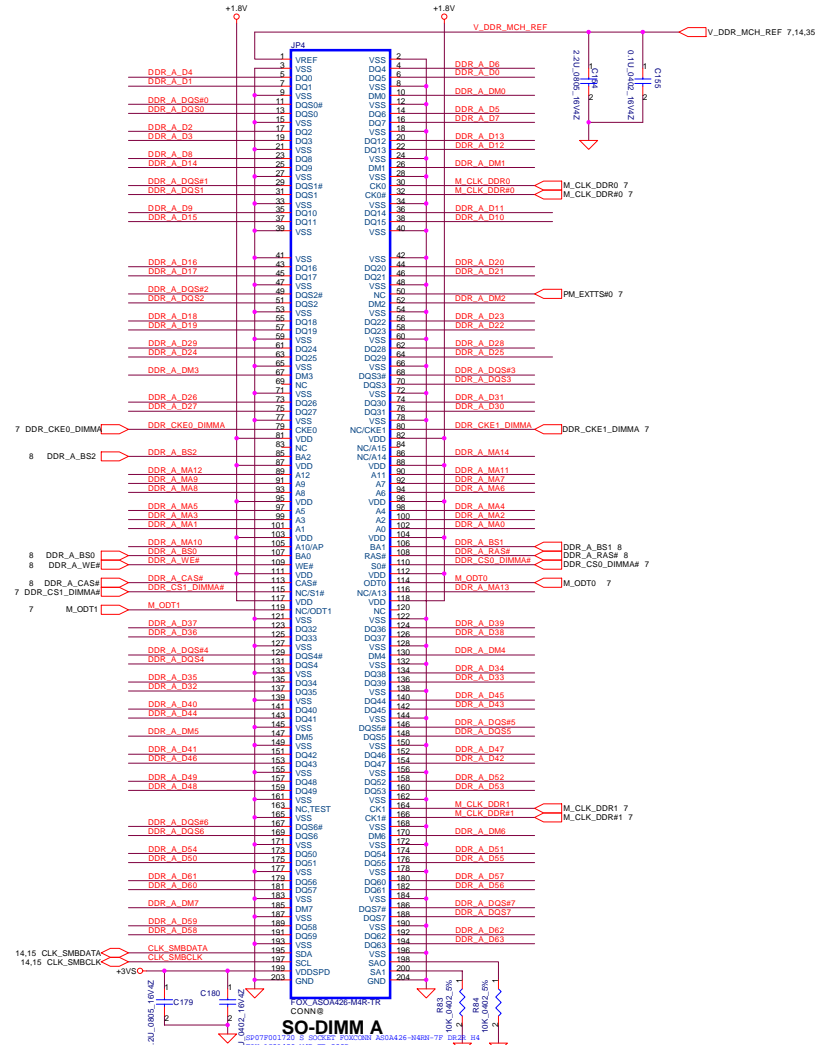
Layout Note:
Place near JP34



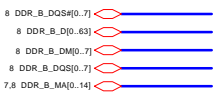
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



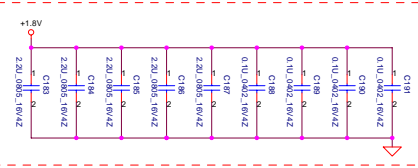
Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"



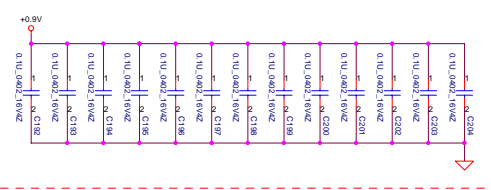
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	DDR1-SODIMM SLOT1	
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				Customer	LA-3901P
				Date	Monday, October 22, 2007
				Sheet	13 of 42



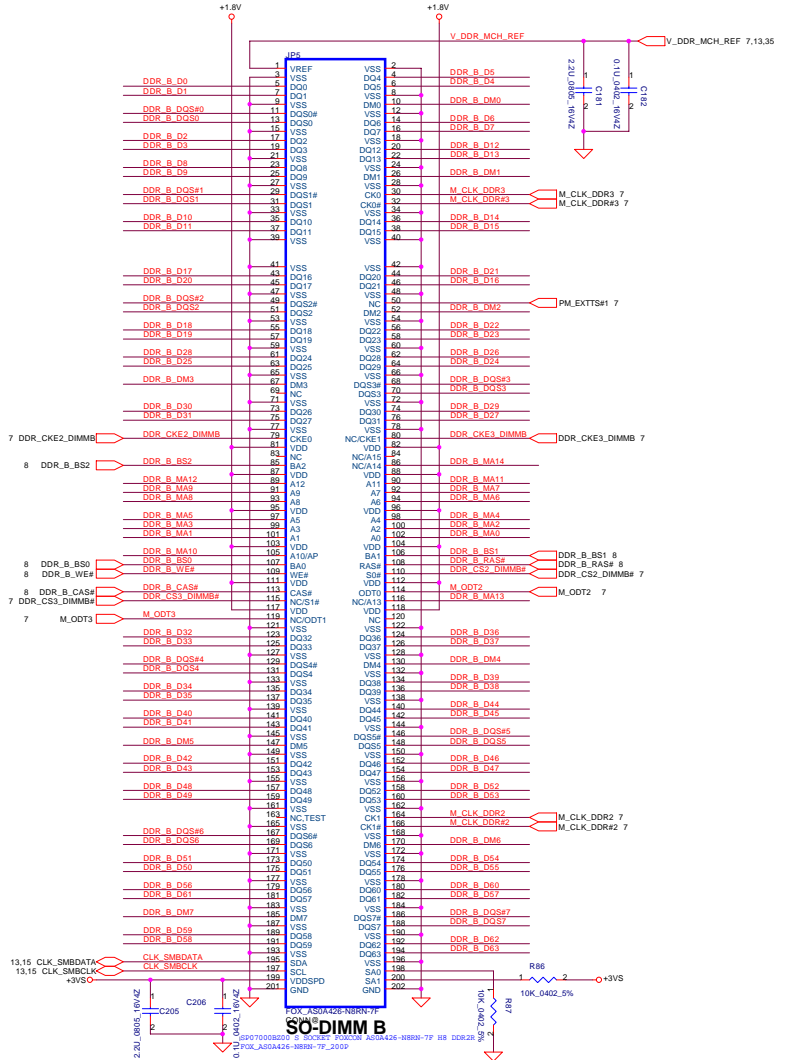
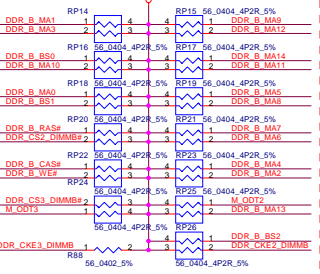
Layout Note:
Place near JP10



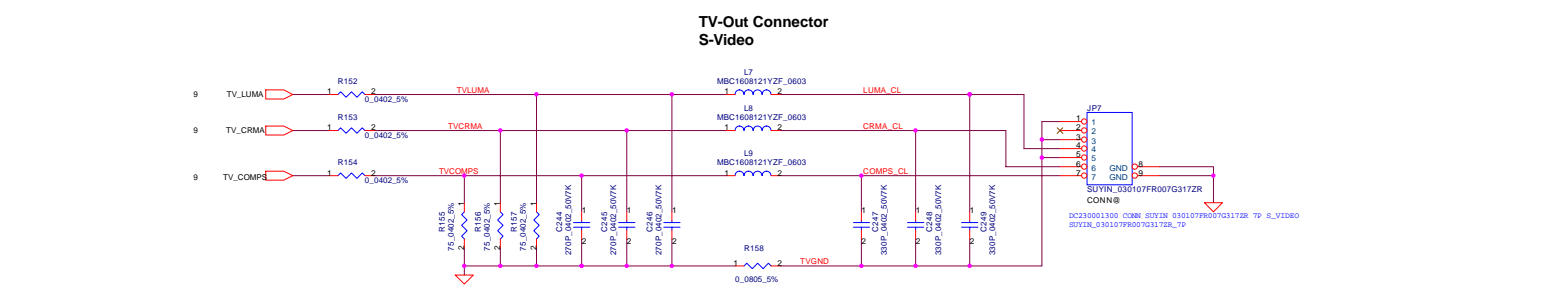
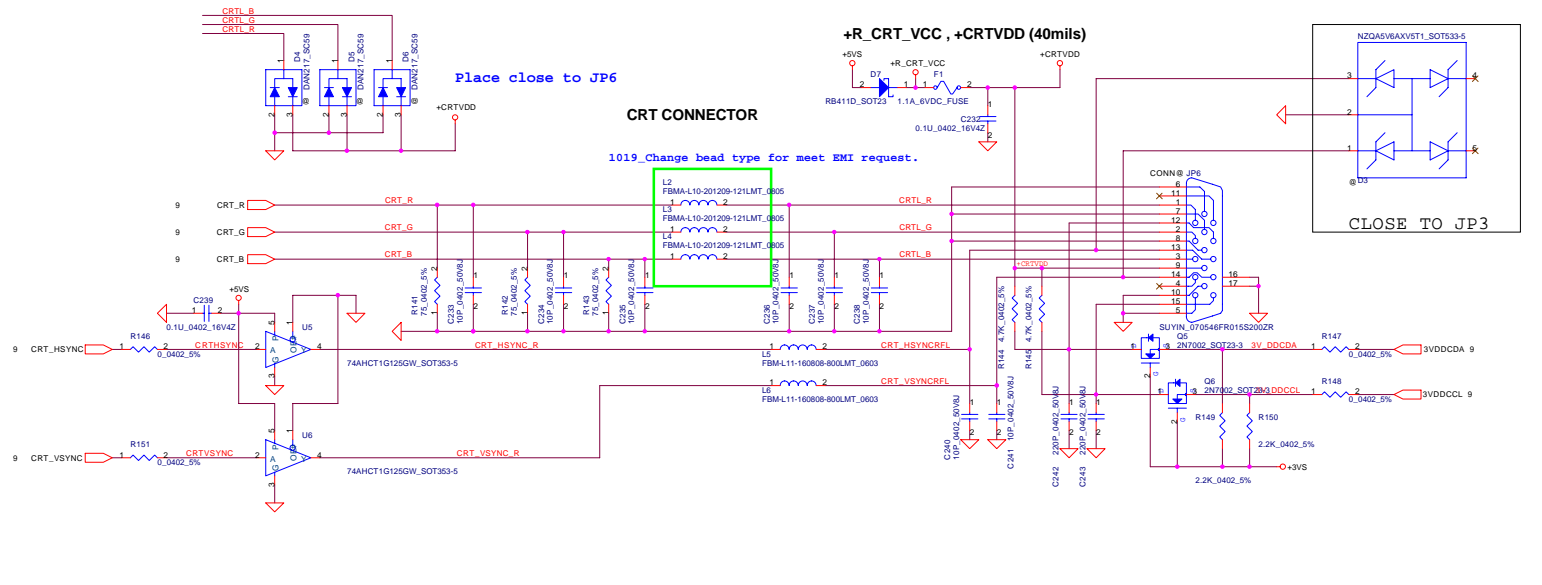
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



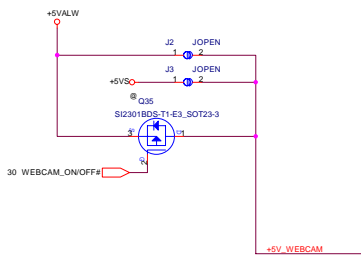
Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



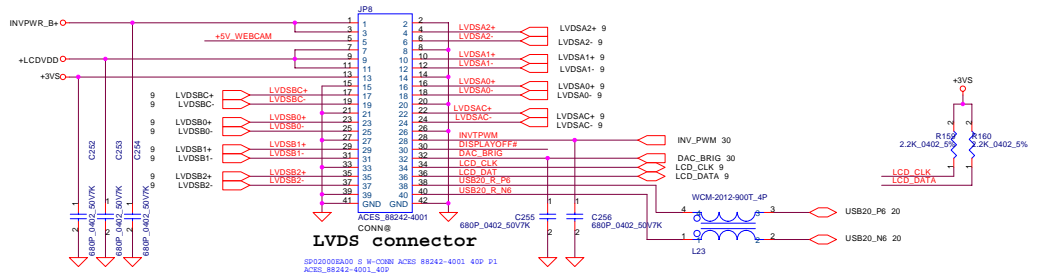
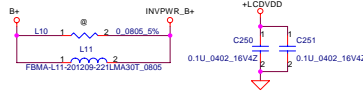
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	DDR1-SODIMM SLOT	
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				LA-3981P	Rev 0.3
Date:	Monday, October 22, 2007	Sheet	14	of 42	



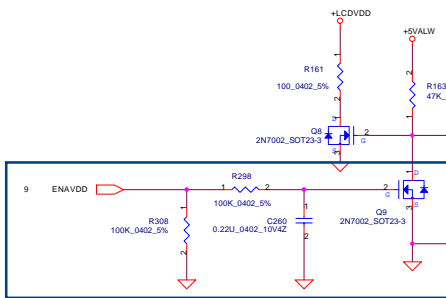
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>			
Compal Electronics, Inc. CRT & TVout Connector			Title CRT & TVout Connector
Size Document Number LA-3981P			Rev 0.3
Date: Monday, October 22, 2007			Sheet 16 of 42



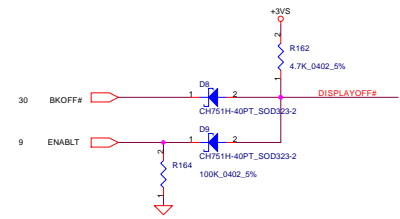
LVDS CONN



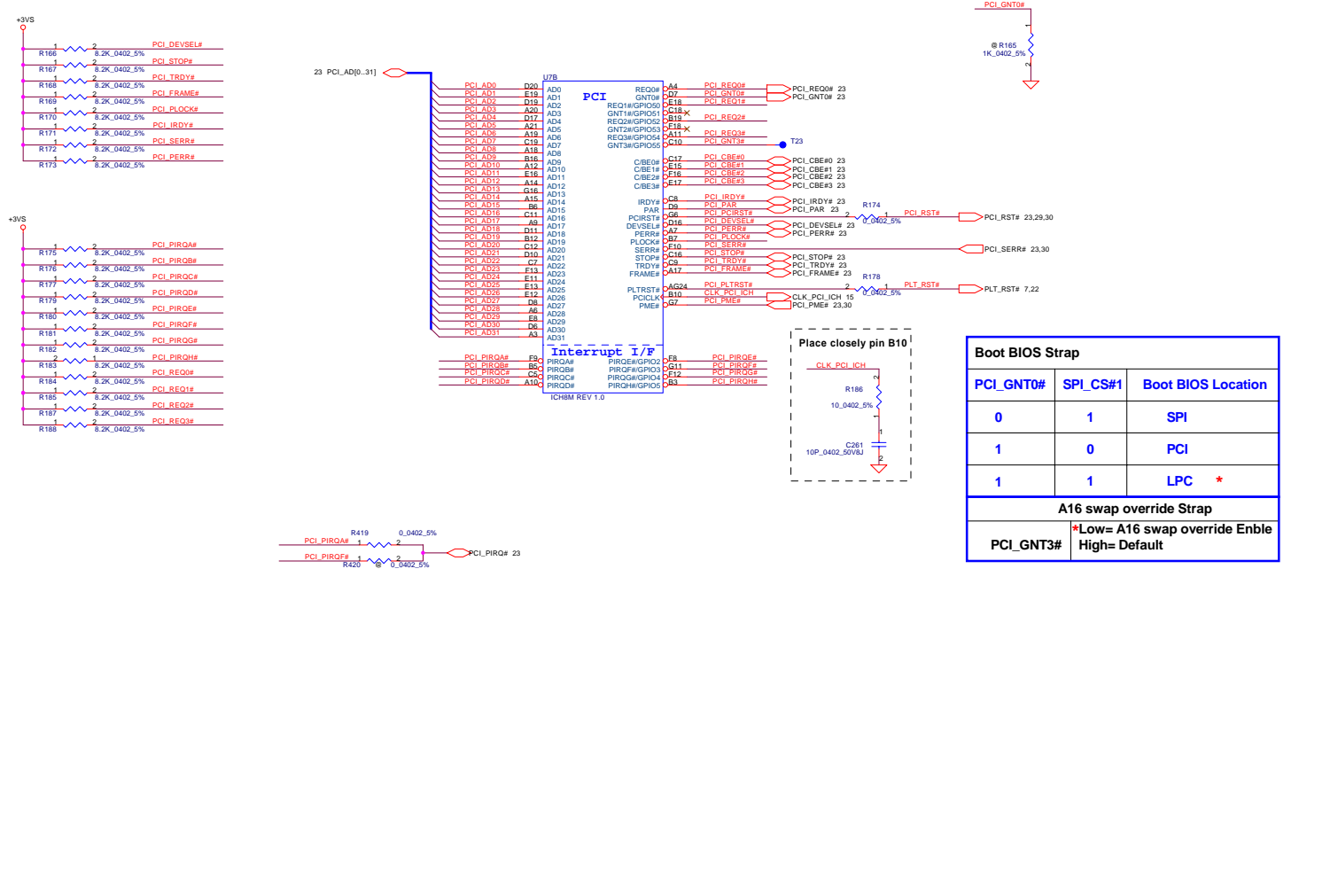
LVDS connector
 ACES_86242-4001
 CONNR
 680P_0402_50V7K
 C256 680P_0402_50V7K
 WCM-2012-900T_4P
 L23
 USB20_P6 20
 USB20_N6 20



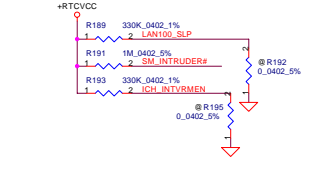
Avoid Panel display garbage after power on.



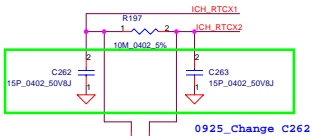
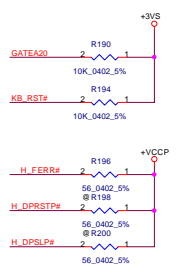
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	LCD CONN.	
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Size	Document Number	Rev	LA-398IP		
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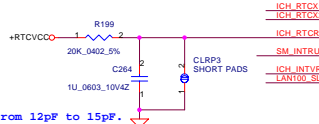
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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				LA-3981P	Rev 0.3
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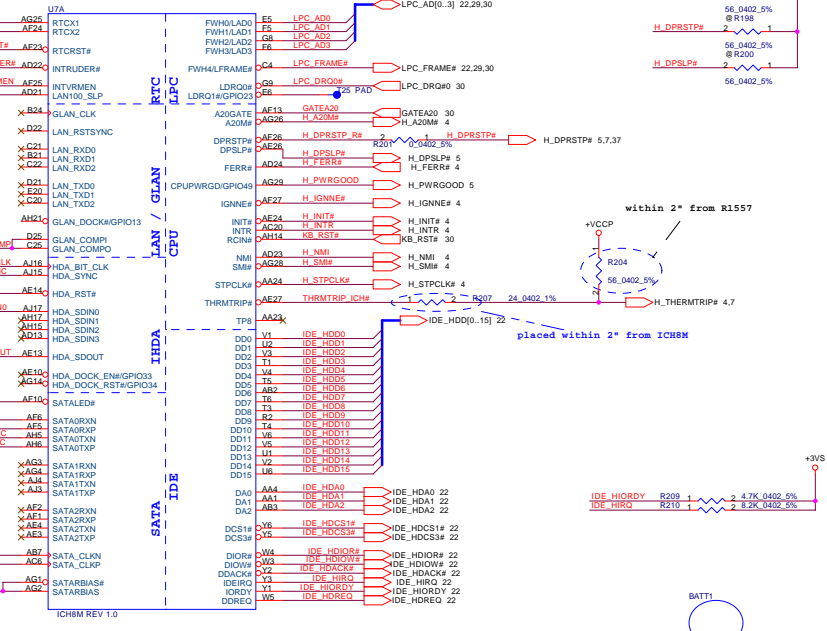
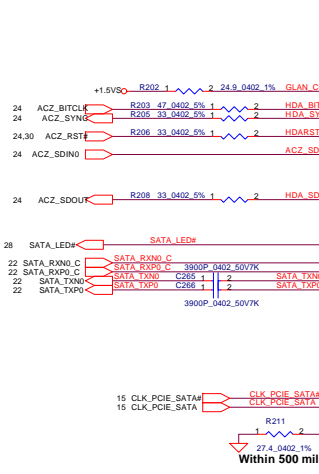
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCLL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCLL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



0925_Change C262 and C263 from 12pF to 15pF.



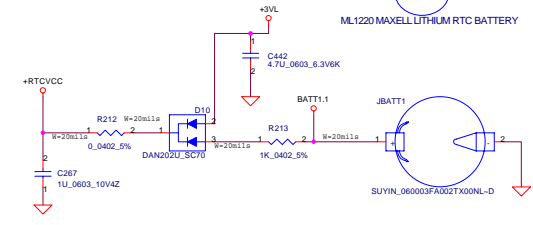
32.768KHZ_12.5P_Q13MC30810018



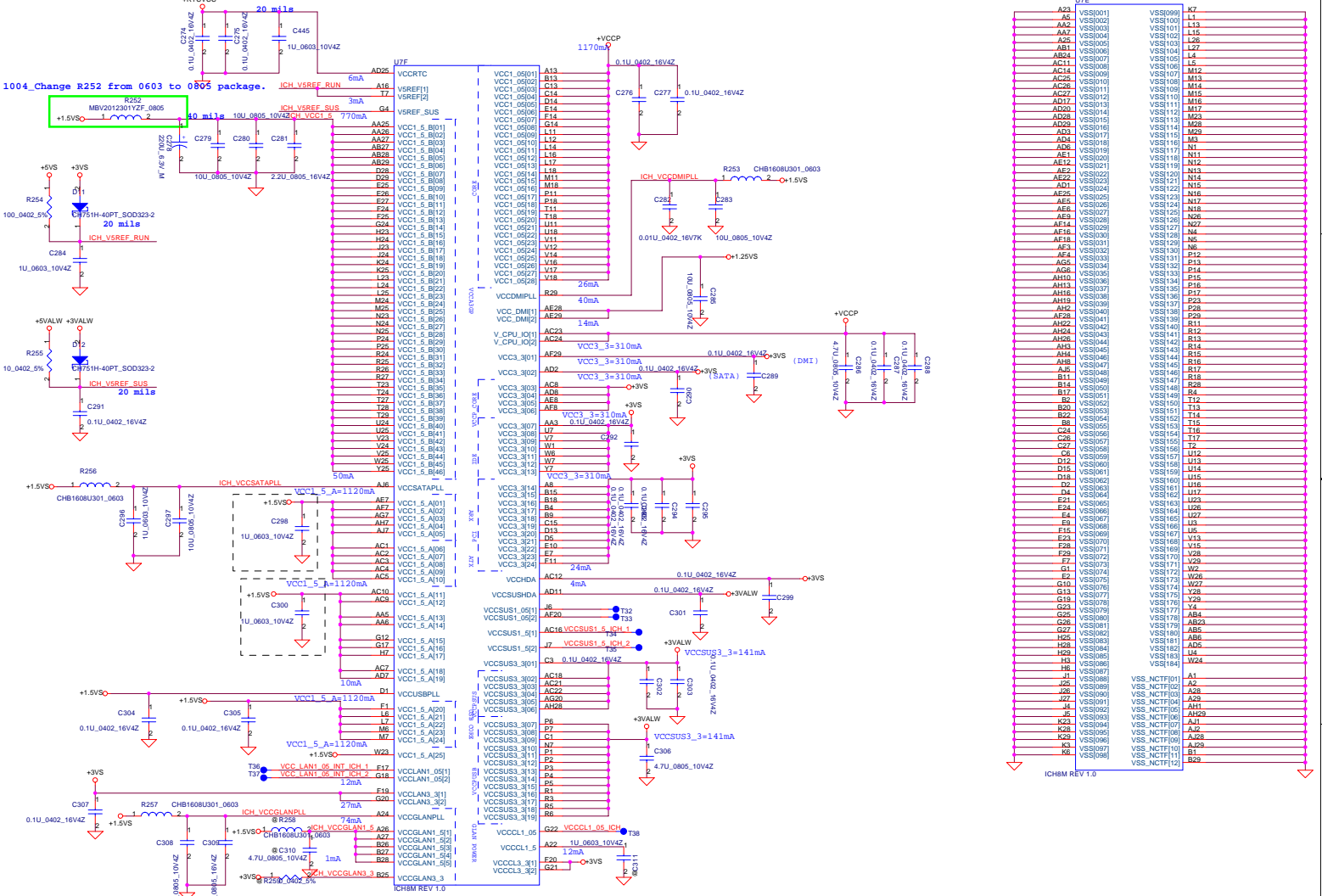
within 2" from R1557

placed within 2" from ICH8M

within 500 mils



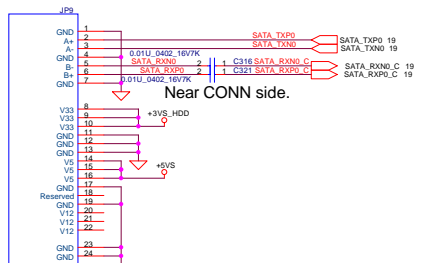
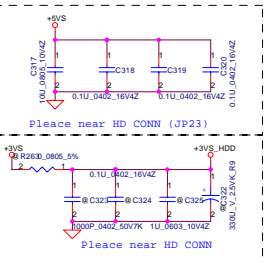
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title
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				Document Number LA-3981P
				Rev 0.3
				Date: Monday, October 22, 2007
				Sheet 18 of 42



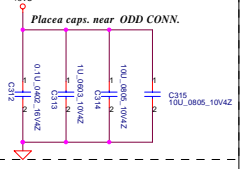
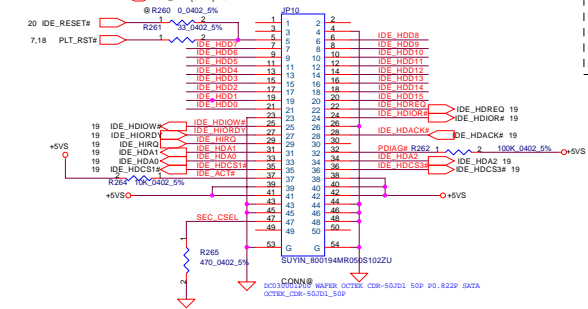
U7E	K7
AC	VSS000
AA2	VSS001
AA7	VSS002
AA5	VSS003
AB1	VSS004
AA6	VSS005
AB4	VSS006
AB1	VSS007
AC14	VSS008
AC3	VSS009
AC5	VSS010
AC26	VSS011
AC27	VSS012
AD17	VSS013
AD20	VSS014
AD3	VSS015
AD1	VSS016
AD4	VSS017
AD8	VSS018
AE1	VSS019
AE12	VSS020
AE2	VSS021
AE22	VSS022
AE1	VSS023
AE22	VSS024
AE3	VSS025
AE4	VSS026
AE5	VSS027
AE9	VSS028
AE14	VSS029
AE16	VSS030
AE3	VSS031
AE4	VSS032
AG5	VSS033
AG6	VSS034
AH10	VSS035
AH13	VSS036
AH18	VSS037
AH18	VSS038
AH18	VSS039
AH22	VSS040
AH24	VSS041
AH28	VSS042
AH1	VSS043
AH4	VSS044
AH1	VSS045
AH6	VSS046
B14	VSS047
B17	VSS048
B22	VSS049
B20	VSS050
B22	VSS051
B8	VSS052
C28	VSS053
C28	VSS054
C27	VSS055
C28	VSS056
D12	VSS057
D14	VSS058
D18	VSS059
D1	VSS060
EA2	VSS061
E24	VSS062
E4	VSS063
E3	VSS064
F15	VSS065
F28	VSS066
F7	VSS067
G1	VSS068
G2	VSS069
G10	VSS070
G13	VSS071
G19	VSS072
G25	VSS073
G28	VSS074
G27	VSS075
H25	VSS076
H29	VSS077
H31	VSS078
H8	VSS079
J1	VSS080
J25	VSS081
J27	VSS082
J4	VSS083
K23	VSS084
K28	VSS085
K29	VSS086
K8	VSS087
K6	VSS088
LA-3901P	VSS_NCTF01
LA-3901P	VSS_NCTF02
LA-3901P	VSS_NCTF03
LA-3901P	VSS_NCTF04
LA-3901P	VSS_NCTF05
LA-3901P	VSS_NCTF06
LA-3901P	VSS_NCTF07
LA-3901P	VSS_NCTF08
LA-3901P	VSS_NCTF09
LA-3901P	VSS_NCTF10
LA-3901P	VSS_NCTF11
LA-3901P	VSS_NCTF12

Security Classification	2007/03/26	Deciphered Date	2006/03/10	Title
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Compal Electronics, Inc.
				ICH8(4) POWER&GND
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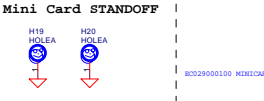
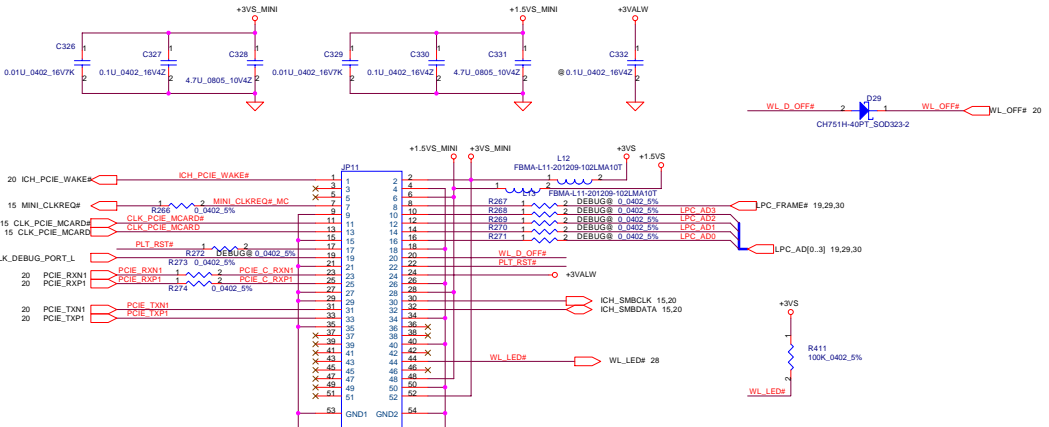
HDD Connector



CD-ROM Connector

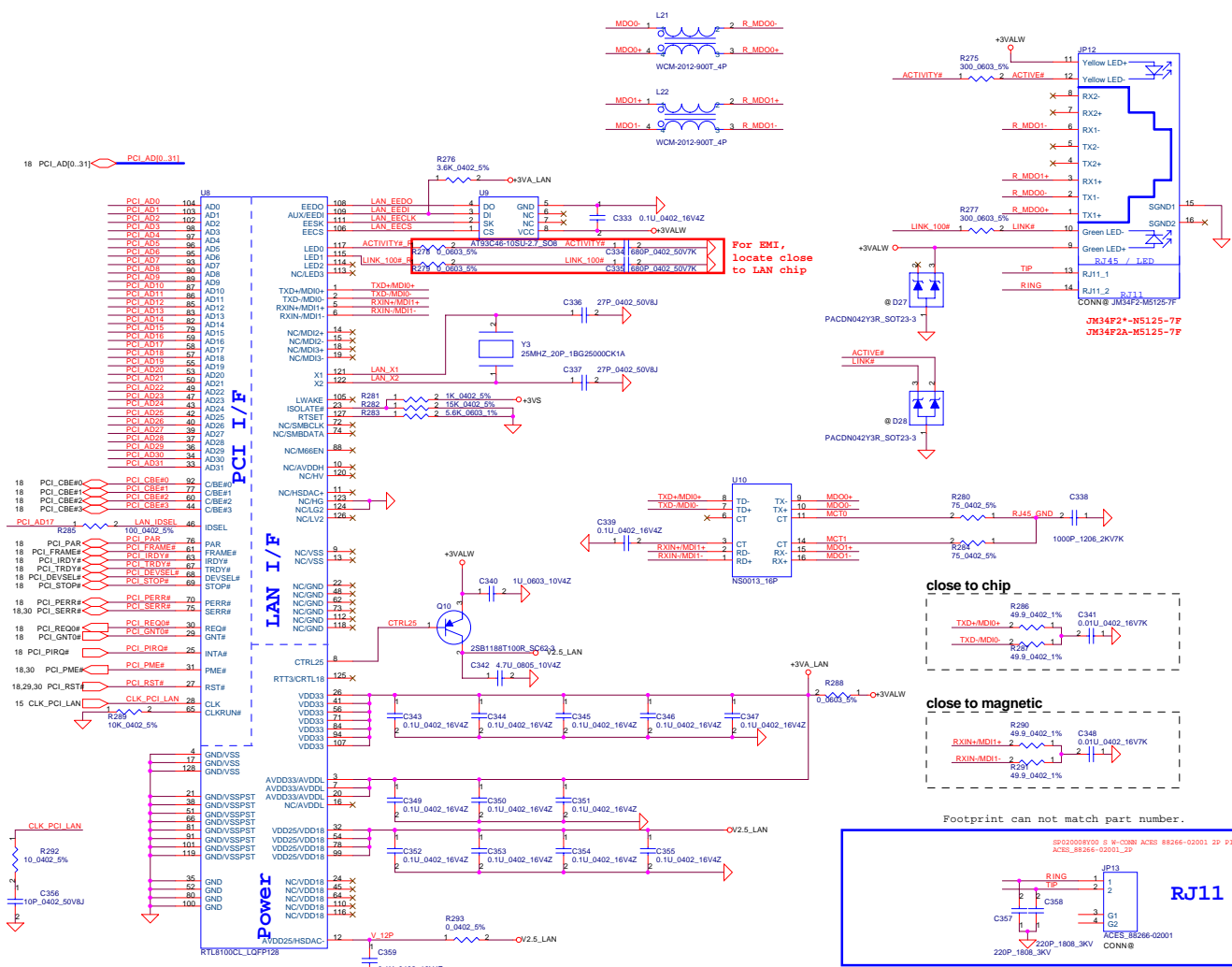


Mini-Express Card---WLAN



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Title HDD/ODD/Mini Card CONN.			Rev 0.3
Date Monday, October 22, 2007			Sheet 22 of 42

Close to JP12.



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Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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Size	Document Number	Rev			
	LA-3981P	0.3			
Date	Monday, October 22, 2007	Sheet	23	of	42

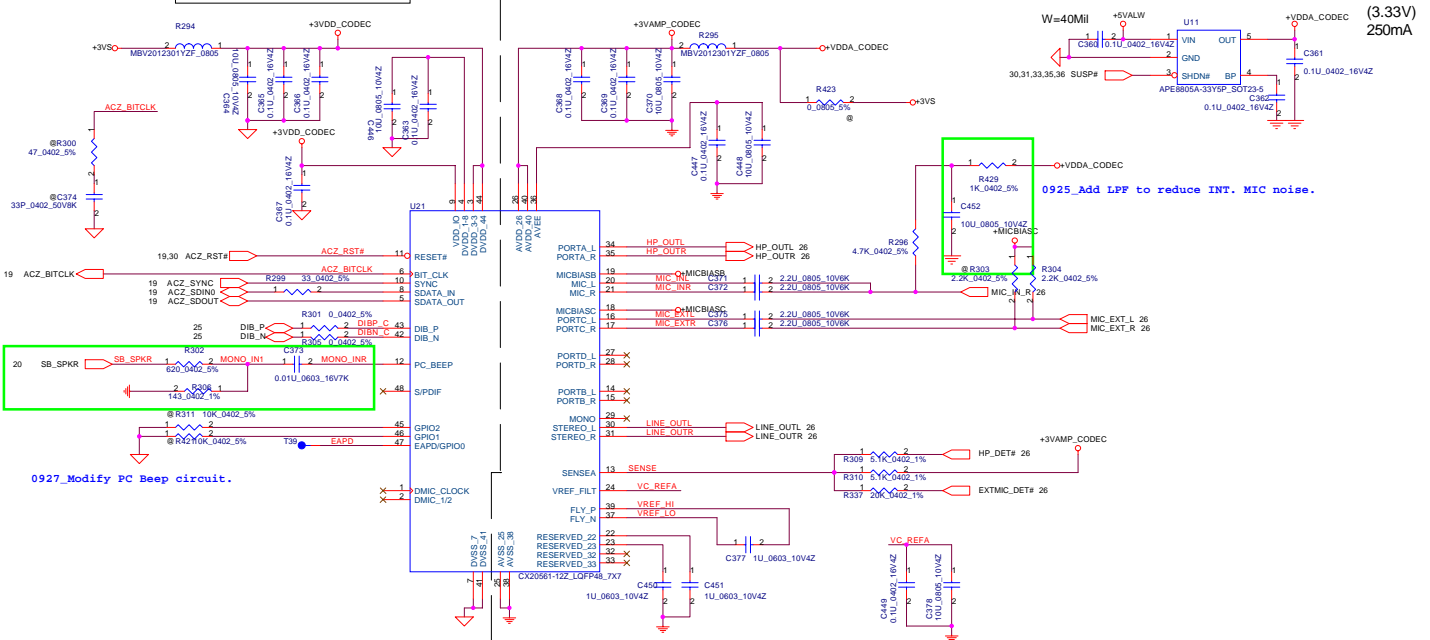
In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

AUDIO CODEC

For Layout: Place decoupling caps near the power pins of SmartAMC device.

CODEC POWER

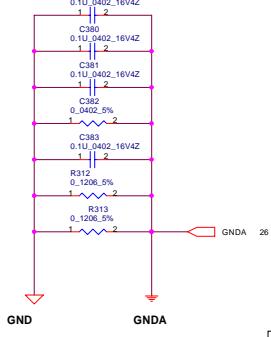
(3.33V)
250mA



0927_Modify PC Beep circuit.

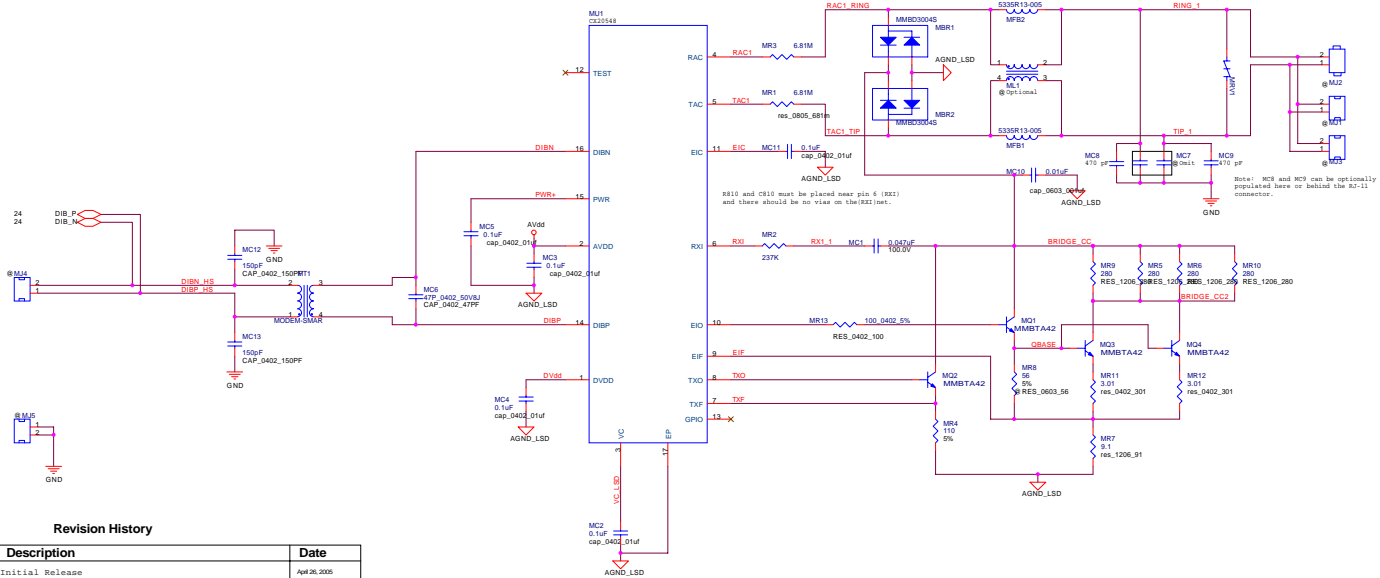
0925_Add LPF to reduce INT. MIC noise.

DIGITAL ANALOG



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	AMOM codec	
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				LA-398IP	Rev 0.3
				Date	Monday, October 22, 2007
				Sheet	24 of 42

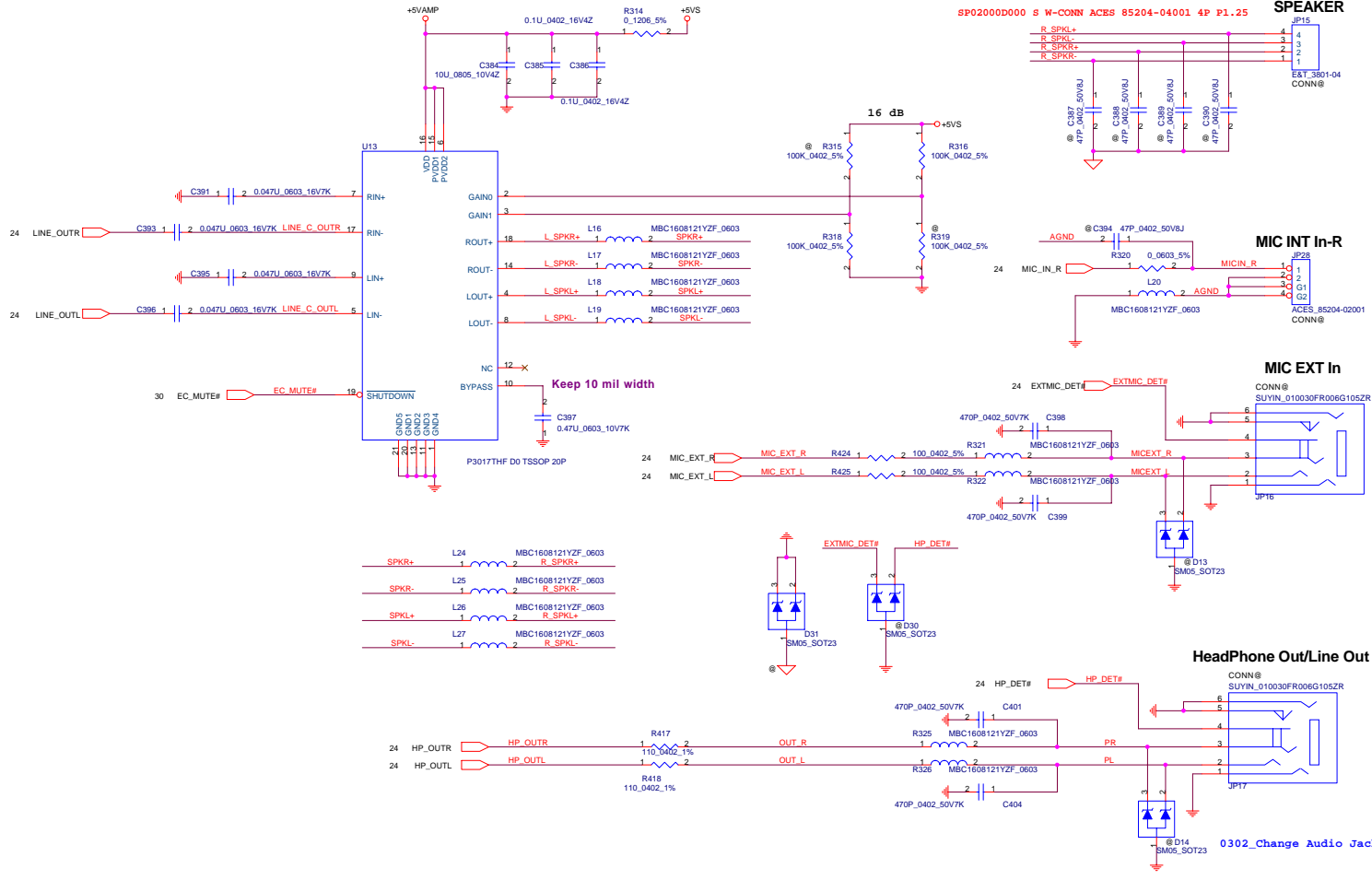


Note: MC8 and MC9 can be optionally populated here or behind the R2-11 connector.

Revision History

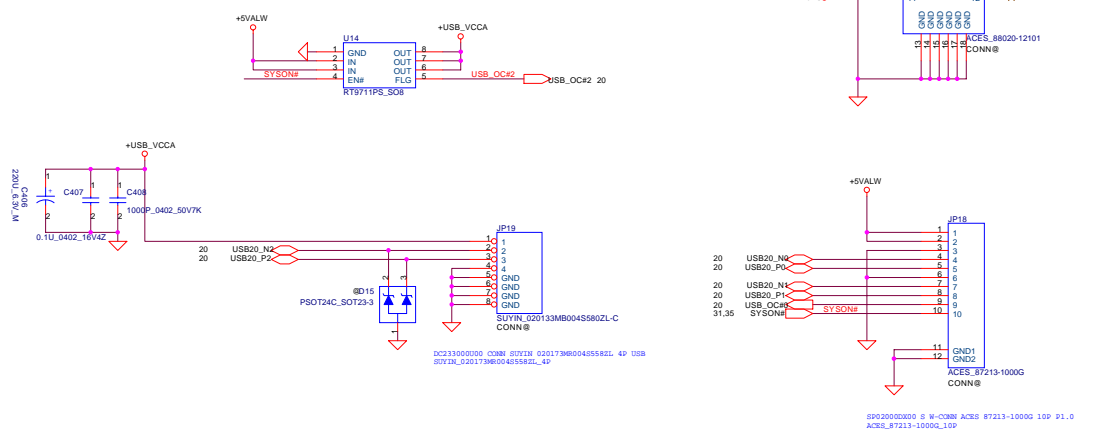
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

Security Classification	Compal Secret Data	Deciphered Date	File
	2007/03/26	2007/07/26	AMOM-CX20548
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Rev	0.3	Date	Monday, October 22, 2007
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Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2007/08/29	AMP & Audio Jack
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Size	Document Number	LA-398IP	Rev	0.3
Date	Monday, October 22, 2007	Sheet	26	of 42

USB Port



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Issued Date	2007/03/26	Deciphered Date	2006/07/26	USB CONN.	
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Size	Document Number	Rev		0.3	
	LA-398IP				
Date	Monday, October 22, 2007	Sheet	27	of	42

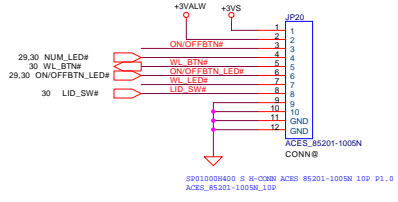
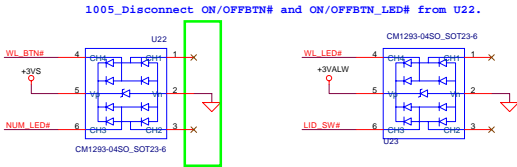
POWER LED(Left 1)

M/BtoS/B

Battery Charge LED(Left 2)

HDD LED(Left 3)

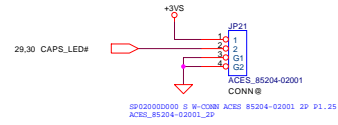
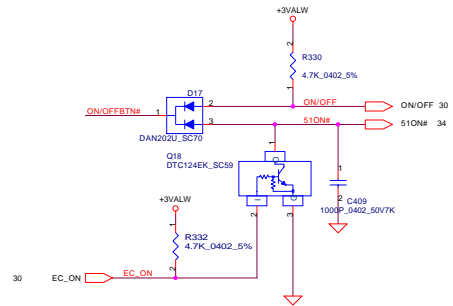
Wireless ON/OFF LED(Left 4)



0927_Change R329, R331, R333 (75 ohm), R335 (33 ohm) to 27 ohm.

Power ON/OFF

M/B to SB(Caps Lock LED)



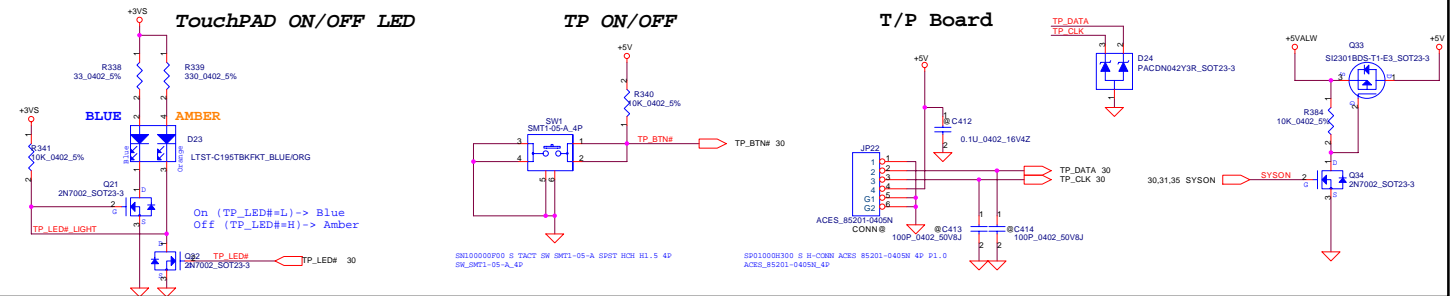
On (WL_ON#=L) -> Blue
Off (WL_ON#=H) -> Amber

D21, D25, D23 Footprint can not match part number.

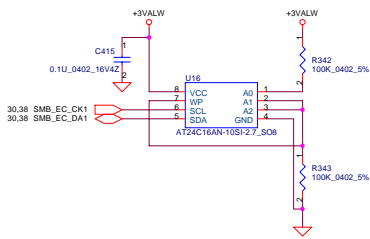
TouchPAD ON/OFF LED

TP ON/OFF

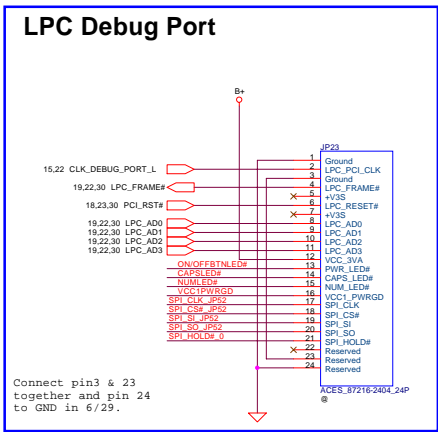
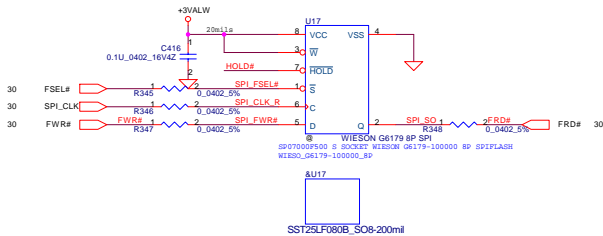
T/P Board



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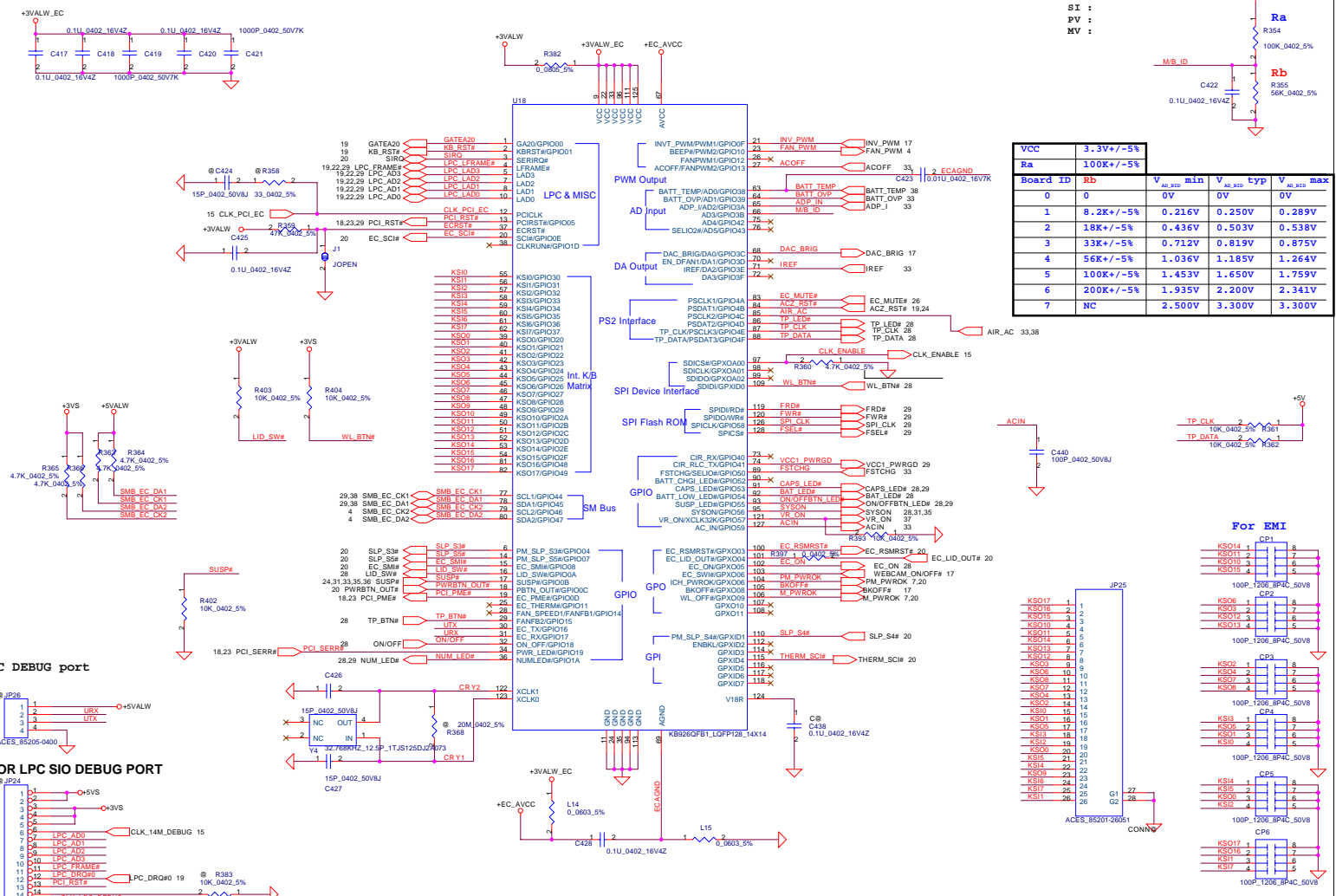


SPI ROM

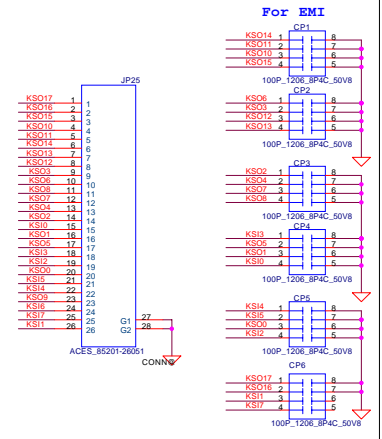
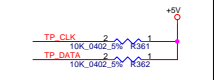


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Date	Monday, October 22, 2007	Sheet	29	of 42

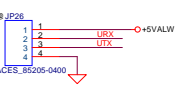
Board ID : DB : 4
 SI :
 PV :
 MV :
 +3VALW_EC
 Ra
 R354
 100K_0402_5%



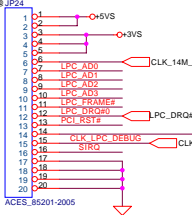
Board ID	Rb	V _{min}	V _{typ}	V _{max}
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	1.8K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V



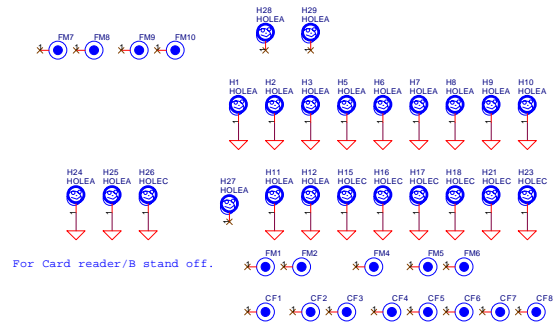
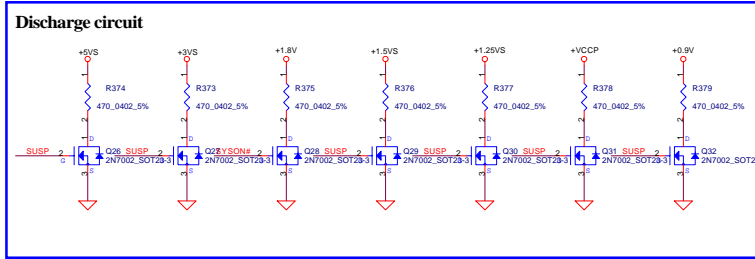
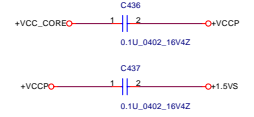
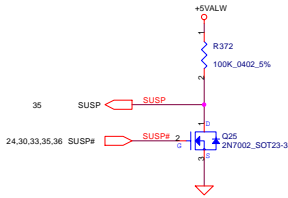
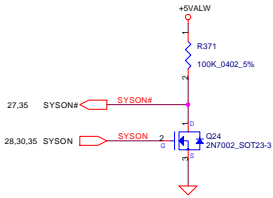
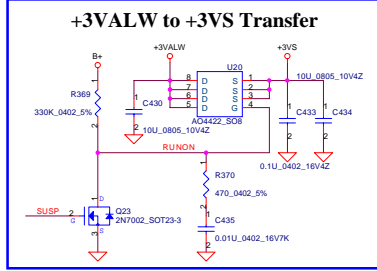
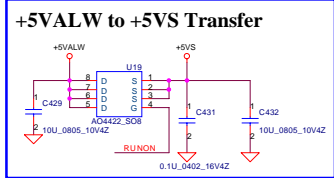
EC DEBUG port



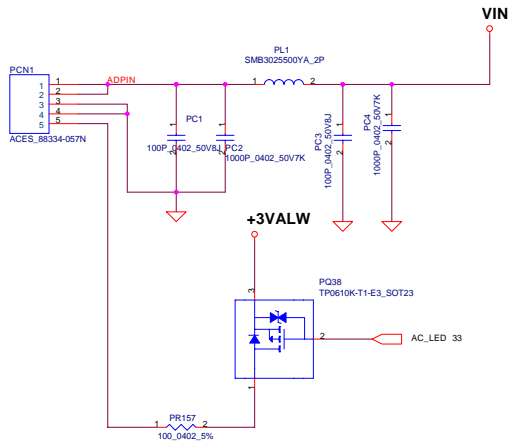
FOR LPC SIO DEBUG PORT



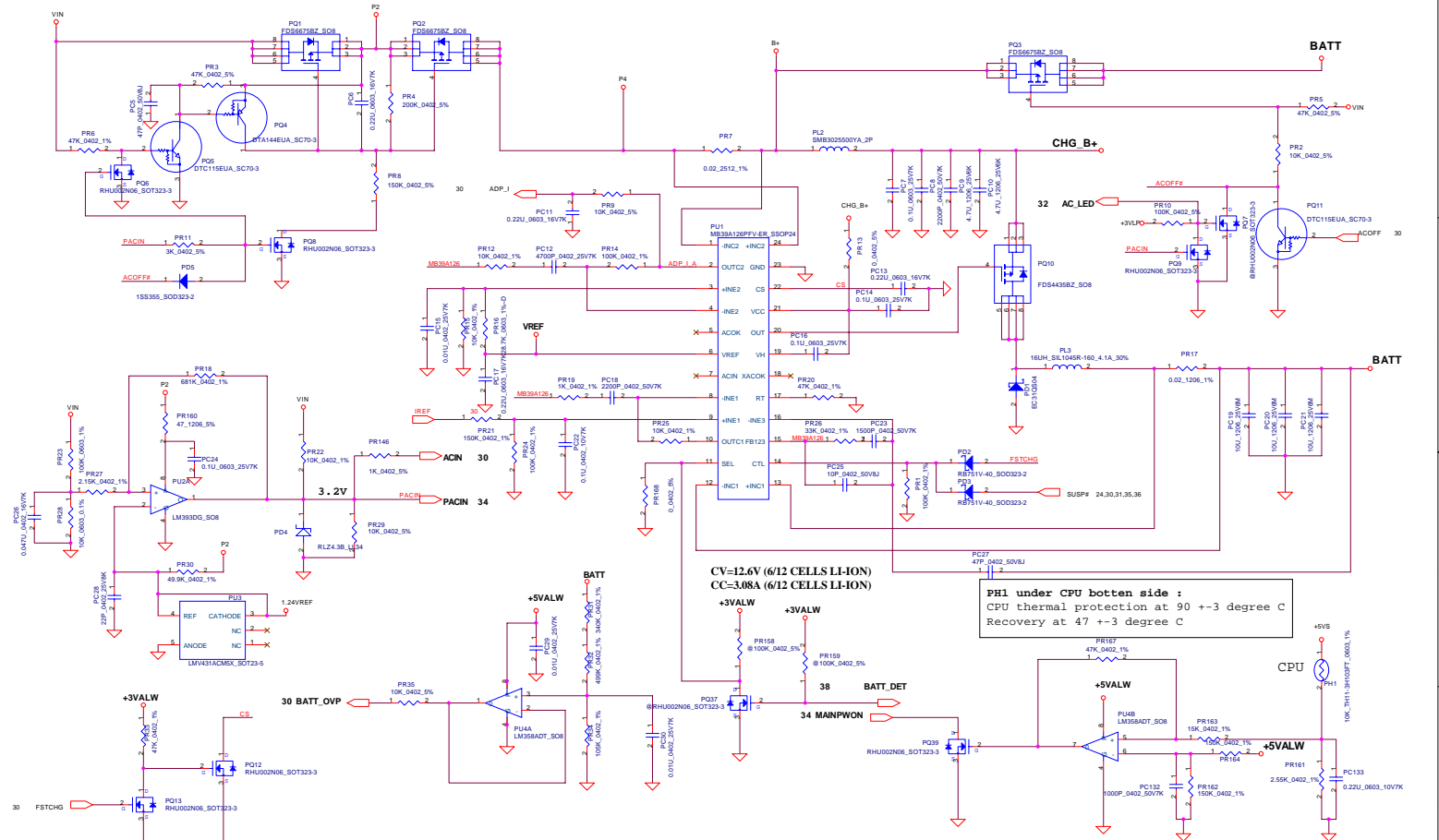
Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	EC KB926/KB con
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Size	Document Number	LA-3981P		Rev	0.3
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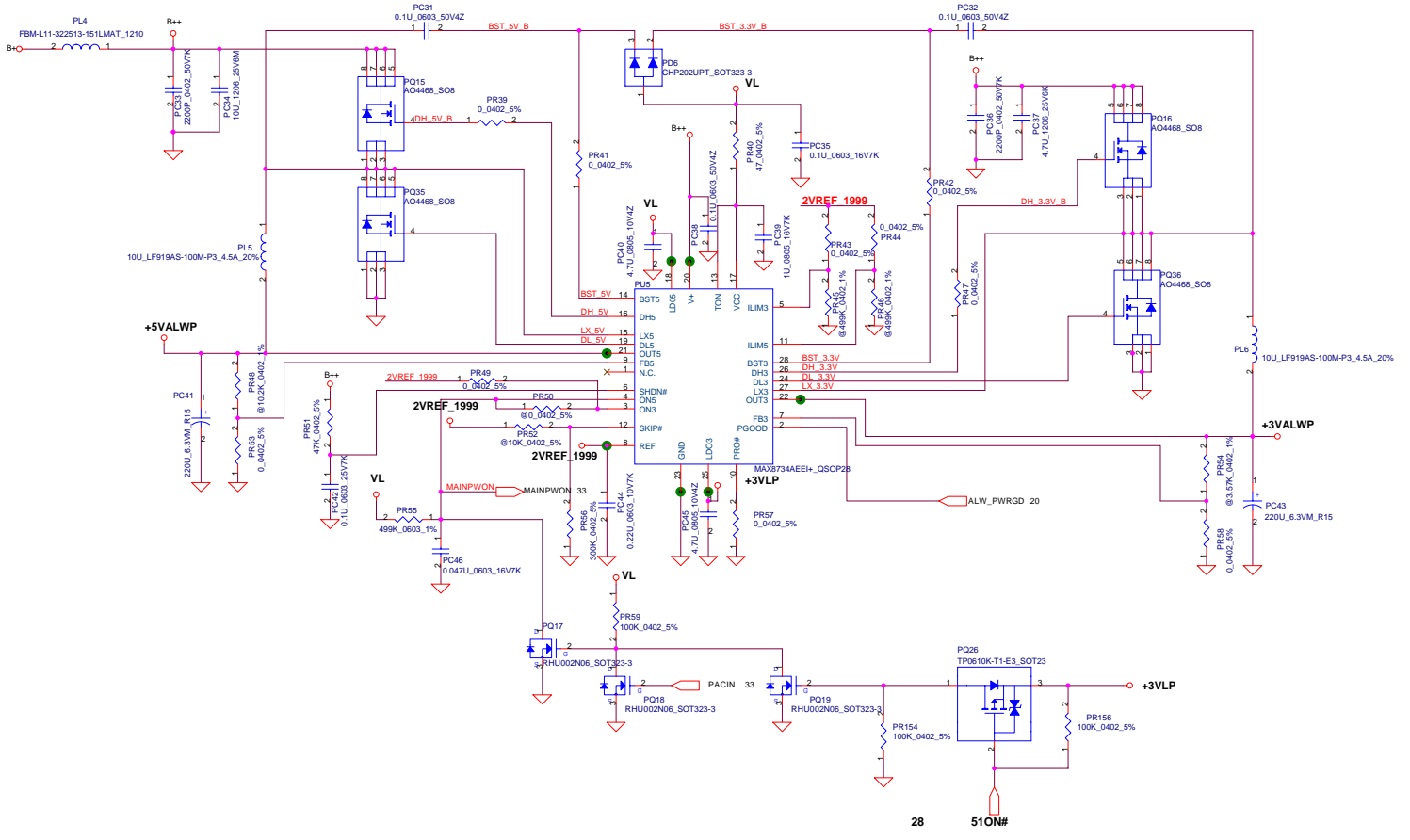


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Date	Monday, October 22, 2007	Sheet	32 of 42	Rev

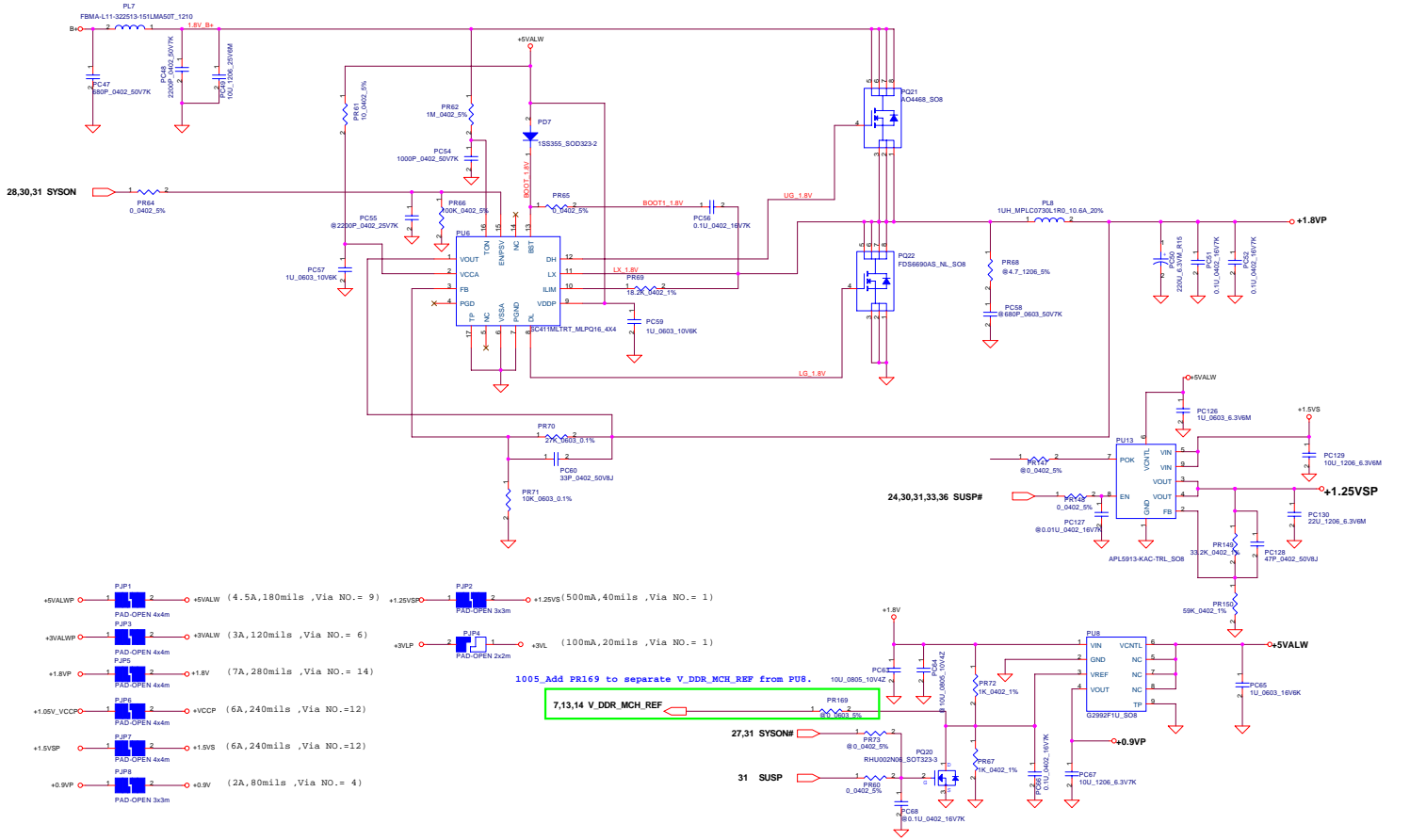


P11 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

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28,30,31 SYSON

24,30,31,33,36 SUSP#

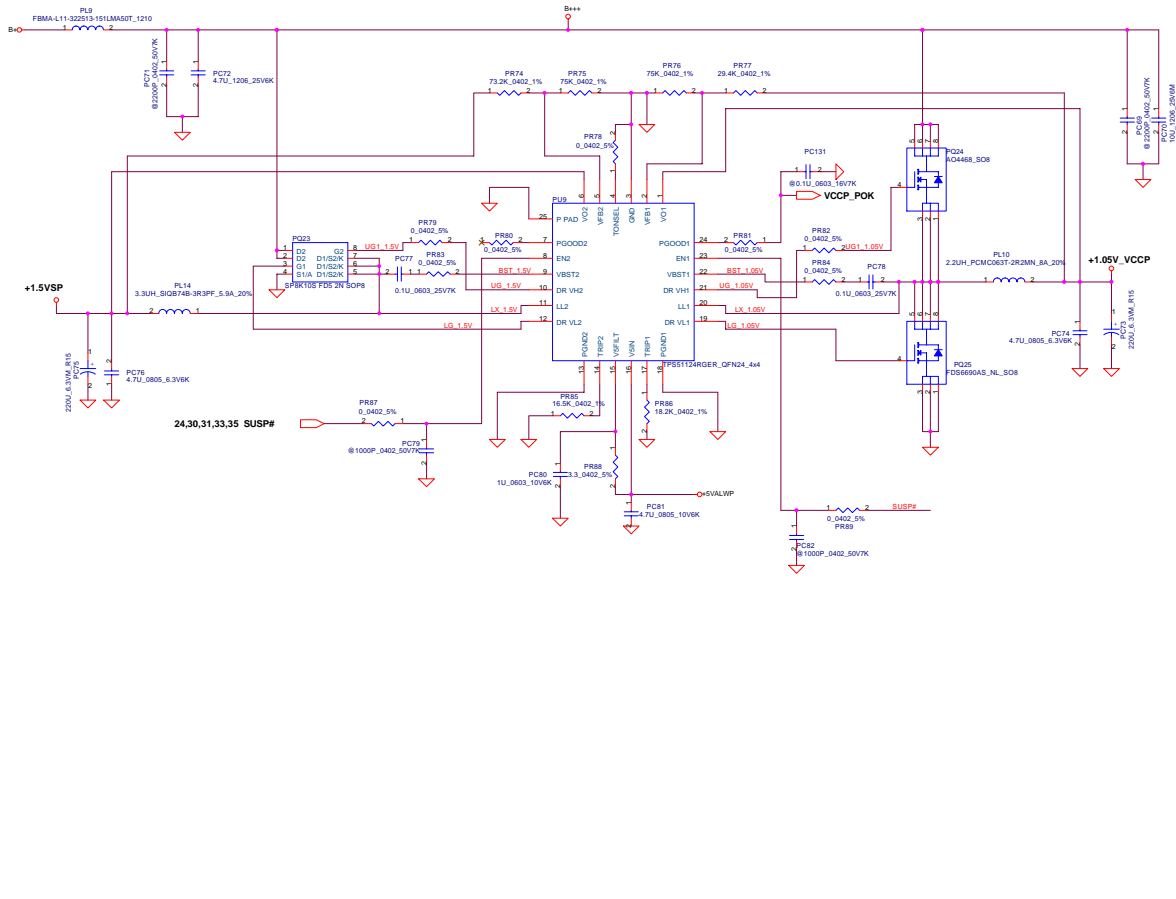
27,31 SYSON#

31 SUSP

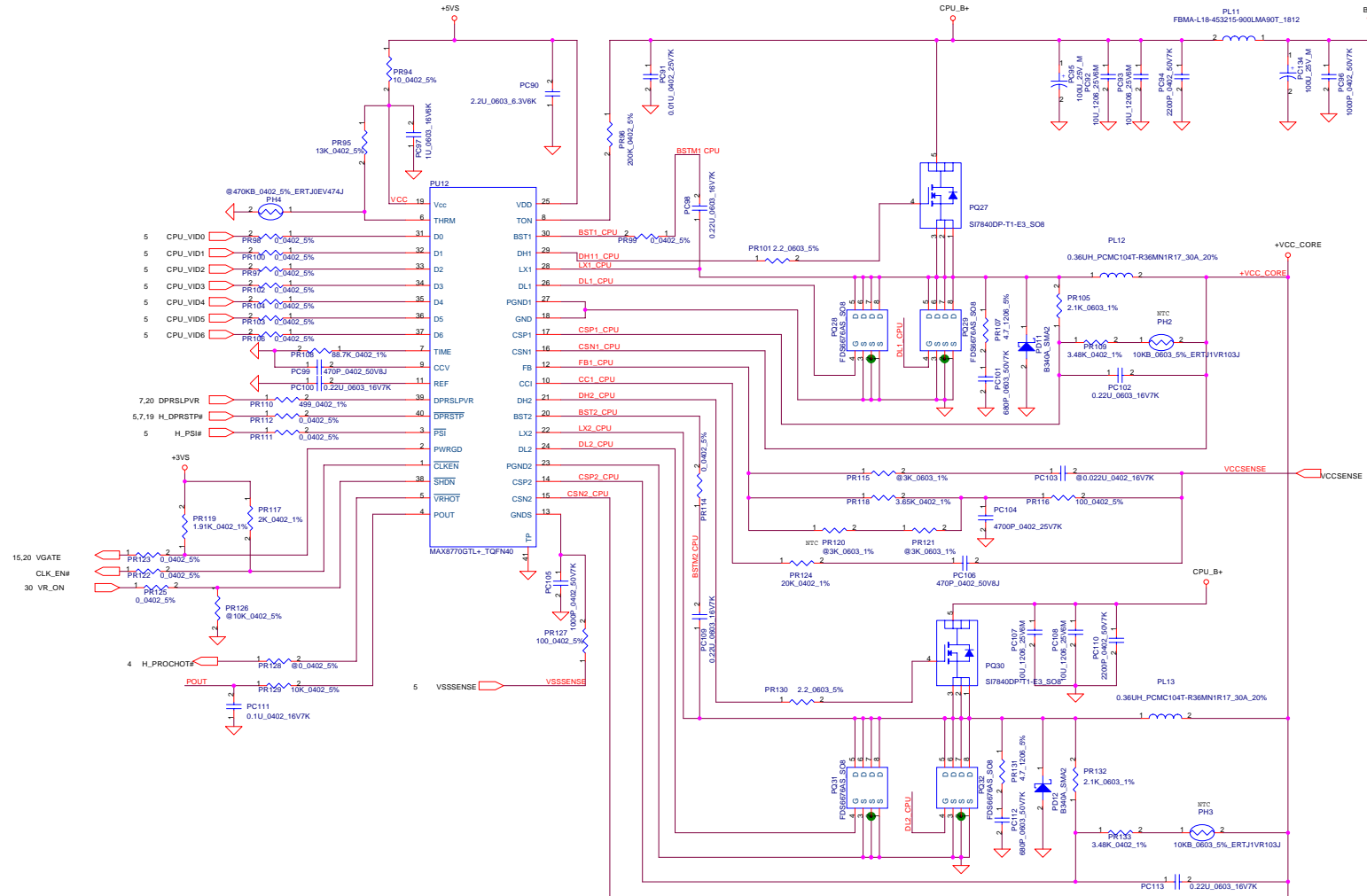
1005_Add FR169 to separate V_DDR_MCH_REF from PUS.
7,13,14 V_DDR_MCH_REF

- +SVALWP PJP1 2 +SVALW (4.5A,180mils ,Via NO.= 9)
- +SVALWP PJP2 2 +SVALW (3A,120mils ,Via NO.= 6)
- +1.8VP PJP3 2 +1.8V (7A,280mils ,Via NO.= 14)
- +1.05V_VCCP PJP6 2 +VCCP (6A,240mils ,Via NO.=12)
- +1.5VSP PJP7 2 +1.5VS (6A,240mils ,Via NO.=12)
- +0.9VP PJP8 2 +0.9V (2A,80mils ,Via NO.= 4)
- +1.25VSP PJP2 2 +1.25VSP (500mA,40mils ,Via NO.= 1)
- +9VP PJP2 1 +9V (100mA,20mils ,Via NO.= 1)

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				Date	Monday, October 25, 2009
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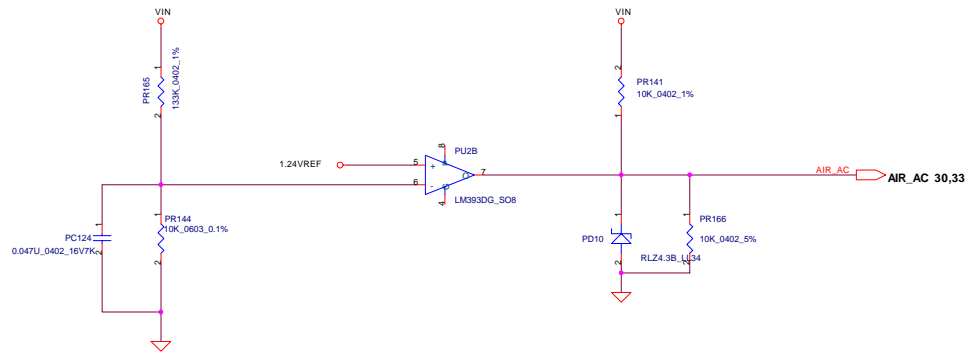
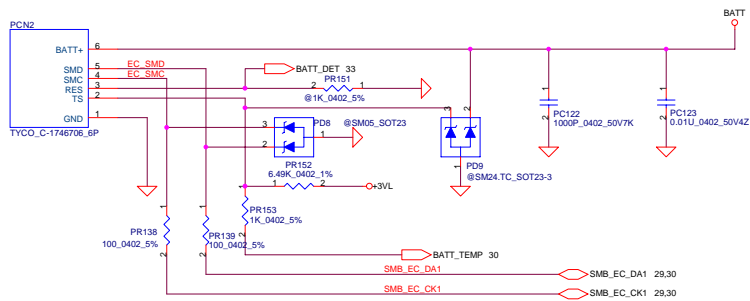


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File	+CPU CORE	
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				Size Custom
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Item	Reason for change	PG#	Modify List	Date	Phase
1			1009_FL8 change to 1uH.		
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

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Version Change List (P. I. R. List) for HW Circuit

Item	Change Item	Page	Date	Phase
1	Change C262 and C263 from 15pF to 12pF	19	7/16	DB --> SI
2	Reserved R245 and Add R422	20	7/16	DB --> SI
3	Add D29 prevent leakage issue	22	7/16	DB --> SI
4	Reserved diode D30 D31 for ESD	26	7/16	DB --> SI
5	Reserved R423 for coat down plan	24	7/24	DB --> SI
6	Remove Q12-Q17, R323 R324 R327 R328 R417 R418	26	7/30	DB --> SI
7	Change EXT MIC port B to port C	24	7/31	DB --> SI
8				DB --> SI
9				DB --> SI
10				DB --> SI
11				DB --> SI
12				DB --> SI
13				DB --> SI
14				DB --> SI
15				DB --> SI
16				DB --> SI
17				DB --> SI
18				DB --> SI
19				DB --> SI
20				DB --> SI
21				DB --> SI
22				DB --> SI
23				DB --> SI
24				DB --> SI
25				DB --> SI
26				DB --> SI
27				DB --> SI
28				DB --> SI
29				DB --> SI

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3

2

1

Rev 0.3

Version Change List (P. I. R. List) for HW Circuit

Item	Change Item	Page	Date	Phase	
1	Change R296 R337 R value	24	Follow conexant new design rule	8/6	SI --> FV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	Follow conexant new design rule	8/6	SI --> FV
3	Change PIRQ from F to A	18	Choose R419 then control PIRQ A	8/14	SI --> FV
4	Connect PCI_SERR# to EC GPIO pin.	18	Connect PCI_SERR# to EC GPIO pin.	8/31	SI --> FV
5	Modify PC BEEP circuit.	20	Modify PC BEEP circuit.	8/31	SI --> FV
6	For support Intel Penryn CPU.	04	Reserve R426 and R427 for support Intel Penryn CPU.	9/3	SI --> FV
7	For ESD request.	28	Add U22 and U23 for ESD request.	9/3	SI --> FV
8	For EMI request.	26	Add L24-L27	9/5	SI --> FV
9	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	Change C391, C393, C395, C396 from 0.47uF to 0.047uF	9/7	SI --> FV
10	Add R417 and R418 to fine-tune Vp-p.	26	Add R417 and R418 to fine-tune Vp-p.	9/7	SI --> FV
11	For ESD request.	20	Add U22 and U23 for ESD request.	9/7	SI --> FV
12					SI --> FV
13					SI --> FV
14					SI --> FV
15					SI --> FV
16					SI --> FV
17					SI --> FV
18					SI --> FV
19					SI --> FV
20					SI --> FV
21					SI --> FV
22					SI --> FV
23					SI --> FV
24					SI --> FV
25					SI --> FV
26					SI --> FV
27					SI --> FV
28					SI --> FV
29					SI --> FV
30					SI --> FV
31					SI --> FV
32					SI --> FV
33					SI --> FV
34					SI --> FV
35					SI --> FV
36					SI --> FV
37					SI --> FV
38					SI --> FV

Security Classification	Compal Secret Data		Title	
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Solve Vref miss when entry S3 mode.	7	Stuff R43 and R46.	9/25	PV --> MV
2	Solve wave ripple on CRT and TV.	10	Change C439 from 0.47uF to 4.7uF.	9/25	PV --> MV
3	Solve RTC timing too exceed.	18	Change C262 and C263 from 12pF to 15pF.	9/25	PV --> MV
4	Reduce INT.MIC noise.	24	Add LFP (R429 and C452).	9/25	PV --> MV
5	Solve S3 resume fail when use Micron DDR module.	35	Add PR169 to separate V_DDR_MCH_REF from P08.	10/05	PV --> MV
6	Solve pop noise when entry or resume from S3.	24	Modify FC Beep (C373, R302, R306) circuit.	9/27	PV --> MV
7	Solve EMI fail for Memory module.	7	Change R34/R35 from 20 ohm to 30 ohm.	9/27	PV --> MV
8	Fine-tune LED brightness.	28	Change R329, R331, R333, R335 from 33 ohm to 27 ohm.	9/27	PV --> MV
9	ICH 1.5V power rail 700mA current requirement.	21	Change R252 package from 0603 to 0805.	10/04	PV --> MV
10	Solve can not power on when stuff U22.	28	Disconnect ON/OFFBTN# and ON/OFFBTN_LED# from U22.	10/05	PV --> MV
11	For EMI request.	16	Change L2, L3, L4 to FBMA-L10-201209-121LMT_0805.	10/19	PV --> MV
12	To avoid too easy to open solder for CLR2.	15	Change CLR2P1 and CLR2P2 type like the same as PJP4.	10/19	PV --> MV
13	Solve acoustic noise issue.	10	Change R64, R79, R81 from 0 ohm to 1uH/400mA inductor.	10/22	PV --> MV

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