

# Compal confidential

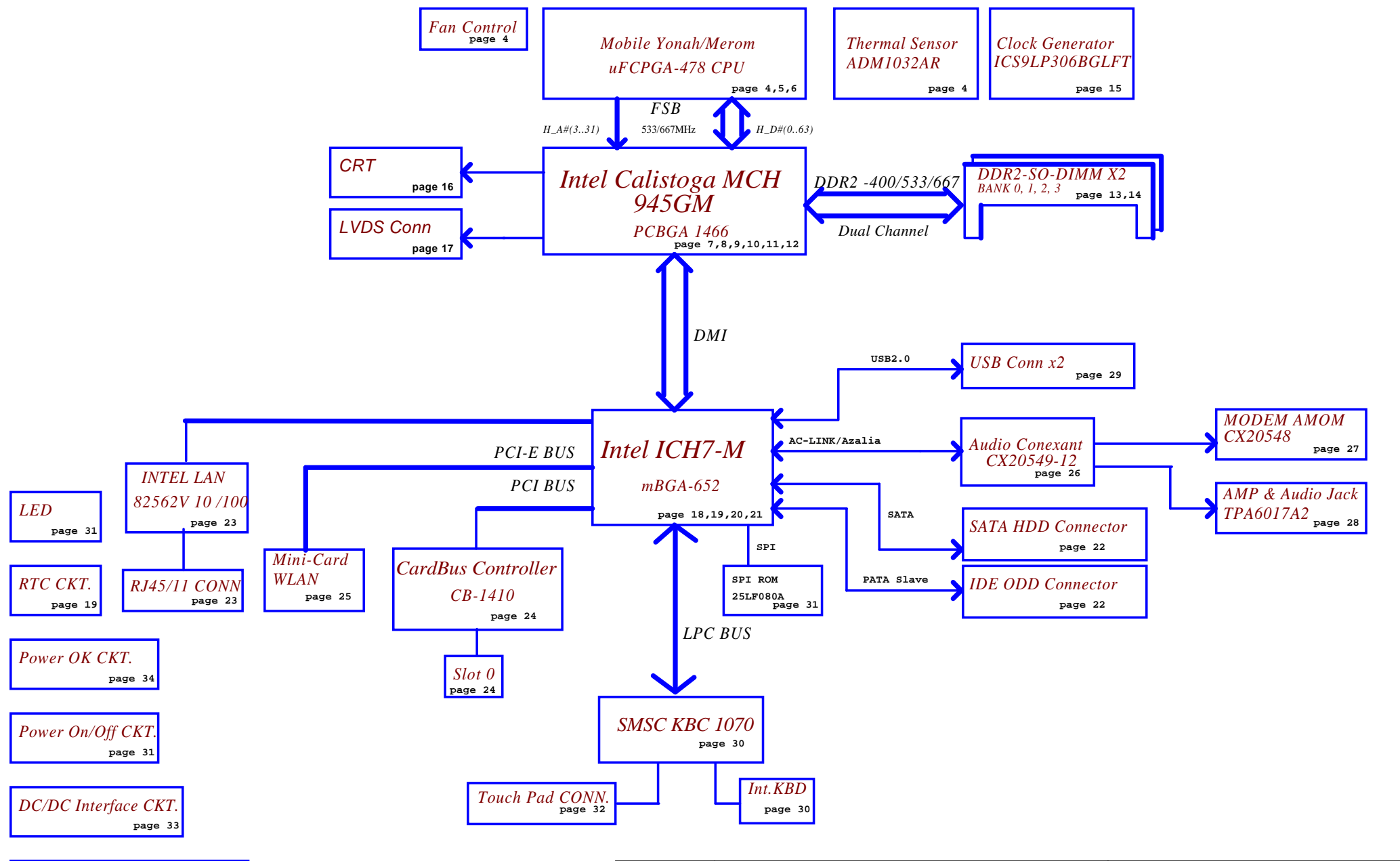
## Schematics Document Mobile Yonah uFCPGA with Intel Calistoga\_GM+ ICH7-M core logic

2007-03-20

REV:0.5

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				Custom	LA-349IP	0.5
Date: Tuesday, March 20, 2007				Sheet	1	of 47

# Volga 2.0



**Power Circuit DC/DC**  
Page 37, 38, 39, 40

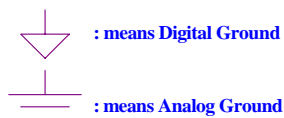
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				Document Number	0.5
				LA-3491P	
				Date: Tuesday, March 20, 2007	Sheet 2 of 47

## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## Symbol Note :



NOXDP@ : means just build when XDP function disable.

LP@ : means just build when Low power clock gen. install

BATT@ : means need be mounted when 45 level assy or rework stage.

45@ : means need be mounted when 45 level assy or rework stage.

14@ : means need be mounted when 14.1"

WLAN@ : means need be mounted when have wireless LED Function

WLAN14@ : means need be mounted when have wireless LED Function and 14"

XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

CONN@ : means ME parts

Debug@ : means Mini debug card use

**Calistoga 945GM R3 SA0000059L0**

**Calistoga 945GM R1 SA0000059A0**

**Calistoga 940GML R3 SA000011C10**

**Calistoga 940GML R1 SA000011C00**

**ICH7 R3 SA00000V1A0**

**ICH7 R1 SA00000V1F0**

**IAT50 945GM FF 46147932L01**

**IAT50 940GML DF 46147932L02**

**IAT50 940GML DF 46147932L03 (No WLAN)**

**IAT60 945GM FF 46147932L21**

**IAT60 940GML DF 46147932L22**

**IAT60 940GML DF 46147932L23 (No WLAN)**

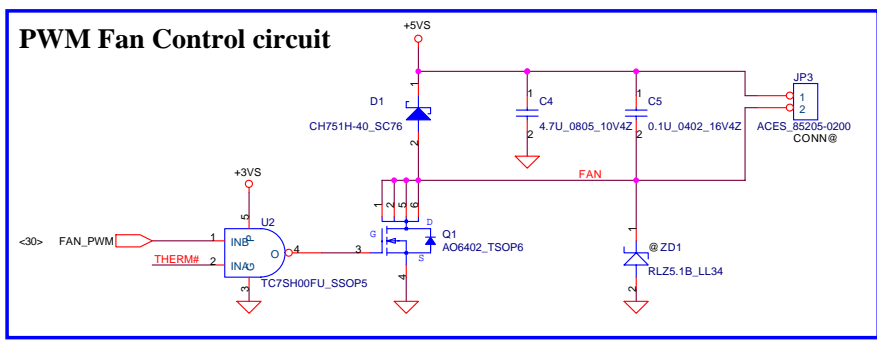
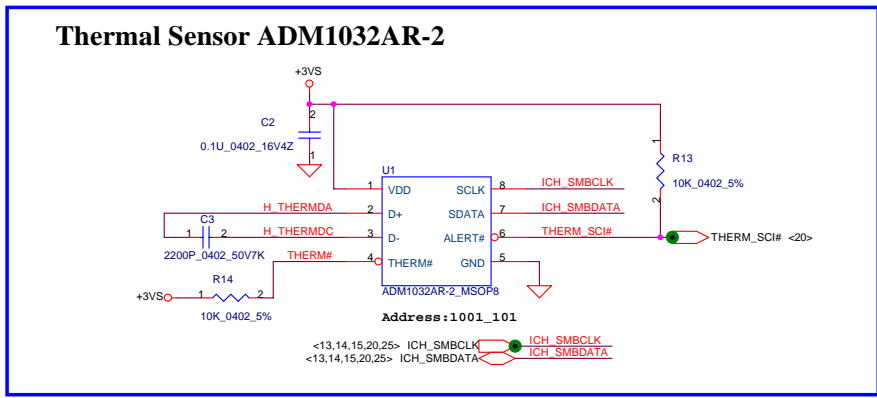
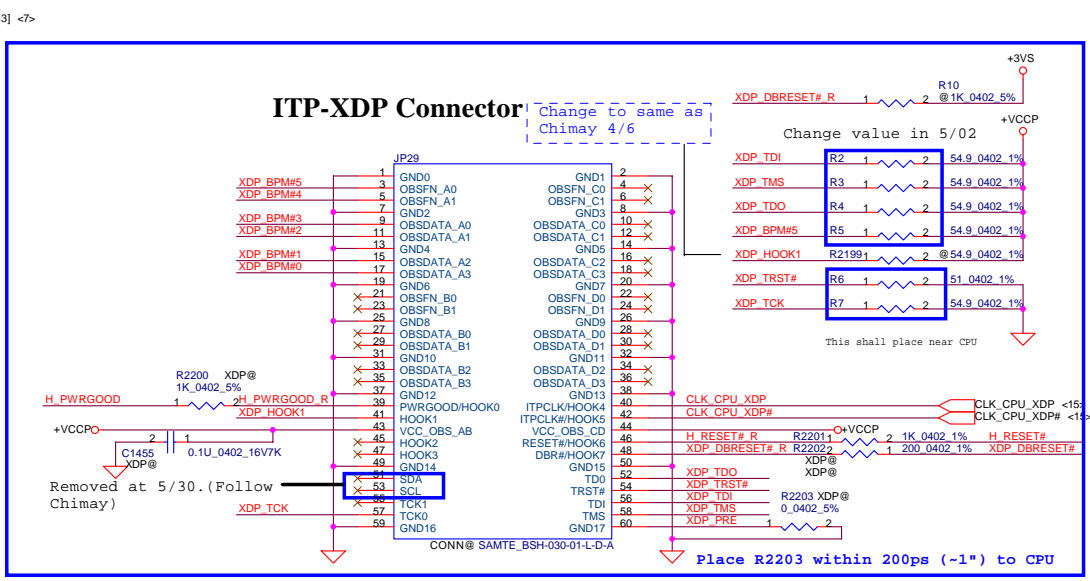
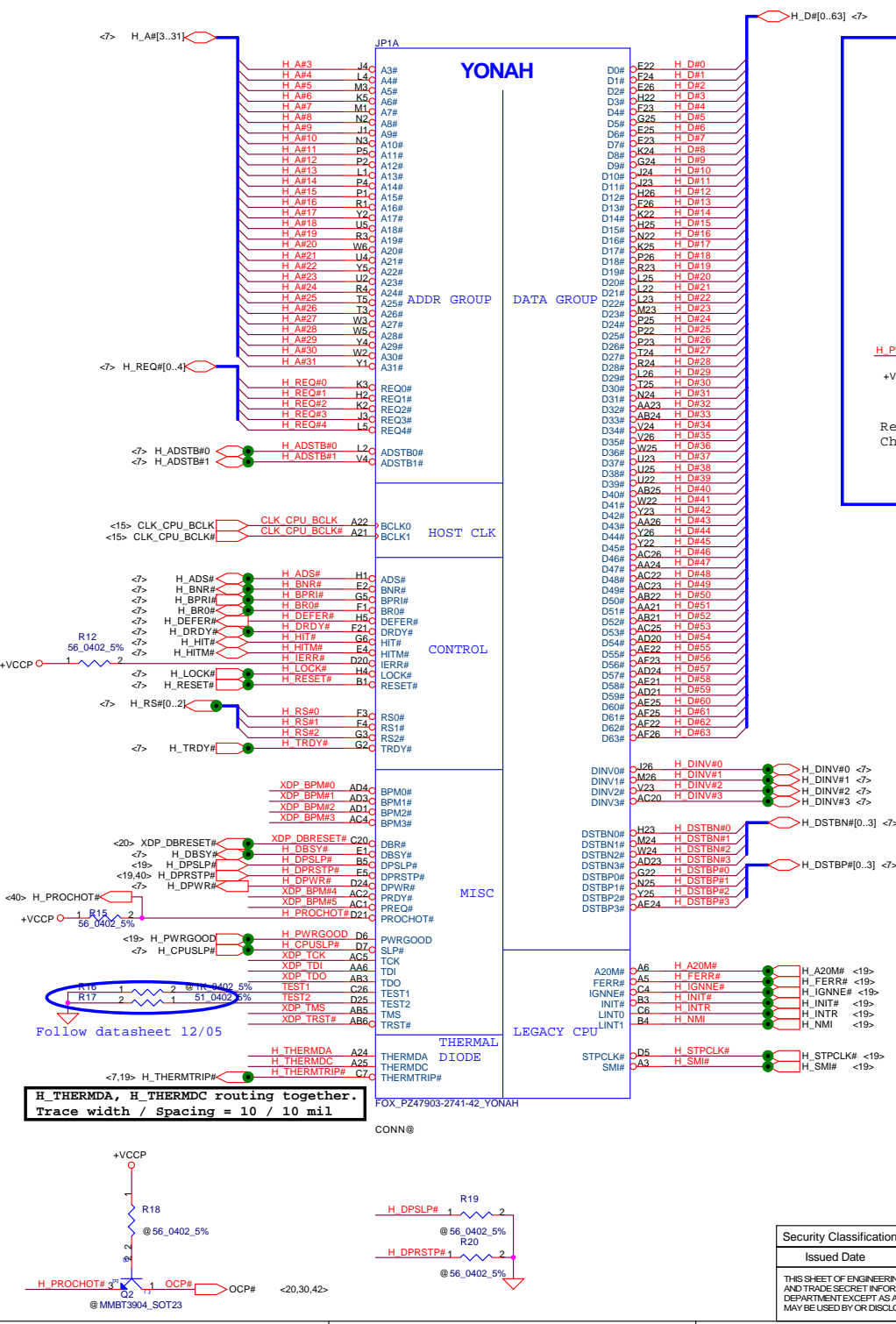
## External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C

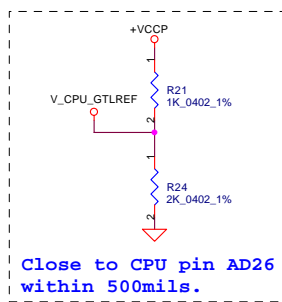
## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

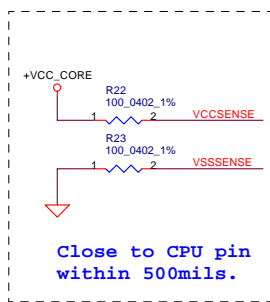
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					LA-3491P	0.5
Date: Tuesday, March 20, 2007				Sheet 3 of 47		



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Issued Date	2006/10/26	Deciphered Date	2006/07/26	Compal Electronics, Inc.	
				Yonah CPU in mFCPGA479	
Size	Document Number	Date		Rev	
	LA-3491P	Tuesday, March 20, 2007		0.5	
				Sheet	4 of 47

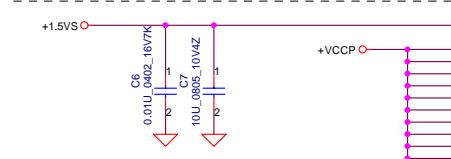


Close to CPU pin AD26 within 500mils.



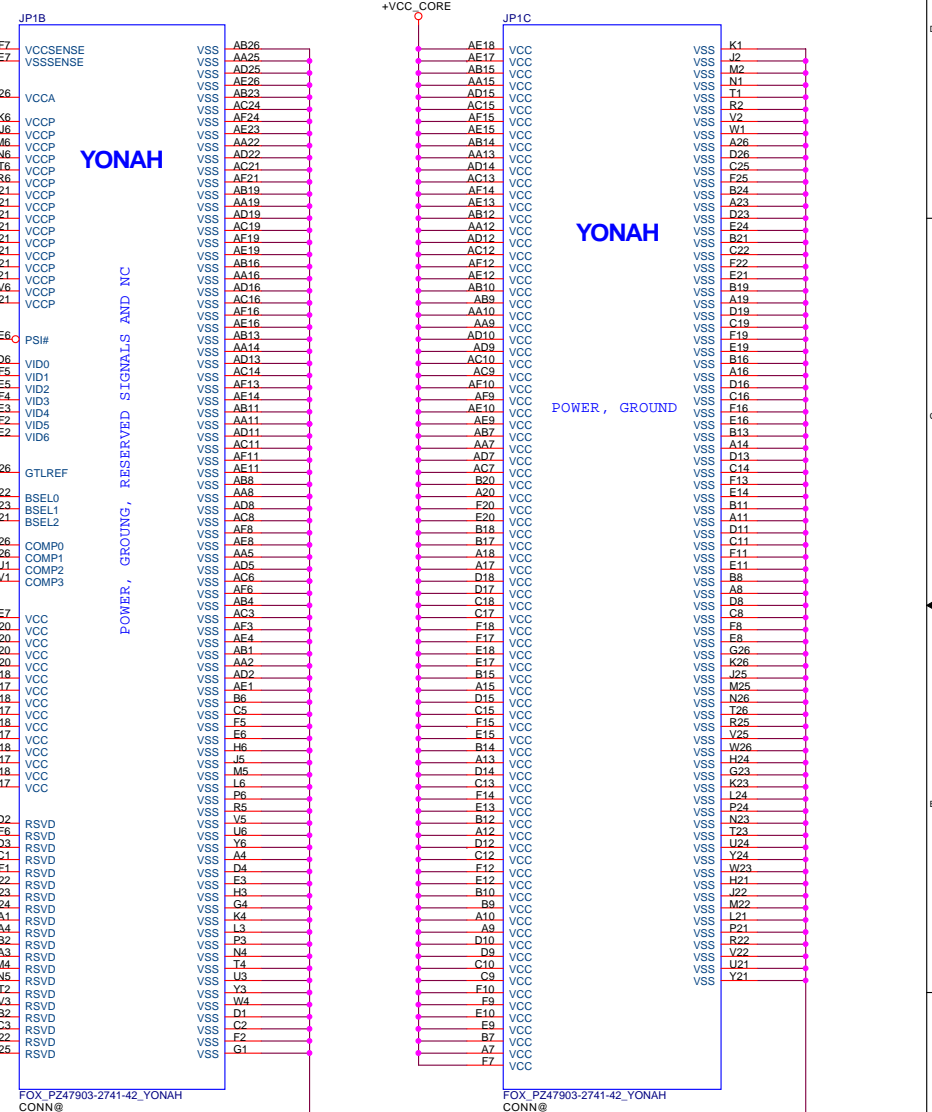
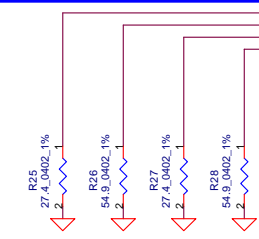
Close to CPU pin within 500mils.

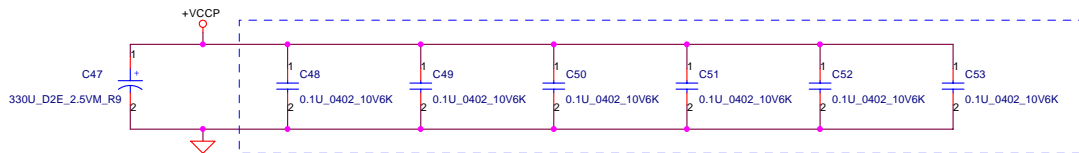
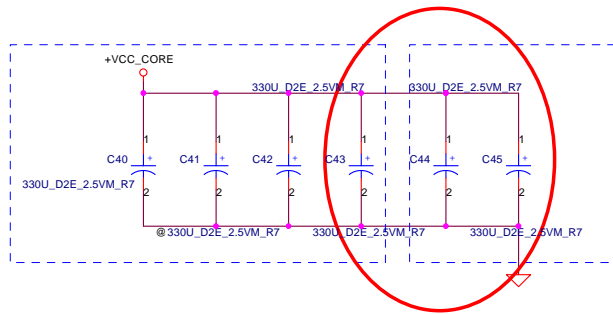
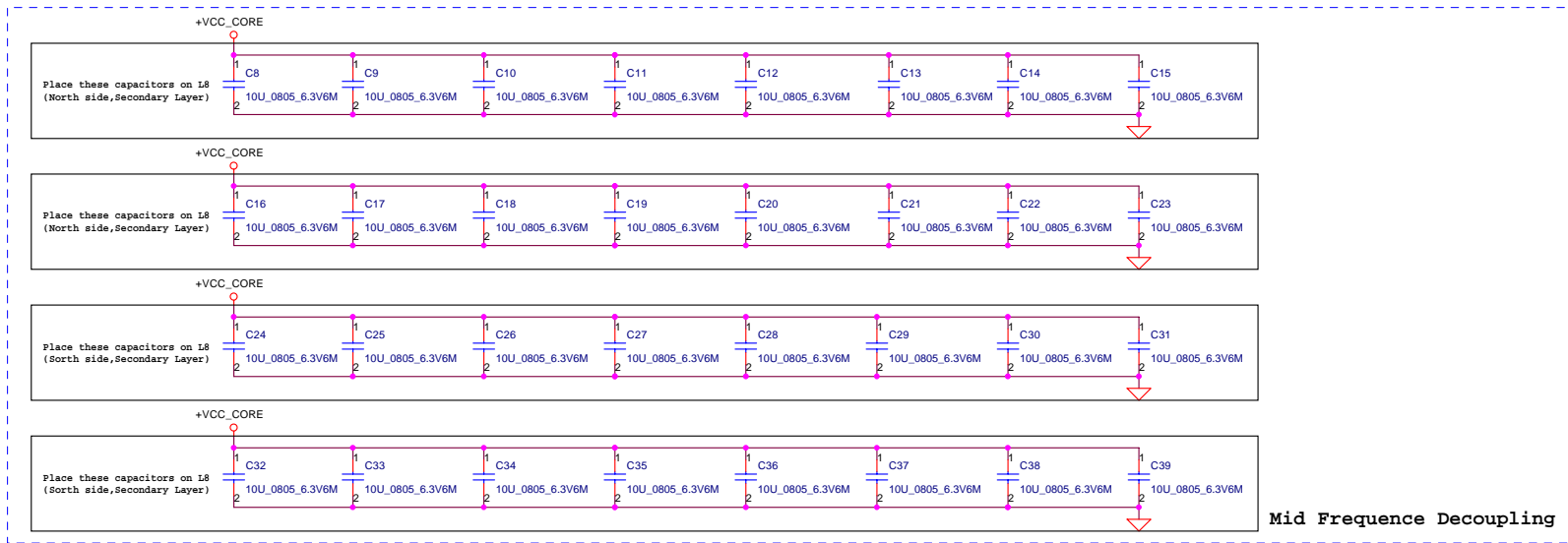
Length match within 25 mils  
The trace width 18 mils space  
7 mils



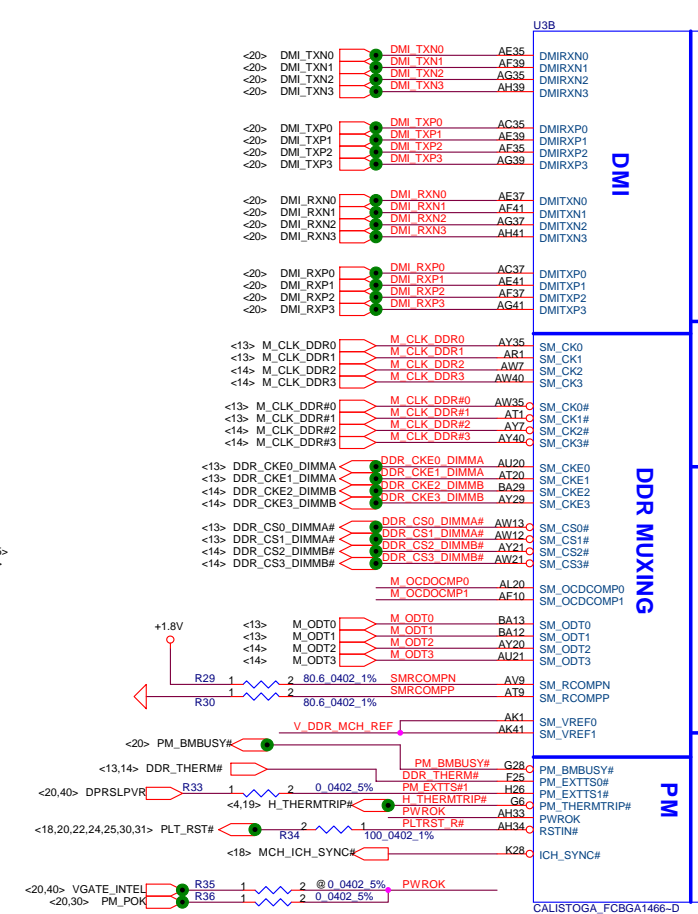
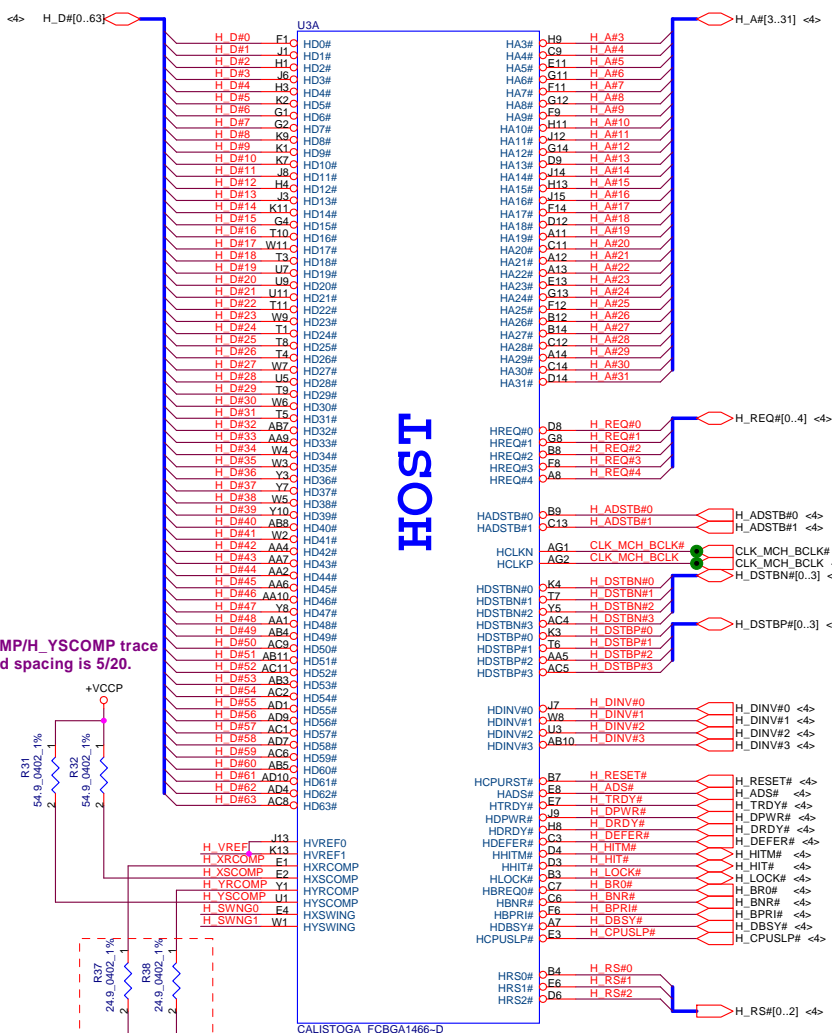
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.





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				Size	Document Number
Date: Tuesday, March 20, 2007				Sheet	6 of 47



Description at pagell.

H\_XSCOMP/H\_YSCOMP trace width and spacing is 5/20.

Layout Note:  
H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 18/20.

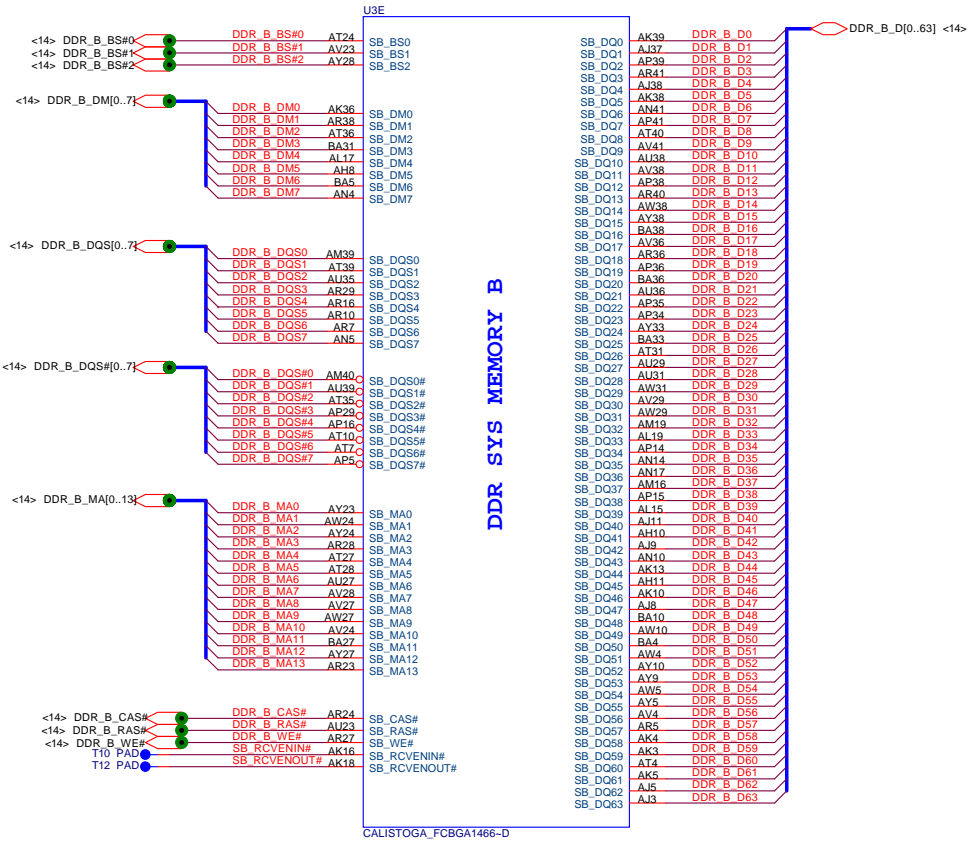
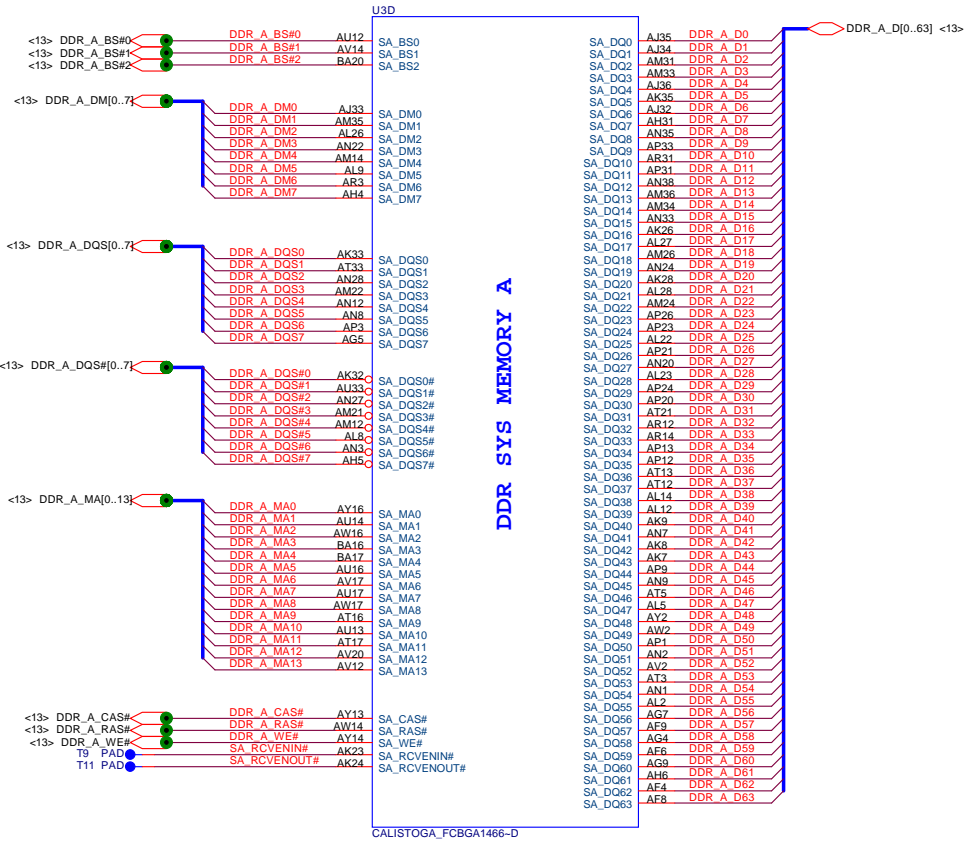
Layout Note:  
V\_DDR\_MCH\_REF trace width and spacing is 20/20.

Layout Note:  
Route as short as possible

Stuff R42 & R43 for A1 Calistoga

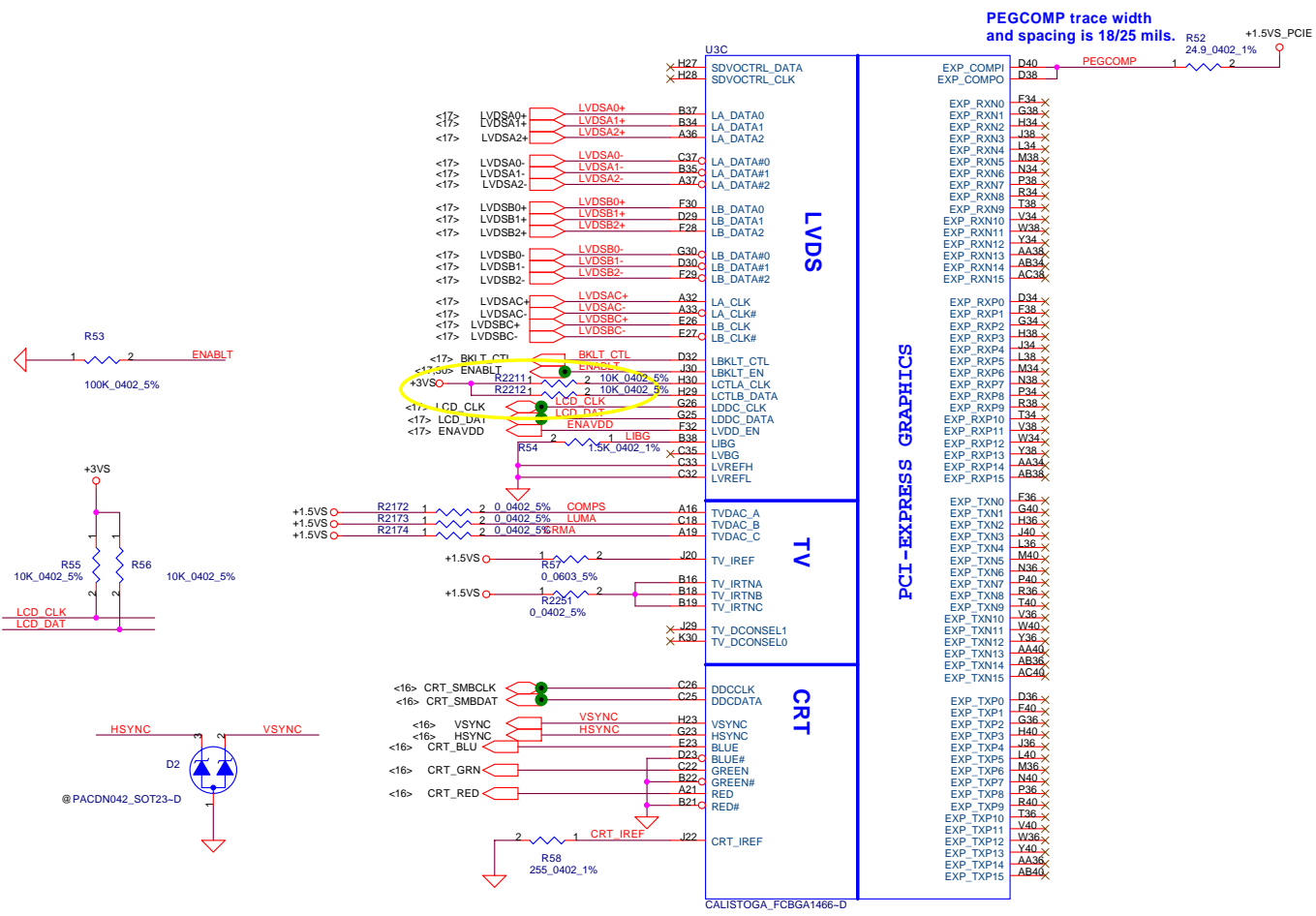
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Size	Document Number	Rev	
	LA-3491P	0.5	
Date:	Tuesday, March 20, 2007	Sheet	7 of 47

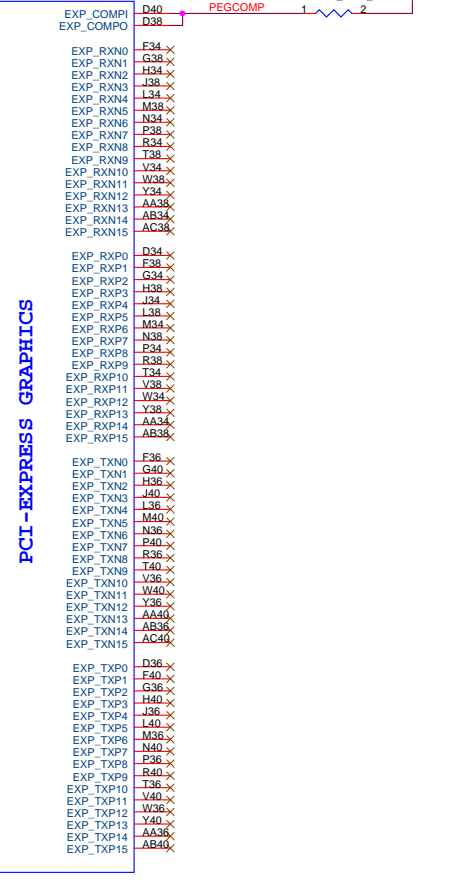


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				LA-3491P	Rev 0.5
Date:	Tuesday, March 20, 2007	Sheet	8	of	47





PEGCOMP trace width and spacing is 18/25 mils.

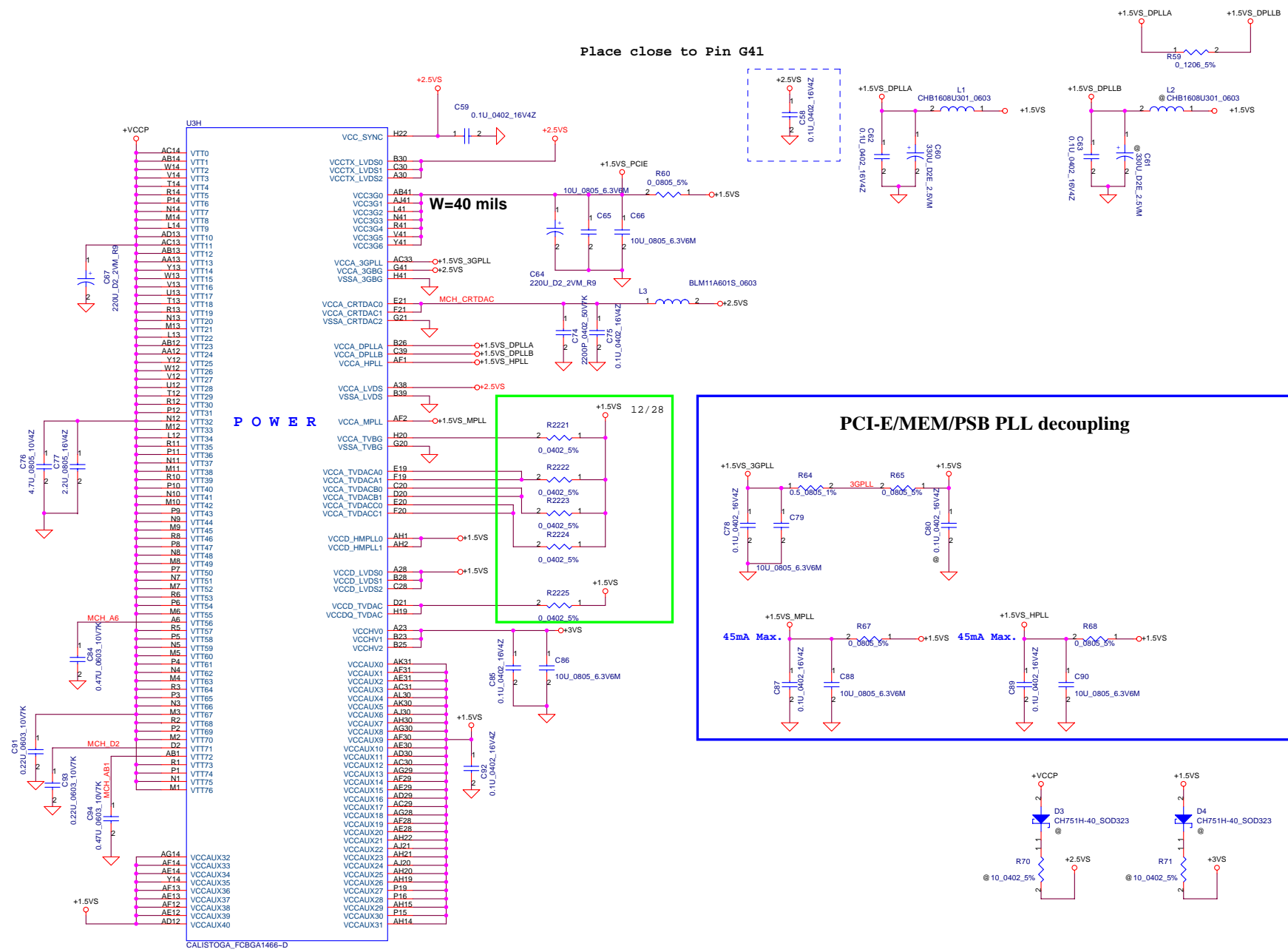


LVDS  
TV  
CRT  
PCI-EXPRESS GRAPHICS

CALISTOGA\_FC8GA1466-D

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Size	Document Number	Rev	
	LA-3491P	0.5	
Date:	Tuesday, March 20, 2007	Sheet	9 of 47



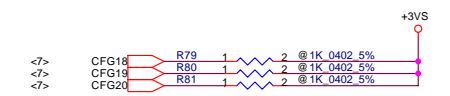
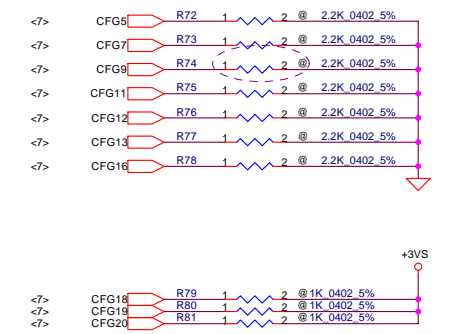
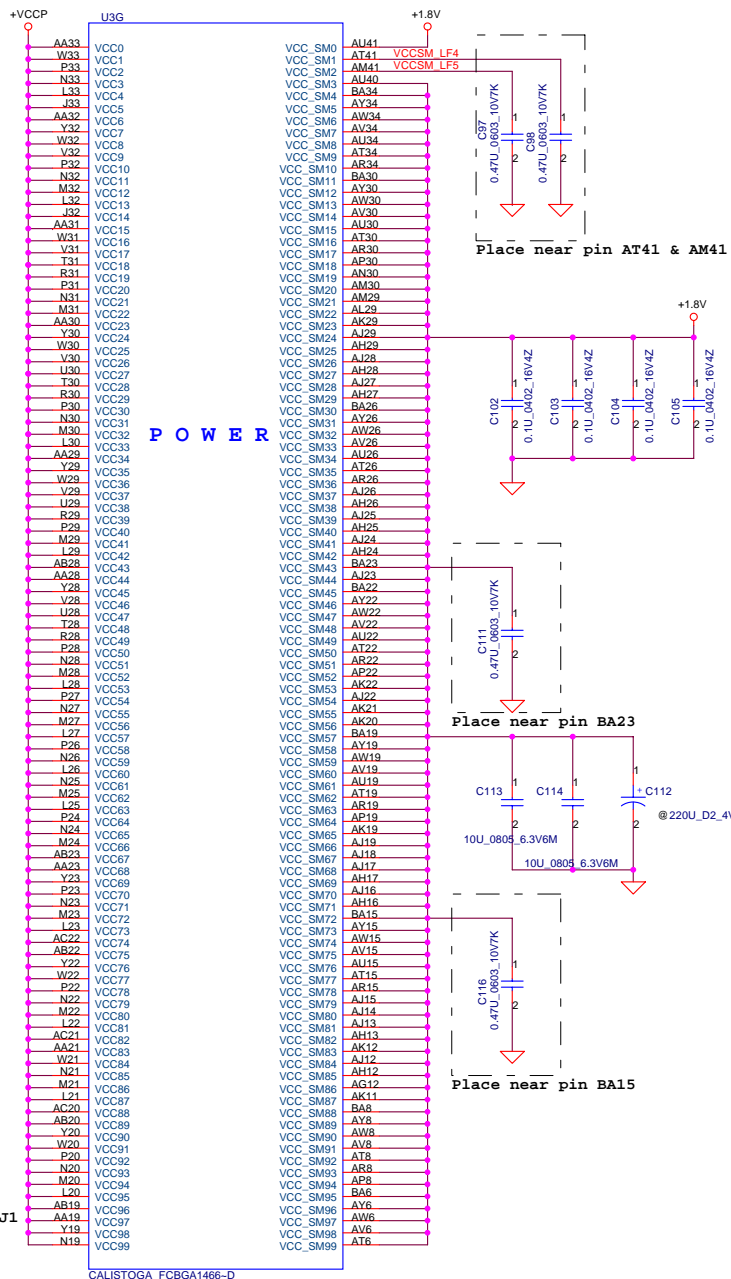
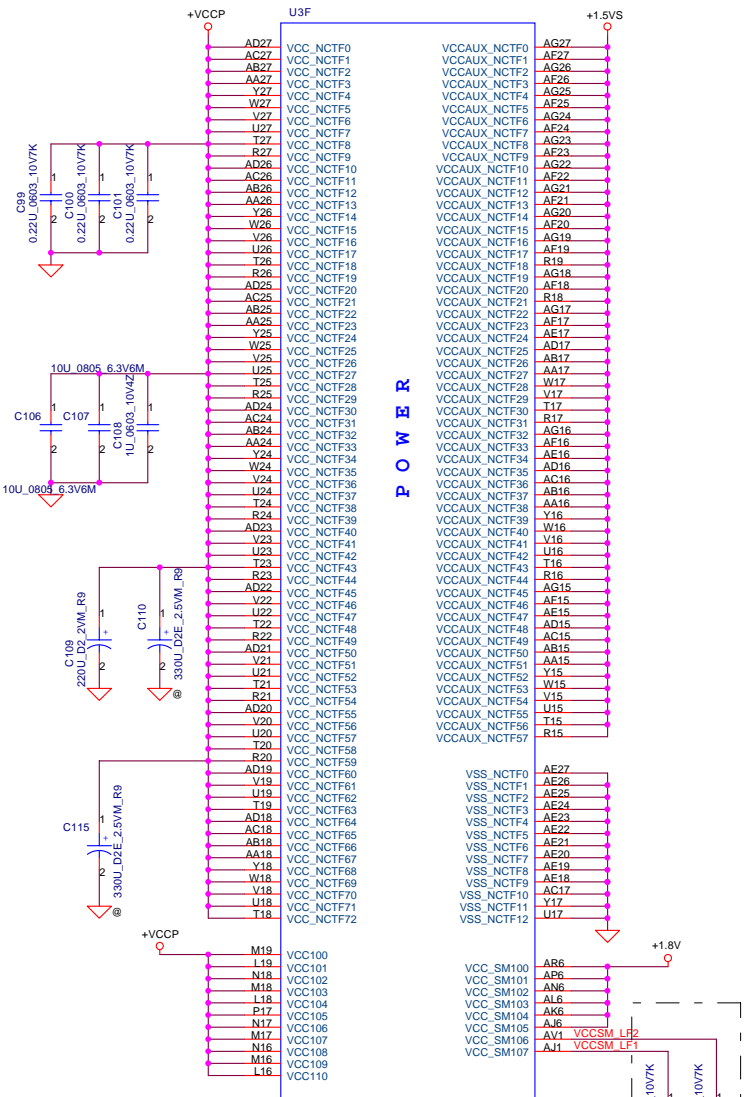
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Title	Calistoga (4/6)			
Size	Document Number	Rev		
	LA-3491P	0.5		
Date:	Tuesday, March 20, 2007	Sheet	10	of 47

# Strap Pin Table

CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

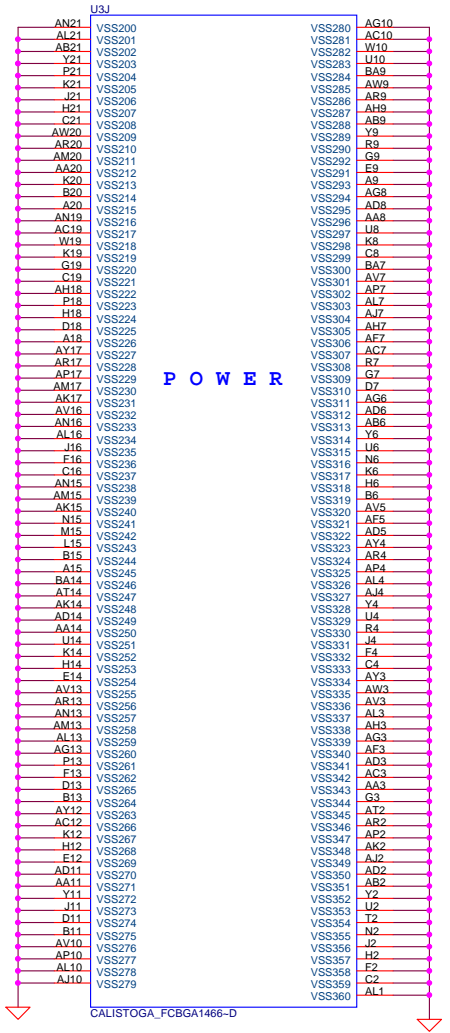
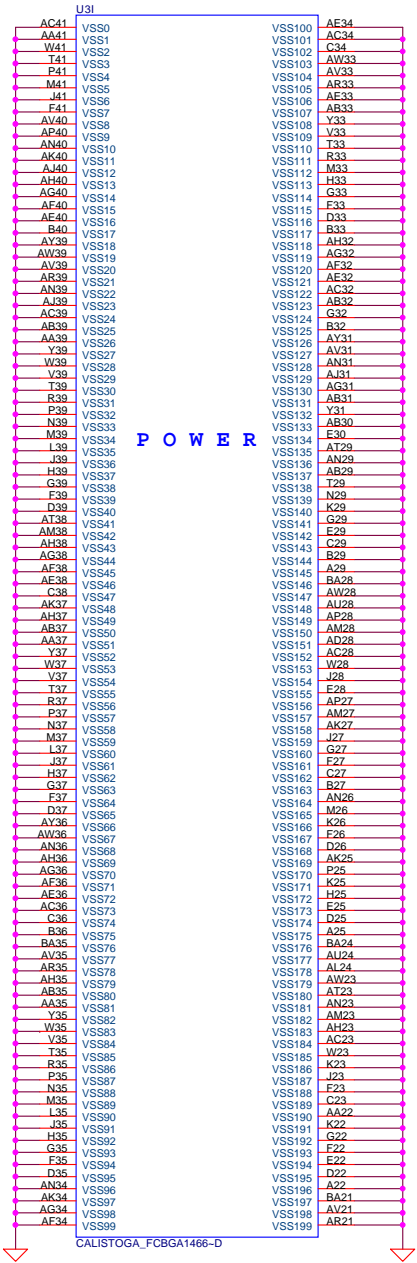
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal Operation *(Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-downs resistor #eqs)Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.



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Issued Date	2006/10/26	Deciphered Date
		2006/07/26

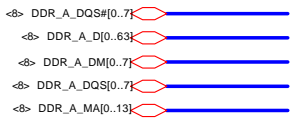
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		<b>Calistoga (5/6)</b>	
Size	Document Number	Rev	
	LA-3491P	0.5	
Date:	Tuesday, March 20, 2007	Sheet	11 of 47

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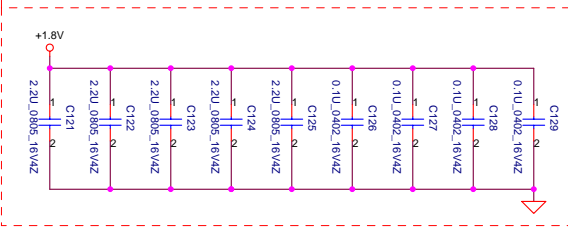


CALISTOGA\_FCBGA1466-D

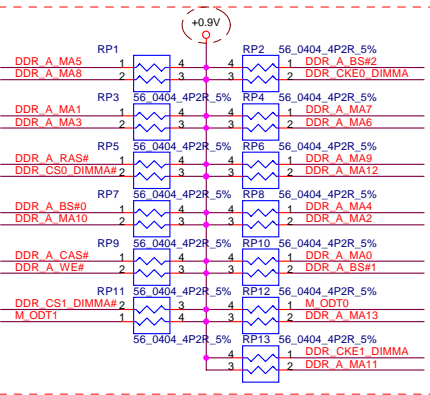
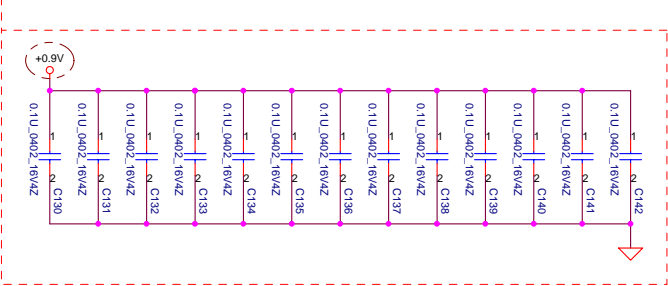
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	<b>Compal Electronics, Inc.</b>
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Date:	Tuesday, March 20, 2007	Sheet	12 of 47	



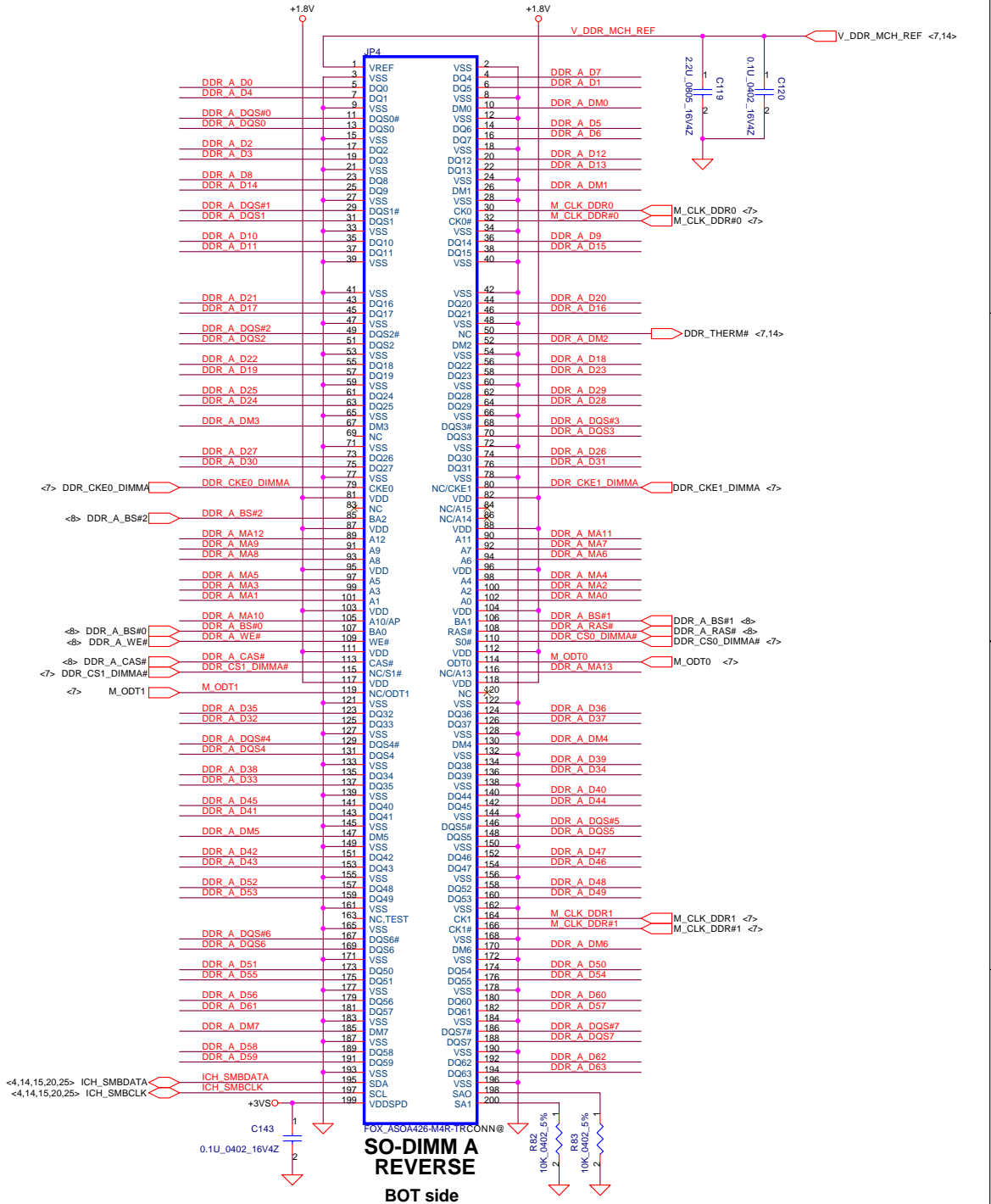
Layout Note:  
Place near JP4



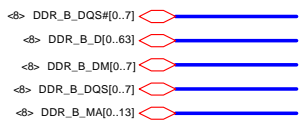
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V



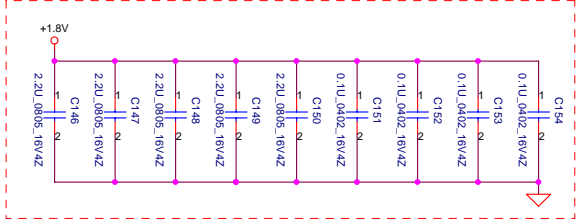
Layout Note:  
Place these resistor closely JP34, all trace length Max=1.5"



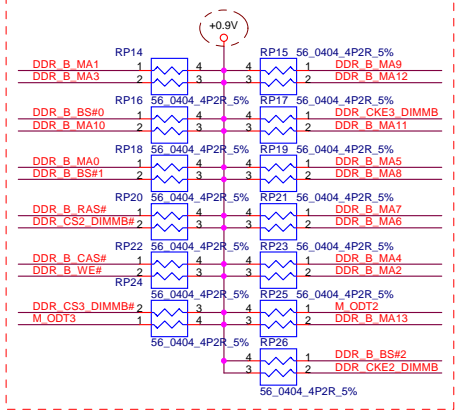
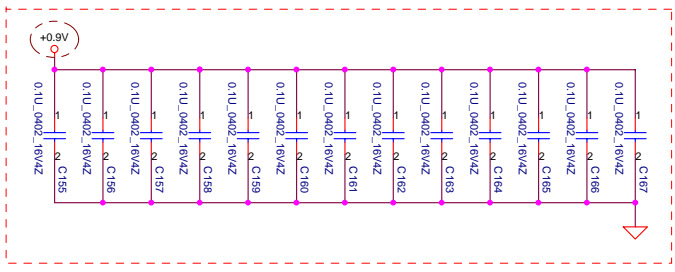
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Issued Date			2006/10/26	Deciphered Date		2006/07/26	Compal Electronics, Inc.		
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Date:			Tuesday, March 20, 2007	Sheet		13	of 47		



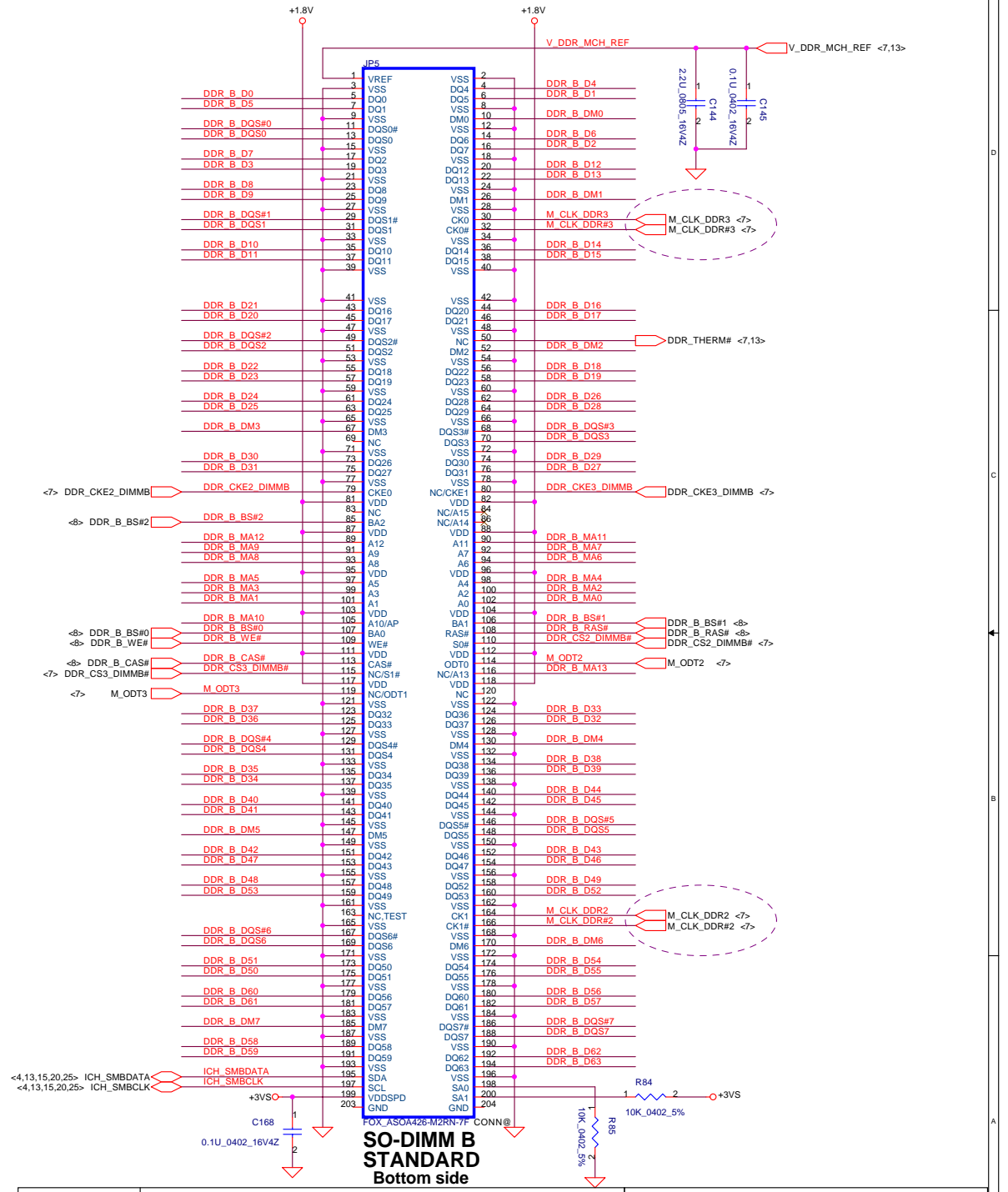
**Layout Note:**  
Place near JP34



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place these resistor closely JP10, all trace length Max=1.5"



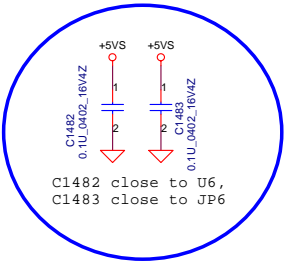
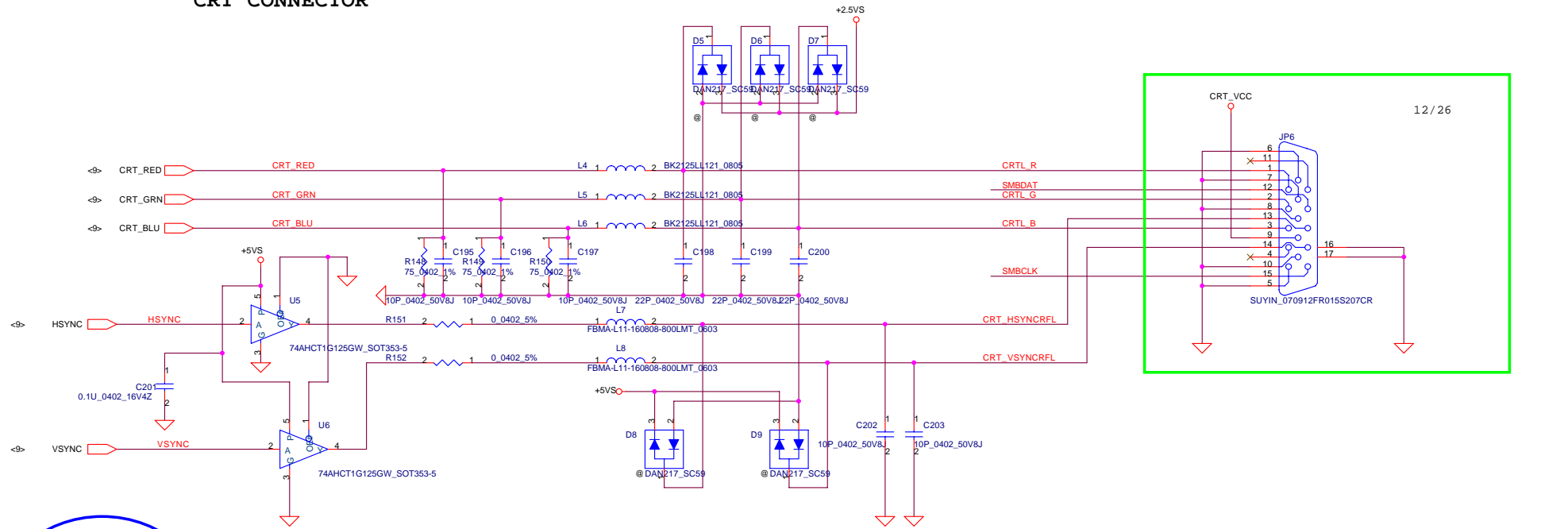
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	Title	
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				LA-3491P	
				Date:	Tuesday, March 20, 2007
				Sheet	14 of 47

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DDRII-SODIMM SLOT2		
Rev	0.5	

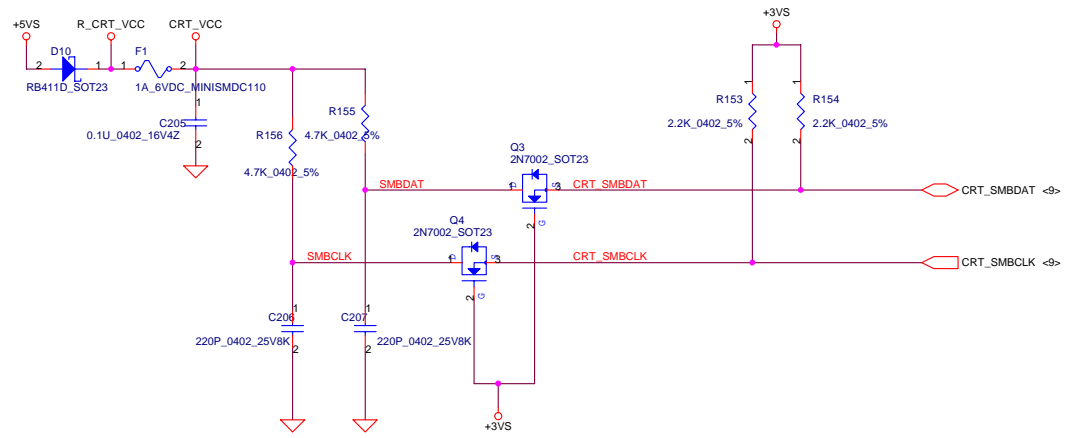




# CRT CONNECTOR



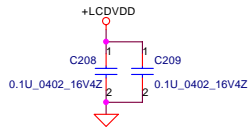
0119 HSYNC, VSYNC refernce +5VS



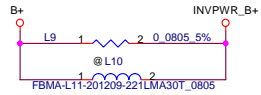
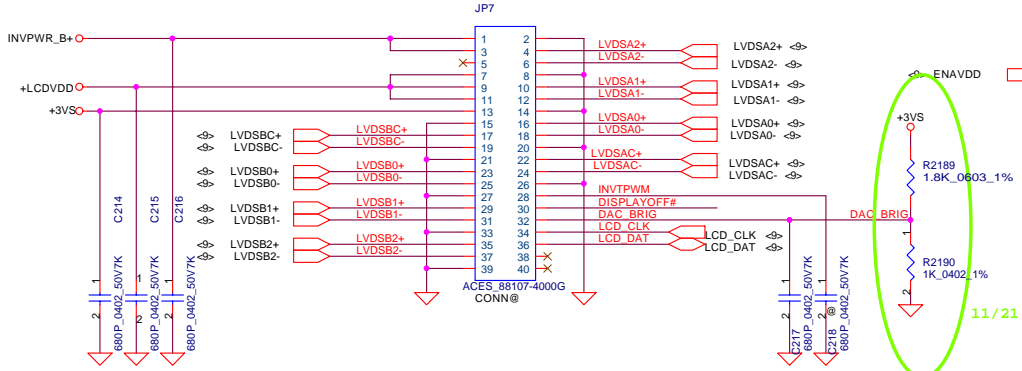
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				CRT Connector		
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					LA-3491P	0.5
				Date:	Tuesday, March 20, 2007	Sheet 16 of 47



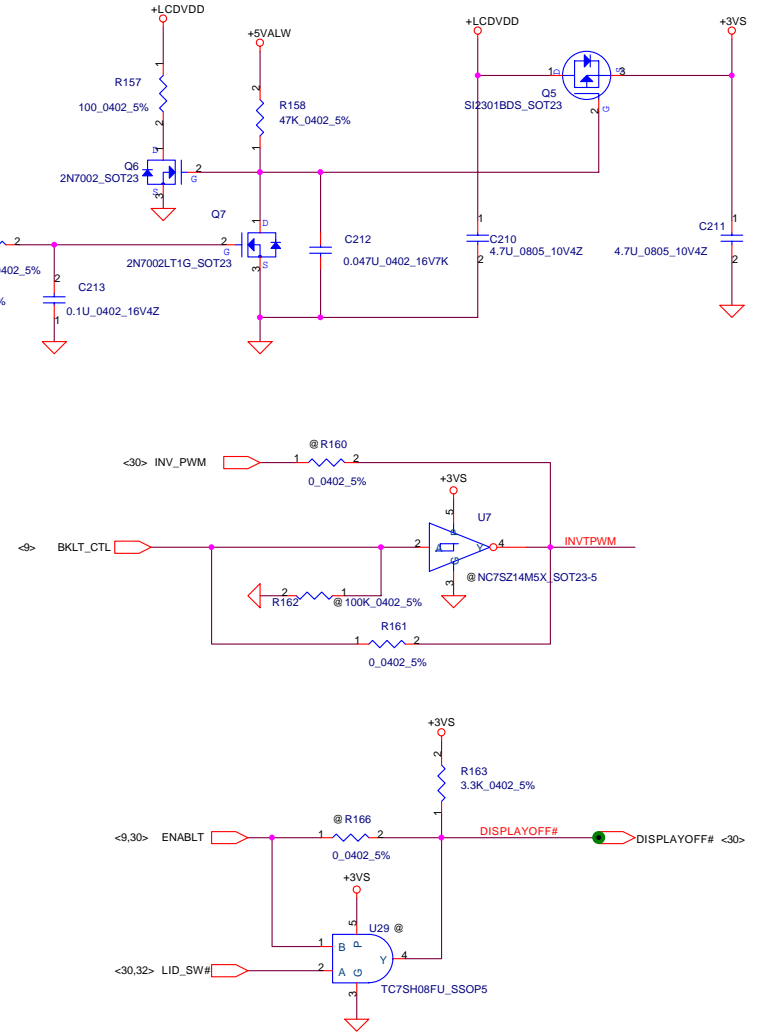
# LVDS CONN



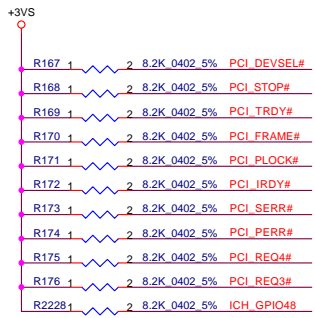
## LVDS connector



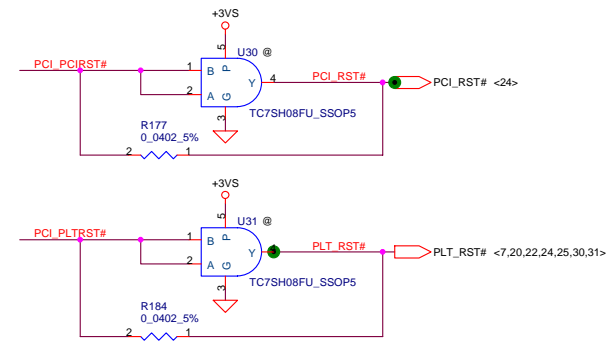
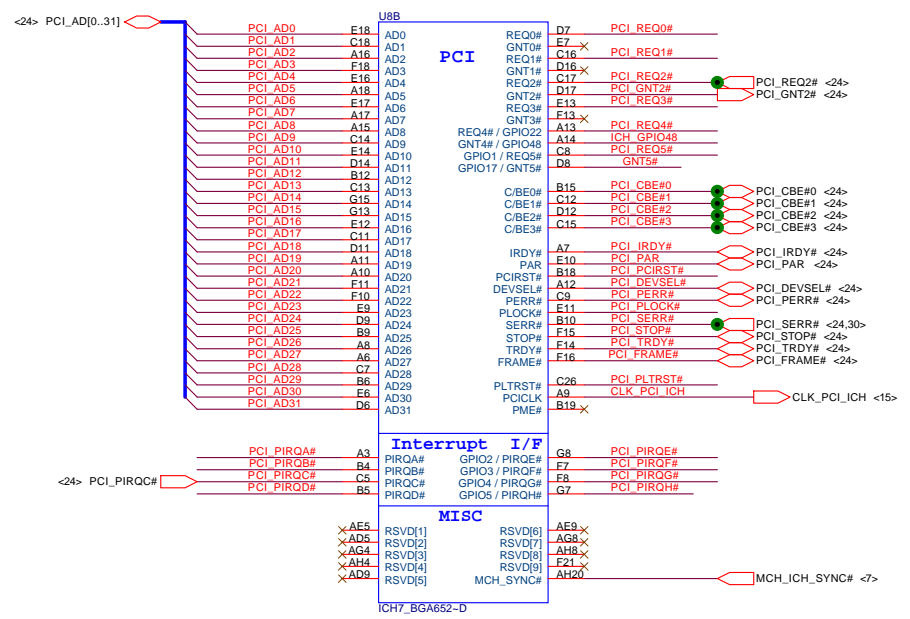
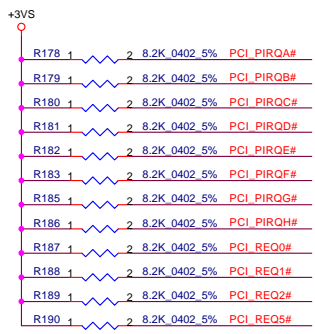
## LCD/PANEL BD. CONN.



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				LCD CONN.		
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					LA-3491P	0.5
				Date:	Tuesday, March 20, 2007	Sheet 17 of 47



Change to RP before SI phase

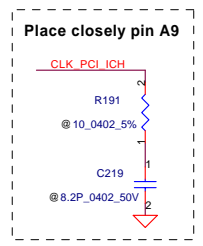


**GNT5# and GNT4# have internal pull high 20K**

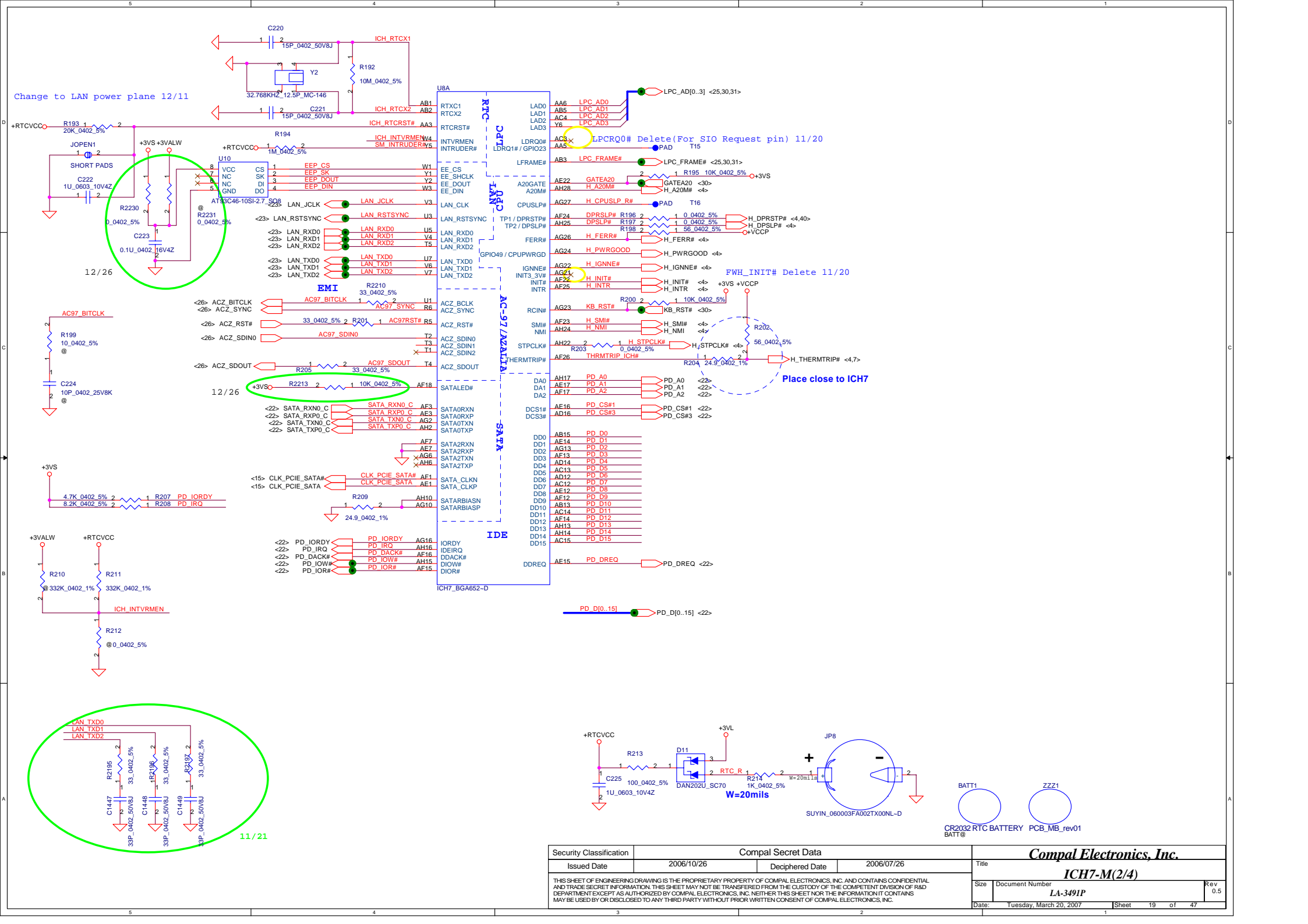
**Boot BIOS destination**

GNT5#	GNT4#	
0	1	SPI@ (Default)
1	0	PCI@
1	1	LPC@

The pad must be placed on PCB easily contact space for BIOS team setting.



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Size	Document Number	Rev	Date: Tuesday, March 20, 2007   Sheet 18 of 47		
	LA-3491P	0.5			

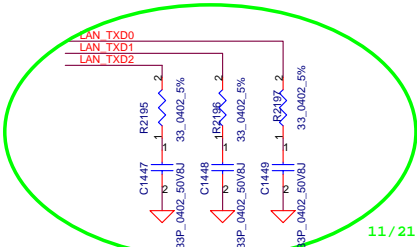


Change to LAN power plane 12/11

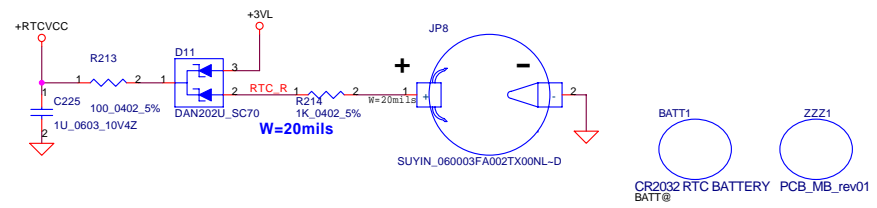
LPCRQ0# Delete (For SIO Request pin) 11/20

FWH\_INIT# Delete 11/20

Place close to ICH7



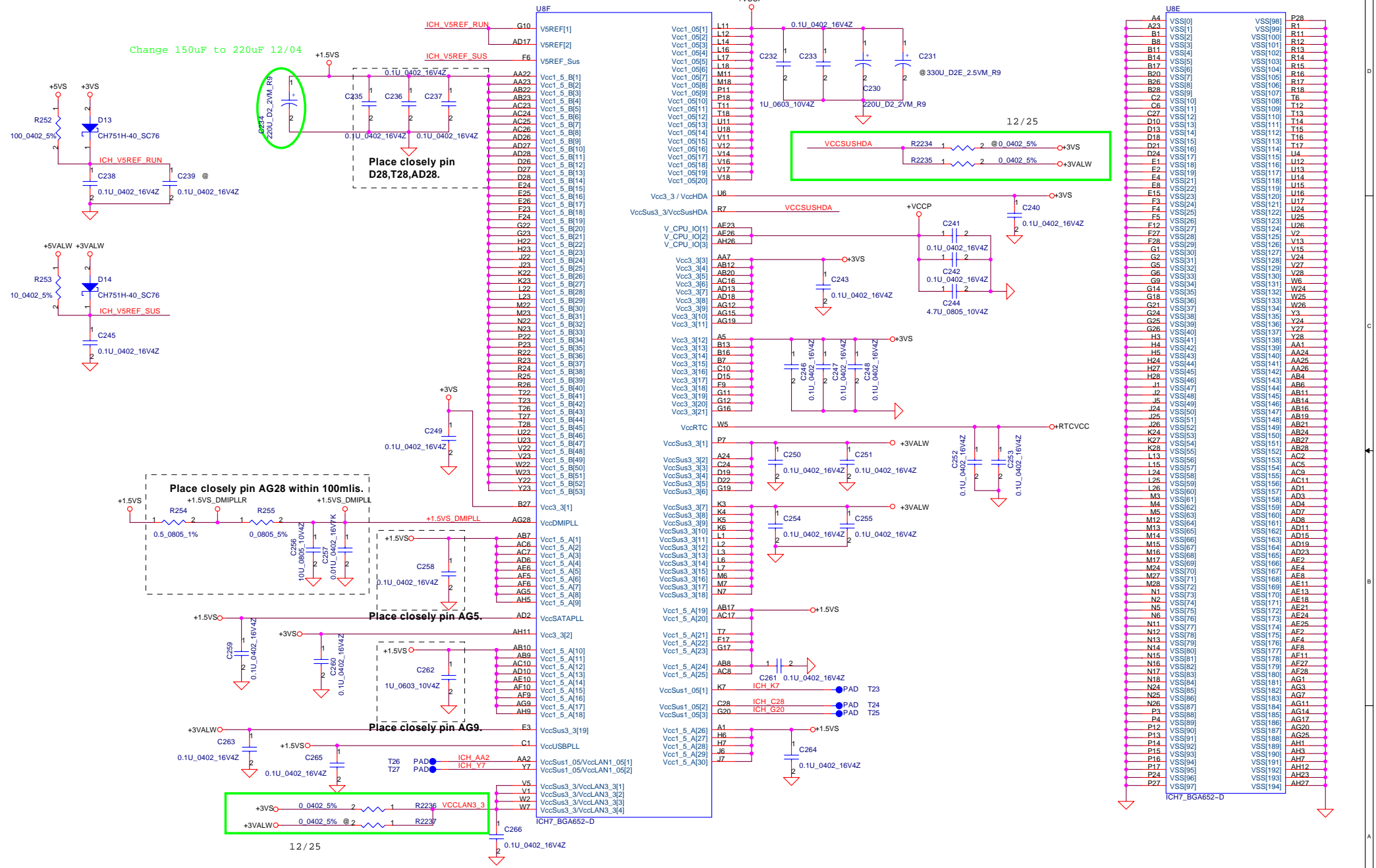
11 / 21



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				LA-3491P	Rev 0.5
Date:	Tuesday, March 20, 2007	Sheet	19	of	47



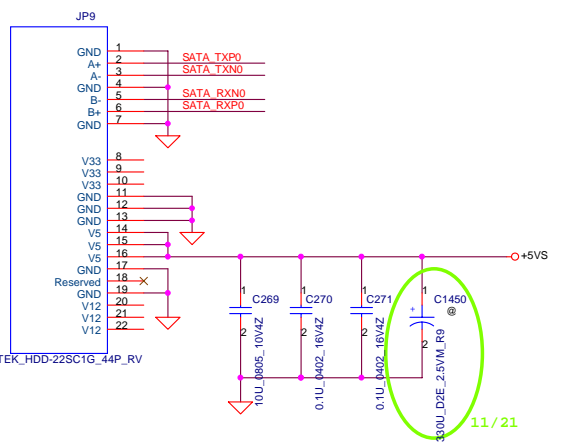
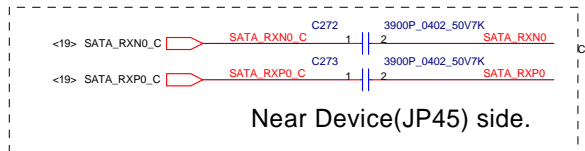
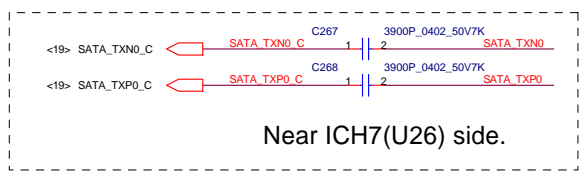
Change 150uF to 220uF 12/04



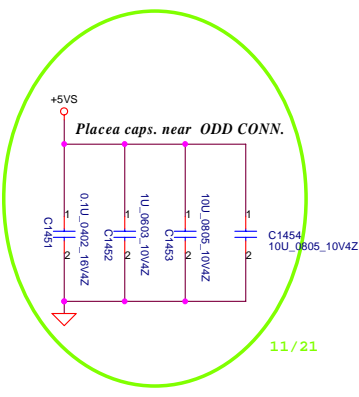
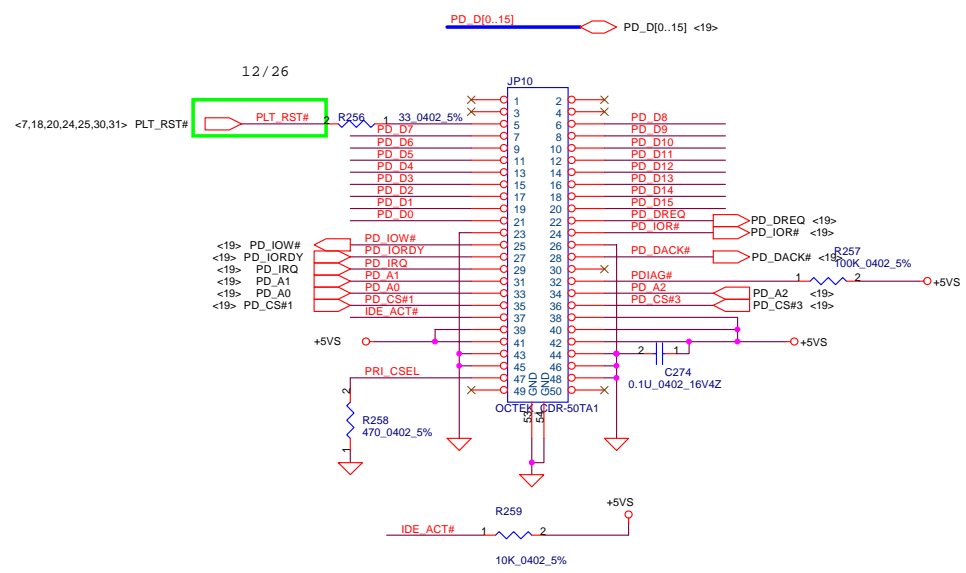
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Date:	Tuesday, March 20, 2007	Sheet	21	of	47

### SATA CONN



### CD-ROM Connector

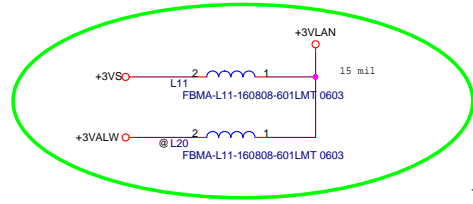
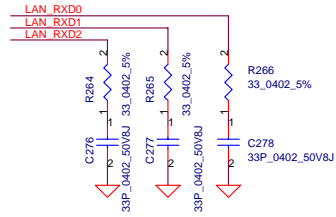
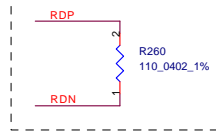
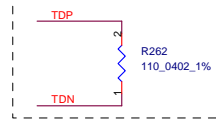
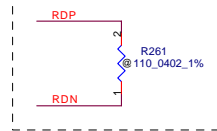


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				LA-3491P	0.5
Date:	Tuesday, March 20, 2007	Sheet	22	of	47

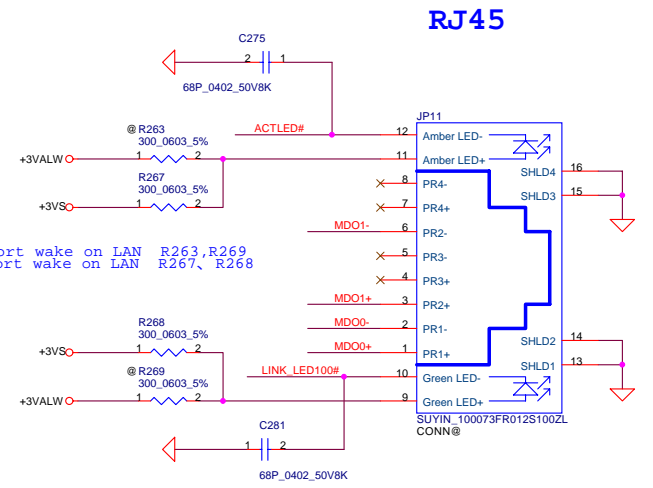
close to U12chip(Intel rule)

close to U12chip(Intel rule)

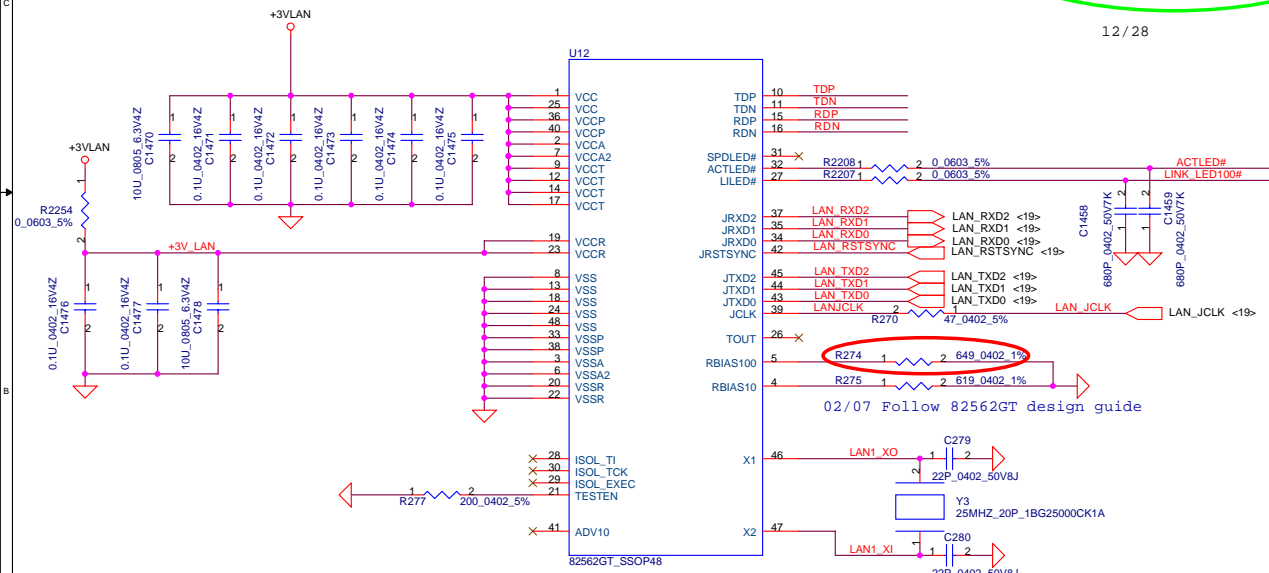
close to U13



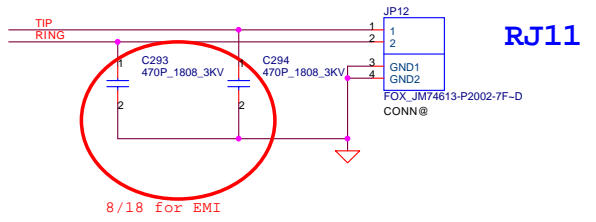
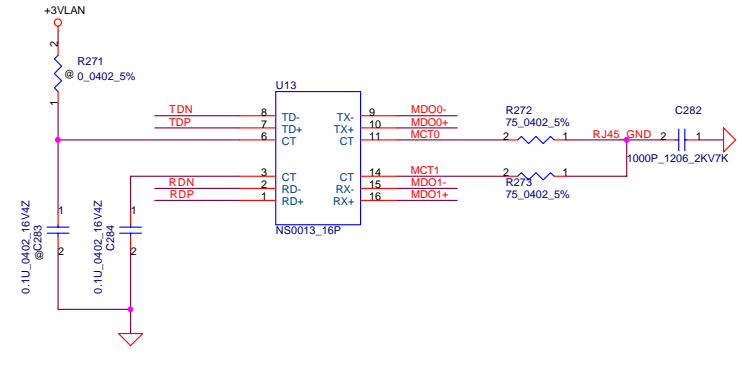
12 / 28



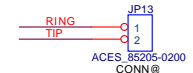
Support wake on LAN R263, R269  
Don't Support wake on LAN R267, R268



02/07 Follow 82562GT design guide



8/18 for EMI

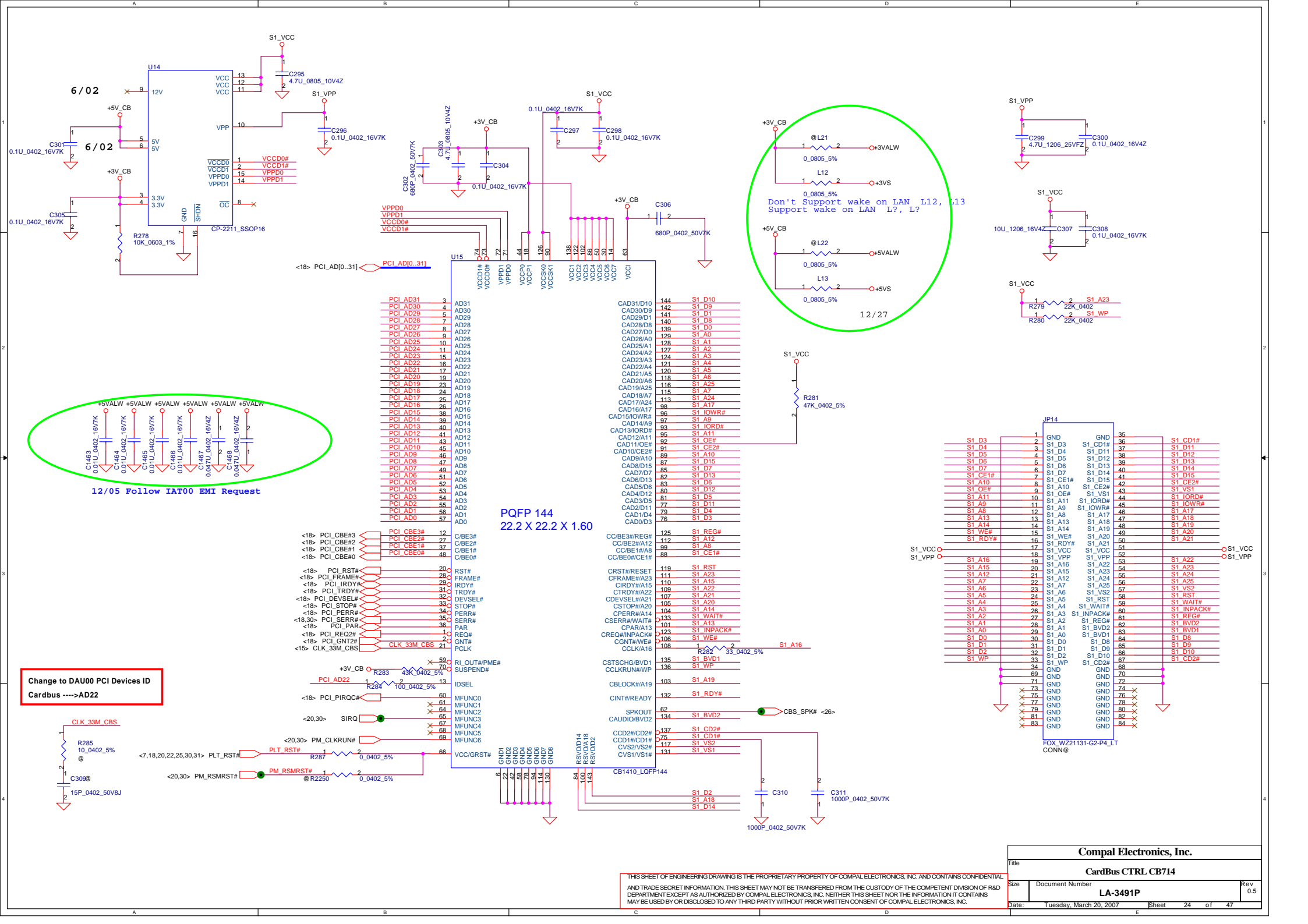


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Title			
82562EZ LAN			
Size	Document Number	Rev	
Custom	LA-3491P	0.5	
Date:	Tuesday, March 20, 2007	Sheet	23 of 47

Compal Electronics, Inc.





Change to DAU00 PCI Devices ID  
Cardbus ---->AD22

Don't Support wake on LAN L12, L13  
Support wake on LAN L7, L?

12/05 Follow IAT00 EMI Request

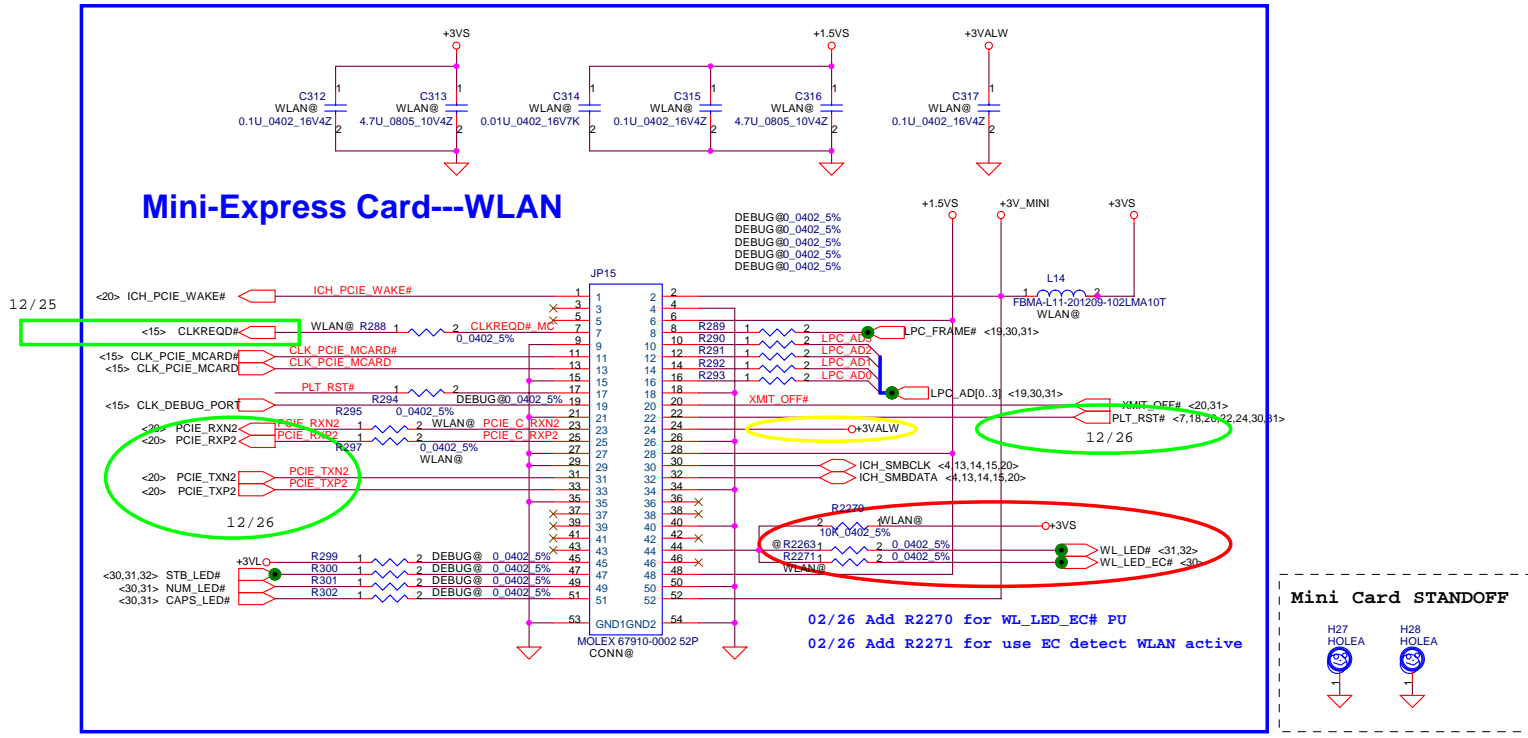
PCI AD31	3	AD31	CAD31/D10	144	S1 D10
PCI AD30	4	AD30	CAD30/D9	142	S1 D9
PCI AD29	5	AD29	CAD29/D8	141	S1 D8
PCI AD28	6	AD28	CAD28/D7	140	S1 D7
PCI AD27	7	AD27	CAD27/D6	139	S1 D6
PCI AD26	8	AD26	CAD26/A0	129	S1 A0
PCI AD25	9	AD25	CAD25/A1	128	S1 A2
PCI AD24	10	AD24	CAD24/A2	127	S1 A1
PCI AD23	11	AD23	CAD22/A4	124	S1 A3
PCI AD22	12	AD22	CAD21/A5	121	S1 A4
PCI AD21	13	AD21	CAD20/A6	120	S1 A6
PCI AD20	14	AD20	CAD19/A25	118	S1 A5
PCI AD19	15	AD19	CAD18/A7	116	S1 A25
PCI AD18	16	AD18	CAD17/A24	115	S1 A7
PCI AD17	17	AD17	CAD16/A17	113	S1 A24
PCI AD16	18	AD16	CAD15/OWR#	98	S1 A17
PCI AD15	19	AD15	CAD14/A9	97	S1 A9
PCI AD14	20	AD14	CAD13/IORD#	93	S1 IORD#
PCI AD13	21	AD13	CAD12/A11	92	S1 A11
PCI AD12	22	AD12	CAD11/OE#	91	S1 OE#
PCI AD11	23	AD11	CAD10/CE2#	89	S1 CE2#
PCI AD10	24	AD10	CAD9/A10	89	S1 A10
PCI AD9	25	AD9	CAD8/D15	87	S1 D15
PCI AD8	26	AD8	CAD8/D13	85	S1 D7
PCI AD7	27	AD7	CAD7/D7	82	S1 D13
PCI AD6	28	AD6	CAD5/D6	83	S1 D6
PCI AD5	29	AD5	CAD4/D12	81	S1 D12
PCI AD4	30	AD4	CAD3/D5	77	S1 D5
PCI AD3	31	AD3	CAD2/D11	79	S1 D4
PCI AD2	32	AD2	CAD1/D4	76	S1 D1
PCI AD1	33	AD1	CAD0/D3	76	S1 D3
PCI A00	34	A00			
PCI CBE3#	12	C/BE3#	CC/BE3#/REG#	125	S1 REG#
PCI CBE2#	27	C/BE2#	CC/BE2#/A12	112	S1 A12
PCI CBE1#	37	C/BE1#	CC/BE1#/A8	99	S1 A8
PCI CBE0#	48	C/BE0#	CC/BE0#/CE1#	88	S1 CE1#
PCI RST#	20	RST#	CRST#/RESET	119	S1 RST
PCI FRAME#	28	FRAME#	CFRAME#/A23	111	S1 A23
PCI IRDY#	31	IRDY#	CIRDY#/A15	110	S1 A15
PCI TRDY#	32	TRDY#	CTRDY#/A22	109	S1 A22
PCI DEVSEL#	33	DEVSEL#	CDEVSEL#/A21	107	S1 A21
PCI STOP#	33	STOP#	CSTOP#/A20	105	S1 A20
PCI PERR#	34	PERR#	CPERR#/A14	104	S1 A14
PCI SERR#	35	SERR#	CSERR#/WAIT#	101	S1 WAIT#
PCI PAR#	36	PAR#	CPAR#/A13	101	S1 A13
PCI REQ2#	1	REQ#	CREQ#/INPACK#	123	S1 INPACK#
PCI GNT2#	2	GNT#	CGNT#/WE#	106	S1 WE#
CLK_33M_CBS	21	CLK#	CCLK#/A16	108	S1 A16
RI_OUT#/PME#	59	SUSPEND#	CSTSCHG#/BVD1	135	S1 BVD1
PCI AD22	13	IDSEL	CCLKRUN#/WP	136	S1 WP
PCI_PIRQ0	60	MFUNC0	CBLOCK#/A19	103	S1 A19
PCI_PIRQ1	61	MFUNC1	CINT#/READY	132	S1 RDY#
PCI_PIRQ2	62	MFUNC2	SPKOUT	62	S1 BVD2
PCI_PIRQ3	63	MFUNC3	CAUDIO/BVD2	134	S1 BVD2
PCI_PIRQ4	64	MFUNC4			
PCI_PIRQ5	65	MFUNC5			
PCI_PIRQ6	66	MFUNC6			
PLT_RST#	66	PLT_RST#	CCD2#/CD2#	137	S1 CD2#
PM_RSMRST#	66	PM_RSMRST#	CCD1#/CD1#	135	S1 CD1#
			CVS2#/VS2#	117	S1 VS2
			CVS1#/VS1#	131	S1 VS1

QFP144  
22.2 X 22.2 X 1.60

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# Mini-Express Card--WLAN

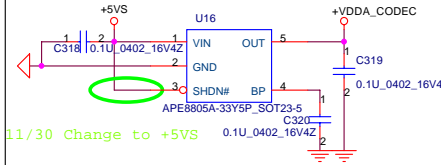


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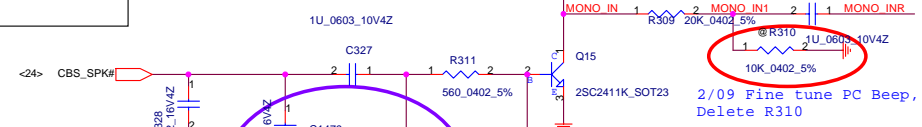
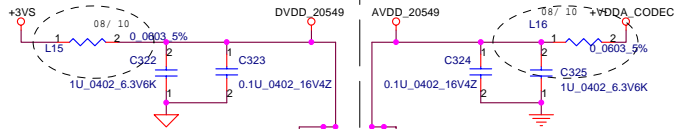
Title			<b>Compal Electronics, Inc.</b>		
Size			<b>Mini-Card</b>		
Document Number			<b>LA-3491P</b>		
Date			Tuesday, March 20, 2007		
Sheet			25 of 47		
Rev			0.5		

### CODEC POWER

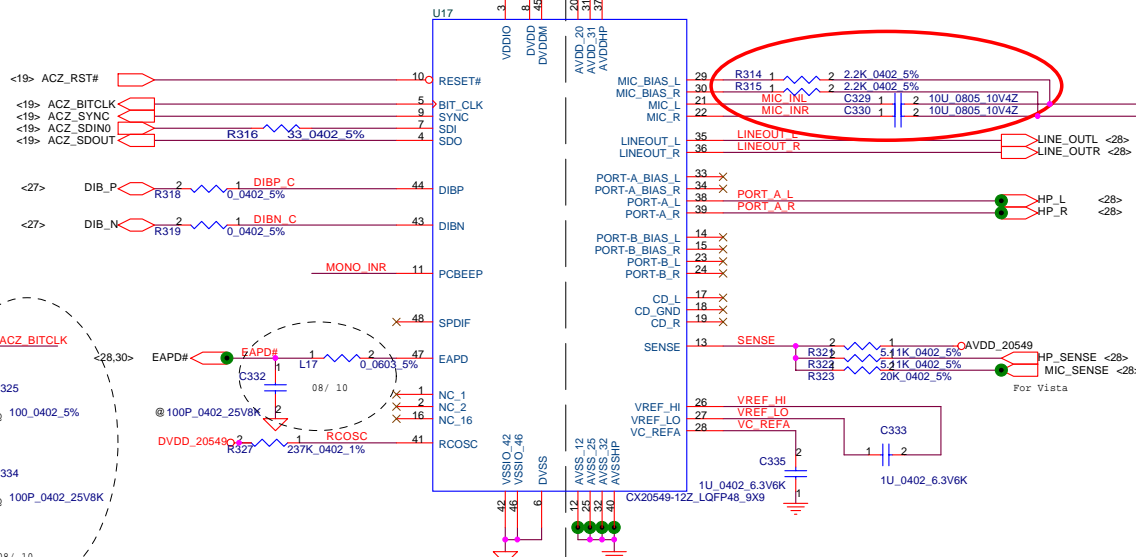


### AUDIO CODEC

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

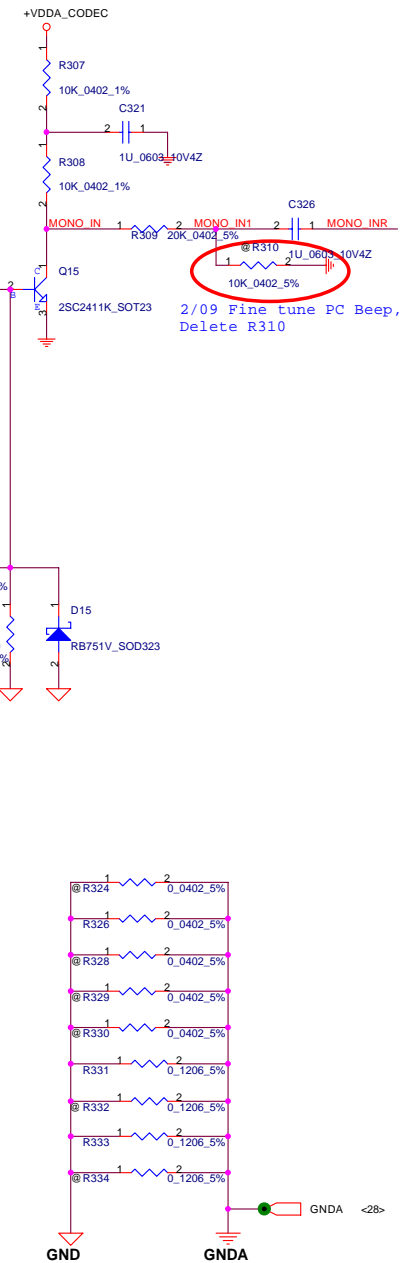


03/10 Delete CBS de-pop circuit  
03/20 Add CBS de-pop circuit, Change Q43 from FET to BJT

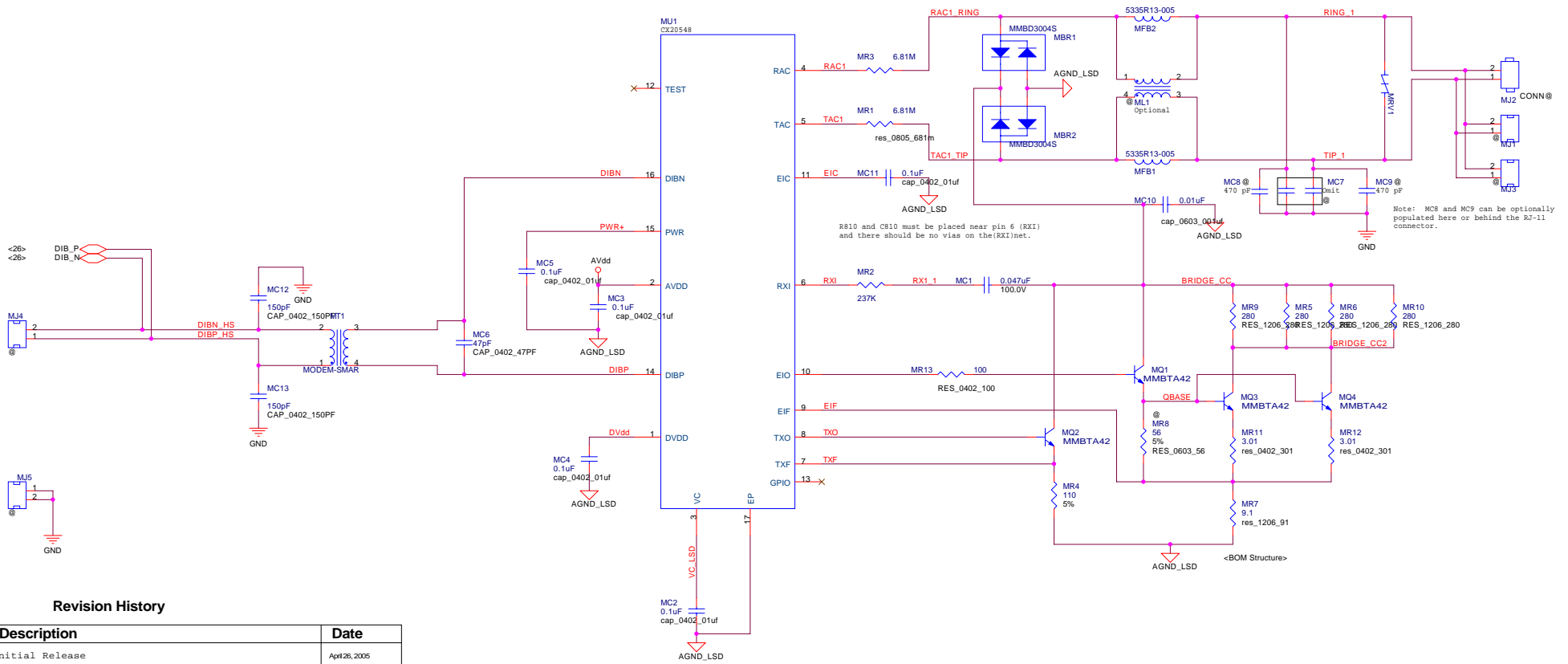


### DIGITAL

### ANALOG



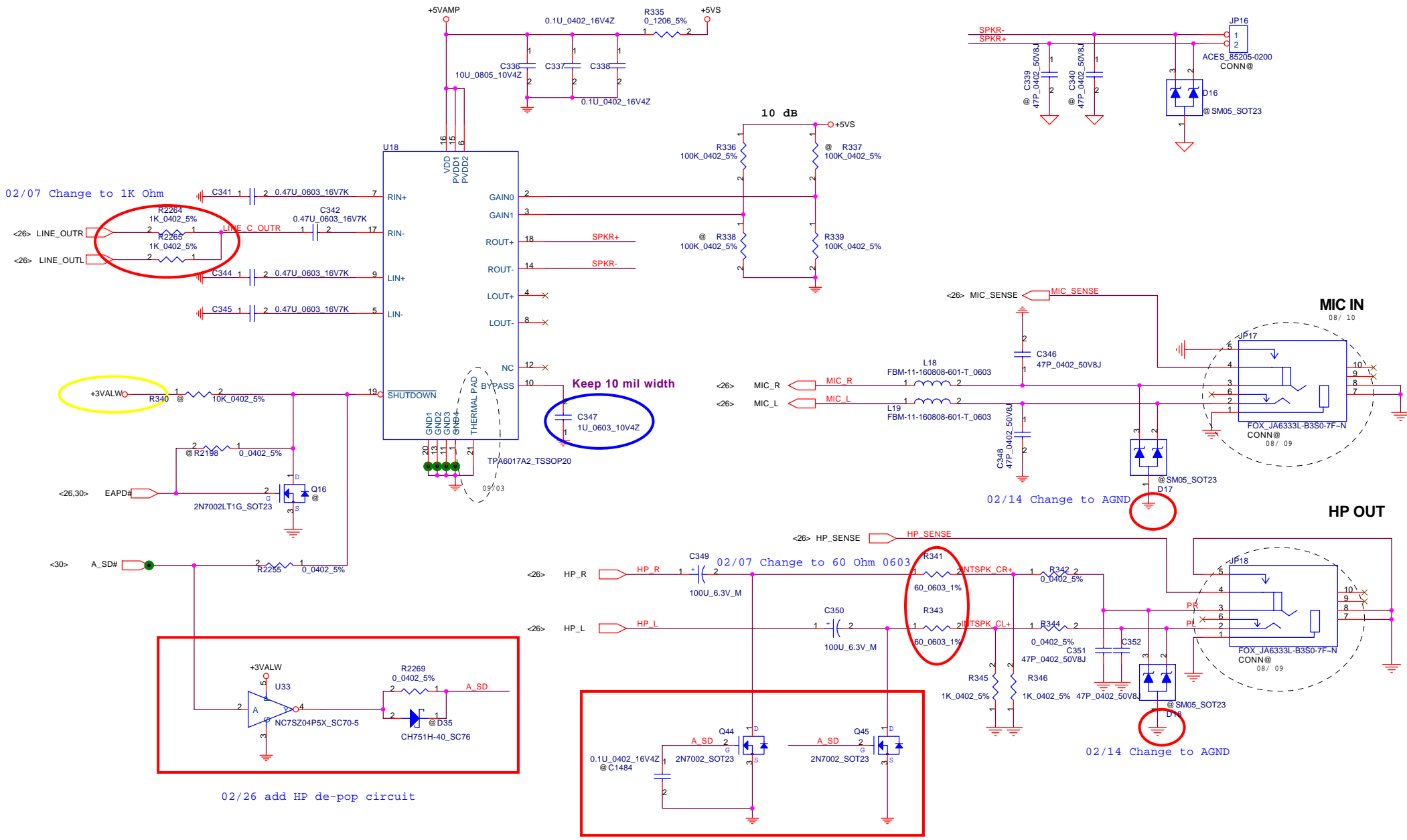
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	Size	Document Number
				Custom	LA-3491P
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				Sheet	26 of 47



**Revision History**

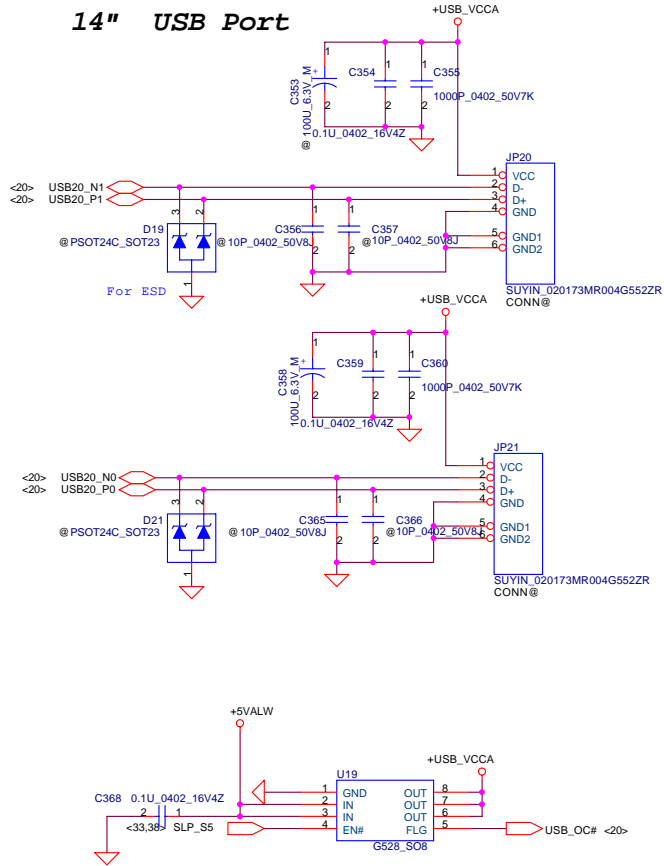
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC9 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2005

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				LA-3491P	Rev 0.5
Date: Tuesday, March 20, 2007				Sheet 27	of 47



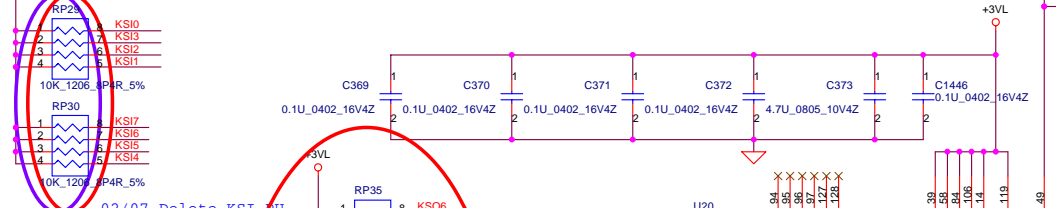
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Custom	LA-3491P			0.5	
Date:	Tuesday, March 20, 2007	Sheet	28	of	47

# 14" USB Port

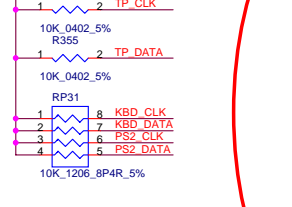


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				Size	Document Number	0.5
Date: Tuesday, March 20, 2007				Sheet	29	of 47

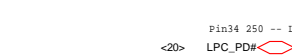
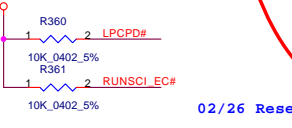
03/10 Add Keyboard scan input PU resistor



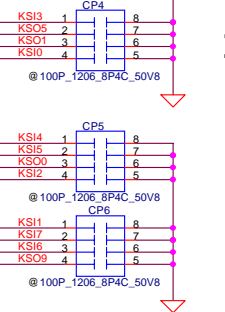
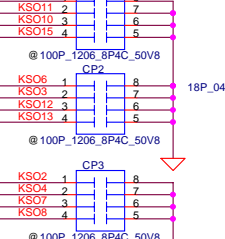
02/07 Delete KSI PU, 1070 had internal PU



Note: R94 must be removed when R1354 stuff and R87 remove.



BMI Add



INT\_KBD CONN.

INT\_KBD CONN. ACES\_85201-2405 CONN@

250@	1021@
R127	R129
R128	R131
R977	R78
R62	

- Keyboard/Mouse Interface
- KSO0 21 KSO0
  - KSO1 20 KSO1
  - KSO2 19 KSO2
  - KSO3 18 KSO3
  - KSO4 17 KSO4
  - KSO5 16 KSO5
  - KSO6 15 KSO6
  - KSO7 14 KSO7
  - KSO8 13 KSO8
  - KSO9 12 KSO9
  - KSO10 11 KSO10
  - KSO11 10 KSO11
  - KSO12 9 KSO12
  - KSO13 8 KSO13
  - KSI0 29 KSI0
  - KSI1 28 KSI1
  - KSI2 27 KSI2
  - KSI3 26 KSI3
  - KSI4 25 KSI4
  - KSI5 24 KSI5
  - KSI6 23 KSI6
  - KSI7 22 KSI7

- General Purpose I/O Interface
- OUT0 124
  - OUT1/IRQR# 125
  - OUT7/SMI# 123
  - OUT8/KBRST# 122
  - OUT9/PWM0 121
  - OUT10/PWM1 120
  - GPIO0 107
  - GPIO1 79
  - GPIO2 80
  - GPIO3 81
  - GPIO4/KSO14 83
  - GPIO5/KSO15 84
  - GPIO7/PWM3 85
  - GPIO8/RXD 86
  - GPIO9/XTXD 87
  - GPIO11/AB2A\_DATA 88
  - GPIO12/AB2A\_CLK 89
  - GPIO13/AB2B\_DATA 90
  - GPIO14/AB2B\_CLK 91
  - GPIO15/FAN\_TACH1 92
  - GPIO16/FAN\_TACH2 101
  - GPIO17/A20M 102
  - GPIO20/PS2CLK 103
  - GPIO21/PS2DATA 105
  - GPIO24/KSO16 74
  - GPIO27 74

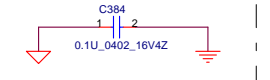
- Power Mgmt/SIRQ
- <20,24> PM\_CLKRUN# 55
  - <20,24> SIRQ 57
  - <15> CLK\_PCI\_EC 54
  - <20> RUNSCI\_EC# 56
  - <19,25,31> LPC\_AD3 51
  - <19,25,31> LPC\_AD2 50
  - <19,25,31> LPC\_AD1 48
  - <19,25,31> LPC\_AD0 46
  - <19,25,31> LPC\_FRAME# 52
  - <7,18,20,22,24,25,31> PLT\_RST# 53
  - LPC\_PD# 45

- LPC Bus
- LAD[3] 61
  - LAD[2] 60
  - LAD[1] 59
  - LAD[0] 58
  - LDR[0] 52
  - LFRAME# 52
  - LRESET# 53
  - LPCPD#/GPIO23 45

- Miscellaneous
- AB1A\_DATA 111
  - AB1A\_CLK 112
  - AB1B\_DATA 109
  - AB1B\_CLK 110
  - PGM Strap/GPIO25 73
  - EA Strap/GPIO26/KSO17 108
  - CLOCK1 59
  - CLK\_14M\_KBC 75
  - 32KHz\_OUT#/GPIO22 76
  - 32KHz\_OUT#/GPIO22 76
  - RESET\_OUT#/GPIO06 78
  - PWRGD 77
  - VCC1\_PWRGD 61
  - EC\_GPIO19 61
  - TEST PIN 69
  - DMS\_LED#/GPIO10 116
  - BAT\_LED# 113
  - PWR\_LED#/R051TX 114
  - FDD\_LED#/R051RX 114

- SMSC\_1070\_TQFP-128P
- VCC0 68
  - AGND 72
  - VSS 11
  - VSS 12
  - VSS 13
  - VSS 14
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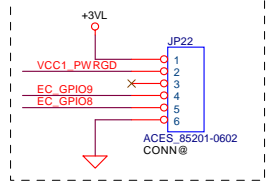
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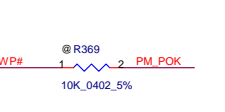
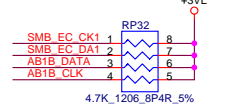
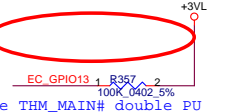
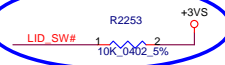
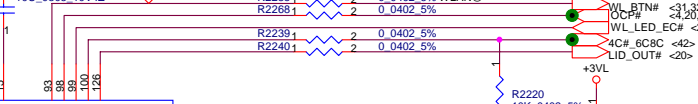
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Issued Date	2006/10/26
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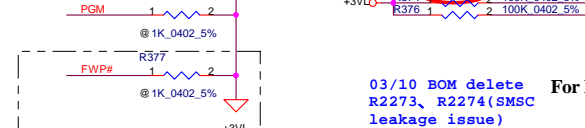
BIOS debug port Place under KB area



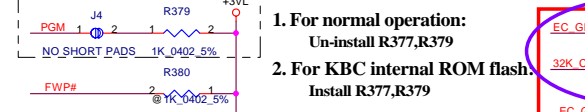
02/14 Reserve R2268 for OCP#



02/07 Delete THM\_MAIN# double PU



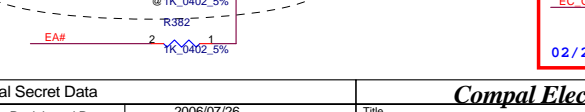
02/07 Reserve VCC0 to +3VL Add R2267 to GND



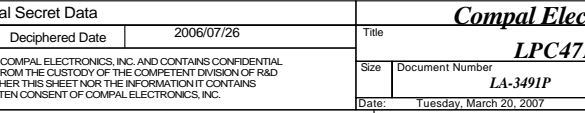
02/07 Reserve VCC0 to +RTCVCC



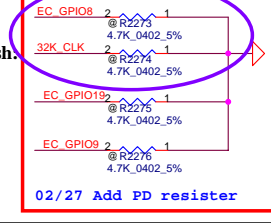
02/08 Delete NUM\_LED# Double PU



02/27 Add PD resistor



- For normal operation: Un-install R377,R379
- For KBC internal ROM flash: Install R377,R379

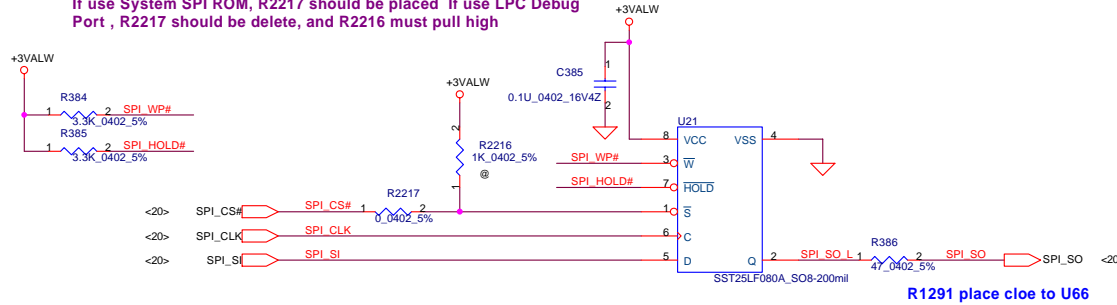


Compal Electronics, Inc. LPC47N1021

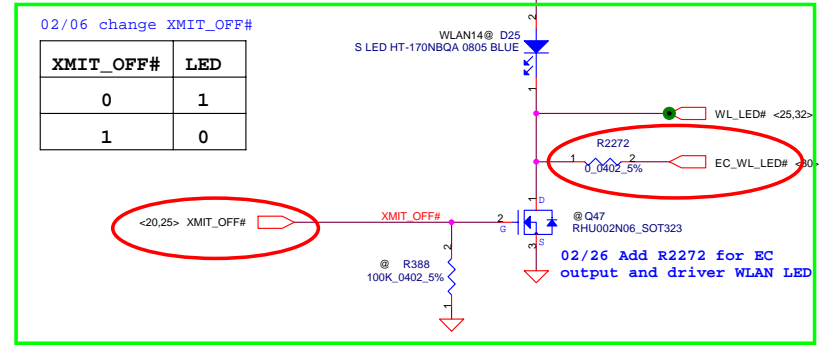
Size	Document Number	Rev
	LA-3491P	0.5
Date:	Tuesday, March 20, 2007	Sheet 30 of 47

# BIOS ROM

If use System SPI ROM, R2217 should be placed If use LPC Debug Port, R2217 should be delete, and R2216 must pull high



# Wireless LED BLUE

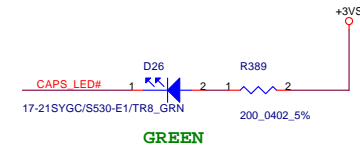


# \*WLAN LED Control note

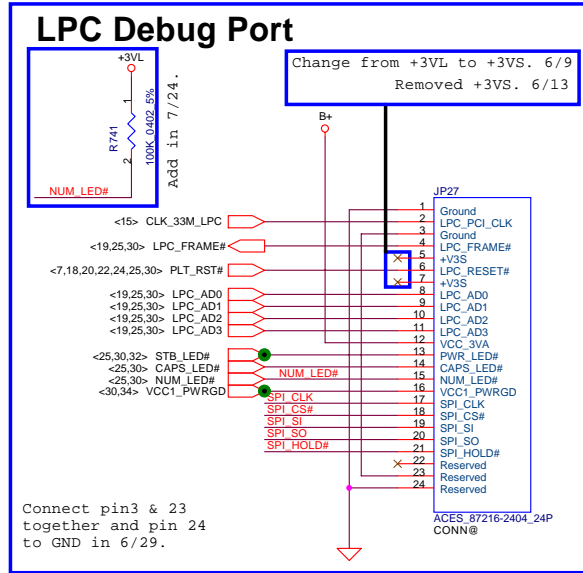
WLAN have 3 ways control, the table list componet must be stuff

1	WLAN Card	R2263
2	XMIT_OFF#	R388 BQ47
3	EC control	R2270, R2271, R2272

# CAP LED

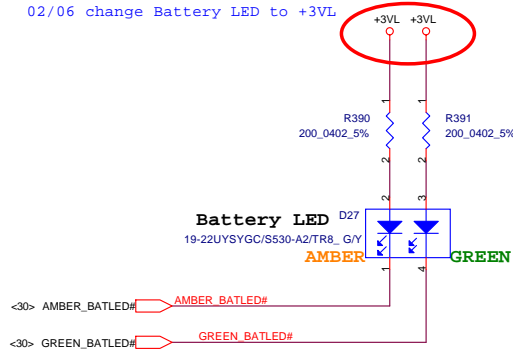


# LPC Debug Port

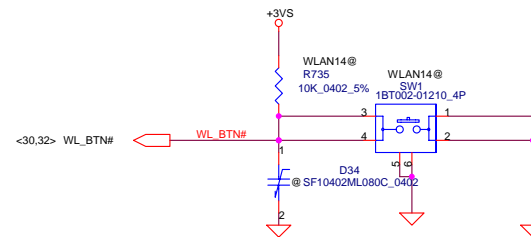


# Charge LED

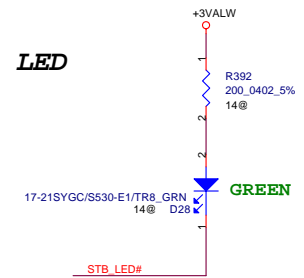
02/06 change Battery LED to +3VL



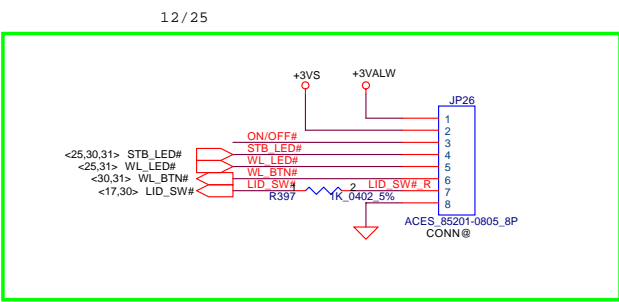
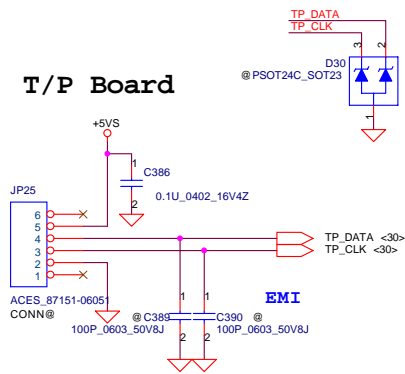
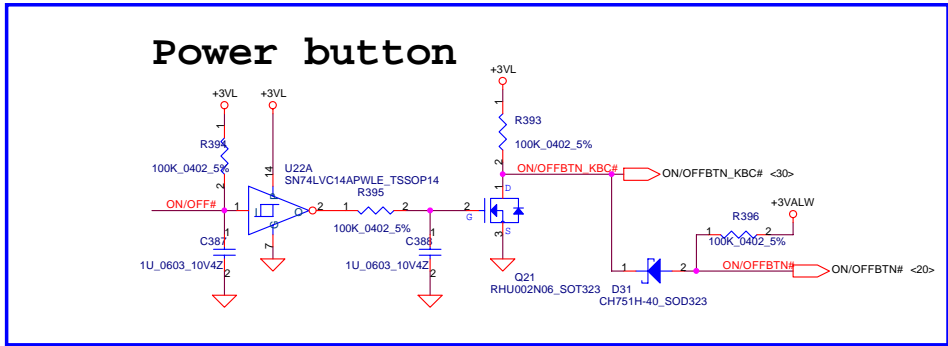
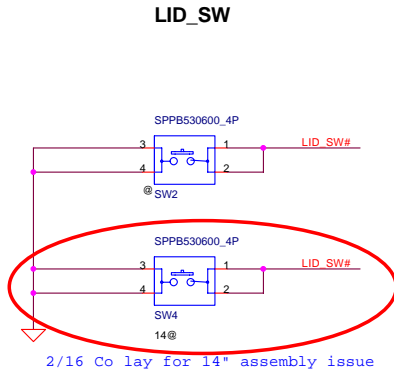
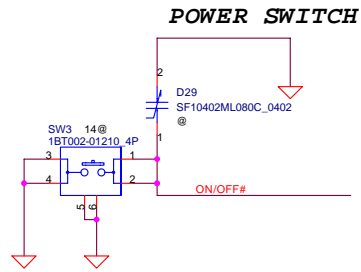
# WL ON/OFF



# POWER LED



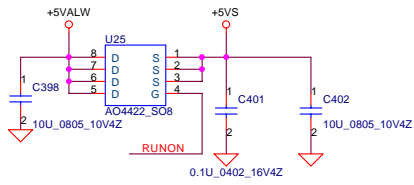
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Size	Document Number	Date		Rev		0.5	
	LA-3491P	Tuesday, March 20, 2007		Sheet 31 of 47			



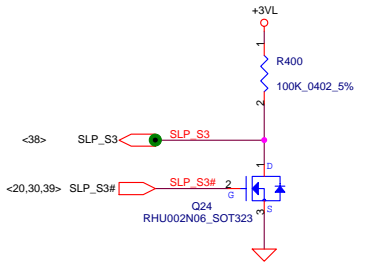
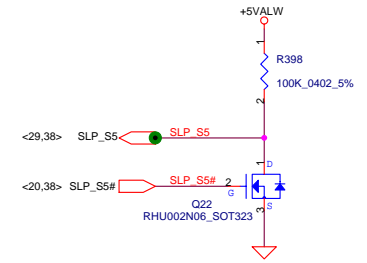
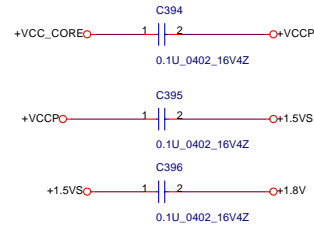
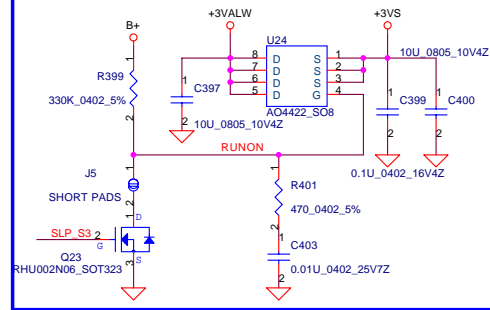
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	Title	
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				Size	Document Number
				LA-3491P	0.5
Date:	Tuesday, March 20, 2007	Sheet	32	of	47



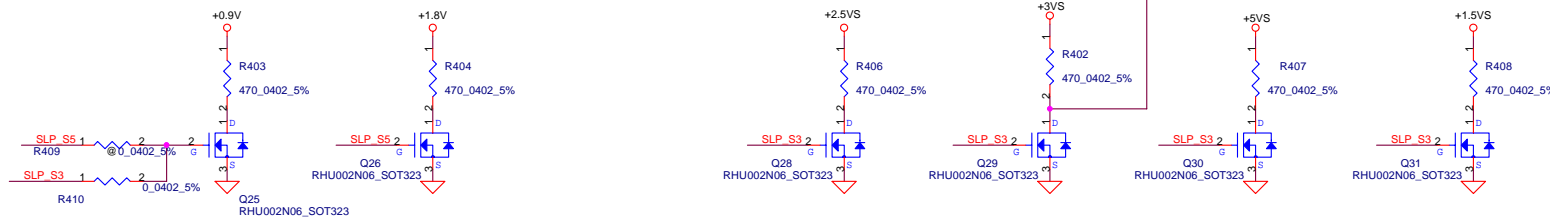
### +5VALW to +5VS Transfer



### +3VALW to +3VS Transfer

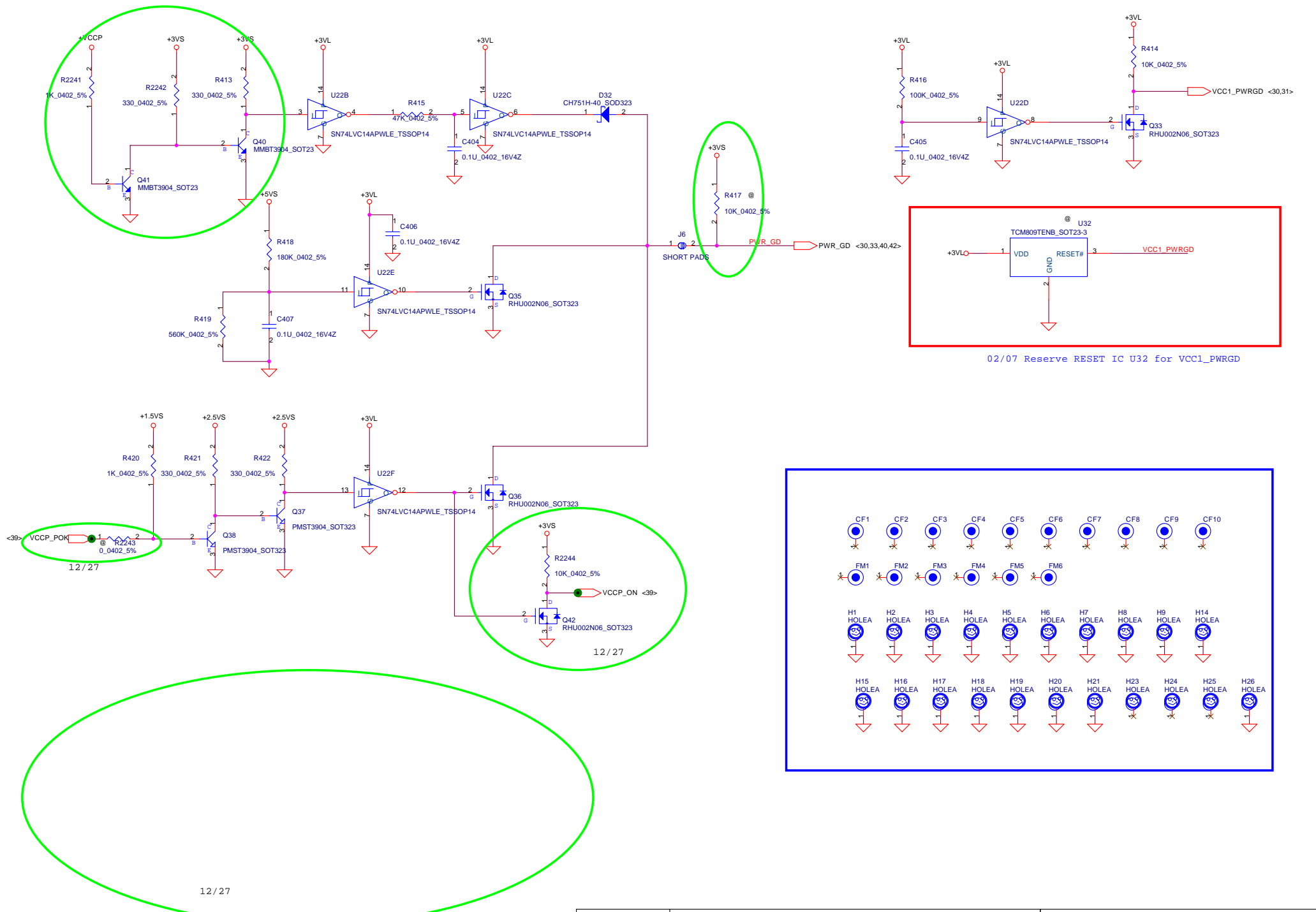


### Discharge circuit



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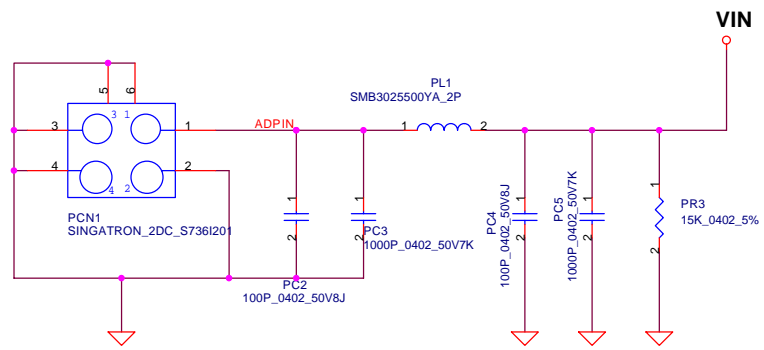
Title			<b>Compal Electronics, Inc.</b>	
			<b>DC/DC Circuits</b>	
Size	Document Number			Rev
	LA-3491P			0.5
Date:	Tuesday, March 20, 2007	Sheet	33	of 47



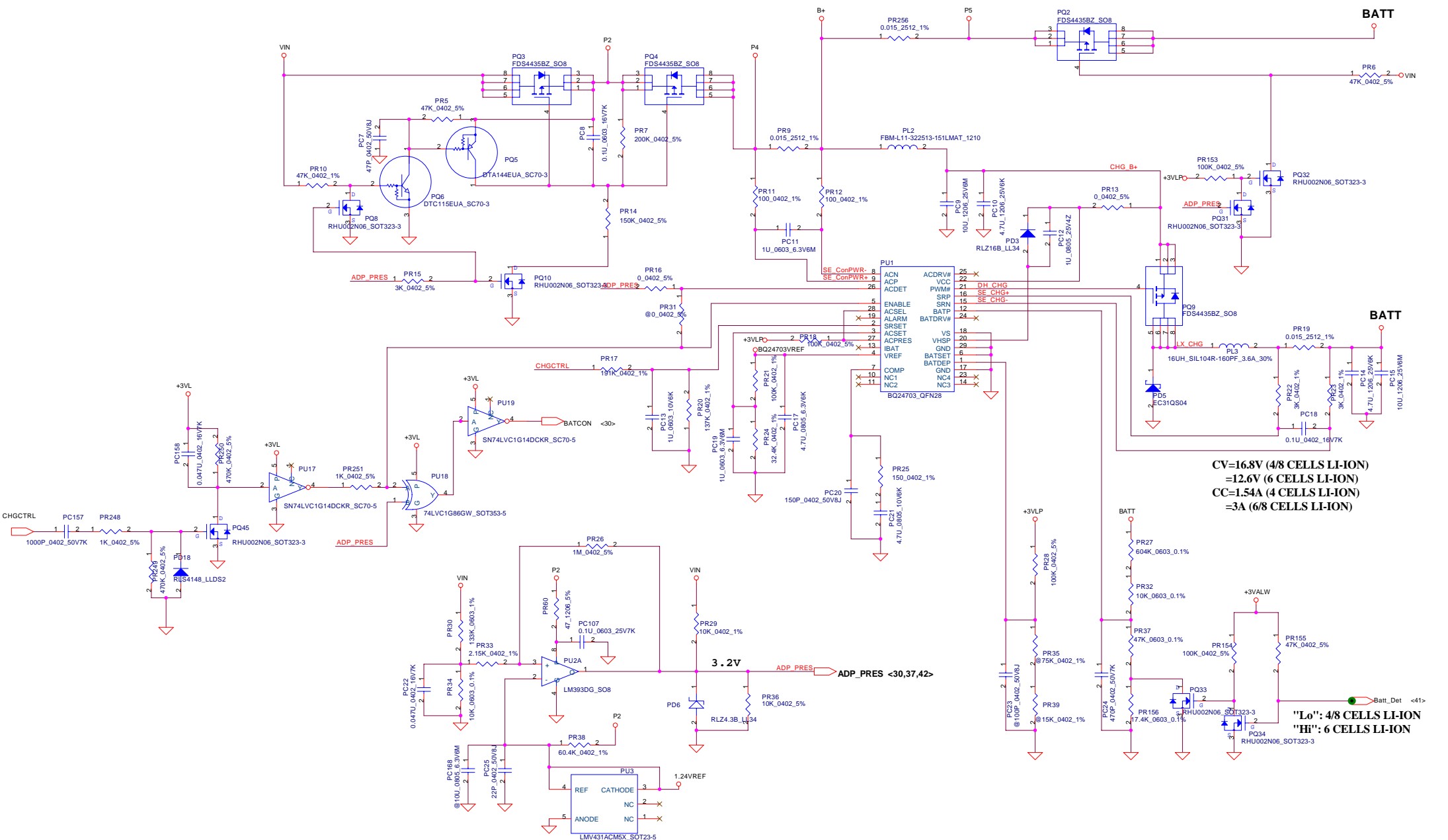
12 / 27

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Date:	Tuesday, March 20, 2007	Sheet	34	of	47

Rev 0.5



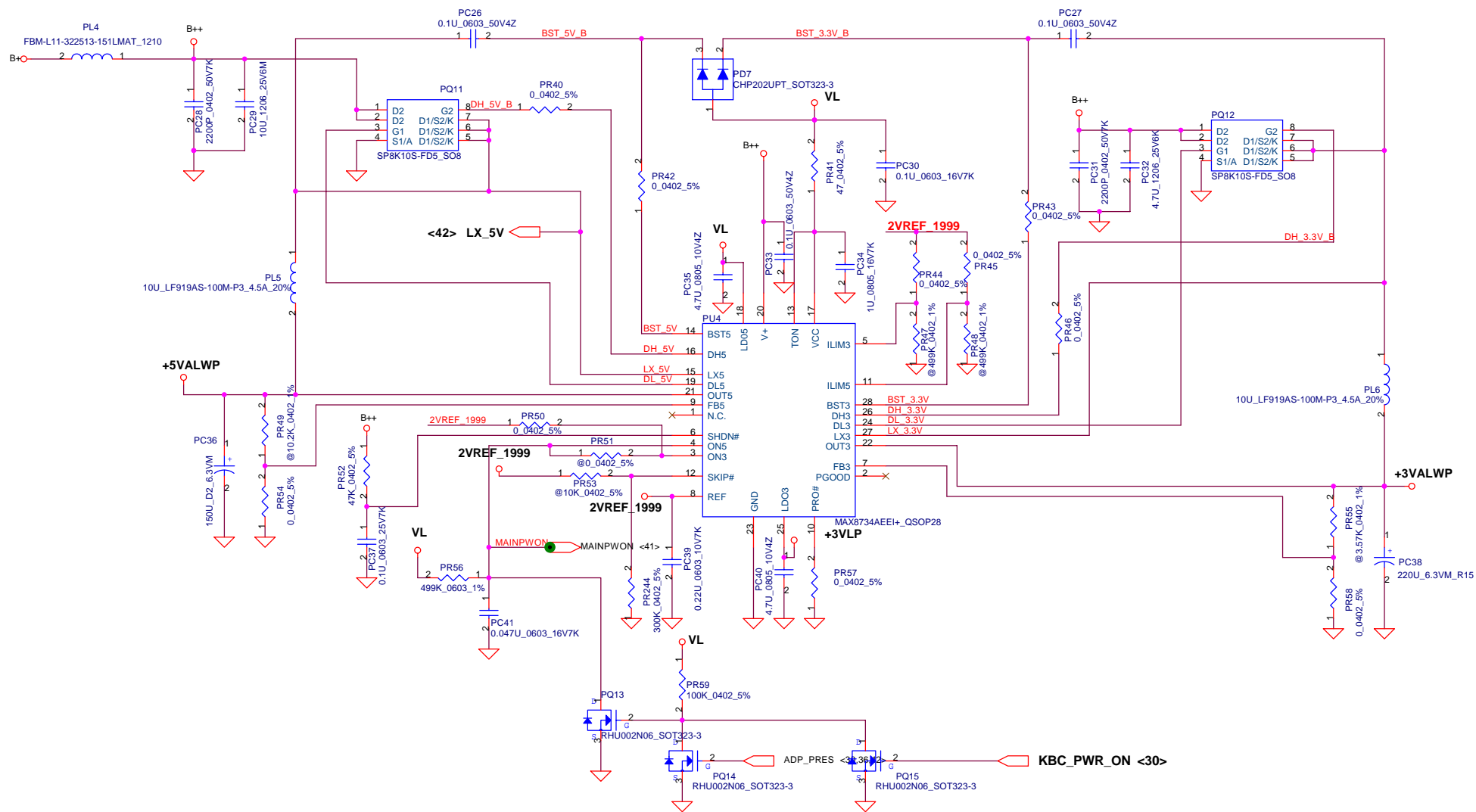
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				Date:	Tuesday, March 20, 2007



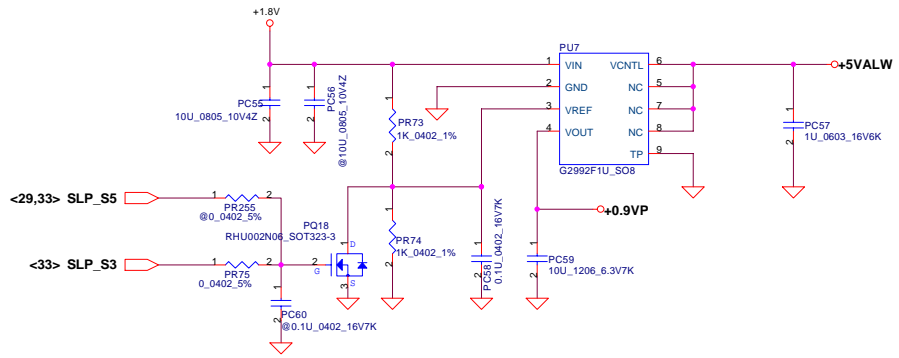
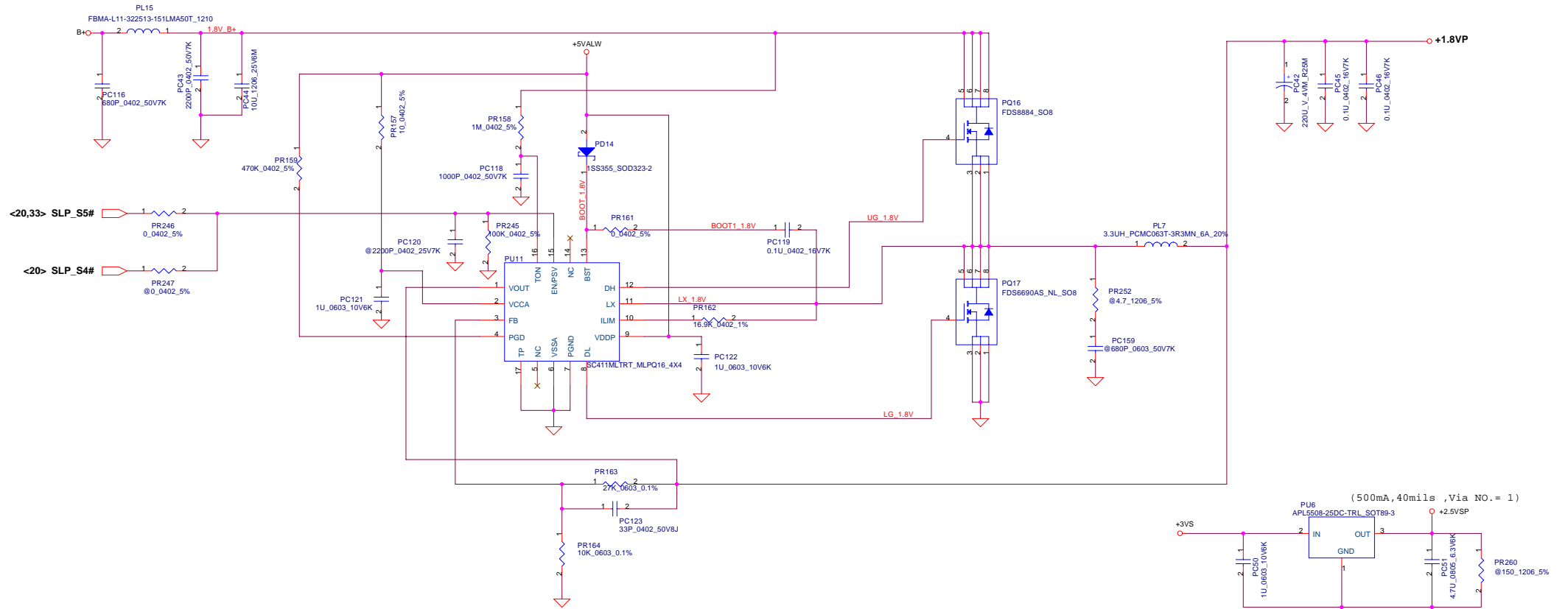
**CV=16.8V (4/8 CELLS LI-ION)**  
**=12.6V (6 CELLS LI-ION)**  
**CC=1.54A (4 CELLS LI-ION)**  
**=3A (6/8 CELLS LI-ION)**

**"Lo": 4/8 CELLS LI-ION**  
**"Hi": 6 CELLS LI-ION**

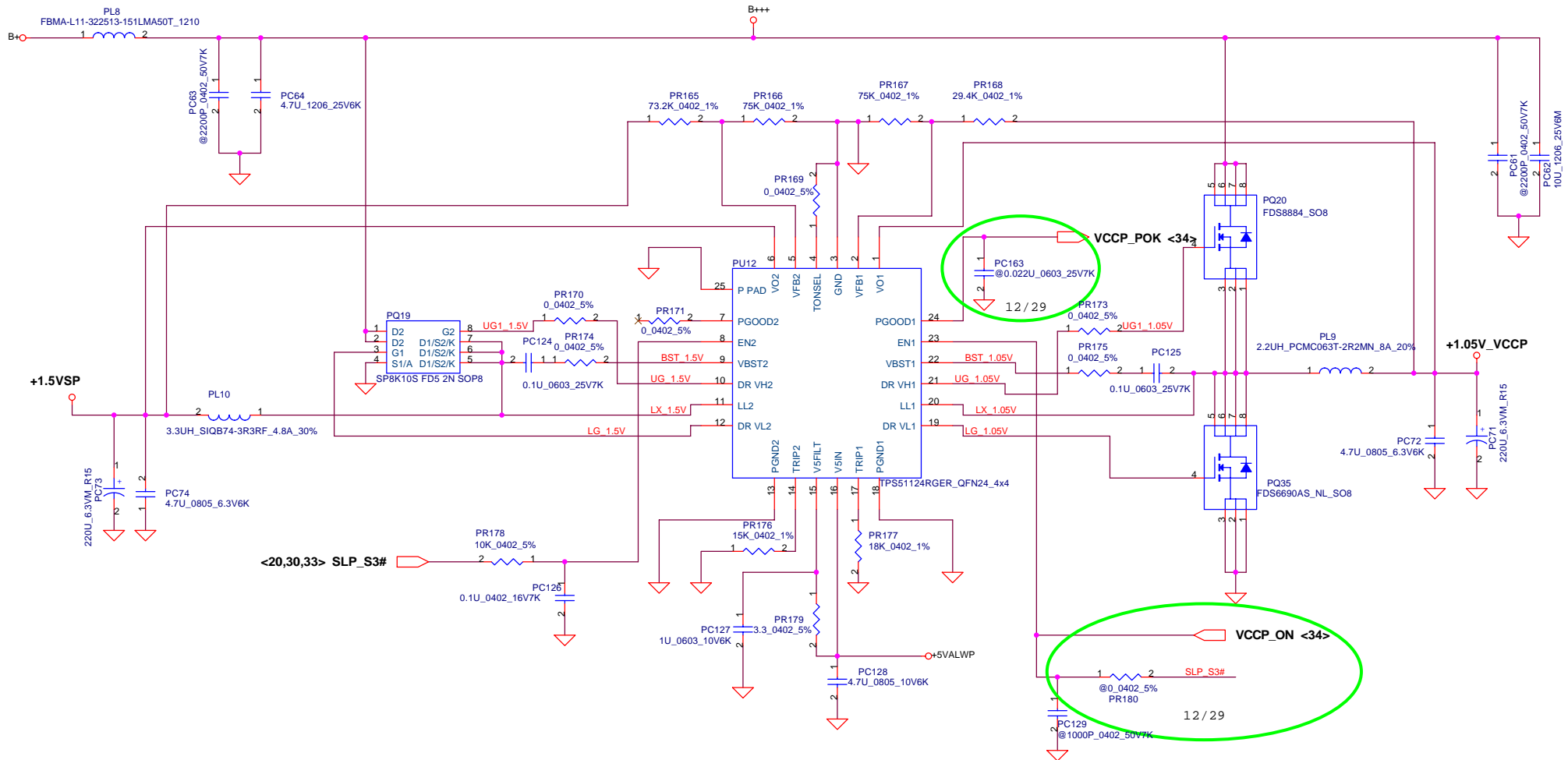
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Issued Date	Deciphered Date	Title	Charger	
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Date:	Tuesday, March 20, 2007	Sheet	36	of 47



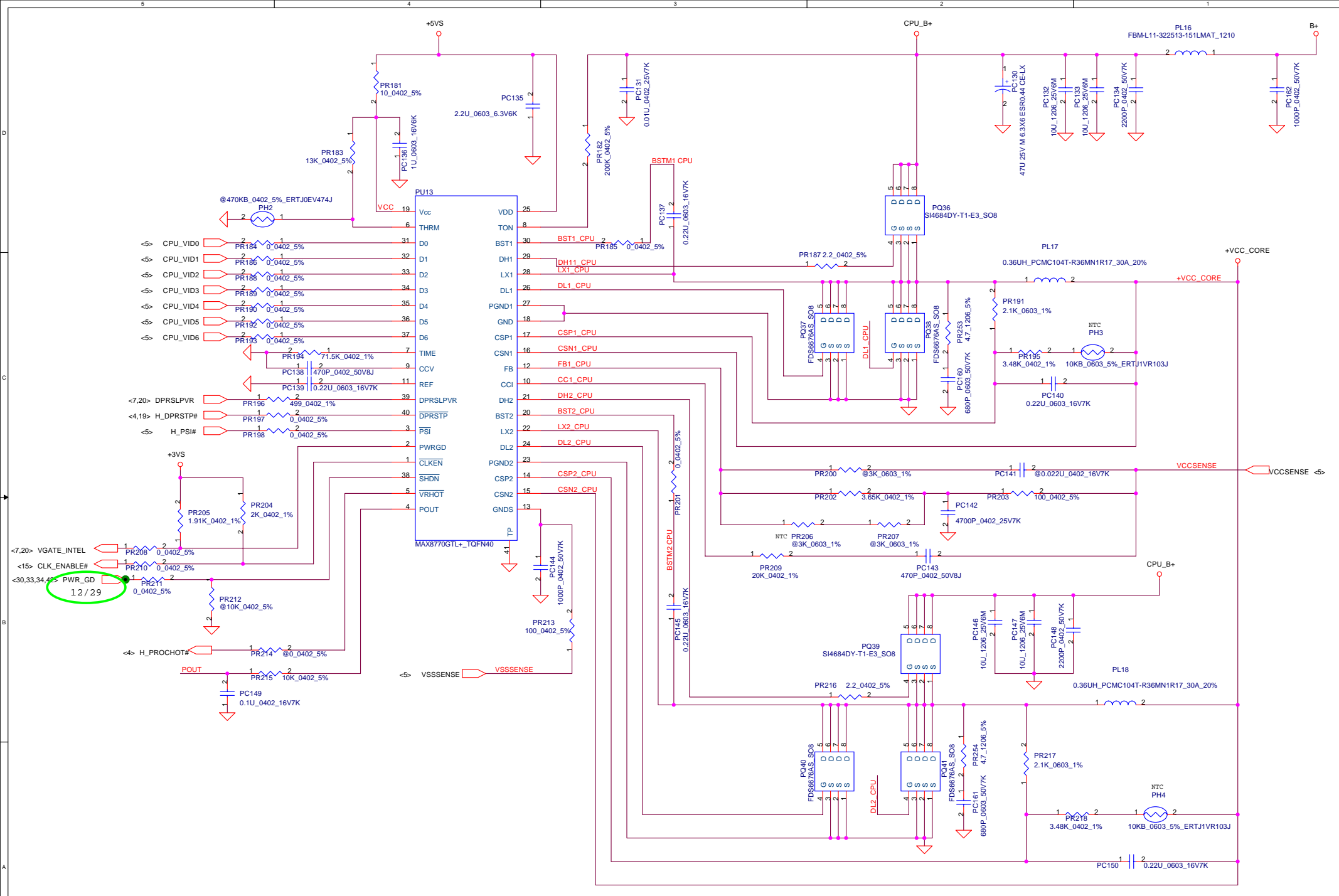
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Issued Date	2006/10/26	Deciphered Date	2006/07/26		
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	LA-3491P	0.5		
Date:	Tuesday, March 20, 2007	Sheet	38	of 47



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Date:	Tuesday, March 20, 2007	Sheet	39	of	47

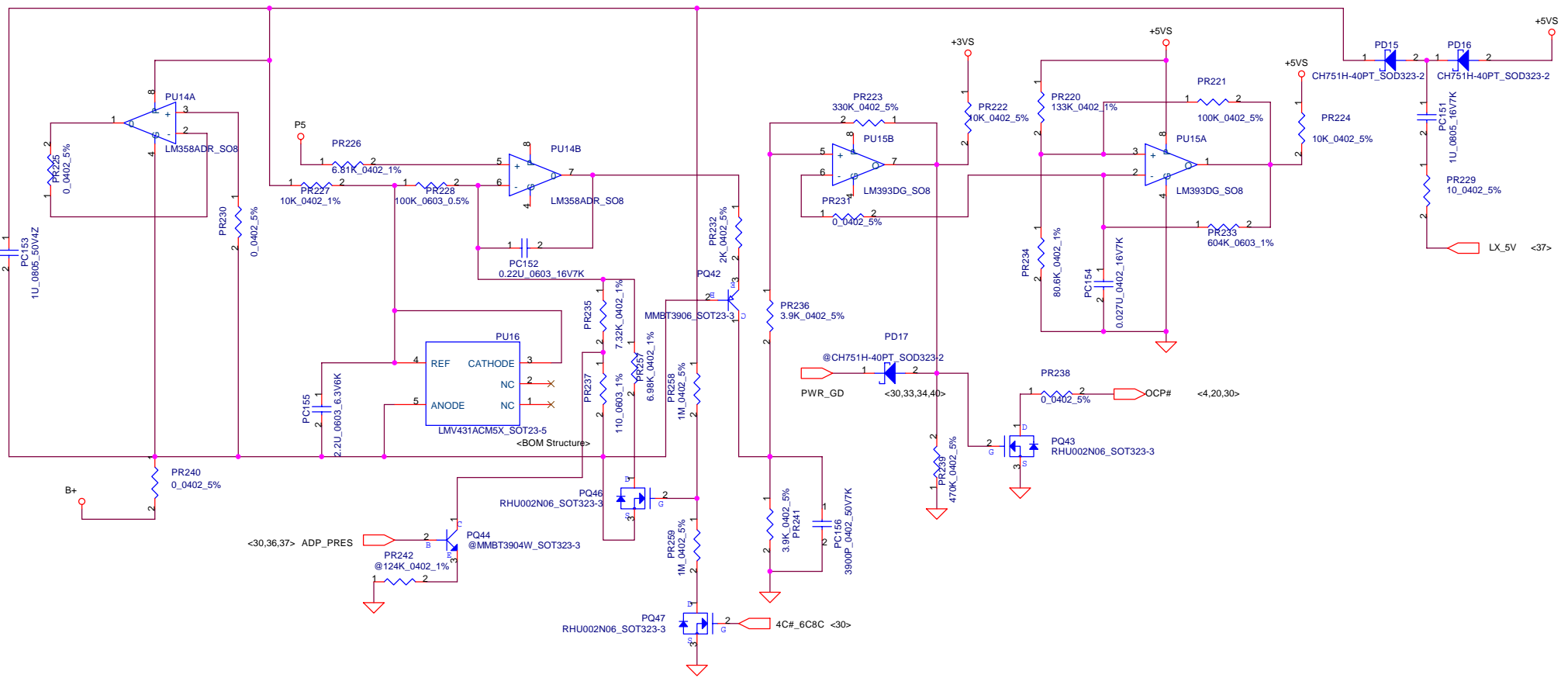


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Title: <b>+CPU_CORE</b>			
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Date: Tuesday, March 20, 2007				Sheet 42 of 47	

Version change list (P.I.R. List)

HW section

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve Disable TV-out power plane resistor	Page 10	Add R2221, R2222, R2223, R2224, R2225 for Disable TV-out power plane	01/02	DB2
2	R2211, R2212 Change to 10k follow datasheet	Page 9	Change R2211, R2212 to 10K_0402_5%	01/02	DB2
3	Disable TV-out follow datasheet	Page 9	Add resistor to +1.5VS power TVDAC_A(R2172)、TVDAC_B(R2173)、TVDAC_C(R2174)、 TV_IREF(R57) BTVIRTNA、TVIRTNB、TVIRTNC(R2251)	01/02	DB2
4	Change CPU and NB BCLK follow heavenly2.0	Page 15	CPU --->CPUCLKT0/C0 NB --->CPUCLKT1/C1	01/02	DB2
5	Change Mini card CLK From SRC3 to SRC7	Page 15	Change to SRC7	01/02	DB2
6	CRT connector PCB footprint error	Page 16	Change JP6 PCB Footprint form SUYIN_070912FR015S207CR_15P to ALLTO_C10510-115A5-L_15P	01/02	DB2
7	+ENAVDD add a 100k Pull low follow datasheet	Page 17	Add R2247 to GND	01/02	DB2
8	LCDVDD enable timing	Page 17	Change R159 to 47k, C213 to 0.1u	01/02	DB2
9	Change AND gate that one gate one chip	Page 18	Change U28(4 in 1) to U30, U31	01/02	DB2
10	Reserve EE PROM power plane +3VS	Page 19	Reserve R2230 for don't support wake up LAN Reserve R2231 for support wake up LAN	01/02	DB2
11	Add R2213 and verify need or not ?	Page 19	Add R2213	01/02	DB2
12	Change PCIE from port 1 to port 2 follow caymus	Page 20 Page 25	Change MINI Card PCIE from Port 1to Port2	01/02	DB2
13	Reserve LAN_RST# that can fine tune from EC	Page 20 Page 30	Reserve R2233 for fine tune LAN_RST# timing	01/02	DB2
14	Change R to RP , keep original design	Page 20	Change to RP33, RP34	01/02	DB2
15	Reserve +3VS power plane for don't support wake up LAN	Page 21	If R2237 ---->support wake up LAN If R2236 ---->Don't support wake up LAN	01/02	DB2
16	Reserve +3VALW power plane to verify HDA codec	Page 21	If R2234 ---->AC97 codec If R2235 ---->HD Codec	01/02	DB2
17	Reserve +3VALW power plane support wake up LAN	Page 23	If L11 ---->Don't support wake up LAN If L20 ---->Support wake up LAN	01/02	DB2
18	Reserve +3VALW power plane support wake up LAN	Page 24	If L12, L13 ---->Don't support wake up LAN If L21, L22 ---->Support wake up LAN	01/02	DB2
19	Reserve 0 ohm resistor for SMSC1070	Page 30	Reserve R2238, R2239, R2240	01/02	DB2

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Title			HW PIR (1)		
Size	Document Number	Rev			
Custom		0.5			
Date:	Tuesday, March 20, 2007	Sheet	43	of	47

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Item	Reason for change	PG#	Modify List	Date	Phase
20	Wireless LED design issue	Page 31	Delete Q20	01/02	DB2
21	Change POK circuit form PGOOD to VCCP_ON	Page 34	Add R2244, Q42, and reserve R2243	01/02	DB2
22	LID_SW# add 10k pull high	Page 30	Add R2253 for LID_SW# pull high	01/16	SI
23	Change use EAPD# to control Amp Shutdown	Page 28	Reserve R2198 and add R2252 pull high	01/16	SI
24	Change Battery LED power from +3VALW to +3VL	Page 31	Change Battery LED power from +3VALW to +3VL	02/06	PV
25	XMIT_OFF# control error	Page 31	Delete Q46	02/06	PV
26	Delete KSI PU, 1070 had internal PU	Page 30	Delete RP29, RP30	02/07	PV
27	Reserve SMSC 1070 VCC0 to +3VL, Add R2267 to GND	Page 30	Reserve R2266 to +3VL, Add R2267 to GND	02/07	PV
28	Change Codec Mix Resistor from 20k to 1k	Page 28	Change R2264, R2265 to 1K	02/07	PV
29	Change LAN82562GT RBIAS resistor to 649 ohm	Page 23	Change R274 to 649 ohm	02/07	PV
30	Reserve RESET IC for VCC1_PWRGD	Page 34	Reserve RESET IC U32 for VCC1_PWRGD	02/07	PV
31	THM_MAIN# Double pull high	Page 30	Delete R356	02/07	PV
32	Fine tune PC Beep	Page 26	BOM delete R310	02/09	PV
33	Change Hp series resistor to 60 ohm 0603	Page 28	Change R341, R343 to 60 ohm 0603	02/14	PV
34	Reserve OCP# to EC GPIO29(pin 98)	Page 30	Reserve R2268 to EC GPIO29(pin98)	02/14	PV
35	HP, MIC ESD Diode change to AGND	Page 28	HP, MIC ESD Diode change to AGND	02/14	PV
36	HP de pop when boot	Page 28	Add inverter to prevent HP pop noise	02/26	PV
37	C43, C44, C45 impact ME parts	Page 06	Change CPU core decoupling capacitor height limit 1.9mm for short term solution(SGA19331D00)	02/26	PV
38	WLAN LED use XMIT_OFF# have error behave	Page 25 Page 30 Page 31	02/26 Add R2270 for WL_LED_EC# PU 02/26 Add R2271 for use EC detect WLAN active 02/26 Add R2272 for EC output and driver WLAN LED	02/26	PV

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Title

HW PIR (2)

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Date:

Tuesday, March 20, 2007

Sheet

44

of

47

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Item	Reason for change	PG#	Modify List	Date	Phase
1	The PR172 changes to HW side	39	Remove PR172	2006/12/29	DB2
2	Change the +1.05V_VCCP power sequence	39	Remove PR180	2006/12/29	DB2
3	The +1.05V_VCCP dynamic range is over spec.	39	Change PL9 from 3.3UH to 2.2UH	2007/01/03	DB2
4	Adjust +1.5VSP voltage range	39	Change PR165 from 75K_ohm to 73.2K_ohm	2007/01/03	DB2
5	Change the PD18 diode	36	Change PD18 from 1SS355 to RLS4148	2007/01/16	SI
6	Change the +3VALWP output capacitor.	37	Change PC38 from 150U_D2_6.3VM to 220U_6.3V_R15	2007/01/16	SI
7	Change the +0.9VP output capacitor.	38	Change PC59 from 22U to 10U	2007/01/16	SI
8	Change the +1.05V_VCCP output capacitor.	39	Change PC71 from 220U_V_4VM_R25M to 220U_6.3V_R15	2007/01/16	SI
9	Change the +1.5VSP output capacitor.	39	Change PC73 from 220U_6.3VM_R15 to 220U_6.3V_R15	2007/01/16	SI
10	Change the +1.5VSP choke size.	39	Change PL11 from 3.3UH_PCMC063T-3R3MN_6A_20% to 3.3UH_SIQB74-3R3RF_4.8A_30%	2007/01/16	SI
11	Change PD14 diode	38	Change PD14 from CH751H-40PT to 1SS355	2007/02/05	PV
12	Adjust PU3 operation current	36	Change PR38 from 75K_ohm to 60.4K_ohm	2007/02/05	PV
13	Change PC25 capacitor.	36	Change PC25 form .022U to 22P	2007/02/05	PV
14	Change the +1.5VSP power sequence	39	1. Change PR178 form 0_ohm to 10K_ohm 2. Add PC126 0.1U	2007/02/05	PV

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Date:

Tuesday, March 20, 2007

Sheet

46

of

47

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