

Compal confidential

Schematics Document

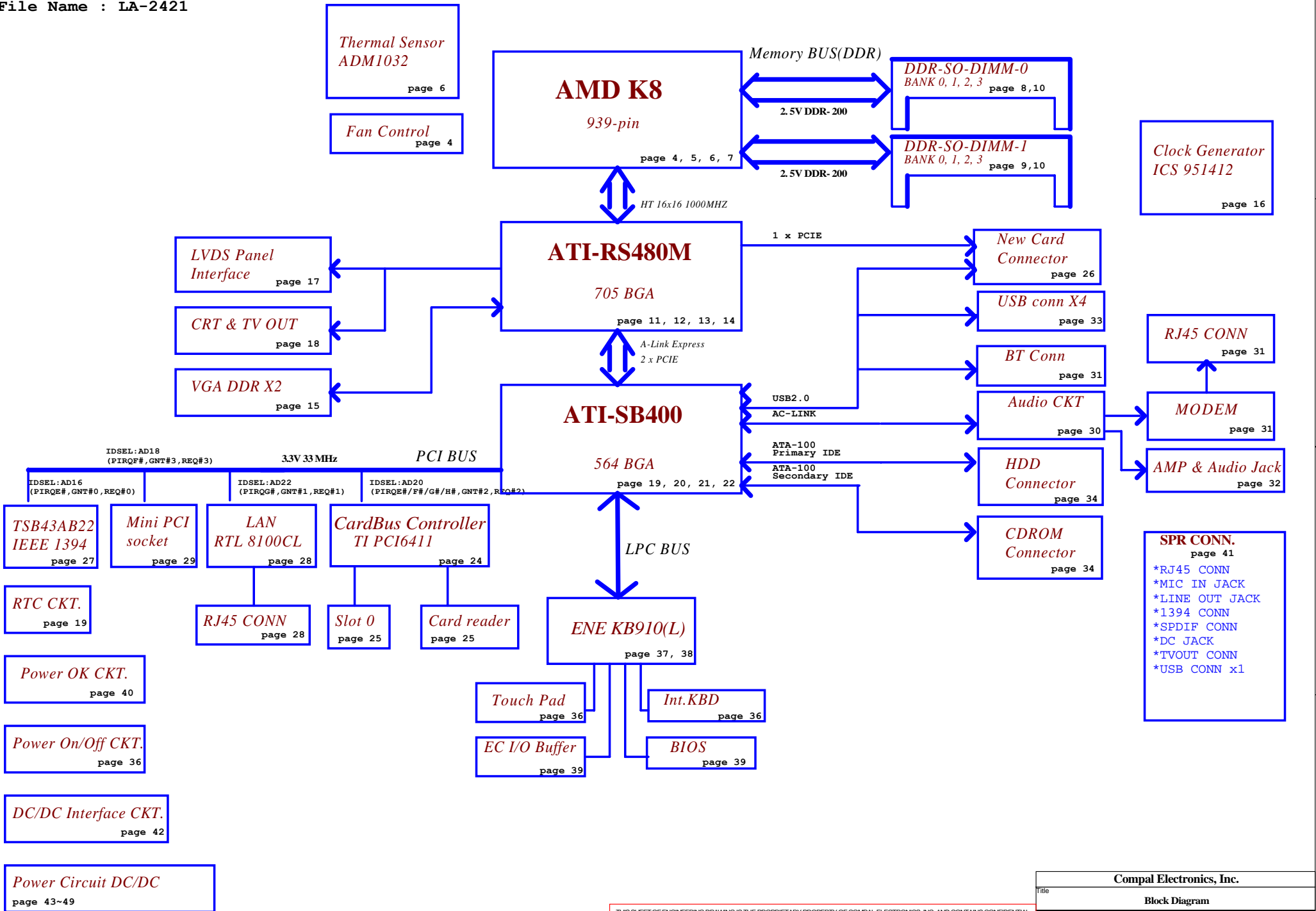
AMD K8 with ATI RS480M+ATI SB400

2005-01-04

REV: 0.6

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Title		
Cover Sheet		
Size	Document Number	Rev
	LA-2421	0.6
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Title Block Diagram		
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Voltage Rails

power plane State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
S0	○	○	○
S1	○	○	○
S3	○	○	✗
S5 S4/AC	○	✗	✗
S5 S4/AC don't exist	✗	✗	✗

○ MEANS ON

✗ MEANS OFF

PCI Devices

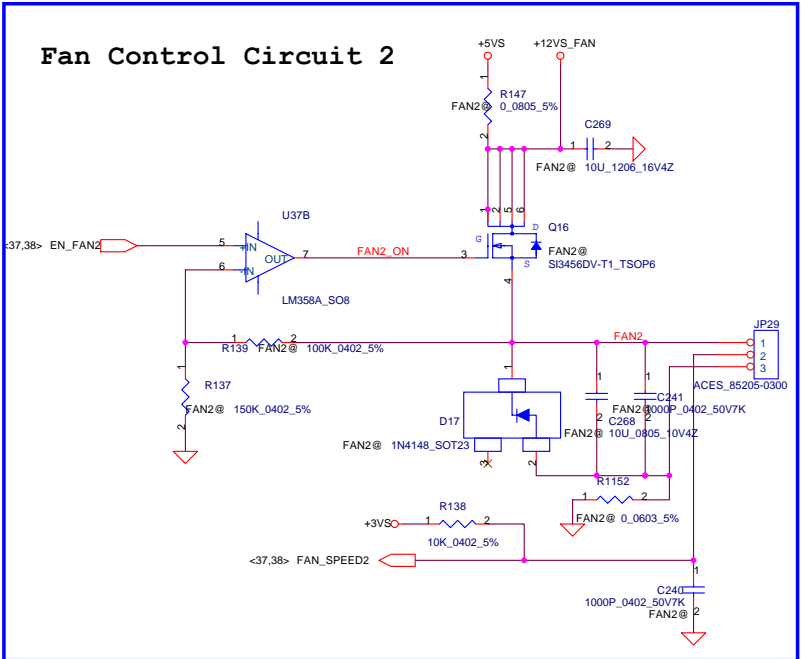
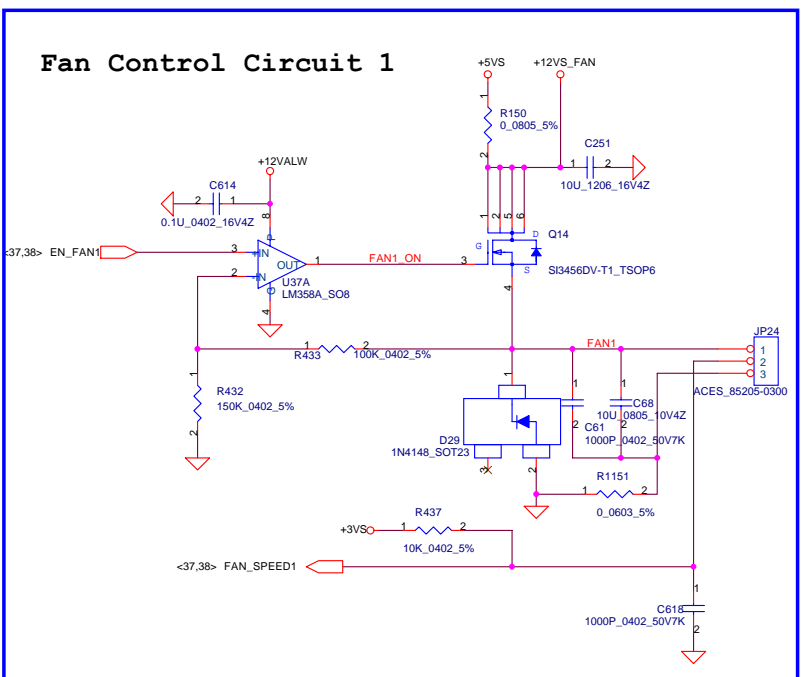
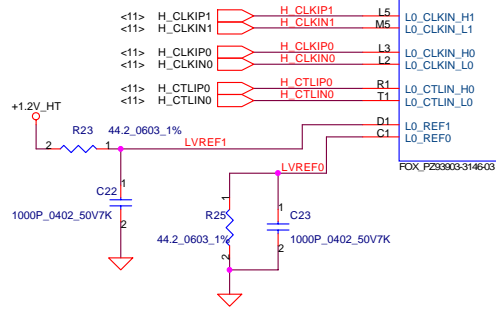
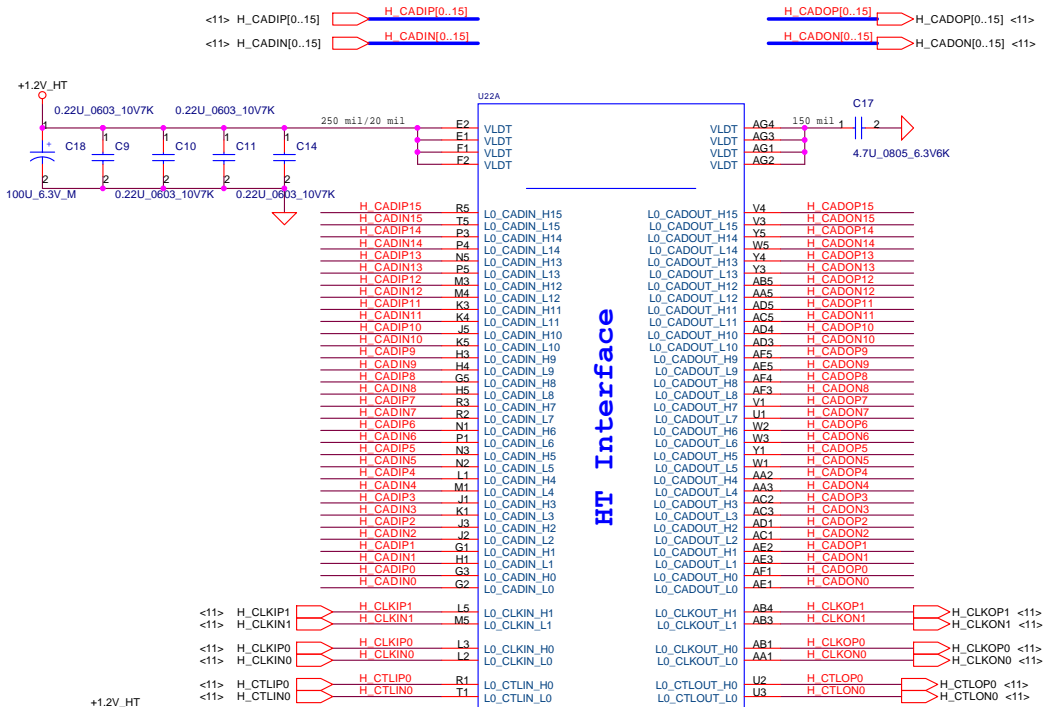
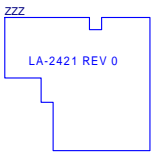
INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A

EXTERNAL	IDSEL #	REQ/GNT #	PIRQ
1394	AD16	0	E
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS	AD20	2	E,F,G,H
Mini-PCI (no use)	AD19	4	F

Compal Electronics, Inc.

Notes List		
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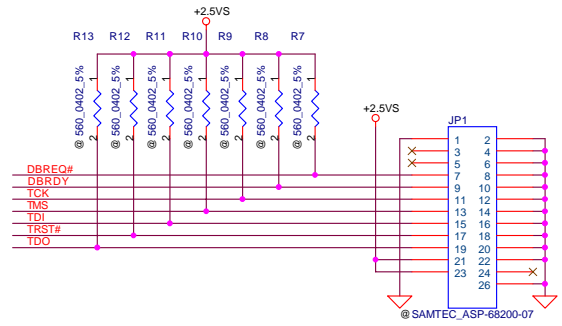
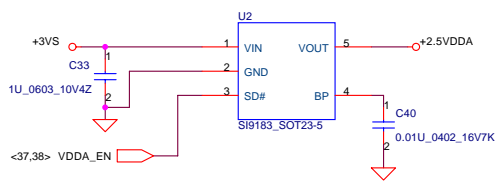
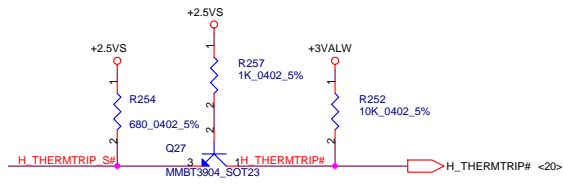
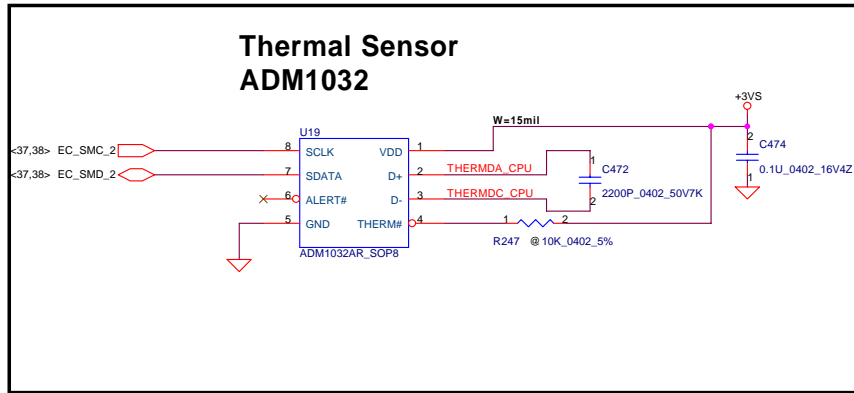
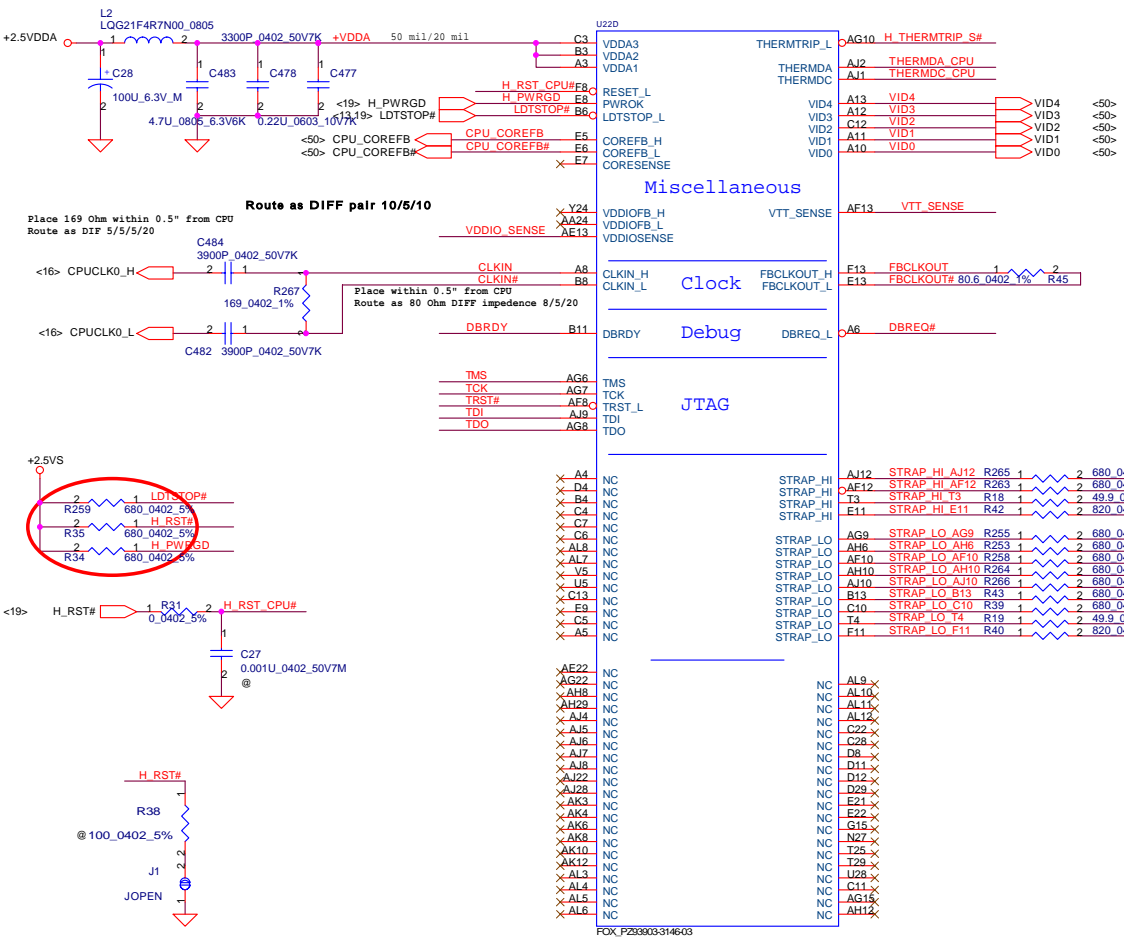
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HT Interface

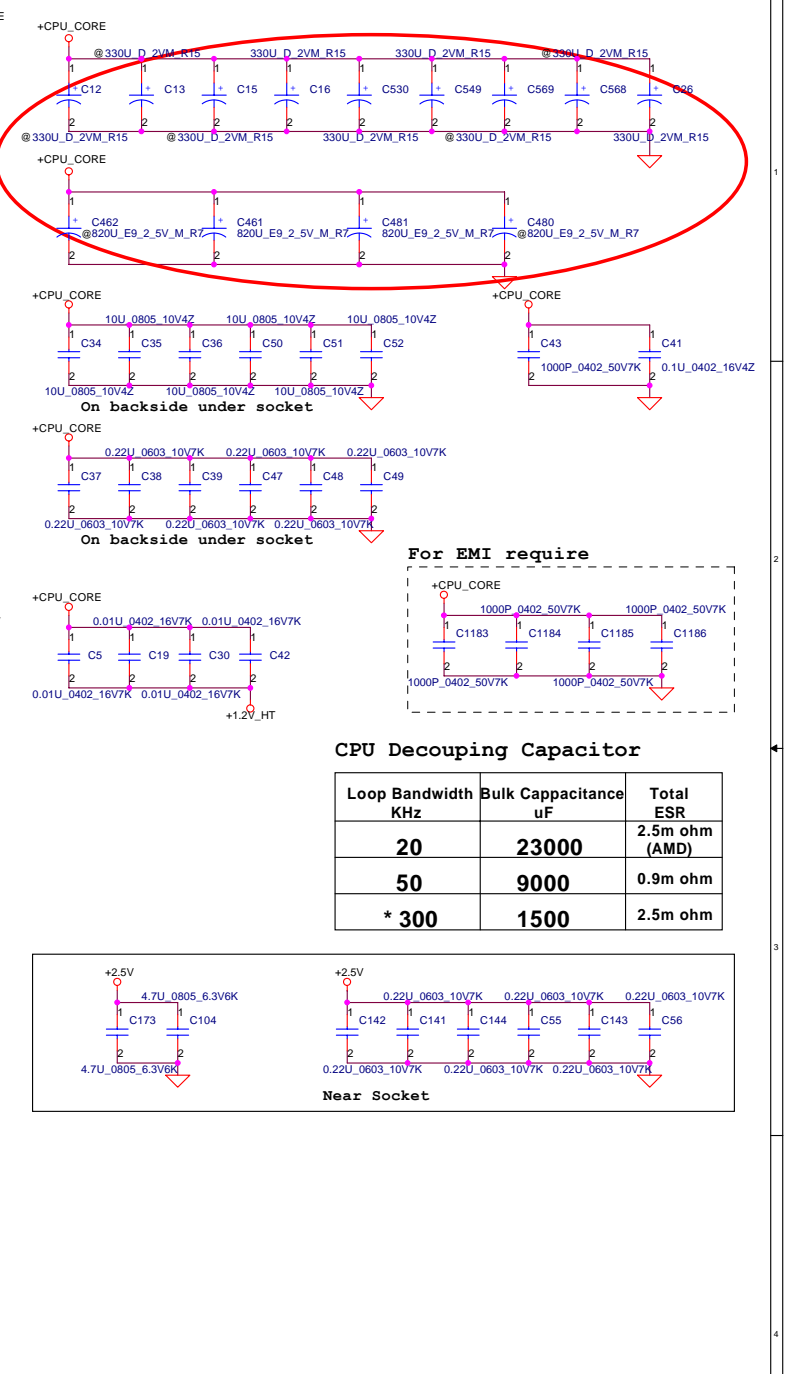
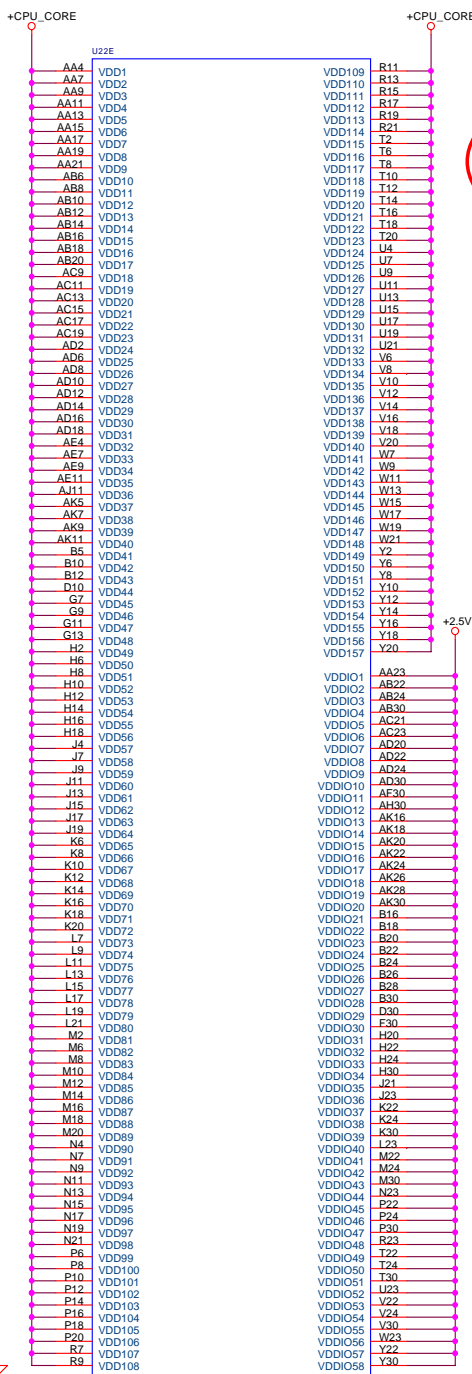
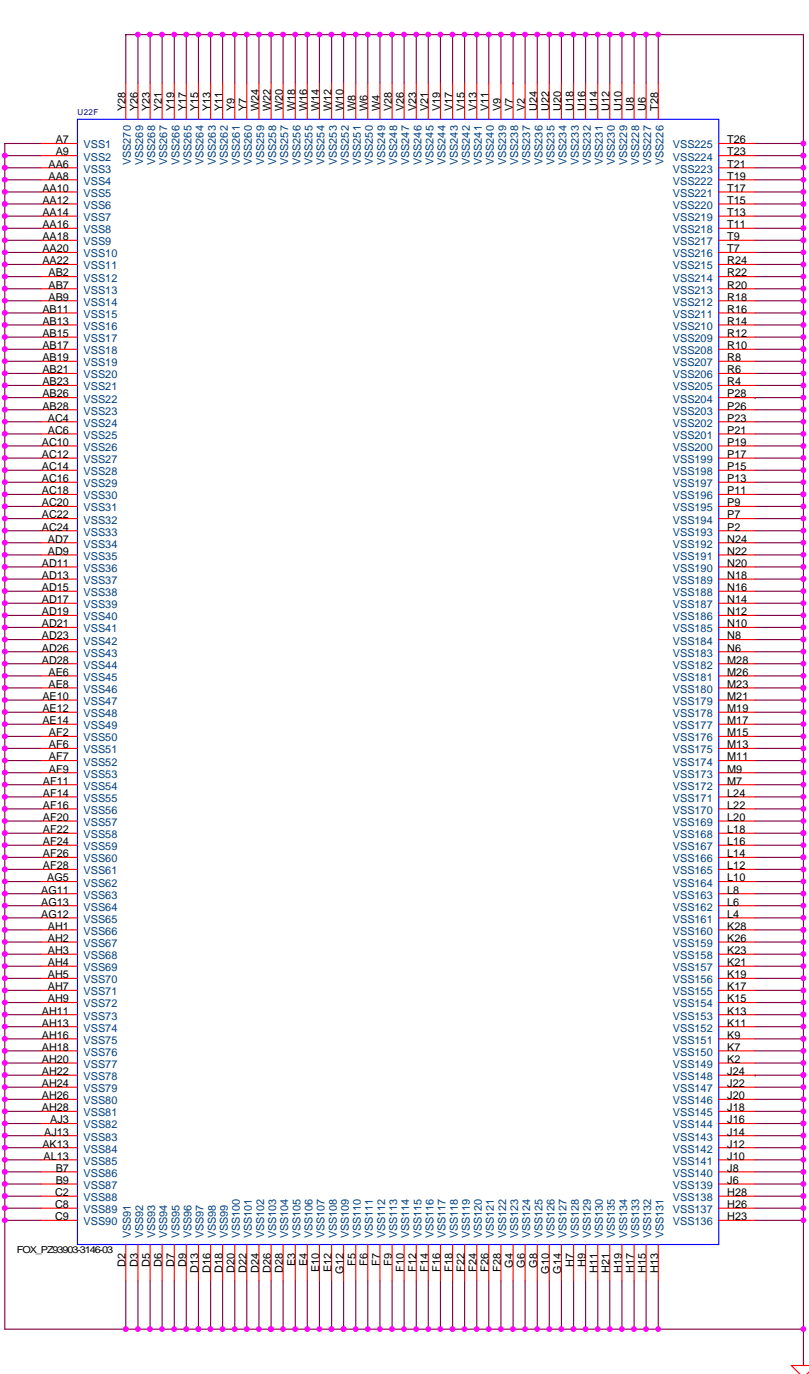
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Compal Electronics, Inc.			
Title			
Claw Hammer CPU (Host Bus)			
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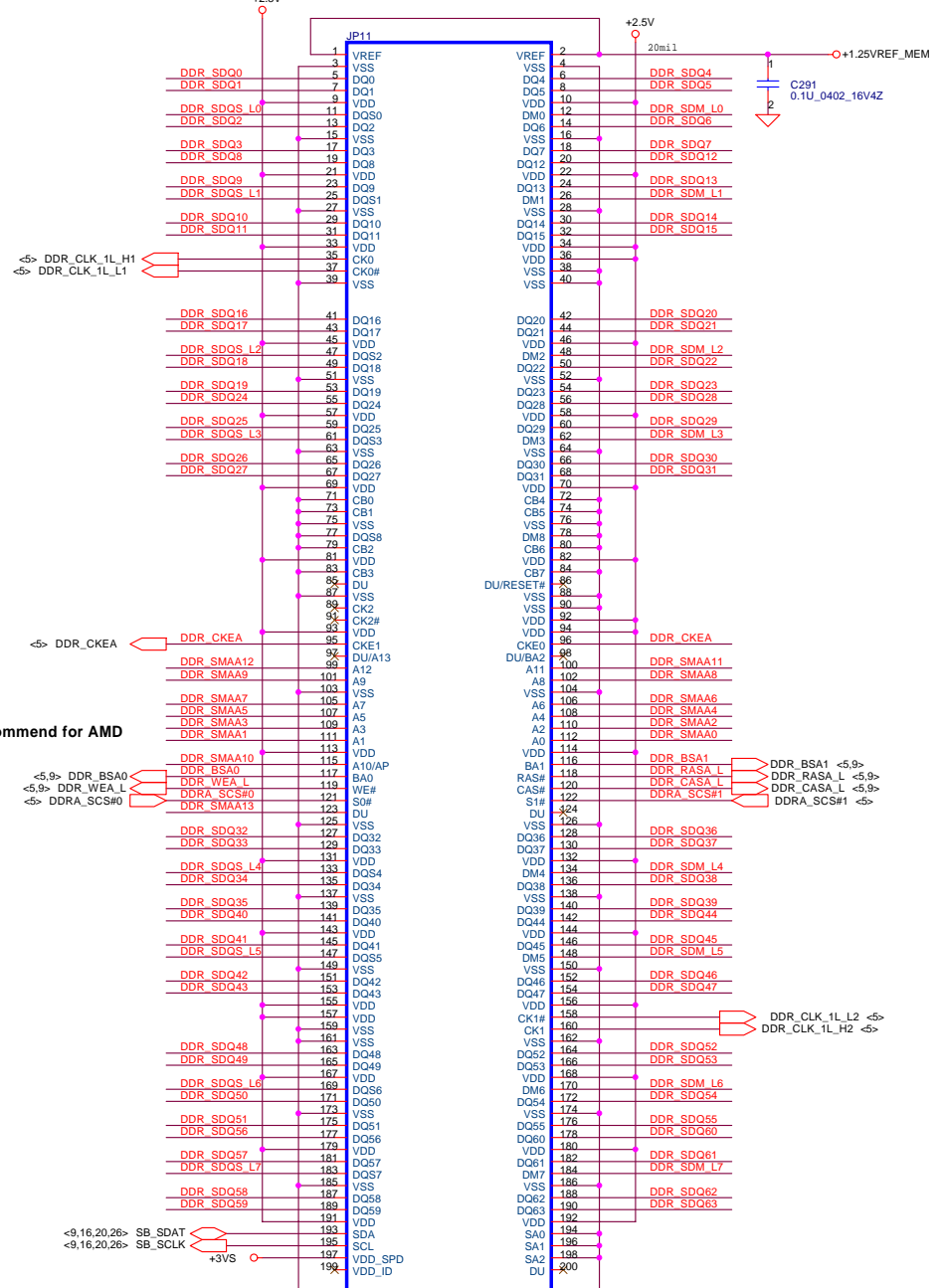
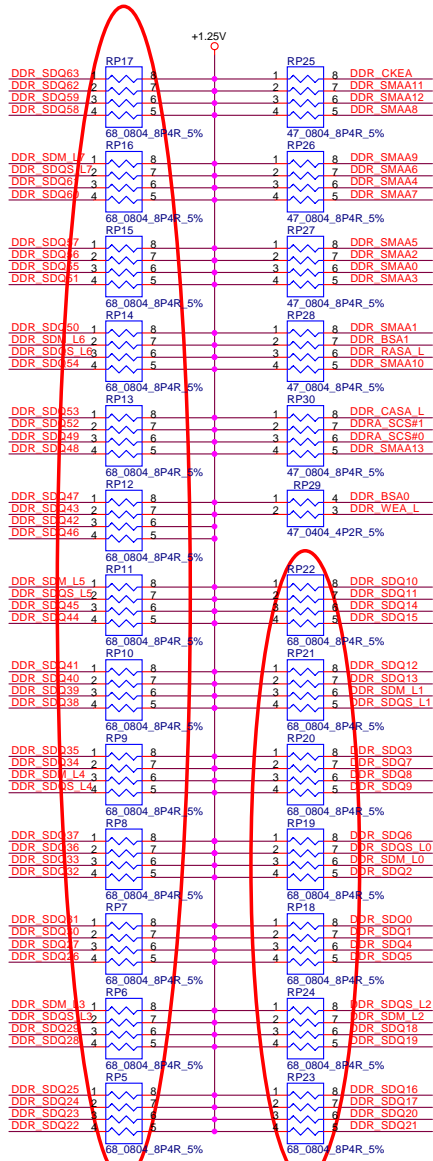
Compal Electronics, Inc.			
ClawHammer (MISC)			
Title	Document Number	Rev	
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Custom			
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Compal Electronics, Inc.
Claw Hammer (Power & Ground)

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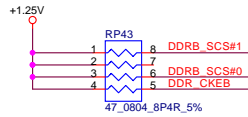
Note:
DDR_SMAA13 Recommend for AMD

AMP_1565917-1
SO-DIMM0
Top Side

- <5,9> DDR_SDQ[0..63]
- <5,9> DDR_SDQS_L[0..7]
- <5,9> DDR_SDM_L[0..7]
- <5,9> DDR_SMAA[0..13]

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Compal Electronics, Inc.			
DDR-SODIMM SLOT0			
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<-> DDR_CLK_2L_H1
<-> DDR_CLK_2L_L1

Layout note

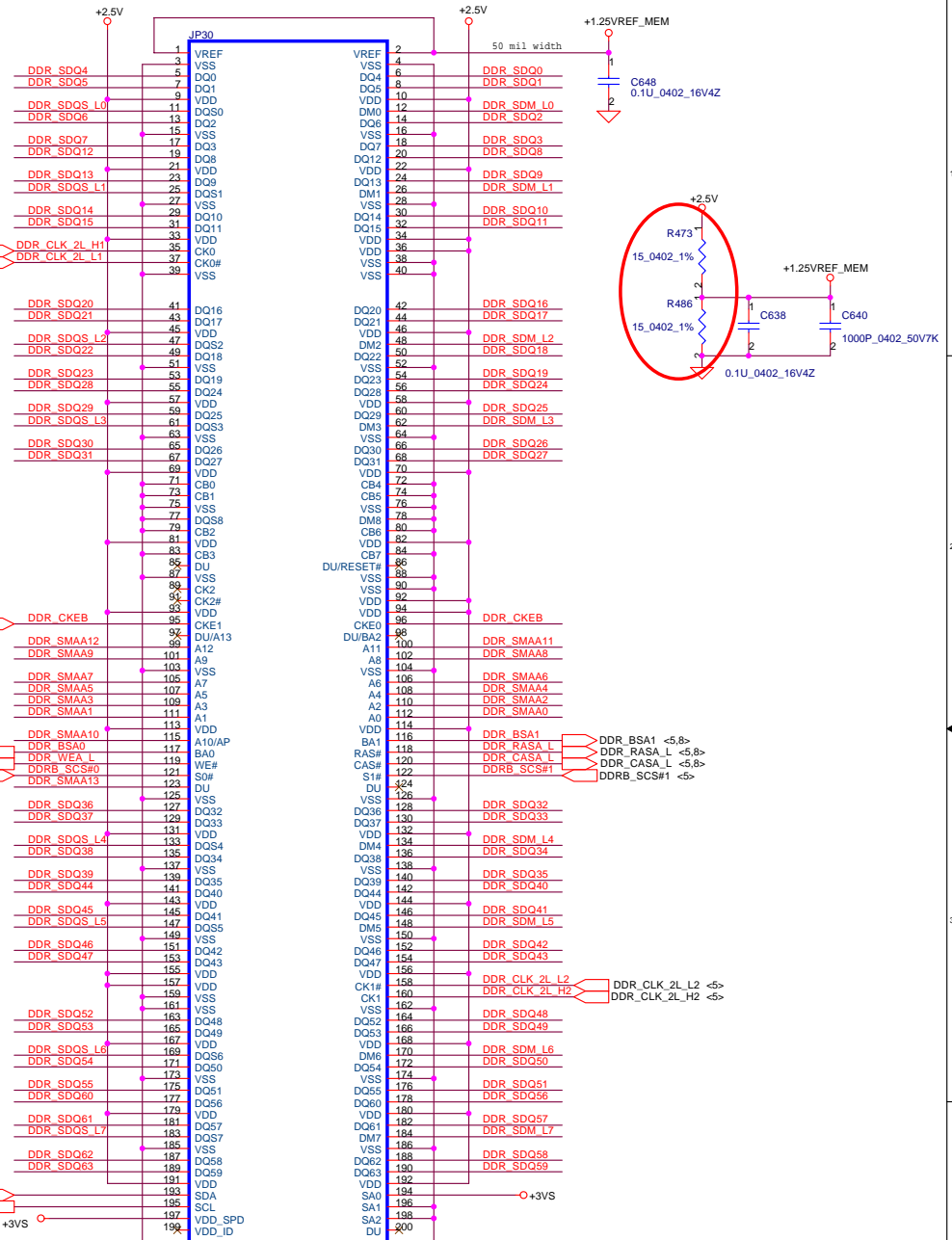
Note:
DDR_SMAA13 Recommend
for AMD.

<-5,8> DDR_BSA0
<-5,8> DDR_WEA L
<-> DDRB_SCS#0
<-> DDRB_SCS#1

<-5,8> DDR_SDQS_L[0..7] <-> DDR_SDQS_L[0..7]
<-5,8> DDR_SDM_L[0..7] <-> DDR_SDM_L[0..7]
<-5,8> DDR_SMAA[0..13] <-> DDR_SMAA[0..13]
<-5,8> DDR_SDQ[0..63] <-> DDR_SDQ[0..63]

<-8,16,20,26> SB_SDAT
<-8,16,20,26> SB_SCLK

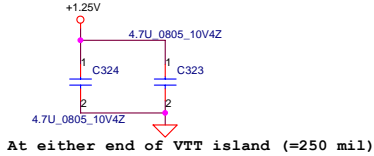
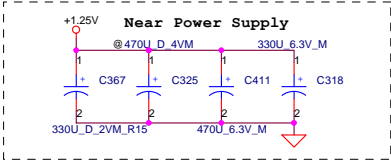
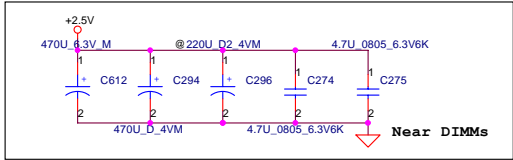
+3VS



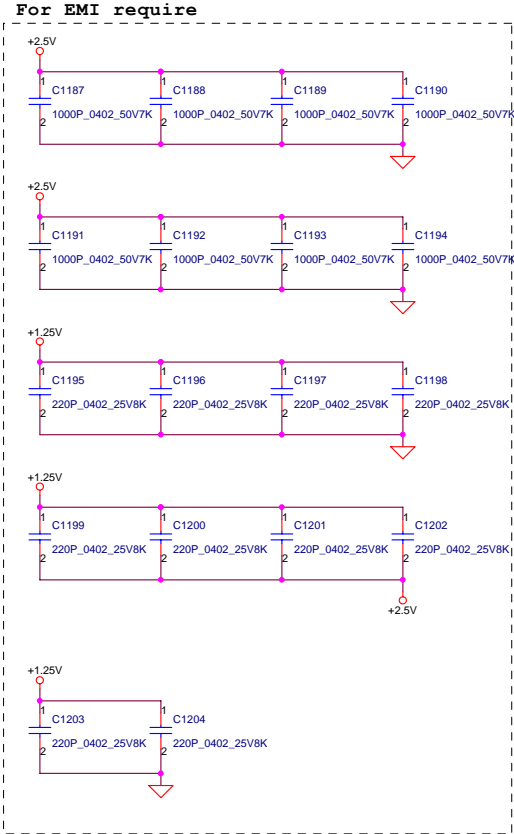
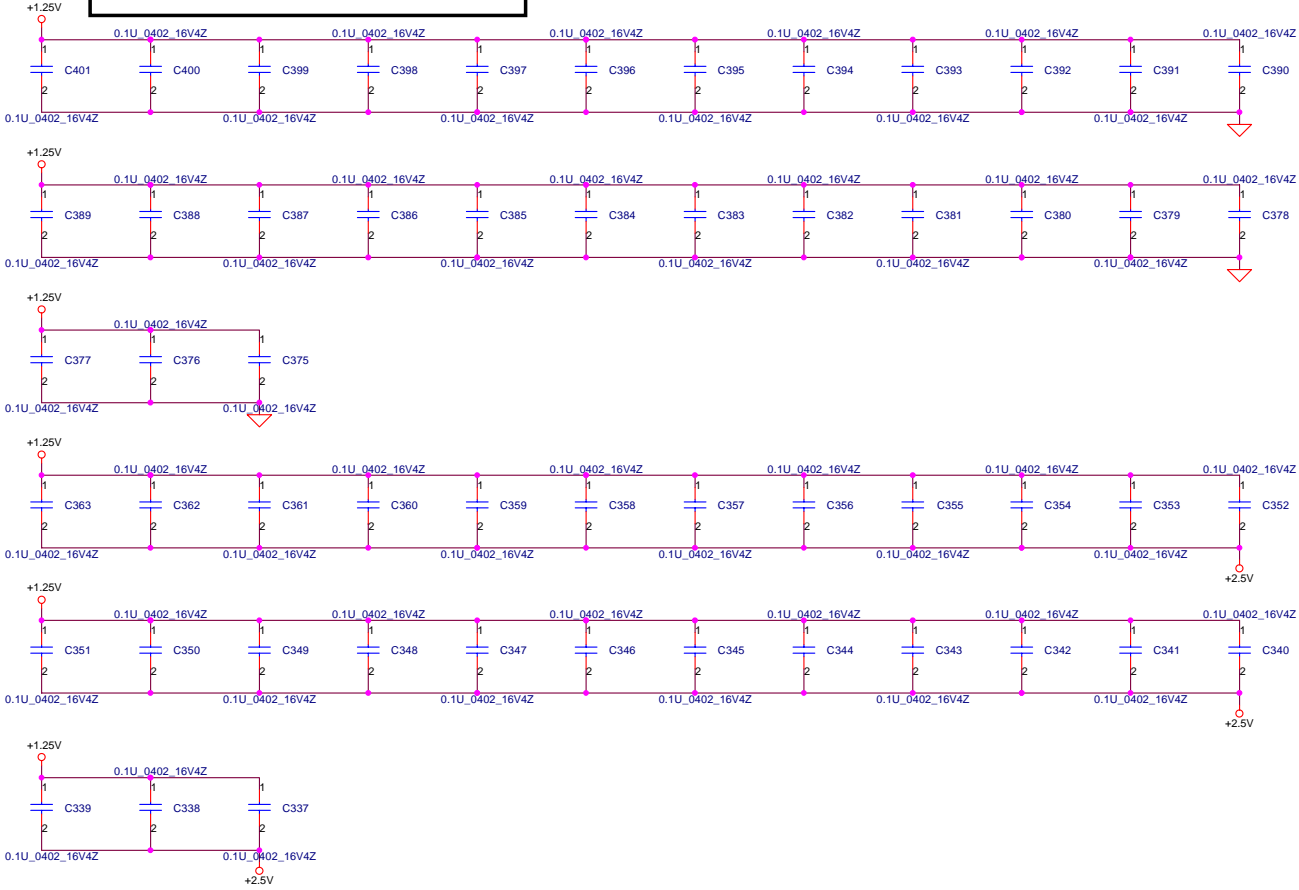
**DIMM1
Bottom Side**

Compal Electronics, Inc.		
DDR-SODIMM SLOT1		
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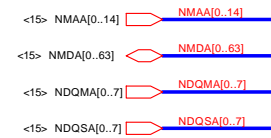
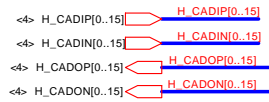


Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS



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Compal Electronics, Inc.			
DDR SODIMM Decoupling			
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HYPER TRANSPORT CPU I/F

MEM_A I/F

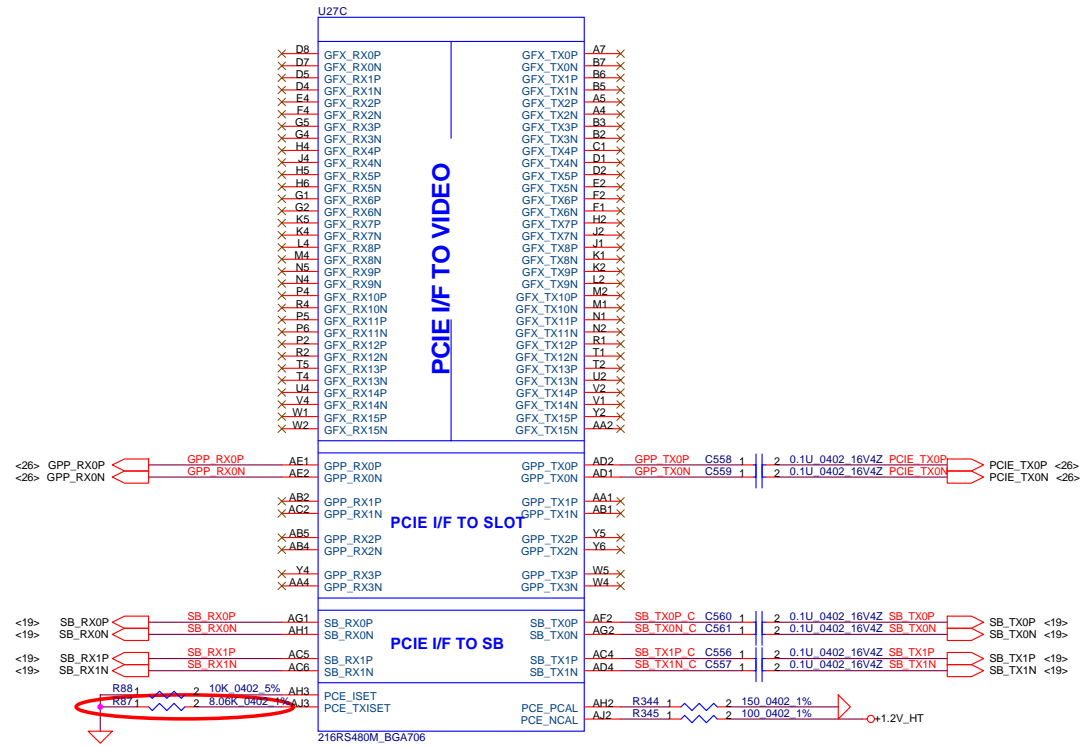
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Title: **RS480M HIT/MEM**

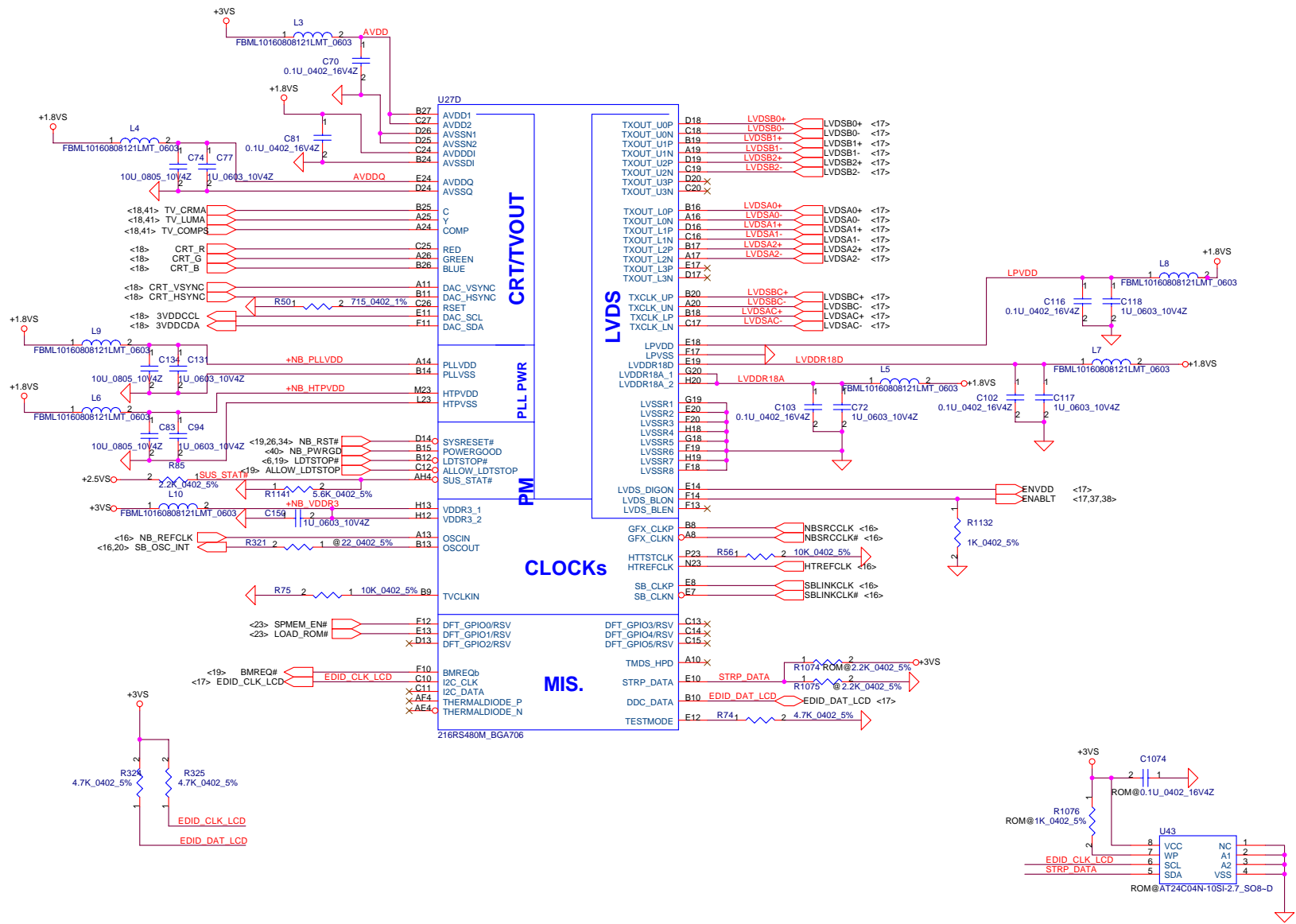
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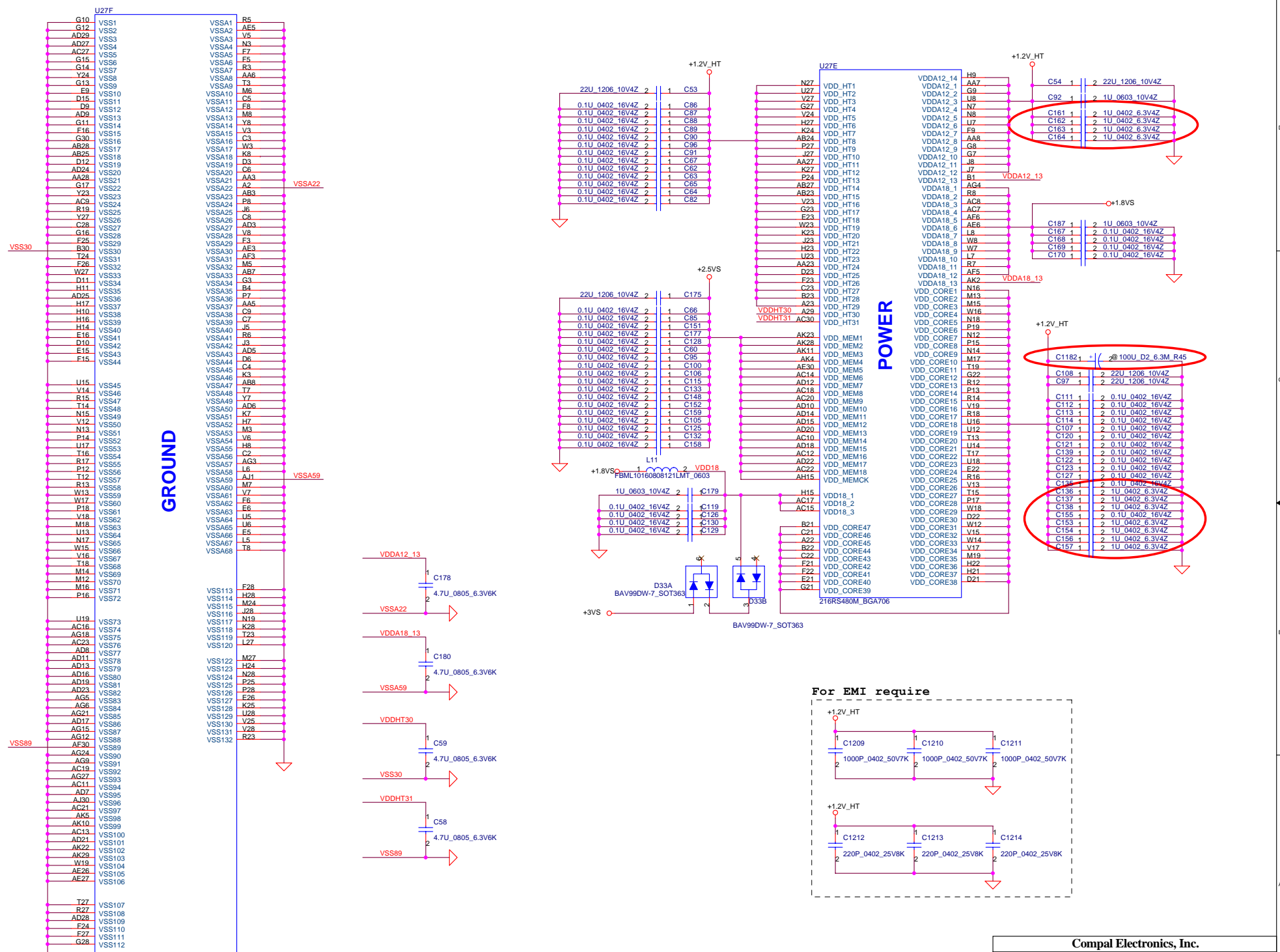
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Title PCIE			
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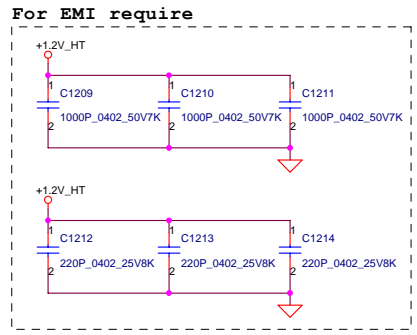
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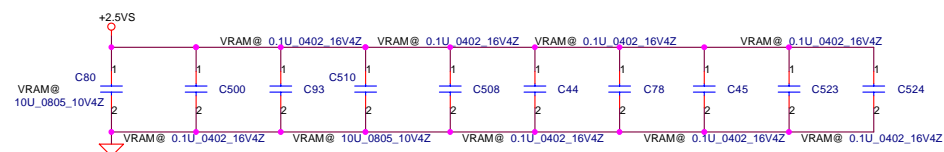
Compal Electronics, Inc.		
Power/GND		
Title		
Size	Document Number	Rev
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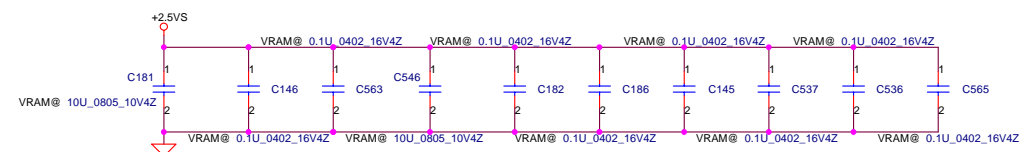
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Title RS480M Power/GND		
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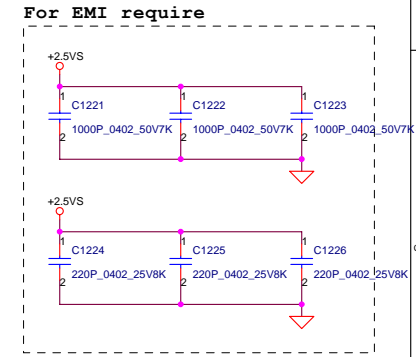
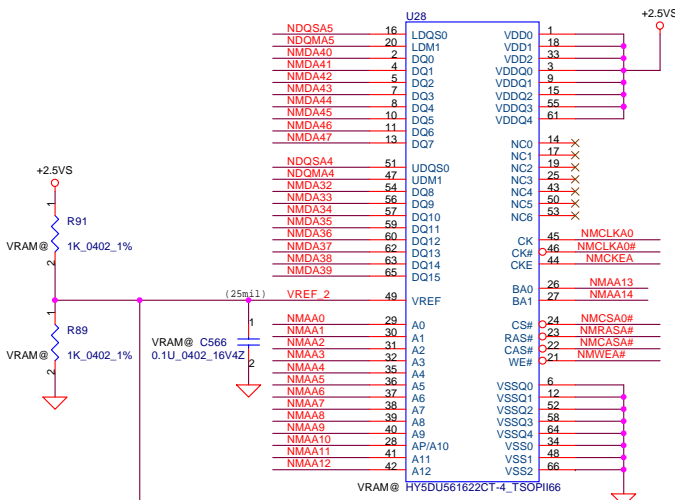
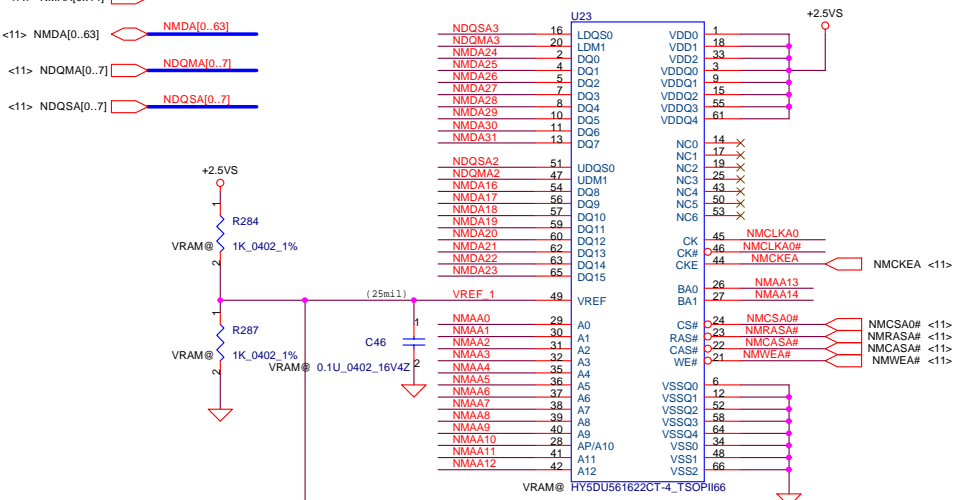


As close as possible to related pin

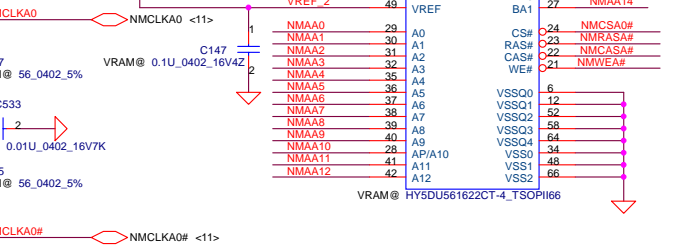
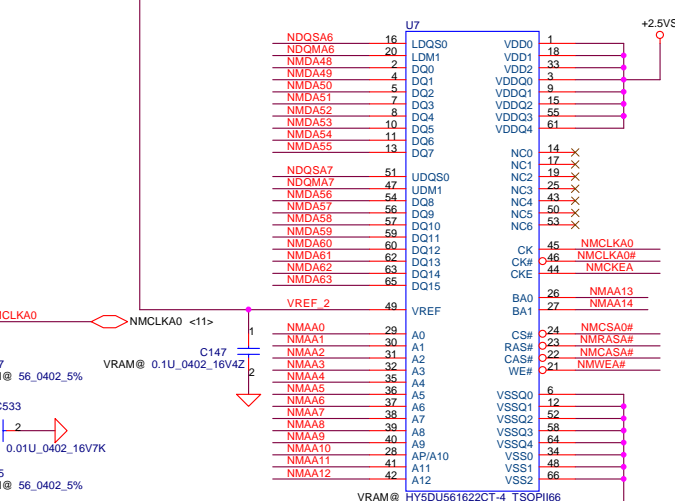
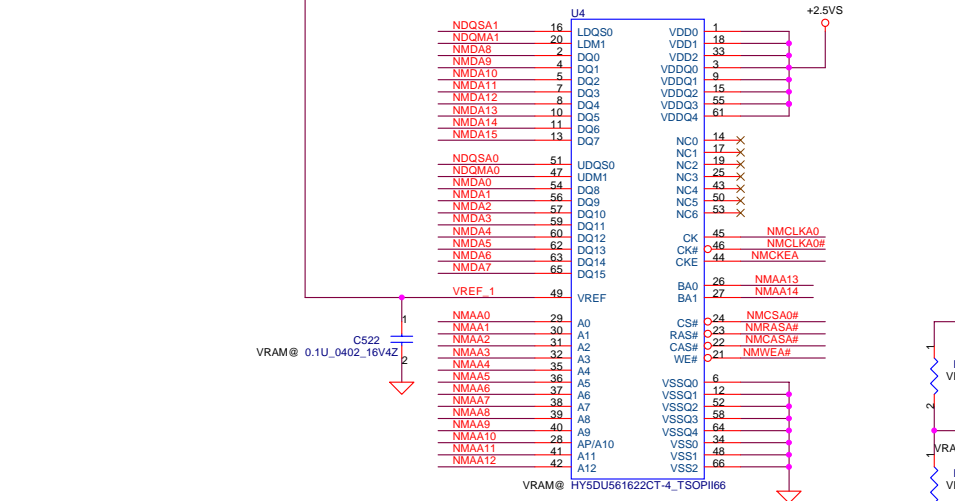


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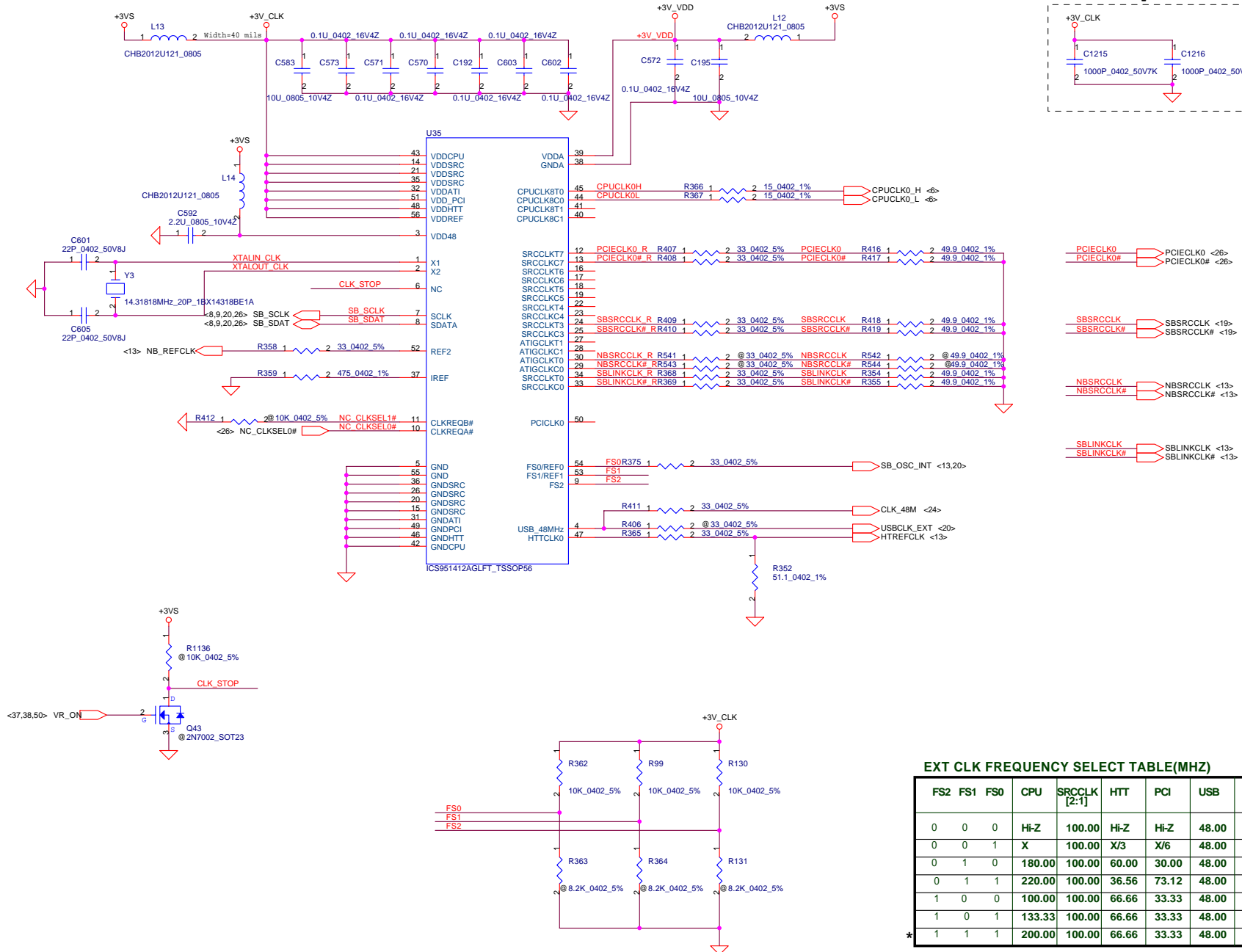
- <11> NMAA[0..14] NMAA[0..14]
- <11> NMDA[0..63] NMDA[0..63]
- <11> NDQMA[0..7] NDQMA[0..7]
- <11> NDQSA[0..7] NDQSA[0..7]



For EMI require



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EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

Compal Electronics, Inc.

Clock Generator

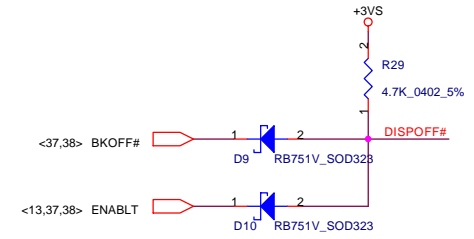
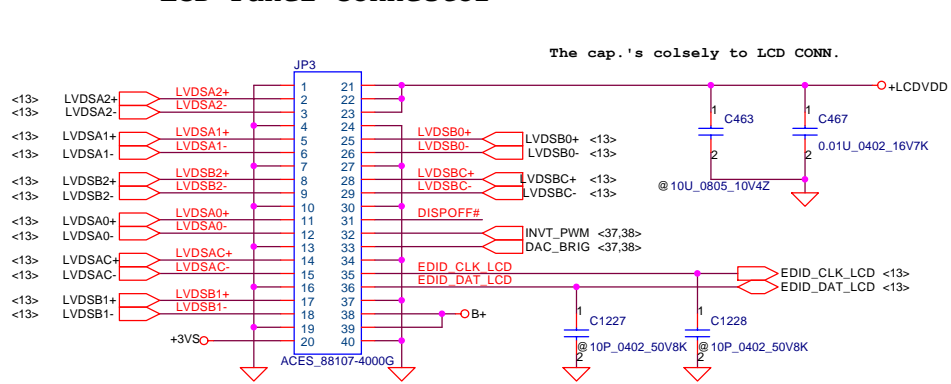
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Size: Document Number **LA-2421** Rev 0.6

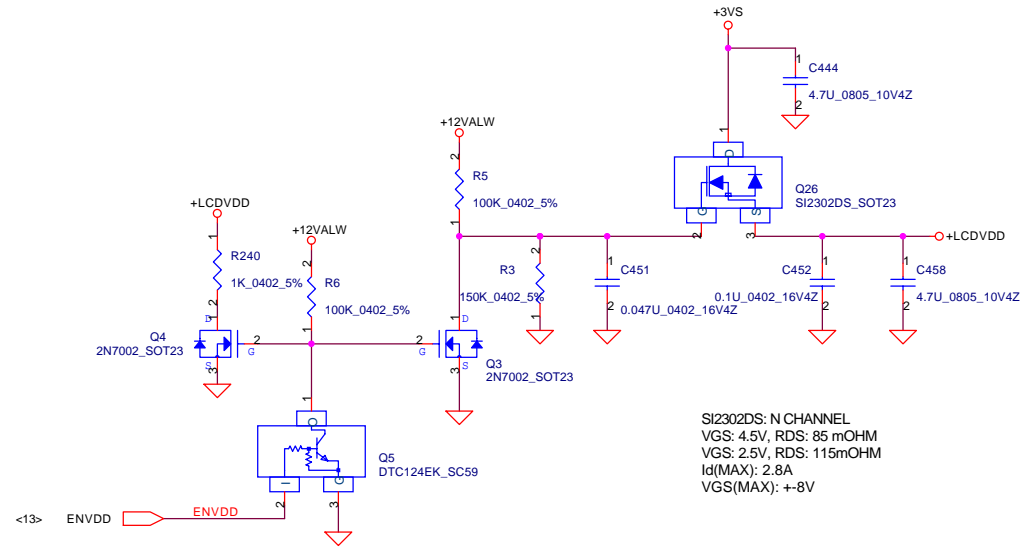
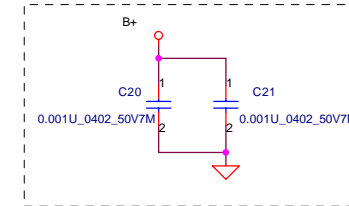
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LCD Panel Connector



EMI require



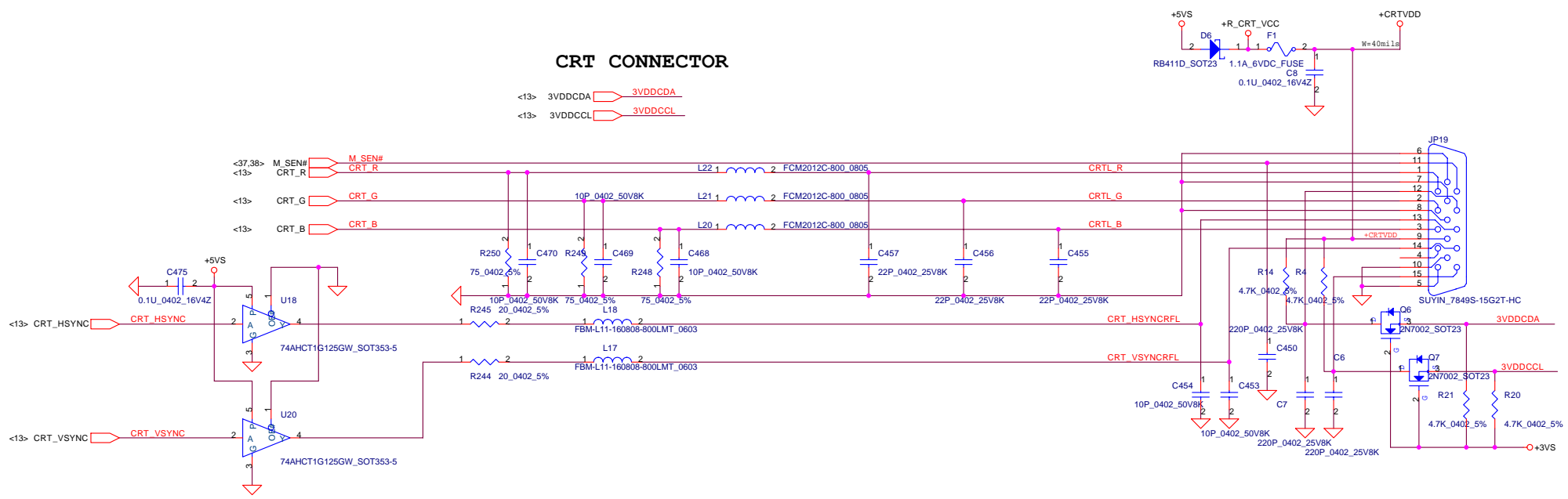
SI2302DS: N CHANNEL
 VGS: 4.5V, RDS: 85 mOHM
 VGS: 2.5V, RDS: 115mOHM
 Id(MAX): 2.8A
 VGS(MAX): +-8V

Compal Electronics, Inc.		
Title: LVDS Connector		
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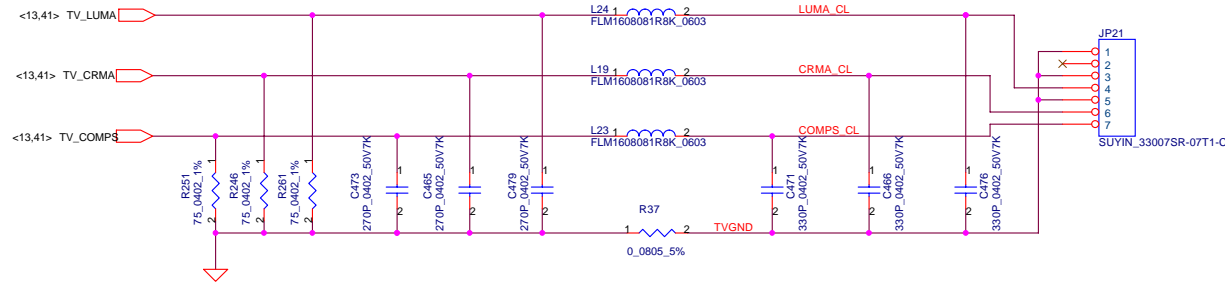
CRT CONNECTOR

<13> 3VDDCCA  3VDDCCA
 <13> 3VDDCCL  3VDDCCL



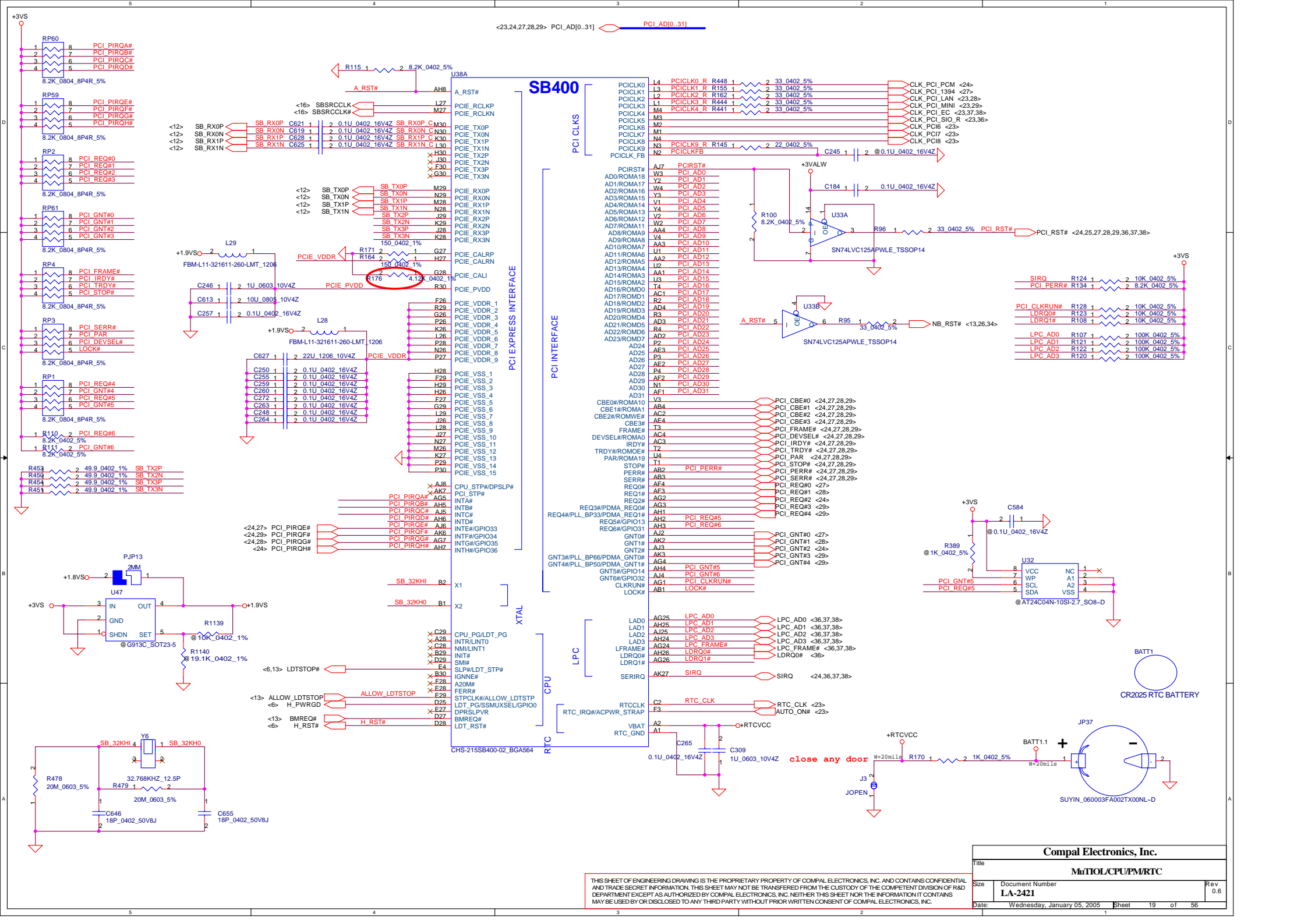
TV-Out Connector

S-Video



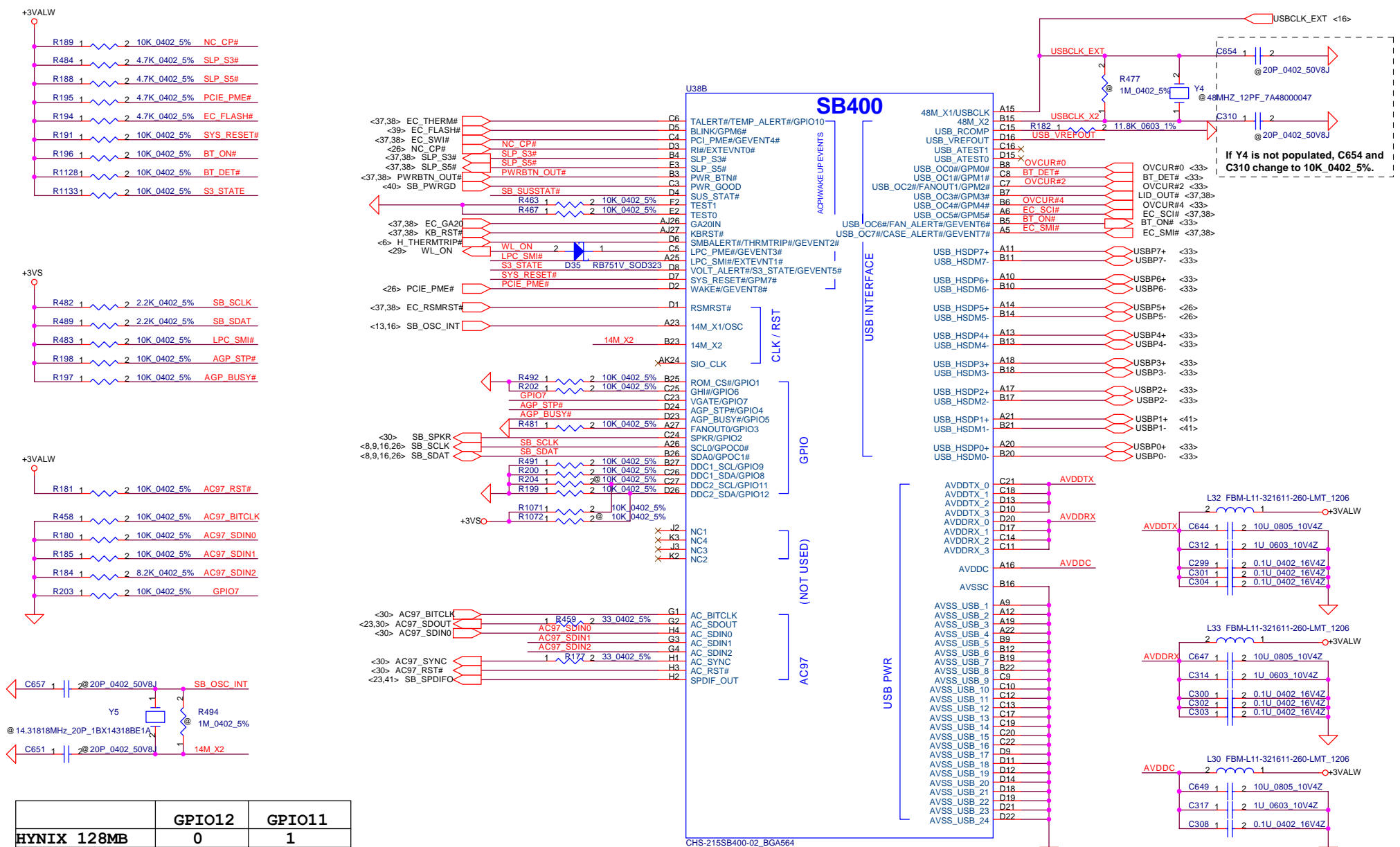
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Compal Electronics, Inc.			
Title CRT & TVout Connector			
Size	Document Number	Rev	
	LA-2421	0.6	
Date:	Wednesday, January 05, 2005	Sheet	18 of 56



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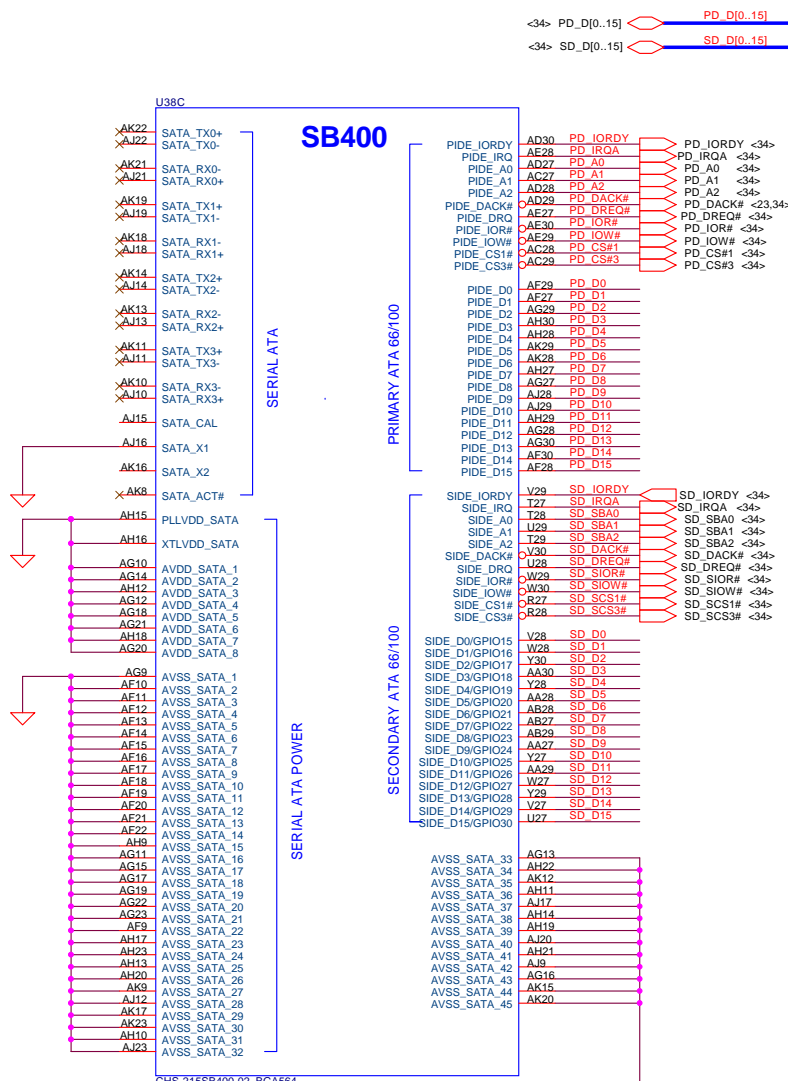
Compal Electronics, Inc.			
Title			
MnTOL/CPU/PM/RTC			
Size	Document Number	Rev	
	LA-2421	0.6	
Date:	Wednesday, January 05, 2005	Sheet	19 of 56



	GPIO12	GPIO11
HYNIX 128MB	0	1
SAMSUNG 128MB	1	1
No VRAM	0	0
Reserved	1	0

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Compal Electronics, Inc.		
Title USB/LPC/AC97/MAC		
Size	Document Number LA-2421	Rev 0.6
Date:	Wednesday, January 05, 2005	Sheet 20 of 56



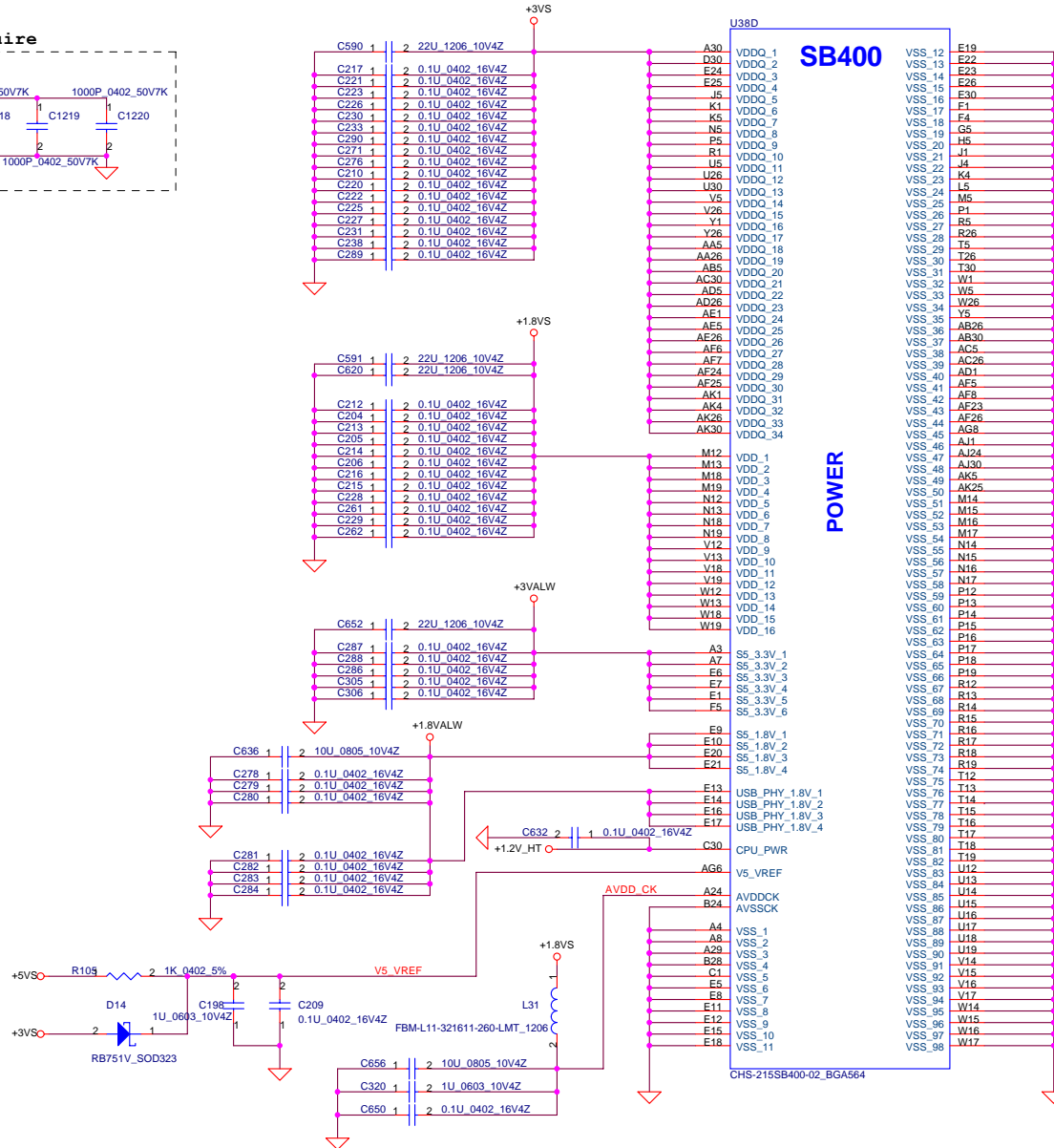
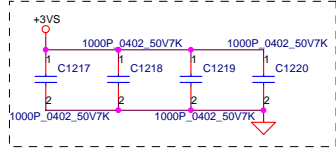
<34> PD_D[0..15] PD_D[0..15]
 <34> SD_D[0..15] SD_D[0..15]

CHS-215SB400-02_BGA564

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Compal Electronics, Inc.			
Title			
IDE/SATA			
Size	Document Number	Rev	
Custom	LA-2421	0.6	
Date:	Wednesday, January 05, 2005	Sheet	21 of 56

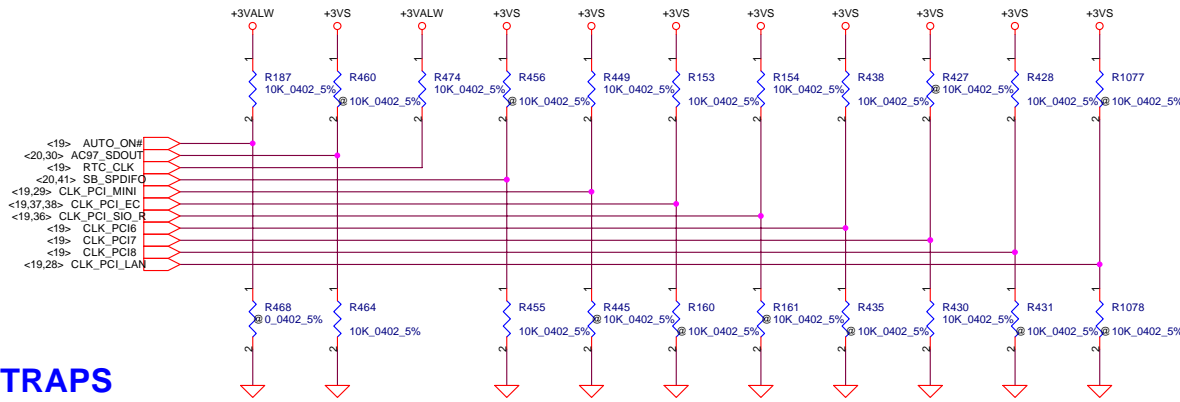
For EMI require



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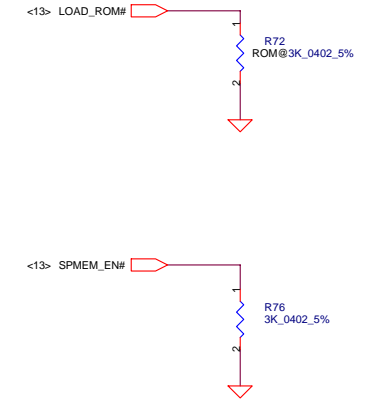
Compal Electronics, Inc.		
Title Power/GND		
Size	Document Number LA-2421	Rev 0.6
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REQUIRED STRAPS



	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz XTAL MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz OSC MODE DEFAULT	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	14MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM	DEFAULT

NB STRAPS



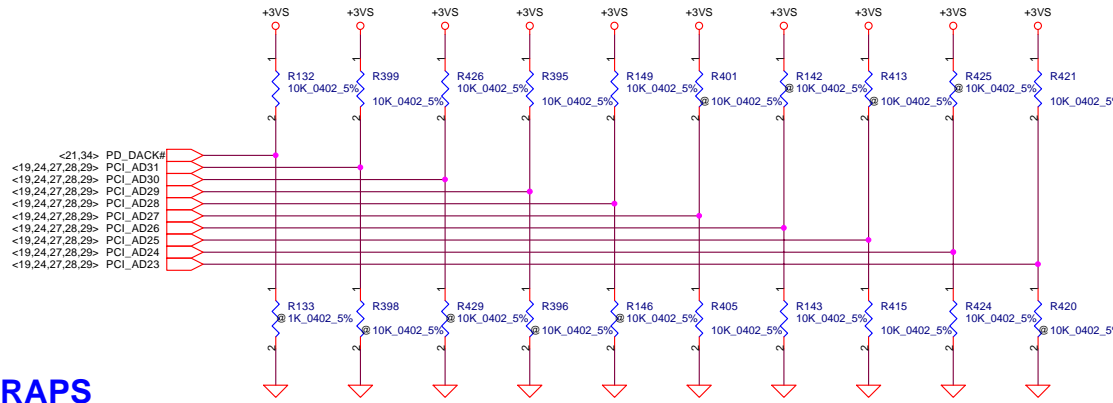
LOAD_ROM#:LOAD ROM STRAP ENABLE strap

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

SPMEM_EN#:SIDE PORT MEMORY ENABLE strap

High, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

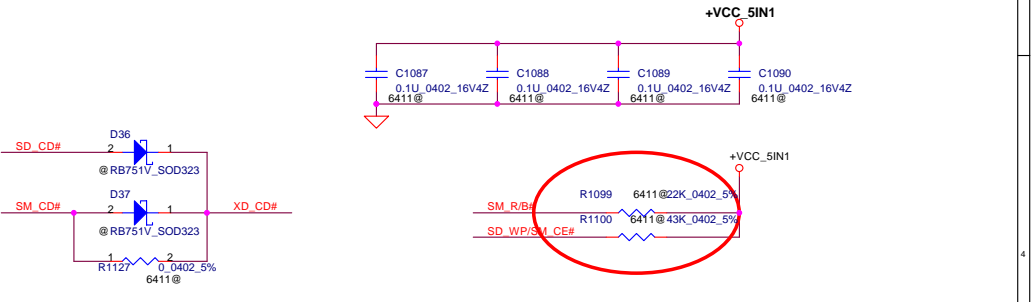
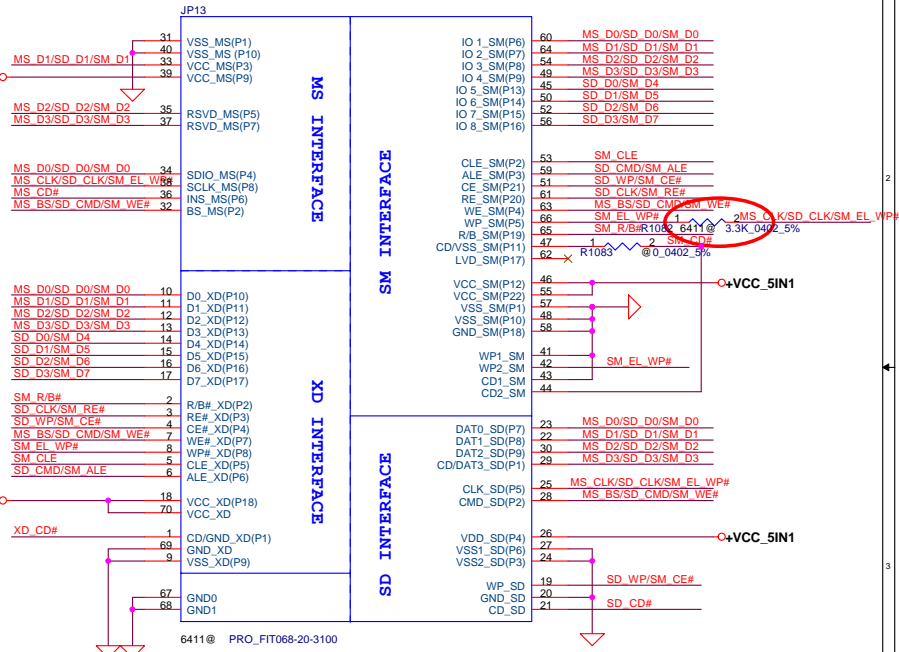
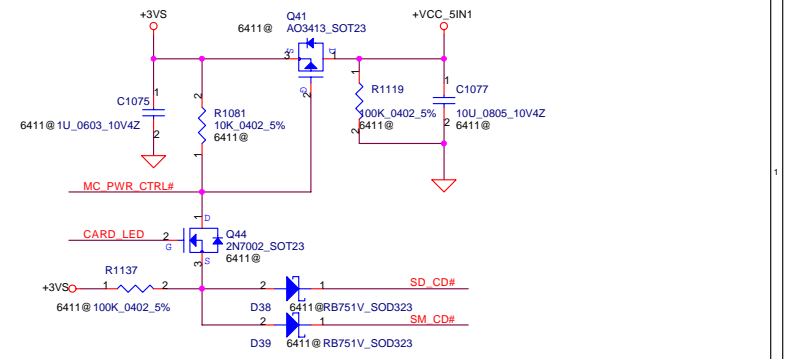
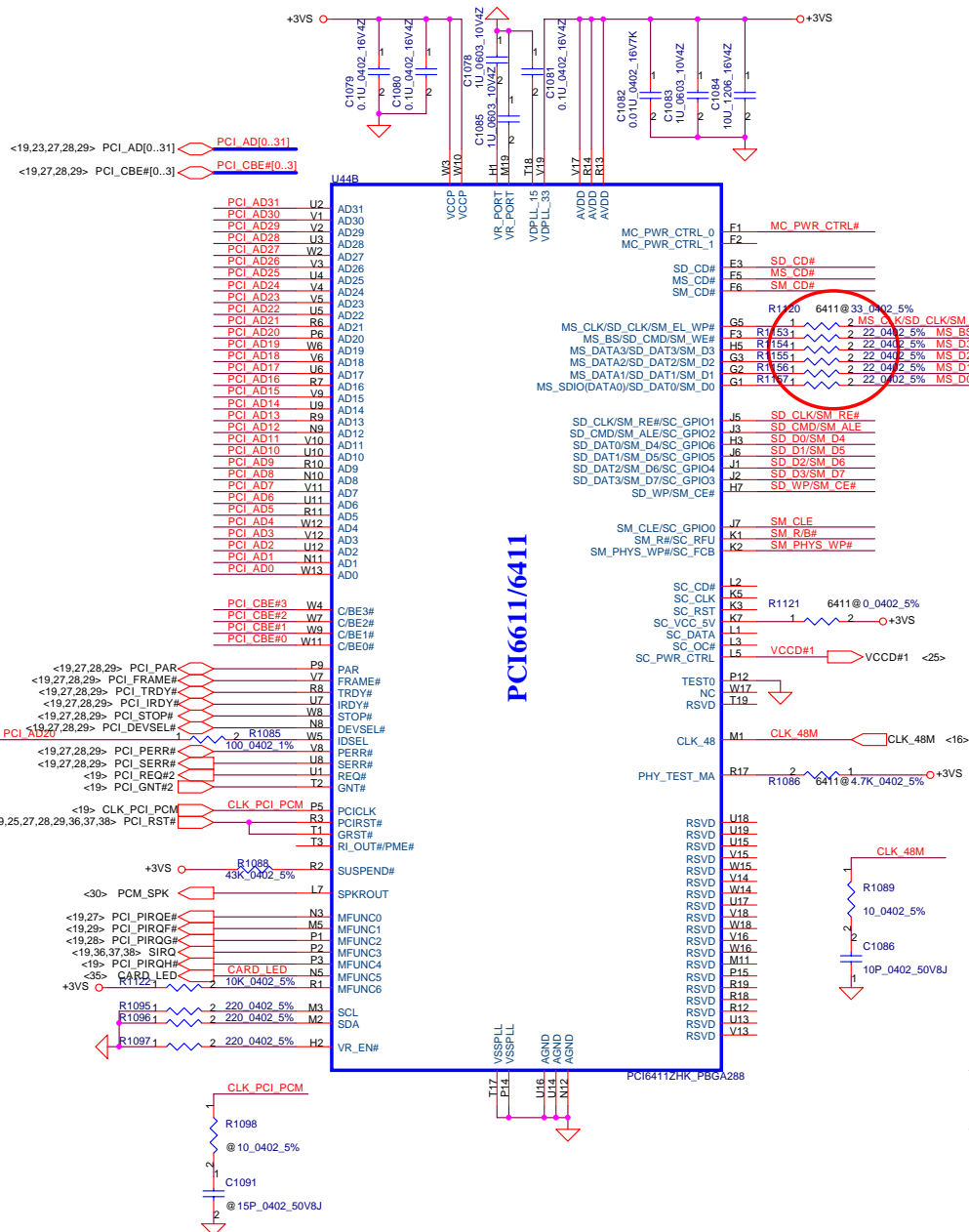
DEBUG STRAPS



	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS ACPI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

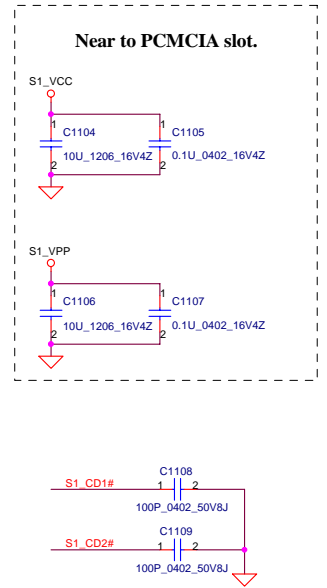
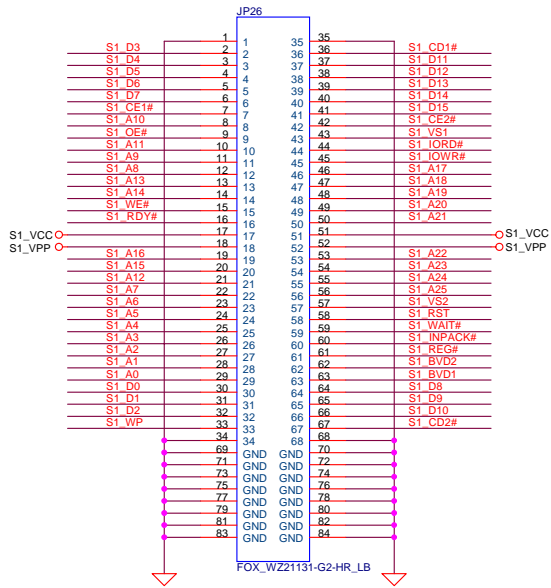
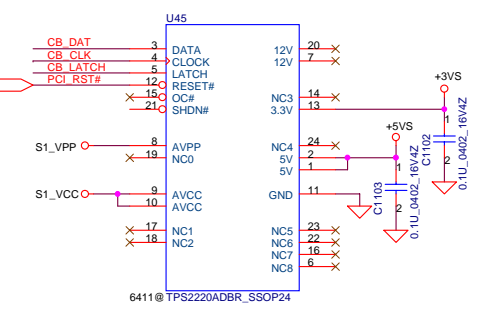
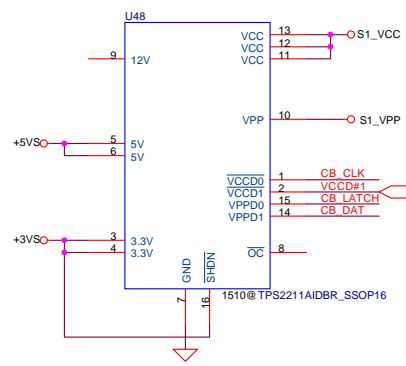
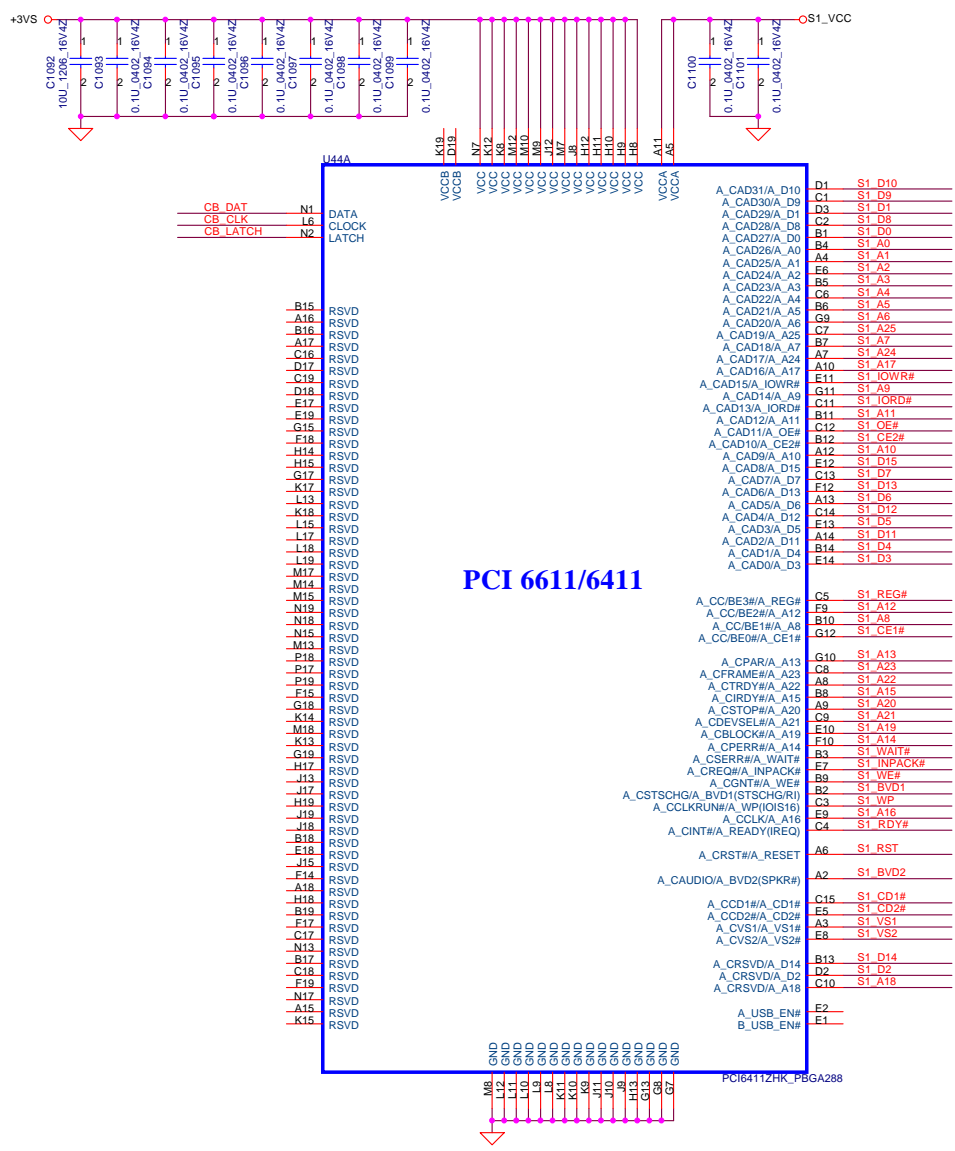
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Compal Electronics, Inc.		
Hardware Strap		
Size	Document Number	Rev
	LA-2421	0.6
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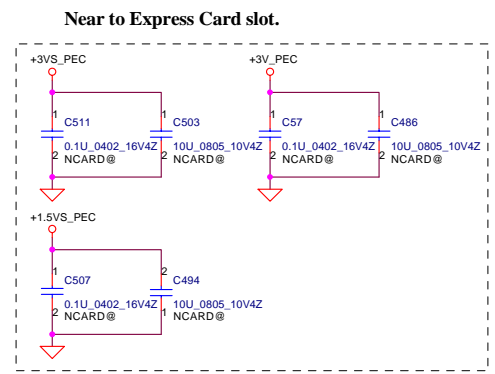
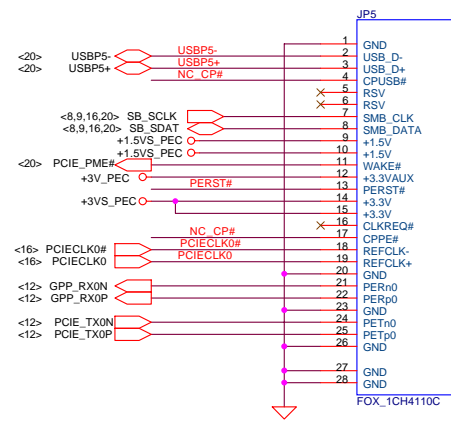
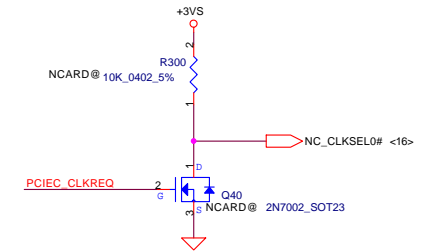
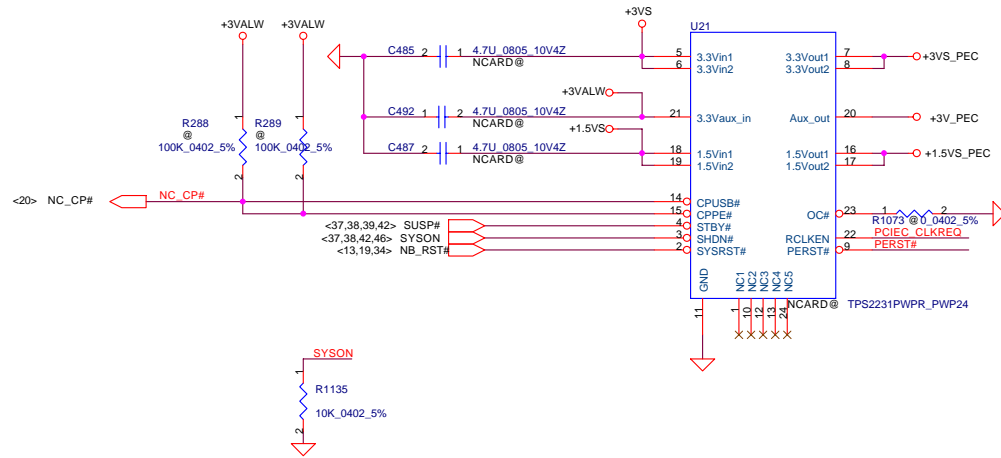


Compal Electronics, Inc.			
TL PCI6411 PCI/SD			
Title			
Size	Document Number	Rev	
Custom	LA-2421	0.6	
Date:	Wednesday, January 05, 2005	Sheet	24 of 56

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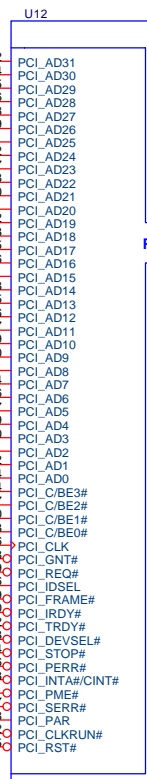


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Title		
Compal Electronics, Inc.		
Express Card socket		
Size	Document Number	Rev
Custom	LA-2421	0.6
Date:	Wednesday, January 05, 2005	Sheet 26 of 56

<19,23,24,28,29> PCI_AD[0..31]

- PCI_AD31
- PCI_AD30
- PCI_AD29
- PCI_AD28
- PCI_AD27
- PCI_AD26
- PCI_AD25
- PCI_AD24
- PCI_AD23
- PCI_AD22
- PCI_AD21
- PCI_AD20
- PCI_AD19
- PCI_AD18
- PCI_AD17
- PCI_AD16
- PCI_AD15
- PCI_AD14
- PCI_AD13
- PCI_AD12
- PCI_AD11
- PCI_AD10
- PCI_AD9
- PCI_AD8
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- PCI_AD4
- PCI_AD3
- PCI_AD2
- PCI_AD1
- PCI_AD0

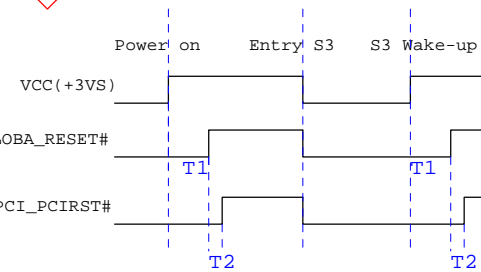
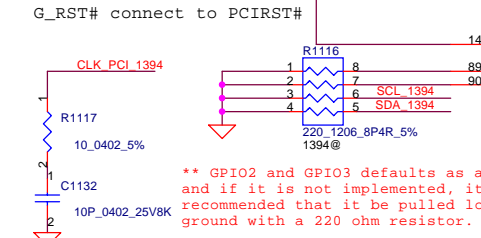
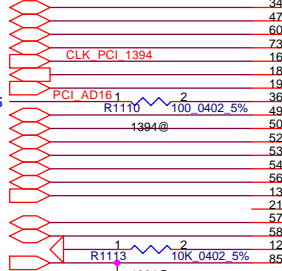


TSB43AB22

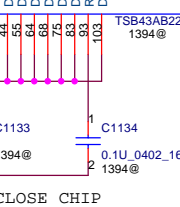
PCI BUS INTERFACE



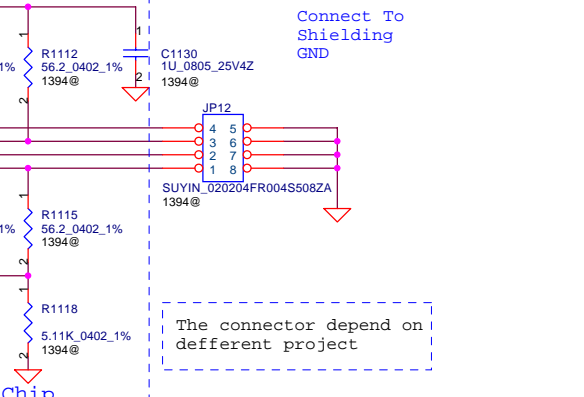
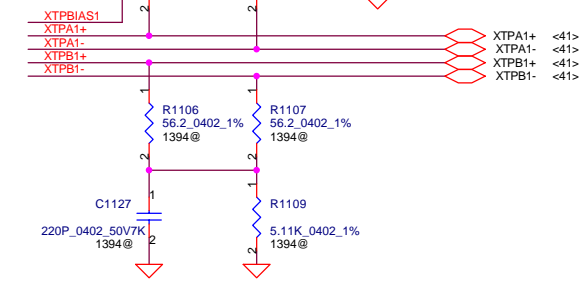
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- <19,24,28,29> PCI_CBE#2
- <19,24,28,29> PCI_CBE#1
- <19,24,28,29> PCI_CBE#0
- <19> CLK_PCI_1394
- <19> PCI_GNT#0
- <19> PCI_REQ#0
- ID: AD16
- PCI_FRAME#
- PCI_IRDY#
- PCI_TRDY#
- PCI_DEVSEL#
- PCI_STOP#
- PCI_PERR#
- PCI_PIRQE#
- PCI_SERR#
- PCI_PAR
- PCI_RST#



Note: GLOBAL_RESET#
Can Connect to
PCI_PCIRST#



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The connector depend on defferent project

EEPROM cancel
need System
Support

Close Chip

Connect To
Shielding
GND

Compal Electronics, Inc.		
Title IEEE 1394 CONTROLLER		
Size	Document Number LA-2421	Rev 0.6
Date:	Wednesday, January 05, 2005	Sheet 27 of 56

<19.23,24,27,29> PCI_AD[0..31]

PCI AD0	104	AD0
PCI AD1	103	AD1
PCI AD2	102	AD2
PCI AD3	98	AD3
PCI AD4	97	AD4
PCI AD5	95	AD5
PCI AD6	95	AD6
PCI AD7	93	AD7
PCI AD8	90	AD8
PCI AD9	89	AD9
PCI AD10	87	AD10
PCI AD11	86	AD11
PCI AD12	85	AD12
PCI AD13	83	AD13
PCI AD14	82	AD14
PCI AD15	79	AD15
PCI AD16	58	AD16
PCI AD17	58	AD17
PCI AD18	57	AD18
PCI AD19	55	AD19
PCI AD20	53	AD20
PCI AD21	49	AD21
PCI AD22	49	AD22
PCI AD23	47	AD23
PCI AD24	43	AD24
PCI AD25	42	AD25
PCI AD26	42	AD26
PCI AD27	39	AD27
PCI AD28	37	AD28
PCI AD29	36	AD29
PCI AD30	33	AD30
PCI AD31	33	AD31

PCI I/F

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<19.24,27,29>	PCI_CBE#2	CBE#2	44
<19.24,27,29>	PCI_CBE#3	CBE#3	44

<19.24,27,29>	PCI_AD22	1	LAN_IDSEL	46
<19.24,27,29>	PCI_PAR	76	PAR	76
<19.24,27,29>	PCI_FRAME#	61	FRAME#	61
<19.24,27,29>	PCI_IRDY#	63	IRDY#	63
<19.24,27,29>	PCI_TRDY#	67	TRDY#	67
<19.24,27,29>	PCI_DEVSEL#	68	DEVSEL#	68
<19.24,27,29>	PCI_STOP#	69	STOP#	69

<19.24,27,29>	PCI_PERR#	70	PERR#	70
<19.24,27,29>	PCI_SERR#	75	SERR#	75
<19>	PCI_REQ#1	30	REQ#	30
<19>	PCI_GNT#1	29	GNT#	29

<19.24>	PCI_PIRQG#	25	INTA#	25
<29,37,38>	PME_EC#	31	PME#	31
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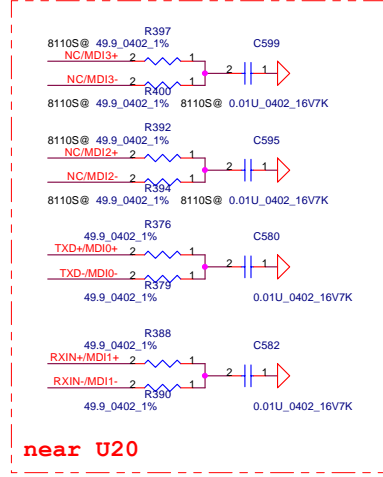
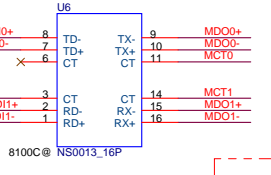
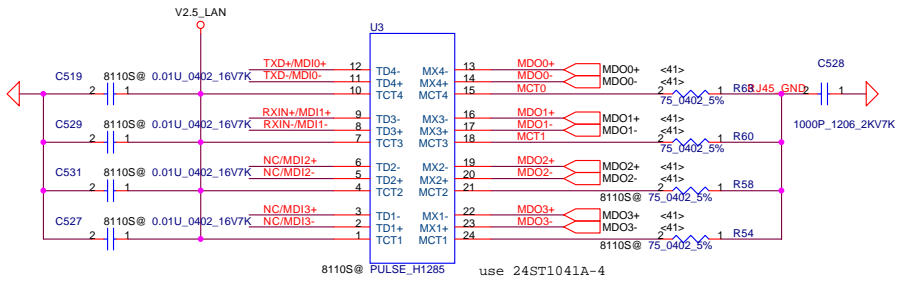
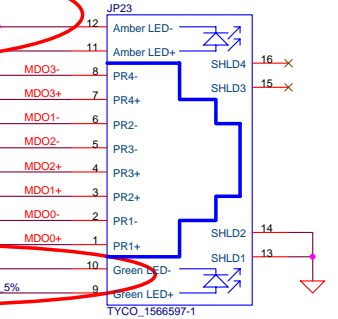
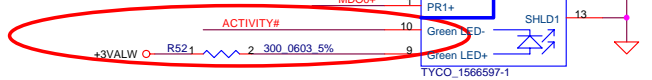
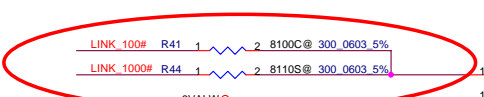
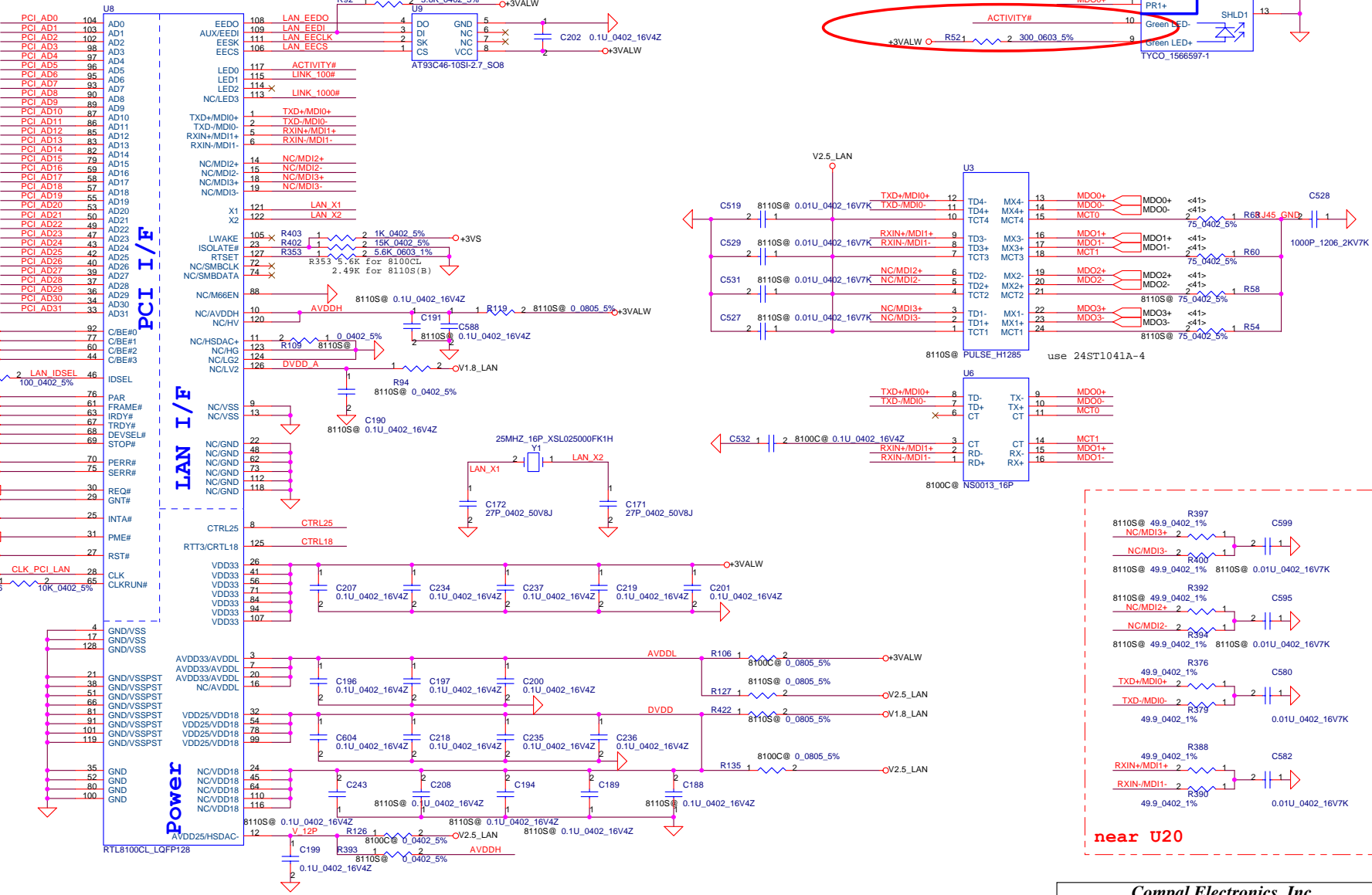
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<19.23>	CLK_RUN#	65	CLKRUN#	65

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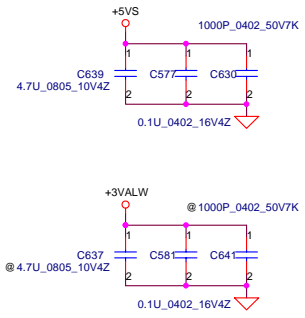
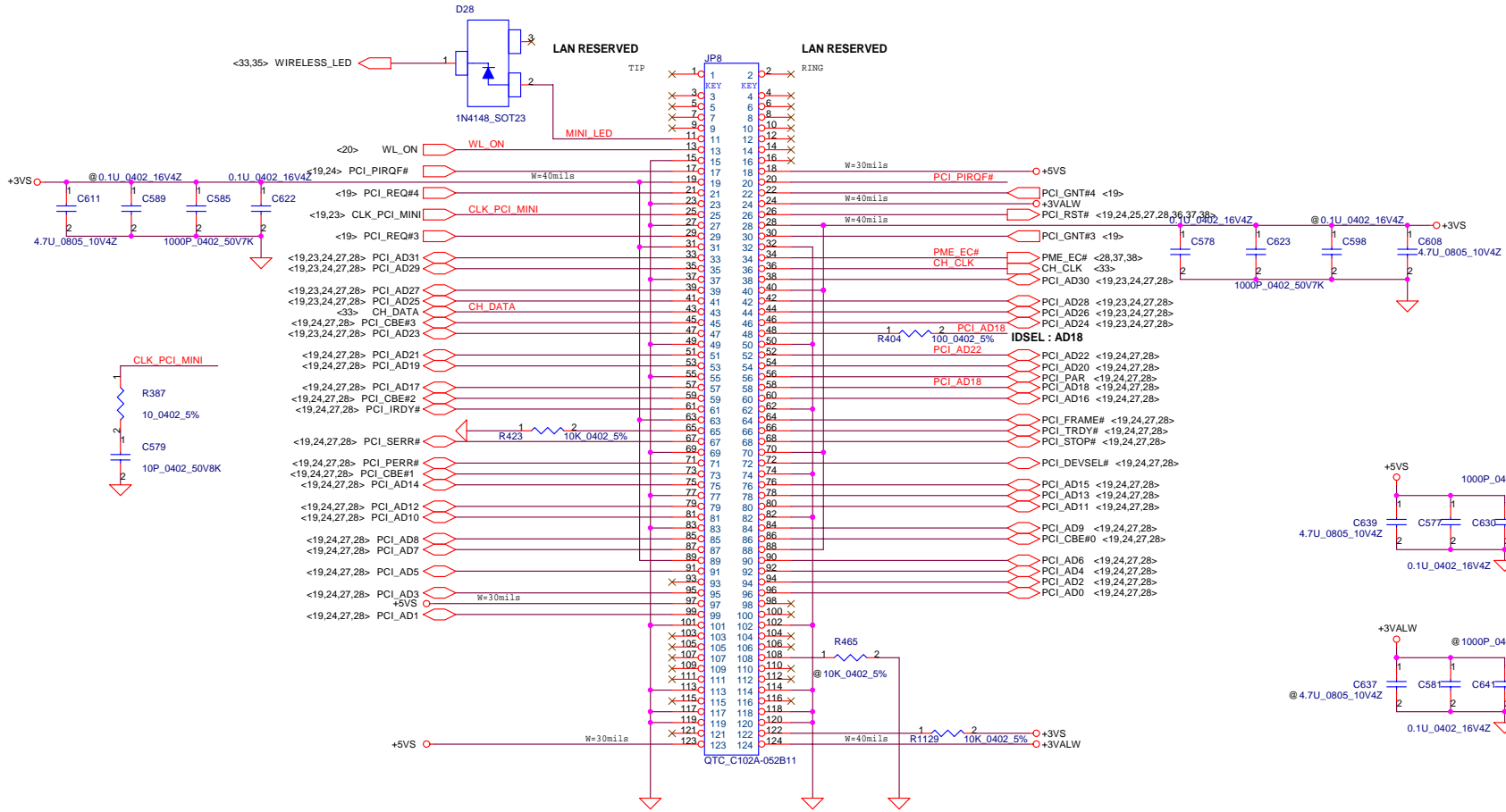
LAN I/F

Power



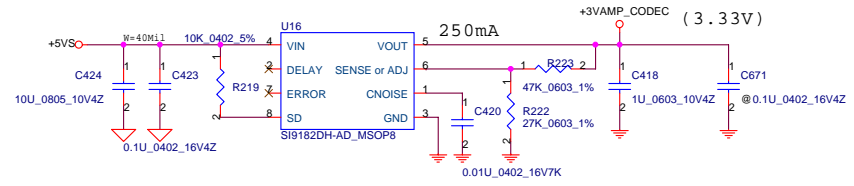
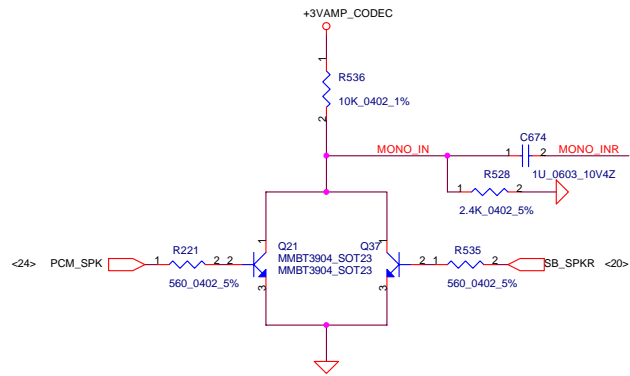
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Title			
LAN RealTech8100CL/8110SBL			
Size	Document Number	Rev	
	LA-2421	0.6	
Date:	Wednesday, January 05, 2005	Sheet	28 of 56

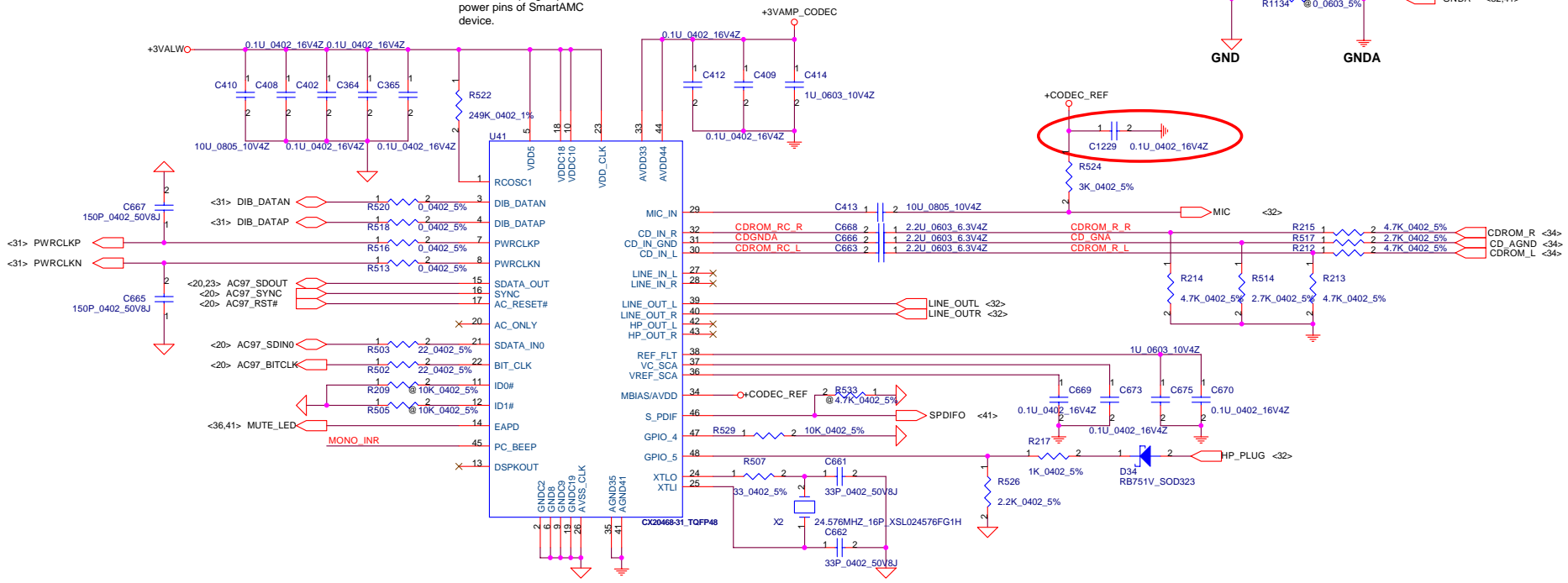


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Compal Electronics, Inc.		
Title Mini PCI Slot		
Size	Document Number LA-2421	Rev 0.6
Date:	Wednesday, January 05, 2005	Sheet 29 of 56



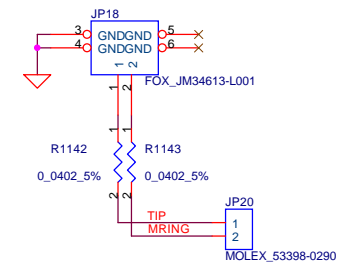
For Layout:
Place decoupling caps near the power pins of SmartAMC device.



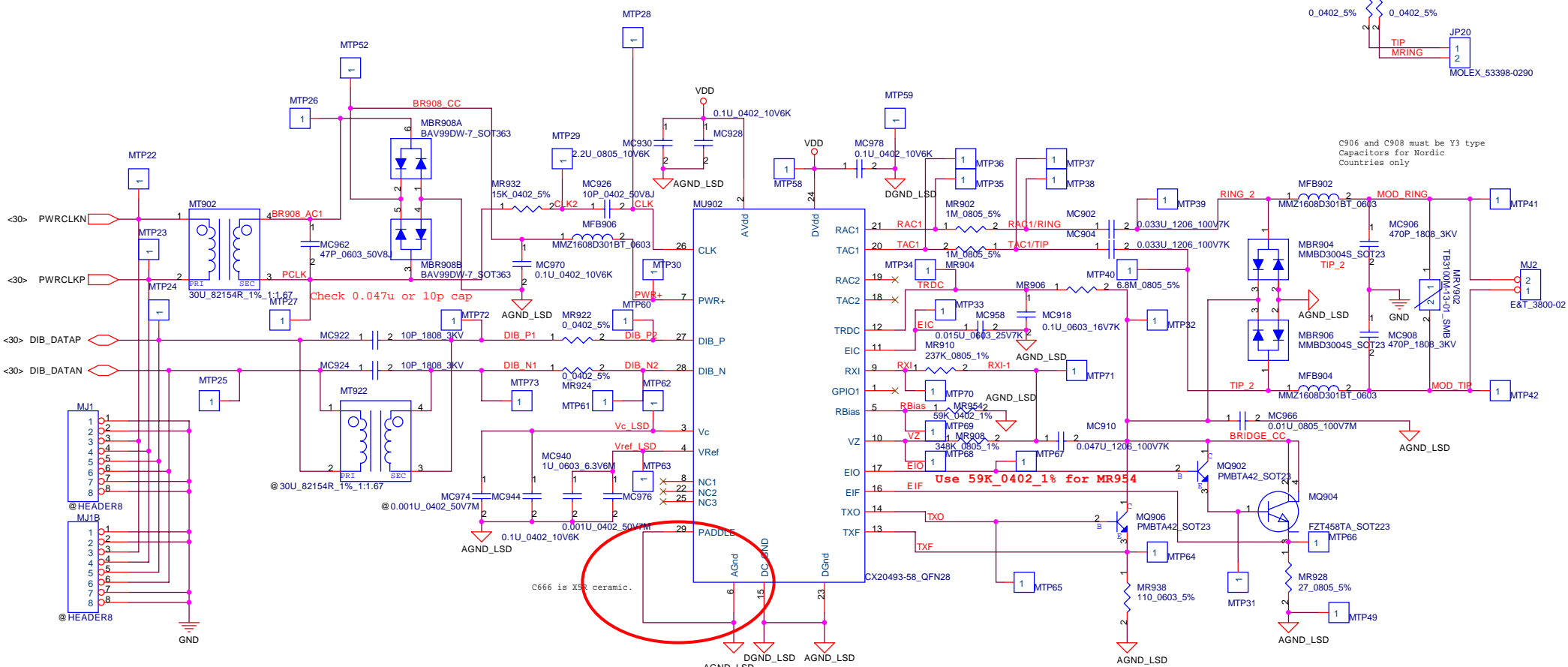
Compal Electronics, Inc.		
Title Codec CX20468-31		
Size	Document Number LA-2421	Rev 0.6
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RJ11 CONN.



C906 and C908 must be Y3 type Capacitors for Nordic Countries only

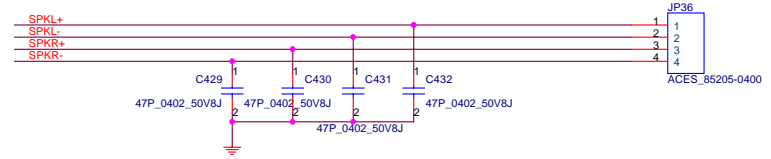
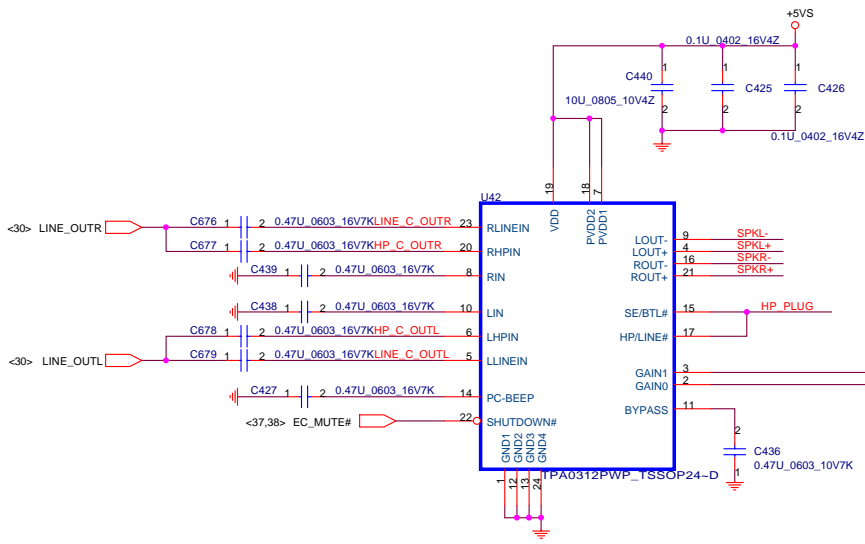


Compal Electronics, Inc.

AMOM_modem

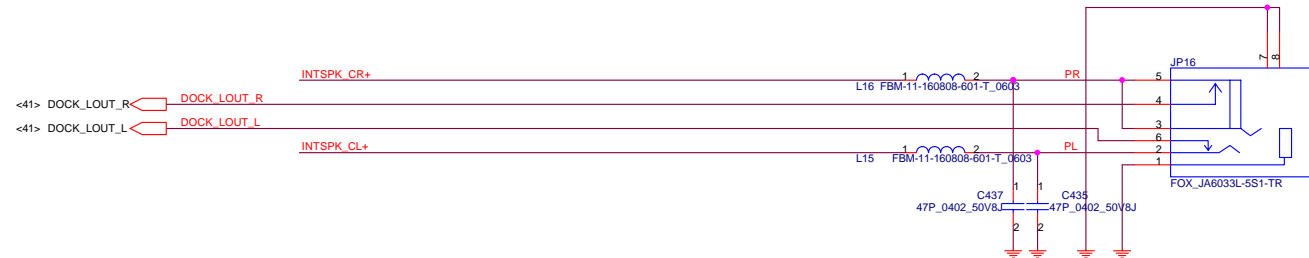
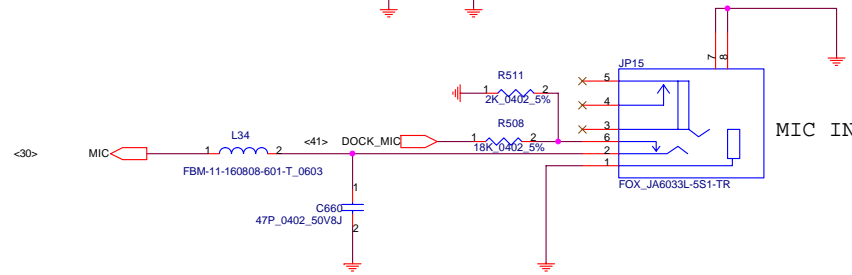
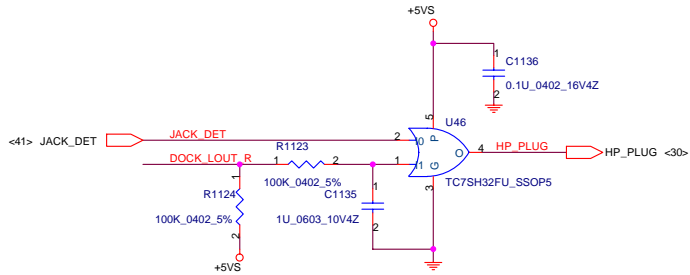
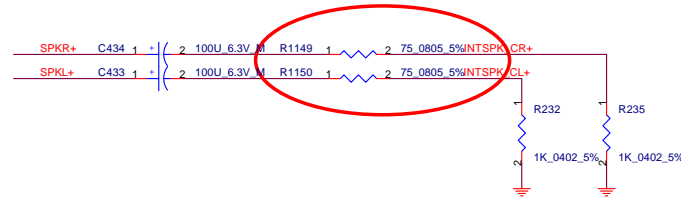
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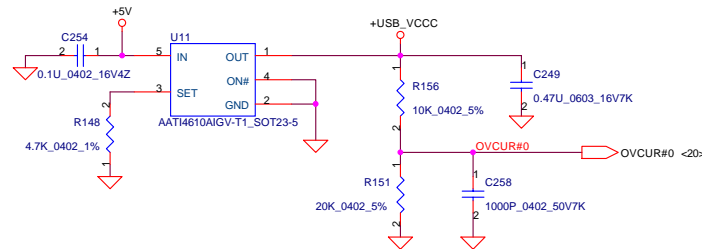
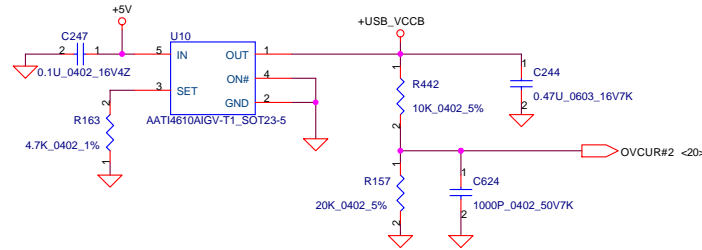
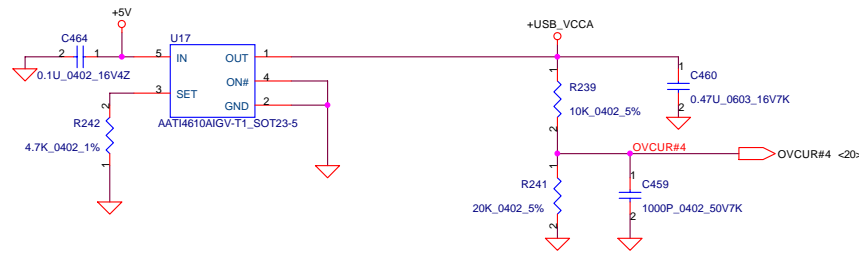
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av (inv)
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0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

HEADPHONE OUT/LINE OUT

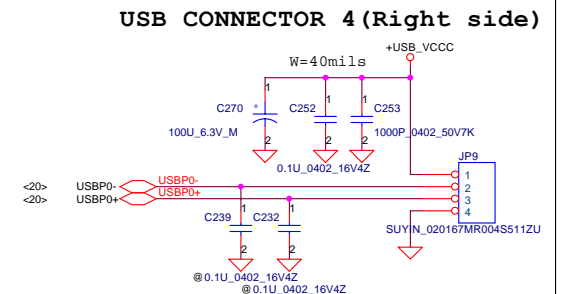
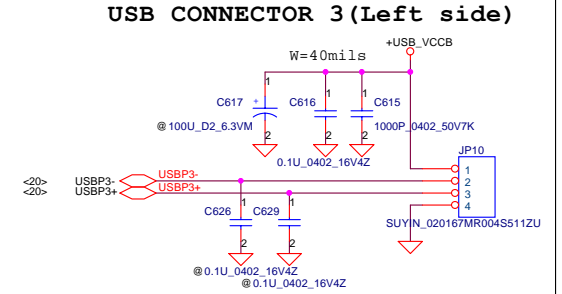
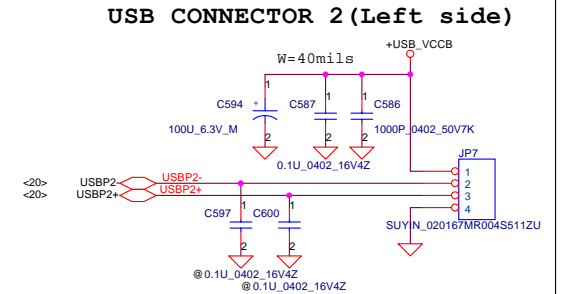
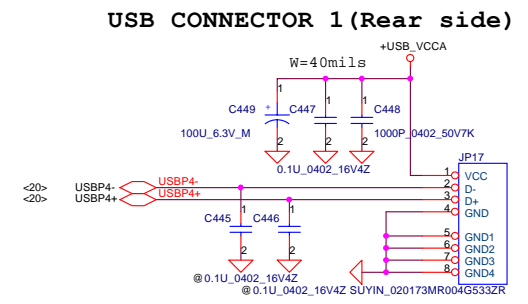


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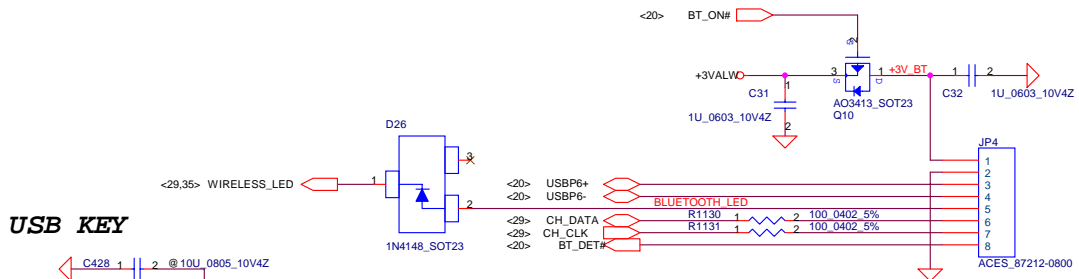
Compal Electronics, Inc.		
Title AMP & Audio Jack		
Size	Document Number LA-2421	Rev 0.6
Custom Date	Wednesday, January 05, 2005	Sheet 32 of 56



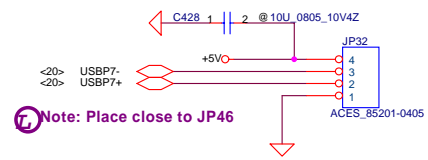
Note: PLACE CLOSE TO EACH USB PORT



BT CONNECTOR



USB KEY



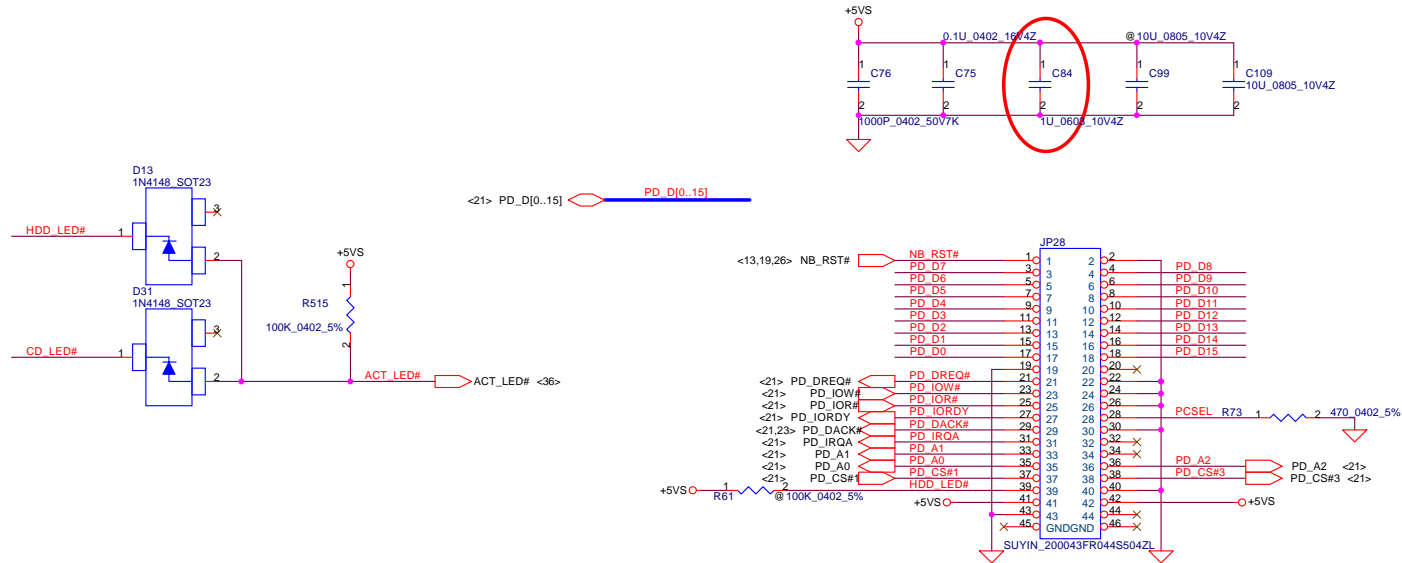
Note: Place close to JP46

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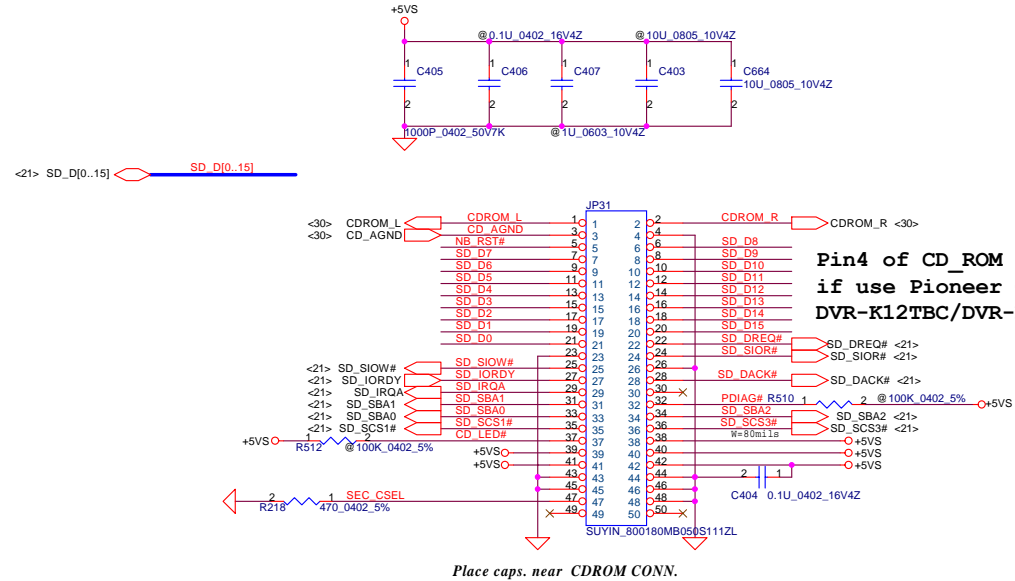
Compal Electronics, Inc.		
Title Bluetooth & USB CONN.		
Size	Document Number LA-2421	Rev 0.6
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HDD/CD-ROM Module

Place caps. near HDD CONN.

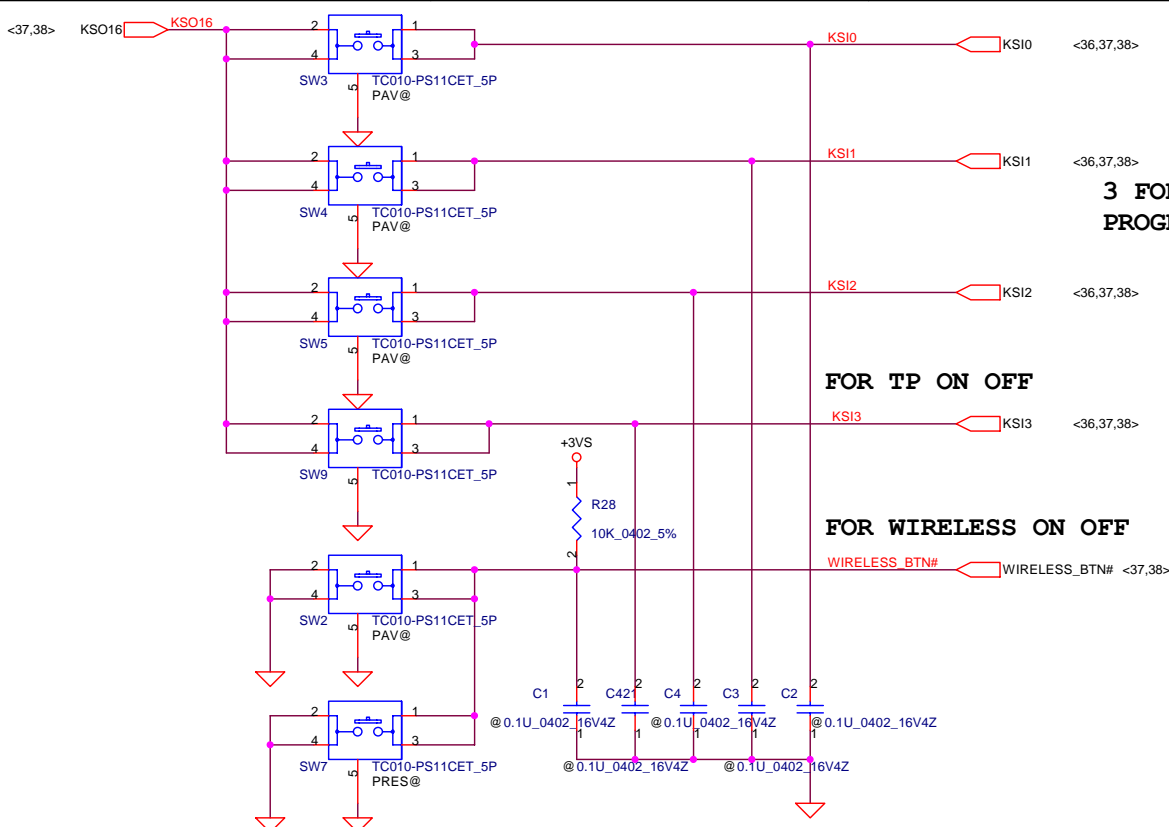


Place caps. near CDROM CONN.



Compal Electronics, Inc.		
HDD & CDROM Connector		
Title		
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3 FOR PROGRAMING

FOR TP ON OFF

FOR WIRELESS ON OFF

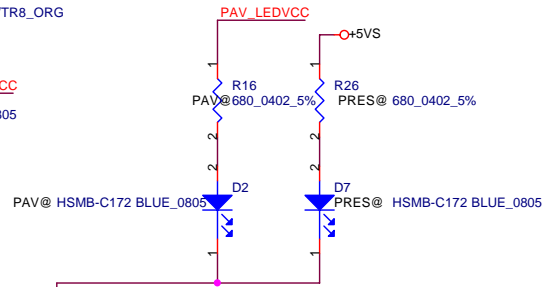
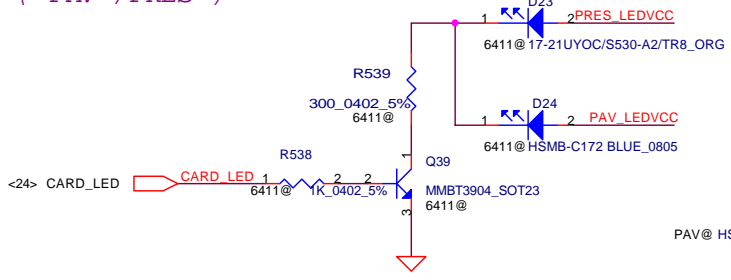
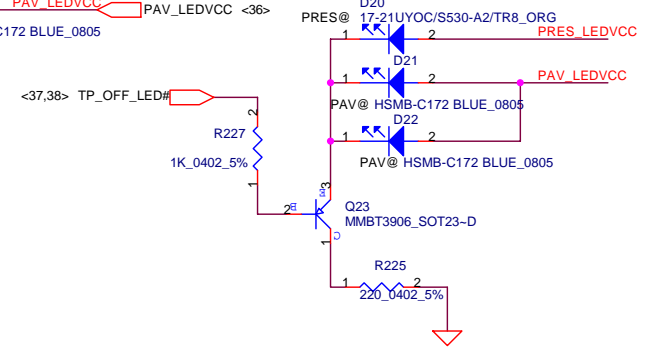
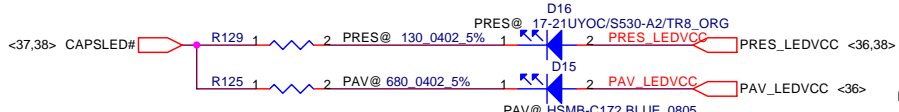
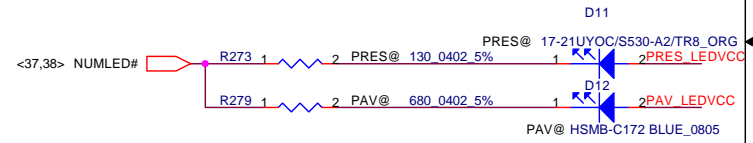
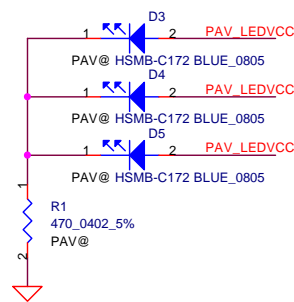
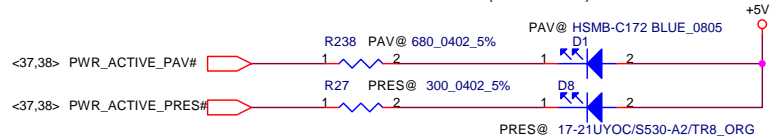
FOR POWER BUTTON BACKLIGHT (PAV)

FOR POWER BUTTON BACKLIGHT (PRES)

FOR 3 PROGRAMING BUTTON BACKLIGHT (PAV)

FOR CARDREADER INDICATOR (PAV /PRES)

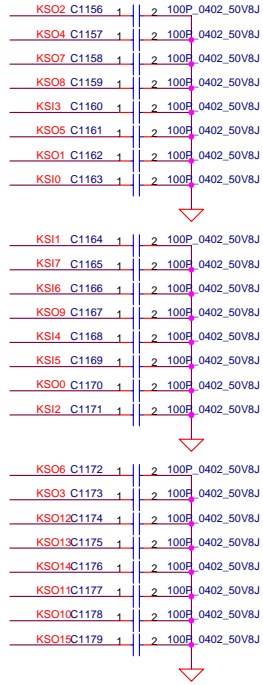
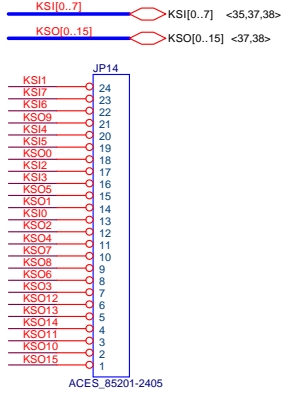
FOR WIRLESS LED



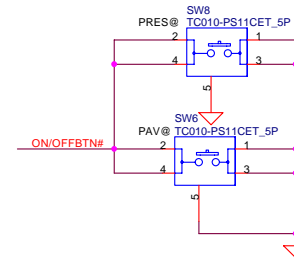
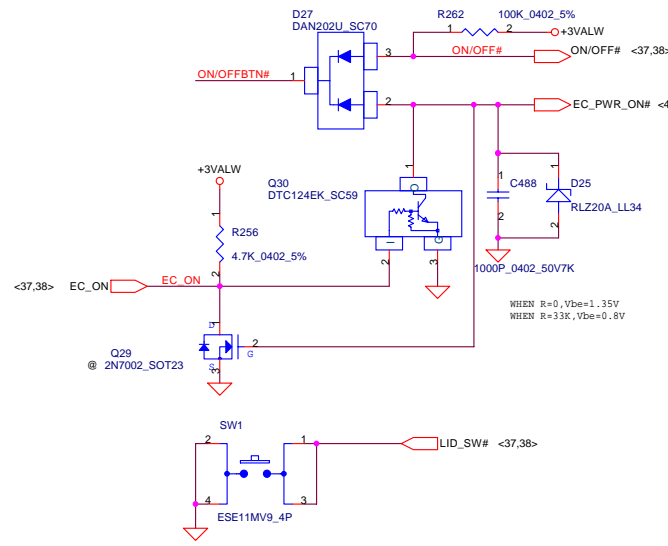
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Compal Electronics, Inc.		
LED INDICATOR		
Title		
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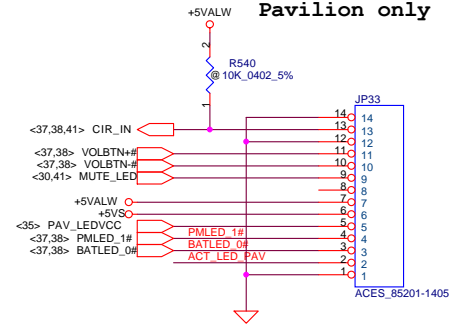
INT_KBD CONN.



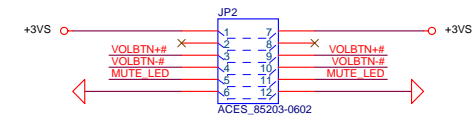
Power BTN



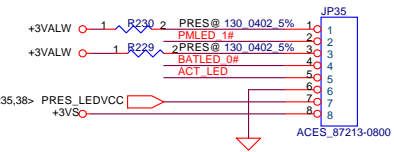
Front Board CONNECTOR Pavilion only



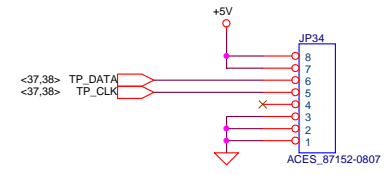
PRESARIO only



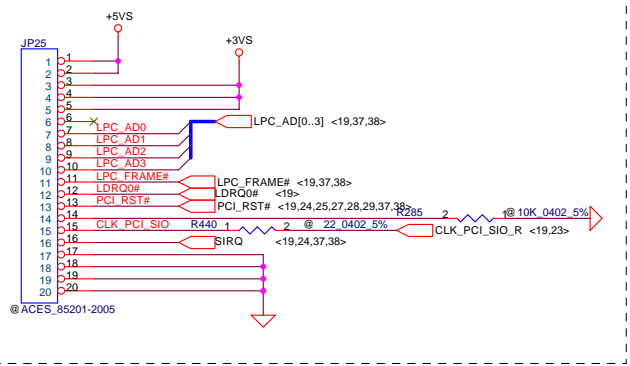
PRESARIO only



TP CONNECTOR

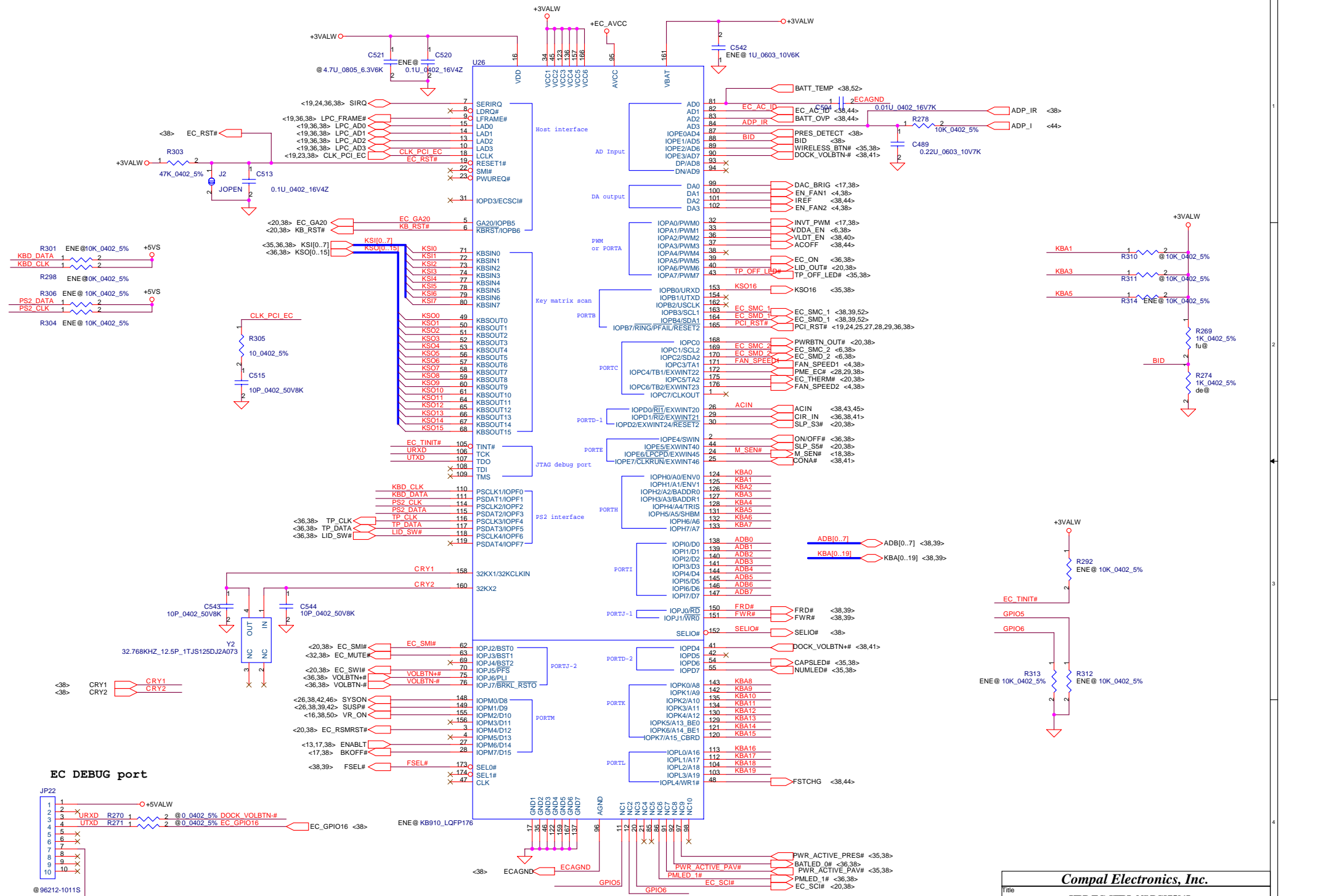


FOR LPC SIO DEBUG PORT



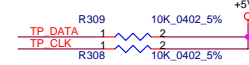
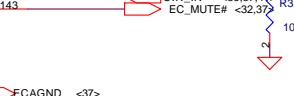
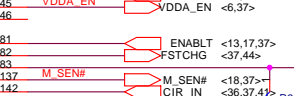
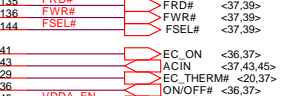
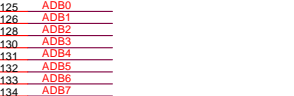
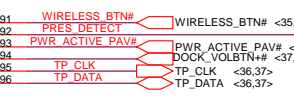
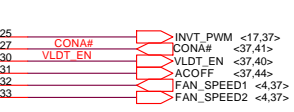
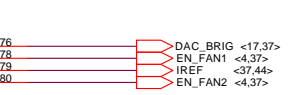
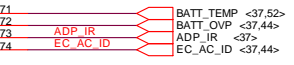
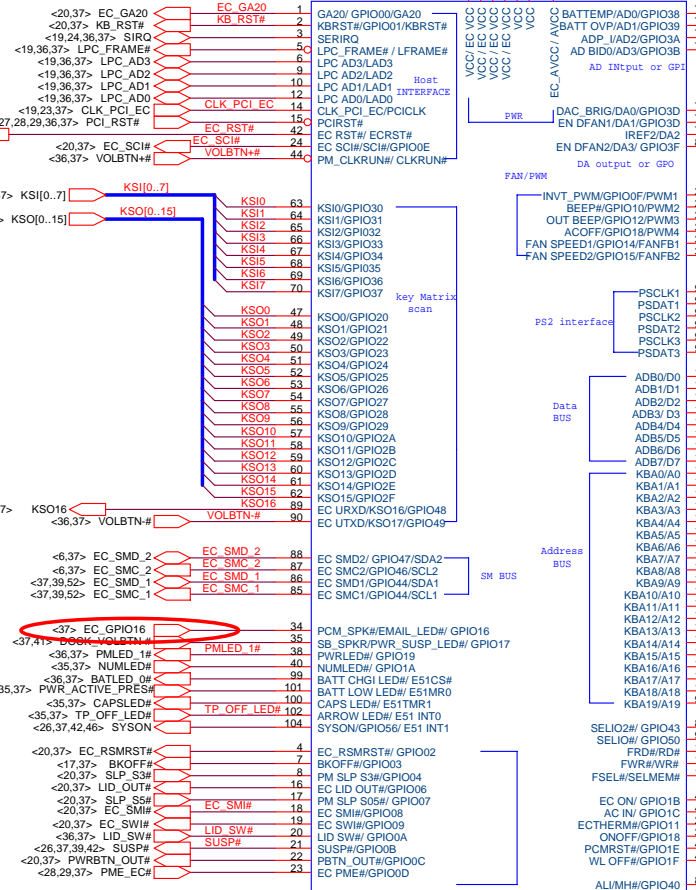
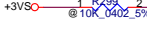
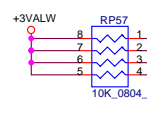
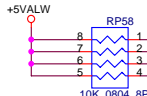
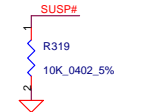
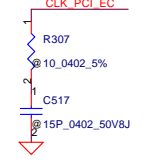
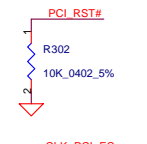
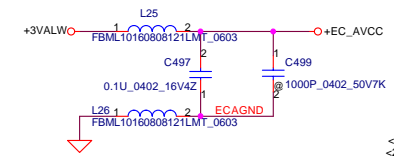
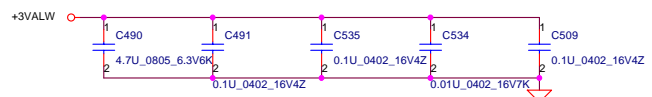
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Compal Electronics, Inc.		
Title KBD,ON/OFF,T/P,LED/B		
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Compal Electronics, Inc.		
KBD EC CTRL-NS-PC87591L		
Title		
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Check ENE

Compal Electronics, Inc.



KBD EC CTRL-KB910L

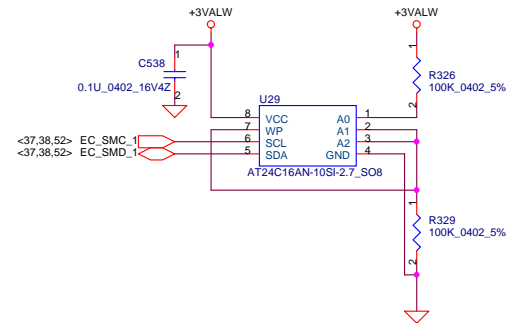
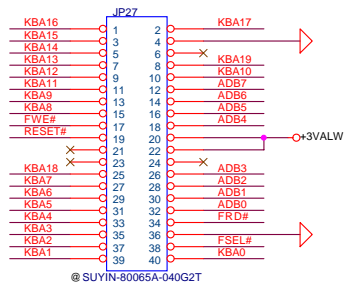
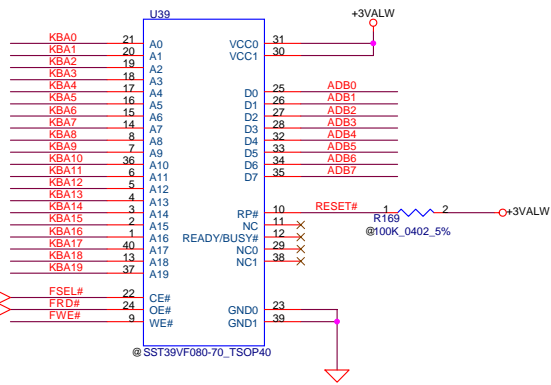
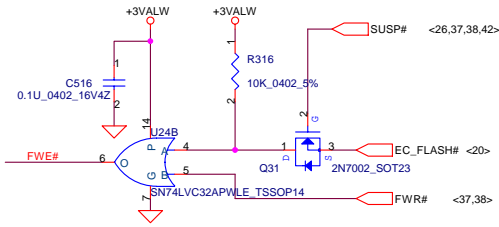
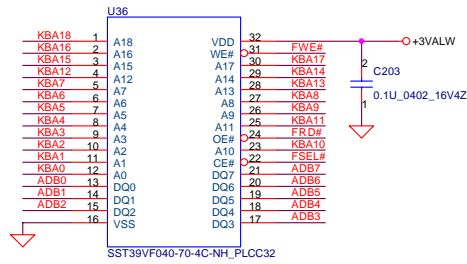
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Size	Document Number	Rev
	LA-2421	0.6

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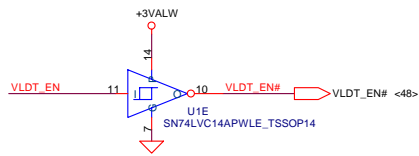
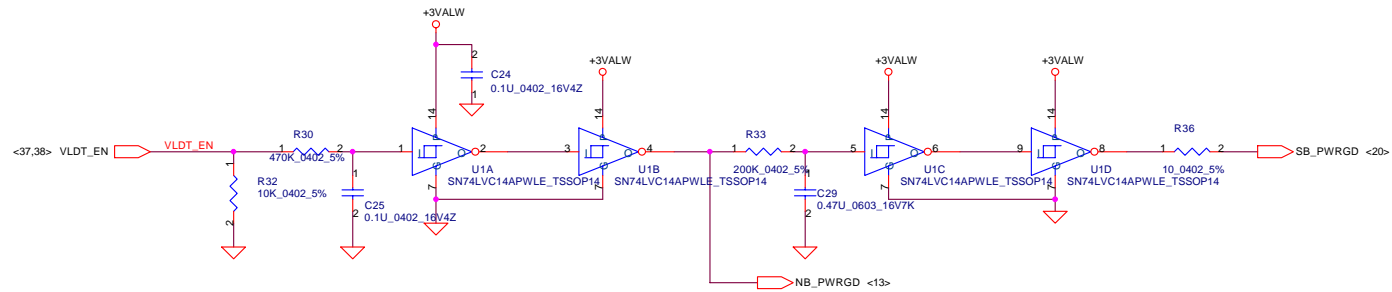
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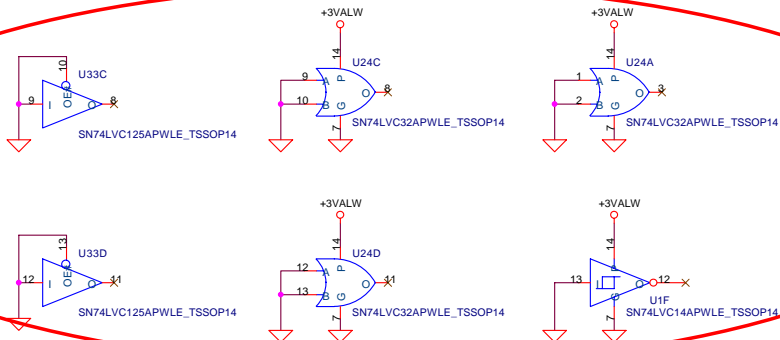
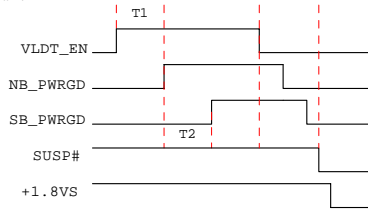
Compal Electronics, Inc.

Title		
BIOS & EC I/O Port		
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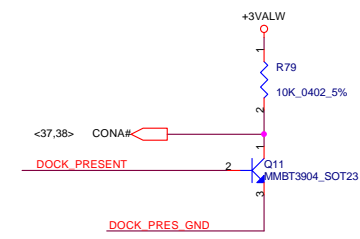
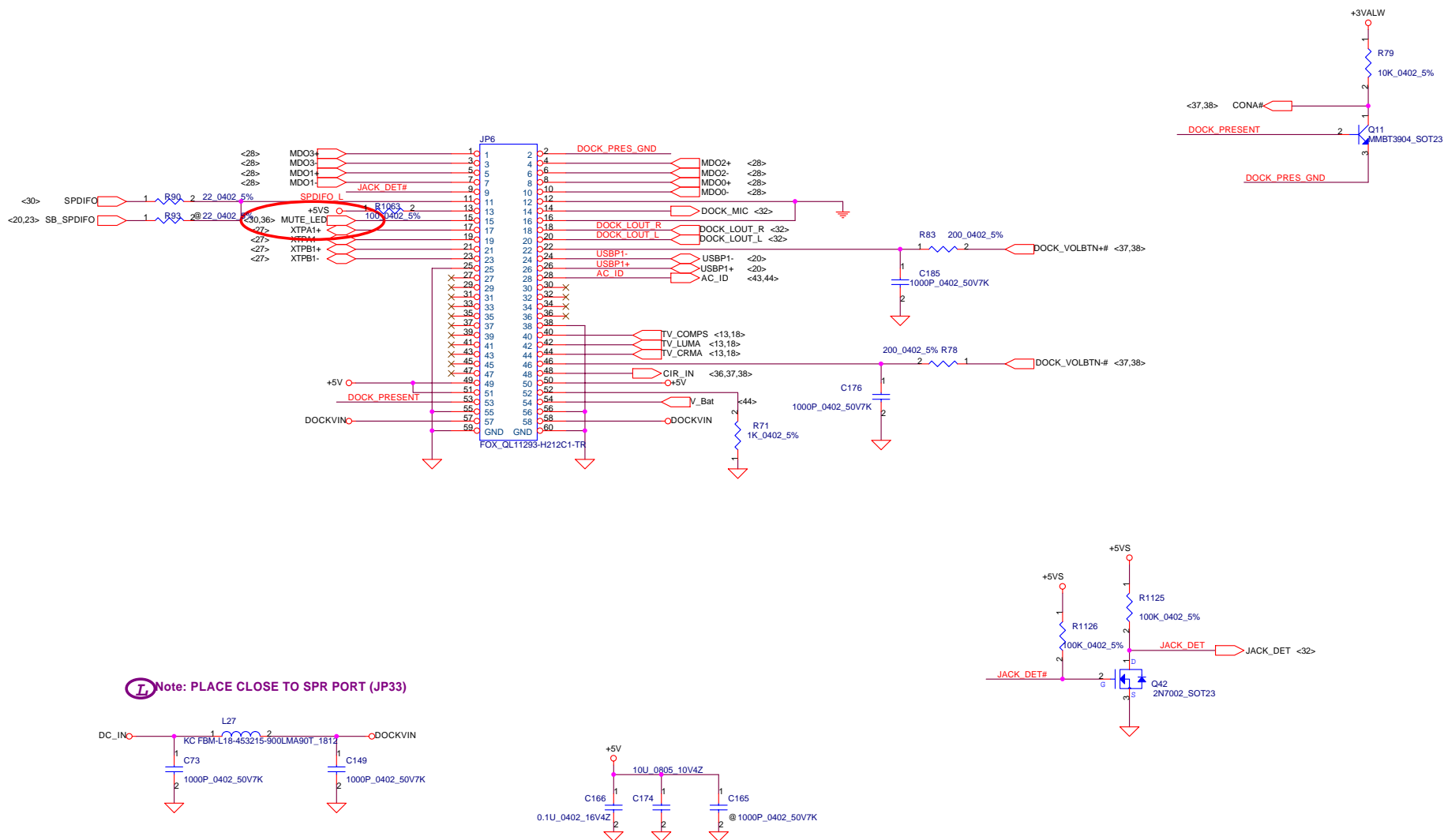


note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.

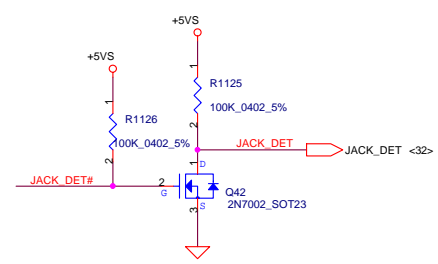
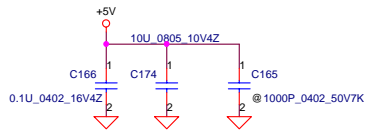
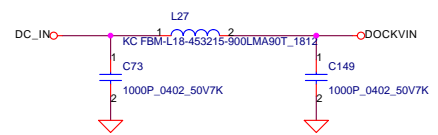


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Compal Electronics, Inc.		
Title Power OK/Reset Conn. & MUTE Switch		
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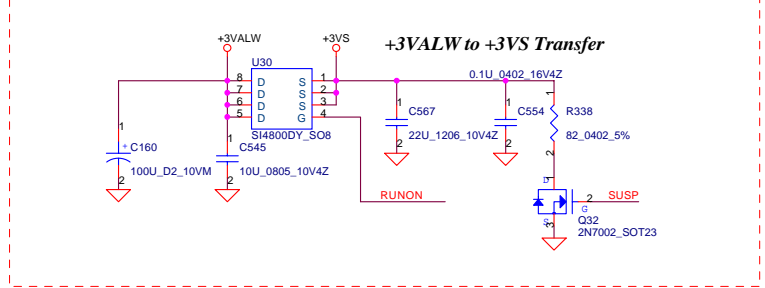
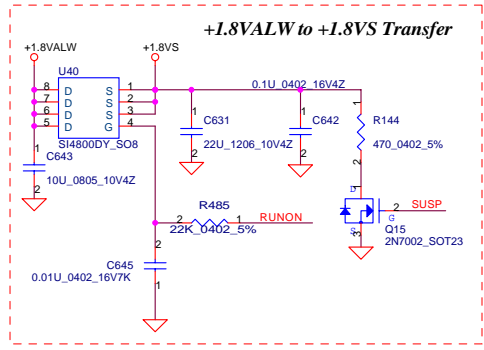
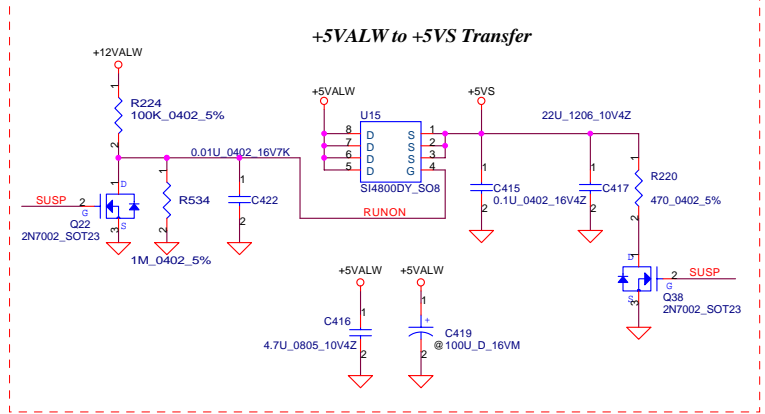
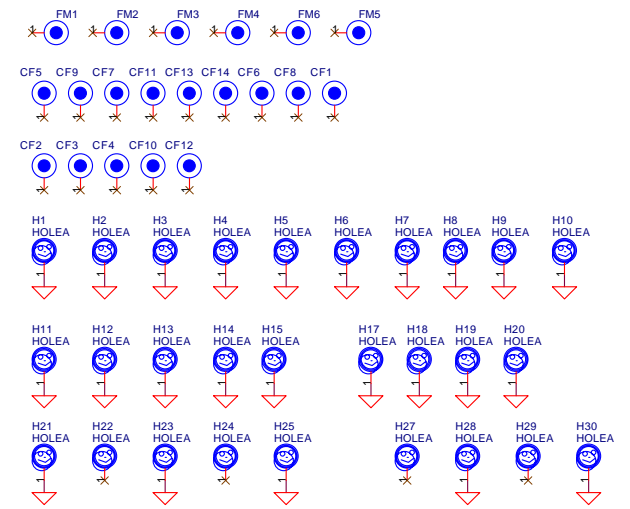
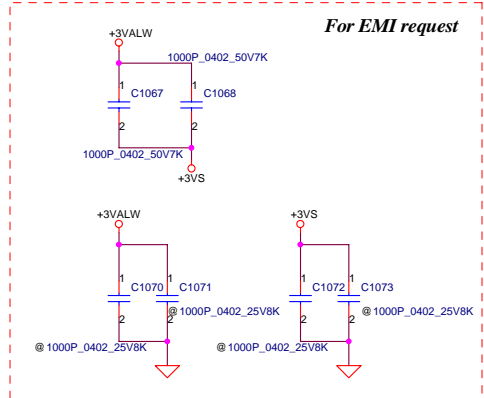
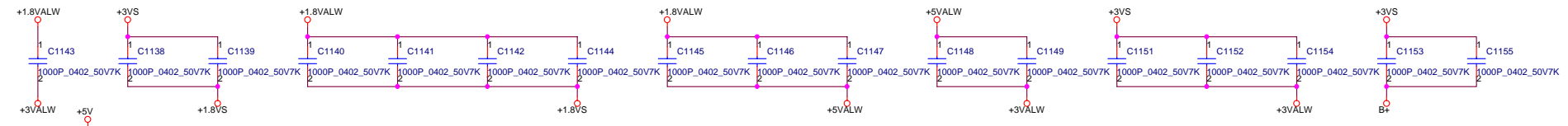
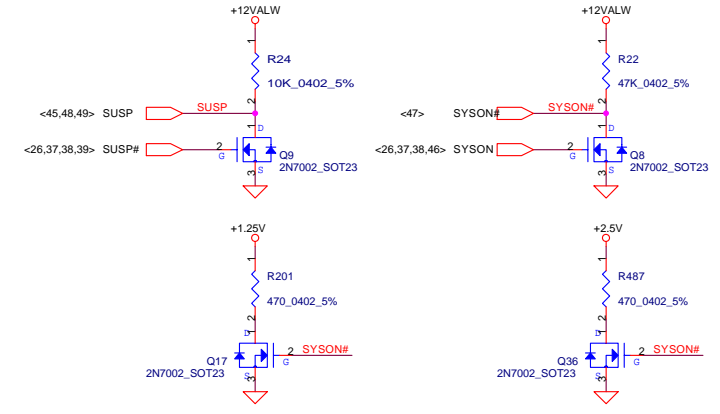
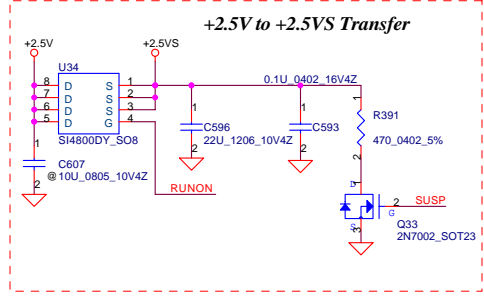
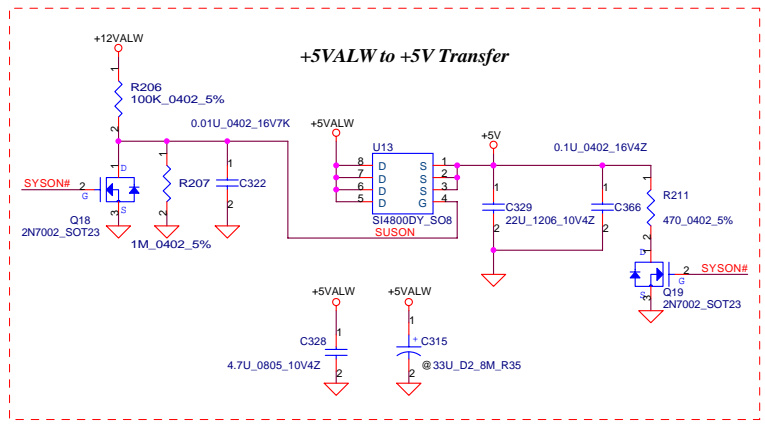


Note: PLACE CLOSE TO SPR PORT (JP33)



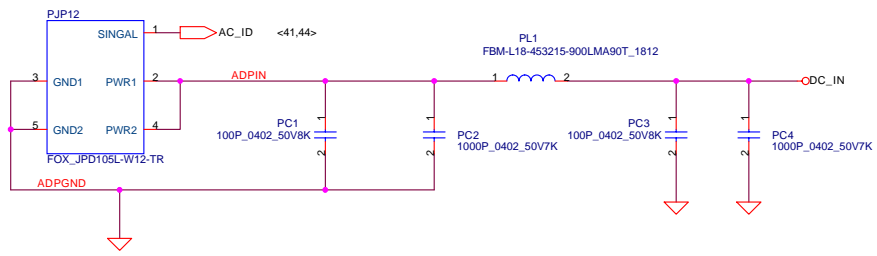
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SPR Connector		
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	LA-2421	0.6
Date:	Wednesday, January 05, 2005	Sheet 41 of 56

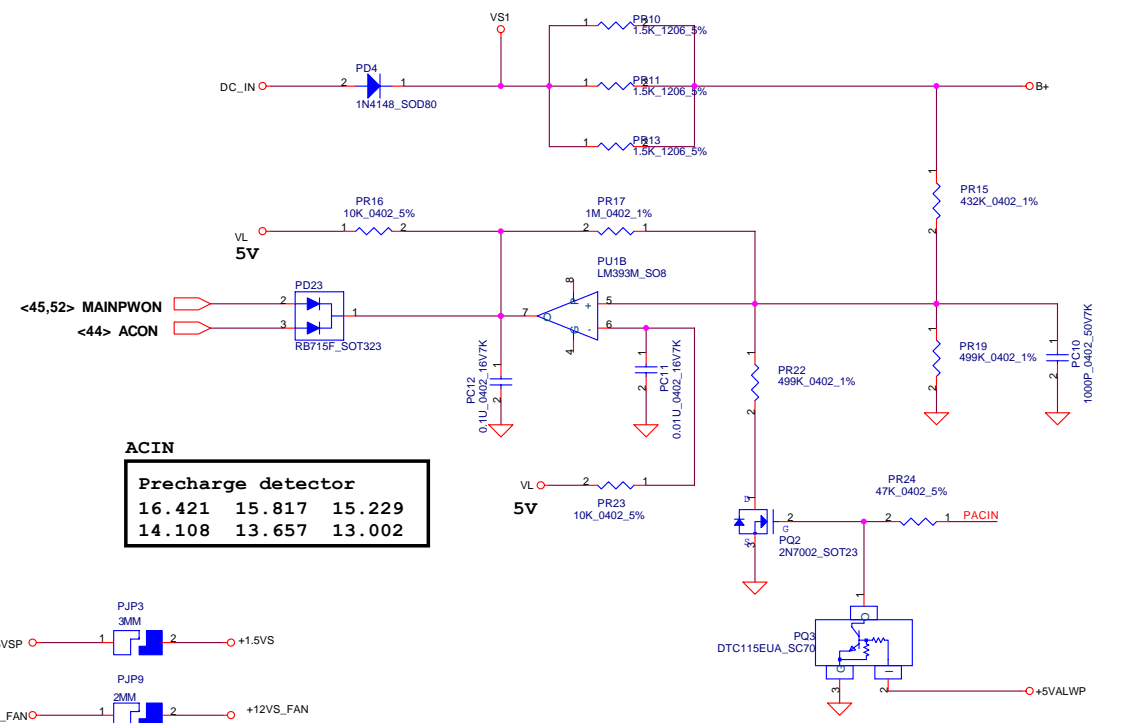
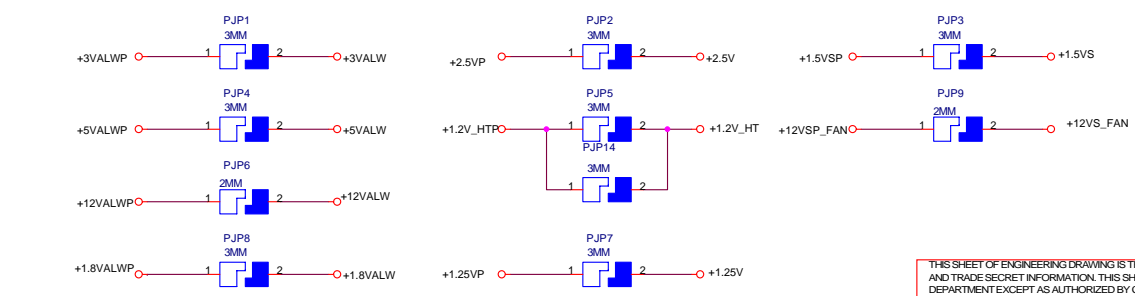
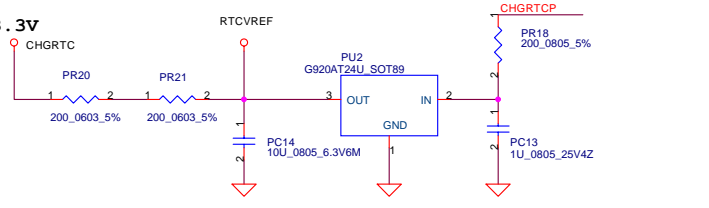
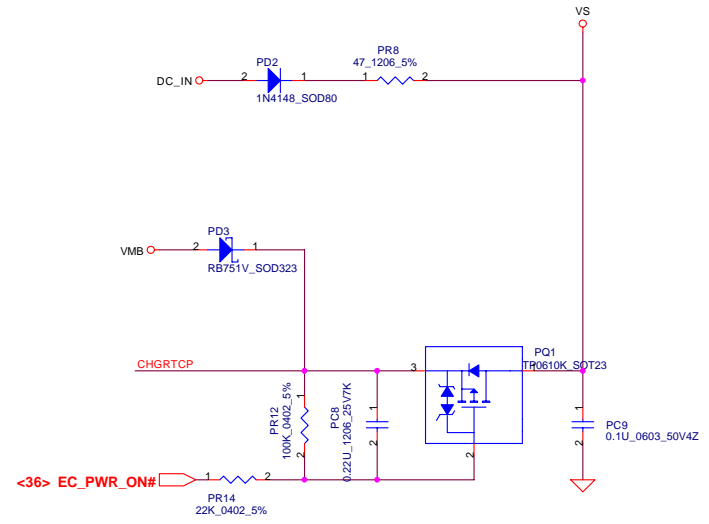
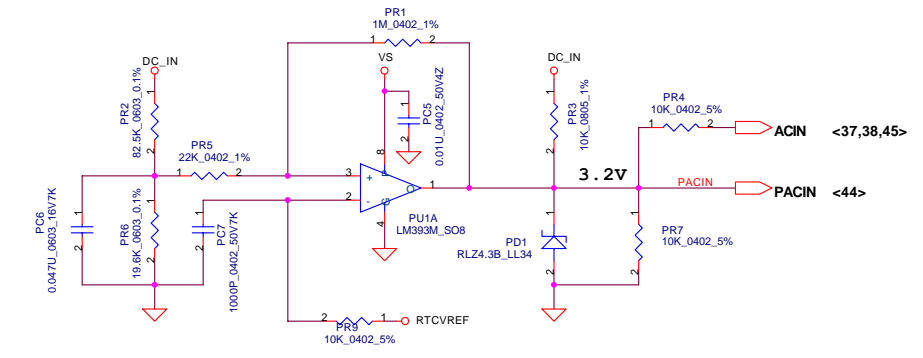


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Compal Electronics, Inc.		
File	DC/DC Circuit	
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Custom	LA-2421	0.6
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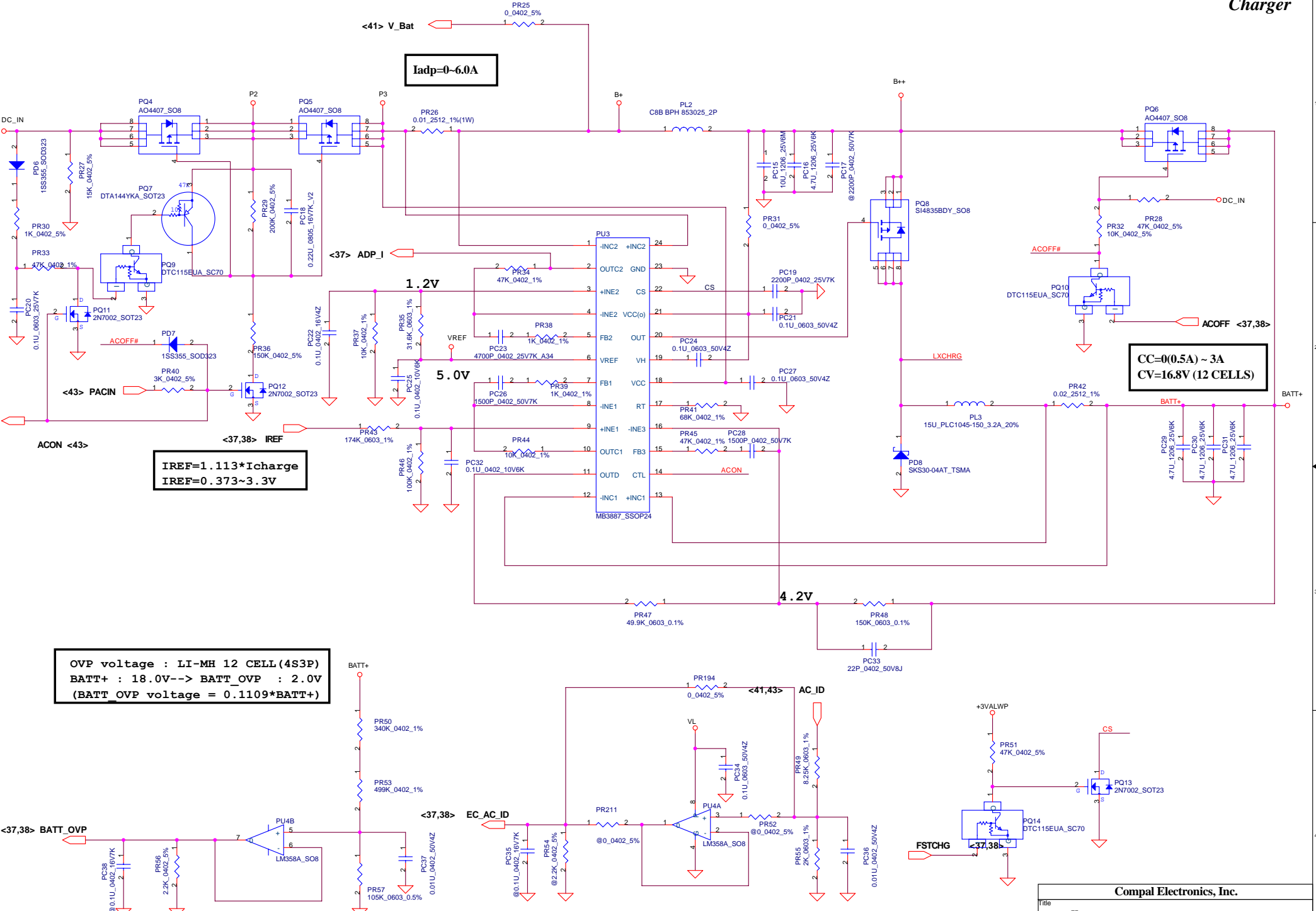
Vin Detector		
18.202	17.841	17.481
17.568	17.210	16.858



ACIN		
16.421	15.817	15.229
14.108	13.657	13.002

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Compal Electronics, Inc.		
File		
Detector		
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I_{adp}=0-6.0A

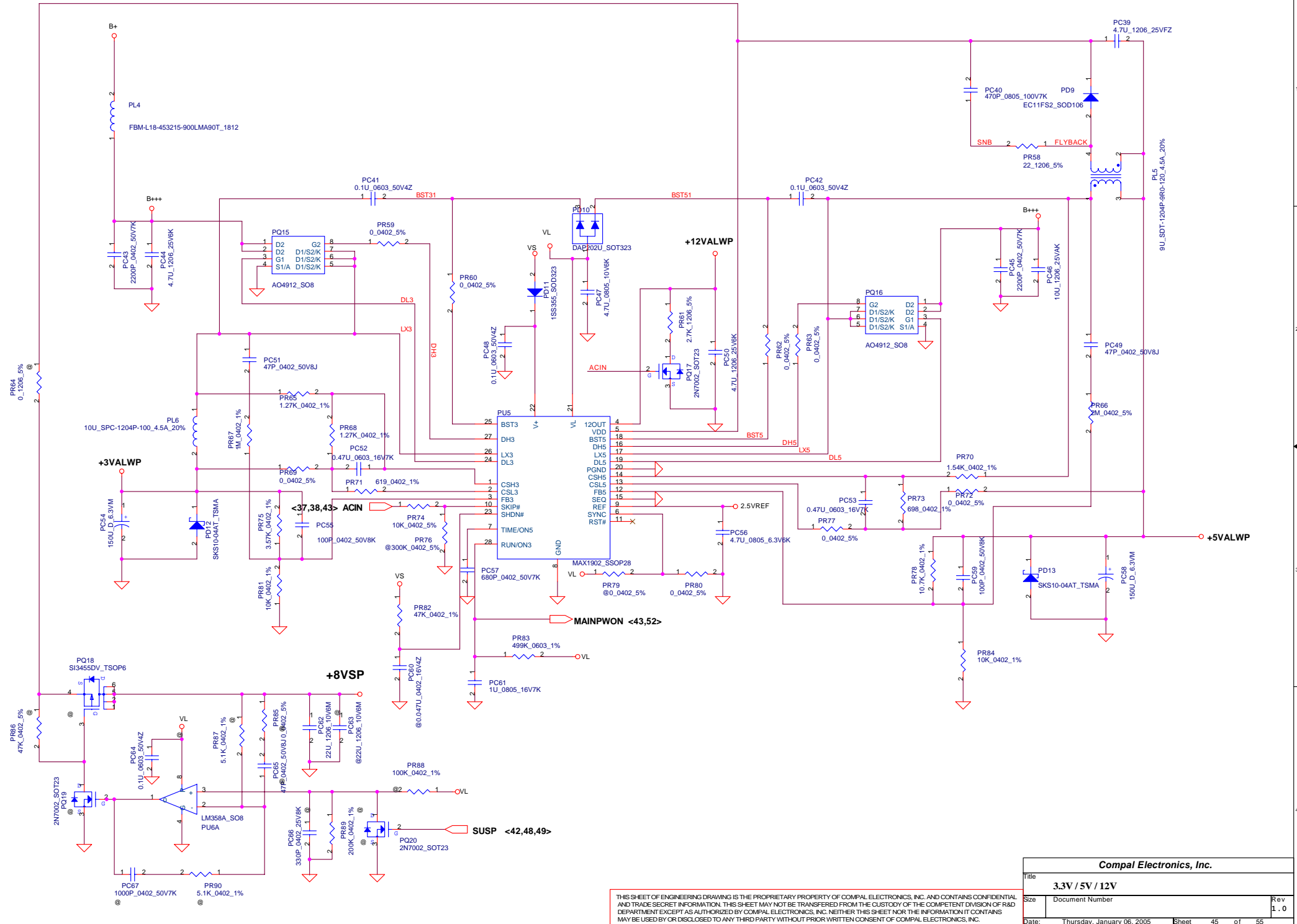
CC=0(0.5A) ~ 3A
CV=16.8V (12 CELLS)

I_{REF}=1.113*I_{charge}
I_{REF}=0.373~3.3V

OVP voltage : LI-MH 12 CELL(4S3P)
BATT+ : 18.0V--> BATT_OVP : 2.0V
(BATT_OVP voltage = 0.1109*BATT+)

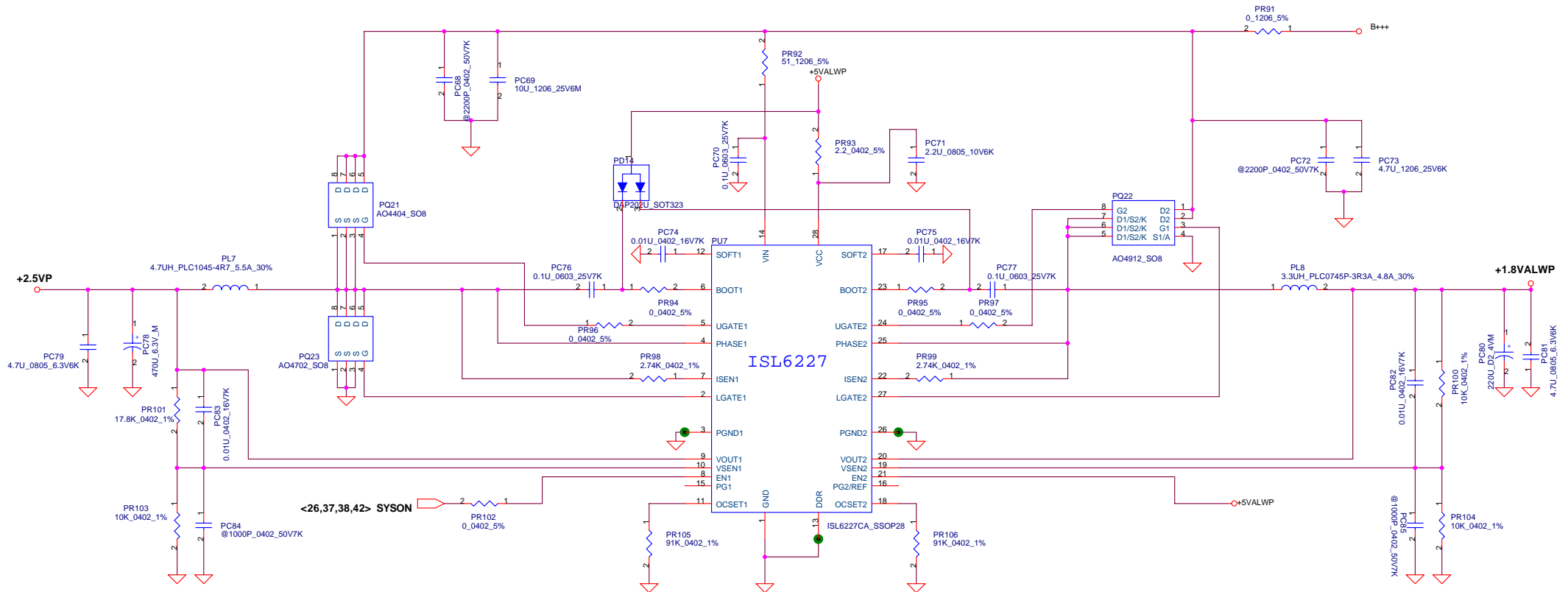
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Compal Electronics, Inc.		
Title Charger		
Size	Document Number	Rev
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Compal Electronics, Inc.		
Title 3.3V / 5V / 12V		
Size	Document Number	Rev
Date:	Thursday, January 06, 2005	Sheet 45 of 55

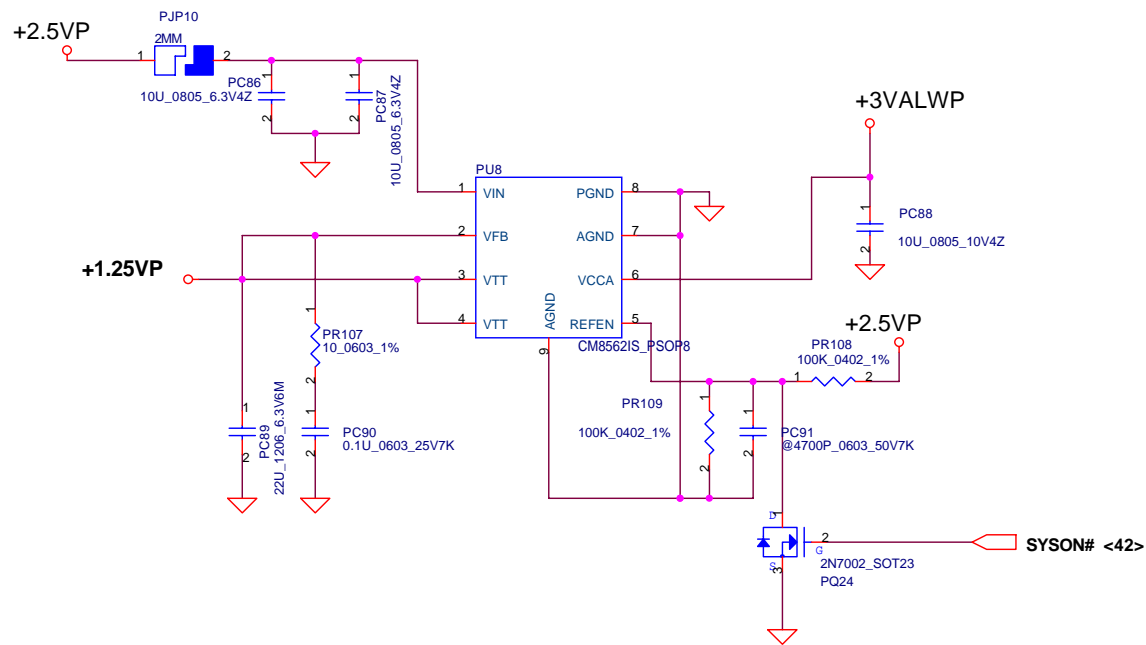


$I_{limit} = 10.3 / R_{ILIM} * (140 + R_{sense}) / R_{ds(on)}$
 $R_{sense} = 1K, R_{ILIM} = 51K, R_{ds(on)} tpy. = 19.7m\Omega, Max = 24m\Omega.$
 $I_{limit\ Min} = 9.6 / 51K * (100 + 1K) / (24m\Omega * 1.3) = 6.636A$
 $I_{limit\ Max} = 9.6 / 51K * (100 + 1K) / 19.7m\Omega = 10.897A$
 $+VCCP\ O.C.P. = 6.636A \sim 10.897A$

$I_{limit} = 9.6 / R_{ILIM} * (100 + R_{sense}) / R_{ds(on)}$
 $R_{sense} = 2K, R_{ILIM} = 107K, R_{ds(on)} tpy. = 19.7m\Omega, Max = 24m\Omega.$
 $I_{limit\ Min} = 9.6 / 107K * (100 + 2K) / (24m\Omega * 1.3) = 6.0388A$
 $I_{limit\ Max} = 9.6 / 107K * (100 + 2K) / 19.7m\Omega = 9.564A$
 $+VCCP\ O.C.P. = 6.038A \sim 9.564A$

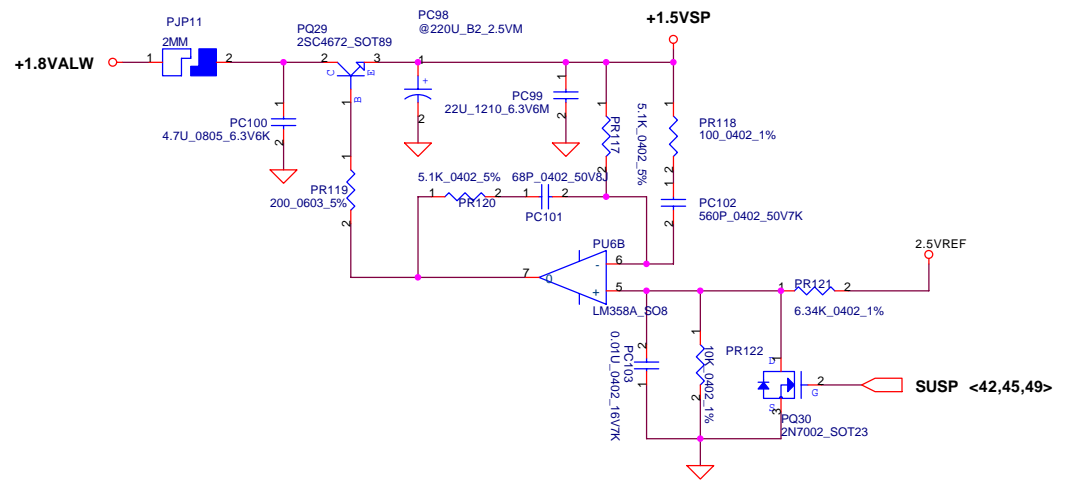
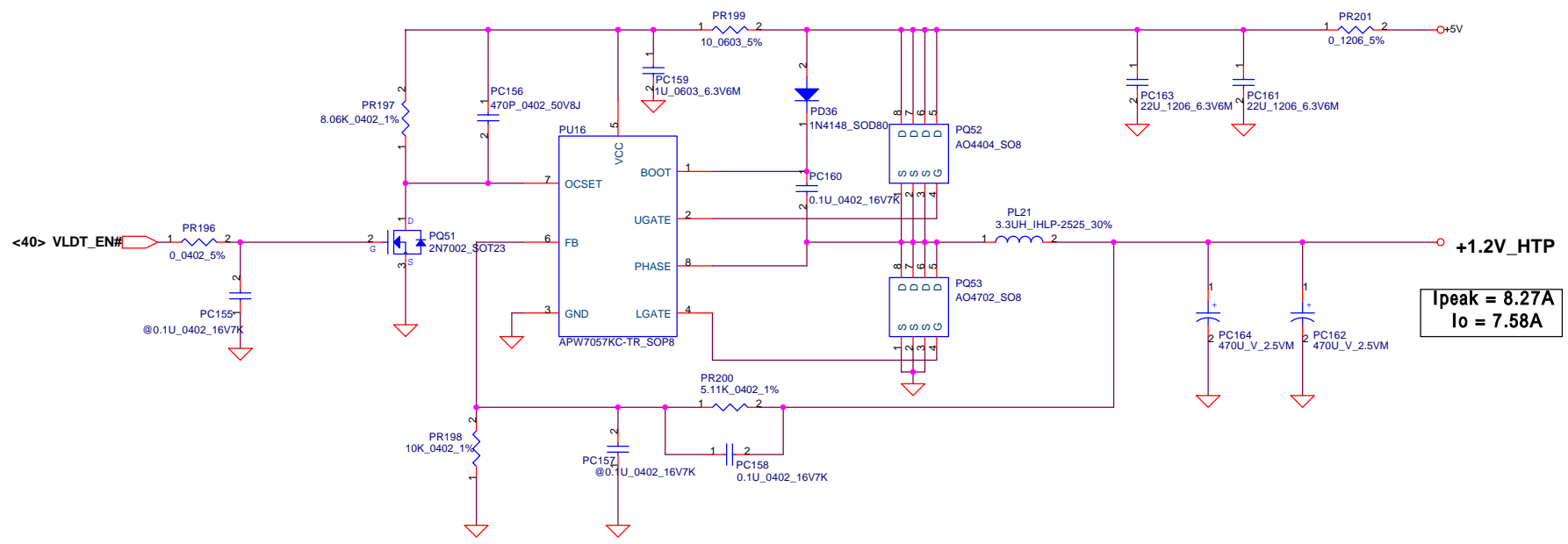
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COMPAL ELECTRONICS, INC		
Title DDR POWER 2.5VP & +1.8VALWP		
Size B	Document Number	Rev 0.1
Date: Wednesday, January 05, 2005	Sheet 46 of 55	



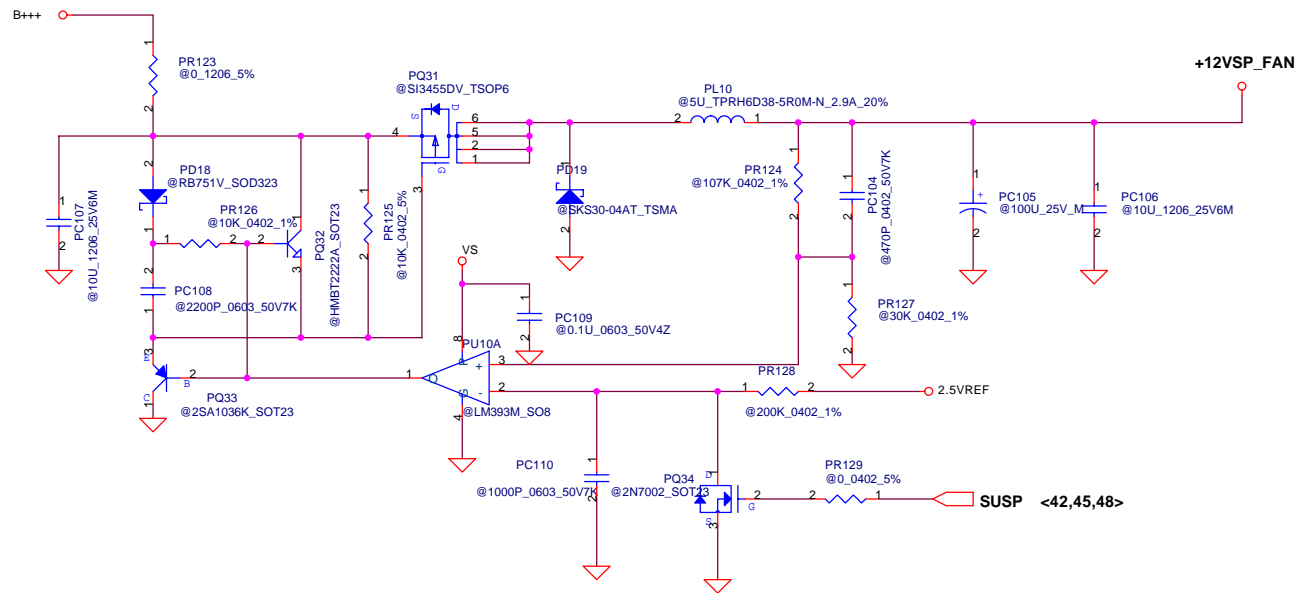
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COMPAL ELECTRONICS, INC		
Title +1.25VP		
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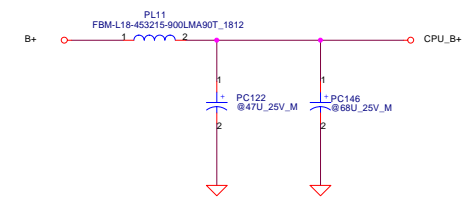
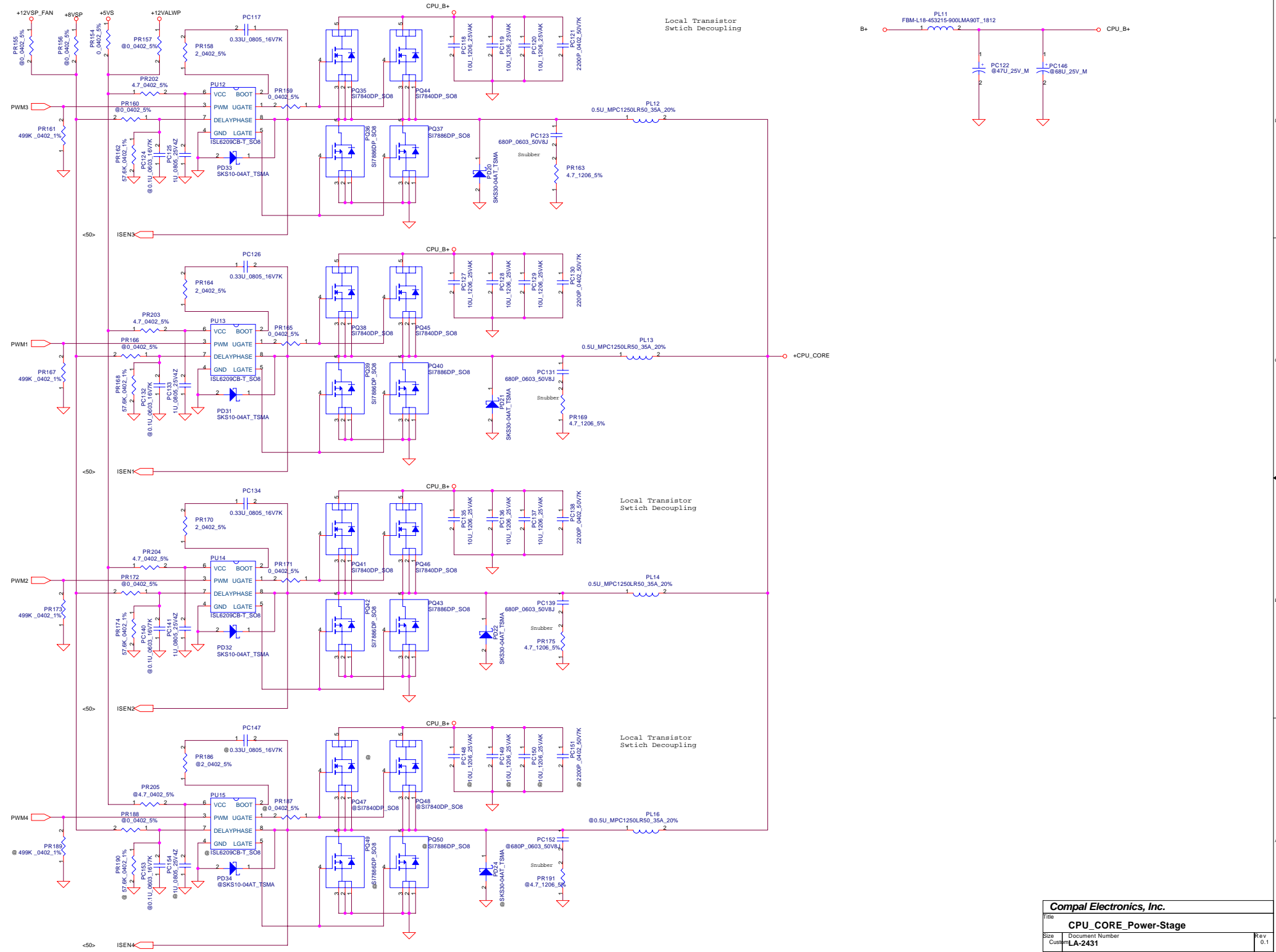
COMPAL ELECTRONICS, INC		
Title 1.2V_HTP / +1.5VSP		
Size	Document Number	Rev
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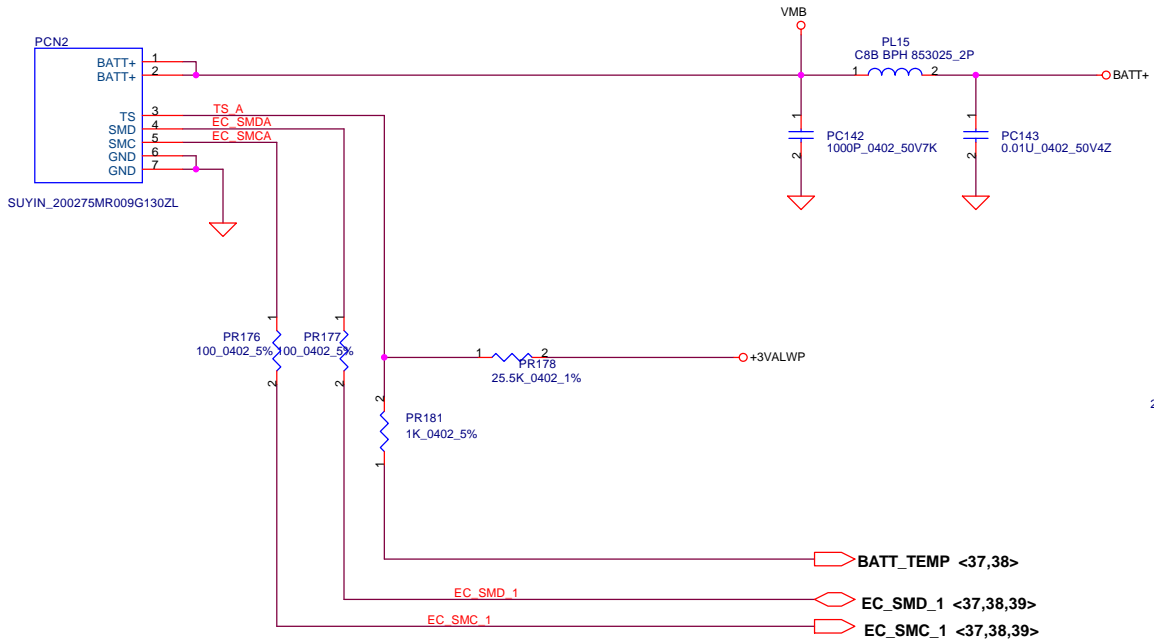
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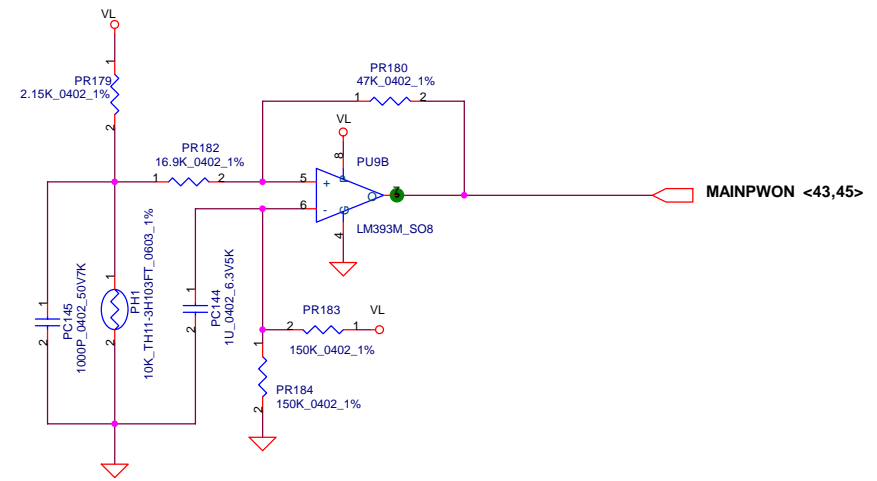
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COMPAL ELECTRONICS, INC		
FAN 12V		
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PH2 near main Battery CONN :
 BAT. thermal protection at 84 degree C
 Recovery at 45 degree C



SUYIN_200275MR009G130ZL

BATT_TEMP <37,38>
 EC_SMD_1 <37,38,39>
 EC_SMC_1 <37,38,39>

COMPAL ELECTRONICS, INC		
Title		
BATTERY CONN / OTP		
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POWER PIR LIST

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PIR			
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PIR LIST

Pre-DB

2004/6/05

- 1.page16 add R541/R542/R543/R544 and net NBSRCCLK_R/ NBSRCCLK/ NBSRCCLK#_R/ NBSRCCLK#.
- 2.page13 add net NBSRCCLK/NBSRCCLK#.
- 3.page13 change R85 pin2 from +2.5VS to +2.5V.
- 4.page14 add D33.
- 5.page19 del D18 and remove C265 to U38 pinA2.

2004/6/08

- 1.page13 del R82 change net name from SUS_STAT# to NB_SUSSTAT#.

2004/6/19

- 1.page19 Change U32,C584,R389 to @.
- 2.page23 Change R460 to @ and Add R464.

2004/6/25

- 1.page40 Change R30 from 10K_0402 to 340K_0402_1%.
- 2.Page4/6 change C18, C28 to SF10001M100 ELE CAP 100U 6.3V M B (6.3X6.0) CV-AX.
- 3.Page19 Add JP37, del BATT1

2004/6/28

- 1.Page26 Change U2 from R5535 to TPS2231.
- 2.Page26 Change C485/C487 to 4.8U_0805,change C486 to 10U_0805.
- 3.Page26 Change C503/C494 to 10U_0805,C492 to 4.7U_0805.
- 4.Page26 Del R268,Add Q40 2N7002.

Update for DB2

- 1.page34 change IDE Resistor from 0402 to 8P4R.
- 4.page27 change DOCK@ to 1394@.
- 5.ME update connector check and sub-board connector change to hot bar.
- 6.change 470U placement for +1.25V.
- 7.page40 change R33 from 0603 to 0402 type and R30 to 470k_0402_5%.
8. change C18, C28 to SF10001M100 ELE CAP 100U 6.3V M B (6.3X6.0) CV-AX.
9. change C318 to bottom side SF33001M100 ELE CAP 330U 6.3V M B (6.3X7.7) CV-AX
10. change C411 to bottom side SF47001M000 ELE CAP 470U 6.3V M B (10X10.5) CV-EX
11. change C325 to SGA19471D20.
13. change BATT1 to SP07S00080L(socket) + GC20323MX00(battery) (Page 19)
14. change new card power switch from RICOH to TI.
15. Remove PME_EC# from SB and pin C4 wire to EC_SWI#
16. Disconnect UTXD from U26.154
17. Page 23 update hardware strap for SB400 A21 (PA_IXP400AD1 & 105-A27800-00C R1.1)
18. Page 13 add EEPROM for NB to solve boot up intermittently
19. Page 23 strap select 14 MHz OSC mode, it is generated from NB to SB and delete 14 MHz crystal at SB
20. 1394 controller change to TI
21. Update PIRQ routing
22. X2 change size.
23. Cardbus controller change to TI
24. Fan circuit change to MOS
25. Change AMP to TPA0312 and add TC7SH32FU to solve HP_PLUG issue
26. Implement HP wireless/bluetooth control requirement. Change host to SB. (Page 20)
27. Change CRT connector JP19 (Page18)
28. Modify KB910L debug pin RXD=pin#35 & TXD=pin#34
29. No need PWR_BACK# from EC controller
30. DFX review: Change blue LED footprint to be same as amber LED footprint.
31. AC97 primary codec SDATA_IN0 should connect to SB's AC97_SDIN0 (Page 30)
32. R182 change to 11.8 k (Page 20)
33. Reserve D36, D37, and R1127 for XD detect issue. (Page24)
34. PCIE_PME# change to pin #D2 of SB. (Page 20)

35. WL_ON connect to pin #C5 of SB/ BT_ON# connect to pin #B5/ BT_DET# connect to pin #C8. (Page 20)
36. Add R1132 to ensure ENABL is low during power up.(Page 13)
37. AGP_BUSY# and AGP_STP# pull up to solve shut down issue. (Page 20)
38. Delete R159 (OVCUR#3) and LID_OUT# change to GPM3# and add R1133 pull up S3_STATE to +3VALW (Page20)
39. Change all blue LED's footprint to LED_17-21UYOC-S530-A2-TR8_2P
40. Change R532 to 0603 size and add R1134 (Page 30)
41. Add AC-caps for PCI and LPC bus turn path. (Page 42)
42. Delete R541, R542, R543 and R544. (Page 16)

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Title		
LAN RealTech8100BL		
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Update for SI

1. Applying CLK_STOP of ICS951418. (Page 16)
2. R176 change to 4.12k 1% (page 19)
3. Add pull down resistor for SYSON (R1135) and SUSP# (R319), due to TPS2231 internal pull-up when +3VALW present, EC can not control at the first 10 ms.
4. Reverse JP33 and JP34
5. TI CardReader workaround: add Q44, R1137, D38, and D39 to prevent signal output earlier than power up (page 24)
7. MU902's pin29 connect to AGND_LSD (page 31)
9. Change C621, C619, C628, and C625 to 0.01U from 0.1U (page 19)
10. DDR change to single channel from dual channel.
11. Swap pin40 and 44 of docking connector (JP6) for TV-out signal. (page 41)
12. Update from ATi AP note of SB, unused SATA pins connect to GND. (page21).
13. Reserve R1138 for XD_WP# pin at socket side. (page 24)
14. Reserve U47 to generate independent +1.9VS to PCIE_PVDD and PCIE_VDDR. (page 19)
15. For KB910L, pin #94 is for DOCK_VOLBTN+# and pin #34 is for EC_GPIO16. (page 38)
16. Add R1141 on SUS_STAT# per ATI recommend. (page 13)
17. PR110 connect to +5V due to +3VS too dirty that will cause TV display garbage. (page 48)
18. Update PCIE connector (JP5) pin defined of #7, #8, and #9 and reserve backward compatible due to there are two different version of NewCard spec. (page 26)
19. GPP_RX0N/P connect to JP5.21/22 and PCIE_TX0N/P connect to JP5.24/25 (page 26)
20. Reserve D40 and D41 for NewCard hot-plug detected. (page 26)
21. Adjust AMP output to 10 dB: Add R237/R233, delete R236/R234. (page 32)
22. Change CP1 ~ CP6 to C1156 ~ C1179 due to cost saving. (page 36)
23. Add C1180 and C1181 for EMI requirement. (page 42)
24. Add C160 due to +3VS unstable. (page 42)
25. R1121 change to 0_0402_5% per TI recommend (page 24)

Update for SI-R (Rev 0.4)

1. DDR_SDM_L2 length mismatch (page 9)
2. Add U48 (TPS2211A) for PCI1510RGVF (page 25)
3. NC_CP# connects to U38.D3 for New Card hot-plug (page 20)
4. R51 and R77 change from 49.9_0402_1% to 61.9_0402_1% (page 11)
5. Change C621, C619, C628, and C625 to 0.1U from 0.01U --- ATI final decision for SB A22 RPO3 and future (page 19)
6. Q25 change from MMBT3906 to PDTA114EK and R228 change to 0_0402_5% due to Hitach HDD LED will not be turn off light. (page 36)

Update for SI-2 (Rev 0.4B)

1. Remove C27 due to Sempron CPU intermittent boot-up issue. (page 6)
2. Change Q39 to MMBT3904 due to CARD_LED is high active signal. (page 35)
3. D40 and D41 replace by R1146 and R1148 due to TPS2231 truth table treat both CPUUSB# andCPPE# as the same. (page 26)
4. R87 change to 8.06k_1% due to New Card eye-diagram issue. (page 12)

Update for PV (Rev 0.5)

1. Add R1149 and R1150 for headphone gain degrading. (page 32)
2. Modify AVDDTX and AVDDR layout to improve USB signal quality.
3. Change wireless LED power from +5V to +5VS (page 35)
4. Follow TI layout guideline.
5. Change R1099 and R1100 to 2.2k per TI recommend for XD certification. (page 24)
6. Change LAN LED indicator color, Green is for link and Amber is for activity. (page 28)
7. Change R34, R35 and R259 from 1k to 680 base on AMD design guide. (page 6)
8. Change R286, R290, R473, and R486 from 100 to 15 base on AMD recommendation. (page 5/ 9)
9. Reserve C1182 at NB VDD_CORE and change C161 ~ C164, C136 ~C138, C153, C154, C156, C157 from 0.1uF to 1uF due to +1.2V_HT is not stable and clean. (page 14)
10. Delete R1083 due to SM card detect issue (quick or slow). (page 24)
11. Add C1183 ~ C1220, 1000pF or 220pF, on +2.5V, +1.25V, +CPU_CORE, +3V_CLK, +3VS, and +1.2V_HT for EMI require. (page 7/ 10/ 14/ 16/ 22)
12. Change R155, R162, R441, R444, and R448 from 22 ohm to 33 ohm due to EMI require. (page 19)
13. Wire MUTE_LED to JP6.15 due to HP docking spec V0.8 update (page 41)
14. Add C1151 and C1152 to isolate GND and change C61 and C241 from 0.1uF to 1000pF for EMI. (page 4)
15. Add C1221 ~ C1226 on +2.5VS for EMI (page 15)
16. Reserve C1227 and C1228 on EDID_CLK/DAT for EMI. (page 17)
17. Remove R64, R65, R69, and R70 due to EMI. (page 5)
18. RTC battery change to CR2025 (165mAh) due to power consumption less than 5uA. (page 19)

Title			
<Title>			
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Update for PV-2 (Rev 0.6)

1. Delect R1138, wire WP# pins of XD and SM together (SM_EL_WP#) and series 3.3k ohm (R1082) to CLK per HP recommendation. (page 24)
2. Tie un-used inputs of U24 and U33 to GND. (page 40)
3. Delect all reserve 0 ohm resistors. (page 34)
4. Add C1229 for power (+CODEC_REF) stable on MIC_IN. (page 30)
5. R53 change to 91_0402_5% due to HT output from RS480 need to improve rising and falling time. (page 11)
6. Reserve R1153 ~ R1157 for SanDisk 256MB SD card overshoot and undershoot issue. (page 24)
7. De-feature mother board populate R274, and full-feature mother board populate R269 for 90W adapter protection. (page 37)

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