

Compal confidential

Schematics Document

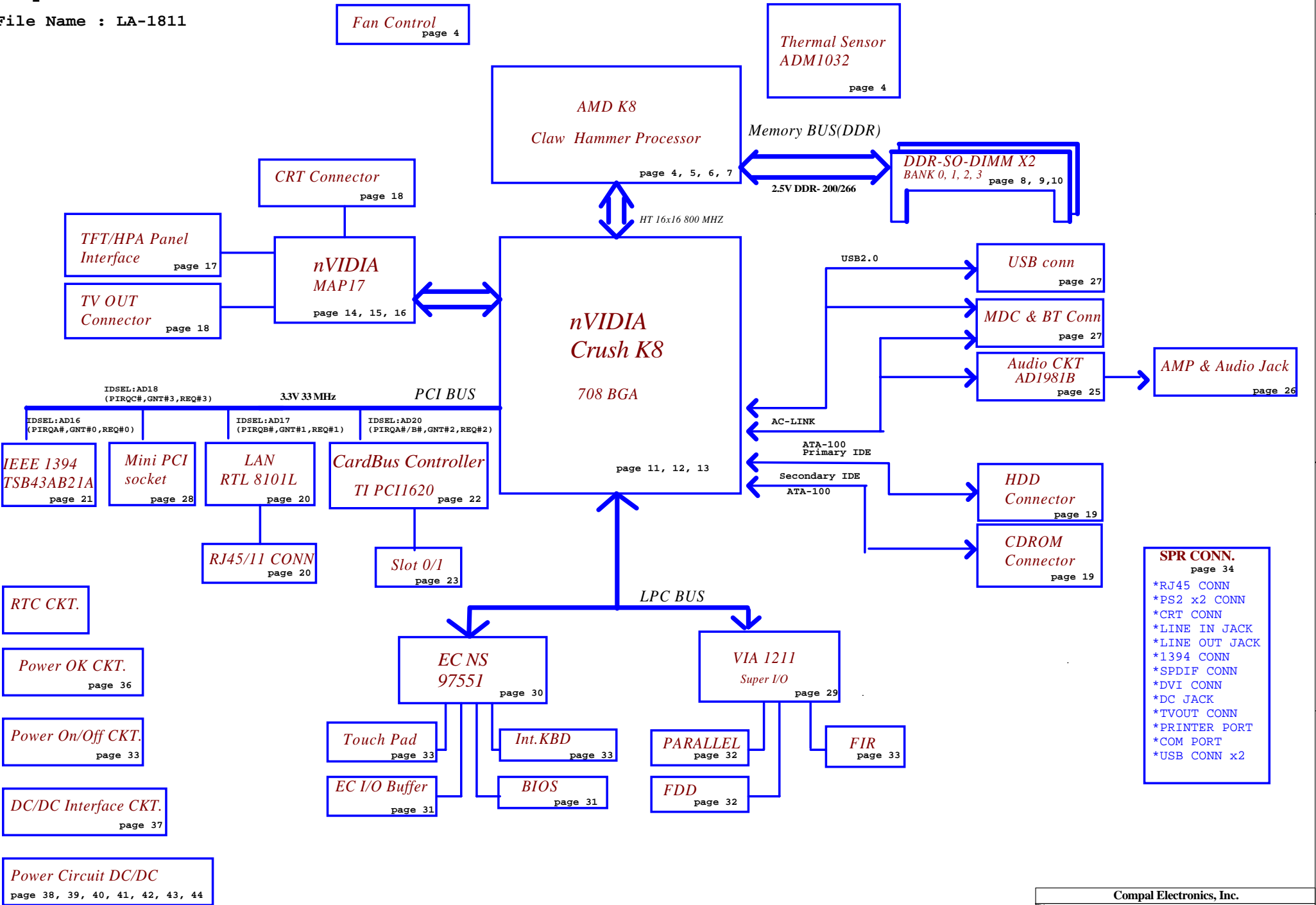
ClawHammer AMD K8 with nVIDIA Chrush K8

2004-04-16

REV: 0.1

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Compal Electronics, Inc.		
Title		
Cover Sheet		
Size	Document Number	Rev
	LA-2392	0.1
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Compal Electronics, Inc.		
Title Block Diagram		
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Voltage Rails

power plane State	+1.2VALW +3VALW +5VALW 12VALW	+1.25V +2.5V +3V +5V	+1.2V_HT +1.2VS +1.5VS +2.5VS +3VS +5VS
S0	○	○	○
S1	○	○	○
S3	○	○	✗
S5 S4/AC	○	✗	✗
S5 S4/AC don't exist	✗	✗	✗

○ MEANS ON

✗ MEANS OFF

PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
--------	---------------	---------	-----------	------

INTERNAL

USB 2.0	2	AD13	N/A	G
AC97 MODEM	6	AD17	N/A	M
AC97	6	AD17	N/A	L
ATA 100	8	AD20	N/A	
ETHERNET	5	AD16	N/A	K
LPC I/F	1	AD12	N/A	
SMBUS	1	AD12	N/A	F

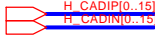
EXTERNAL

VGA	0	AD16	N/A	E
1394	0	AD16	0	A
LAN	1	AD17	1	B
CARD BUS	4	AD20	2	A, B
Wireless LAN	2	AD18	3	C
Mini-PCI (no use)	3	AD19	4	D

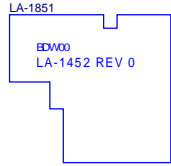
Compal Electronics, Inc.		
Notes List		
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<11> H_CADIP[0..15]
<11> H_CADIN[0..15]



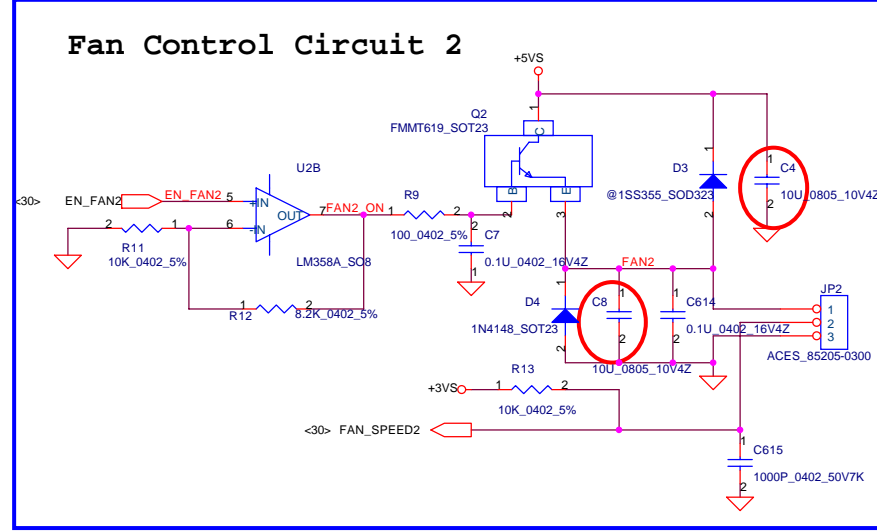
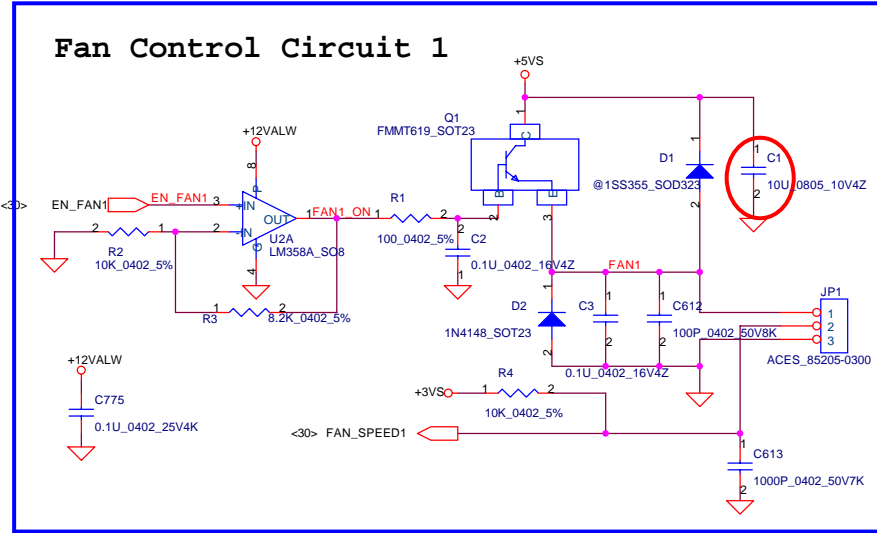
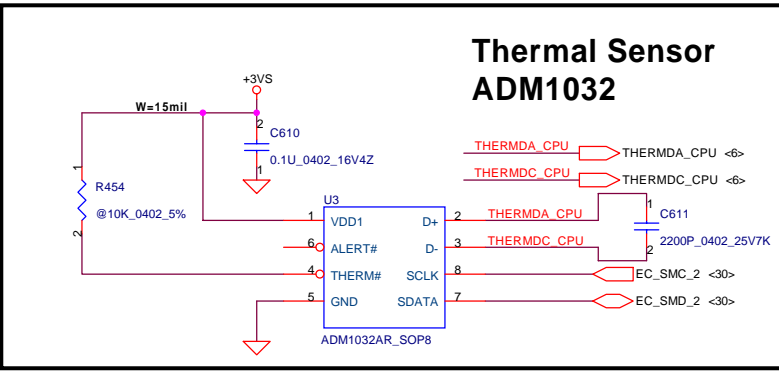
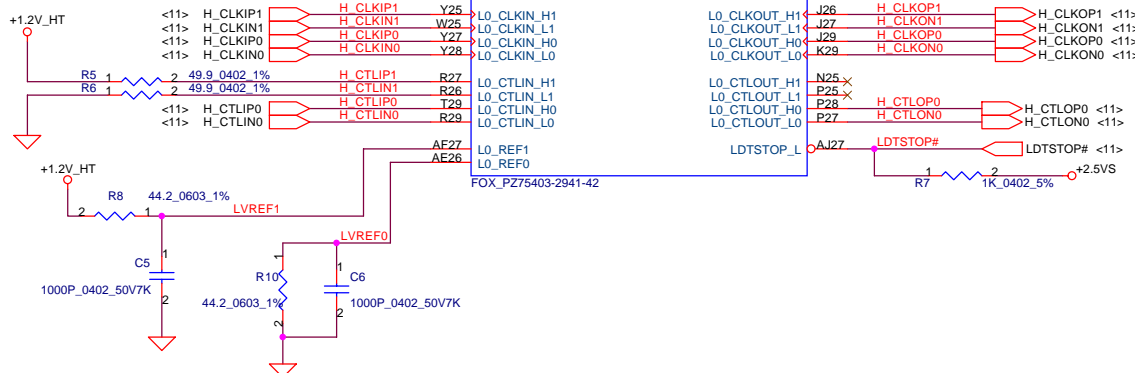
H_CADOP[0..15]
H_CADON[0..15]



U1A

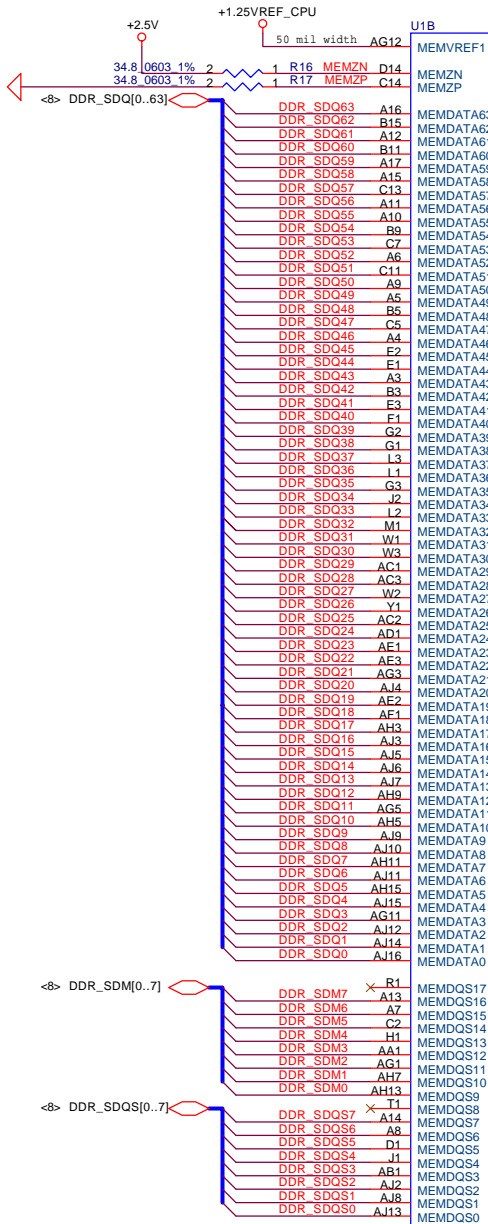
Claw Hammer-DTR

HTT Interface



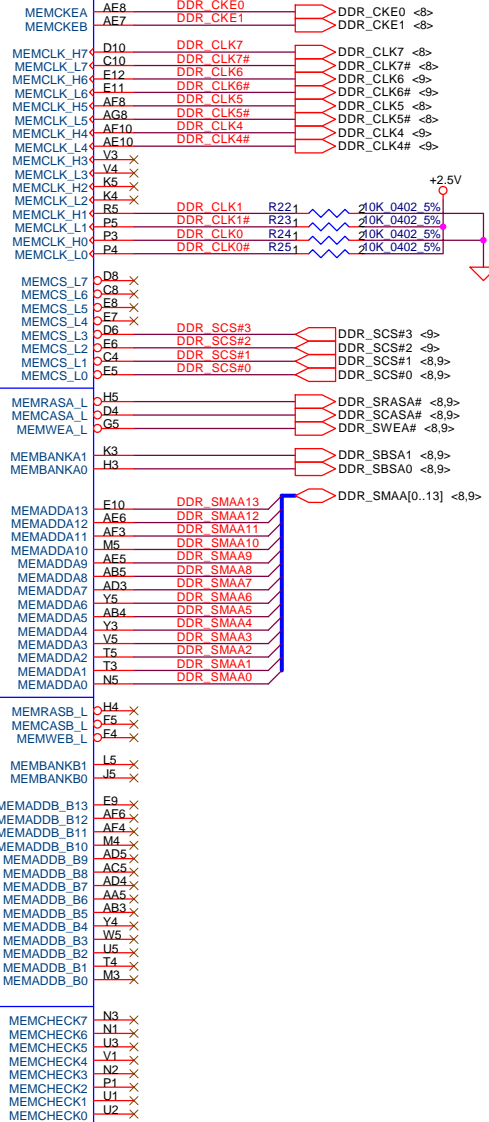
Compal Electronics, Inc.		
Title		
Claw Hammer CPU (Host Bus)		
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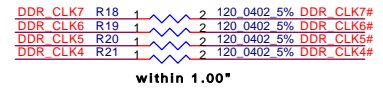


Claw Hammer-DTR

DDR Memory



DDR_CLK5/5# & DDR_CLK7/7#
 route to nearest DIMM
 DDR_CLK4/4# & DDR_CLK6/6#
 route to farthest DIMM

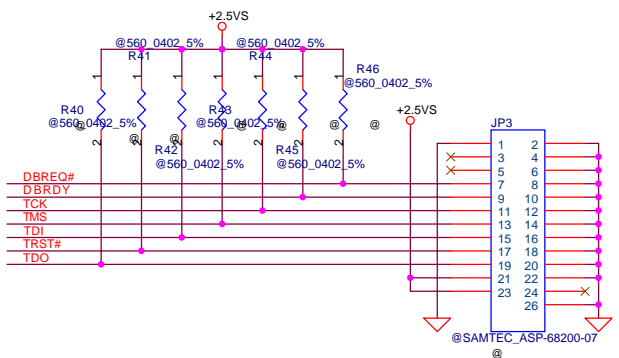
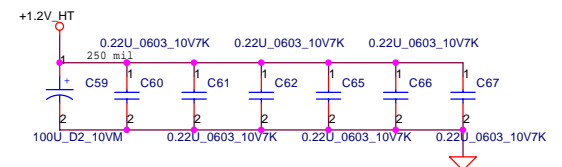
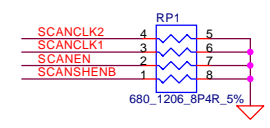
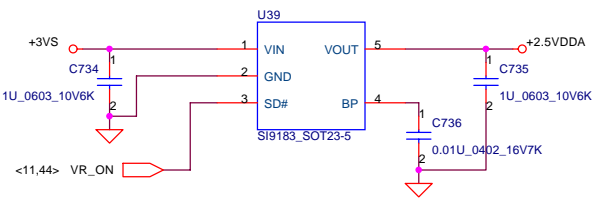
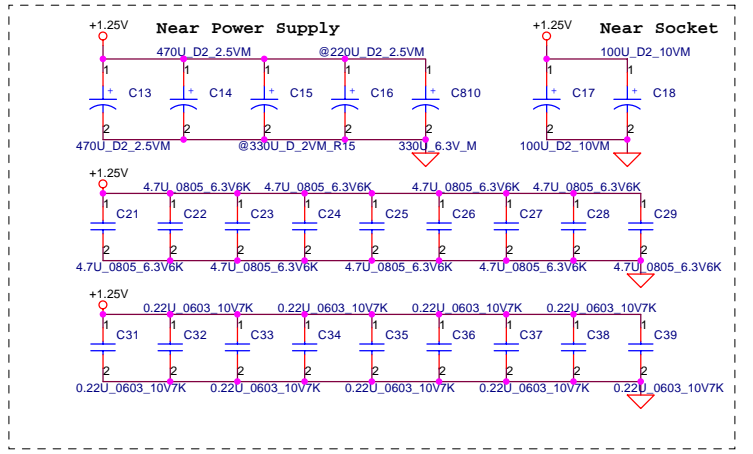
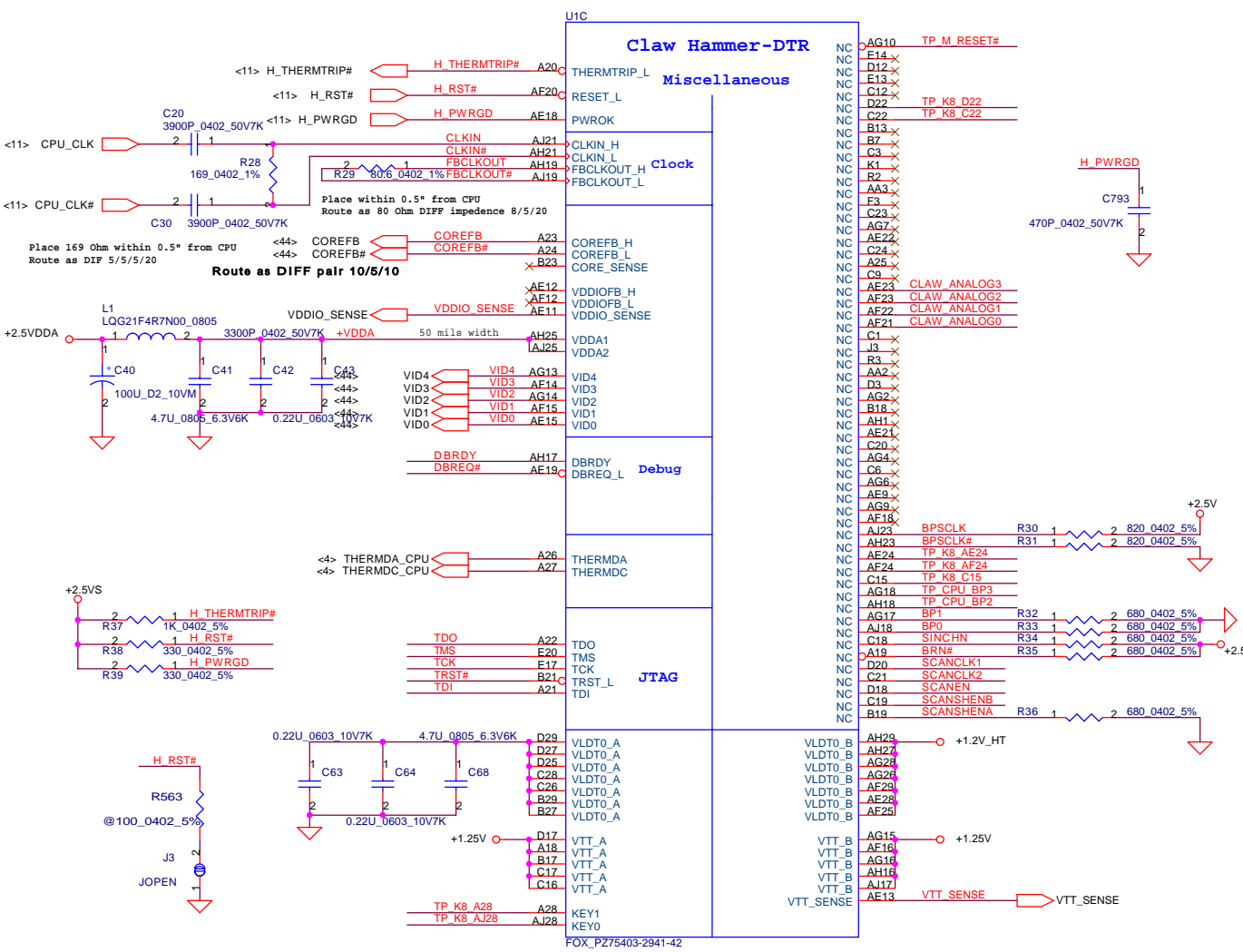


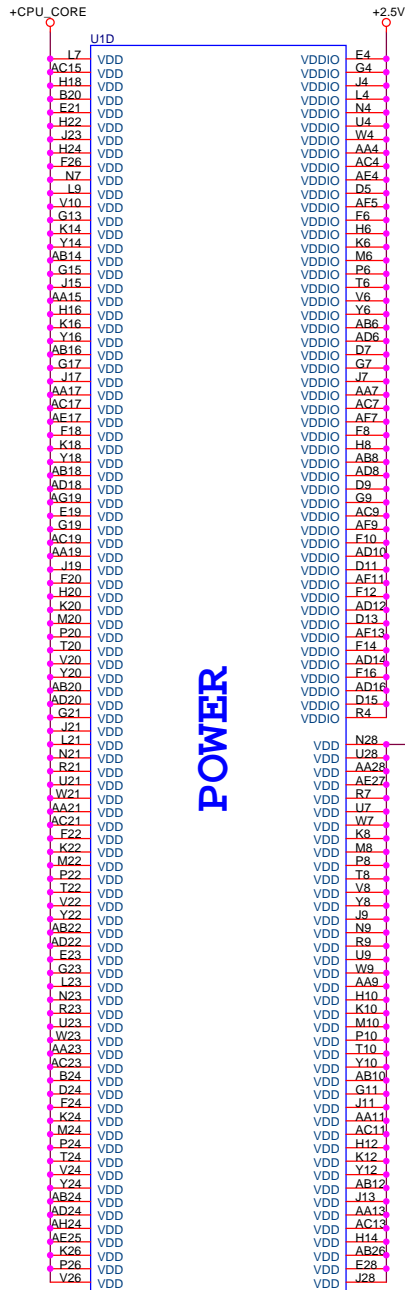
A CHANGE ADDRESS

B CHANGE ADDRESS

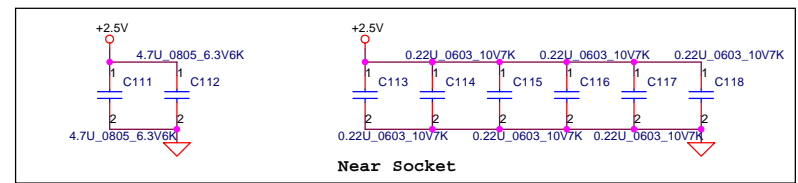
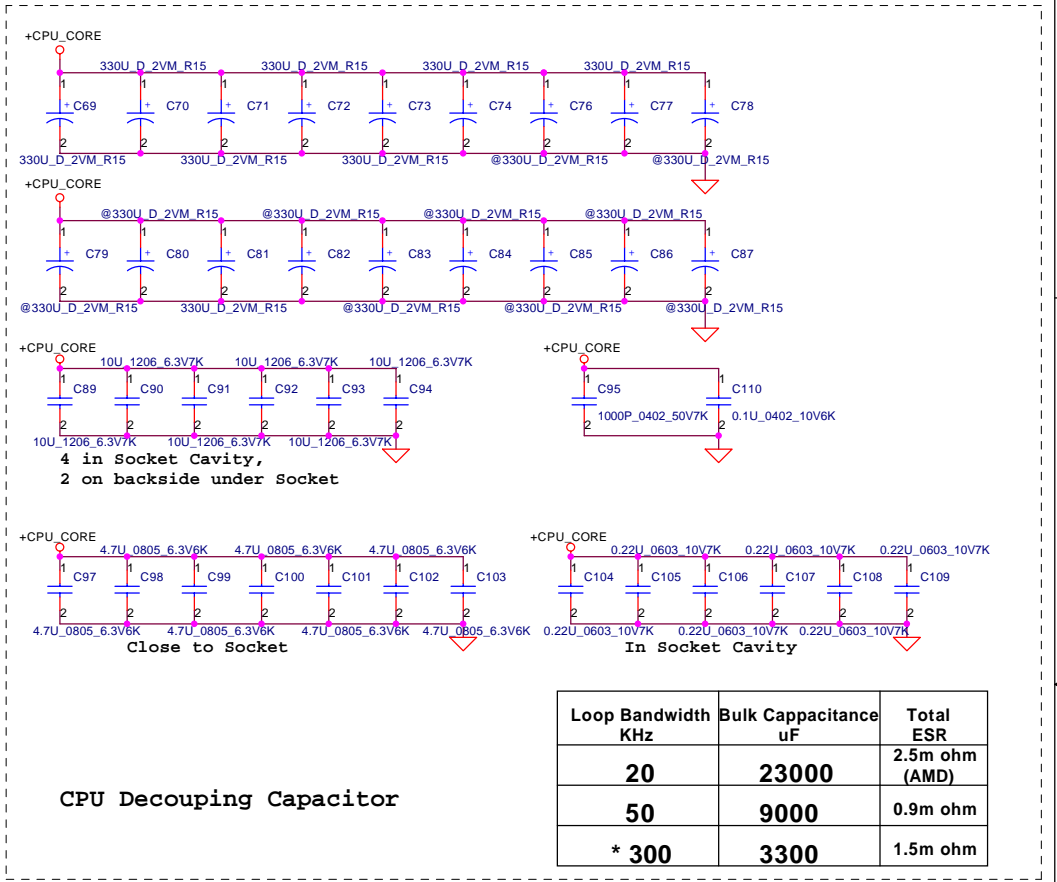
Compal Electronics, Inc.
Claw Hammer (MEMORY BUS)
 Title
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U1E	Pin	Signal	U1E	Pin	Signal
	B2	VSS	L28	R28	VSS
	AH20	VSS		W28	VSS
	AB21	VSS		AC28	VSS
	W22	VSS		AH28	VSS
	M23	VSS		AC29	VSS
	L24	VSS		F27	VSS
	AG25	VSS		H2	VSS
	AC27	VSS		K2	VSS
	D2	VSS		M2	VSS
	G4	VSS		T2	VSS
	J4	VSS		V2	VSS
	L4	VSS		Y2	VSS
	N4	VSS		AB2	VSS
	U4	VSS		AD2	VSS
	W4	VSS		AH2	VSS
	AA4	VSS		B4	VSS
	AC4	VSS		AB4	VSS
	AE4	VSS		B6	VSS
	AD5	VSS		G6	VSS
	Y15	VSS		J6	VSS
	AE16	VSS		L6	VSS
	J18	VSS		N6	VSS
	C20	VSS		R6	VSS
	R20	VSS		U6	VSS
	U20	VSS		AC20	VSS
	W20	VSS		AE20	VSS
	AA20	VSS		AD20	VSS
	AC20	VSS		D21	VSS
	AE20	VSS		F21	VSS
	AD20	VSS		H21	VSS
	D7	VSS		K21	VSS
	G7	VSS		M21	VSS
	J7	VSS		AE21	VSS
	AA7	VSS		T21	VSS
	AC17	VSS		V21	VSS
	AE17	VSS		Y21	VSS
	F18	VSS		AD21	VSS
	K18	VSS		AC21	VSS
	H18	VSS		E22	VSS
	Y18	VSS		G22	VSS
	AB18	VSS		J22	VSS
	AD18	VSS		L22	VSS
	AG19	VSS		U22	VSS
	E19	VSS		W22	VSS
	G19	VSS		AA22	VSS
	AC19	VSS		AC22	VSS
	AA19	VSS		AE22	VSS
	H19	VSS		AD22	VSS
	F20	VSS		AC22	VSS
	H20	VSS		AE22	VSS
	K20	VSS		AD23	VSS
	M20	VSS		F23	VSS
	P20	VSS		H23	VSS
	T20	VSS		K23	VSS
	V20	VSS		U23	VSS
	Y20	VSS		W23	VSS
	AB20	VSS		AA28	VSS
	AD20	VSS		AE27	VSS
	G21	VSS		R7	VSS
	J21	VSS		AD23	VSS
	L21	VSS		AG23	VSS
	N21	VSS		G24	VSS
	R21	VSS		J24	VSS
	U21	VSS		N24	VSS
	W21	VSS		R24	VSS
	J21	VSS		U24	VSS
	AA21	VSS		W24	VSS
	AC21	VSS		AA24	VSS
	F22	VSS		AC24	VSS
	K22	VSS		AG24	VSS
	M22	VSS		AD24	VSS
	P22	VSS		AE24	VSS
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	T24	VSS		J13	VSS
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	Y24	VSS		AD17	VSS
	AB24	VSS		B16	VSS
	AD24	VSS		G18	VSS
	AH24	VSS		AA18	VSS
	AE25	VSS		AC18	VSS
	K26	VSS		D19	VSS
	P26	VSS		F19	VSS
	V26	VSS		H19	VSS
				K19	VSS
				Y19	VSS
				AB19	VSS
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				AE19	VSS
				J20	VSS
				L20	VSS
				N20	VSS

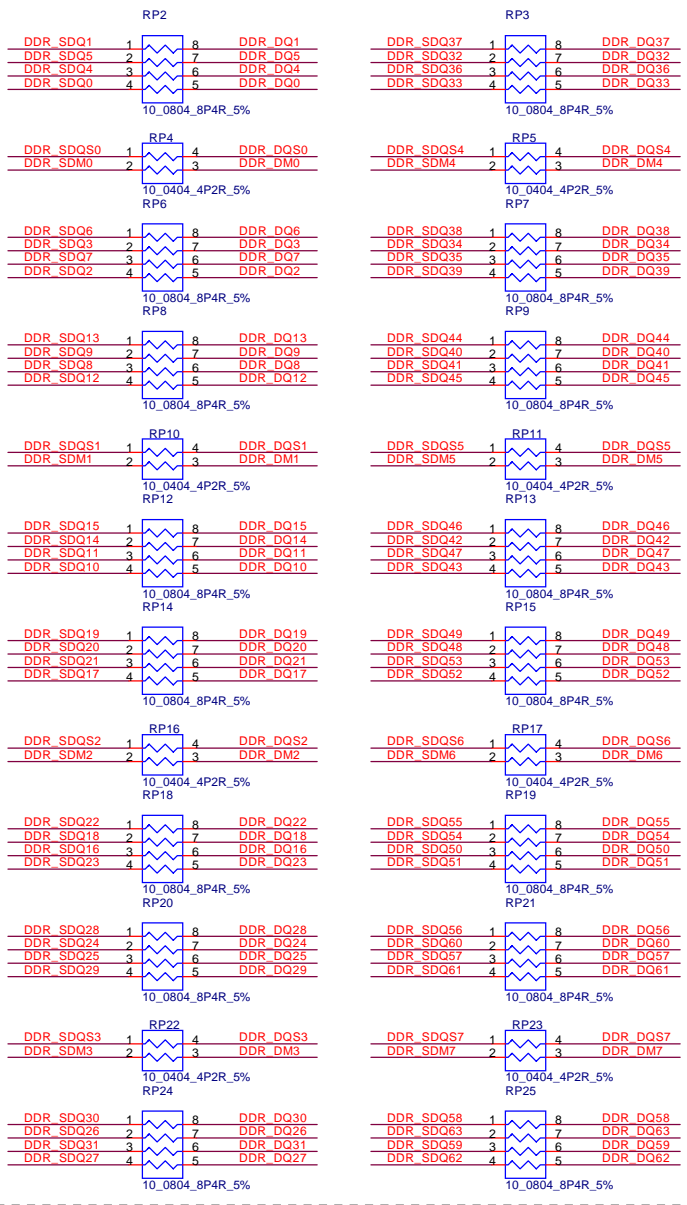


FOX_PZ75403-2941-42

FOX_PZ75403-2941-42

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Claw Hammer (Power & Ground)		
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Note:
DDR_SMAA13 Recommend for AMD

Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil



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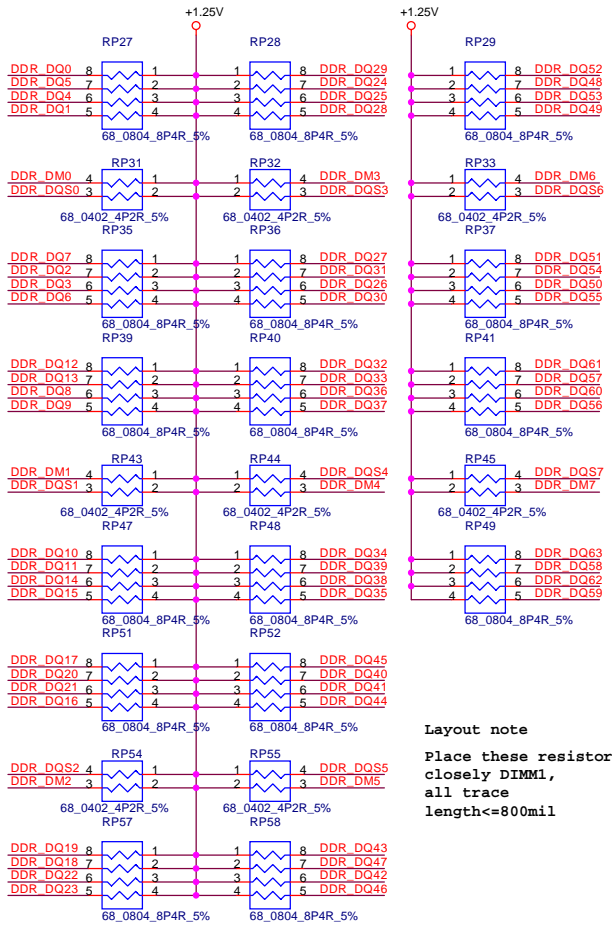
Title: **DDR-SODIMM SLOT0**

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SO-DIMM0
REVERSE

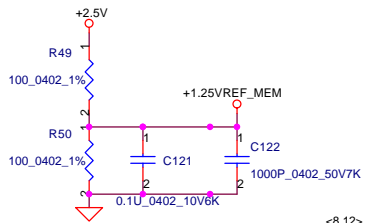
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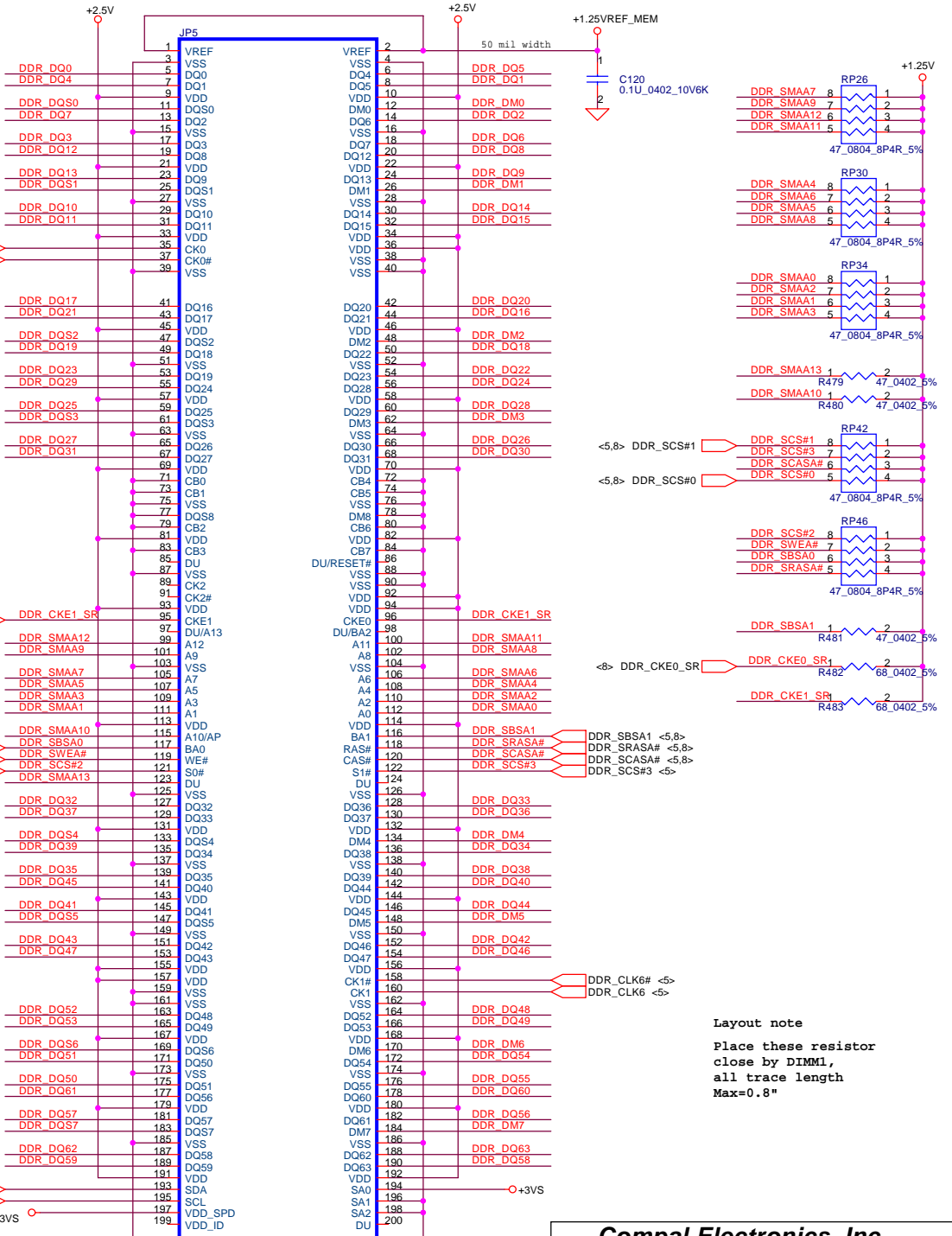
Layout note
Place these resistor closely DIMM1, all trace length<=800mil

Note:
DDR_SMAA13 Recommend for AMD.

- <8> DDR_DQS[0..7]
- <8> DDR_DQ[0..63]
- <8> DDR_DM[0..7]
- <5,8> DDR_SMAA[0..13]



- <8,12> DIMM_SMDATA
- <8,12> DIMM_SMCLK

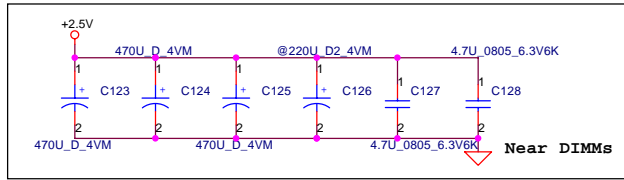


Layout note
Place these resistor close by DIMM1, all trace length Max=0.8"

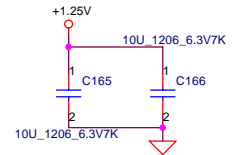
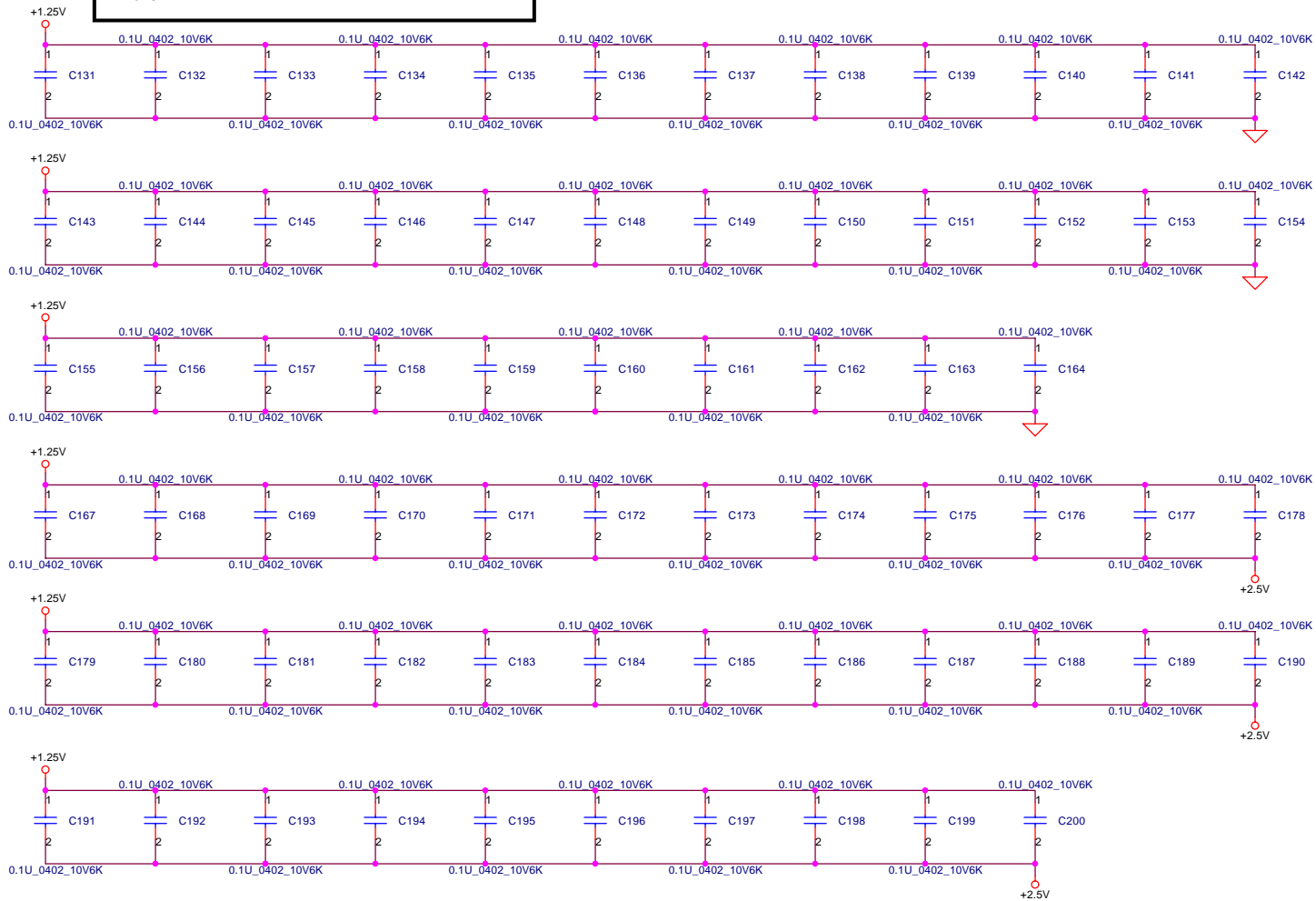
DIMM1 STANDARD

Compal Electronics, Inc.		
title		
DDR-SODIMM SLOT1		
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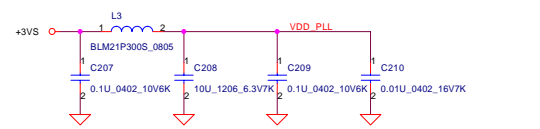
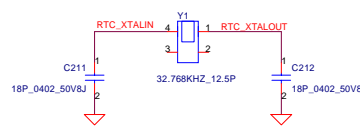
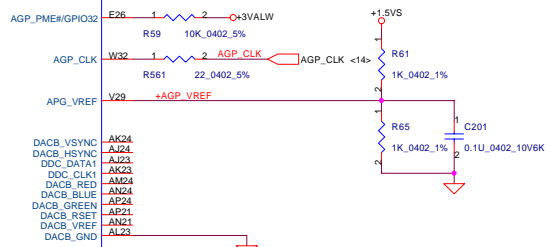
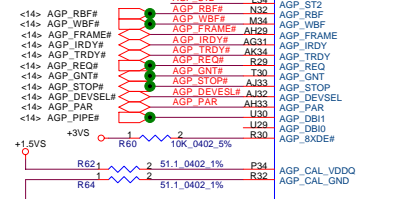
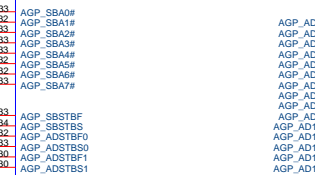
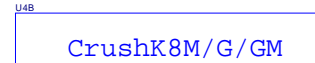
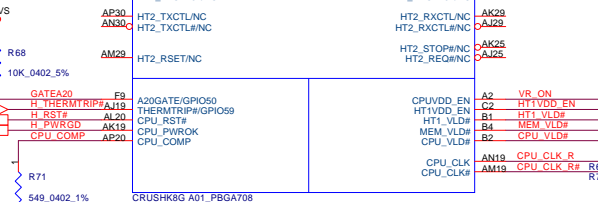
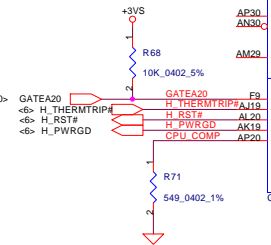
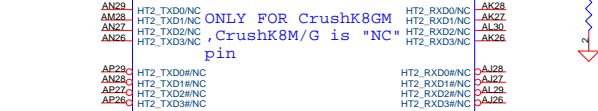
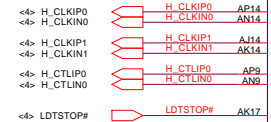
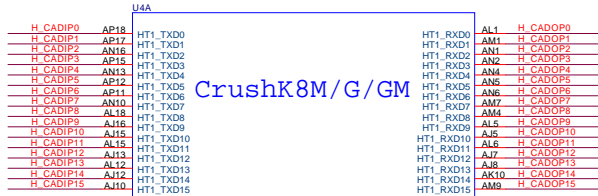
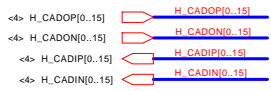


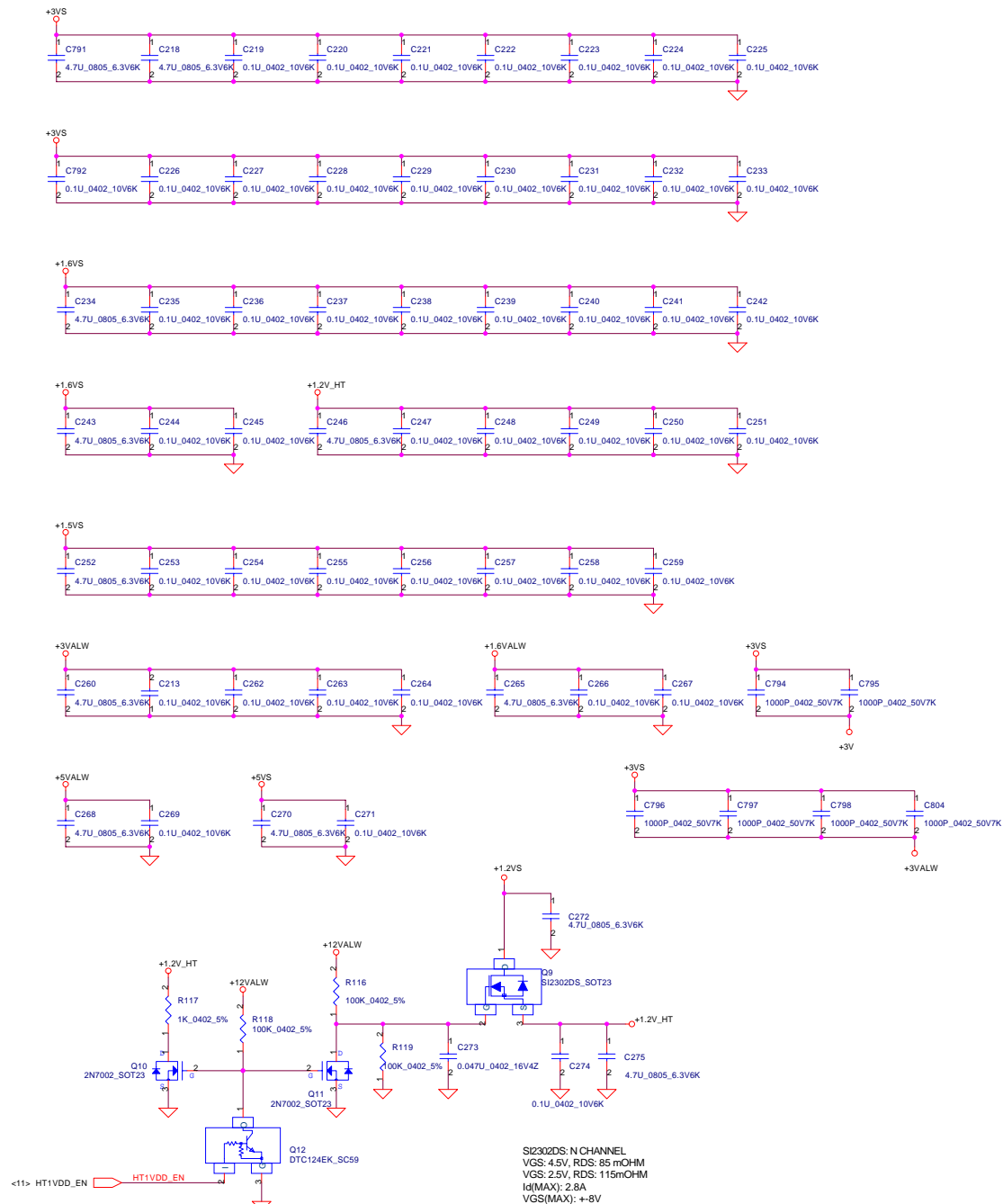
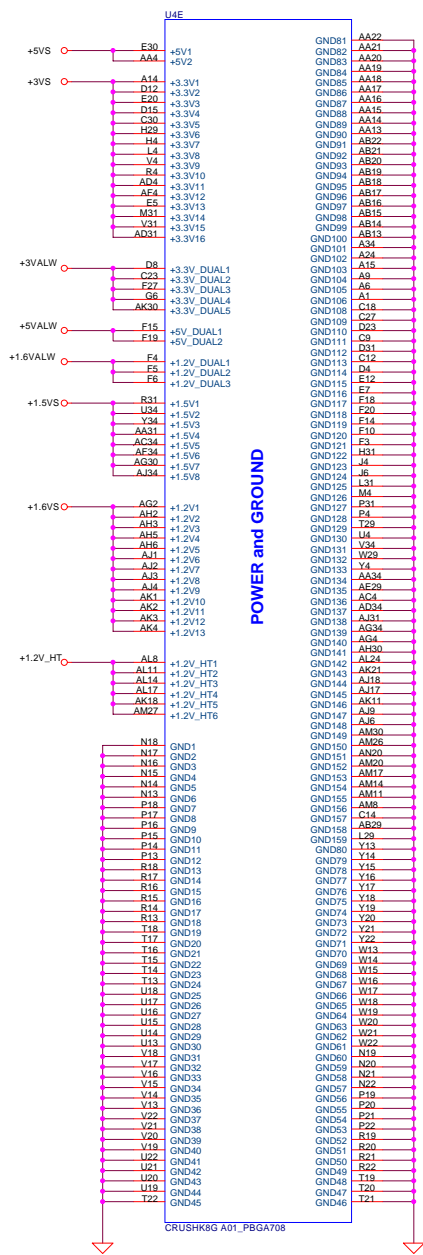
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS

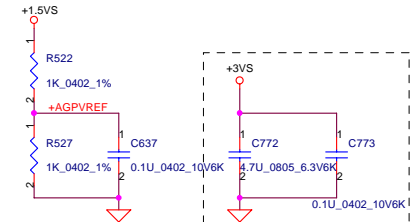
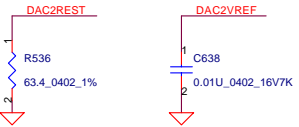
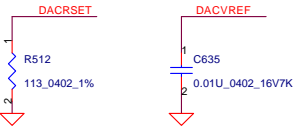
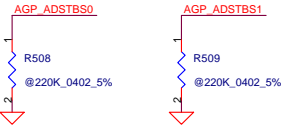
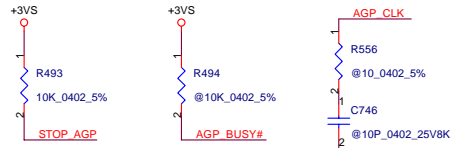


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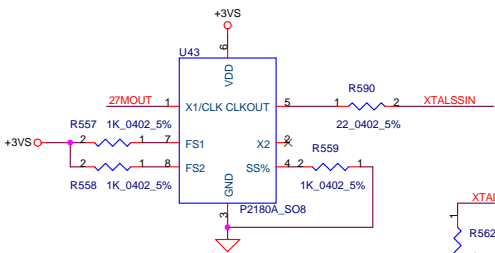
Compal Electronics, Inc. DDR SODIMM Decoupling		
Title		
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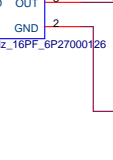
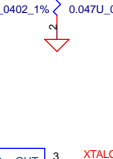
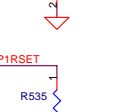
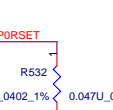
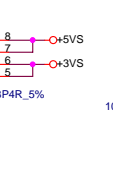
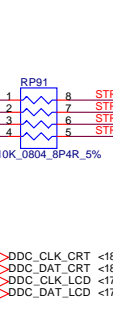
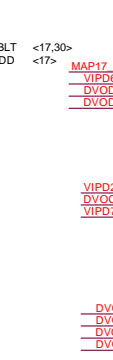
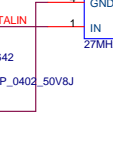
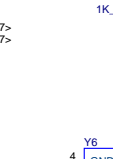
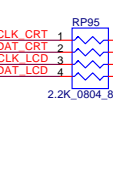
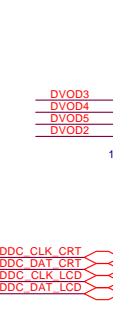
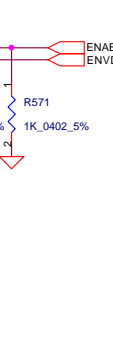
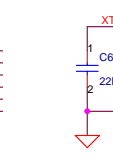
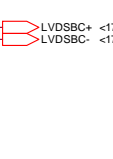
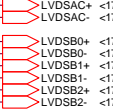
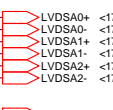
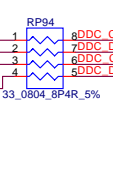
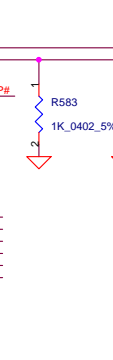
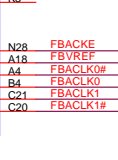
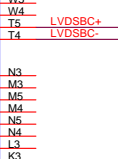
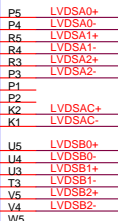
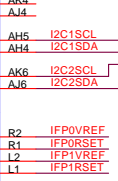
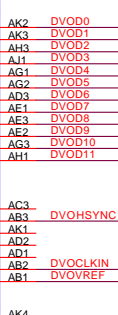
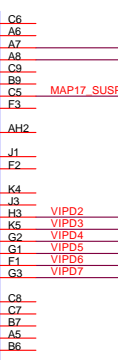
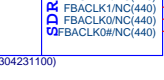
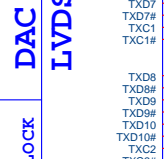
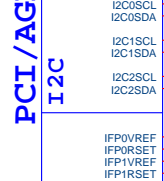
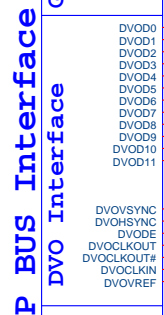
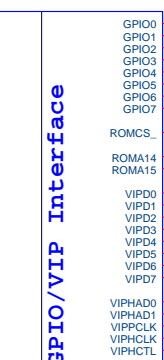
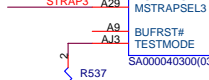
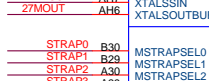
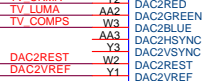
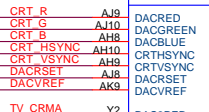
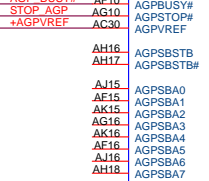
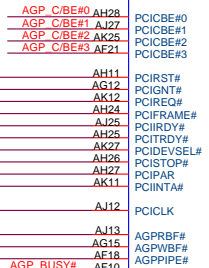
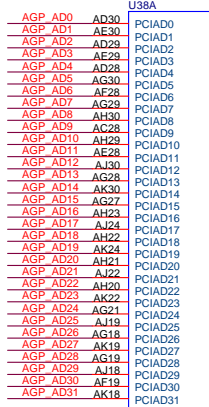


Place close to U43.6

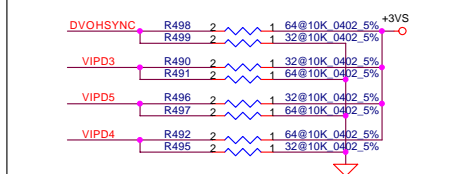


SST Ratio selection table for W180

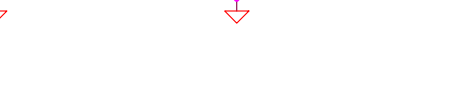
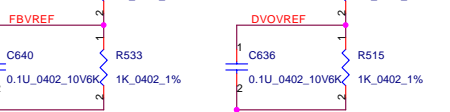
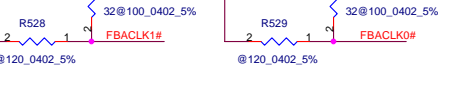
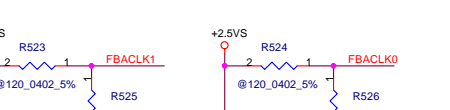
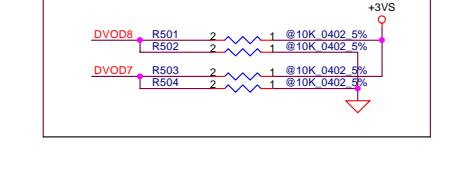
Modulation setting	SST Ratio
SS#	
0	1.25%
1	3.75%



DVOHSYNC	VIPD3	VIPD5	VIPD4	DEVICE
1	1	0	1	MAP17-116 (16MB)
0	1	1	0	* MAP17-232 (32MB)
1	0	0	1	MAP17-464 (64MB)



DVOD8	DVOD7	TVMODE
0	0	SECAM
0	1	* NTSC
1	0	PAL
1	1	VGA



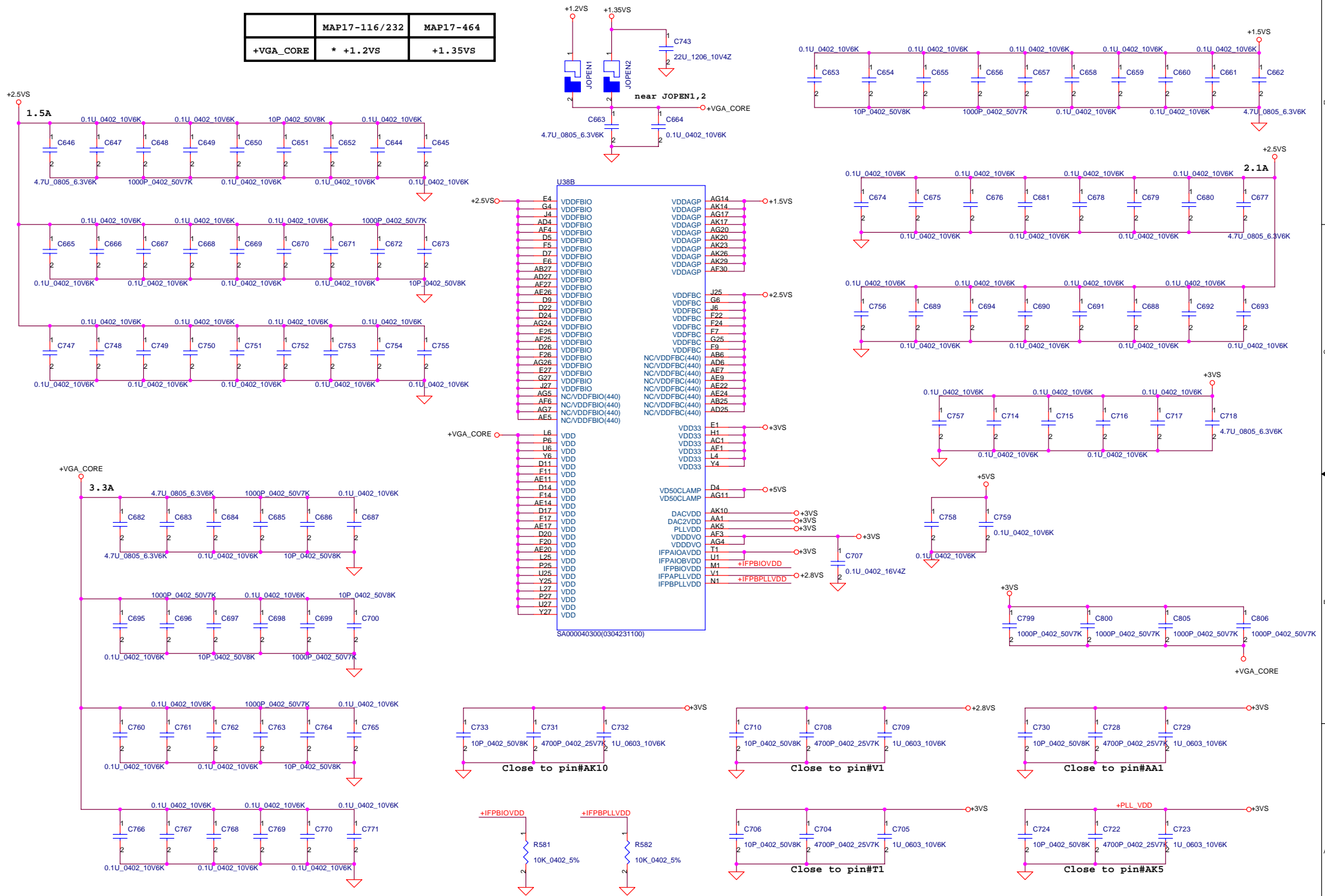
Compal Electronics, Inc.

MAP17 AGP Interface(1/3)

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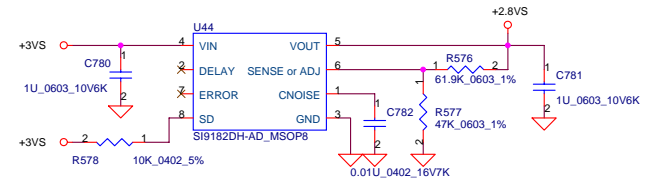
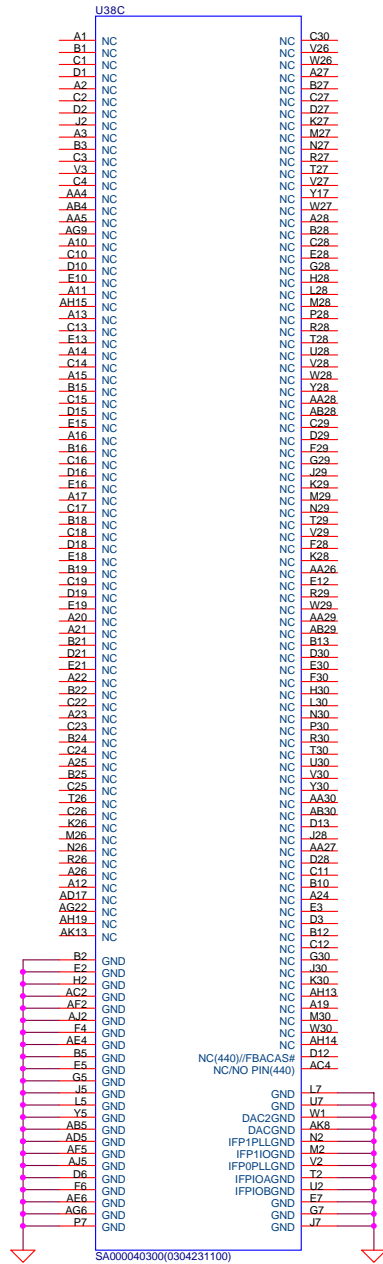
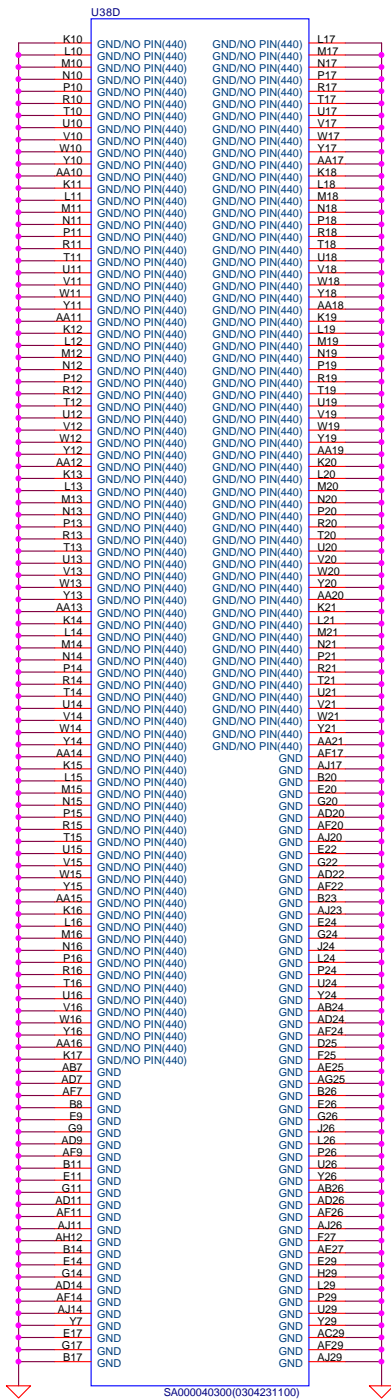
Size: Custom
Date: Friday, April 16, 2004
Document Number: LA-2392
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	MAP17-116/232	MAP17-464
+VGA_CORE	* +1.2VS	+1.35VS



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MAP17 Power (2/3)		
Title		
Size	Document Number	Rev
Custom	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 15 of 53



Compal Electronics, Inc.

Title: **MAP17 NC/GND(3/3)**

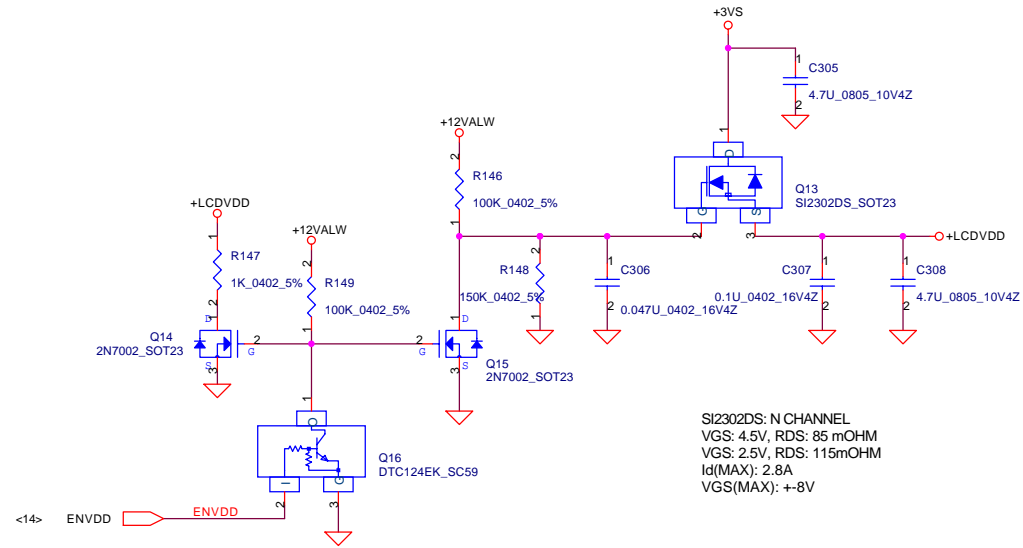
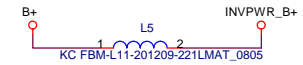
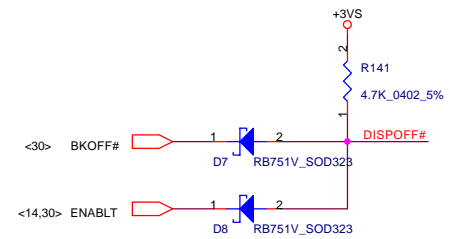
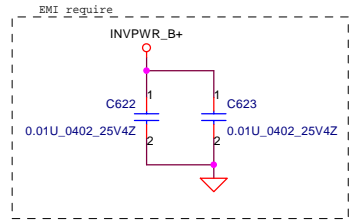
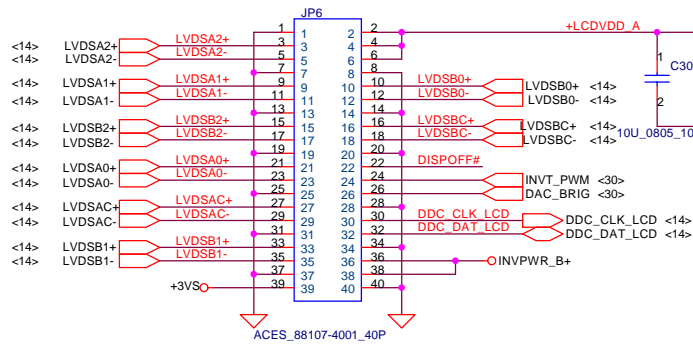
Size	Document Number	Rev
Custom	LA-2392	0.1

Date: Friday, April 16, 2004 Sheet 16 of 53

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LCD Panel Connector

The cap.'s colselly to LCD CONN.

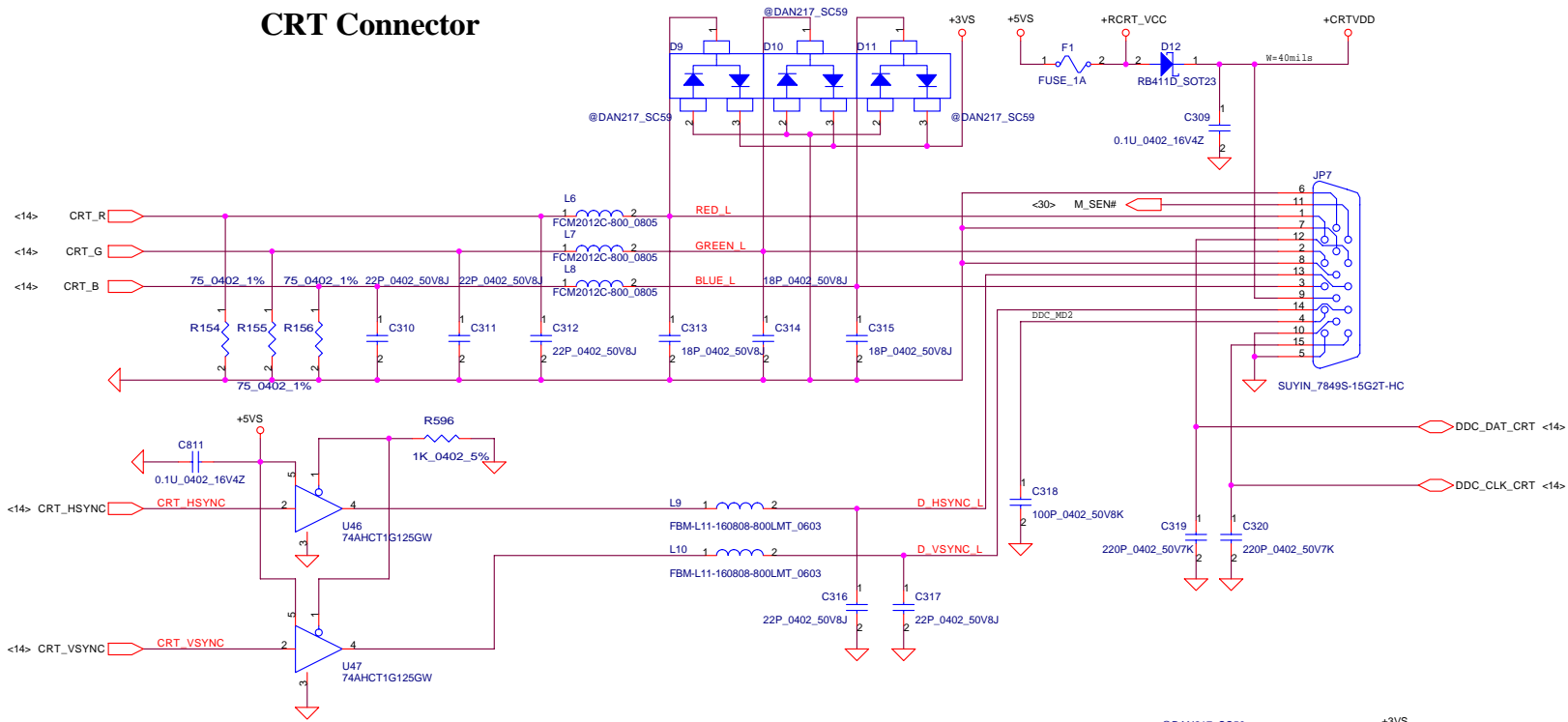


SI2302DS: N CHANNEL
 VGS: 4.5V, RDS: 85 mOHM
 VGS: 2.5V, RDS: 115mOHM
 Id(MAX): 2.8A
 VGS(MAX): +-8V

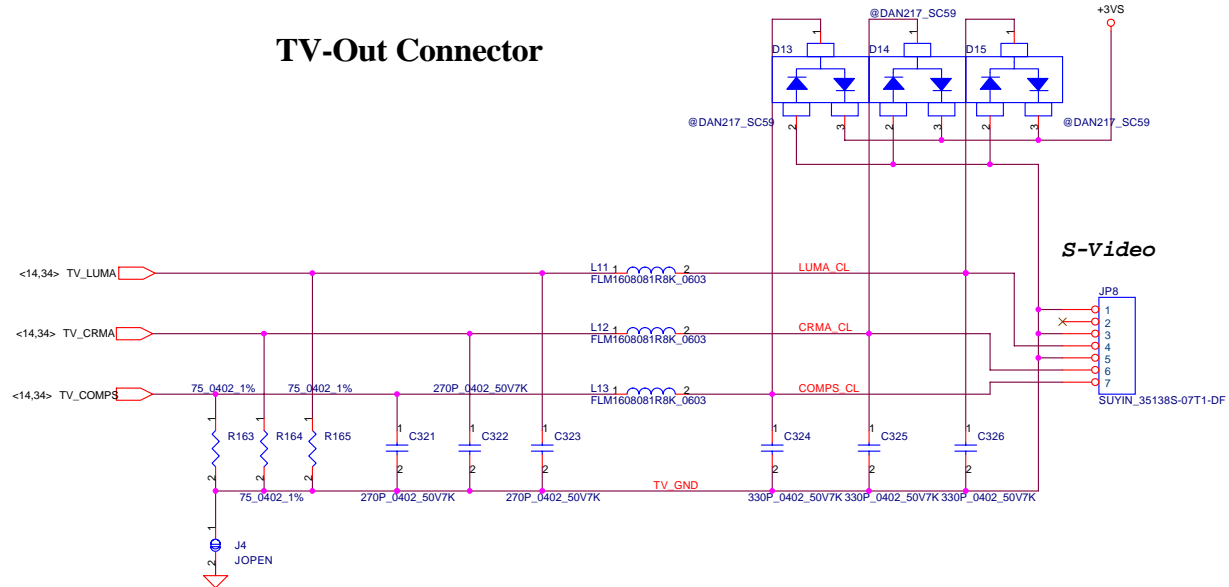
Compal Electronics, Inc.		
Title LVDS Connector		
Size	Document Number LA-2392	Rev 0.1
Date:	Friday, April 16, 2004	Sheet 17 of 53

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CRT Connector



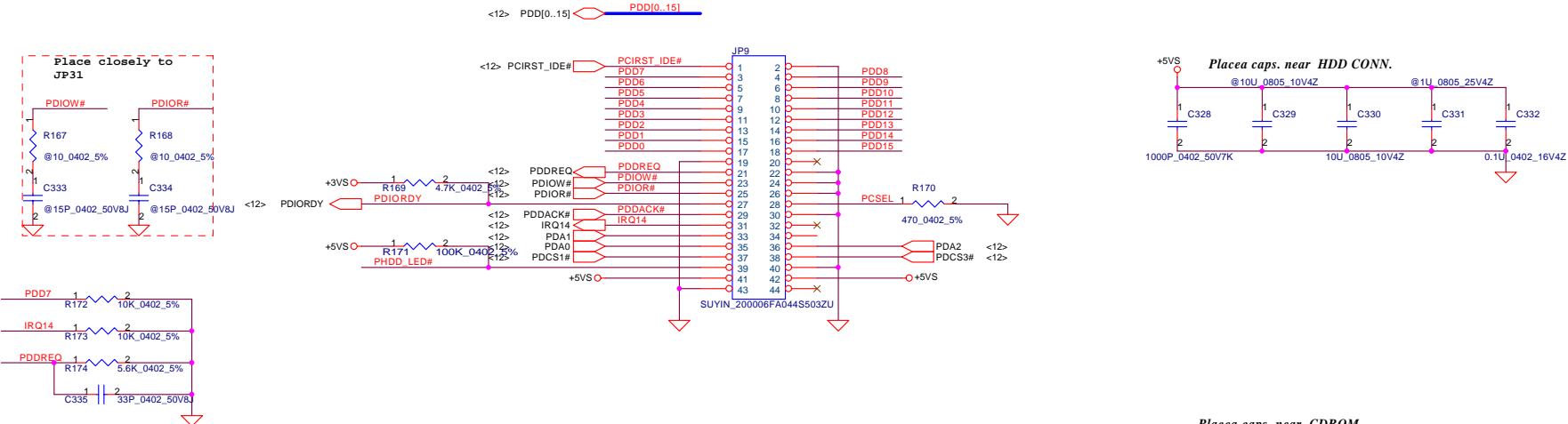
TV-Out Connector



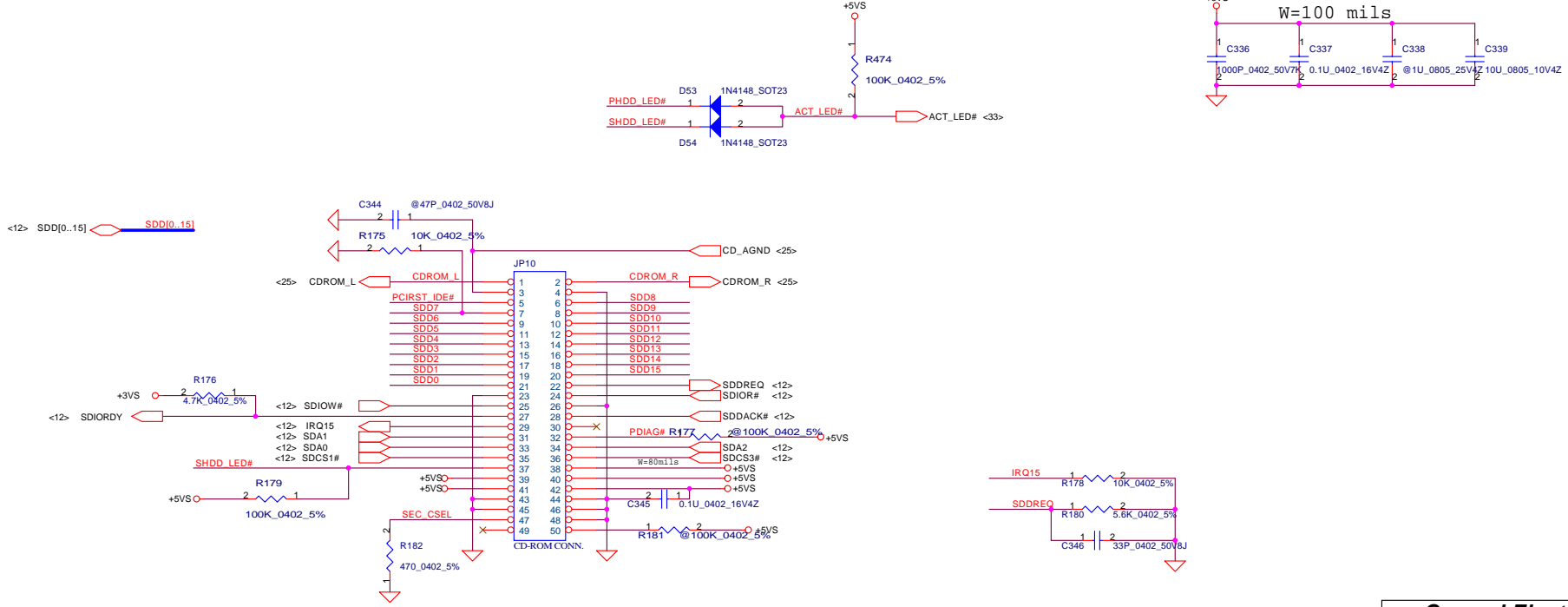
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Compal Electronics, Inc.		
Title CRT & TVout Connector		
Size	Document Number LA-2392	Rev 0.1
Date:	Friday, April 16, 2004	Sheet 18 of 53

HDD Connector

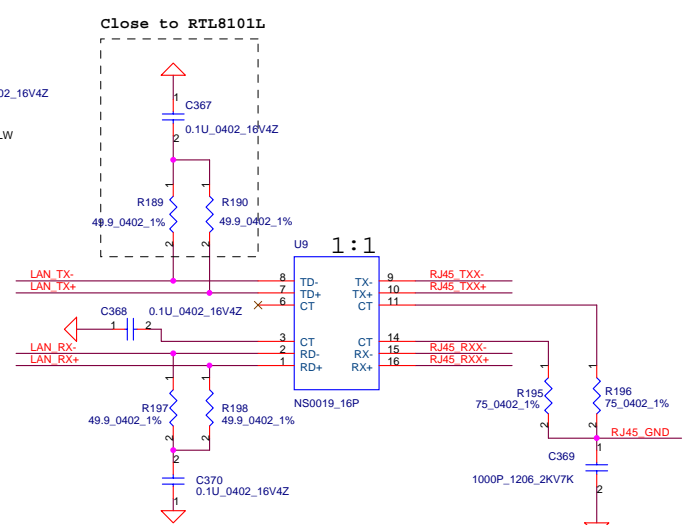
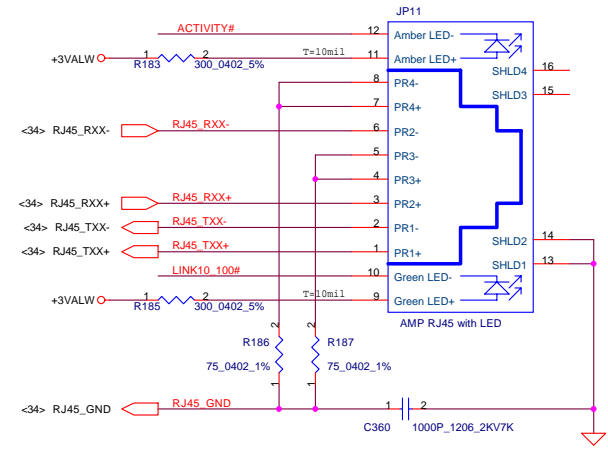
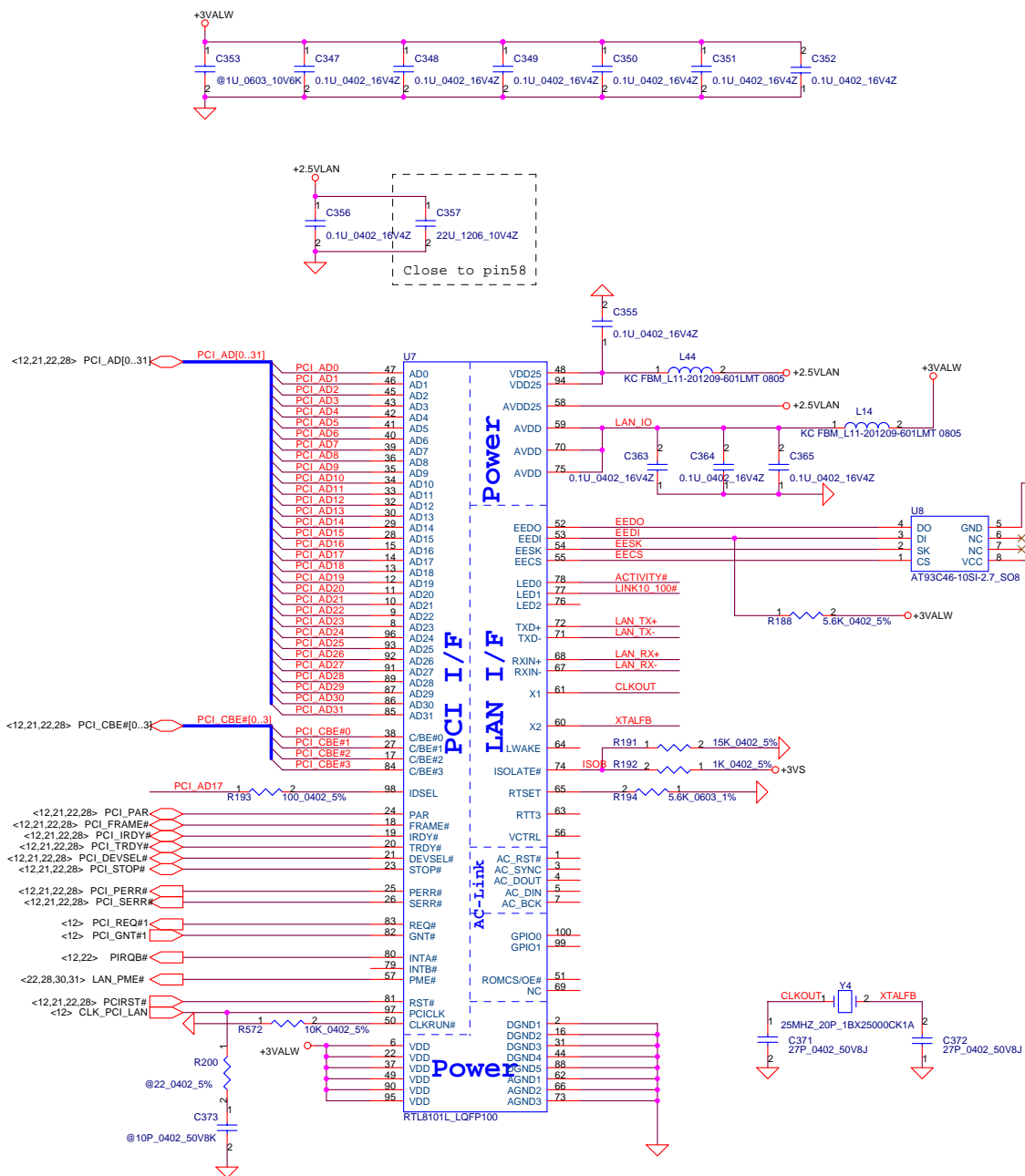


CD-ROM Connector



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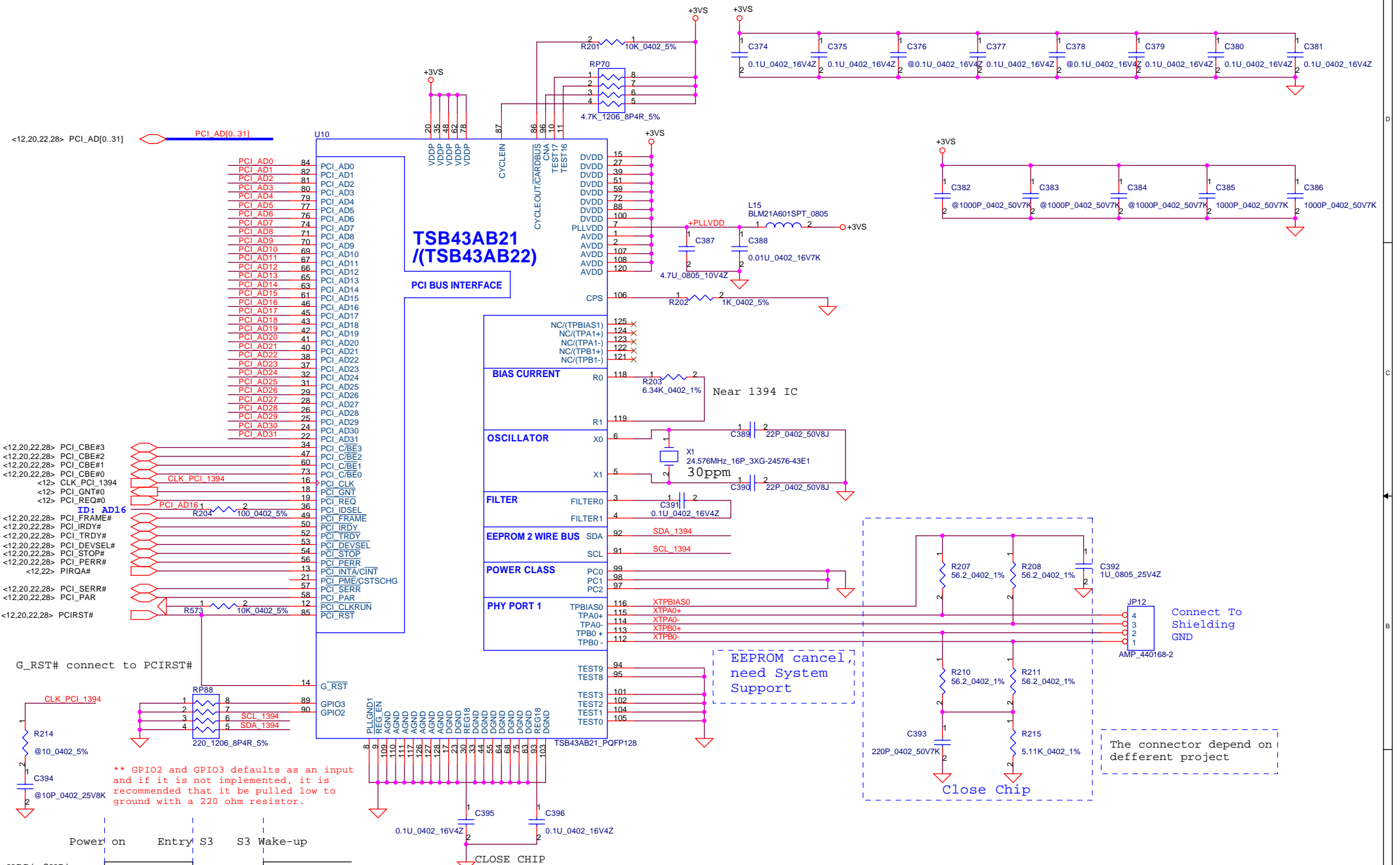
Compal Electronics, Inc.		
Title	IDE/FDD/CD-ROM Module	
Size	Document Number	Rev
Custom	LA-2392	0.1
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- Layout Recommend :
1. LAN_RD+, LAN_RD- should be equal length as possible
 2. LAN_TD+, LAN_TD- should be equal length as possible
 3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
 4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

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Compal Electronics, Inc.		
Title LAN RealTech8100BL		
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<12.20.22,28> PCI_AD[0..31]

PCI_AD0	84	PCI_AD0
PCI_AD1	82	PCI_AD1
PCI_AD2	81	PCI_AD2
PCI_AD3	80	PCI_AD3
PCI_AD4	79	PCI_AD4
PCI_AD5	77	PCI_AD5
PCI_AD6	76	PCI_AD6
PCI_AD7	74	PCI_AD7
PCI_AD8	71	PCI_AD8
PCI_AD9	70	PCI_AD9
PCI_AD10	69	PCI_AD10
PCI_AD11	67	PCI_AD11
PCI_AD12	66	PCI_AD12
PCI_AD13	65	PCI_AD13
PCI_AD14	63	PCI_AD14
PCI_AD15	61	PCI_AD15
PCI_AD16	61	PCI_AD15
PCI_AD17	46	PCI_AD16
PCI_AD18	43	PCI_AD17
PCI_AD19	42	PCI_AD18
PCI_AD20	41	PCI_AD19
PCI_AD21	40	PCI_AD20
PCI_AD22	38	PCI_AD21
PCI_AD23	38	PCI_AD22
PCI_AD24	32	PCI_AD23
PCI_AD25	31	PCI_AD24
PCI_AD26	29	PCI_AD25
PCI_AD27	28	PCI_AD26
PCI_AD28	26	PCI_AD27
PCI_AD29	25	PCI_AD28
PCI_AD30	24	PCI_AD29
PCI_AD31	22	PCI_AD30

<12.20.22,28> PCI_CBE#3
 <12.20.22,28> PCI_CBE#2
 <12.20.22,28> PCI_CBE#1
 <12.20.22,28> PCI_CBE#0
 <12> CLK_PCI_1394
 <12> PCI_GNT#0
 <12> PCI_REC#0
 ID: AD16
 <12.20.22,28> PCI_FRAME#
 <12.20.22,28> PCI_IRDY#
 <12.20.22,28> PCI_TRDY#
 <12.20.22,28> PCI_DEVSEL#
 <12.20.22,28> PCI_STOP#
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 <12.20.22,28> PCI_SERR#
 <12.20.22,28> PCI_PAR
 <12.20.22,28> PCIRST#

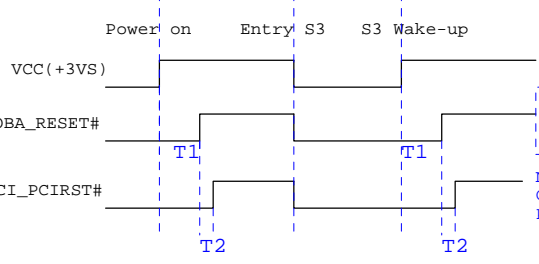
G_RST# connect to PCIRST#

CLK PCI 1394

R214 @10_0402_5%

C394 @10P_0402_25V8K

** GPIO2 and GPIO3 defaults as an input and if it is not implemented, it is recommended that it be pulled low to ground with a 220 ohm resistor.

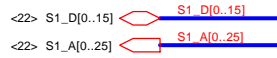


Compal Electronics, Inc.		
Title		
IEEE 1394 CONTROLLER		
Size	Document Number	Rev
	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 21 of 53

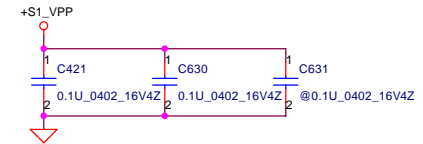
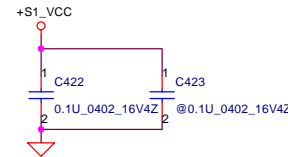
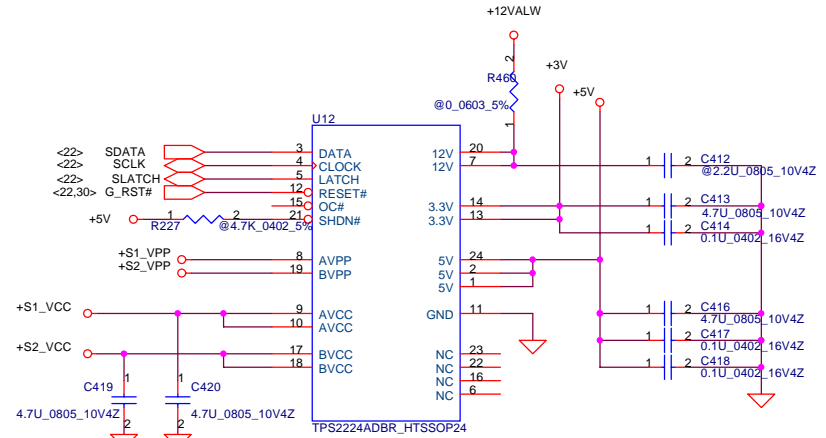
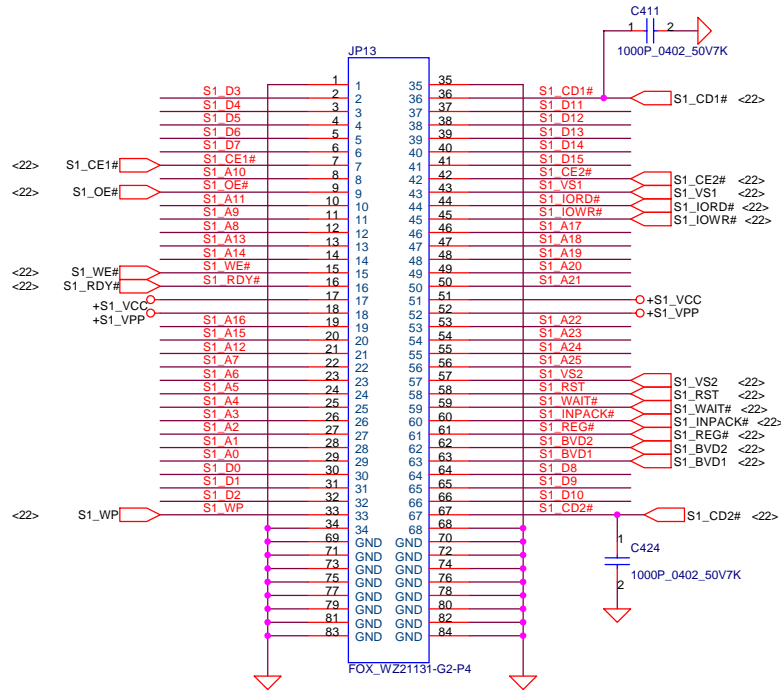
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CARDBUS

SOCKET

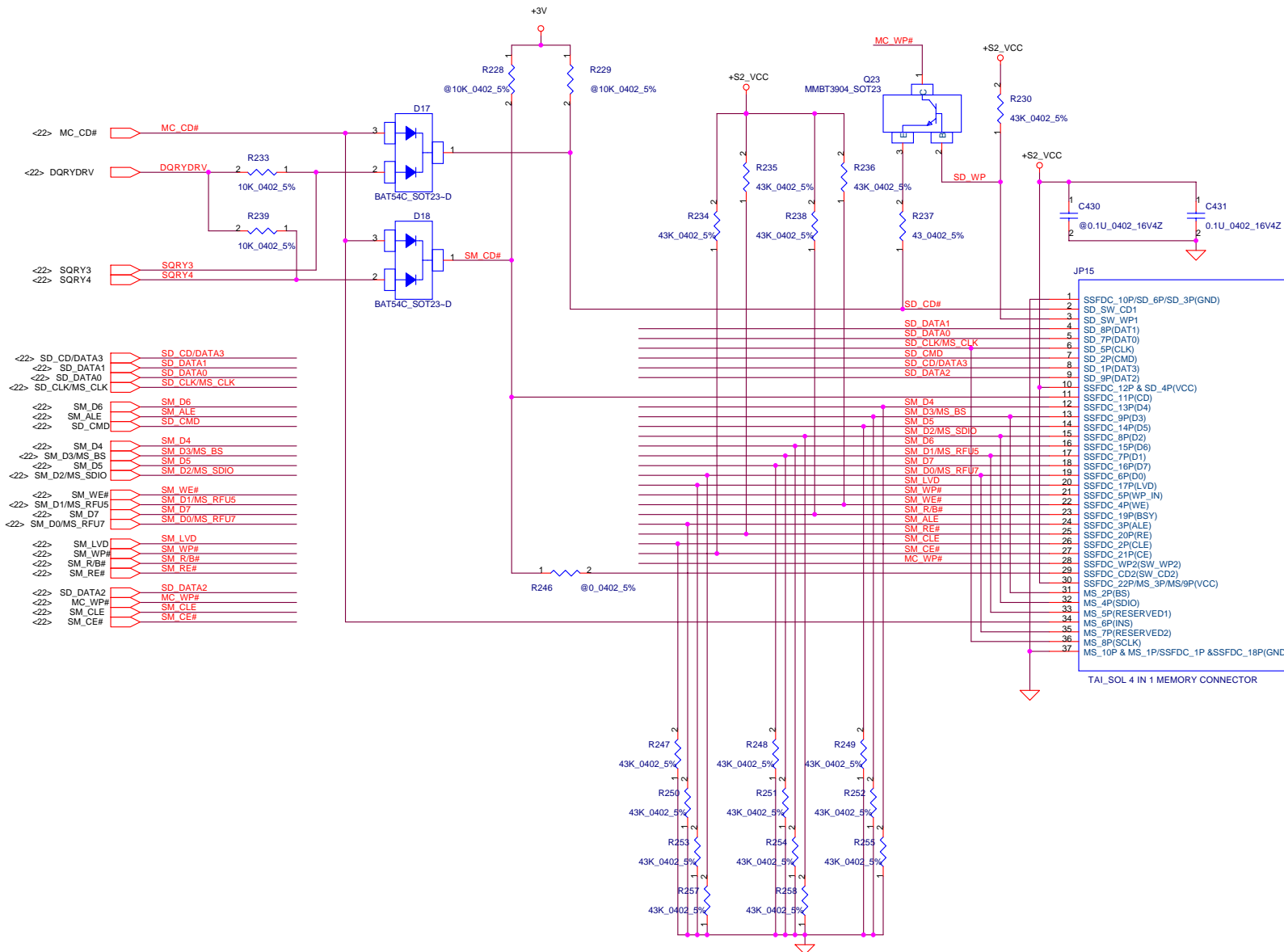


PCMCIA POWER CTRL.



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Compal Electronics, Inc.		
CARD BUS SOCKET		
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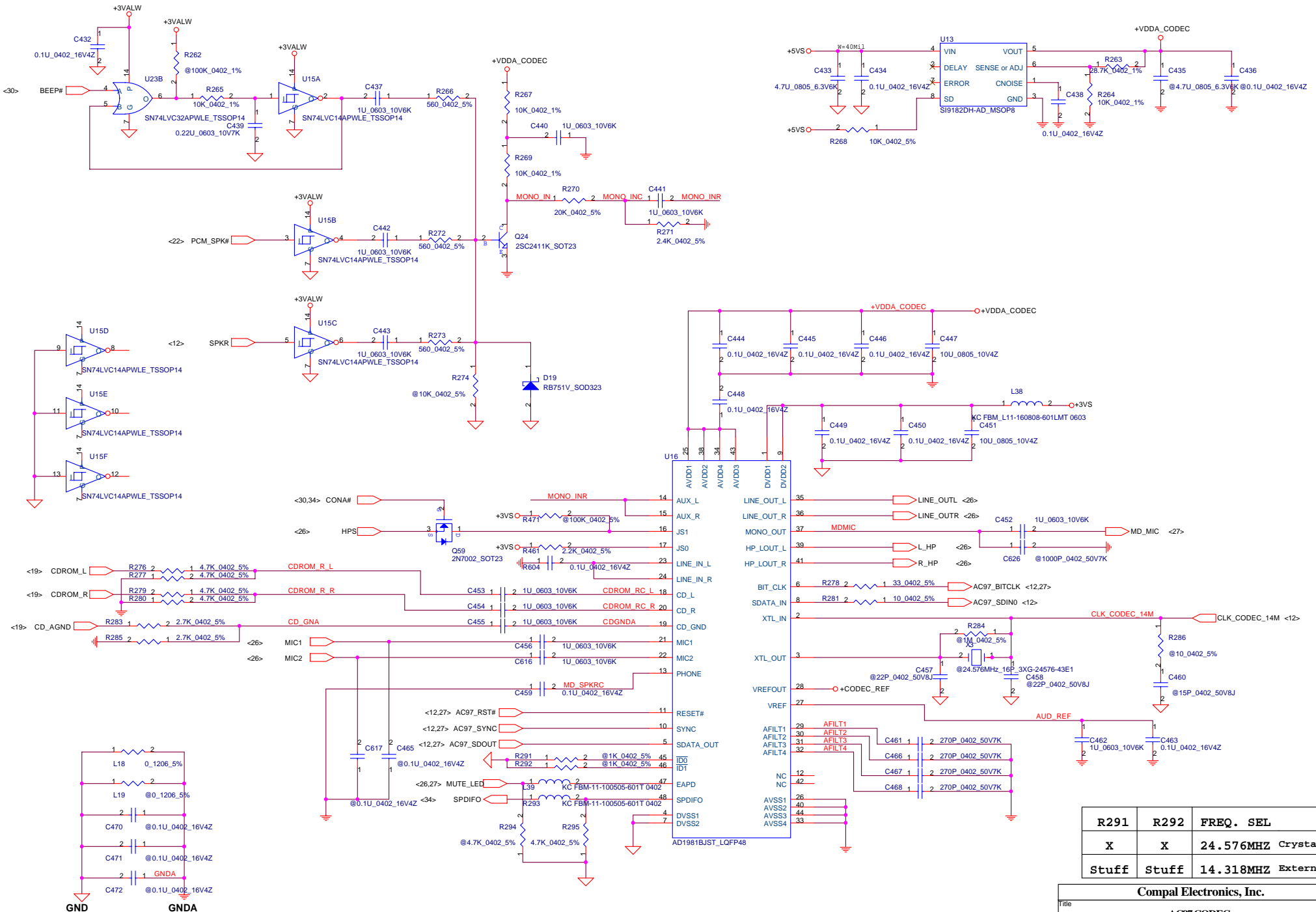
- <22> MC_CD# MC_CD#
- <22> DQRYDRV DQRYDRV
- <22> SQR3 SQR3
- <22> SQR4 SQR4
- <22> SD_CD/DATA3 SD_CD/DATA3
- <22> SD_DATA1 SD_DATA1
- <22> SD_DATA0 SD_DATA0
- <22> SD_CLK/MS_CLK SD_CLK/MS_CLK
- <22> SM_D6 SM_D6
- <22> SM_ALE SM_ALE
- <22> SD_CMD SD_CMD
- <22> SM_D4 SM_D4
- <22> SM_D3/MS_BS SM_D3/MS_BS
- <22> SM_D5 SM_D5
- <22> SM_D2/MS_SDIO SM_D2/MS_SDIO
- <22> SM_WE# SM_WE#
- <22> SM_D1/MS_RFU5 SM_D1/MS_RFU5
- <22> SM_D7 SM_D7
- <22> SM_D0/MS_RFU7 SM_D0/MS_RFU7
- <22> SM_LVD SM_LVD
- <22> SM_WP# SM_WP#
- <22> SM_R/B# SM_R/B#
- <22> SM_RE# SM_RE#
- <22> SD_DATA2 SD_DATA2
- <22> MC_WP# MC_WP#
- <22> SM_CLE SM_CLE
- <22> SM_CE# SM_CE#

1	SSFDC_10P/SD_6P/SD_3P(GND)
2	SD_SW_CD1
3	SD_SW_WP1
4	SD_8P(DAT1)
5	SD_7P(DAT0)
6	SD_5P(CLK)
7	SD_2P(CMD)
8	SD_1P(DAT3)
9	SD_9P(DAT2)
10	SSFDC_12P & SD_4P(VCC)
11	SSFDC_11P(CD)
12	SSFDC_13P(D4)
13	SSFDC_9P(D3)
14	SSFDC_14P(D5)
15	SSFDC_8P(D2)
16	SSFDC_15P(D6)
17	SSFDC_7P(D1)
18	SSFDC_16P(D7)
19	SSFDC_6P(D0)
20	SSFDC_17P(LVD)
21	SSFDC_5P(WP_IN)
22	SSFDC_4P(WE)
23	SSFDC_19P(BSY)
24	SSFDC_3P(ALE)
25	SSFDC_20P(RE)
26	SSFDC_2P(CLE)
27	SSFDC_21P(CE)
28	SSFDC_WP2(SW_WP2)
29	SSFDC_CD2(SW_CD2)
30	SSFDC_22P/MS_3P/MS/9P(VCC)
31	MS_2P(BS)
32	MS_4P(SDIO)
33	MS_5P(RESERVED1)
34	MS_6P(INS)
35	MS_7P(RESERVED2)
36	MS_8P(SCLK)
37	MS_10P & MS_1P/SSFDC_1P & SSFDC_18P(GND)

TAI_SQ1 4 IN 1 MEMORY CONNECTOR

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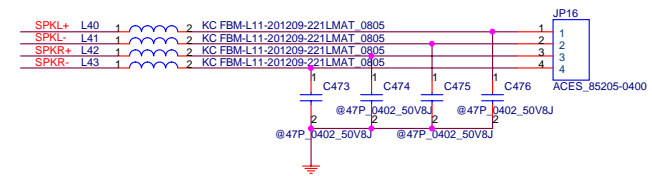
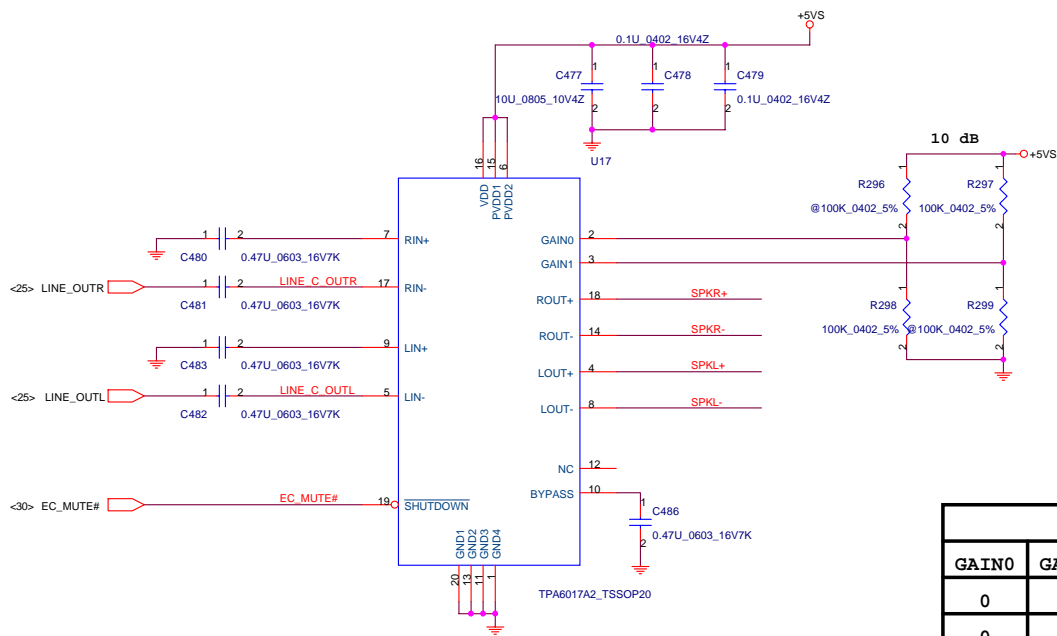
Compal Electronics, Inc.		
Title 4IN 1 CARD READERSOCKET		
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R291	R292	FREQ. SEL
X	X	24.576MHZ Crystal
Stuff	Stuff	14.318MHZ External

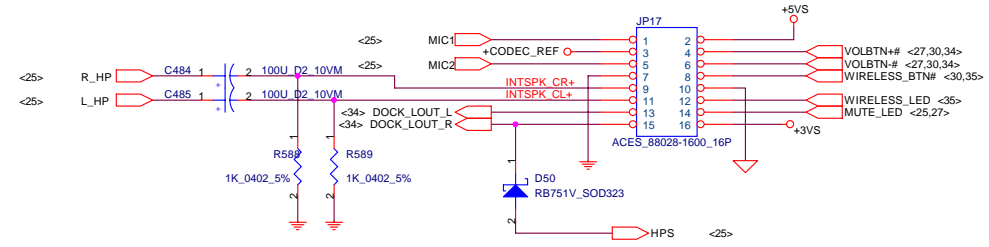
Compal Electronics, Inc.		
AC97 CODEC		
Title		
Size	Document Number	Rev
	LA-2392	0.1
Custom	Friday, April 16, 2004	Sheet 25 of 53

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Gain Settings		
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

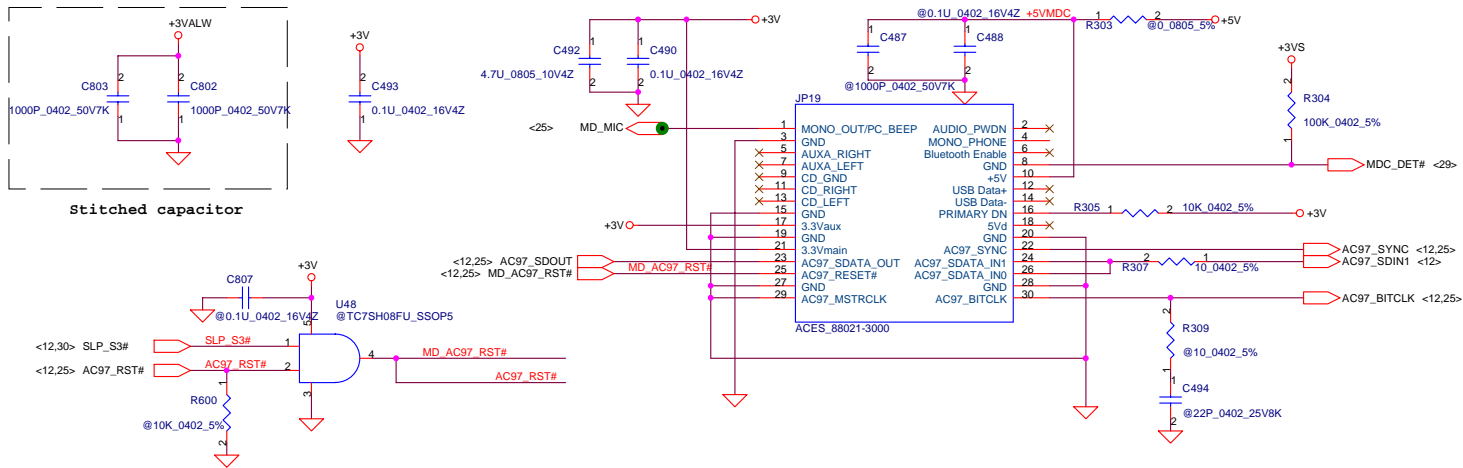
AUDIO CONNECTOR



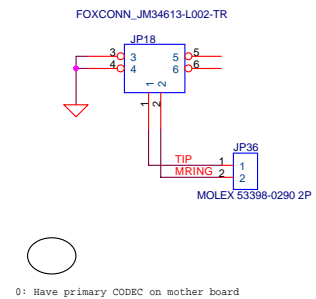
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
Title AMP & Audio Jack		
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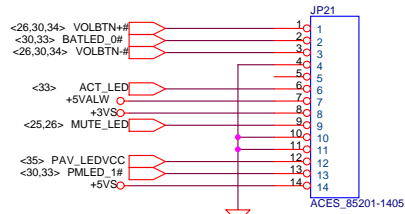
MDC Conn.



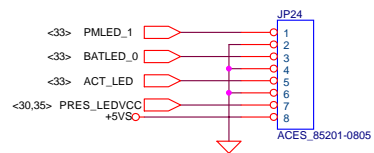
RJ11 CONN.



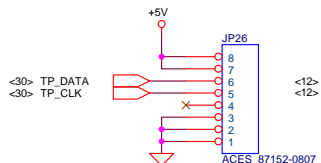
Front Board CONNECTOR Pavilion only



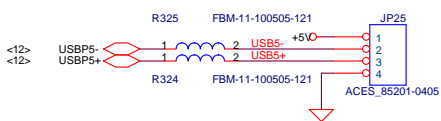
Front Board CONNECTOR PRESARIO only



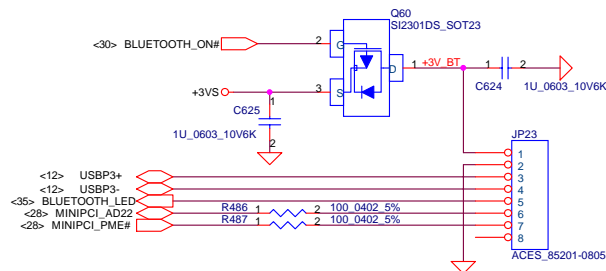
TP CONNECTOR



USB KEY

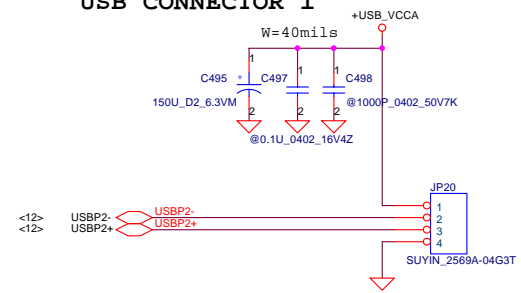


BT CONNECTOR

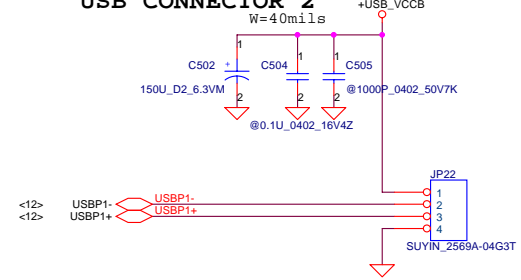


Note: PLACE CLOSE TO EACH USB PORT

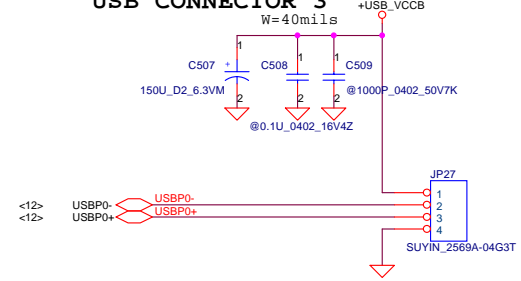
USB CONNECTOR 1



USB CONNECTOR 2



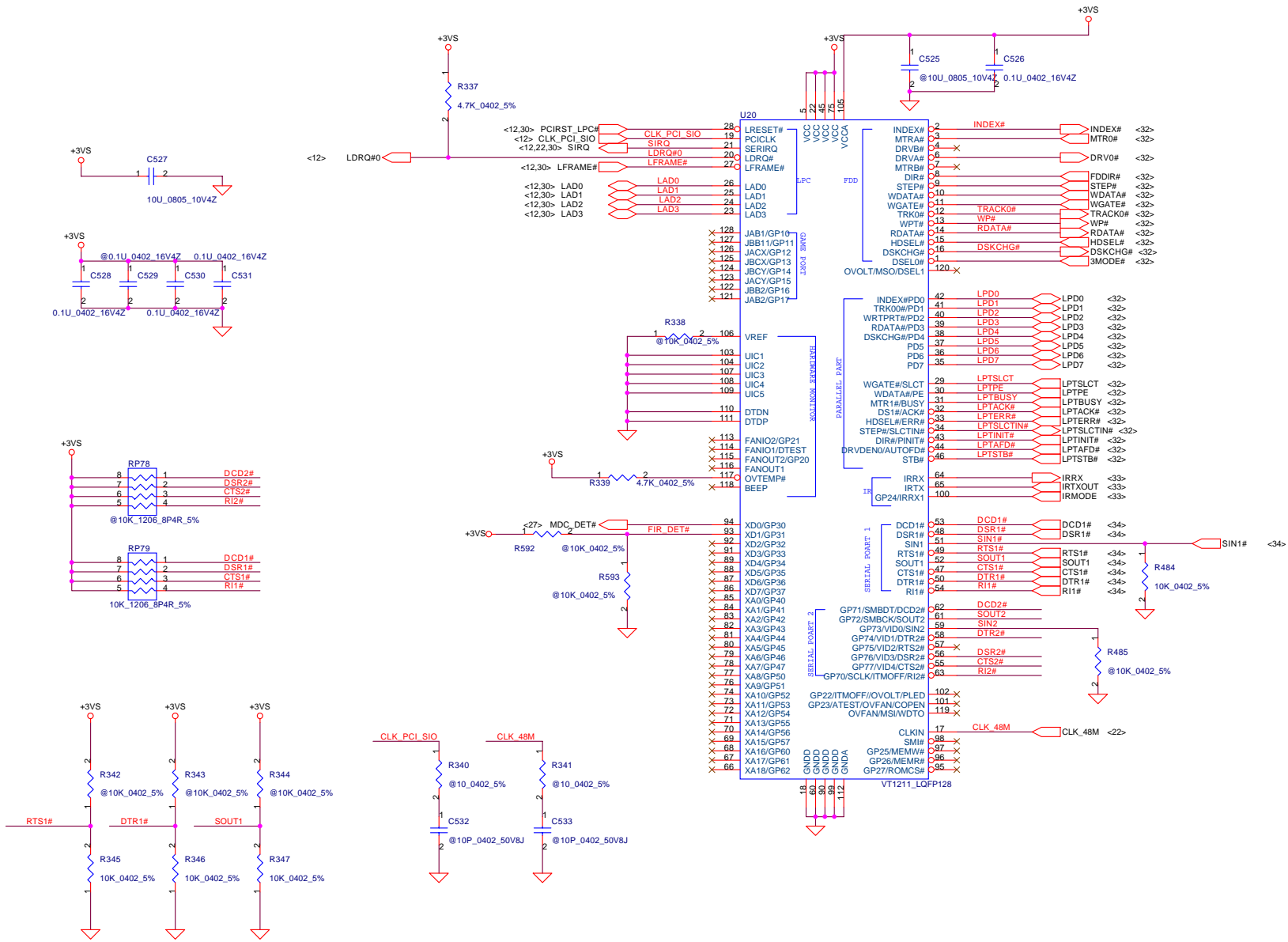
USB CONNECTOR 3



Compal Electronics, Inc.

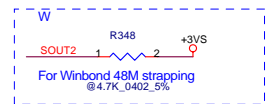
Title		MDC, Bluetooth & USB CONN.	
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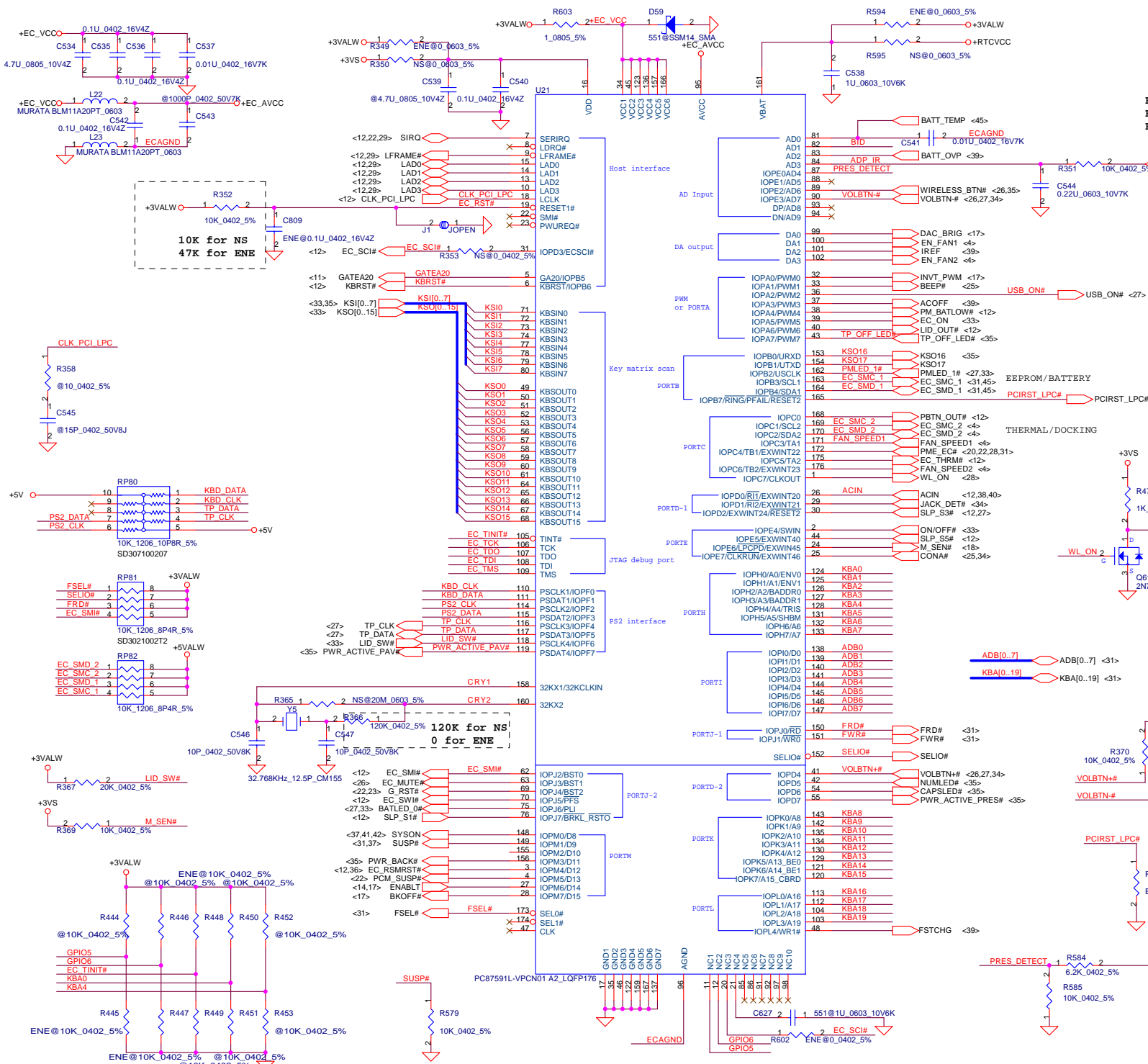


Base address 1:2Eh/2Ph 0:Normal Operation 0: Enable ROM I/F as GPIO
 Base address 0:4Eh/4Ph 1:Test Mode 1:Enable Flash Rom

Super I/O strapping for VT1211



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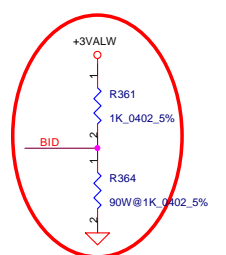
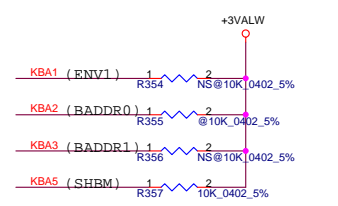


I/O Address		Data
BADDR1-0	Index	2F
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL) (HCFGGBAH, HCFGGBAL)+1	
1 1	Reserved	

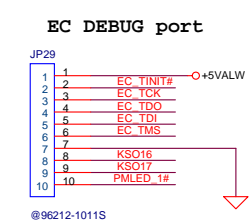
For 591: NS@ IRE 0 0 0
 For 551: NS@ + 551@ * OBD 0 1 0
 For ENE: ENE@ DEV 1 0
 PROG 1 1 0

ENVO ENV1 TRIS
 IRE 0 0 0
 OBD 0 1 0
 DEV 1 0
 PROG 1 1 0

SHBM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



	R364	R361
HR61 120W	V	
HR64 90W	V	V
HR64 120W		V



Compal Electronics, Inc.



KBD EC CTRL-NS PC87591L

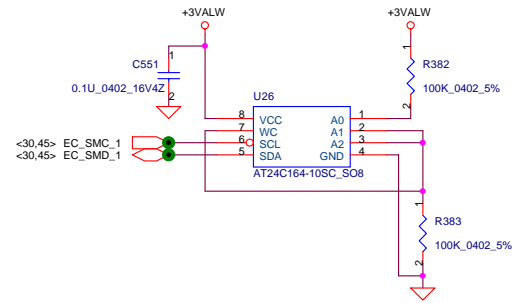
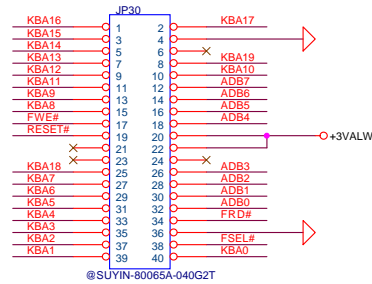
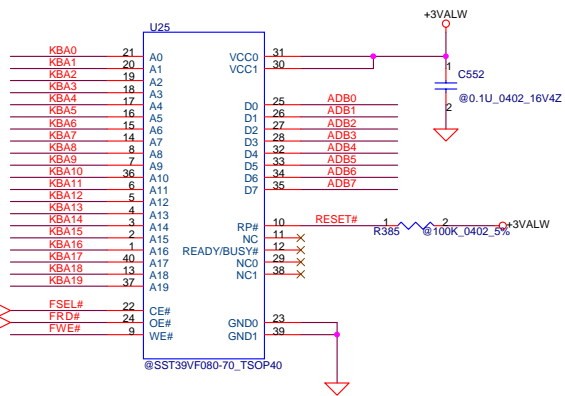
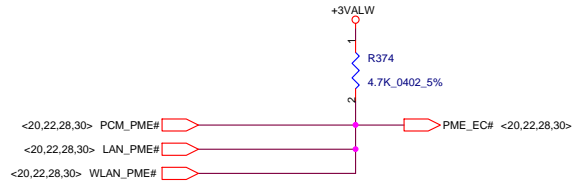
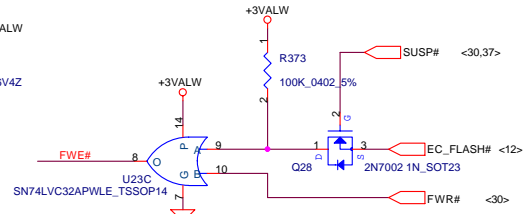
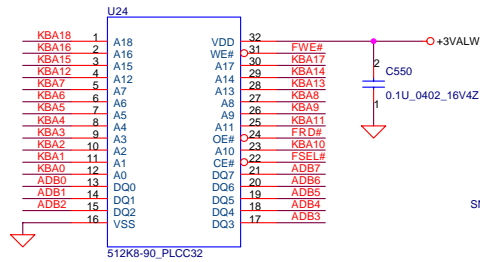
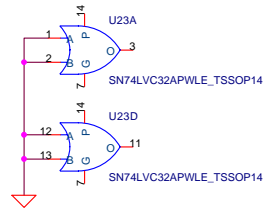
Title		
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INPUT

OUTPUT

<30> ADB[0..7]  ADB[0..7]
 <30> KBA[0..19]  KBA[0..19]

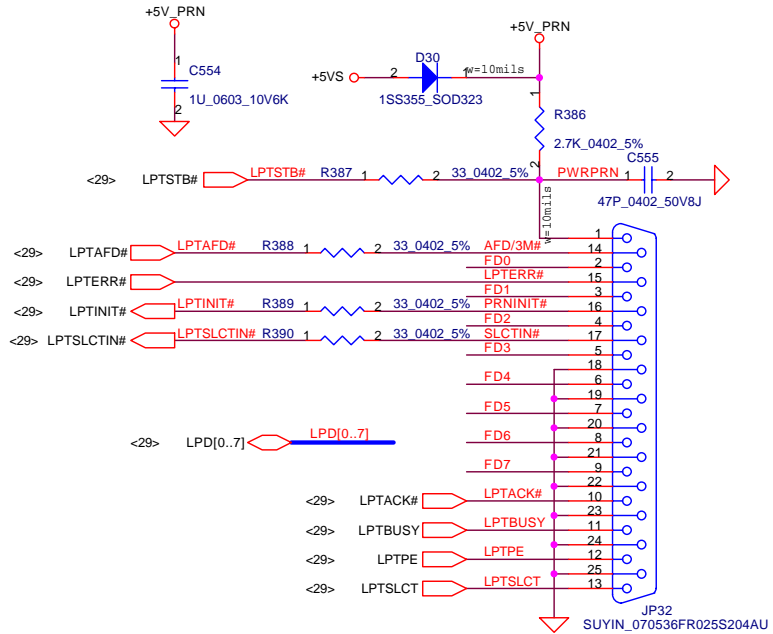


Compal Electronics, Inc.

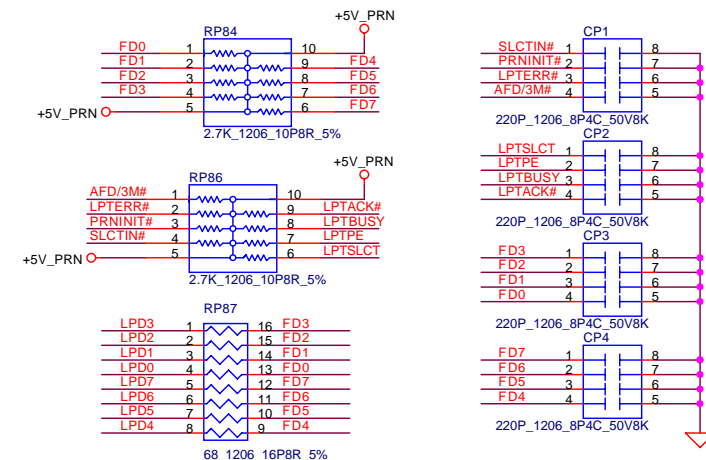
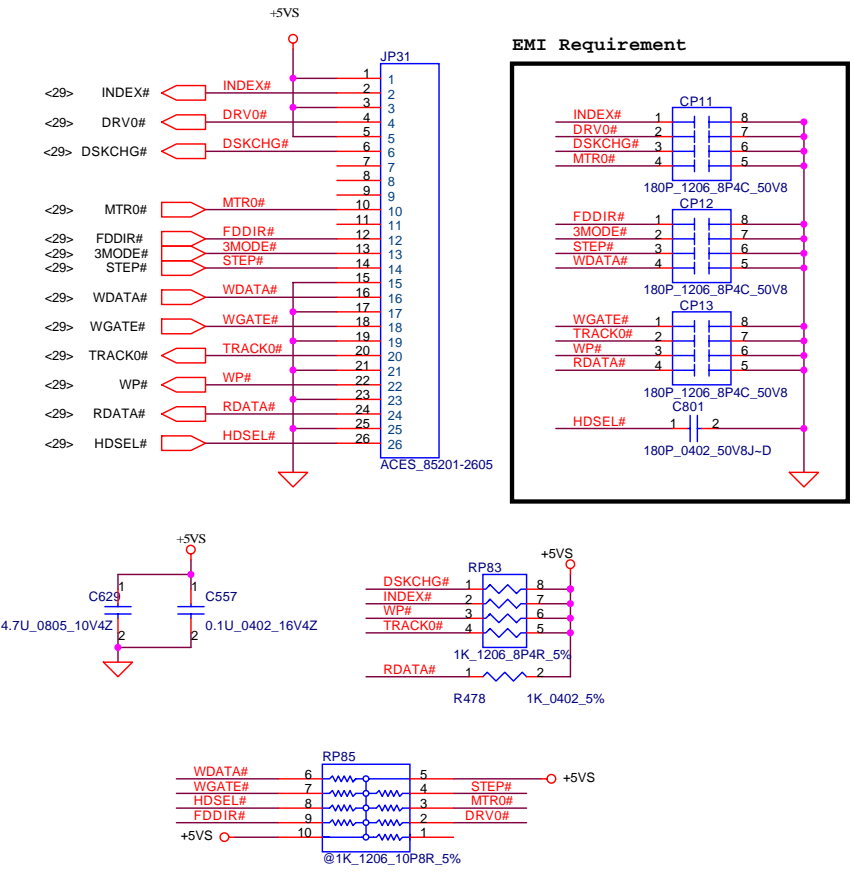
Title			
BIOS & EC I/O Port			
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Parallel Port



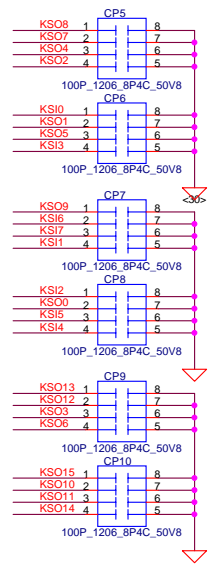
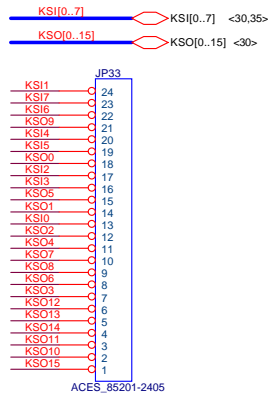
FDD CONN.



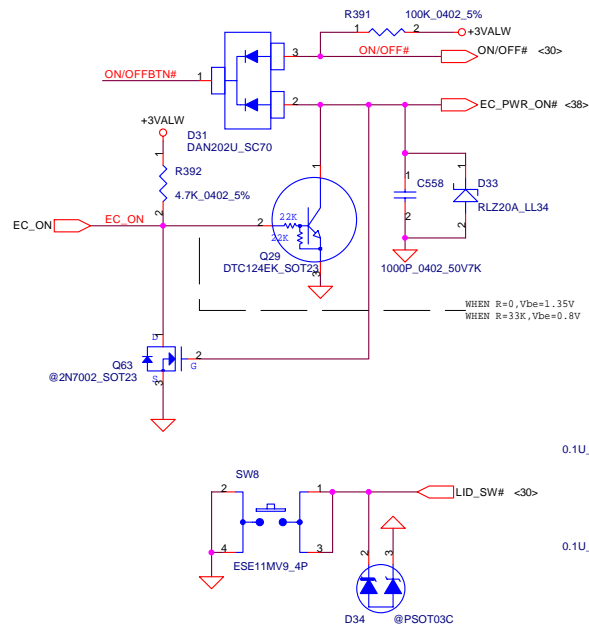
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Title		
Parallel port & FDD Connector		
Size	Document Number	Rev
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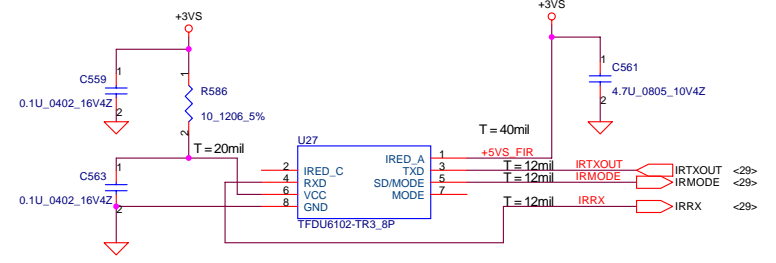
INT_KBD CONN.



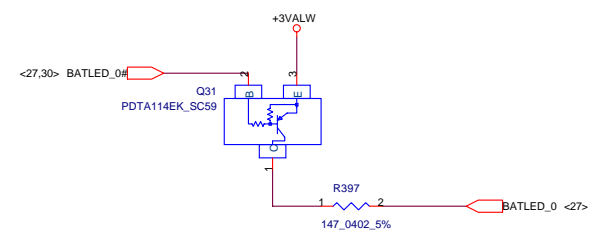
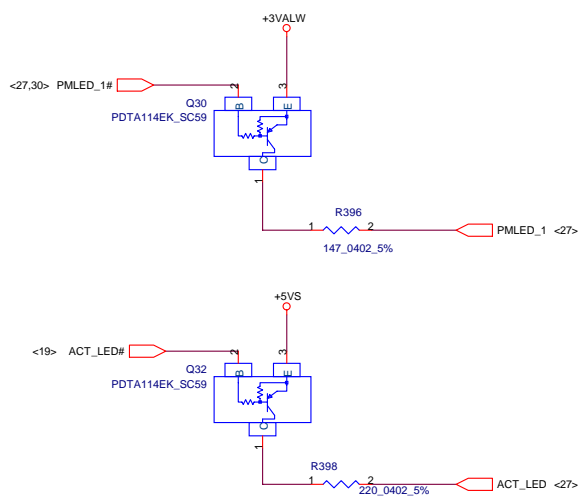
Power BTN



FIR Module

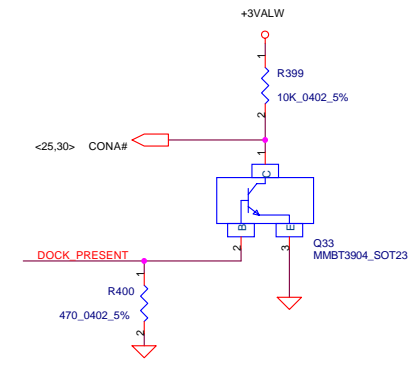
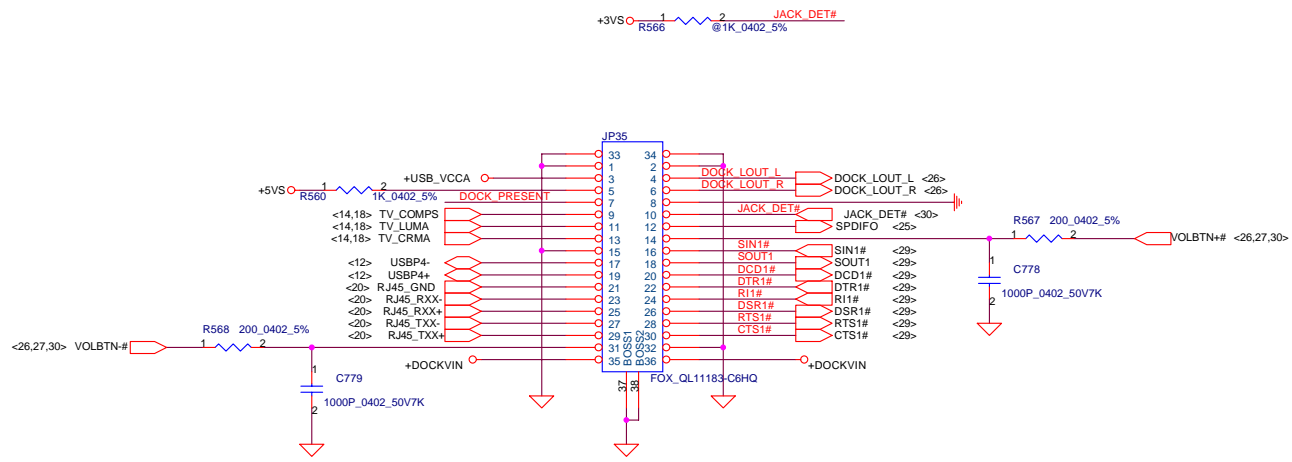


Touch Pad & Status LED Conn.

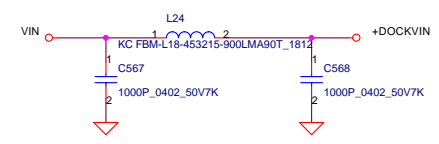
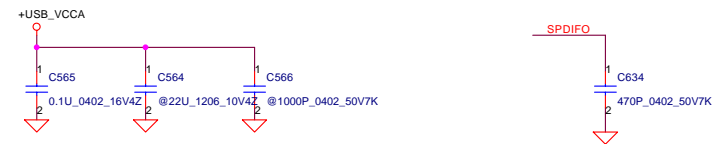
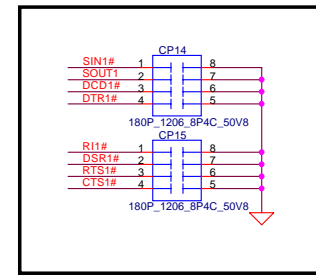


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Compal Electronics, Inc.			
Title KBD,ON/OFF,I/P,LED & FIR			
Size	Document Number	Rev	
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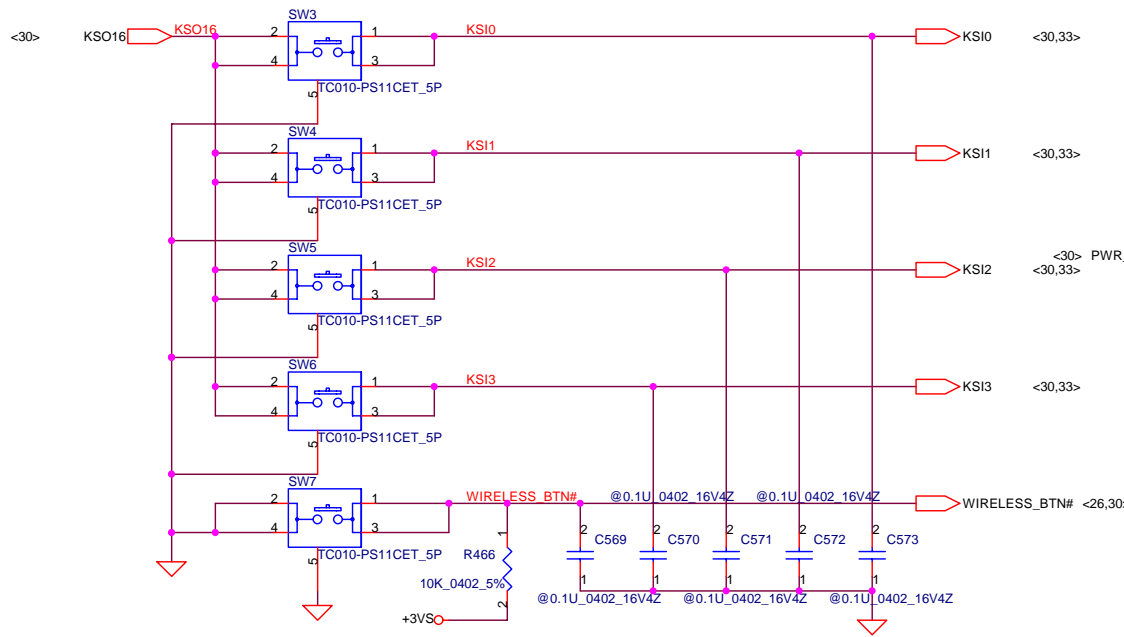


EMI Requirement

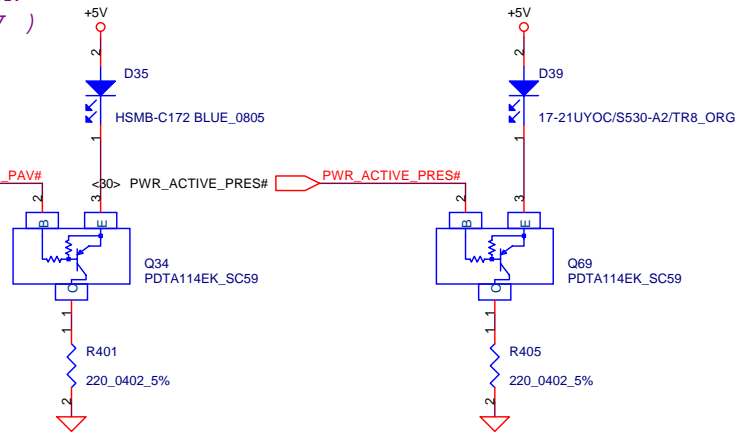


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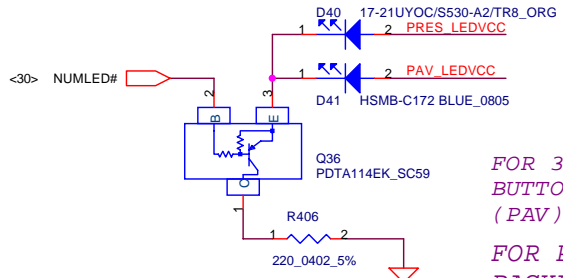
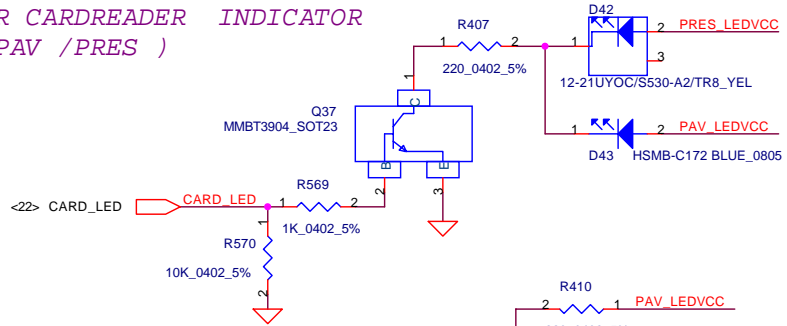
Compal Electronics, Inc.		
Title SPR Connector		
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FOR POWER BUTTON BACKLIGHT (PAV)

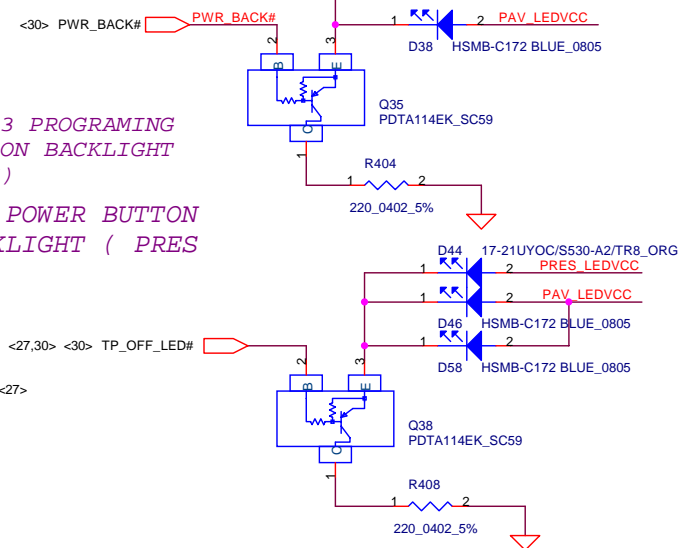


FOR CARDREADER INDICATOR (PAV / PRES)

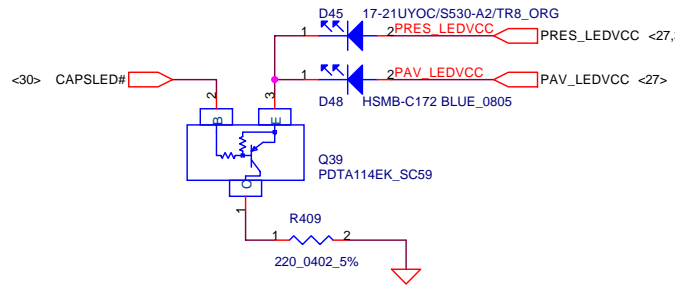
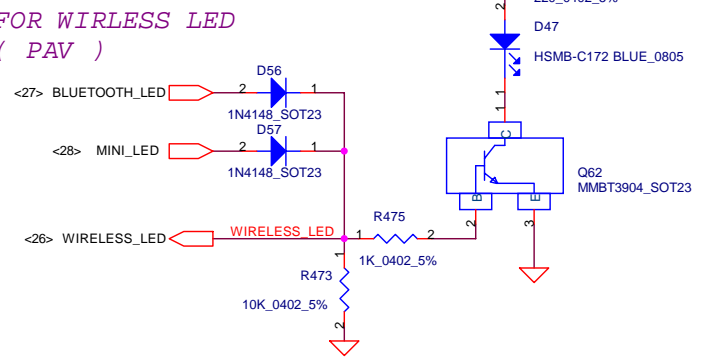


FOR 3 PROGRAMMING BUTTON BACKLIGHT (PAV)

FOR POWER BUTTON BACKLIGHT (PRES)

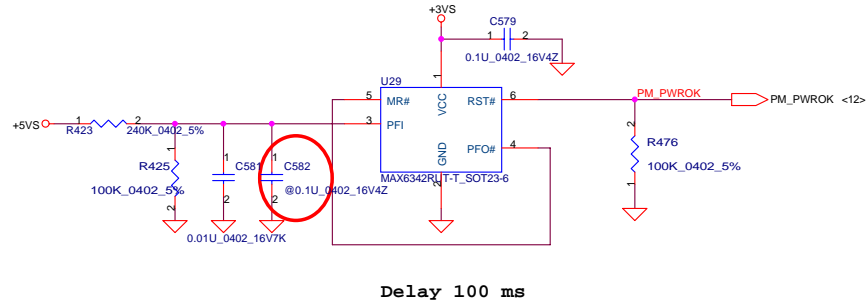
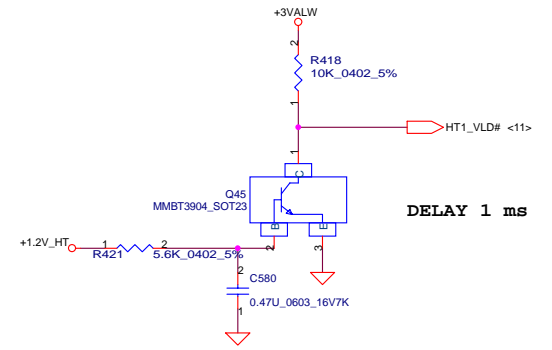
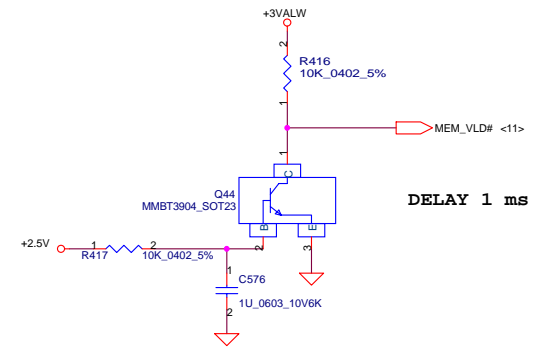
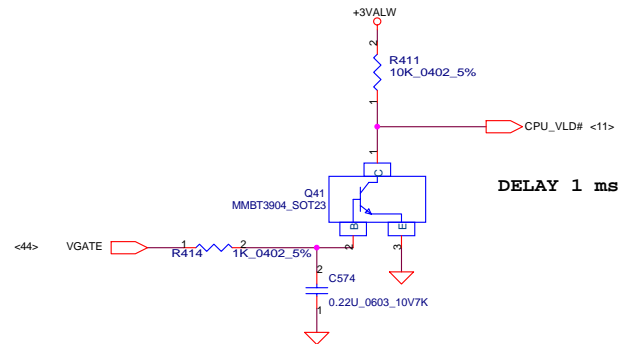
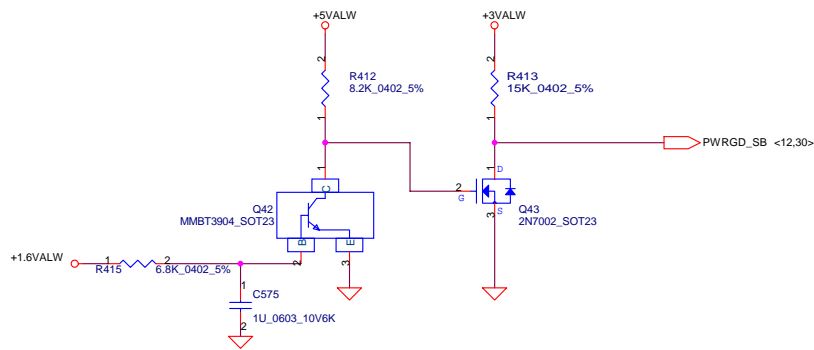


FOR WIRELESS LED (PAV)



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Title LED & Fan Circuit		
Size B	Document Number LA-2392	Rev 0.1
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Delay 100 ms

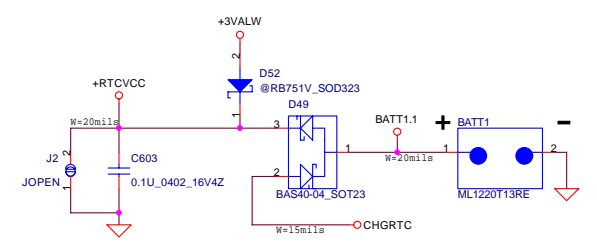
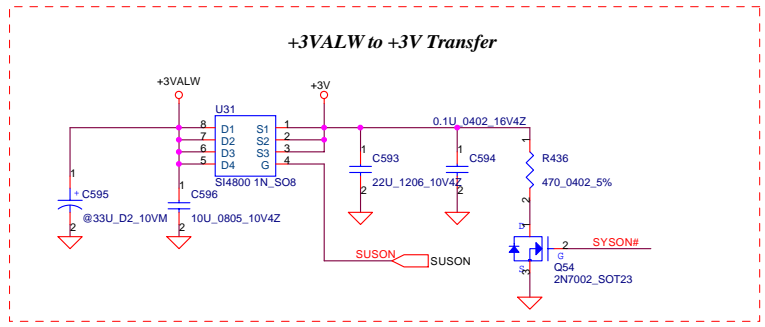
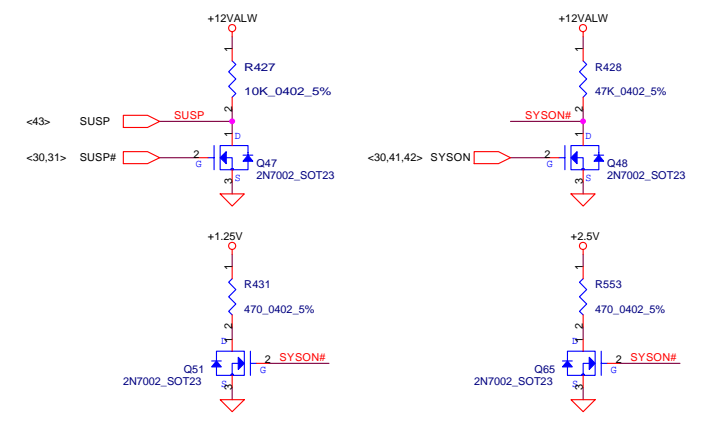
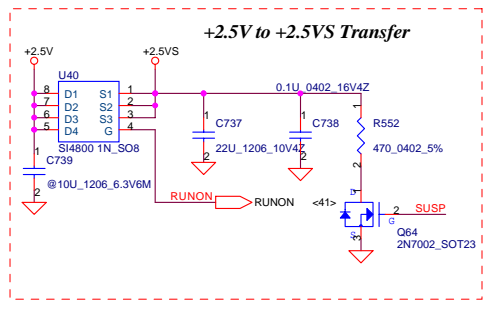
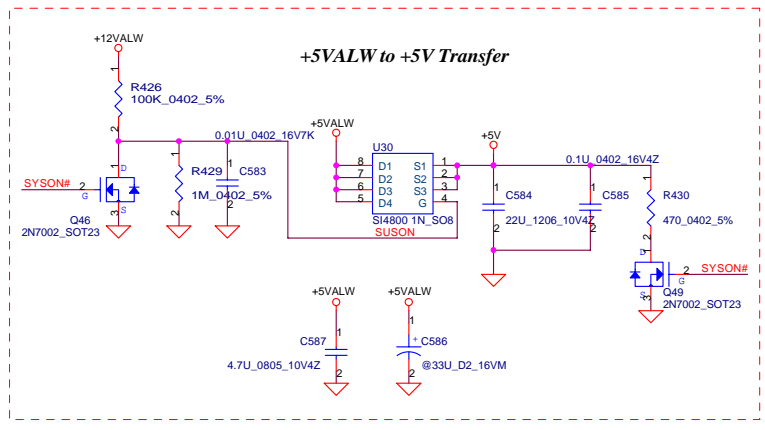
DELAY 1 ms

DELAY 1 ms

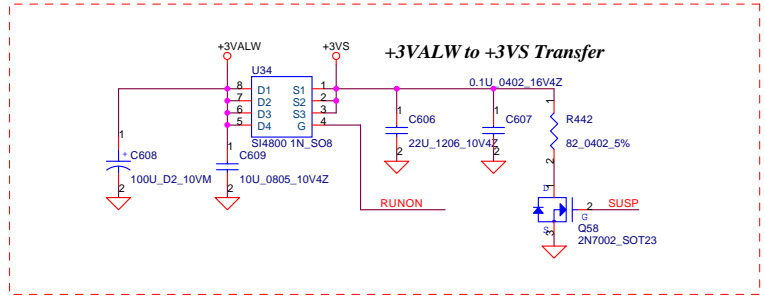
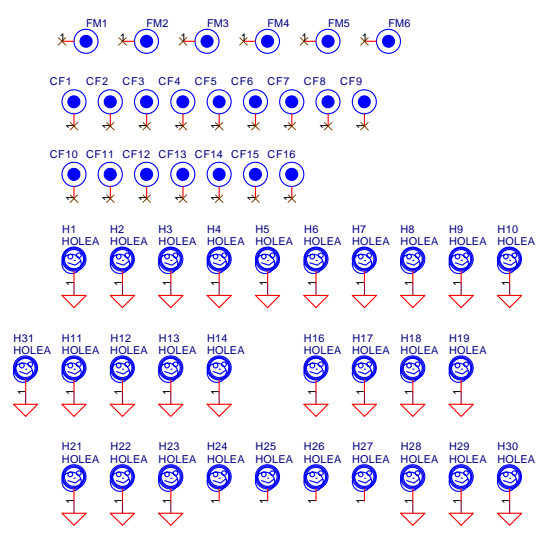
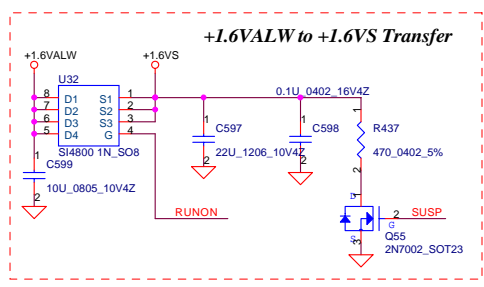
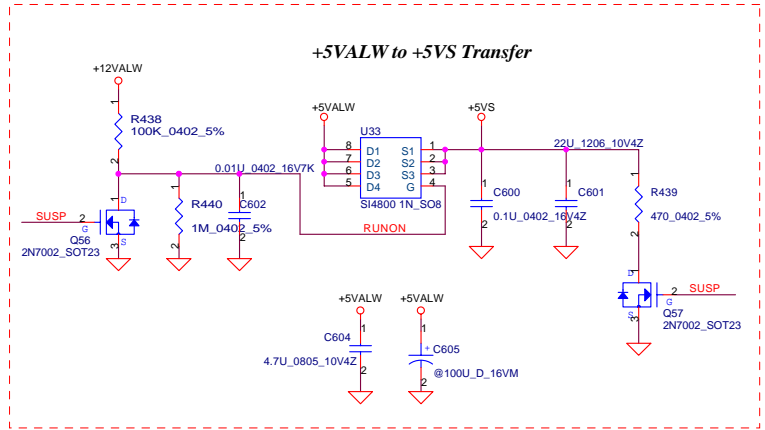
DELAY 1 ms

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Compal Electronics, Inc.		
File	Power OK/Reset Conn.& MUTE Switch	
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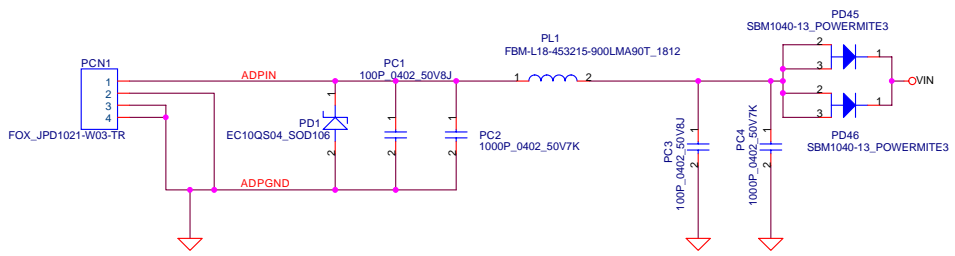


For customer request
they don't wanna
charge RTC

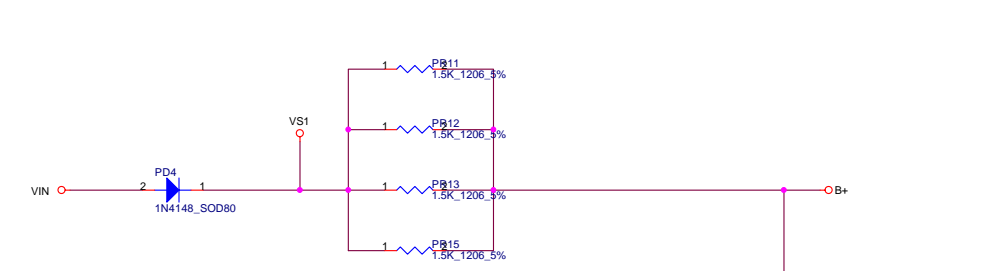
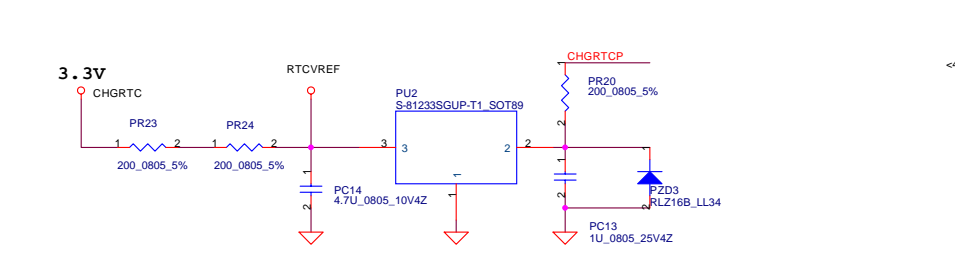
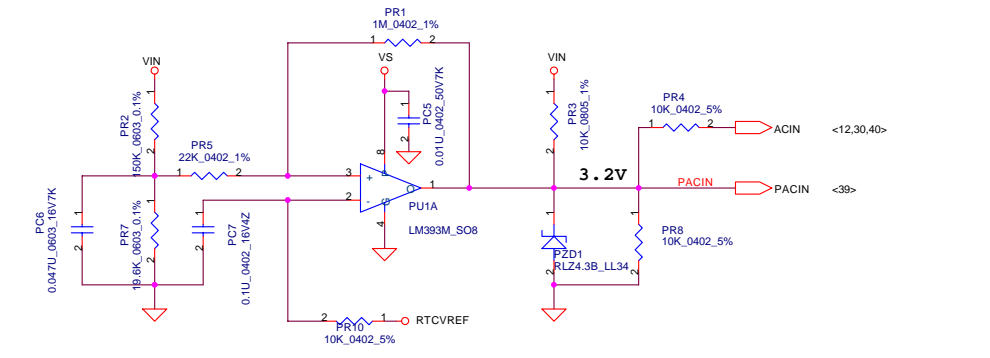
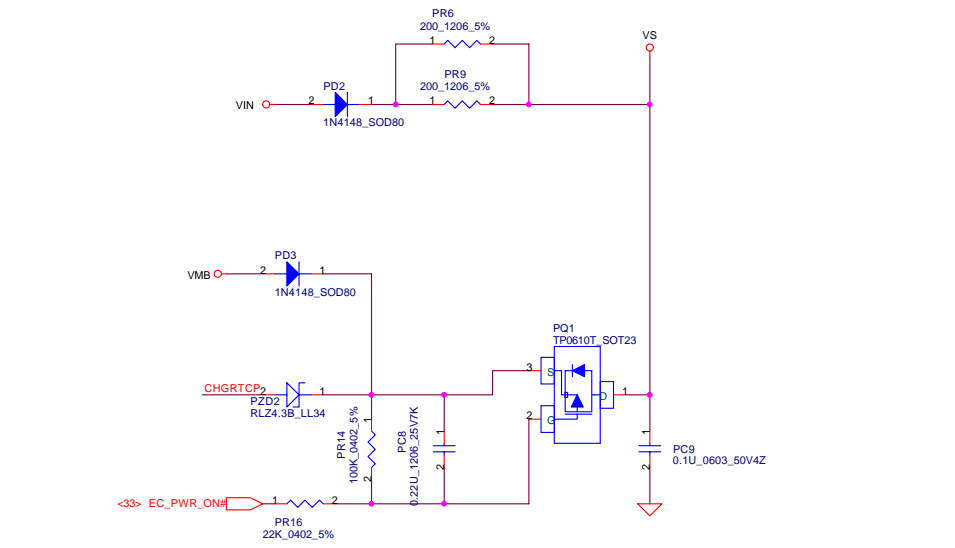


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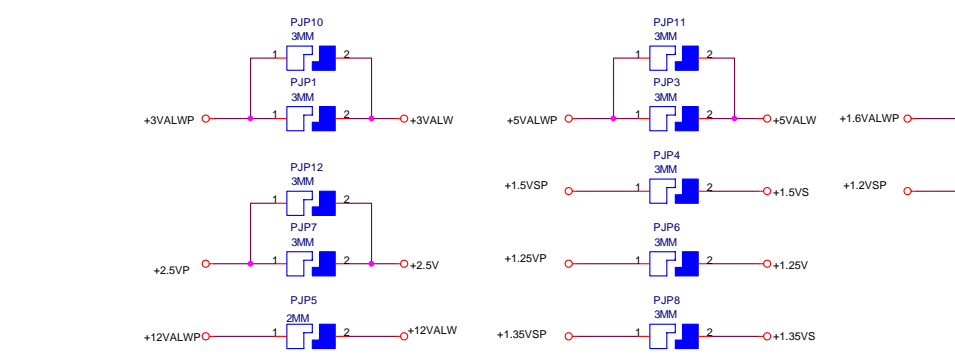
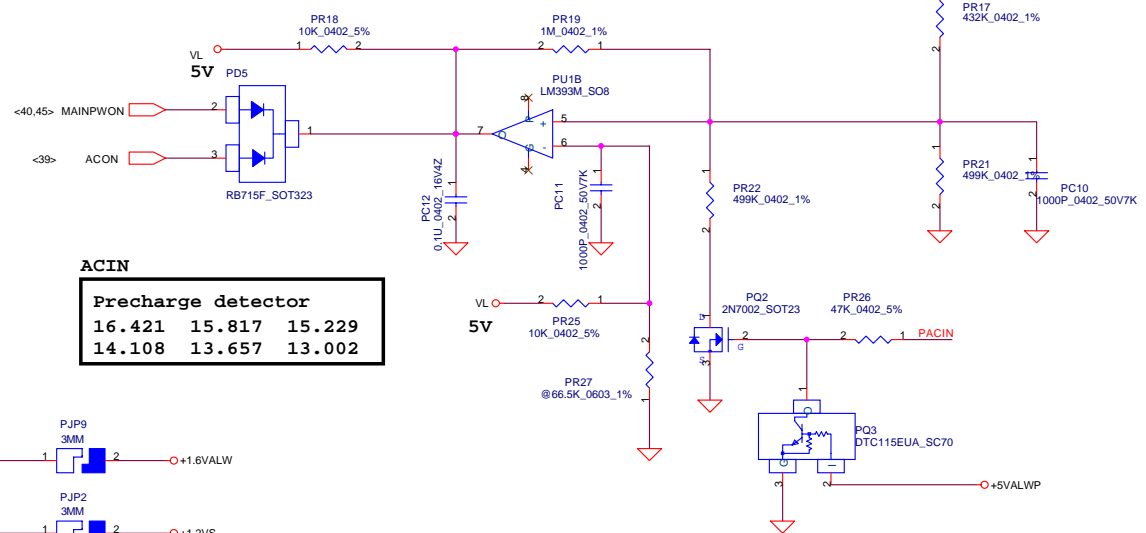
Compal Electronics, Inc.		
File: DC/DC Circuit		
Size: LA-2392	Document Number: LA-2392	Rev: 0.1
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Vin Detector		
18.202	17.841	17.481
17.568	17.210	16.858



ACIN		
16.421	15.817	15.229
14.108	13.657	13.002



Compal Electronics, Inc.		
File	Detector	
Size	Document Number	Rev
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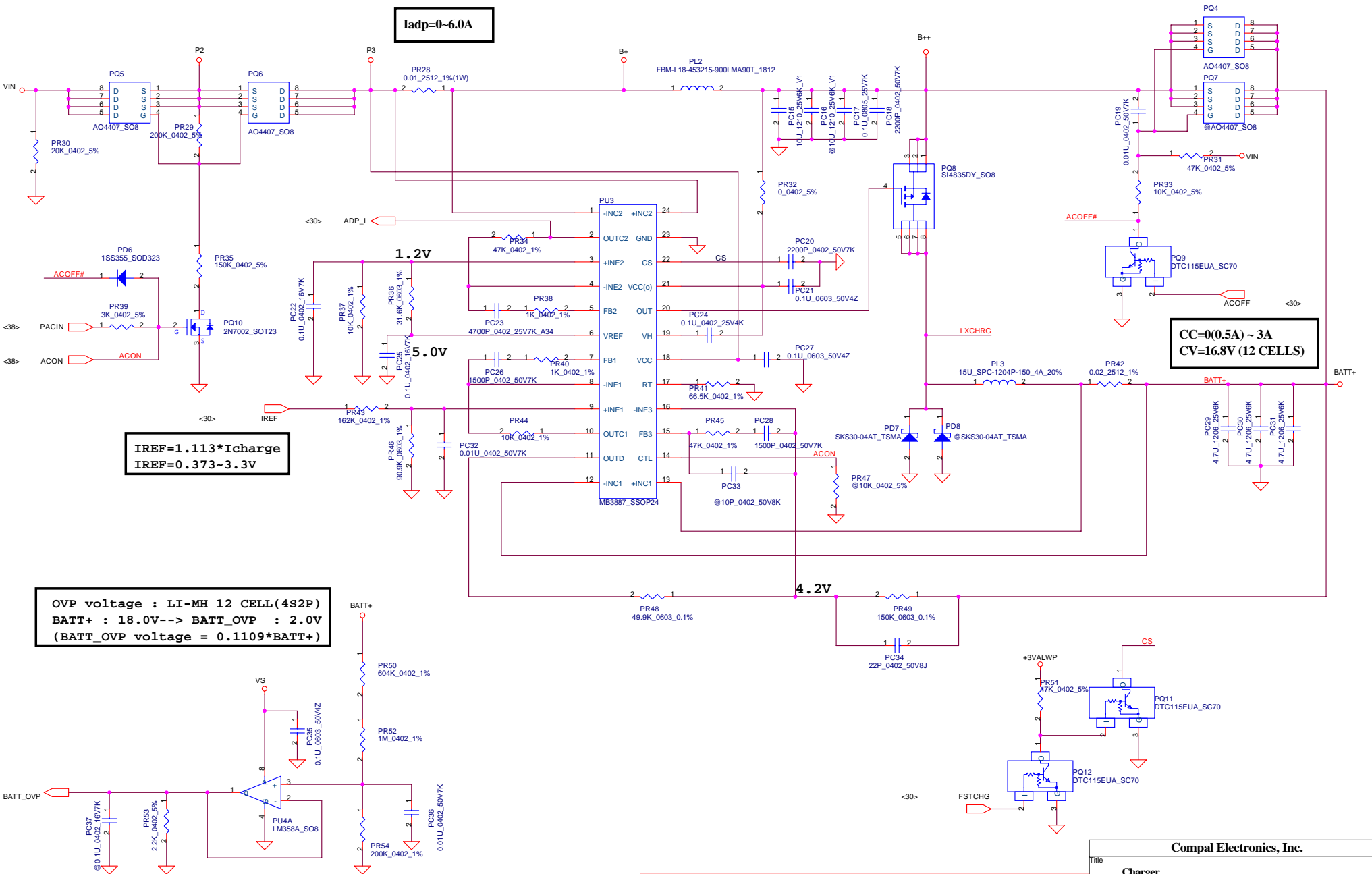
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I_{adp}=0-6.0A

**CC=(0.5A) ~ 3A
CV=16.8V (12 CELLS)**

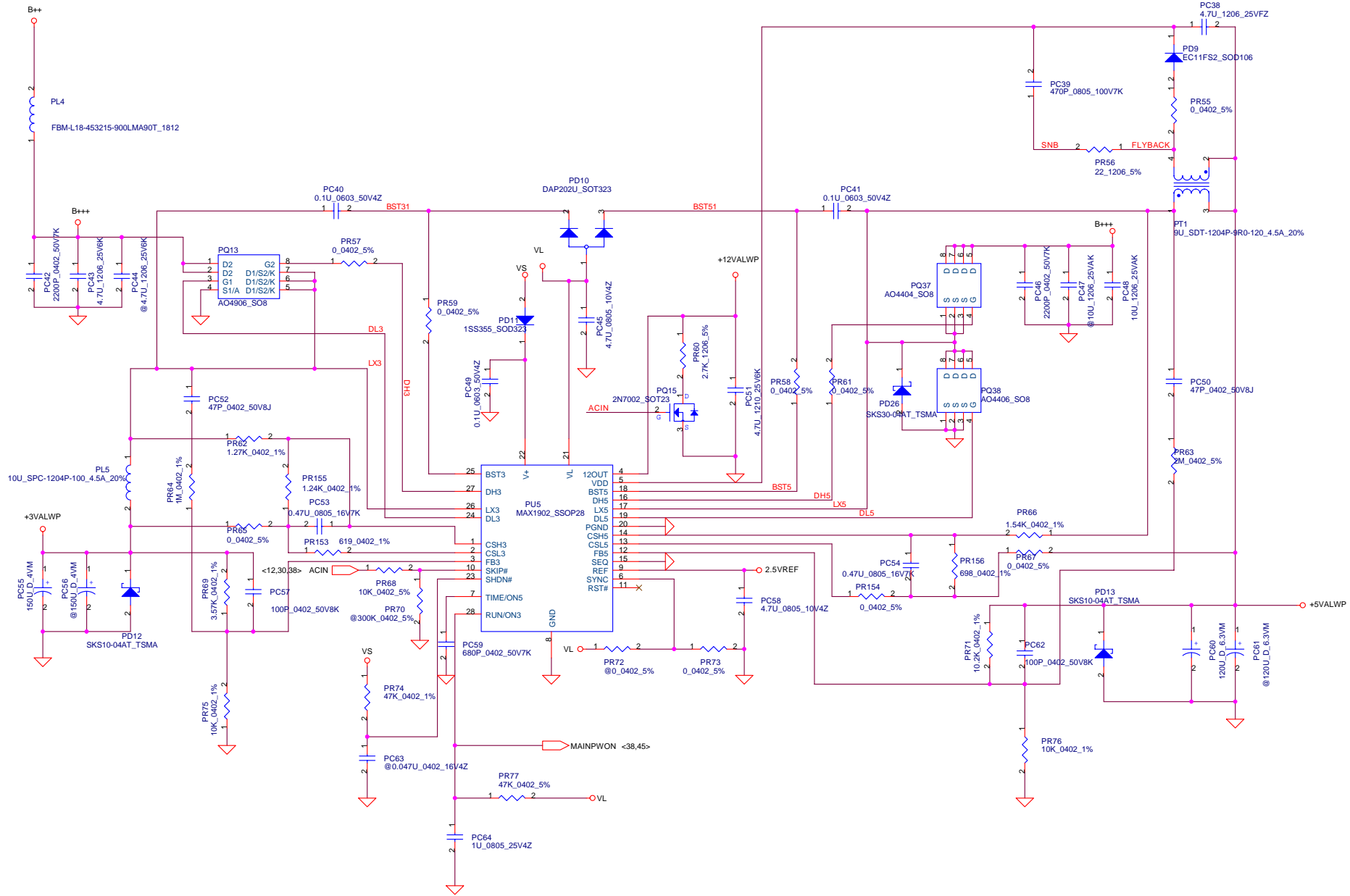
**I_{REF}=1.113*I_{charge}
I_{REF}=0.373~3.3V**

**OVP voltage : LI-MH 12 CELL(4S2P)
BATT+ : 18.0V--> BATT_OVP : 2.0V
(BATT_OVP voltage = 0.1109*BATT+)**



Compal Electronics, Inc.		
Title	Charger	
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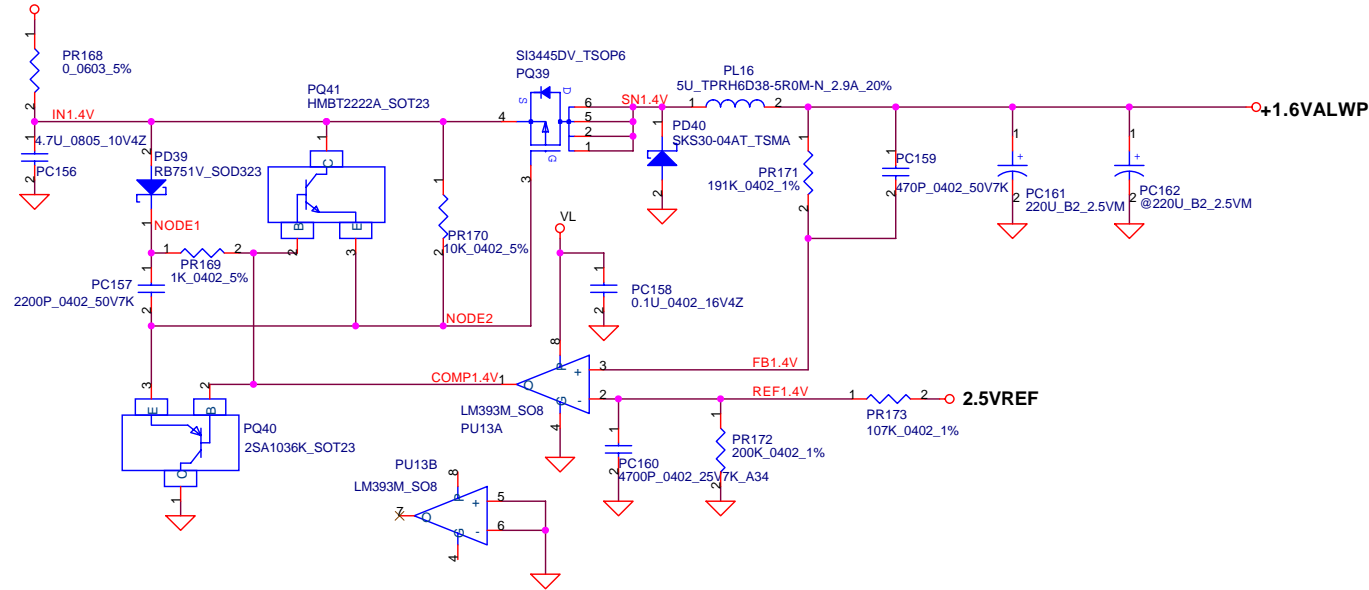
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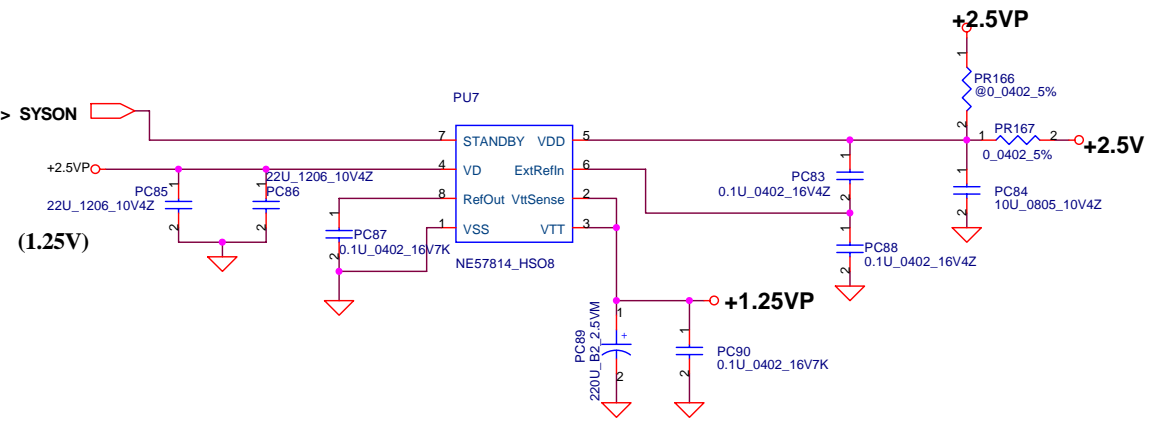
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Compal Electronics, Inc.		
Title	3.3V / 5V / 12V	
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+5VALWP

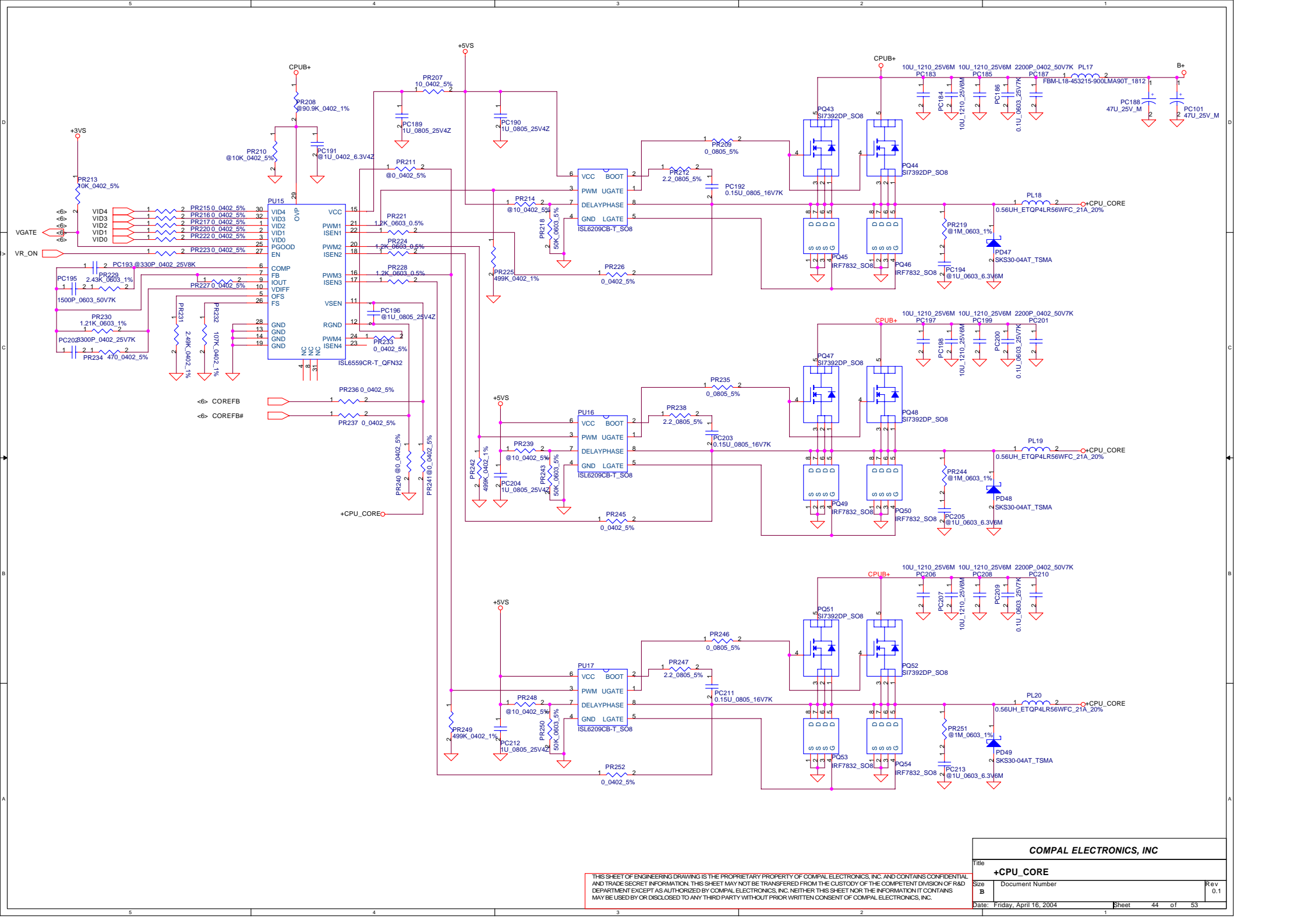


<30,37,41> SYSON



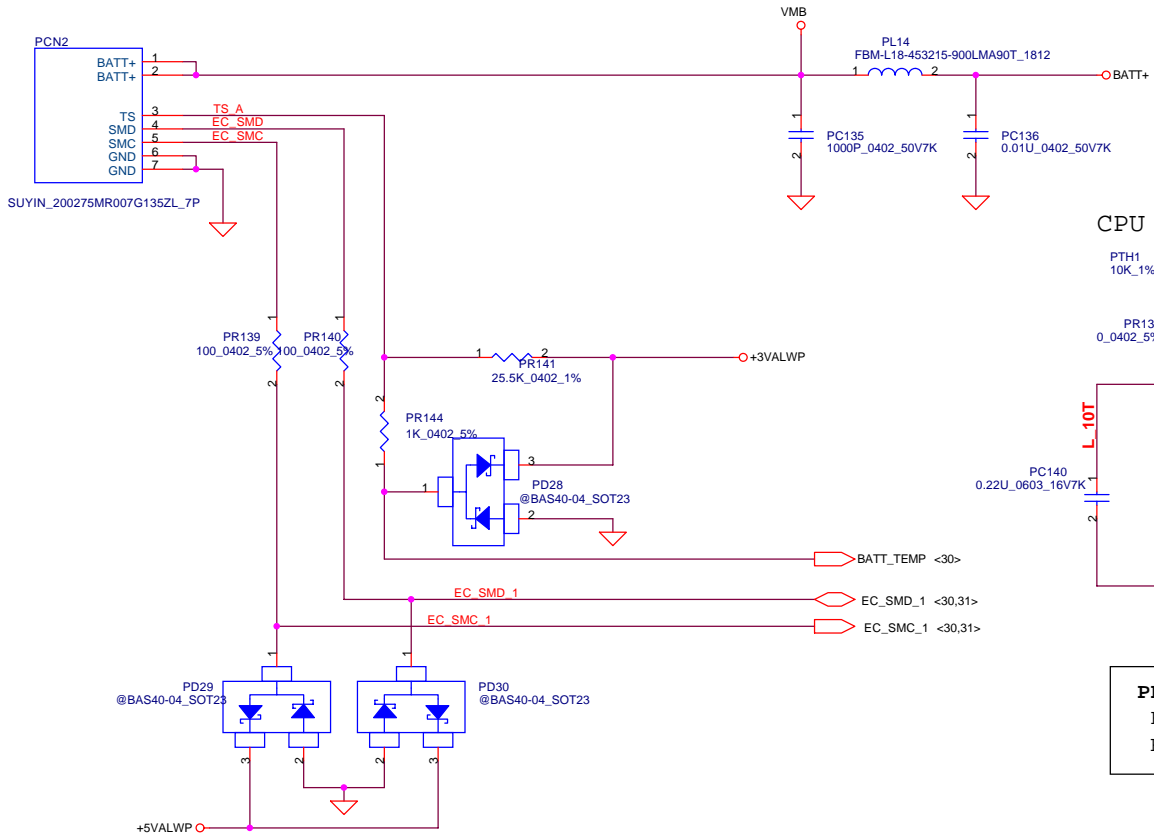
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COMPAL ELECTRONICS, INC		
Title		
+1.6VALWP & +1.25VP		
Size B	Document Number LA-2392	Rev 0.1
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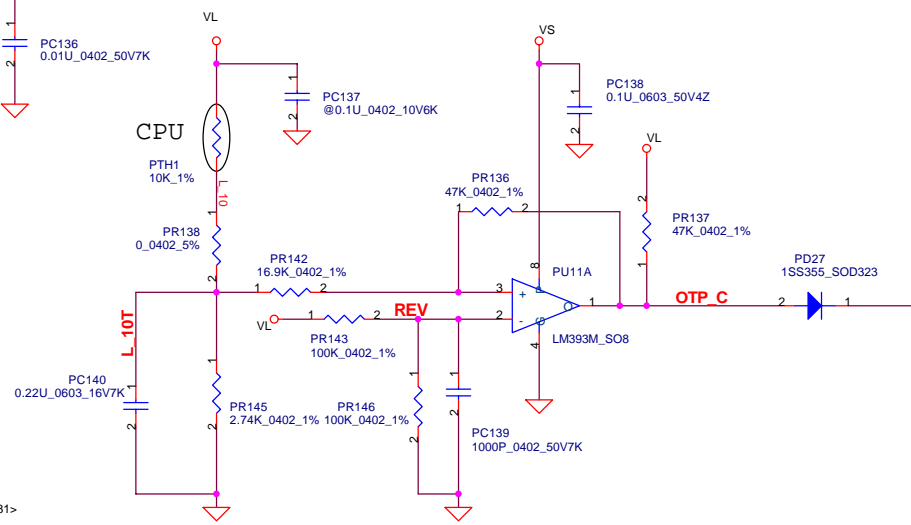


COMPAL ELECTRONICS, INC			
Title			
+CPU_CORE			
Size	Document Number		Rev
B			0.1
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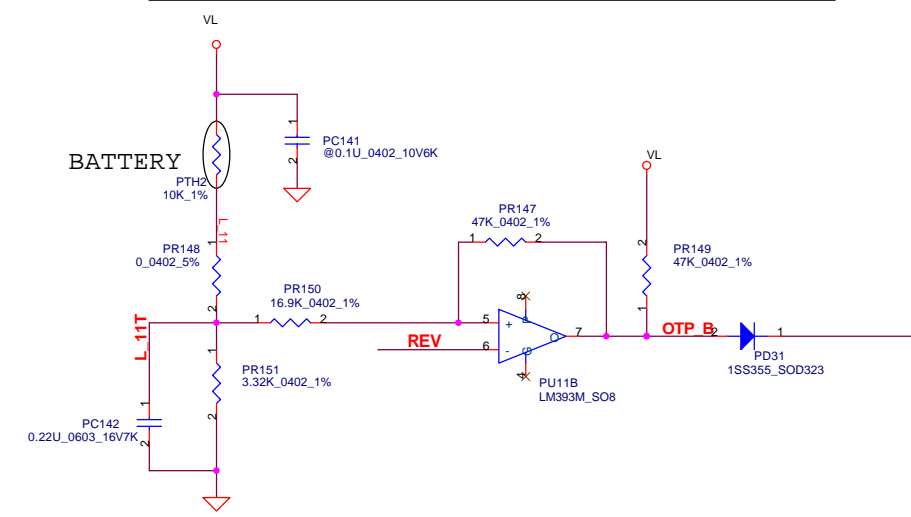
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PH1 under CPU botten side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 84 +/-3 degree C
 Recovery at 45 +/-3 degree C



<38,40> MAINPWON

COMPAL ELECTRONICS, INC		
Title BATTERY CONN / OTP		
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POWER PIR LIST

PHASE			
DB2	page	Reason for change	Modify list
	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174k_0603_1% to 150k_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvment noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202
PV-2	46	Improve the compensation	Change PC168 and PR183
	46	Modify the control signal of MAX1980 (strat the MAX1980 at the same time with MAX1937)	Delete PR180 and add PR208 from pin 13 of MAX1937 to pin 13 of MAX1980

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COMPAL ELECTRONICS, INC			
Title			
PIR			
Size	Document Number	Rev	
	LA-2392	0.1	
Date: Friday, April 16, 2004	Sheet	46	of 53

POWER PIR LIST

PHASE			
DB2	page	Reason for change	Modify list
	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174k_0603_1% to 150k_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvment noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202
PV-2	46	Improve the compensation	Change PC168 and PR183
	46	Modify the control signal of MAX1980 (strat the MAX1980 at the same time with MAX1937)	Delete PR180 and add PR208 from pin 13 of MAX1937 to pin 13 of MAX1980

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COMPAL ELECTRONICS, INC			
Title			
PIR			
Size	Document Number		Rev
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		1	

POWER PIR LIST (2)

PHASE	page	Reason for change	Modify list
	39	Modify charger for using 90W adapter	Change PR34 from 47K_0402_1% To 10K_0402_1% Change PR38 from 1K_0402_1% To 10K_0402_1% Change PR28 from 0.01_2512_1% To 0.012_2512_1% Change PR36 from 31.6K_0603_1% To 37.4K_0603_1% Change DC Jack
	39,40,41	Change capacitor size for cost down	Change PC48, PC72 from 10u_1210_25V to 10u_1206_25V Change PC29, PC30, PC31, PC43, PC67 from 4.7u_1210_25V to 4.7u_1206_25V

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COMPAL ELECTRONICS, INC		
Title		
PWR PIR(2)		
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	1	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Fixed USB 1.1 rising/falling time error	P12	Delete C785, C786, C787, C788, C789, & C790	0.3
2		Fixed TV-out no display	P14	Swap TV_CRMA and TV_COMPS	0.3
3		Prevent PCI1620 latched up	P22	Reserve G_RST# to pin U37.C11	0.3
4		Design change (solve for HR60 audio issue)	P26	Move two load resistors from sub-board to M/B and swap JP17.2 and JP17.3	0.3
5		Supported wake up from TP	P27	Change TP connector JP26's power pin from +5VS to +5V	0.3
6		EMI required (solve for 48 MHz noise from FDD connector)	P32	Add CP11, CP12, CP13, and C801	0.3
7		Design change (TFDU6102 design guide)	P33	Delete C560 and C562 & add R586 Change C561 from 10uf to 4.7uf	0.3
8		EMI required (solve for 48 MHz noise from serial port)	P34	Add CP14, and CP15	0.3
9		ID required (for Pavillion)	P35	Add D58	0.3
10		EMI required	P25	Add L38, and L39	0.3
11		Add bypass cap. to solve for AC97 link cross a split plane	P27	Add C802, C803, C804, C805, and C806	0.3
12		Design change (reserve space for power placement and no need too many caps.)	P07	Delete C75, and C88	0.3
13		RealTech 8101L design guide	P20	Change R194 to 5.6K +/- 1%	0.3
14		Solve for SPDIF no output	P34	Delete C634	0.3
15		CPU_CLK is current drive from CK8. So, delete damping resistors.	P11	Change R69, and R70 from 15 ohm to 0 ohm	0.3
16		Solve for burst frequency error	P14	Change C642, and C643 from 18 pF to 22 pF	0.3
17		Solve for chrominance and burst level	P18	Change L11, L12, and L13 to 1.8uH	0.3

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Compal Electronics, Inc.		
Title	P.I.R HISTORY	
Size	Document Number	Rev
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		AMD change Tdiode spec up to 127 degree	P4	Change U3 from MAX6649 to ADM1032	0.4
2		Support wake from Lan	P20	Populate R188	0.4
3		To avoid PCI 1620 unknow action	P22	Reserve R591	0.4
4		To restrain audio noise	P25	Change R267 pull up to +5VAMP_CODEEC, and delete C626	0.4
5		USB_OC# high should be between 2.5V to 5.5V	P27	Change R310 and R315 to 10K / R314 and R319 to 20K	0.4
6		To detect FIR	P29	Add R592 and R593	0.4
7		TP should be pull up to +5V	P30	RP80 pull up to +5V	0.4
8		In order to compatible with NS97551 -- changing pin87 ~ 90 to GPIO	P30	BID routed from pin88 to pin82	0.4
9		In order to compatible with NS97551 -- removing +RTCVCC	P30	Add R594 and R595	0.4
10		To prevent noise generated from FAN to +5VS cause audio noise while shut down	P4	Delete D1 and D3 / add C3, C8, C612, and C614	0.4
11		Solve for PCI 1620 working abnormal -- fine tune G_RST# timing	P22	Populate R587, delete R225, C410	0.4
12		Double mount issue, already exist at audio board.	P30	Delete D28 and D29	0.4
13		Fast power on for battery only	P33	Change R392 from 100K to 4.7K	0.4
14		Presario LED color should be amber	P35	Change D39, D40, D42, D44, and D45 from XX_GRN to XX_ORG	0.4
15		To develop SI 9182 max effect	P25	Change C438 from 0.01UF to 0.1UF	0.4
16		For EMI	P26	Add L40, L41, L42, and L43 / delete C473, C474, C475, and C476	0.4
17		For VGA HSYNC/VSYNC average peak to peak issue	P18	Add R159 and R160	0.4
18		For 512MB non-JEDEC module (16 chips)	P9	Change RP42, RP46, and R481 from 68 Ohm to 47 Ohm	0.4

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		To use the same source as HR60	P4	Change U3 footprint to SOP8	0.5
2		To reset CK8 while boot up control by EC	P12	Add R97 to link EC_RSMRST# and PWRGD_SB	0.5
3		For EMI	P15	Change C648, C672, C685, C696, C699, C763, and C656 to 1000P Change C651, C673, C686, C697, C700, C764, C654, C733, C710, C730, C706, and C724 to 10P	0.5
4		To solve voltage level of HSYNC and VSYNC is over spec	P18	Add U46 and U47, and R596, R597, and R598 on CRT_HSYNC and CRT_VSYNC	0.5
5		Solve for data lost while transfer data from LAN	P20	Change U9 from NS0013 to NS0019	0.5
6		TI recommendation --- avoid unknow state while initiate	P22	Populate R591	0.5
7		Mechanical restricted area	P25	R263 and R264 change footprint to R_0402	0.5
8		For EMI	P25	L39 and R293 change to CHB1608U301_0402	0.5
9		For EMI	P26	L40, L41, L42, and L43 change to KC FBM-L11-201209-221LMAT_0805	0.5
10		nVIDIA recommendation for WOR	P27	Add U48, C807, R599, and R600	0.5
11		Due to MD_SPK is no longer use, so prevent input pin floating.	P25	Delete R287 and change R288 to 0_0402_5%. Also add C808.	0.5
12		Due to USB data has leakage problem, so need to delay USB_VCC power up timing controlled by EC to solve for unknow device while power on with battery only.	P27 P30	Wired R368.2 to U18.4 and U19.4	1.0

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Cost Down	P4	Change C1, C4, C8, C330, C339, C447, C596, C599, C609 from 10U_1206_10V4Z to 10U_0805_10V4Z	0.5C
2		Cost Down	P6	Delete C15 (330U_D_2VM_R15), Add C810 (330U_6.3V_M)	0.5C
3		Cost Down	P12 P25 P14 P26 P15 P27 P18 P29 P20 P30 P22 P31	Delete 0_0402_5% -- R97, R105, R108, R282, R288, R289, R300, R312, R313, R317, R318, R320, R321, R326, R327, R359, R368, R375, R377, R381, R393, R469, R587, R597, R598, R219 Delete 0_0603_5% -- R462, L26, L27, L30, L32, L33, L34 Delete 0_0805_5% -- R459, R465, L16, L20, Delete 0_1206_5% -- R394,	0.5C
4		Cost Down (VBIOS can cover it)	P14	Delete R502 and R503	0.5C
6		Improve reliability	P18	Add C811	0.5C
7		Cost Down	P18	Change D12 from RB491D_SOT23 to RB411D_SOT23	0.5C
8		Cost Down (RTL8101L integrate those parts)	P20	Delete Q22, C353, C354, C358, C359 and add L44	0.5C
9		Cost Down	P21	Delete C376, C378, C382, C383, C384	0.5C
10		Cost Down (EC can control it)	P22	Delete D16 and R218	0.5C
11		Internal pull up	P23	Delete R227	0.5C
12		Cost Down	P23	Delete C423 and C631	0.5C
13		Cost Down (No reserve PCI1520)	P24	Delete R231, R232, R240, R241, R242, R243, R244, R245, R256, R259, R260, RP71, RP71, RP73, RP74, RP75, RP76, RP77, C430	0.5C
14		Cost Down	P25	Delete C435, C436, C808, and add R604	0.5C
15		Cost Down	P28	Delete C512, C515, C522, C524	0.5C
16		Cost Down	P29	Delete C525, C529	0.5C
17		Cost Down	P30	Change U21 from 87591L to 97551, delete C539 and C543, add R603, D59, C627	0.5C
19		Cost Down	P43	Delete C564, C566	0.5C

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