

888Z3 LA-1044 REV2.0 SCHEMATIC DOCUMENT

Intel (Tualatin) with VIA (VT8606-TwisterT + VT8231)

BOM 記號

LN_ SKU W/SS 要打
 L@ SKU WO/SS 要打
 1394@ SKU W/1394 要打
 TV@ SKU W/TVOUT 要打
 DJ@ SKU W/AUDIO DJ 要打
 DJN_ SKU WO/AUDIO DJ 要打
 EQ@ SKU W/EQ 要打
 EQN_ SKU WO/EQ 要打
 F@ SKU W/FPR 要打
 FN_ SKU WO/FPR 要打
 SPR@ SKU W/DOCKING CONN. 要打

鋼版不開:

JOPEN1
 JOPEN8
 JOPEN9
 JOPEN10

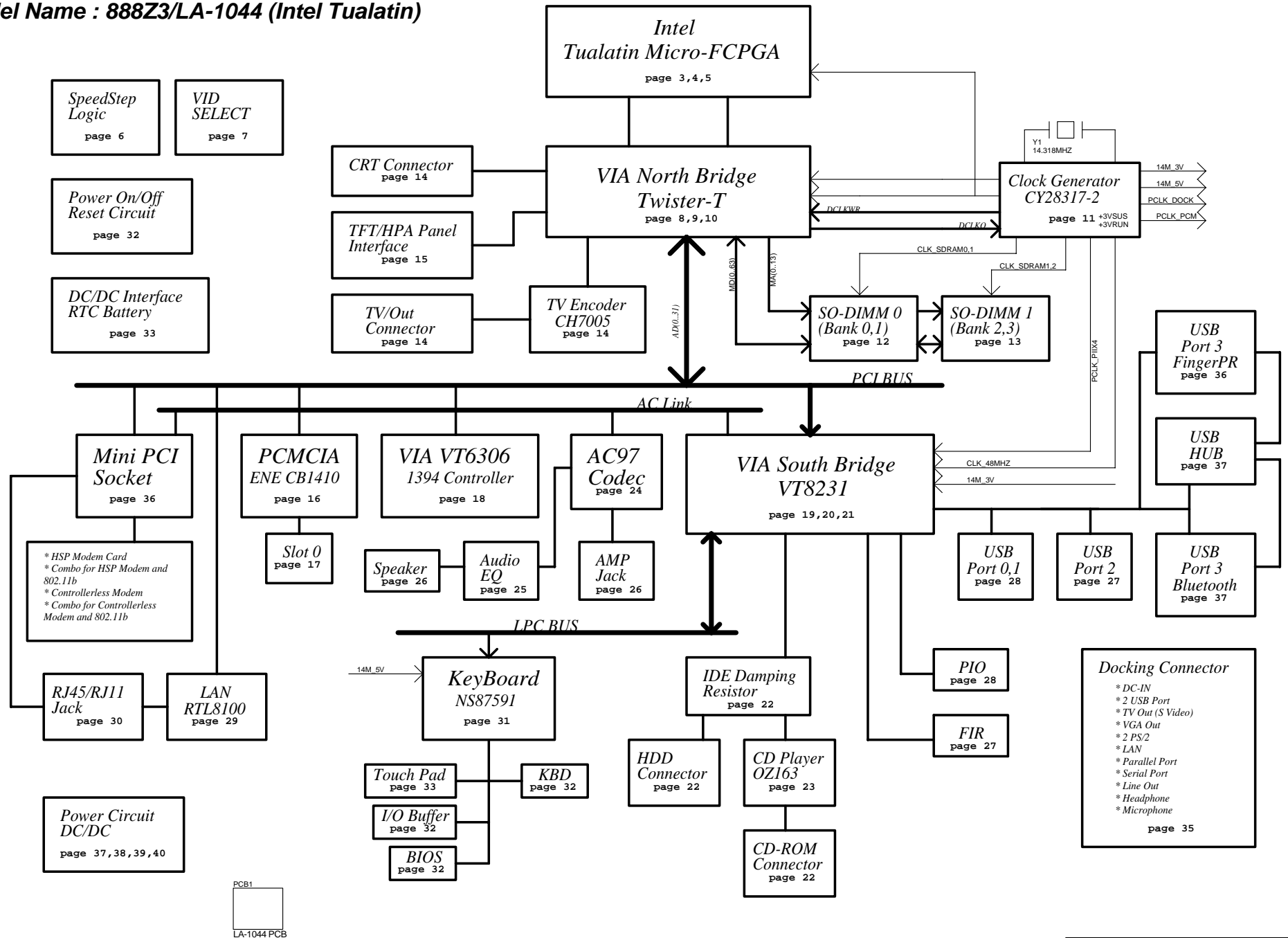
PCB Layer
 Structure:

TOP
 GND1
 IN1
 GND2
 VCC
 IN2
 GND3
 BOT

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Size B	Document Number 401196	Rev 2A
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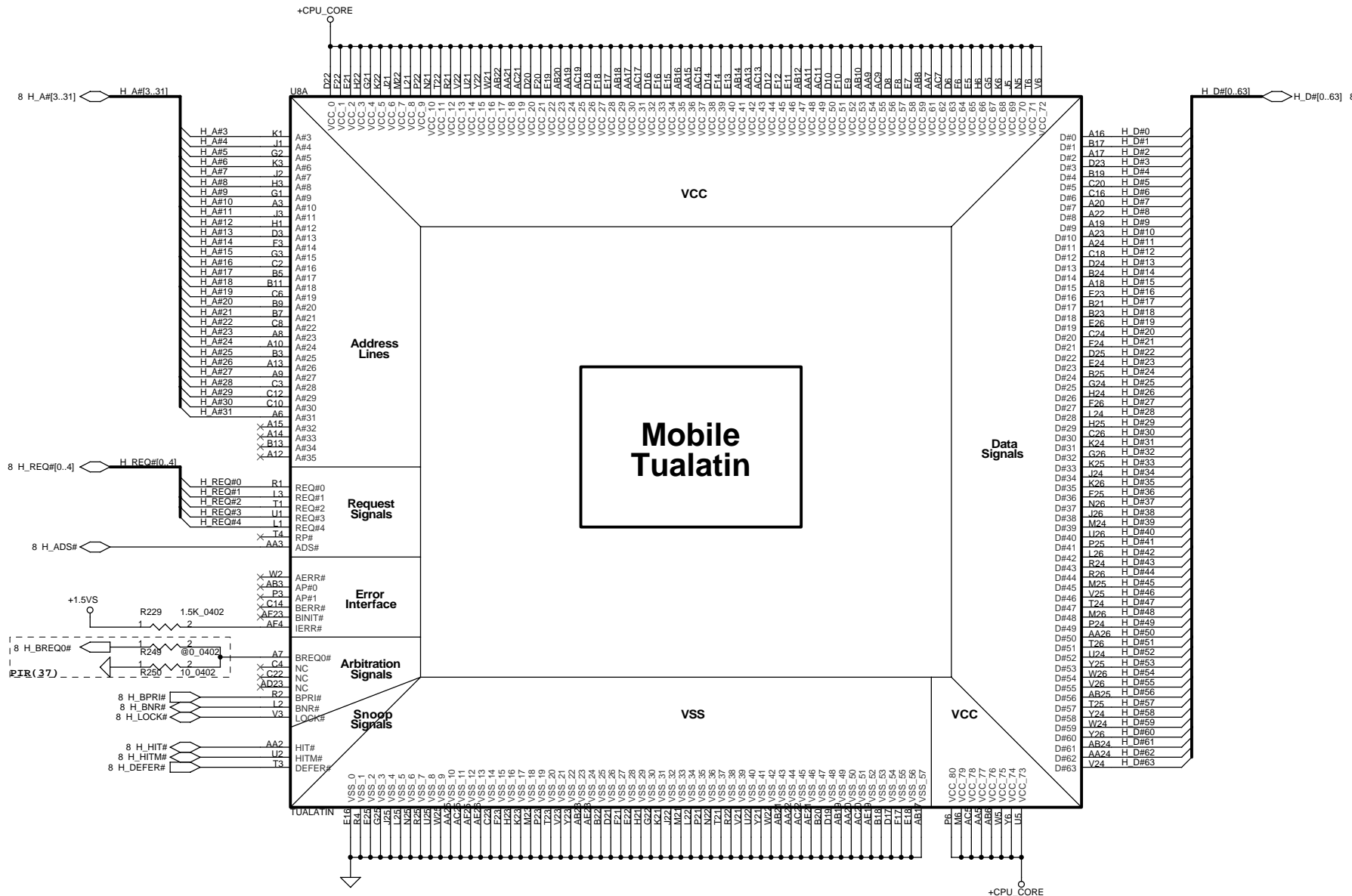
Model Name : 888Z3/LA-1044 (Intel Tualatin)



PCB1
LA-1044 PCB

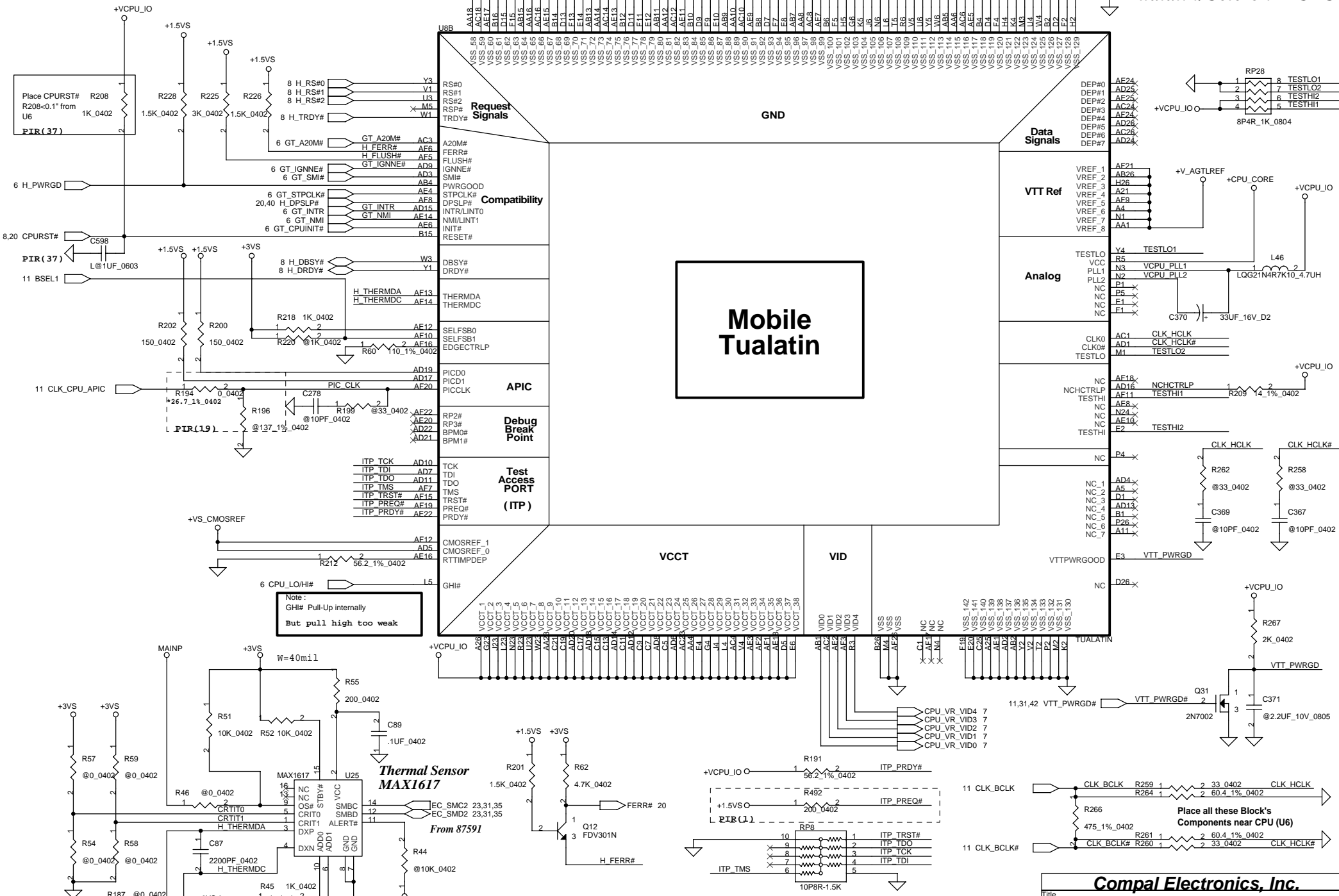
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Mobile Tualatin

Note:
GH# Pull-up internally
But pull high too weak

Thermal Sensor MAX1617

From 87591

Address:1001_110X

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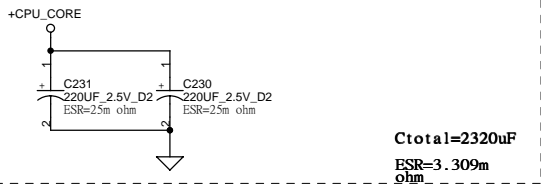
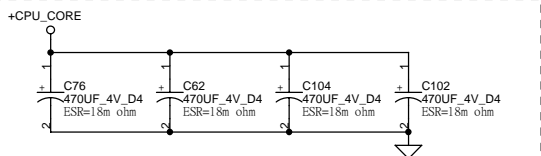
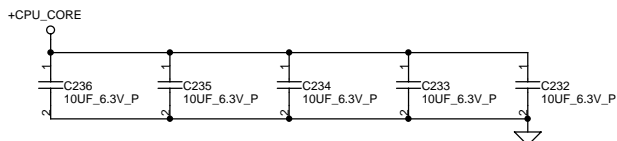
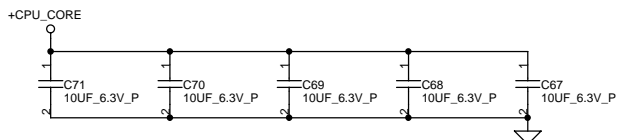
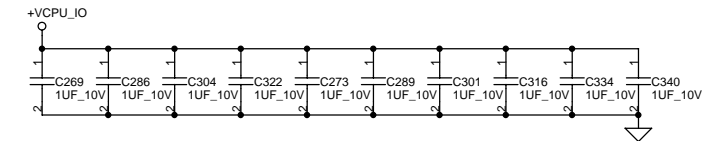
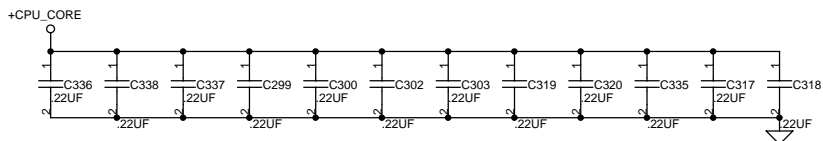
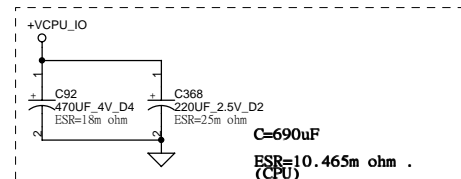
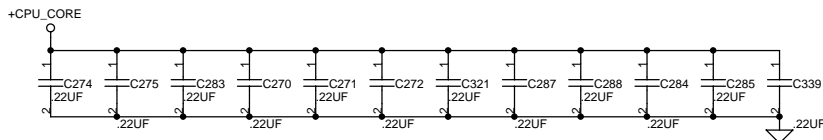
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Customer		SCHEMATIC, M/B LA-1044	
Document Number	401196	Rev	2A
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Layout note :

Place close to CPU, Use 2-3 vias per PAD.
 Place 0.22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

Layout note :

Place close to CPU,
 Use 2 vias per PAD.



Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	QS (MP)	
0	0	1	1	1	1.40V		300 MHz & 0.95V : 4.11A
0	1	1	0	0	1.15V		500 MHz & 1.05V : 6.38A
							533 MHz & 1.05V : 6.61A
							700 MHz & 1.10V : 8.40A
							733 MHz & 1.15V : 9.39A
							800 MHz & 1.15V : 9.84A
							1000 MHz & 1.40V : 16.83A
							1066 MHz & 1.40V : 17.46A
							1133 MHz & 1.40V : 18.11A

EMTS updated by the note released on April 27 , 2001.

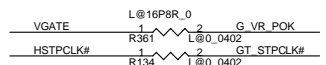
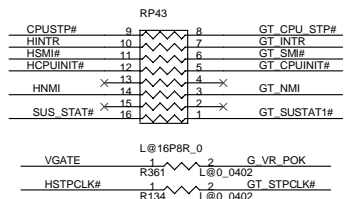
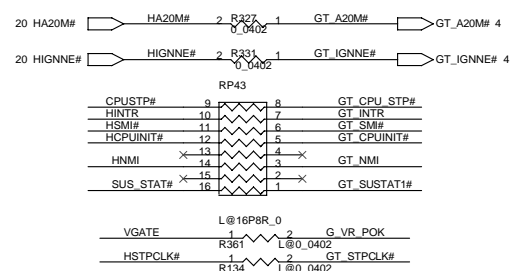
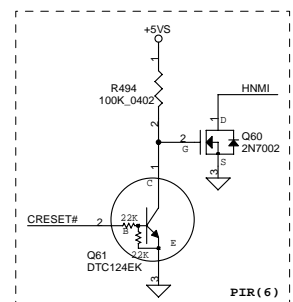
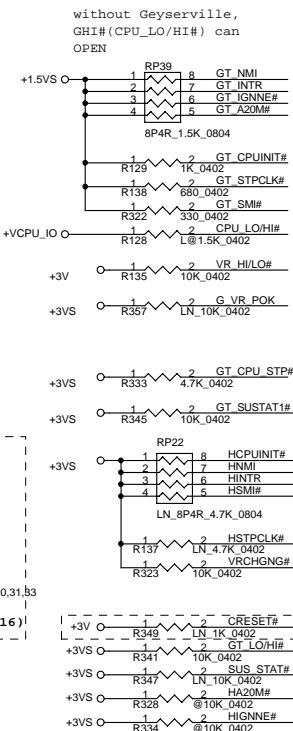
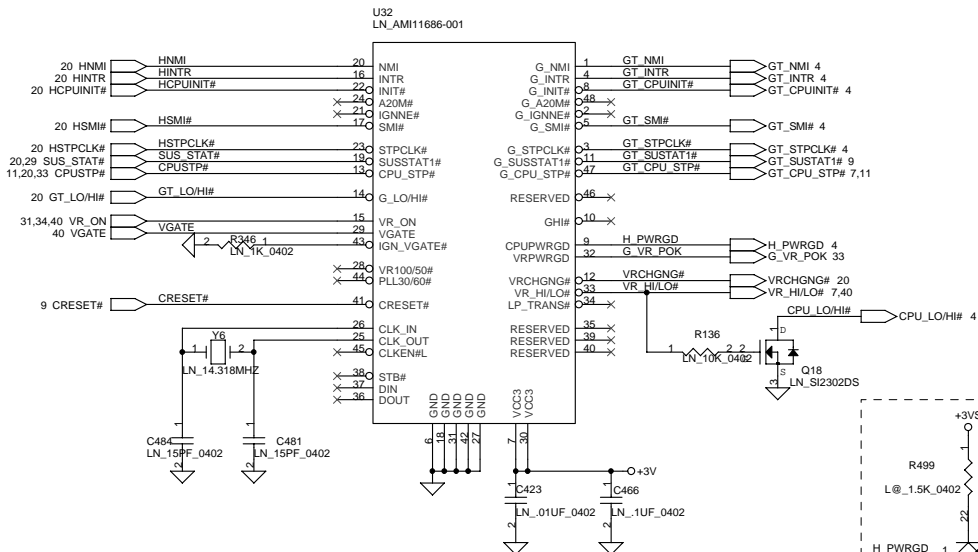
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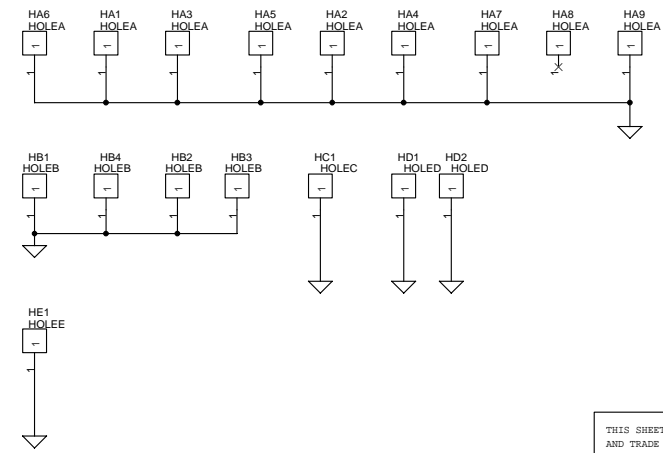
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Size: Custom, Document Number: 401196, Rev: 2A

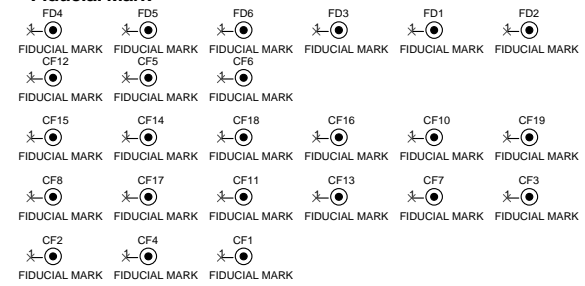
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for without Geyserville

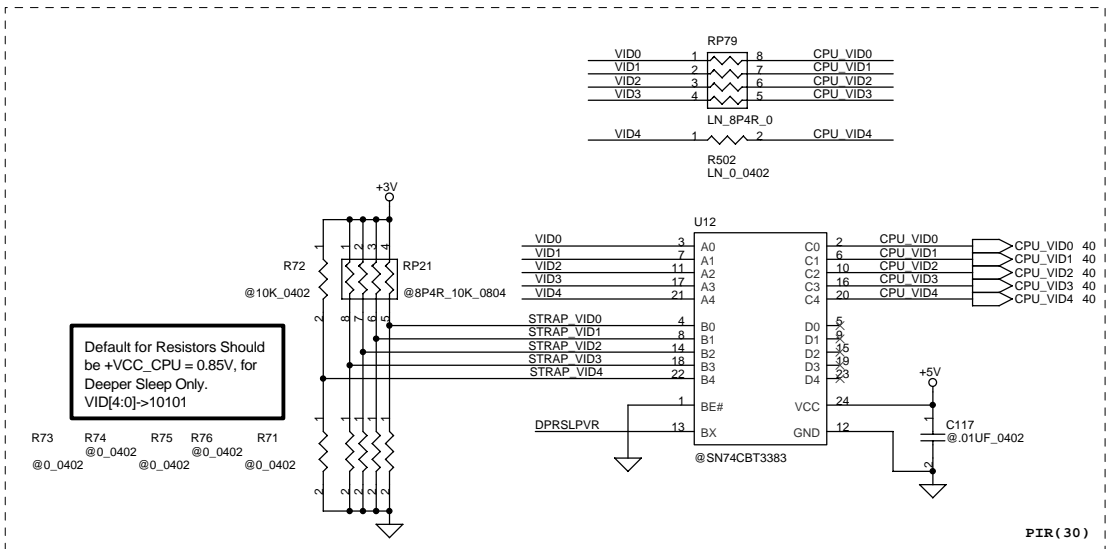
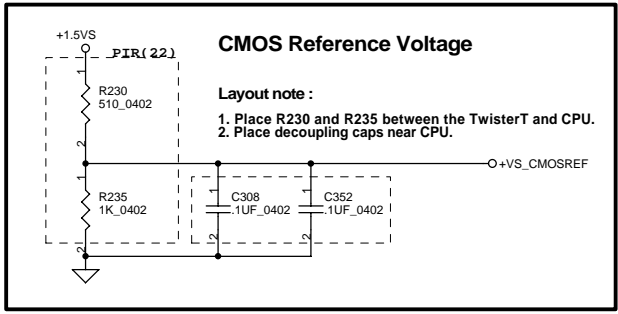
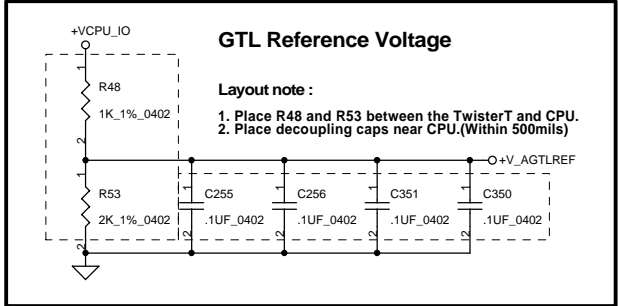
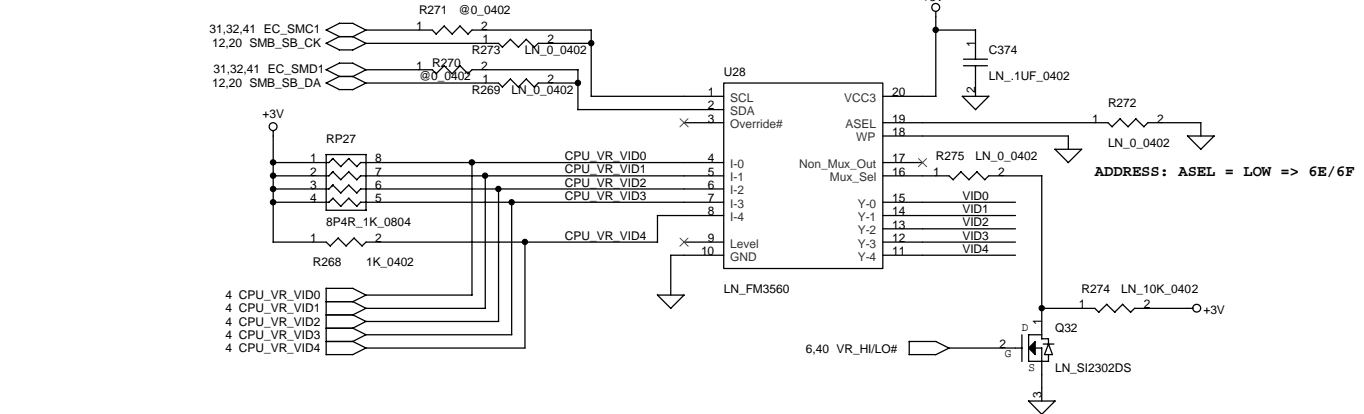
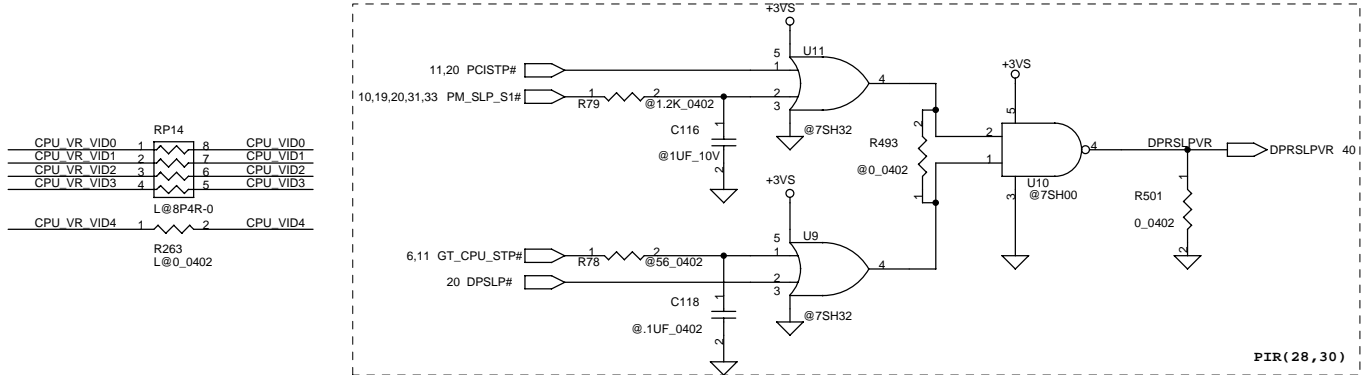


Fiducial Mark



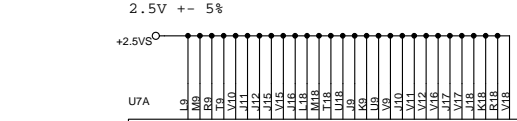
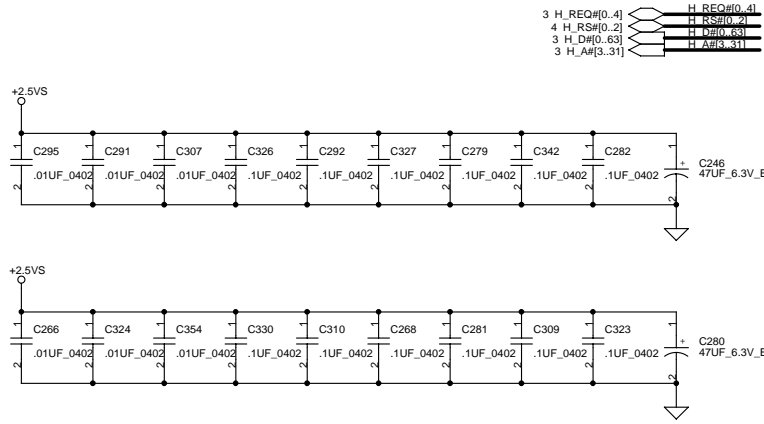
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<p>Date</p> <p>星期二一月17, 2002</p>	<p>Sheet</p> <p>6 of 44</p>	



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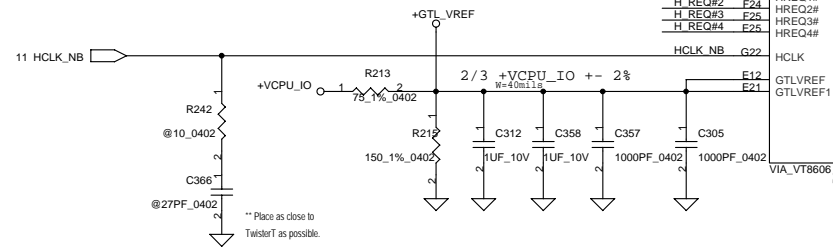
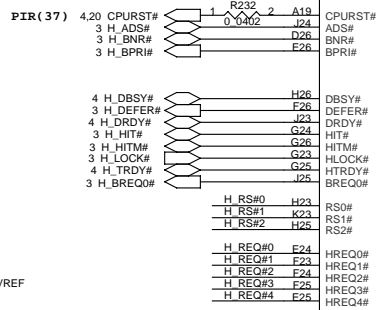
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H_A#3	A25	HA3#	VDD25	LD00#	F19	H_D#0
H_A#4	D24	HA4#	VDD25	HD1#	B18	H_D#1
H_A#5	B25	HA5#	VDD25	HD2#	B16	H_D#2
H_A#6	B26	HA6#	VDD25	HD3#	A16	H_D#3
H_A#7	F23	HA7#	VDD25	HD4#	C18	H_D#4
H_A#8	C26	HA8#	VDD25	HD5#	C17	H_D#5
H_A#9	C24	HA9#	VDD25	HD6#	D18	H_D#6
H_A#10	A23	HA10#	VDD25	HD7#	D15	H_D#7
H_A#11	C25	HA11#	VDD25	HD8#	D17	H_D#8
H_A#12	D22	HA12#	VDD25	HD9#	C16	H_D#9
H_A#13	B24	HA13#	VDD25	HD10#	B17	H_D#10
H_A#14	D25	HA14#	VDD25	HD11#	D16	H_D#11
H_A#15	F22	HA15#	VDD25	HD12#	A17	H_D#12
H_A#16	C23	HA16#	VDD25	HD13#	A15	H_D#13
H_A#17	D21	HA17#	VDD25	HD14#	E16	H_D#14
H_A#18	A20	HA18#	VDD25	HD15#	D19	H_D#15
H_A#19	C22	HA19#	VDD25	HD16#	A14	H_D#16
H_A#20	A21	HA20#	VDD25	HD17#	E18	H_D#17
H_A#21	B23	HA21#	VDD25	HD18#	F17	H_D#18
H_A#22	A22	HA22#	VDD25	HD19#	B14	H_D#19
H_A#23	B21	HA23#	VDD25	HD20#	C15	H_D#20
H_A#24	E20	HA24#	VDD25	HD21#	E14	H_D#21
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H_A#28	A24	HA28#	VDD25	HD25#	D13	H_D#25
H_A#29	B20	HA29#	VDD25	HD26#	C13	H_D#26
H_A#30	D20	HA30#	VDD25	HD27#	E9	H_D#27
H_A#31	C21	HA31#	VDD25	HD28#	C12	H_D#28
				HD29#	D12	H_D#29
				HD30#	E16	H_D#30
				HD31#	A13	H_D#31
				HD32#	B12	H_D#32
				HD33#	B13	H_D#33
				HD34#	A12	H_D#34
				HD35#	E13	H_D#35
				HD36#	D11	H_D#36
				HD37#	D10	H_D#37
				HD38#	A11	H_D#38
				HD39#	E10	H_D#39
				HD40#	E8	H_D#40
				HD41#	C8	H_D#41
				HD42#	D8	H_D#42
				HD43#	C11	H_D#43
				HD44#	B10	H_D#44
				HD45#	A10	H_D#45
				HD46#	F7	H_D#46
				HD47#	D6	H_D#47
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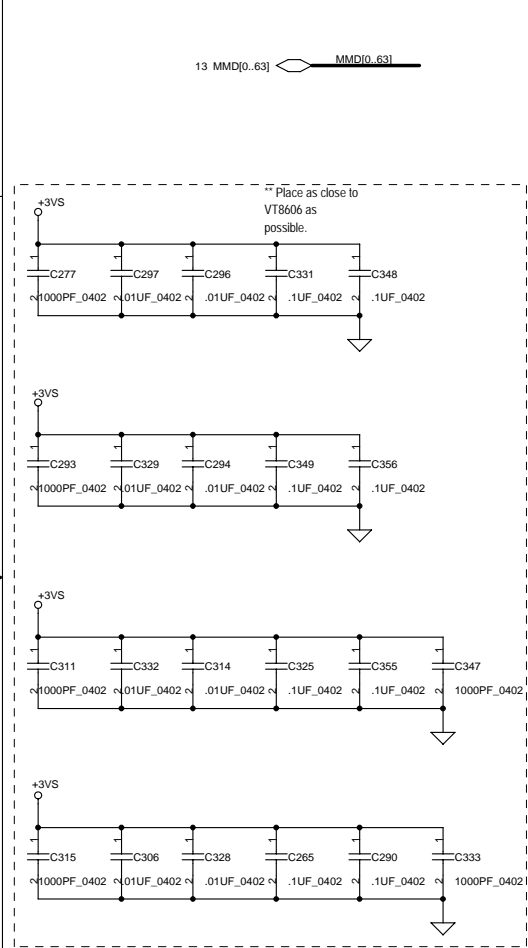
**VT8606
TwisterT**

HOST INTERFACE

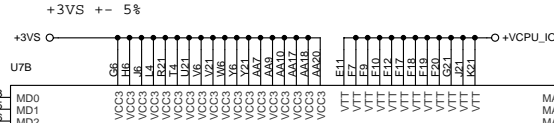


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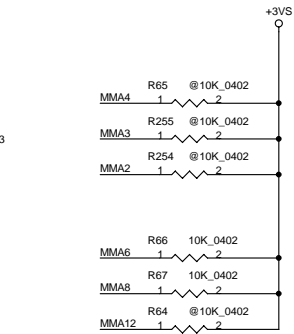
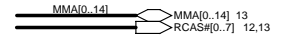
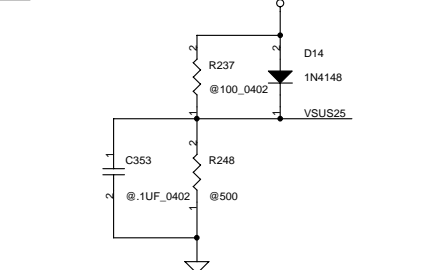
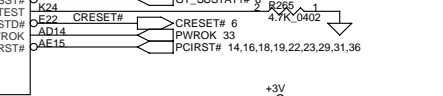
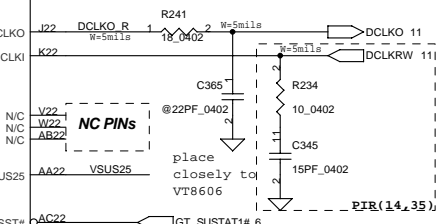
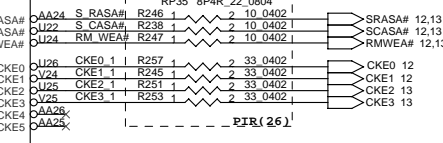
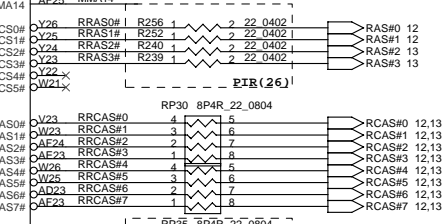
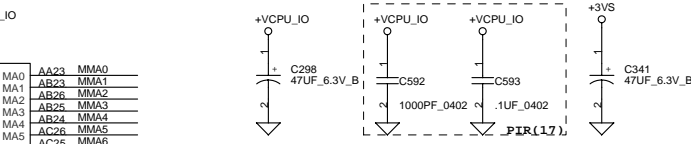
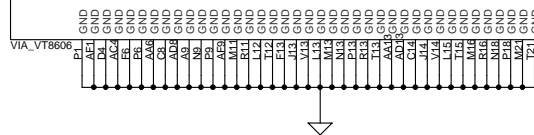


MMD0	M23	MD0
MMD1	K28	MD1
MMD2	L26	MD2
MMD3	L28	MD3
MMD4	M26	MD4
MMD5	M24	MD5
MMD6	N26	MD6
MMD7	N24	MD7
MMD8	P28	MD8
MMD9	P26	MD9
MMD10	R23	MD10
MMD11	R25	MD11
MMD12	P22	MD12
MMD13	T23	MD13
MMD14	T25	MD14
MMD15	T22	MD15
MMD16	A22	MD16
MMD17	AF22	MD17
MMD18	AB21	MD18
MMD19	AE21	MD19
MMD20	AB20	MD20
MMD21	AD20	MD21
MMD22	AE20	MD22
MMD23	AC18	MD23
MMD24	AF18	MD24
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MMD33	L23	MD33
MMD34	M22	MD34
MMD35	L24	MD35
MMD36	M25	MD36
MMD37	N23	MD37
MMD38	N25	MD38
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MMD40	P28	MD40
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MMD59	AE17	MD59
MMD60	AC17	MD60
MMD61	AD16	MD61
MMD62	AF16	MD62
MMD63	AB16	MD63



**VT8606
TwisterT**

DRAM INTERFACE



- MA4 L DISABLE INTA# CLAIM
- H ENABLE INTA# CLAIM
- MA3 L DISABLE I/O ACCESS
- H ENABLE I/O ACCESS
- MA2 L ADDRESS MAPPING 1
- H ADDRESS MAPPING 0
- MA12 MA8 CPU FSB FREQ.

- 00 = 66 MHZ
- 01 = AUTO
- 11 = 133 MHZ
- 10 = 100 MHZ
- MA6 GTL INTRNAL PULLUPS
- 0 ENABLE
- 1 DISABLE

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VCCRGB	2.5V +- 0.25V
VCCA	2.5V +- 0.25V
VCCDAC	2.5V +- 0.25V
VCCPLL1	2.5V +- 0.25V
VCCPLL2	2.5V +- 0.25V
VCCPLL	3.3V +- 0.3V -> 2.5V +- 0.25V
VCCLVDS	3.3V +- 0.3V
VDDD	2.5V +- 0.25V

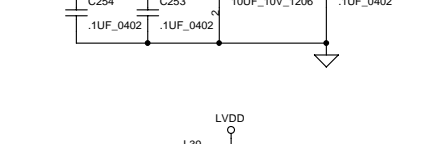
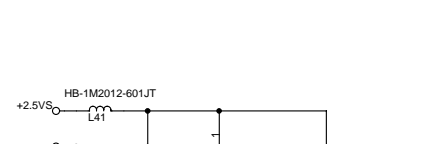
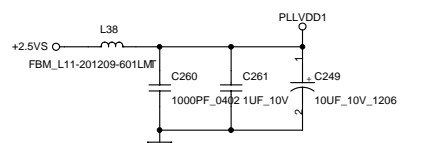
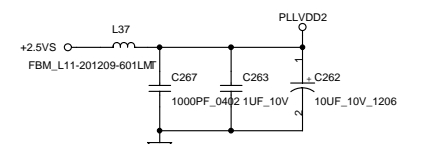
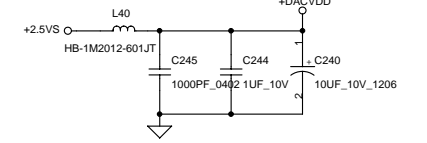
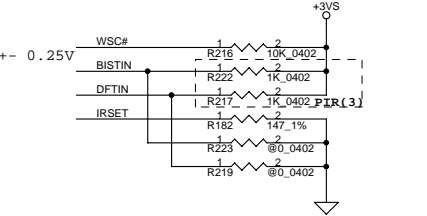
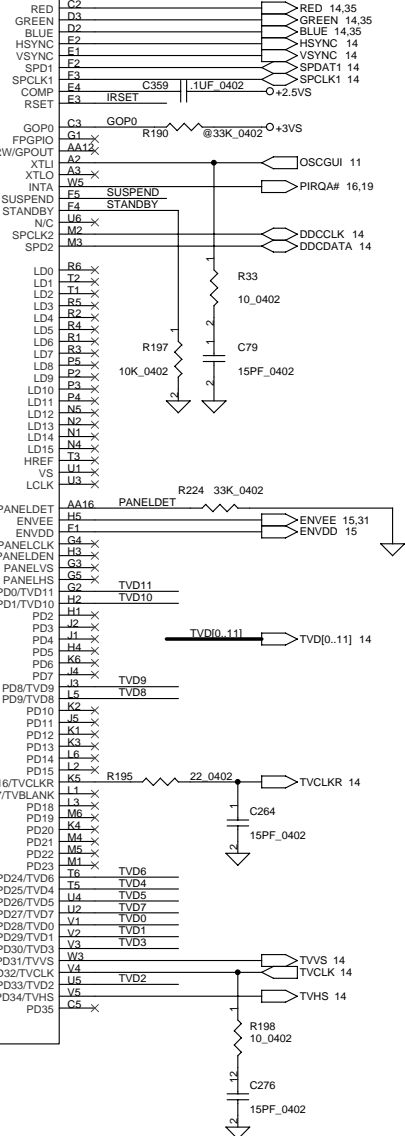
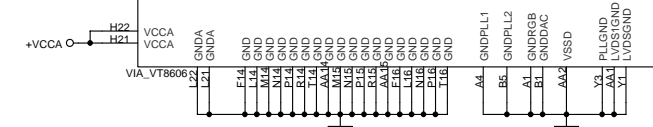
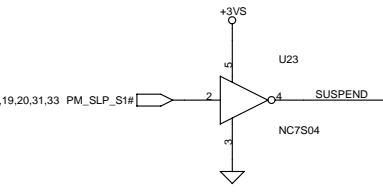
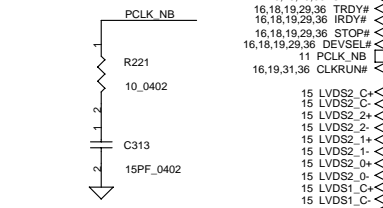
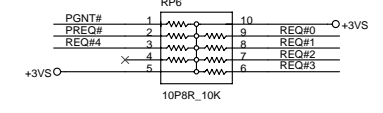
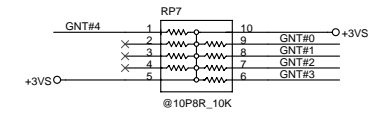
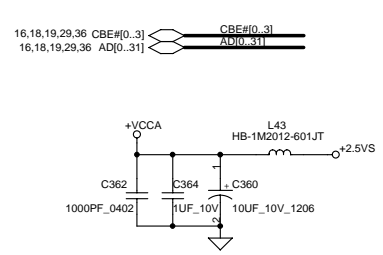
**VT8606
TwisterT**

PCI INTERFACE

DISPLAY INTERFACE

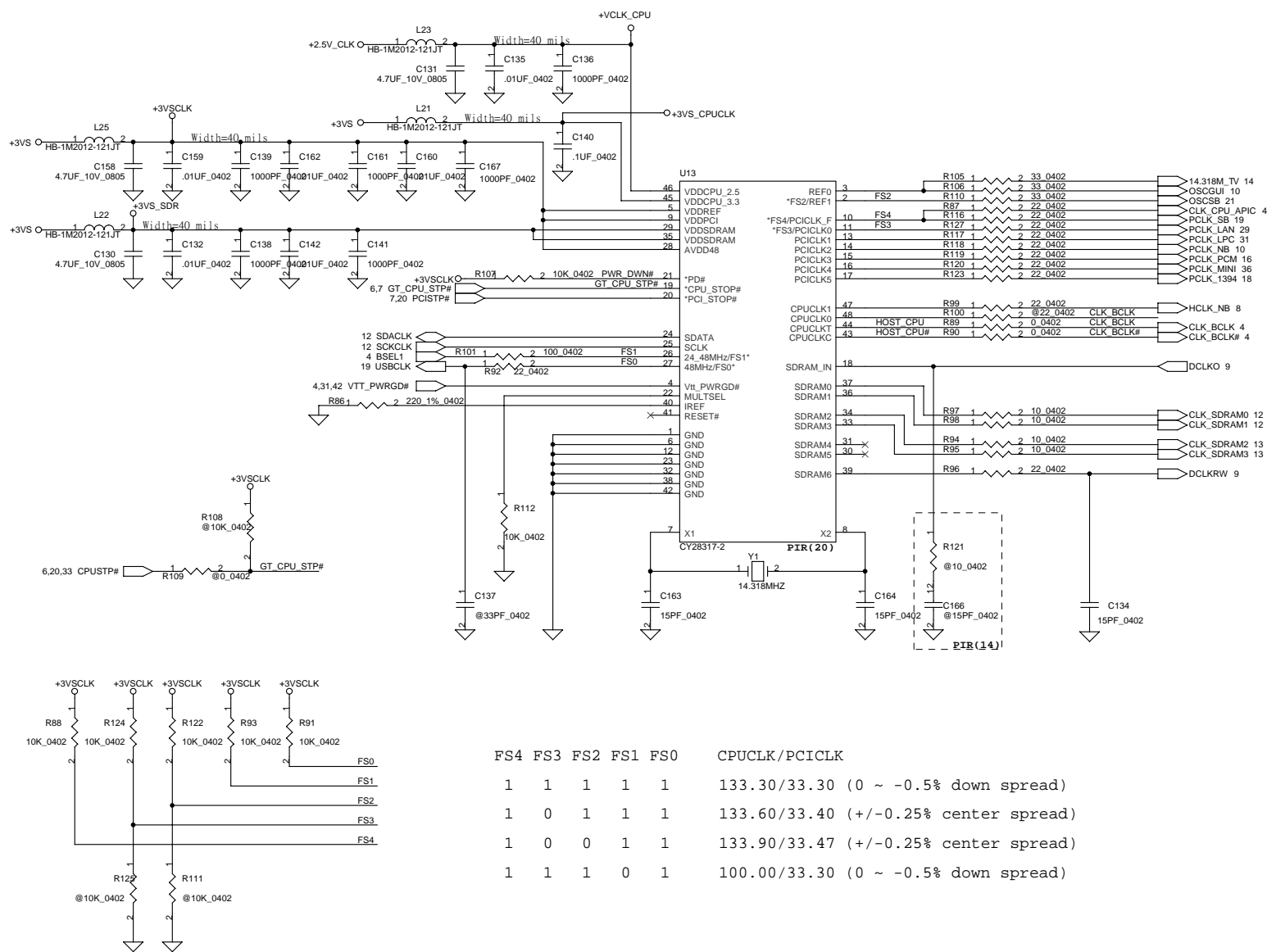
LVDS

AD0	AE14	AD0	AE14	AD0	AE14
AD1	AE13	AD1	AE13	AD1	AE13
AD2	AE12	AD2	AE12	AD2	AE12
AD3	AE11	AD3	AE11	AD3	AE11
AD4	AE10	AD4	AE10	AD4	AE10
AD5	AE9	AD5	AE9	AD5	AE9
AD6	AE8	AD6	AE8	AD6	AE8
AD7	AE7	AD7	AE7	AD7	AE7
AD8	AE6	AD8	AE6	AD8	AE6
AD9	AE5	AD9	AE5	AD9	AE5
AD10	AE4	AD10	AE4	AD10	AE4
AD11	AE3	AD11	AE3	AD11	AE3
AD12	AE2	AD12	AE2	AD12	AE2
AD13	AE1	AD13	AE1	AD13	AE1
AD14	AE0	AD14	AE0	AD14	AE0
AD15	AE0	AD15	AE0	AD15	AE0
AD16	AE0	AD16	AE0	AD16	AE0
AD17	AE0	AD17	AE0	AD17	AE0
AD18	AE0	AD18	AE0	AD18	AE0
AD19	AE0	AD19	AE0	AD19	AE0
AD20	AE0	AD20	AE0	AD20	AE0
AD21	AE0	AD21	AE0	AD21	AE0
AD22	AE0	AD22	AE0	AD22	AE0
AD23	AE0	AD23	AE0	AD23	AE0
AD24	AE0	AD24	AE0	AD24	AE0
AD25	AE0	AD25	AE0	AD25	AE0
AD26	AE0	AD26	AE0	AD26	AE0
AD27	AE0	AD27	AE0	AD27	AE0
AD28	AE0	AD28	AE0	AD28	AE0
AD29	AE0	AD29	AE0	AD29	AE0
AD30	AE0	AD30	AE0	AD30	AE0
AD31	AE0	AD31	AE0	AD31	AE0
CBE#0	AE12C	CBE#0	AE12C	CBE#0	AE12C
CBE#1	AD9C	CBE#1	AD9C	CBE#1	AD9C
CBE#2	AD9C	CBE#2	AD9C	CBE#2	AD9C
CBE#3	AD7C	CBE#3	AD7C	CBE#3	AD7C
REQ#0	AC5	REQ#0	AC5	REQ#0	AC5
REQ#1	AD5	REQ#1	AD5	REQ#1	AD5
REQ#2	AE4	REQ#2	AE4	REQ#2	AE4
REQ#3	AD4	REQ#3	AD4	REQ#3	AD4
REQ#4	AE2	REQ#4	AE2	REQ#4	AE2
GNT#0	AB5	GNT#0	AB5	GNT#0	AB5
GNT#1	AE4	GNT#1	AE4	GNT#1	AE4
GNT#2	AE3	GNT#2	AE3	GNT#2	AE3
GNT#3	AE3	GNT#3	AE3	GNT#3	AE3
GNT#4	AE2	GNT#4	AE2	GNT#4	AE2
PREQ#	AC15C	PREQ#	AC15C	PREQ#	AC15C
PGNT#	AD15C	PGNT#	AD15C	PGNT#	AD15C
FRAME#	AE9C	FRAME#	AE9C	FRAME#	AE9C
PLOCK#	AE5C	PLOCK#	AE5C	PLOCK#	AE5C
PAR	AB10C	PAR	AB10C	PAR	AB10C
SERR#	AE10C	SERR#	AE10C	SERR#	AE10C
TRDY#	AD10C	TRDY#	AD10C	TRDY#	AD10C
IRDY#	AE10C	IRDY#	AE10C	IRDY#	AE10C
STOP#	AE10C	STOP#	AE10C	STOP#	AE10C
DEVSEL#	AB9C	DEVSEL#	AB9C	DEVSEL#	AB9C
PCLK_NB	AB11C	PCLK_NB	AB11C	PCLK_NB	AB11C
CLKRUN#	AE15C	CLKRUN#	AE15C	CLKRUN#	AE15C
ZCP	AD1	ZCP	AD1	ZCP	AD1
ZCM	AE1	ZCM	AE1	ZCM	AE1
Z2P	AA4	Z2P	AA4	Z2P	AA4
Z2M	AA4	Z2M	AA4	Z2M	AA4
Z1P	AC3	Z1P	AC3	Z1P	AC3
Z1M	AD3	Z1M	AD3	Z1M	AD3
Z0P	AD2	Z0P	AD2	Z0P	AD2
Z0M	AD2	Z0M	AD2	Z0M	AD2
YCP	AB1	YCP	AB1	YCP	AB1
YCM	AC1	YCM	AC1	YCM	AC1
Y5	Y5	Y5	Y5	Y5	Y5
Y2P	AA5	Y2P	AA5	Y2P	AA5
Y2M	AA5	Y2M	AA5	Y2M	AA5
Y4	Y4	Y4	Y4	Y4	Y4
Y1P	AA3	Y1P	AA3	Y1P	AA3
Y1M	AA3	Y1M	AA3	Y1M	AA3
Y0P	AB3	Y0P	AB3	Y0P	AB3
Y0M	AB3	Y0M	AB3	Y0M	AB3



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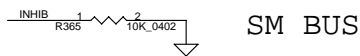
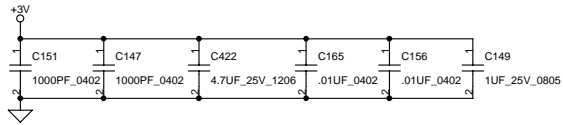
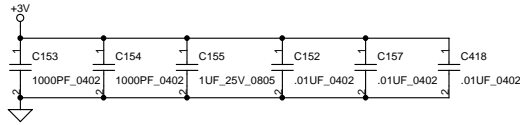
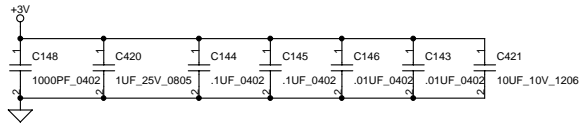
	FS4	FS3	FS2	FS1	FS0	CPUCLK/PCICLK
	1	1	1	1	1	133.30/33.30 (0 ~ -0.5% down spread)
	1	0	1	1	1	133.60/33.40 (+/-0.25% center spread)
	1	0	0	1	1	133.90/33.47 (+/-0.25% center spread)
	1	1	1	0	1	100.00/33.30 (0 ~ -0.5% down spread)

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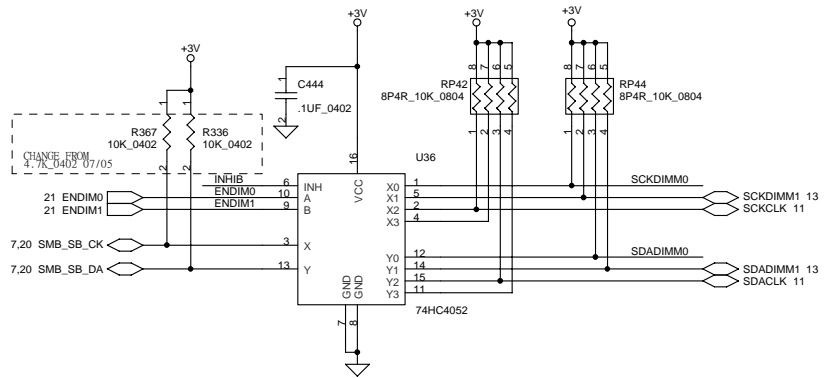
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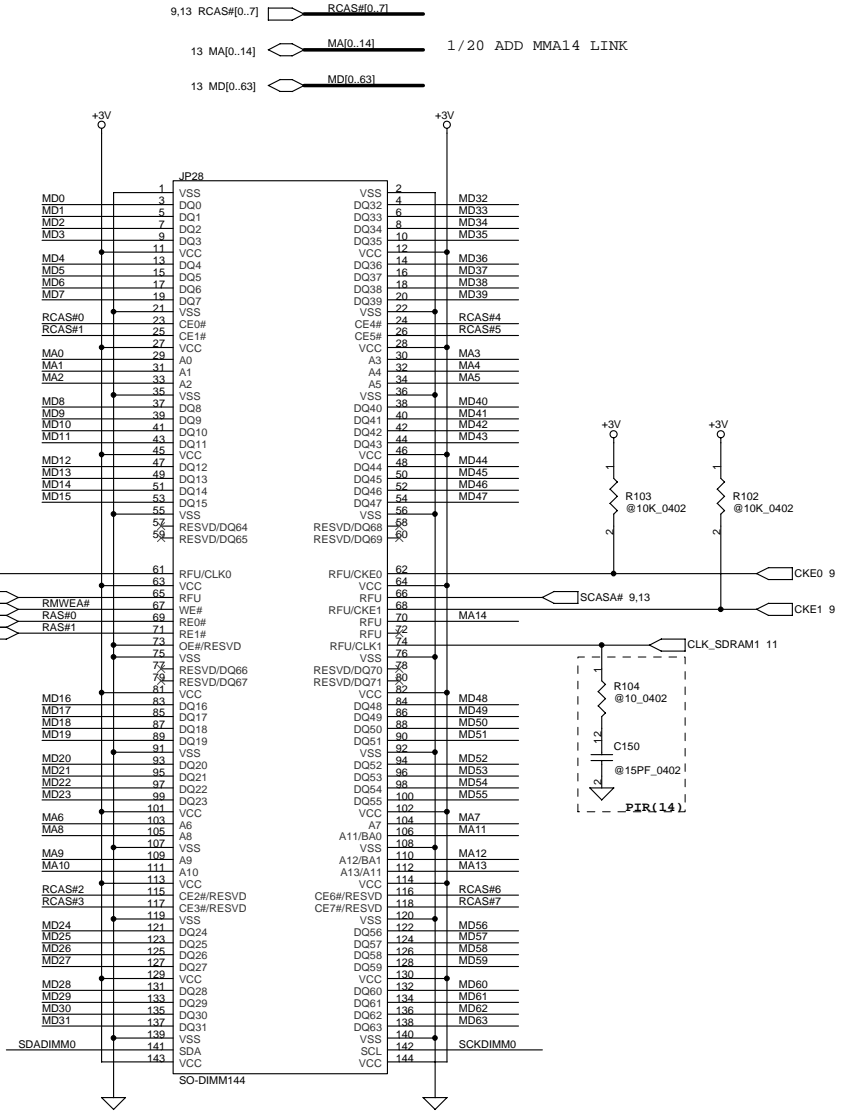
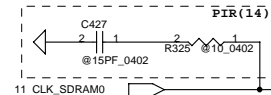
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SM BUS



INHIB	ENDIM1	ENDIM0	Channel ON
0	0	0	SO-DIMM0
0	0	1	SO-DIMM1
0	1	0	Clock Generator
1	X	X	NONE



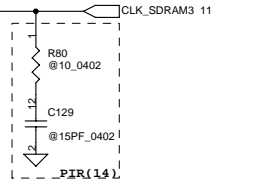
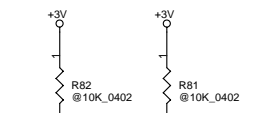
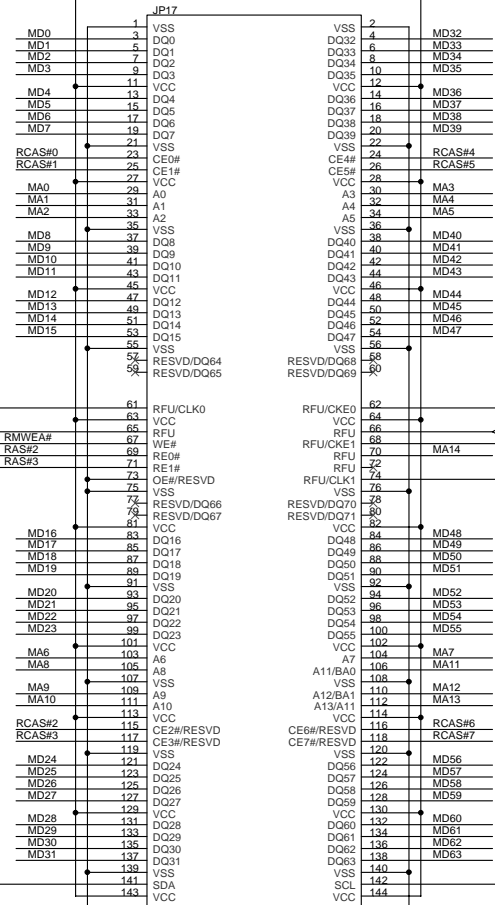
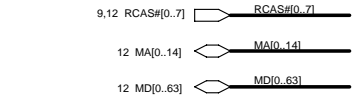
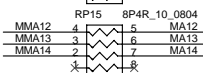
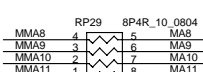
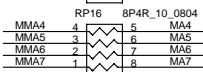
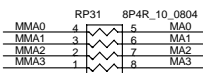
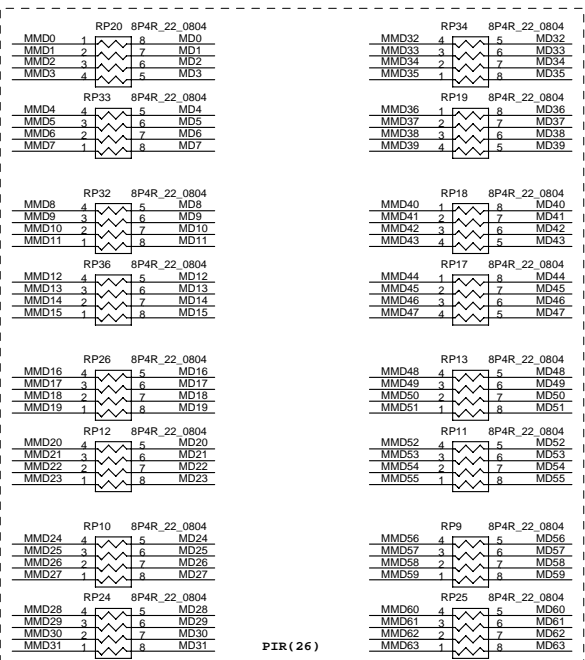
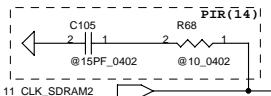
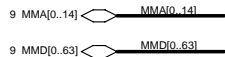
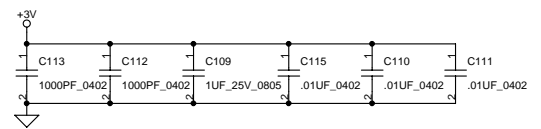
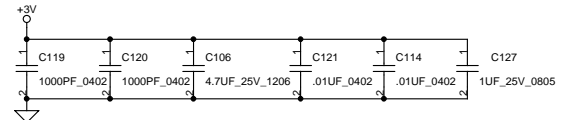
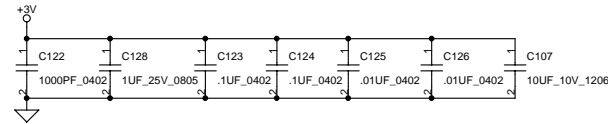
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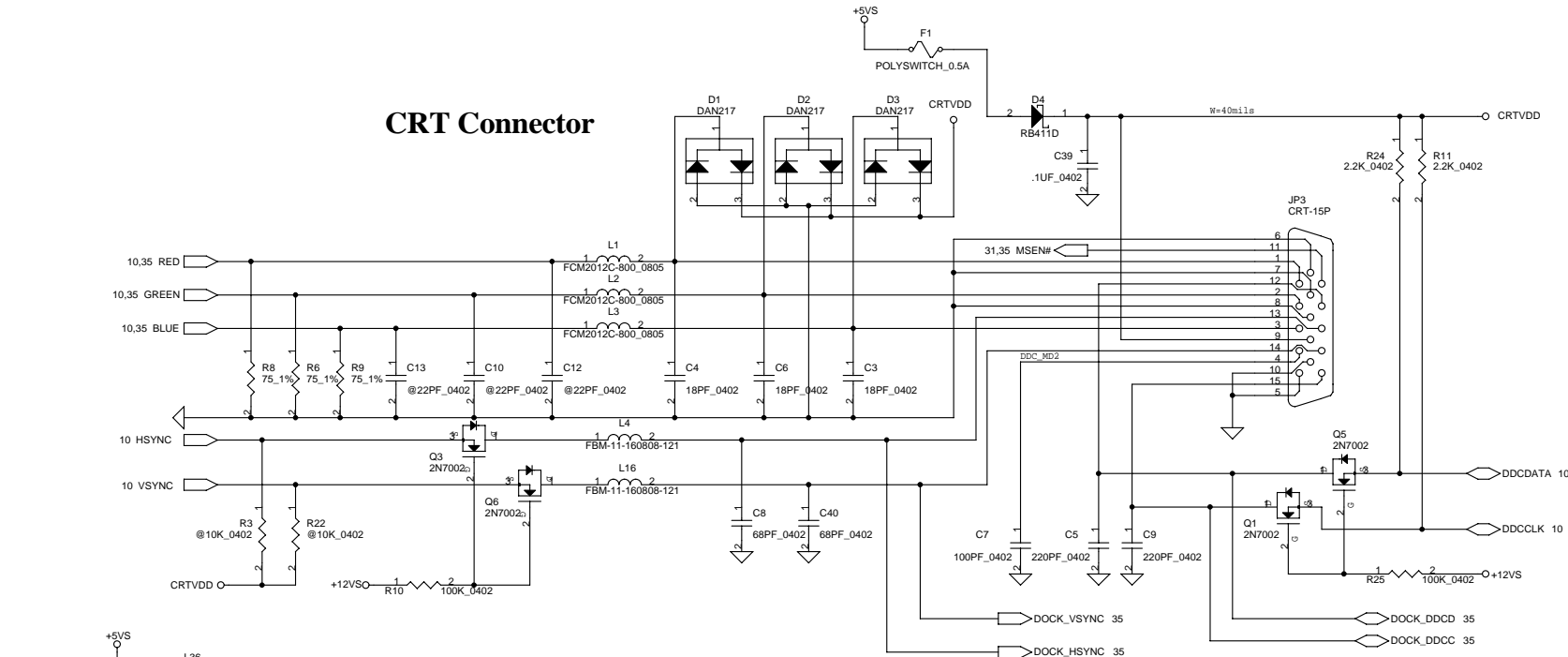


P1R (26)

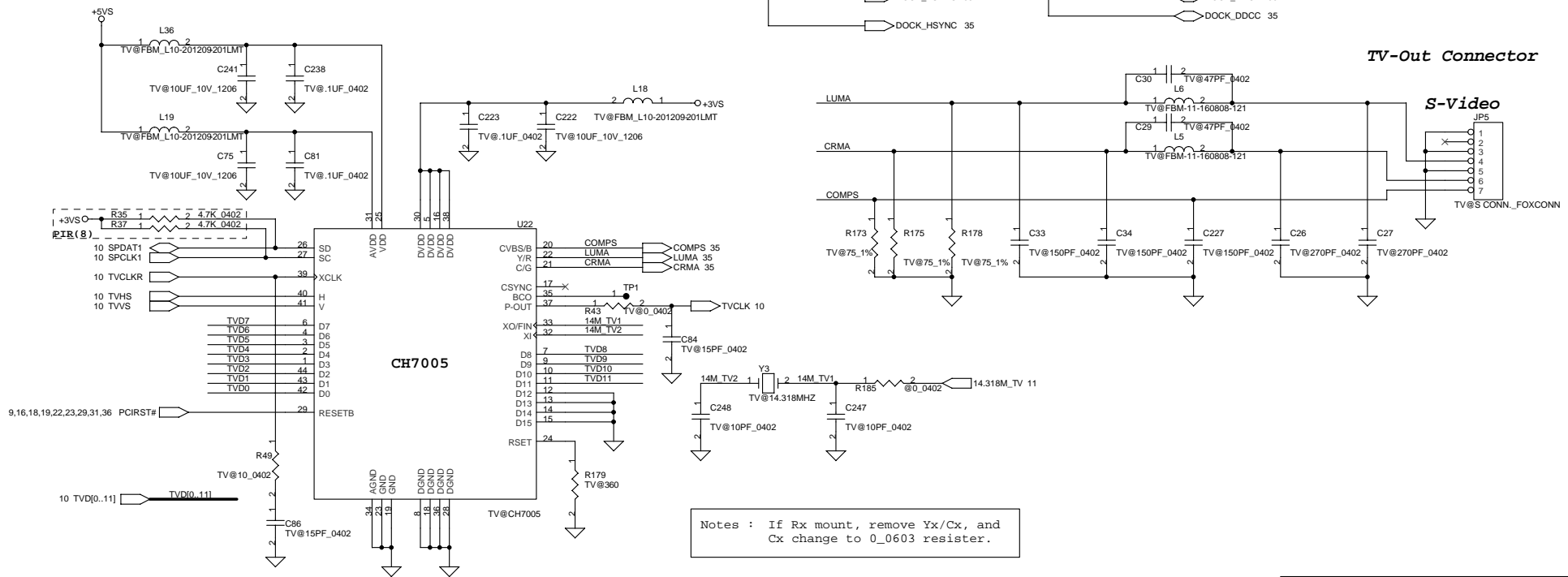
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CRT Connector



TV-Out Connector



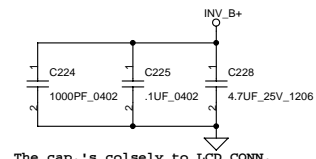
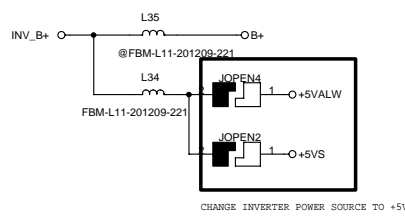
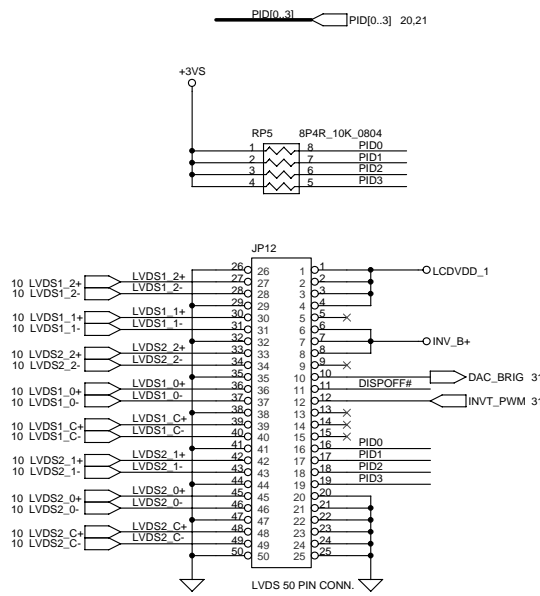
Notes : If Rx mount, remove Yx/Cx, and Cx change to 0_0603 resistor.

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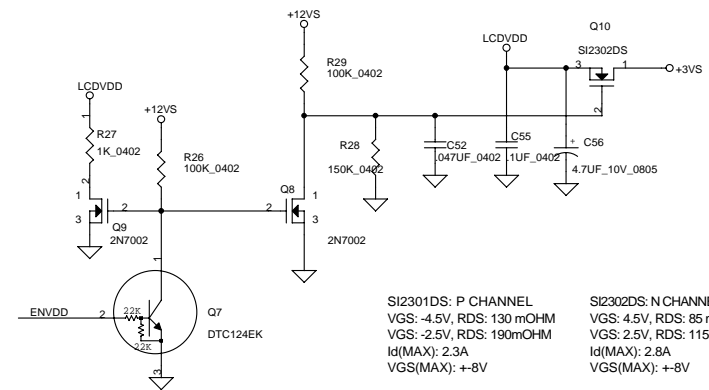
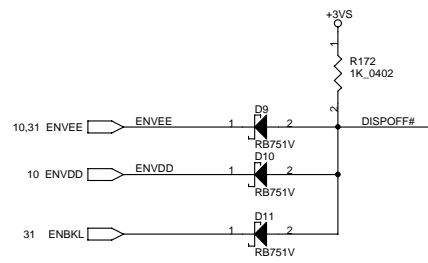
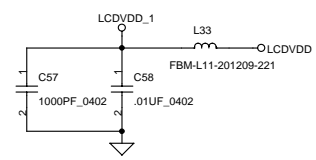
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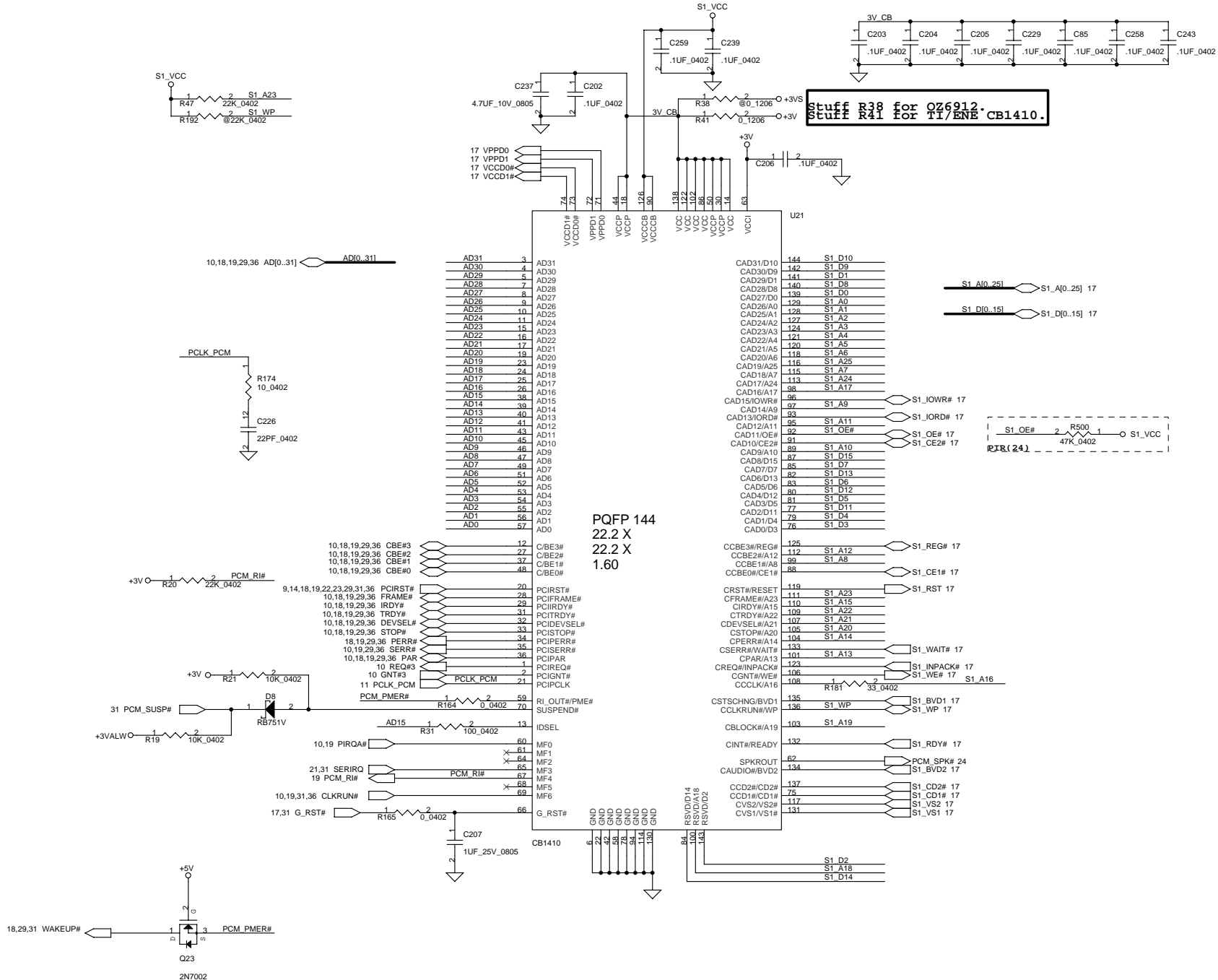


The cap.'s colselly to LCD CONN.



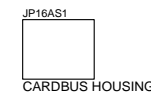
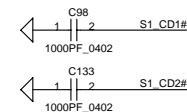
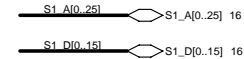
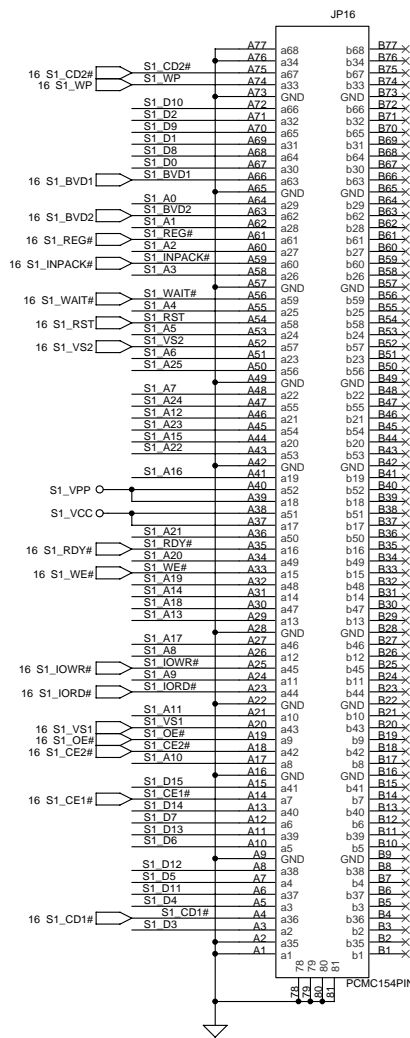
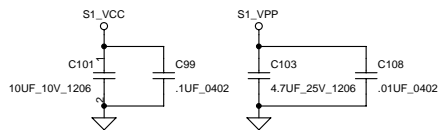
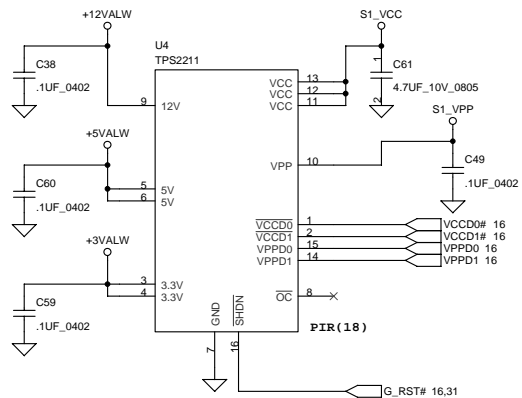
SI2301DS: P CHANNEL
 VGS: -4.5V, RDS: 130 mOHM
 VGS: -2.5V, RDS: 190mOHM
 Id(MAX): 2.3A
 VGS(MAX): +8V

SI2302DS: N CHANNEL
 VGS: 4.5V, RDS: 85 mOHM
 VGS: 2.5V, RDS: 115mOHM
 Id(MAX): 2.8A
 VGS(MAX): +8V



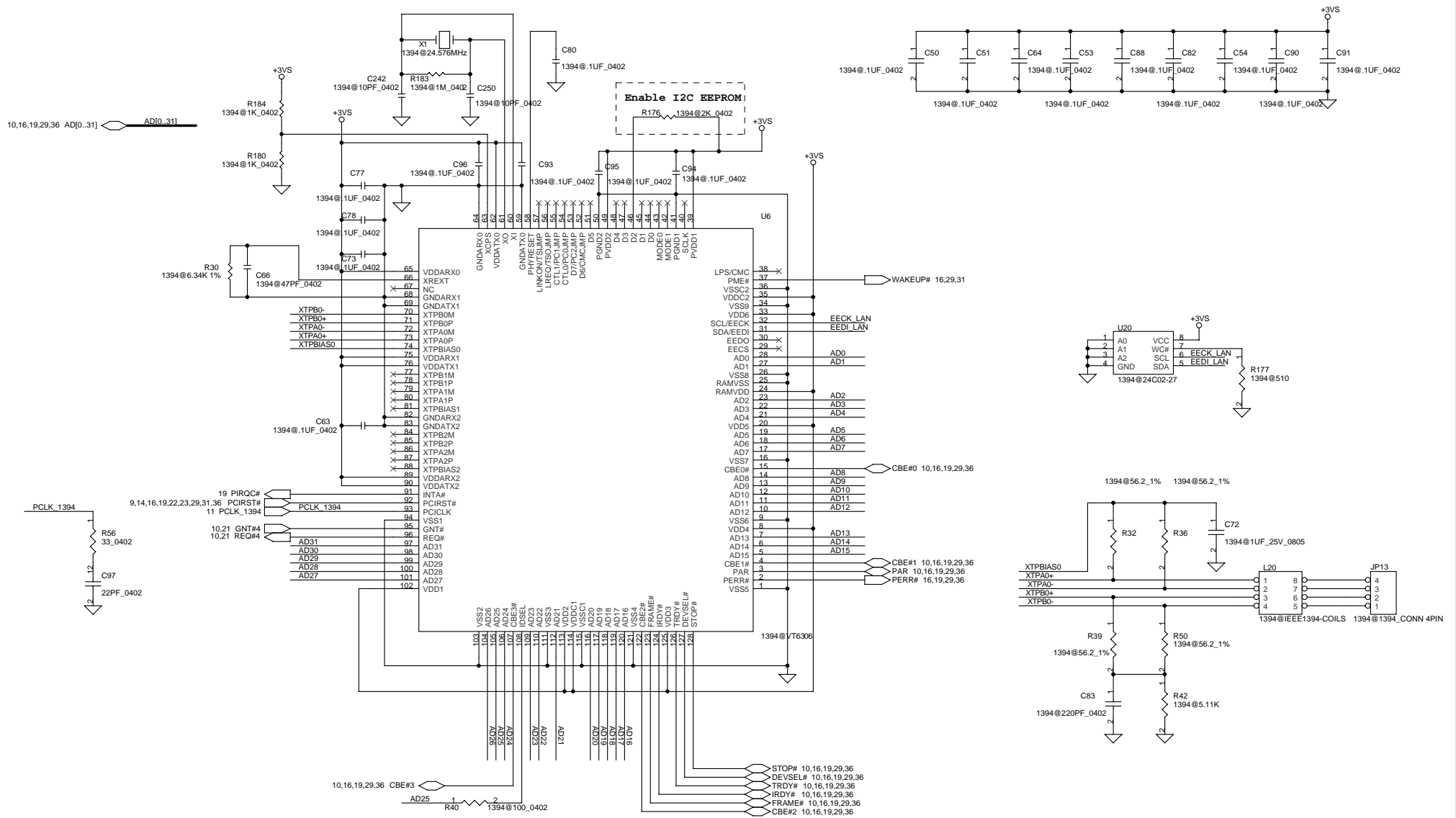
PQFP 144
22.2 X
22.2 X
1.60

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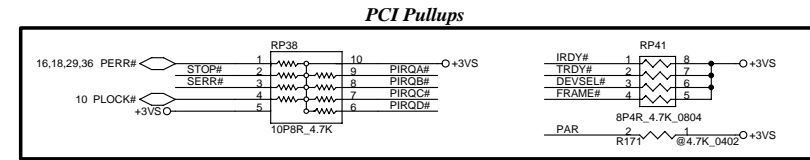
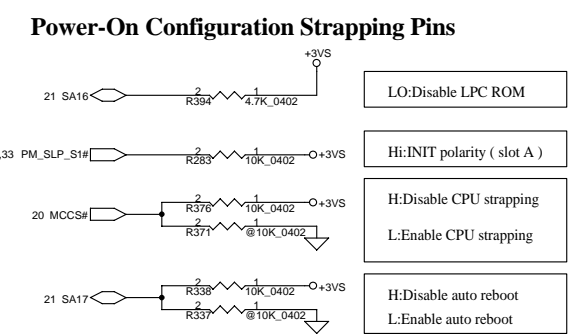
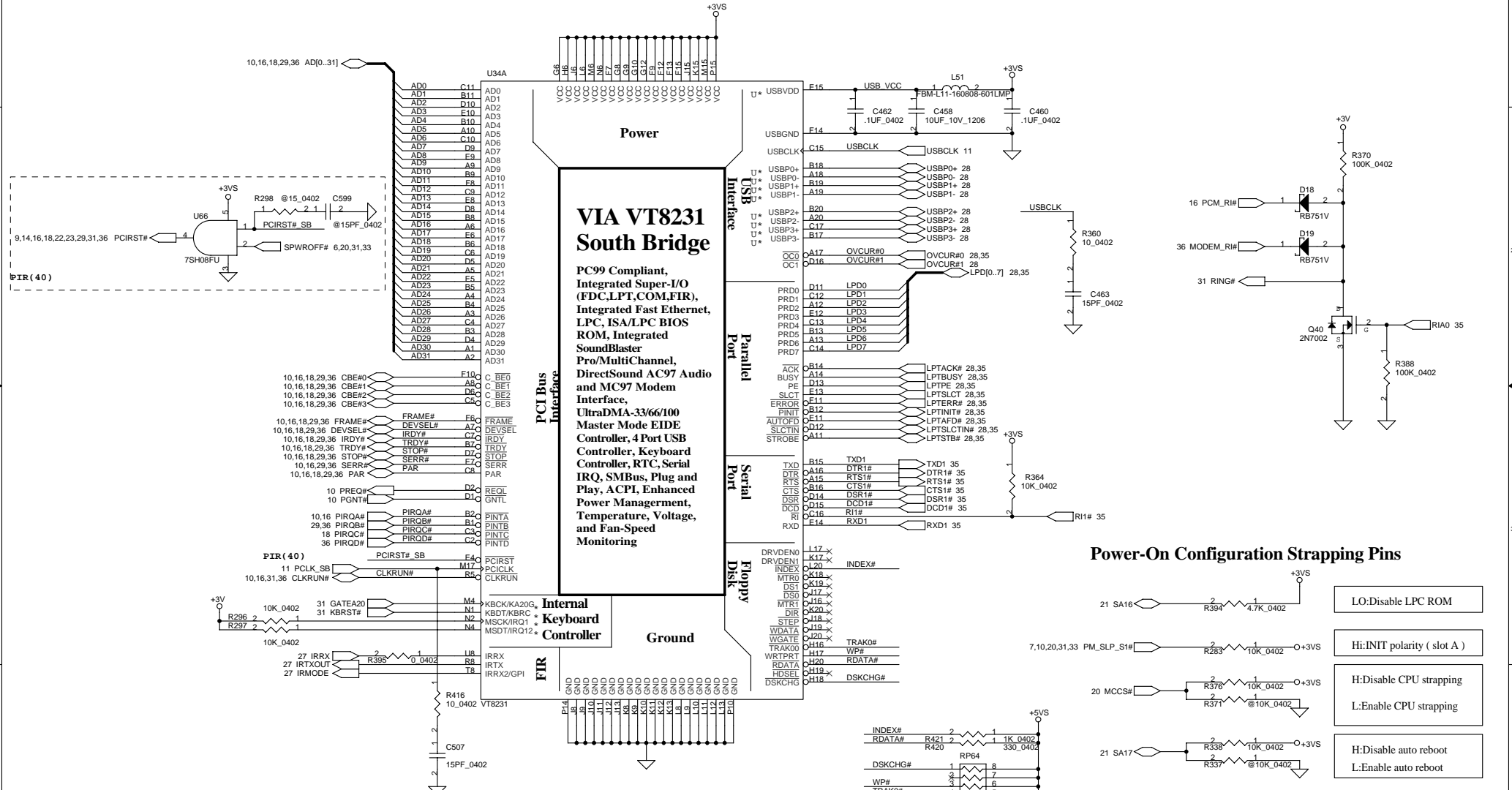
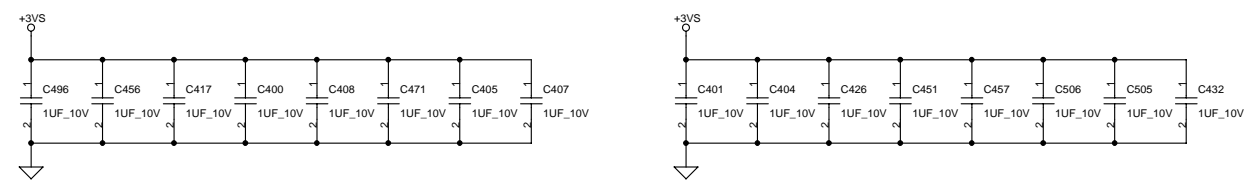
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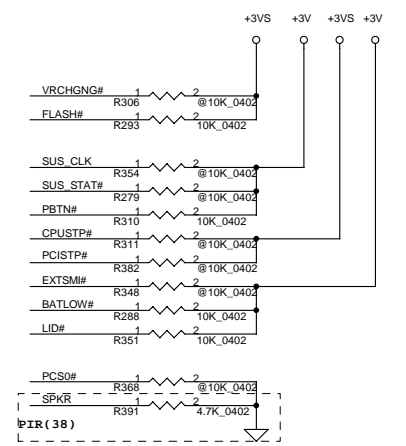
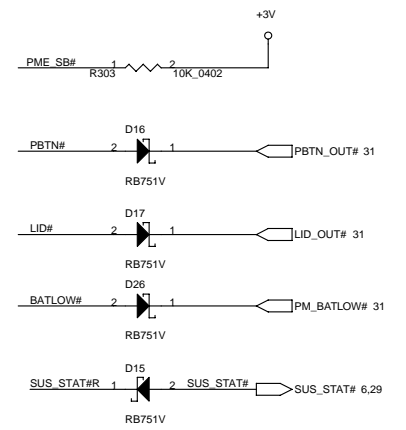
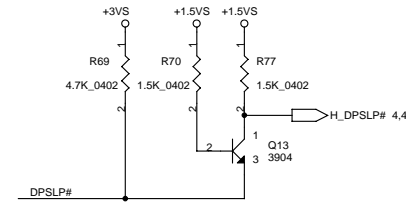
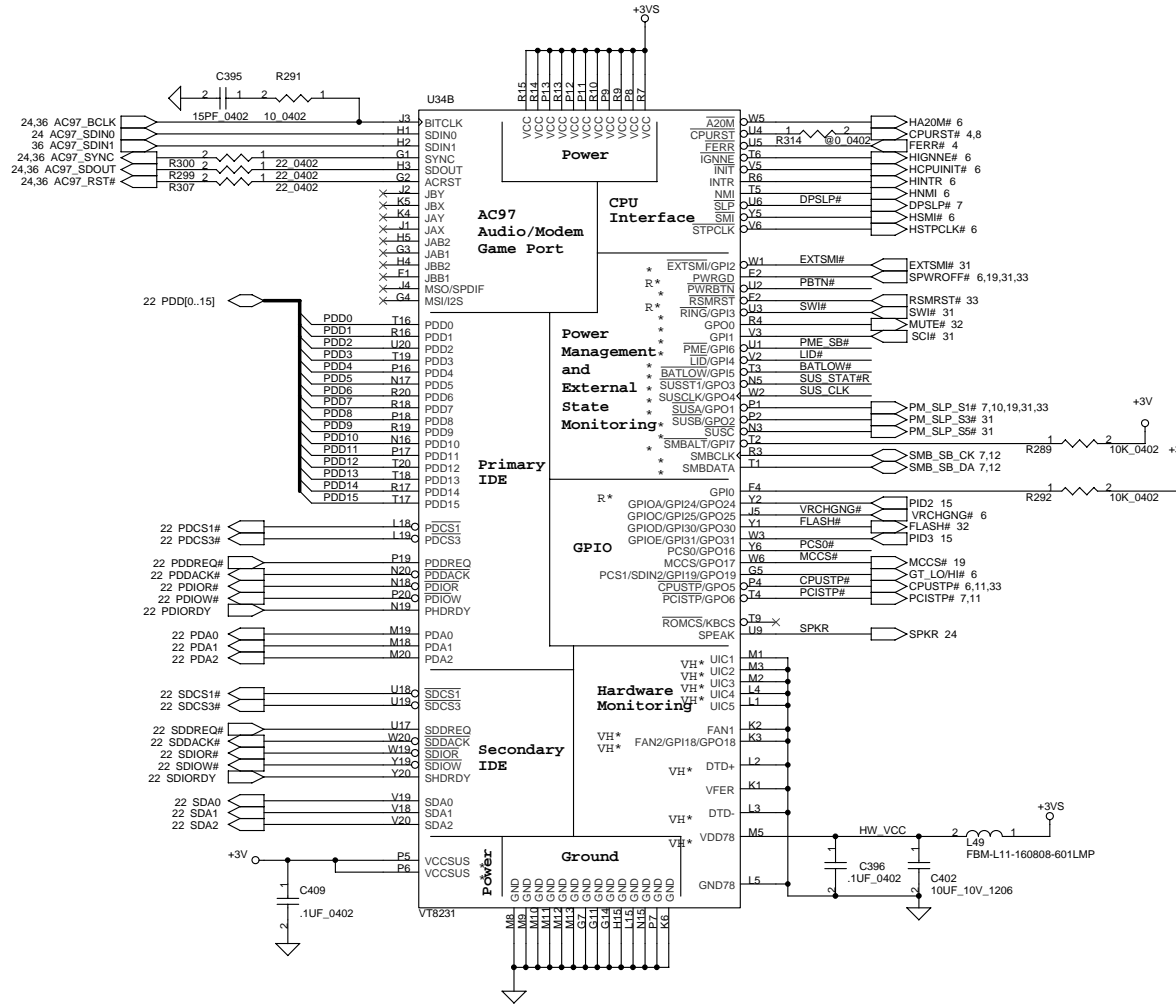


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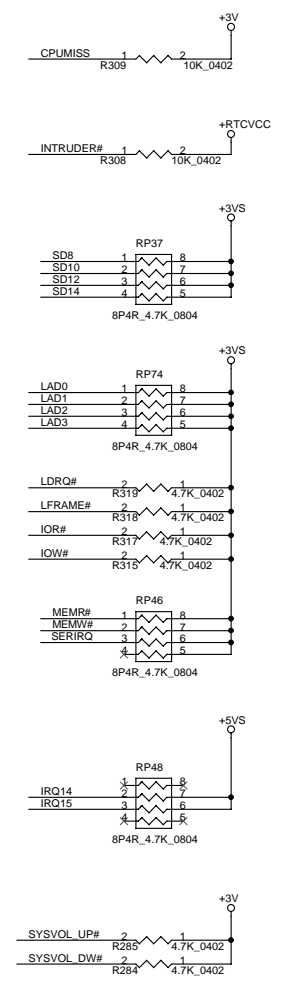
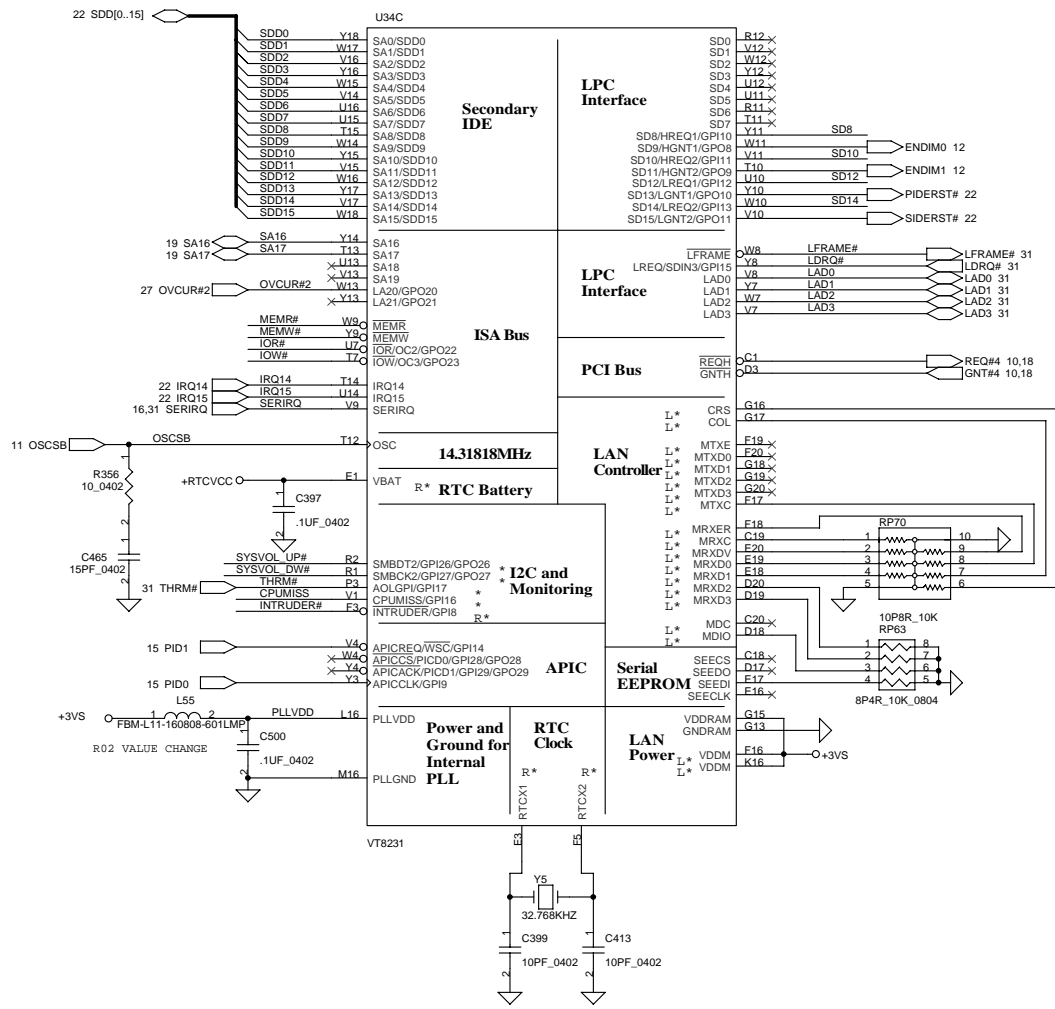
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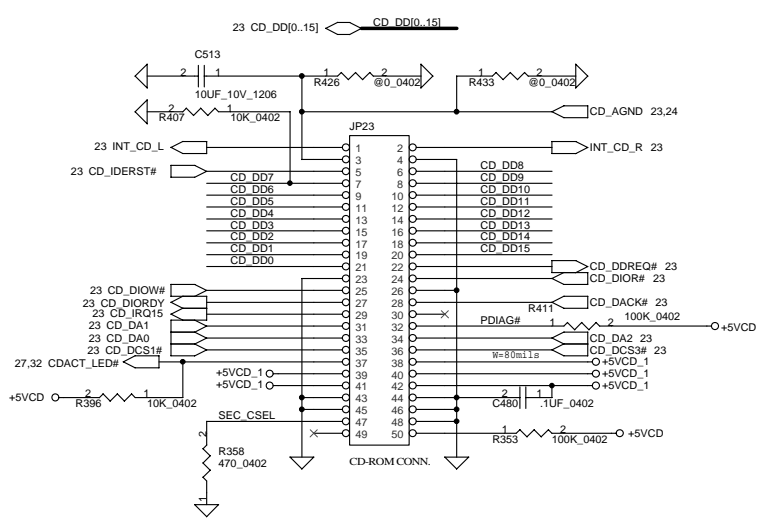
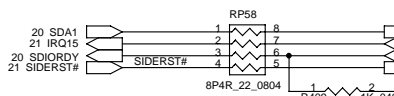
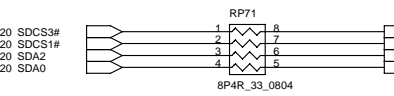
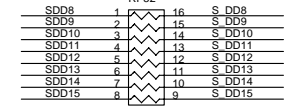
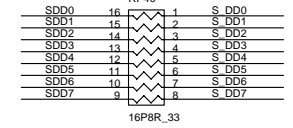
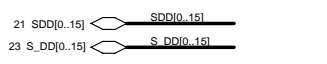
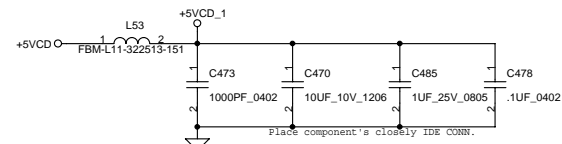
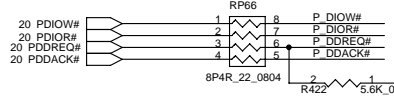
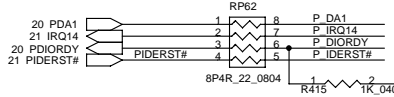
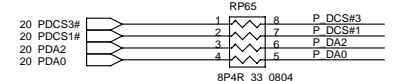
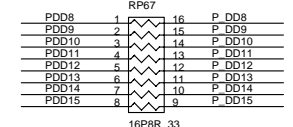
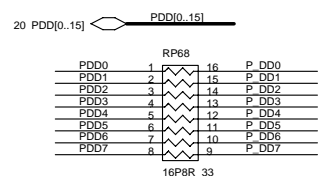
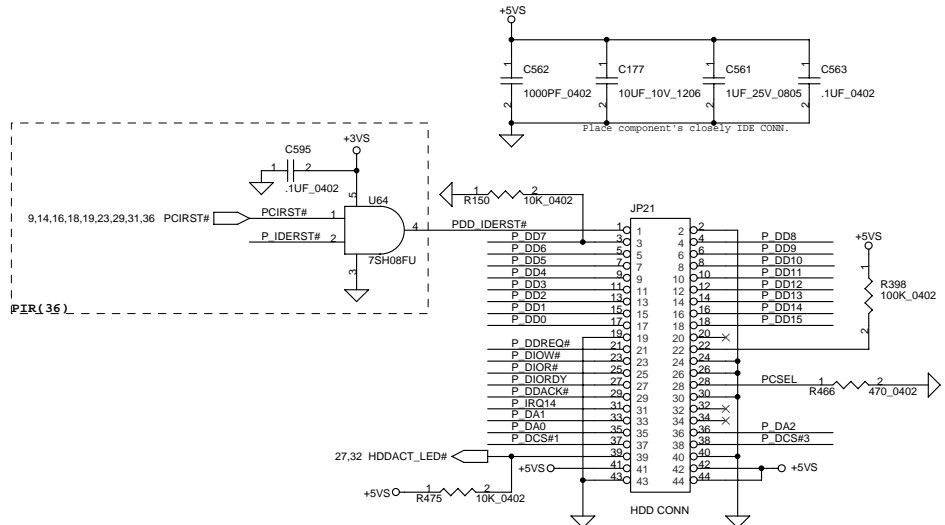


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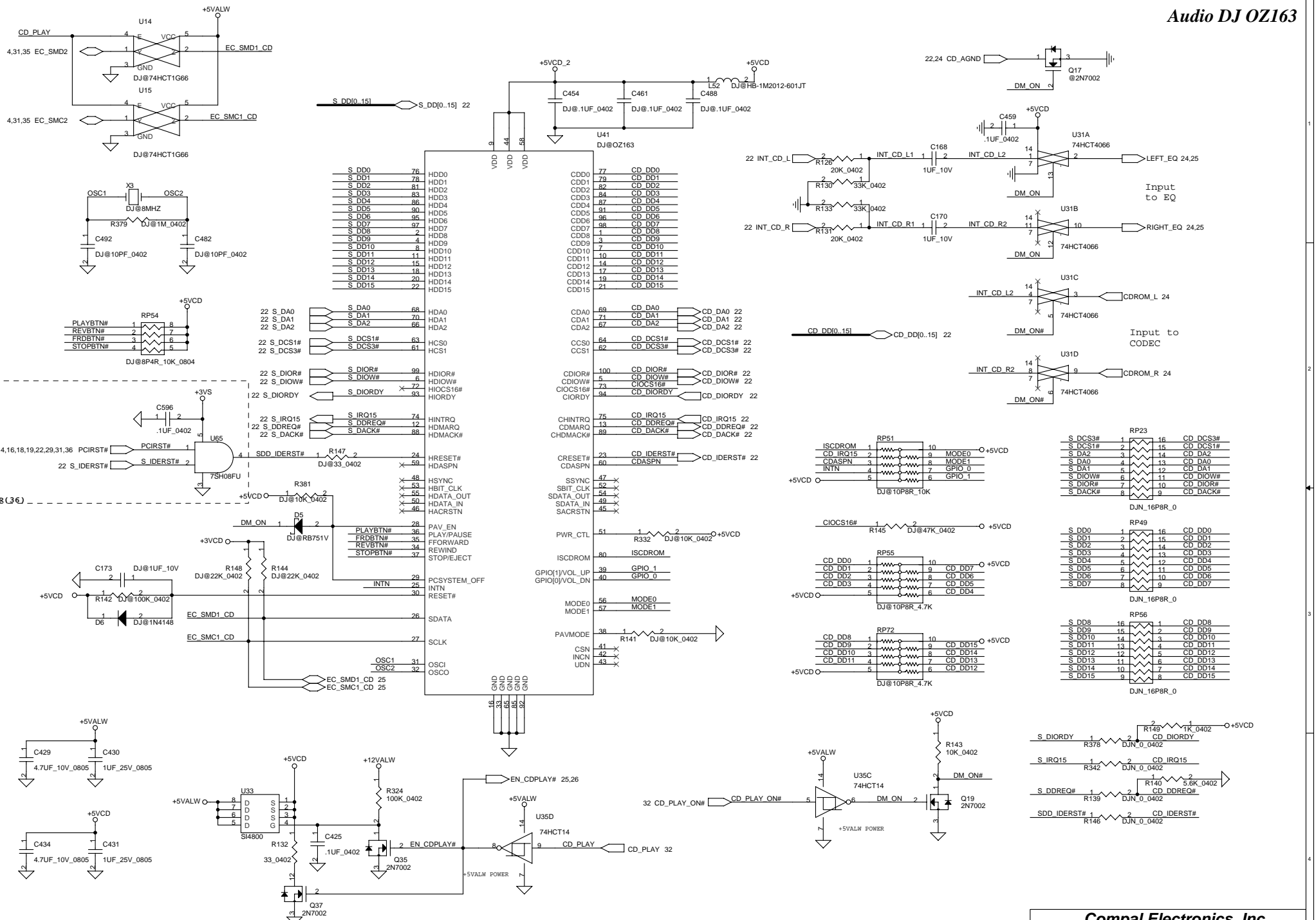
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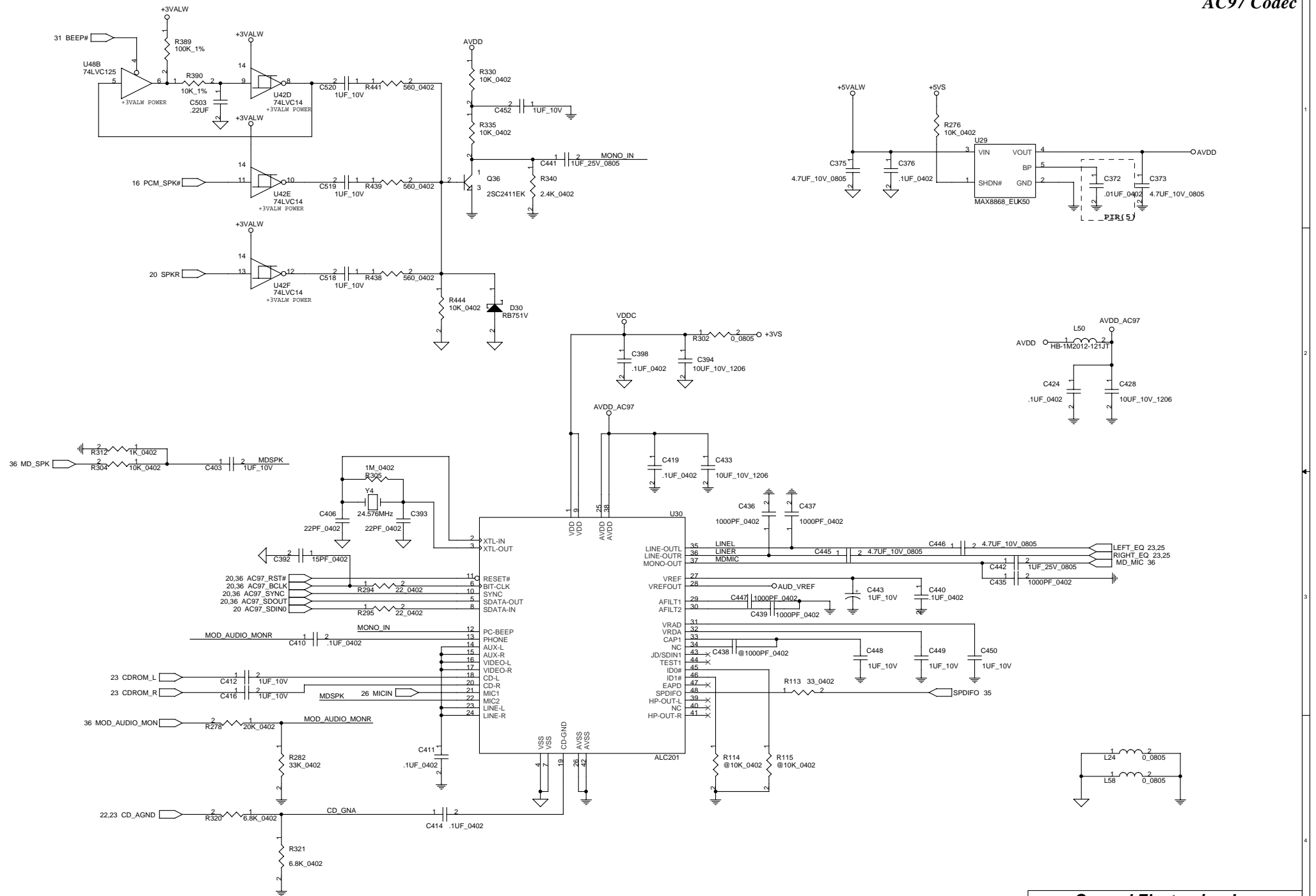
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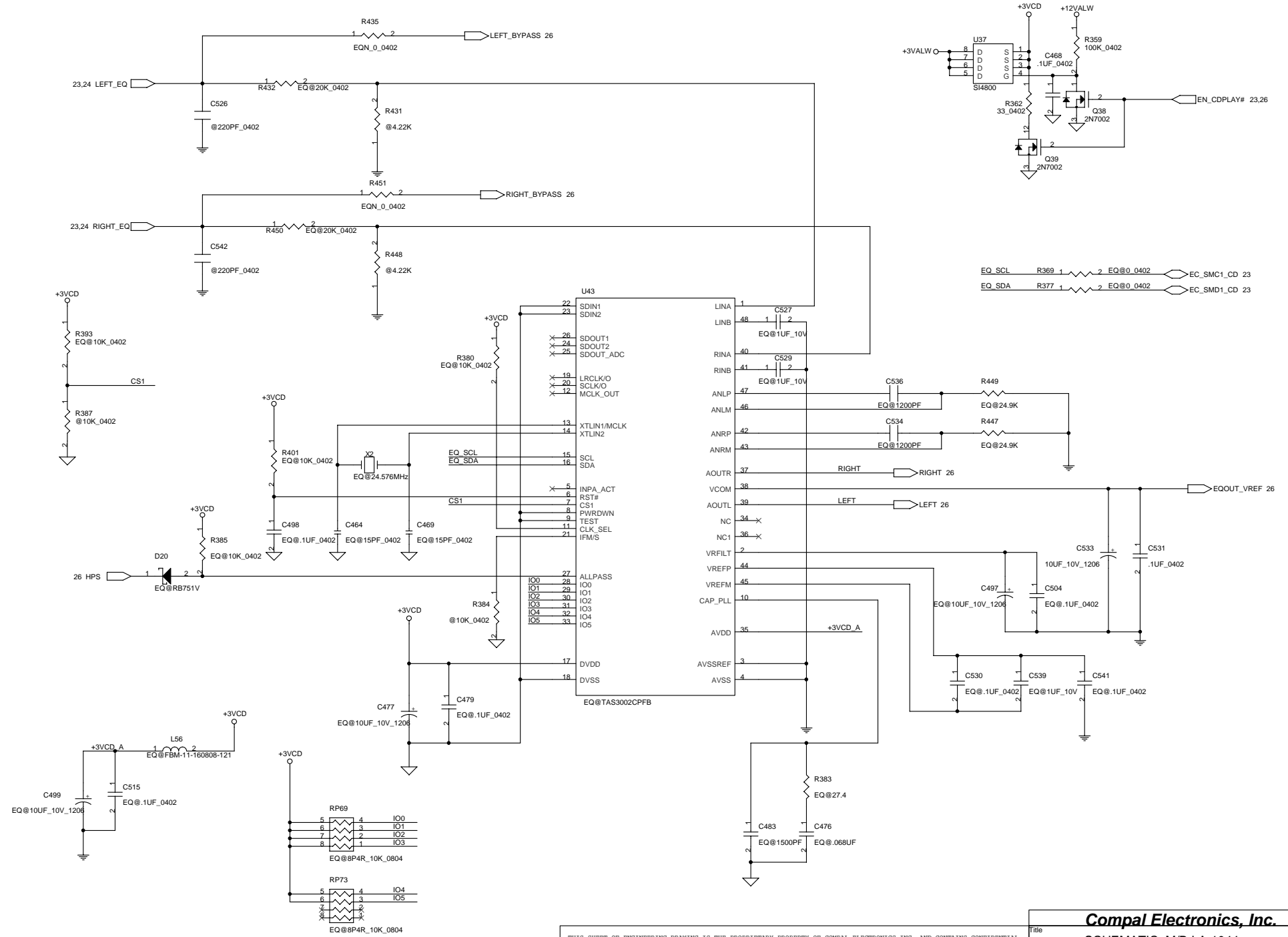


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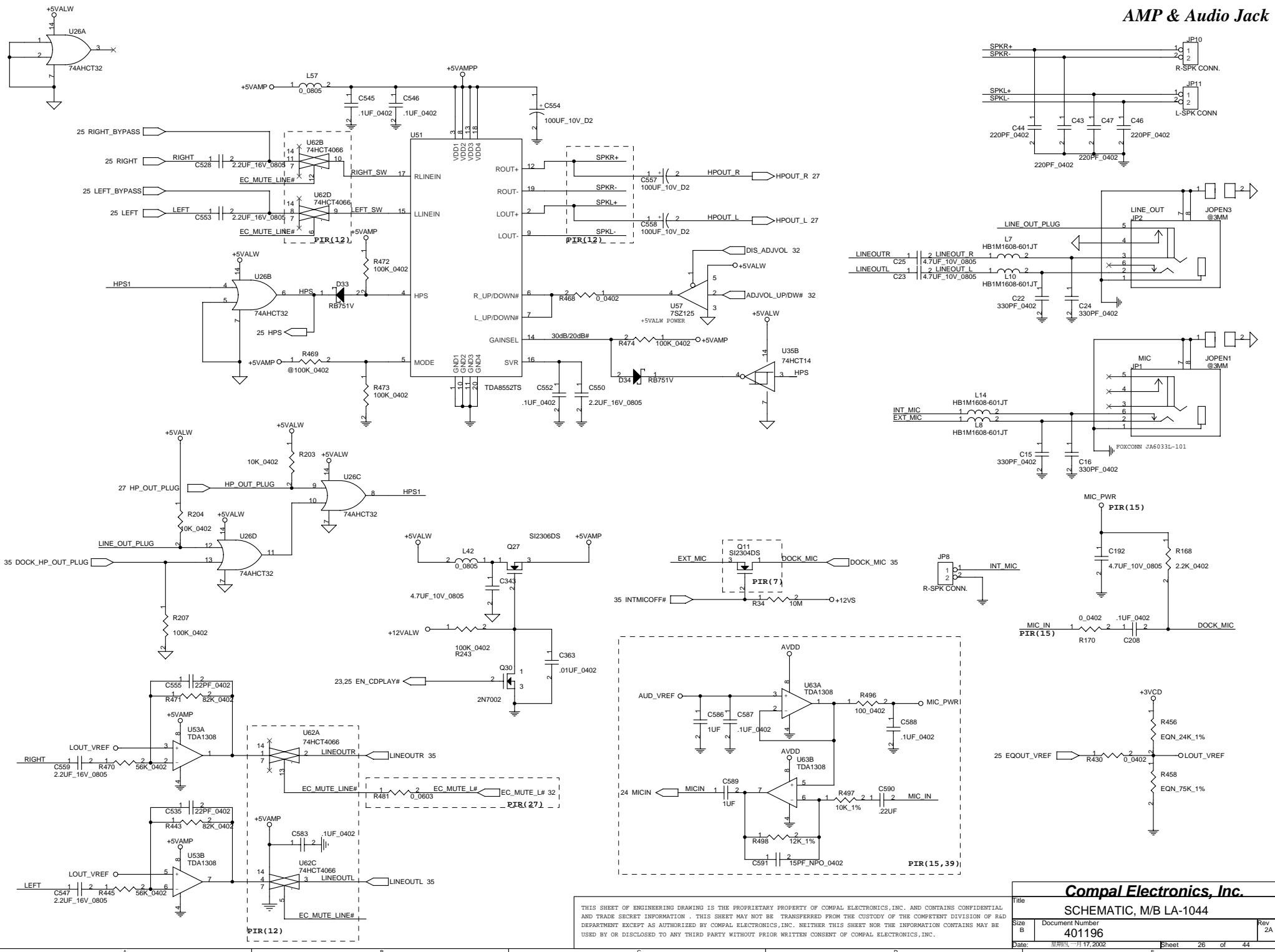
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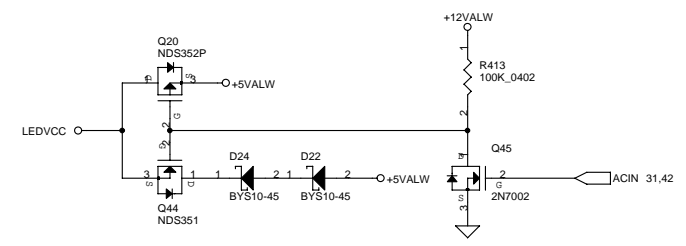
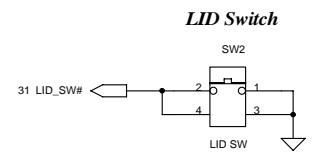
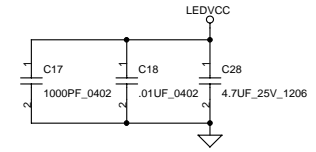
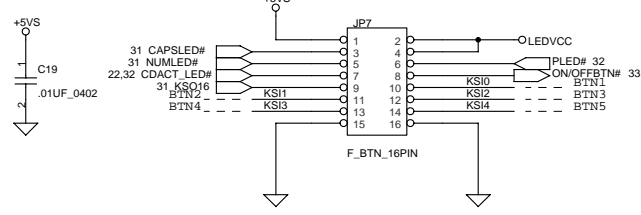
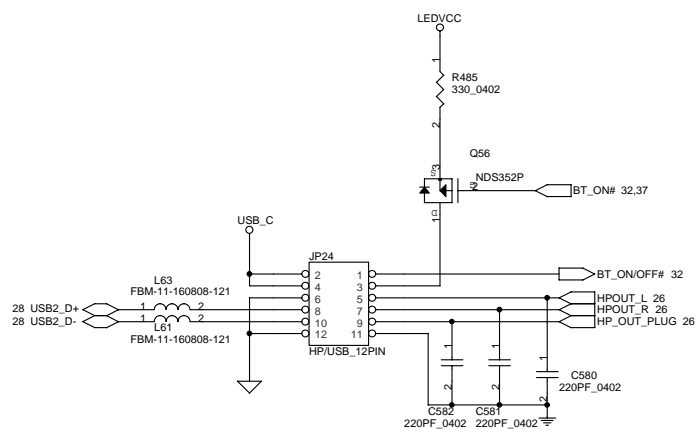
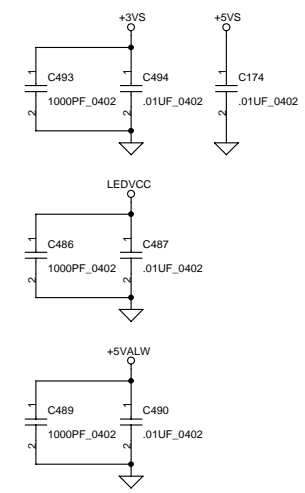
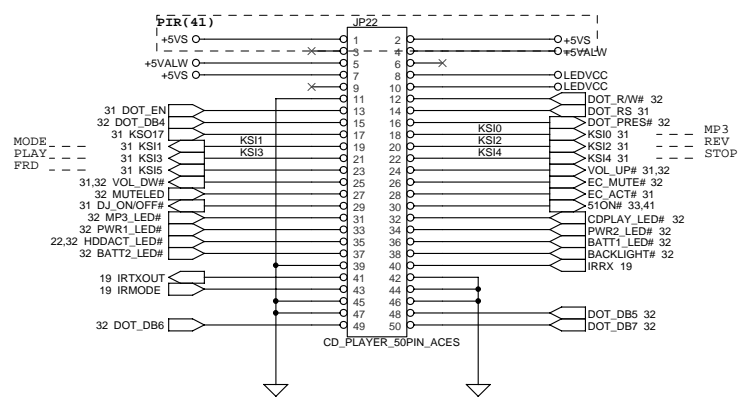
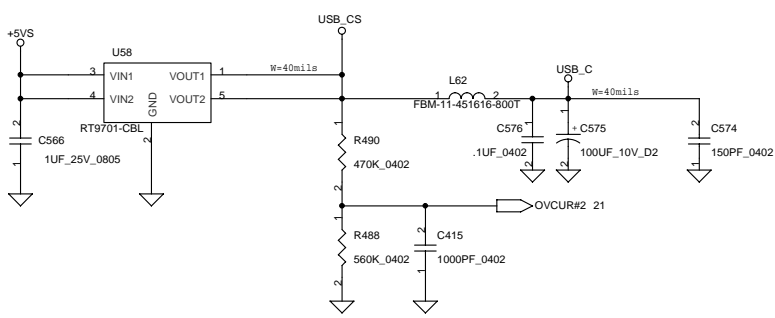
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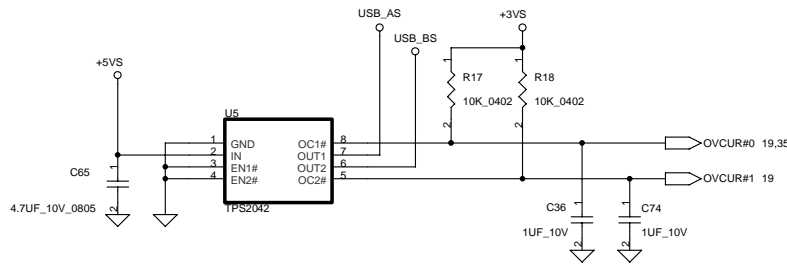
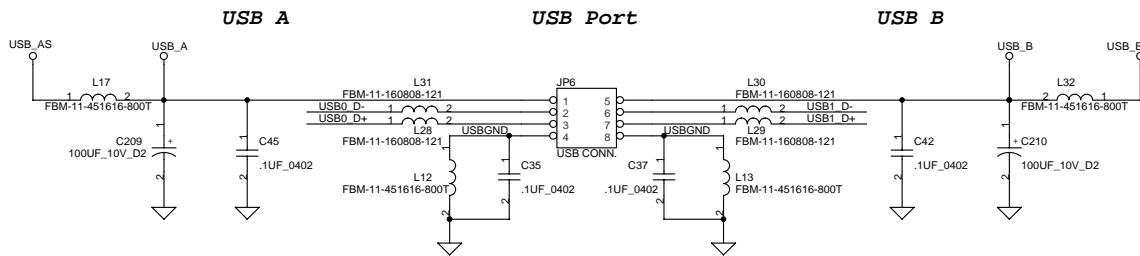
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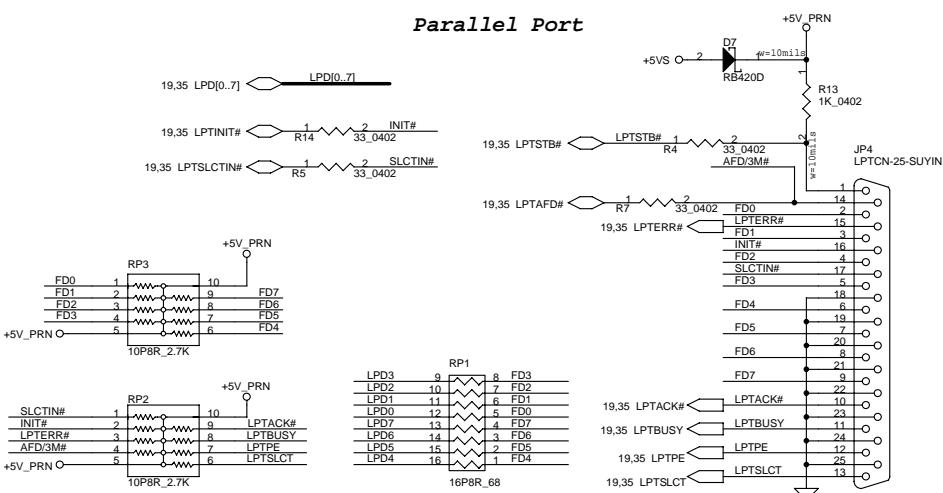


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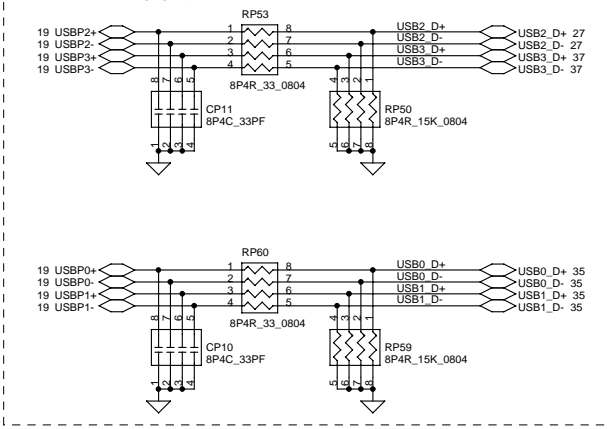
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Parallel Port

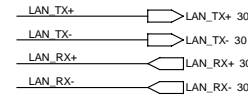
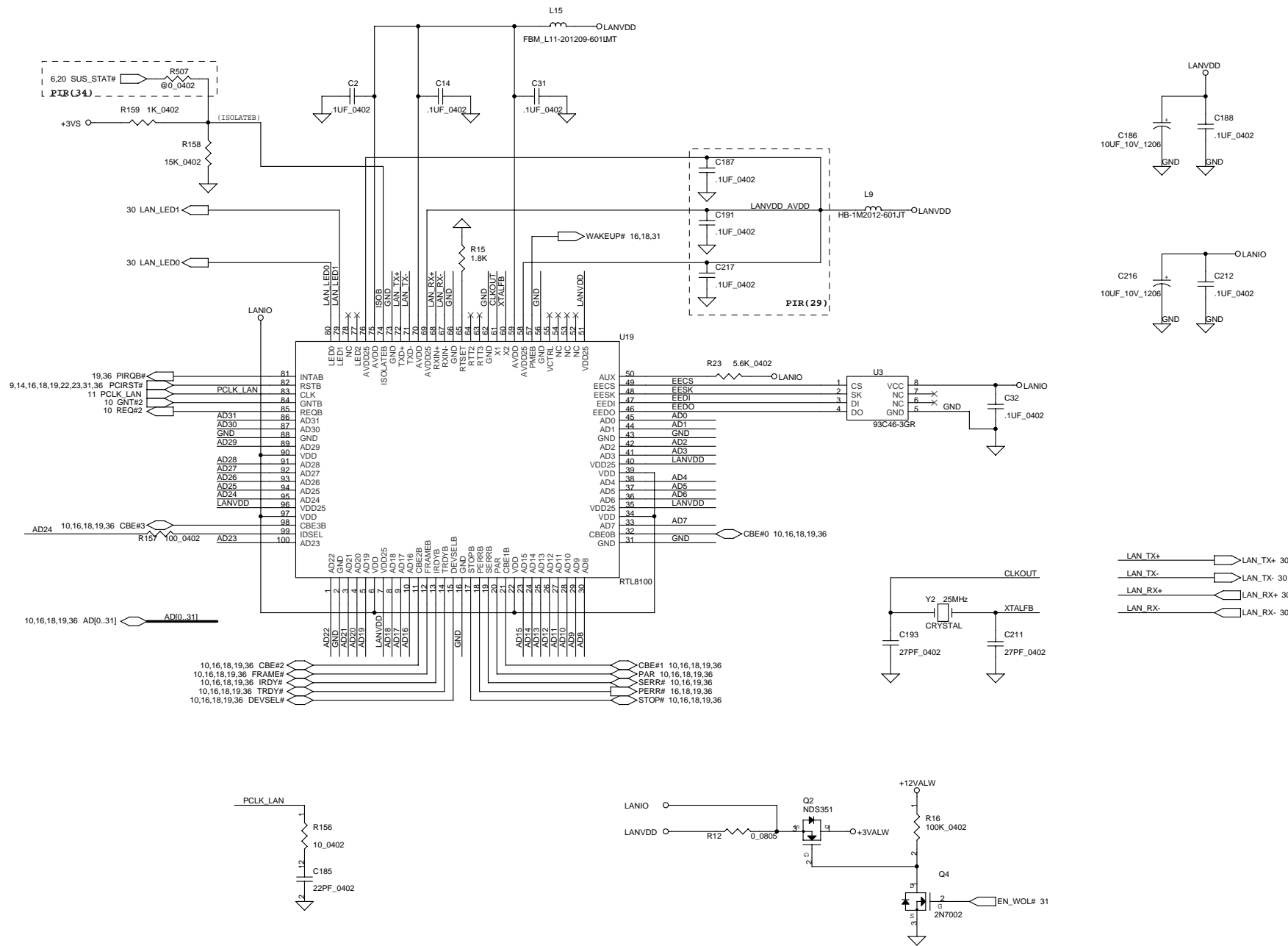


The component's most place cloely VT8231.



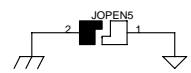
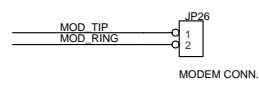
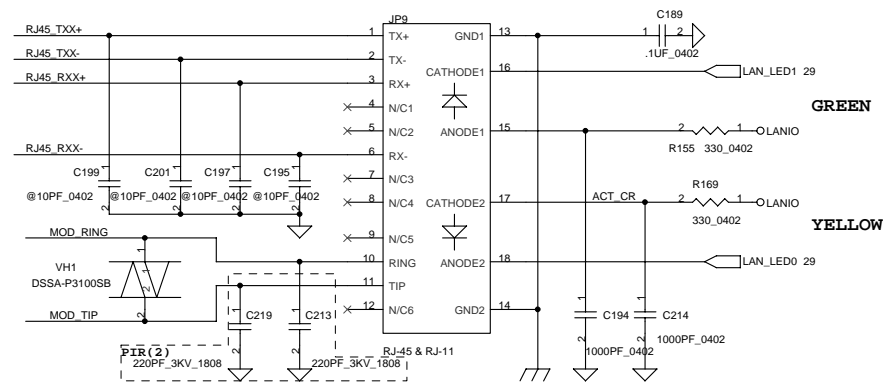
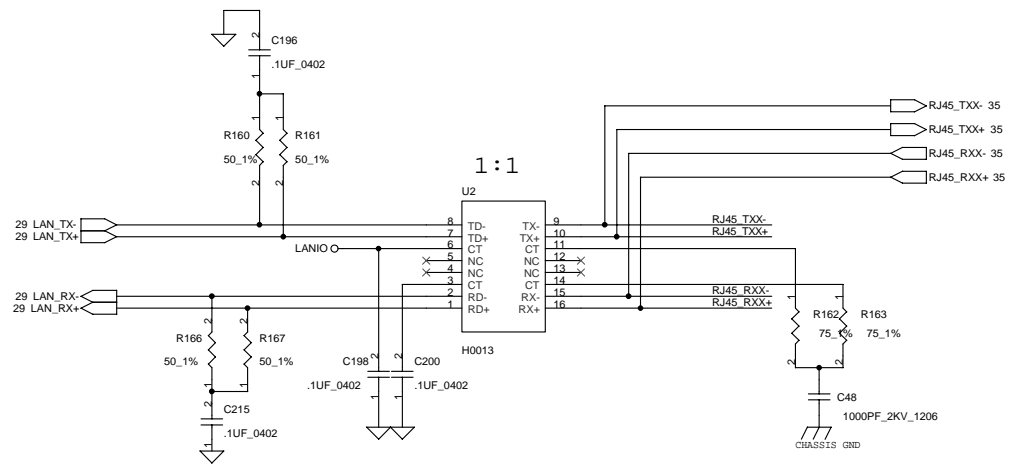
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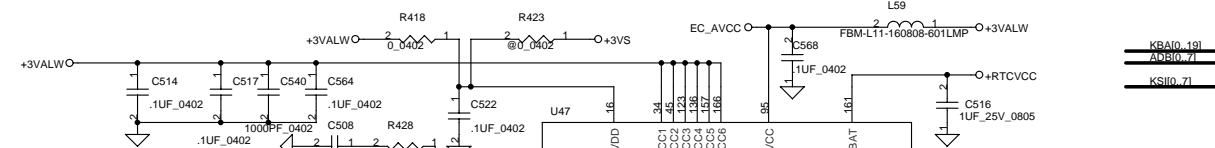
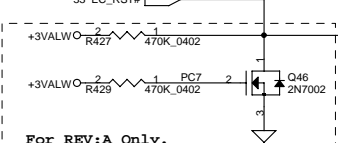
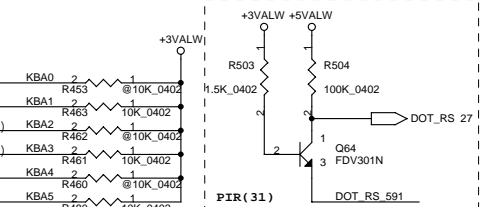
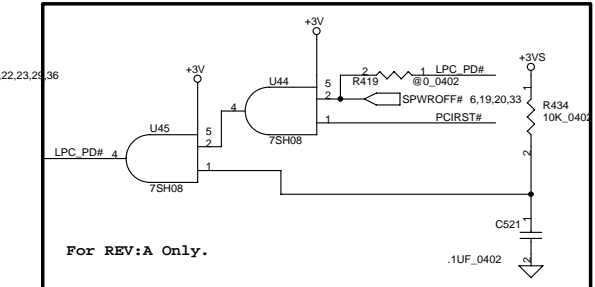
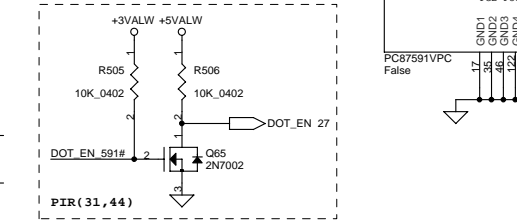
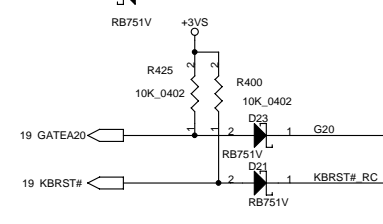
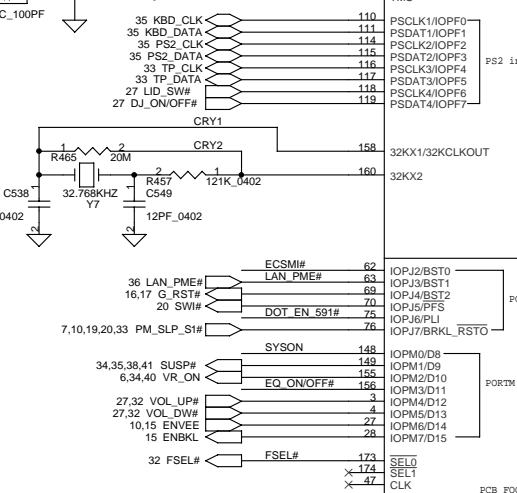
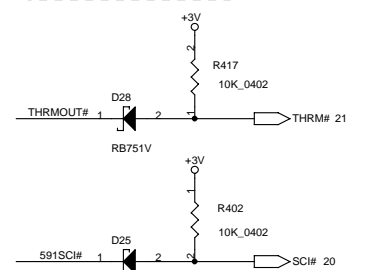
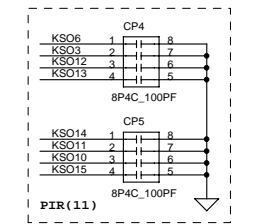
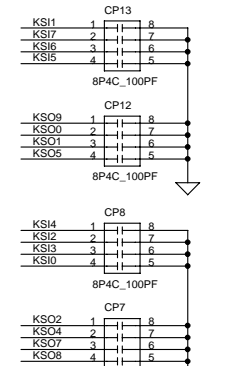
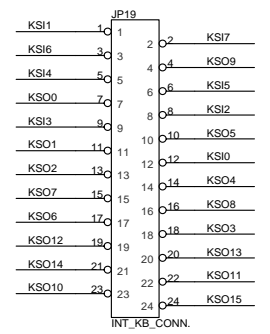


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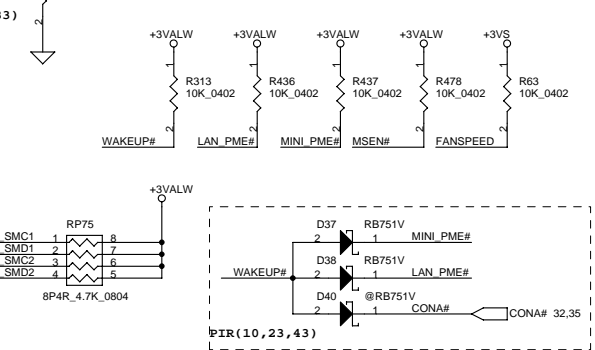
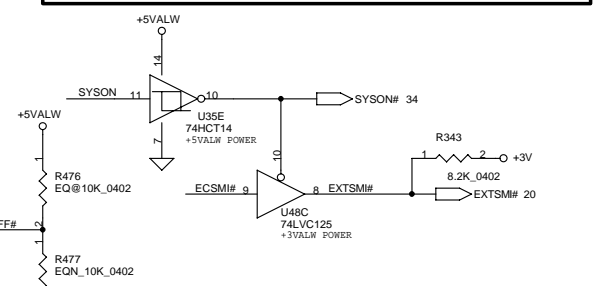


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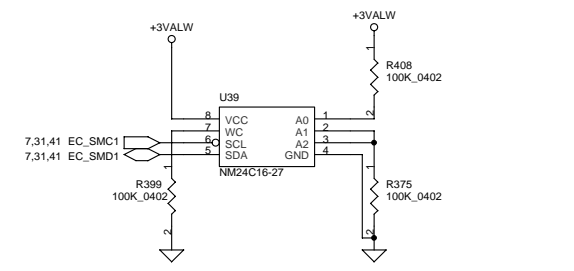
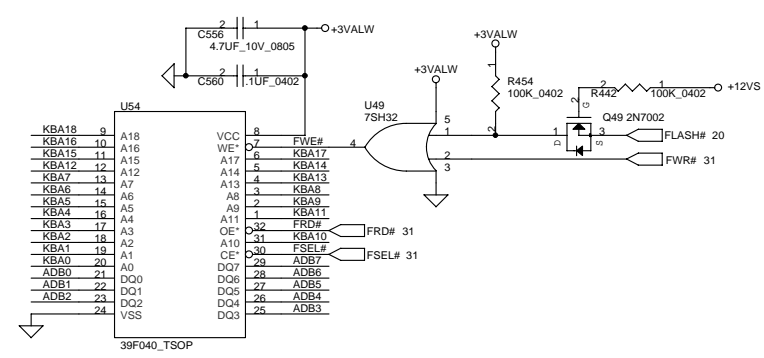
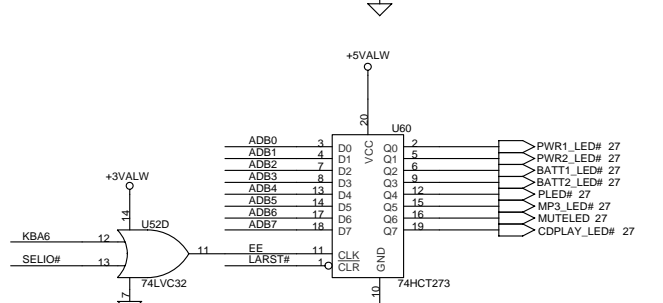
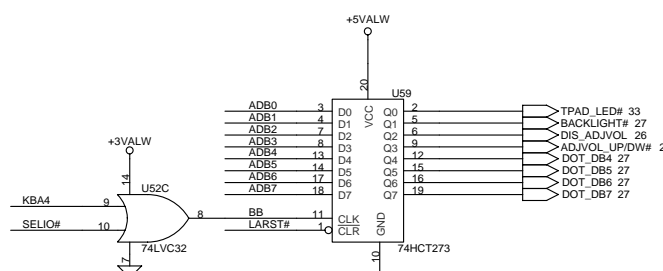
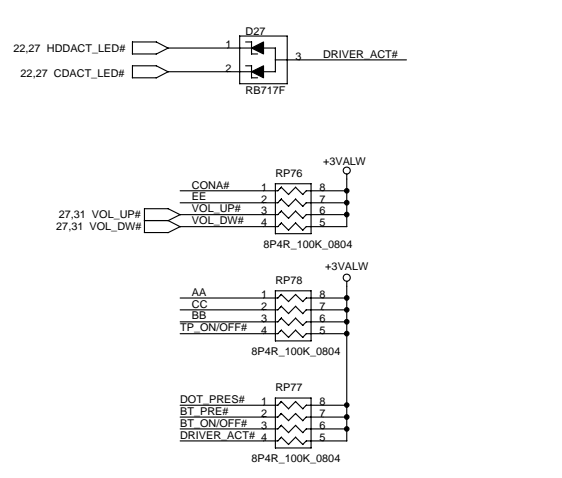
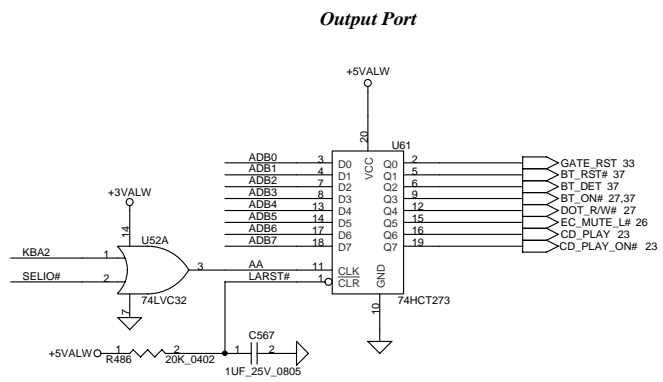
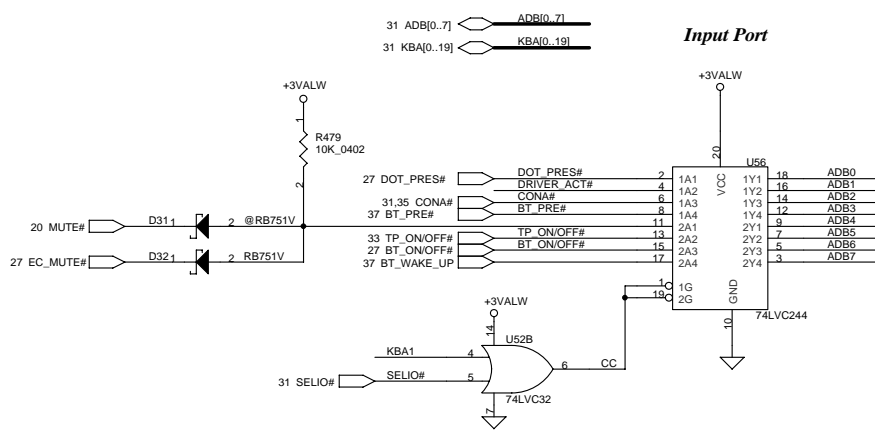
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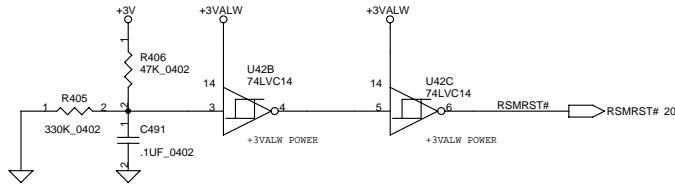


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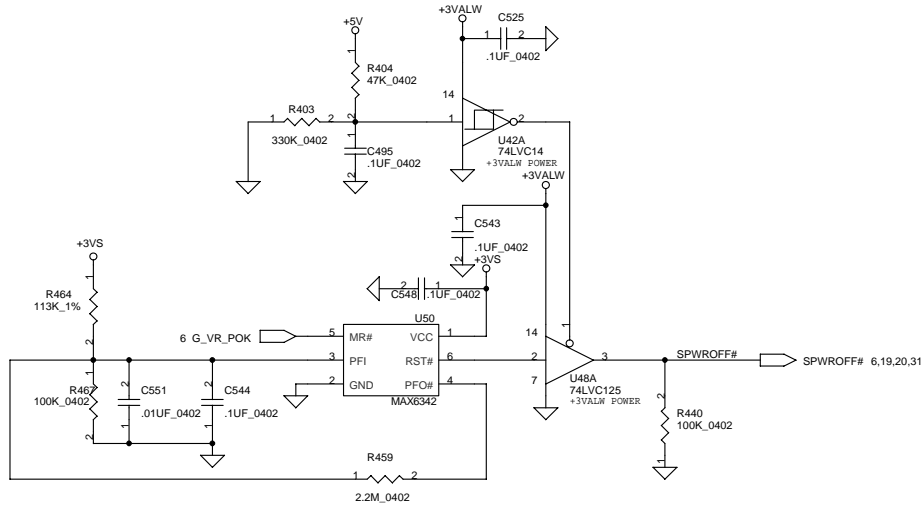


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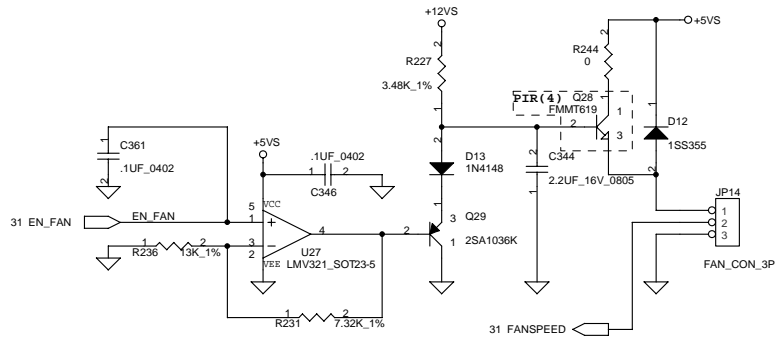
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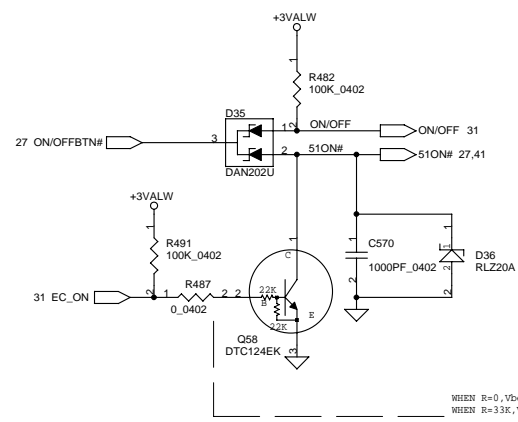
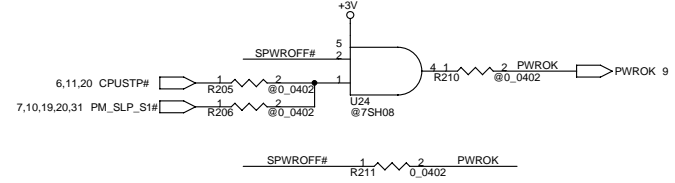
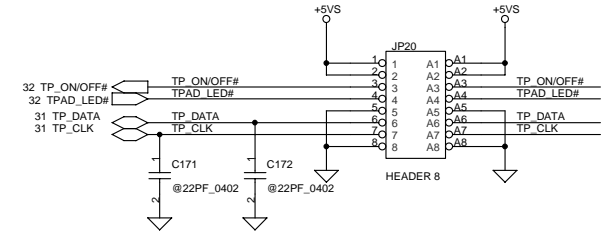
PWR ON CKT



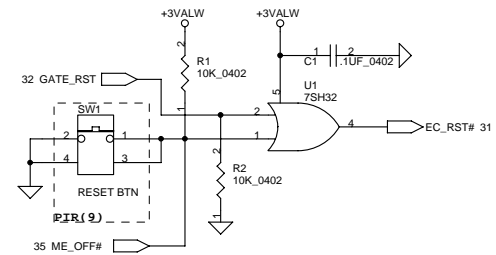
FAN Connector



Second FAN connector
P1R(13, 32)



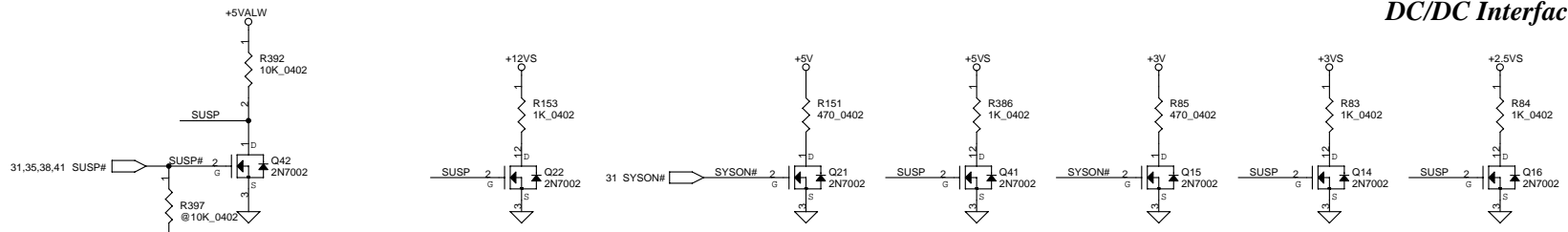
M/E OFF Button



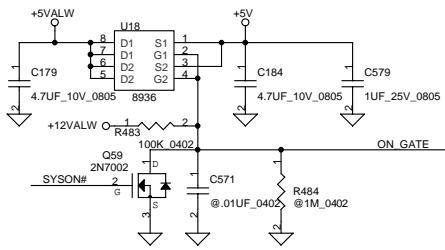
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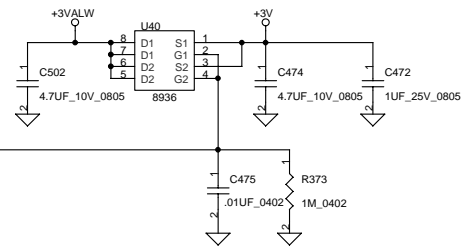
DC/DC Interface & RTC



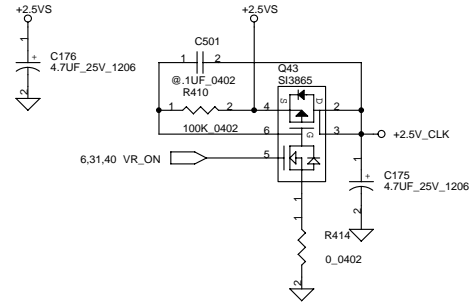
+5VALW To +5V Transfer



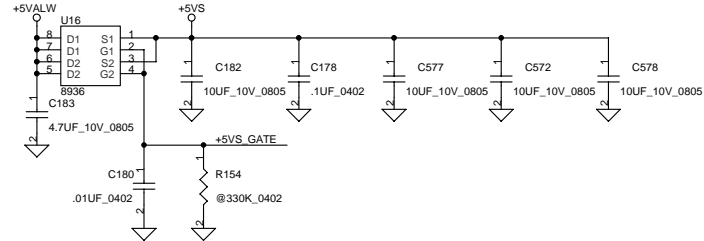
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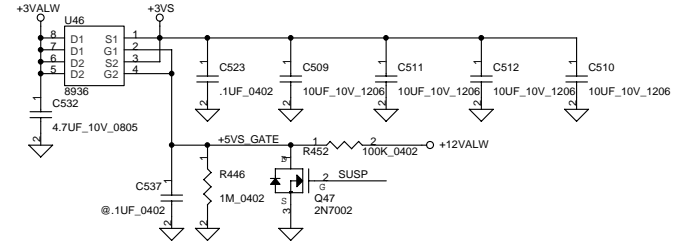
+2.5VS To +2.5VCLK Transfer



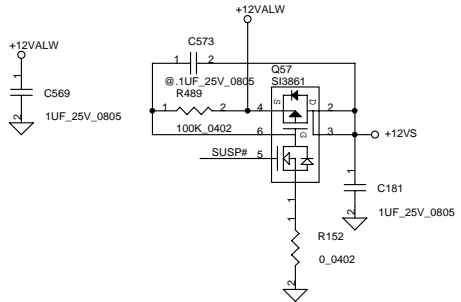
+5VALW To +5VS Transfer



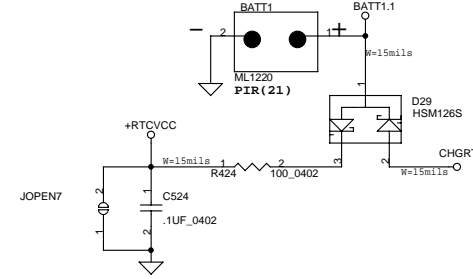
+3VALW To +3VS Transfer



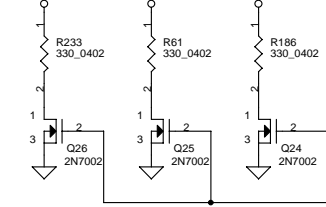
+12VALW To +12VS Transfer



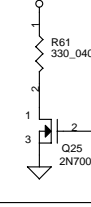
RTC BATT



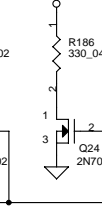
+2.5V_CLK



+VCPU_IO

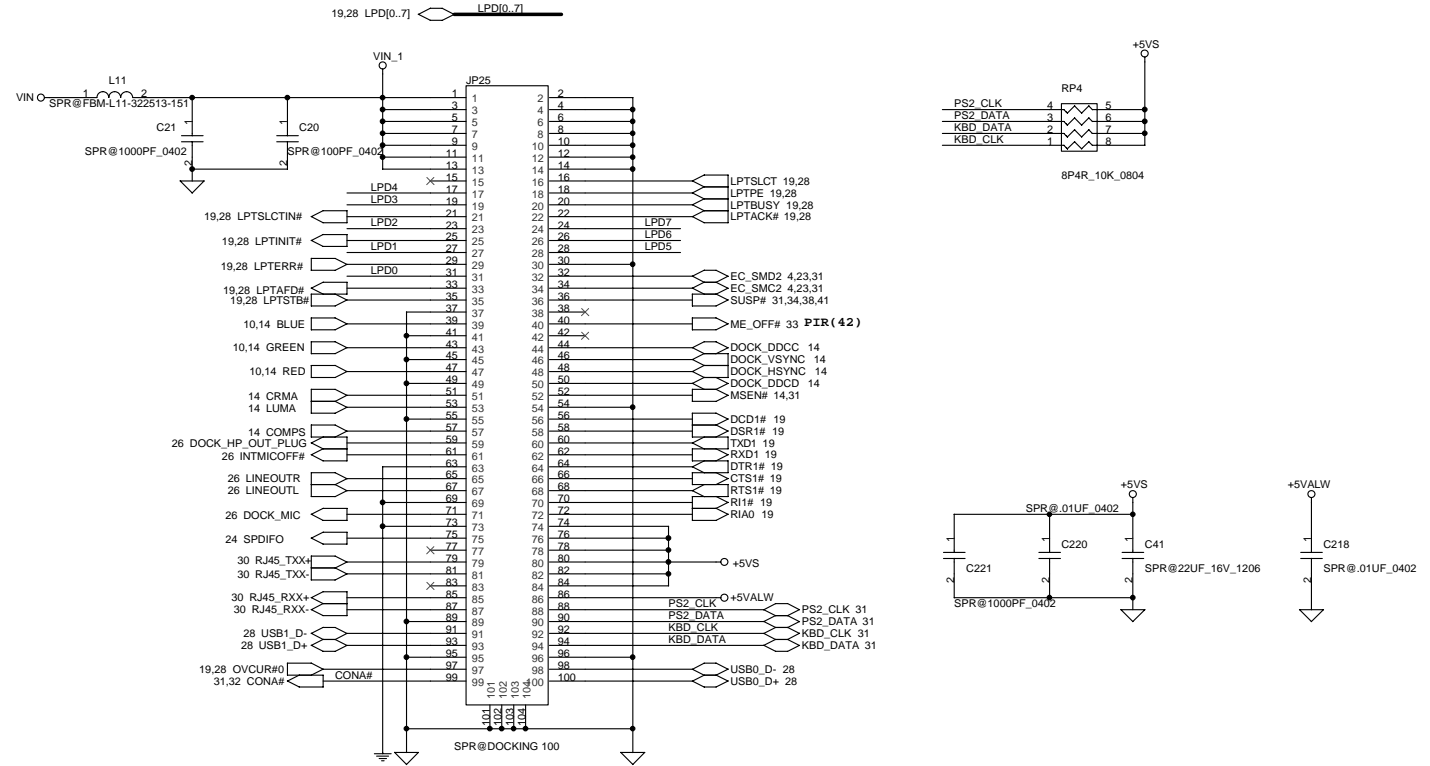


+CPU_CORE



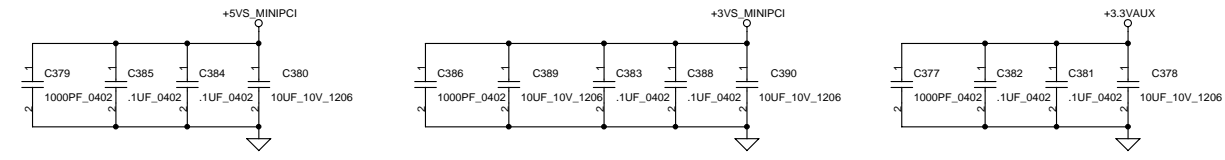
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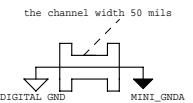
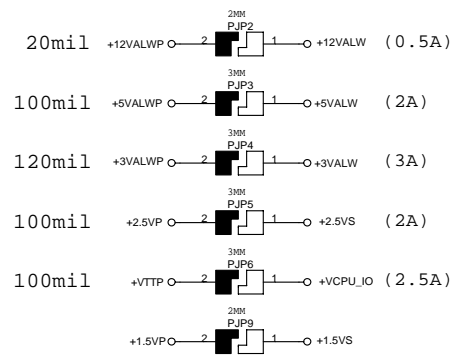
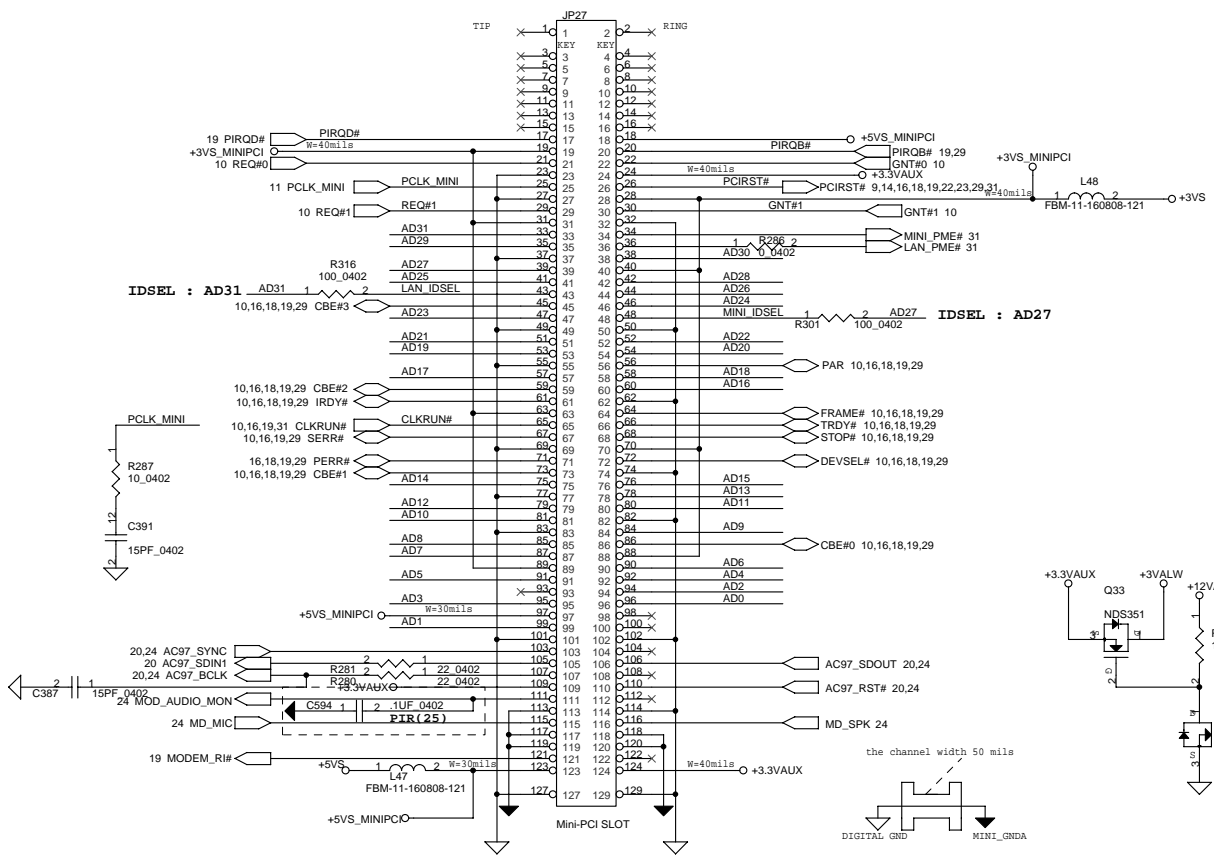


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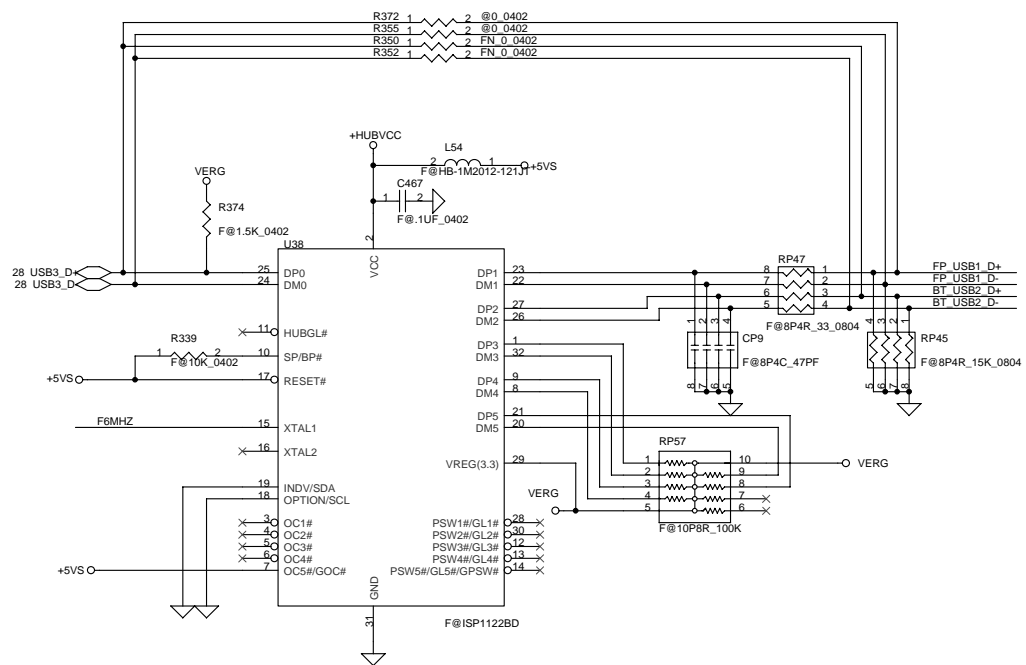


AD[0..31] AD[0..31] 10,16,18,19,29

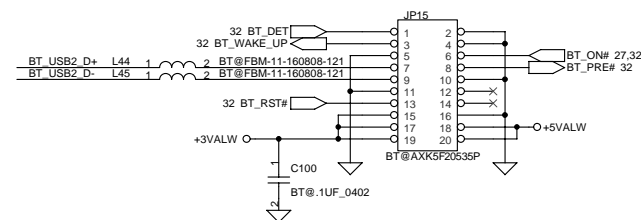


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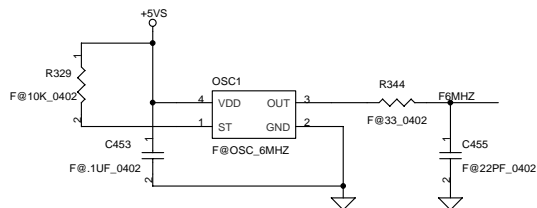
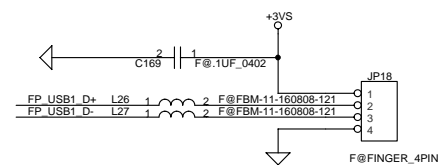
<p>Compal Electronics, Inc.</p> <p>SHEMATIC, M/B LA-1044</p>		
<p>Title</p>	<p>Document Number</p> <p>401196</p>	<p>Rev</p> <p>2A</p>
<p>Date</p> <p>2002年11月17日</p>	<p>Sheet</p> <p>36</p>	<p>of</p> <p>44</p>



Bluetooth Connector

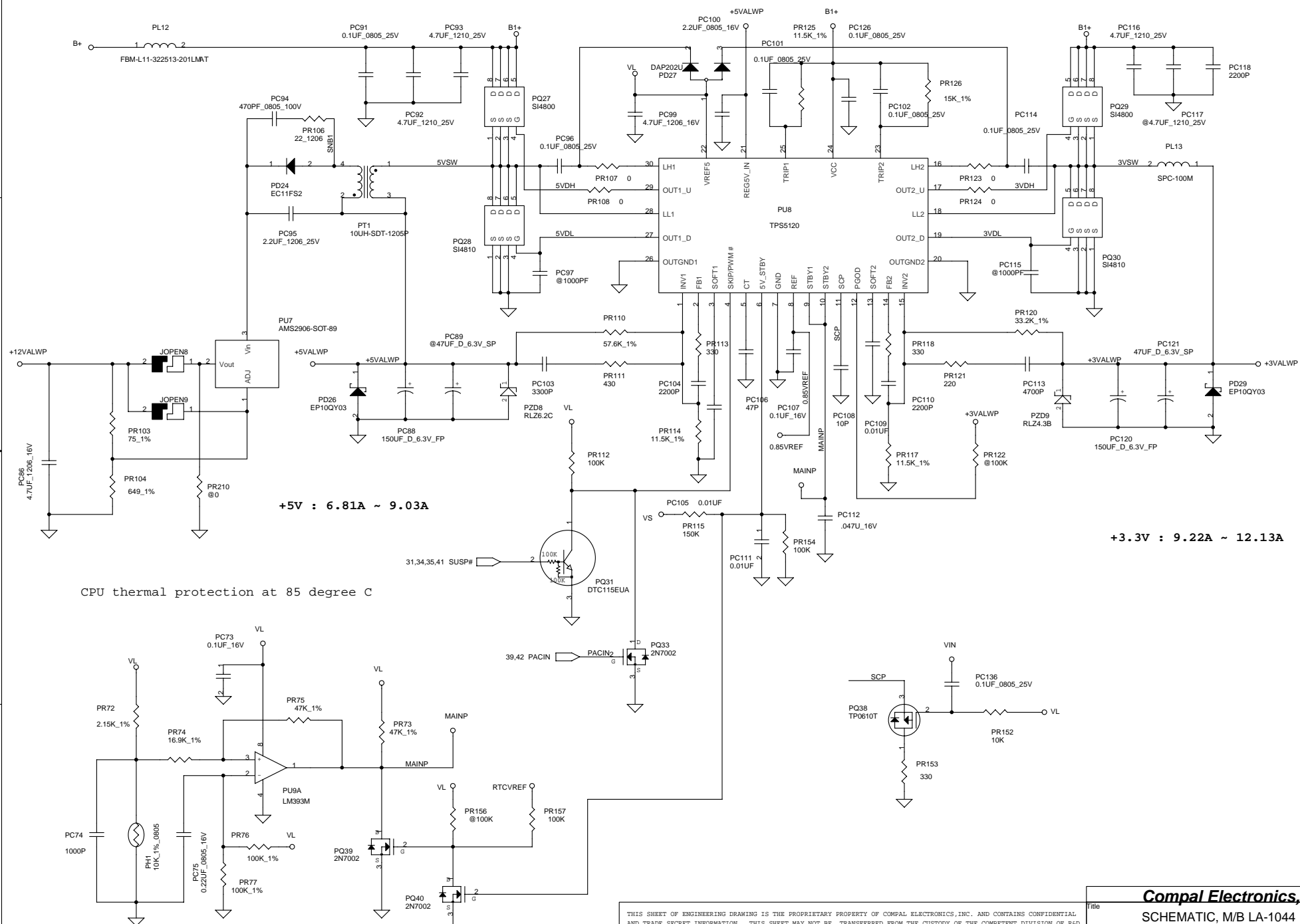


Finger Printer Connector



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+5V : 6.81A ~ 9.03A

+3.3V : 9.22A ~ 12.13A

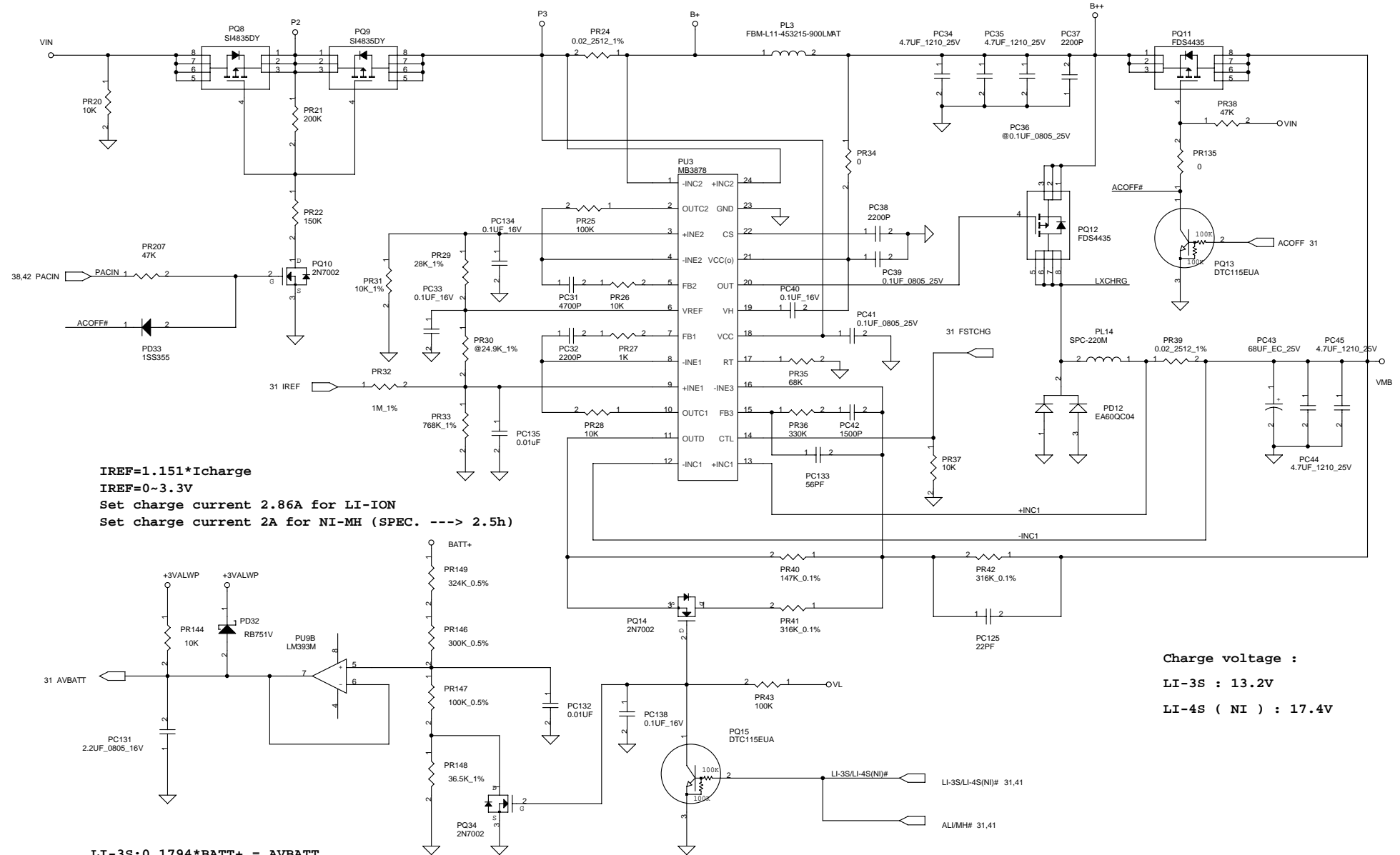
CPU thermal protection at 85 degree C

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I_{adp}=0~2.60A
Air-line:50W

Charger



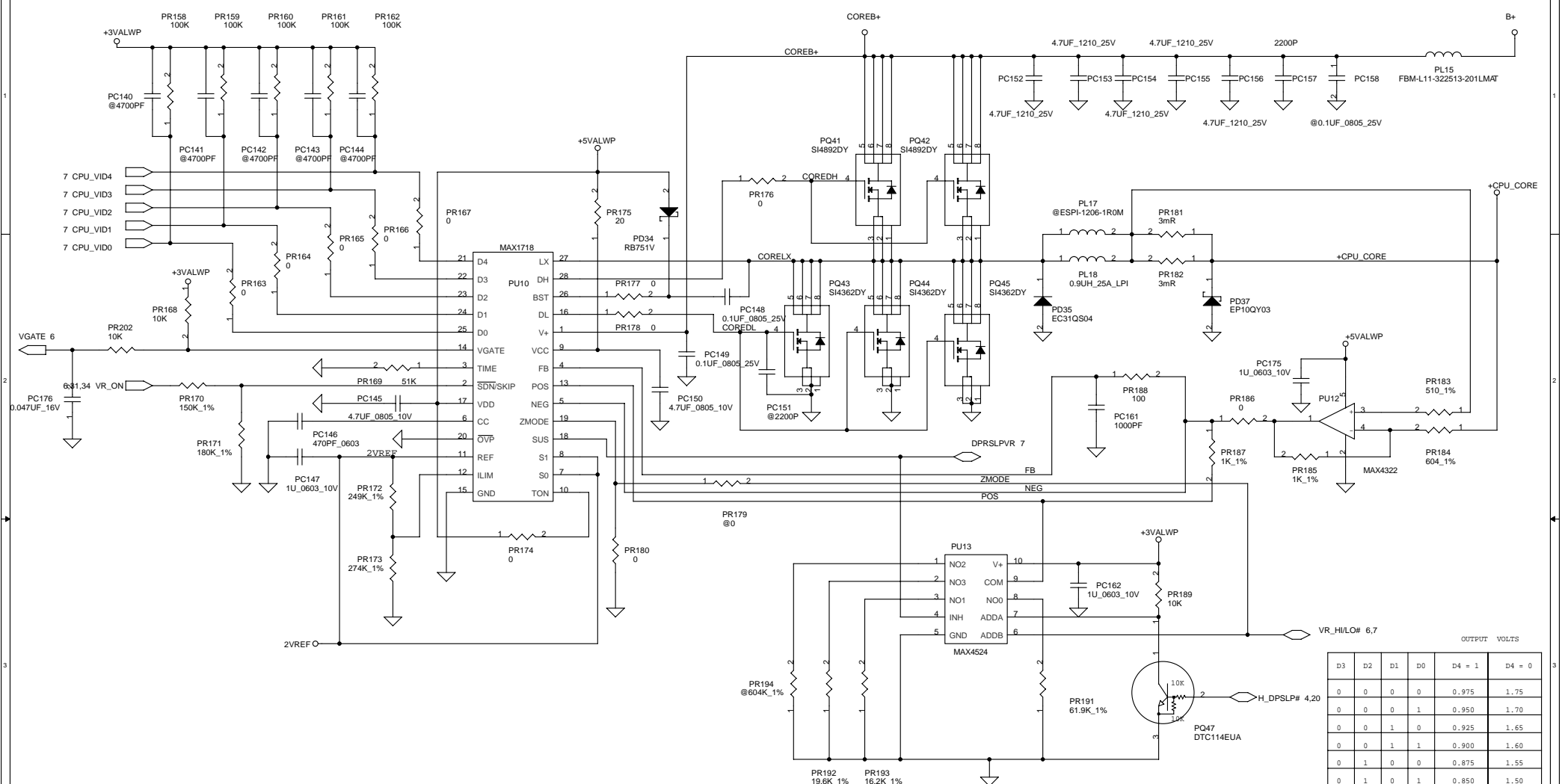
IREF=1.151*I_{charge}
IREF=0~3.3V
Set charge current 2.86A for LI-ION
Set charge current 2A for NI-MH (SPEC. ---> 2.5h)

Charge voltage :
LI-3S : 13.2V
LI-4S (NI) : 17.4V

LI-3S:0.1794*BATT+ = AVBATT
LI-4S(NI):0.1381*BATT+ = AVBATT

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MODE	OFFSET	RBOTTOM	VoLte (ΩA)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.950	X	X
BATTERY SLEEP	-9mV	16.2K	1.083	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.332	1	1
BATTERY MODE	-16mV	61.9K	1.131	0	0
PERFORMANCE MODE			1.400	0	1

OUTPUT VOLTS					
D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	0	0	1	0.950	1.70
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

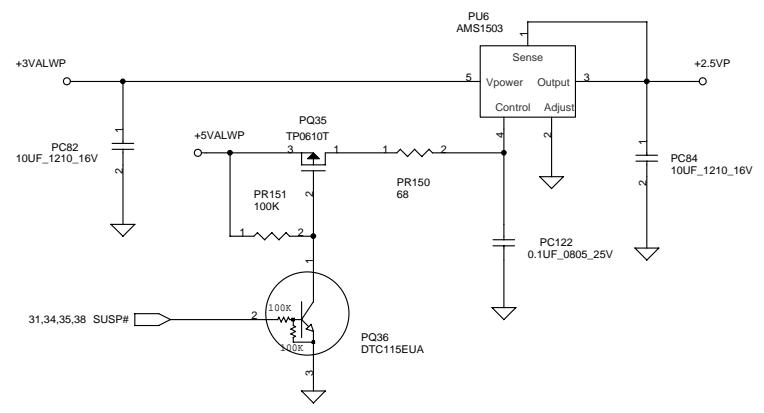
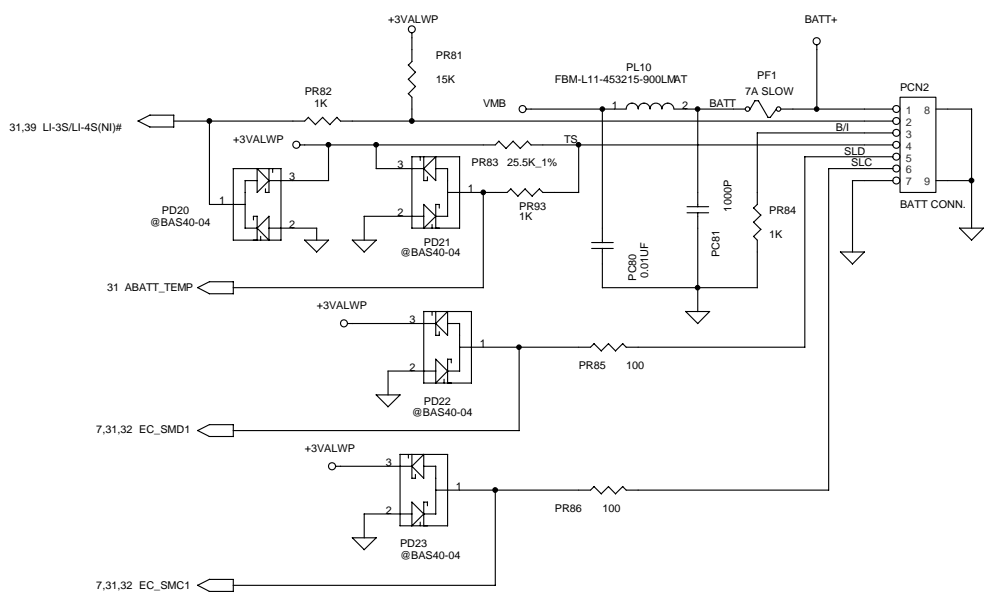
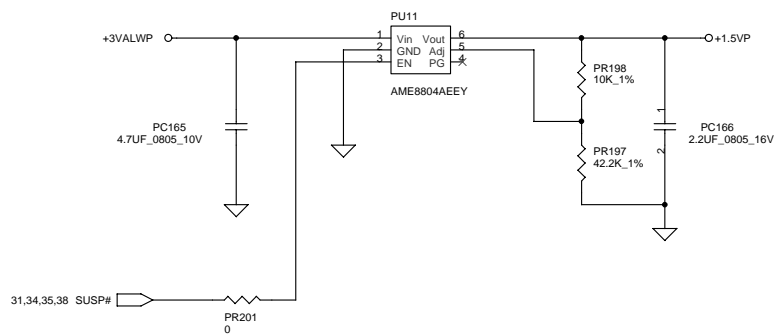
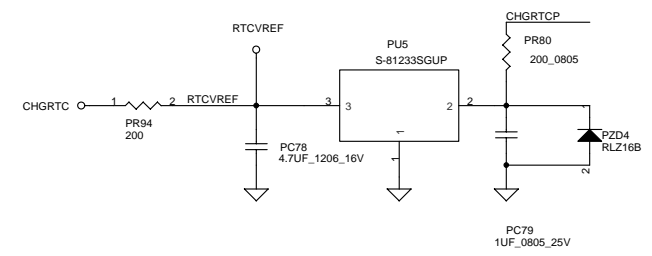
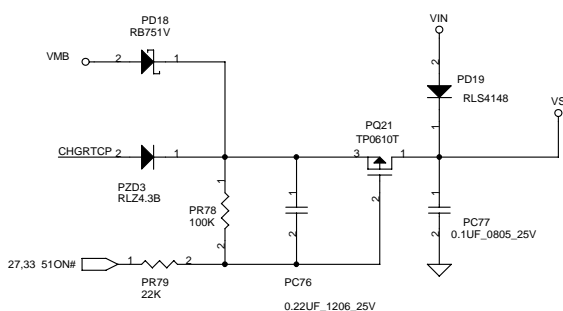
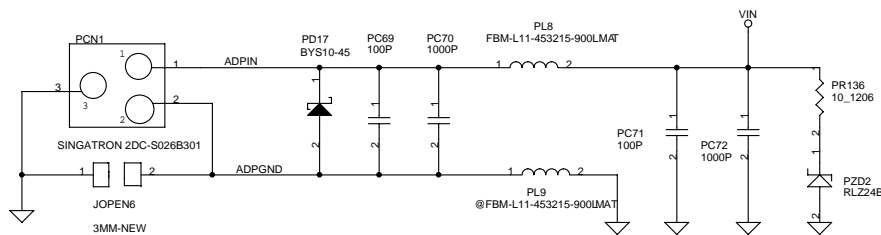
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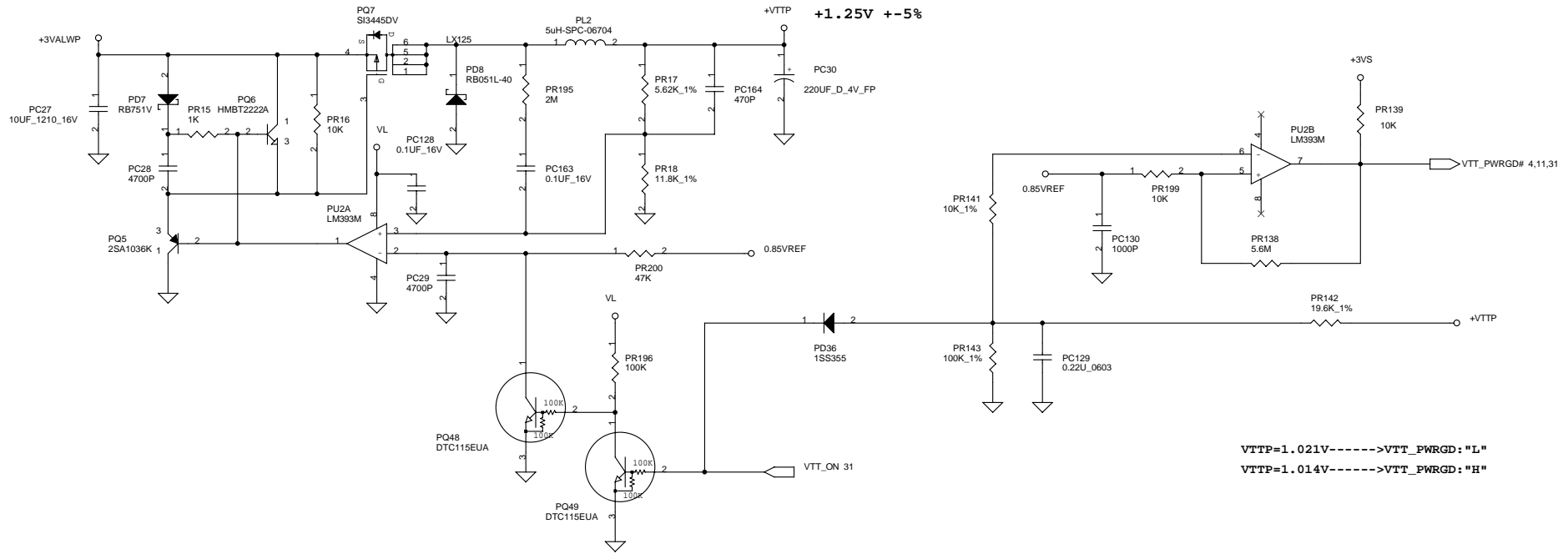
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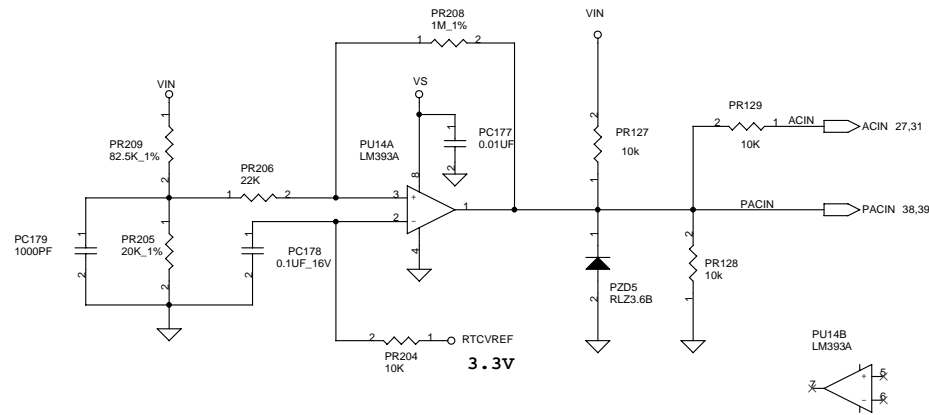
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VIN detector		
16.90	17.55	18.22
16.46	17.08	17.72

Detector



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_IO	1.25V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for TwisterT(VT8606) core power.	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Mini-PCI	AD27	0	PIRQB#
Mini-PCI(LAN)	AD31	1	PIRQD#
LAN(RTL8100)	AD24	2	PIRQB#
CardBus(CB1410)	AD15	3	PIRQA#
IEEE-1394 Controller	AD25	4	PIRQC#

EC SM Bus1 address

Device	Address
CPU voltage Mux	0110 1110 b
Smart Battery	0001 011X b
EEPROM	1010 000X b

EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Docking	0011 011X b

P.S:Default Resistor & Capacitor's package are 0603.
Default 8P4R package is 0402.

For C1-test

1.Solving can't boot-up issue.

Pull-high(R492;200 ohm) I TP_PREQ# to +VCPU_I/O.

2.For solving high voltage test fail issue.

Change C219,C213 from 1000P_2KV_1206 to 220P_3KV_1808.

3.To avoid the chipset enter an unpredictable state.(VIA's recommend by AN198)

Add two 1K ohm pull-high resistor at R217,R222.

4.Change Q28 from 2SC2411EK(P=0.2W) to FMMT619(P=0.625W) for increasing system reliability.

5.For solving Microphone noise issue.

Change C372 from 0.1uF to 0.01uF.

6.For solving 1.06GHz QS CPU speed detect incorrect issue.

Add Q60 2N7002

Add Q61 DTC124EK

Add R494 100K_0402

7.Exchange Q11.1 and Q11.3 for solving external MIC. can't be disable on docking side.

8.Cahnge R35,R37 from TV@4.7K_0402 to 4.7K_0402 for solving B3C082.

9.For solving ESD fail issue.

Exchange SW1.1,SW1.3 with SW1.2,SW1.4

10.For solving EC can't resume from idle mode issue.

Add D37 and D38.(RB751V)

11.For EMI requirement.

Add CP4,CP5 8P4C_100PF.

12.For solving audio sound can't be muted issue.

Del Q48,Q50,Q51,Q52,Q53,Q54,Q55,R455.

Add U62(74HCT4066),C583(0.1UF).

13.Reserve for second FAN.

Add JP29,C584(0.1UF),D39(1N4148),Q62(NDS351),R495(0_0402).

14.For solving SDRAM clock timing can't meet PC133 specification issue.

Del R234,R121,R325,R104,R68,R80

Del C345,C166,C427,C150,C105,C129

15.For solving the record sound is much weaker issue.

Add U63(TDA1308)

Add R496(100_0402)

Add R497(10K_0603_1%)

Add R498(22K_0603_1%)

Add C588(0.1UF_0402)

Add C590(0.22UF_0603)

Add C591(15PF_NPO_0603)

Add C586(1UF_0603)

Add C587(0.1UF_0402)

Add C589(1UF_0603)

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16. For solving Celeron-T CPU can't power on issue.(Celeron-T SKU only)

Add Q63(FDV301N)
Add R499(1.5K_0402)

17. VIA recommend. It can increasing +VCPU_IO power plan noise immunity.

Add C592(1000PF_0402)
Add C593(1UF_0402)

18. To change CardBus power switcher from CP2211(ENE) to TPS2211(TI).

19. To change 133MHz from +/-0.25% center spread to -0.5% down spread.

Del R196(137_1%_0402)
Change R194 from 26.7_1%_0402 to 0_0402.

20. To change clock generator from ICS950602 to CY28317 for solving system up issue.

21. Change RTC battery from VL1220(Panasonic) to ML1220(Maxell) for purchase policy.

22. Intel recommend that change +VS_CMOSREF voltage divider from 1K/2K to 510/1K.

Change R230 from 1K ohm to 510 ohm.
Change R235 from 2K ohm to 1K ohm.

23. EC team change their SPEC. for support dock-on to wake up EC(591).

Add D40.

24. Add a pull high resistor(R500,47K ohm) for solving cardbus card can't be detected.

25. For solving audio noise from PHONE channel.

Add C594,0.1UF_0402.

26. For EMI team requirement.

1. Change R256,R252,R240,R239 from 0_0402 to 22_0402.
2. Change R246,R238,R247 from 0_0402 to 10_0402.
3. Change R257,R245,R251,R253 from 0_0402 to 33_0402.
4. Change RP9-RP13,RP17-RP20,RP24-RP26,RP32-RP34,RP36.

27. For solving c-test unit can't power-on issue.(2001/9/20)

Change net "EC_MUTE#" to "EC_MUTE_L".
Change R481 from 10M ohm to 0_0603.

28. For Intel PMU SPEC. and SKU change.(2001/9/25)

1.)For all SKU.
Del R79(1.2K_0402)
Del C116(1UF_10V)
Del U11(7SH32)
2.)For Tualatin SKU only.
Stuff R78,C118,U9,R493,U10,R349
3.)For Celeron-T SKU only.
Stuff R501

29. Increasing LANVDD power plan noise immunity.(2001/9/25)

Add C187,C191,C217(1UF_0402)

For C2-test

30. BIOS can't support C4 and deeper sleep mode,so delete unnecessary components for all of the Tualatin CPU SKU.(2001/10/11)

Del U9,U10,R493,U12,C117,R74,R76,R72,RP21,R78,C118.
Add R501(0_0402),R502(0_0402),RP79(8P4R_0).

31. Build two sets level shifter for solving CD-player board unstable issue.(2001/10/11)

Add Q64,Q65(FDV301N).
Add R503,R505(1.5K_0402).
Add R504(100K_0402).
Add R506(1K_0402).

32. Delete second FAN circuit unnecessarily in all of SKU.(2001/10/11)

Del JP29,C584,Q62,D39,R495.

33. For solving wake up from Ring failure issue.(To divide On-board LAN and MINI-PCI card's AUX. power plan for saving power consumption.(2001/10/11)

34. Reserve R507(@0_0402) for BIOS team request.(2001/10/17)

35. SDRAM skew didn't met specification.(2001/10/17)

Add R234(10_0402),C345(15PF_0402).

36. For solving IDE bus reset incorrect issue.(2001/10/18)

Add U64,U65(7SH08FU).
Add C595,C596(1UF_0402).

37. For solving Celeron-T 933MHz CPU reboot fail issue.(2001/10/24)

Add R250(10_0402),R232(0_0402)
Add C598(1UF_0603) for Celeron-T SKU only.
Del R249,R314
Change R208 from 56.2_1%_0402 to 1K_0402.

38. To correct pull-up resistor error.(2001/10/24)

Del R290(1K_0402)
Add R508(4.7K_0402),R391(4.7K_0402)

39. For solving internal microphone echo issue.(2001/10/24)

Change R498 from 22K_1% to 12K_1%.

40. For solving PCIRST# from VT8231 has glitch issue. It causes system cold boot from LAN failure.(2001/10/24)

Add U66(7SH08FU)
Del R298.

41. Change JP22.1 & JP22.2 's power plan from +3VS to +5VS for increasing IR transmission distance.

For MP(REV1.0)

42. For solving system auto re-start while system hot dock to SPR.

Disconnection JP25.38 and JP25.42

43. EC team request.

Delete D40.

For MP(REV2.0)

44. For solving CD-Play board abnormal issue.

Change R505 from 1.5K_0402 to 10K_0402.
Change R506 from 1K_0402 to 10K_0402.
Change Q65 from FDV301N to 2N7002.

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