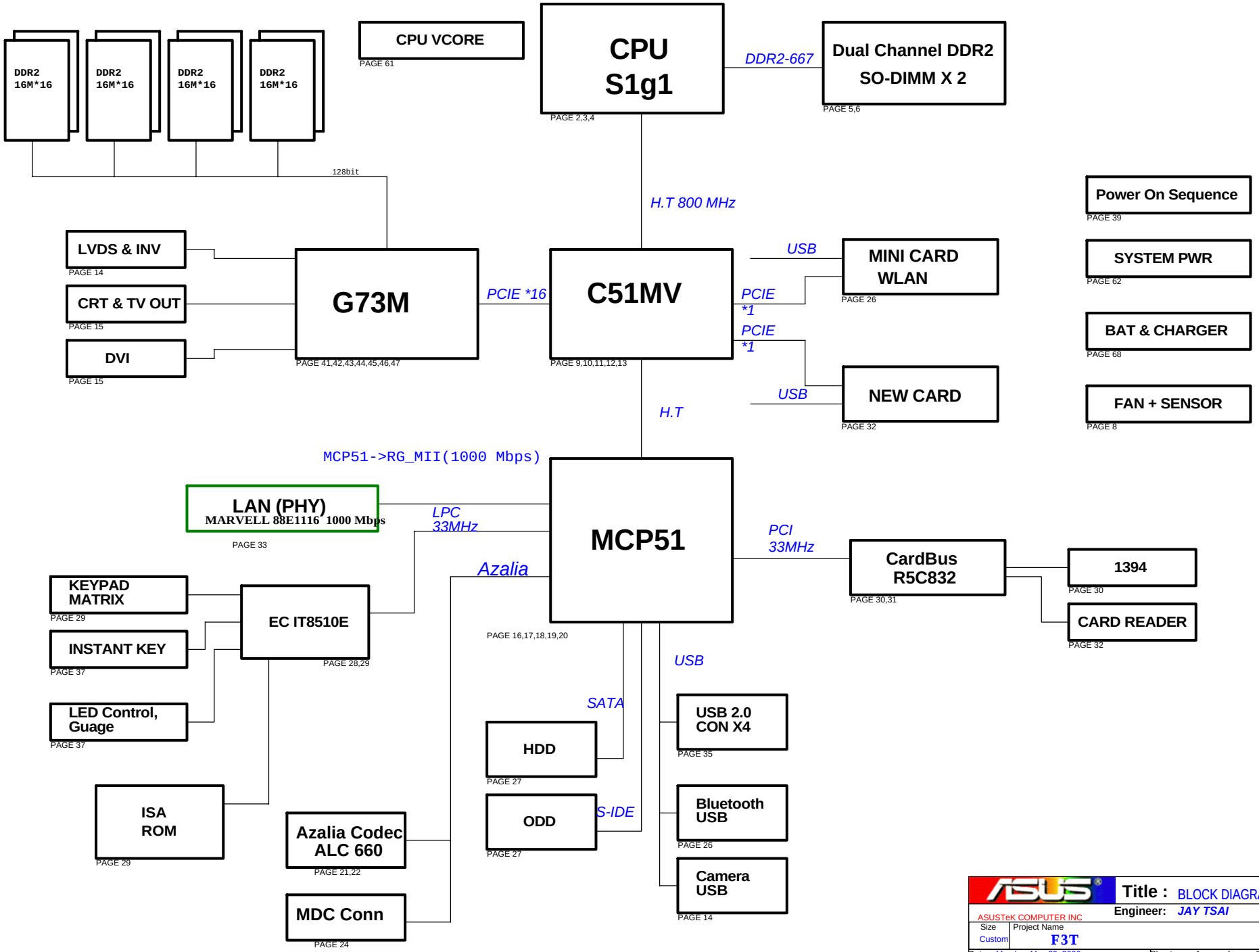
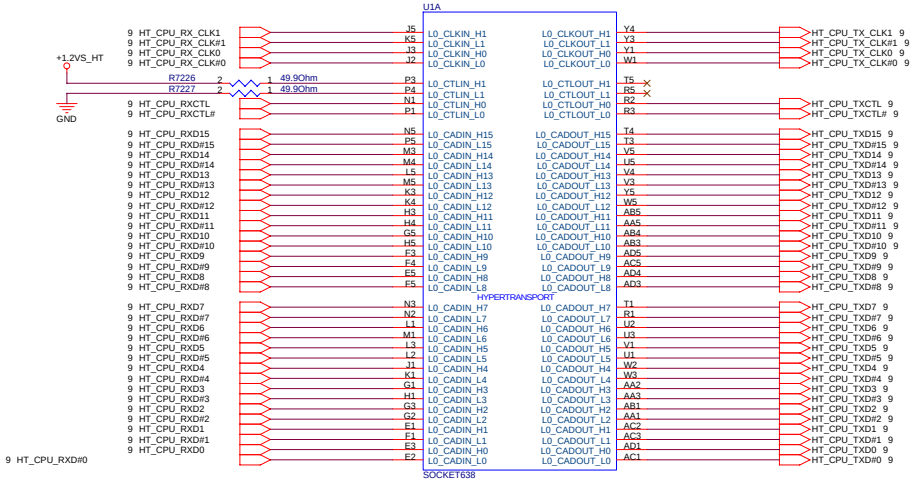
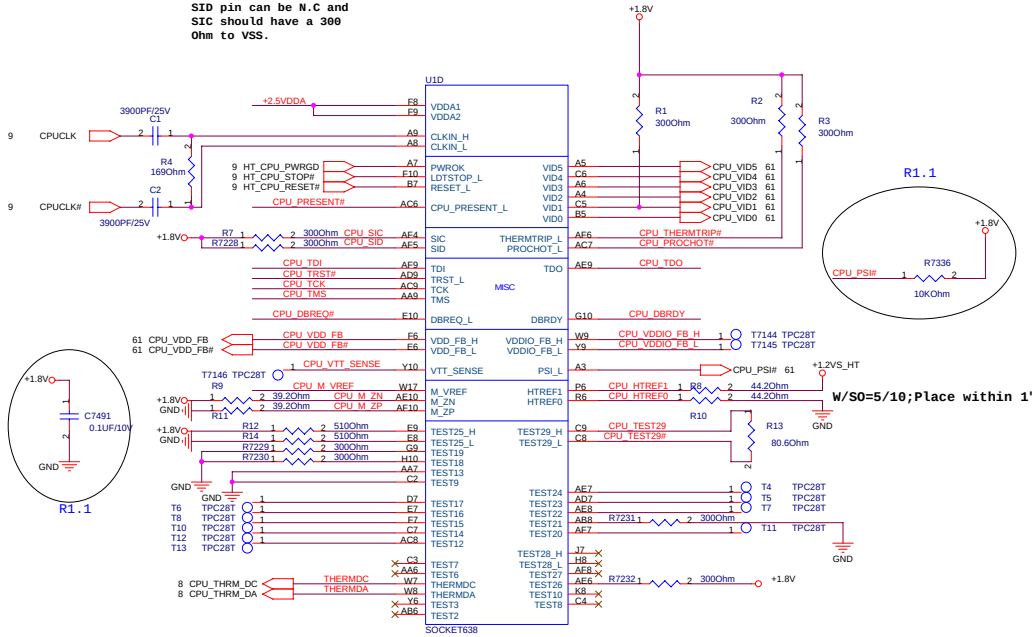
F3T Block Diagram



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 1 of 74	

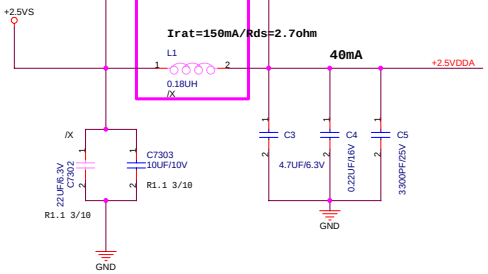
Note.AMD suggest :If AMD SI is not used,ths SID pin can be N.C and SIC should have a 300 Ohm to VSS.

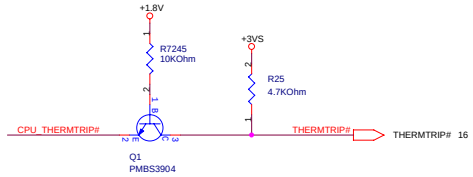


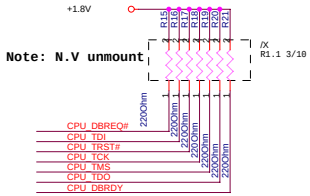


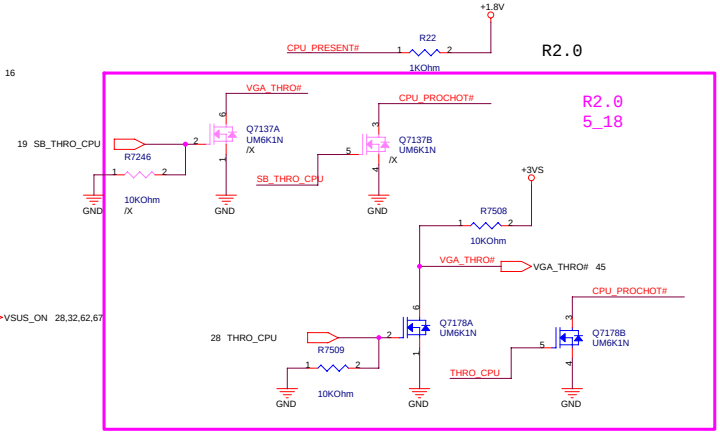
R2.0 4_24

R2.0 4_27
To change mount L7037.

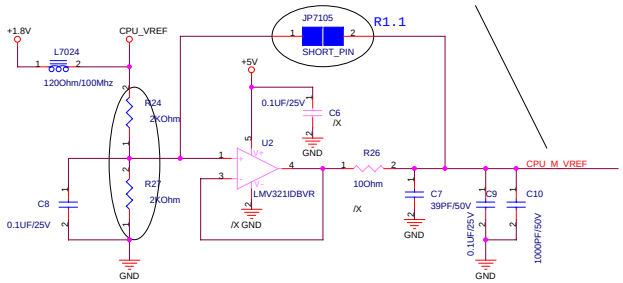




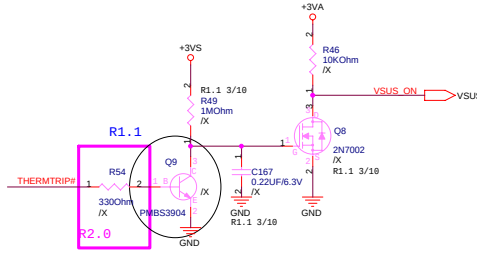




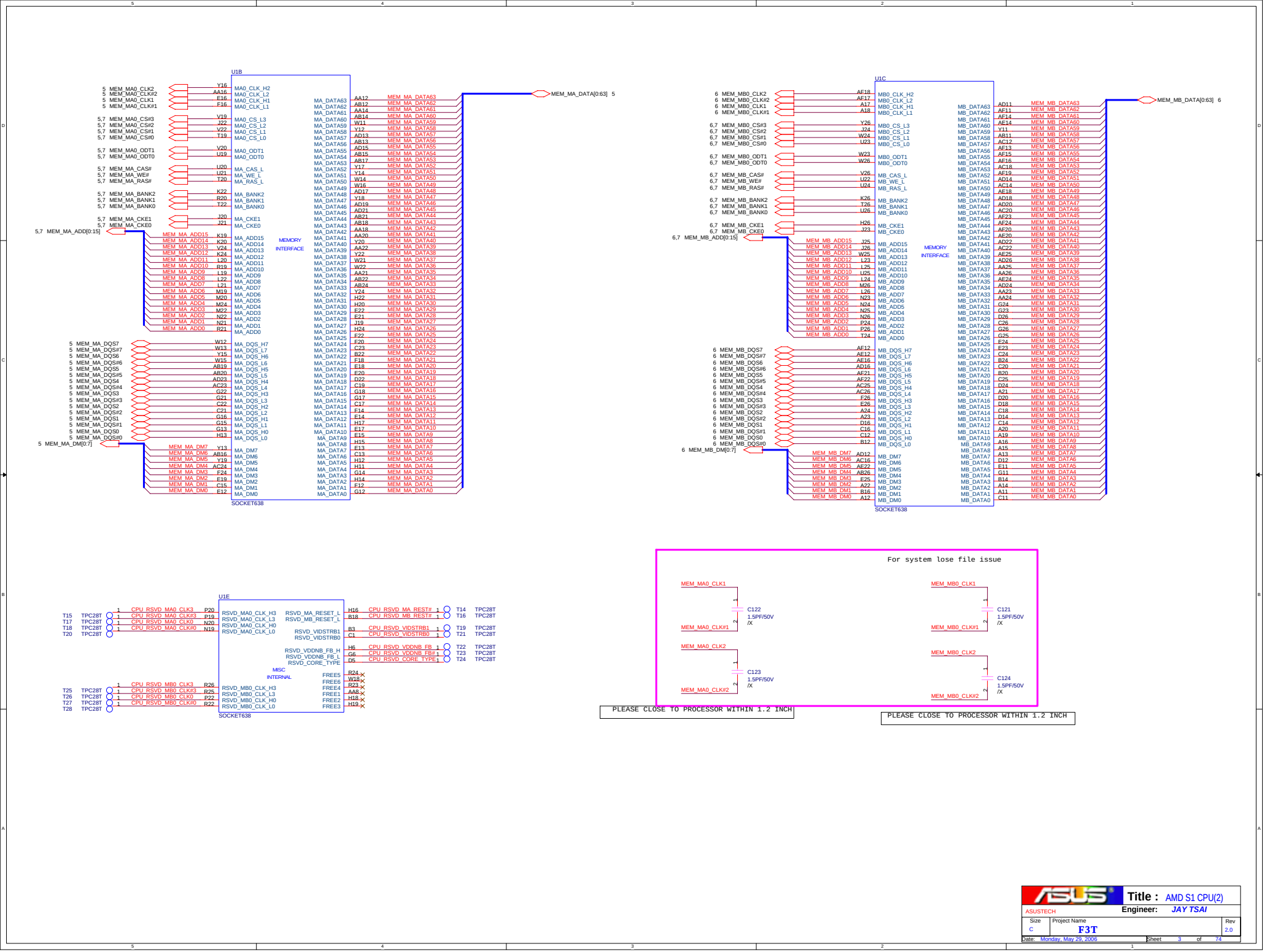
15mils trace,20mil spece /Shorter than 6"



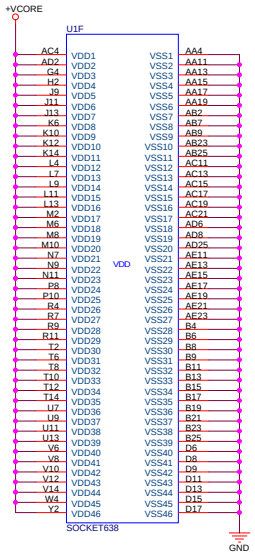
Nearby SO-DIMM

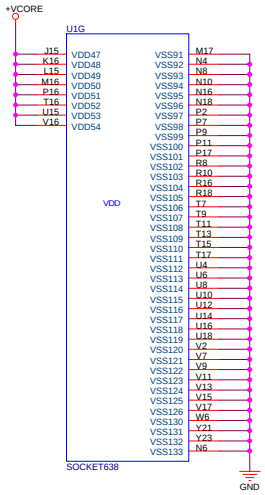


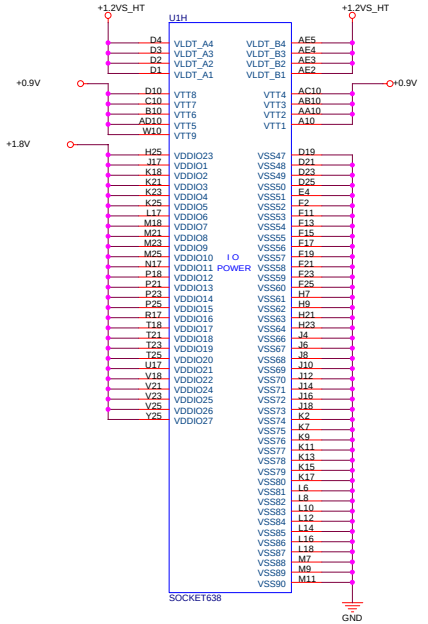
ASUSTECH	Title : AMD S1 CPU(1)		
	Engineer: JAY TSAI		
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 2 of 74		

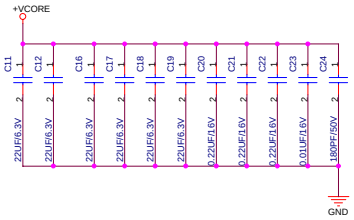


ASUSTECH	Title : AMD S1 CPU(2)		
	Engineer: JAY TSAI		
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 3 of 74		

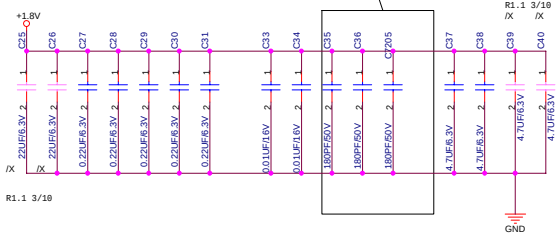


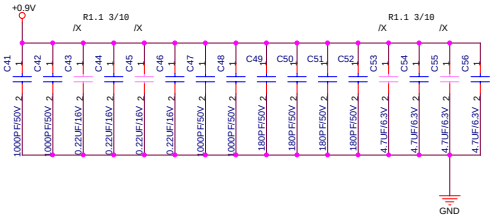


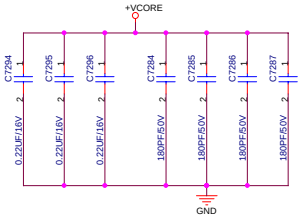


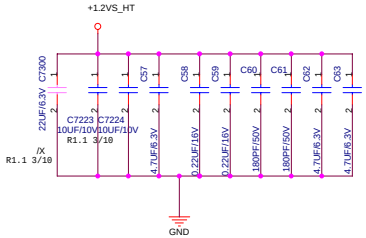


For DDR2 add/cmd refer to split plane.

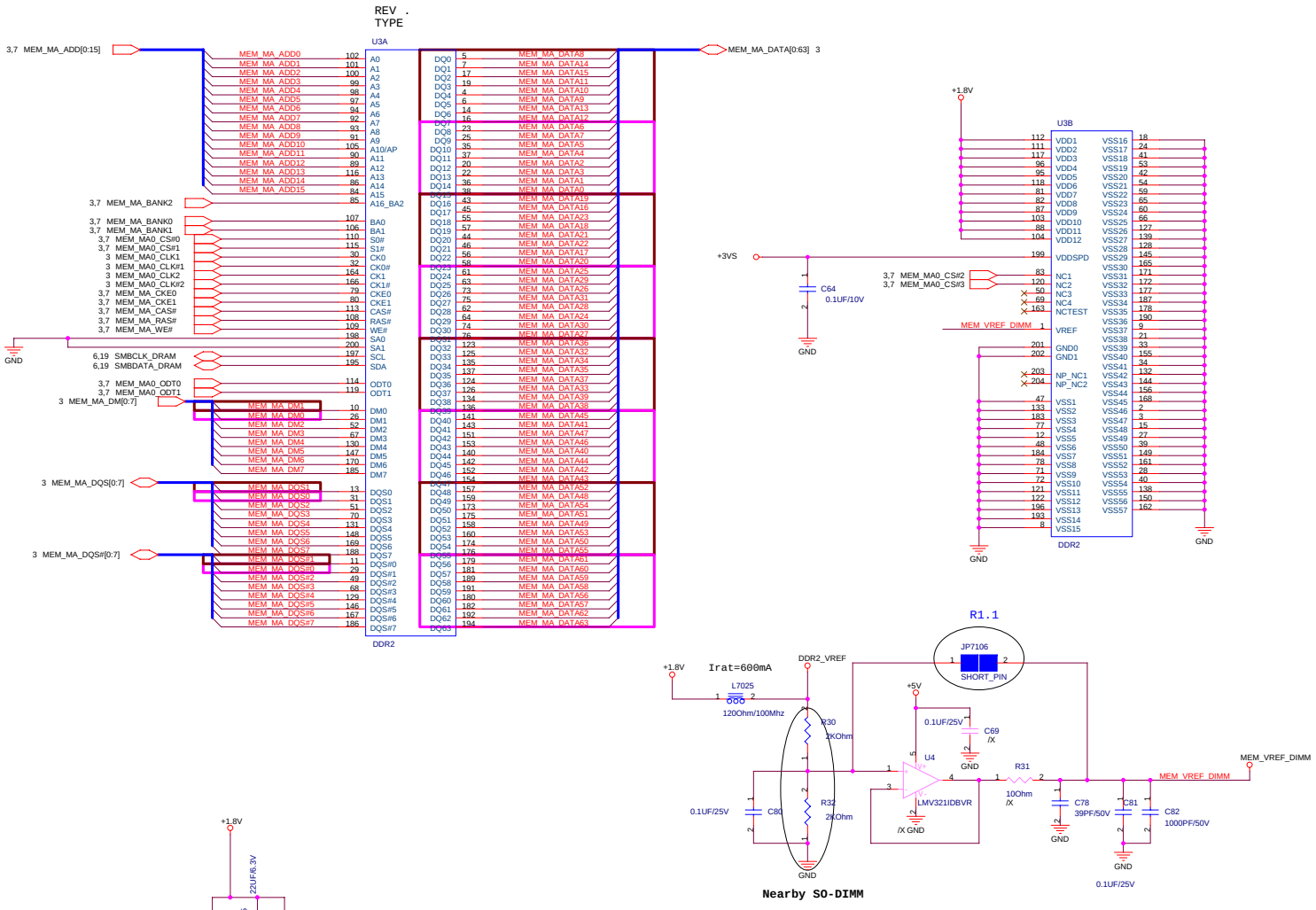






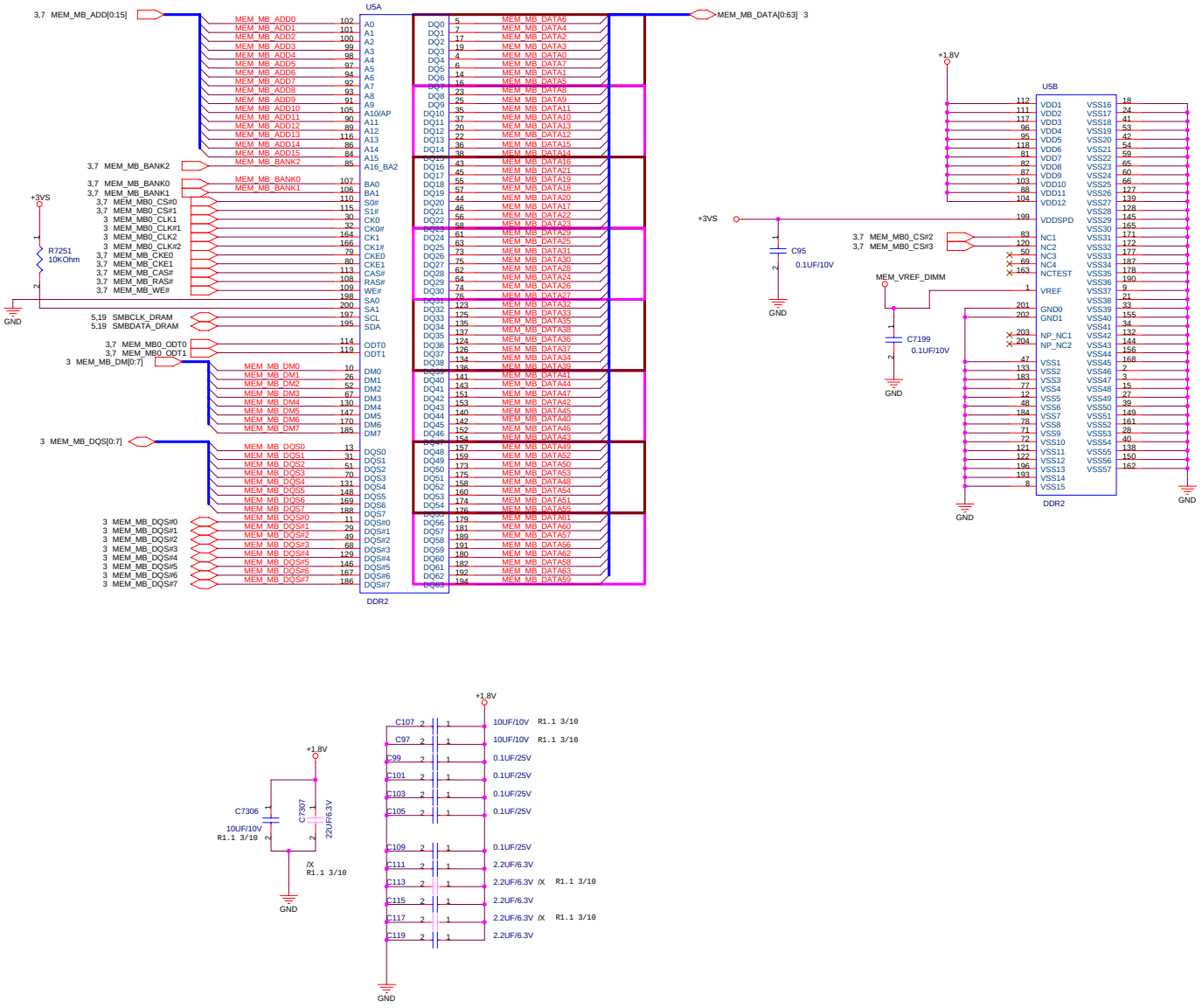


ASUSTECH	Title : AMD S1 CPU(3)	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 4 of 74	



ASUSTECH	Title : DDR2_SO_DIMM(0)	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 5 of 74	

STD. TYPE



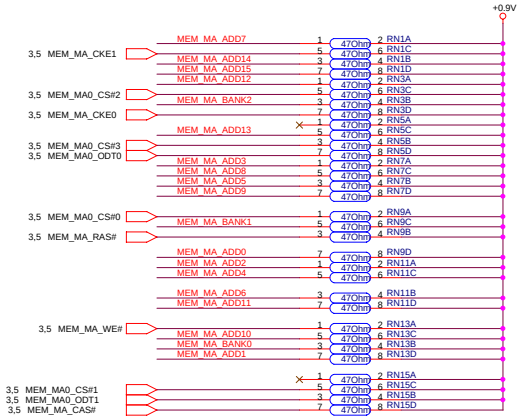
ASUSTECH	Title : DDR2_SO_DIMM(1)	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 6 of 74	

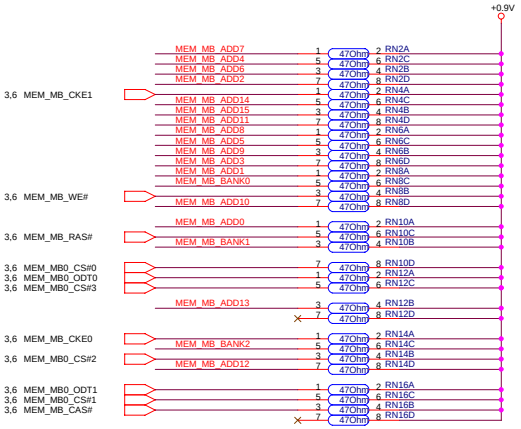
3,5 MEM_MA_ADD[0:15]

3,5 MEM_MA_BANK[0:2]

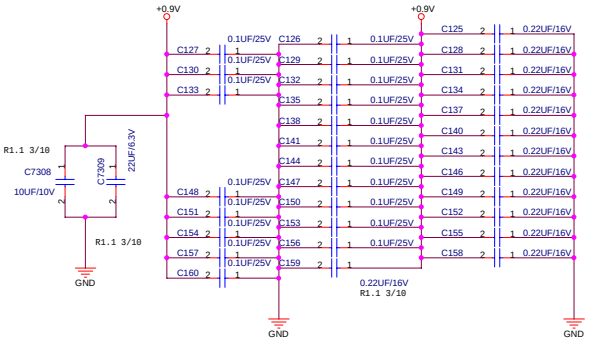
3,6 MEM_MB_ADD[0:15]

3,6 MEM_MB_BANK[0:2]





Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9V



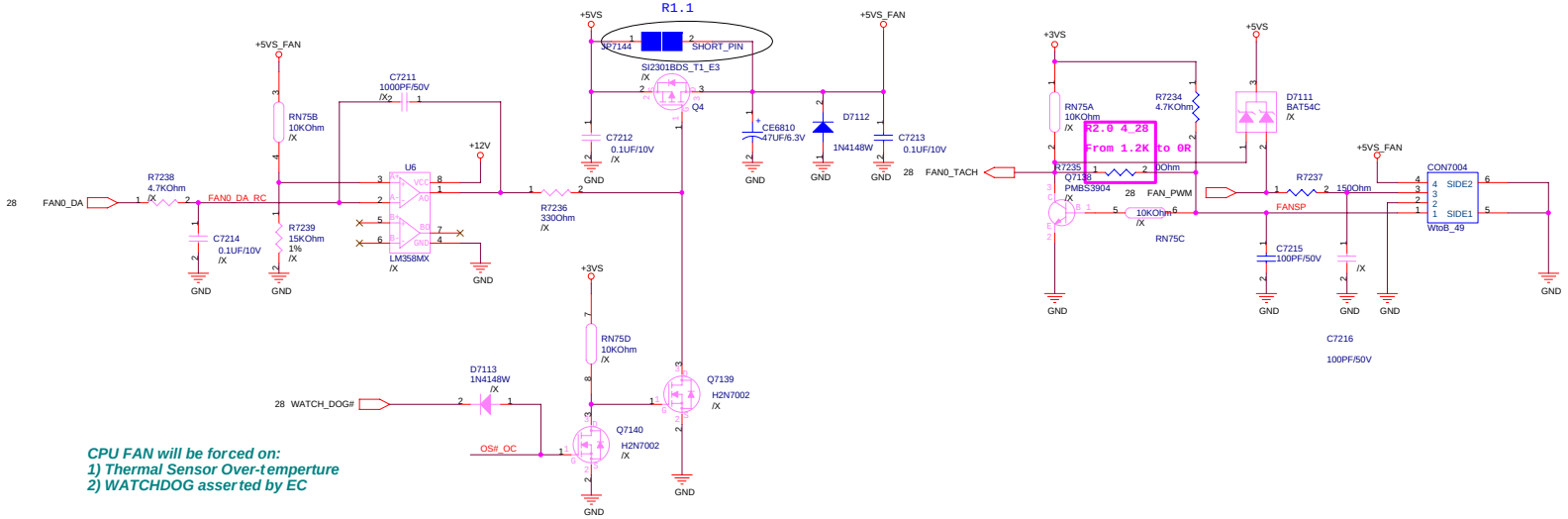
ASUSTECH

Title : DDR2TERMINATIONS

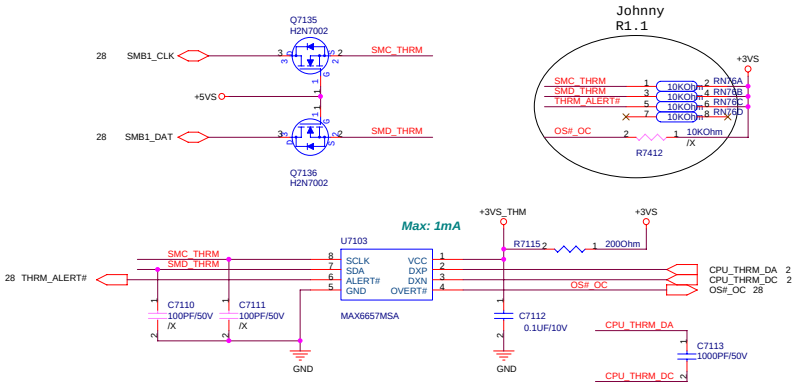
Engineer: JAY TSAI

Size	Project Name	Rev
C	F3T	2.0

Date: Monday, May 29, 2006 Sheet 7 of 74



CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC



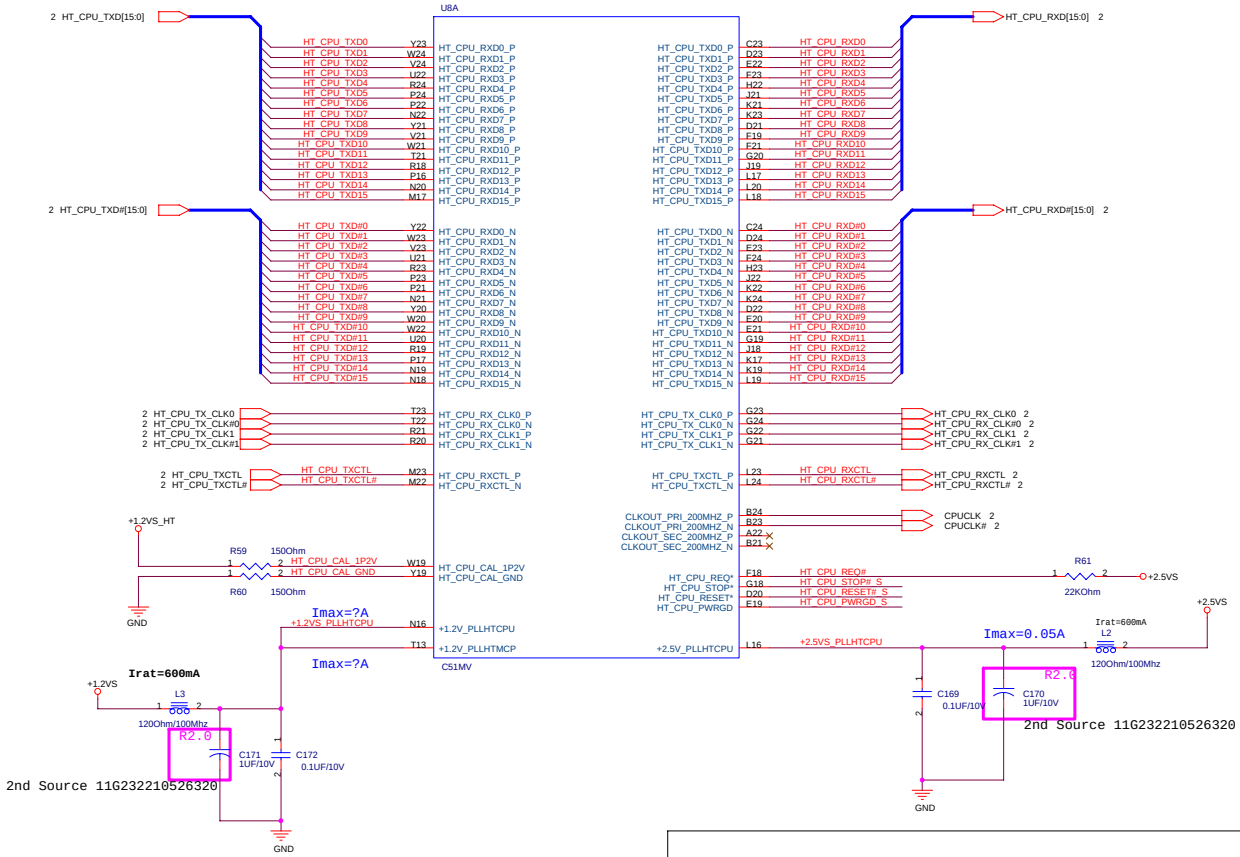
Route CPU_THRM_DA and
CPU_THRM_DC
on the same layer

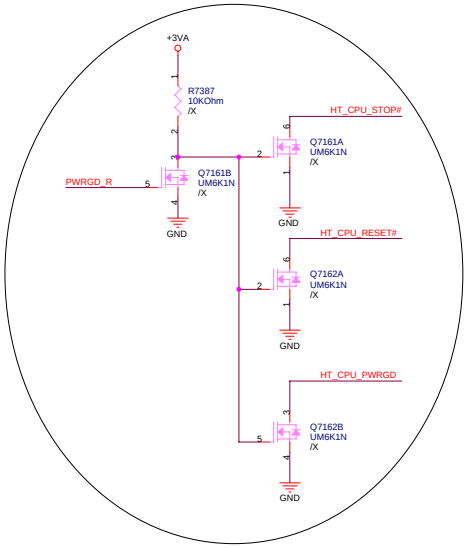
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

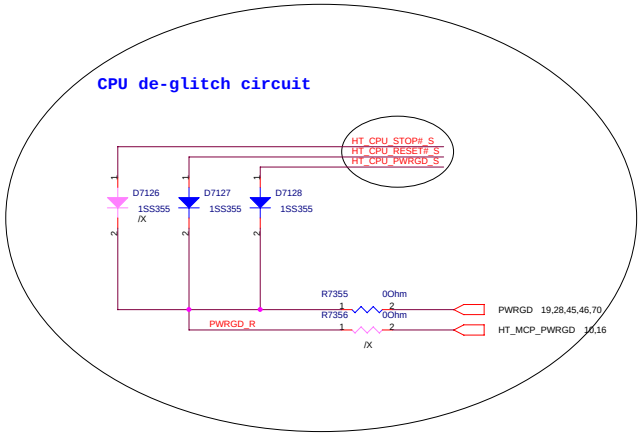
Avoid FSB,Power

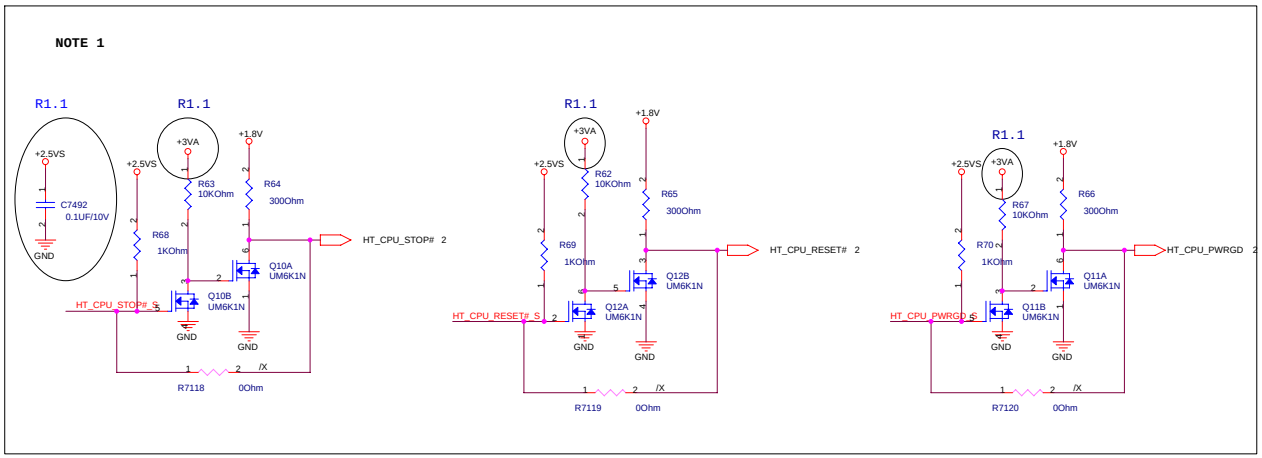
ASUSTECH	Title : THERMAL&FAN	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 8 of 74	

2nd source
P/N:02G190009020

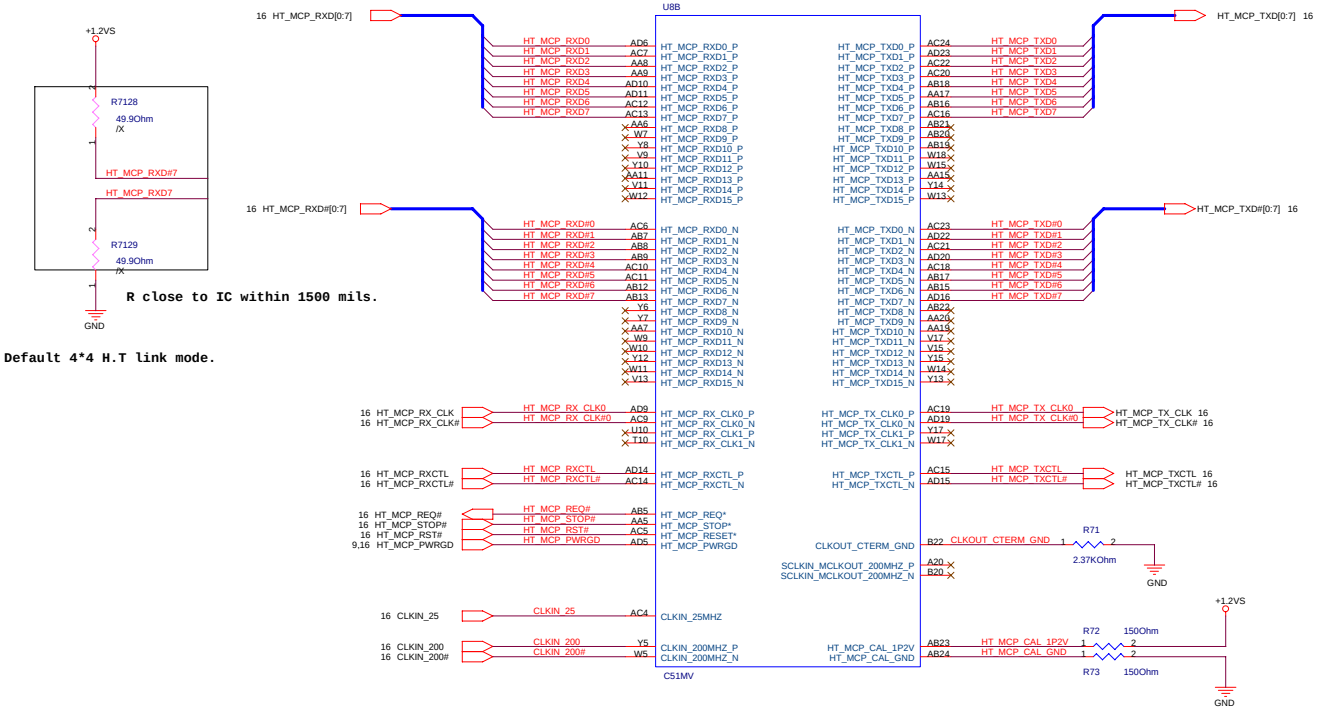








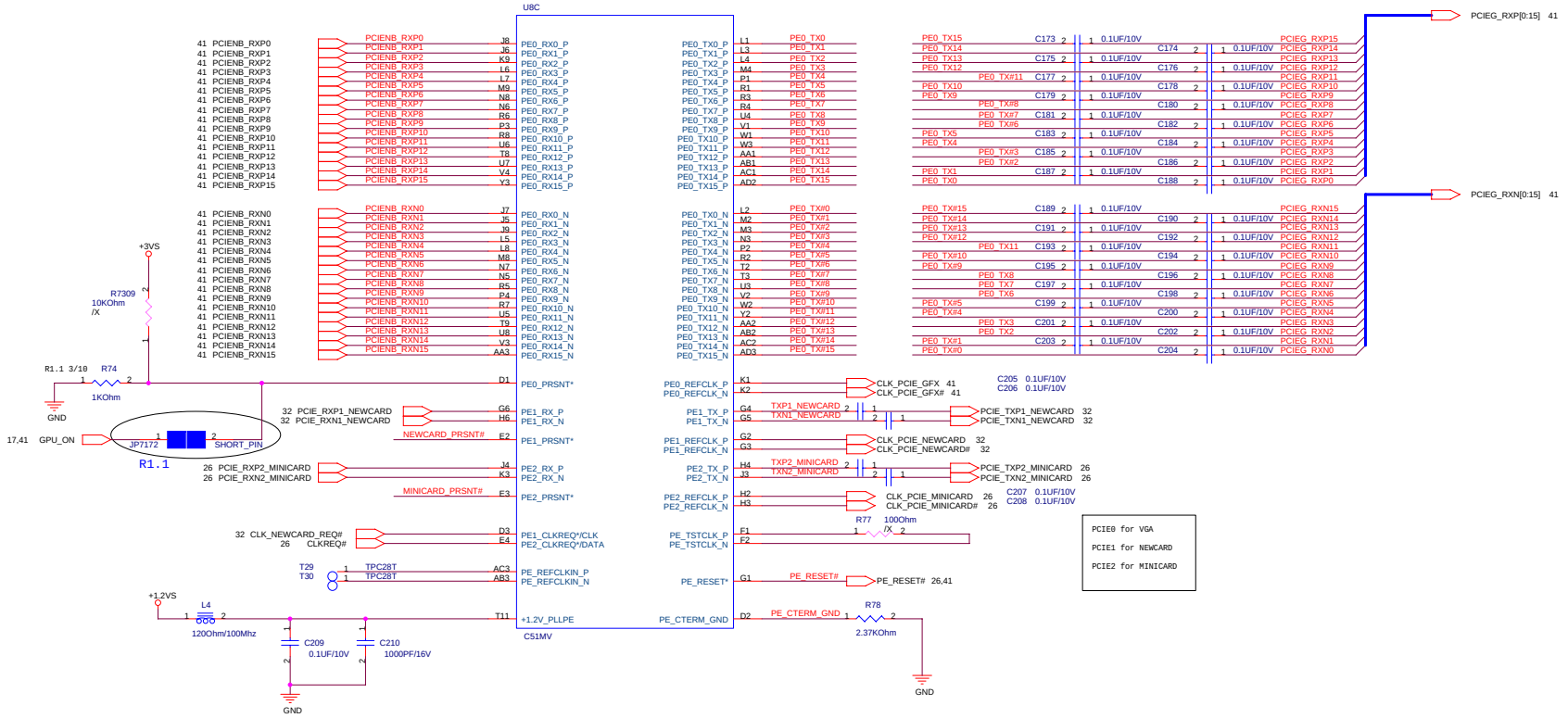
ASUSTECH	Title : C51M HT_CPU	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 9 of 74	



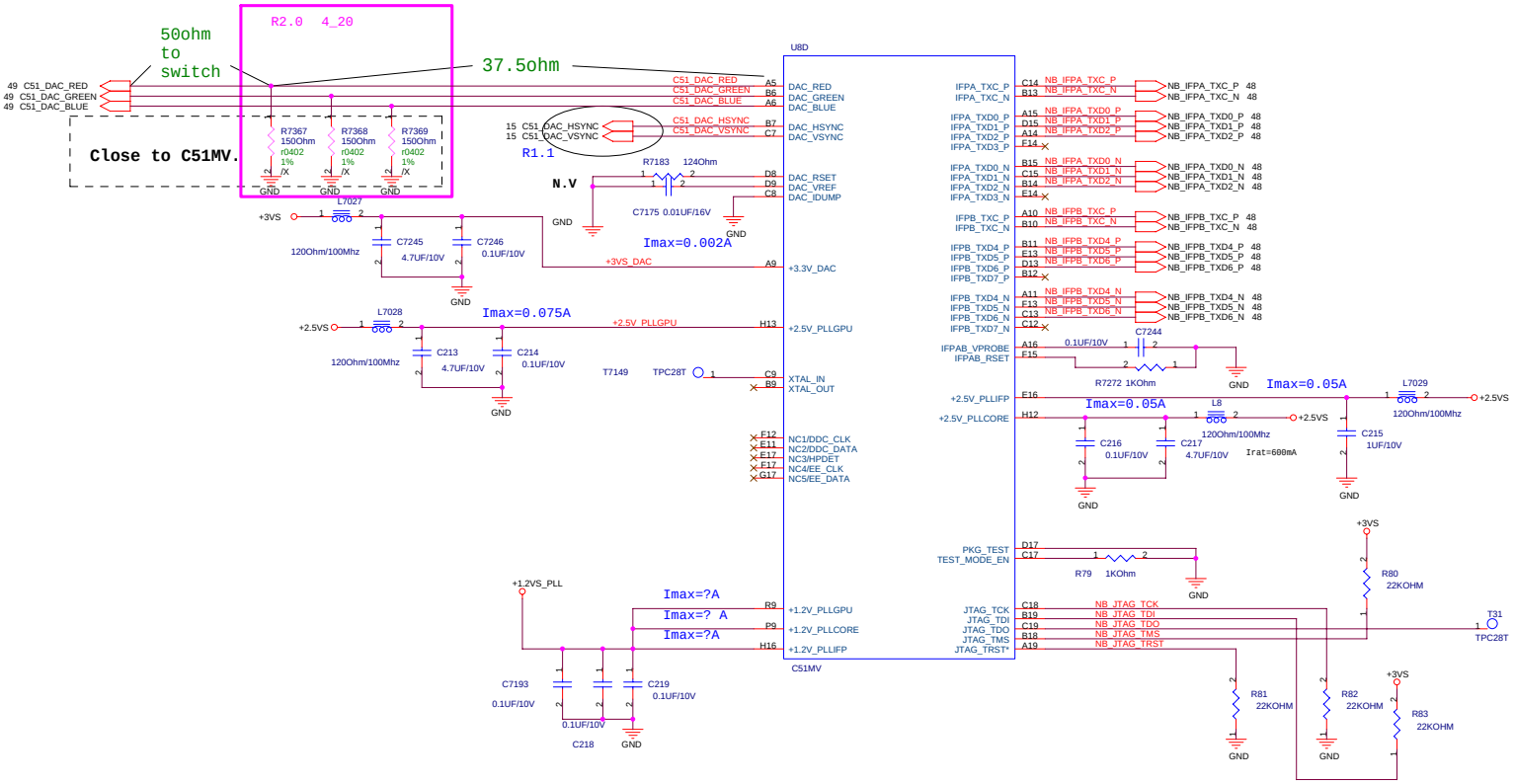
Default 4*4 H.T link mode.

ASUSTECH	Title : C51 HT_MCP		
	Engineer: JAY TSAI		
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 10 of 74		

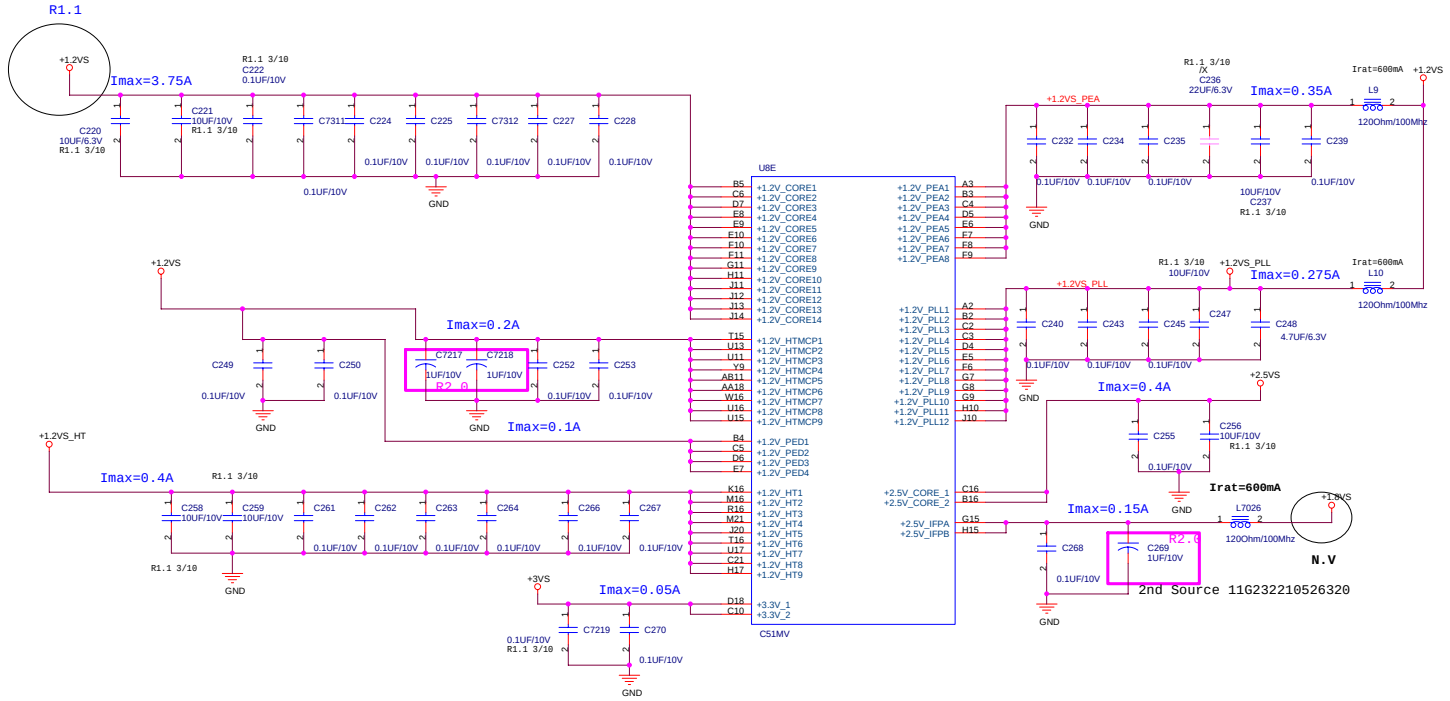
Polarity
Inversion:PE0_TX2,3,6,7,8,11/PE0_TX#2,3,6,7,8,11



ASUSTECH	Title : C51M PCIEx16	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 11 of 74	

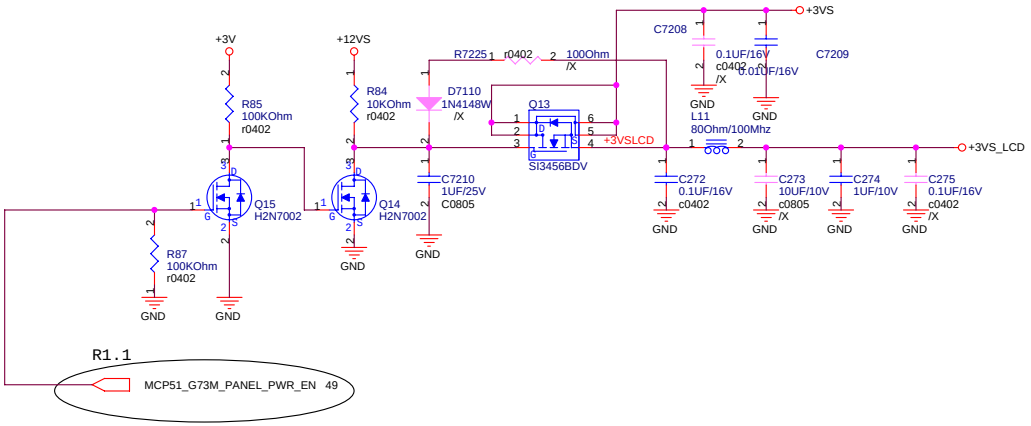


ASUSTECH	Title : C51M RGB&TV OUT	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 12 of 74	



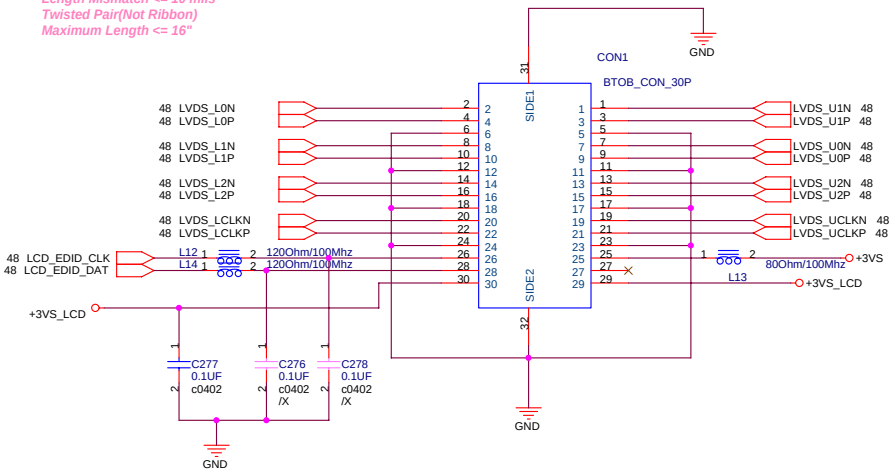
ASUSTECH	Title : C51M PWR&GND		
	Engineer: JAY TSAI		
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 13 of 74		

LCD Power

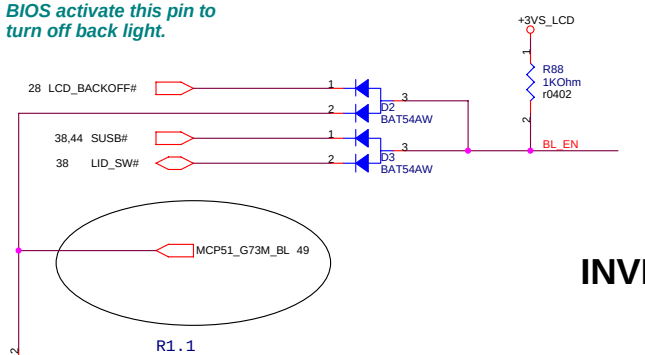


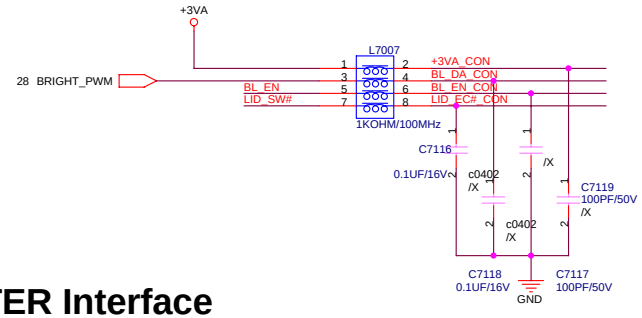
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

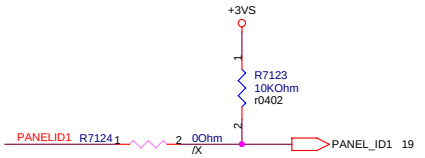
LCD LVDS Interface



BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.



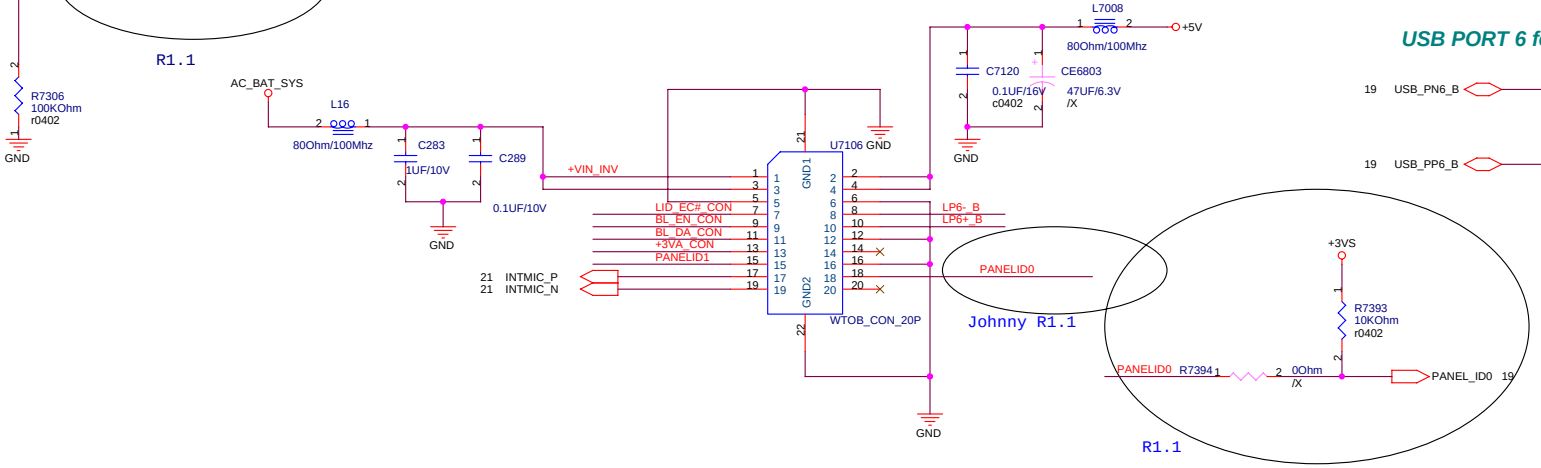




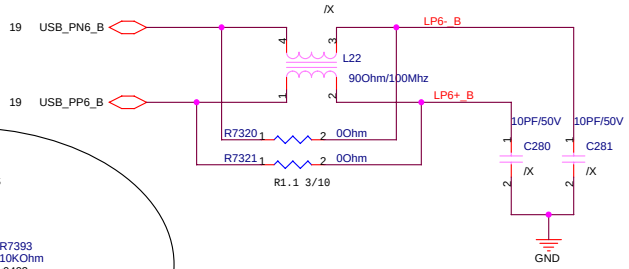
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR

INVERTER Interface

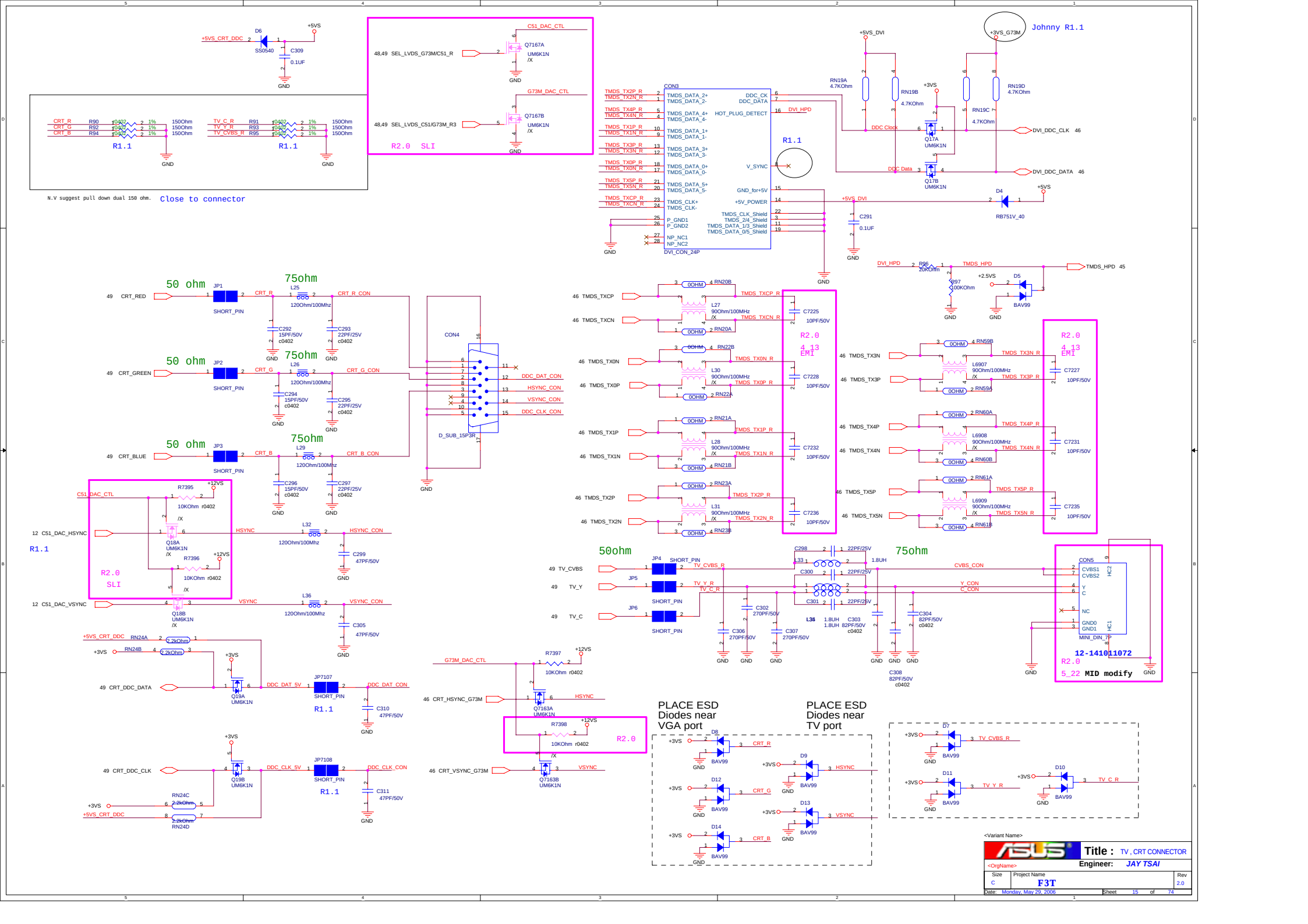


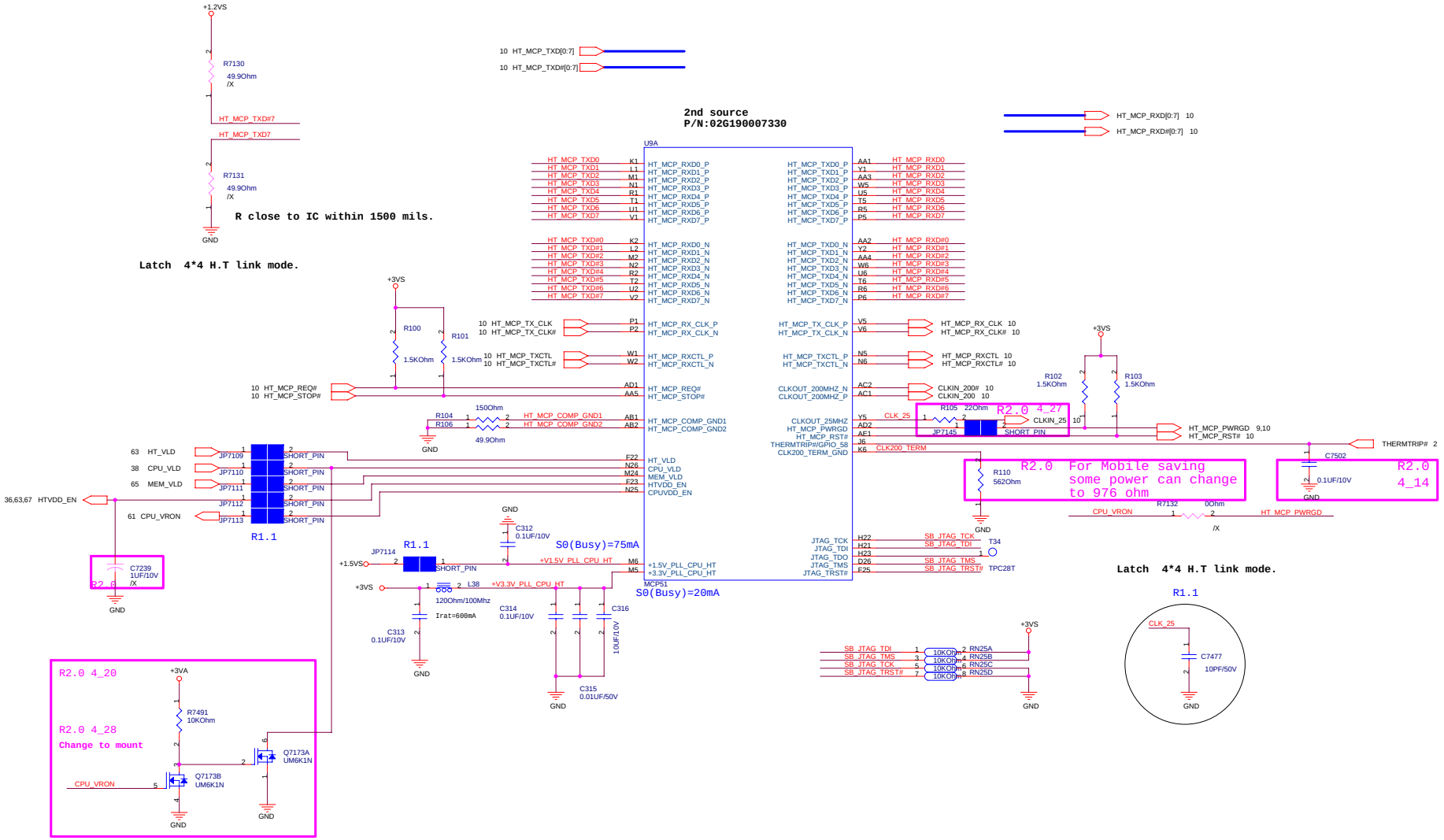
USB PORT 6 for USB CAMERA



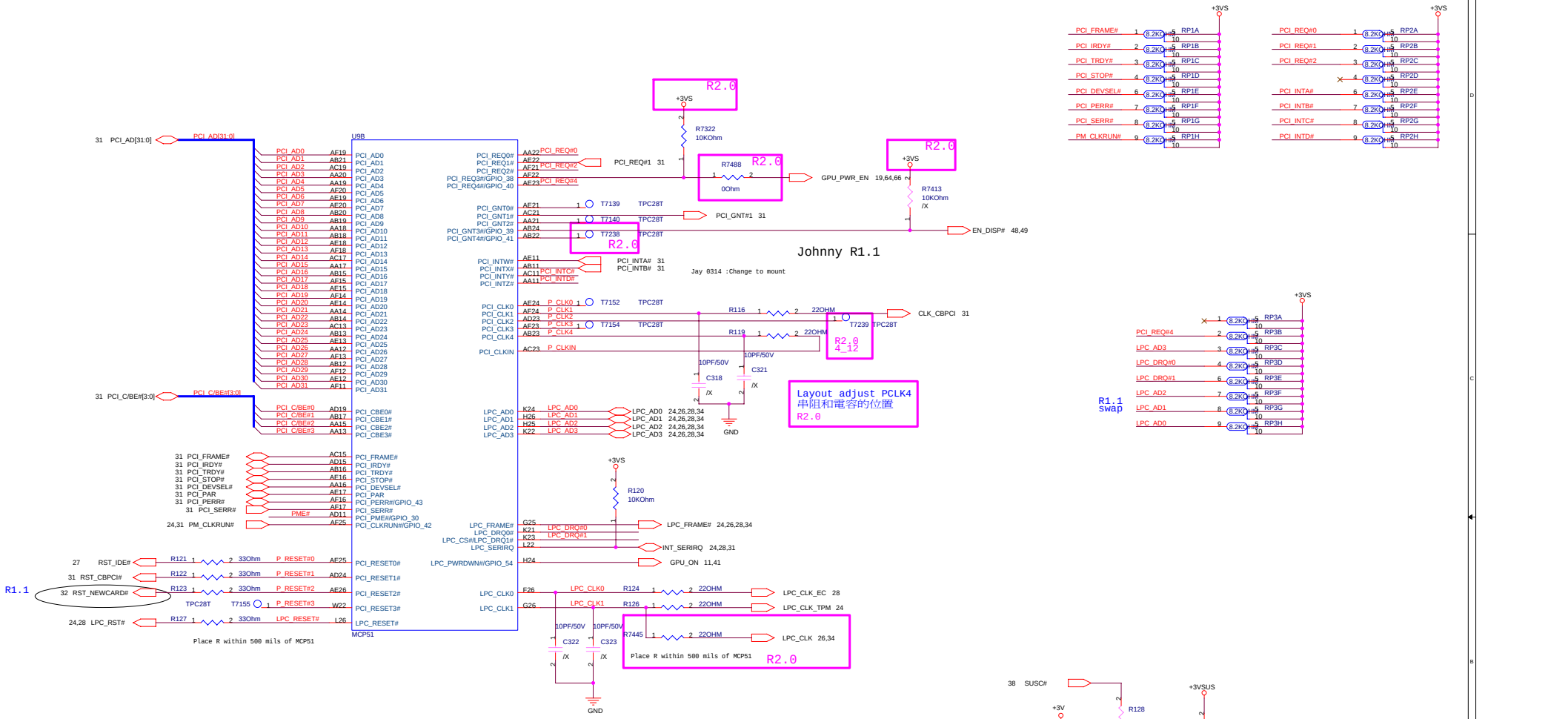
<Variant Name>

ASUS	Title : LVDS & INVERTER	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 14 of 74	

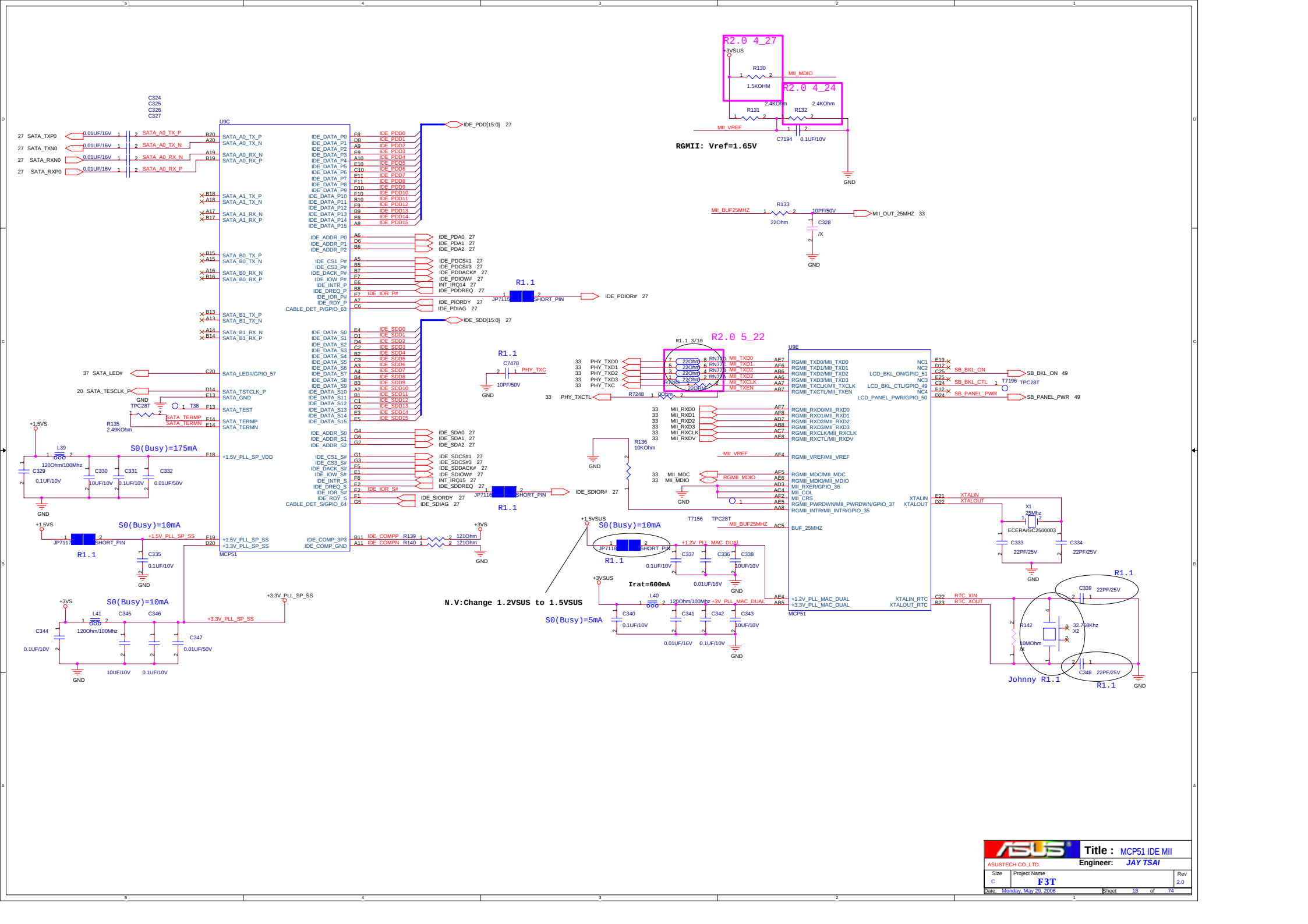

Johnny R1.1
Close to connector
N.V suggest pull down dual 150 ohm.
R2.0 SLI
R1.1
R2.0 4_13 EMI
50 ohm
75ohm
50ohm
PLACE ESD Diodes near VGA port
PLACE ESD Diodes near TV port
12-141011072
R2.0 5_22 MID modify
Title : TV , CRT CONNECTOR
Engineer: JAY TSAI
Project Name F3T
Date: Monday, May 29, 2006
Sheet 15 of 74



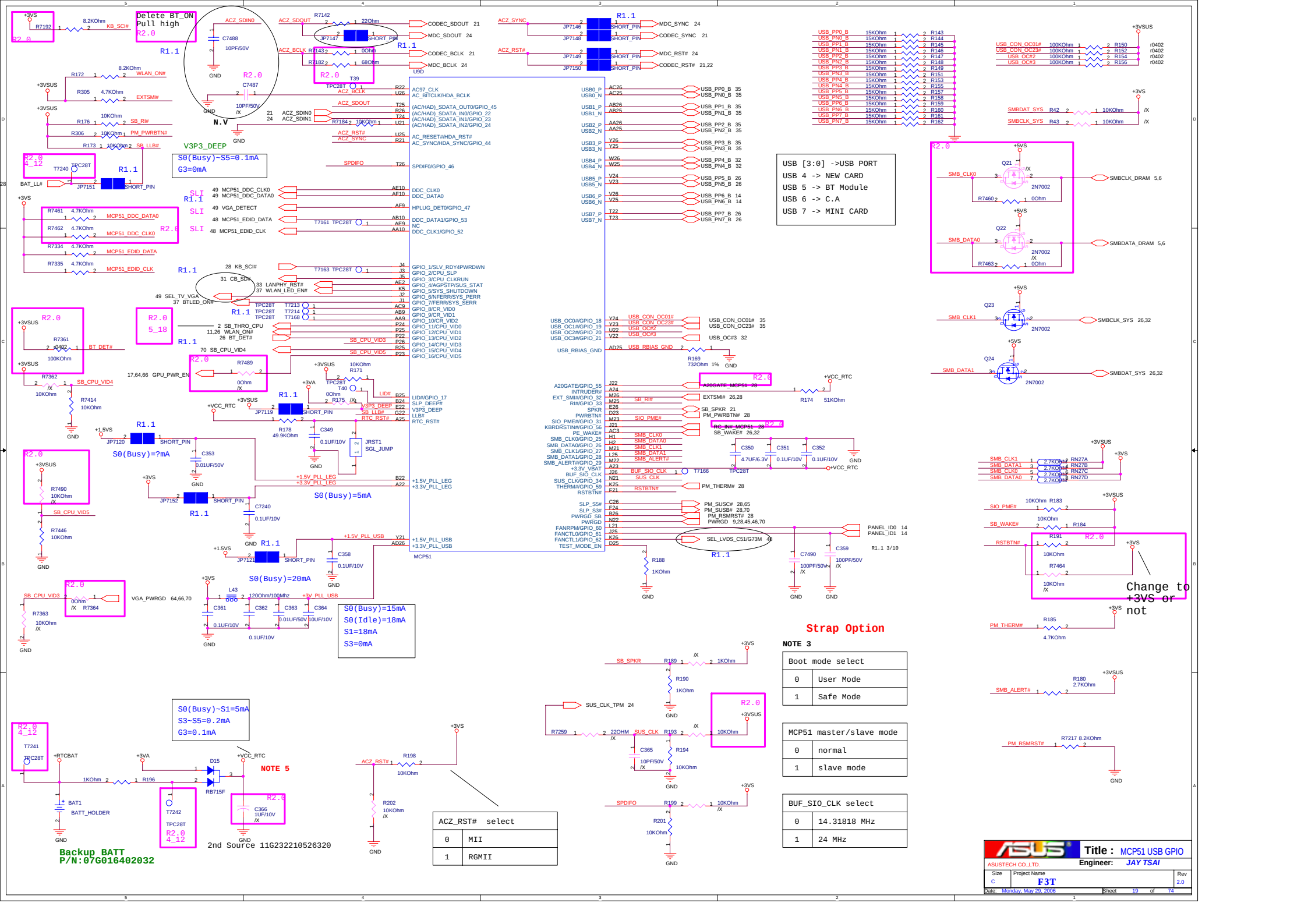
ASUSTECH CO.,LTD.	Title :	SB_HT_I/F	
	Engineer:	JAY TSAI	
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 16 of 74		

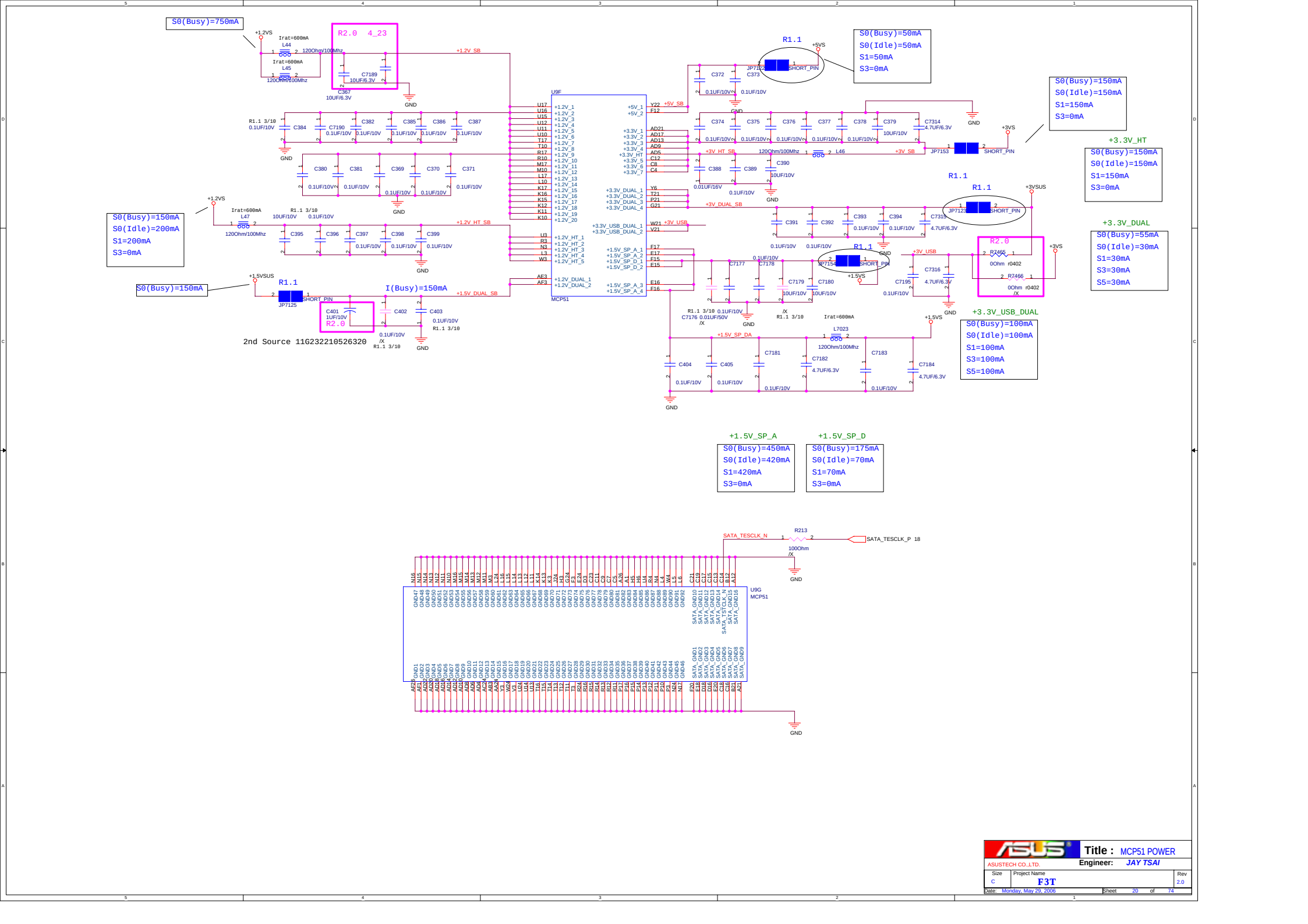


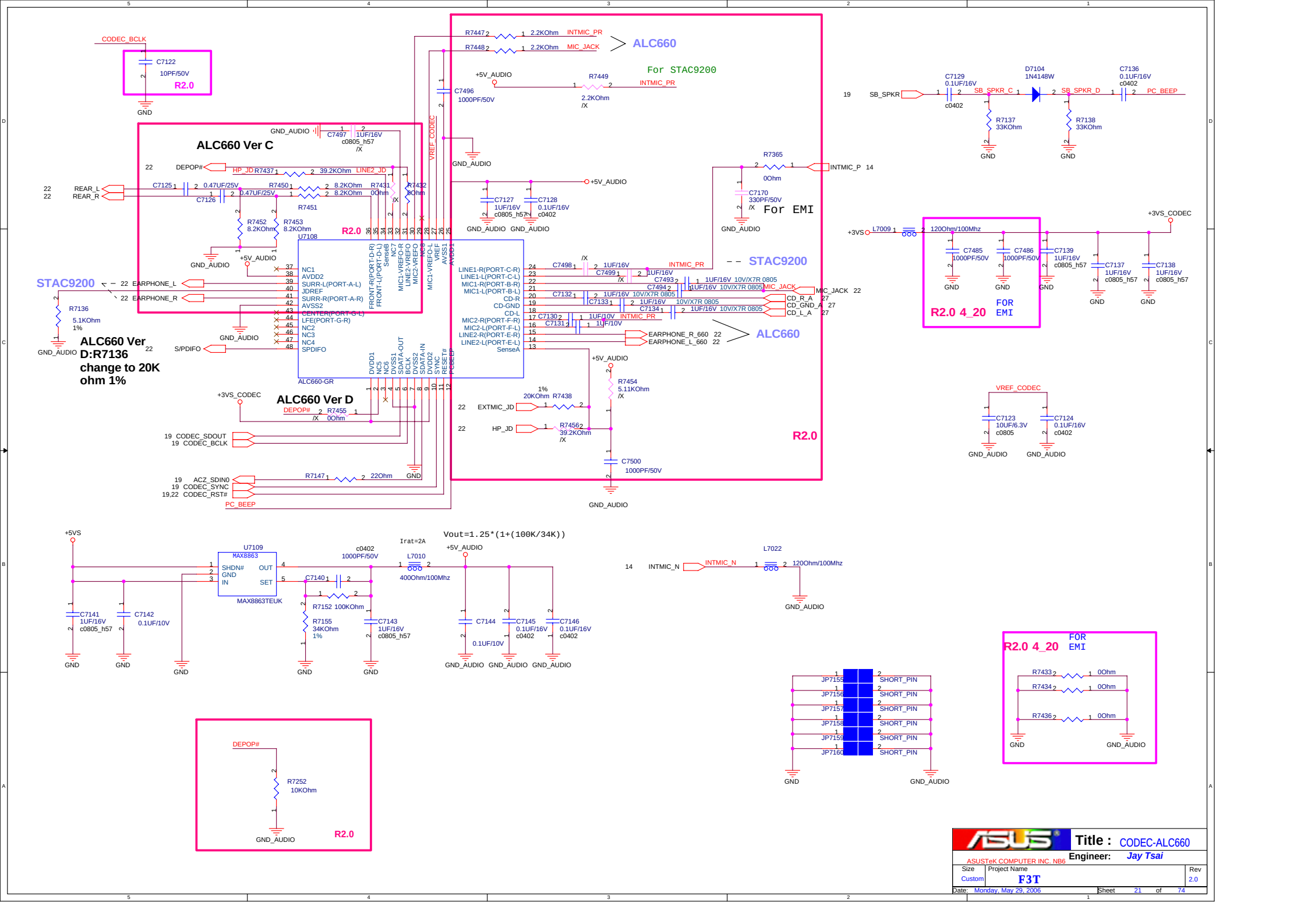
ASUSTECH COM.,LTD.	Title : PCI I/F		
	Engineer: JAY TSAI		
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 17 of 74		

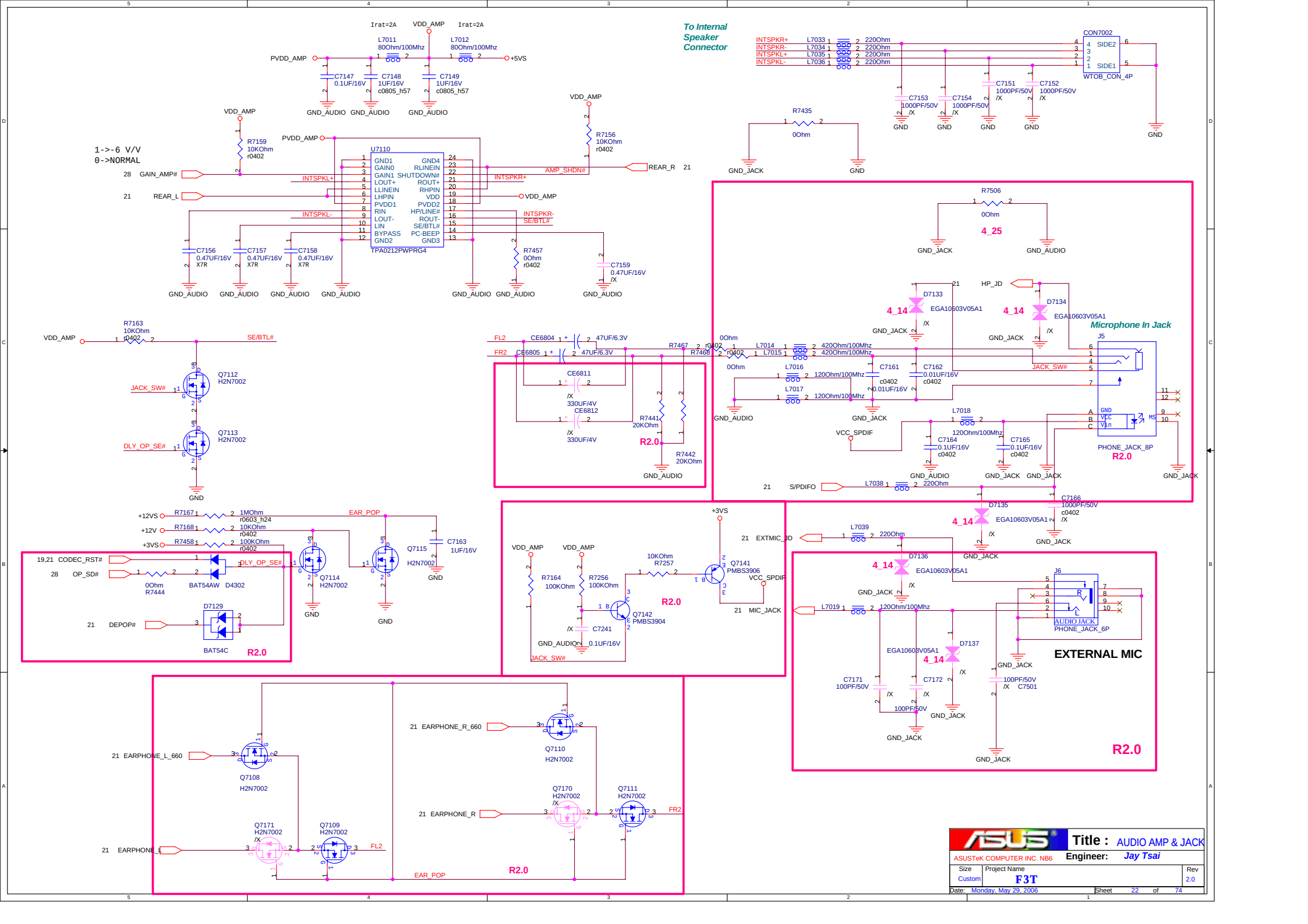


ASUSTECH COM.,LTD.	Title : MCP51 IDE MII		
	Engineer: JAY TSAI		
Size: C	Project Name: F3T		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 18 of 74		


Delete BT_ON Pull high
R2.0
R1.1
V3P3_DEEP
S0(Busy)~S5=0.1mA
G3=0mA
S0(Busy)=?mA
S0(Busy)=5mA
S0(Busy)=20mA
S0(Busy)=15mA
S0(Idle)=18mA
S1=18mA
S3=0mA
S0(Busy)~S1=5mA
S3~S5=0.2mA
G3=0.1mA
USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 5 -> BT Module
USB 6 -> C.A
USB 7 -> MINI CARD
Change to +3VS or not
Strap Option
NOTE 3
Boot mode select
0 User Mode
1 Safe Mode
MCP51 master/slave mode
0 normal
1 slave mode
BUF_SIO_CLK select
0 14.31818 MHz
1 24 MHz
ACZ_RST# select
0 MII
1 RGMII
NOTE 5
Backup BATT
P/N:07G016402032
2nd Source 11G232210526320
Title : MCP51 USB GPIO
ASUSTECH CO.,LTD.
Engineer: JAY TSAI
Size C
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 19 of 74


S0(Busy)=750mA
R2.0 4_23
S0(Busy)=50mA
S0(Idle)=50mA
S1=50mA
S3=0mA
S0(Busy)=150mA
S0(Idle)=150mA
S1=150mA
S3=0mA
+3.3V_HT
S0(Busy)=150mA
S0(Idle)=150mA
S1=150mA
S3=0mA
S0(Busy)=150mA
S0(Idle)=200mA
S1=200mA
S3=0mA
+3.3V_DUAL
S0(Busy)=55mA
S0(Idle)=30mA
S1=30mA
S3=30mA
S5=30mA
S0(Busy)=150mA
I(Busy)=150mA
+3.3V_USB_DUAL
S0(Busy)=100mA
S0(Idle)=100mA
S1=100mA
S3=100mA
S5=100mA
2nd Source 11G232210526320
+1.5V_SP_A
S0(Busy)=450mA
S0(Idle)=420mA
S1=420mA
S3=0mA
+1.5V_SP_D
S0(Busy)=175mA
S0(Idle)=70mA
S1=70mA
S3=0mA
U9F
MCP51
U9G
MCP51
SATA_TESCLK_N
SATA_TESCLK_P 18
Title : MCP51 POWER
ASUSTECH CO.,LTD.
Engineer: JAY TSAI
Size C
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 20 of 74


CODEC_BCLK
C7122
10PF/50V
R2.0
GND
ALC660 Ver C
GND_AUDIO
C7497
1UF/16V
c0805_h57
/X
22 DEPOP#
HP_JD R7437 39.2KOhm LINE2_JD
22 REAR_L
22 REAR_R
C7125 0.47UF/25V
C7126 0.47UF/25V
R7450 8.2KOhm
R7451 8.2KOhm
R7431 0Ohm
R7432 0Ohm
R7452 8.2KOhm
R7453 8.2KOhm
U7108
+5V_AUDIO
STAC9200
22 EARPHONE_L
22 EARPHONE_R
R7136
5.1KOhm
1%
ALC660 Ver D:R7136 change to 20K ohm 1%
22 S/PDIFO
NC1
AVDD2
SURR-L(PORT-A-L)
JDREF
SURR-R(PORT-A-R)
AVSS2
CENTER(PORT-G-L)
LFE(PORT-G-R)
NC2
NC3
NC4
SPDIFO
ALC660-GR
FRONT-R(PORT-D-R)
FRONT-L(PORT-D-L)
SenseB
NC7
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
NC8
MIC1-VREFO-L
VREF
AVSS1
AVDD1
DVDD1
NC5
NC6
DVSS1
SDATA-OUT
BCLK
SDATA-IN
DVDD2
SYNC
RESET#
PCBEEP
+3VS_CODEC
ALC660 Ver D
DEPOP#
R7455 0Ohm
/X
19 CODEC_SDOUT
19 CODEC_BCLK
19 ACZ_SDIN0
19 CODEC_SYNC
19,22 CODEC_RST#
R7147 22Ohm
PC_BEEP
VREF_CODEC
R7447 2.2KOhm INTMIC_PR
R7448 2.2KOhm MIC_JACK
ALC660
For STAC9200
+5V_AUDIO
R7449 2.2KOhm
INTMIC_PR
/X
C7496 1000PF/50V
C7127 1UF/16V c0805_h57
C7128 0.1UF/16V c0402
R7365 0Ohm
INTMIC_P 14
C7170 330PF/50V
/X
For EMI
STAC9200
LINE1-R(PORT-C-R)
LINE1-L(PORT-C-L)
MIC1-R(PORT-B-R)
MIC1-L(PORT-B-L)
CD-R
CD-GND
CD-L
MIC2-R(PORT-F-R)
MIC2-L(PORT-F-L)
LINE2-R(PORT-E-R)
LINE2-L(PORT-E-L)
SenseA
C7498 1UF/16V
C7499 1UF/16V
C7493 1UF/16V 10V/X7R 0805
C7494 1UF/16V 10V/X7R 0805
MIC_JACK
C7132 1UF/16V 10V/X7R 0805
C7133 1UF/16V 10V/X7R 0805
C7134 1UF/16V 10V/X7R 0805
C7130 1UF/10V INTMIC_PR
C7131 1UF/10V
MIC_JACK 22
CD_R_A 27
CD_GND_A 27
CD_L_A 27
EARPHONE_R_660 22
EARPHONE_L_660 22
ALC660
R7454 5.11KOhm
/X
1% 20KOhm R7438
22 EXTMIC_JD
22 HP_JD
R7456 39.2KOhm
/X
R2.0
C7500 1000PF/50V
SB_SPKR
C7129 0.1UF/16V c0402
D7104 1N4148W
C7136 0.1UF/16V c0402
SB_SPKR_C
SB_SPKR_D
PC_BEEP
R7137 33KOhm
R7138 33KOhm
+3VS
L7009 120Ohm/100Mhz
C7485 1000PF/50V
C7486 1000PF/50V
C7139 1UF/16V c0805_h57
C7137 1UF/16V c0805_h57
C7138 1UF/16V c0805_h57
R2.0 4_20
FOR EMI
C7123 10UF/6.3V c0805
C7124 0.1UF/16V c0402
+5VS
U7109
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
C7141 1UF/16V c0805_h57
C7142 0.1UF/10V
R7152 100KOhm
R7155 34KOhm 1%
C7140
C7143 1UF/16V c0805_h57
c0402 1000PF/50V
Irat=2A
L7010 400Ohm/100Mhz
Vout=1.25*(1+(100K/34K))
C7144 0.1UF/10V
C7145 0.1UF/16V c0402
C7146 0.1UF/16V c0402
14 INTMIC_N
L7022 120Ohm/100Mhz
JP7155 SHORT_PIN
JP7156 SHORT_PIN
JP7157 SHORT_PIN
JP7158 SHORT_PIN
JP7159 SHORT_PIN
JP7160 SHORT_PIN
R7433 0Ohm
R7434 0Ohm
R7436 0Ohm
R7252 10KOhm
Title : CODEC-ALC660
Engineer: Jay Tsai
ASUSTeK COMPUTER INC. NB6
Size Custom
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 21 of 74


To Internal Speaker Connector
CON7002
WTOB_CON_4P
1->6 V/V
0->NORMAL
TPA0212PWPRG4
Microphone In Jack
PHONE_JACK_8P
PHONE_JACK_6P
EXTERNAL MIC
R2.0
Title : AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB6
Engineer: Jay Tsai
Project Name F3T
Date: Monday, May 29, 2006

Title : MIC Pre-AMP

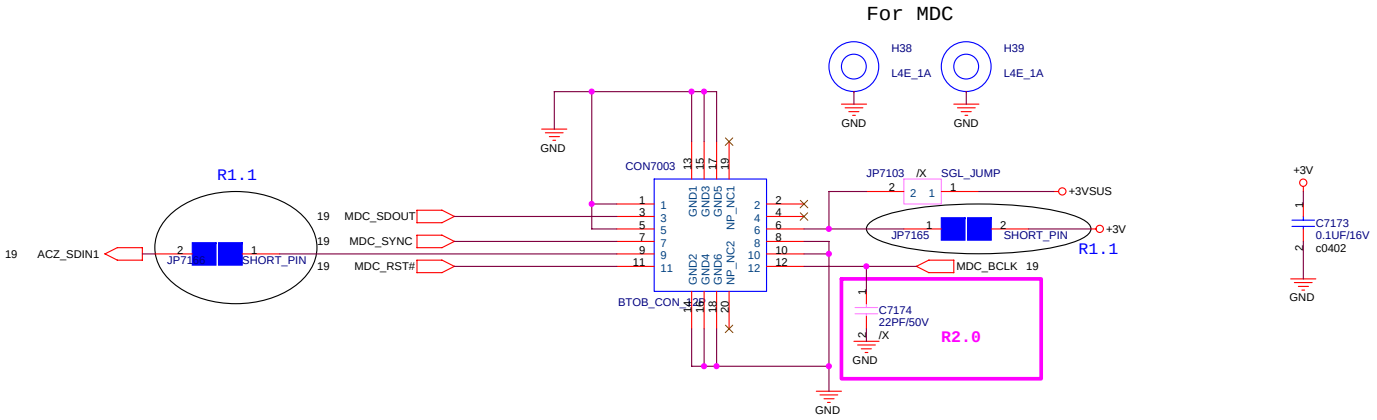
ASUSTek COMPUTER INC. NB1

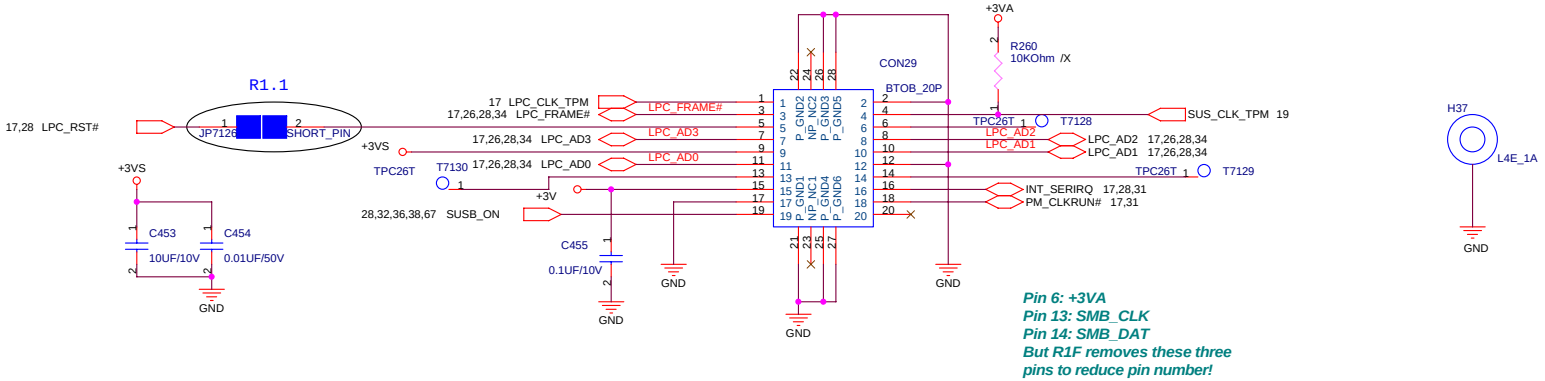
Engineer: JAY TSAI

Size	Project Name	Rev
C	F3T	1.0

Date: Monday, May 29, 2006 Sheet 23 of 74

MDC CONN.





Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

ASUSTeK COMPUTER INC	Title : MODULE-TPM/MDC	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 24 of 74	

Title : N/A

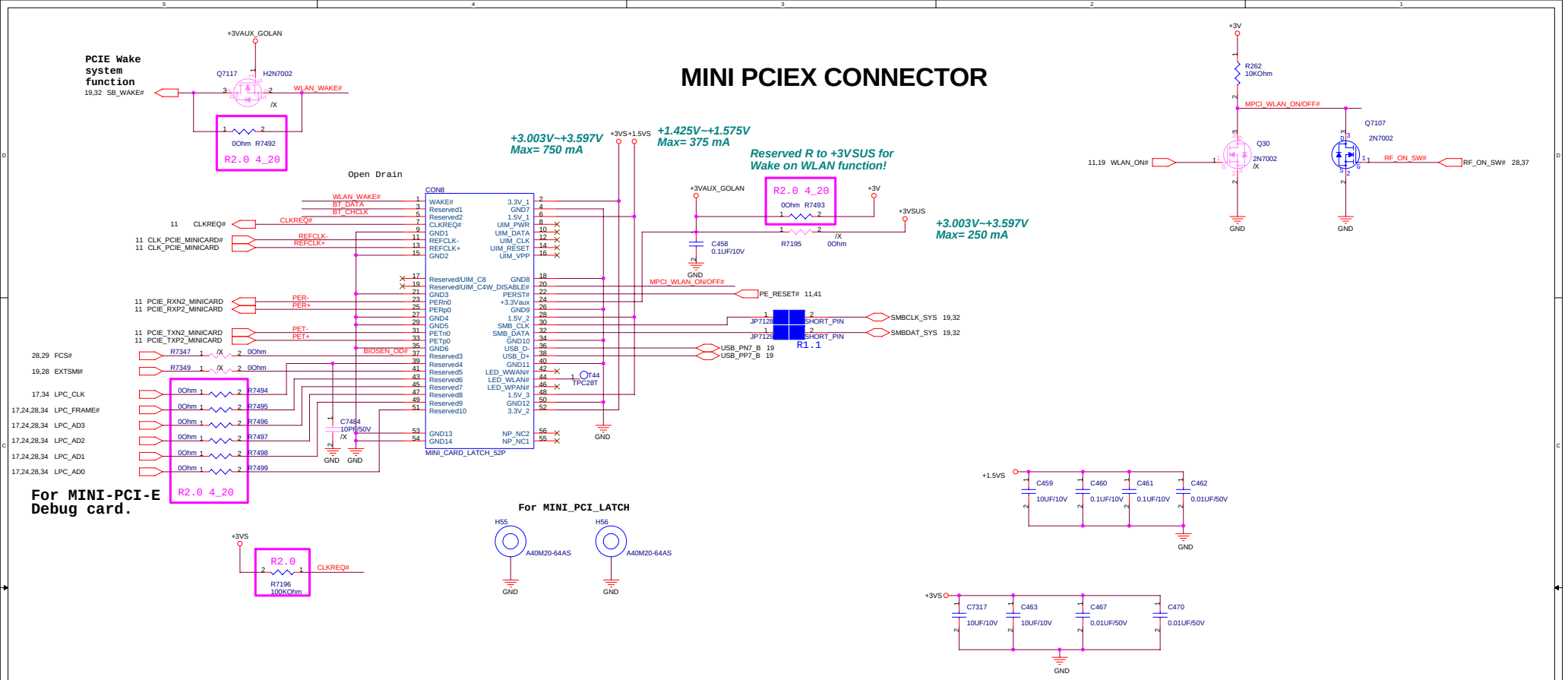
ASUSTeK COMPUTER INC

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	F3T	1.0

Date: Monday, May 29, 2006 Sheet 25 of 74

MINI PCIEX CONNECTOR



BLUETOOTH CONNECTOR

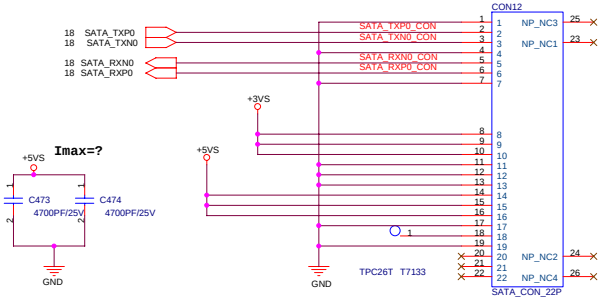
ASUSTeK COMPUTER INC
Engineer: JAY TSAI

Title : MINI PCIEX (TV) & BT Conn

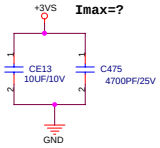
Size	Project Name	Rev
C	F3T	2.0

Date: Monday, May 29, 2006 Sheet 26 of 74

SATA_HDD

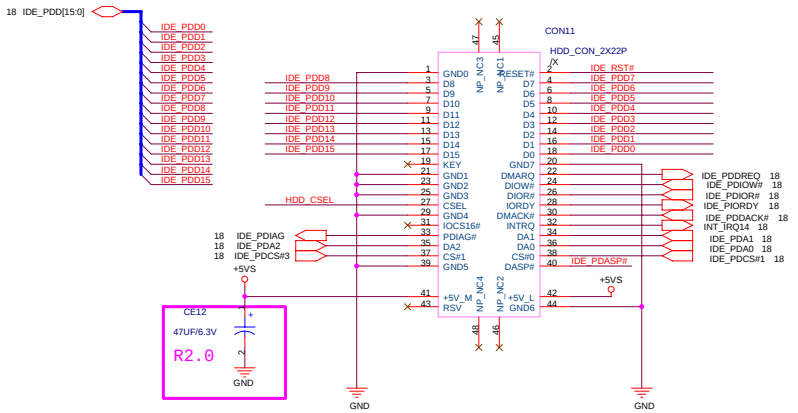


JAY0308->ME modify part number
to 12G15110022R .

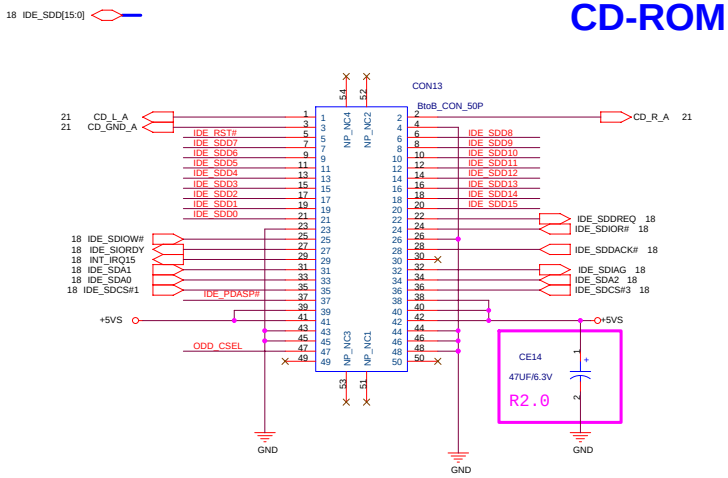


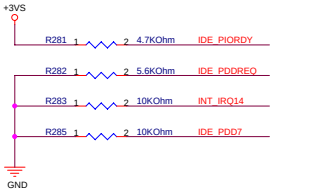
HDD

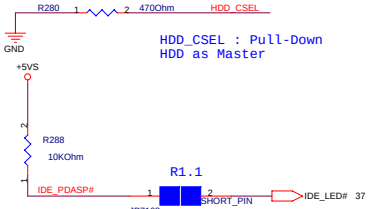
R1.1



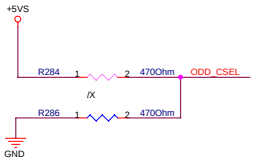
CD-ROM



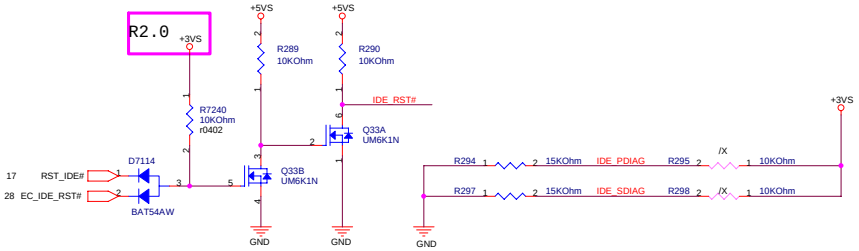


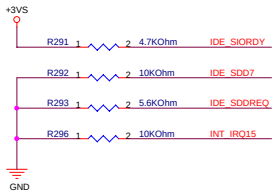


HDD_CSEL : Pull-Down
HDD as Master

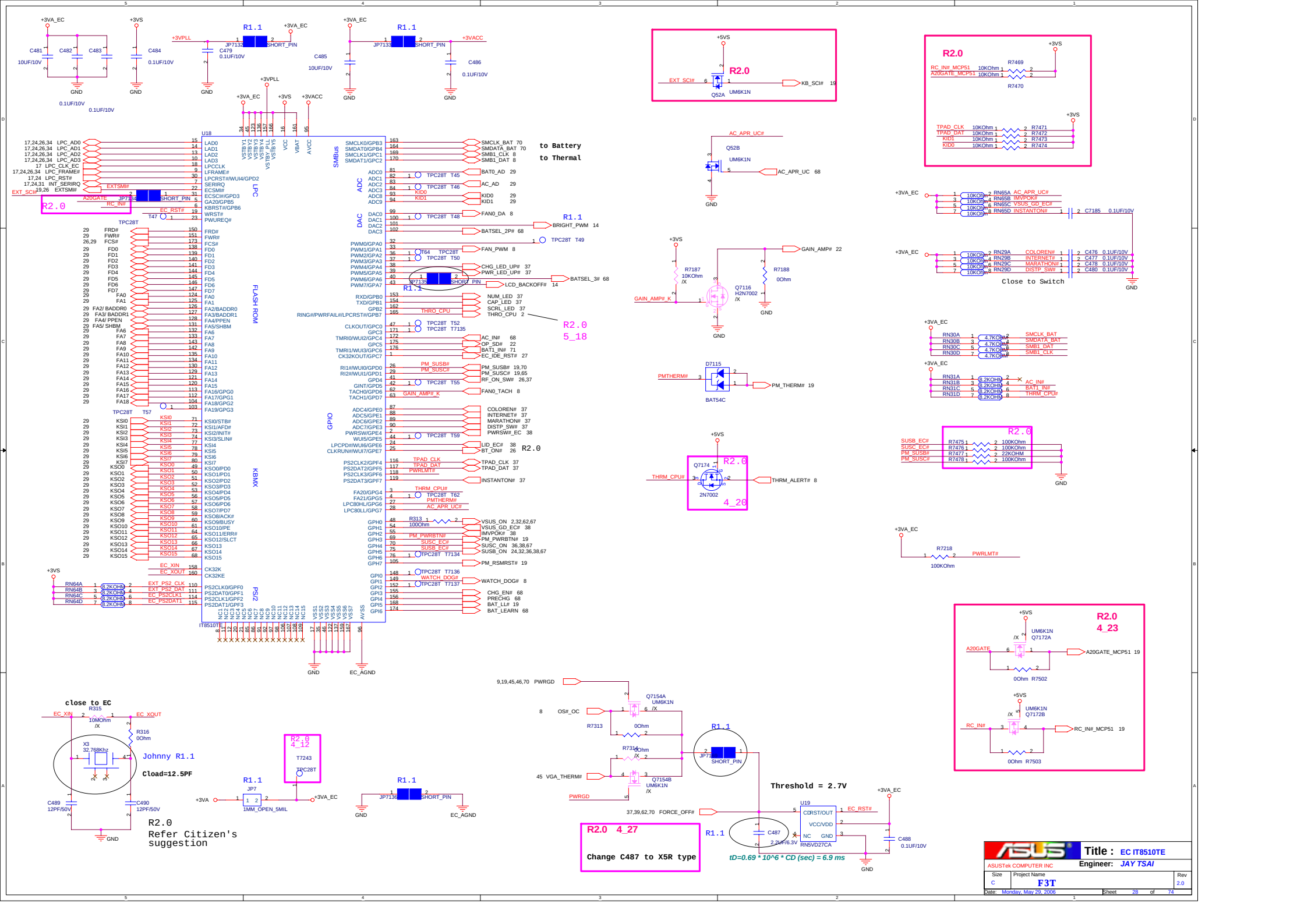


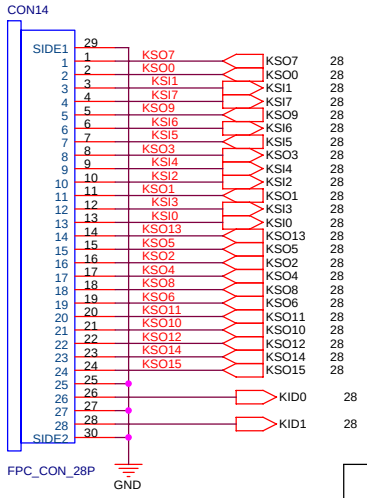
ODD_CSEL
Pull-Up: CDROM as Slave
Pull-Down: CDROM as Master



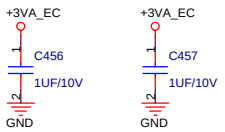


ASUSTEK CO.,LTD.	Title : HDD&ODD	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 27 of 74	


U18
IT8510TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
R2.0
R1.1
close to EC
Johnny R1.1
Cload=12.5PF
R2.0
Refer Citizen's suggestion
Threshold = 2.7V
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Change C487 to X5R type
Close to Switch
Title : EC IT8510TE
Engineer: JAY TSAI
ASUSTek COMPUTER INC
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 28 of 74



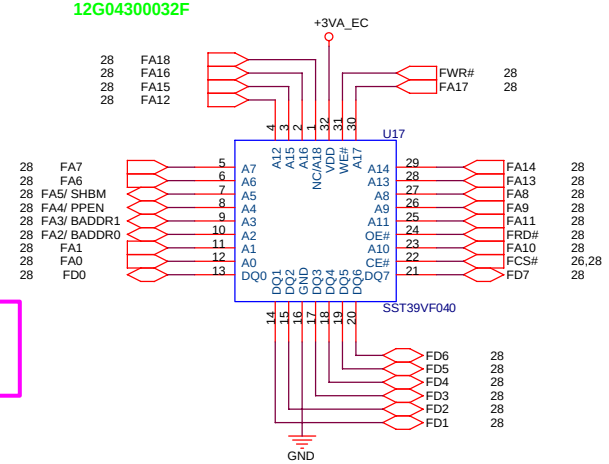
TYPE	JP	UK	US
KID1	H	H	L
KID2	L	H	L



ISA ROM

SST-PLCC32 4Mbits Flash ROM
PN:05G001014110(+3.3V)

PLCC32 Socket PN:
12G04300032F



R2.0 4_28

Mount BIOS IC

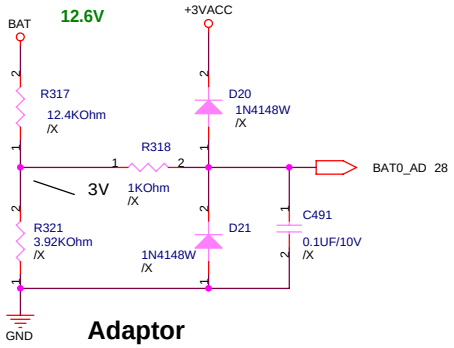
EC ADC

R2.0

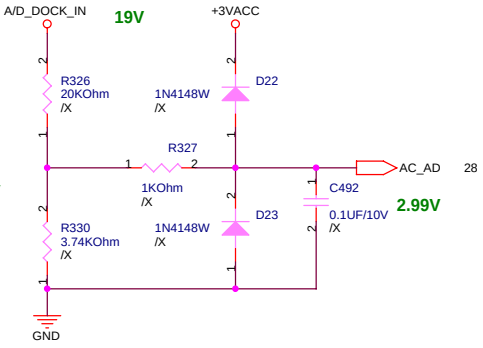
4_20

Battery

12.6V

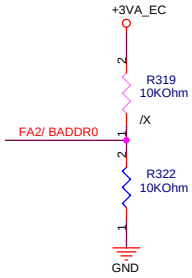


Adaptor

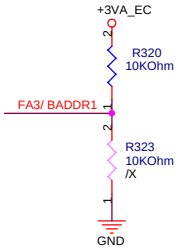


EC Hardware Strap

strap value sampled after VSTBY power up reset

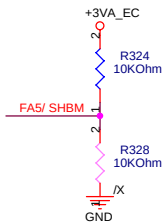


PNPCFG base address set by SWCBAHR/SWCBALR

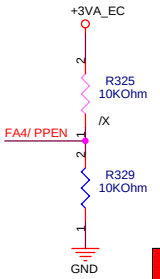


BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

Share Memory



SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS



PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

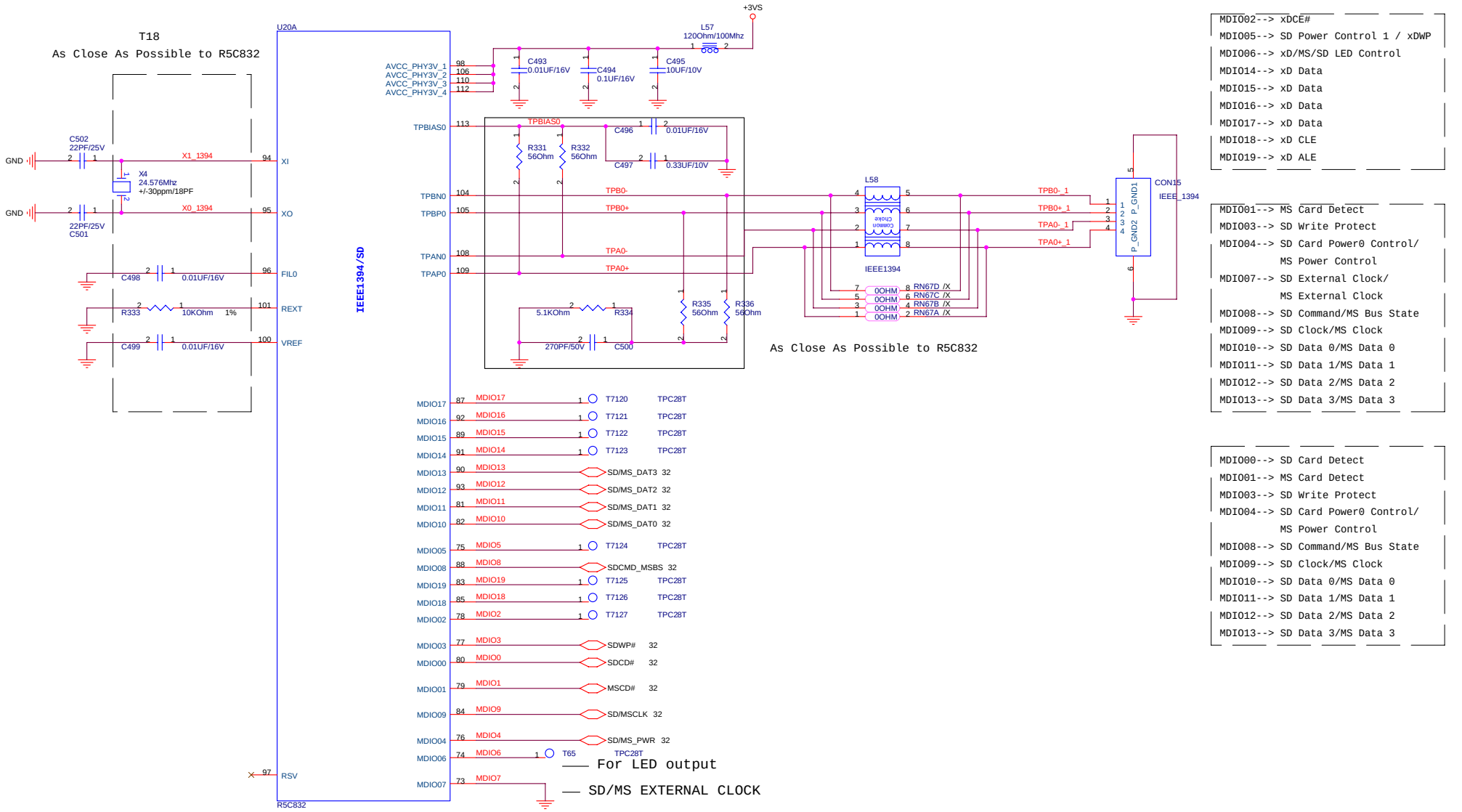
ASUSTek COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	F3T	2.0

Date: Monday, May 29, 2006 Sheet 29 of 74

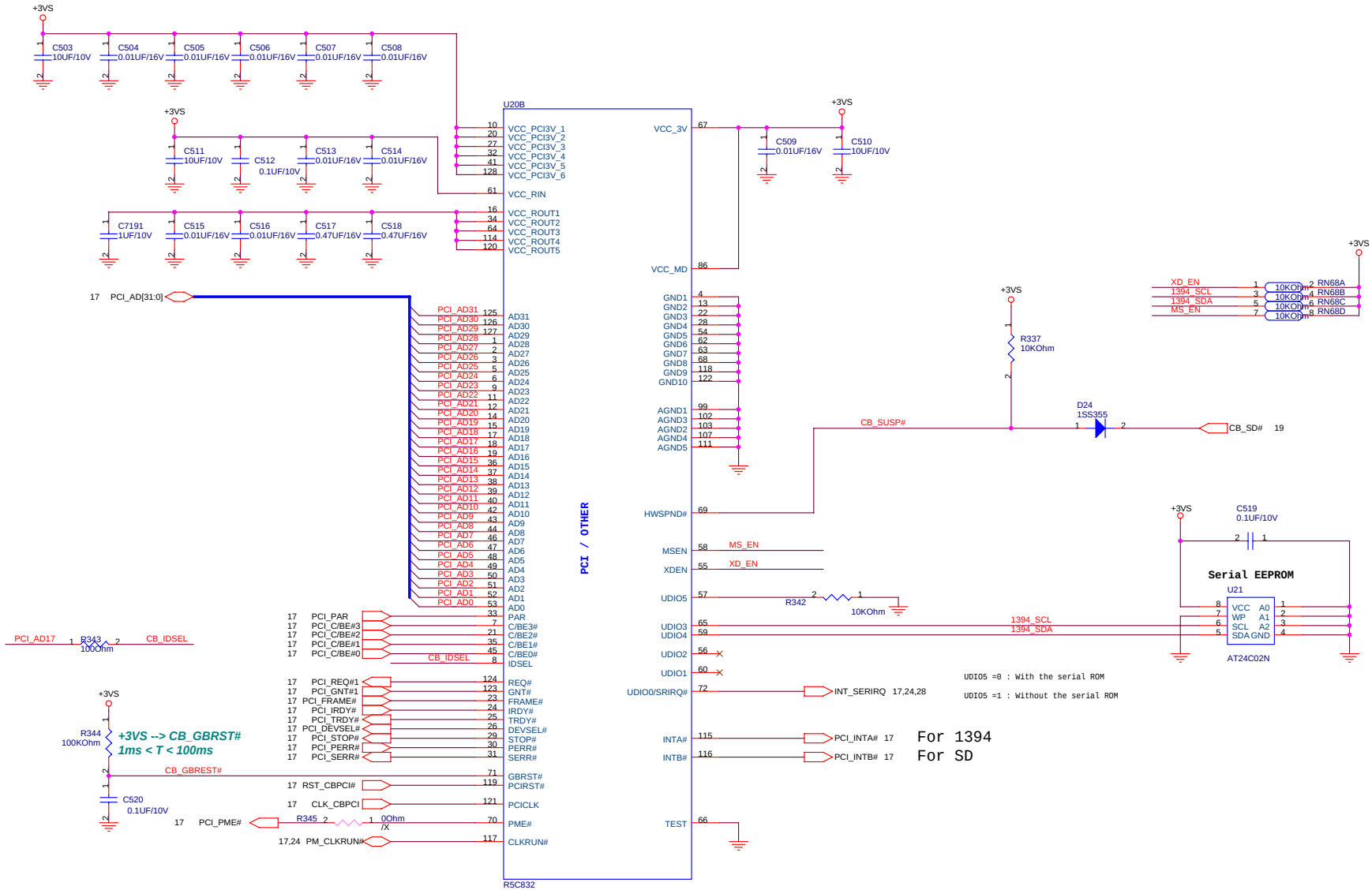


MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

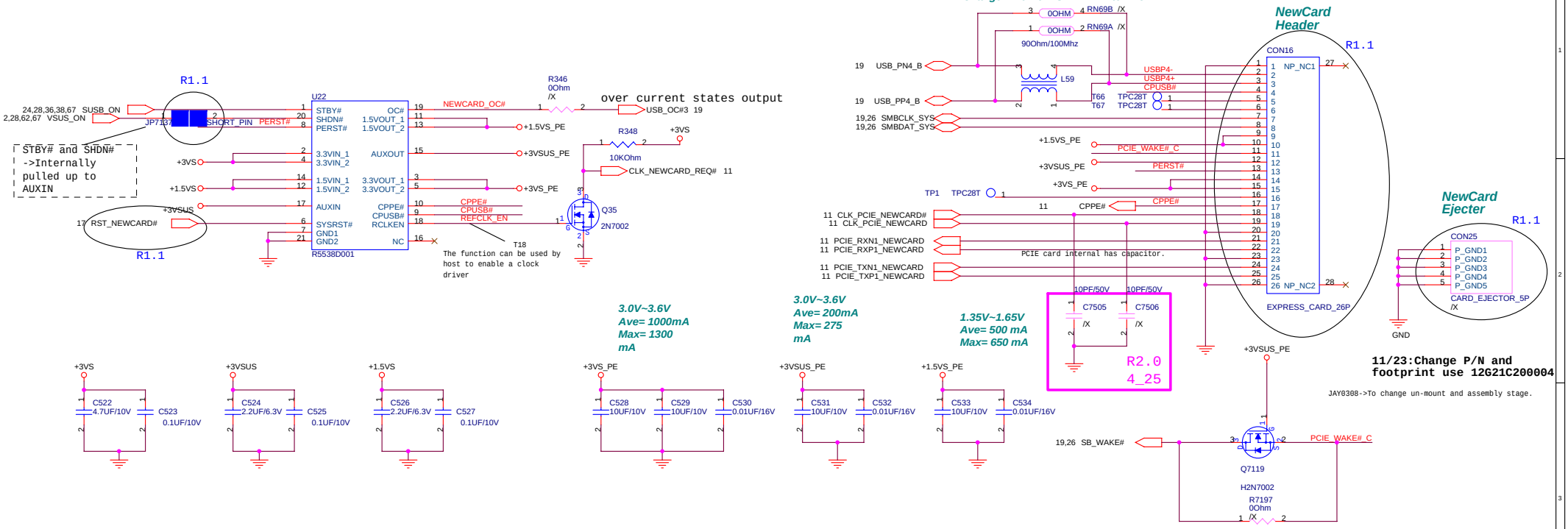
ASUSTek COMPUTER INC	Title : RICOH R5C832(1)	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 30 of 74	



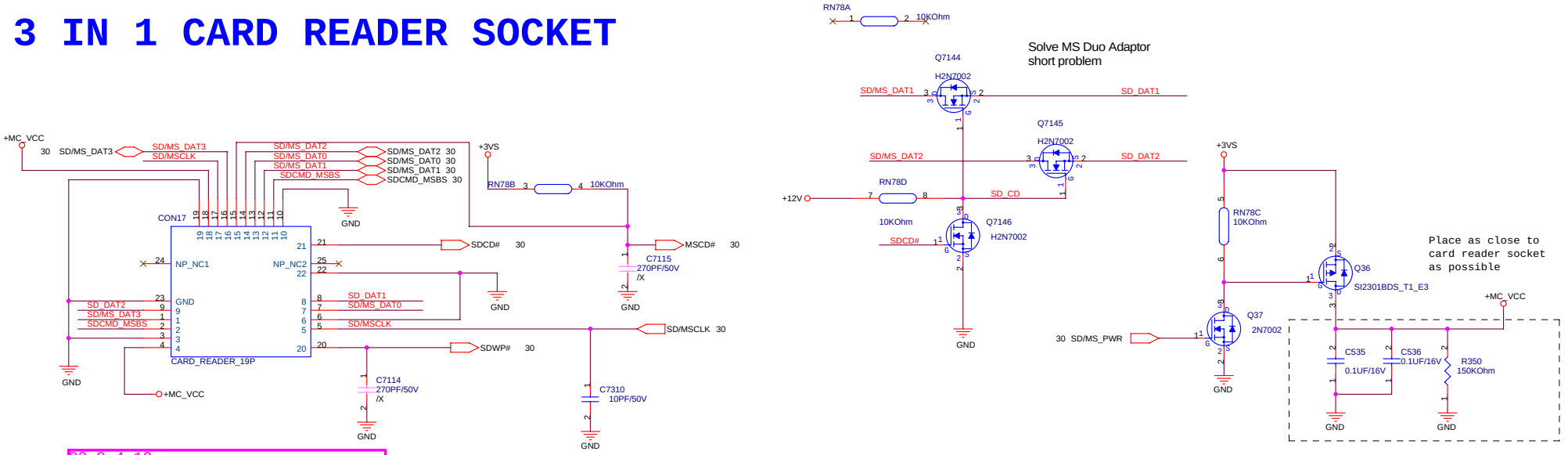
ASUSTek COMPUTER INC	Title : RICOH R5C832(2)	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 31 of 74	

NEW CARD SOCKET

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

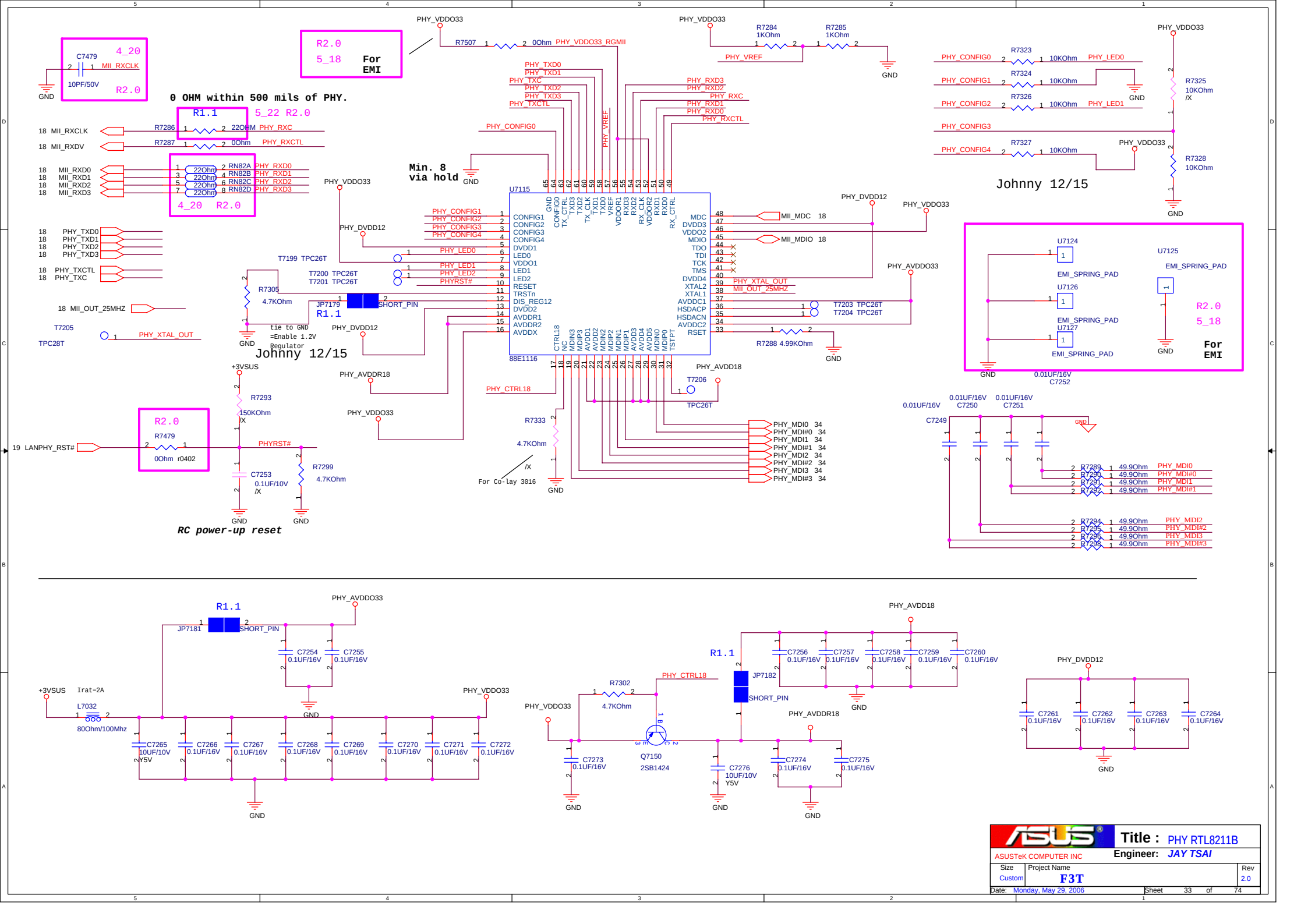


3 IN 1 CARD READER SOCKET



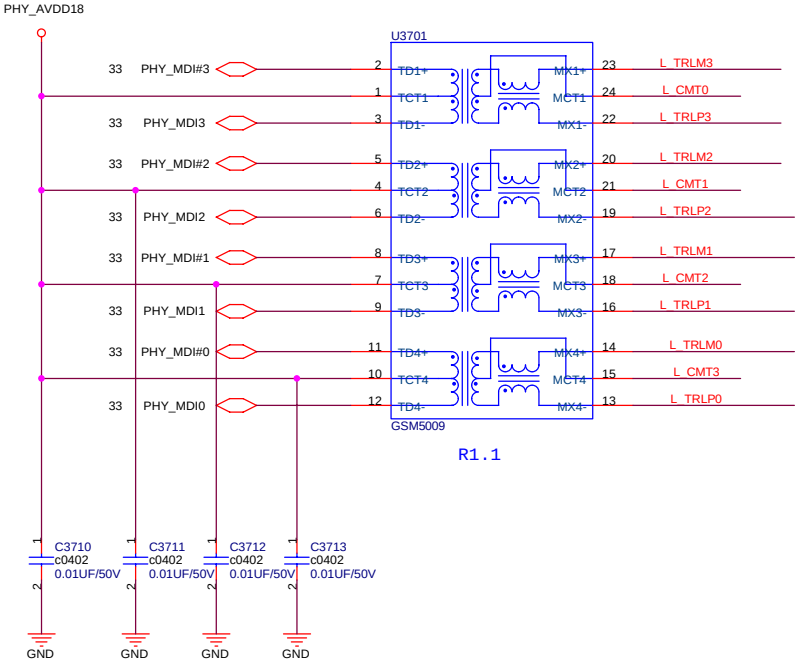
R2.0 4_19
P/N change from 12G340001911 to 12G340001920

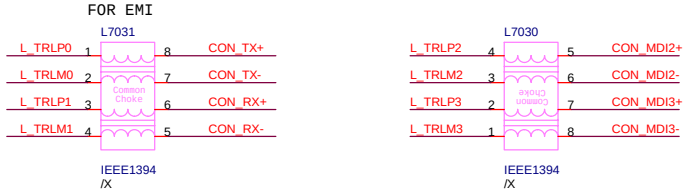
ASUSTek COMPUTER INC	Title : NEWCARD&CARD READER	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 32 of 74	

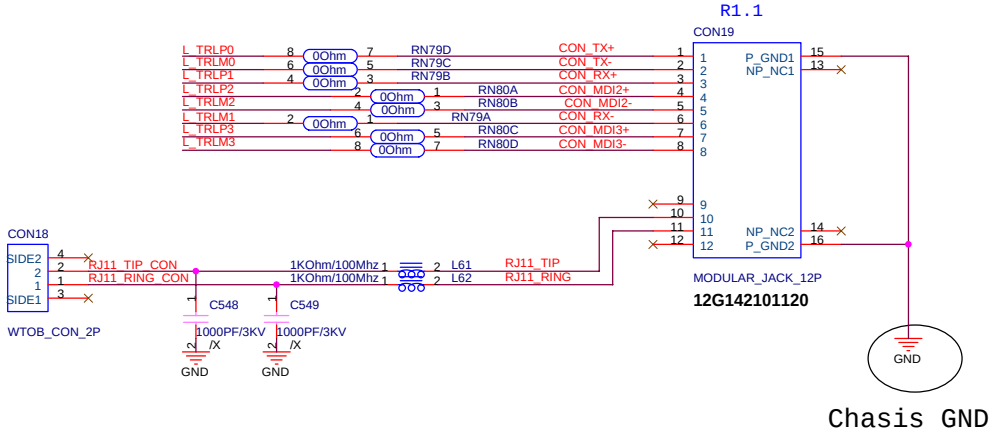


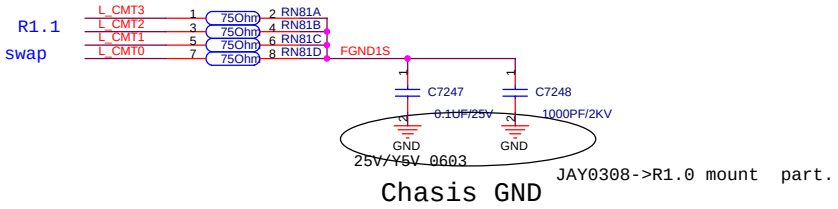
ASUSTeK COMPUTER INC	Title : PHY RTL8211B	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 33 of 74	

LAN PORT

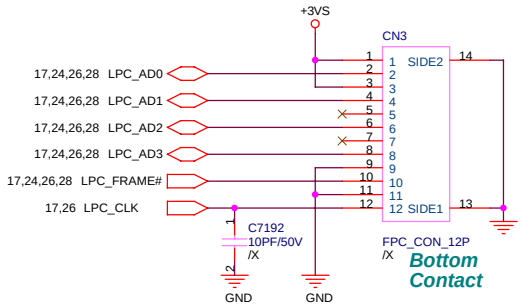




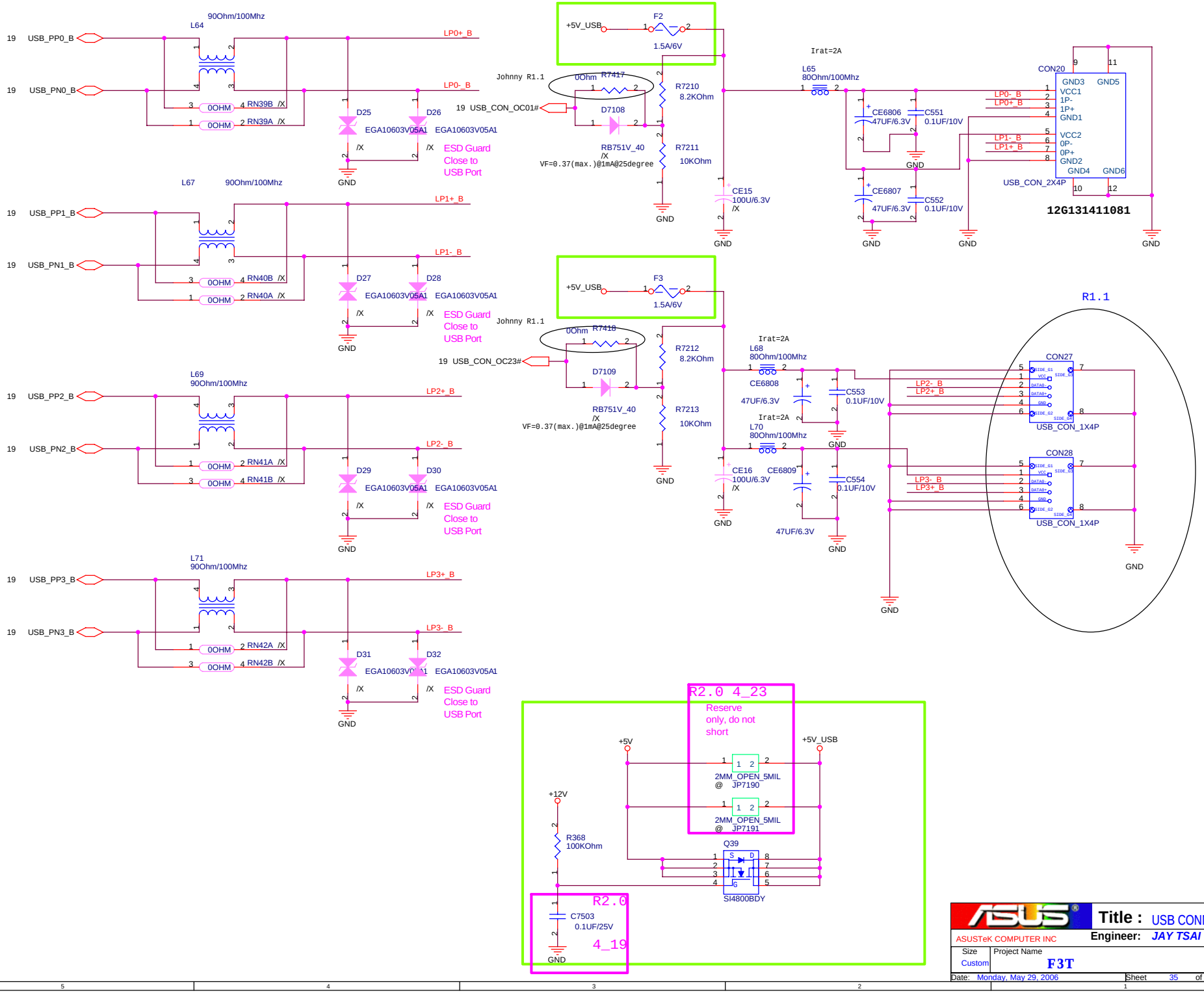




LPC DEGUG CONNCTOR



ASUSTeK COMPUTER INC	Title : RJ11+45	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 34 of 74	



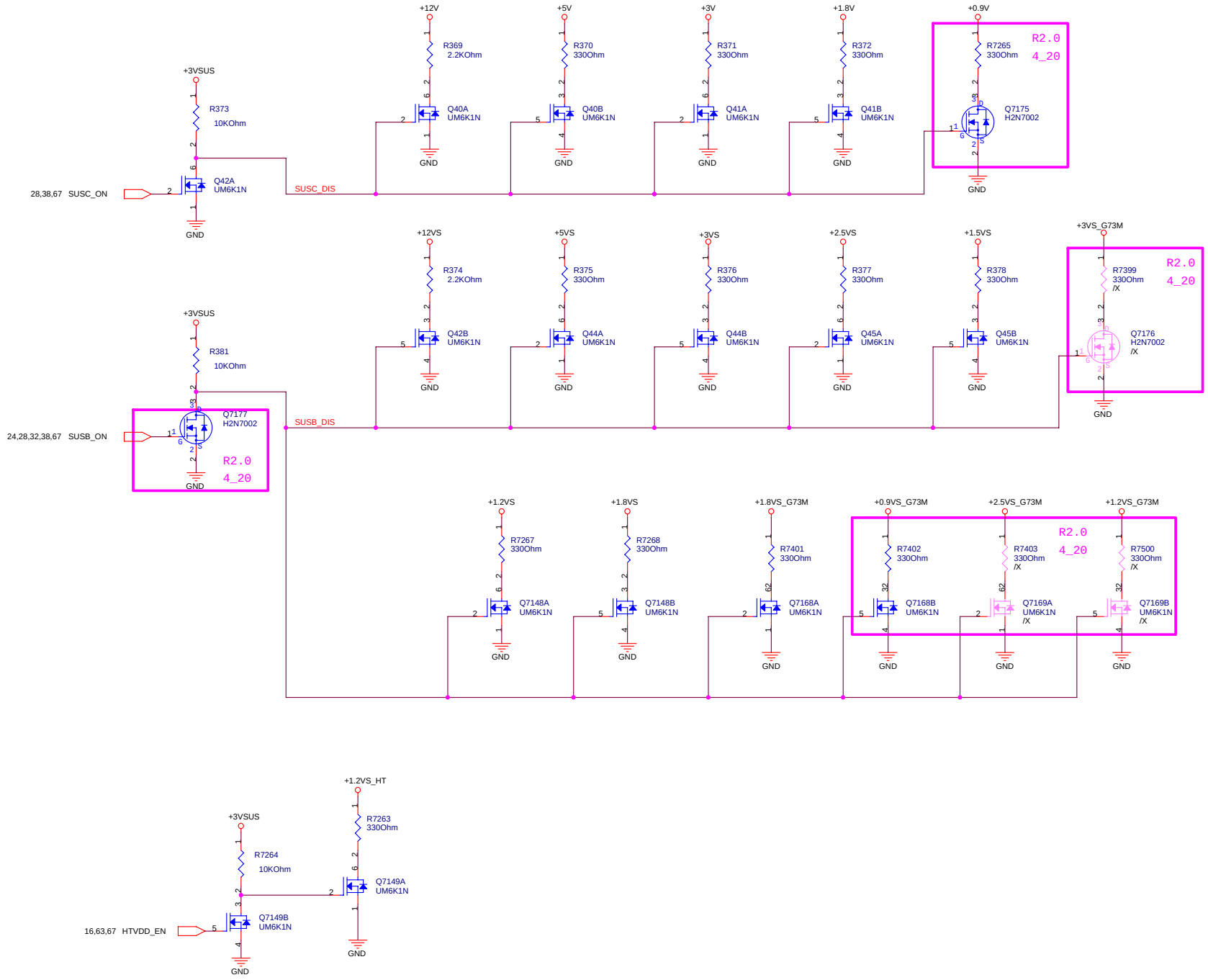
ASUSTeK COMPUTER INC

Title : USB CONN X 4

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	F3T	2.0

Date: Monday, May 29, 2006 Sheet 35 of 74



ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 36 of 74	

R2.0 4_27
ME change T.P switch from
12G09103004E to 12G09103004P

PWR_SW# 38
DISTP_SW# 28
MARATHON# 28
COLOREN# 28
INSTANTON# 28
INTERNET# 28
SW3 SW4 SW6 SW7 SW8 SW5
TP_SWITCH_4P
GND

For Side SW

+3VA_EC
R7125 10KOhm
R7126 330Ohm
C7121 0.1UF/10V
26,28 RF_ON_SW#
SW9 SLIDE_SWITCH_6P
GND

SHUT_DOWN#

+3VA
R1.1 3/10 R7224 100KOhm /X
C7207 0.1UF/16V /X
FORCE_OFF#
SW10 TP_SWITCH_4P
FORCE_OFF# 28,39,62,70
GND

R2.0 4_27
LED 1,2,3,5,6,7,8 P/N change from
07G015700021 to 07G015700341

LED 4 P/N change from
07G015700024 to 07G015700064

for Cap. Lock

+5VS
R7201 330Ohm
LED5 GREEN
CAP_LED#
28 CAP_LED
Q7121 H2N7002
GND

for Num Lock

+5VS
R7202 330Ohm
LED8 GREEN
NUM_LED#
28 NUM_LED
Q7123 H2N7002
GND

for Scroll Lock

+5VS
R7203 330Ohm
LED7 GREEN
SCRL_LED#
28 SCRL_LED
Q7122 H2N7002
GND

For SATA/IDE LED

+5VS
R7209 330Ohm
LED6 GREEN
HDD_LED#

R2.0
+12VS
+3VS
RN71A 8.2KOHM
RN71B 8.2KOHM
D33 BAT54AW
18 SATA_LED#
27 IDE_LED#
Q7125 H2N7002
Q7124 H2N7002
GND

TOUCH PAD SWITCH

TP_LEFT_SW#
TP_RIGHT_SW#
SW2 SW1 TP_SWITCH_4P
D35 D34 181K /X
12G091030050
GND

TP_RIGHT_SW#
TP_LEFT_SW#
CON23 FPC_CON_12P
12G18340120A
+5VS
+5VS_TP
L72 80Ohm/100Mhz
C555 0.1UF/10V
28 TPAD_CLK
28 TPAD_DAT

For POWER LED

R1.1
+5VSUS
R7204 330Ohm
LED2 GREEN
PWR_LED#
RN71C 8.2KOHM
Q7127 H2N7002
Q7130 H2N7002
28 PWR_LED_UP#
GND

For BT LED

+5VS
R7205 330Ohm
LED1 GREEN
BT_LEDON#
+3VSUS
R2.0
RN71D 8.2KOHM
RN72A 8.2KOHM
Q7126 H2N7002
Q7129 H2N7002
19 BTLED_ON#
GND

For WireLess LED

+5VS
R7206 330Ohm
LED3 GREEN
WLANLED_EN#
+3VSUS
R2.0
RN72B 8.2KOHM
RN72C 8.2KOHM
Q7128 H2N7002
Q7131 H2N7002
19 WLAN_LED_EN#
GND

R1.1
+5VO
+5VSUS
JP7104 1MM_OPEN_5MIL

For BATTERY LED

+5VLCM
R7207 330Ohm
LED4 ORANGE
CHG_LED#

R1.1
+5VSUS
RN72D 8.2KOHM
Q7132 H2N7002
Q7134 H2N7002
28 CHG_LED_UP#
GND

R2.0
Delete T/P LED circuit

ASUSTeK COMPUTER INC	Title : LED/SW/TouchPad	
	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 37 of 74	

POWER SWITCH

28,36,67 SUSC_ON — JP7138 SHORT_PIN — SUSC# 17

24,28,32,36,67 SUSB_ON — JP7139 SHORT_PIN — SUSB# 14,44

R1.1

R2.0 5_4 Change to for P/N

R1.1 3/10

+3VA — U15C, U15A, U15D, U15B — 74LVC14APW/G /X

+3VSUS — R7189 100KOhm — Q55 2N7002 — VSUS_GD_EC# 28

62,70 VSUS_GD# — C7186 0.1UF/10V

For SB timing 10ms.

+3VSUS — R395 100KOhm /X — Q56 2N7002 — IMVPOK# 28

61,70 CPUPWR_GD

JP7140 SHORT_PIN — CPU_VLD 16

R1.1

28 PWRSW#_EC — R7219 0Ohm /X — U15E, U15F — 74LVC14APW/G /X

R7220 0Ohm

PWR_ON# — R398 1MOhm /X — C557 0.22UF/10V /X

D36 RB751V_40 /X — SW_SW# — Q57 2N7002 /X

R397 100KOhm /X — C558 0.1UF/10V /X

R2.0 4_12 T7244 TPC28T — PWR_SW# — PWR_SW# 37

+3VA_EC — R7221 100KOhm — R7222 33Ohm — C7196 0.1UF/10V — GND

R2.0 — R400 100KOhm

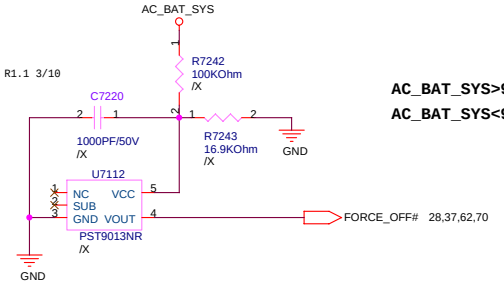
JP7141 SHORT_PIN — LID_EC# 28

R2.0 4_22 — D37 1SS355 /X — LID_SW# 14

C559 0.1UF/10V — R7501 0Ohm

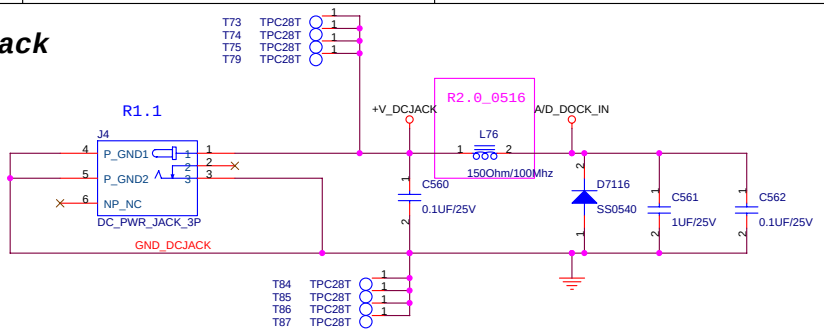
ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
Engineer: JAY TSAI		
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 38 of 74	

Without Battery & Pull out Adapter



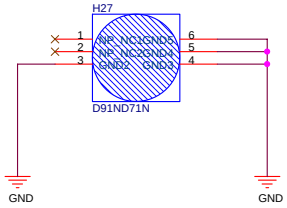
AC_BAT_SYS>9V =1
AC_BAT_SYS<9V =0

DC Power Jack

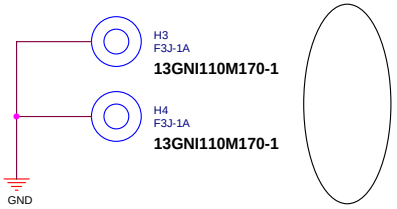


Note:Reserved

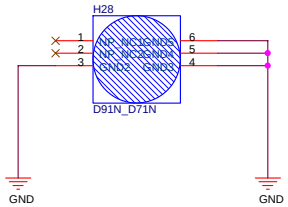
FOR LEFT UNDER



FOR FAN

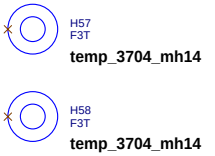


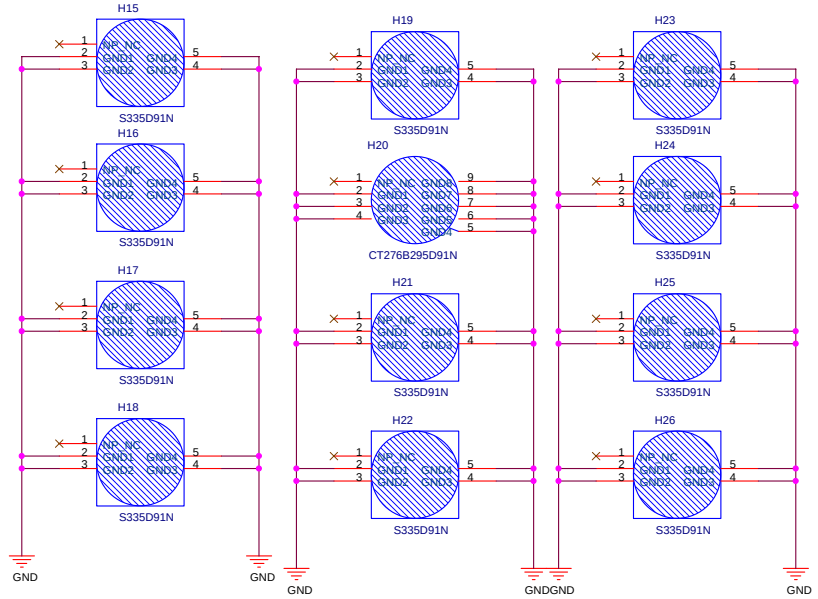
FOR RIGHT UP



R2.0
4_20

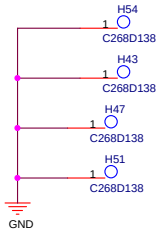
FOR FAN
Fix Hole
position



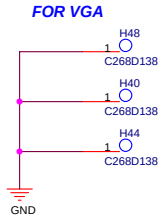


FOR SCREW HOLE

FOR CPU



FOR VGA



ASUSTeK COMPUTER INC	Title : DC/ BATT IN & Screw Hole	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 39 of 74	

Title :	N/A
ASUSTeK COMPUTER INC	Engineer: JAY TSAI
Size: Custom	Project Name: F3T
Rev: 1.0	
Date: Monday, May 29, 2006	Sheet 40 of 74

11 PCIEG_RXP[0:15]
11 PCIEG_RXN[0:15]
11 PCIENB_RXP[0:15]
11 PCIENB_RXN[0:15]

2nd source
P/N:02G190009710

N.V suggest ,Dual layout

U7113
NCTSZ32M5X_NL
/X
+3VS_G73M
R1.1
GND
11,26 PE_RESET#
R405 0Ohm
R7315 100Ohm
Johnny R1.1
10KOhm
R7316
/X
PE_RESET#_R
R1.1
GND

Polarity
Inversion:PCIENB_RXP1,2,4,6,10,14/PCIENB_RXN1,2,4,6,10,14

U25A

T7142 TPC28T PEX_TSTCLK_OUT AM12
T7143 TPC28T PEX_TSTCLK_OUT# AM11
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*

11 CLK_PCIE_GFX AH14 PEX_REFCLK
11 CLK_PCIE_GFX# AJ14 PEX_REFCLK*

C593 0.1UF

PCIENB_RXP0 C594 0.1UF	PCIEG_TXP0	AJ15	PEX_TX0
	PCIEG_TXN0	AK15	PEX_TX0*
PCIEG_RXP0		AK13	PEX_RX0
PCIEG_RXN0		AK14	PEX_RX0*
C595			
PCIENB_RXN1 C596 0.1UF	PCIEG_TXP1	AH16	PEX_TX1
	PCIEG_TXN1	AG16	PEX_TX1*
PCIEG_RXP1		AM14	PEX_RX1
PCIEG_RXN1		AM15	PEX_RX1*
PCIENB_RXN2 C597 0.1UF	PCIEG_TXP2	AG17	PEX_TX2
PCIENB_RXP2 C598 0.1UF	PCIEG_TXN2	AH17	PEX_TX2*
PCIEG_RXP2		AL15	PEX_RX2
PCIEG_RXN2		AL16	PEX_RX2*
PCIENB_RXP3 C599 0.1UF	PCIEG_TXP3	AG18	PEX_TX3
PCIENB_RXN3 C606 0.1UF	PCIEG_TXN3	AH18	PEX_TX3*
PCIEG_RXP3		AK16	PEX_RX3
PCIEG_RXN3		AK17	PEX_RX3*
PCIENB_RXN4 C607 0.1UF	PCIEG_TXP4	AK18	PEX_TX4
PCIENB_RXP4 C608 0.1UF	PCIEG_TXN4	AJ18	PEX_TX4*
PCIEG_RXP4		AL17	PEX_RX4
PCIEG_RXN4		AL18	PEX_RX4*
PCIENB_RXP5 C612 0.1UF	PCIEG_TXP5	AJ19	PEX_TX5
PCIENB_RXN5 C613 0.1UF	PCIEG_TXN5	AH19	PEX_TX5*
PCIEG_RXP5		AM18	PEX_RX5
PCIEG_RXN5		AM19	PEX_RX5*
PCIENB_RXN6 C614 0.1UF	PCIEG_TXP6	AG20	PEX_TX6
PCIENB_RXP6 C615 0.1UF	PCIEG_TXN6	AH20	PEX_TX6*
PCIEG_RXP6		AK19	PEX_RX6
PCIEG_RXN6		AK20	PEX_RX6*
PCIENB_RXP7 C616 0.1UF	PCIEG_TXP7	AG21	PEX_TX7
PCIENB_RXN7 C617 0.1UF	PCIEG_TXN7	AH21	PEX_TX7*
PCIEG_RXP7		AL20	PEX_RX7
PCIEG_RXN7		AL21	PEX_RX7*
PCIENB_RXP8 C623 0.1UF	PCIEG_TXP8	AK21	PEX_TX8
PCIENB_RXN8 C624 0.1UF	PCIEG_TXN8	AJ21	PEX_TX8*
PCIEG_RXP8		AM21	PEX_RX8
PCIEG_RXN8		AM22	PEX_RX8*
PCIENB_RXP9 C625 0.1UF	PCIEG_TXP9	AJ22	PEX_TX9
PCIENB_RXN9 C626 0.1UF	PCIEG_TXN9	AH22	PEX_TX9*
PCIEG_RXP9		AK22	PEX_RX9
PCIEG_RXN9		AK23	PEX_RX9*
PCIENB_RXN10 C631 0.1UF	PCIEG_TXP10	AG23	PEX_TX10
PCIENB_RXP10 C632 0.1UF	PCIEG_TXN10	AH23	PEX_TX10*
PCIEG_RXP10		AL23	PEX_RX10
PCIEG_RXN10		AL24	PEX_RX10*
PCIENB_RXP11 C633 0.1UF	PCIEG_TXP11	AK24	PEX_TX11
PCIENB_RXN11 C634 0.1UF	PCIEG_TXN11	AJ24	PEX_TX11*
PCIEG_RXP11		AM24	PEX_RX11
PCIEG_RXN11		AM25	PEX_RX11*
PCIENB_RXP12 C639 0.1UF	PCIEG_TXP12	AJ25	PEX_TX12
PCIENB_RXN12 C640 0.1UF	PCIEG_TXN12	AH25	PEX_TX12*
PCIEG_RXP12		AK25	PEX_RX12
PCIEG_RXN12		AK26	PEX_RX12*
PCIENB_RXP13 C641 0.1UF	PCIEG_TXP13	AH26	PEX_TX13
PCIENB_RXN13 C642 0.1UF	PCIEG_TXN13	AG26	PEX_TX13*
PCIEG_RXP13		AL26	PEX_RX13
PCIEG_RXN13		AL27	PEX_RX13*
PCIENB_RXN14 C643 0.1UF	PCIEG_TXP14	AK27	PEX_TX14
PCIENB_RXP14 C644 0.1UF	PCIEG_TXN14	AJ27	PEX_TX14*
PCIEG_RXP14		AM27	PEX_RX14
PCIEG_RXN14		AM28	PEX_RX14*
PCIENB_RXP15 C645 0.1UF	PCIEG_TXP15	AJ28	PEX_TX15
PCIENB_RXN15 C646 0.1UF	PCIEG_TXN15	AH27	PEX_TX15*
PCIEG_RXP15		AL28	PEX_RX15
PCIEG_RXN15		AL29	PEX_RX15*

G73M

R1.1
at least 80 mils
+1.2VS_G73M
+1.2VSP_PEXIOVDD
PEX_IOVDD_0 AD23
PEX_IOVDD_1 AE23
PEX_IOVDD_2 AE24
PEX_IOVDD_3 AE25
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AG25
C567 0.1UF
C568 1UF/10V c0603
C569 4.7UF/6.3V
1.42 A
+1.2VS_G73M R1.1
+1.2VSP_PEXIOVDD
GND
PEX_IOVDDQ_0 AC16
PEX_IOVDDQ_1 AC17
PEX_IOVDDQ_2 AC21
PEX_IOVDDQ_3 AC22
PEX_IOVDDQ_4 AE18
PEX_IOVDDQ_5 AE21
PEX_IOVDDQ_6 AE22
PEX_IOVDDQ_7 AE12
PEX_IOVDDQ_8 AF18
PEX_IOVDDQ_9 AF21
PEX_IOVDDQ_10 AF22
C572 C573 C574 C575 0.1UF
place near Balls
GND

G72M 10A
G73M 16.25 A
VGA_VCORE
place north of GPU bottom side
VDD_0 K16
VDD_1 K17
VDD_2 N13
VDD_3 N14
VDD_4 N16
VDD_5 N17
VDD_6 N19
VDD_7 N20
VDD_8 P13
VDD_9 P14
VDD_10 P16
VDD_11 P17
VDD_12 P19
VDD_13 R16
VDD_14 R17
VDD_15 T13
VDD_16 T14
VDD_17 T15
VDD_18 T18
VDD_19 T19
C579 C580 C582 0.1UF
T92
TPC28T
place sourth of GPU bottom side
C585 C586 C587 C589 C590 0.1UF
C591 22UF/6.3V
C592 22UF/6.3V
GND
+1.2VSP_NV_PLLAVDD
T13=NV_PLLAVDD for G73*

place west of GPU bottom side
VGA_VCORE
VDD_20 U13
VDD_21 U14
VDD_22 U15
VDD_23 U18
VDD_24 U19
VDD_25 V16
VDD_26 V17
VDD_27 W13
VDD_28 W14
VDD_29 W16
VDD_30 W17
VDD_31 W19
VDD_32 Y13
VDD_33 Y14
VDD_34 Y16
VDD_35 Y17
VDD_36 Y19
VDD_37 Y20
C600 C601 C602 C603 C605 0.1UF
C609 C610 0.1UF
C611 22UF/6.3V
GND
VDD_LP_0 P20
VDD_LP_1 T20
VDD_LP_2 T23
VDD_LP_3 U20
VDD_LP_4 U23
VDD_LP_5 W20

R1.1
+3VS_G73M
110 mA
VDD33_0 AC11
VDD33_1 AC12
VDD33_2 AC24
VDD33_3 AD24
VDD33_4 AE11
VDD33_5 AE12
VDD33_6 H7
VDD33_7 J7
VDD33_8 K7
VDD33_9 L10
VDD33_10 L7
VDD33_11 L8
VDD33_12 M10
C622 C620 C621 0.1UF
C7204 1UF/10V c0603
GND
R1.1
+1.2VS_G73M
at least 12 mils
100 mA
L79 220Ohm
Place near L1202
PEX_PLLAVDD AF15 +1.2VSP_PEX_PLLAVDD
PEX_PLLDVDD AE15 +1.2VSP_PEX_PLLDVDD
PEX_PLLGND AE16
C628 0.1UF
C629 1UF/10V c0603
C630 4.7UF/6.3V
GND
20 mA
L80 220Ohm
C636 0.1UF
C637 1UF/10V c0603
C638 4.7UF/6.3V
Place near L1203
GND

AM10=GND for G73*
NC_0 AM10
NC_1 AM8
NC_2 AM9
NC_3 B32
NC_4 A6
GND

at least 5 mils
8 mA
+1.2VSP_NV_PLLAVDD
+1.2VS_G73M R1.1
L78 220Ohm
C570 0.1UF
C571 4.7UF/6.3V
GND GND

R1.1

Johnny R1.1
+3VS_G73M R1.1
R7357 10KOhm
R7358 0Ohm /X
PE_RESET#_R
11,17 GPU_ON
Q7155 2N7002
C7495 0.1UF /X

<Variant Name>

ASUSTek COMPUTER INC
Title : G73M(1)_PCI-E
Engineer: JAY TSAI
Size C
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 41 of 74

INFINEON 03G151236011 DDR2 16M*16-2.5 1.8V INFINEON/HYB18T256161AFL-25
HYNIX 03G151236210 DDR2 16M*16-2.5 1.8V HYNIX/HY5PS561621AFP-25
SAMSUNG 03G151236112 DDR2 16M*16-2.5 1.8V SAMSUNG/K4N56163QF-ZC25

U25B

FBAD0 N27
FBAD1 M27
FBAD2 N28
FBAD3 L29
FBAD4 K27
FBAD5 K28
FBAD6 J29
FBAD7 J28
FBAD8 P30
FBAD9 N31
FBAD10 N30
FBAD11 N32
FBAD12 L31
FBAD13 L30
FBAD14 J30
FBAD15 L32
FBAD16 H30
FBAD17 K30
FBAD18 H31
FBAD19 F30
FBAD20 H32
FBAD21 E31
FBAD22 D30
FBAD23 E30
FBAD24 H28
FBAD25 H29
FBAD26 E29
FBAD27 J27
FBAD28 E27
FBAD29 E27
FBAD30 E28
FBAD31 F28
FBAD32 AD29
FBAD33 AE29
FBAD34 AD28
FBAD35 AC28
FBAD36 AB29
FBAD37 AA30
FBAD38 Y28
FBAD39 AB30
FBAD40 AM30
FBAD41 AE30
FBAD42 AJ31
FBAD43 AJ30
FBAD44 AJ32
FBAD45 AK29
FBAD46 AM31
FBAD47 AL30
FBAD48 AE32
FBAD49 AE30
FBAD50 AE31
FBAD51 AD30
FBAD52 AC31
FBAD53 AC32
FBAD54 AB32
FBAD55 AB31
FBAD56 AG27
FBAD57 AE28
FBAD58 AH28
FBAD59 AG28
FBAD60 AG29
FBAD61 AD27
FBAD62 AE27
FBAD63 AE28

FBADQM0 M29
FBADQM1 M30
FBADQM2 V30
FBADQM3 F29
FBADQM4 AA29
FBADQM5 AK30
FBADQM6 AC30
FBADQM7 AG30

FBAWDQS0 L28
FBAWDQS1 K31
FBAWDQS2 G32
FBAWDQS3 G28
FBAWDQS4 AB28
FBAWDQS5 AL32
FBAWDQS6 AE32
FBAWDQS7 AH30

FBARDQS0 M28
FBARDQS1 K32
FBARDQS2 G31
FBARDQS3 G27
FBARDQS4 AA28
FBARDQS5 AL31
FBARDQS6 AE31
FBARDQS7 AH29

FBADQS_WP0
FBADQS_WP1
FBADQS_WP2
FBADQS_WP3
FBADQS_WP4
FBADQS_WP5
FBADQS_WP6
FBADQS_WP7

FBADQS_RN0
FBADQS_RN1
FBADQS_RN2
FBADQS_RN3
FBADQS_RN4
FBADQS_RN5
FBADQS_RN6
FBADQS_RN7

G73M

FBVDD_0 A12
FBVDD_1 A15
FBVDD_2 A18
FBVDD_3 A21
FBVDD_4 A24
FBVDD_5 A27
FBVDD_6 A3
FBVDD_7 A30
FBVDD_8 A6
FBVDD_9 A9
FBVDD_10 AA32
FBVDD_11 AD32
FBVDD_12 AG32
FBVDD_13 AK32
FBVDD_14 C32
FBVDD_15 F32
FBVDD_16 J32
FBVDD_17 M32
FBVDD_18 R32
FBVDD_19 V32

FBVDDQ_0 AA25
FBVDDQ_1 AA26
FBVDDQ_2 AB25
FBVDDQ_3 AB26
FBVDDQ_4 G11
FBVDDQ_5 G12
FBVDDQ_6 G15
FBVDDQ_7 G18
FBVDDQ_8 G21
FBVDDQ_9 G22
FBVDDQ_10 H11
FBVDDQ_11 H12
FBVDDQ_12 H15
FBVDDQ_13 H18
FBVDDQ_14 H21
FBVDDQ_15 H22
FBVDDQ_16 L26
FBVDDQ_17 L26
FBVDDQ_18 M25
FBVDDQ_19 M26
FBVDDQ_20 R25
FBVDDQ_21 V25
FBVDDQ_22 V26
FBVDDQ_23

R1.1
+1.8VS_G73M
C648 0.022UF/16V
C649
3.6A
Place Below GPU
C650
C651 4700PF/25V
C652 4700PF/25V
C653 220PF/25V
0.022UF/16V 0.022UF/16V
GND
C654 4700PF/25V
C656 4700PF/25V
C660 0.022UF/16V
C661 4700PF/25V
C662
C666 4.7UF/6.3V
C667 0.1UF
0.022UF/16V
C668 4700PF/25V
C669
C670 0.1UF
C671 0.1UF
C672 0.1UF
C673
C674 4700PF/25V
4700PF/25V
0.022UF/16V

FBA_CMD0 P32
FBA_CMD1 P31
FBA_CMD2 U30
FBA_CMD3 Y31
FBA_CMD4 W32
FBA_CMD5 W31
FBA_CMD6 T32
FBA_CMD7 V27
FBA_CMD8 T28
FBA_CMD9 T31
FBA_CMD10 U32
FBA_CMD11 W29
FBA_CMD12 W30
FBA_CMD13 T27
FBA_CMD14 V28
FBA_CMD15 V31
FBA_CMD16 U31
FBA_CMD17 R27
FBA_CMD18 V29
FBA_CMD19 T30
FBA_CMD20 W28
FBA_CMD21 R29
FBA_CMD22 R30
FBA_CMD23 P29
FBA_CMD24 U28
FBA_CMD25 Y32
FBA_CMD26

FBA_A3 FBA_A0 FBA_A2 FBA_A1 FBE_A3 FBE_A4 FBE_A5 FBA_CS1# FBA_CS0# FBA_WE# FBA_BA0 FBA_CKE FBE_RST FBE_A2 FBA_A12 FBA_RAS# FBA_A11 FBA_A10 FBA_BA1 FBA_A8 FBA_A9 FBA_A6 FBA_A5 FBA_A7 FBA_A4 FBA_CAS#
47

FBA_CKE
R406 10KOhm
GND

FBA_CLK0 P28
FBA_CLK0* P29
FBA_CLK1 V27
FBA_CLK1* AA27

FBA_CLK0
FBA_CLK0*
R407 487Ohm
FBA_CLK1
FBA_CLK1#
R408 487Ohm
R407,R408 place at VRAM Side
487 ohm;only for G73M

R1.1
+1.8VS_G73M
FBA_RST
JP7142 1 2 SHORT_PIN
RFU2 Y30
RFU3 AC26
R411 0Ohm
FBA_DEBUG AC27
FBA_REFCLK D32
FBA_REFCLKN D31
T93 TPC28T
T94 TPC28T
R410 10KOhm /X
FBA_ODT
R412 10KOhm
GND
FBA_PLLVDD G23
FBA_PLLAVDD G25
FBA_PLLGND G24
T95 TPC28T
at least 5 mils
+1.2VSP_FBA_PLLAVDD
C676 0.01UF/25V
C677 0.1UF
GND
+1.2VS_G73M
L81 180Ohm
30 mA

DDR2: VREF = 0.5 * +1.8VS
DDR3: VREF = 0.7 * +1.8VS

+1.8VS_G73M
R415 1KOhm r0402
FB_VREF1 E32
R418 1KOhm r0402
C680 0.1UF
GND
FB_VREF1

U26 R1.1
U27 R1.1
U28 R1.1
U29 R1.1

CK CK# CKE RAS# CAS# WE# CS# NC/A13 BA0 BA1 NC/BA2 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 LDQ0/DQ0 LDQ1/DQ1 LDQ2/DQ2 LDQ3/DQ3 LDQ4/DQ4 LDQ5/DQ5 LDQ6/DQ6 LDQ7/DQ7 UDQ0/DQ0 UDQ1/DQ1 UDQ2/DQ2 UDQ3/DQ3 UDQ4/DQ4 UDQ5/DQ5 UDQ6/DQ6 UDQ7/DQ7 UDQS UDQS# LDQS LDQS# VREF VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDL VDD1 VDD2 VDD3 VDD4 VDD5 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10 VSSDL VSS1 VSS2 VSS3 VSS4 VSS5 ODT NC1 NC2 NC3 NC4 UDM LDM

HYB18T256161AFL_25

FBADQM3 FBADQM1 FBAVREF0 FBA_ODT
FBADQM0 FBADQM2 FBAVREF0 C647 0.1UF Place near U27.J2
FBADQM7 FBADQM5 FBAVREF1 FBA_ODT
FBADQM4 FBADQM6 FBAVREF1 C675 0.1UF Place near U29.J2

R1.1
+1.8VS_G73M
R413 1KOhm r0402
R414 1KOhm r0402
Place near U26.J2
Place near U28.J2
R416 1KOhm r0402
C678 0.047UF/16V
R417 1KOhm r0402
C679 0.047UF/16V
GND

<Variant Name>
<OrgName>
Title : G73M(2)-FBA
Engineer: JAY TSAI
Size: Custom
Project Name: F3T
Rev: 2.0
Date: Monday, May 29, 2006
Sheet 42 of 74

JAY1110:Change form +0.9VS to +1.8V for G73M

DDR2 Terminated FBVTT=0.5* +1.8VS
Unterminated FBVTT=+1.8VS

U25C

G73M

U30

U31

U32

U33

HYB18T256161AFL_25

R420, R421 place at VRAM Side

487 ohm;only for G73M

FBCAL_PD_VDDQ:G73* 40ohm

FBCAL_PU_GND:G73* 30ohm(N.V)

FBCAL_TERM_GND :G73* 40ohm (N.V)

place near U31.J2

place near U33.J2

place near U30.J2

place near U32.J2

<Variant Name>

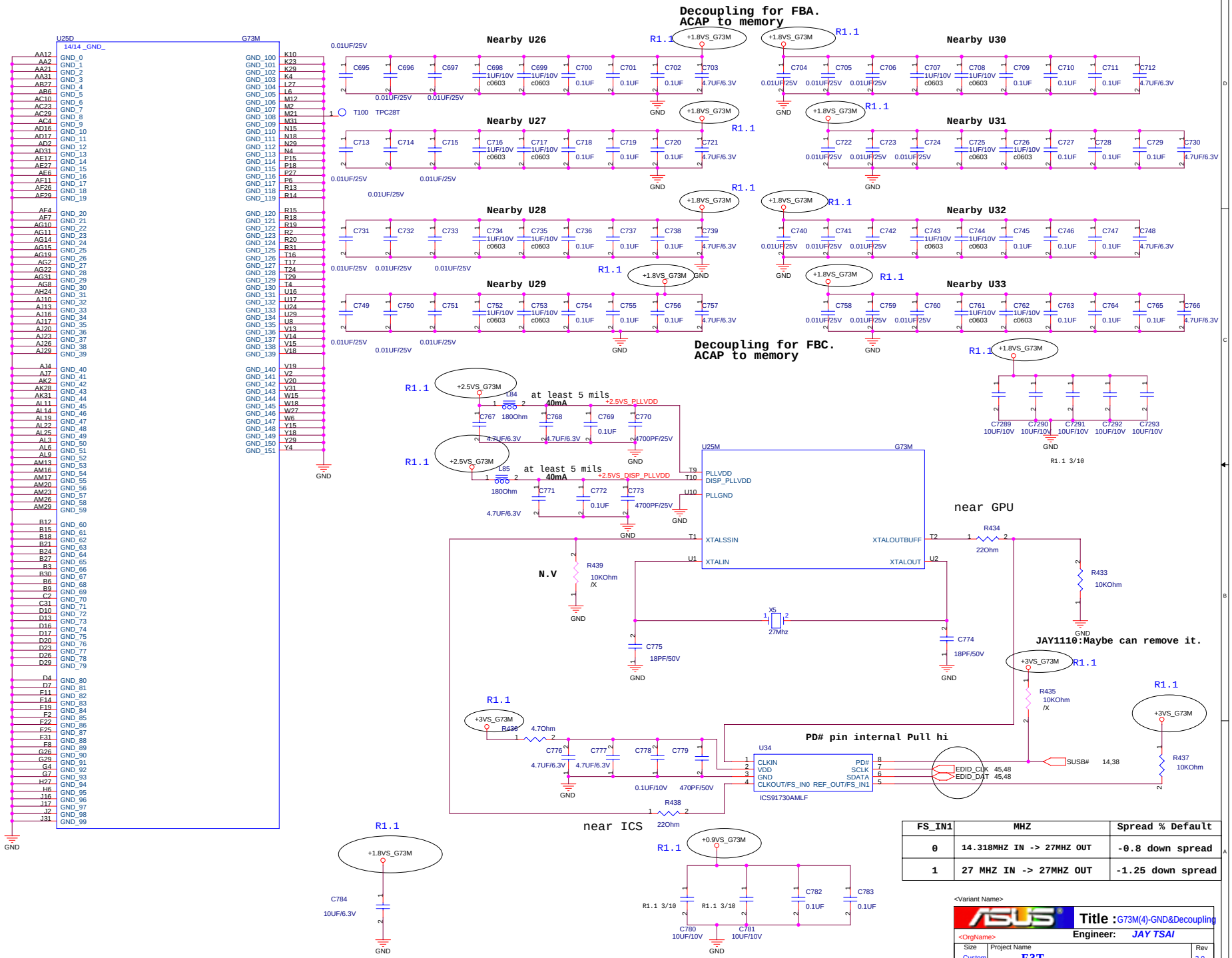
Title : G73M(3)-FBC

<OrgName>

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	F3T	2.0

Date: Monday, May 29, 2006 Sheet 43 of 74



FS_IN1	MHZ	Spread % Default
0	14.318MHZ IN -> 27MHZ OUT	-0.8 down spread
1	27 MHZ IN -> 27MHZ OUT	-1.25 down spread

<Variant Name>

ASUS

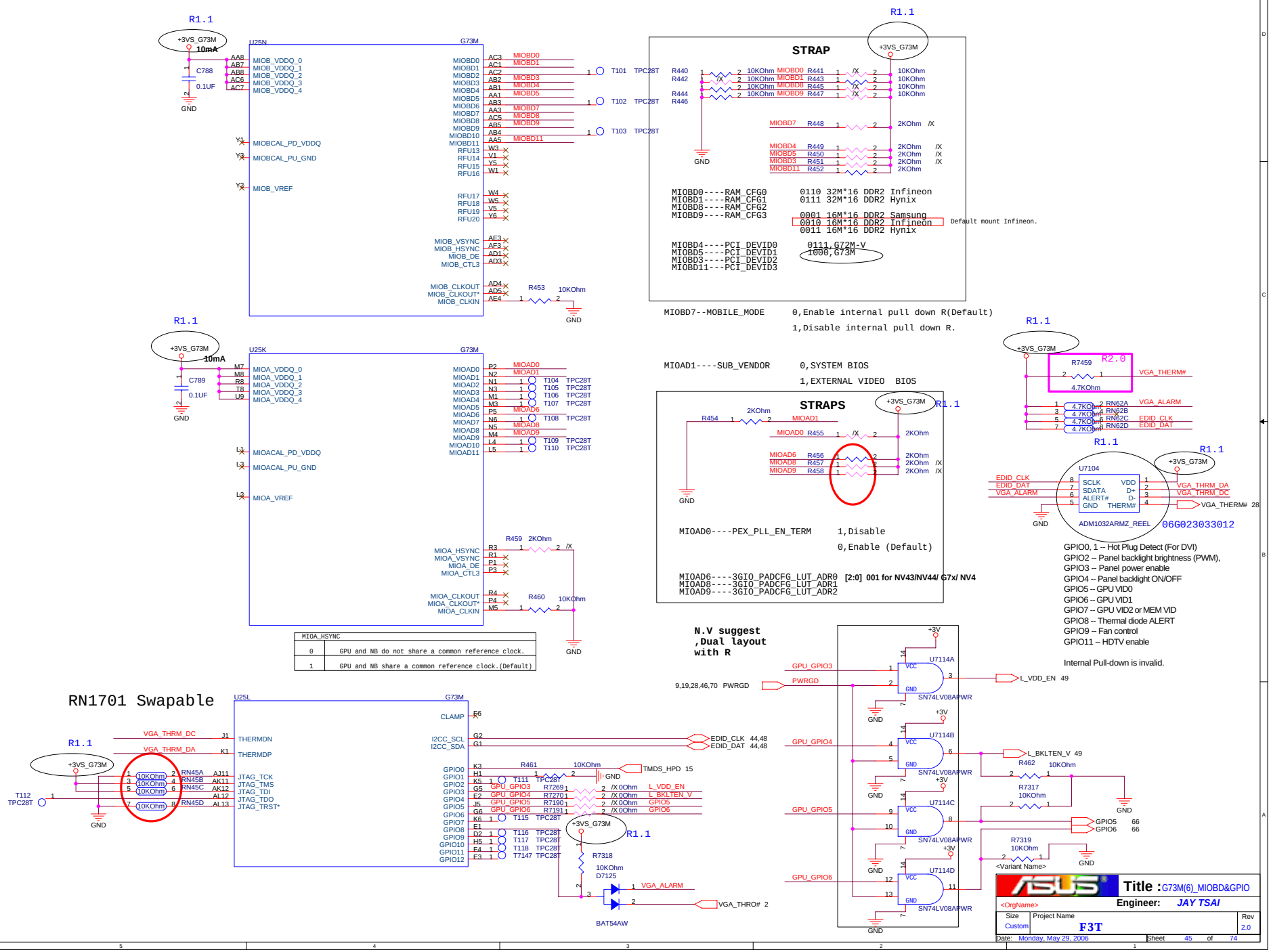
Title : G73M(4)-GND&Decoupling

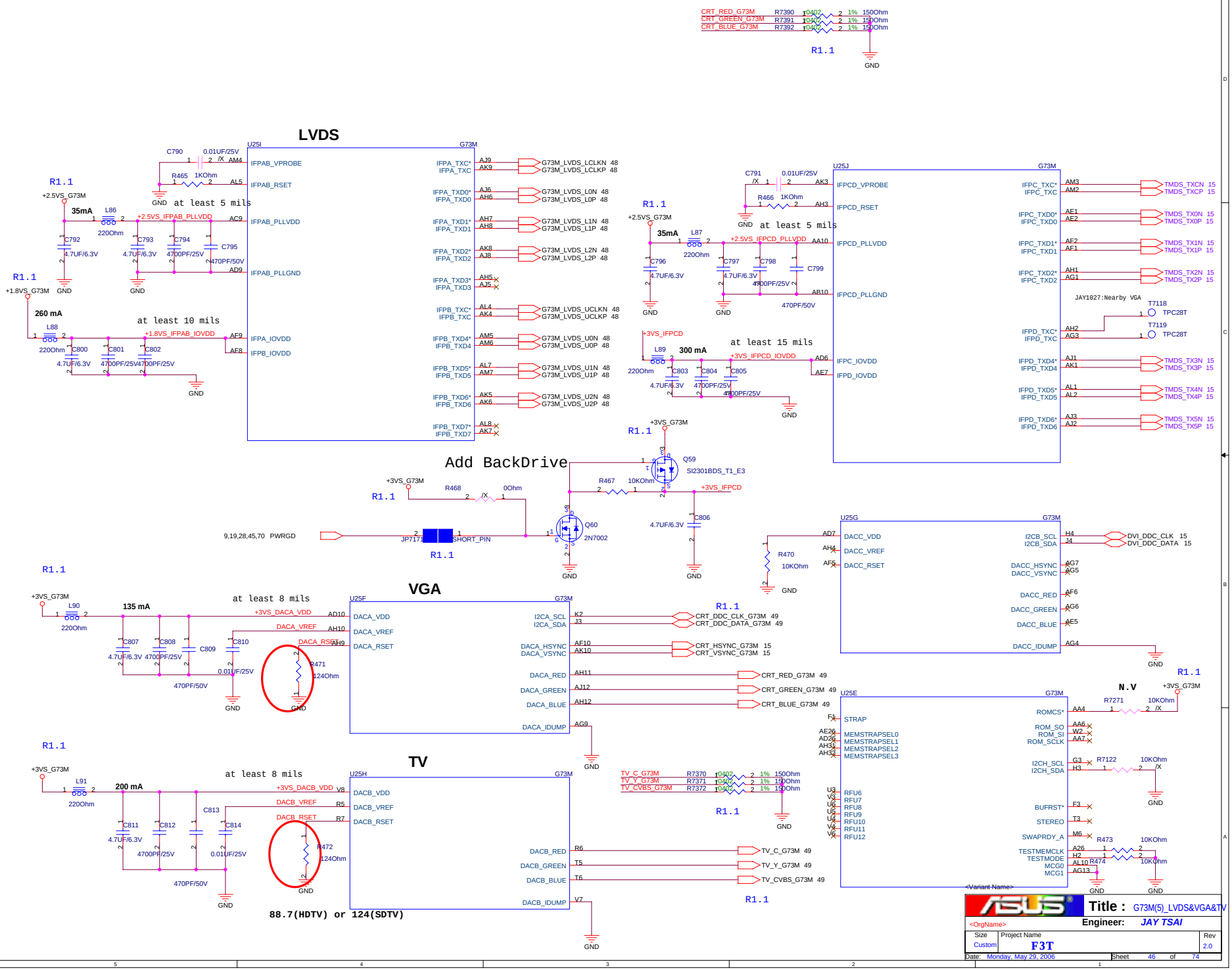
<OrgName>

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	F3T	2.0

Date: Monday, May 29, 2006 Sheet 44 of 74


R1.1
+3VS_G73M
10mA
C788
0.1UF
GND
U25N
G73M
MIOB_VDDQ_0
MIOB_VDDQ_1
MIOB_VDDQ_2
MIOB_VDDQ_3
MIOB_VDDQ_4
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_CLKOUT
MIOB_CLKOUT*
MIOB_CLKIN
R453
10KOhm
T101
T102
T103
TPC28T
STRAP
R440
R441
R442
R443
R444
R445
R446
R447
R448
R449
R450
R451
R452
2KOhm
MIOBD0----RAM_CFG0
MIOBD1----RAM_CFG1
MIOBD8----RAM_CFG2
MIOBD9----RAM_CFG3
0110 32M*16 DDR2 Infineon
0111 32M*16 DDR2 Hynix
0001 16M*16 DDR2 Samsung
0010 16M*16 DDR2 Infineon
0011 16M*16 DDR2 Hynix
Default mount Infineon.
MIOBD4----PCI_DEVID0
MIOBD5----PCI_DEVID1
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3
0111,G72M-V
1000,G73M
MIOBD7--MOBILE_MODE
0,Enable internal pull down R(Default)
1,Disable internal pull down R.
U25K
MIOA_VDDQ_0
MIOA_VDDQ_1
MIOA_VDDQ_2
MIOA_VDDQ_3
MIOA_VDDQ_4
MIOACAL_PD_VDDQ
MIOACAL_PU_GND
MIOA_VREF
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CTL3
MIOA_CLKOUT
MIOA_CLKOUT*
MIOA_CLKIN
R459
R460
2KOhm
T104
T105
T106
T107
T108
T109
T110
MIOAD1----SUB_VENDOR
0,SYSTEM BIOS
1,EXTERNAL VIDEO BIOS
STRAPS
R454
R455
R456
R457
R458
MIOAD0----PEX_PLL_EN_TERM
1,Disable
0,Enable (Default)
MIOAD6----3GIO_PADCFG_LUT_ADR0 [2:0] 001 for NV43/NV44/ G7x/ NV4
MIOAD8----3GIO_PADCFG_LUT_ADR1
MIOAD9----3GIO_PADCFG_LUT_ADR2
MIOA_HSYNC
0
GPU and NB do not share a common reference clock.
1
GPU and NB share a common reference clock.(Default)
R7459
R2.0
4.7KOhm
VGA_THERM#
VGA_ALARM
EDID_CLK
EDID_DAT
RN62A
RN62B
RN62C
RN62D
U7104
SCLK
SDATA
ALERT#
GND
VDD
D+
D-
THERM#
ADM1032ARMZ_REEL
06G023033012
VGA_THRM_DA
VGA_THRM_DC
VGA_THERM# 28
GPIO0, 1 -- Hot Plug Detect (For DVI)
GPIO2 -- Panel backlight brightness (PWM),
GPIO3 -- Panel power enable
GPIO4 -- Panel backlight ON/OFF
GPIO5 -- GPU VID0
GPIO6 -- GPU VID1
GPIO7 -- GPU VID2 or MEM VID
GPIO8 -- Thermal diode ALERT
GPIO9 -- Fan control
GPIO11 -- HDTV enable
Internal Pull-down is invalid.
N.V suggest ,Dual layout with R
RN1701 Swapable
U25L
G73M
CLAMP
THERMDN
THERMDP
VGA_THRM_DC
VGA_THRM_DA
I2CC_SCL
I2CC_SDA
EDID_CLK 44,48
EDID_DAT 44,48
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*
RN45A
RN45B
RN45C
RN45D
10KOhm
T112
TPC28T
R461
TMDS_HPD 15
GPU_GPIO3
GPU_GPIO4
GPU_GPIO5
GPU_GPIO6
R7269
R7270
R7190
R7191
/X 0Ohm
L_VDD_EN
L_BKLTEN_V
GPIO5
GPIO6
R7318
D7125
BAT54AW
VGA_ALARM
VGA_THRO# 2
9,19,28,46,70 PWRGD
PWRGD
U7114A
U7114B
U7114C
U7114D
SN74LV08APWR
L_VDD_EN 49
L_BKLTEN_V 49
R462
R7317
R7319
<Variant Name>
GPIO5 66
GPIO6 66
Title : G73M(6)_MIOBD&GPIO
<OrgName>
Engineer: JAY TSAI
Size
Custom
Project Name
F3T
Rev
2.0
Date: Monday, May 29, 2006
Sheet 45 of 74

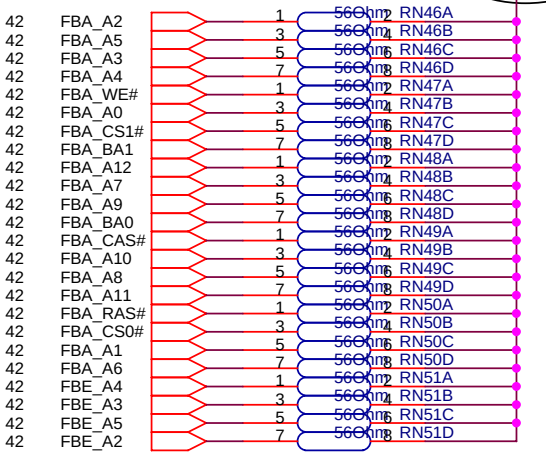

CRT_RED_G73M R7390 0402 2 1% 150Ohm
CRT_GREEN_G73M R7391 0402 2 1% 150Ohm
CRT_BLUE_G73M R7392 0402 2 1% 150Ohm
R1.1
GND
LVDS
U25I
G73M
C790 0.01UF/25V /X
R465 1KOhm
GND at least 5 mils
IFPAB_VPROBE
IFPAB_RSET
IFPAB_PLLVDD
IFPAB_PLLGND
+2.5VS_G73M
35mA
L86
220Ohm
+2.5VS_IFPAB_PLLVDD
C792 4.7UF/6.3V
C793 4.7UF/6.3V
C794 4700PF/25V
C795 470PF/50V
+1.8VS_G73M
260 mA
L88
220Ohm
C800 4.7UF/6.3V
C801 4700PF/25V
C802 4700PF/25V
at least 10 mils
+1.8VS_IFPAB_IOVDD
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXC* IFPA_TXC
IFPA_TXD0* IFPA_TXD0
IFPA_TXD1* IFPA_TXD1
IFPA_TXD2* IFPA_TXD2
IFPA_TXD3* IFPA_TXD3
IFPB_TXC* IFPB_TXC
IFPB_TXD4* IFPB_TXD4
IFPB_TXD5* IFPB_TXD5
IFPB_TXD6* IFPB_TXD6
IFPB_TXD7* IFPB_TXD7
G73M_LVDS_LCLKN 48
G73M_LVDS_LCLKP 48
G73M_LVDS_L0N 48
G73M_LVDS_L0P 48
G73M_LVDS_L1N 48
G73M_LVDS_L1P 48
G73M_LVDS_L2N 48
G73M_LVDS_L2P 48
G73M_LVDS_UCLKN 48
G73M_LVDS_UCLKP 48
G73M_LVDS_U0N 48
G73M_LVDS_U0P 48
G73M_LVDS_U1N 48
G73M_LVDS_U1P 48
G73M_LVDS_U2N 48
G73M_LVDS_U2P 48
U25J
C791 0.01UF/25V /X
R466 1KOhm
GND at least 5 mils
IFPCD_VPROBE
IFPCD_RSET
IFPCD_PLLVDD
IFPCD_PLLGND
+2.5VS_G73M
35mA
L87
220Ohm
+2.5VS_IFPCD_PLLVDD
C796 4.7UF/6.3V
C797 4.7UF/6.3V
C798 4700PF/25V
C799 470PF/50V
+3VS_IFPCD
300 mA
L89
220Ohm
C803 4.7UF/6.3V
C804 4700PF/25V
C805 4700PF/25V
at least 15 mils
+3VS_IFPCD_IOVDD
IFPC_IOVDD
IFPD_IOVDD
IFPC_TXC* IFPC_TXC
IFPC_TXD0* IFPC_TXD0
IFPC_TXD1* IFPC_TXD1
IFPC_TXD2* IFPC_TXD2
IFPD_TXC* IFPD_TXC
IFPD_TXD4* IFPD_TXD4
IFPD_TXD5* IFPD_TXD5
IFPD_TXD6* IFPD_TXD6
TMDS_TXCN 15
TMDS_TXCP 15
TMDS_TX0N 15
TMDS_TX0P 15
TMDS_TX1N 15
TMDS_TX1P 15
TMDS_TX2N 15
TMDS_TX2P 15
TMDS_TX3N 15
TMDS_TX3P 15
TMDS_TX4N 15
TMDS_TX4P 15
TMDS_TX5N 15
TMDS_TX5P 15
JAY1027:Nearby VGA
T7118 TPC28T
T7119 TPC28T
Add BackDrive
+3VS_G73M
R468 0Ohm /X
9,19,28,45,70 PWRGD
JP7173 SHORT_PIN
Q60 2N7002
R467 10KOhm
Q59 SI2301BDS_T1_E3
+3VS_IFPCD
C806 4.7UF/6.3V
U25G
DACC_VDD
DACC_VREF
DACC_RSET
R470 10KOhm
I2CB_SCL
I2CB_SDA
DACC_HSYNC
DACC_VSYNC
DACC_RED
DACC_GREEN
DACC_BLUE
DACC_IDUMP
DVI_DDC_CLK 15
DVI_DDC_DATA 15
VGA
U25F
+3VS_G73M
L90 220Ohm
135 mA
at least 8 mils
+3VS_DACA_VDD
DACA_VREF
DACA_RSET
C807 4.7UF/6.3V
C808 4700PF/25V
C809 470PF/50V
C810 0.01UF/25V
R471 124Ohm
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
CRT_DDC_CLK_G73M 49
CRT_DDC_DATA_G73M 49
CRT_HSYNC_G73M 15
CRT_VSYNC_G73M 15
CRT_RED_G73M 49
CRT_GREEN_G73M 49
CRT_BLUE_G73M 49
TV
U25H
+3VS_G73M
L91 220Ohm
200 mA
at least 8 mils
+3VS_DACB_VDD
DACB_VREF
DACB_RSET
C811 4.7UF/6.3V
C812 4700PF/25V
C813 470PF/50V
C814 0.01UF/25V
R472 124Ohm
DACB_VDD
DACB_VREF
DACB_RSET
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
TV_C_G73M 49
TV_Y_G73M 49
TV_CVBS_G73M 49
88.7(HDTV) or 124(SDTV)
U25E
STRAP
MEMSTRAPSEL0
MEMSTRAPSEL1
MEMSTRAPSEL2
MEMSTRAPSEL3
RFU6
RFU7
RFU8
RFU9
RFU10
RFU11
RFU12
ROMCS*
ROM_SO
ROM_SI
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*
STEREO
SWAPRDY_A
TESTMEMCLK
TESTMODE
MCG0
MCG1
N.V
R7271 10KOhm /X
R7122 10KOhm /X
R473 10KOhm
R474 10KOhm
<Variant Name>
Title : G73M(5)_LVDS&VGA&TV
<OrgName>
Engineer: JAY TSAI
Size Custom
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 46 of 74

R1.1

SWAPABLE

+0.9VS_G73M

FBA CMD/ADDR Termination

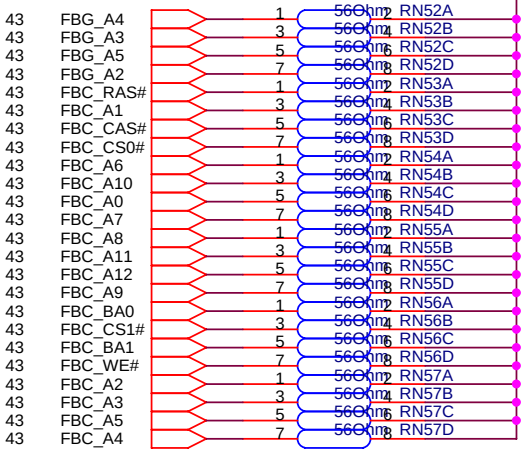


+0.9VS_G73M

R1.1

SWAPABLE

FBC CMD/ADDR Termination



<Variant Name>

<OrgName>	Title : G73M-Termination	
	Engineer: JAY TSAI	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 47 of 74	

R2.0 SLI

12 NB_IFPA_TXC_P
12 NB_IFPA_TXC_N
12 NB_IFPA_TXD0_P
12 NB_IFPA_TXD0_N
12 NB_IFPA_TXD1_P
12 NB_IFPA_TXD1_N
12 NB_IFPA_TXD2_P
12 NB_IFPA_TXD2_N
12 NB_IFPB_TXC_P
12 NB_IFPB_TXC_N
12 NB_IFPB_TXD4_P
12 NB_IFPB_TXD4_N
12 NB_IFPB_TXD5_P
12 NB_IFPB_TXD5_N
12 NB_IFPB_TXD6_P
12 NB_IFPB_TXD6_N

U7116 /X
U7117 /X
U7118 /X
U7119 /X
STMAV340
S=0 B
S=1 C
+5VS
GND

LVDS_LCLKP 14
LVDS_LCLKN 14
LVDS_L0P 14
LVDS_L0N 14
LVDS_L1P 14
LVDS_L1N 14
LVDS_L2P 14
LVDS_L2N 14
LVDS_UCLKP 14
LVDS_UCLKN 14
LVDS_U0P 14
LVDS_U0N 14
LVDS_U1P 14
LVDS_U1N 14
LVDS_U2P 14
LVDS_U2N 14

JP7183 SHORT_PIN
JP7184 SHORT_PIN
R7415 0Ohm /X
R7308 10KOhm r0402 /X
R1.1
Johnny R1.1
EN_DISP# 17,49
SEL_LVDS_C51/G73M_R

15,49 SEL_LVDS_G73M/C51_R
R7307 10KOhm r0402 /X
Q7151A UM6K1N /X
R7330 10KOhm r0402 /X
Q7151B UM6K1N /X
SEL_LVDS_C51/G73M_R3 15,49
+3VS
R7331 10KOhm r0402 /X
R7332 10KOhm r0402 /X
44,45 EDID_CLK
44,45 EDID_DAT
Q7152B UM6K1N
Q7152A UM6K1N
R7480 0Ohm
R7481 0Ohm
LCD_EDID_CLK 14
LCD_EDID_DAT 14
19 MCP51_EDID_CLK
19 MCP51_EDID_DATA
Q7153B UM6K1N /X
Q7153A UM6K1N /X

G73M_LVDS_LCLKP
G73M_LVDS_LCLKN
G73M_LVDS_L0P
G73M_LVDS_L0N
G73M_LVDS_L2N
G73M_LVDS_L2P
G73M_LVDS_L1N
G73M_LVDS_L1P
G73M_LVDS_UCLKP
G73M_LVDS_UCLKN
G73M_LVDS_U0P
G73M_LVDS_U0N
G73M_LVDS_U1P
G73M_LVDS_U1N
G73M_LVDS_U2P
G73M_LVDS_U2N
0Ohm
RN83A LVDS_LCLKP
RN83B LVDS_LCLKN
RN83C LVDS_L0P
RN83D LVDS_L0N
RN84A LVDS_L2N
RN84B LVDS_L2P
RN84C LVDS_L1N
RN84D LVDS_L1P
RN85A LVDS_UCLKP
RN85B LVDS_UCLKN
RN85C LVDS_U0P
RN85D LVDS_U0N
RN86A LVDS_U1P
RN86B LVDS_U1N
RN86C LVDS_U2P
RN86D LVDS_U2N
R1.1
SWAP

19 SEL_LVDS_C51/G73M
SEL_LVDS_C51/G73M
R7359 0Ohm /X
SEL_LVDS_C51/G73M_R
SEL_LVDS_C51/G73M_R 49

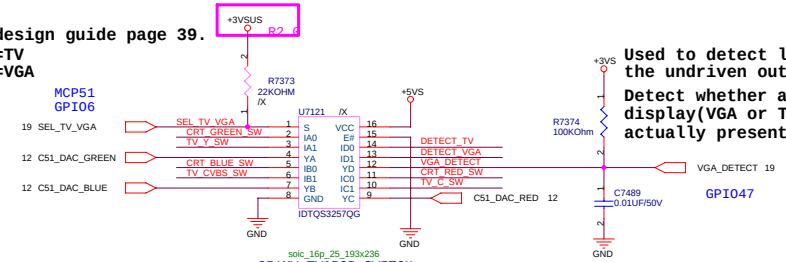
<Variant Name>
Title : LVDS SWITCH
<OrgName>
Engineer: JAY TSAI
Size B
Project Name F3T
Rev 2.0
Date: Monday, May 29, 2006
Sheet 48 of 74

Nvidia design guide page 39.
"1" =TV
"0" =VGA

MCP51
GPIO6

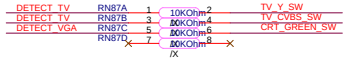
Used to detect load on the undriven output.

Detect whether a display(VGA or TV) is actually present.

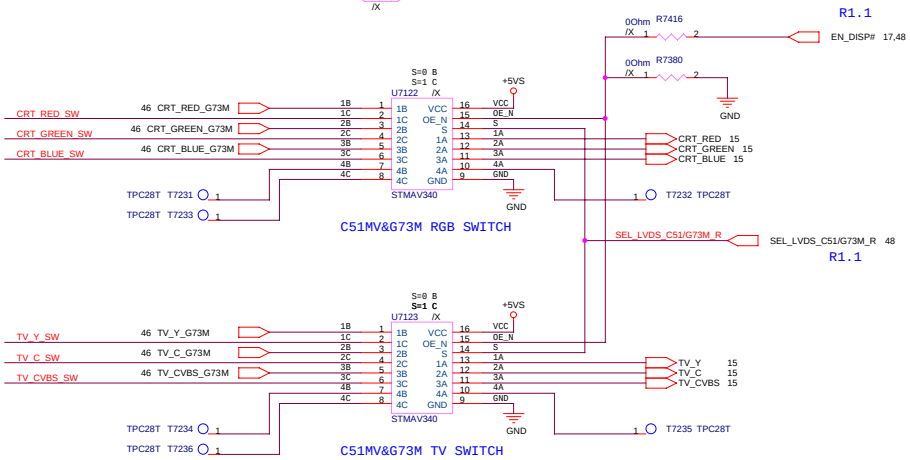


BY Pass CRT

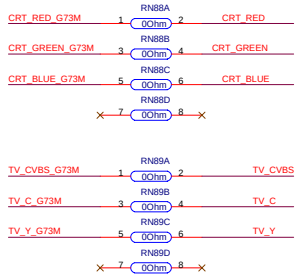
To support monochrome VGA display monitor detection.



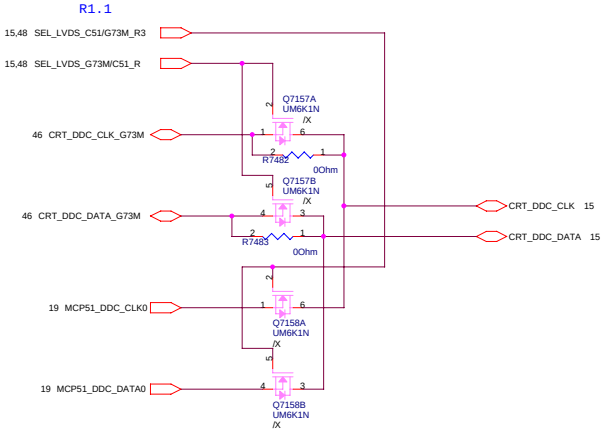
R1.1



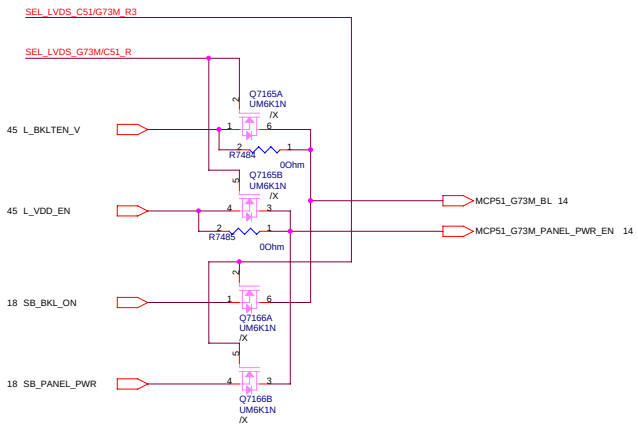
R1.1



R1.1



R1.1



ASUS

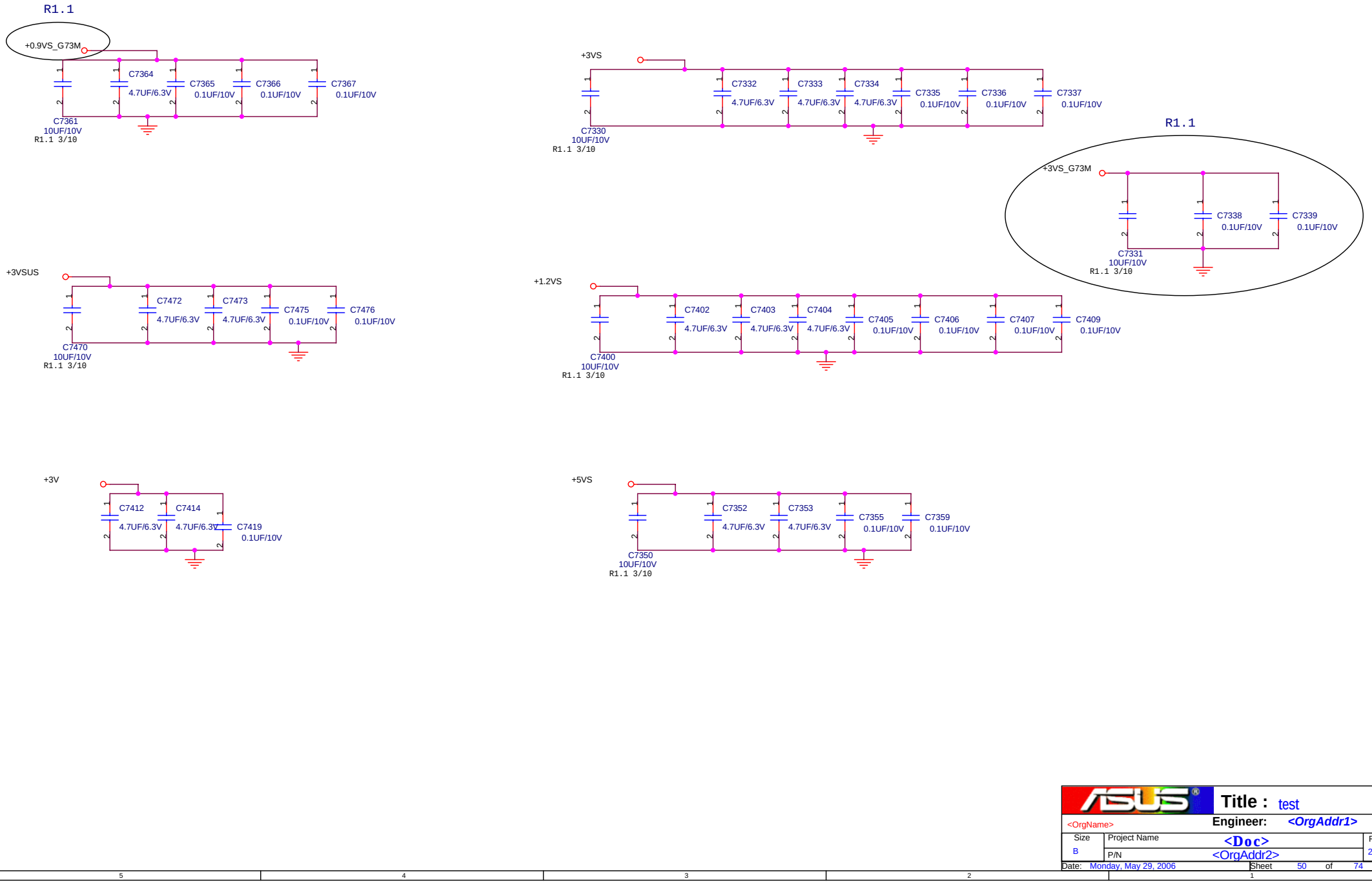
Title : TV&CRT&BACKLIGHT&LCD PWR switch

<OrgName>

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	<Doc>	2.0
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 49 of 74



<OrgName>	Engineer: <OrgAddr1>	
Size: B	Project Name: <Doc>	Rev: 2.0
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 50 of 74	

Title : test

R2.0

Delete Test Parts

ASUS	Title : test		
<OrgName>	Engineer: <OrgAddr1>		
Size: A	Project Name: <Doc>		Rev: 2.0
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006		Sheet 51 of 74	

ASUS	Title : test		
<OrgName>	Engineer: <OrgAddr1>		
Size A	Project Name <Doc>		Rev 1
	P/N <OrgAddr2>		
Date: Monday, May 29, 2006		Sheet 52 of 74	

Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 53 of 74

Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 54 of 74

Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 55 of 74

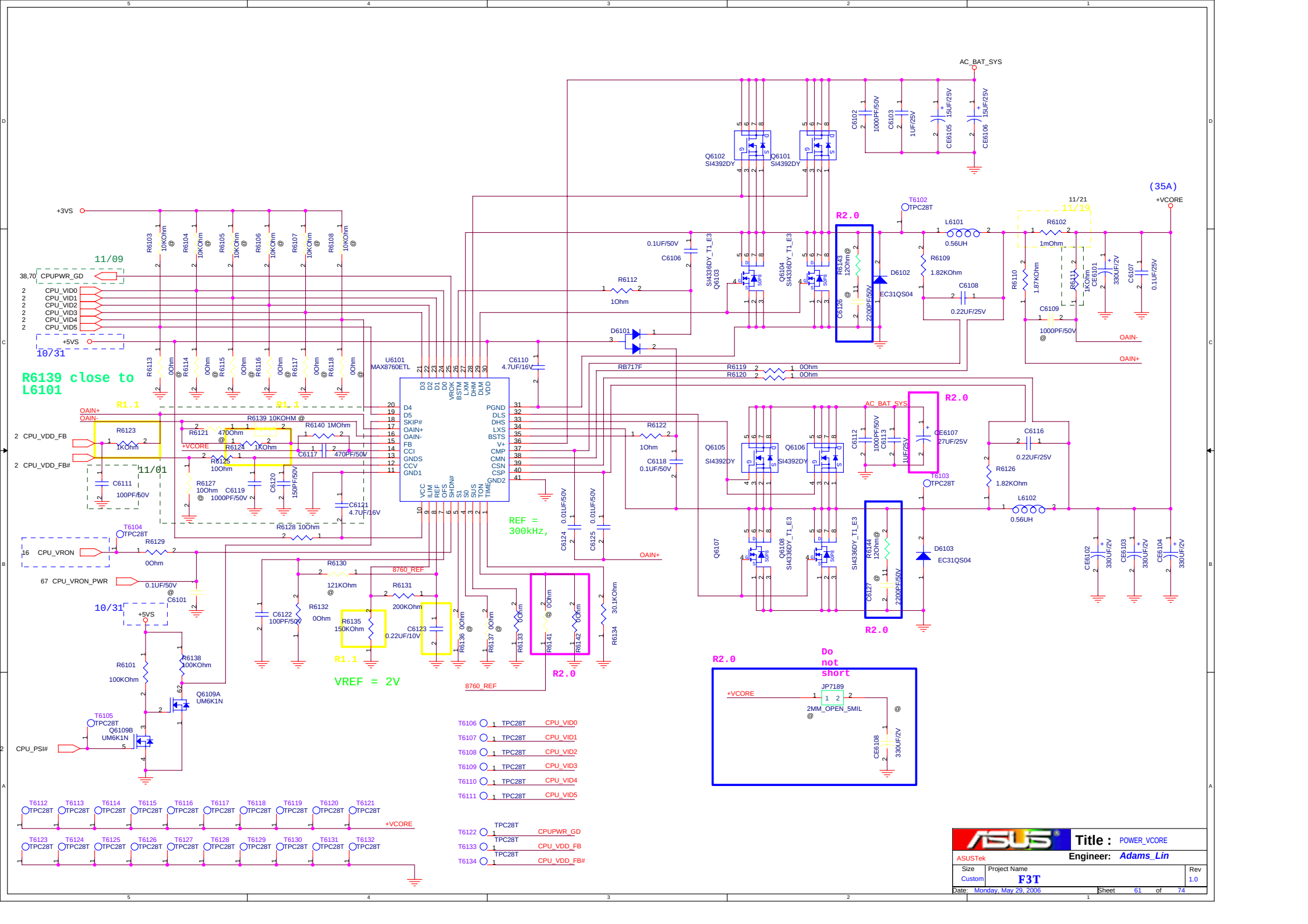
Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 56 of 74

Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 57 of 74

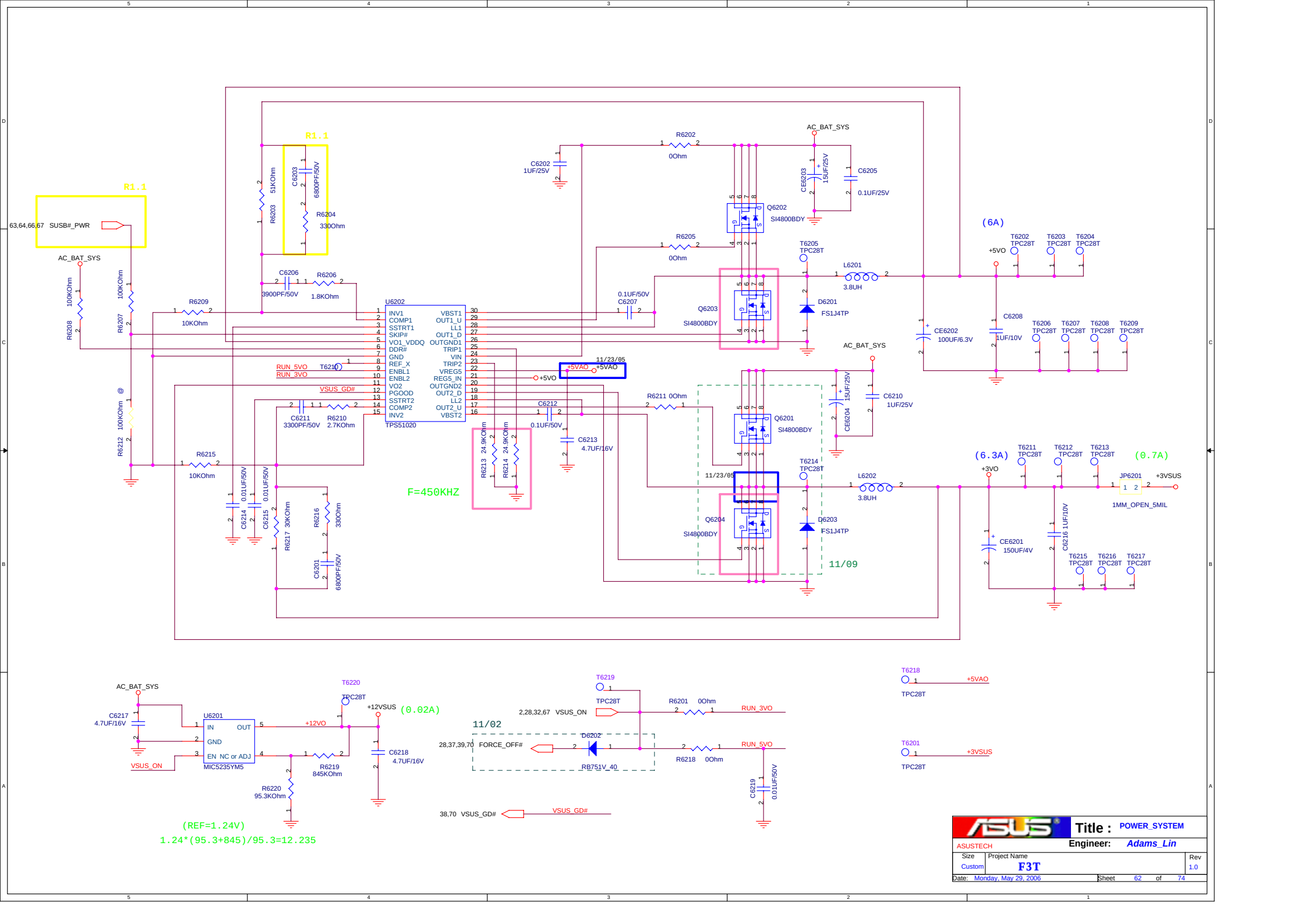
Title :	test	
<OrgName>	Engineer:	*<OrgAddr1>*
Size: A	Project Name: **<Doc>**	Rev: 1
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 58 of 74	

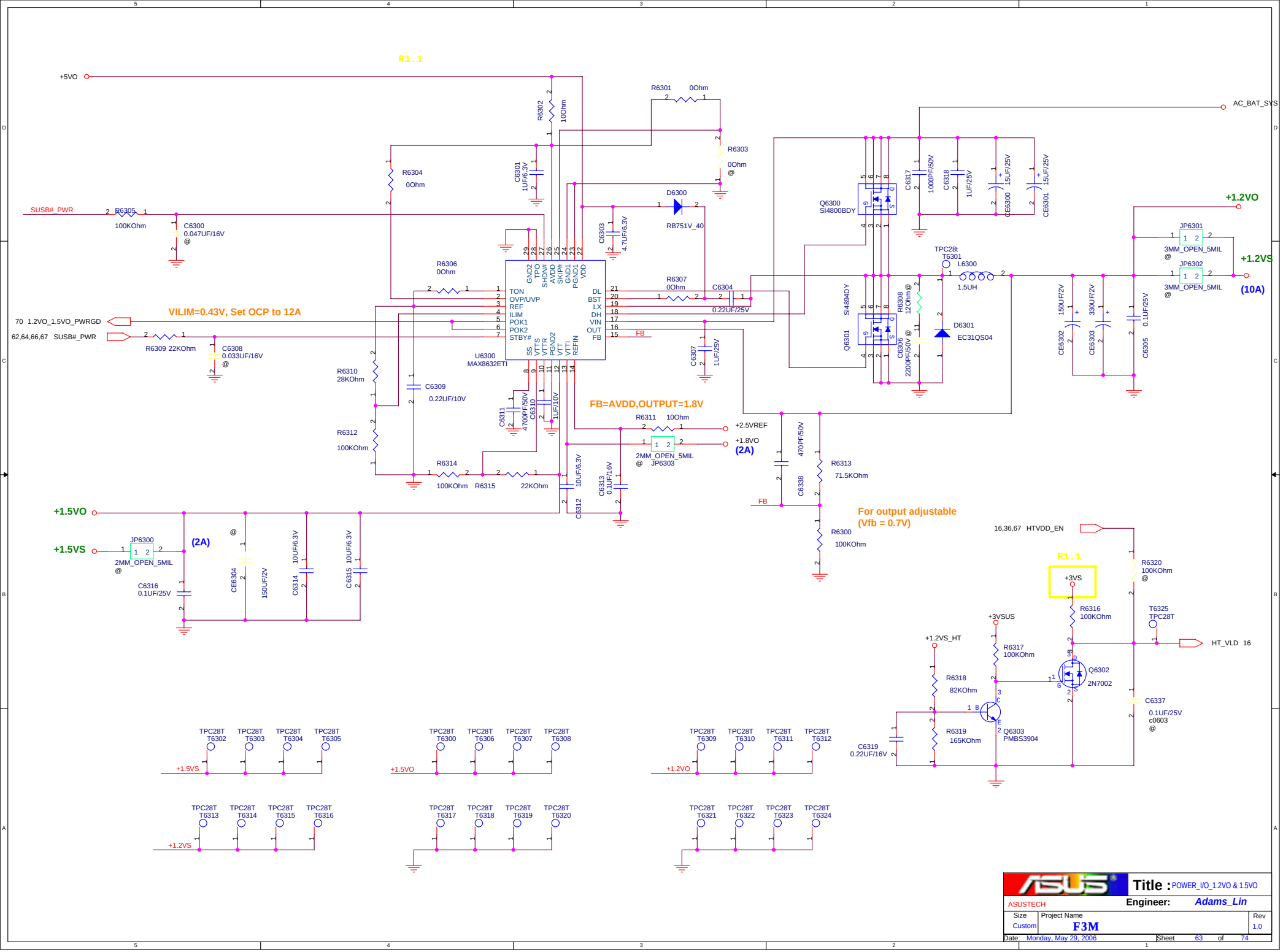
Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 59 of 74

Title :	test
<OrgName>	Engineer: *<OrgAddr1>*
Size: A	Project Name: **<Doc>**
	P/N: <OrgAddr2>
	Rev: 1
Date: Monday, May 29, 2006	Sheet 60 of 74

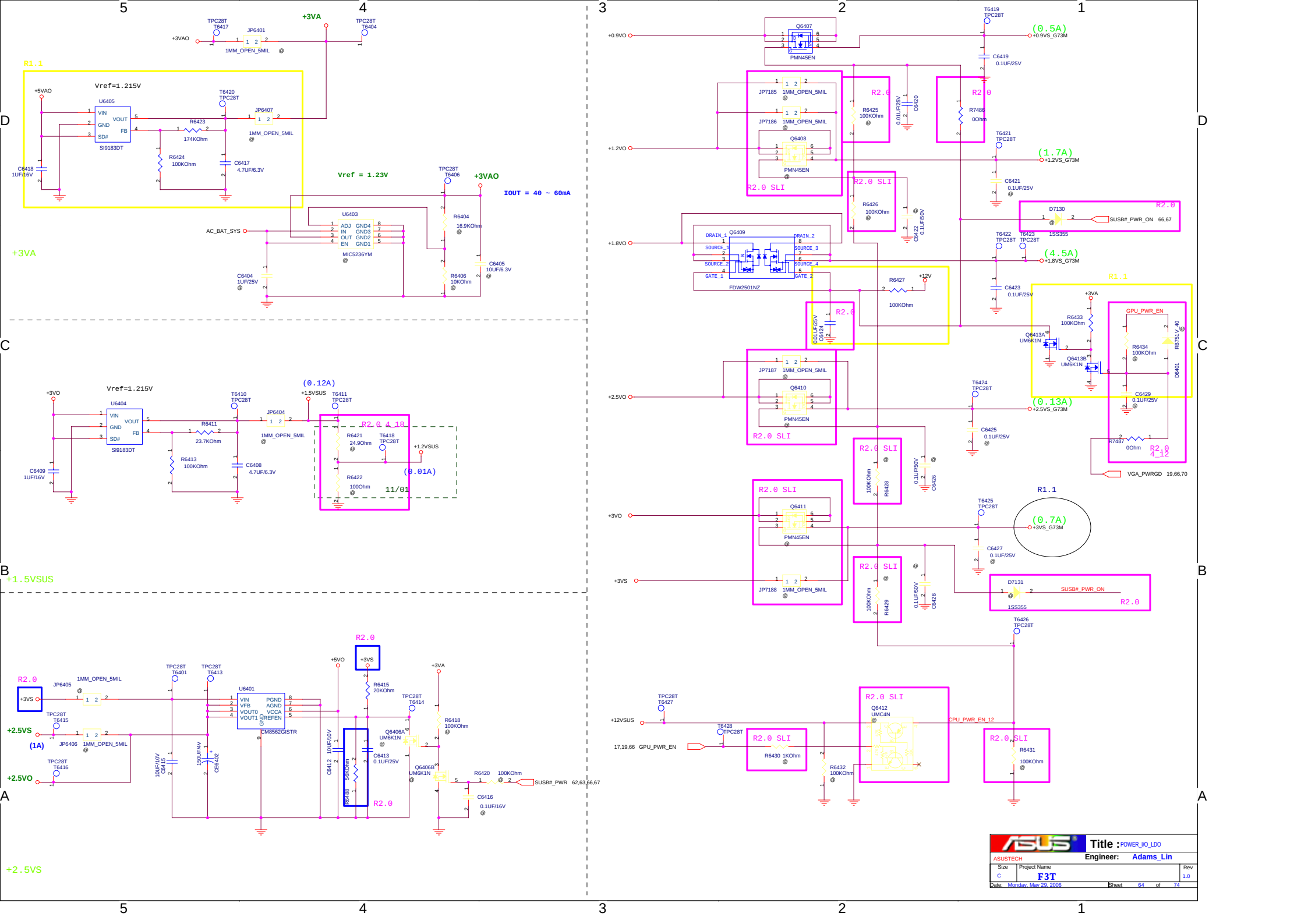


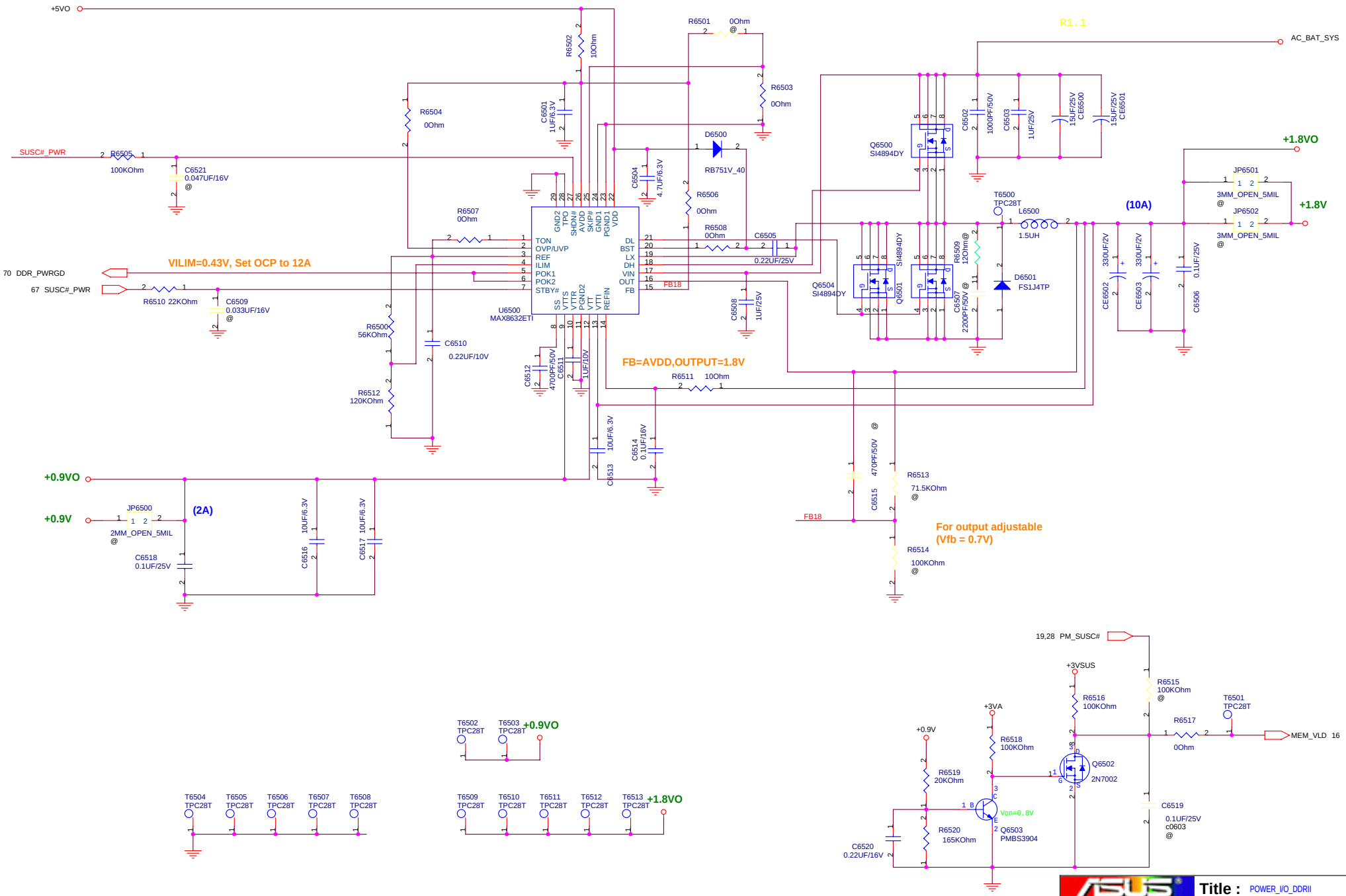
Title :	POWER_VCORE
ASUSTek	Engineer: Adams_Lin
Size: Custom	Project Name: F3T
Rev: 1.0	
Date: Monday, May 29, 2006	Sheet 61 of 74


R1.1
63,64,66,67 SUSB#_PWR
AC_BAT_SYS
R6208 100KOhm
R6207 100KOhm
R6212 100KOhm @
R6209 10KOhm
R6215 10KOhm
R6203 51KOhm
C6203 680PF/50V
R6204 330Ohm
C6206 3900PF/50V
R6206 1.8KOhm
C6211 3300PF/50V
R6210 2.7KOhm
C6214 0.01UF/50V
C6215 0.01UF/50V
R6217 30KOhm
R6216 330Ohm
C6201 6800PF/50V
U6202
TPS51020
INV1 COMP1 SSTRT1 SKIP# VO1_VDDQ DDR# GND REF_X ENBL1 ENBL2 VO2 PGOOD SSTRT2 COMP2 INV2
VBST1 OUT1_U LL1 OUT1_D OUTGND1 TRIP1 VIN TRIP2 VREG5 REG5_IN OUTGND2 OUT2_D LL2 OUT2_U VBST2
RUN_5VO
RUN_3VO
T6210
VSUS_GD#
+5VO
+5VAO
11/23/05
C6212 0.1UF/50V
C6213 4.7UF/16V
R6213 24.9KOhm
R6214 24.9KOhm
F=450KHZ
R6202 0Ohm
C6202 1UF/25V
R6205 0Ohm
C6207 0.1UF/50V
R6211 0Ohm
Q6202 SI4800BDY
Q6203 SI4800BDY
Q6201 SI4800BDY
Q6204 SI4800BDY
CE6203 15UF/25V
C6205 0.1UF/25V
CE6204 15UF/25V
C6210 1UF/25V
D6201 FS1J4TP
D6203 FS1J4TP
L6201 3.8UH
L6202 3.8UH
CE6202 100UF/6.3V
C6208 1UF/10V
CE6201 150UF/4V
C6216 1UF/10V
(6A)
(6.3A)
(0.7A)
T6202 T6203 T6204 T6205 T6206 T6207 T6208 T6209 T6211 T6212 T6213 T6214 T6215 T6216 T6217 TPC28T
JP6201 1MM_OPEN_5MIL
+3VO
+3VSUS
11/09
U6201
MIC5235YM5
IN OUT GND EN NC or ADJ
C6217 4.7UF/16V
VSUS_ON
T6220
+12VSUS
+12VO
(0.02A)
R6219 845KOhm
R6220 95.3KOhm
C6218 4.7UF/16V
(REF=1.24V)
1.24*(95.3+845)/95.3=12.235
T6219
2,28,32,67 VSUS_ON
11/02
28,37,39,70 FORCE_OFF#
D6202 RB751V_40
R6201 0Ohm
R6218 0Ohm
C6219 0.01UF/50V
38,70 VSUS_GD#
T6218
T6201
Title : POWER_SYSTEM
ASUSTECH
Engineer: Adams_Lin
Size Custom
Project Name F3T
Rev 1.0
Date: Monday, May 29, 2006
Sheet 62 of 74

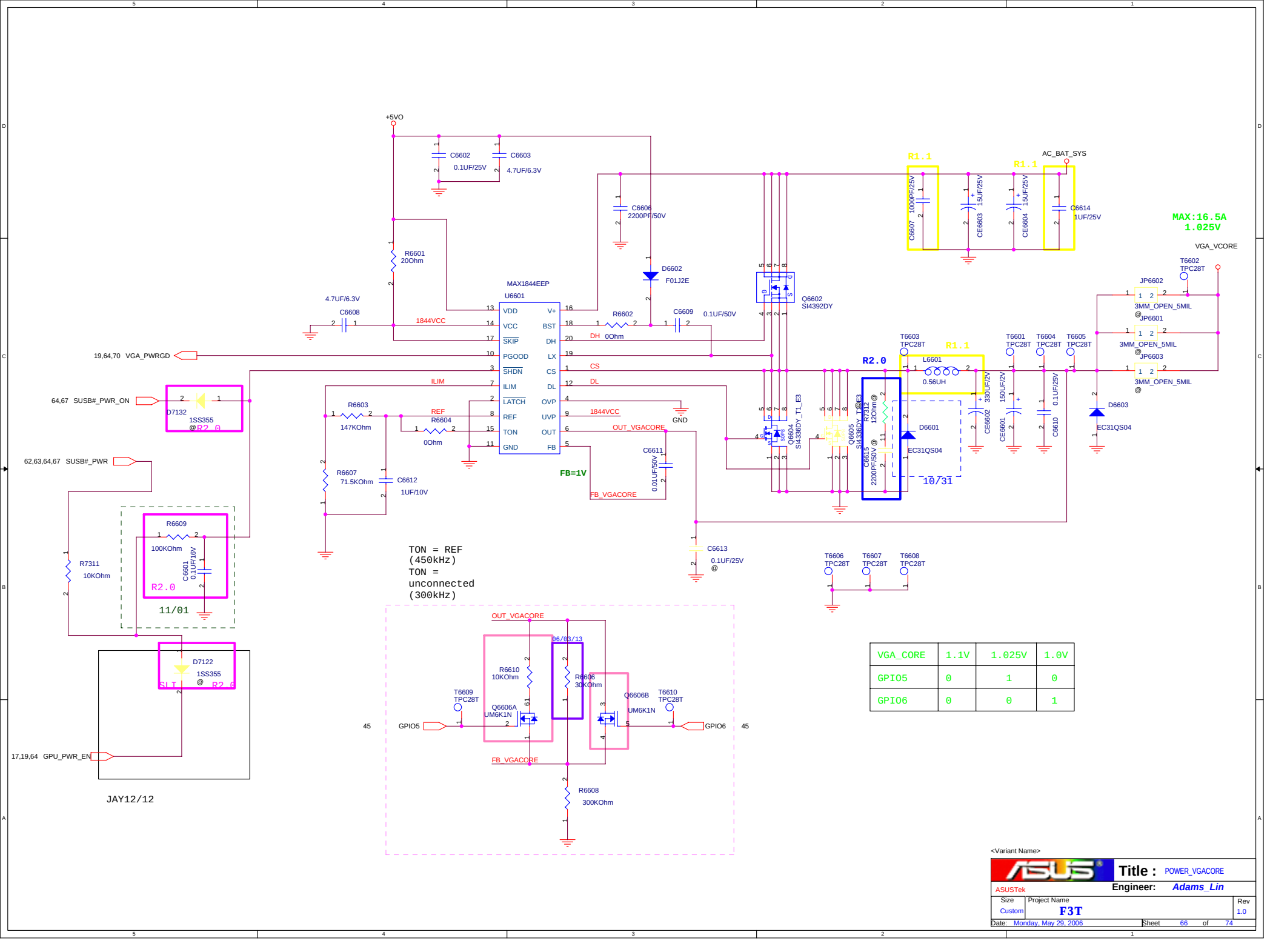


ASUSTECH	Title : POWER_I/O_1.2VO & 1.5VO	
	Engineer: Adams_Lin	
Size: Custom	Project Name: F3M	Rev: 1.0
Date: Monday, May 29, 2006	Sheet 63 of 74	


+3VA
R1.1
Vref=1.215V
+5VAO
U6405
VIN
VOUT
GND
FB
SD#
SI9183DT
R6423
174KOhm
R6424
100KOhm
C6417
4.7UF/6.3V
C6418
1UF/16V
JP6401
1MM_OPEN_5MIL
TPC28T T6417
TPC28T T6404
TPC28T T6420
JP6407
Vref = 1.23V
+3VAO
IOUT = 40 ~ 60mA
U6403
ADJ GND4
IN GND3
OUT GND2
EN GND1
MIC5236YM
AC_BAT_SYS
R6404
16.9KOhm
R6406
10KOhm
C6405
10UF/6.3V
C6404
1UF/25V
TPC28T T6406
+3VO
Vref=1.215V
U6404
SI9183DT
R6411
23.7KOhm
R6413
100KOhm
C6408
4.7UF/6.3V
C6409
1UF/16V
JP6404
TPC28T T6410
TPC28T T6411
+1.5VSUS
(0.12A)
R2.0 4_18
R6421
24.9Ohm
R6422
100Ohm
TPC28T T6418
+1.2VSUS
(0.01A)
11/01
+1.5VSUS
R2.0
+5VO
+3VS
+3VA
R6415
20KOhm
R6418
100KOhm
U6401
VIN PGND
VFB AGND
VOUT0 VCCA
VOUT1 VREFEN
CM8562GISTR
JP6405
JP6406
TPC28T T6401
TPC28T T6413
TPC28T T6414
TPC28T T6415
TPC28T T6416
+2.5VS
(1A)
+2.5VO
10UF/10V C6415
150UF/4V CE6402
10UF/10V C6412
5.6KOhm R6488
C6413
0.1UF/25V
Q6406A UM6K1N
Q6406B UM6K1N
R6420
100KOhm
SUSB#_PWR 62,63,66,67
C6416
0.1UF/16V
+2.5VS
+0.9VO
Q6407
PMN45EN
JP7185
JP7186
R6425
100KOhm
C6420
0.01UF/25V
R7486
0Ohm
T6419 TPC28T
(0.5A)
+0.9VS_G73M
C6419
0.1UF/25V
+1.2VO
Q6408
PMN45EN
R2.0 SLI
R6426
100KOhm
C6422
0.1UF/50V
T6421 TPC28T
(1.7A)
+1.2VS_G73M
C6421
0.1UF/25V
D7130
1SS355
SUSB#_PWR_ON 66,67
+1.8VO
Q6409
FDW2501NZ
DRAIN_1
DRAIN_2
SOURCE_1
SOURCE_2
SOURCE_3
SOURCE_4
GATE_1
GATE_2
R6427
100KOhm
+12V
T6422 TPC28T
T6423 TPC28T
(4.5A)
+1.8VS_G73M
C6423
0.1UF/25V
C6424
0.01UF/25V
R1.1
R6433
100KOhm
Q6413A UM6K1N
Q6413B UM6K1N
GPU_PWR_EN
R6434
100KOhm
RB751V-40
D6401
C6429
0.1UF/25V
R7487
0Ohm
R2.0 4_12
VGA_PWRGD 19,66,70
+2.5VO
Q6410
PMN45EN
JP7187
T6424 TPC28T
(0.13A)
+2.5VS_G73M
C6425
0.1UF/25V
R6428
100KOhm
C6426
0.1UF/50V
+3VO
Q6411
PMN45EN
JP7188
R6429
100KOhm
C6428
0.1UF/50V
T6425 TPC28T
(0.7A)
+3VS_G73M
C6427
0.1UF/25V
D7131
1SS355
SUSB#_PWR_ON
T6426 TPC28T
+12VSUS
T6427 TPC28T
T6428 TPC28T
17,19,66 GPU_PWR_EN
R6430 1KOhm
R6432
100KOhm
Q6412 UMC4N
CPU_PWR_EN_12
R6431
100KOhm
ASUSTECH
Title : POWER_I/O_LDO
Engineer: Adams_Lin
Size C
Project Name F3T
Rev 1.0
Date: Monday, May 29, 2006
Sheet 64 of 74



ASUSTECH	Title : POWER_I/O_DDRII	
	Engineer: Adams_Lin	
Size: Custom	Project Name: F3M	Rev: 1.1
Date: Monday, May 29, 2006	Sheet 65 of 74	



VGA_CORE	1.1V	1.025V	1.0V
GPIO5	0	1	0
GPIO6	0	0	1

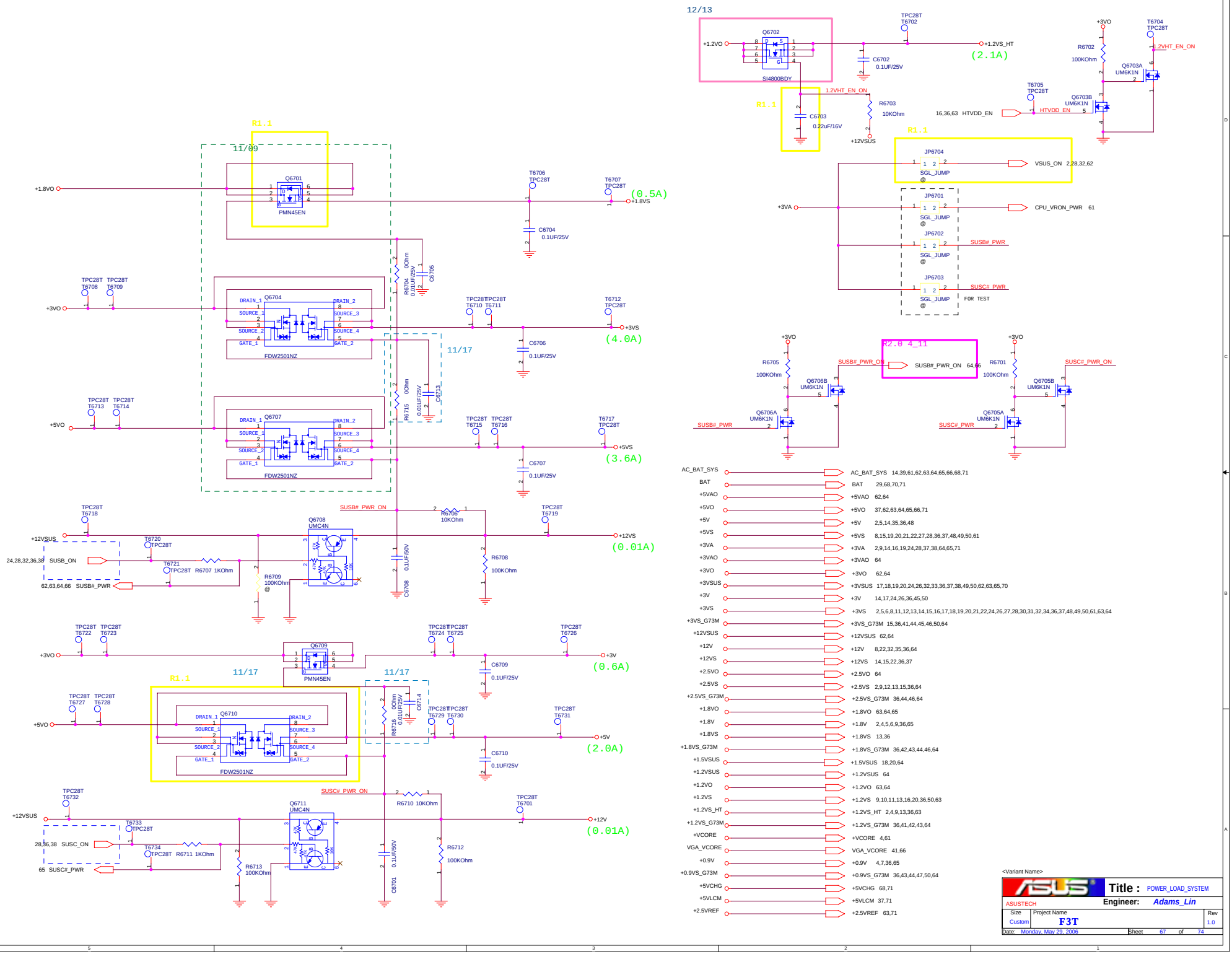
<Variant Name>

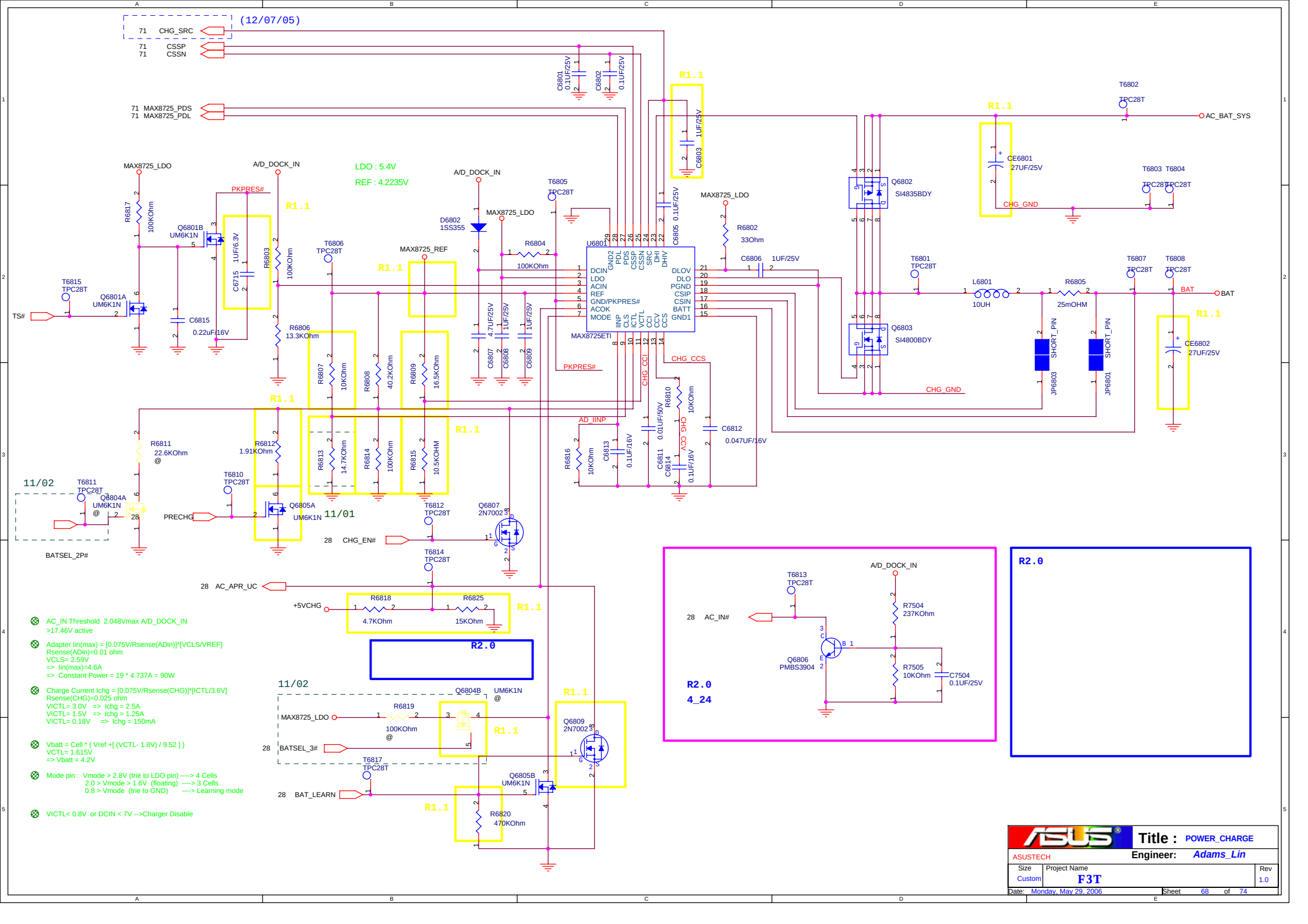
Title : POWER_VGACORE

ASUSTek Engineer: Adams_Lin

Size	Project Name	Rev
Custom	F3T	1.0

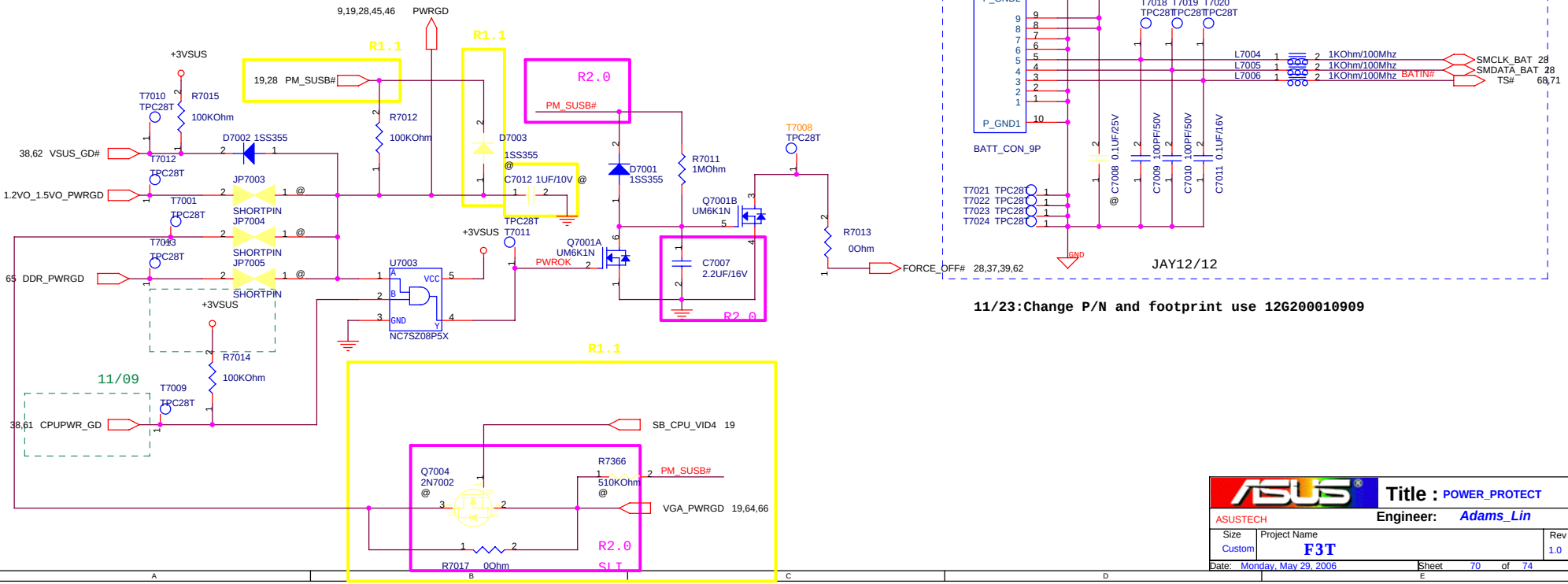
Date: Monday, May 29, 2006 Sheet 66 of 74


12/13
Q6702
SI4800BDY
+1.2VO
+1.2VS_HT
(2.1A)
C6702
0.1UF/25V
TPC28T T6702
1.2VHT_EN_ON
R6703
10KOhm
C6703
0.22uF/16V
+12VSUS
R1.1
+3VO
R6702
100KOhm
Q6703A
UM6K1N
T6704
TPC28T
T6705
TPC28T
Q6703B
UM6K1N
HTVDD_EN
16,36,63 HTVDD_EN
JP6704
SGL_JUMP
VSUS_ON 2,28,32,62
JP6701
CPU_VRON_PWR 61
JP6702
SUSB#_PWR
JP6703
SUSC#_PWR
FOR TEST
+3VA
R1.1
11/09
Q6701
PMN45EN
+1.8VO
T6706
TPC28T
T6707
TPC28T
+1.8VS
(0.5A)
C6704
0.1UF/25V
R6704
0Ohm
0.01UF/25V
C6705
TPC28T T6708
TPC28T T6709
+3VO
Q6704
FDW2501NZ
DRAIN_1
SOURCE_1
SOURCE_2
GATE_1
DRAIN_2
SOURCE_3
SOURCE_4
GATE_2
TPC28T T6710
TPC28T T6711
T6712
TPC28T
+3VS
(4.0A)
C6706
0.1UF/25V
11/17
R6715
0Ohm
0.01UF/25V
C6713
TPC28T T6713
TPC28T T6714
+5VO
Q6707
FDW2501NZ
TPC28T T6715
TPC28T T6716
T6717
TPC28T
+5VS
(3.6A)
C6707
0.1UF/25V
TPC28T T6718
+12VSUS
T6720
TPC28T
24,28,32,36,38 SUSB_ON
T6721
TPC28T
R6707 1KOhm
62,63,64,66 SUSB#_PWR
R6709
100KOhm
@
Q6708
UMC4N
SUSB#_PWR_ON
R6708
10KOhm
TPC28T T6719
+12VS
(0.01A)
C6708
0.1UF/50V
R6708
100KOhm
TPC28T T6722
TPC28T T6723
+3VO
Q6709
PMN45EN
TPC28T T6724
TPC28T T6725
TPC28T T6726
+3V
(0.6A)
C6709
0.1UF/25V
11/17
R1.1
TPC28T T6727
TPC28T T6728
+5VO
Q6710
FDW2501NZ
R6716
0Ohm
0.01UF/25V
C6714
TPC28T T6729
TPC28T T6730
TPC28T T6731
+5V
(2.0A)
C6710
0.1UF/25V
TPC28T T6732
+12VSUS
T6733
TPC28T
28,36,38 SUSC_ON
T6734
TPC28T
R6711 1KOhm
65 SUSC#_PWR
R6713
100KOhm
Q6711
UMC4N
SUSC#_PWR_ON
R6710 10KOhm
TPC28T T6701
+12V
(0.01A)
C6701
0.1UF/50V
R6712
100KOhm
R2.0 4_11
SUSB#_PWR_ON
SUSB#_PWR_ON 64,66
R6705
100KOhm
Q6706B
UM6K1N
Q6706A
UM6K1N
SUSB#_PWR
R6701
100KOhm
Q6705B
UM6K1N
Q6705A
UM6K1N
SUSC#_PWR_ON
SUSC#_PWR
AC_BAT_SYS 14,39,61,62,63,64,65,66,68,71
BAT 29,68,70,71
+5VAO 62,64
+5VO 37,62,63,64,65,66,71
+5V 2,5,14,35,36,48
+5VS 8,15,19,20,21,22,27,28,36,37,48,49,50,61
+3VA 2,9,14,16,19,24,28,37,38,64,65,71
+3VAO 64
+3VO 62,64
+3VSUS 17,18,19,20,24,26,32,33,36,37,38,49,50,62,63,65,70
+3V 14,17,24,26,36,45,50
+3VS 2,5,6,8,11,12,13,14,15,16,17,18,19,20,21,22,24,26,27,28,30,31,32,34,36,37,48,49,50,61,63,64
+3VS_G73M 15,36,41,44,45,46,50,64
+12VSUS 62,64
+12V 8,22,32,35,36,64
+12VS 14,15,22,36,37
+2.5VO 64
+2.5VS 2,9,12,13,15,36,64
+2.5VS_G73M 36,44,46,64
+1.8VO 63,64,65
+1.8V 2,4,5,6,9,36,65
+1.8VS 13,36
+1.8VS_G73M 36,42,43,44,46,64
+1.5VSUS 18,20,64
+1.2VSUS 64
+1.2VO 63,64
+1.2VS 9,10,11,13,16,20,36,50,63
+1.2VS_HT 2,4,9,13,36,63
+1.2VS_G73M 36,41,42,43,64
+VCORE 4,61
VGA_VCORE 41,66
+0.9V 4,7,36,65
+0.9VS_G73M 36,43,44,47,50,64
+5VCHG 68,71
+5VLCM 37,71
+2.5VREF 63,71
<Variant Name>
Title : POWER_LOAD_SYSTEM
ASUSTECH
Engineer: Adams_Lin
Size Custom
Project Name F3T
Rev 1.0
Date: Monday, May 29, 2006
Sheet 67 of 74


(12/07/05)
71 CHG_SRC
71 CSSP
71 CSSN
71 MAX8725_PDS
71 MAX8725_PDL
C6801 0.1UF/25V
C6802 0.1UF/25V
C6803 1UF/25V
C6805 0.1UF/25V
R1.1
T6802 TPC28T
AC_BAT_SYS
CE6801 27UF/25V
CHG_GND
T6803 T6804 TPC28T TPC28T
Q6802 SI4835BDY
Q6803 SI4800BDY
MAX8725_LDO
A/D_DOCK_IN
LDO : 5.4V
REF : 4.2235V
PKPRES#
R6817 100KOhm
Q6801B UM6K1N
C6715 1UF/6.3V
R6803 100KOhm
T6806 TPC28T
MAX8725_REF
D6802 1SS355
T6805 TPC28T
R6804 100KOhm
U6801
MAX8725ETI
DCIN LDO ACIN REF GND/PKPRES# ACOK MODE
DLOV DLO PGND CSIP CSIN BATT GND1
R6802 33Ohm
C6806 1UF/25V
T6801 TPC28T
L6801 10UH
R6805 25mOHM
T6807 TPC28T
T6808 TPC28T
BAT
SHORT_PIN JP6803
SHORT_PIN JP6801
CE6802 27UF/25V
T6815 TPC28T
Q6801A UM6K1N
TS#
C6815 0.22uF/16V
R6806 13.3KOhm
C6807 4.7UF/25V
C6808 1UF/25V
C6809 1UF/25V
R6807 10KOhm
R6808 40.2KOhm
R6809 16.5KOhm
CHG_CCS
CHG_CCI
R6810 10KOhm
C6812 0.047UF/16V
AD_IINP
R6816 10KOhm
C6813 0.1UF/16V
C6811 0.01UF/50V
C6814 0.1UF/16V
R6811 22.6KOhm
R6812 1.91KOhm
R6813 14.7KOhm
R6814 100KOhm
R6815 10.5KOHM
11/02
T6811 TPC28T
Q6804A UM6K1N
BATSEL_2P#
T6810 TPC28T
PRECHG
Q6805A UM6K1N
11/01
T6812 TPC28T
Q6807 2N7002
28 CHG_EN#
T6814 TPC28T
28 AC_APR_UC
+5VCHG
R6818 4.7KOhm
R6825 15KOhm
R2.0
11/02
Q6804B UM6K1N
MAX8725_LDO
R6819 100KOhm
28 BATSEL_3#
Q6809 2N7002
T6817 TPC28T
28 BAT_LEARN
Q6805B UM6K1N
R6820 470KOhm
T6813 TPC28T
28 AC_IN#
R7504 237KOhm
Q6806 PMBS3904
R7505 10KOhm
C7504 0.1UF/25V
R2.0
4_24
R2.0
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.46V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01 ohm
VCLS= 2.59V
=> Iin(max)=4.6A
=> Constant Power = 19 * 4.737A = 90W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.0V => Ichg = 2.5A
VICTL= 1.5V => Ichg = 1.25A
VICTL= 0.18V => Ichg = 150mA
Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.615V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Title : POWER_CHARGE
ASUSTECH
Engineer: Adams_Lin
Size Custom
Project Name F3T
Rev 1.0
Date: Monday, May 29, 2006
Sheet 68 of 74

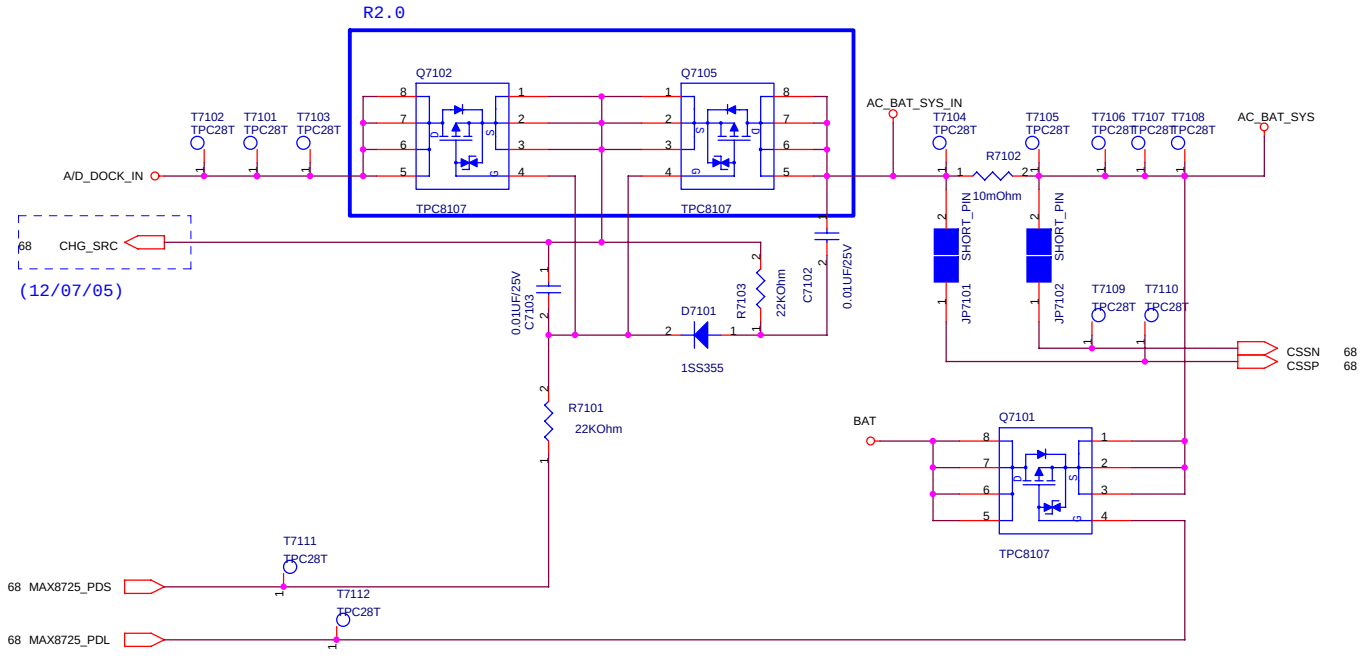
Title :	
ASUSTECH	Engineer: Adams_Lin
Size: Custom	Project Name: F3T
Rev: 1.0	
Date: Monday, May 29, 2006	Sheet 69 of 74

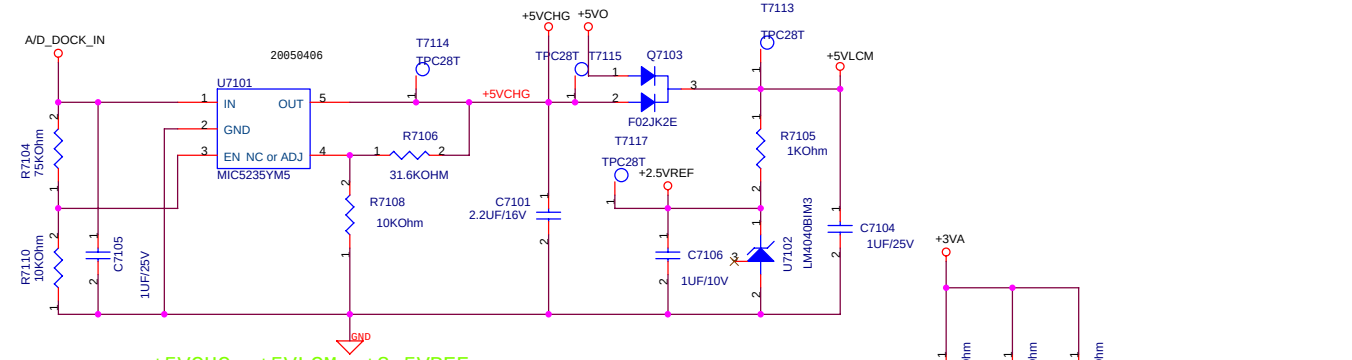
R2.0

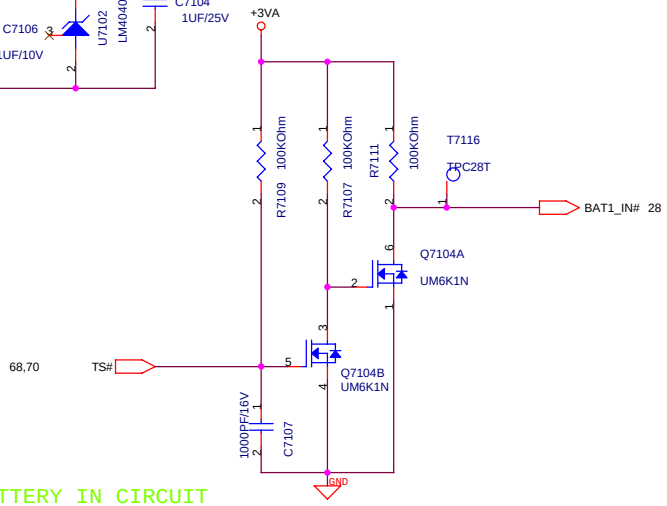


11/23:Change P/N and footprint use 12G200010909

ASUSTECH	Title : POWER_PROTECT	
	Engineer: Adams_Lin	
Size: Custom	Project Name: F3T	Rev: 1.0
Date: Monday, May 29, 2006	Sheet 70 of 74	







ASUSTECH	Title : POWER_SWITCH_5VLCM	
	Engineer: Adams_Lin	
Size: Custom	Project Name: F3T	Rev: 1.0
Date: Monday, May 29, 2006	Sheet 71 of 74	

Title : SYSTEM RESOURCE

Engineer: JAY TSAI

Size	Project Name	Rev
C	F3T	1.0

Date: Monday, May 29, 2006 Sheet 72 of 74

NOTE 1

The level shifter for the signals from us: CPU_RST, CPU_PWGD, HT_STOP outputs from C51, these 3 signals are bi-directional signals and we may use the input the portion of the I/O buffer. We confirmed 1.8V is in the area that is may not be recognized correctly.

NOTE 2 **ROM Strap Block Location**

The ROM Strap logic is implemented in the subtractive device in the system. This ensures that there is the minimum amount of logic between the subtractive device and the system BIOS, thus reducing the portions of the design that must come up operating correctly on reset. The companion MCP needs only PCI_CLK and the LPC bus to come up before it can complete its ROM Strap. C51 needs the Hypertransport link to the companion MCP to come up before the ROM Strap can begin. This link boots to a fixed frequency and relies on the clock from the companion MCP so it should require no additional configuration to start up.

NOTE 3 **Getting Pointers to Safe or User Tables**

The first read by the ROM Strap logic is to read a fixed address to get a pointer to the BIOS table There are two pointers—one for the Safe table and one for the User table. The C51 will always read from the User table, but the companion MCP may override it and force it to read from the Safe table. The C51 will be unaware that this has occurred, but will receive a pointer to the Safe table instead of the User table. The C51 will always check that the table has the magic value 2B16D065h as the first entry in the table..

Note: The User and Safe tables may reside at any address in the ROM BIOS image. There are no restrictions for data alignment for any of these tables; they may appear at any byte-aligned

NOTE 4

1. What is "Defer shut down"?

Ans:The signal is used only in system with more than one MCP51 (master/slave). The master will wait for the slave (via this pin) before shutting down.

NOTE 5

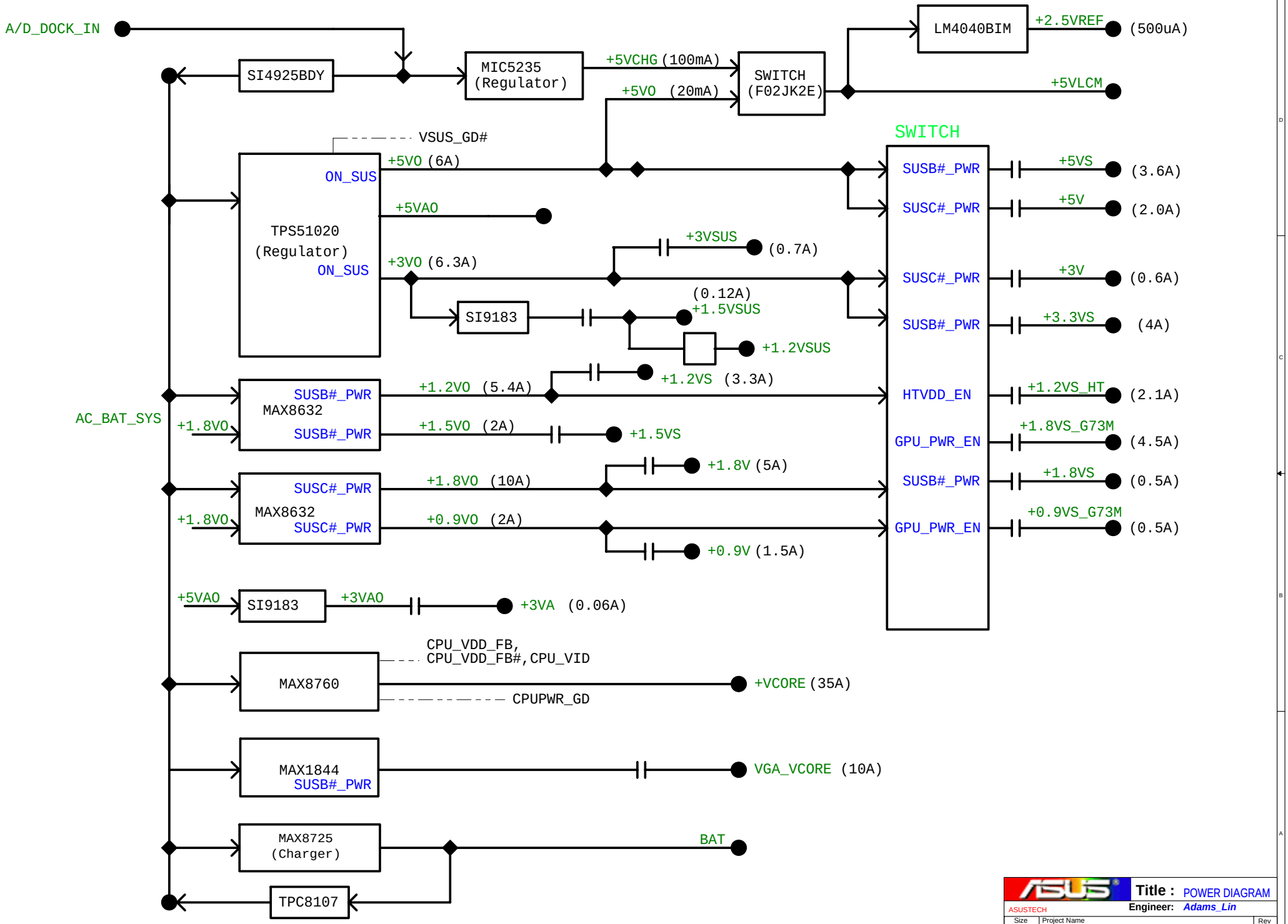
2. Why is 4.7uF necessary for VCC_RTC?

Ans: VBAT input consumes much more power (10~20 times more) when the chip is powered up. 10uA is only when it is powered by battery.

NOTE 6

Battery discharge current is 6A.

ASUS	Title : NOTE	
1	Engineer: JAY TSAI	
Size: C	Project Name: F3T	Rev: 1.0
Date: Monday, May 29, 2006	Sheet 73 of 74	



ASUSTECH	Title : POWER DIAGRAM	
	Engineer: Adams_Lin	
Size: Custom	Project Name: F3T	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 74 of 74	

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