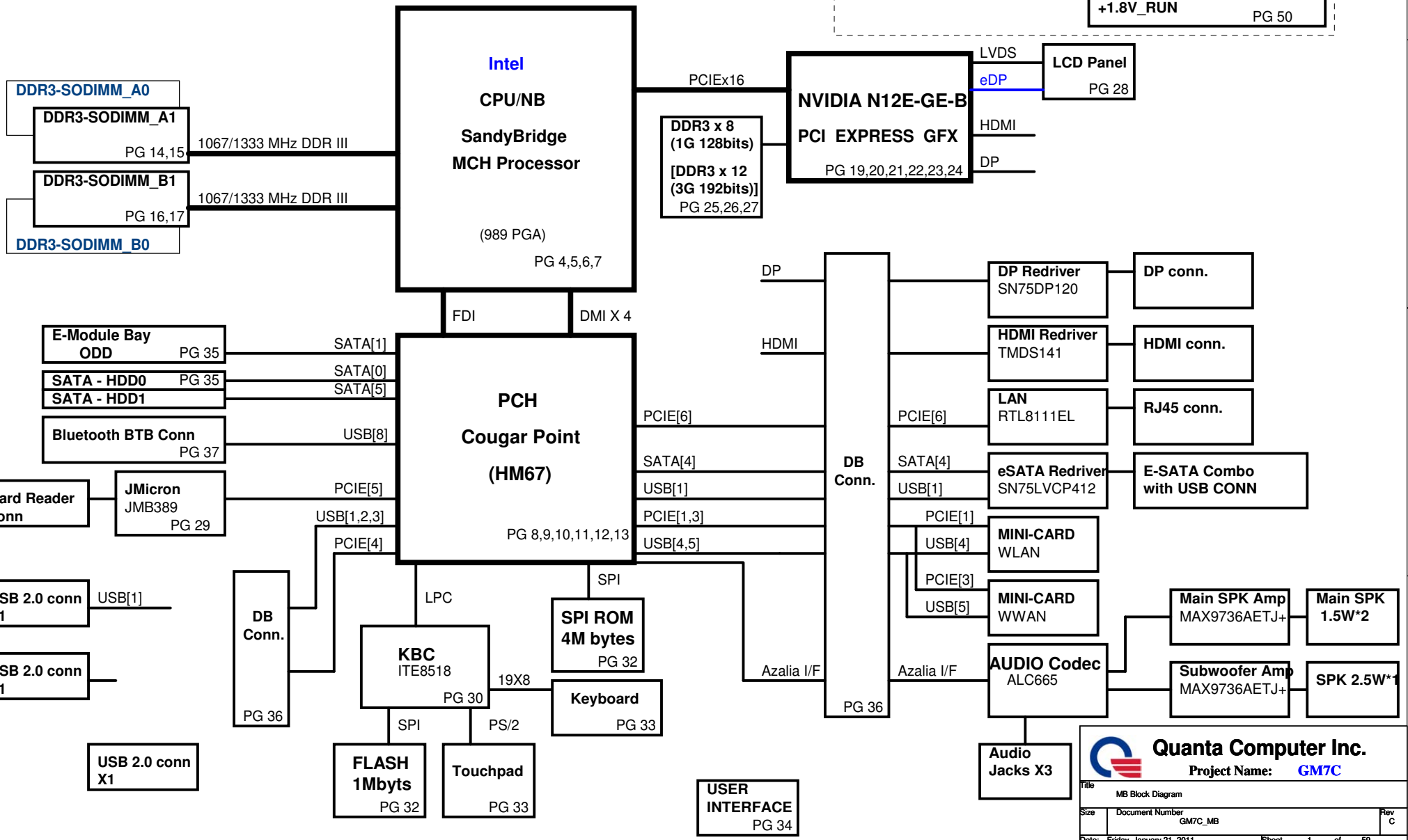


System Block Diagram of GM7C

FAN & THERMAL
SMSC EMC2112 PG 31

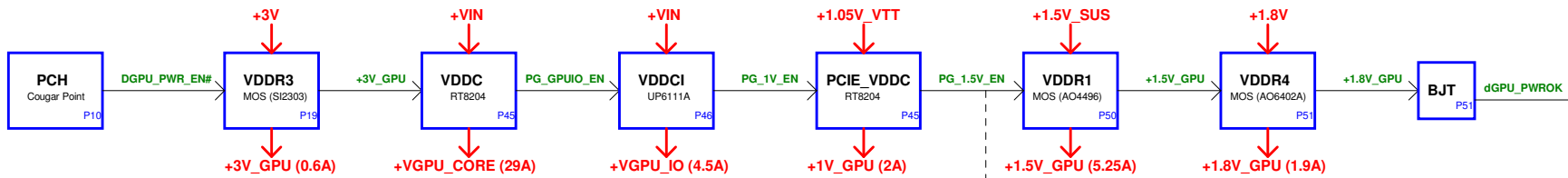
REGULATOR	
+1.5V_SUS/+0.75V_DDR_VTT	PG 44
+1.05V_RUN	PG 46
+1.1V_RUN_VTT	PG 45
POWER	
CPU CORE	PG 43
DC/DC +3.3V_ALW/+5V_ALW/ +15V_ALW	PG 47
VGA / Nvidia	PG 48
VGA / Intel	PG 49
+1.8V_RUN	PG 50



Quanta Computer Inc.
Project Name: **GM7C**

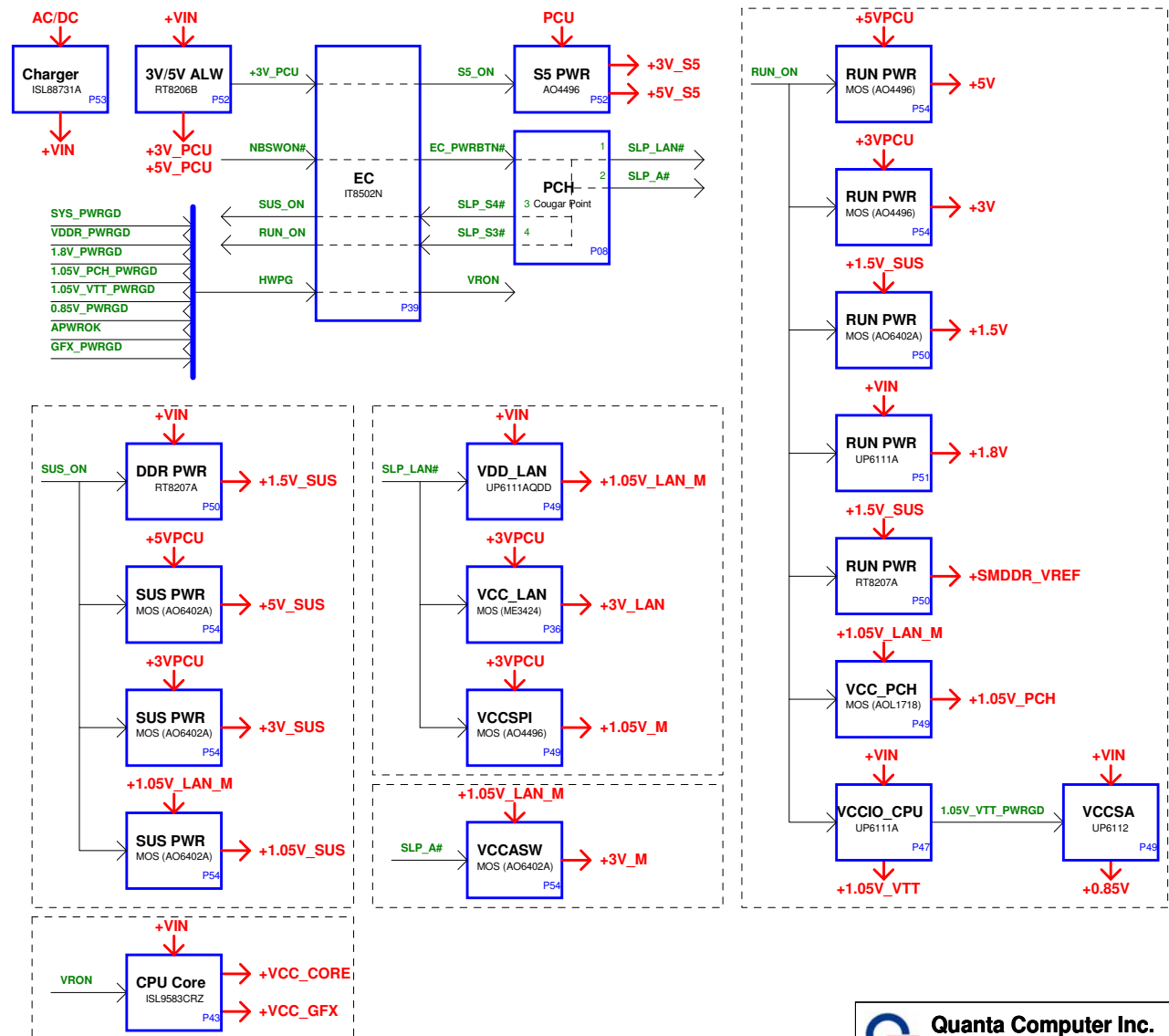
Title	MB Block Diagram	
Size	Document Number	Rev
	GM7C_MB	C
Date:	Friday, January 21, 2011	Sheet 1 of 59

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)




Main Power Rails

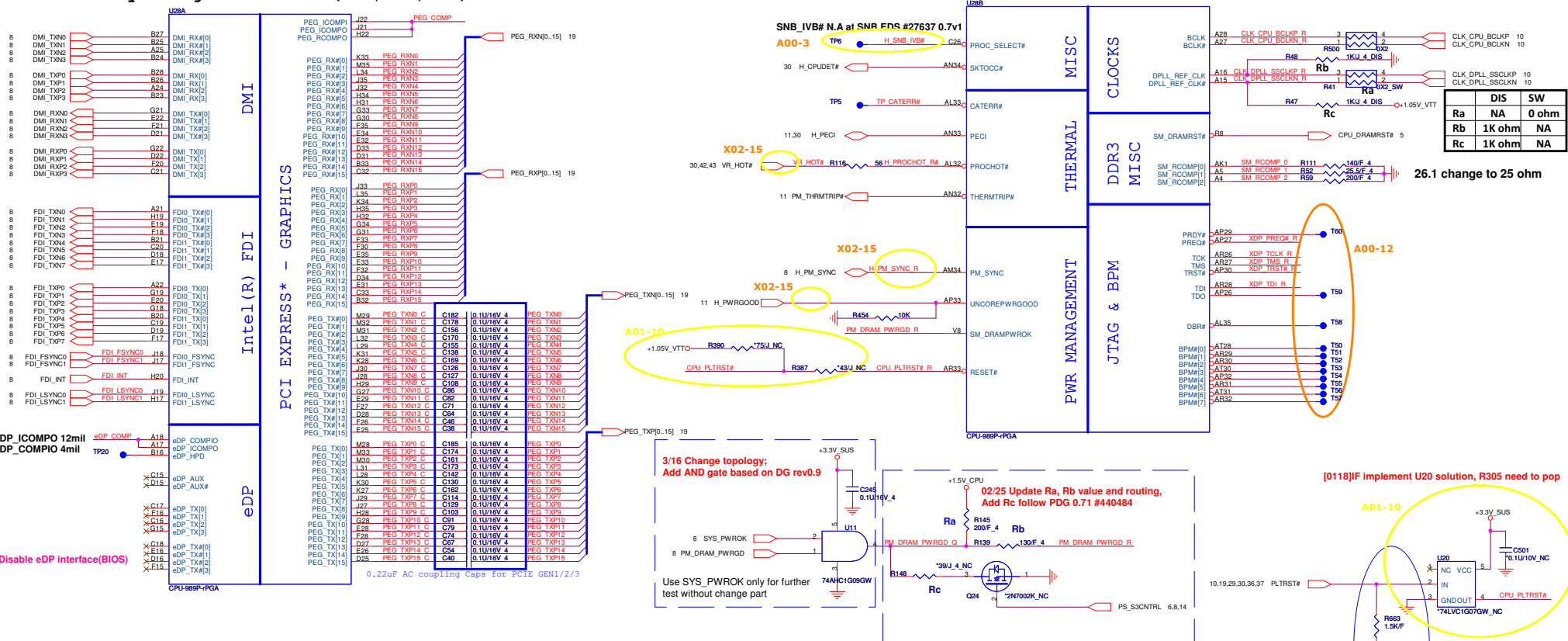
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+0.75V_DDR_VTT	+0.75V	DDR3 reference voltage	RUN_ON	
+0.85V	+0.9V	Intel new power rail	1.05V_VTT_PWRGD	
+1.05V_LAN_M	+1.05V	LAN M power for iAMT	SLP_LAN#	
+1.05V_M	+1.05V	ME power for iAMT	SLP_A#	
+1.05V_PCH	+1.05V	PCH core power	RUN_ON	
+1.05V_SUS	+1.05V	USB3.0 chip power	SUSD	
+1.05V_VTT	+1.05V	CPU core logic power	RUN_ON	
+1.5V	+1.5V	I/O module power	RUN_ON	
+1.5V_CPU	+1.5V	CPU DDR3 controller power	RUN_ON_D	
+1.5V_GPU	+1.5V	GPU DDR3 controller power	PG_1.5V_EN	
+1.5V_SUS	+1.5V	DDR3 SODIMM power	SUS_ON	
+1.8V	+1.8V	CPU/PCH/LVDS power	RUN_ON	
+1.8_GPU	+1.8V	GPU power	+1.5V_GPU	
+1V_GPU	+1V	GPU PCIE VDDC power	PG_1V_EN	
+3V	+3.3V	I/O power	RUN_ON	
+3V_GPU	+3.3V	GPU power	DGPU_PWR_EN#	
+3V_M	+3.3V	PCH/SPI power for iAMT	SLP_A#	
+3V_S5	+3.3V	3V power sequence	S5_ON	
+3V_SUS	+3.3V	USB3.0 chip power	SUSD	
+3VPCU	+3.3V	Always power	SYS_SHDN#	
+5V	+5V	I/O power	RUN_ON	
+5V_S5	+5V	5V power sequence	S5_ON	
+5V_SUS	+5V	USB2.0 power	SUSD	
+5VPCU	+5V	Always power	SYS_SHDN#	
+15V_ALW	+15V	Power sequence		
+SMDDR_VREF	+0.75V	DDR3 reference power	RUN_ON	
+VCC_CORE	+1.1V	CPU Core power	VRON	
+VCC_GFX	+1.52V	Internal GPU Core power	VRON	
+VGPU_CORE	+1V	GPU Core power	DGPU_VRON	
+VGPU_IO	+1V	GPU I/O controller power	PG_GPUIO_EN	
+VIN	+19V	AC power input		



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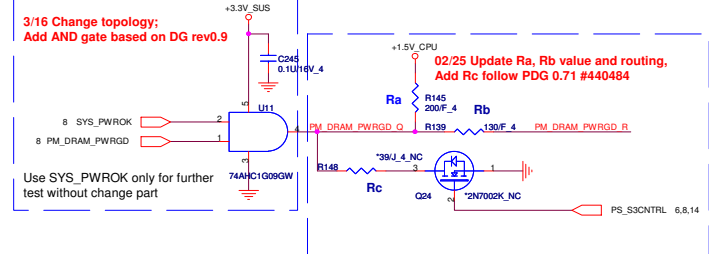
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		Project Name: GM7C	
Title: Blank			
Size	Document Number: GM7C_MB		Rev: C
Date: Friday, January 21, 2011		Sheet: 3	of 59

Sandy Bridge Processor (DMI, PEG, FDI)



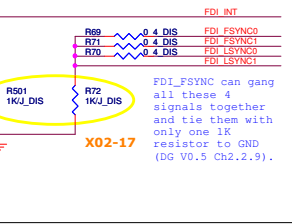
	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

26.1 change to 25 ohm

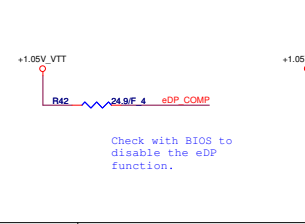


[0118]F implement U20 solution, R305 need to pop

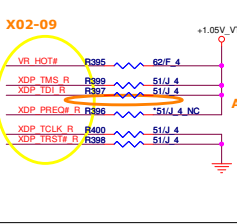
FDI Disabling (Discrete Only)



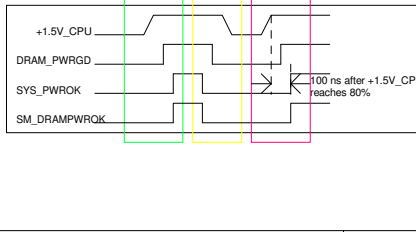
eDP & PEG Compensation



Processor pull-up(CPU)



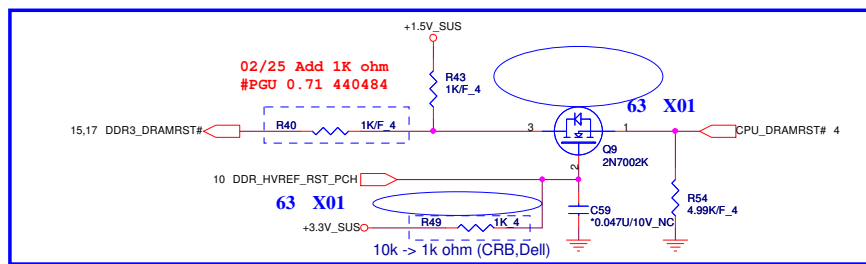
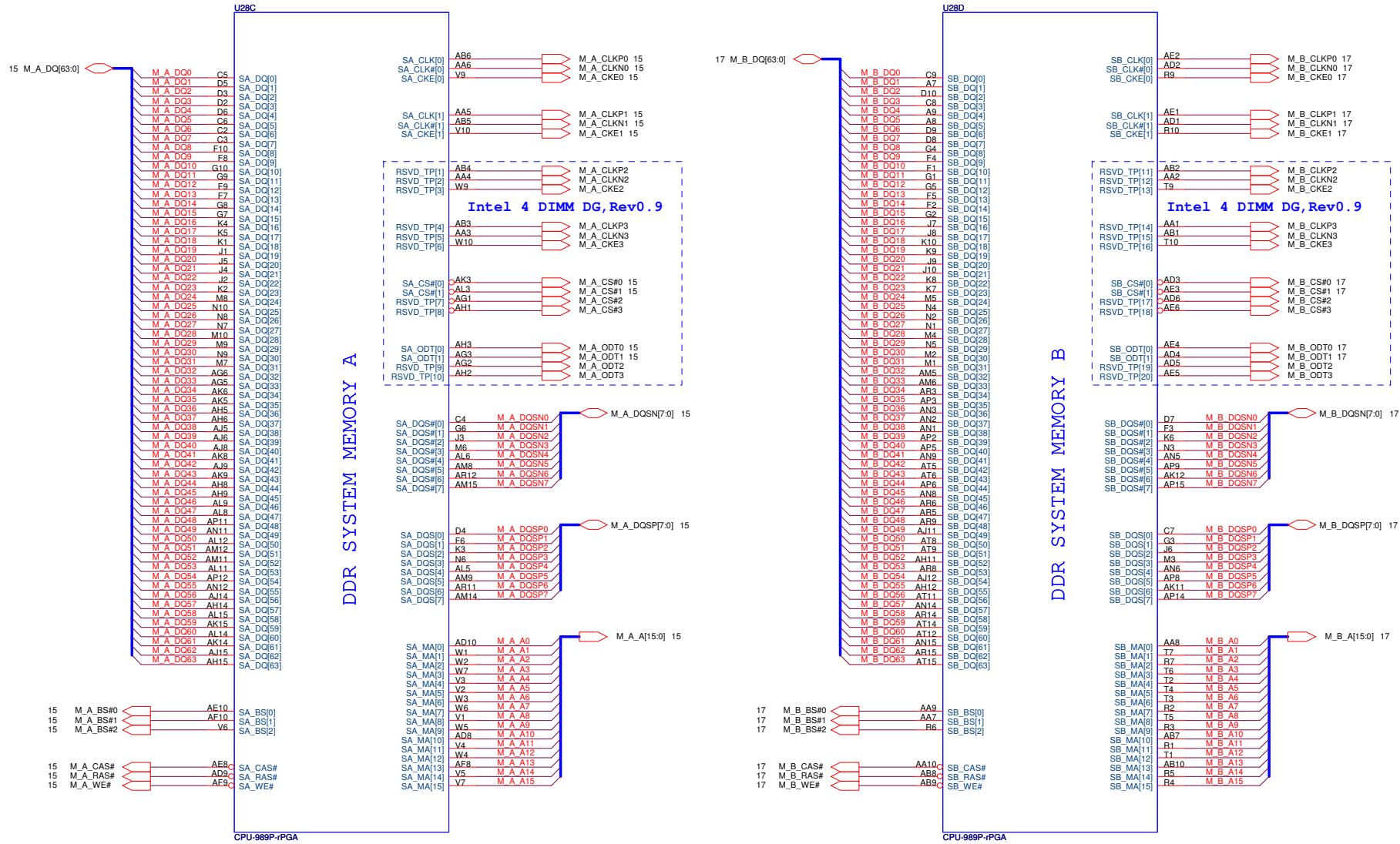
Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H



Quanta Computer Inc.
Project Name: **GM7C**

File: SNB I/4_PEG,DMI,FDI,MISC
Size: Document Number: GM7C_MB
Date: Friday, January 21, 2011 Sheet 4 of 59

Sandy Bridge Processor (DDR3)



Quanta Computer Inc.
Project Name: **GM7C**

Title: **SNB 24_DDR3**

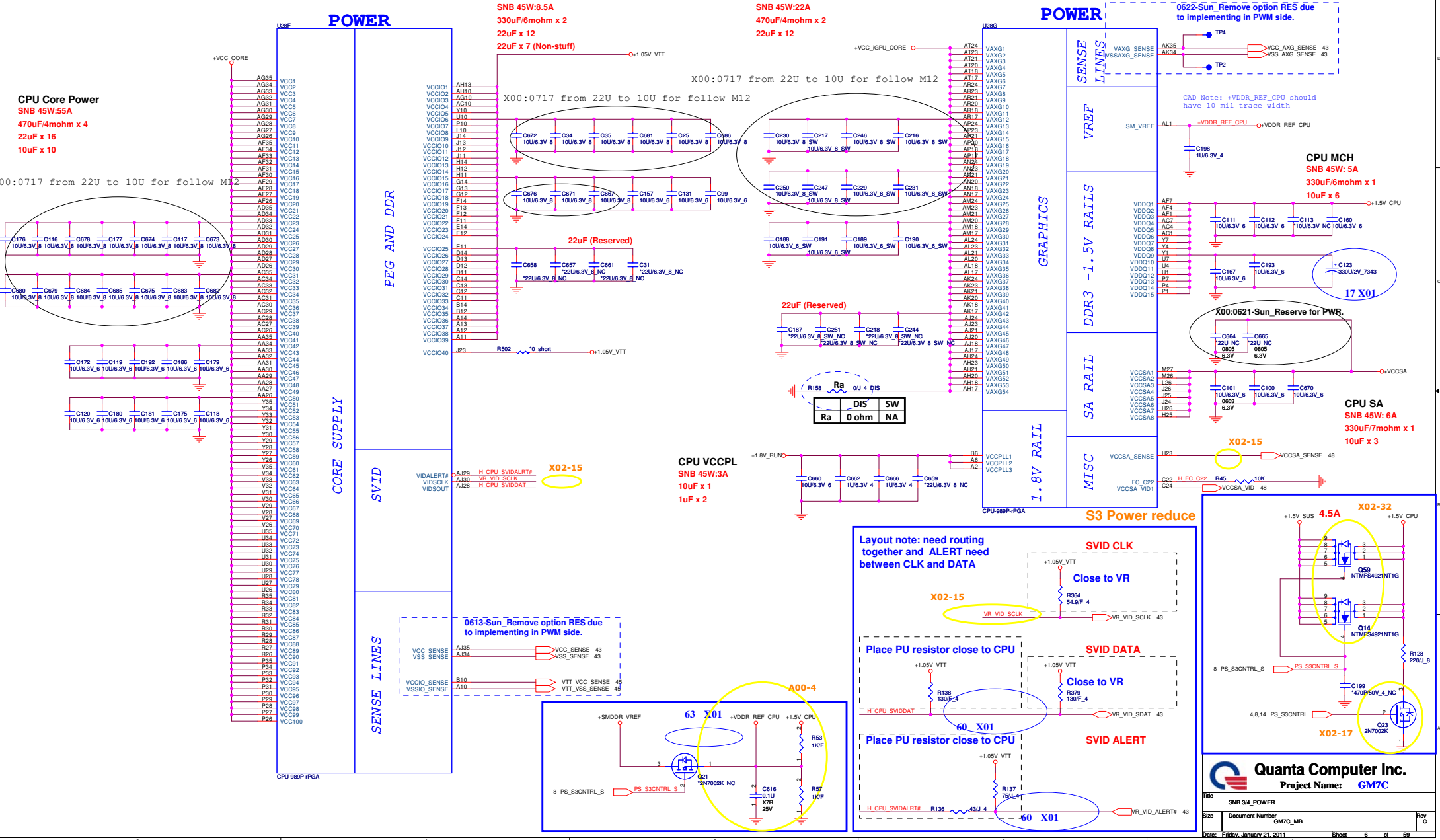
Size: **GM7C_MB**

Date: **Friday, January 21, 2011**

Sheet: **5** of **59**

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

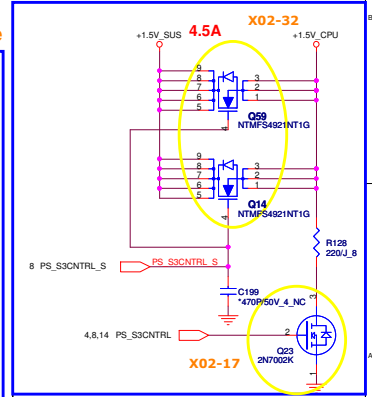


Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
X02-15

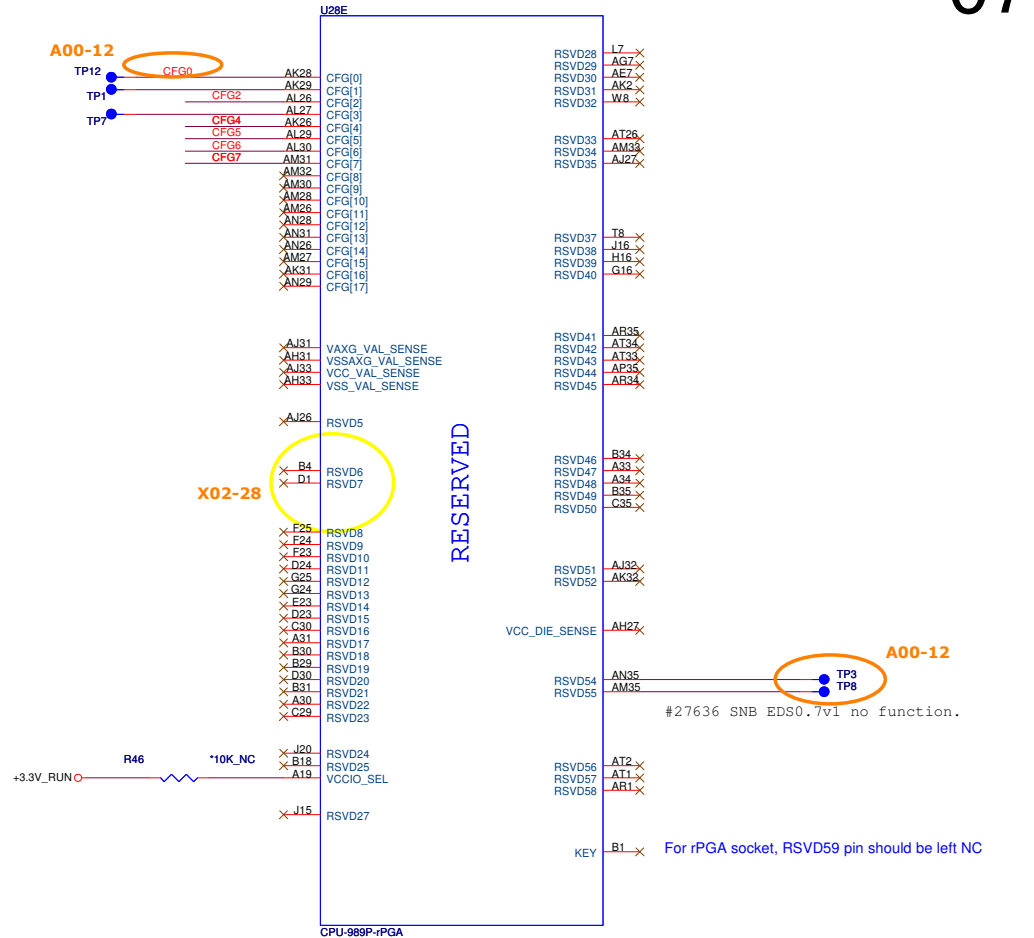
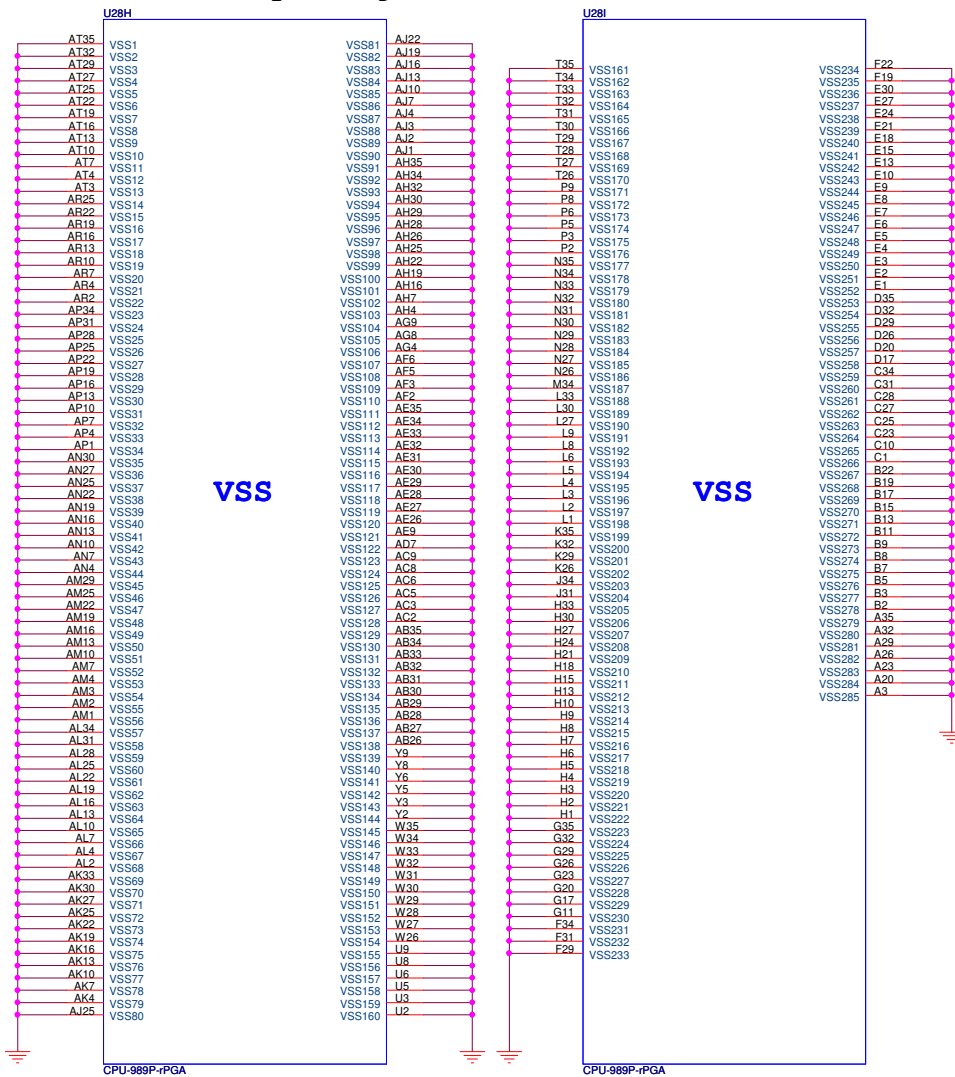
SVID DATA
Place PU resistor close to CPU
Close to VR

SVID ALERT
Place PU resistor close to CPU



Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



VSS

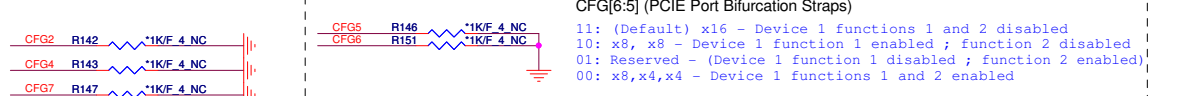
VSS

RESERVED

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

CFG	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



Quanta Computer Inc.
Project Name: **GM7C**

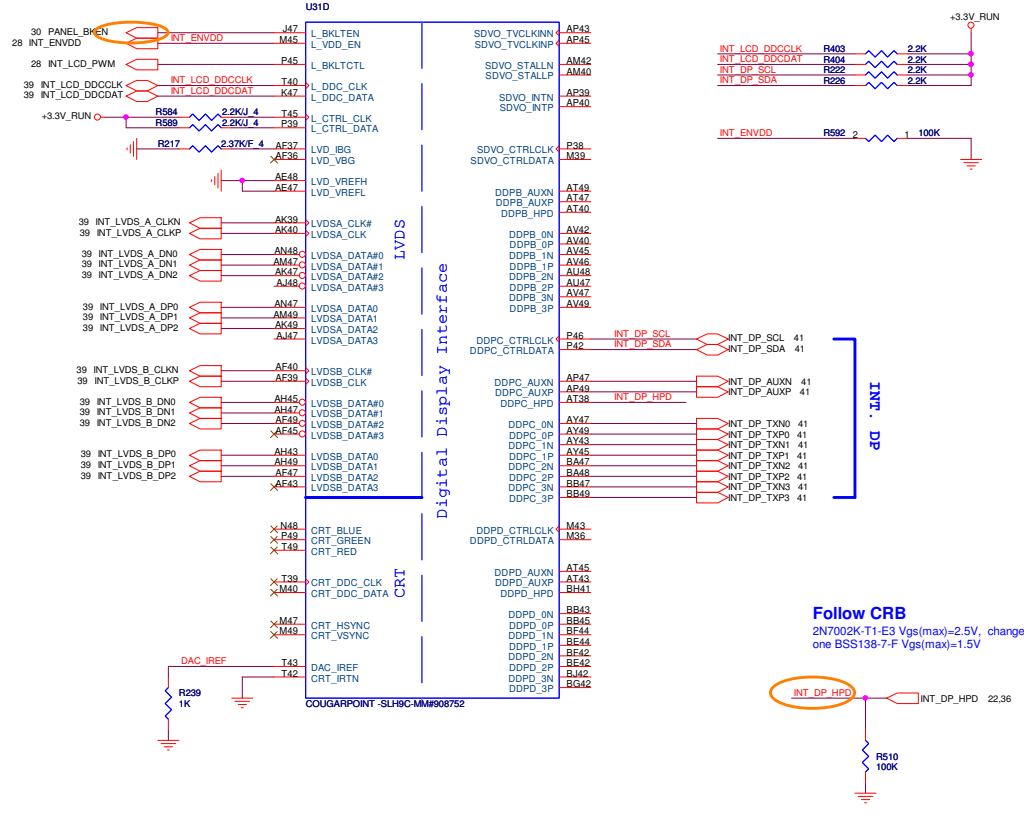
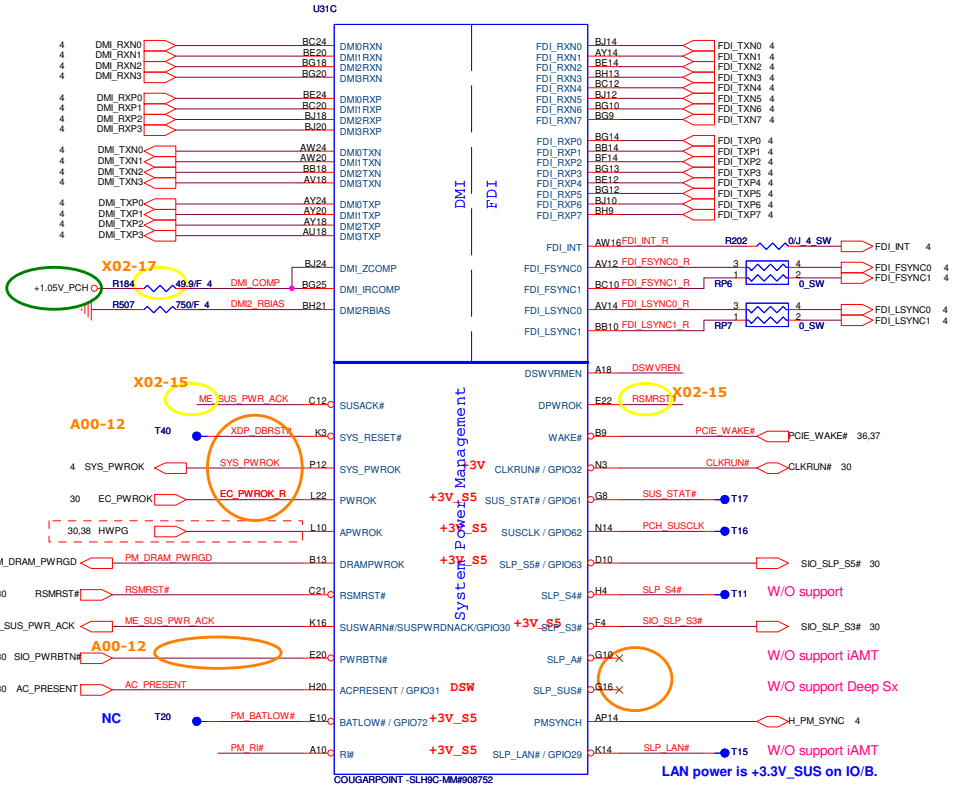
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Size: Document Number: GM7C_MB Rev: C

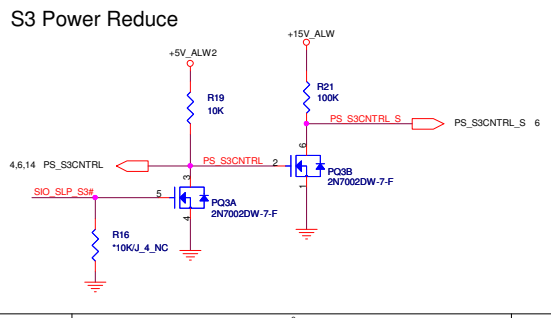
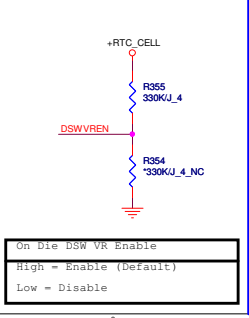
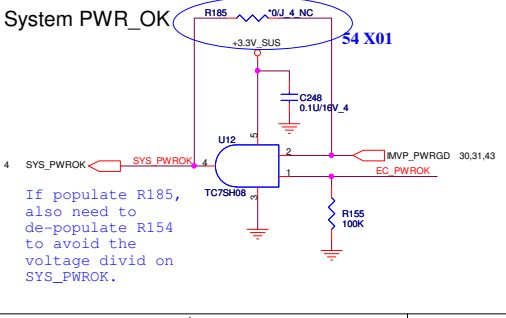
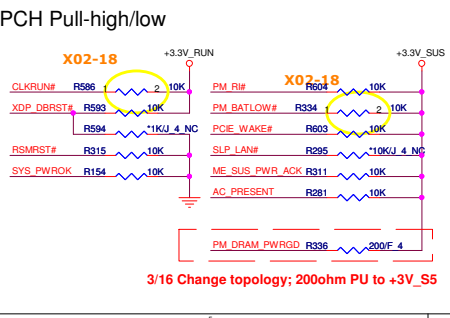
Date: Friday, January 21, 2011 Sheet: 7 of 59

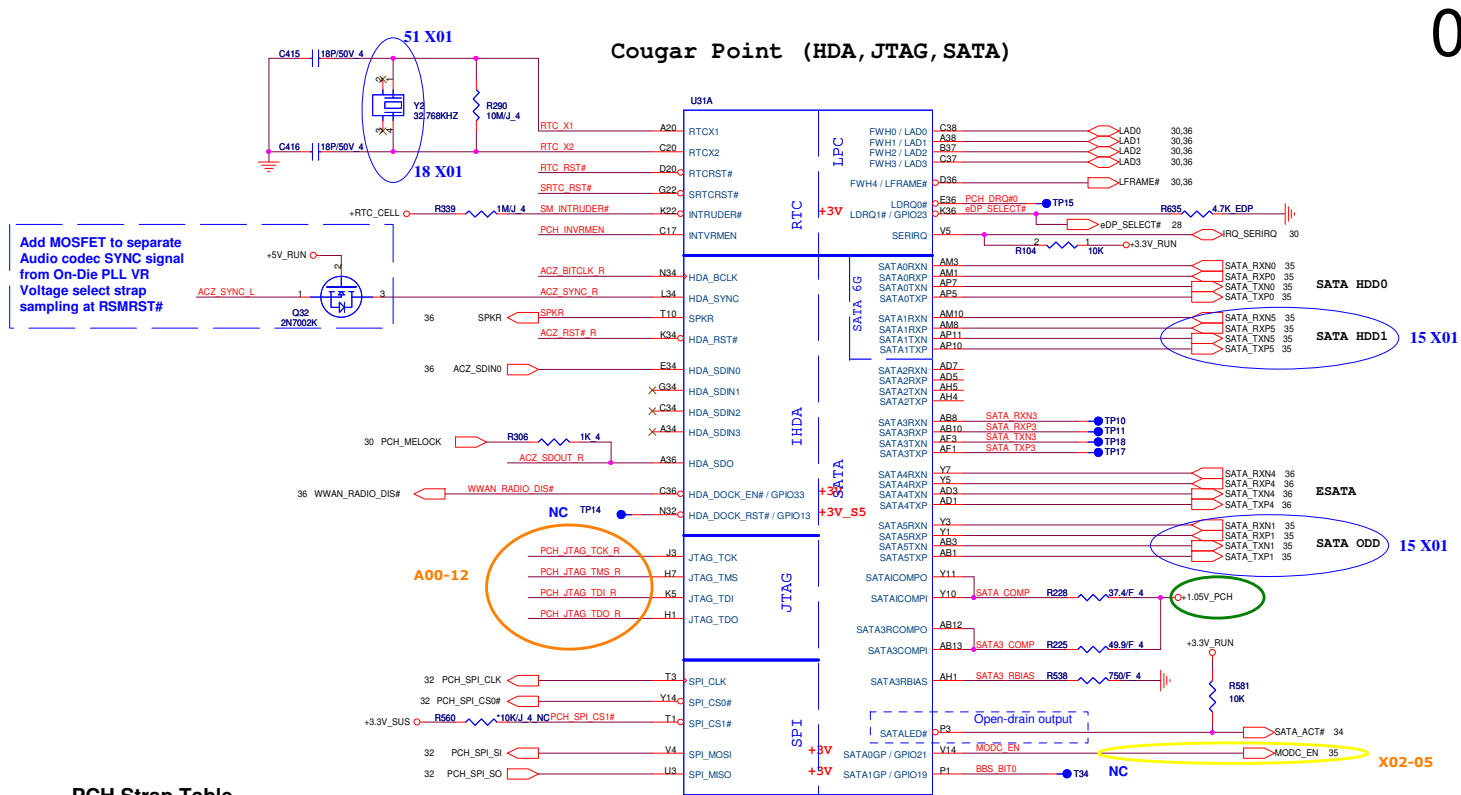
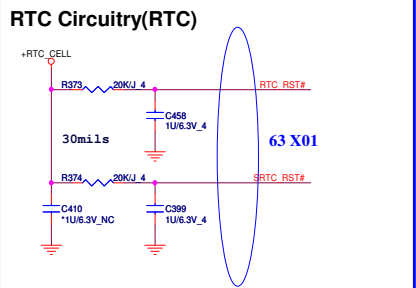
Cougar Point (LVDS, DDI)

Cougar Point (DMI, FDI, PM)

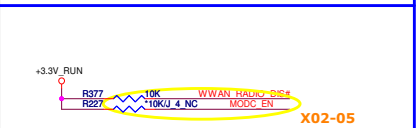
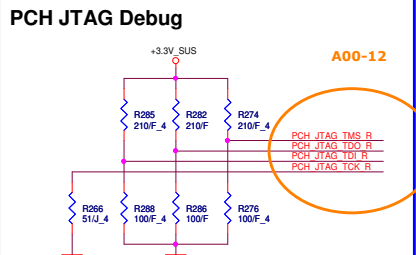
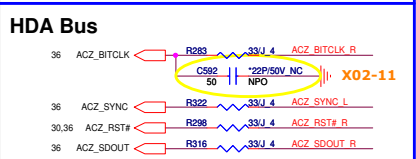


Follow CRB
2N7002K-T1-E3 Vgs(max)=2.5V, change a small one BSS138-7-F Vgs(max)=1.5V





Add MOSFET to separate Audio codec SYNC signal from On-Die PLL VR Voltage select strap sampling at RSMRST#



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN - R291 10KJ 4 NC SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R328 10KJ 4 NC PCI_GNT3# 10									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL - R361 330KJ 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K		R329 10KJ 4 NC BBS_BIT1 10 R582 10KJ 4 NC BBS_BIT0									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3.3V_RUN - R317 10KJ 4 NC ACZ_SDOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWR0K	For Sandy Bridge processor only: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 k Ohm resistor.	+1.8V_RUN - R512 2.2K DF_TVS 11									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R357 10KJ 4 NC PLL_ODVR_EN 11									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3.3V_SUS - R255 10KJ 4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	Need check schematic									
SPI_MOSI	iTPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWR0K	0 = Disable (Internal pull-down 20kohm)										

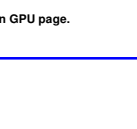
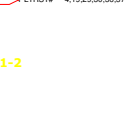
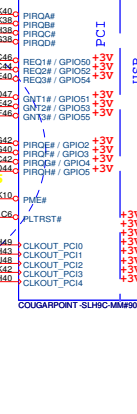
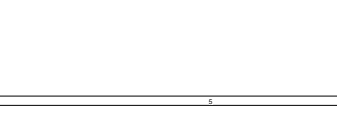
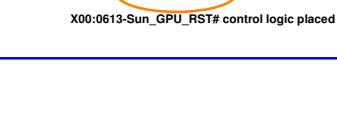
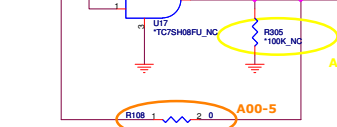
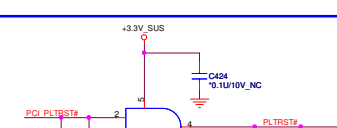
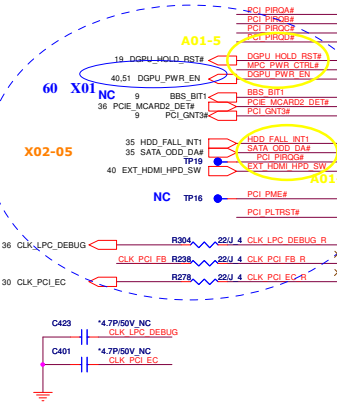
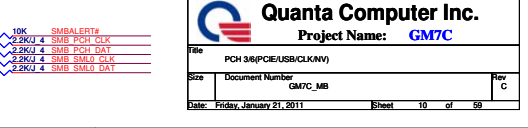
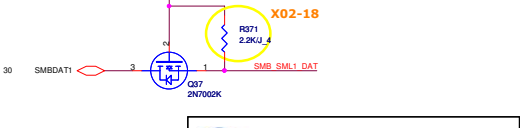
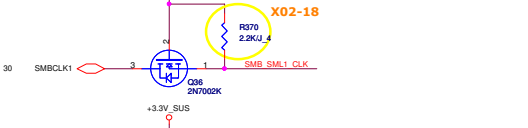
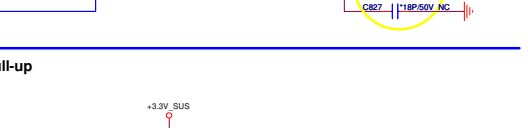
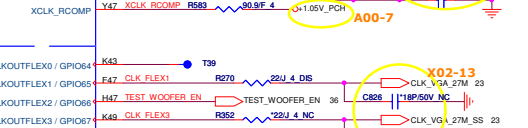
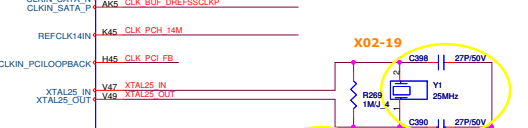
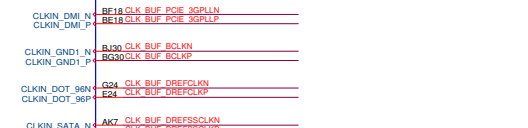
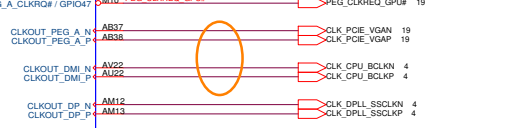
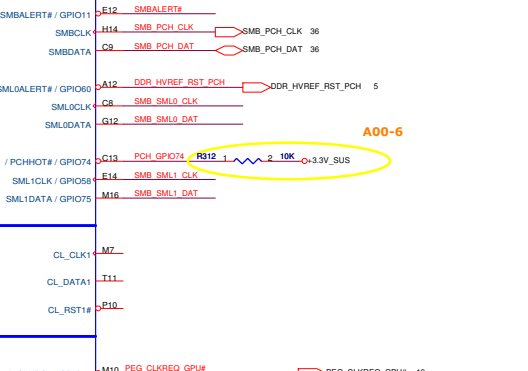
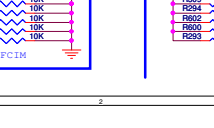
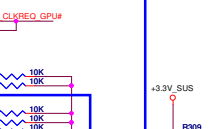
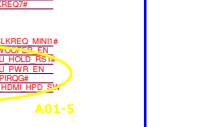
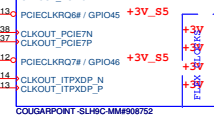
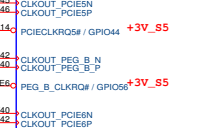
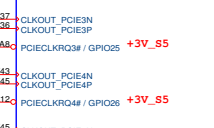
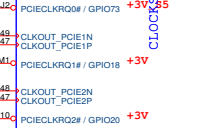
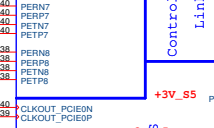
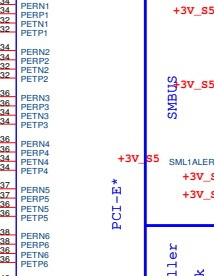
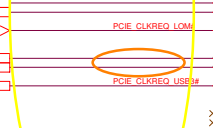
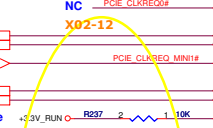
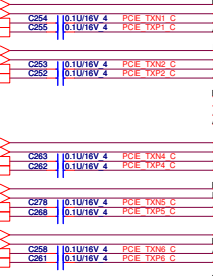
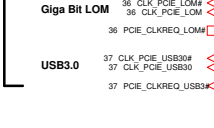
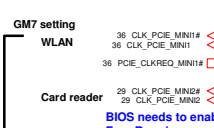
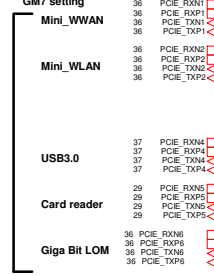
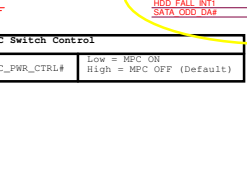
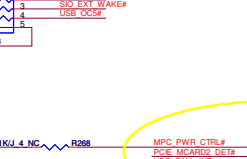
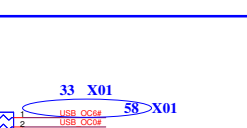
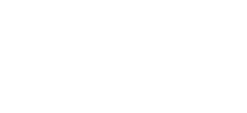
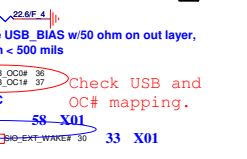
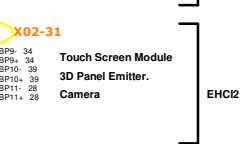
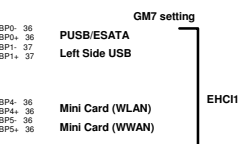
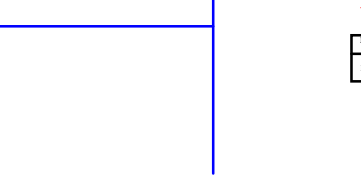
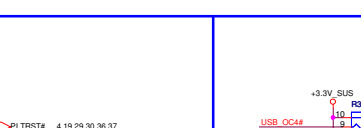
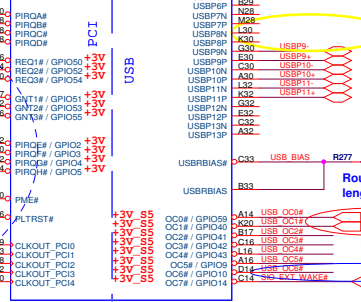
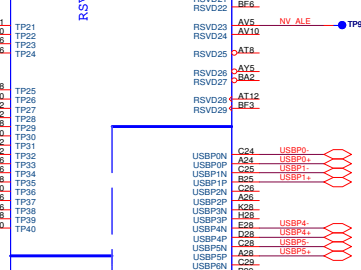
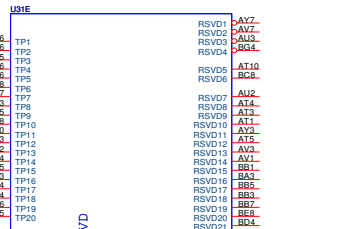
A00-3
New Add in CPT EDS Rev1.0 at 0316

3/16 Remove based on CPT EDS rev1.0

3/16 Remove based on CPT EDS rev1.0

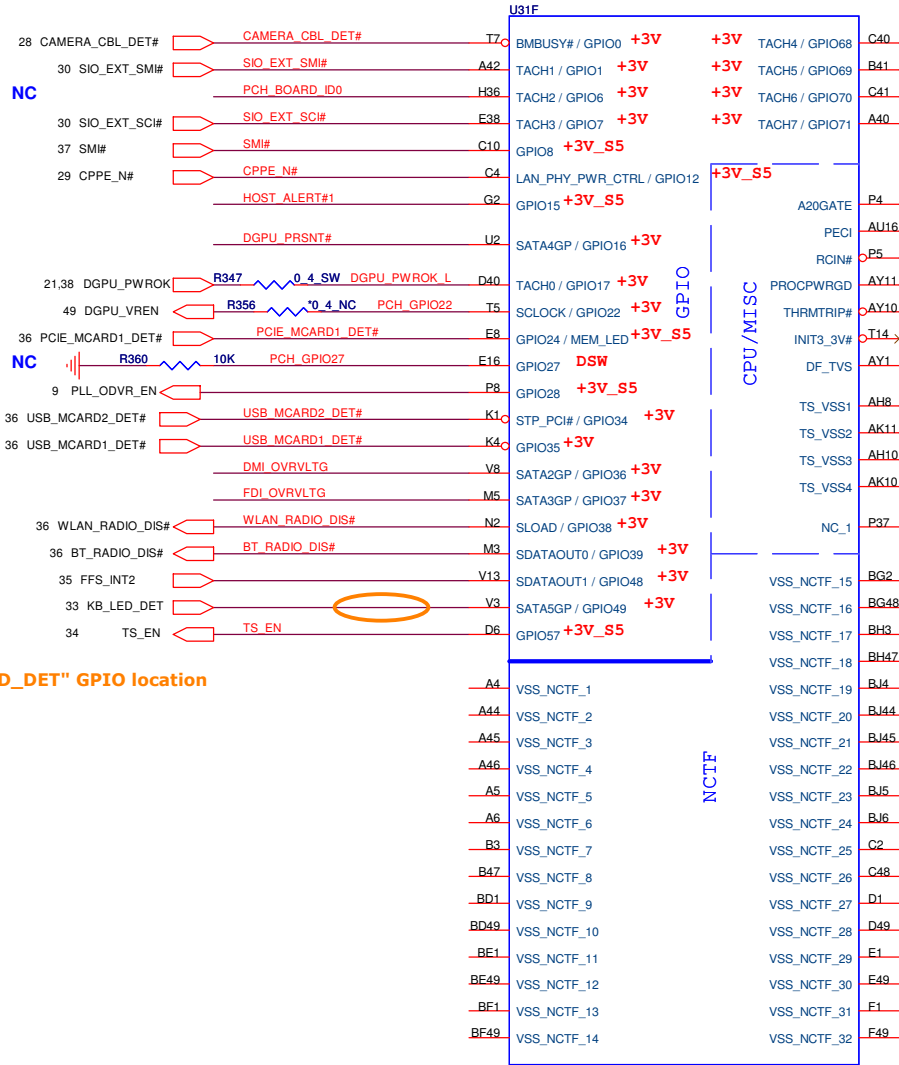
3/16 Remove based on CPT EDS rev1.0

Cougar Point-M (PCI, USB, NVRAM)



Cougar Point (GPIO, VSS_NCTF, RSVD)

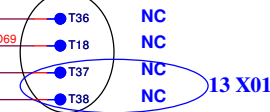
X01: Reserve for no using by BIOS.



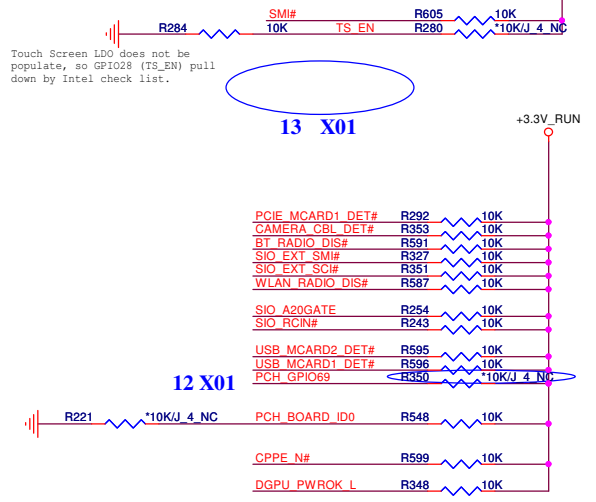
X02-03 Change "KB_LED_DET" GPIO location

X00: Layout: Place R8478 close to CPU side to reduce stub from CPU.

3/16 Connected to GND DG rev0.9



Touch Screen LDO does not be populate, so GPIO28 (TS_EN) pull down by Intel check list.



02/20 DEL for Pre-ES1

BIOS RECOVERY	High = Disable (Default) Low = Enable
Intel ME Crypto Transport Layer Security (TLS) cipher suite	
Low = Disable (Default) High = Enable	

	SWITCHABLE	UMA
Stuff	R8489	R8490
No Stuff	R8490	R8489

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage
DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

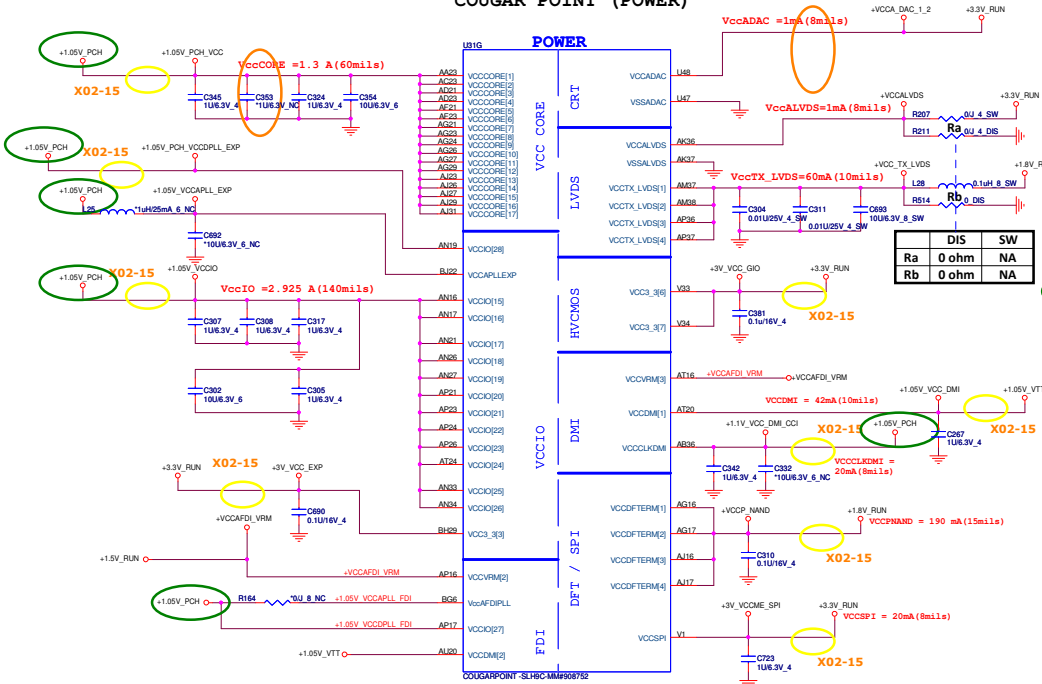
Quanta Computer Inc.
Project Name: **GM7C**

Title: PCH 4/6(GPIO/CPU)

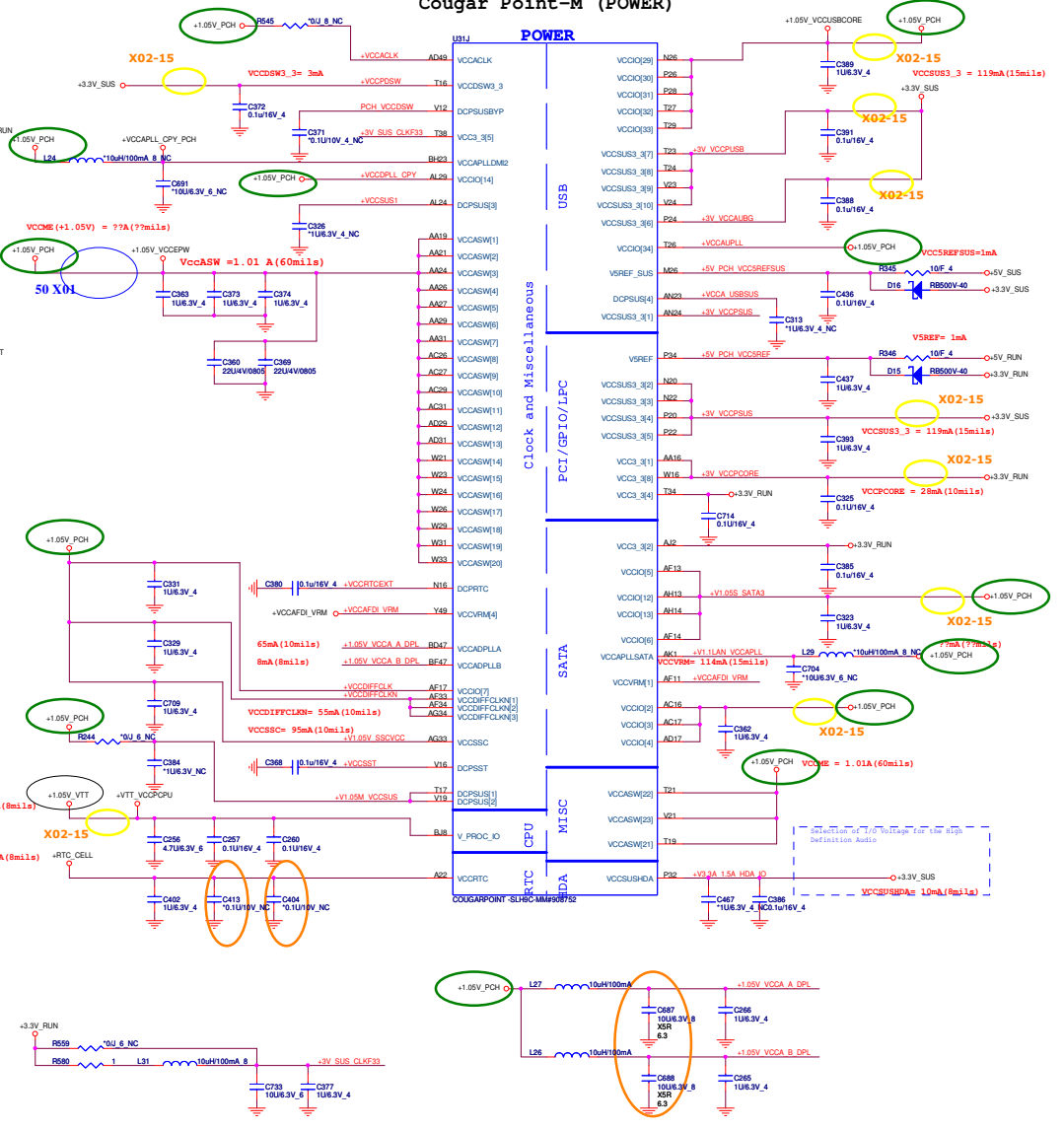
Size: Document Number GM7C-MB

Date: Friday, January 21, 2011 Sheet 11 of 59

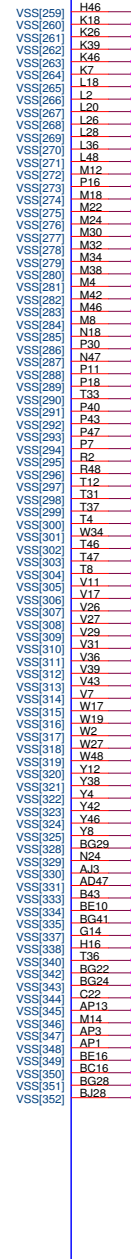
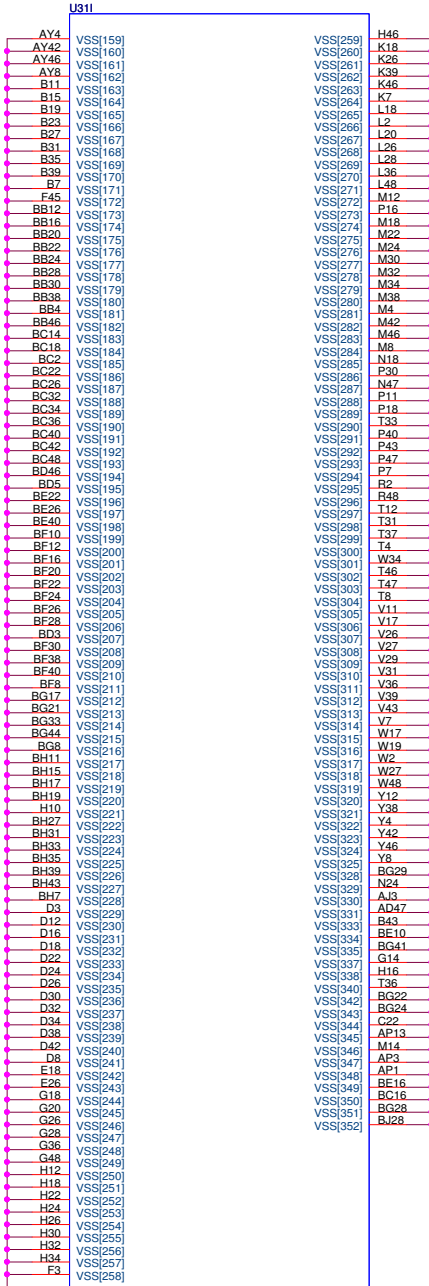
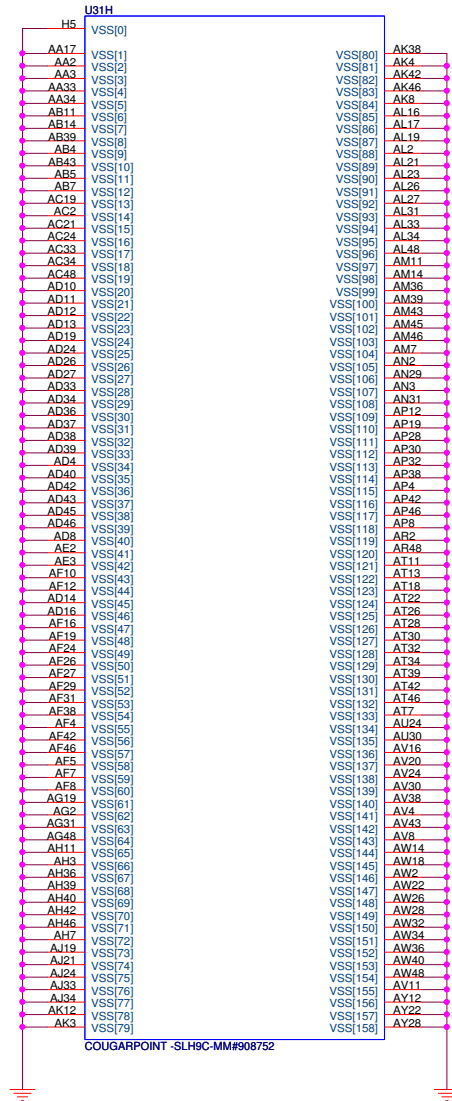
COUGAR POINT (POWER)




Cougar Point-M (POWER)

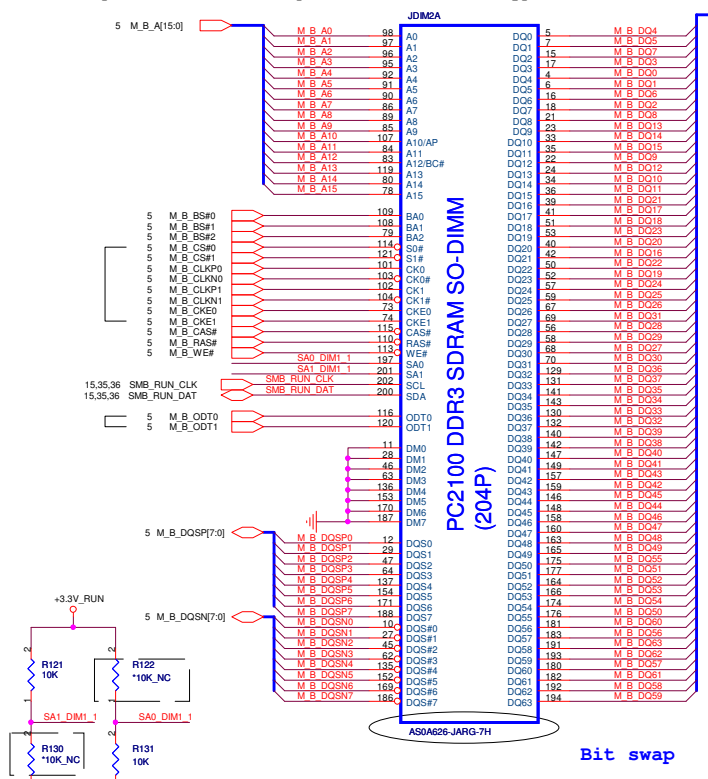


IBEX PEAK-M (GND)



 **Quanta Computer Inc.**
Project Name: **GM7C**

Title		PCH 6/6(GND)	
Size	Document Number	Rev	C
	GM7C_MB		
Date:	Friday, January 21, 2011	Sheet	13 of 59

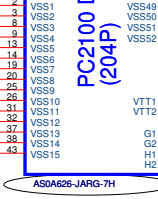
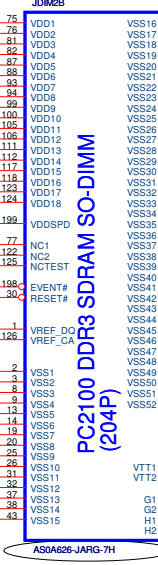
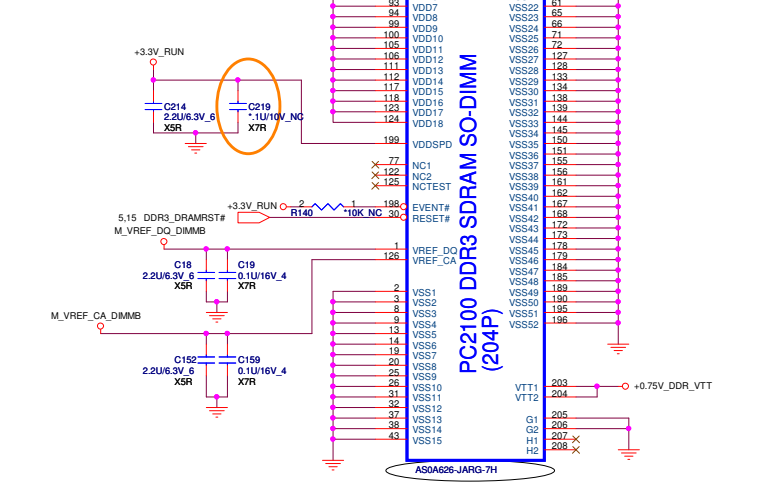


8 X01
0413>Add_DIS for SODIMM

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

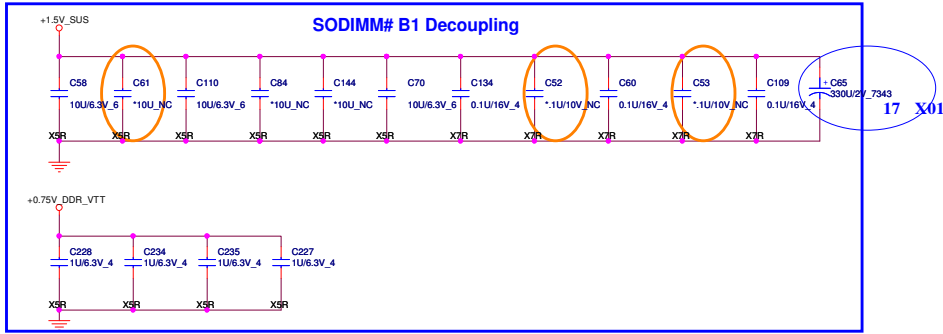
Note:
SO-DIMMA SPD Address is 0xA6
SO-DIMMA TS Address is 0x36

CHB_DIMM1_HEIGHT



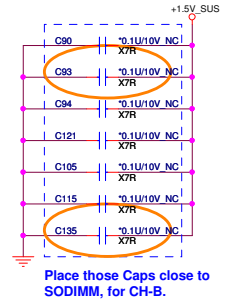
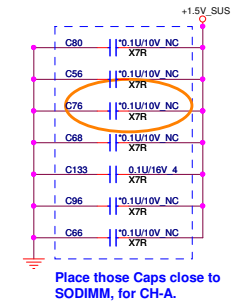
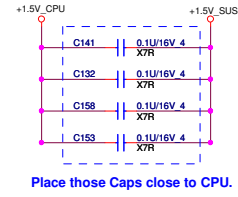
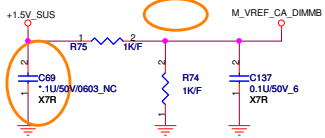
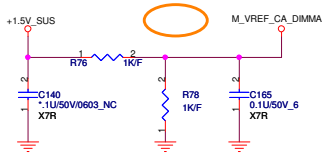
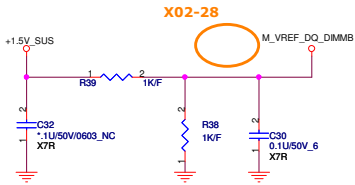
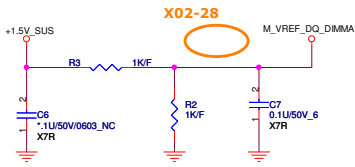
AS0A626-JARG-7H

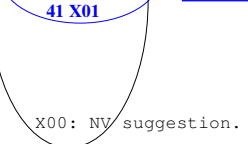
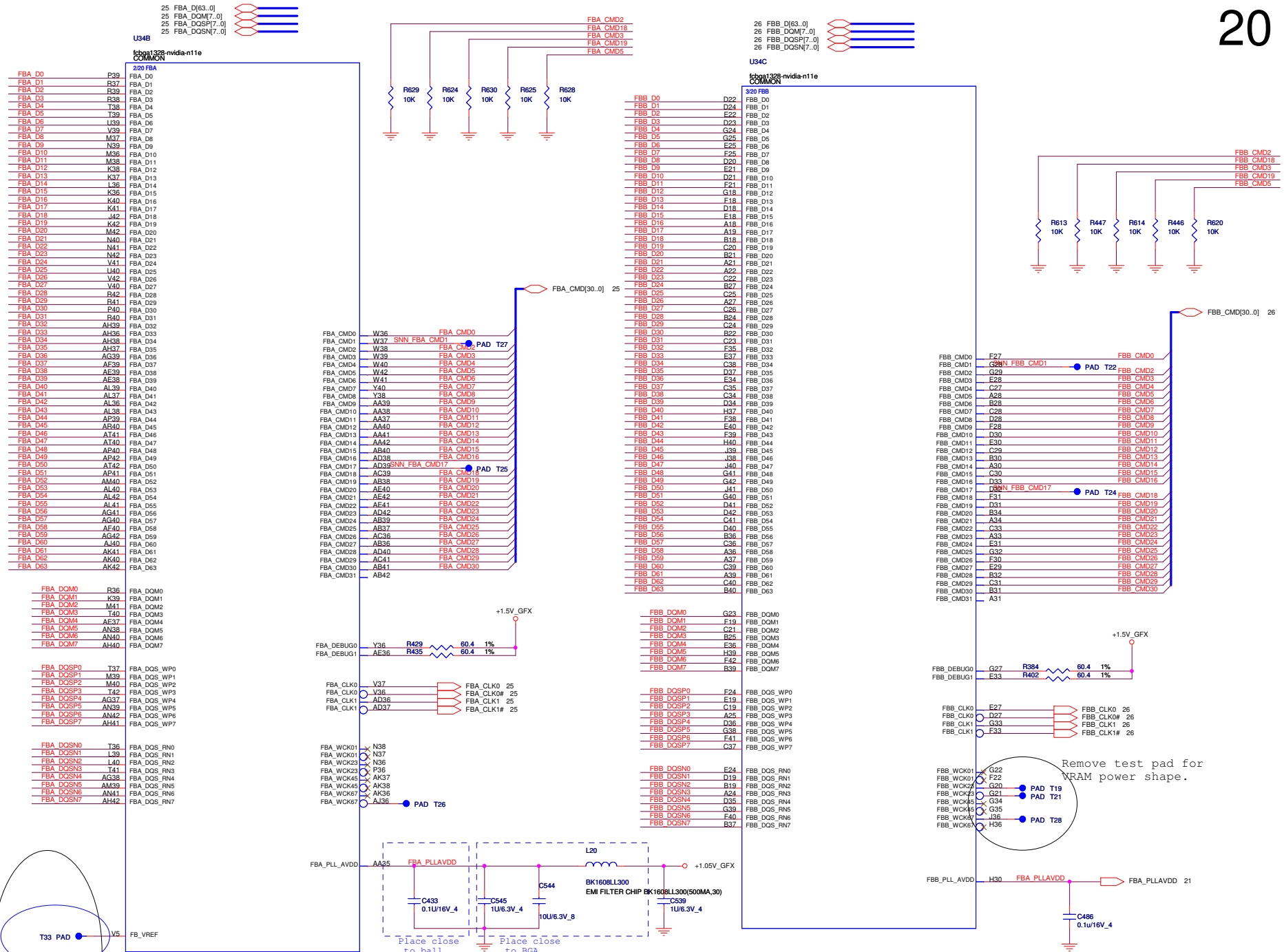
SODIMM# B1 Decoupling



17 X01

Fixed SO-DIMM VREF_DQ : M1 is default.

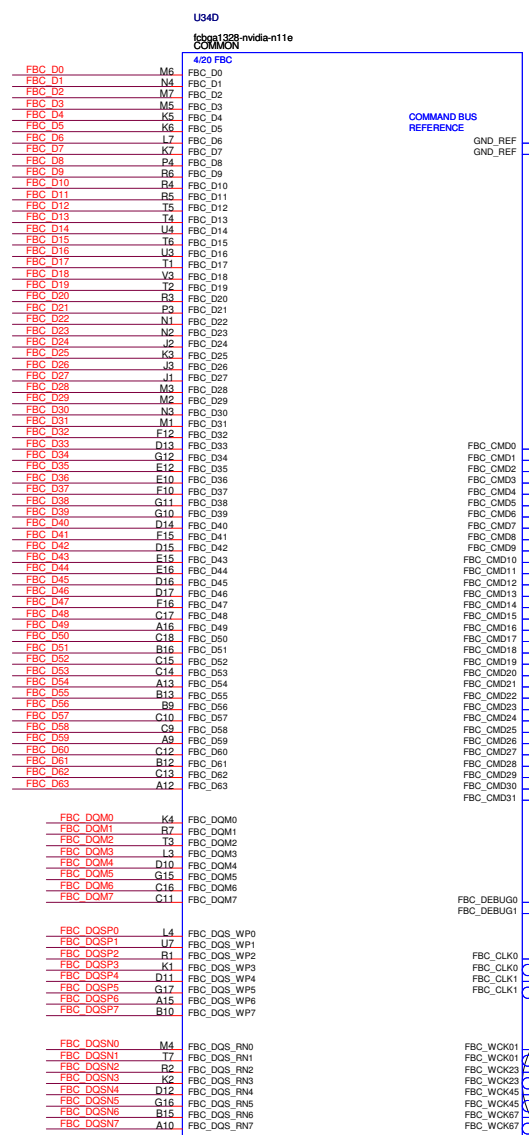




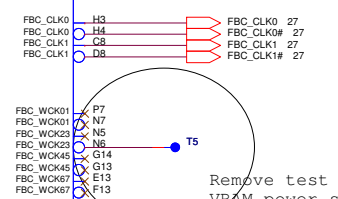
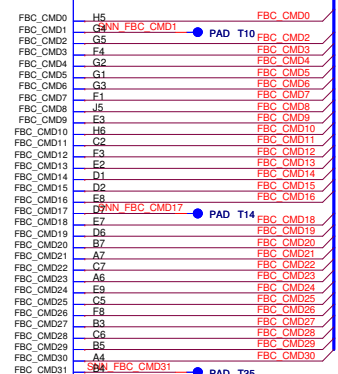
Quanta Computer Inc.
Project Name: **GM7C**

Title	N12E-GE (MEMORY I/F) 2/5		
Size	Document Number	GM7C_MB	Rev
Date:	Friday, January 21, 2011	Sheet	20 of 59

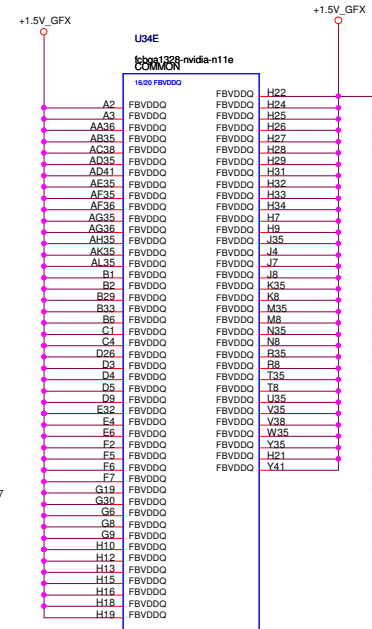
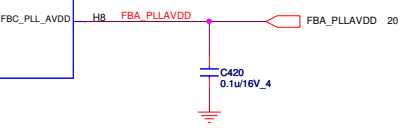
27 FBC_D[63..0]
27 FBC_DQM[7..0]
27 FBC_DQSP[7..0]
27 FBC_DQSN[7..0]



COMMAND BUS REFERENCE

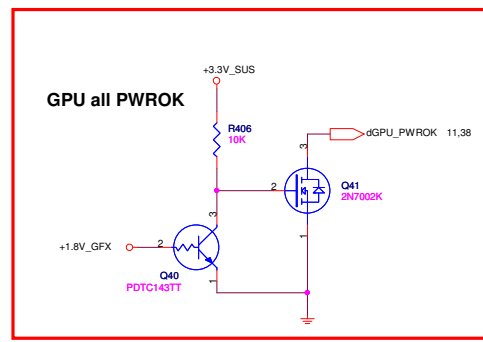
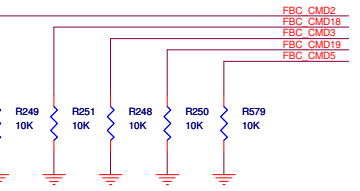


Remove test pad for VRAM power shape.



Place close to GPU balls

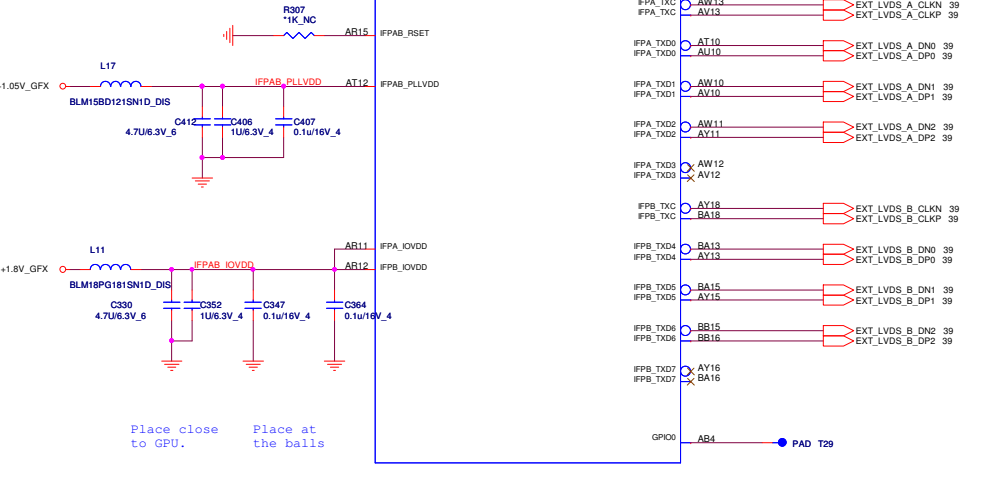
Place close to GPU



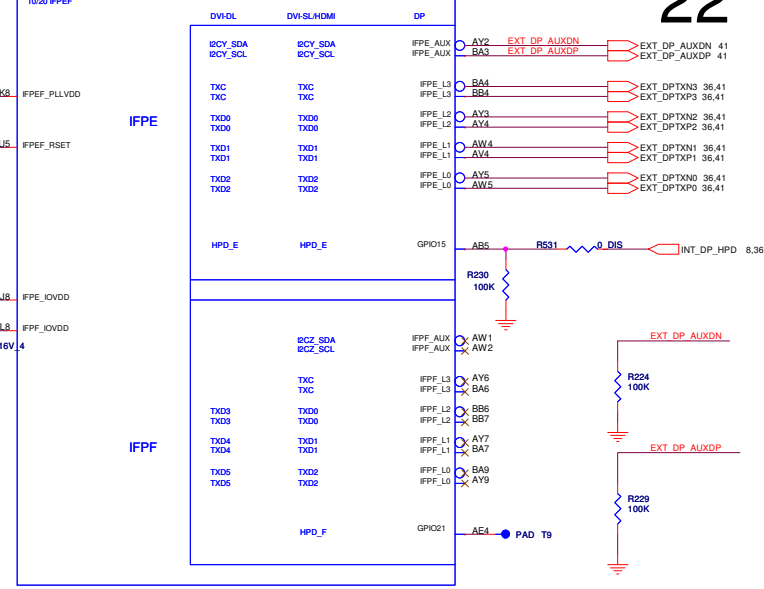
Quanta Computer Inc.
Project Name: **GM7C**

Title	N12E-GE (MEMORY I/F) 3/5		
Size	Document Number	GM7C_MB	Rev C
Date:	Friday, January 21, 2011	Sheet	21 of 59

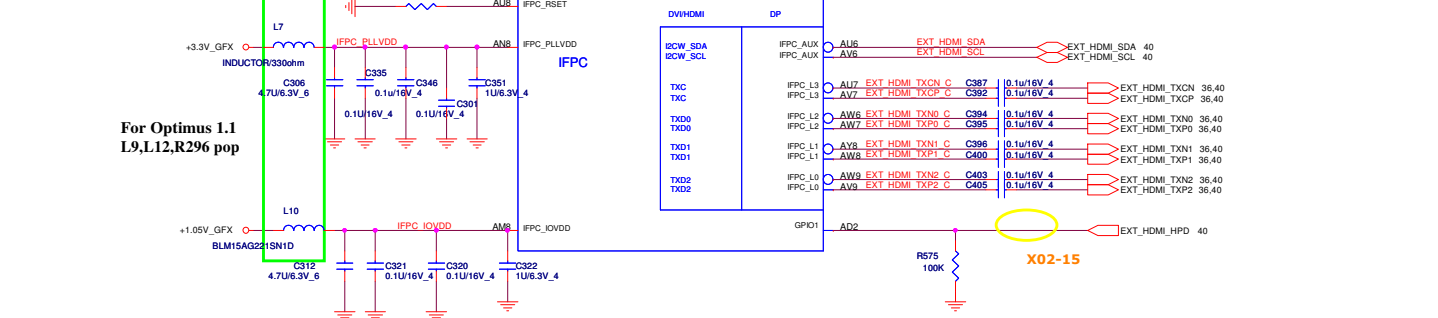
IFPA/B LVDS Dual Link



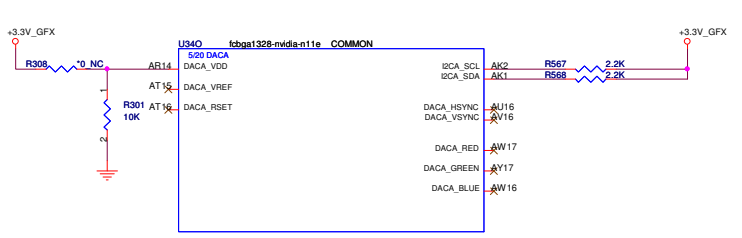
IFPE/F TMSD DVI-I



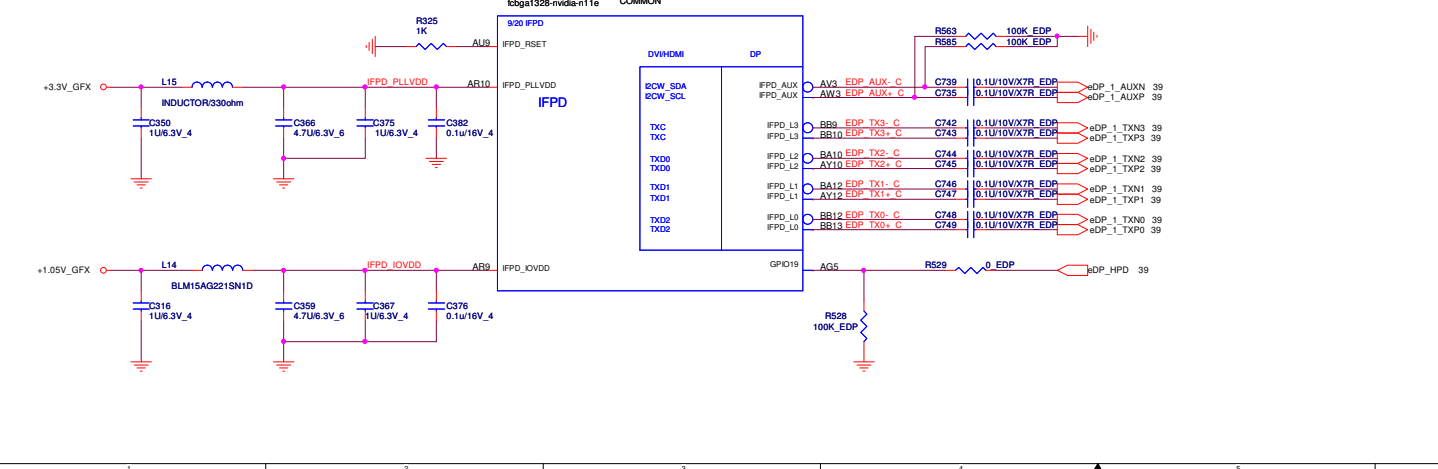
IFPC HDMI



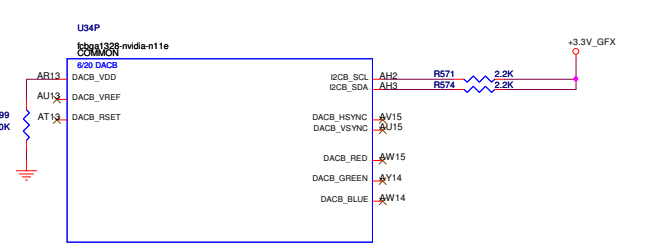
DAC_A VGA



IFPD DP (eDP)



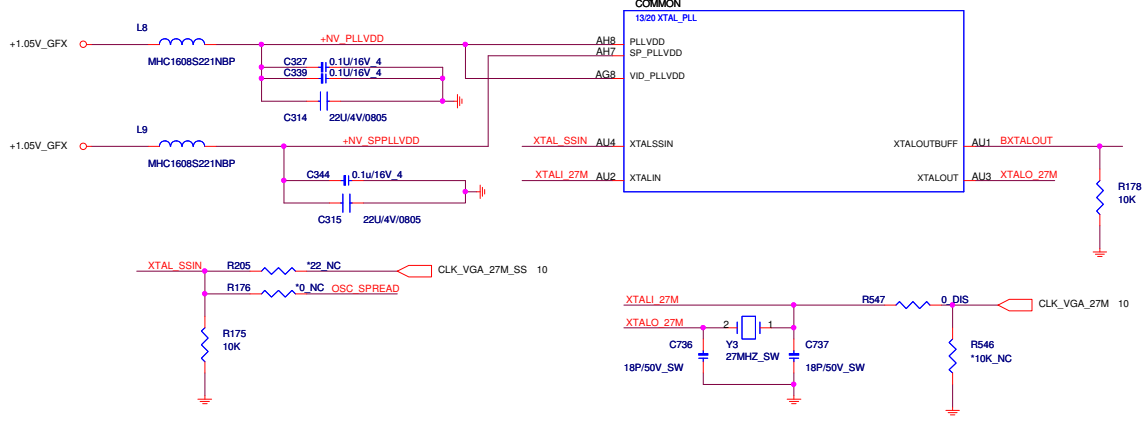
DAC_B Header



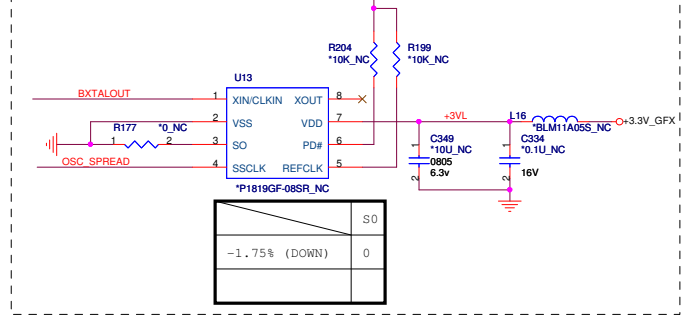
Quanta Computer Inc.
Project Name: **GM7C**

File: N12E-GE (DISPLAY) 4/5
Size: Document Number GM7C_MB
Date: Friday, January 21, 2011 Sheet 22 of 59

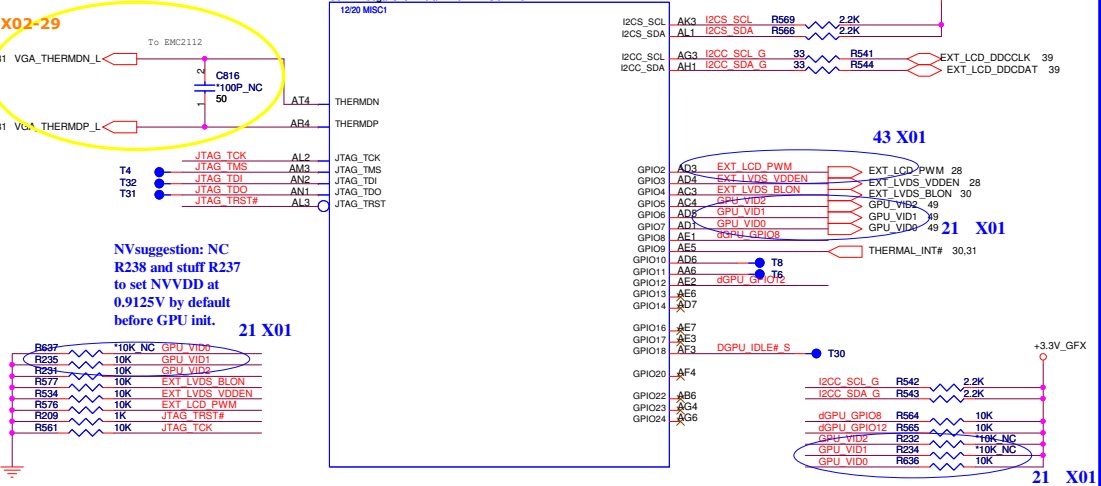
External SS



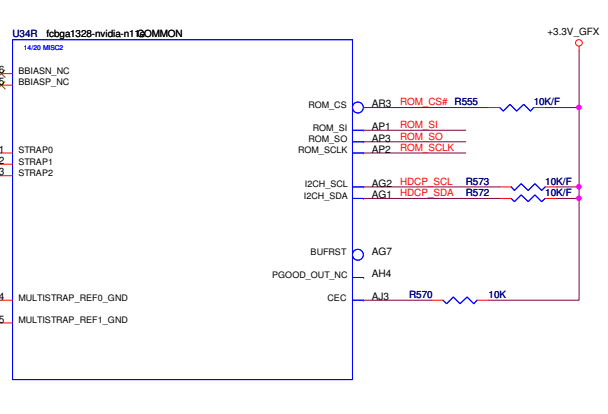
Spread Spectrum



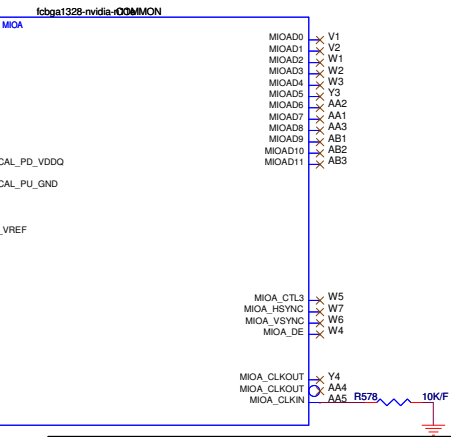
GPIOs, Thermal Sensor



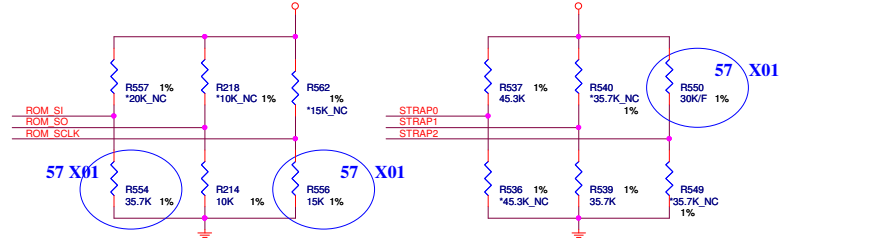
BIOS ROM



NVGEM and MIOA



Straps



Multi-Level Mode straps			
		PU	PD
N12E-GE-B	STRAP2	30K	
	ROM_SCLK		15K
N12E-GE-B-LP	STRAP2		35K
	ROM_SCLK	15K	
Hynix 128Mx16	ROM_SI		35K
Hynix 64Mx16	ROM_SI		15K
Samsung 128Mx16	ROM_SI		45K
Samsung 64Mx16	ROM_SI		20K

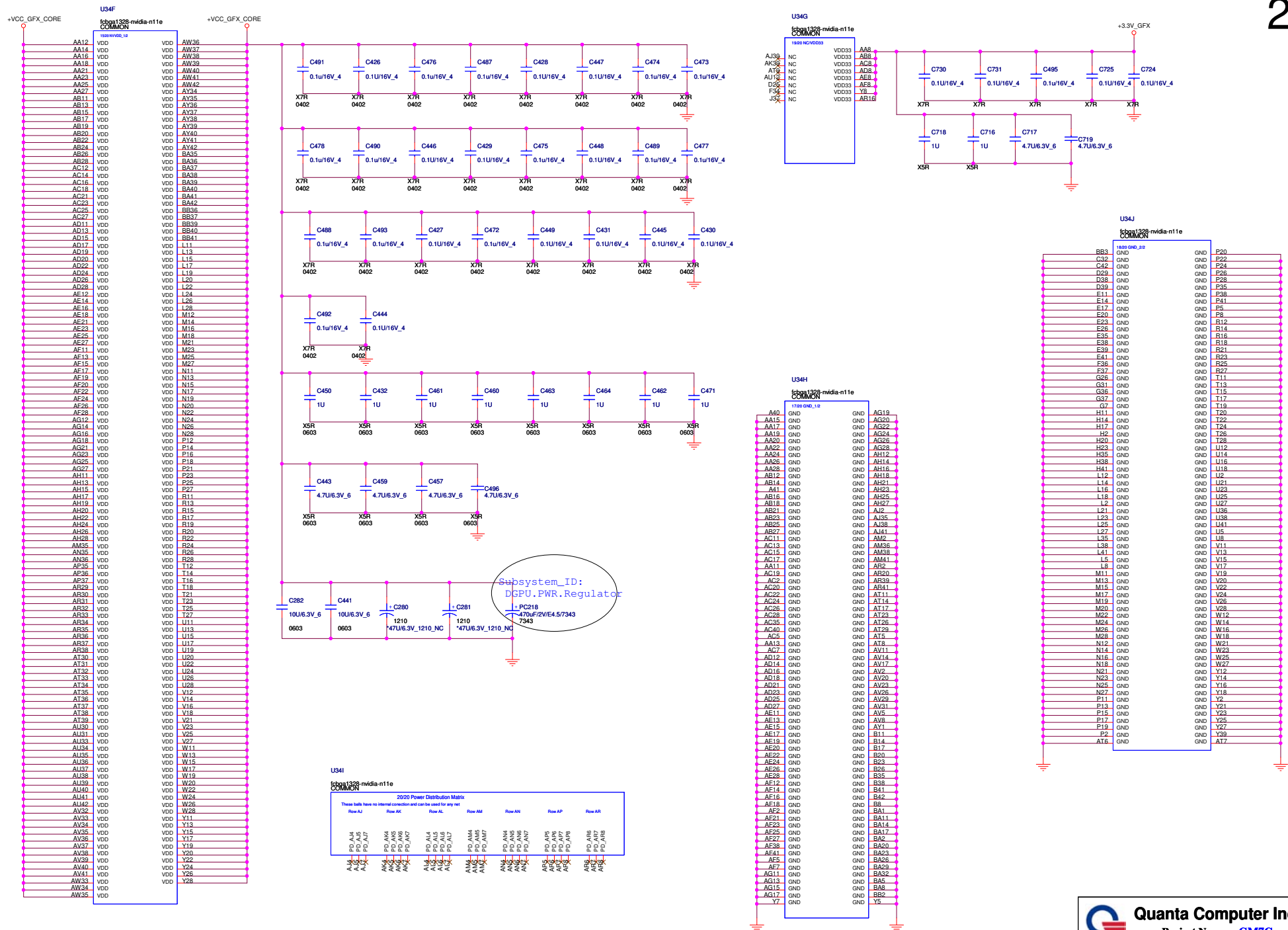
Strapping Resistor Value Decode

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Strap Pin Mode Table	
Pin Name	Multi-Level Bit [3:0]
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG[3:0]
STRAP2	PCI_DEVID[3:0]
ROM_SCLK	PCI_DEVID[4] SUB_VENDOR SLOT_CLK PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3:0]
ROM_SO	XCLK_417 FB_0_BAR_SIZE SMB_ALT_ADDR VGA_DEVICE

Quanta Computer Inc.
Project Name: **GM7C**

Title	N12E-GE(GPIO&STRAPS) 5/5		
Size	Document Number	GM7C_MB	Rev C
Date:	Friday, January 21, 2011	Sheet	23 of 59

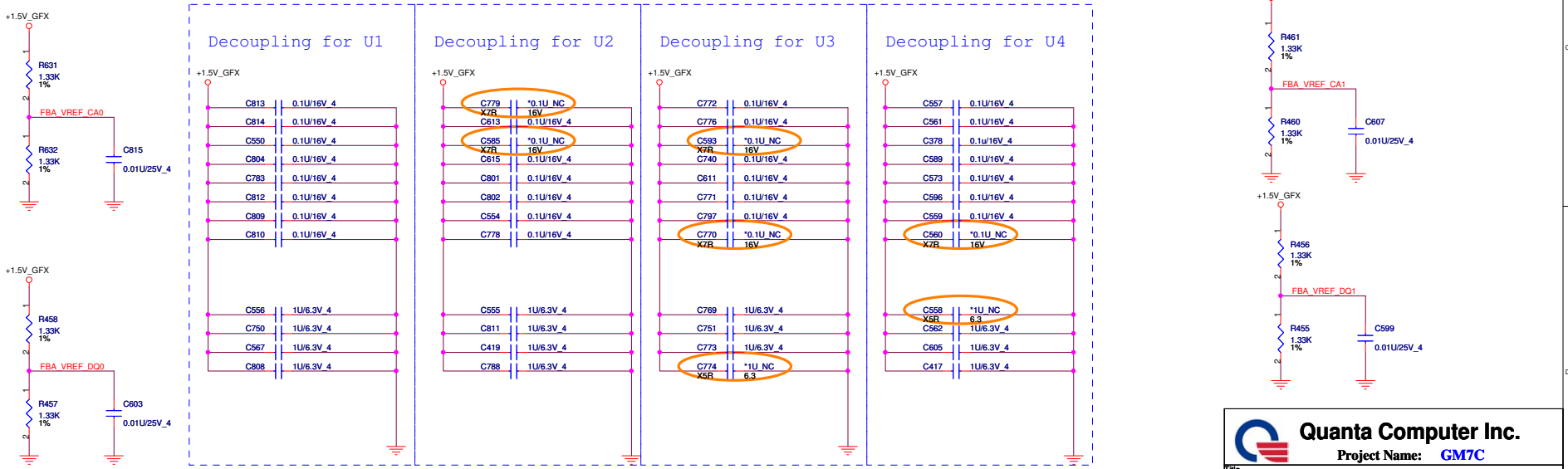
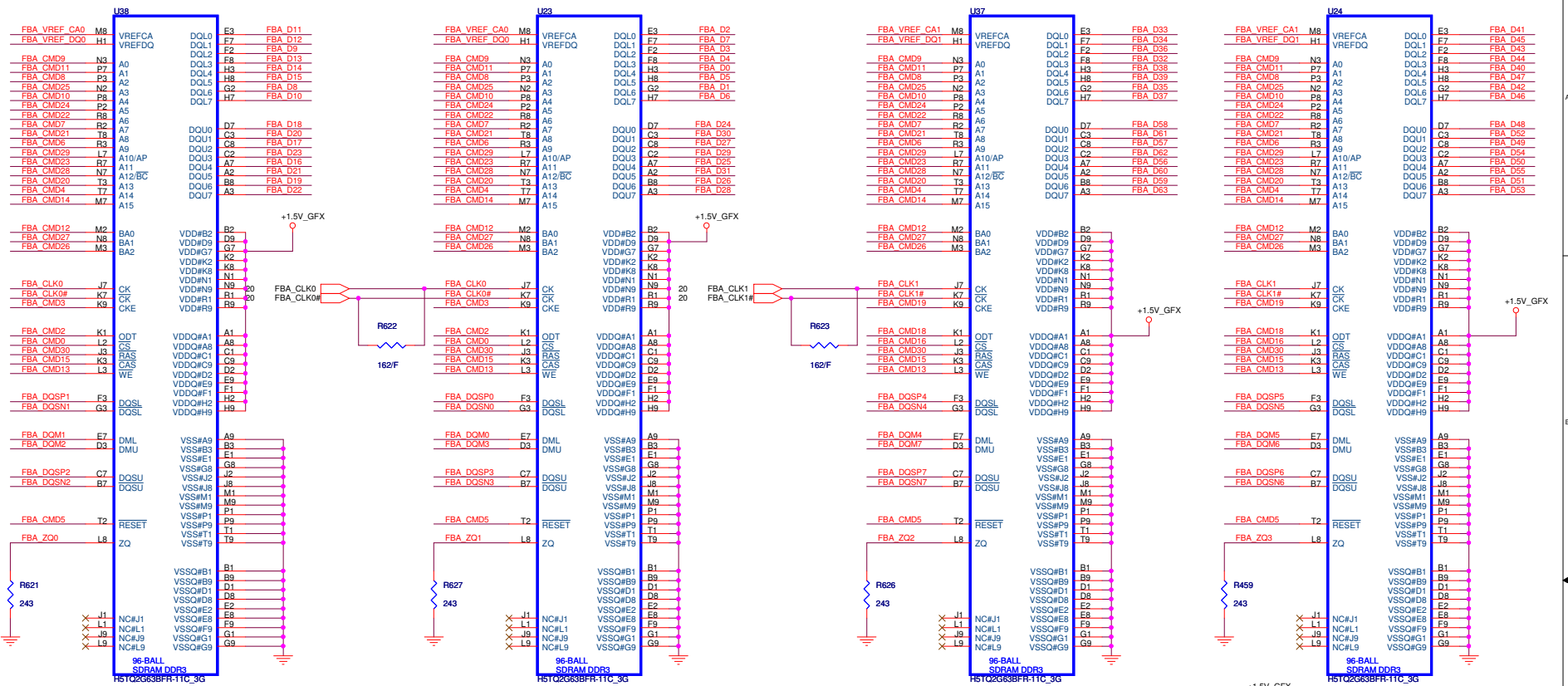


20 FBA_CMD30[30..0]
 20 FBA_D163[0..7]
 20 FBA_DQM[7..0]
 20 FBA_DQS1[7..0]
 20 FBA_DQSN[7..0]

Memory Lower Partition A

Memory Upper Partition A

25



For 128 bit, Partition A don't need to mount

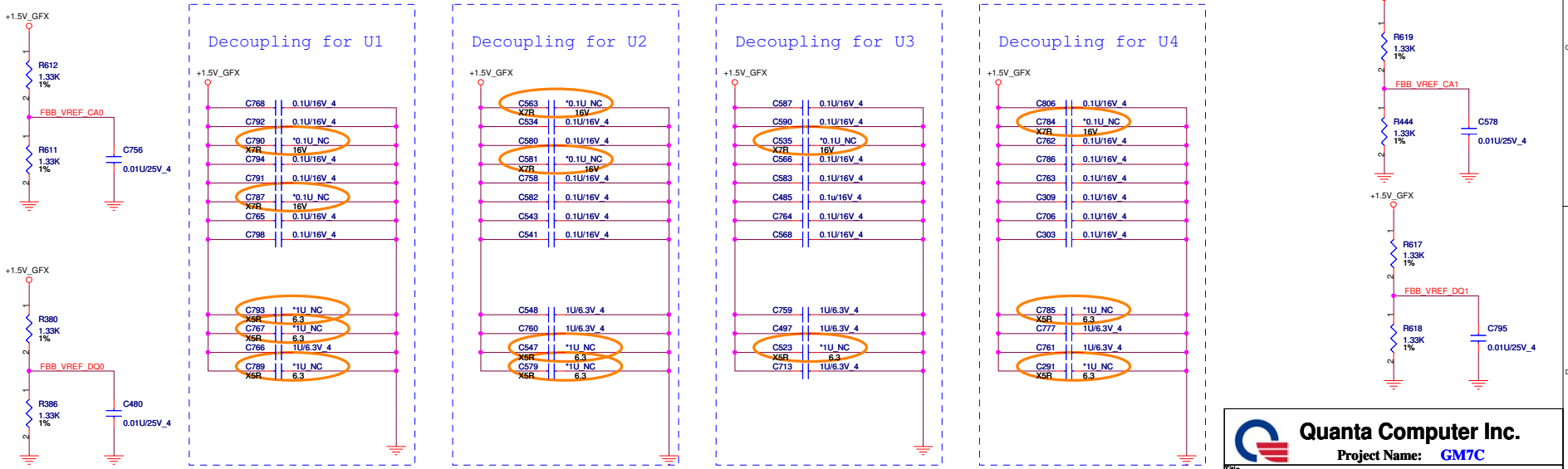
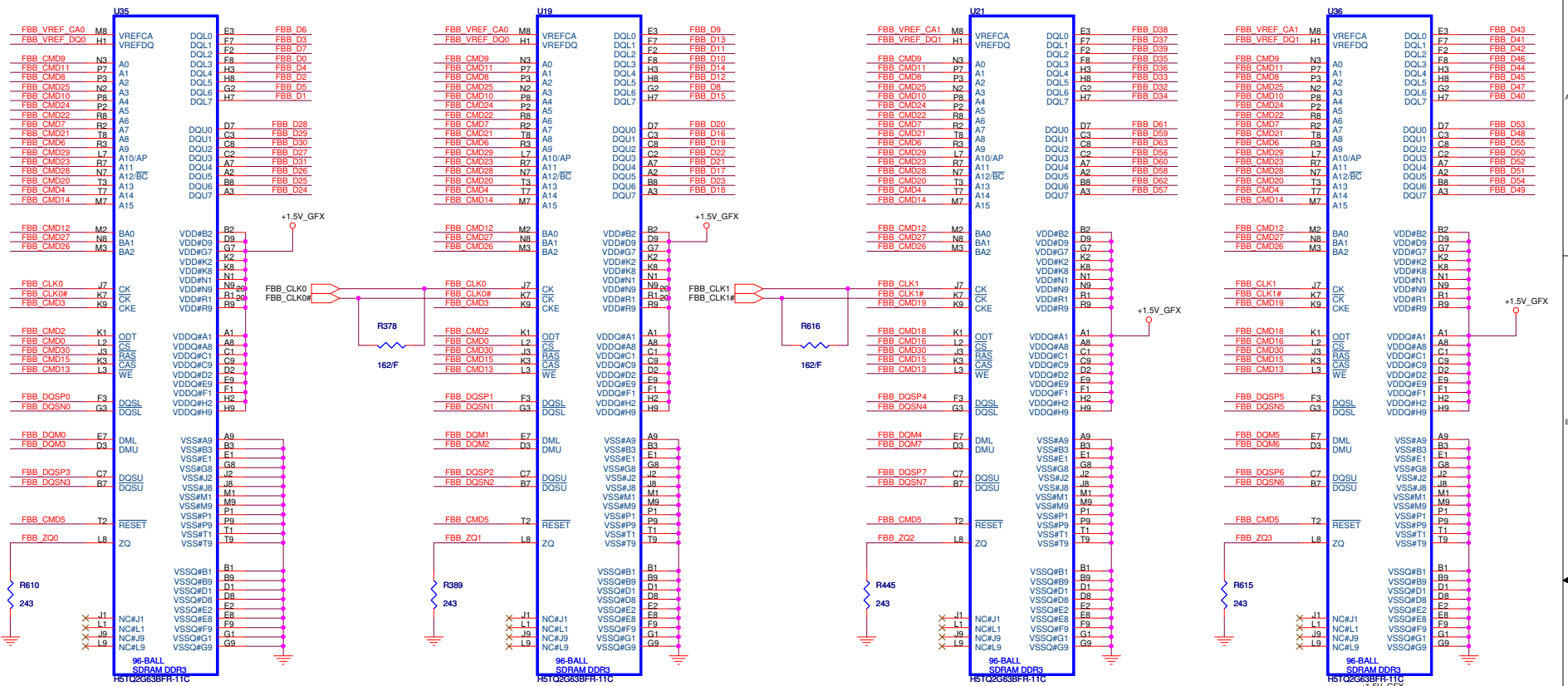
Quanta Computer Inc.
 Project Name: **GM7C**

File: N12E-GE VRAM_Partition A
 Size: Document Number GM7C_MB Rev C
 Date: Friday, January 21, 2011 Sheet 25 of 59

20 FBB_CMD30[0..7]
 20 FBB_D163[0..7]
 20 FBB_DCM[7..0]
 20 FBB_DCSN[7..0]
 20 FBB_DCSN[7..0]

Memory Lower Partition B

Memory Upper Partition B



Quanta Computer Inc.
 Project Name: **GM7C**

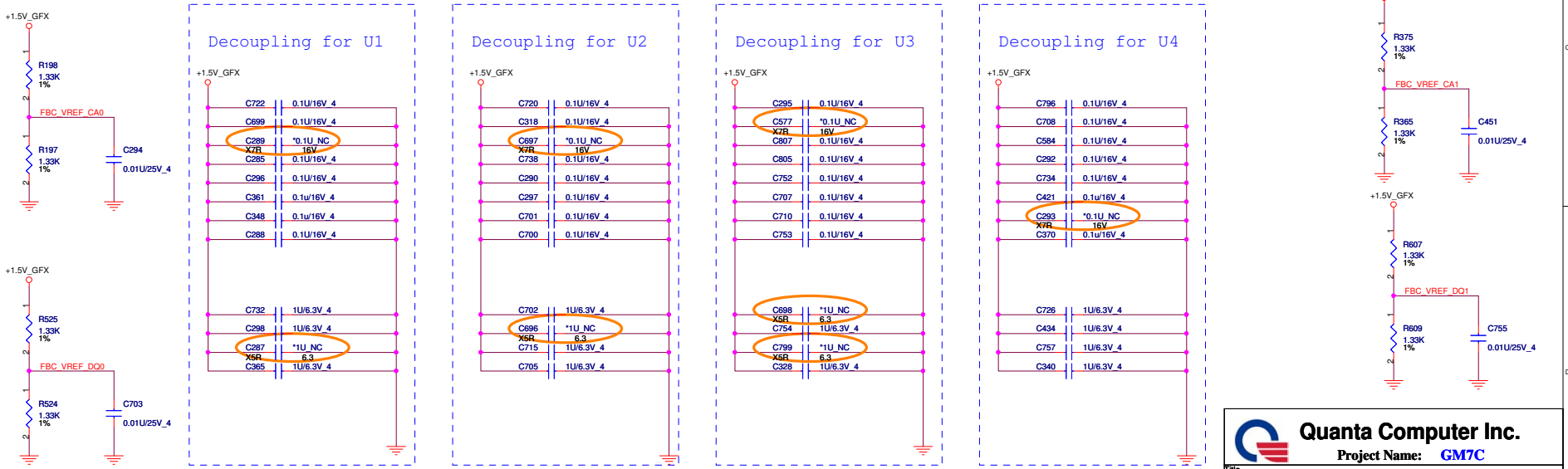
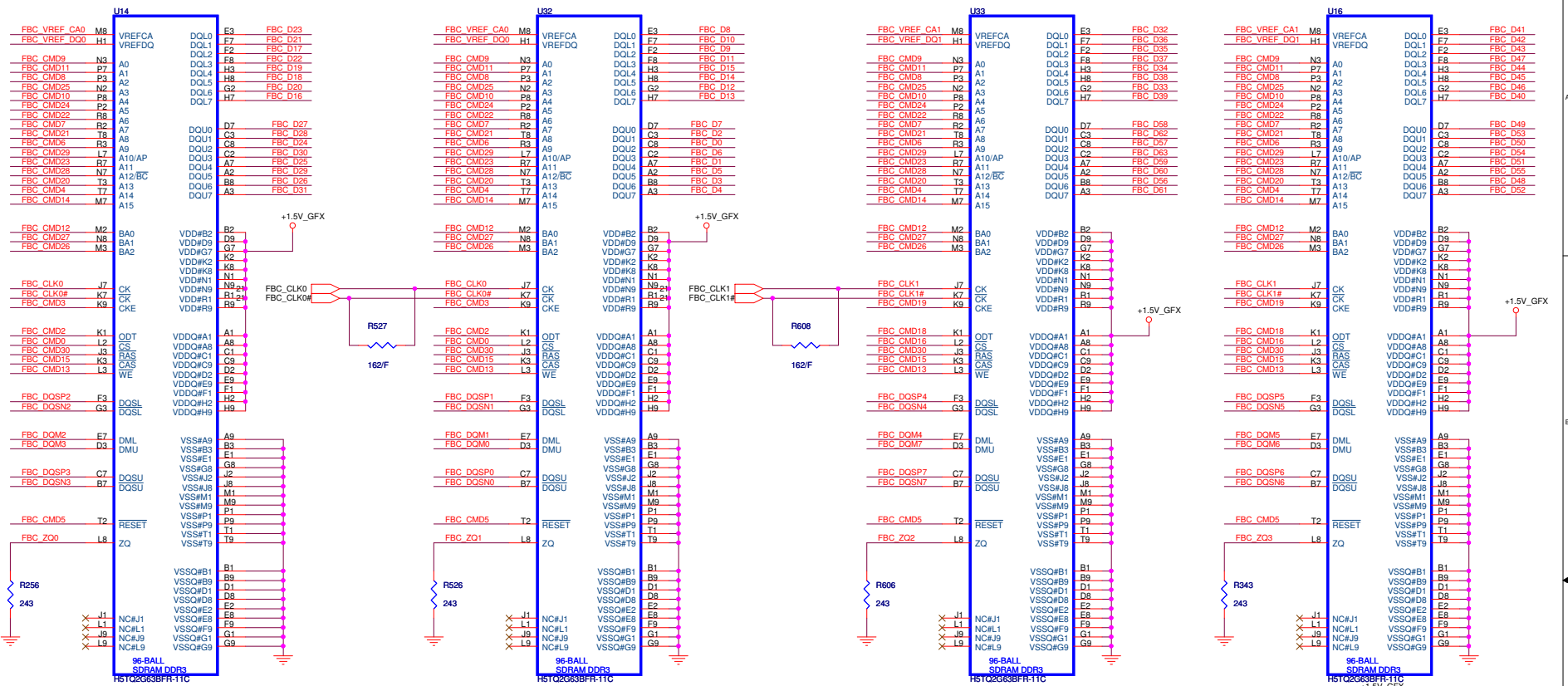
File	N12E-GE VRAM_Partition B	
Size	Document Number	Rev
	GM7C_MB	C
Date:	Friday, January 21, 2011	Sheet 26 of 59

21 FBC_CMD30[30..0]
21 FBC_DI63[0]
21 FBC_DQM[7..0]
21 FBC_DQSP[7..0]
21 FBC_DQSN[7..0]

Memory Lower Partition C

Memory Upper Partition C

27

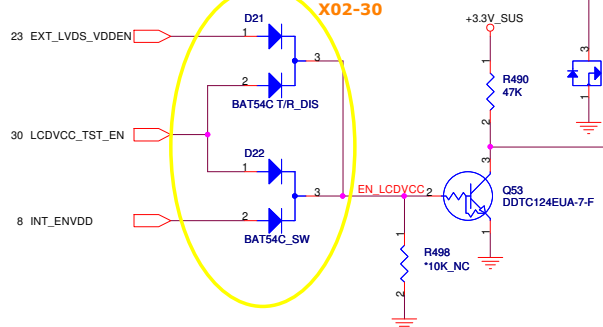


Quanta Computer Inc.
Project Name: **GM7C**

File	N12E-GE VRAM_Partition C		
Size	Document Number	GM7C_MB	Rev C
Date:	Friday, January 21, 2011	Sheet	27 of 59

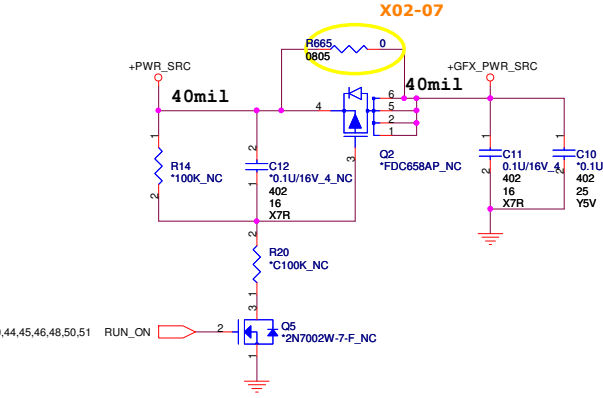
Panel VCC

Support the new imbedded diagnostics.

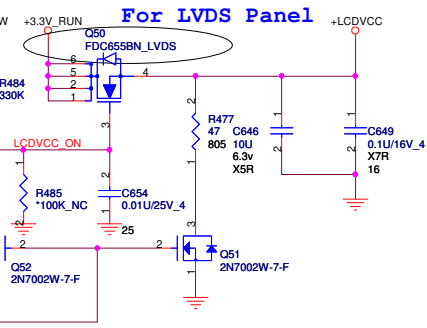


X02-30

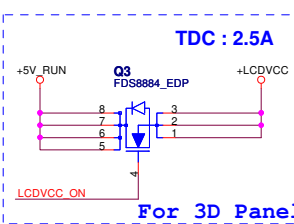
X02-07



For LVDS Panel

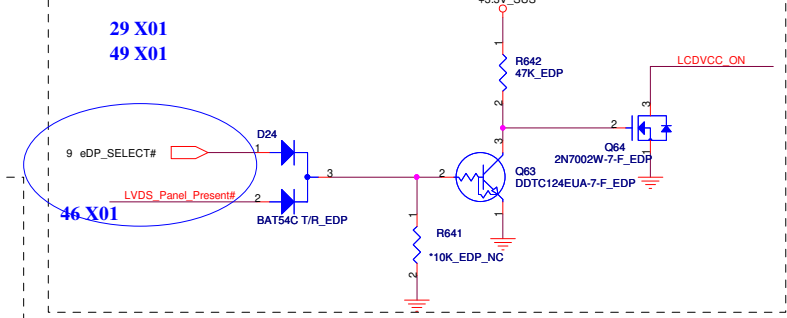


TDC : 2.5A



For 3D Panel

LCDVCC voltage protection circuit for LVDS Panel



29 X01
49 X01

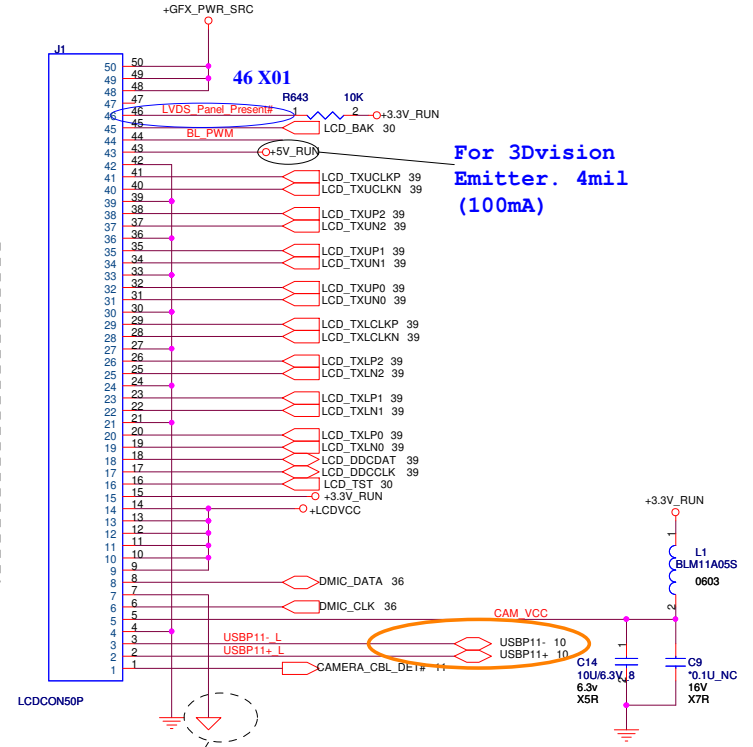
46 X01

EMC Reserve 30 X01

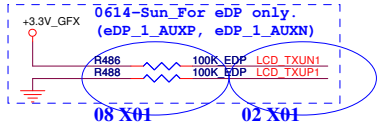
LCD_TXLP0	C817	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXLN0
LCD_TXLP1	C818	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXLN1
LCD_TXLP2	C820	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXLN2
LCD_TXLCLKP	C819	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXLCLKN
LCD_TXUP0	C824	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXUN0
LCD_TXUP1	C821	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXUN1
LCD_TXUP2	C822	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXUN2
LCD_TXUCLKP	C823	2	1	*3.3P/50V/NPO LVDS_NC	LCD_TXUCLKN

Please R close to pin of LCD connector, J1

50Pin LVDS & Array Microphone & Camera Connector



For 3Dvision Emitter. 4mil (100mA)

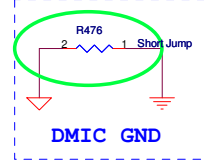


0614-Sun_For eDP only. (eDP 1 AUXP, eDP 1 AUXN)

08 X01

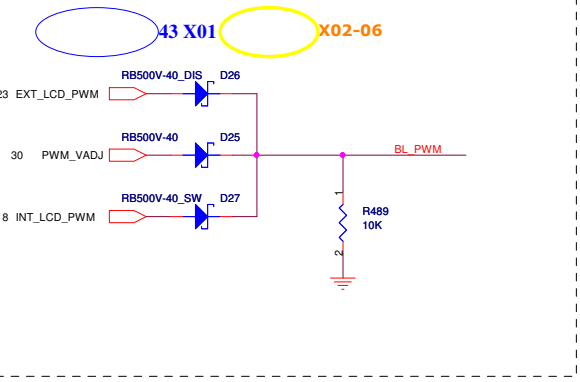
02 X01

16



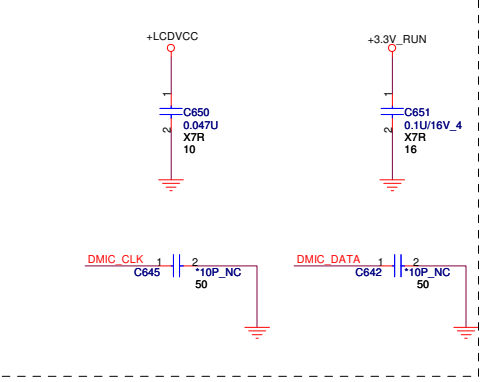
DMIC GND

Backlight Control



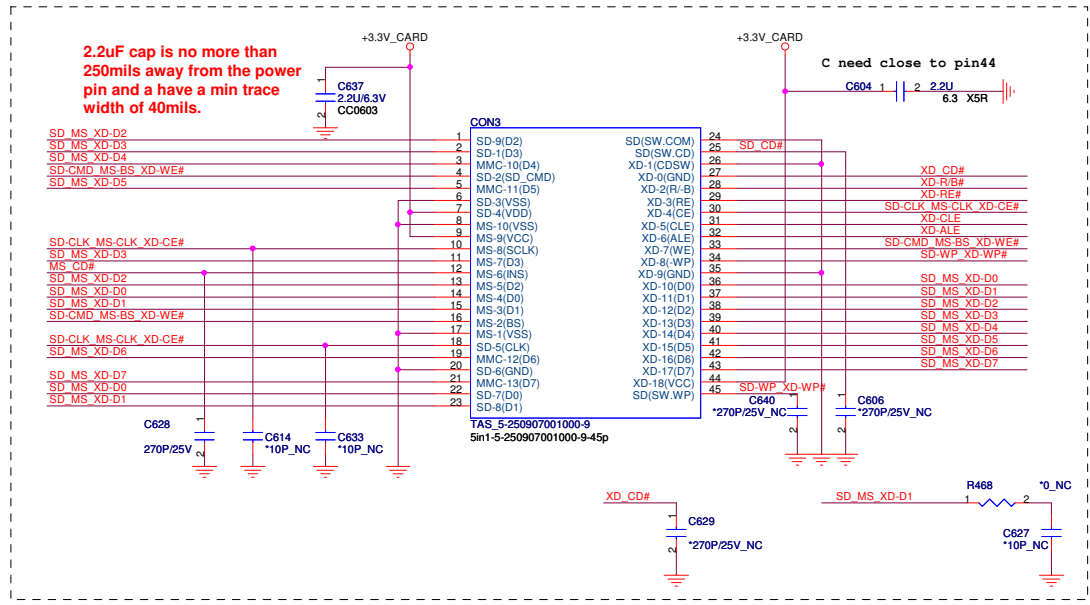
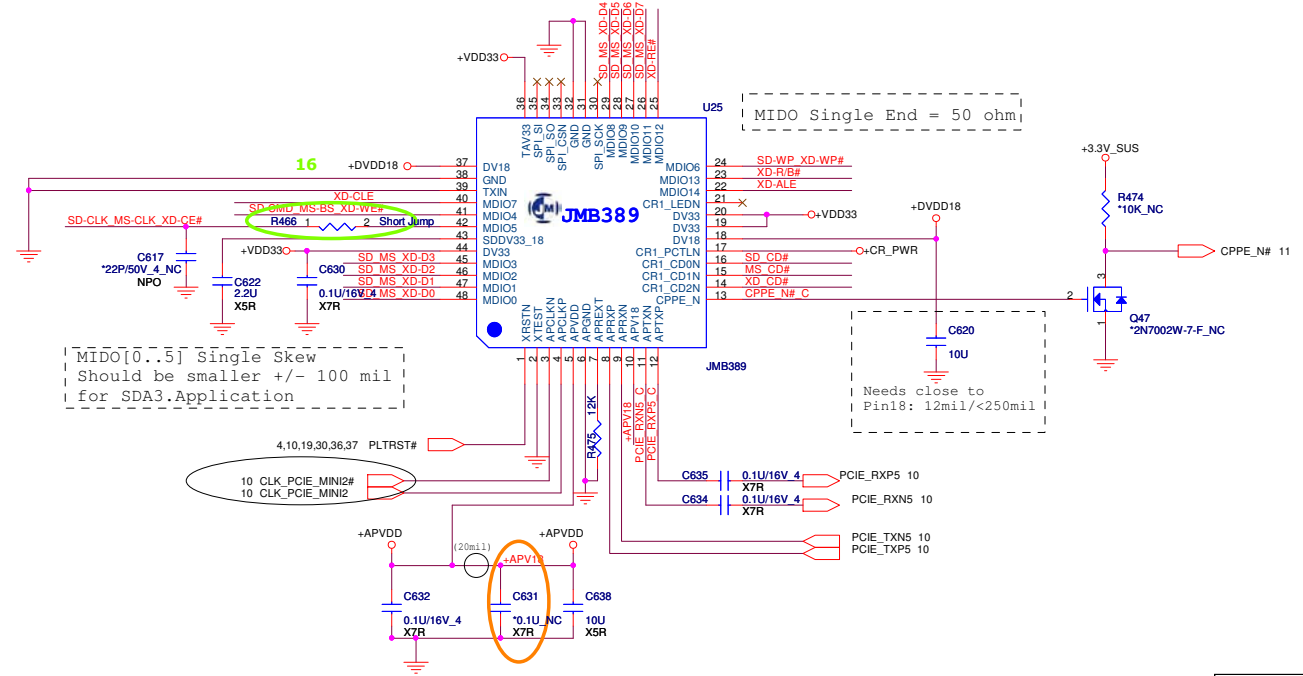
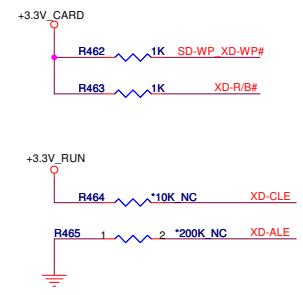
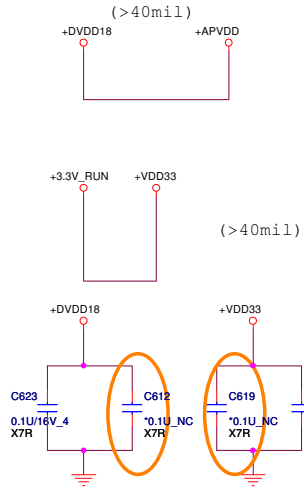
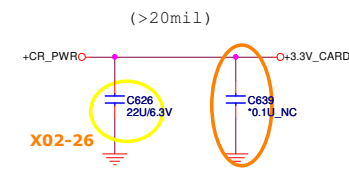
43 X01

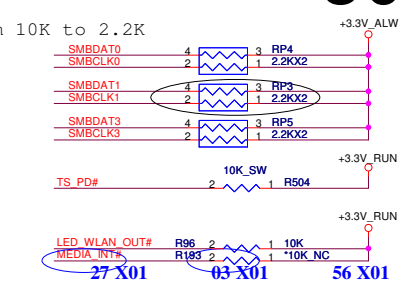
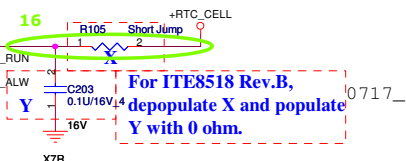
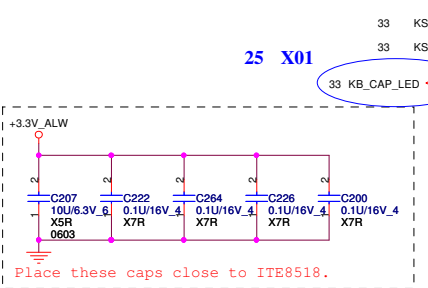
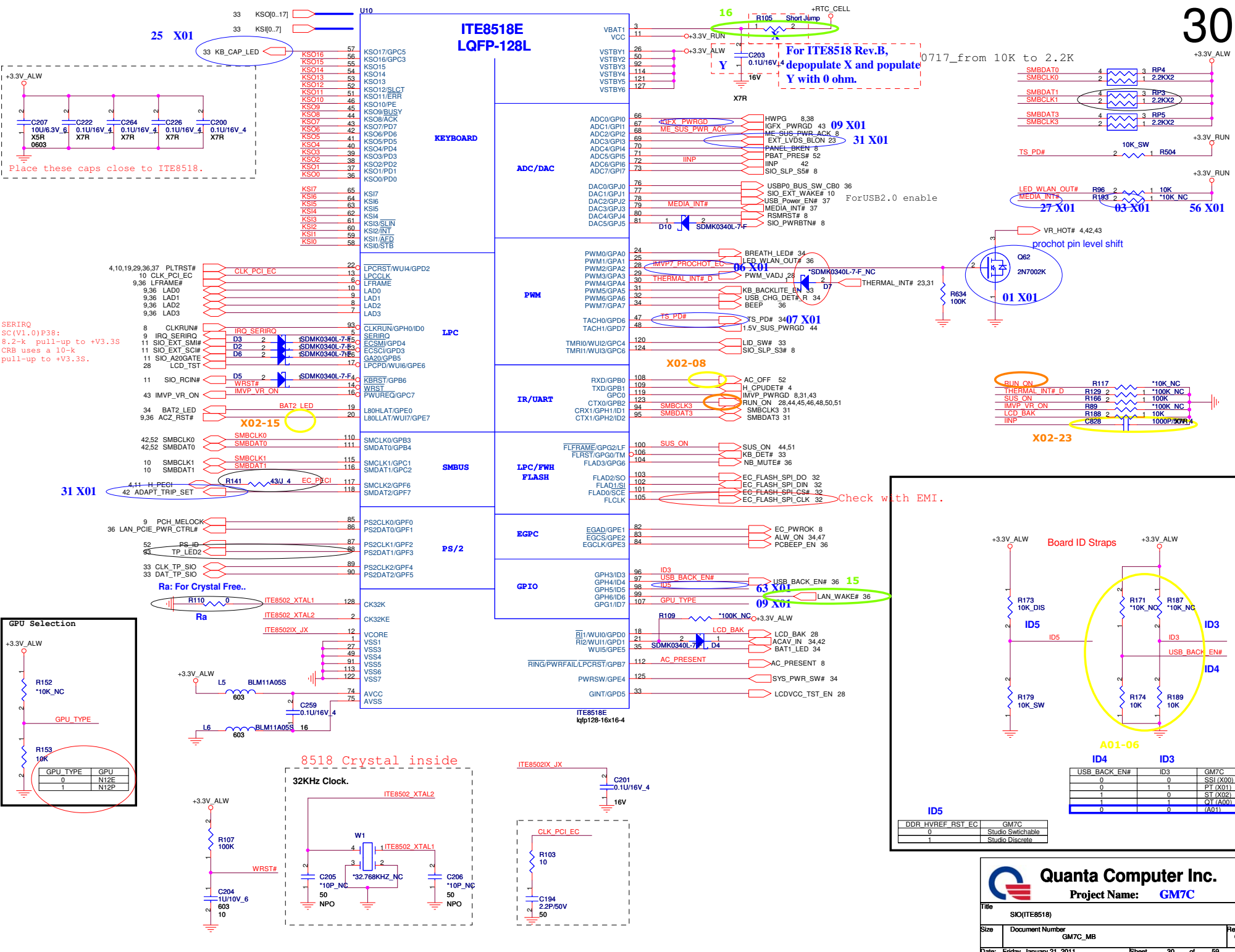
X02-06



Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MD1000	SD/MMC/MS/XD	SD_D0	MS_D0	XD_D0
MD1001		SD_D1	MS_D1	XD_D1
MD1002		SD_D2	MS_D2	XD_D2
MD1003		SD_D3	MS_D3	XD_D3
MD1004		SD_CMD	MS_BS	XD_WE#
MD1005		SD_CLK	MS_CLK	XD_CE#
MD1006		SD_WP		XD_WP#
MD1007				XD_CLE
MD1008		MMC_D4	MS_D4	XD_D4
MD1009		MMC_D5	MS_D5	XD_D5
MD1010		MMC_D6	MS_D6	XD_D6
MD1011		MMC_D7	MS_D7	XD_D7
MD1012				XD_RE#
MD1013				XD_R/B#
MD1014				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1				
CR1_CD2				XD_CD#



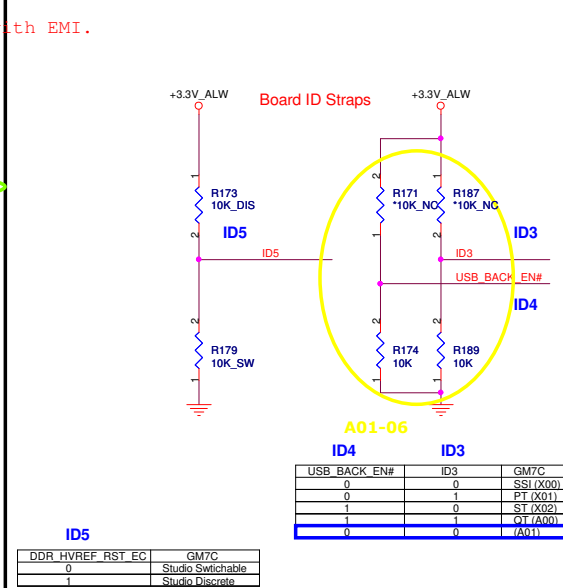
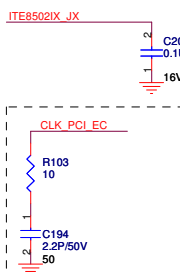
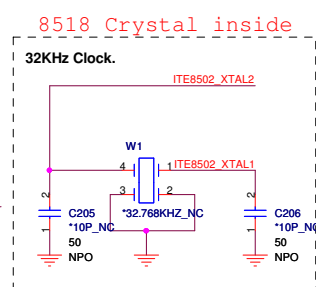
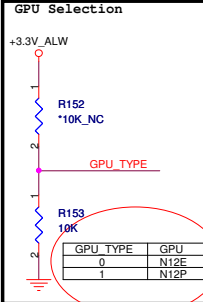
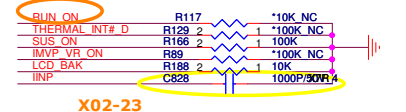


SERIRQ

SC(V1.0)P38:

8.2-k pull-up to +V3.3S

CRB uses a 10-k pull-up to +V3.3S.



Quanta Computer Inc.

Project Name: **GM7C**

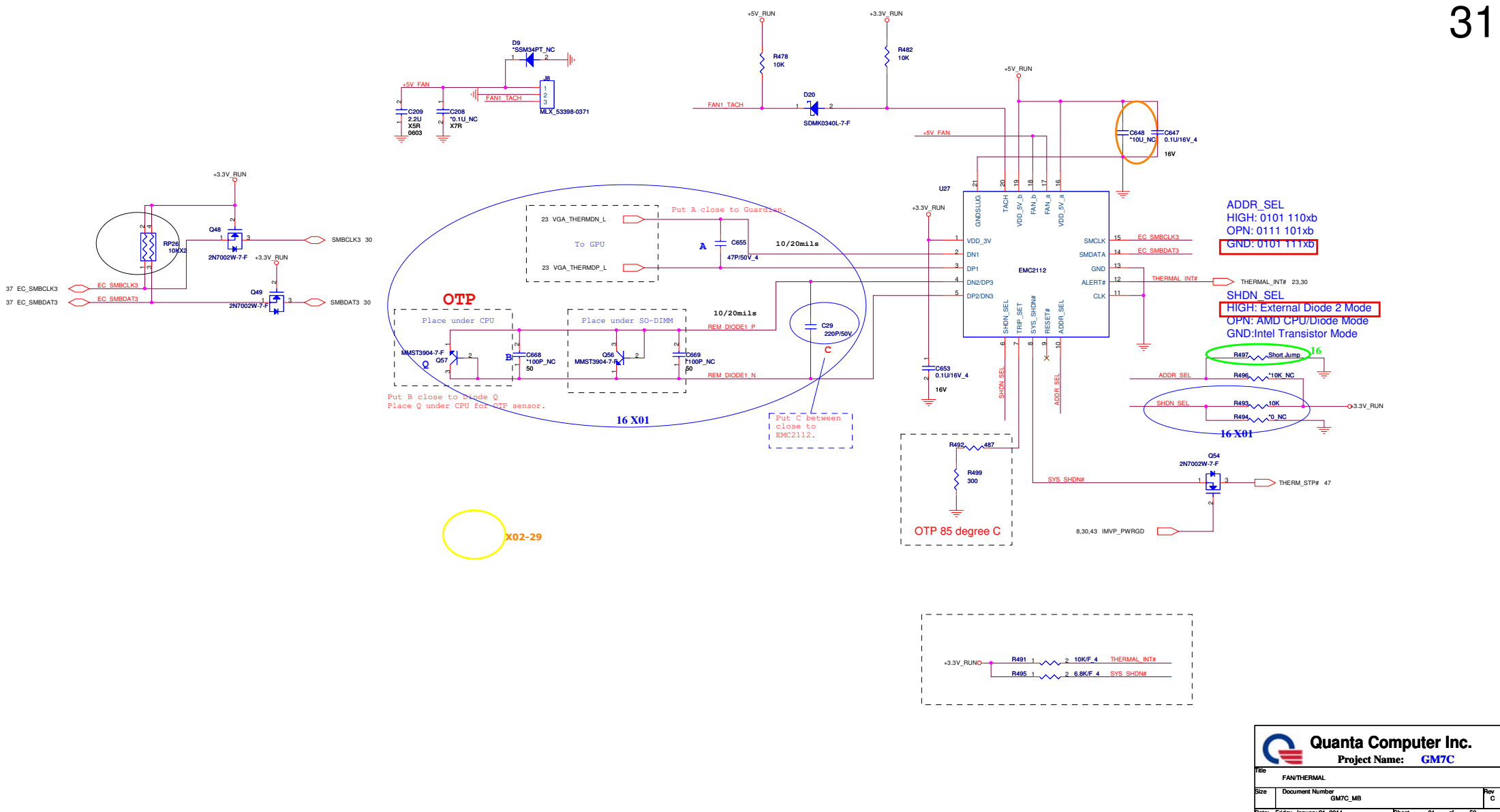
Title: **SIO(ITE8518)**

Size: **Document Number GM7C_MB**

Date: **Friday, January 21, 2011**

Sheet **30** of **59**

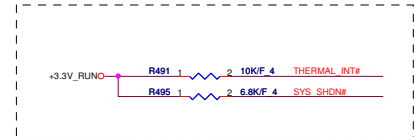
Rev **C**



ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb

SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND: Intel Transistor Mode

R497 Short Jump 16

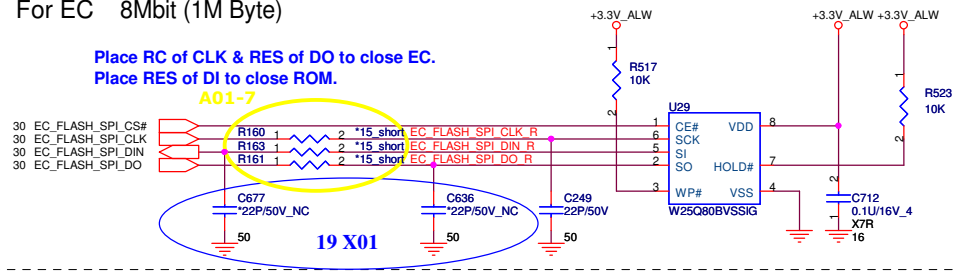


Quanta Computer Inc. Project Name: GM7C	
File	FAN/THERMAL
Size	Document Number GM7C_MB
Date	Friday, January 21, 2011
Sheet	31 of 59

For EC 8Mbit (1M Byte)

Place RC of CLK & RES of DO to close EC.
Place RES of DI to close ROM.

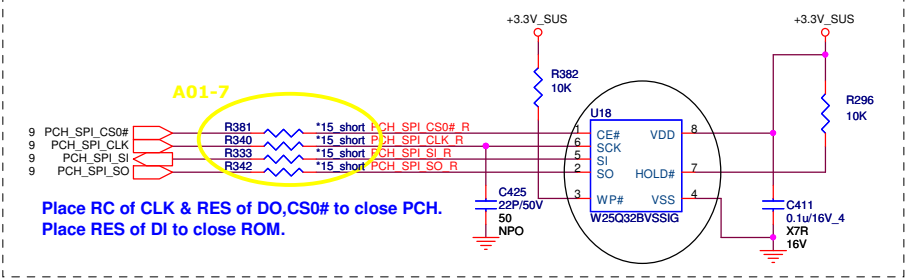
A01-7



For PCH 32Mbit (4M Byte)

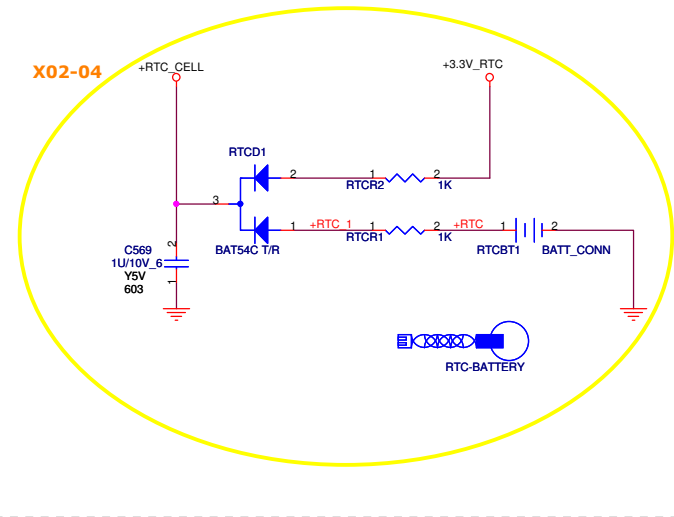
Place RC of CLK & RES of DO,CS0# to close PCH.
Place RES of DI to close ROM.

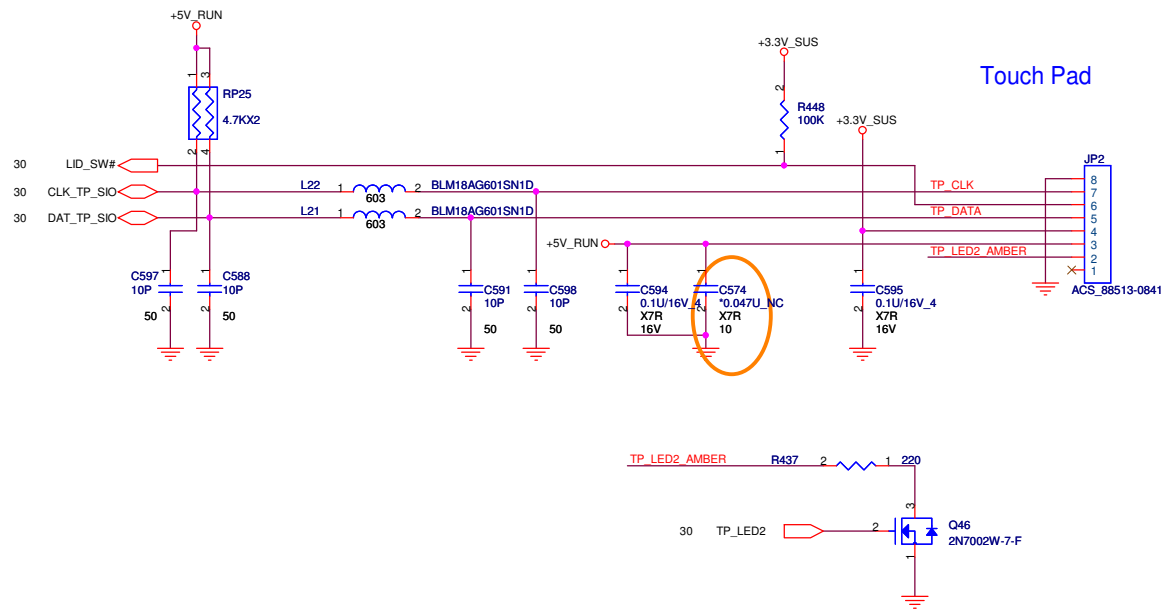
A01-7



RTC BATTERY

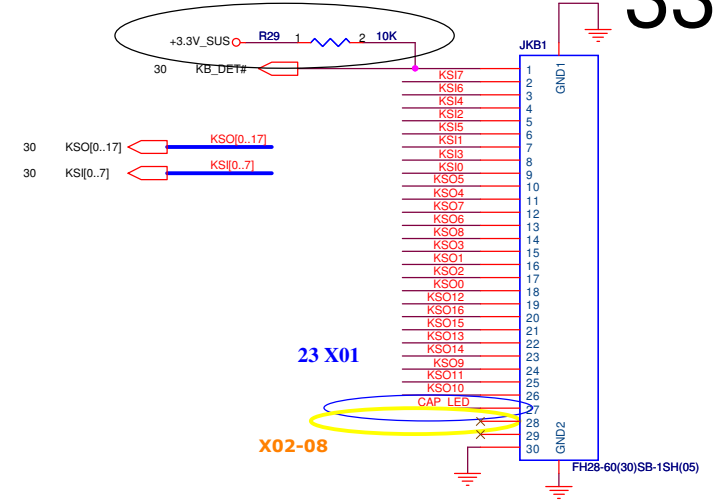
X02-04



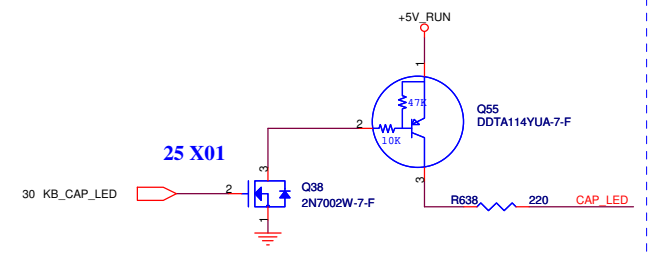


KEYBOARD CONNECTOR

33

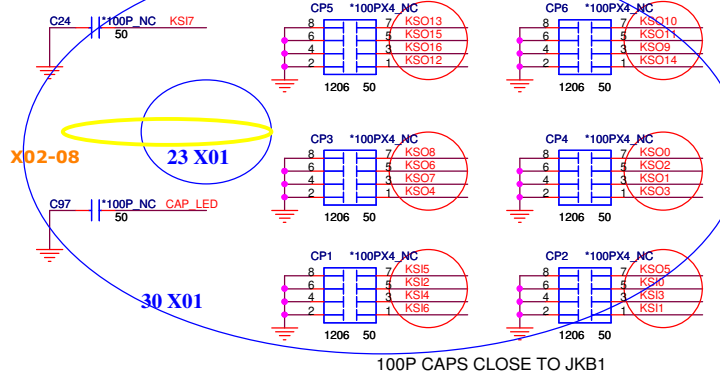
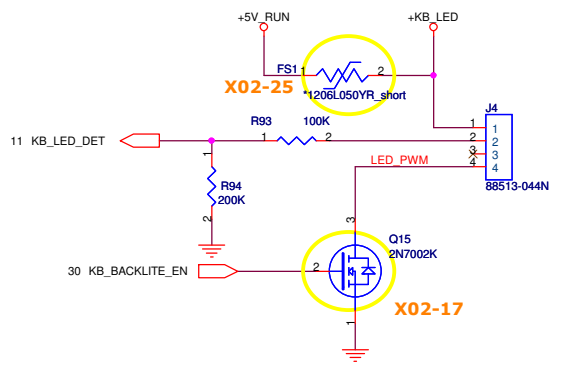


Cap_Lock WLED for GM7C.



Key board illumination

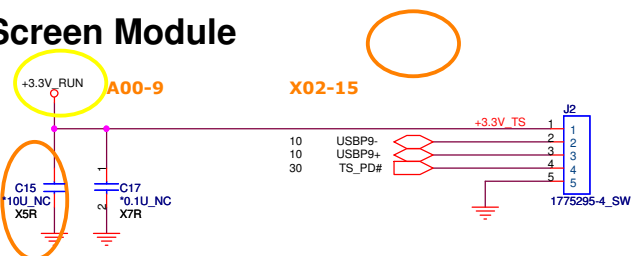
+KB_LED power trace width >10 mil



Quanta Computer Inc.
 Project Name: **GM7C**

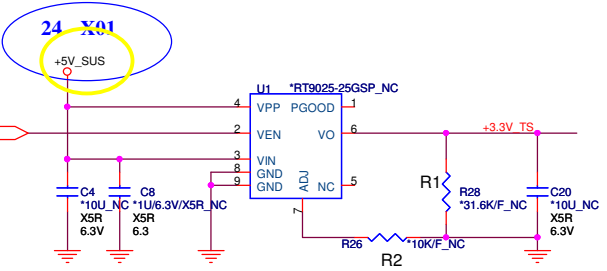
Title	TP / KB	
Size	Document Number	Rev
	GM7C_MB	C
Date:	Friday, January 21, 2011	Sheet 33 of 59

Touch Screen Module



20101208:
2-dimm need to confirm support
S3 wake up by touch screen or not.
20101217:
Need to Check U1 VPP power, J2 pin 1 power
and R504 pull up pwoer rail.

Note:
 1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

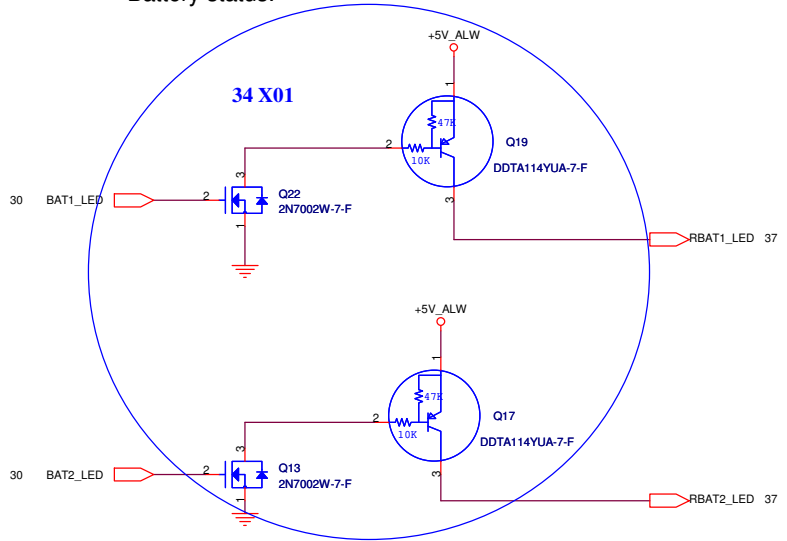


$$V_{out} = 0.8 \times (R2 + R1) / R2$$

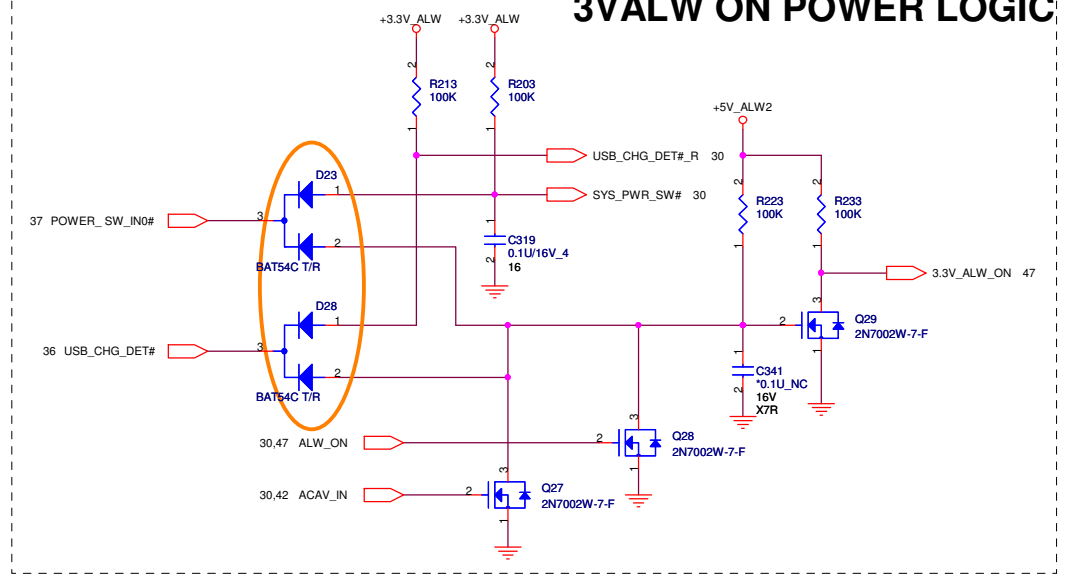
$$3.3 = 0.8 \times (10 + 31.6) / 10$$

LED

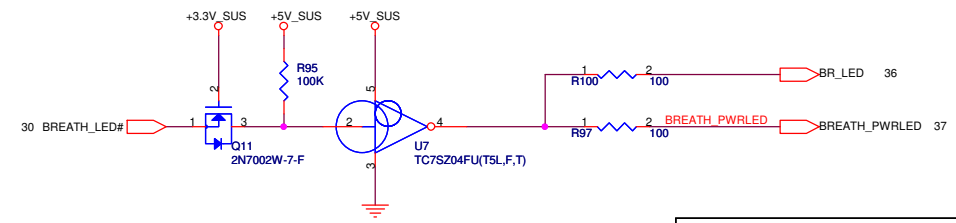
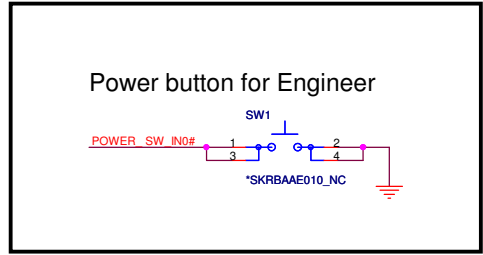
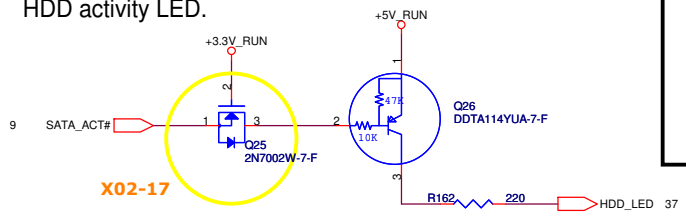
Battery status.



3VALW ON POWER LOGIC



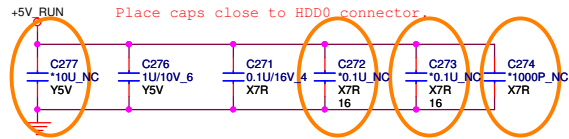
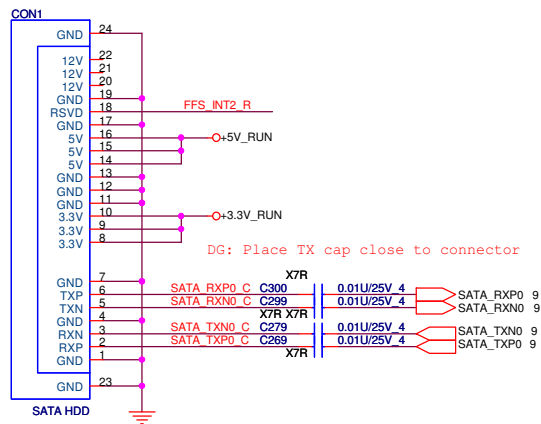
HDD activity LED.



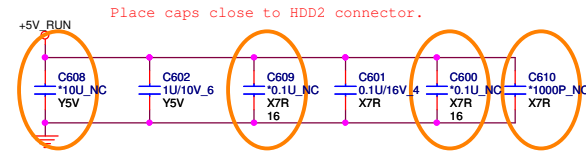
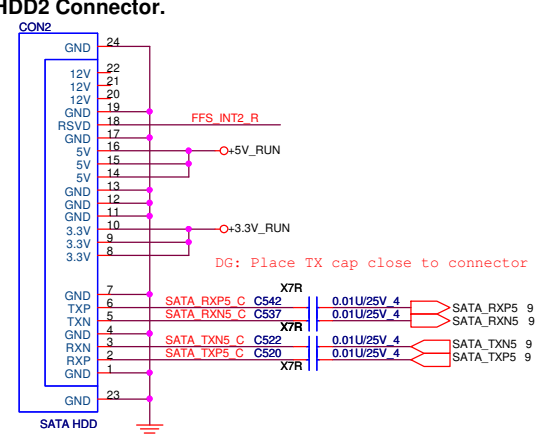
Quanta Computer Inc.
 Project Name: **GM7C**

Title: SWITCH/LED/T-Screen		
Size:	Document Number: GM7C_MB	Rev: C
Date: Friday, January 21, 2011	Sheet: 34	of 59

HDD0 Connector.

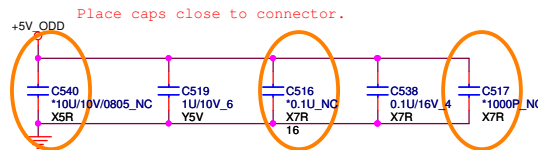
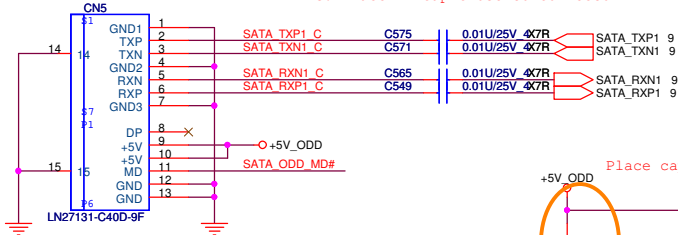


HDD2 Connector.



ODD Connector X02-05

DG: Place TX cap close to connector



Backwards Compatibility

MODC_EN

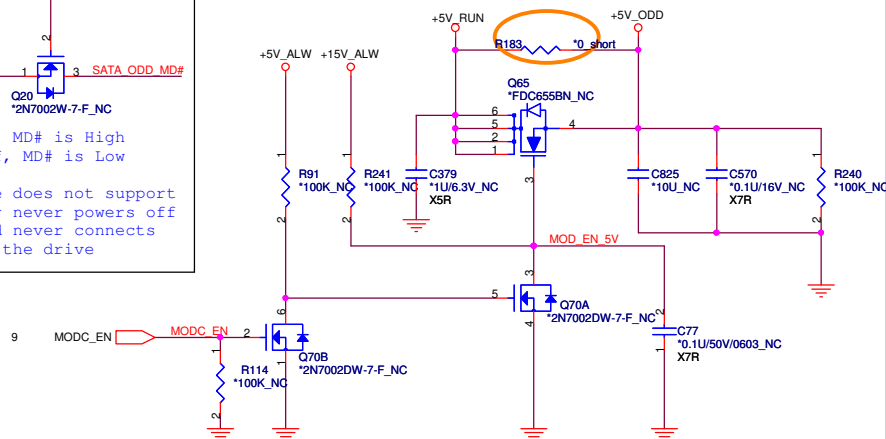
10 SATA_ODD_DA#

Q20 *2N7002W-7-F_NC

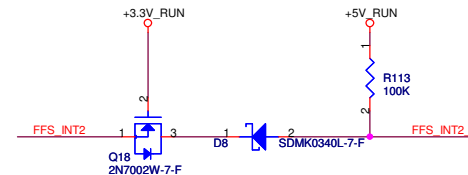
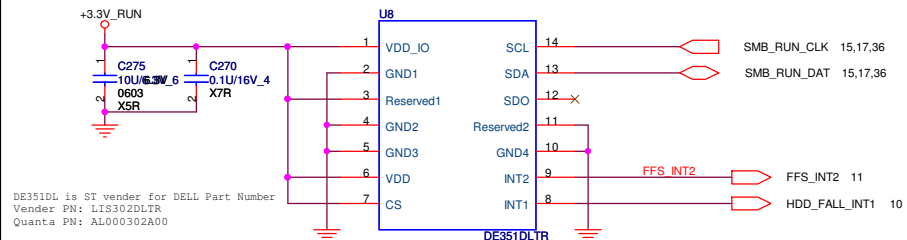
3 SATA_ODD_MD#

Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

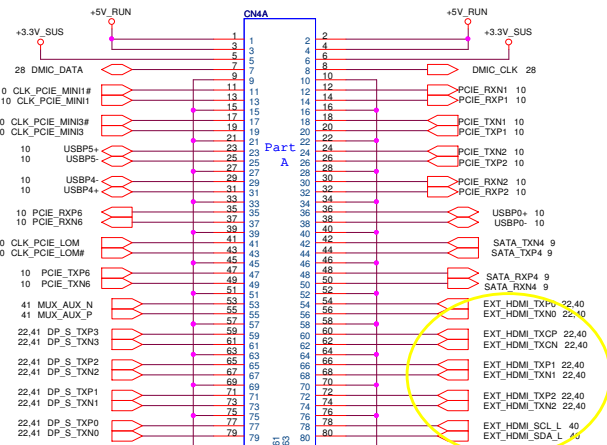


3-axis Fall Sensor (HDD data protector)

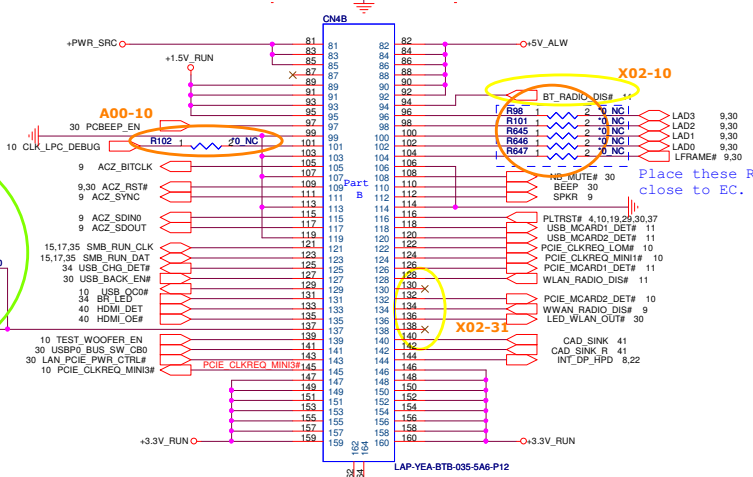


Quanta Computer Inc.
Project Name: **GM7C**

Title			SATA (HDD&ODD)
Size	Document Number	GM7C_MB	
Date:	Friday, January 21, 2011	Sheet	35 of 59



LAP-YEA-BTB-035-5A6-P12 X02-01 Remove DP139 level shift

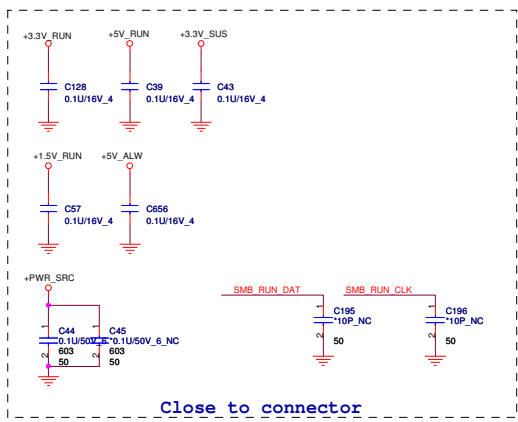
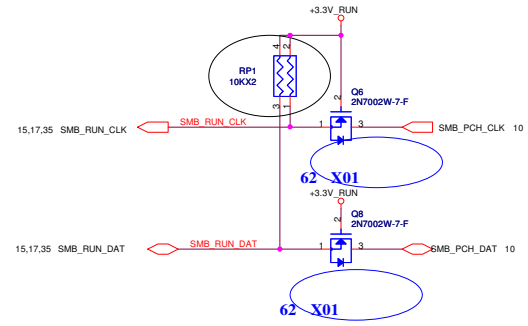


X02-10

Place these R close to EC.

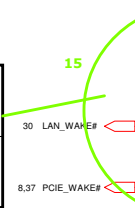
X02-31

LAP-YEA-BTB-035-5A6-P12



Close to connector

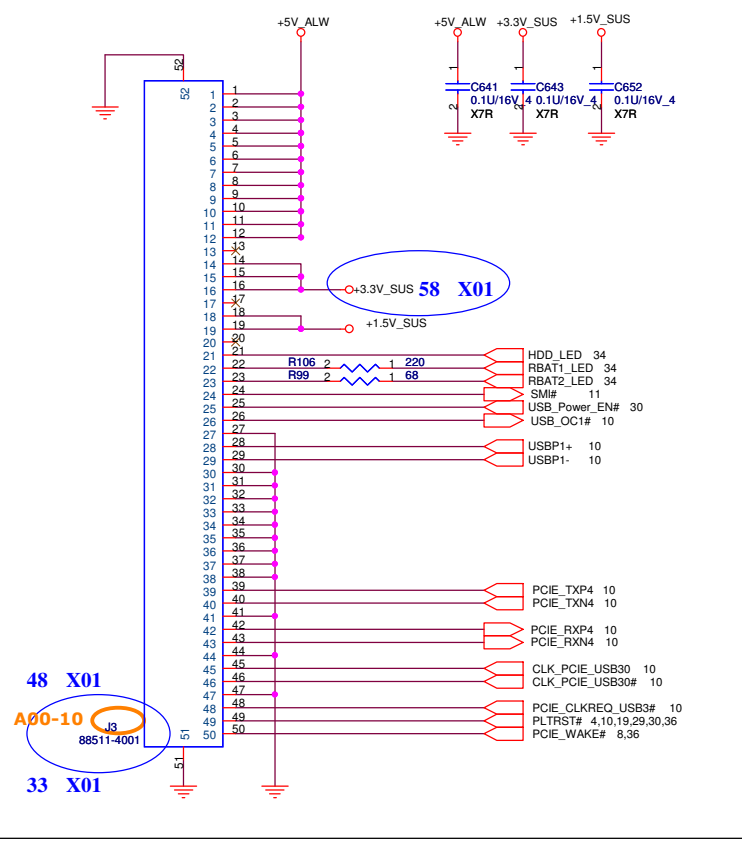
R314	POP	NC
R115		
R112	NC	POP



Quanta Computer Inc. Project Name: GM7C

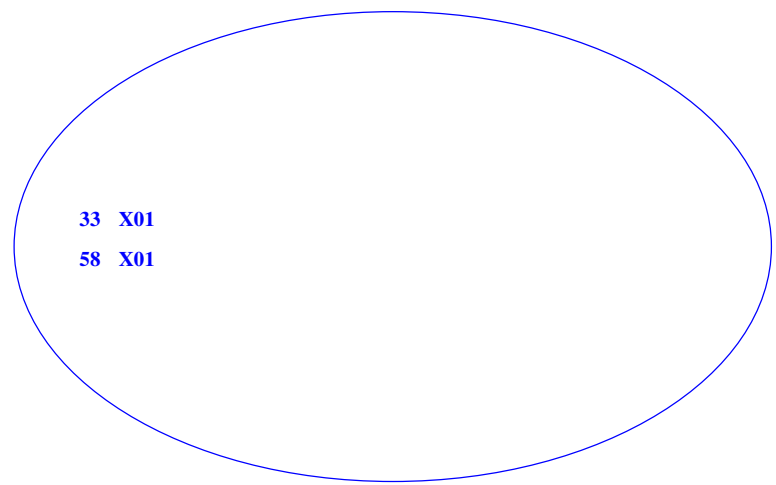
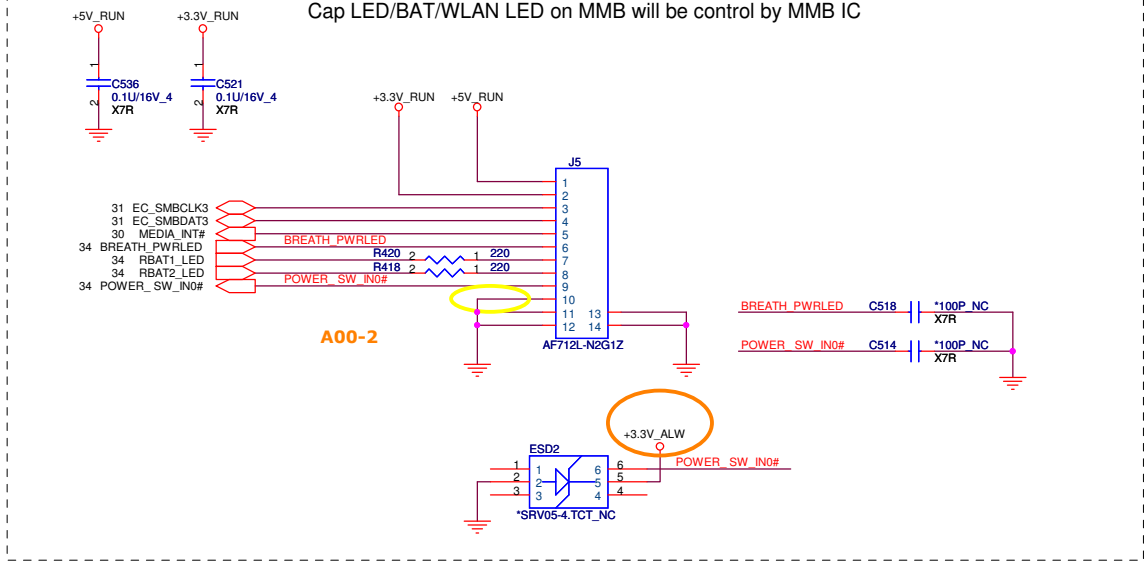
File	DB BTB CON	
Size	Document Number	GM7C_MB
Date	Friday, January 21, 2011	Sheet 36 of 59

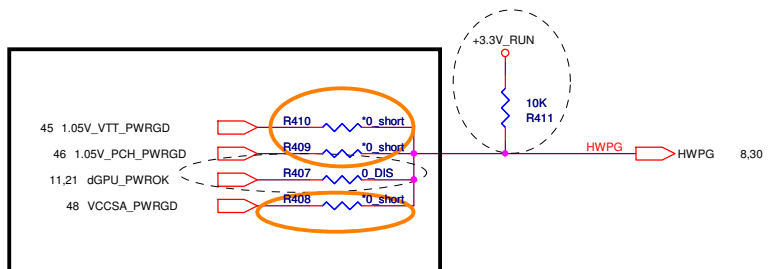
USB IO 50 pins




X02-31 Remove Dell BT375 module

MMB & Power Board 12pins
Cap LED/BAT/WLAN LED on MMB will be control by MMB IC

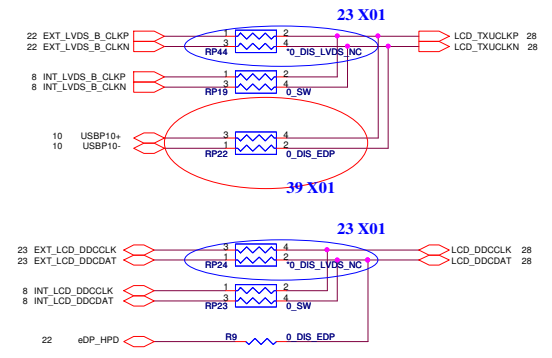
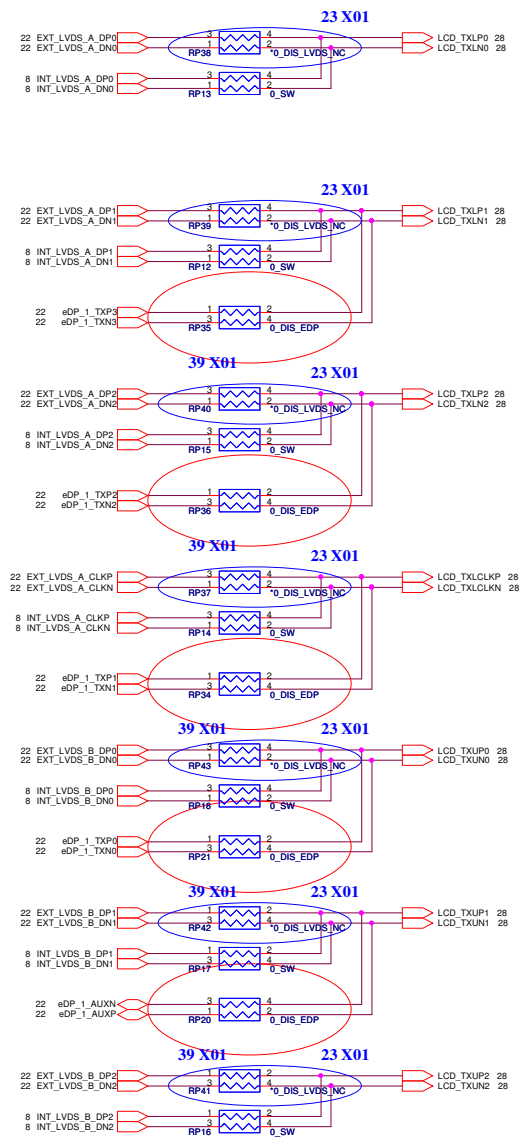




		Quanta Computer Inc.	
		Project Name: GM7C	
Title: System Reset Circuit			
Size	Document Number: GM7C_MB		Rev: C
Date: Friday, January 21, 2011		Sheet: 38	of 59

LVDS Option

3D Emitter



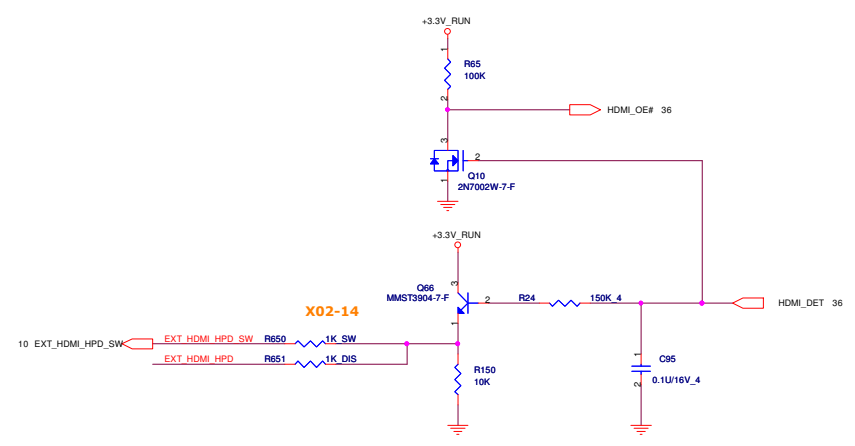
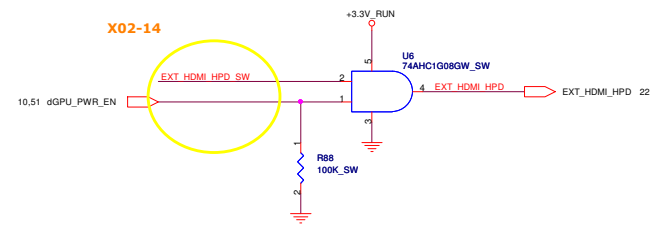
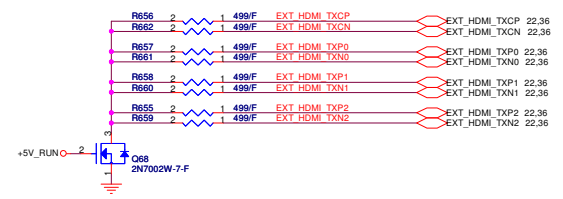
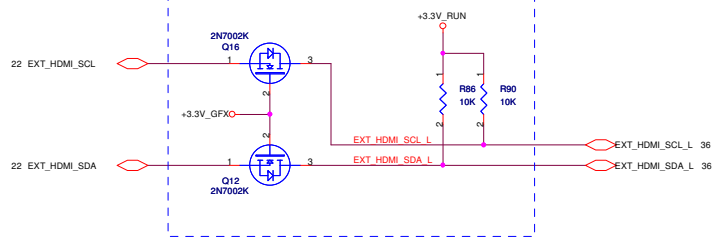
Quanta Computer Inc.
Project Name: **GM7C**

Title: LVDS Option		
Size	Document Number: GM7C_MB	Rev: C
Date: Friday, January 21, 2011 Sheet 39 of 59		

Optimus 1.1

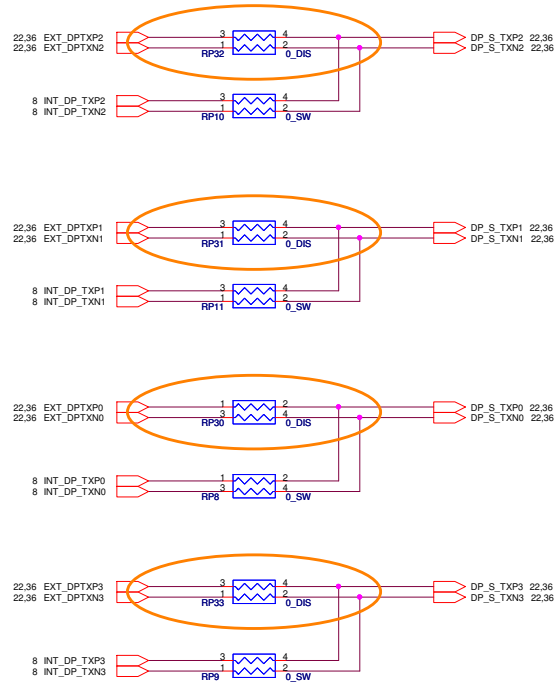
X02-01 Remove DP139 level shift

NV Suggestion: EXT_HDMI_SDA/EXT_HDMI_SCL need gating circuit or MOSFET for level shift power by +3.3V_GFX to prevent leakage.

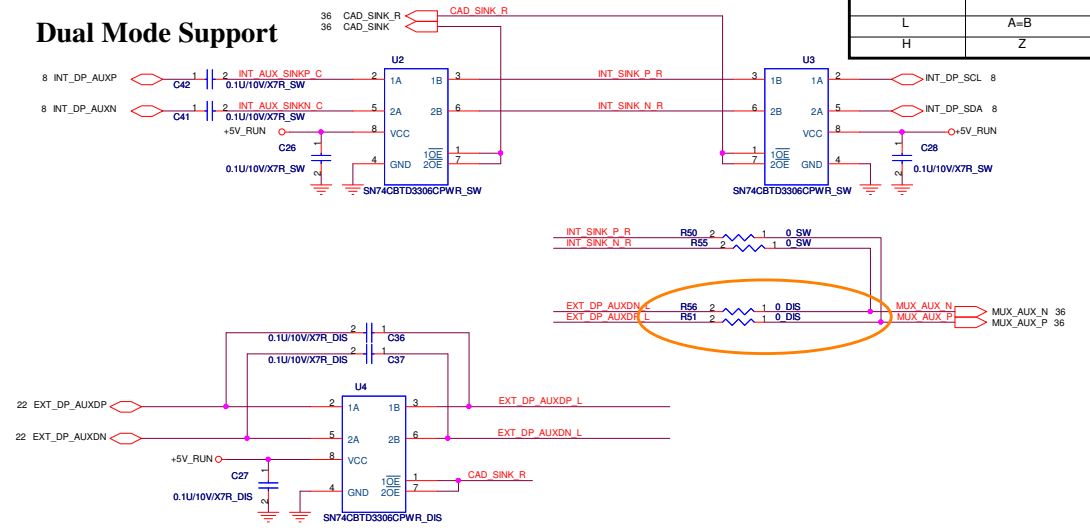


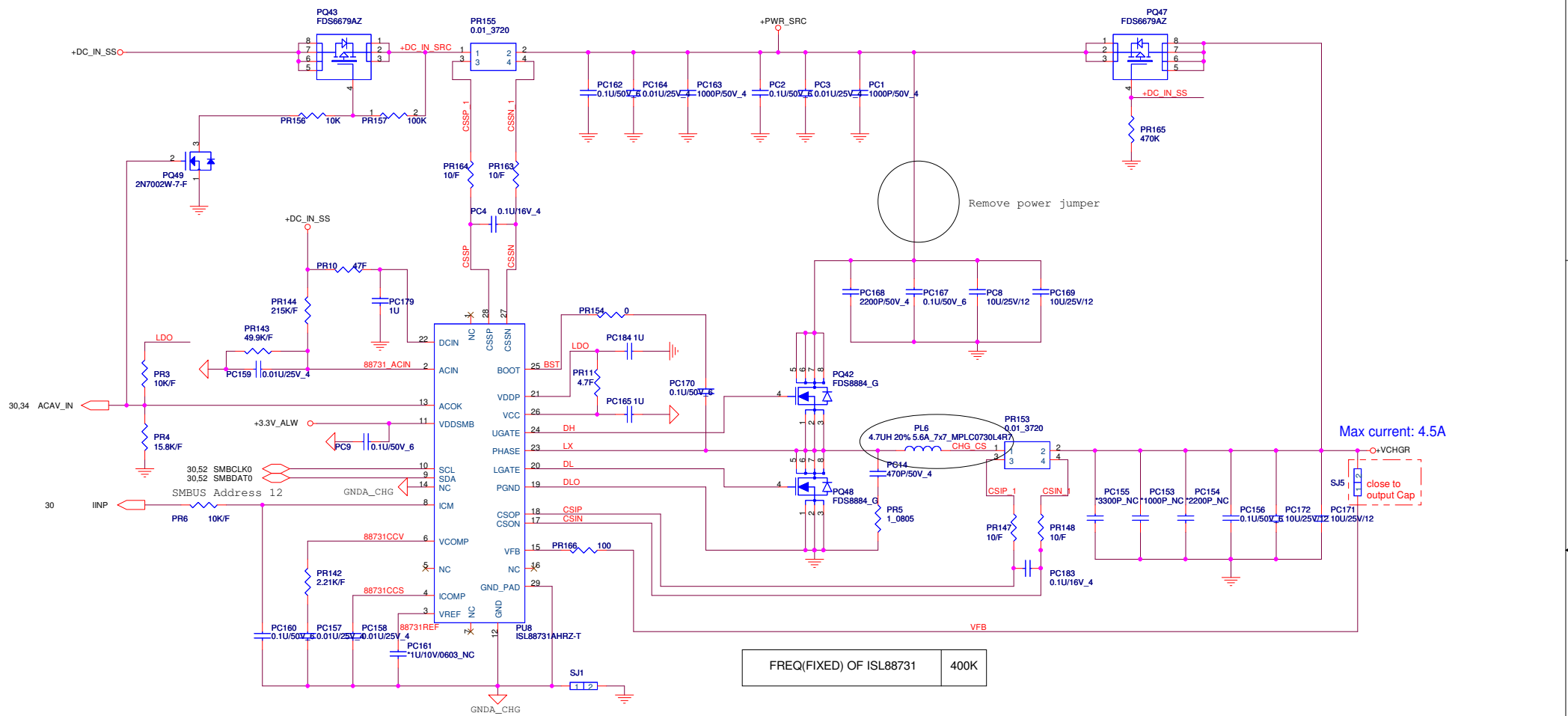
Quanta Computer Inc.
 Project Name: **GM7C**

Title		HDMI Option
Size	Document Number	Rev
	GM7C_MB	C
Date:	Friday, January 21, 2011	Sheet 40 of 59



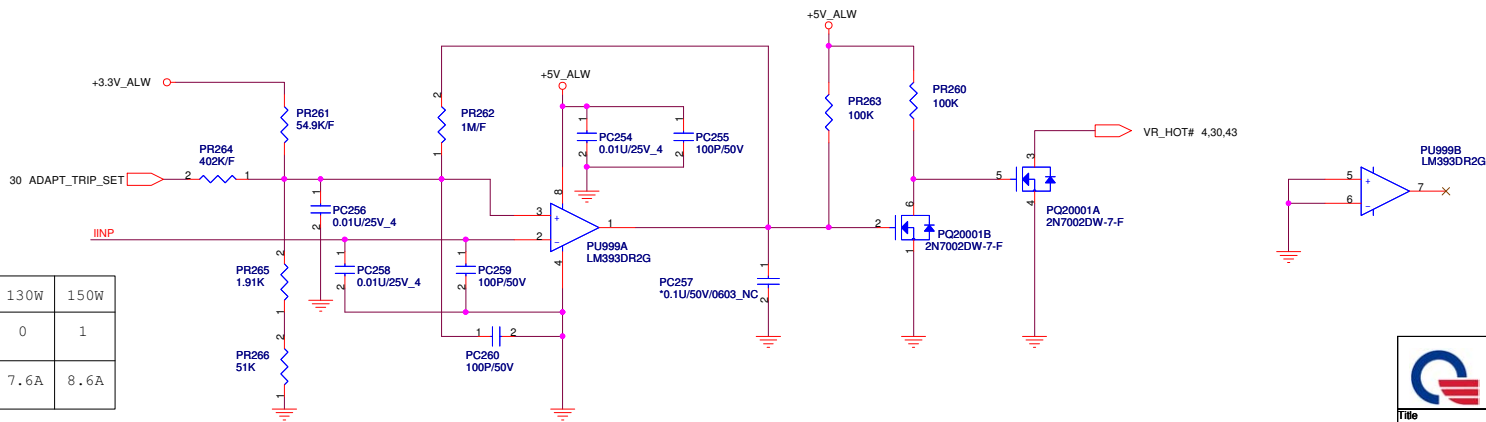
Dual Mode Support

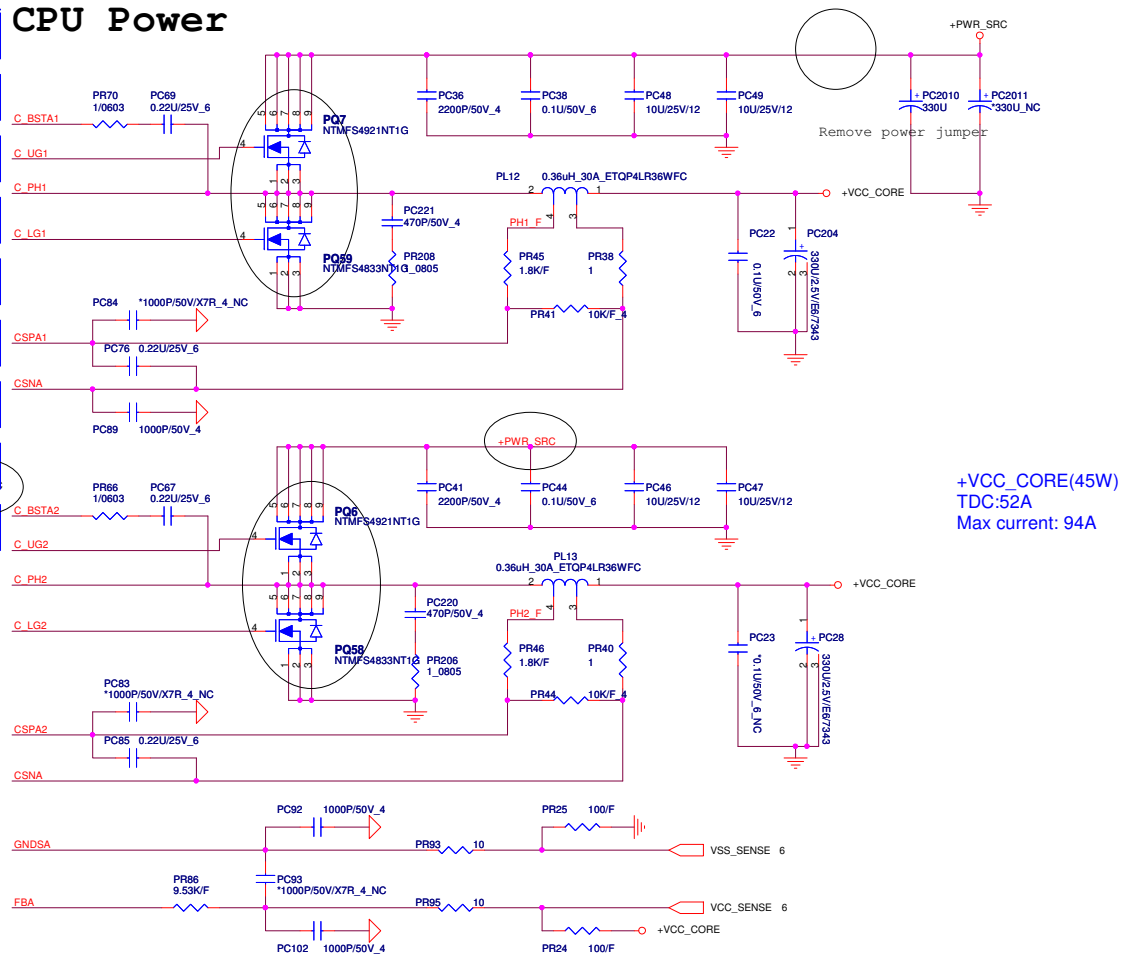
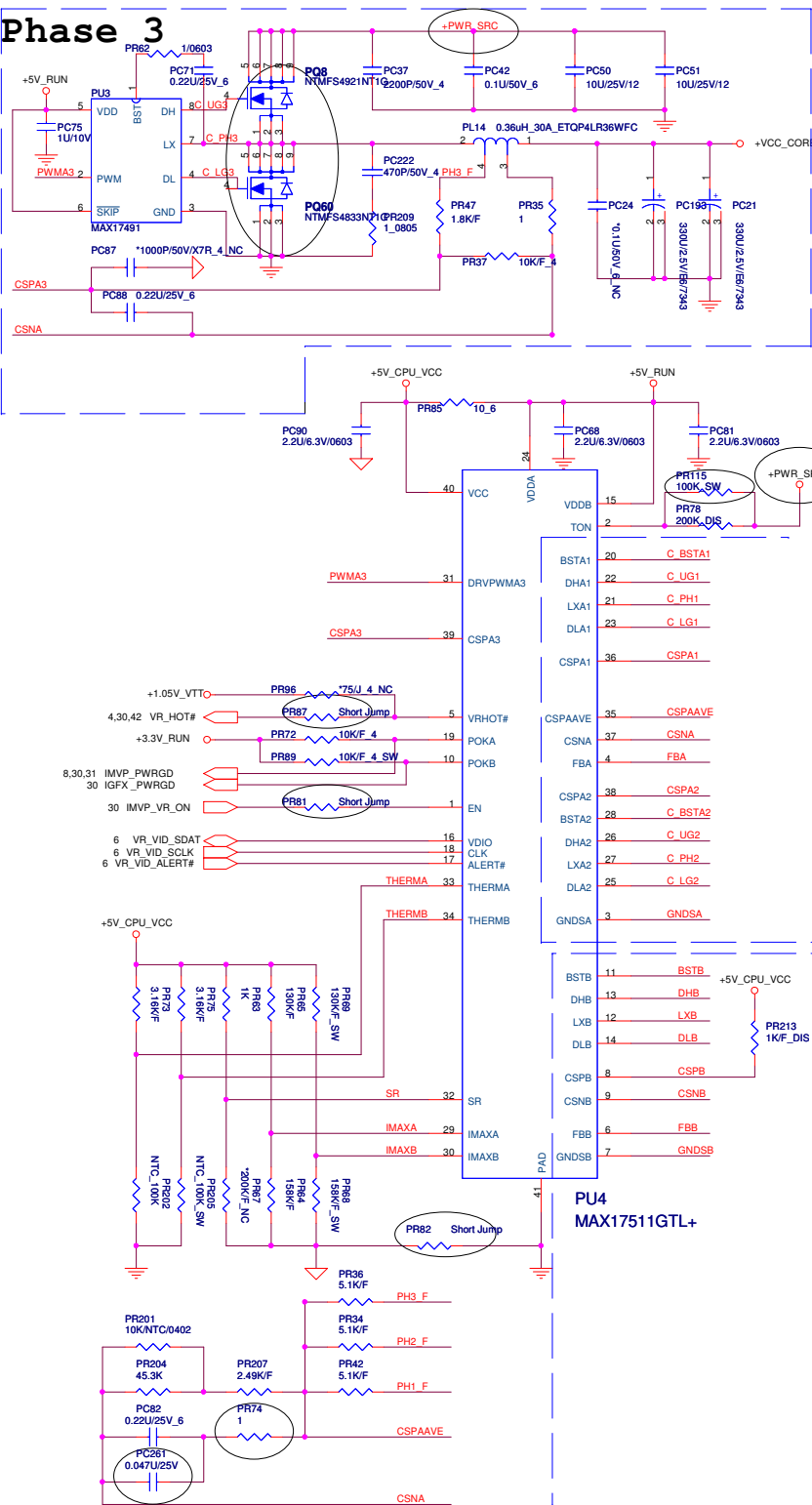




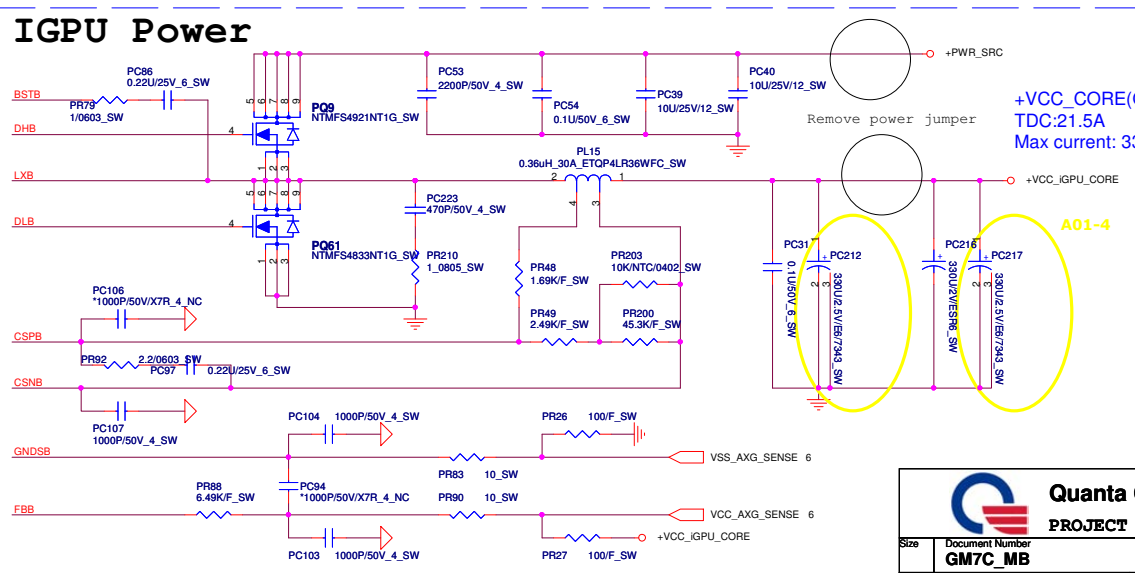
FREQ(FIXED) OF ISL88731	400K
-------------------------	------

Adapter type	130W	150W
ADAPT_TRIP_SET	0	1
Current setting	7.6A	8.6A



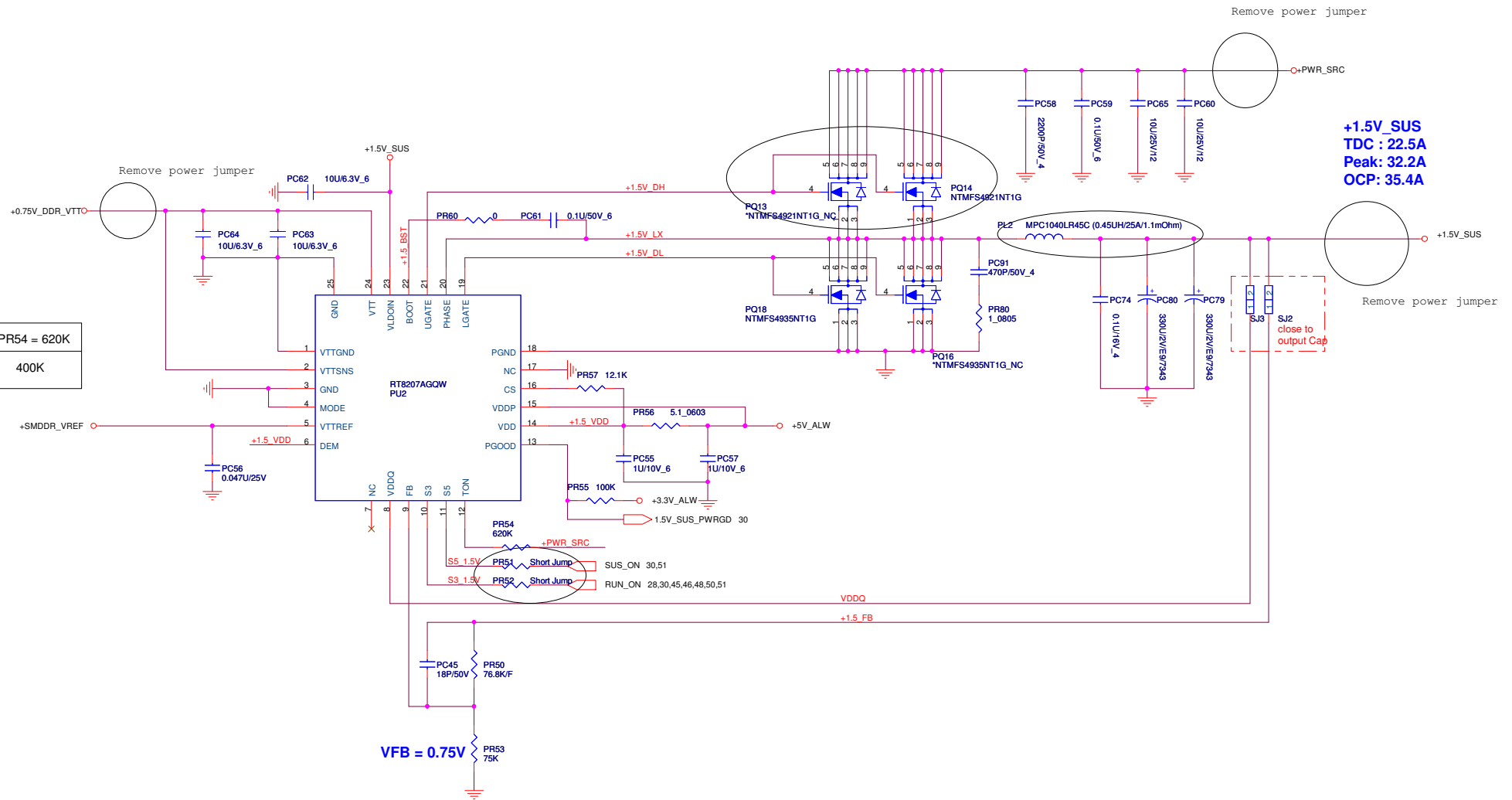


+VCC_CORE(45W)
TDC:52A
Max current: 94A



+VCC_CORE(GT-2/45W)
TDC:21.5A
Max current: 33A

TON	PR54 = 620K
FREQ	400K



+1.5V_SUS
TDC : 22.5A
Peak: 32.2A
OCF: 35.4A

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

VDDQ output voltage selection

FB	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQNS/2	DDR3
V5IN	1.8V	VDDQNS/2	DDR2
FB Resistors	Adjusting	VDDQNS/2	0.75V < VDDQ < 3.3V

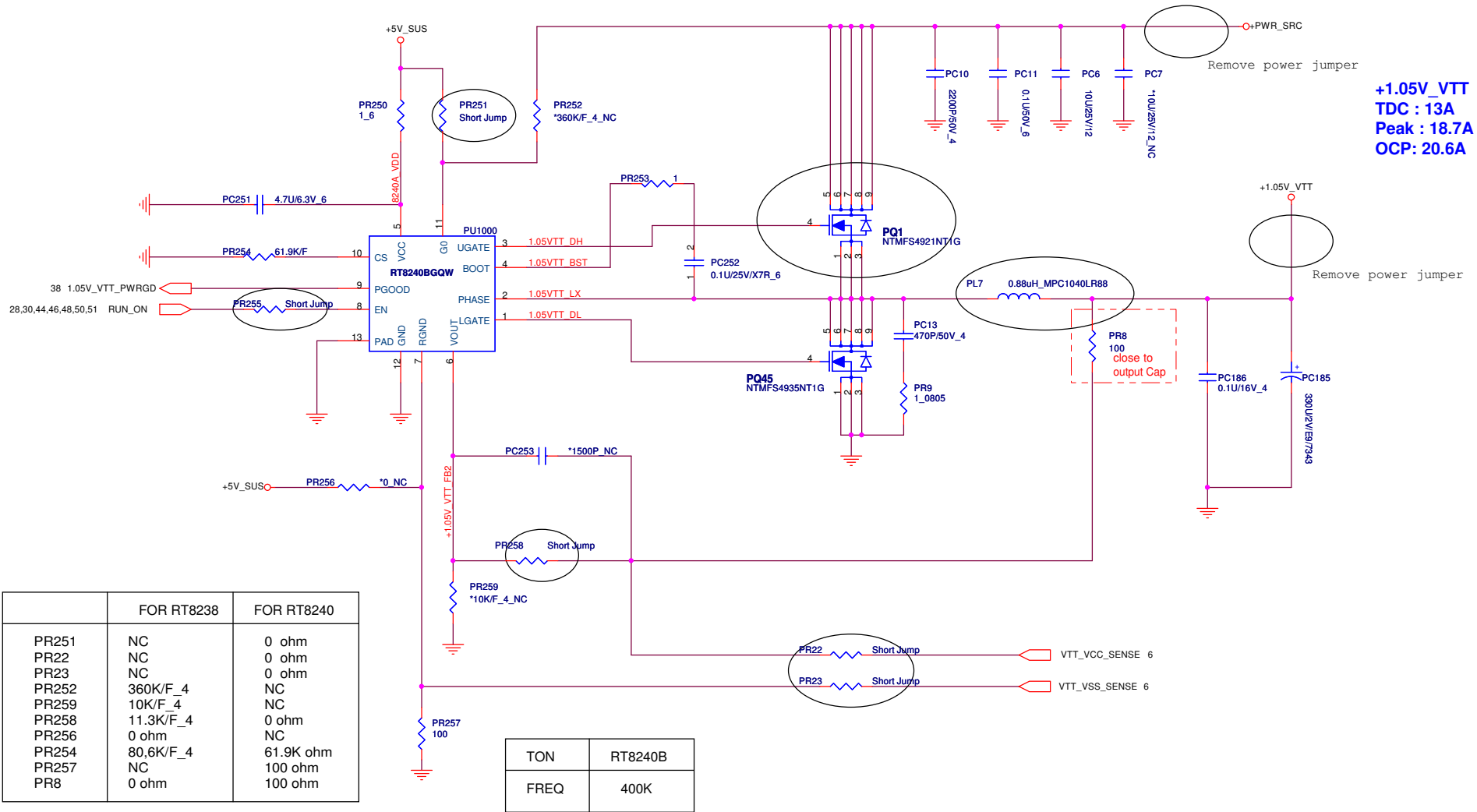
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
 Project Name: **GM7C**

Title		CoverPage
Size	Document Number	Rev
	GM7C_MB	C
Date:	Friday, January 21, 2011	Sheet 44 of 59

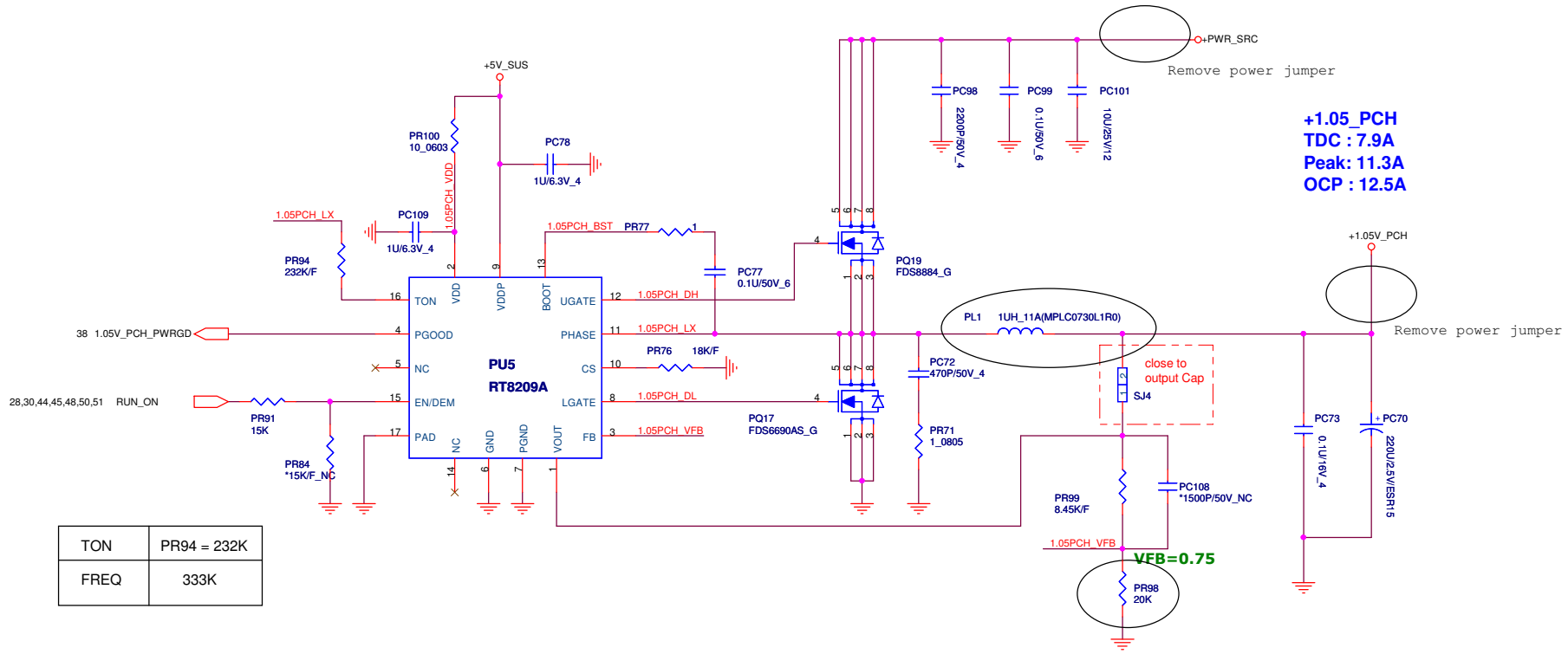
+1.05V_VTT (RT8240B)



+1.05V_VTT
TDC : 13A
Peak : 18.7A
OCP : 20.6A

	FOR RT8238	FOR RT8240
PR251	NC	0 ohm
PR22	NC	0 ohm
PR23	NC	0 ohm
PR252	360K/F_4	NC
PR259	10K/F_4	NC
PR258	11.3K/F_4	0 ohm
PR256	0 ohm	NC
PR254	80.6K/F_4	61.9K ohm
PR257	NC	100 ohm
PR8	0 ohm	100 ohm

TON	RT8240B
FREQ	400K



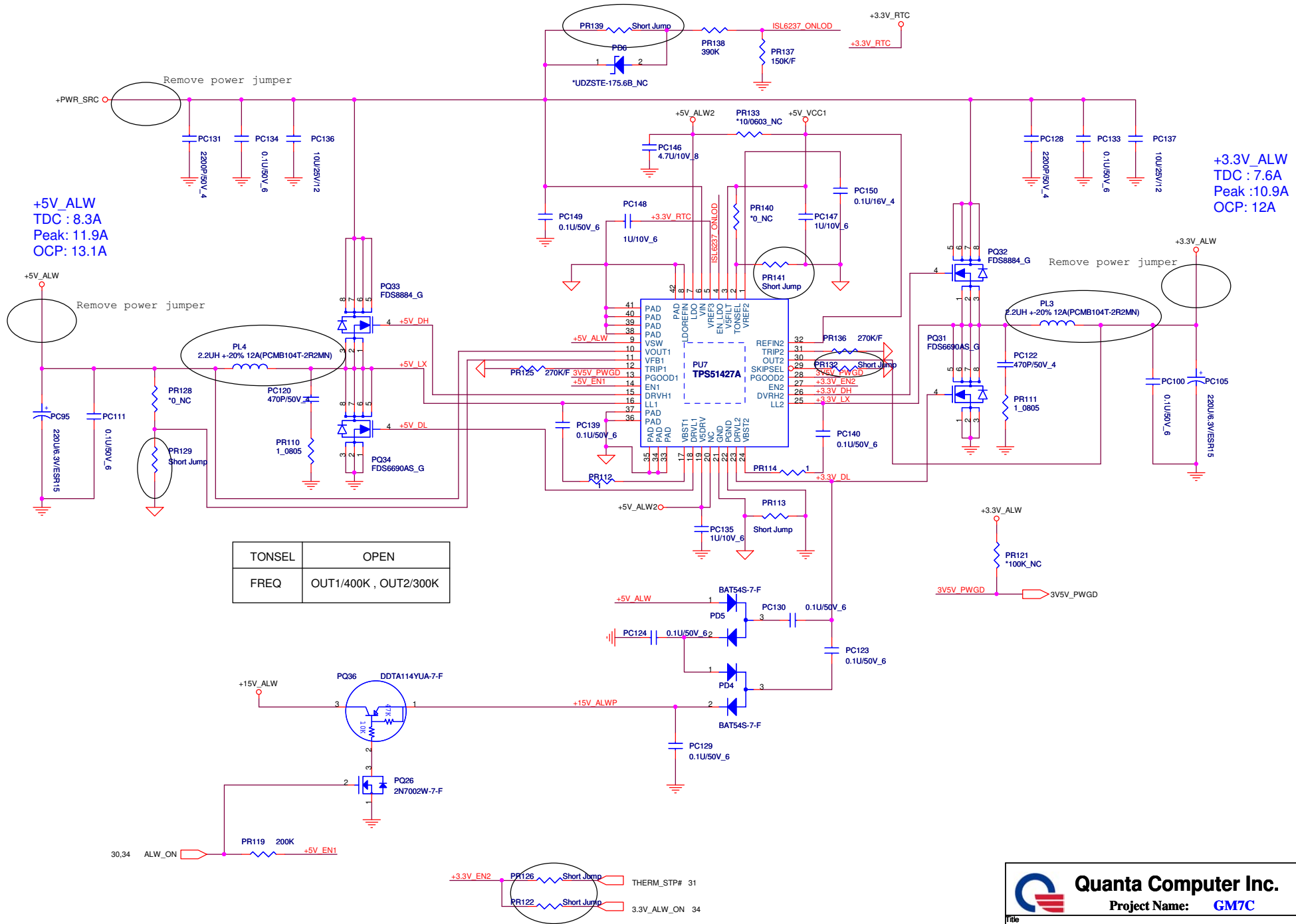
+1.05_PCH
TDC : 7.9A
Peak: 11.3A
OCP : 12.5A

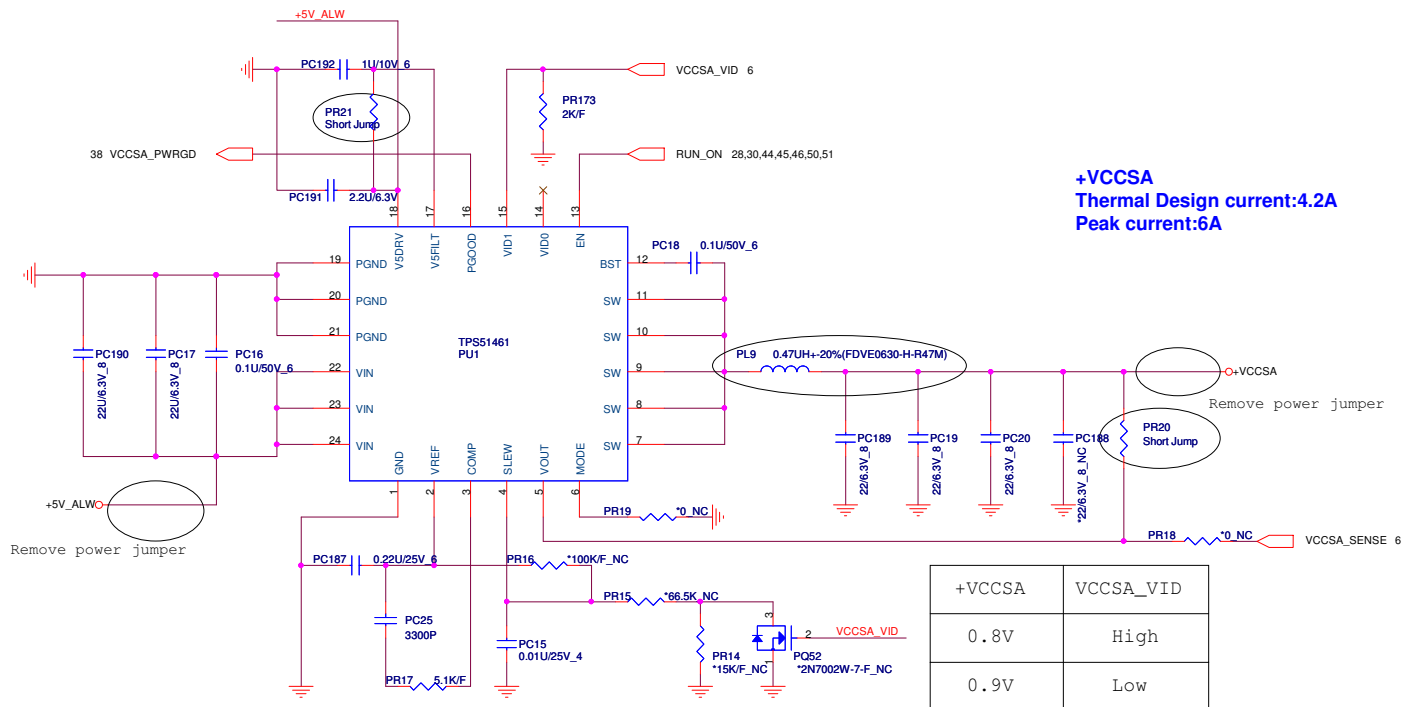
TON	PR94 = 232K
FREQ	333K

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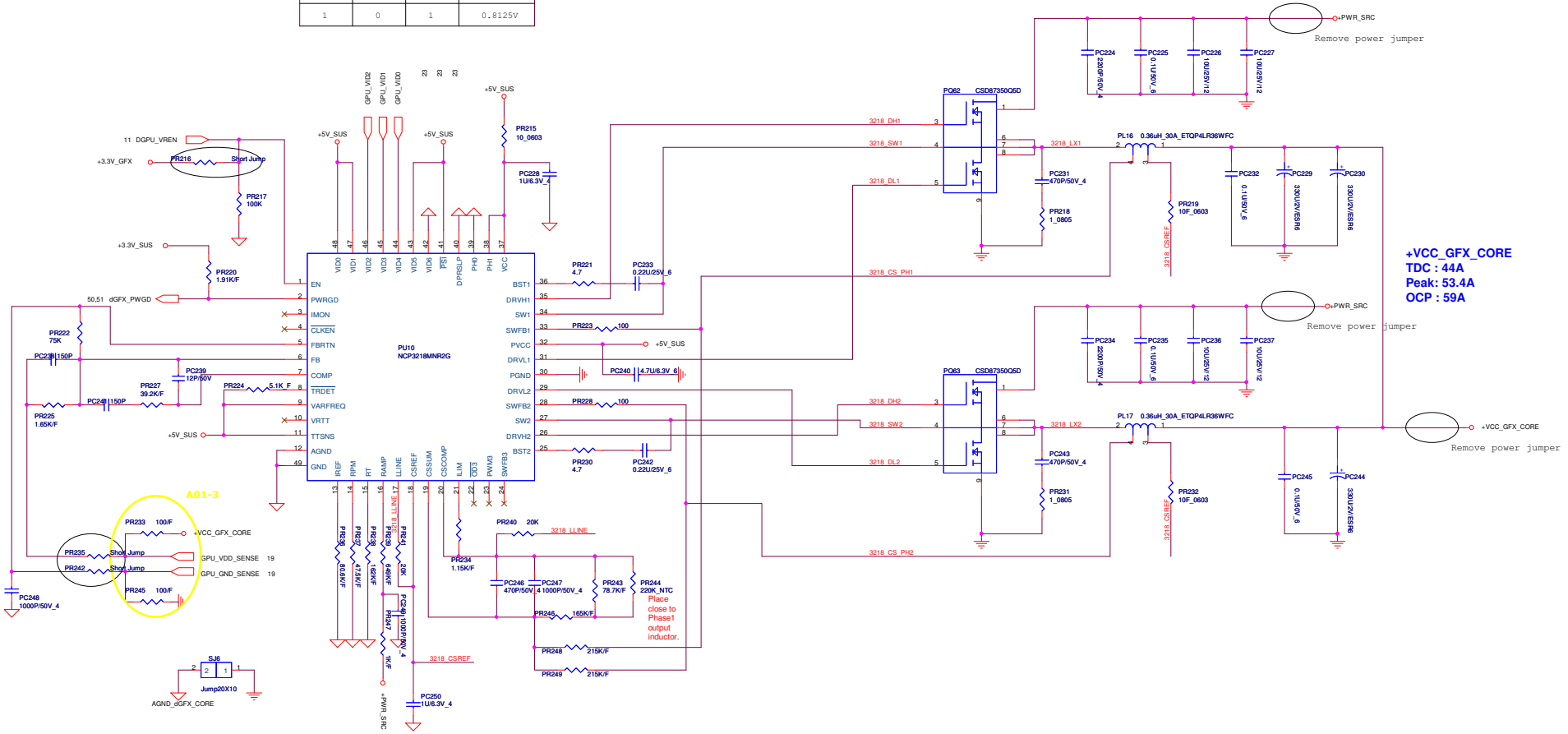
Rev C



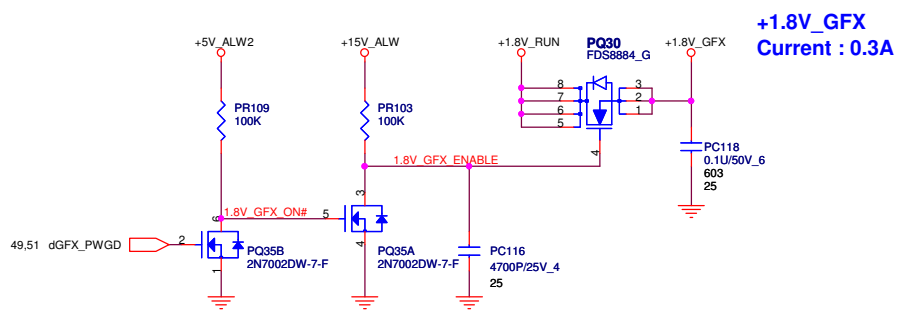
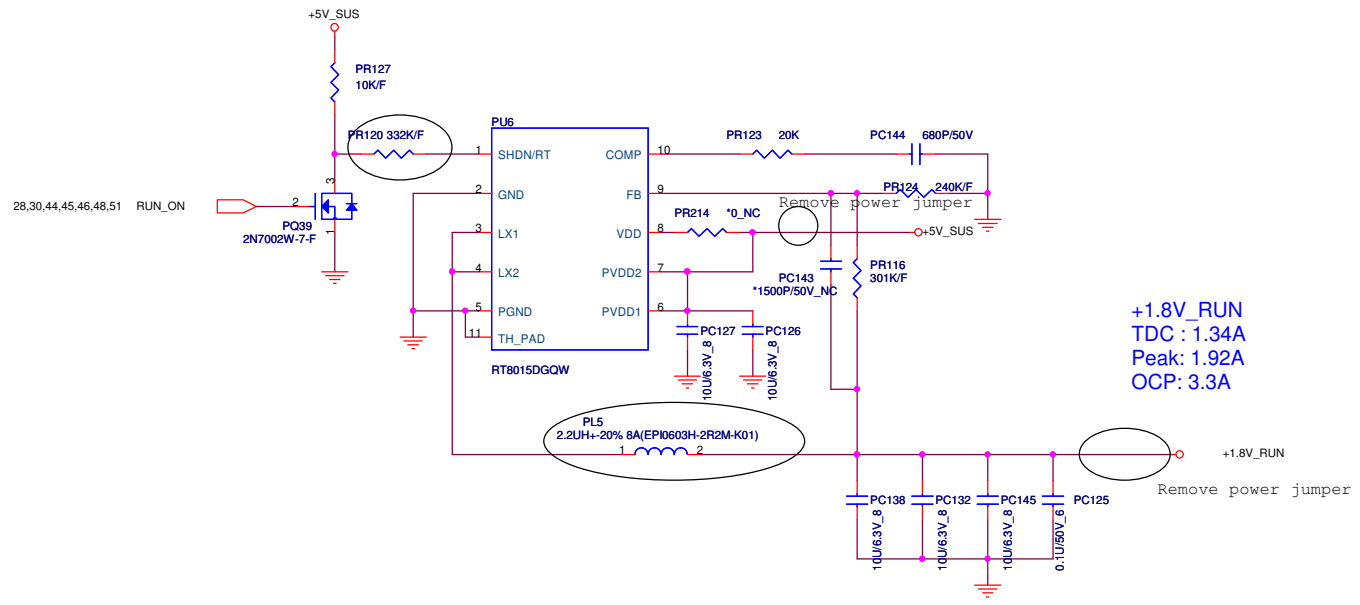


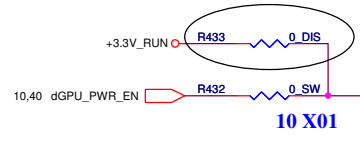
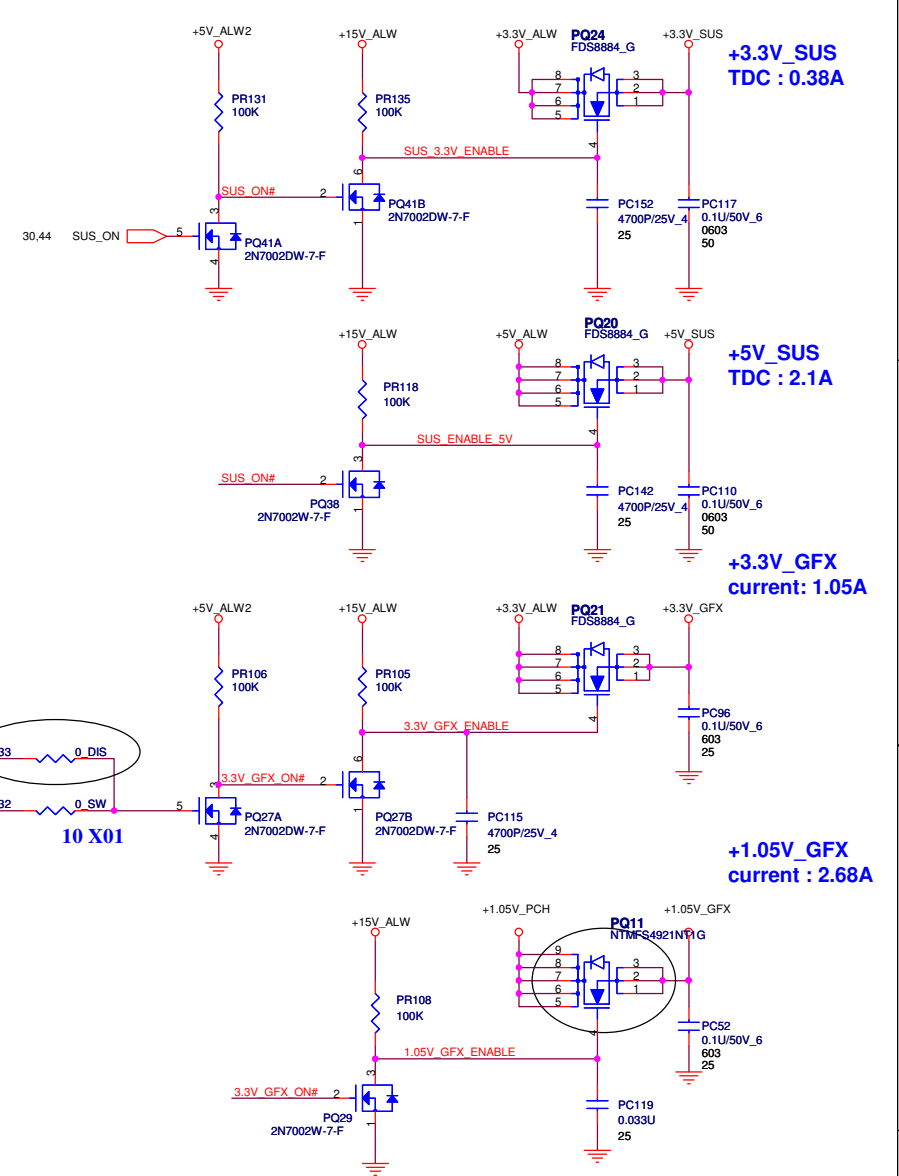
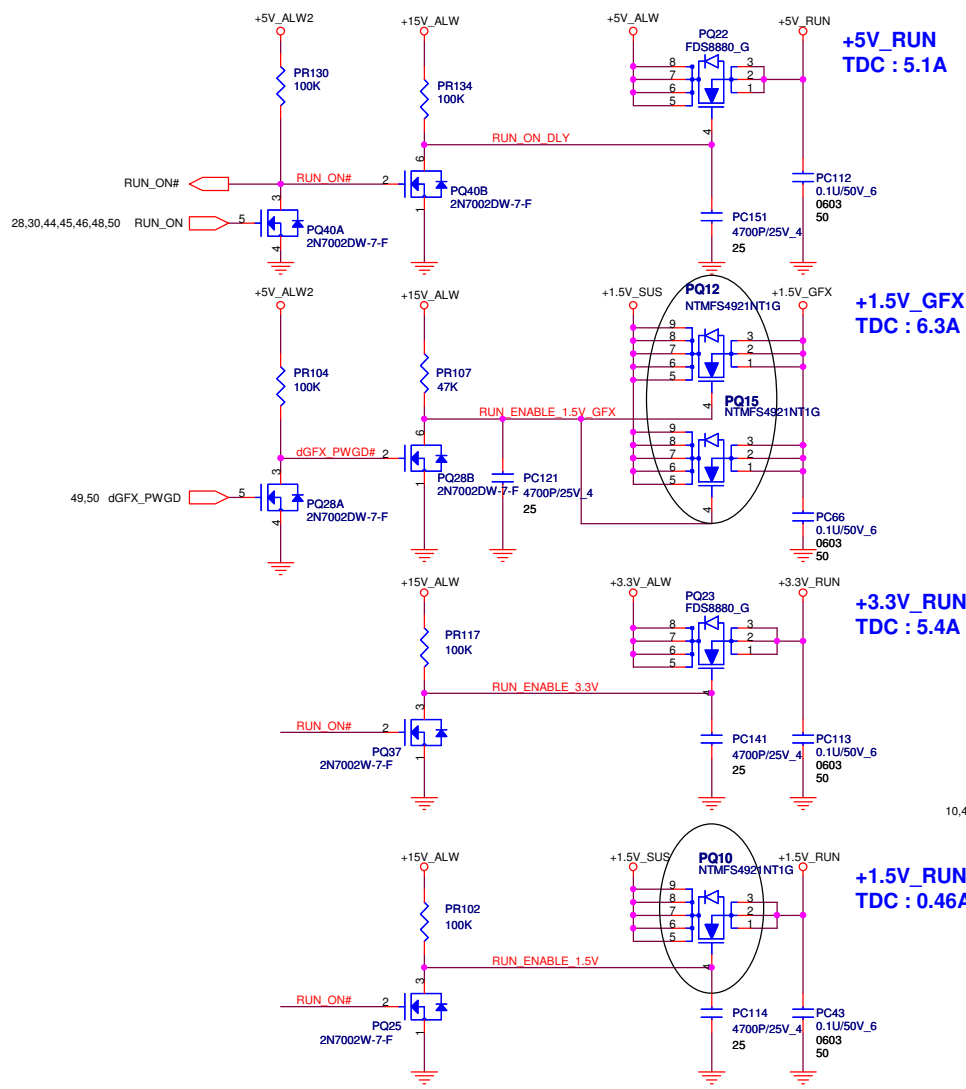
PR16 (100K), PR15 (66.5K), PR14 (15K) & PQ52(2N7002) are NC for TPS51461, (But it is necessary for XPS51461).

GPU_VID0	GPU_VID1	GPU_VID2	Voltage
0	1	1	0.9125V
1	0	0	0.8625V
1	0	1	0.8125V

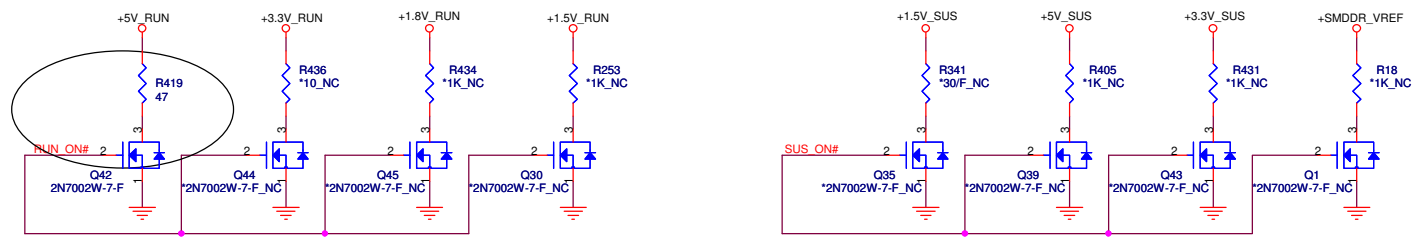


+VCC_GFX_CORE
TDC : 44A
Peak : 53.4A
OCP : 59A



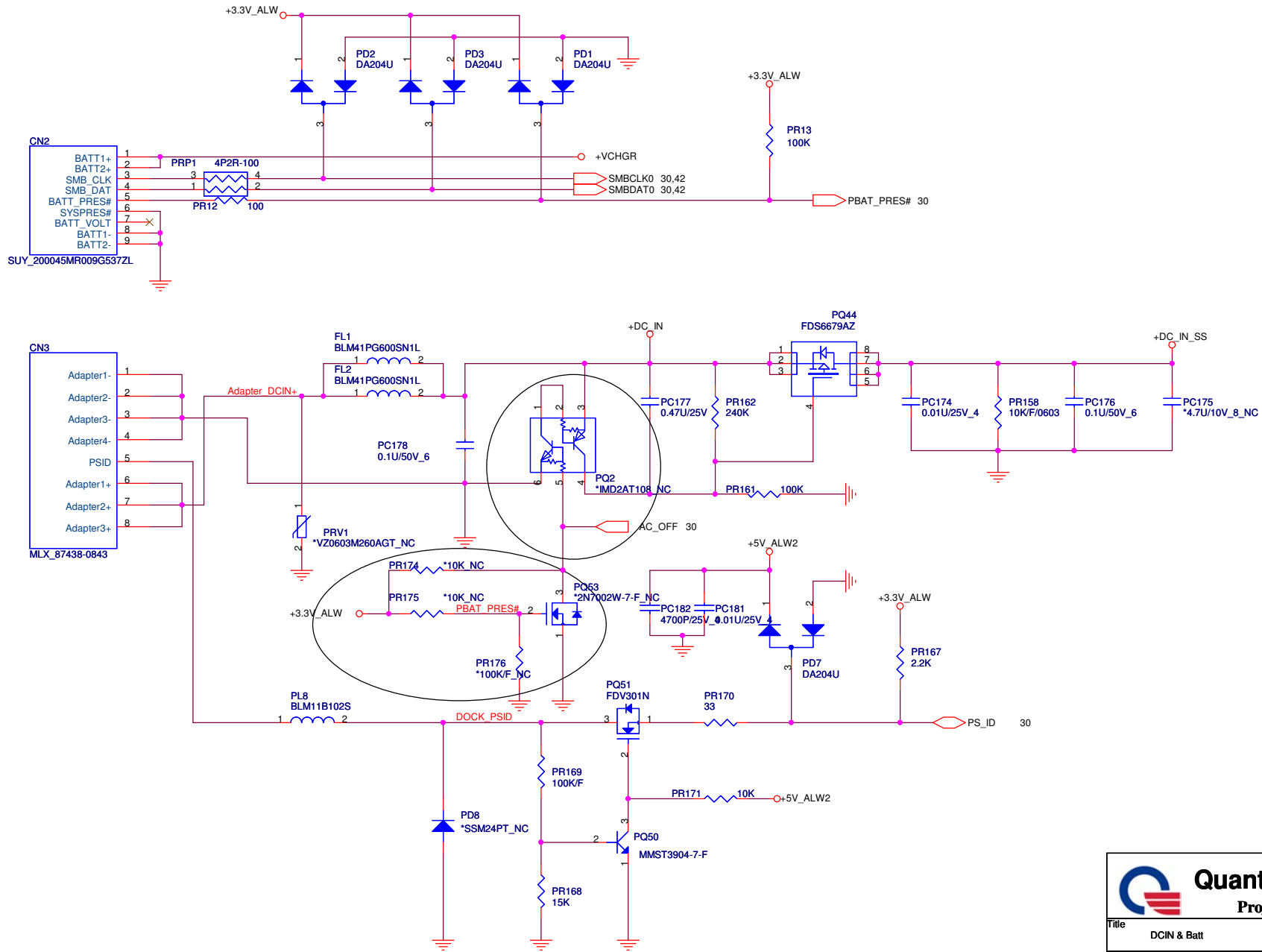



Reserve discharge path

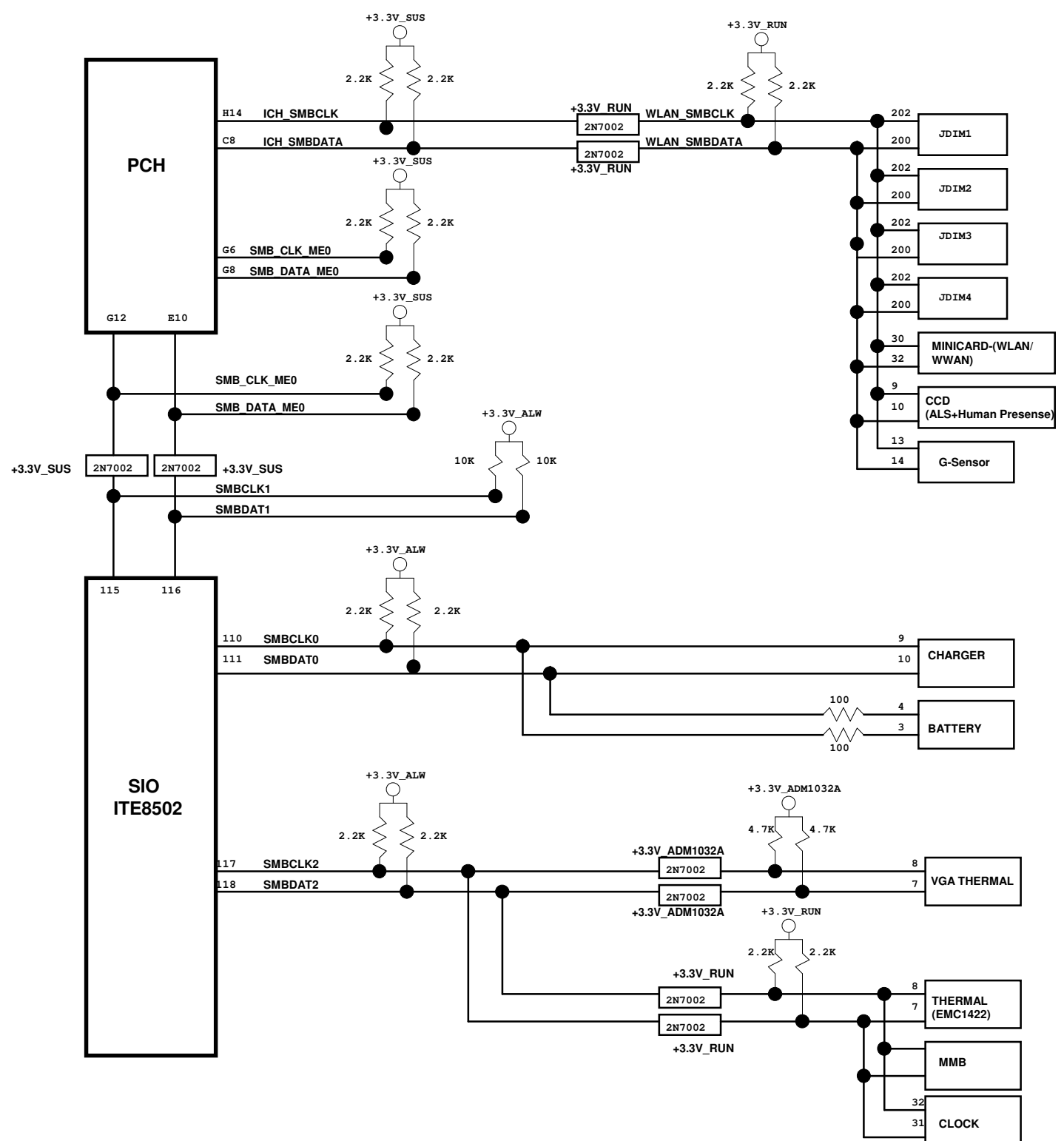


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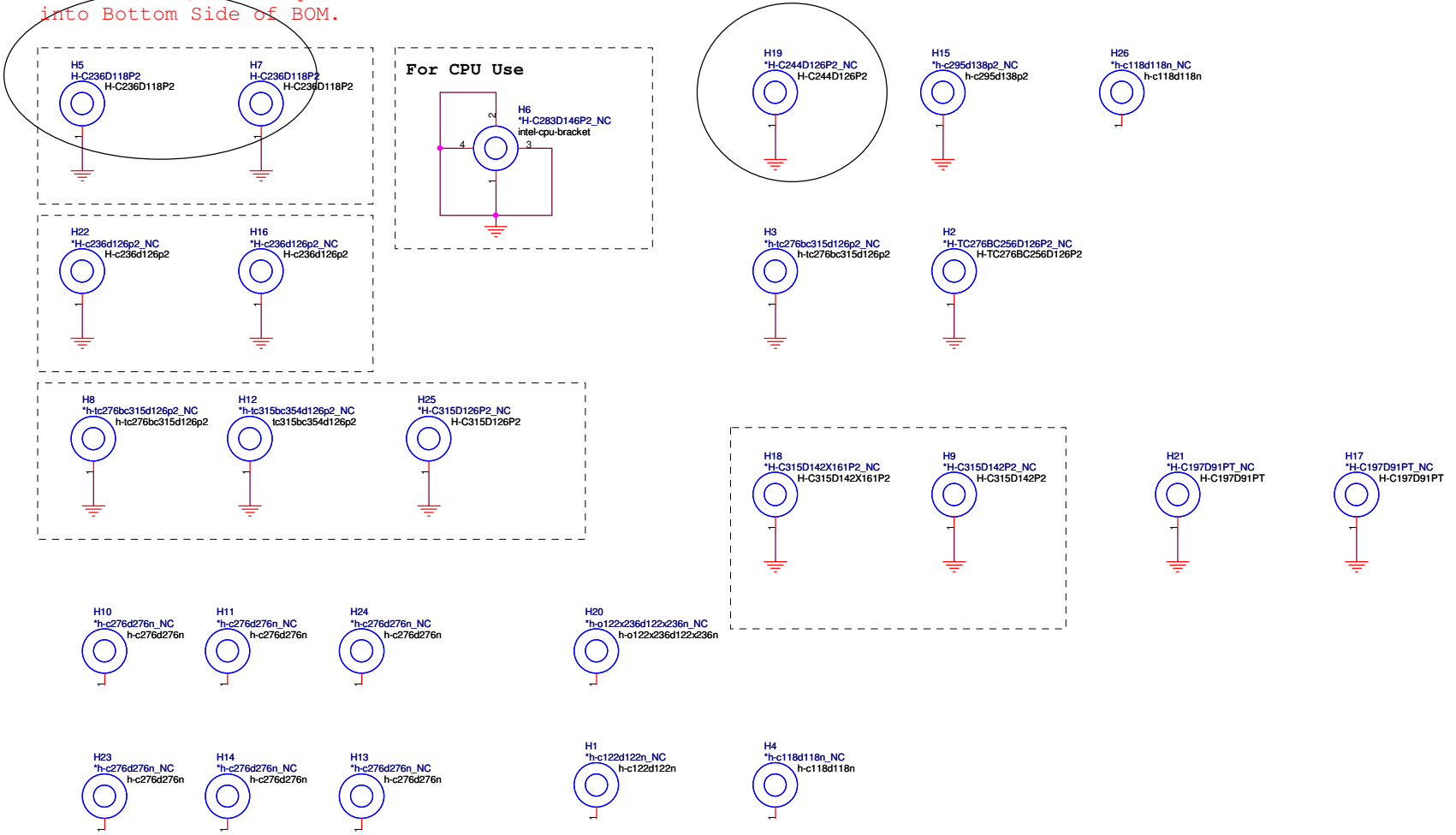
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HCJM5004013
GM7C label on 31 header PN_3M

Add NUT on H5, H7 and put it into Bottom Side of BOM.



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