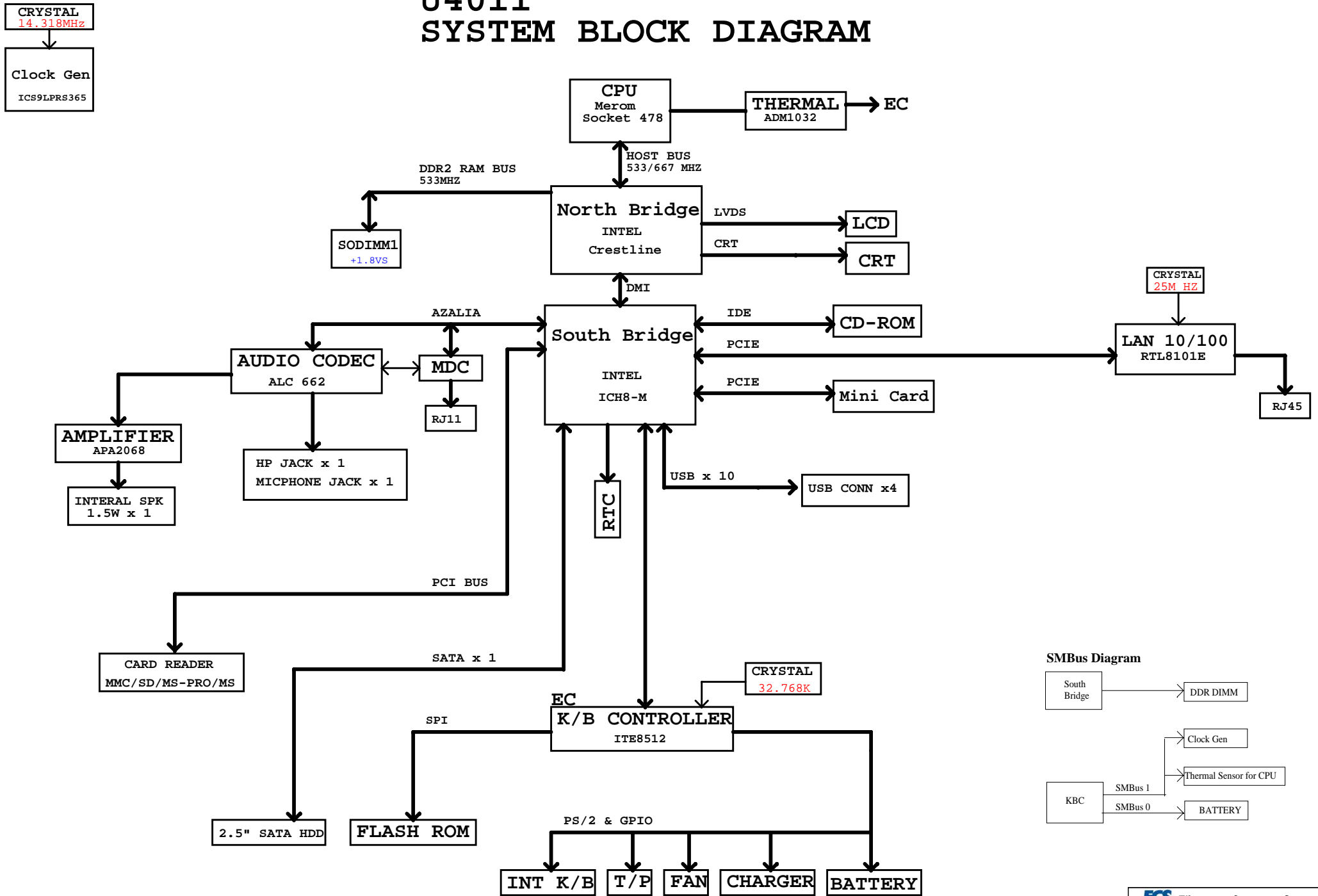
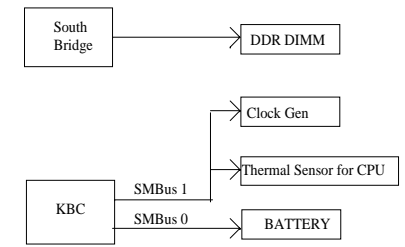


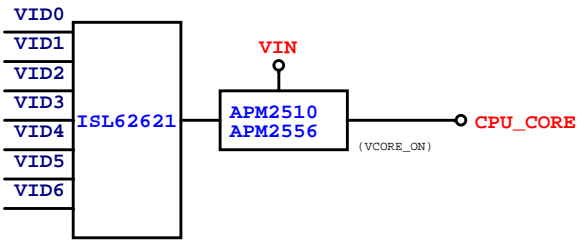
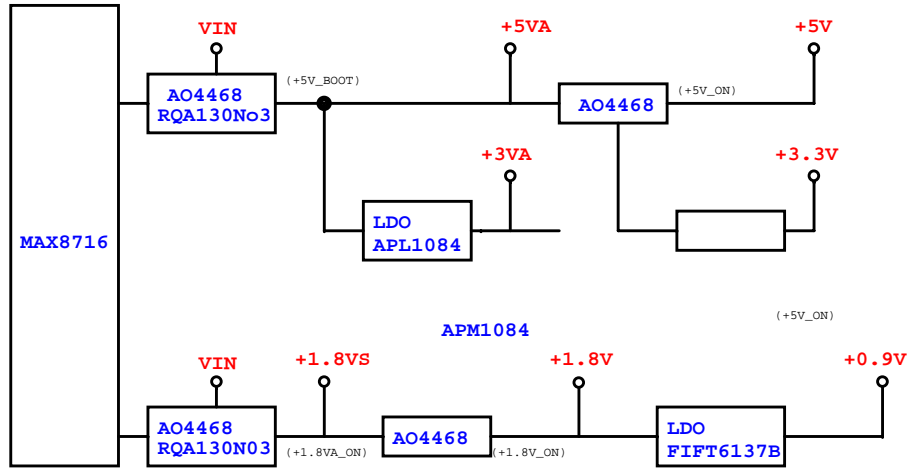
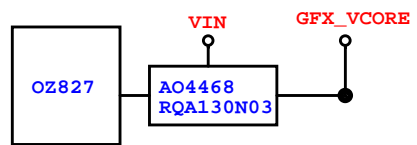
U40II SYSTEM BLOCK DIAGRAM



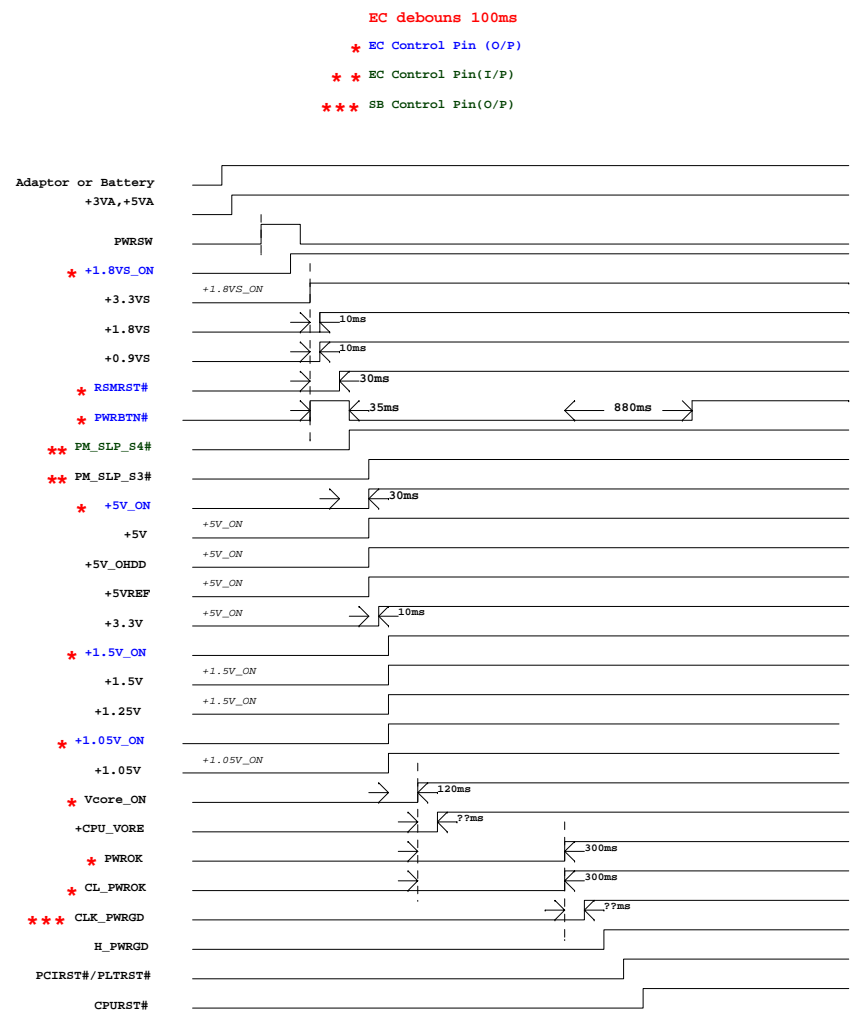
SMBus Diagram



POWER BLOCK DIAGRAM



POWER Sequence



SIS968 GPIO	
GPIO0	NC
GPIO1	NC
GPIO2	PM_THROTTLING#
GPIO3	EC_EXTSMI#
GPIO4	PM_CLKRUN#
GPIO5	NC
GPIO6	NC
GPIO7	NC
GPIO8	NC
GPIO9	NC
GPIO10	SLP_S5#
GPIO11	AGPSTOP_N
GPIO12	DP_SLP#
GPIO13	SB_DPRSLPVR
GPIO14	NC
GPIO15	SLP_S3#
GPIO16	NC
GPIO17	H_A20GATE
GPIO18	H_RCIN#
GPIO19	SB_SMB_CLK
GPIO20	SB_SMB_DATA

ITE8512E GPIO	
GPA0	AUX_PWRGD
GPA1	DDR_V_SW#
GPA2	BTL_BEEP
GPA3	RFLED_ON
GPA4	SCROLL/3G_LED
GPA5	NUM_LED
GPA6	CAPS_LED
GPA7	PWRON_LED
GPB0	PM_SLP_S5#
GPB1	PM_SLP_S3#
GPB2	WEBCAM_ON
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	BT_ON
GPC0	EC_VID5
GPC1	SMBCLK_EC
GPC2	SMBDAT_EC
GPC3	EC_VID2
GPC4	RF_SW_ON#
GPC5	EC_VID1
GPC6	INTERNET#
GPC7	SILENT#
GPD0	EC_PREST#
GPD1	PWRBTN#
GPD2	EC_LPCRST#
GPD3	EC_EXTSCI#
GPD4	EC_EXTSMI#
GPD5	H_PROCHOT#
GPD6	CHG_ON
GPD7	LCDSW
GPE0	EC_PWR_ON
GPE1	SET_V
GPE2	PWROK
GPE3	VCORE_ON
GPE4	LID#
GPE5	AC_IN/OUT#
GPE6	FAN_SPD# or RTCRST
GPE7	AMP_MUTE#
GPF0	3G_ON
GPF1	EC_BSEL1
GPF2	CHG_G_LED
GPF3	CHG_R_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	VGA_SMBCLK
GPF7	VGA_SMBDAT
GPG0	EC_VID3
GPG1	EC_WDOG OK
GPG2	FLFRAME#
GPG6	NEW_CARD_PWR_ON#
GPH0	+1.8V_ON
GPH1	+1.8VS_ON
GPH2	SENBAT_V
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	VDD_CORE_ON
GPH6	EC_VID4

del VGA_TEMP

ITE8512E GPIO	
GPIO0	BATT_TEMP
GPIO1	ADAPTOR_I
GPIO2	BAT_V
GPIO3	CPPE#
GPIO4	BAT_I
GPIO5	EC_CPU_PWR
GPIO6	DDR2_TEMP
GPIO7	ADAP_IN
GPJ0	EC_BRGHT
GPJ1	CHG_I
GPJ2	FAN_CTRL0
GPJ3	SILENT_LED
GPJ4	SMP1_EN#
GPJ5	PM_THROTTLING#

CPU				
	CPU CORE (V)	ICC (mA)	W	TEMP ()
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81
VCC	ICC (mA)	W	TEMP ()	
+1.5V	120	0.18		
+1.05V	2500	2.625	70	

672MX				
	VCC	ICC (mA)	W	TEMP ()
	+1.2V	2303	2.76	
	+1.8V	1215	2.18	70
	+1.05V	80	0.084	

SIS968				
	VCC	ICC (mA)	W	TEMP ()
	+3.3V	86	0.283	
	+1.8V	851	1.531	70
	+1.05V	22	0.022	

307LV				
	VCC	ICC (mA)	W	TEMP ()
	+3.3V	236	1.107	
	+1.8V	565	0.778	70

CLOCK GENERATOR+BUFFER			
VCC	ICC (mA)	W	TEMP ()
+3.3V	400	1.32	70
+1.8V	300	0.54	

ITE8512E			
VCC	ICC (mA)	W	TEMP ()
+3.3V	200	0.66	70
+3.3VA	500	1.65	

RTS5158			
VCC	ICC (mA)	W	TEMP ()
+5V	76	0.38	85

RTL8201CL			
VCC	ICC (mA)	W	TEMP ()
+3.3V	20	0.396	85

ALC662			
VCC	ICC (mA)	W	TEMP ()
+3.3V	23	0.075	70
+5VA	38	0.19	

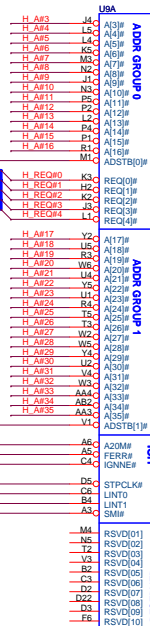
APA2068			
VCC	ICC (mA)	W	TEMP ()
5V	20	0.1	85

ADM1032			
VCC	ICC	W	TEMP ()
+3.3V	170uA	0.56mW	150

SMART POWER TABLE

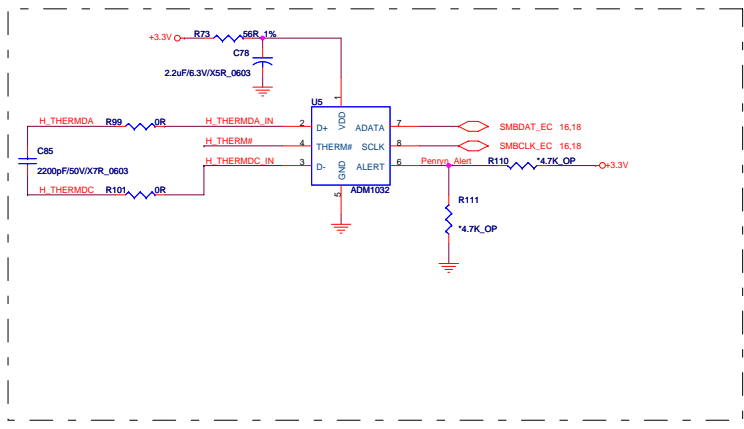
VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

7 H_ADSTB#0
7 H_REQ#(0,4)

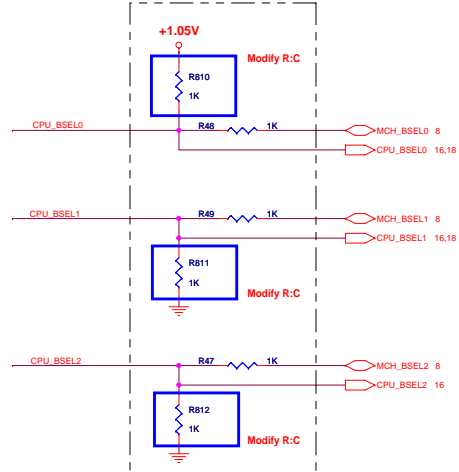


Merom Ball-out Rev 1a

CPU Thermal Sensor

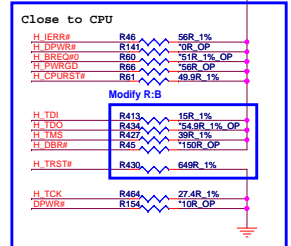
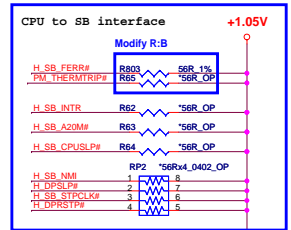
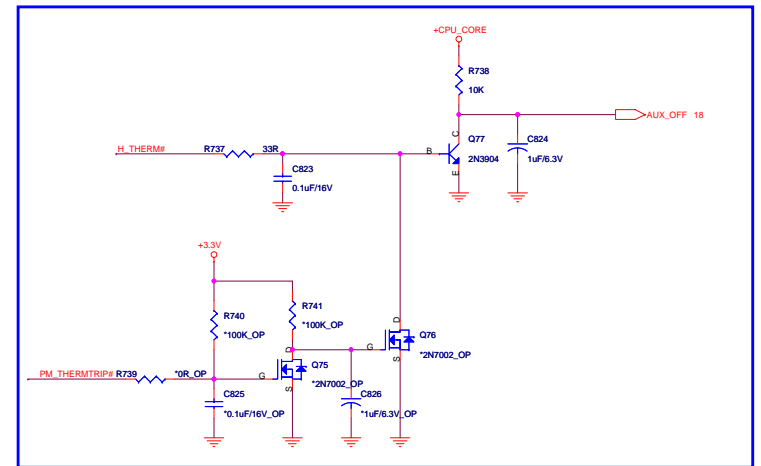


Close to NB

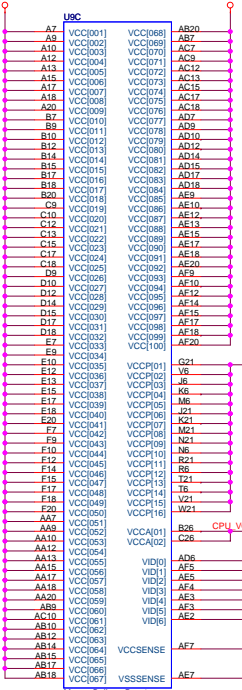


	BSEL2	BSEL1	BSEL0	MHZ
FSB800	0	1	0	200
FSB667	0	1	1	166
FSB533	0	0	1	133

Modify R:B



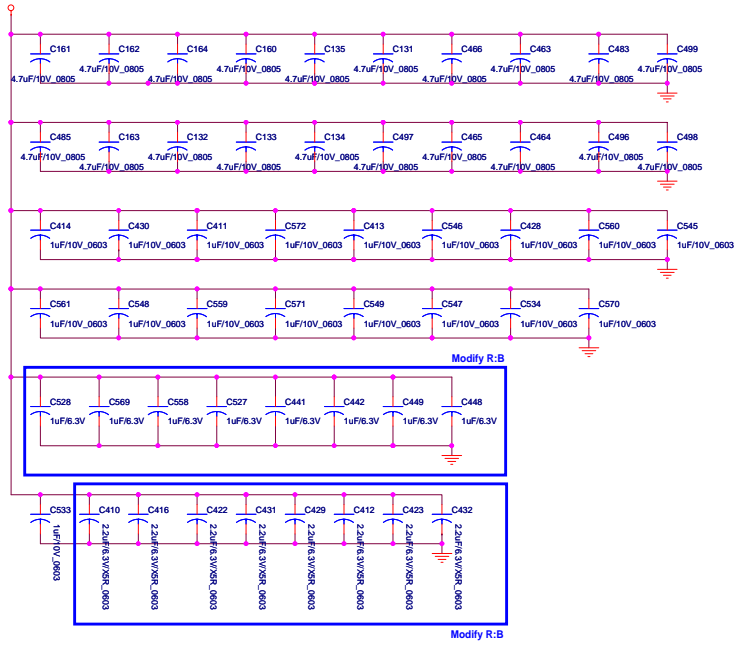
+CPU_CORE



+CPU_CORE



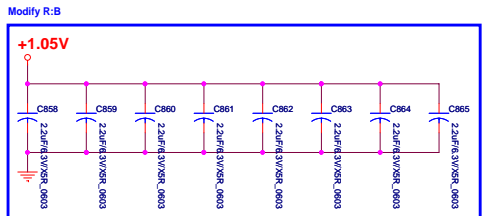
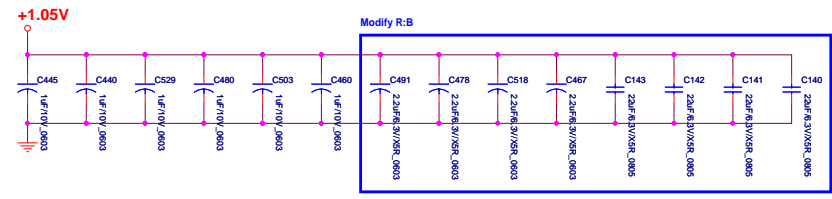
+CPU_CORE

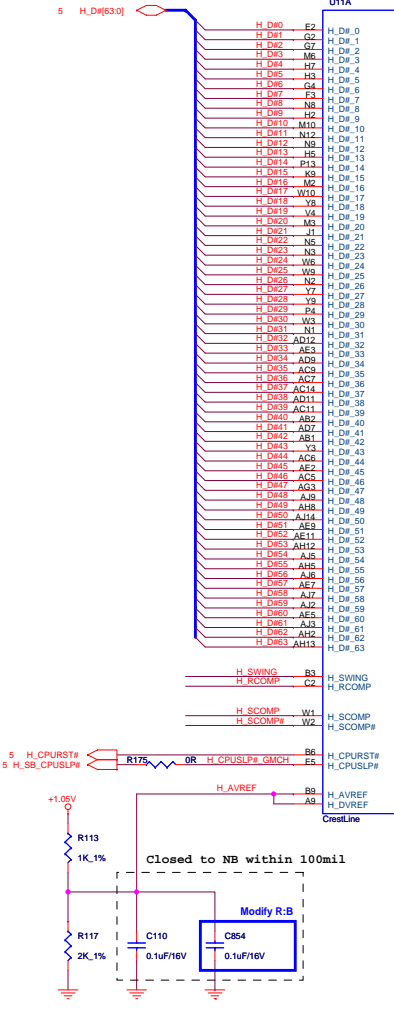
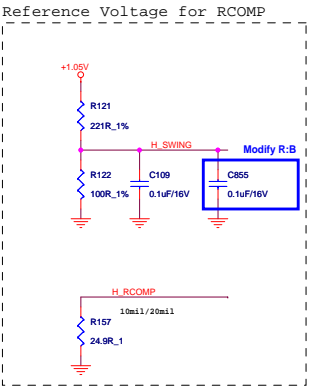
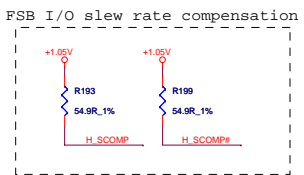
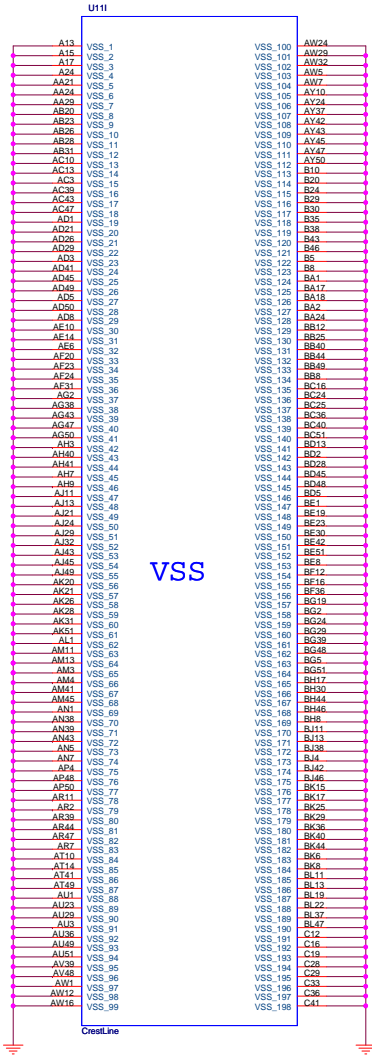


U80

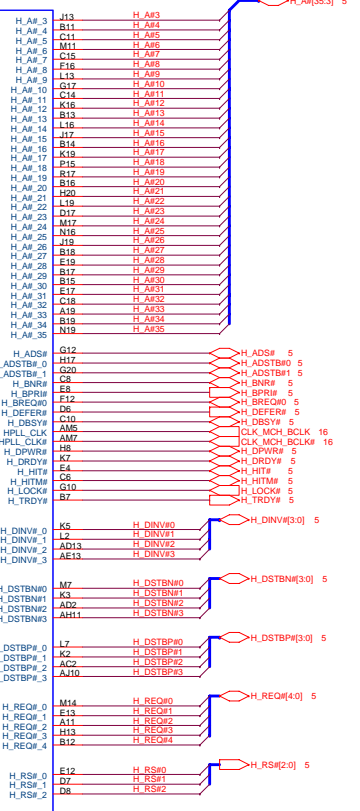
A4	VSS(001)	VSS(082)	P6
A6	VSS(002)	VSS(083)	P21
A11	VSS(003)	VSS(084)	P24
A14	VSS(004)	VSS(085)	R2
A16	VSS(005)	VSS(086)	R5
A19	VSS(006)	VSS(087)	R22
A23	VSS(007)	VSS(088)	R25
A24	VSS(008)	VSS(089)	T1
B6	VSS(009)	VSS(090)	T4
B8	VSS(010)	VSS(091)	T23
B11	VSS(011)	VSS(092)	T26
B13	VSS(012)	VSS(093)	U3
B16	VSS(013)	VSS(094)	U21
B19	VSS(014)	VSS(095)	U2
B21	VSS(015)	VSS(096)	U24
B24	VSS(016)	VSS(097)	V5
C5	VSS(017)	VSS(098)	V22
C8	VSS(018)	VSS(099)	V25
C11	VSS(019)	VSS(100)	W1
C14	VSS(020)	VSS(101)	W4
C19	VSS(021)	VSS(102)	W23
C22	VSS(022)	VSS(103)	W26
C25	VSS(023)	VSS(104)	X3
C27	VSS(024)	VSS(105)	Y2
D1	VSS(025)	VSS(106)	Y6
D4	VSS(026)	VSS(107)	Y24
D8	VSS(027)	VSS(108)	AA2
D11	VSS(028)	VSS(109)	AA5
D13	VSS(029)	VSS(110)	AA8
D16	VSS(030)	VSS(111)	AA11
D18	VSS(031)	VSS(112)	AA14
D21	VSS(032)	VSS(113)	AA17
D23	VSS(033)	VSS(114)	AA19
D26	VSS(034)	VSS(115)	AA22
E3	VSS(035)	VSS(116)	AA25
E6	VSS(036)	VSS(117)	AB1
E8	VSS(037)	VSS(118)	AB4
E11	VSS(038)	VSS(119)	AB8
E16	VSS(039)	VSS(120)	AB11
E19	VSS(040)	VSS(121)	AB13
E21	VSS(041)	VSS(122)	AB16
E24	VSS(042)	VSS(123)	AB19
F5	VSS(043)	VSS(124)	AB23
F8	VSS(044)	VSS(125)	AB26
F11	VSS(045)	VSS(126)	AC6
F16	VSS(046)	VSS(127)	AC3
F19	VSS(047)	VSS(128)	AC6
F21	VSS(048)	VSS(129)	AC11
F24	VSS(049)	VSS(130)	AC14
F27	VSS(050)	VSS(131)	AC16
F29	VSS(051)	VSS(132)	AC19
G4	VSS(052)	VSS(133)	AC21
G7	VSS(053)	VSS(134)	AC24
G11	VSS(054)	VSS(135)	AD2
G23	VSS(055)	VSS(136)	AD5
G26	VSS(056)	VSS(137)	AD8
H4	VSS(057)	VSS(138)	AD11
H5	VSS(058)	VSS(139)	AD13
H21	VSS(059)	VSS(140)	AD16
J2	VSS(060)	VSS(141)	AD19
J5	VSS(061)	VSS(142)	AD22
J6	VSS(062)	VSS(143)	AE1
J25	VSS(063)	VSS(144)	AE4
K1	VSS(064)	VSS(145)	AE8
K4	VSS(065)	VSS(146)	AE11
K23	VSS(066)	VSS(147)	AE14
K26	VSS(067)	VSS(148)	AE16
L3	VSS(068)	VSS(149)	AE19
L6	VSS(069)	VSS(150)	AE23
L21	VSS(070)	VSS(151)	AE26
L24	VSS(071)	VSS(152)	AF1
M2	VSS(072)	VSS(153)	AF4
M5	VSS(073)	VSS(154)	AF8
M9	VSS(074)	VSS(155)	AF11
M22	VSS(075)	VSS(156)	AF13
M25	VSS(076)	VSS(157)	AF16
N1	VSS(077)	VSS(158)	AF19
N4	VSS(078)	VSS(159)	AF21
N23	VSS(079)	VSS(160)	AF24
N26	VSS(080)	VSS(161)	AF26
P3	VSS(081)	VSS(162)	AF25

Merom Ball-out Rev 1a



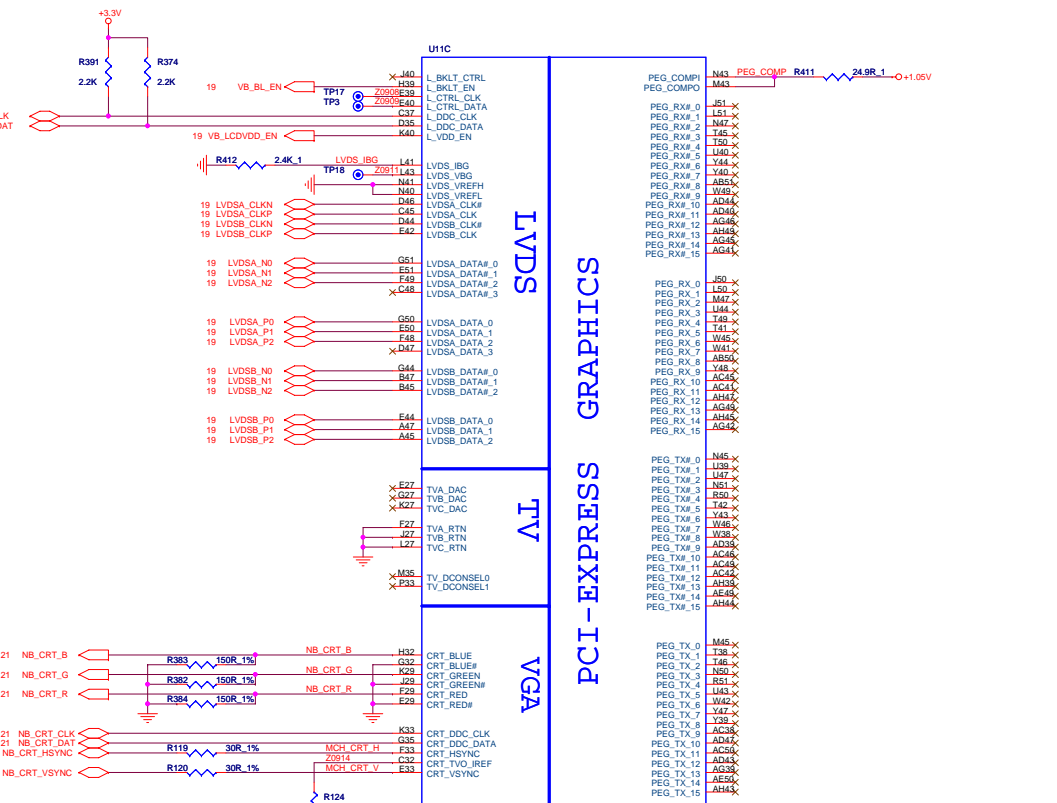
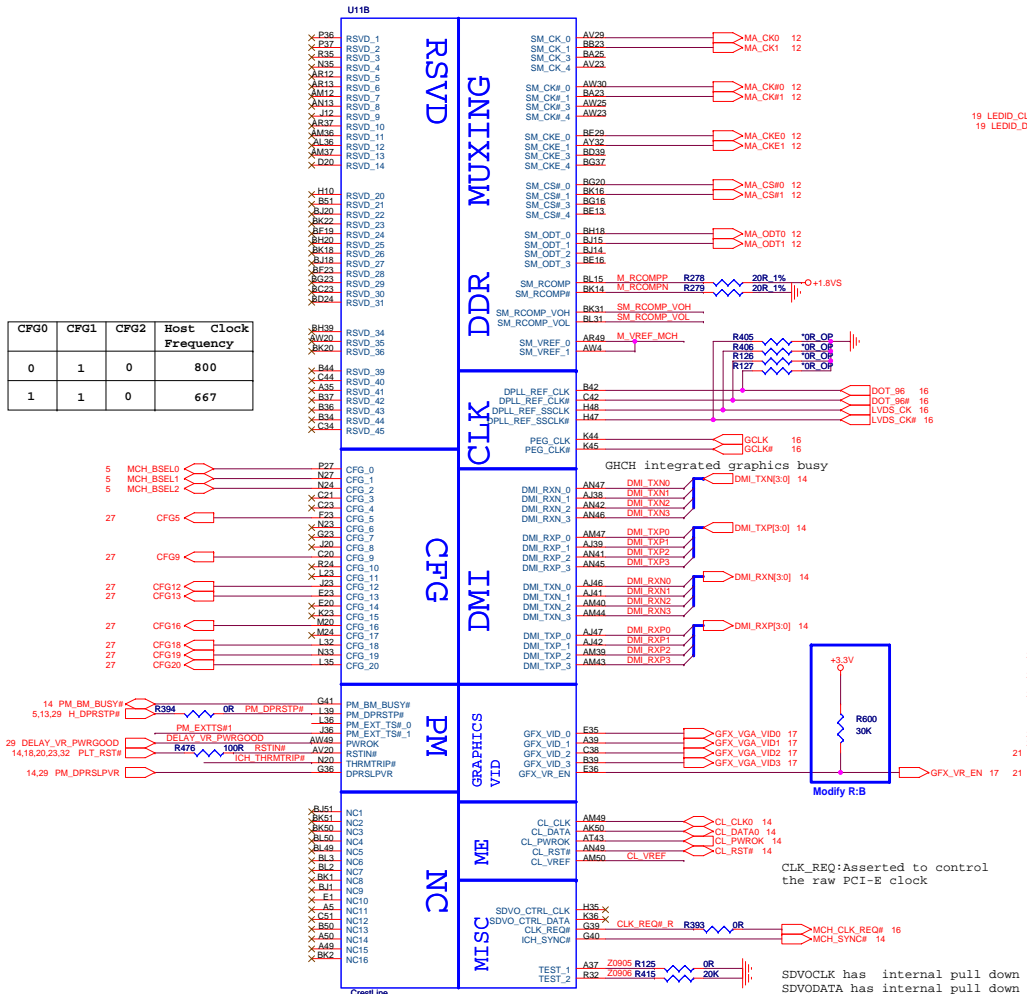


HOST



GCLK => PCI-E & DMI (100MHZ)
 DREFCLK => Display PLLA (nun-ss 96MHZ)
 DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

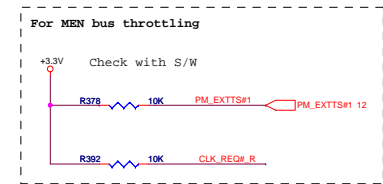
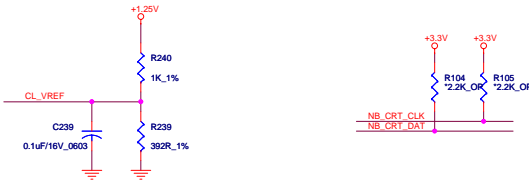
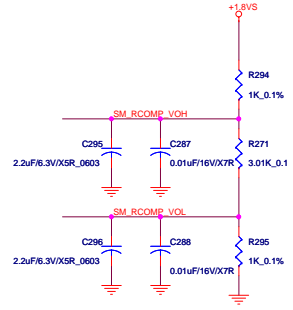
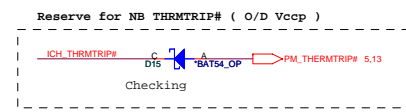
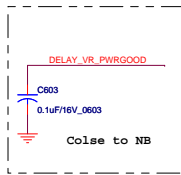
CFG0	CFG1	CFG2	Host Clock Frequency
0	1	0	800
1	1	0	667



CFG20 (IPD) => 1= Only SDVO or PCI-E
 0 = SDVO and PCI-E
 CFG7 (IPU) => 1= Mobility CPU
 0 = Reverse

CLK_REQ: Asserted to control the raw PCI-E clock

SDVOCLK has internal pull down
 SDVO_DATA has internal pull down
 0 = no DVO device
 1 = DVO device present

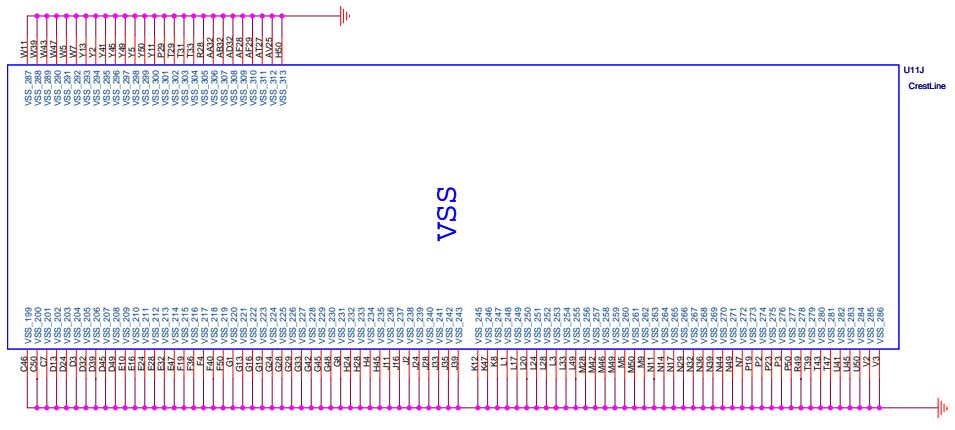


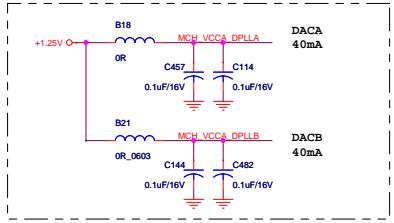
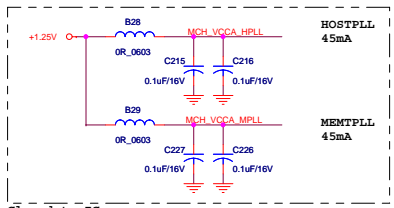
12 MA_DQ[63:0]

MA_D00	AR43	SA_D00
MA_D01	AW44	SA_D01
MA_D02	RA46	SA_D02
MA_D03	AY46	SA_D03
MA_D04	AR41	SA_D04
MA_D05	AR46	SA_D05
MA_D06	AT42	SA_D06
MA_D07	AW47	SA_D07
MA_D08	BB45	SA_D08
MA_D09	BF46	SA_D09
MA_D010	BB47	SA_D010
MA_D011	BJ45	SA_D011
MA_D012	BB47	SA_D012
MA_D013	BG50	SA_D013
MA_D014	BH49	SA_D014
MA_D015	BE46	SA_D015
MA_D016	AW43	SA_D016
MA_D017	BE44	SA_D017
MA_D018	BG42	SA_D018
MA_D019	BE40	SA_D019
MA_D020	BF44	SA_D020
MA_D021	BH45	SA_D021
MA_D022	BG40	SA_D022
MA_D023	BE40	SA_D023
MA_D024	AR40	SA_D024
MA_D025	AW40	SA_D025
MA_D026	AT39	SA_D026
MA_D027	AW36	SA_D027
MA_D028	AW41	SA_D028
MA_D029	AY41	SA_D029
MA_D030	AV38	SA_D030
MA_D031	AT38	SA_D031
MA_D032	AV13	SA_D032
MA_D033	AT13	SA_D033
MA_D034	AW11	SA_D034
MA_D035	AV11	SA_D035
MA_D036	AU15	SA_D036
MA_D037	AT11	SA_D037
MA_D038	BA13	SA_D038
MA_D039	BA11	SA_D039
MA_D040	BE10	SA_D040
MA_D041	BD10	SA_D041
MA_D042	BD8	SA_D042
MA_D043	AY9	SA_D043
MA_D044	BG10	SA_D044
MA_D045	AW9	SA_D045
MA_D046	BD7	SA_D046
MA_D047	BB9	SA_D047
MA_D048	BB5	SA_D048
MA_D049	AV7	SA_D049
MA_D050	AT5	SA_D050
MA_D051	AT7	SA_D051
MA_D052	AY6	SA_D052
MA_D053	BB7	SA_D053
MA_D054	AR5	SA_D054
MA_D055	AR8	SA_D055
MA_D056	AR9	SA_D056
MA_D057	AN3	SA_D057
MA_D058	AM8	SA_D058
MA_D059	AN11	SA_D059
MA_D060	AT9	SA_D060
MA_D061	AN9	SA_D061
MA_D062	AM9	SA_D062
MA_D063	AN11	SA_D063

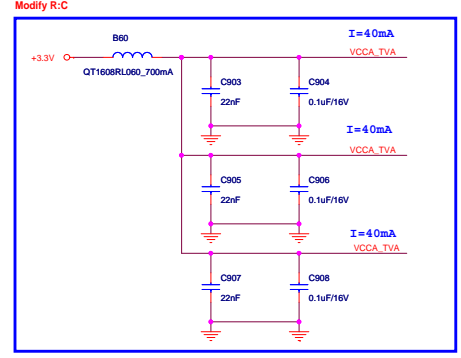
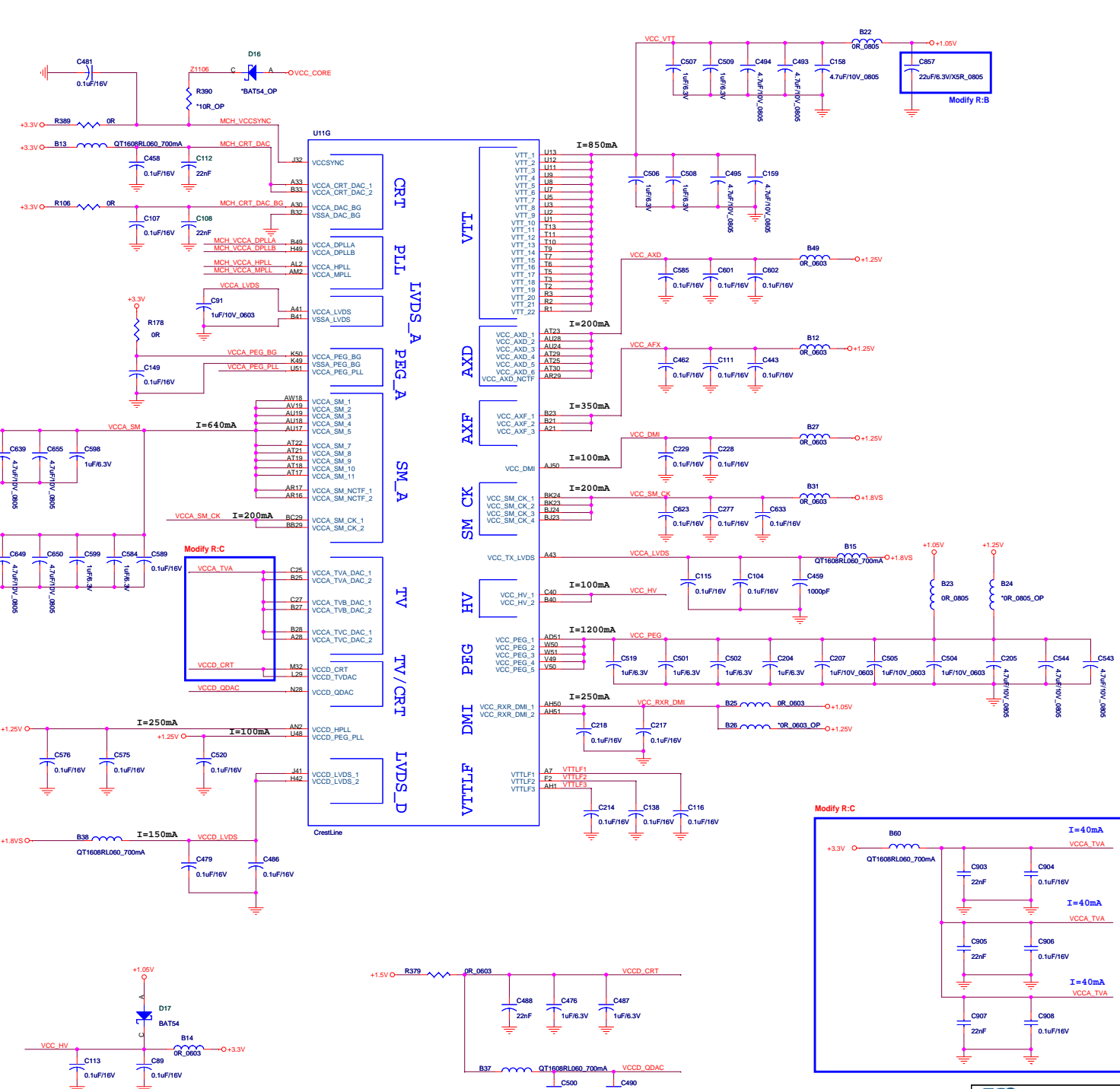
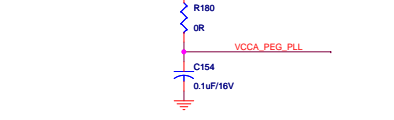
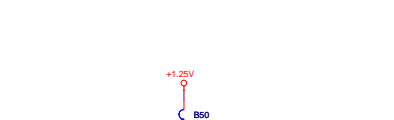
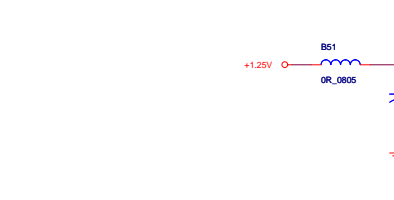
DDR SYSTEM MEMORY A

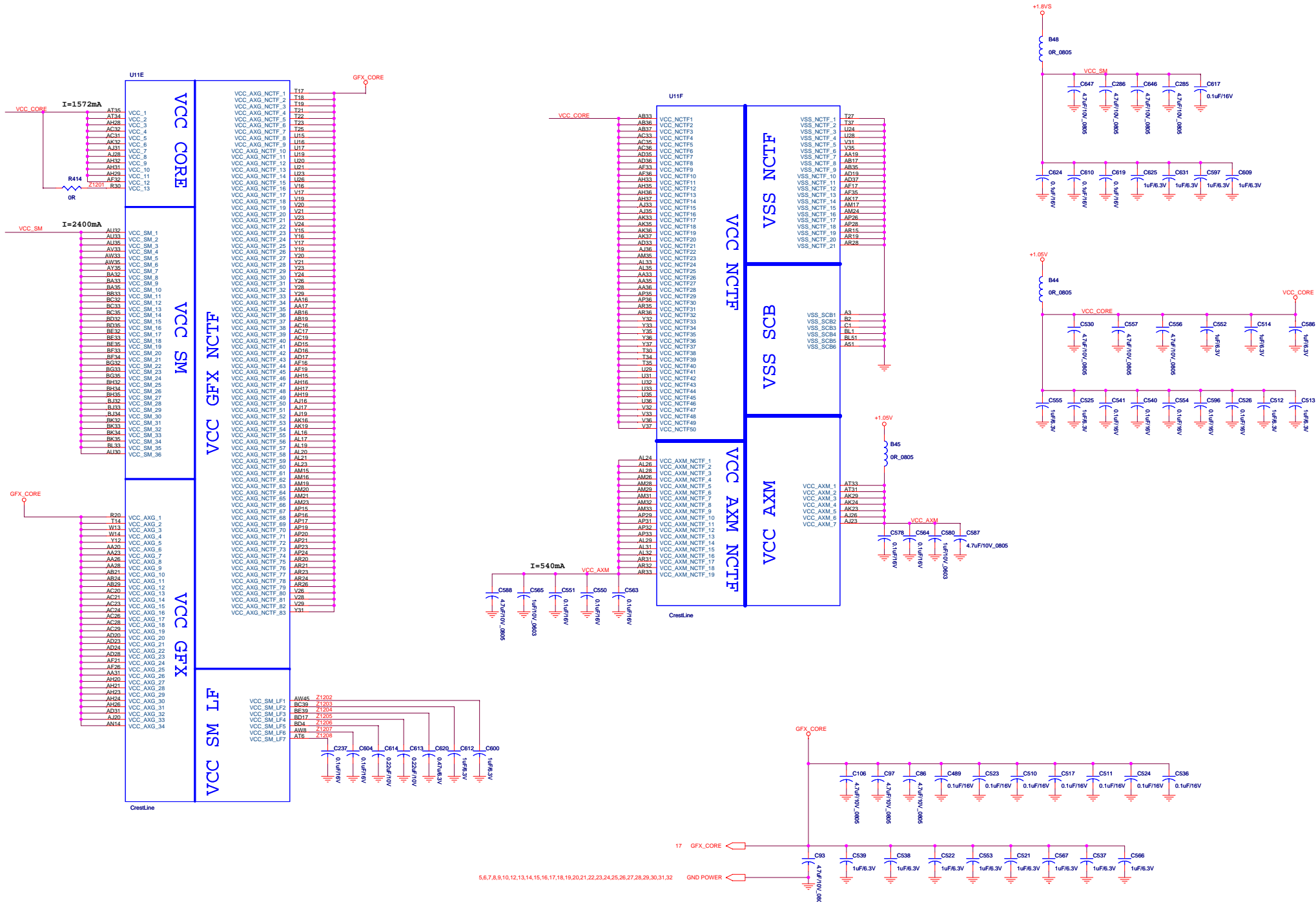
SA_BS_0	BB19	MA_BA0
SA_BS_1	BK19	MA_BA1
SA_BS_2	BP19	MA_BA2
SA_CAS#	BL47	MA_CAS# 12
SA_DM_0	AT45	MA_DM0
SA_DM_1	BD44	MA_DM1
SA_DM_2	BD42	MA_DM2
SA_DM_3	AW38	MA_DM3
SA_DM_4	AW13	MA_DM4
SA_DM_5	RG8	MA_DM5
SA_DM_6	AY5	MA_DM6
SA_DM_7	AN6	MA_DM7
SA_DQS_0	AT46	MA_DQS0
SA_DQS_1	BE48	MA_DQS1
SA_DQS_2	BB43	MA_DQS2
SA_DQS_3	BC37	MA_DQS3
SA_DQS_4	BB16	MA_DQS4
SA_DQS_5	BH6	MA_DQS5
SA_DQS_6	BP2	MA_DQS6
SA_DQS_7	AP3	MA_DQS7
SA_DQS#_0	AT47	MA_DQS#0
SA_DQS#_1	BD47	MA_DQS#1
SA_DQS#_2	BC41	MA_DQS#2
SA_DQS#_3	BA37	MA_DQS#3
SA_DQS#_4	BA16	MA_DQS#4
SA_DQS#_5	BH7	MA_DQS#5
SA_DQS#_6	BC11	MA_DQS#6
SA_DQS#_7	AP2	MA_DQS#7
SA_MA_0	BL19	MAA_A0
SA_MA_1	BD20	MAA_A1
SA_MA_2	BK27	MAA_A2
SA_MA_3	BH28	MAA_A3
SA_MA_4	BL24	MAA_A4
SA_MA_5	BK28	MAA_A5
SA_MA_6	BJ27	MAA_A6
SA_MA_7	BJ25	MAA_A7
SA_MA_8	BL28	MAA_A8
SA_MA_9	BA28	MAA_A9
SA_MA_10	BC19	MAA_A10
SA_MA_11	BE28	MAA_A11
SA_MA_12	BG30	MAA_A12
SA_MA_13	BL16	MAA_A13
SA_MA_14	BJ29	MAA_A14
SA_RAS#	BE18	MA_RAS# 12
SA_RCVEN#	AX29	
SA_WE#	BA19	MA_WE# 12

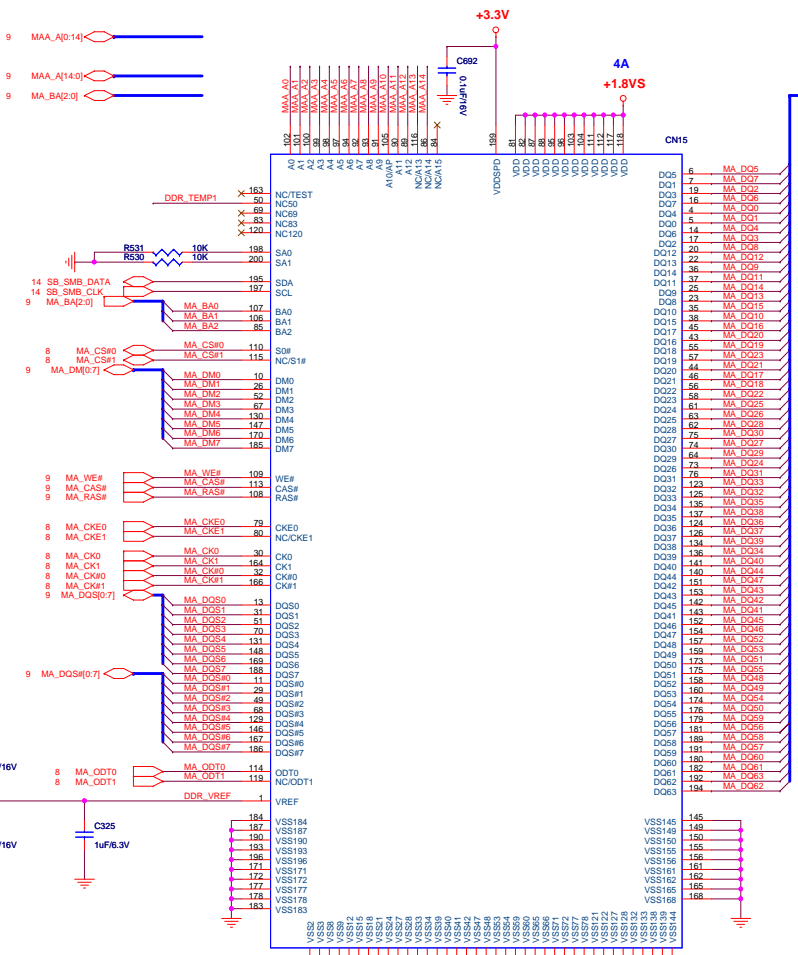




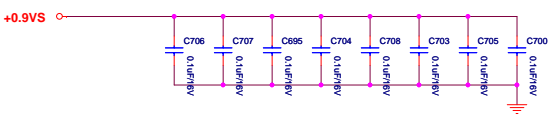
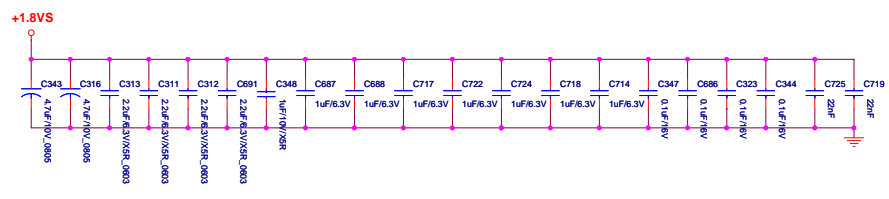
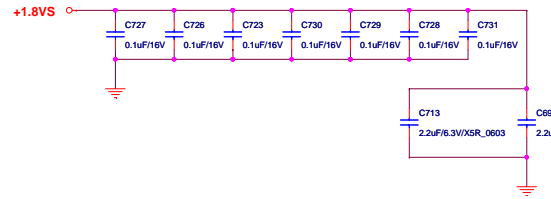
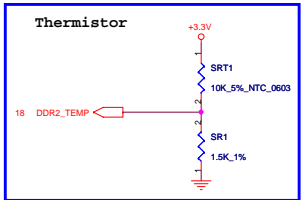
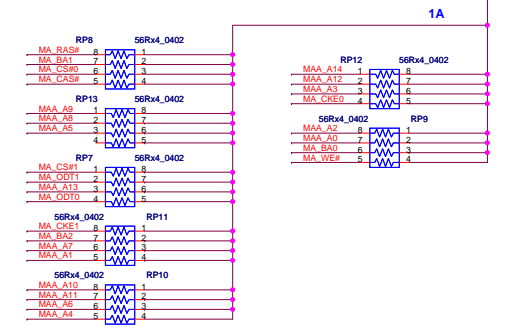
Closed to IC

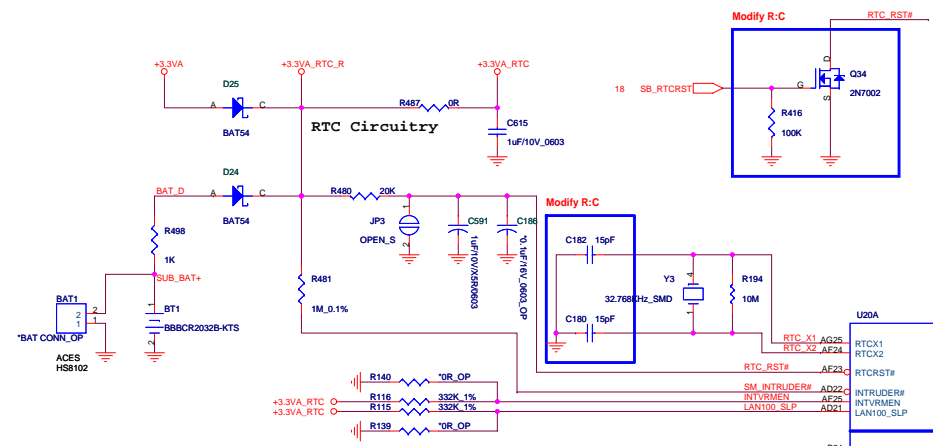






DDR2_Terminate (SWAP RP PIN when layout)

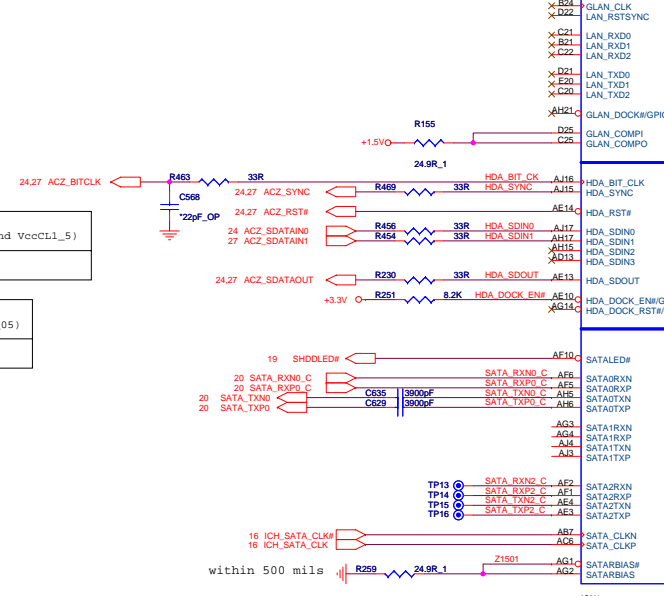




SM_INTRUDER#
 0 = Disable Internal 1.5Vs LDO
 1 = Enable Internal 1.5Vs LDO

ICH8-M Internal VR Enable Strap
 (Internal VR for VccSual_05, VccSual_5 and VccCL1_5)
 Low = Internal VR Disabled
 High = Internal VR Enabled
 (Default)

ICH8-M LAN100_SLP Strap
 (Internal VR for VccLAN1_05 and VccCL1_05)
 Low = Internal VR Disabled
 High = Internal VR Enabled
 (Default)



U20A

RTC

LAN

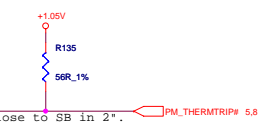
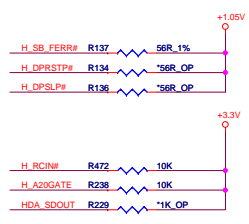
CPU

IHDA

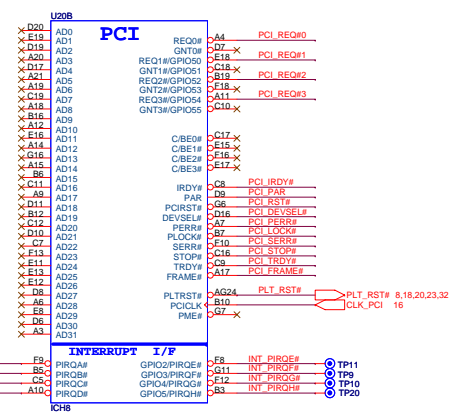
SATA

LPC

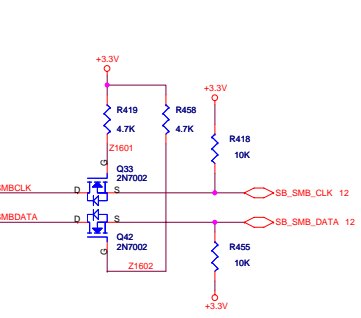
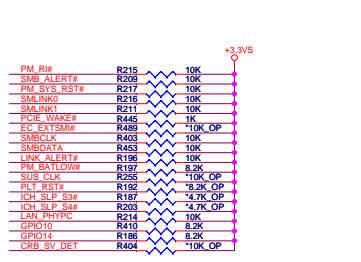
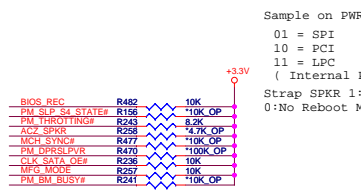
IDE



Intel IRQ14

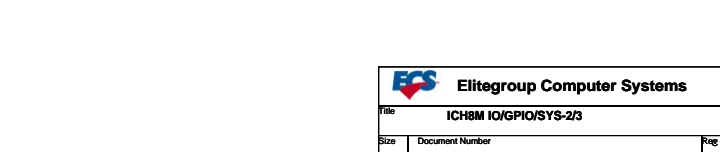
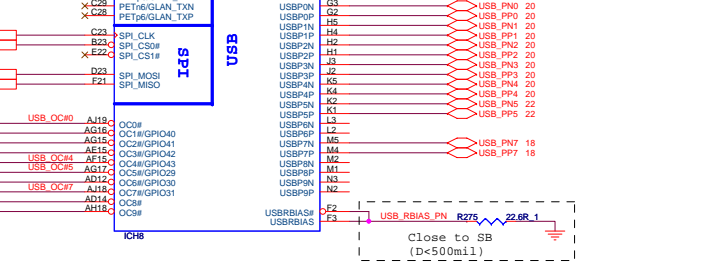
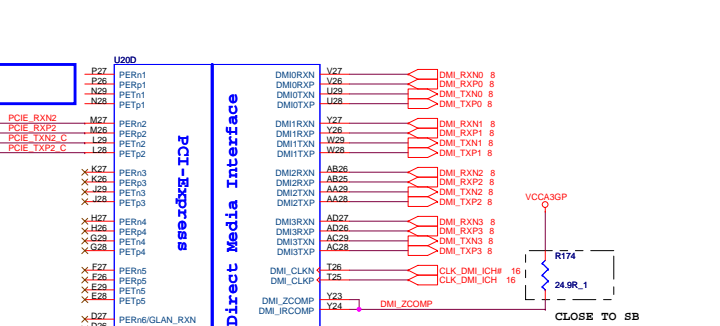
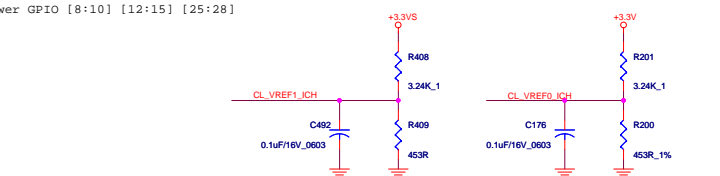
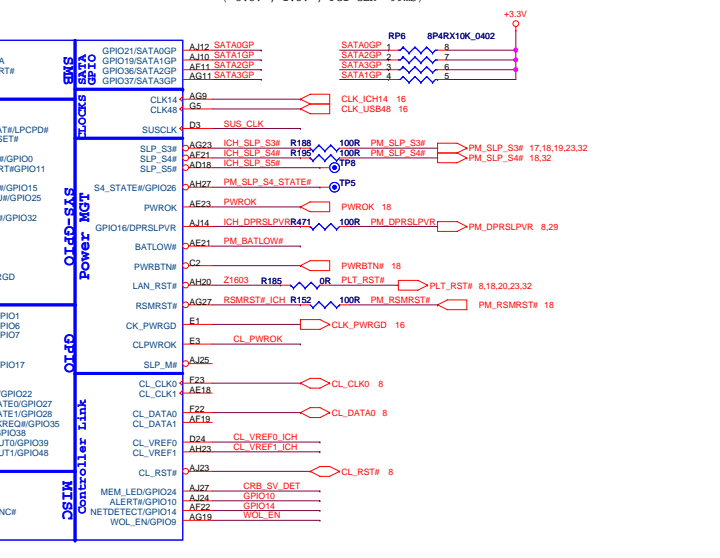
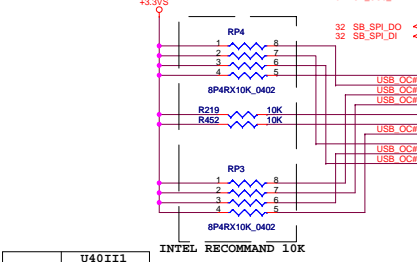
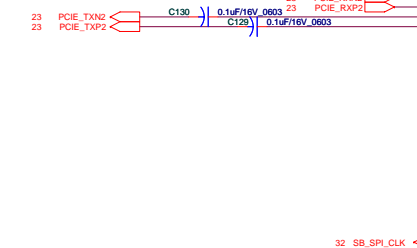
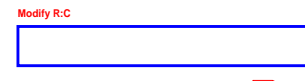
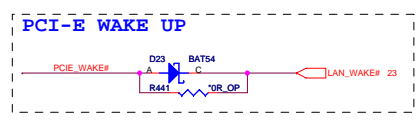


INTA# : NC PREQ#0 : NC
 INTB# : NC PREQ#1 : 1394
 INTC# : 1394 PREQ#2 : NC
 INTD# : (1394) PREQ#3 : NC
 PREQ#4 : NC

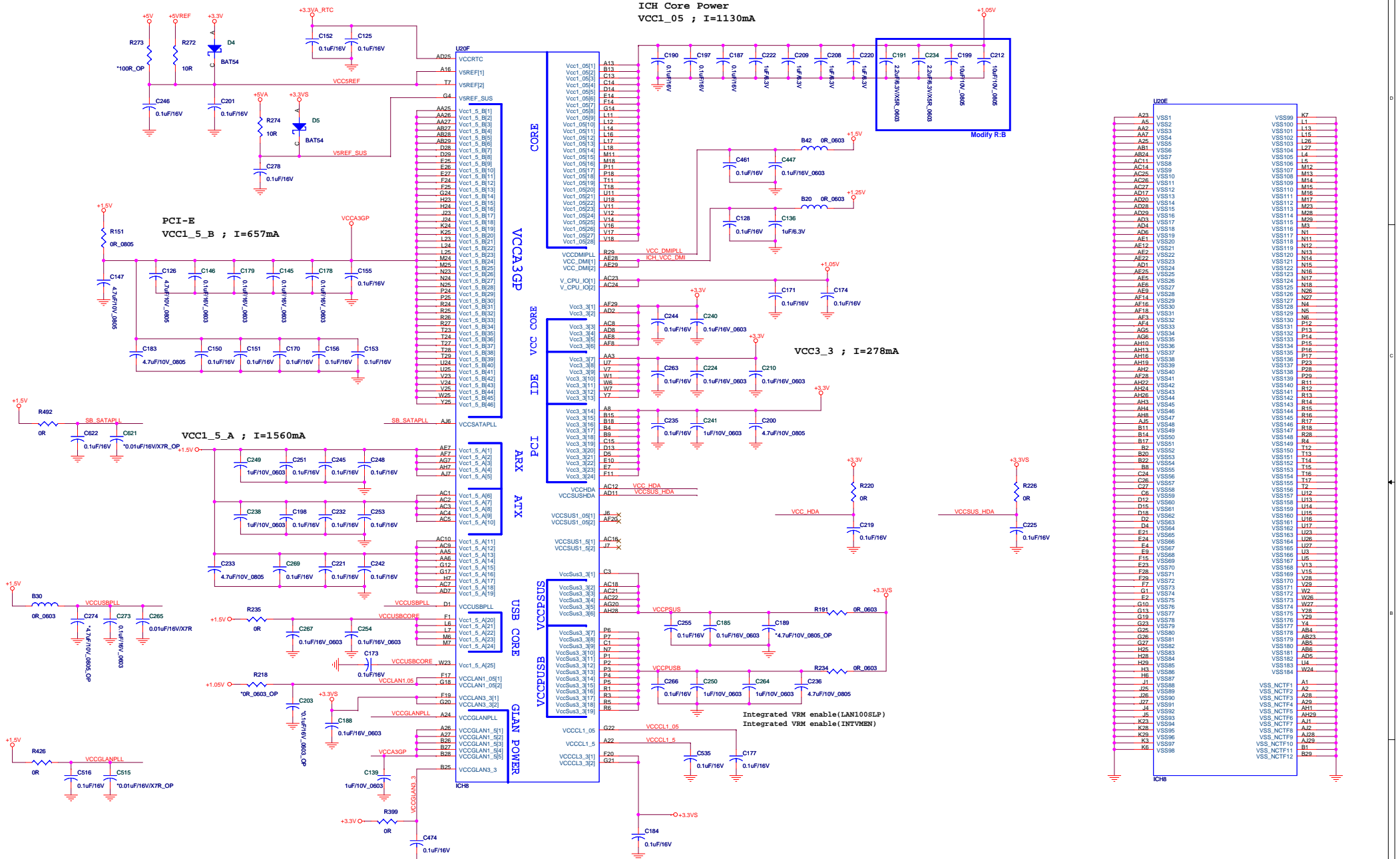


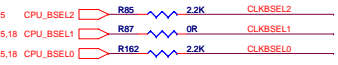
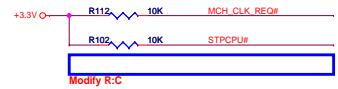
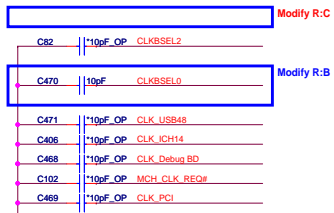
U40I11	
USB0	Mini Card
USB1	USB
USB2	USB
USB3	USB
USB4	USB
USB5	Card Reader
USB6	NC
USB7	CCD
USB8	NC
USB9	NC

U40I11	
PCIE 1	NC
PCIE 2	1.0/1.0 LAN
PCIE 3	NC
PCIE 4	NC
PCIE 5	NC



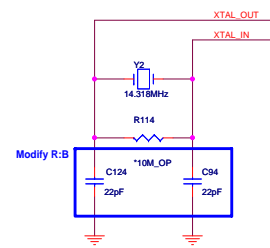
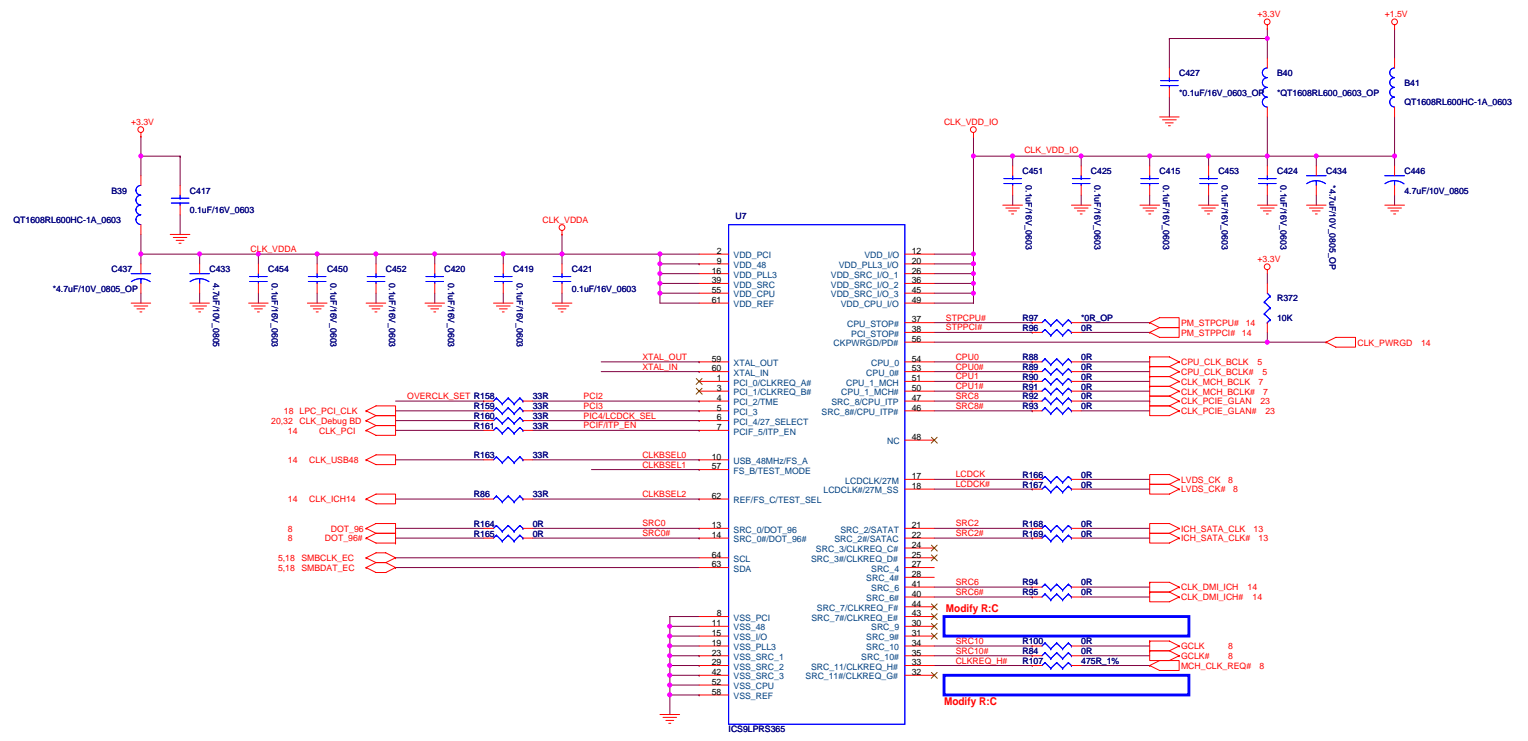
ICH Core Power
VCC1_05 ; I=1130mA





Bsel [0,2] Vil = 0.3 Vih = 0.7

	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ
PSB800	0	1	0	200		
PSB667	0	1	1	166	33	100
PSB533	0	0	1	133		

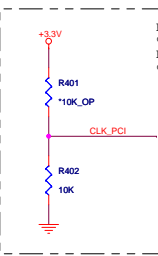


$C_e = 2 * C_L - (C_s + C_i)$
 $C_L =$ Crystal Load Cap = 20p
 $C_i =$ IC internal Cap = 5p
 $C_s =$ 2p
 $C_e =$ Crystal external Cap = 33p

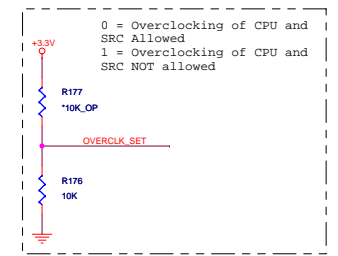
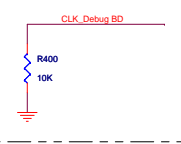
CLK RBQ	From	SRC BUS
C	ICH_SATA	SRC2
G	MINICARD	SRC9
B	LAN 10/100	SRC4
H	MCH_GCLK	SRC10

Pin Configuration

Pin	Signal	Pin	Signal
60	PC0/CRA_1	64	SLK
61	VDDPCI2	65	SDATA
62	PC1/CRA_3	66	REFFSLO/TEST_SEL
63	PC2/ME	67	VDDREF
64	PC3/5	68	XI
65	PC4/27_Sel	69	XC
66	PC5/17P_EN7	70	NDREF
67	PC6/18	71	FS/TEST_MODE
68	PC7/48	72	CLK_PWRGD/PC#
69	USB_48MHz/SA	73	VDDCPU
70	PC8/11	74	CP070
71	PC9/12	75	CPV00
72	SRC10/DTT_56	76	GNDCPU
73	SRC10/DTT_96	77	CPUT1_F
74	GNDS15	78	CPUT1_F
75	VDDPLL3	79	VDDCPU_IO
76	27MHz_NvSS/SRC11	80	NC
77	27MHz_SS/SRC11	81	CPUT2_IP/SR078
78	VDDPLL3_I020	82	CPUT2_IP/SR028
79	SRC12/SATAT1	83	VDDSRC_IO
80	SRC12/SATAT2	84	SRC12/CRA_F
81	SRC12/SATAT3	85	SRC12/CRA_E
82	SRC12/SATAT4	86	GNDSRC
83	SRC12/SATAT5	87	SRC12/CRA_C24
84	SRC12/SATAT6	88	SRC12/CRA_C25
85	SRC12/SATAT7	89	SRC12/CRA_C26
86	SRC12/SATAT8	90	VDDSRC
87	SRC12/SATAT9	91	SRC12/27
88	SRC12/SATAT10	92	SRC12/28
89	SRC12/SATAT11	93	SRC12/29
90	SRC12/SATAT12	94	SRC12/30
91	SRC12/SATAT13	95	SRC12/31
92	SRC12/SATAT14	96	SRC12/32
93	SRC12/SATAT15	97	SRC12/33
94	SRC12/SATAT16	98	SRC12/34
95	SRC12/SATAT17	99	SRC12/35
96	SRC12/SATAT18	100	SRC12/36
97	SRC12/SATAT19	101	SRC12/37
98	SRC12/SATAT20	102	SRC12/38
99	SRC12/SATAT21	103	SRC12/39
100	SRC12/SATAT22	104	SRC12/40
101	SRC12/SATAT23	105	SRC12/41
102	SRC12/SATAT24	106	SRC12/42
103	SRC12/SATAT25	107	SRC12/43
104	SRC12/SATAT26	108	SRC12/44
105	SRC12/SATAT27	109	SRC12/45
106	SRC12/SATAT28	110	SRC12/46
107	SRC12/SATAT29	111	SRC12/47
108	SRC12/SATAT30	112	SRC12/48
109	SRC12/SATAT31	113	SRC12/49
110	SRC12/SATAT32	114	SRC12/50
111	SRC12/SATAT33	115	SRC12/51
112	SRC12/SATAT34	116	SRC12/52
113	SRC12/SATAT35	117	SRC12/53
114	SRC12/SATAT36	118	SRC12/54
115	SRC12/SATAT37	119	SRC12/55
116	SRC12/SATAT38	120	SRC12/56
117	SRC12/SATAT39	121	SRC12/57
118	SRC12/SATAT40	122	SRC12/58
119	SRC12/SATAT41	123	SRC12/59
120	SRC12/SATAT42	124	SRC12/60
121	SRC12/SATAT43	125	SRC12/61
122	SRC12/SATAT44	126	SRC12/62
123	SRC12/SATAT45	127	SRC12/63
124	SRC12/SATAT46	128	SRC12/64
125	SRC12/SATAT47	129	SRC12/65
126	SRC12/SATAT48	130	SRC12/66
127	SRC12/SATAT49	131	SRC12/67
128	SRC12/SATAT50	132	SRC12/68
129	SRC12/SATAT51	133	SRC12/69
130	SRC12/SATAT52	134	SRC12/70
131	SRC12/SATAT53	135	SRC12/71
132	SRC12/SATAT54	136	SRC12/72
133	SRC12/SATAT55	137	SRC12/73
134	SRC12/SATAT56	138	SRC12/74
135	SRC12/SATAT57	139	SRC12/75
136	SRC12/SATAT58	140	SRC12/76
137	SRC12/SATAT59	141	SRC12/77
138	SRC12/SATAT60	142	SRC12/78
139	SRC12/SATAT61	143	SRC12/79
140	SRC12/SATAT62	144	SRC12/80
141	SRC12/SATAT63	145	SRC12/81
142	SRC12/SATAT64	146	SRC12/82
143	SRC12/SATAT65	147	SRC12/83
144	SRC12/SATAT66	148	SRC12/84
145	SRC12/SATAT67	149	SRC12/85
146	SRC12/SATAT68	150	SRC12/86
147	SRC12/SATAT69	151	SRC12/87
148	SRC12/SATAT70	152	SRC12/88
149	SRC12/SATAT71	153	SRC12/89
150	SRC12/SATAT72	154	SRC12/90
151	SRC12/SATAT73	155	SRC12/91
152	SRC12/SATAT74	156	SRC12/92
153	SRC12/SATAT75	157	SRC12/93
154	SRC12/SATAT76	158	SRC12/94
155	SRC12/SATAT77	159	SRC12/95
156	SRC12/SATAT78	160	SRC12/96
157	SRC12/SATAT79	161	SRC12/97
158	SRC12/SATAT80	162	SRC12/98
159	SRC12/SATAT81	163	SRC12/99
160	SRC12/SATAT82	164	SRC12/100



pin7 pull down=pin46/47 for SRC output.
pin7 pull up= pin46/47 for ITP output.

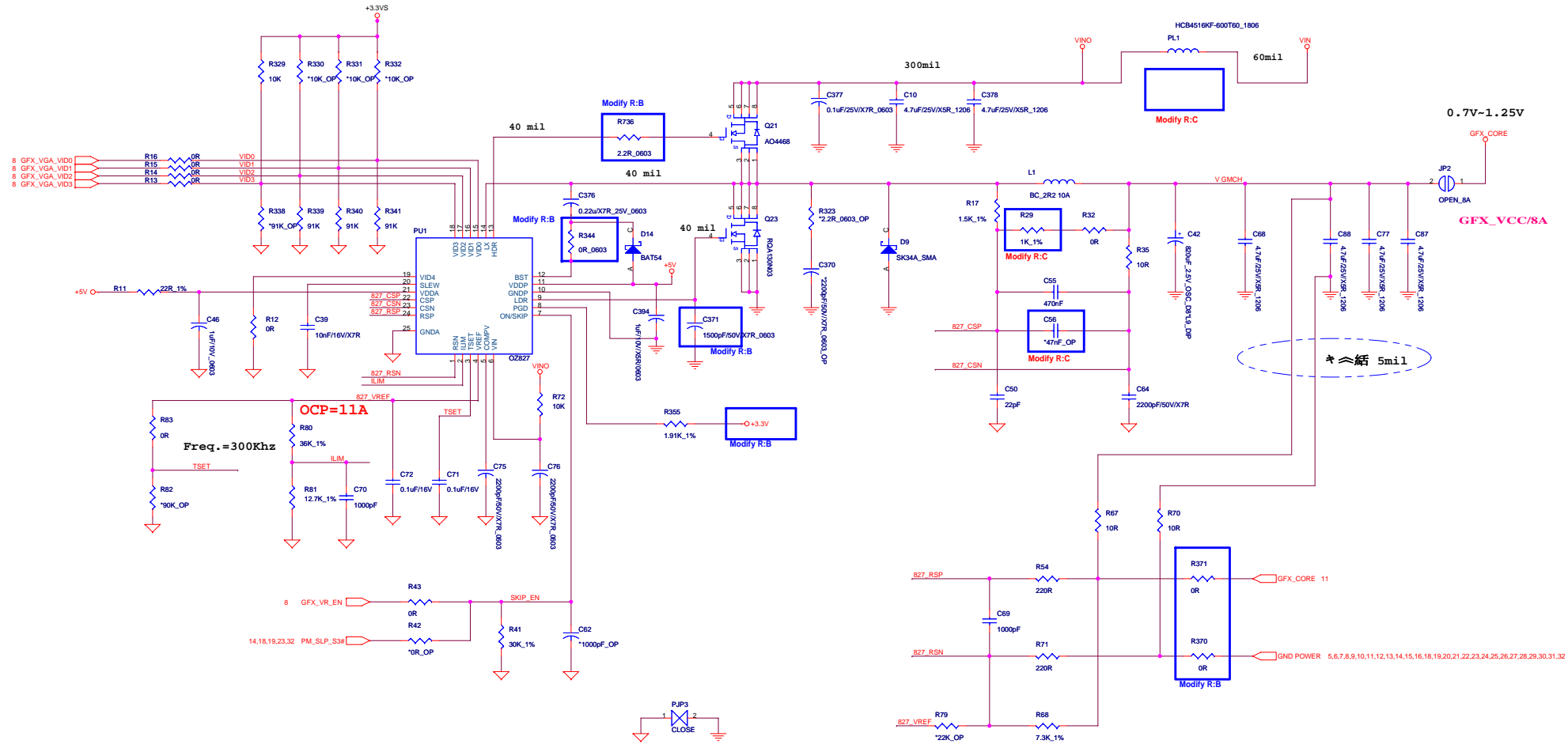


Elitegroup Computer Systems

File: **CLK_GEN (ICS9LPRS365)**

Size: 2555 Document Number

Date: Friday, January 04, 2008 Sheet 16 of 33



LPC: 4Eh-4Fh

RC_IN = KBC RESET

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

Modify R:C

Modify R:B

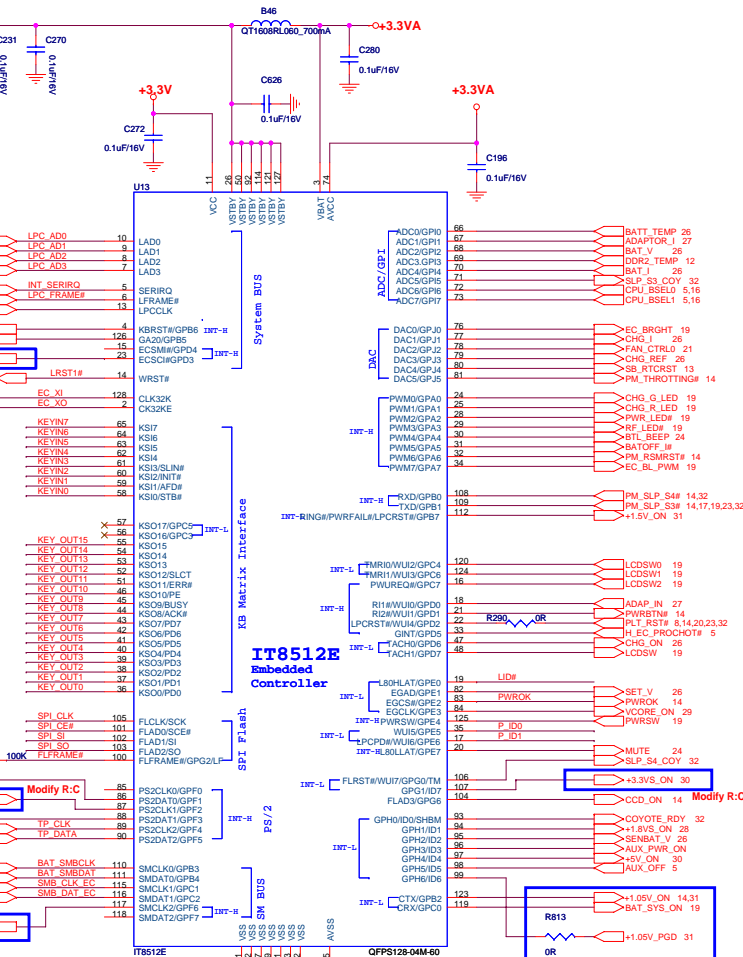
Modify R:C

Modify R:B

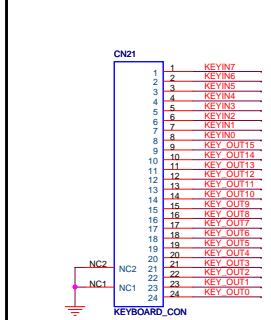
Modify R:C

Modify R:B

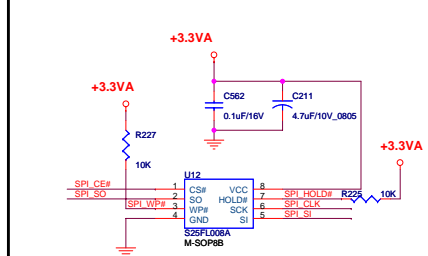
Modify R:C



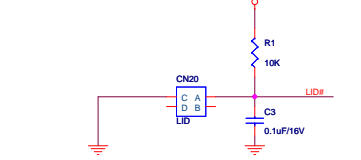
KEYBOARD



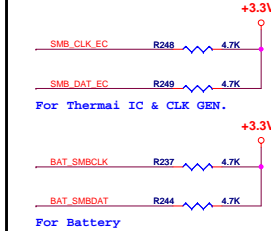
FLASH ROM(SPI)



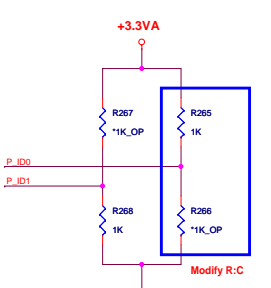
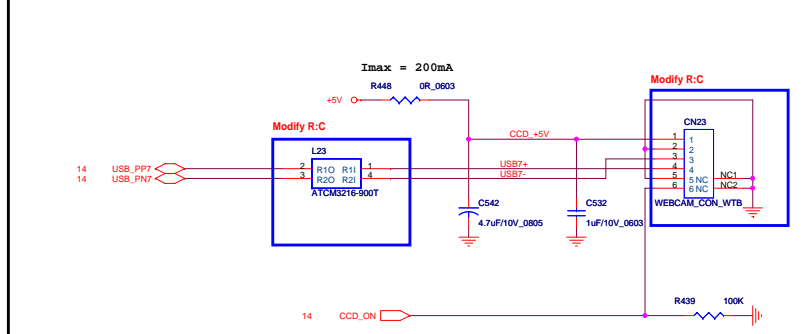
COVER CLOSE



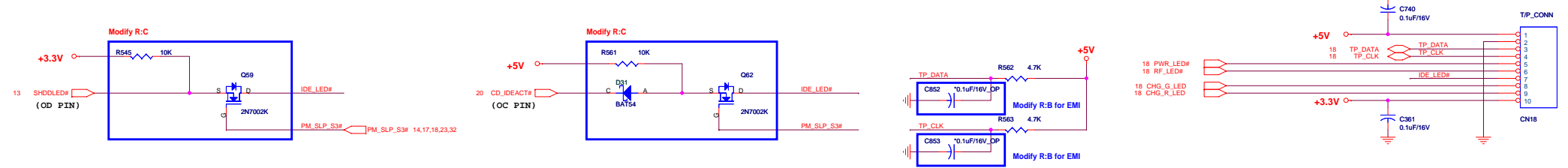
EC SMBUS



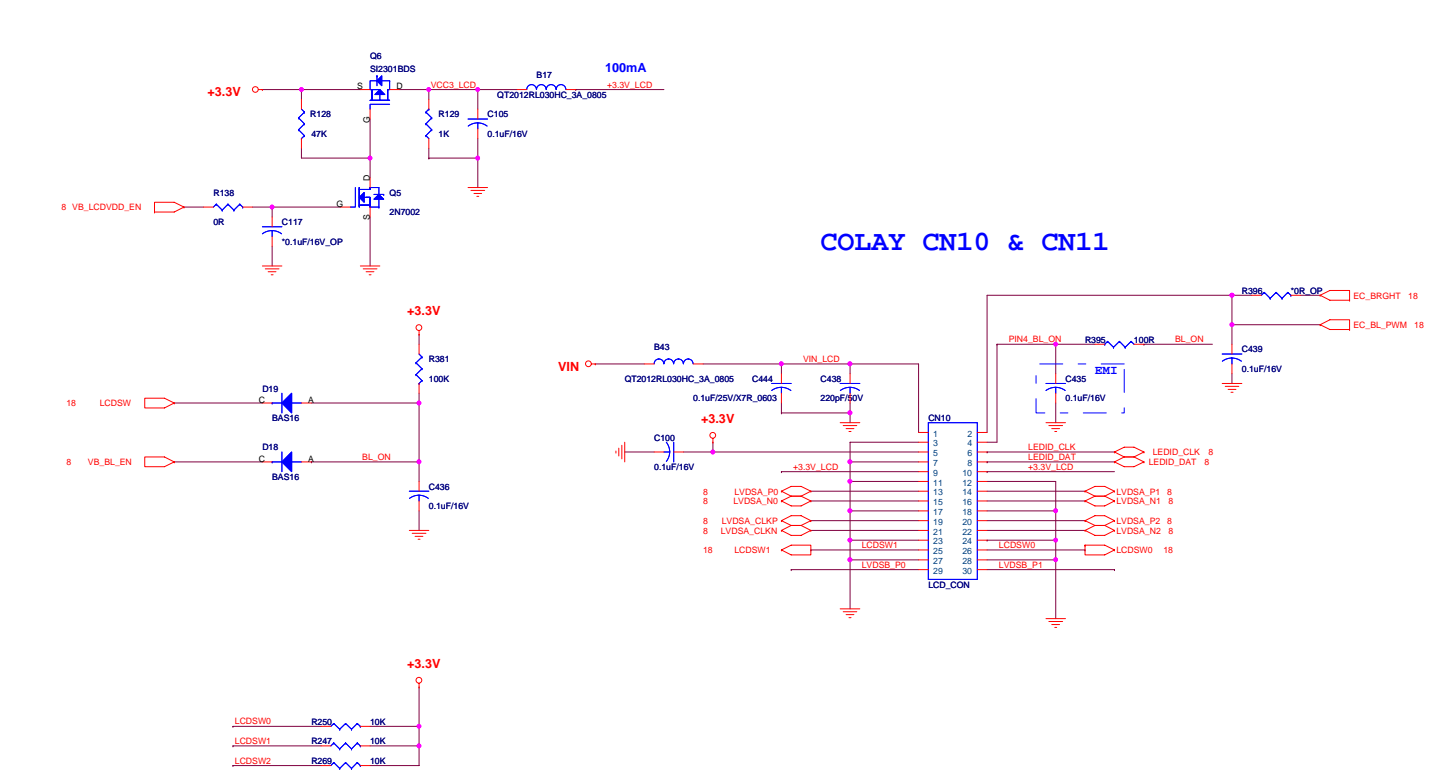
CCD



Touch Pad

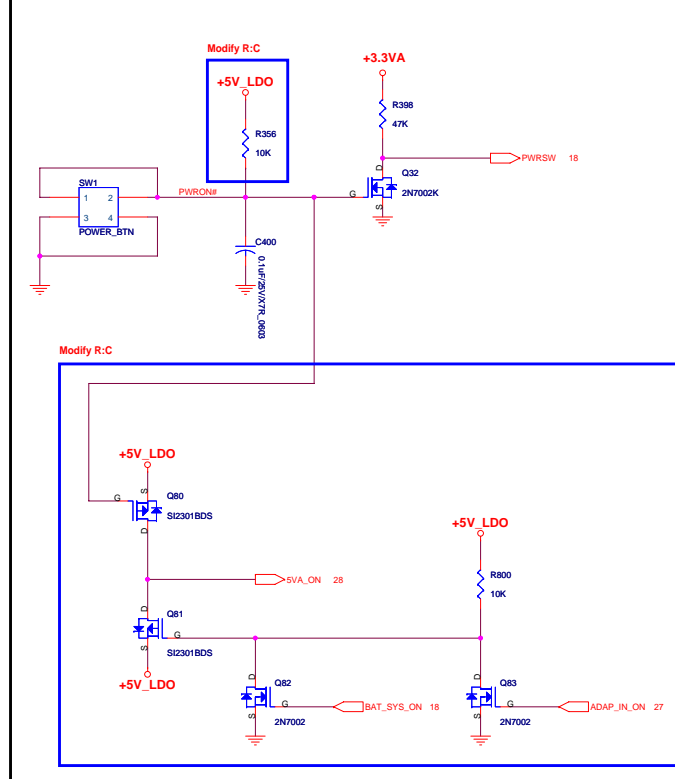


LCD

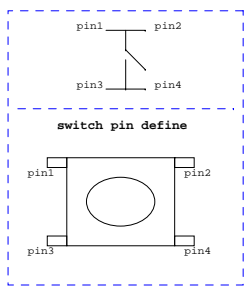


COLAY CN10 & CN11

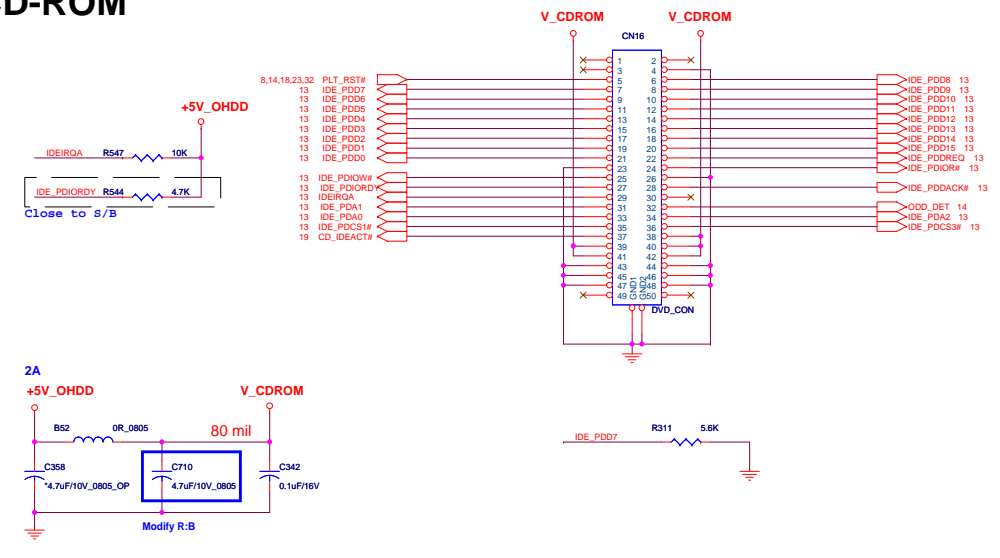
PWR SW



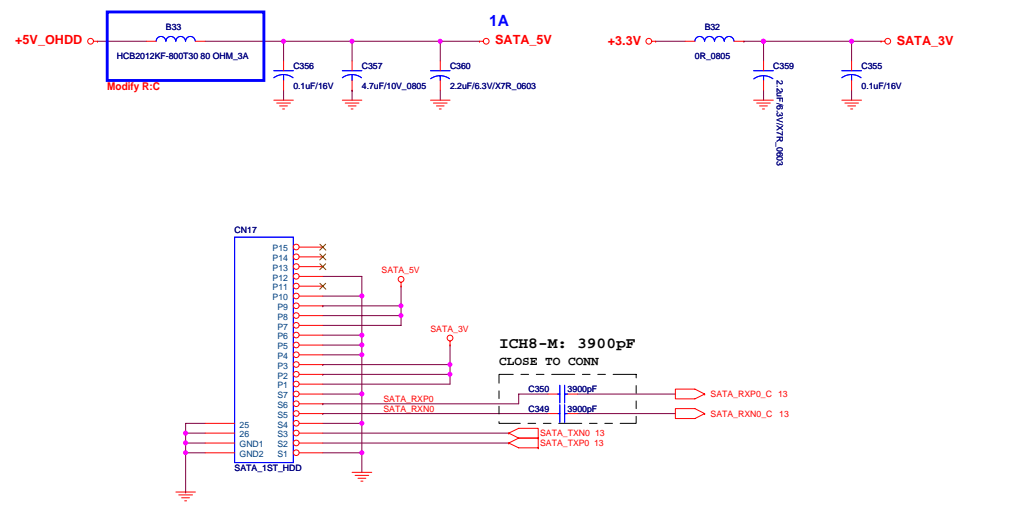
Panel	ID	SW0	SW1	SW2
15"		1	1	1
14"		1	0	1
13"		0	0	1



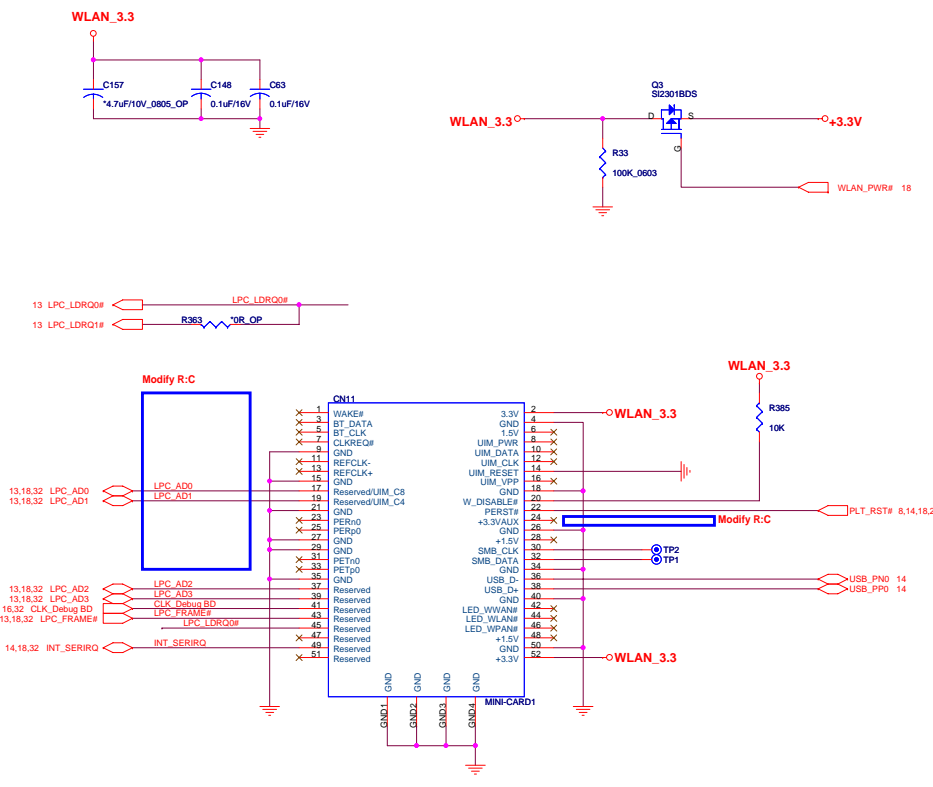
CD-ROM



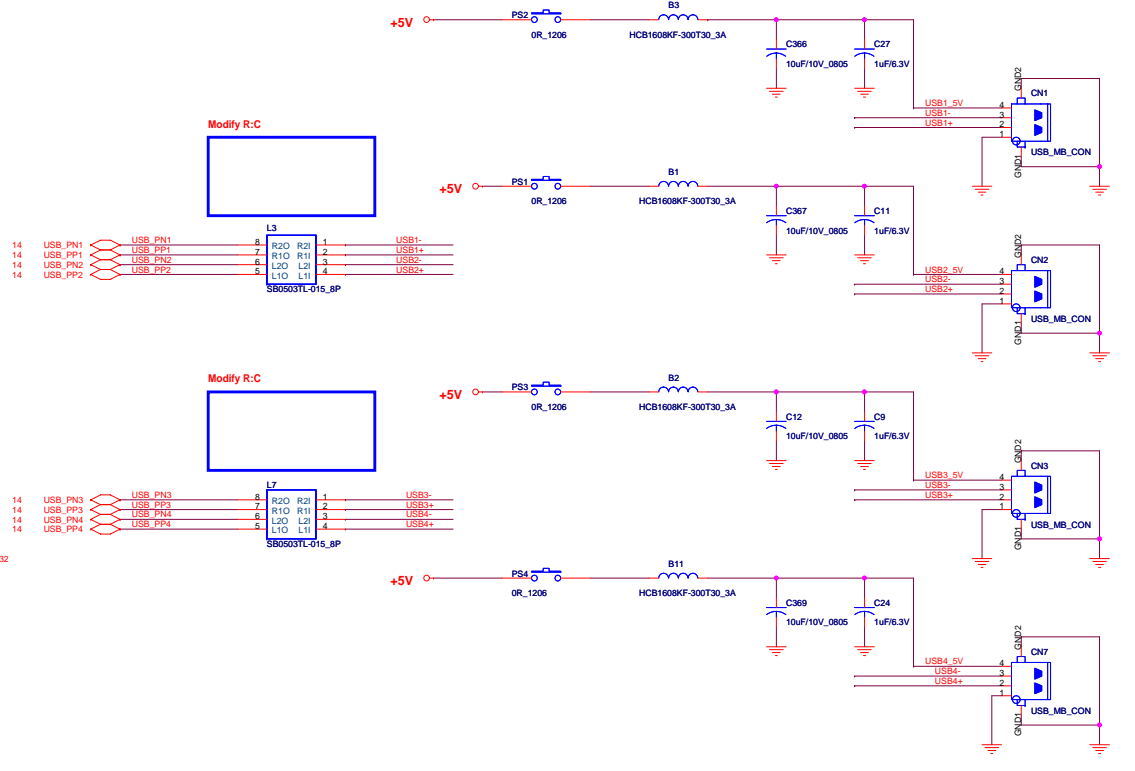
SATA-HDD



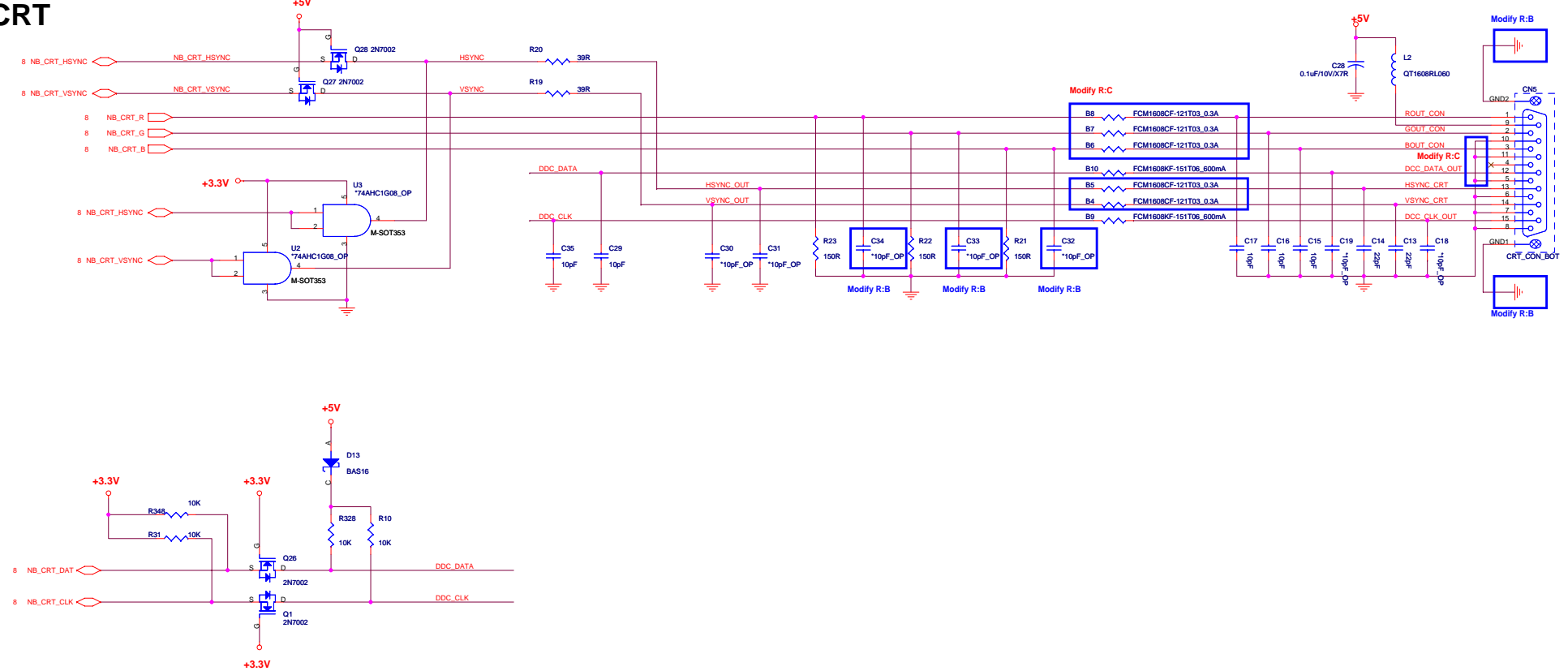
MINI CARD CONN



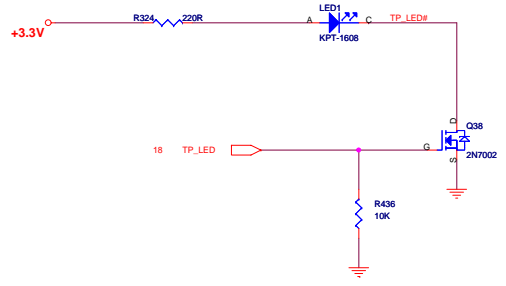
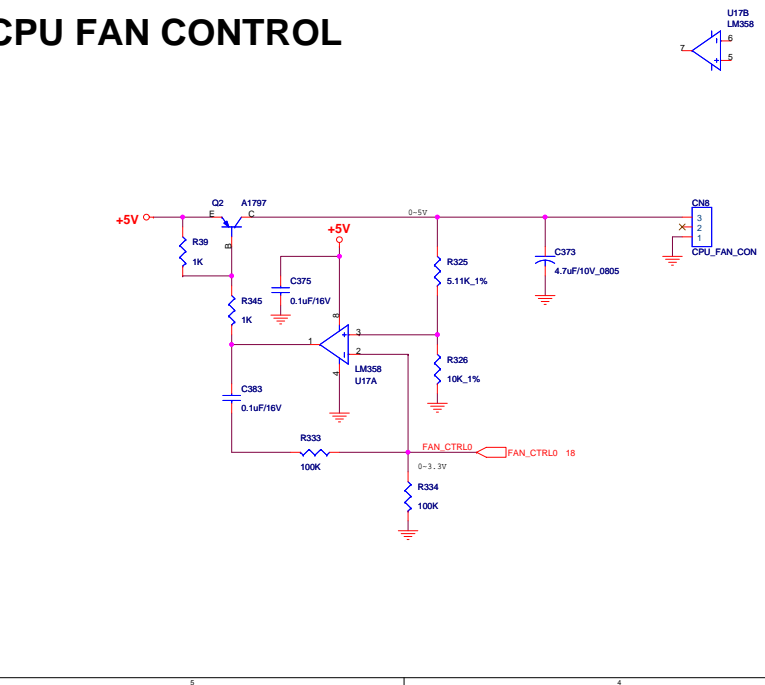
USB Port

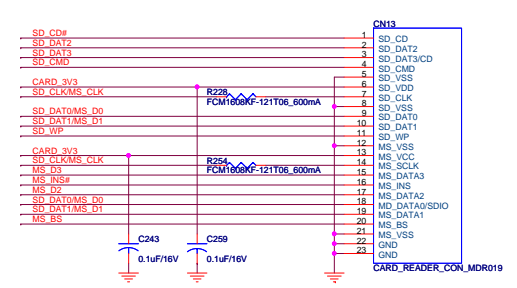
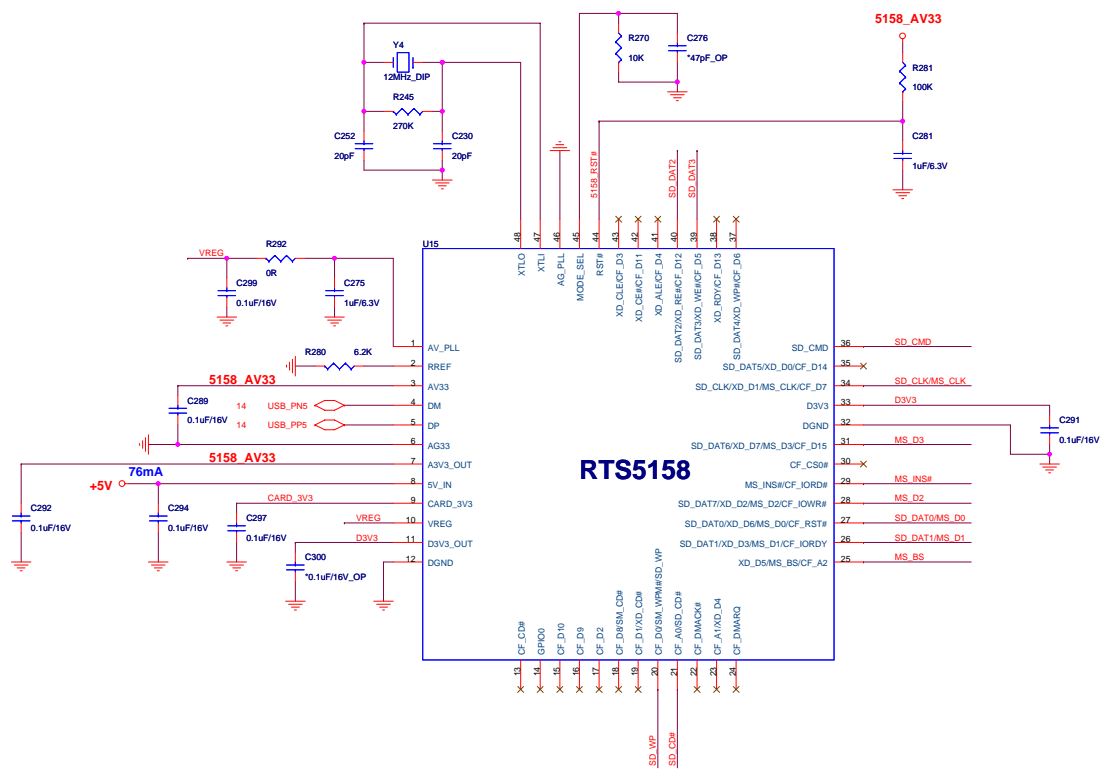


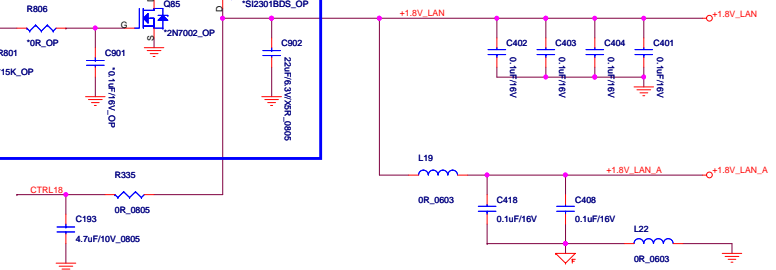
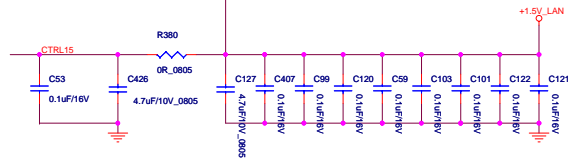
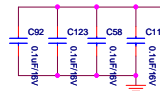
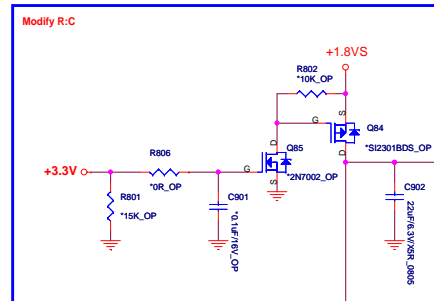
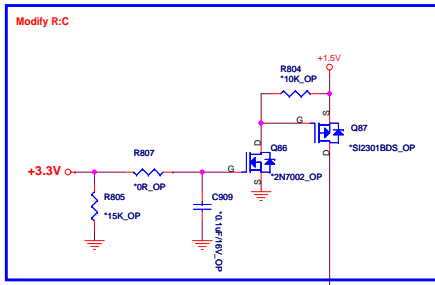
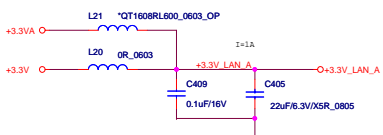
CRT



CPU FAN CONTROL

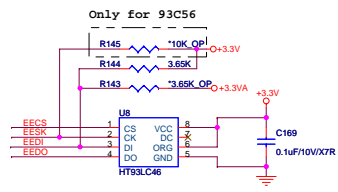
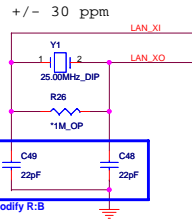
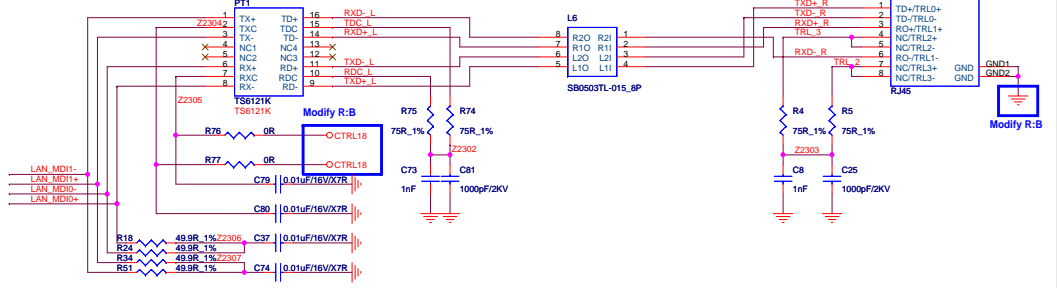
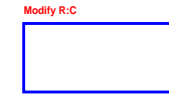
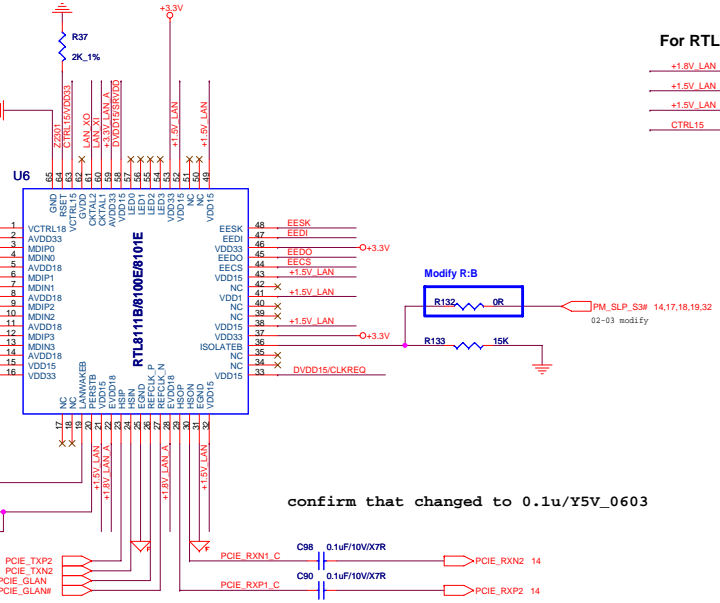
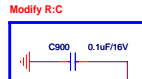
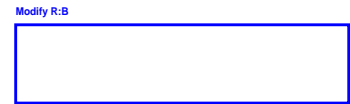






R37 value should be 2.49K (1%) for 8111B/8111C application
R37 should be 2.0K(1%) for 8101E application

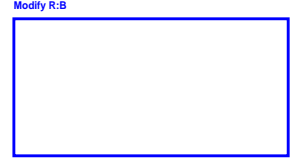
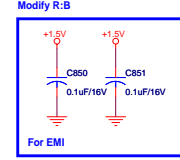
For RTL8111B/8101E application.



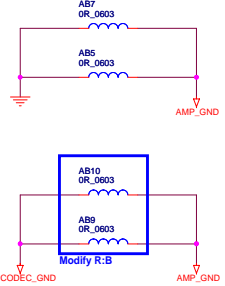
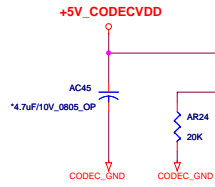
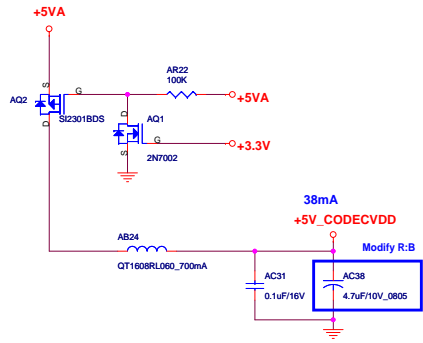
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

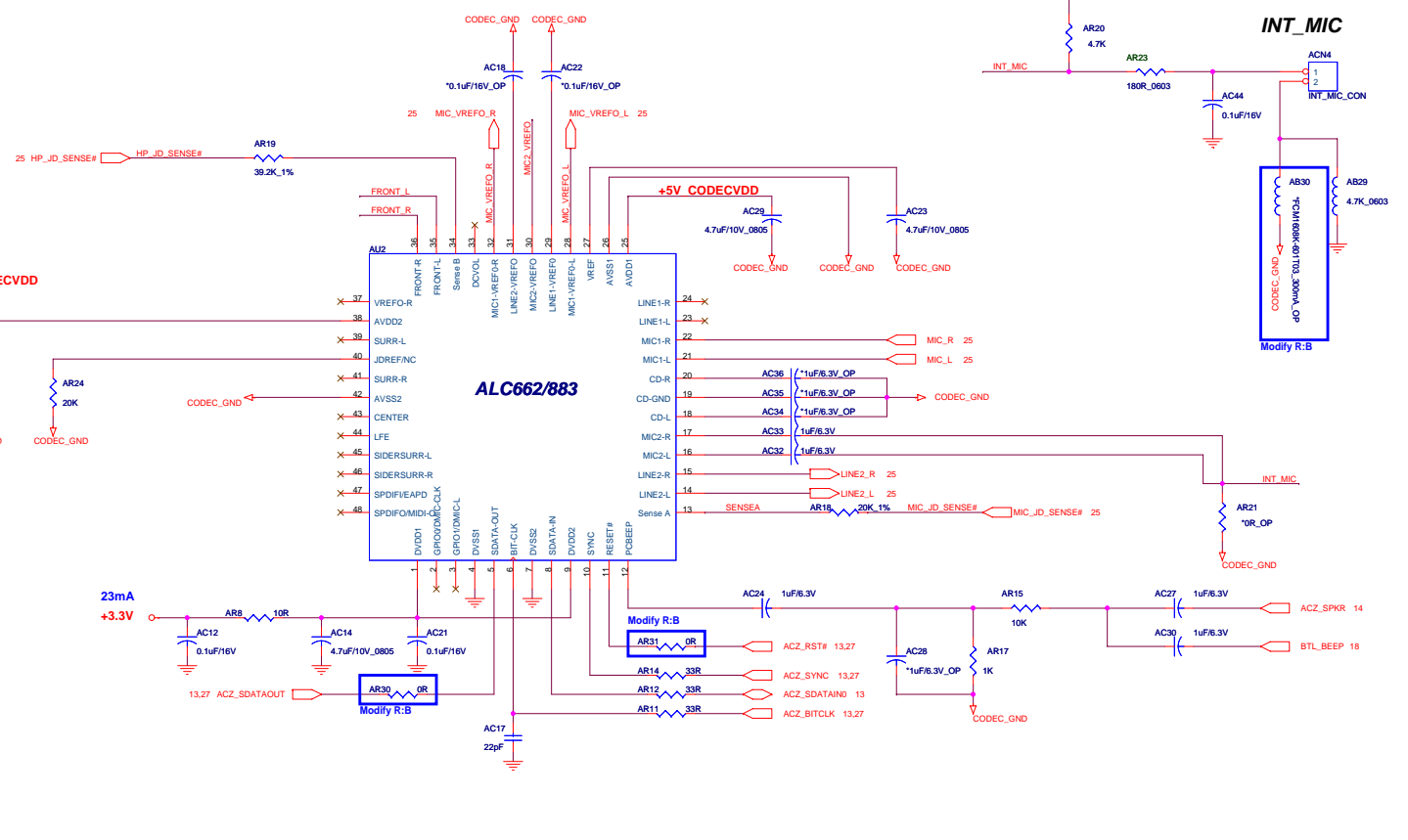
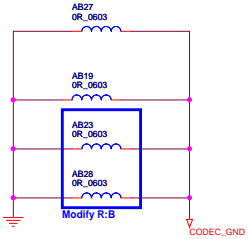
	Q76	Q77
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A



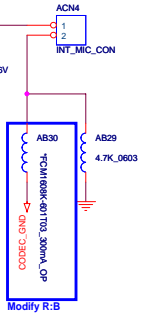
AMP VDD



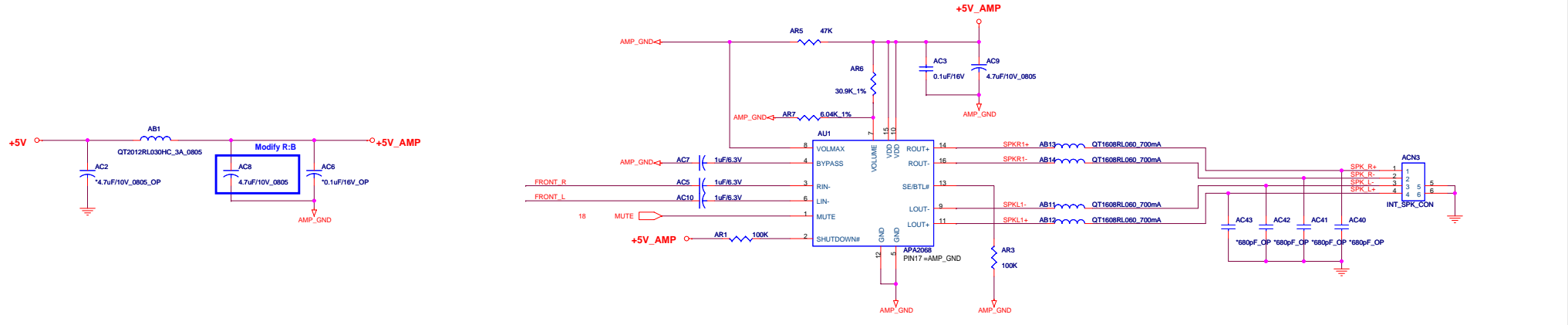
LOCATE UNDER CODEC.
USE 80 MILLS WIDE TRACE
BRIDGING AGND AND DGND PLANES



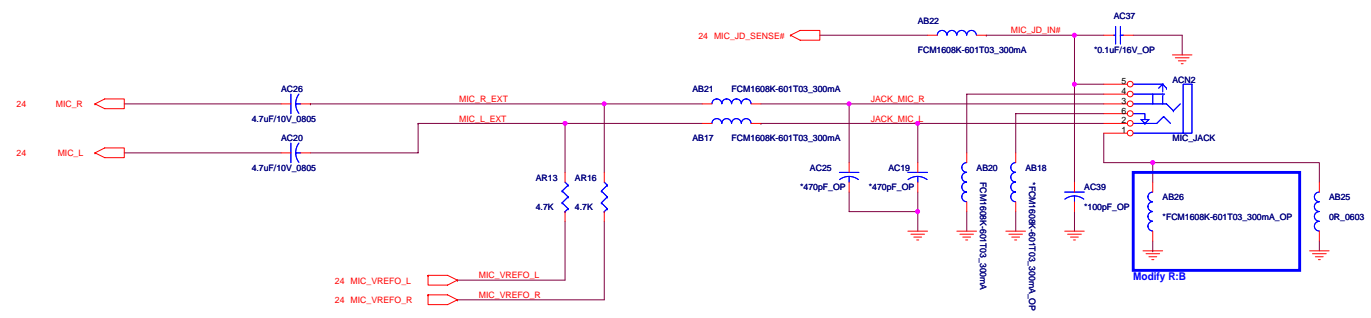
INT_MIC



INT_SPK AMP



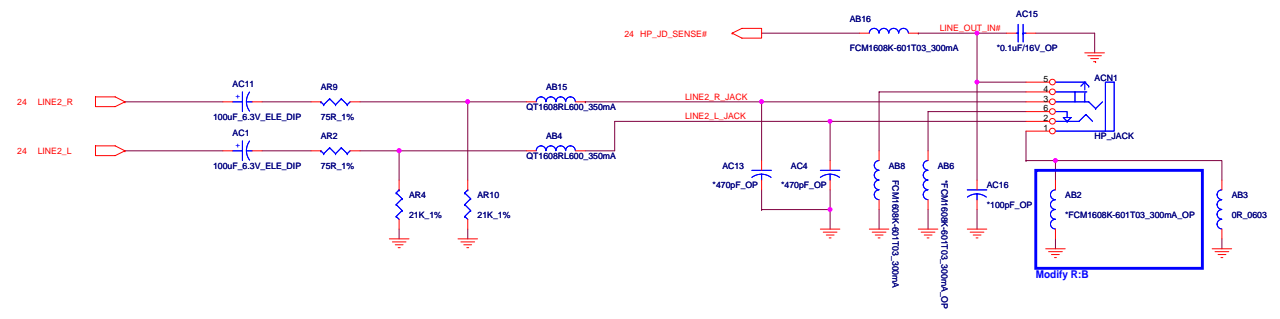
MIC/Line In JACK



Modify R:C

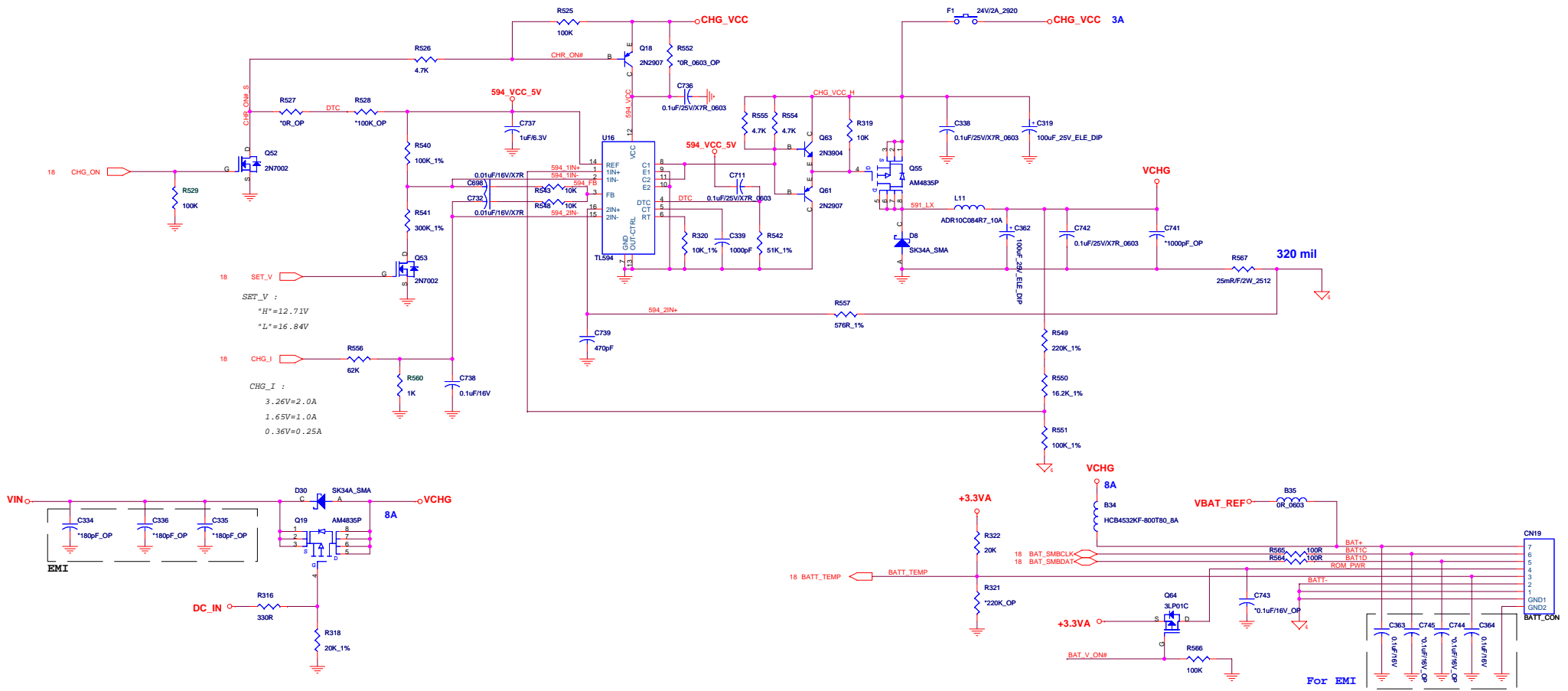


HeadPhone JACK



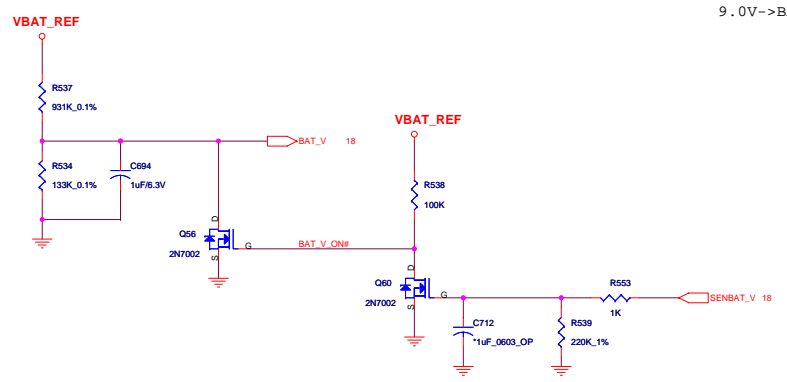
Modify R:C



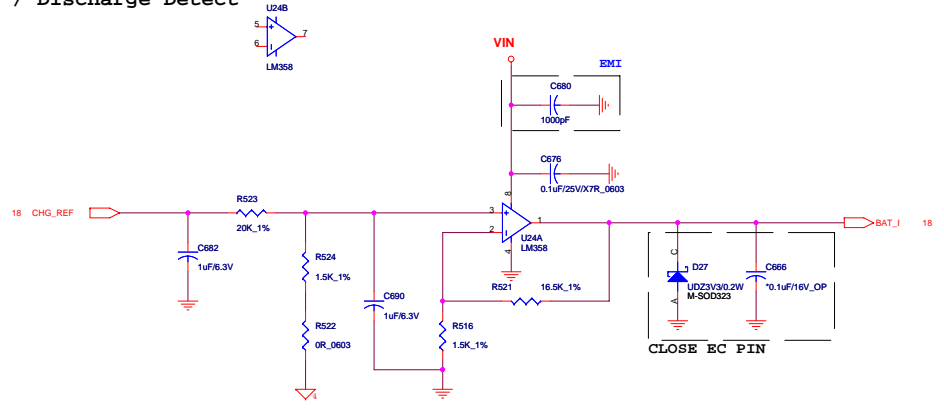


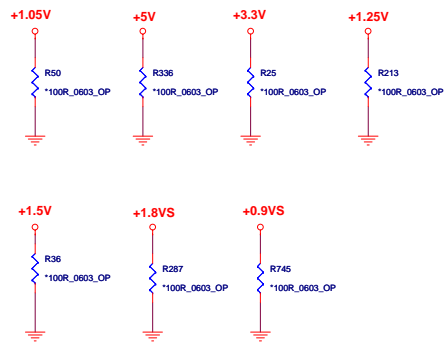
Battery Voltage Detect

- 17.6V->BAT_V=2.2V
- 16.8V->BAT_V=2.1V
- 13.2V->BAT_V=1.65V
- 12.6V->BAT_V=1.575V
- 9.0V->BAT_V=1.125V

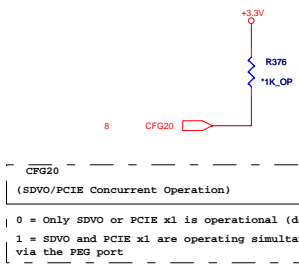
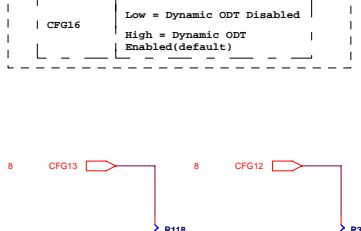
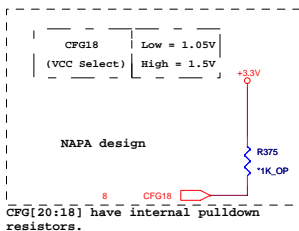
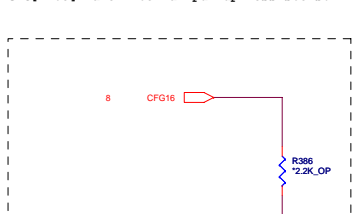
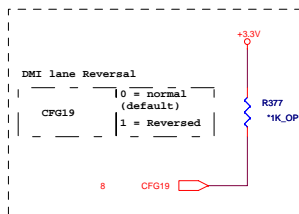
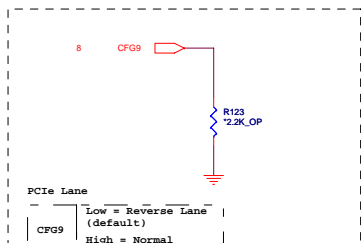
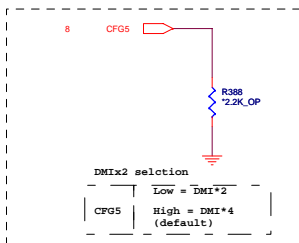
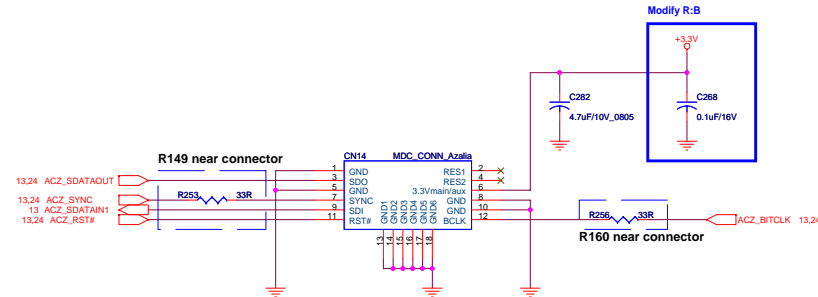


Charge / Discharge Detect



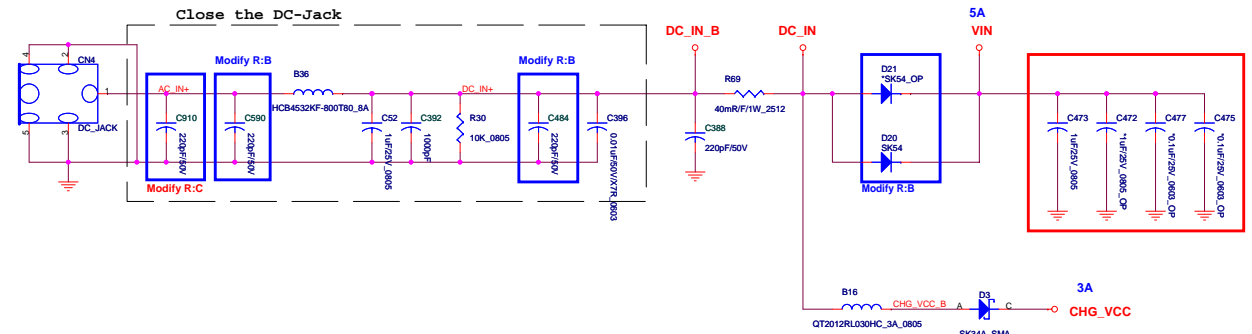


MDC

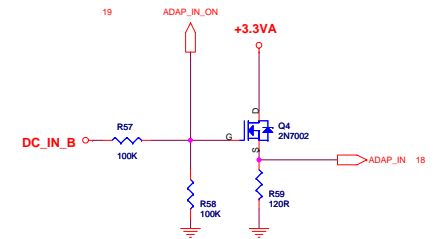
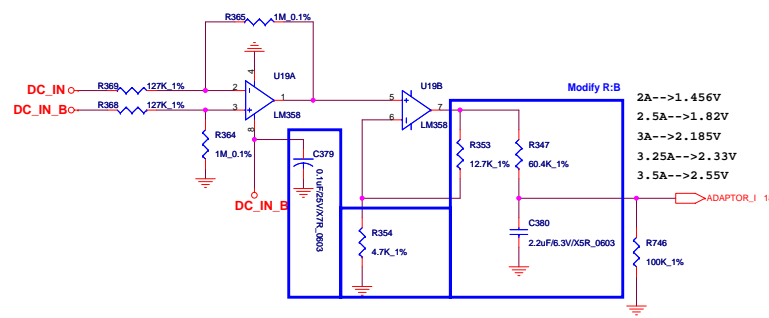


XOR / ALLZ / Clock Un-gating		
CFG12	CFG13	Configuration
0	0	Clock Gating Disabled
0	1	XOR Mode Enabled
1	0	All-Z Mode Enabled
1	1	Normal Operation (Default)

DC IN

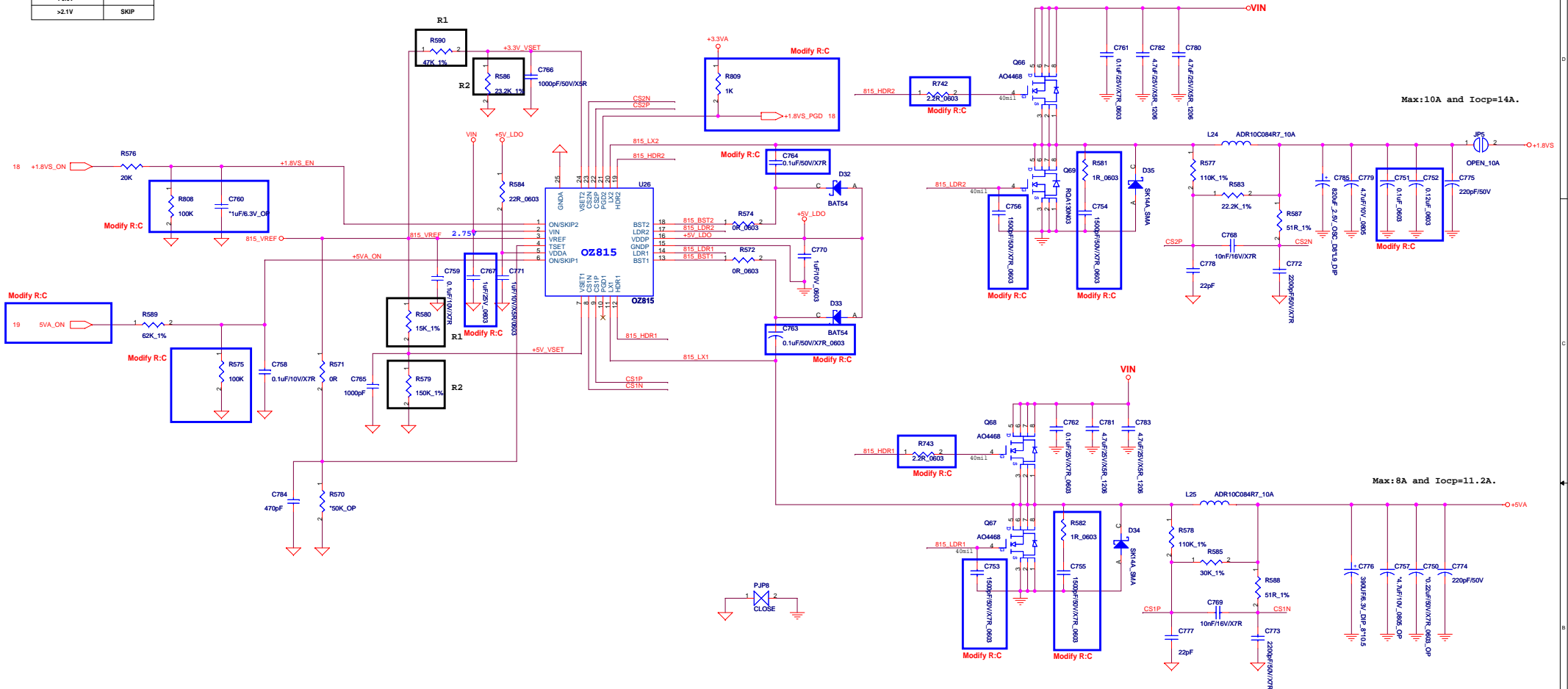


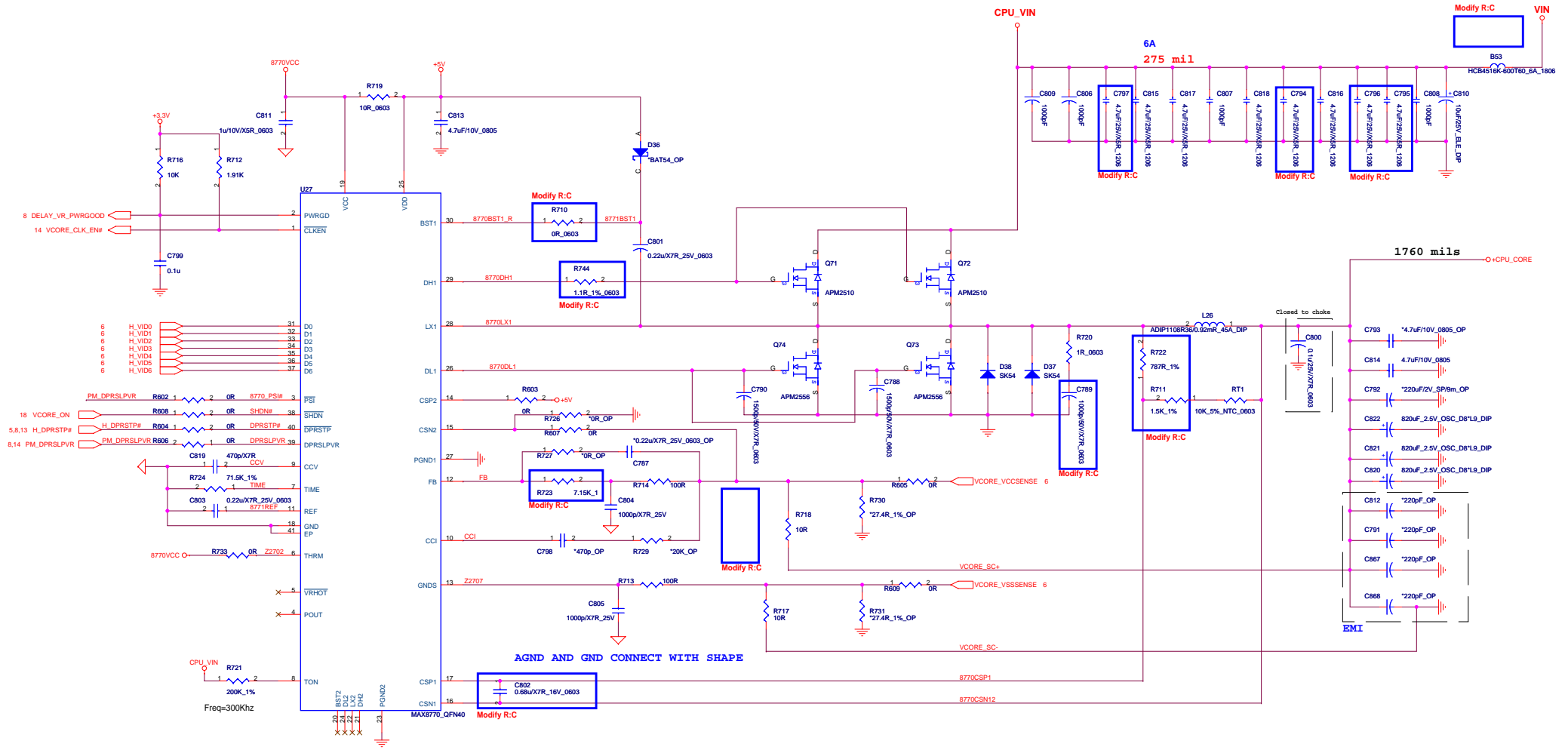
TOTAL POWER



+3V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

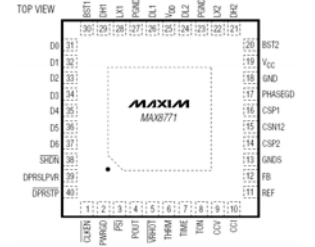
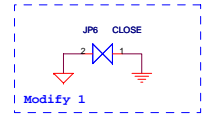
$$\text{Output Voltage} = [V_{ref} \times R2 / (R1 + R2)] \times 2$$

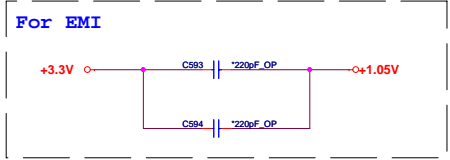
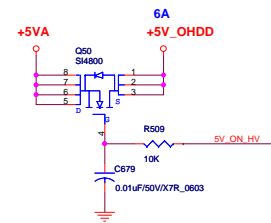
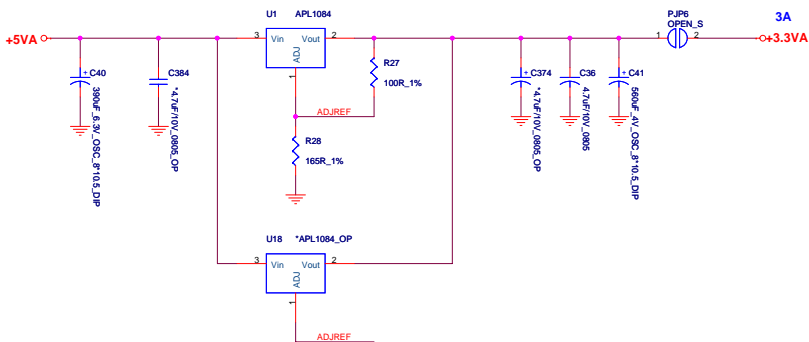
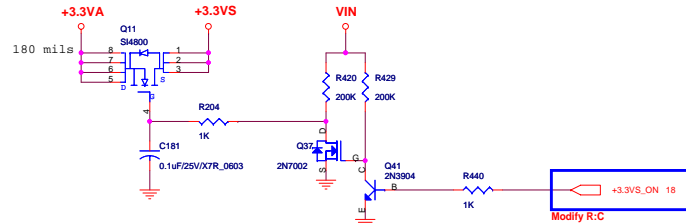
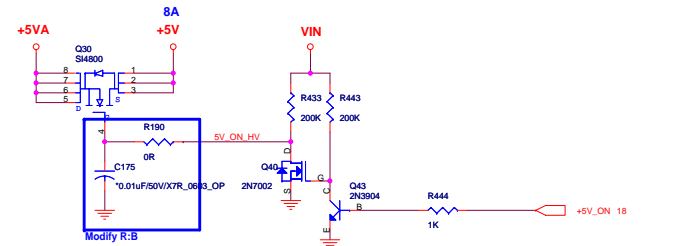
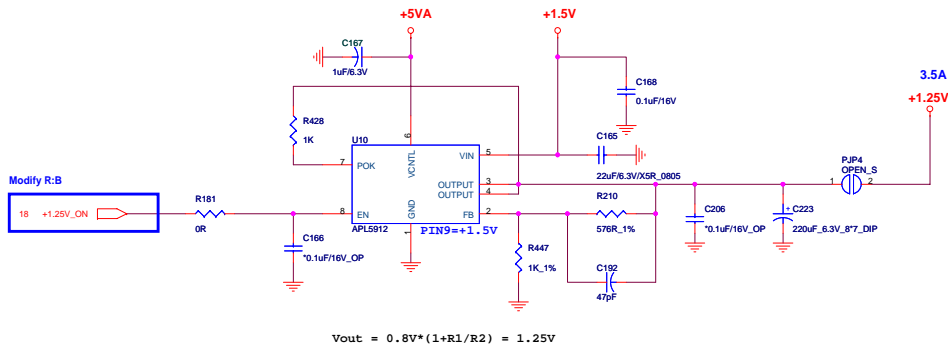
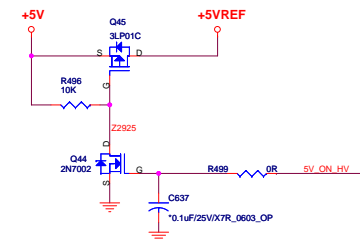
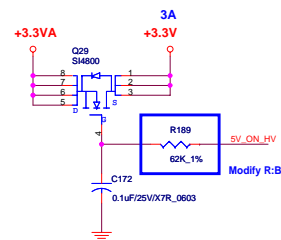
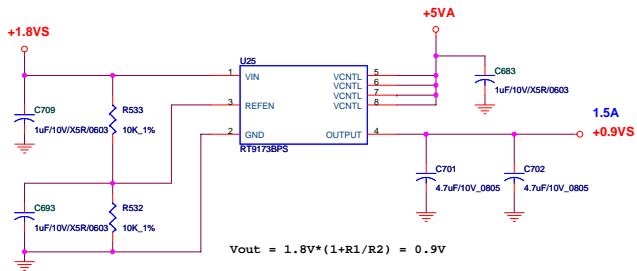




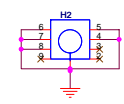
VID TABLE

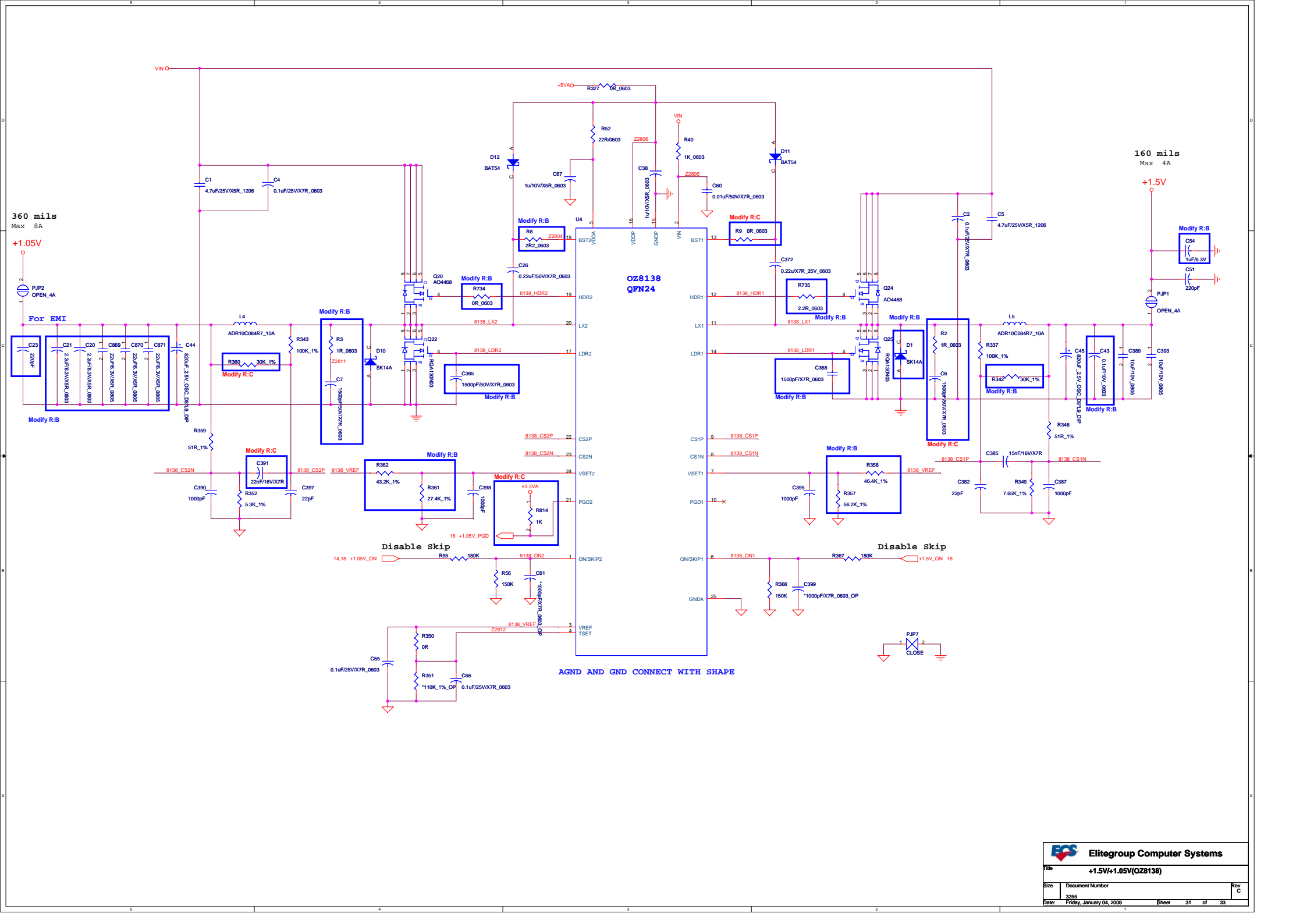
6	5	4	3	2	1	0	Vcore	Status
0	0	0	0	0	0	0	1.2875	(HFM)
0	0	0	1	0	0	0	1.2000	Boot Vout
0	0	1	1	0	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down

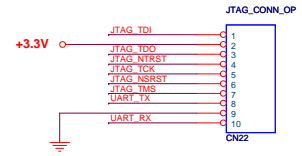
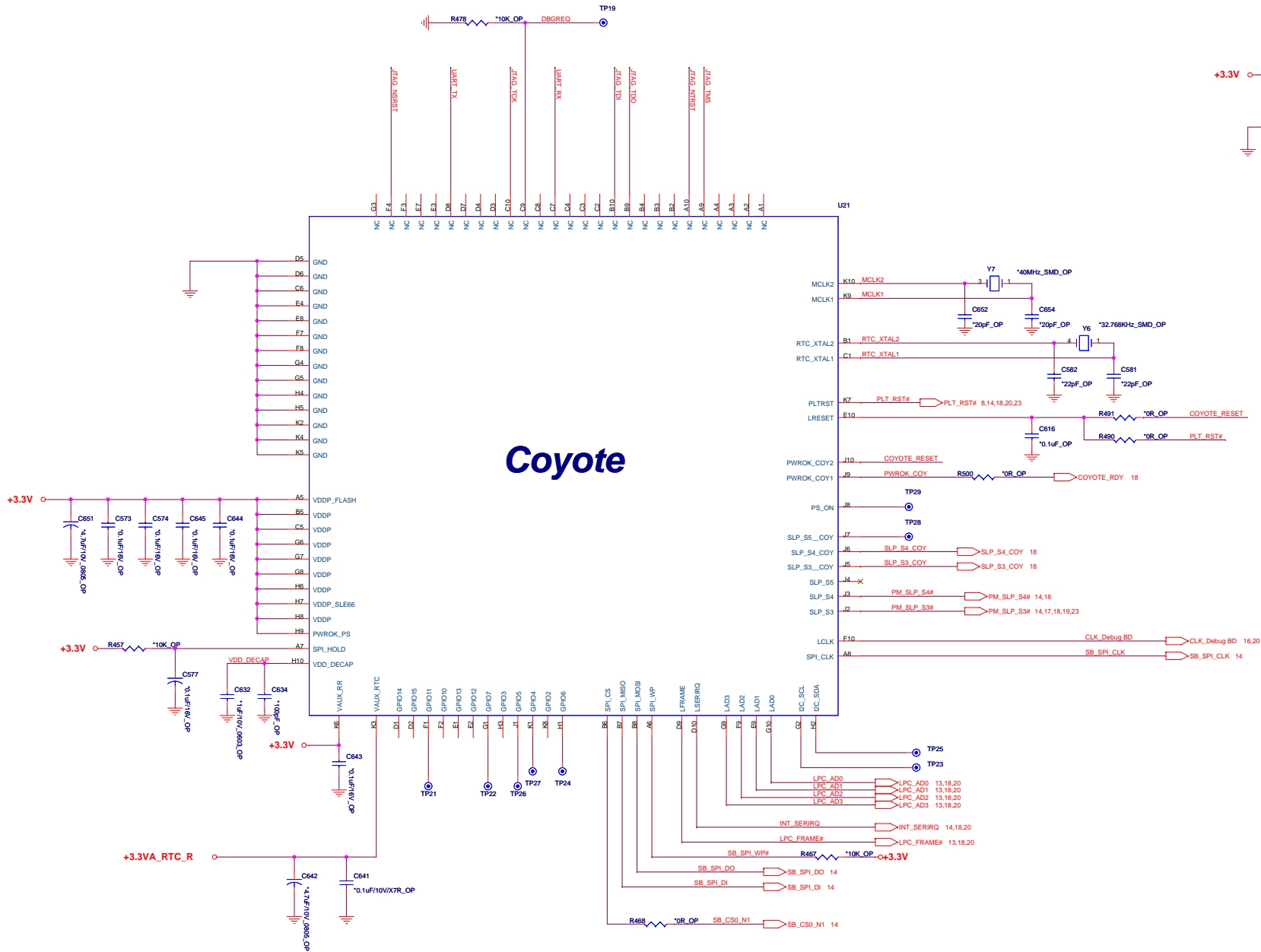




- HOLE1237(24x48)153(38)118(18)18(18)18
- HOLE1291(31)50(195)3(29)3(51)118
- HOLE19(31)53(28)8(36)3(51)118
- HOLE10(18)21(21)1(4)
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- HOLE100(31)53(28)8(36)3(51)118








RA to RB change list:

Page 5,M1->Add C856 1uF/6.3V for +1.05V
Page 5,M2->Modify H_THERM# and PM_THERMTRIP# circuit
Page 6,M3->Add C528/C569/C558/C527/C441/C442/C449/C448 (1uF/6.3V) for +CPU_CORE
Page 6,M4->Add C410/C416/C422/C431/C429/C412/C423/C432 (2.2uF/6.3V/X5R_0603) FOR +CPU_CORE
Page 6,M5->Add C491/C478/C518/C467/C143/C142/C141/C140/C858/C859/C860/C861/C862/C863/C864/C865 (2.2uF/6.3V/X5R_0603) FOR +1.05V
Page 7,M6->Add C855/C854 (0.1uF/16V)
Page 8,M7->Add R600 (30k ohm) for GFX enable pin pull high to +3.3V
Page 10,M8->Add C857 (22uF/6.3V/X5R_0805) for +1.05V
Page 13,M11->C182 change to 6.8pF
Page 13,M12->C180 change to 8.2pF
Page 13,M13->Add C470 (10pF) for EMI
Page 13,M14->C124/C94 change to 22pF
Page 17,M15->R344 change to 0 ohm
Page 17,M16->C371 change to 1500pF/50V/X7R_0603
Page 17,M17->Add R736 2.2R_0603
Page 17,M18->Original R355 pull high to +3.3VS change to pull high to +3.3V
Page 17,M19->Add R371/R370 0 ohm
Page 18,M20->EC_EXTSMI Swarp to U13/Pin 23
Page 18,M21->Add +1.25V_ON (EC Pin117)
Page 19,M22->Delete R397/Q31/Q35
Page 20,M23->Add C710 (4.7uF/10V_0805) for V_CDROM
Page 20,M24->Remove L3/L7 and Add RP20/RP21
Page 21,M25->B6/B7/B8 change to FCM1608CF-600T06 TAI-TECH
Page 21,M26->Remove C34/C33/C32
Page 22,M27->CN23 change (53398-0610L)
Page 23,M28->C48/C49 change to 22pF
Page 23,M29->Delete R131 and Add R132
Page 23,M30->R76/R77 change net link to CTRL18
Page 23,M31->Add R335 and Remove R78
Page 24,M32->Add AB710/AB9/AB23/AB28
Page 24,M33->Add AC38/AC8/AR30/AR31/AB30
Page 25,M34->Remove AB26/AB2
Page 27,M35->Add R745/C590/C484
Page 27,M36->Delete R183/R207/R206/Q9/Q10/R407/Q36
Page 27,M37->R347 change to 60.4K ohm
Page 27,M38->Delete C386 and add R746 100k ohm
Page 28,M39->+5VA and +1.8VS PWM solution change to OZ815
Page 29,M40->CPU_CORE PWM solution change to MAX8770
Page 30,M41->R181 link to +1.25V_ON
Page 31,M42->R189 change to 60.4K ohm
Page 31,M43->R190 change to 0 ohm and C175 OP
Page 32,M44->R360 change to 36K ohm
Page 32,M45->R8/R9 change to 2R2 ohm
Page 32,M46->C365/C368 change to 1500pF
Page 32,M47->R342 change to 30K ohm 1\$
Page 32,M48->R362 change to 43.2K ohm
Page 32,M49->R361 change to 27.4K ohm
Page 32,M50->R357 change to 56.2K ohm
Page 32,M51->R358 change to 46.4K ohm
Page 32,M52->Add C21/C20/C869/C870/C871/R734/R735
Page 32,M53->C43 change to 0.1uF/ Add C54 1uF

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