

ROME-4.5 PLANAR SIT

	DATE	EC NO.	PART NO.
REL	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			1 /88

VER 0.94
MAR/09/2005

- | | |
|--------------------------------------|---|
| 1. TITLE PAGE | 45. CDC CONNECTOR |
| 2. EC HISTORY | 46. CARDBUS CONTROLLER(1/2) |
| 3. CPU(1/3) | 47. CARDBUS CONTROLLER(2/2) |
| 4. CPU(2/3) | 48. CARDBUS/EXC SLOT |
| 5. CPU(3/3) | 49. CARDBUS/EXC PWR CTRL |
| 6. ITP CON/LARGE PTH HOLE/EMI FINGER | 50. < BLANK PAGE > |
| 7. VCCCPUCORE DECOUPLING | 51. GBE BCM5751M(1/2) |
| 8. ALVISO(1/7) : HOST I/F | 52. GBE BCM5751M(2/2) |
| 9. ALVISO(2/7) : DDR2-A | 53. GBE MAGNETICS |
| 10. ALVISO(3/7) : DDR2-B | 54. RJ11/RJ45 CONNECTOR |
| 11. ALVISO(4/7) : PEG/DMI | 55. MINI PCI SLOT |
| 12. ALVISO(5/7) : GRAPHICS | 56. PCI BUS SWITCH |
| 13. ALVISO(6/7) : VCC/GND | 57. DOCKING CONNECTOR |
| 14. ALVISO(7/7) : VCC/GND(NTCF) | 58. H8S/2161B |
| 15. DDR2 SODIMM-A | 59. KEYBOARD CONNECTOR |
| 16. DDR2 SODIMM-B | 60. TOUCH PAD CONNECTOR |
| 17. DDR2 TERMINATION | 61. MISC G/A (PMH6) |
| 18. DDR2 DECOUPLING | 62. IO KEEPER(SUPER I/O, TPM, RFTD) |
| 19. CLOCK GEN(CK410M) | 63. PARALLEL INTERFACE |
| 20. ATI M24(1/6) : PEG I/F | 64. SERIAL INTERFACE |
| 21. ATI M24(2/6) : LVDS/CRT/TV/TMDS | 65. IR MODULE |
| 22. ATI M24(3/6) : CLK/GPIO | 66. THERMAL SENSOR |
| 23. ATI M24(4/6) : ANALOG POWER | 67. I2CBUS/SMBUS |
| 24. ATI M24(5/6) : VCC | 68. FAN CONTROL |
| 25. ATI M24(6/6) : GND | 69. G-SENSOR |
| 26. LCD CONNECTOR | 70. EMC DECOUPLING |
| 27. EXT CRT INTERFACE | 71. RGB SWITCH |
| 28. TV_OUT | 72. DC-IN AND CHARGER (ADP3806) |
| 29. ICH6-M(1/4) : DMI/PCI/LPC/AC97 | 73. CHARGE SELECTOR |
| 30. ICH6-M(2/4) : ATA/USB/PM | 74. BATTERY INPUT |
| 31. ICH6-M(3/4) : PCI EXPRESS | 75. BATTERY MONITOR |
| 32. ICH6-M(4/4) : VCC/GND | 76. POWER SEQUENCE |
| 33. FWH,RTC BATTERY | 77. DC-DC VCC3M/VCC5M (MAX1901ETJ) |
| 34. SATA BRIDGE/HDD CONN | 78. DC-DC VCCCPUCORE (ADP3205) |
| 35. BAY I/F CONN | 79. DC-DC VCORE INPUT CAP |
| 36. USB POWER/CONN | 80. DC-DC VCC1R8M (MAX1993ETG) |
| 37. AUDIO AD1981B | 81. DC-DC VCC1R5M/VCC1R05B (MAX1540ETJ) |
| 38. AUDIO MISC | 82. DC-DC VCCVIDEOCORE (MAX1993ETG) |
| 39. AUDIO INT MIC | 83. DC-DC VCC2R5M/VCC0R9B |
| 40. AUDIO HP & EXT MIC CONN | 84. TSURUMAI-2 |
| 41. AUDIO EXT MIC AMP | 85. LOAD SW 1 (VIDEO) |
| 42. AUDIO SPEAKER | 86. LOAD SW 2 (AUX) |
| 43. AUDIO HDP AMP AN12943A(1/2) | 87. LOAD SW 3 (B,UBAY) |
| 44. AUDIO HDP AMP AN12943A(2/2) | 88. MAX POWER CTRL |

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DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	TITLE PAGE		
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EC HISTORY

	DATE	EC NO.	PART NO.
REL	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			2 /88

SDV

VER.0.33 01/07/2004 RM4_SDV_EC_127
 VER.0.34 01/16/2004 RM4_SDV_EC_128/129/130/131
 VER.0.35 01/20/2004 RM4_SDV_EC_133/135
 VER.0.36 01/23/2004 RM4_SDV_EC_137
 VER.0.37 01/27/2004 RM4_SDV_EC_138 TO 141
 VER.0.38 02/03/2004 RM4_SDV_EC_142--148
 VER.0.39 02/04/2004 RM4_SDV_EC_149/150/151/152
 VER.0.40 02/06/2004 RM4_SDV_EC_153/154/155/156/157
 VER.0.41 02/12/2004 RM4_SDV_EC_158/159/160/161/162
 VER.0.42 02/16/2004 RM4_SDV_EC_163

SDV GERBER RELEASED 02/17/2004

VER.0.43 02/18/2004 RM4_SDV_EC_164/165/166

SIV

VER.0.44 03/26/2004 RM4_SIV_EC_001/002
 VER.0.45 04/01/2004 RM4_SIV_EC_003 TO 008 AND 012
 VER.0.46 04/05/2004 RM4_SIV_EC_09/10/14/19/20/21/22/23/24
 VER.0.47 04/07/2004 CORRECT R872 TO NO-ASMRM AND J31 CRT CONN WIRING.
 VER.0.48 04/08/2004 RM4_SIV_EC_027/28/30/31/34/35
 VER.0.49 04/11/2004 RM4_SIV_EC_35 CORRECTION (R41->ASM) AND
 AND ADD EZJ1V270GA X7 (ESD REASON).

SIV GERBER RELEASED 04/13/2004

VER.0.50 04/16/2004 RM4_SIV_EC_32/33/36/37/38
 AND CORRECT C1000 TO SYMBOL WITH POLARITY.

VER.0.51 04/20/2004 CORRECT R417 TO 0 , R522 TO 2M.
 VER.0.52 04/21/2004 RM4_SIV_EC_39/40/41
 VER.0.53 04/22/2004 RM4_SIV_EC_42/43
 VER.0.54 04/23/2004 RM4_SIV_EC_44

PRE-SIT

VER.0.55 05/18/2004 RM4_SIT_EC_01/02/03/04
 VER.0.56 05/21/2004 RM4_SIT_EC_05/07/09/13/14/15
 VER.0.57 05/25/2004 RM4_SIT_EC_16/17/18
 VER.0.58 05/26/2004 RM4_SIT_EC_ LINKUP/ACTIVITY CHNAGE
 VER.0.59 06/01/2004 RM4_SIT_EC_19
 VER.0.60 06/02/2004 RM4_SIT_EC_20/21/23/24/25
 VER.0.61 06/03/2004 RM4_SIT_EC_26
 VER.0.62 06/04/2004 RM4_SIT_EC_27/28/29
 VER.0.63 06/07/2004 RM4_SIT_EC_23/27 CORRECTION/30
 VER.0.64 06/11/2004 RM4_SIT_EC_32

PRE-SIT GERBER RELEASED ON 06/16/2004

VER.0.65 06/21/2004 RM4_SIT_EC_34
 VER.0.66 06/30/2004 RM4_SIT_EC_35 (R919 -> NO-ASM, R920->ASM)
 VER.0.67 07/07/2004 RM4_SIT_EC_36 CHNAGED 12 PARTS
 VER.0.68 07/20/2004 RM4_SIT_EC_37/38/39/40

SIT

VER.0.69 07/28/2004 RM4_SITA_EC_02/03/06
 VER.0.70 07/29/2004 RM4_SITA_EC_07/08
 VER.0.71 08/03/2004 RM4_SITA_EC_09/10/11
 VER.0.72 08/06/2004 RM4_SITA_EC_12/13/14/15
 VER.0.73 08/16/2004 RM4_SITA_EC_16/17/18
 VER.0.74 08/17/2004 RM4_SITA_EC_19/20/21/22
 VER.0.75 08/18/2004 RM4_SITA_EC_23
 VER.0.76 08/20/2004 RM4_SITA_EC_26
 VER.0.77 08/23/2004 RM4_SITA_EC_27

SIT GERBER RELEASED 08/24/2004.

VER.0.78 08/30/2004 P51 TABLE CORRECTION
 VER.0.79 09/01/2004 RM4_SITA_EC_28
 VER.0.80 09/10/2004 RM4_SITA_EC_29/30

SIT-R

VER.0.81 10/05/2004 RM4_SITR_EC_01/02
 VER.0.82 10/08/2004 RM4_SITR_EC_03/04
 VER.0.83 10/19/2004 RM4_SITR_EC_05/06
 VER.0.84 10/22/2004 RM4_SITR_EC_07/08/10/11
 VER.0.85 10/25/2004 RM4_SITR_EC_12

SIT-R GERBER WAS RELEASED 10/28/2004.

VER.0.86 10/29/2004 RM4_SITR_EC_13
 VER.0.87 11/04/2004 RM4_SITR_EC_15
 VER.0.88 11/08/2004 RM4_SITR_EC_16/17

SVT

VER.0.89 11/09/2004 RM4_SVT_EC_01/02/03
 SVT GERBER WAS RELEASED 11/12/2004.

VER.0.90 11/15/2004 RM4_SVT_EC_04/05
 VER.0.90 11/17/2004 ASSIGNED DWG PN=39T0120.

SVT-R

VER.0.91 11/26/2004 RM4_SVTR_EC_01/02.
 SVT-R GERBER WAS RELEASED 11/30/2004.
 VER.0.91 12/07/2004 ASSIGNED DWG PN=39T0167.

R4.5 SIT

VER.0.92 02/01/2005 RM45_SIT_EC_02
 VER.0.93 02/15/2005 RM45_SIT_EC_01/03
 VER.0.94 02/24/2005 RM45_SIT_EC_04

R4.5 GERBER WAS RELEASED 03/02/2005.

VER.0.94 03/09/2005 CHANGE COMMENTS

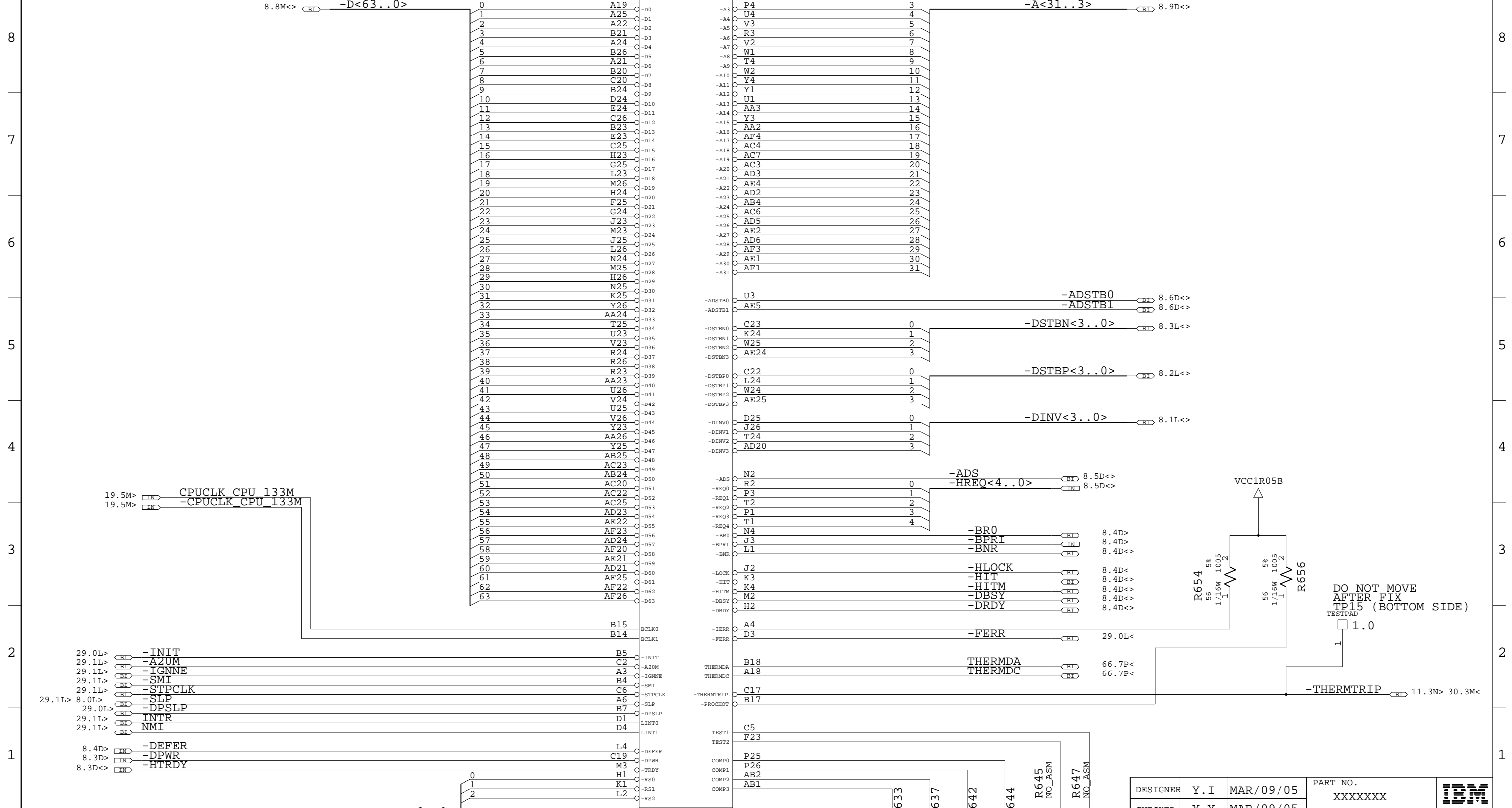
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APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
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REL	DATE MAR/09/05	EC NO. VER.094	PART NO. XXXXXXXX
			DEVELOPMENT NO. 3 / 88

U58

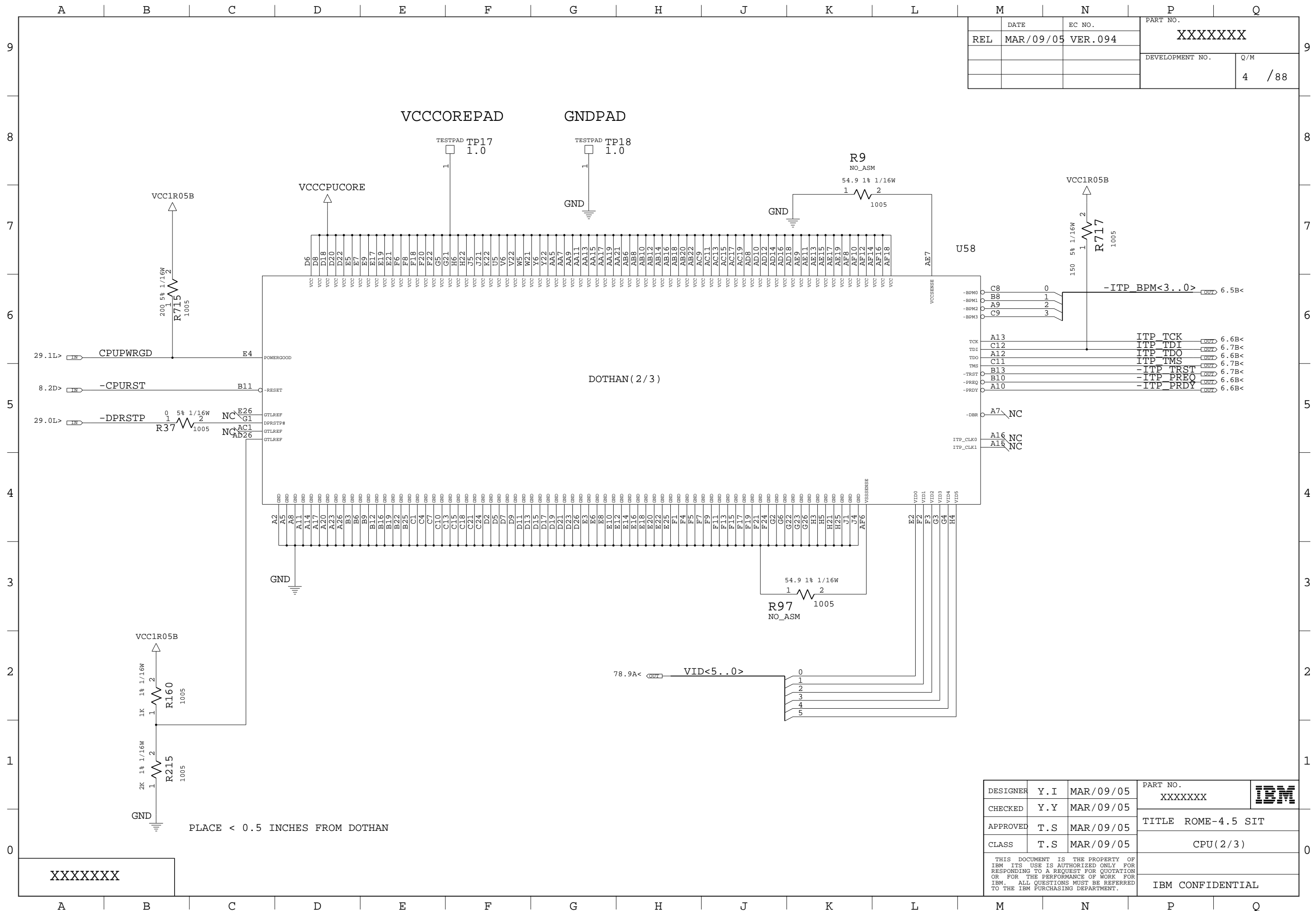
DOTHAN(1/3)



COMP0/2: Z0=27.4 OHM TRACE
COMP1/3: Z0=55 OHM

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO. XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05	TITLE ROME-4.5 SIT	
APPROVED	T. S	MAR/09/05	CLASS CPU(1/3)	
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DATE	EC NO.	PART NO.	
MAR/09/05	VER.094	XXXXXXXX	
REL		DEVELOPMENT NO.	Q/M
			4 / 88

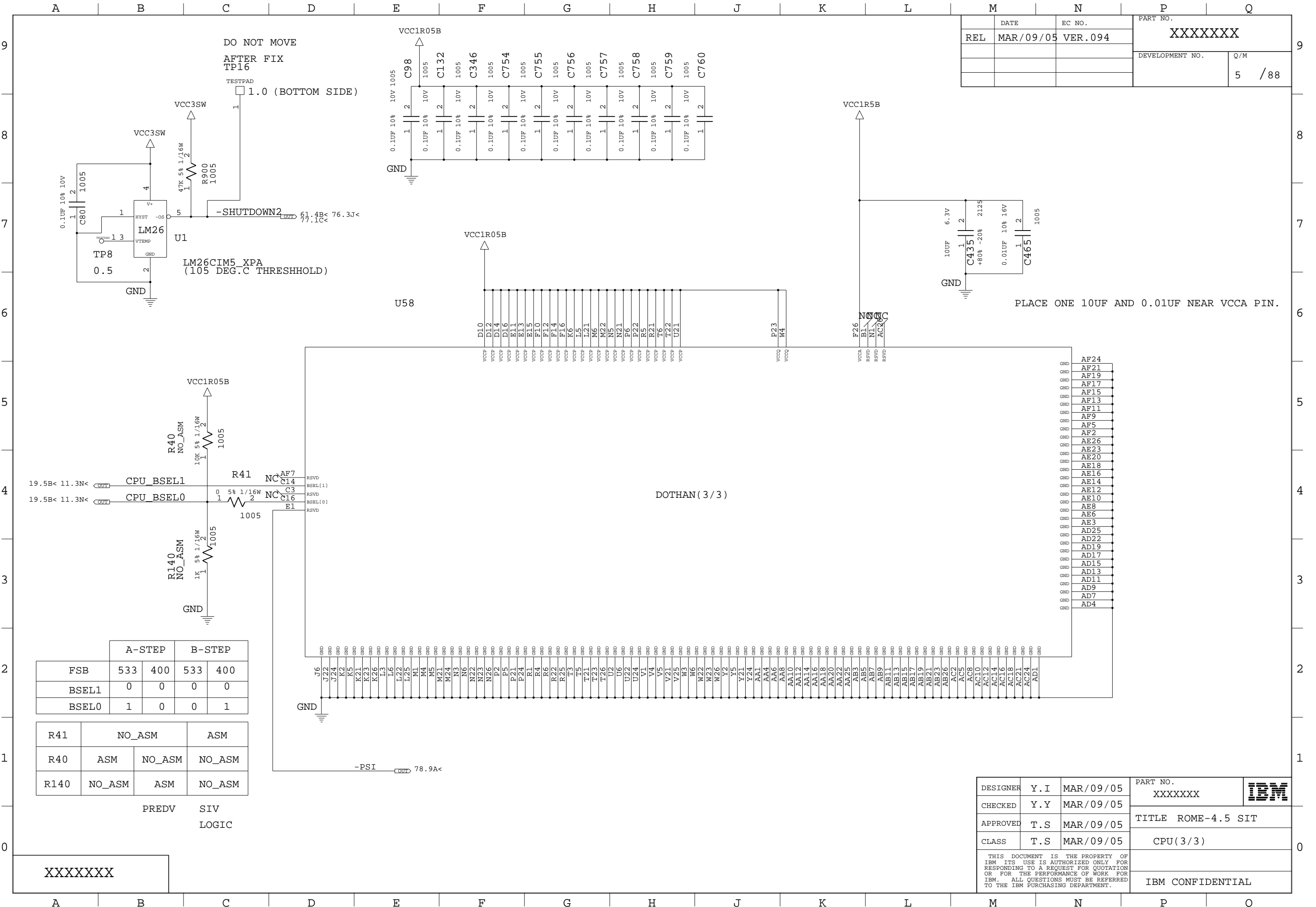
DO THAN (2 / 3)

PLACE < 0.5 INCHES FROM DO THAN

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DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	CPU(2/3)		
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DATE	EC NO.	PART NO.	
REL MAR/09/05	VER.094	XXXXXXXX	
		DEVELOPMENT NO.	Q/M
		5	/88



	A-STEP		B-STEP	
FSB	533	400	533	400
BSEL1	0	0	0	0
BSEL0	1	0	0	1

R41	NO_ASM		ASM
R40	ASM	NO_ASM	NO_ASM
R140	NO_ASM	ASM	NO_ASM

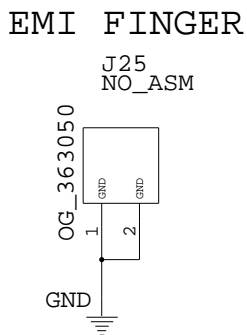
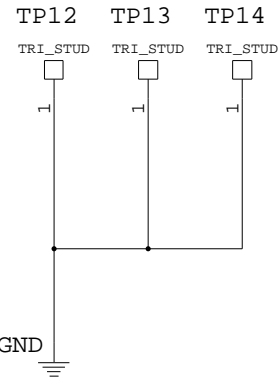
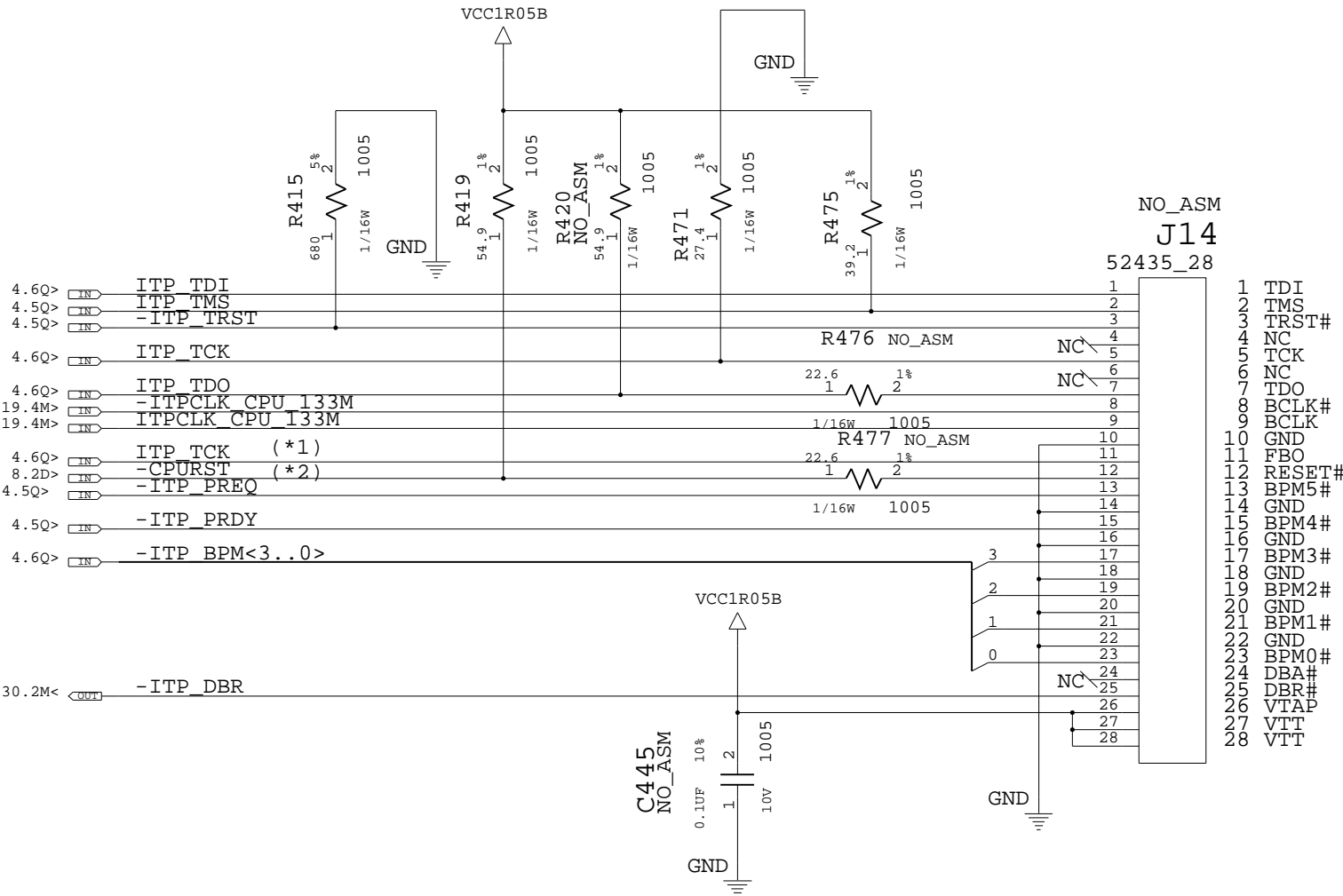
PREDV SIV
LOGIC

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	CPU(3/3)		
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	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
			6	/88

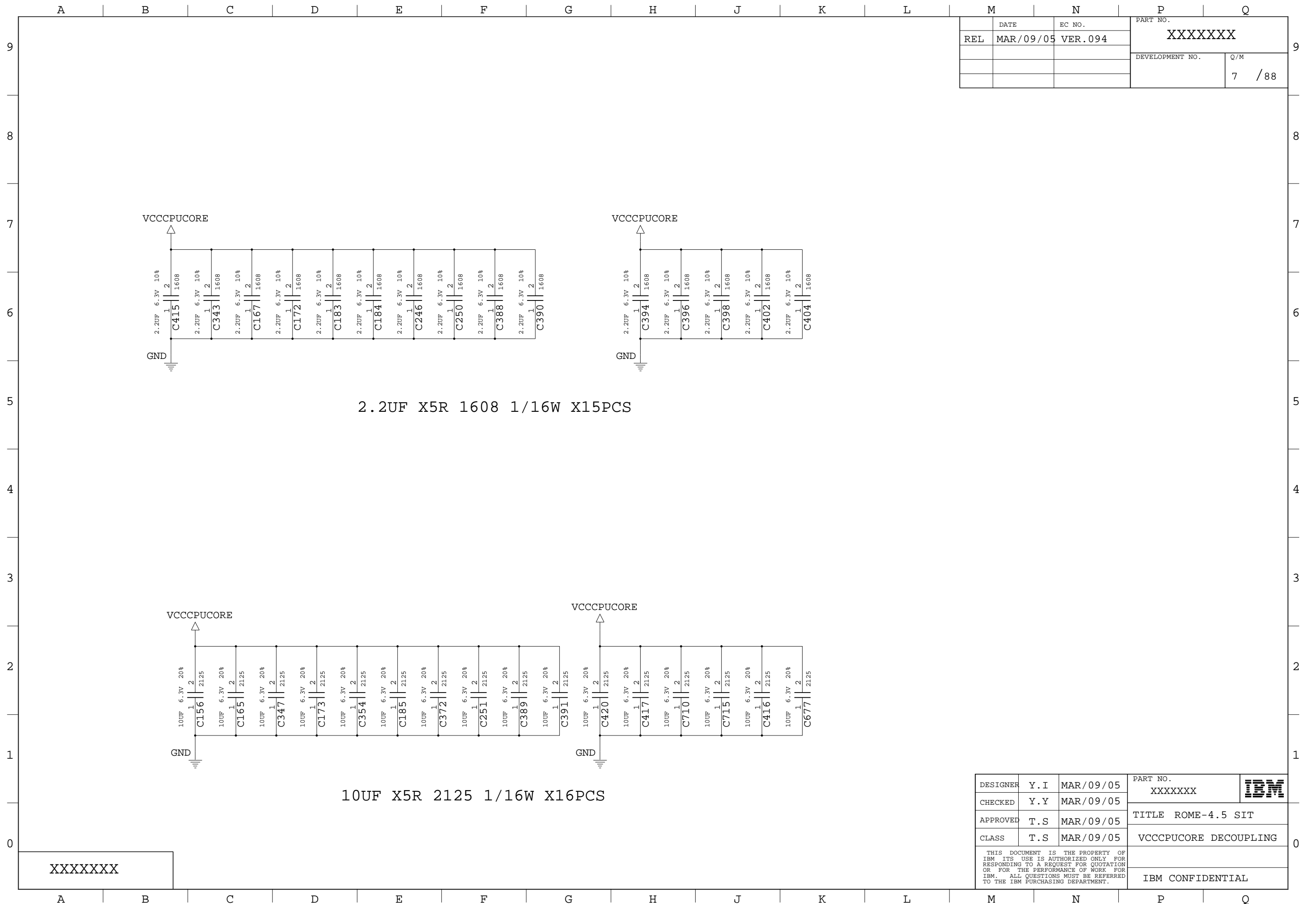
LARGE PTH HOLE



(*1) TCK SIGNAL IS BRANCHED AT DOTHAN PIN
 (*2) -CPURST SIGNAL IS BRANCHED AT ALVISO PIN

XXXXXXXX

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	ITP CONN/LARGE PTH HOLE		
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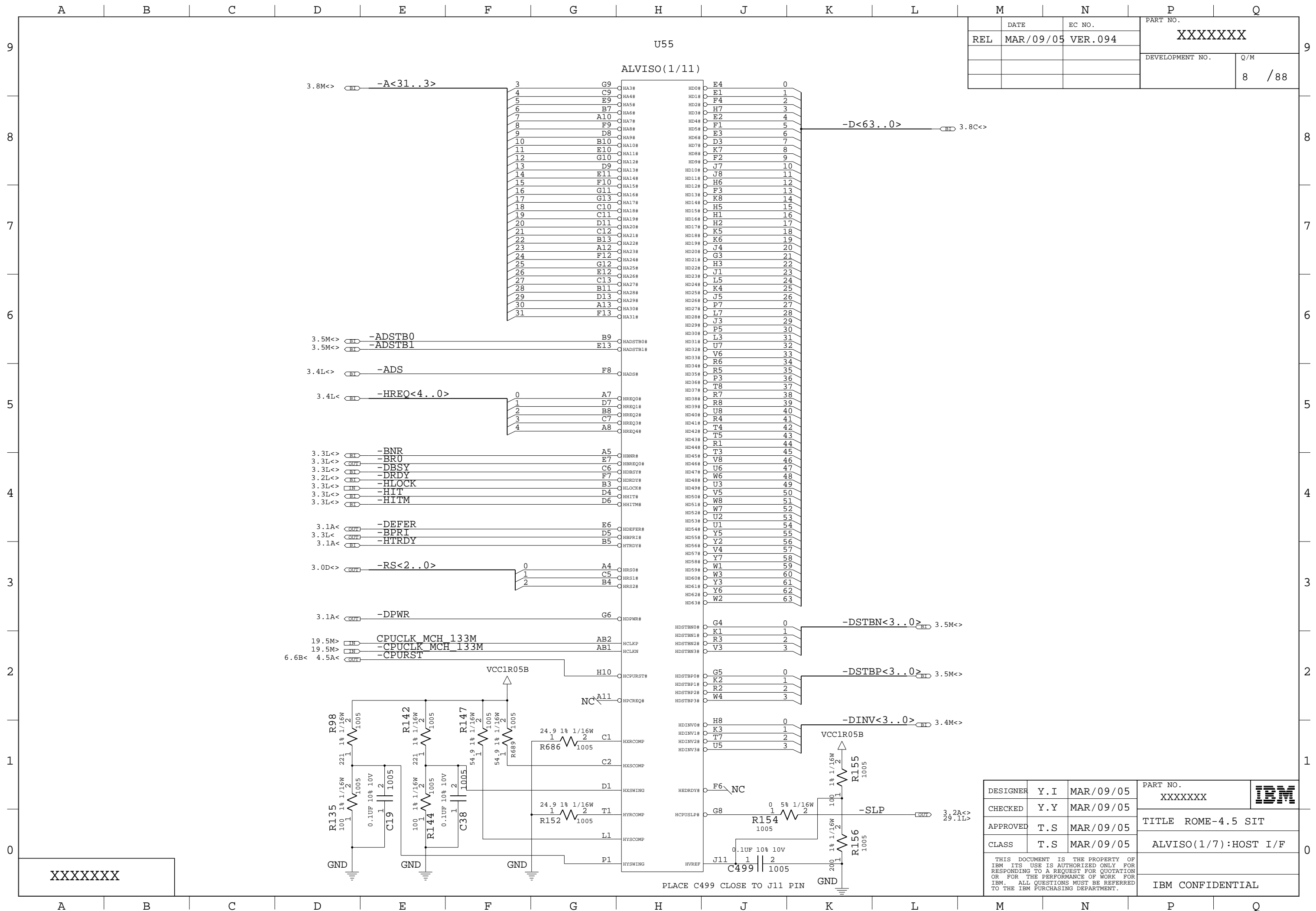
	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				7 / 88

2.2UF X5R 1608 1/16W X15PCS

10UF X5R 2125 1/16W X16PCS

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	VCCCPUCORE DECOUPLING		
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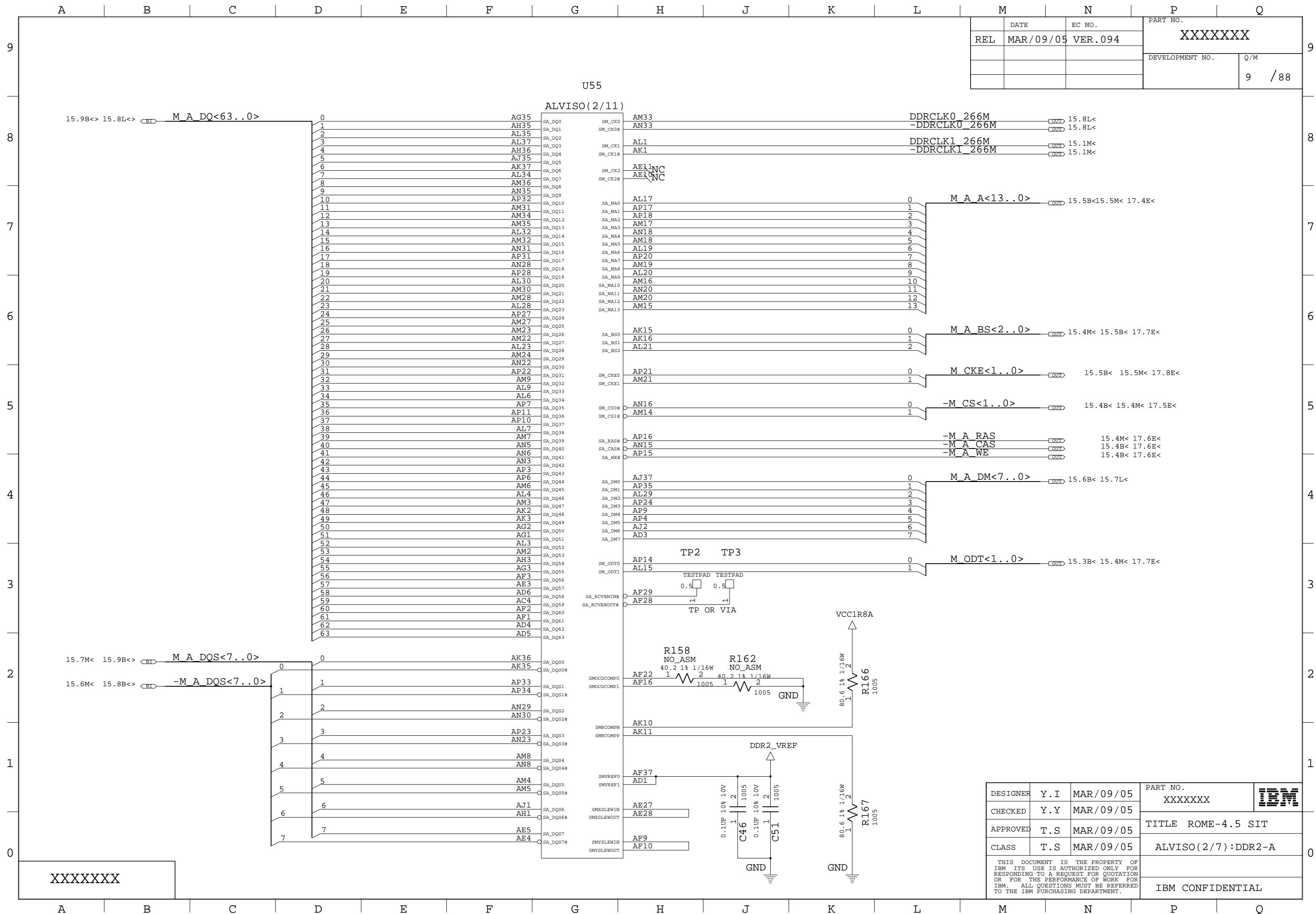
REL	DATE MAR/09/05	EC NO. VER.094	PART NO. XXXXXXXX
			DEVELOPMENT NO. 8 / 88

DESIGNER	Y. I	MAR/09/05	PART NO. XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05	TITLE ROME-4.5 SIT	
APPROVED	T. S	MAR/09/05	ALVISO(1/7):HOST I/F	
CLASS	T. S	MAR/09/05	IBM CONFIDENTIAL	

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PLACE C499 CLOSE TO J11 PIN



DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		9 / 88

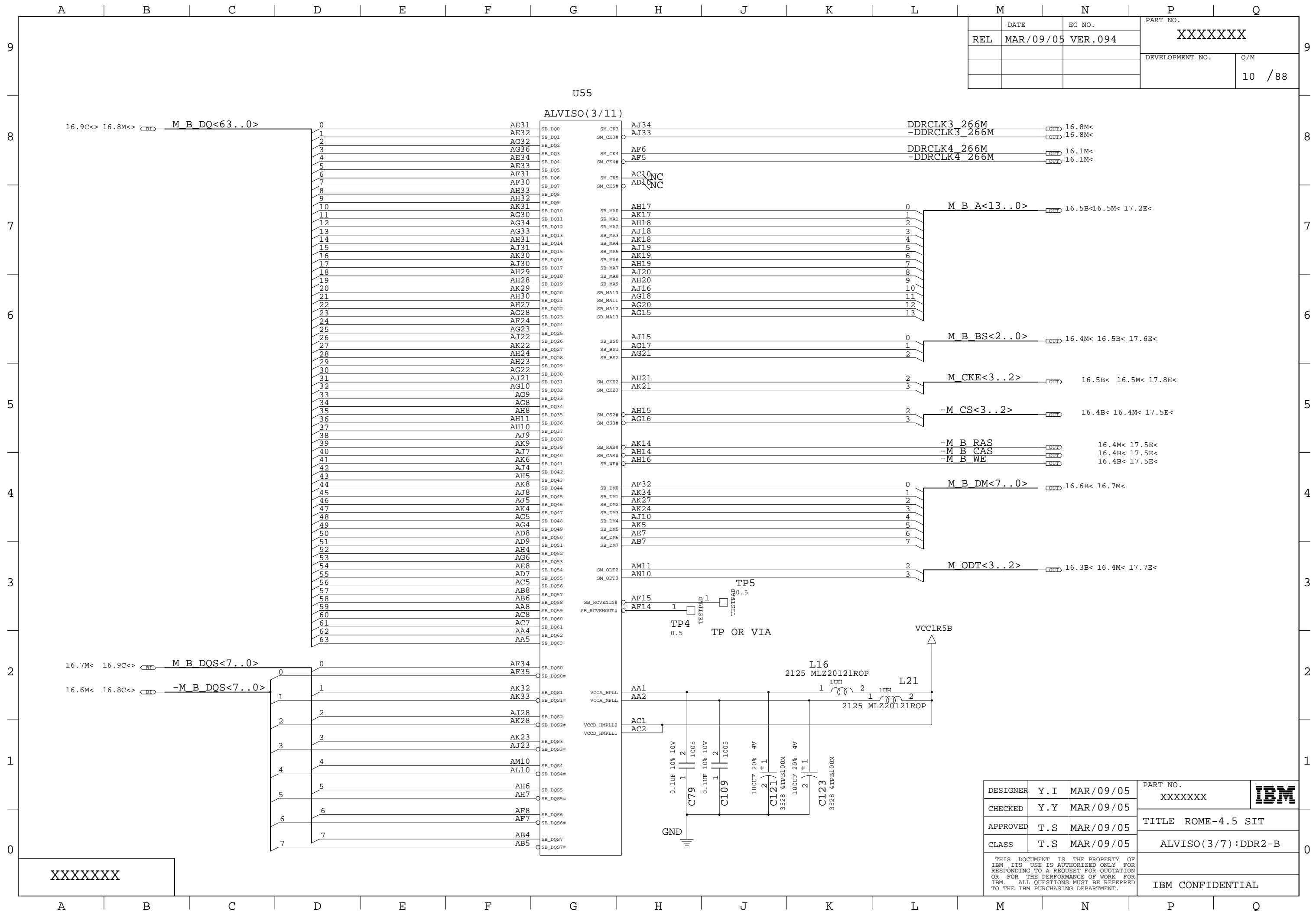
U55
ALVISO (2/11)

0	AG35	SA_DQ0
1	AH35	SA_DQ1
2	AL35	SA_DQ2
3	AL37	SA_DQ3
4	AH36	SA_DQ4
5	AJ35	SA_DQ5
6	AK37	SA_DQ6
7	AL34	SA_DQ7
8	AM36	SA_DQ8
9	AN35	SA_DQ9
10	AP32	SA_DQ10
11	AM31	SA_DQ11
12	AM34	SA_DQ12
13	AM35	SA_DQ13
14	AL32	SA_DQ14
15	AM32	SA_DQ15
16	AN31	SA_DQ16
17	AP31	SA_DQ17
18	AN28	SA_DQ18
19	AP28	SA_DQ19
20	AL30	SA_DQ20
21	AM30	SA_DQ21
22	AM28	SA_DQ22
23	AL28	SA_DQ23
24	AP27	SA_DQ24
25	AM27	SA_DQ25
26	AM23	SA_DQ26
27	AM22	SA_DQ27
28	AL23	SA_DQ28
29	AM24	SA_DQ29
30	AN22	SA_DQ30
31	AP22	SA_DQ31
32	AM9	SA_DQ32
33	AL9	SA_DQ33
34	AL6	SA_DQ34
35	AP7	SA_DQ35
36	AP11	SA_DQ36
37	AP10	SA_DQ37
38	AL7	SA_DQ38
39	AM7	SA_DQ39
40	AN5	SA_DQ40
41	AN6	SA_DQ41
42	AN3	SA_DQ42
43	AP3	SA_DQ43
44	AP6	SA_DQ44
45	AM6	SA_DQ45
46	AL4	SA_DQ46
47	AM3	SA_DQ47
48	AK2	SA_DQ48
49	AK3	SA_DQ49
50	AG2	SA_DQ50
51	AG1	SA_DQ51
52	AL3	SA_DQ52
53	AM2	SA_DQ53
54	AH3	SA_DQ54
55	AG3	SA_DQ55
56	AF3	SA_DQ56
57	AE3	SA_DQ57
58	AD6	SA_DQ58
59	AC4	SA_DQ59
60	AF2	SA_DQ60
61	AF1	SA_DQ61
62	AD4	SA_DQ62
63	AD5	SA_DQ63

SM_CK0	AM33	DDRCLK0 266M	15.8L<
SM_CK0#	AN33	-DDRCLK0 266M	15.8L<
SM_CK1	AL1	DDRCLK1 266M	15.1M<
SM_CK1#	AK1	-DDRCLK1 266M	15.1M<
SM_CK2	AE1		
SM_CK2#	AN1		
SA_MA0	AL17	M A A<13..0>	15.5B<15.5M< 17.4E<
SA_MA1	AP17		
SA_MA2	AP18		
SA_MA3	AM17		
SA_MA4	AN18		
SA_MA5	AM18		
SA_MA6	AL19		
SA_MA7	AP20		
SA_MA8	AM19		
SA_MA9	AL20		
SA_MA10	AM16		
SA_MA11	AN20		
SA_MA12	AM20		
SA_MA13	AM15		
SA_BS0	AK15	M A BS<2..0>	15.4M< 15.5B< 17.7E<
SA_BS1	AK16		
SA_BS2	AL21		
SM_CKE0	AP21	M_CKE<1..0>	15.5B< 15.5M< 17.8E<
SM_CKE1	AM21		
SM_CS0#	AN16	-M CS<1..0>	15.4B< 15.4M< 17.5E<
SM_CS1#	AM14		
SA_RAS#	AP16	-M A RAS	15.4M< 17.6E<
SA_CAS#	AN15	-M A CAS	15.4B< 17.6E<
SA_WE#	AP15	-M A WE	15.4B< 17.6E<
SA_DM0	AJ37	M_A DM<7..0>	15.6B< 15.7L<
SA_DM1	AP35		
SA_DM2	AL29		
SA_DM3	AP24		
SA_DM4	AP9		
SA_DM5	AP4		
SA_DM6	AJ2		
SA_DM7	AD3		
SM_ODT0	AP14	M ODT<1..0>	15.3B< 15.4M< 17.7E<
SM_ODT1	AL15		
SA_RCVENIN#	AF29		
SA_RCVENOUT#	AF28		

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
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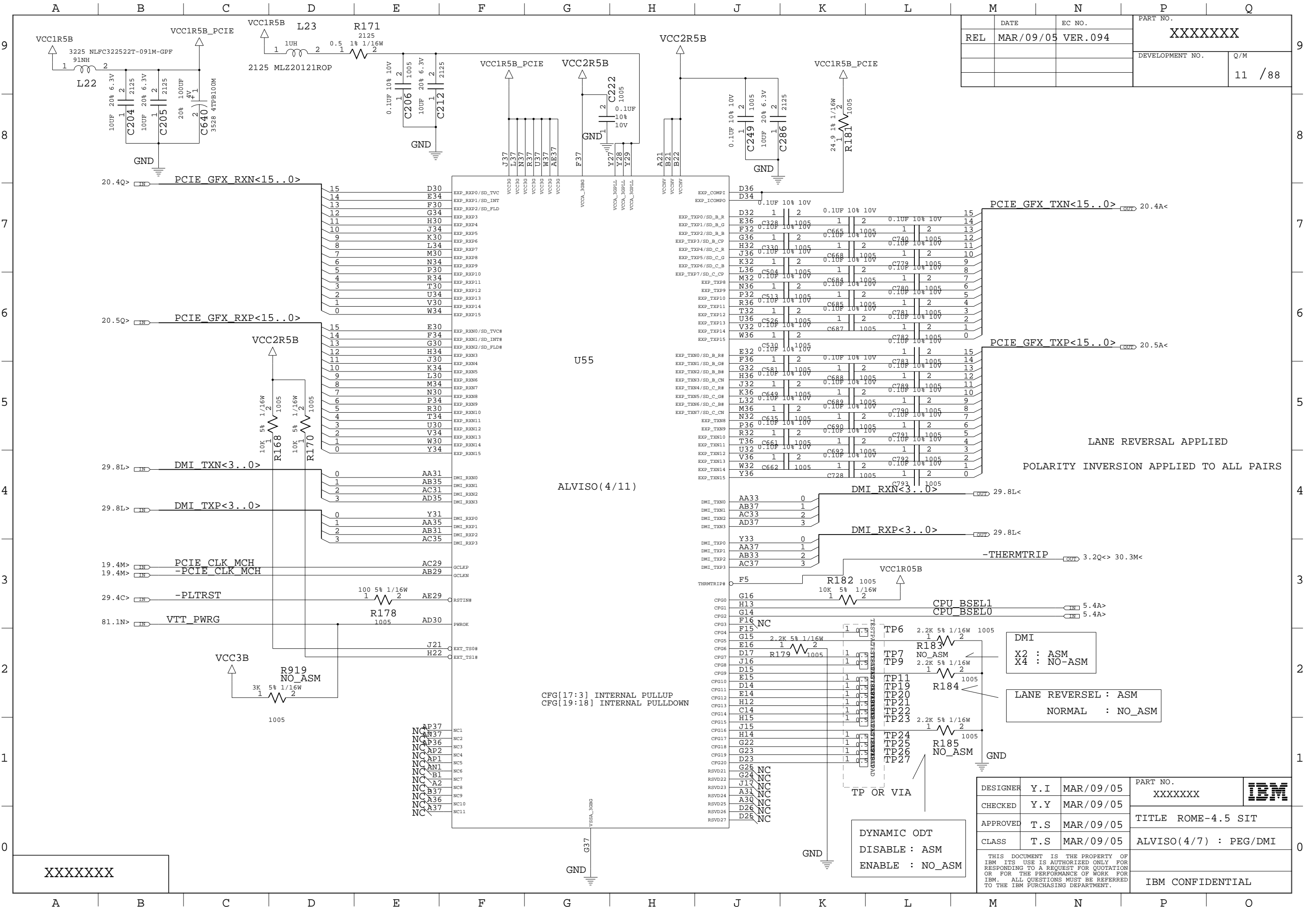


DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		10 /88

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
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		11 / 88



LANE REVERSAL APPLIED
POLARITY INVERSION APPLIED TO ALL PAIRS

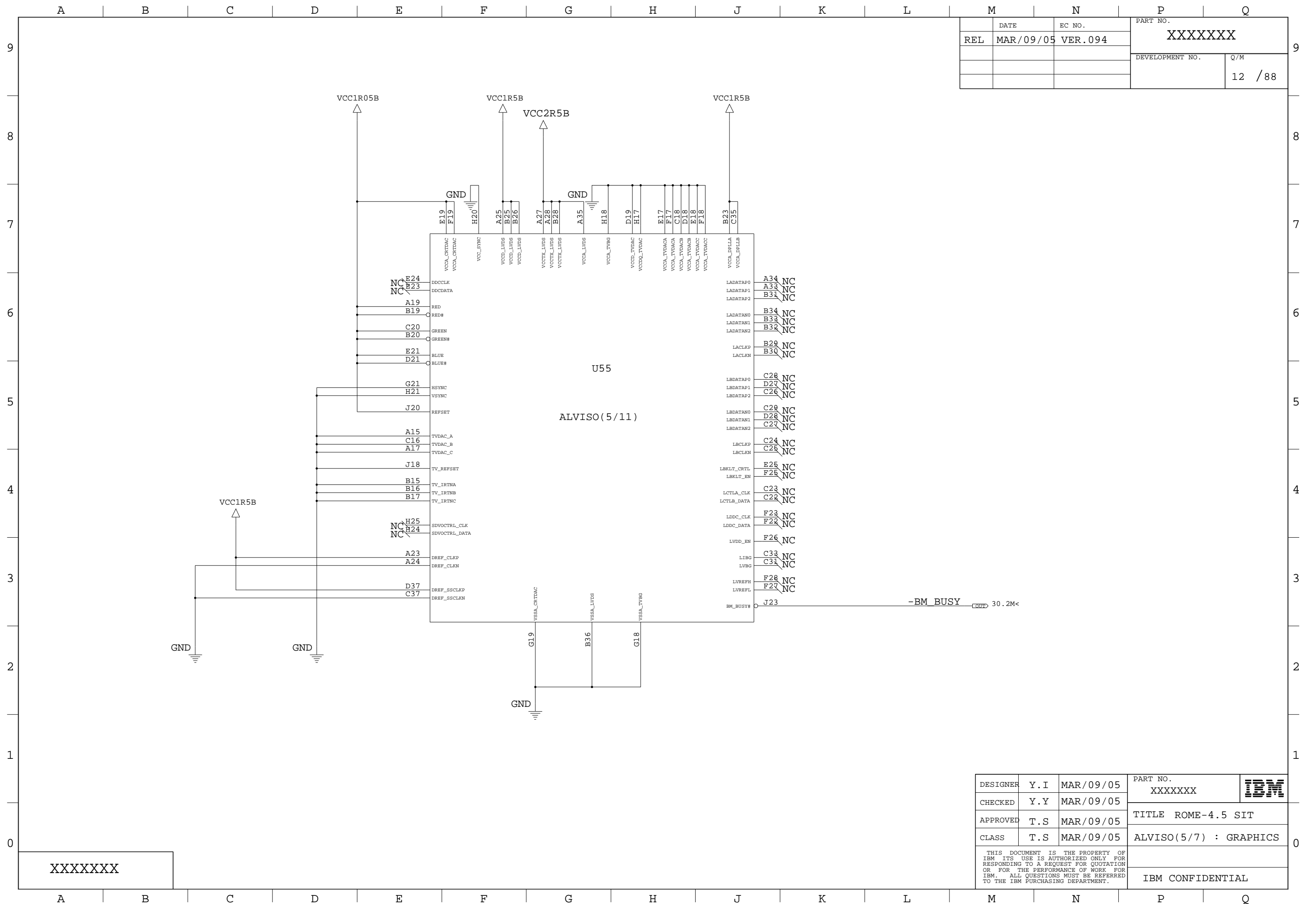
DMI
X2 : ASM
X4 : NO-ASM

LANE REVERSEL : ASM
NORMAL : NO_ASM

DYNAMIC ODT
DISABLE : ASM
ENABLE : NO_ASM

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05	XXXXXXXX		
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CLASS	T.S	MAR/09/05	ALVISO(4/7) : PEG/DMI		
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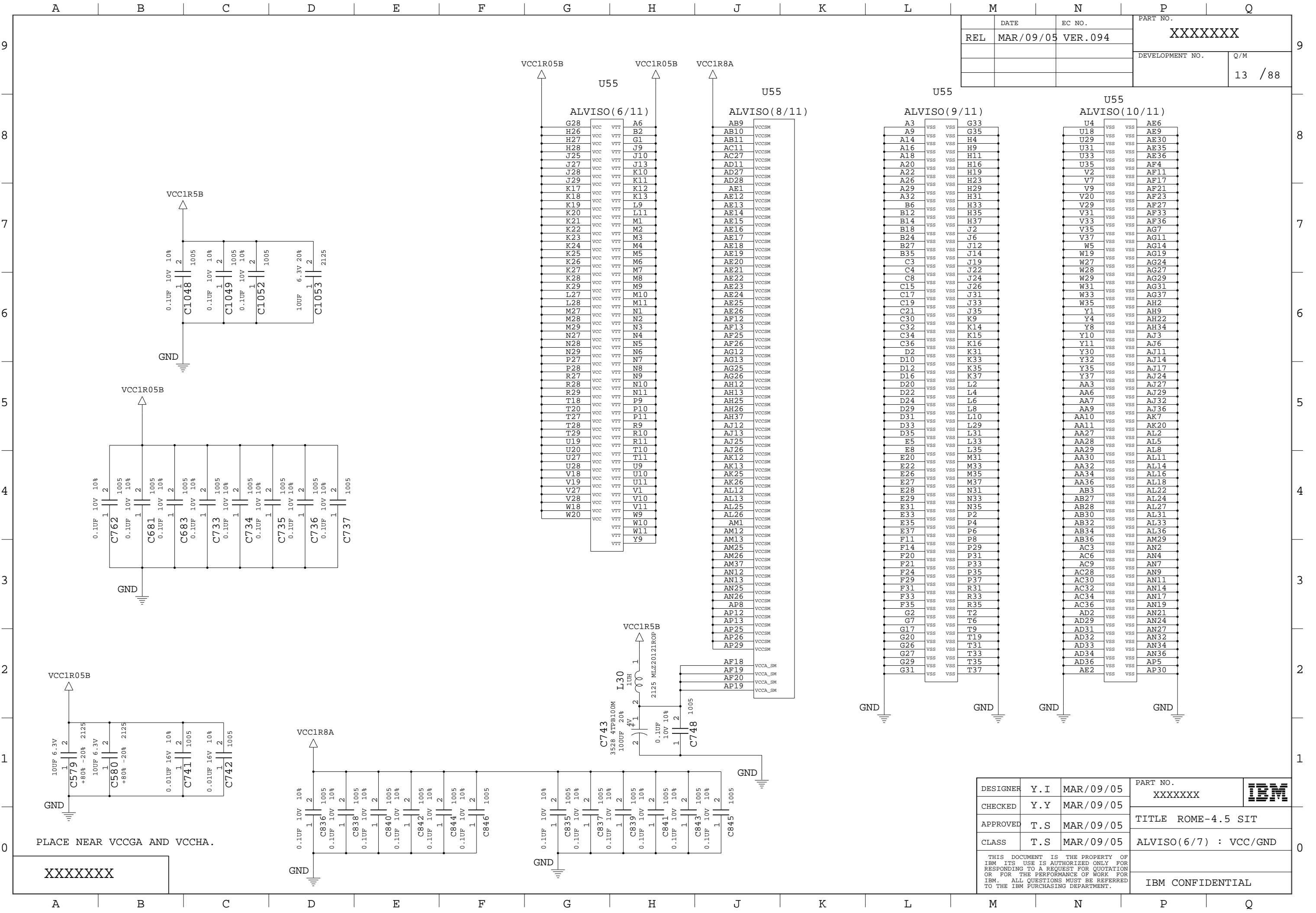
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			DEVELOPMENT NO.	Q/M
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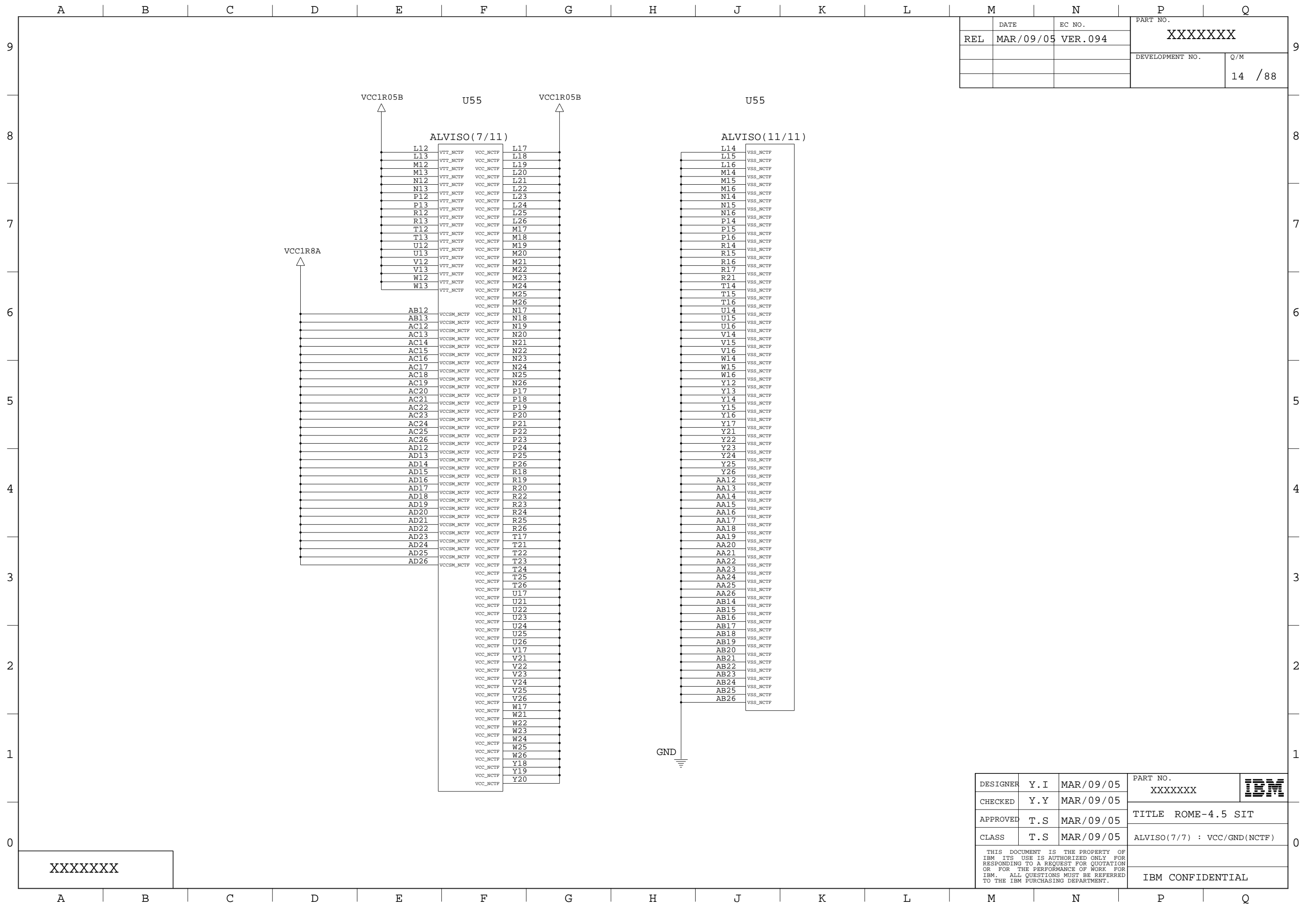
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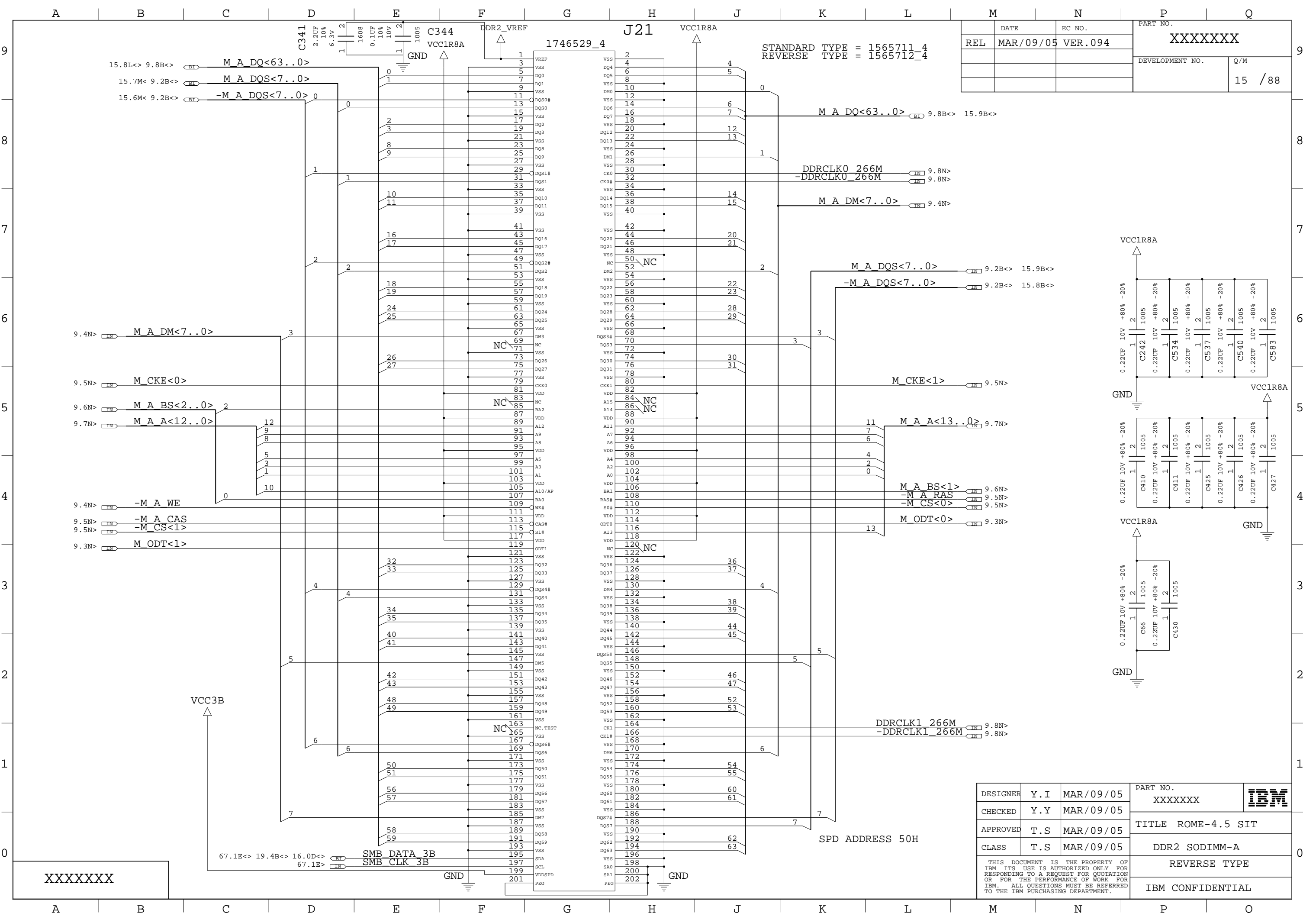
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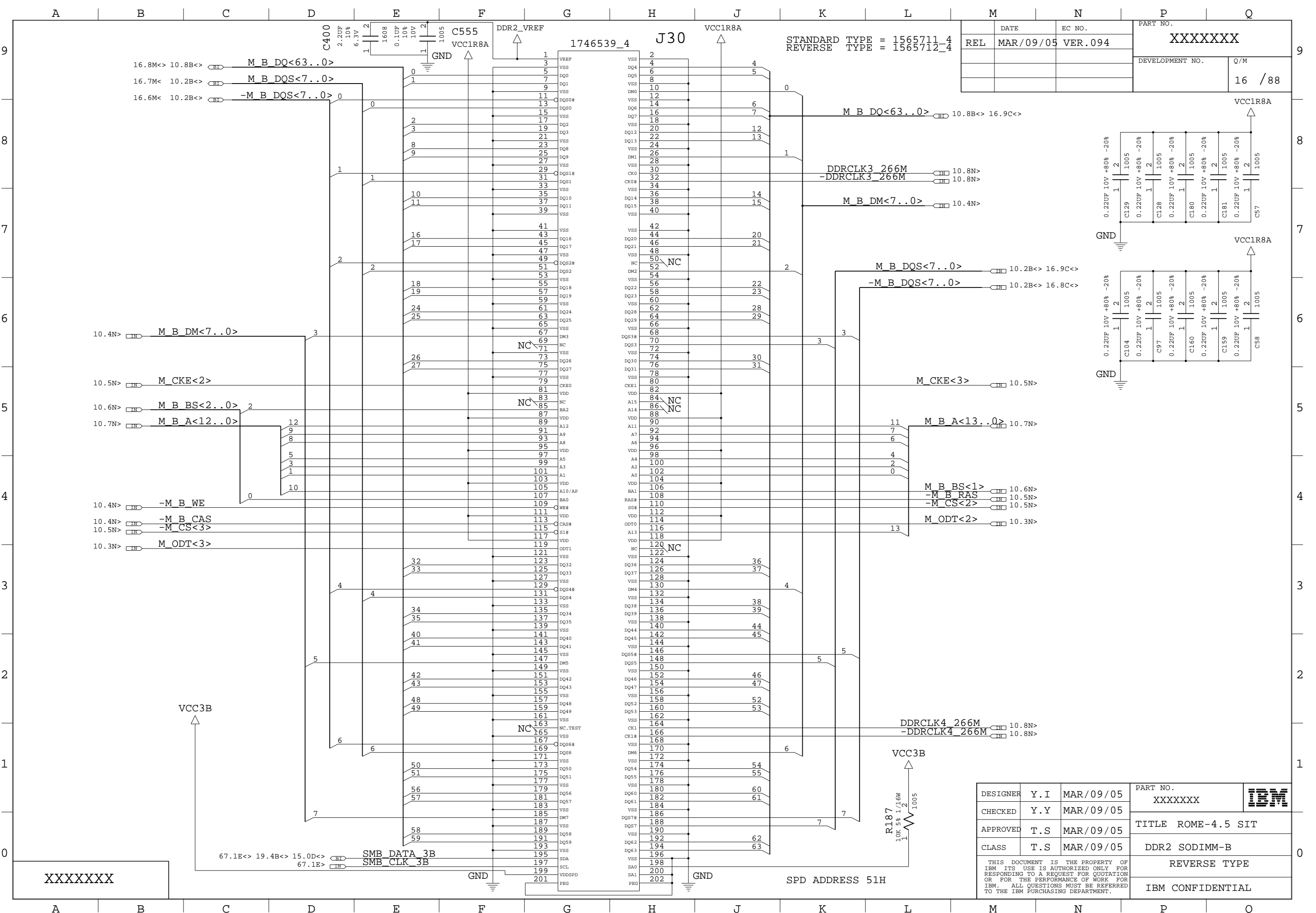
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REL		DEVELOPMENT NO.
		15 / 88

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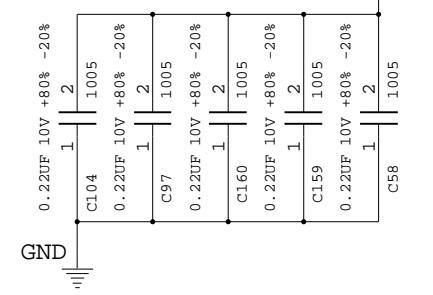
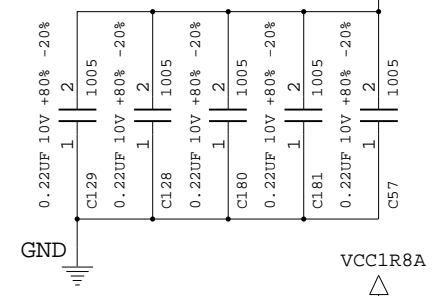
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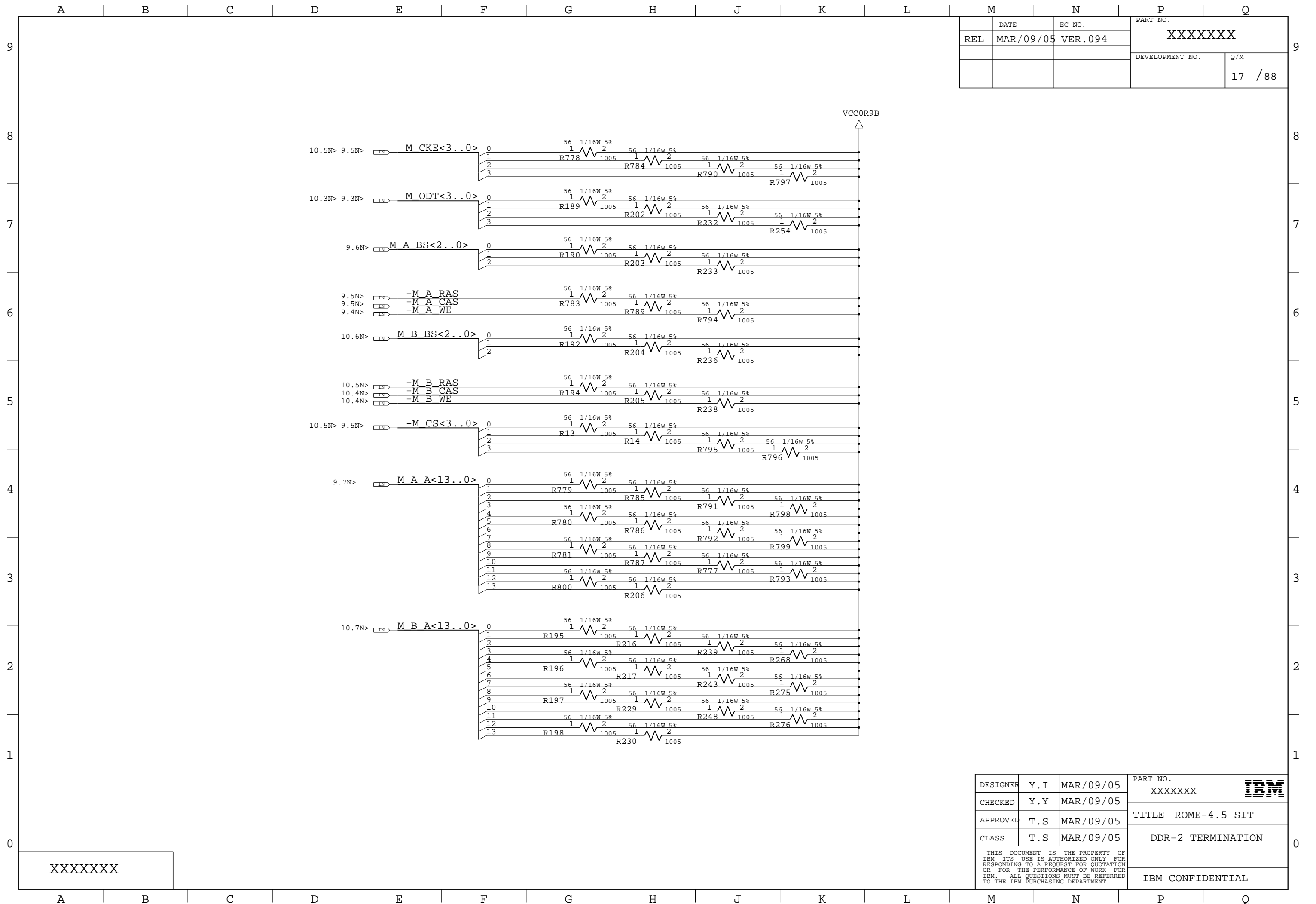
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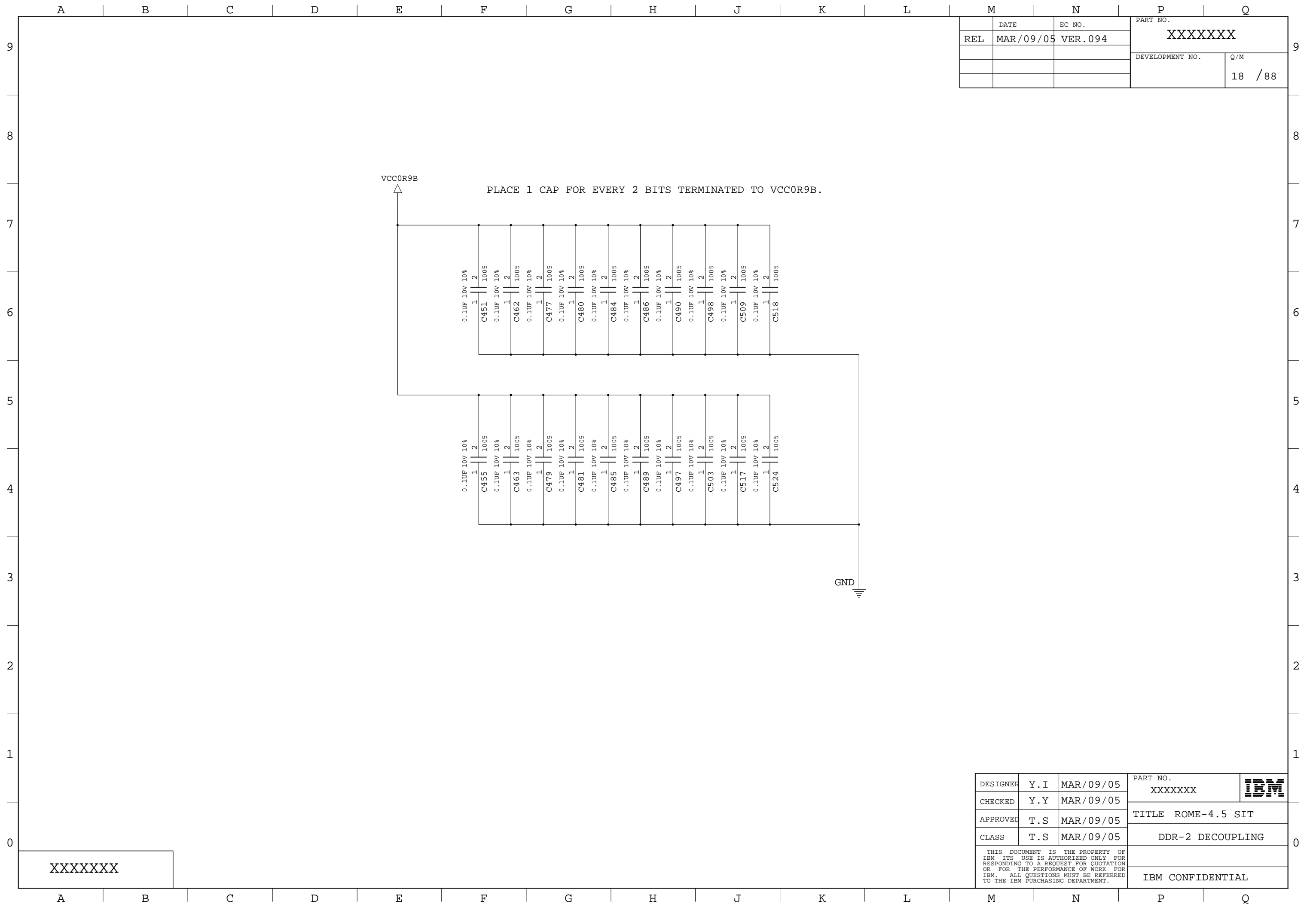
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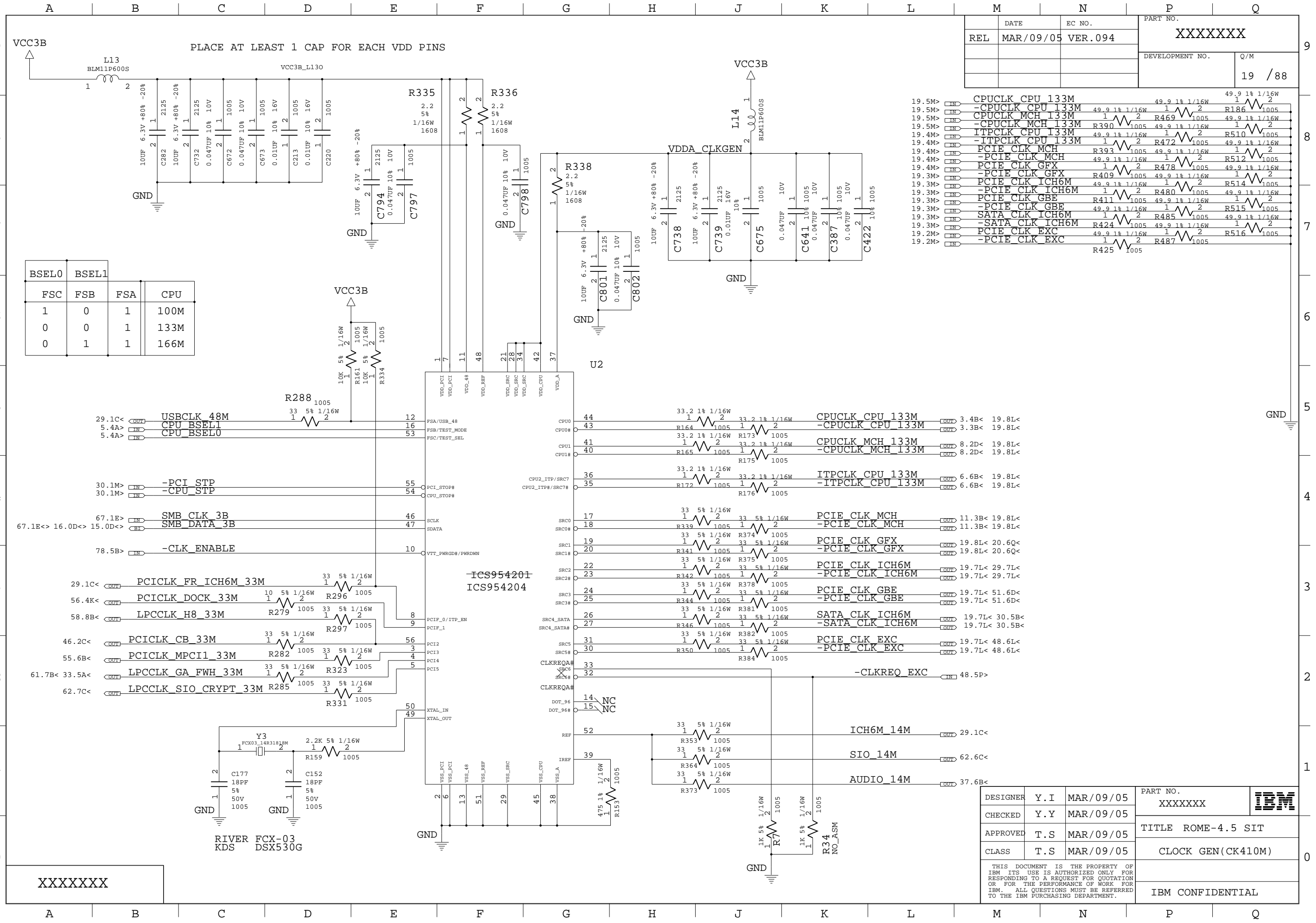
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PLACE AT LEAST 1 CAP FOR EACH VDD PINS

BSEL0	BSEL1	FSC	FSB	FSA	CPU
1	0	1			100M
0	0	1			133M
0	1	1			166M

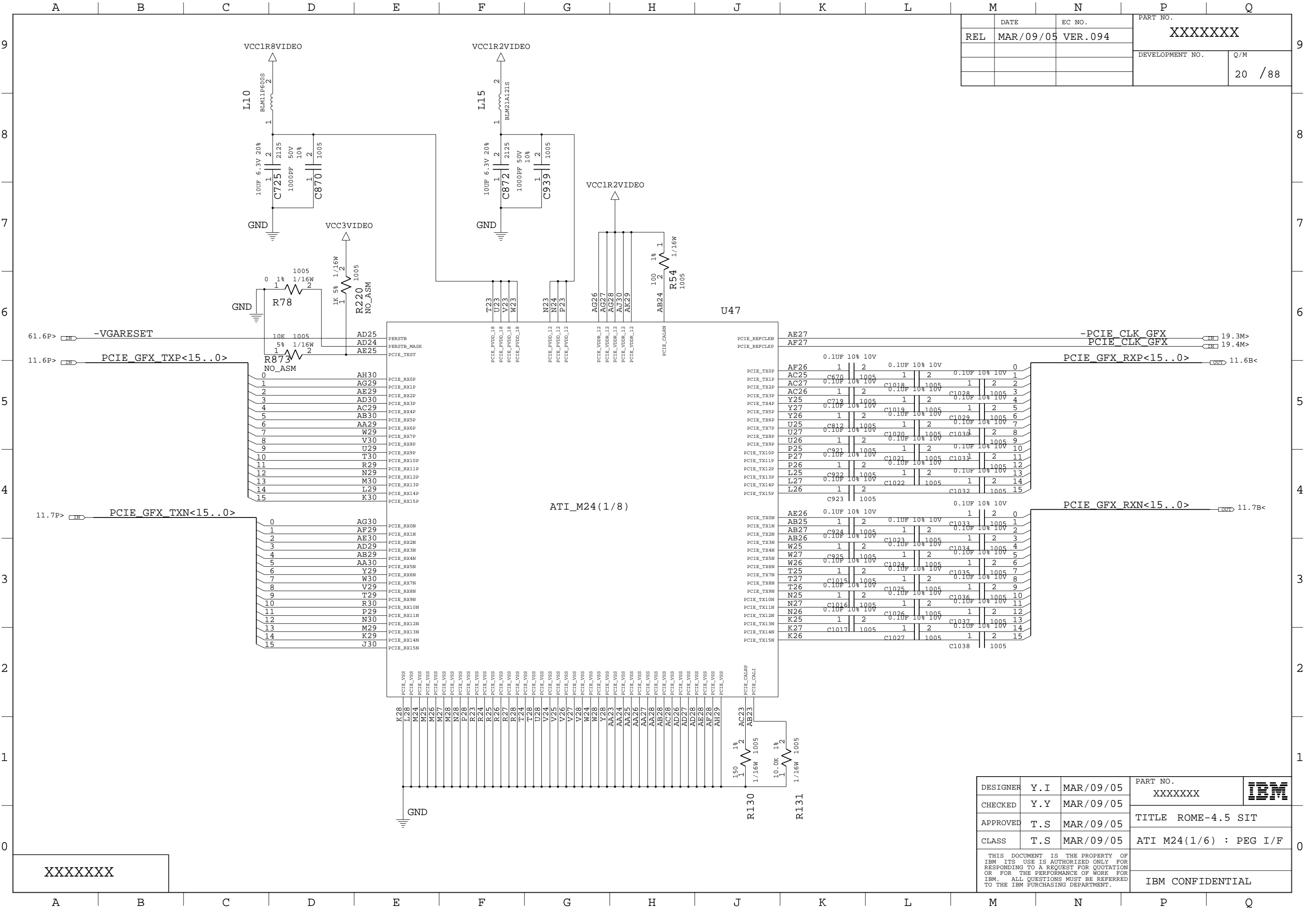
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DEVELOPMENT NO.			Q/M
			19 / 88

Signal	Value	Component	Value	Component	Value	Component
CPUCLK CPU 133M	49.9 1% 1/16W	R186	1005			
CPUCLK MCH 133M	49.9 1% 1/16W	R196	1005			
ITPCLK CPU 133M	49.9 1% 1/16W	R510	1005			
PCIE CLK MCH	49.9 1% 1/16W	R186	1005			
PCIE CLK GFX	49.9 1% 1/16W	R512	1005			
PCIE CLK ICH6M	49.9 1% 1/16W	R514	1005			
PCIE CLK GBE	49.9 1% 1/16W	R515	1005			
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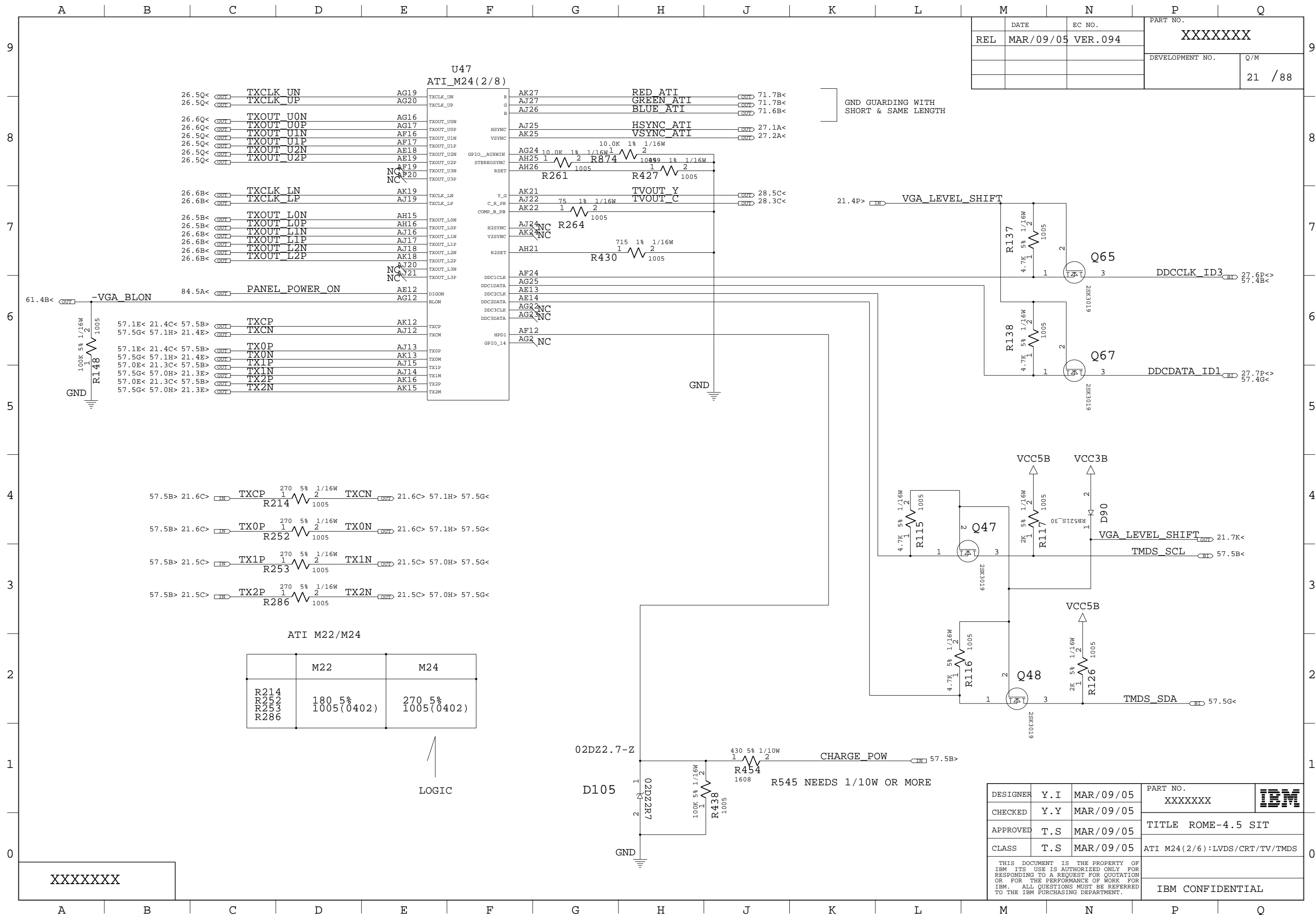
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CLASS	T.S	MAR/09/05	CLOCK GEN(CK410M)		
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CLASS	T. S	MAR/09/05	ATI M24(1/6) : PEG I/F		
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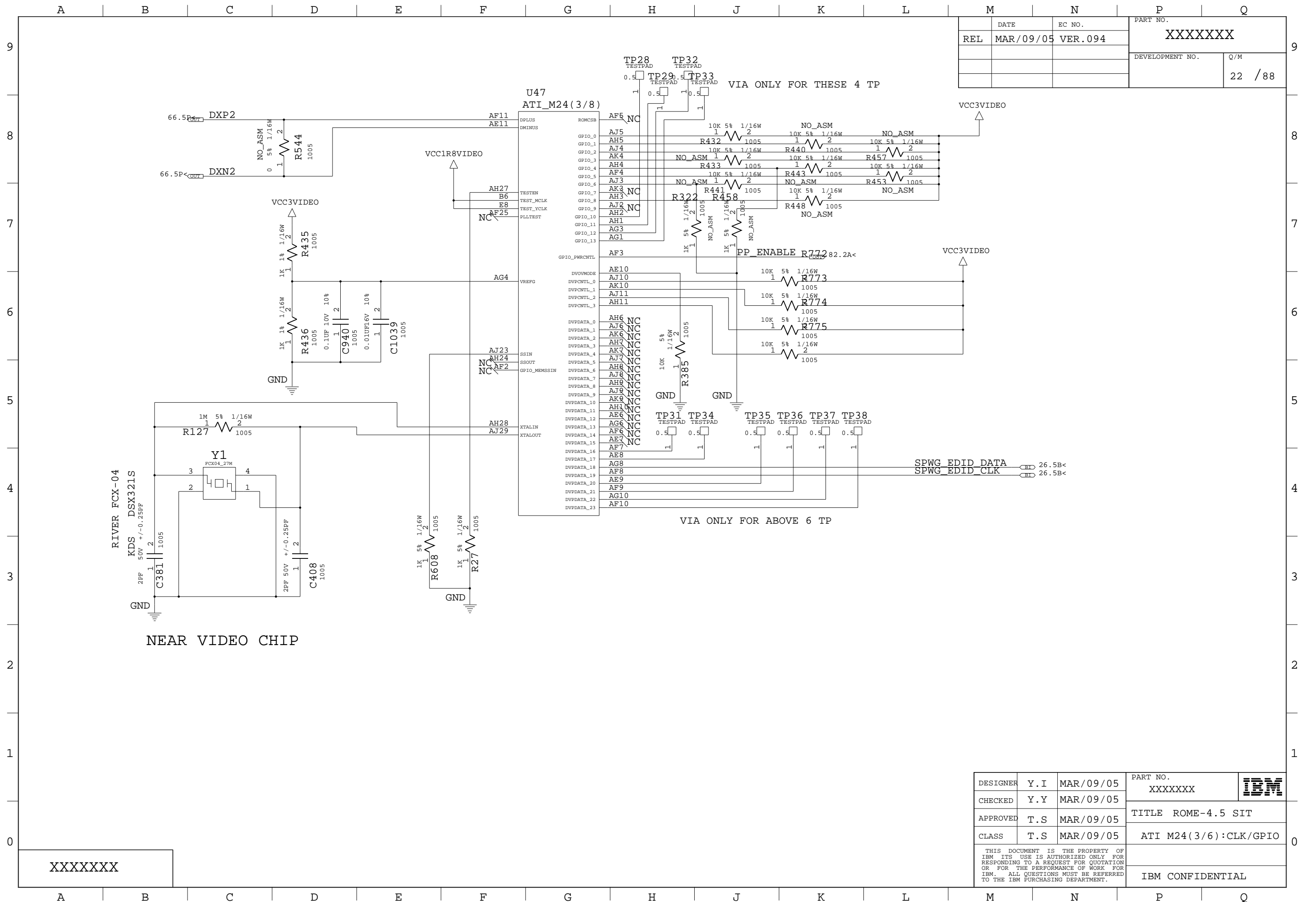


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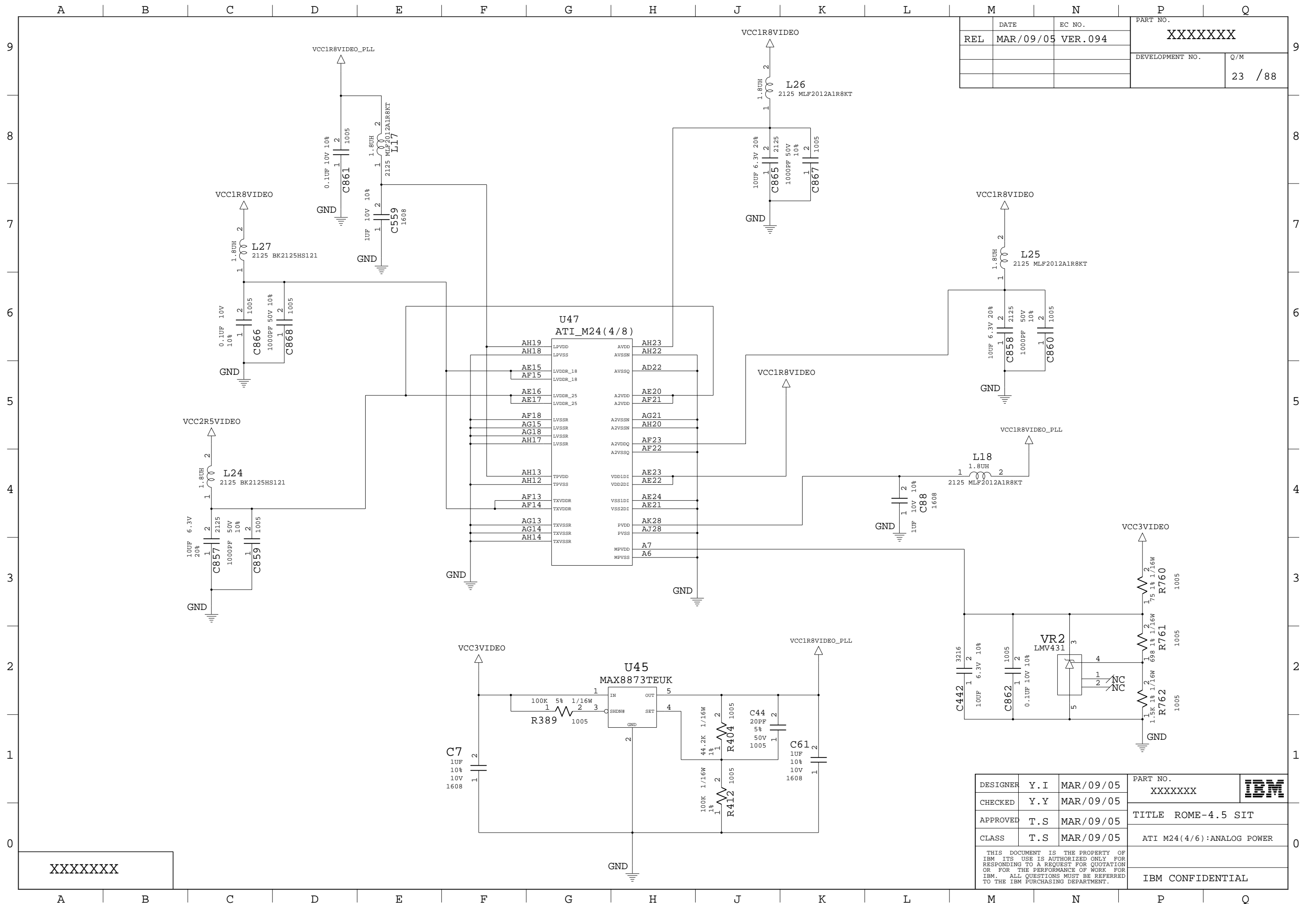




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			DEVELOPMENT NO.	Q/M
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CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	ATI M24(3/6):CLK/GPIO		
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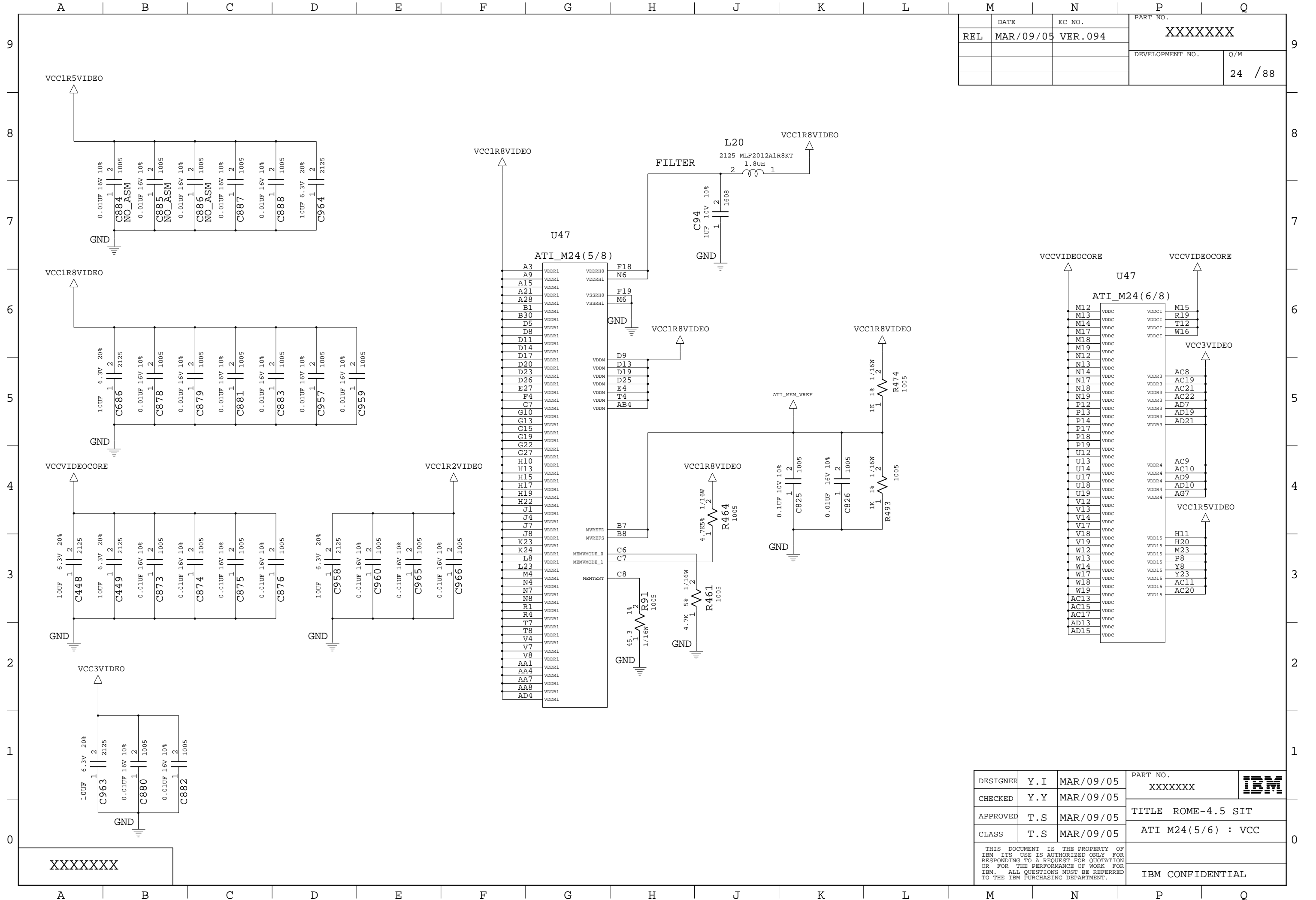


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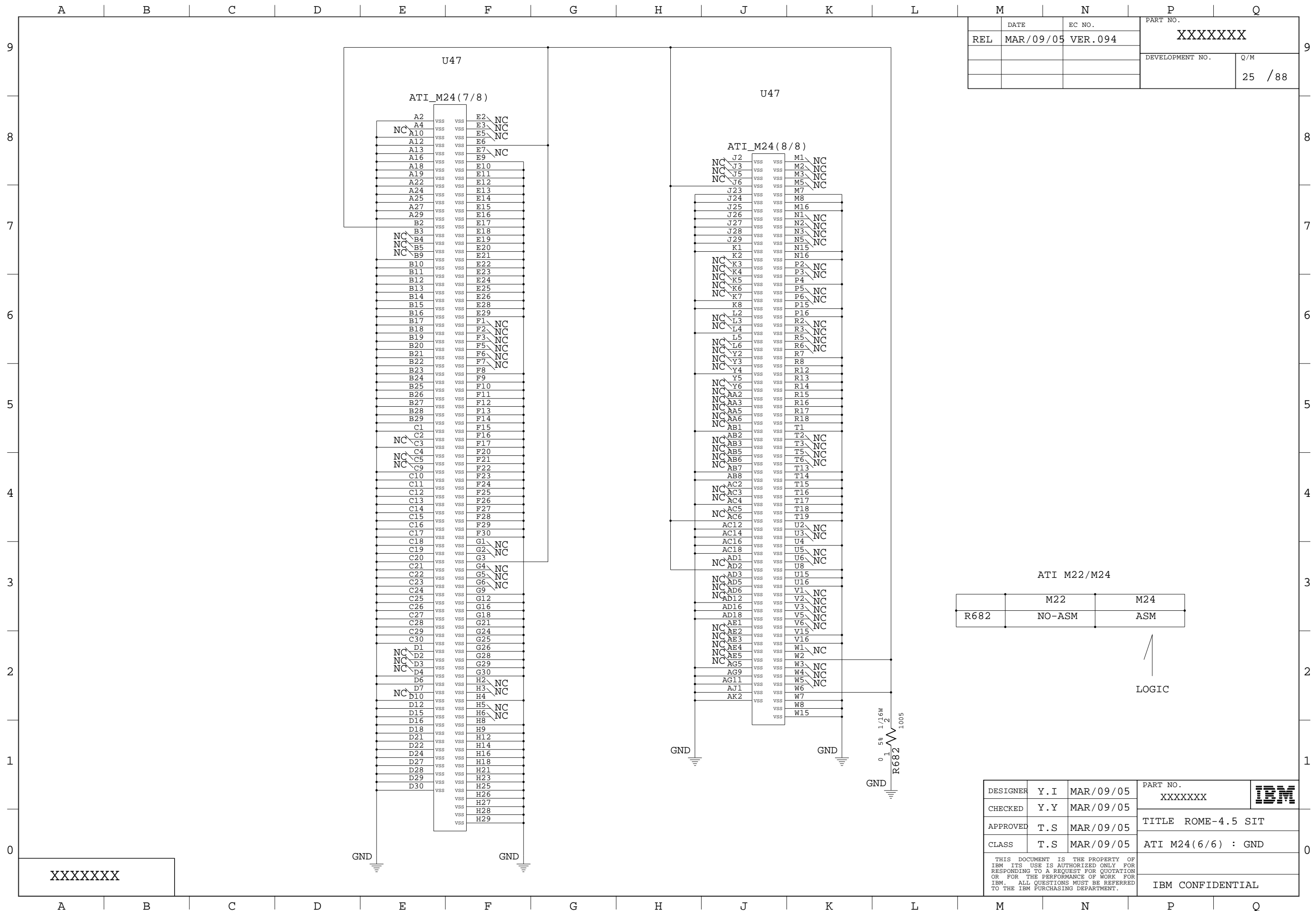
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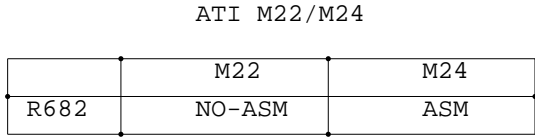


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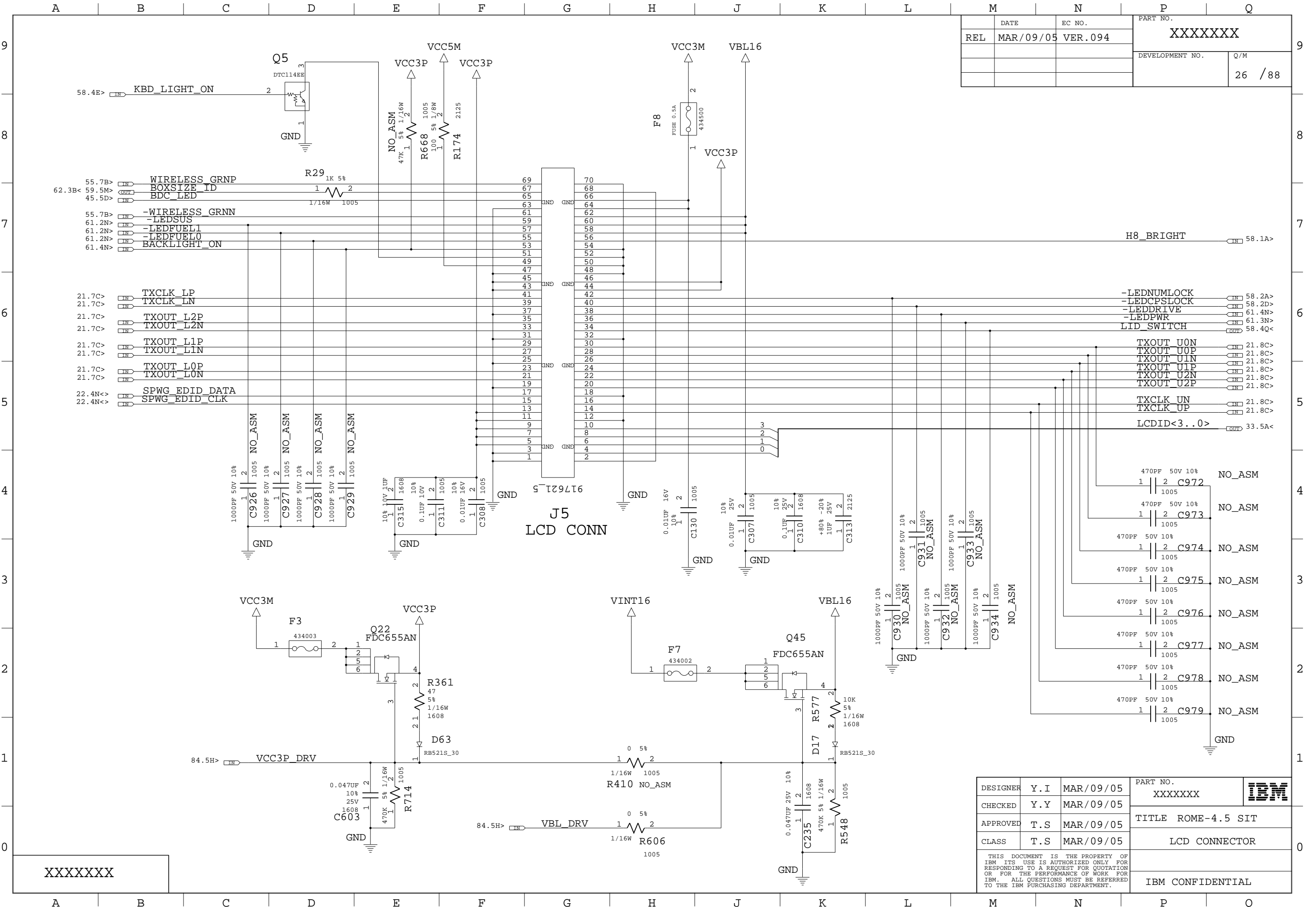
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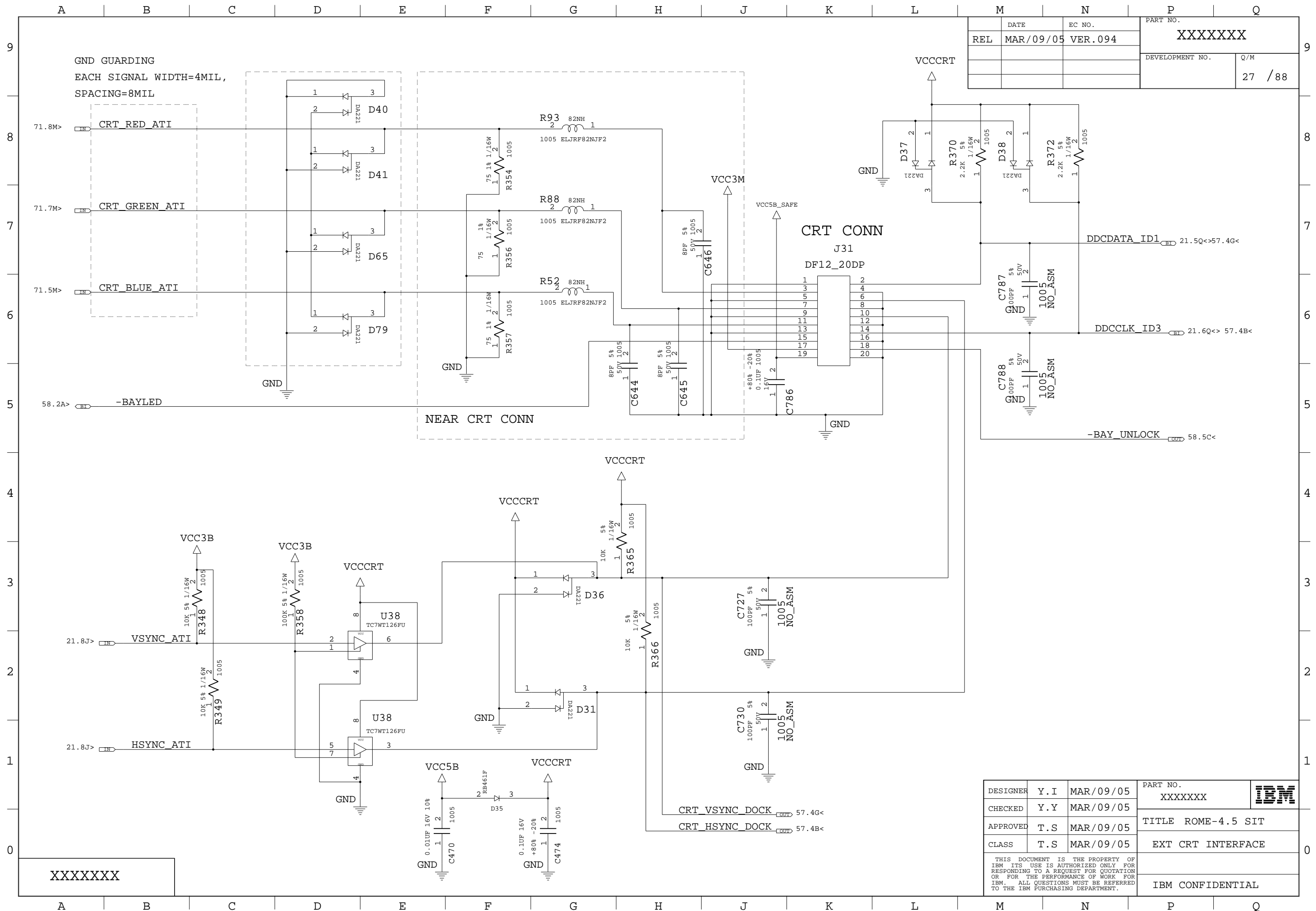


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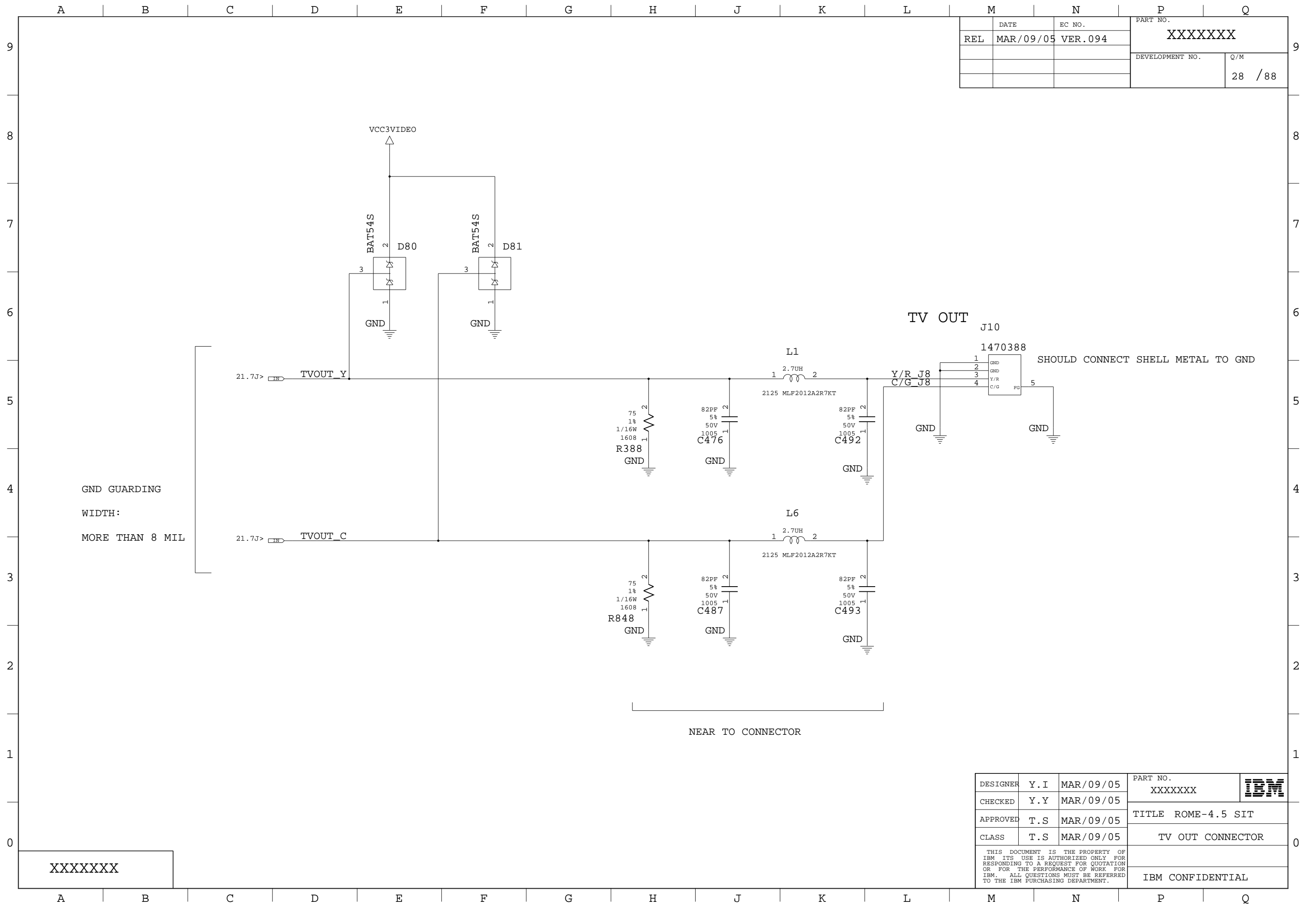
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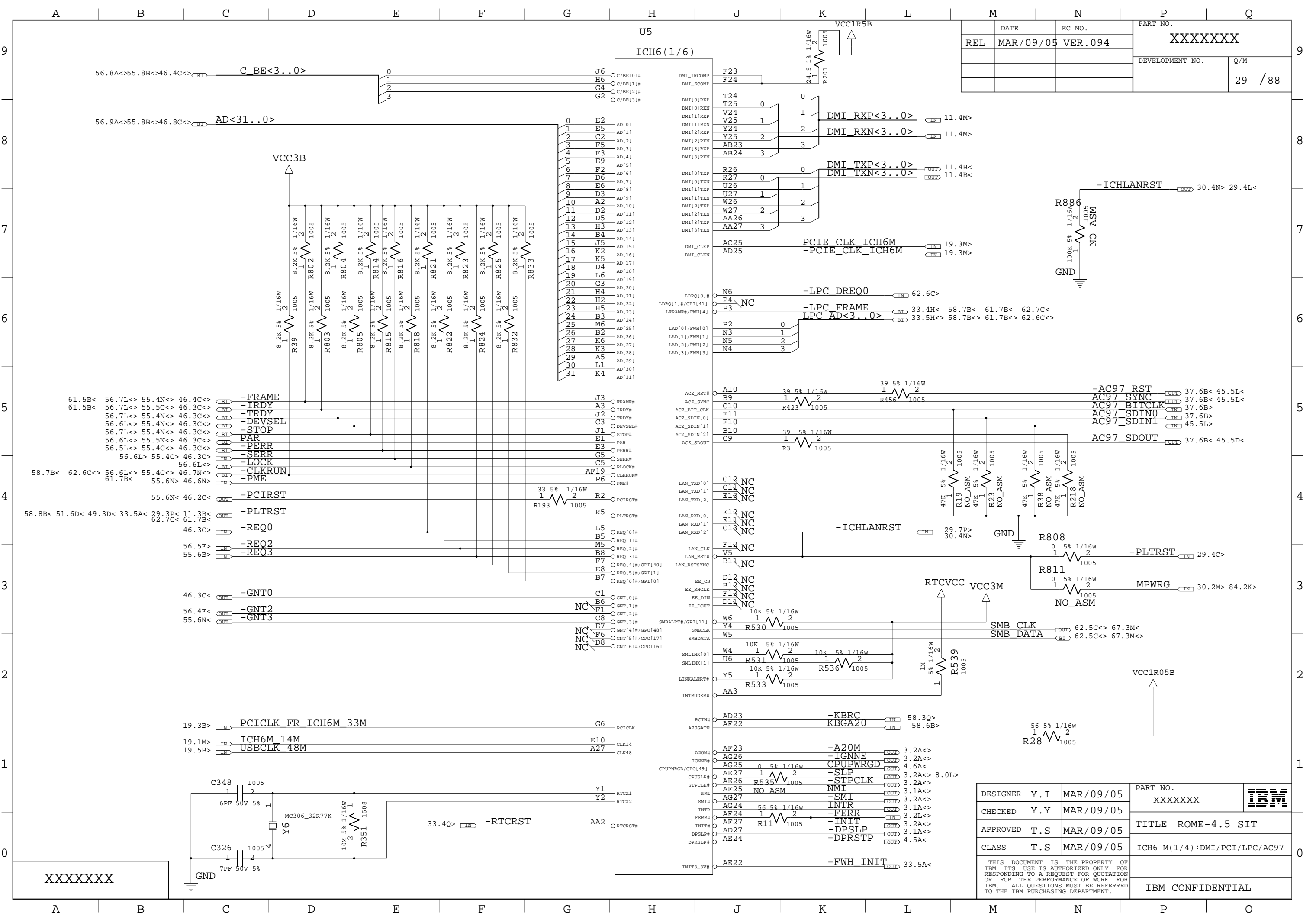
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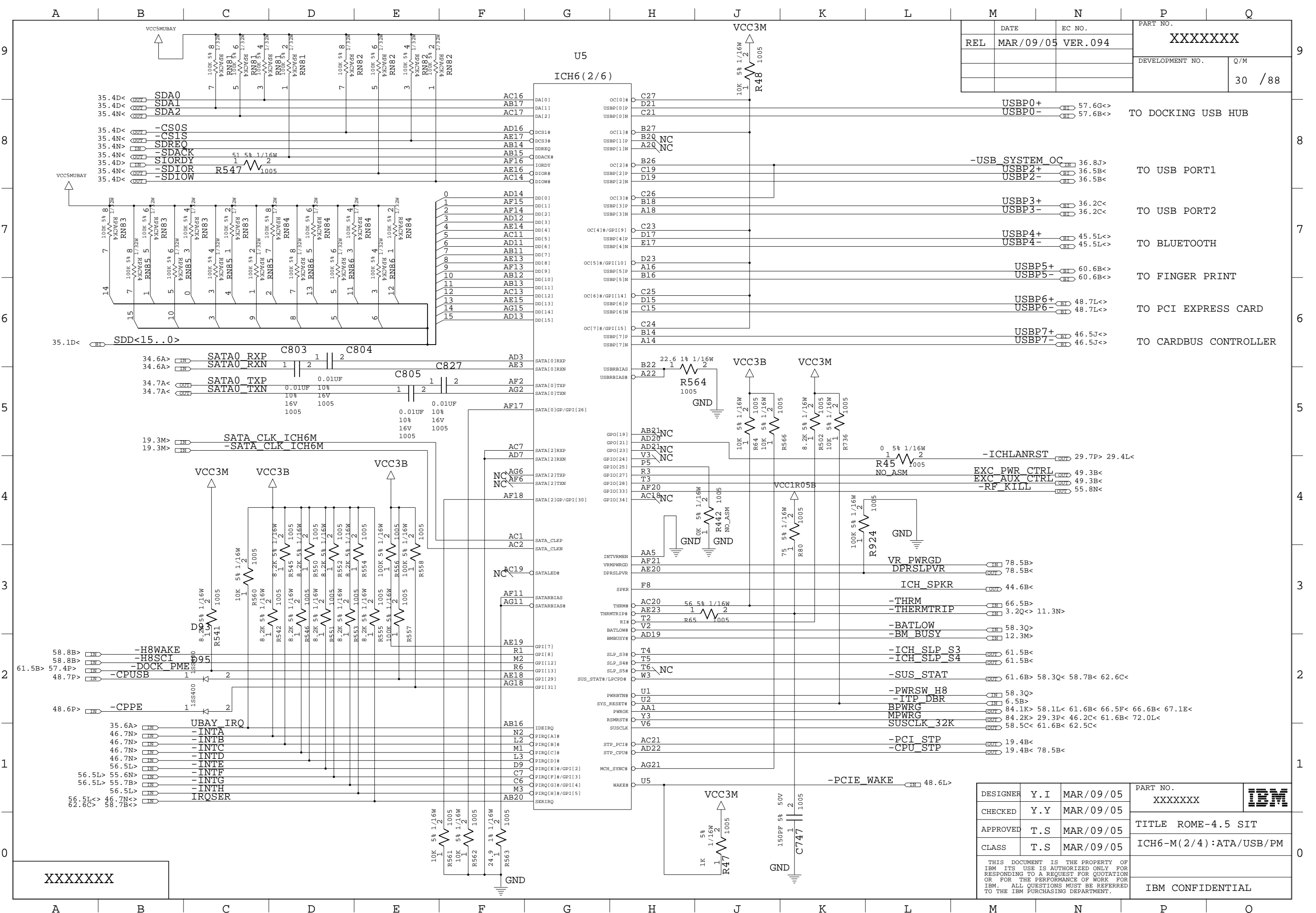
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CLASS	T. S	MAR/09/05	ICH6-M(1/4):DMI/PCI/LPC/AC97		
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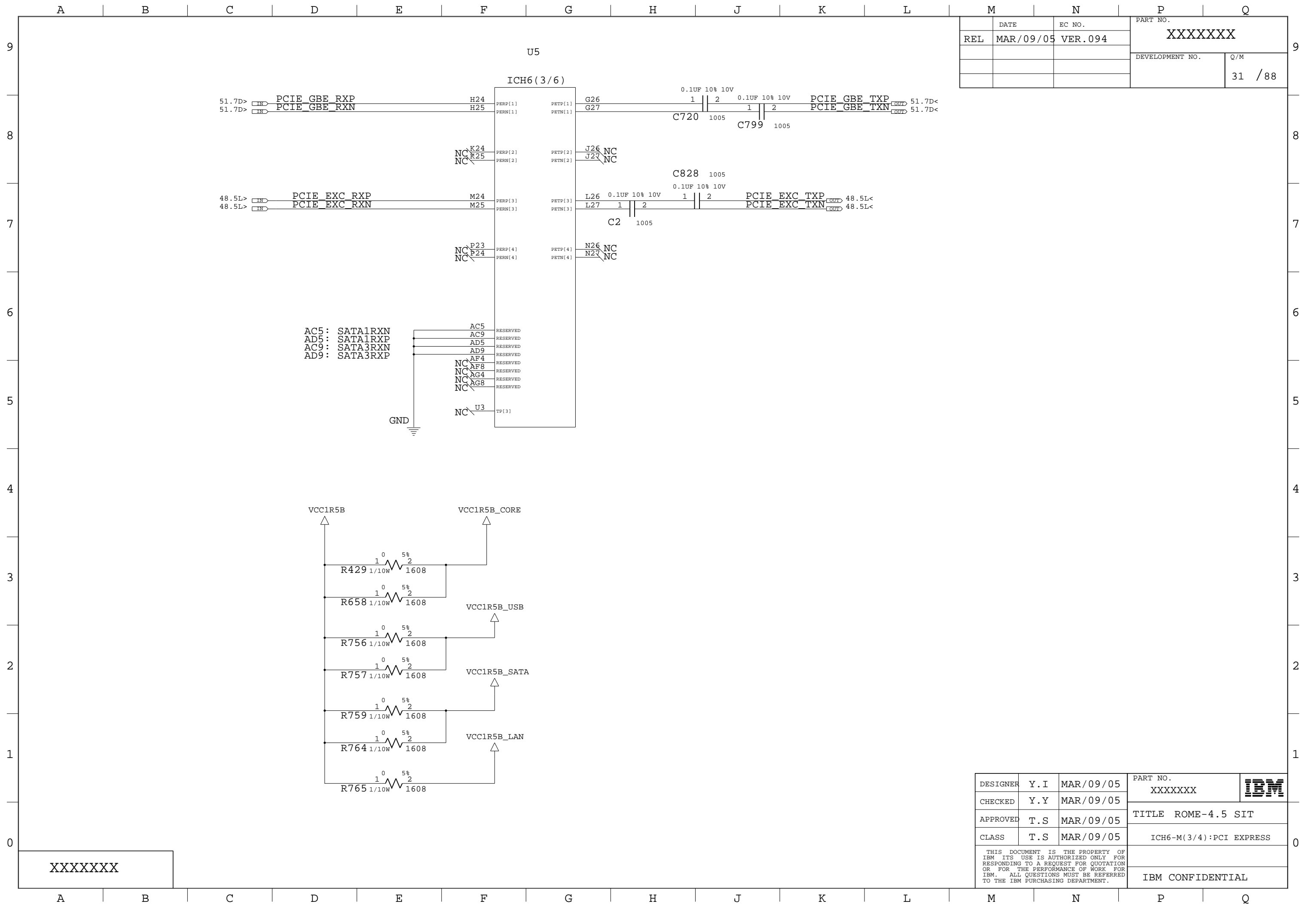


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DEVELOPMENT NO.			Q/M
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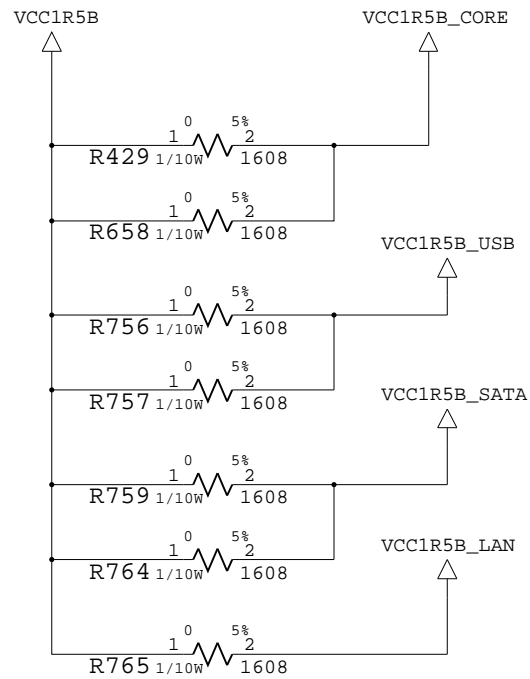
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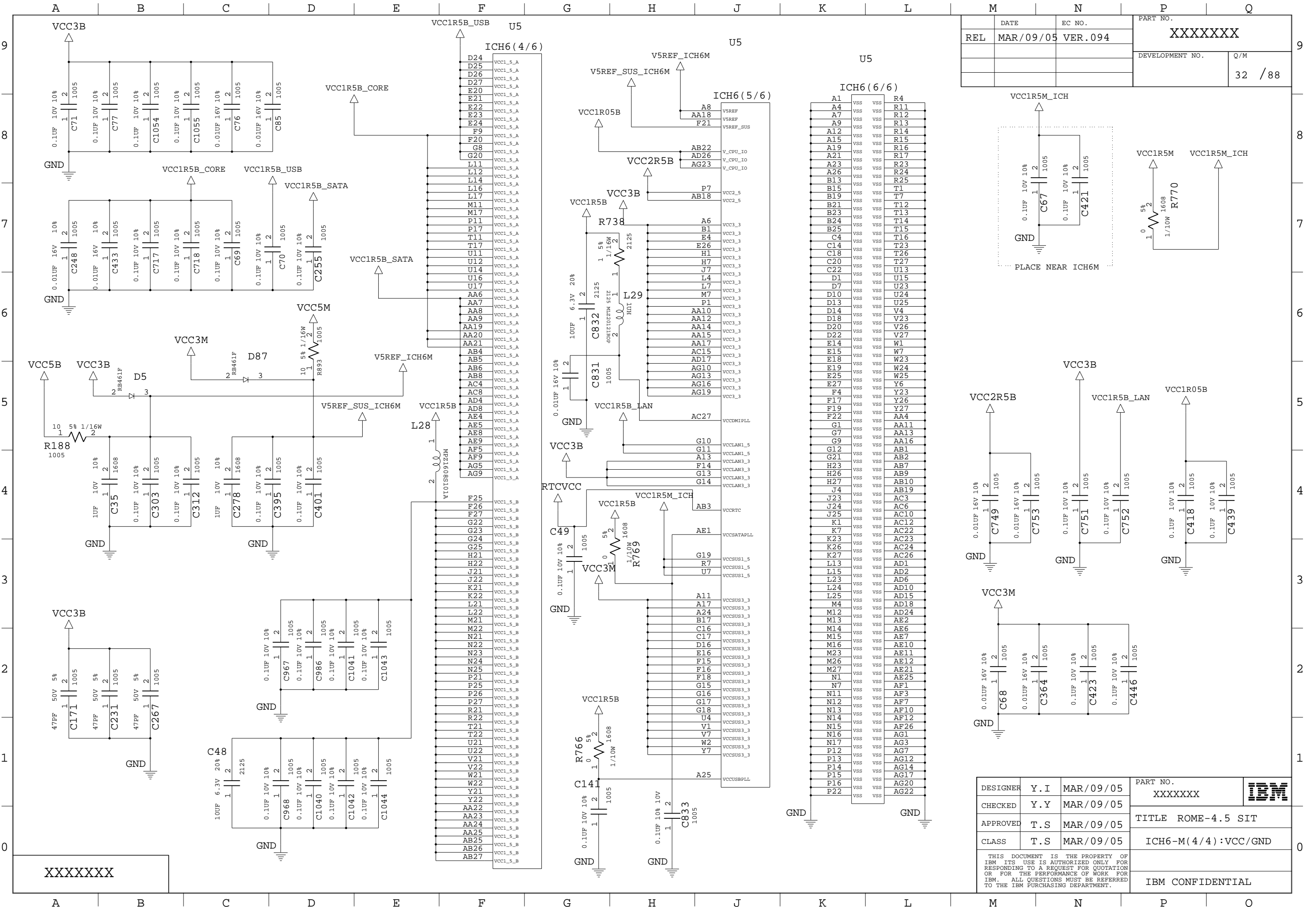
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REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
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AC5: SATA1RXN
 AD5: SATA1RXP
 AC9: SATA3RXN
 AD9: SATA3RXP



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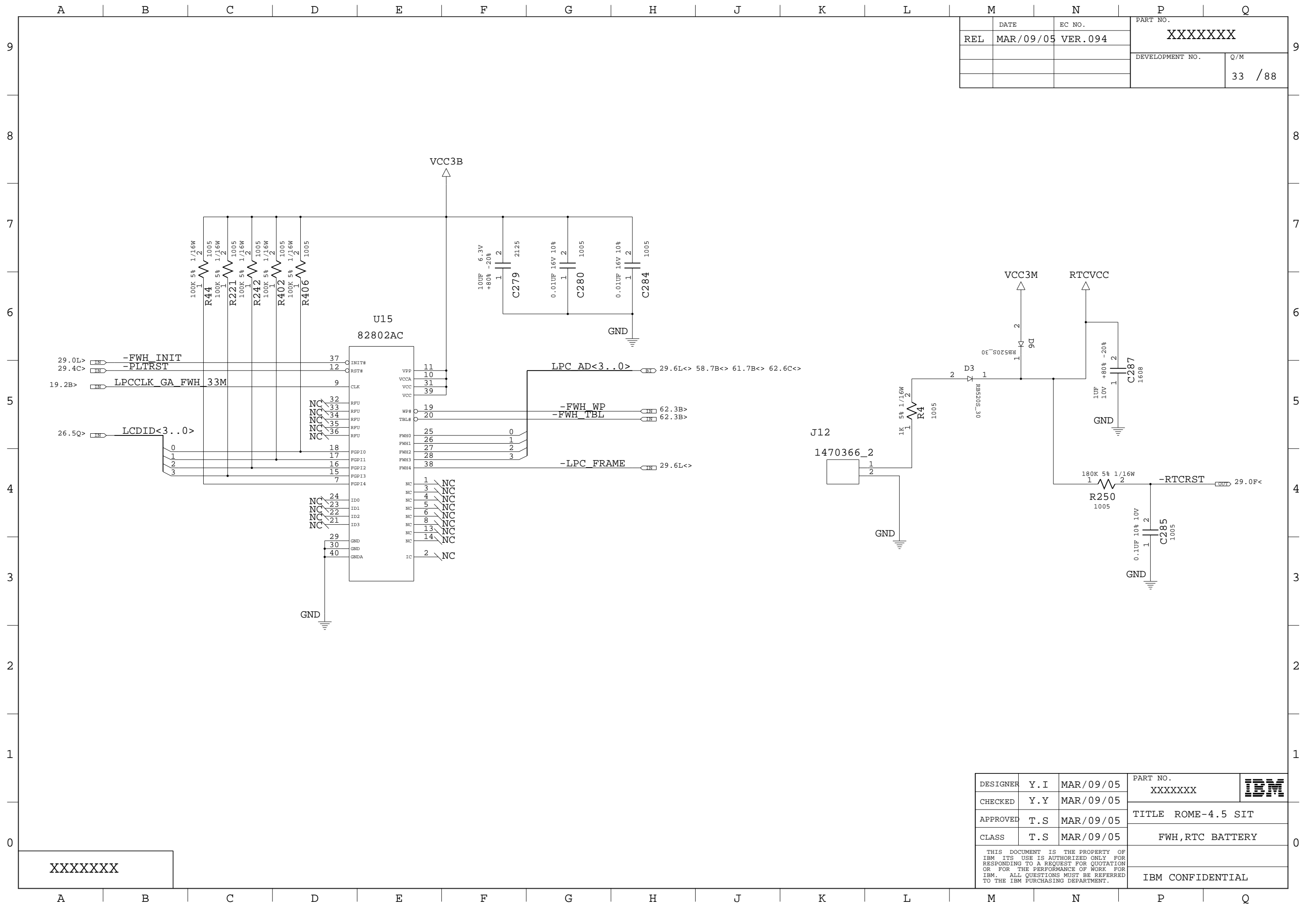


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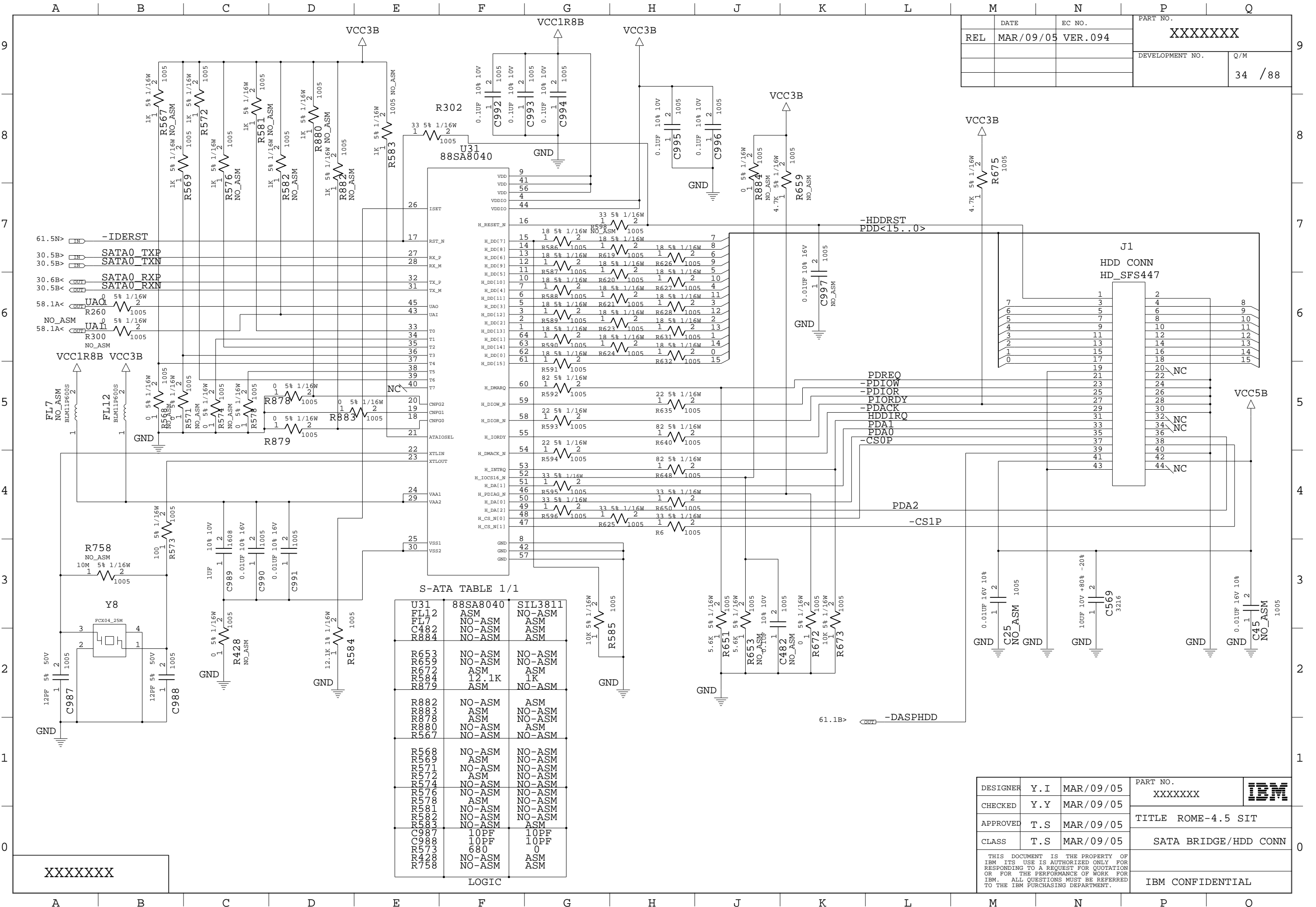


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			DEVELOPMENT NO.
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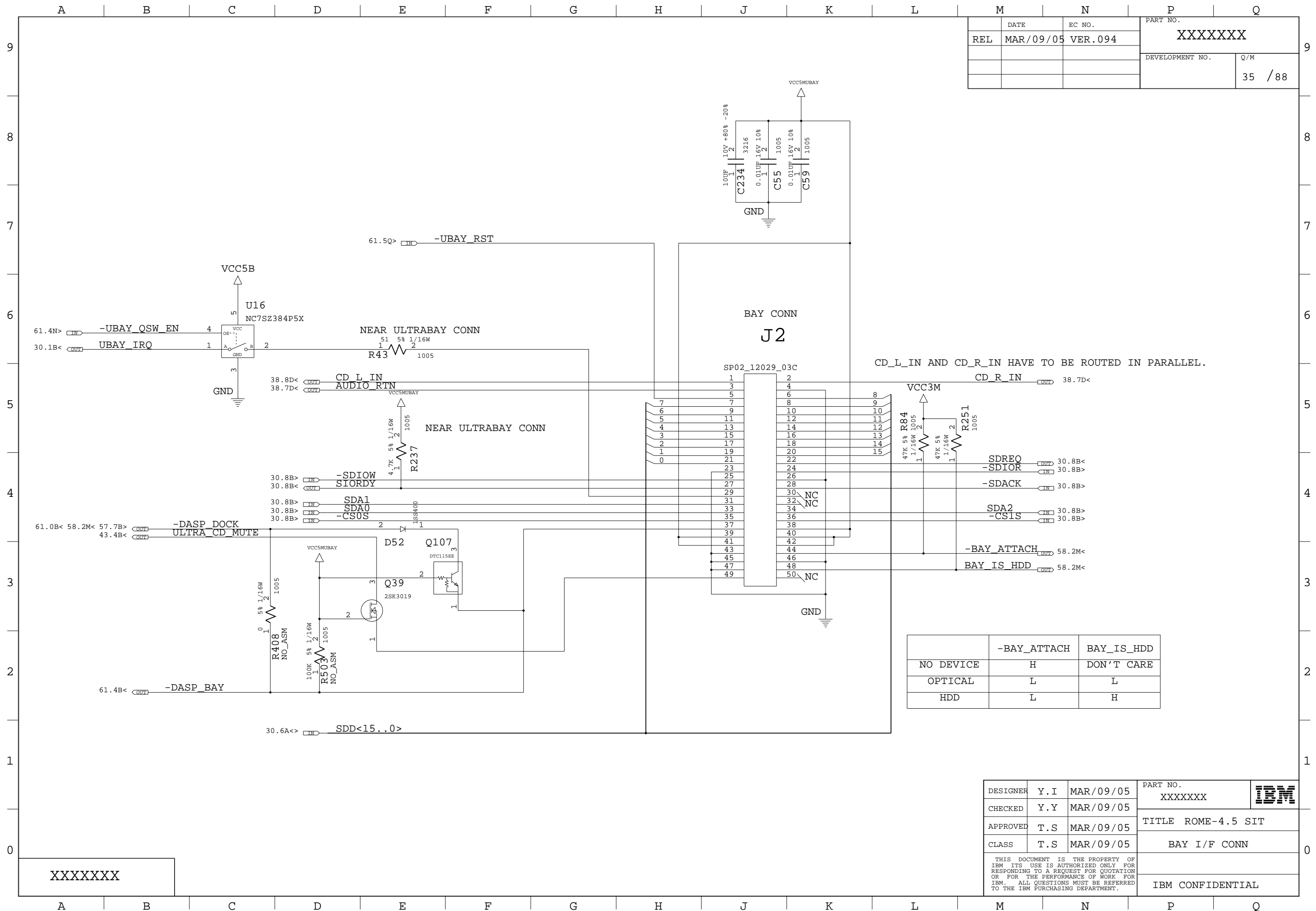
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R6	NO-ASM	NO-ASM
R605	NO-ASM	NO-ASM
R606	NO-ASM	NO-ASM
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R608	NO-ASM	NO-ASM
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R757	NO-ASM	NO-ASM
R758	NO-ASM	NO-ASM

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	SATA BRIDGE/HDD CONN		
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LOGIC

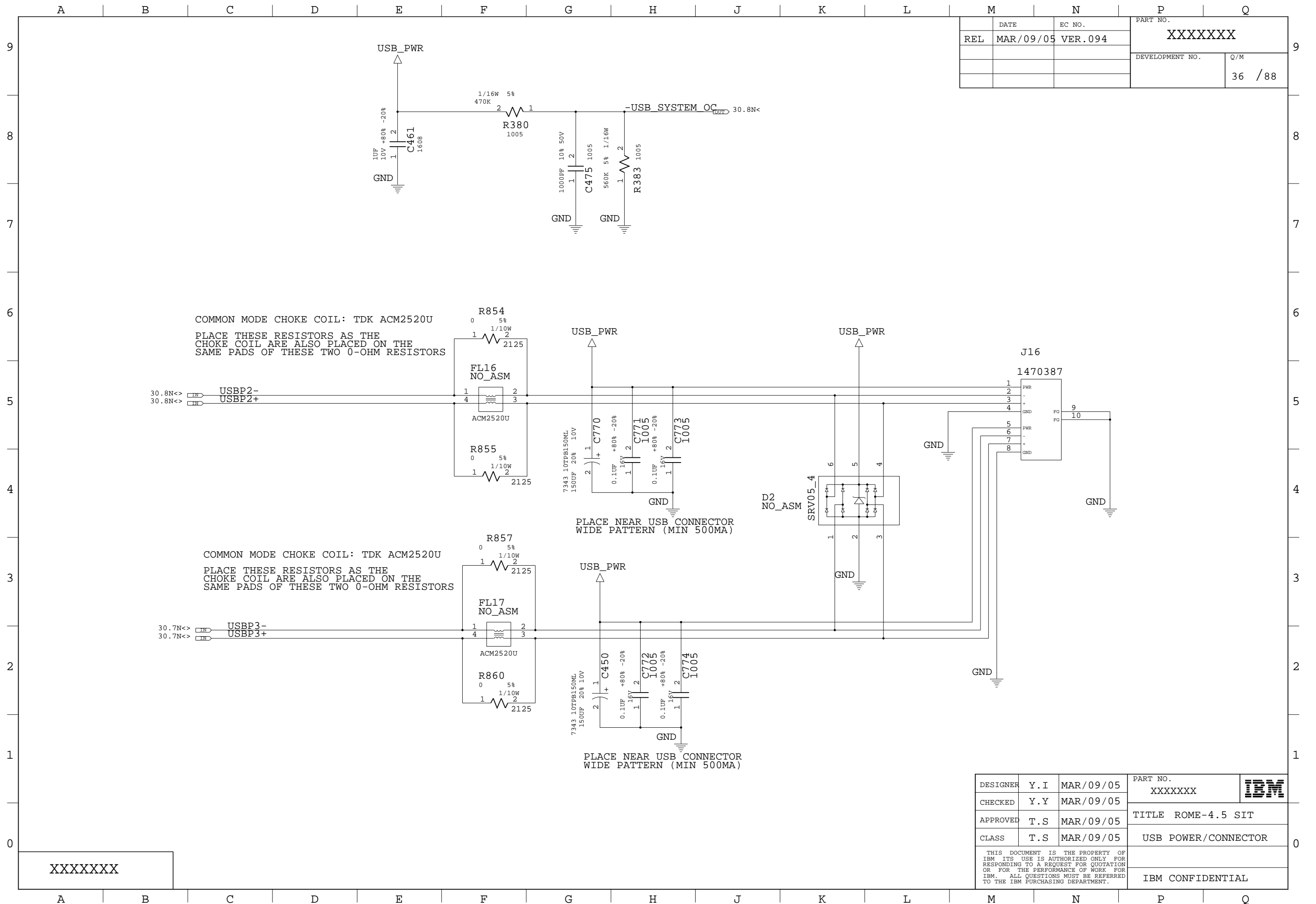


REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			35 / 88

	-BAY_ATTACH	BAY_IS_HDD
NO DEVICE	H	DON'T CARE
OPTICAL	L	L
HDD	L	H

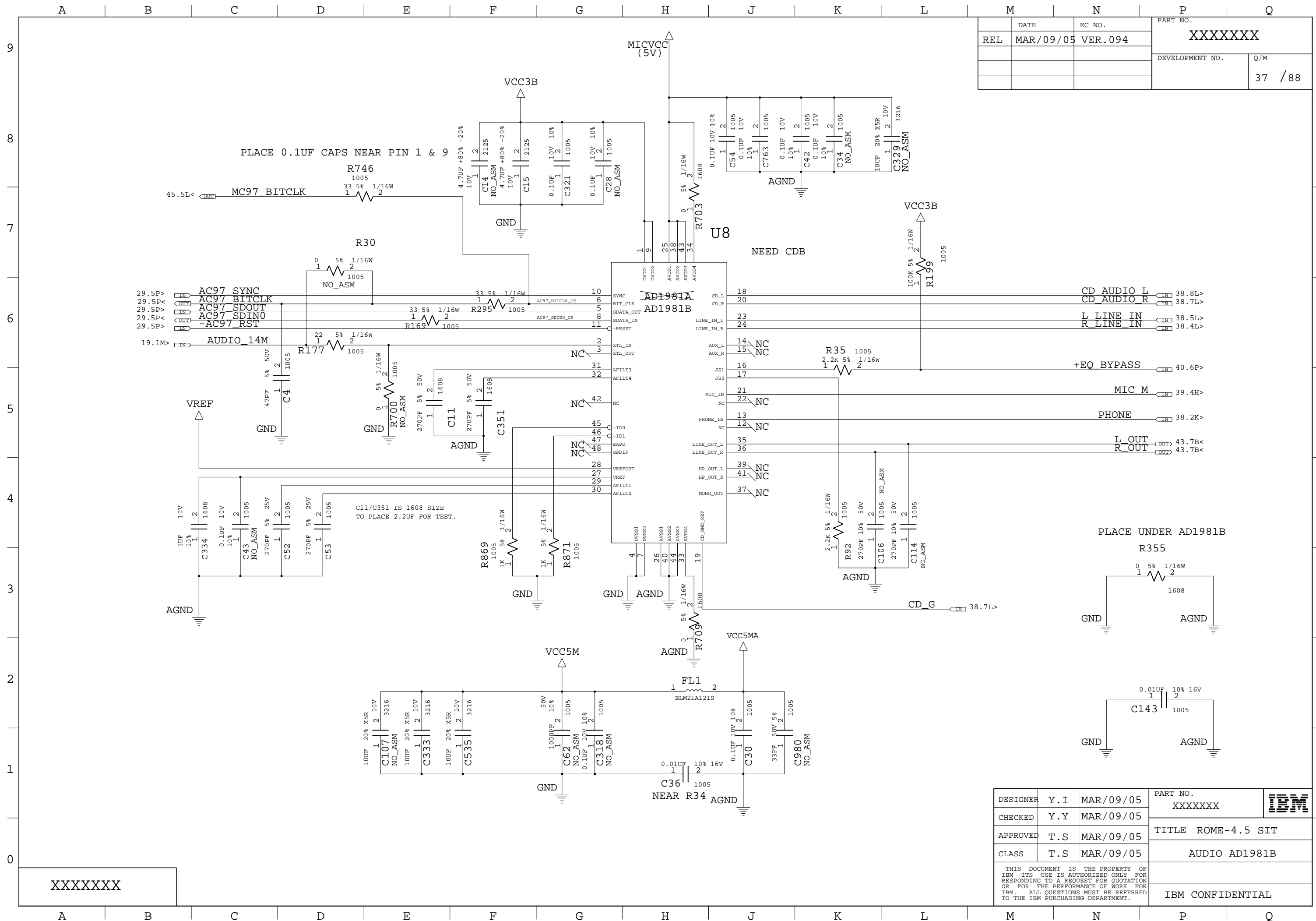
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APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05		BAY I/F CONN	
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XXXXXXXX



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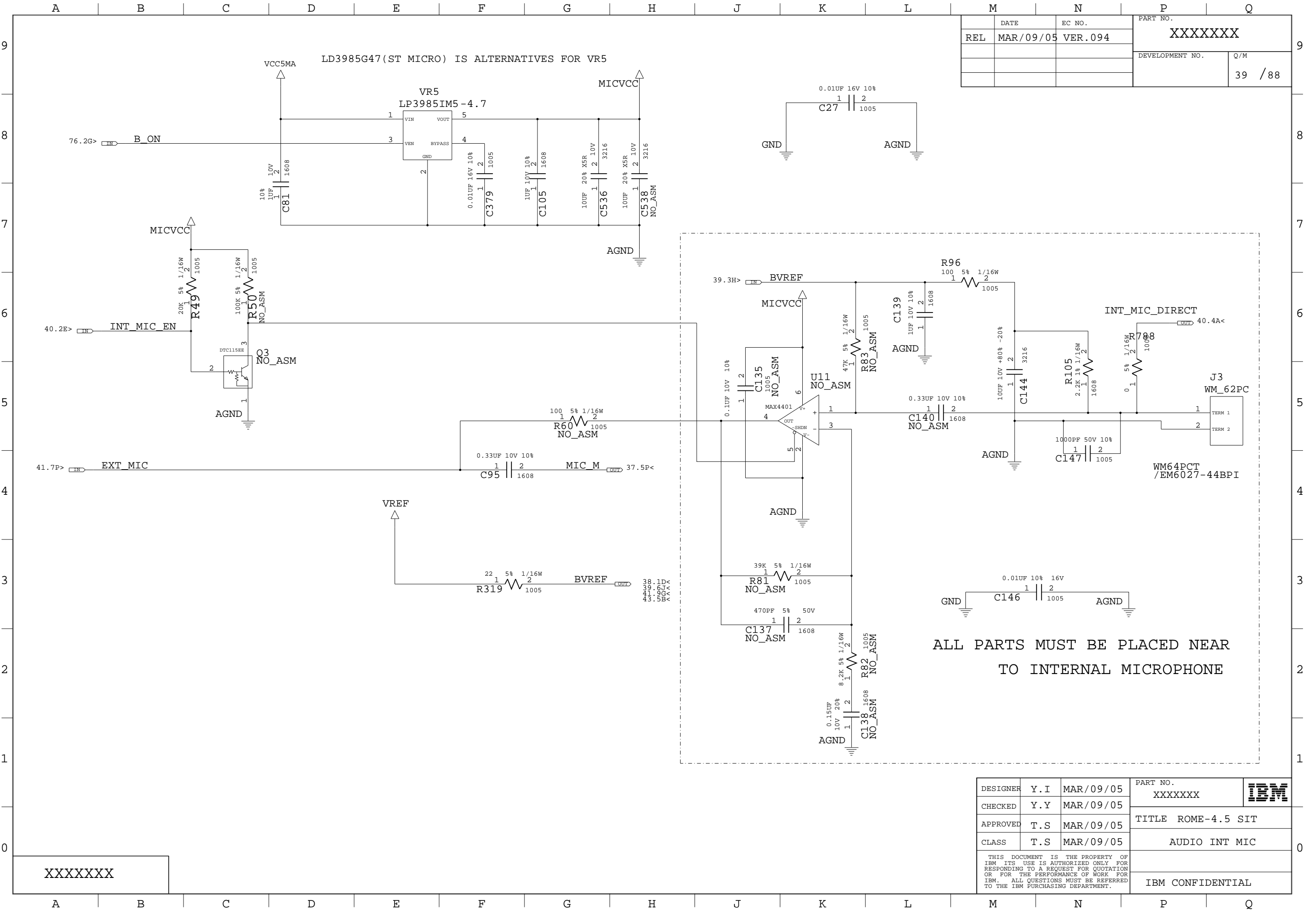




DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		37 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	AUDIO AD1981B		
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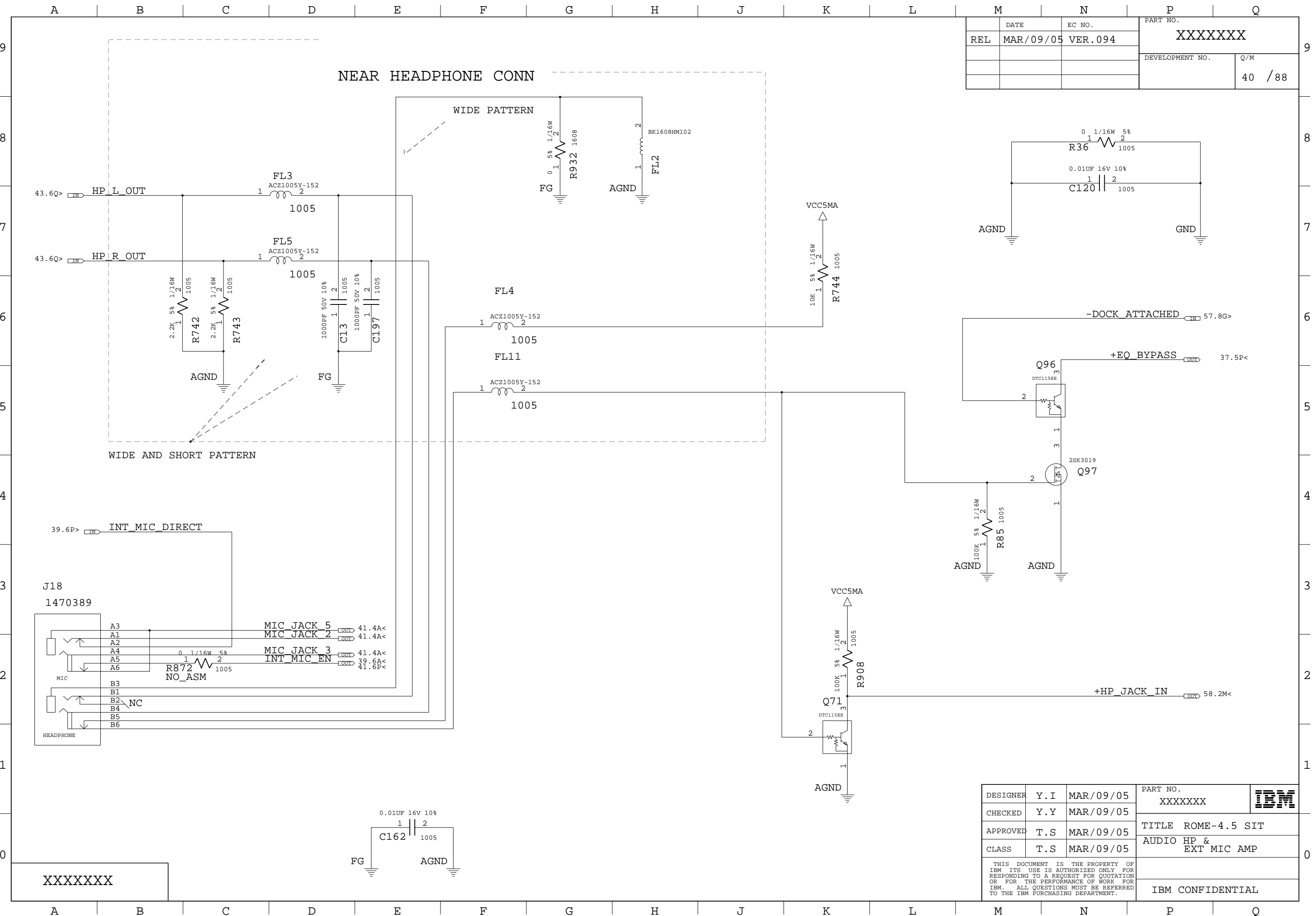
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DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXX
DEVELOPMENT NO.		Q/M
39 / 88		

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	AUDIO INT MIC		
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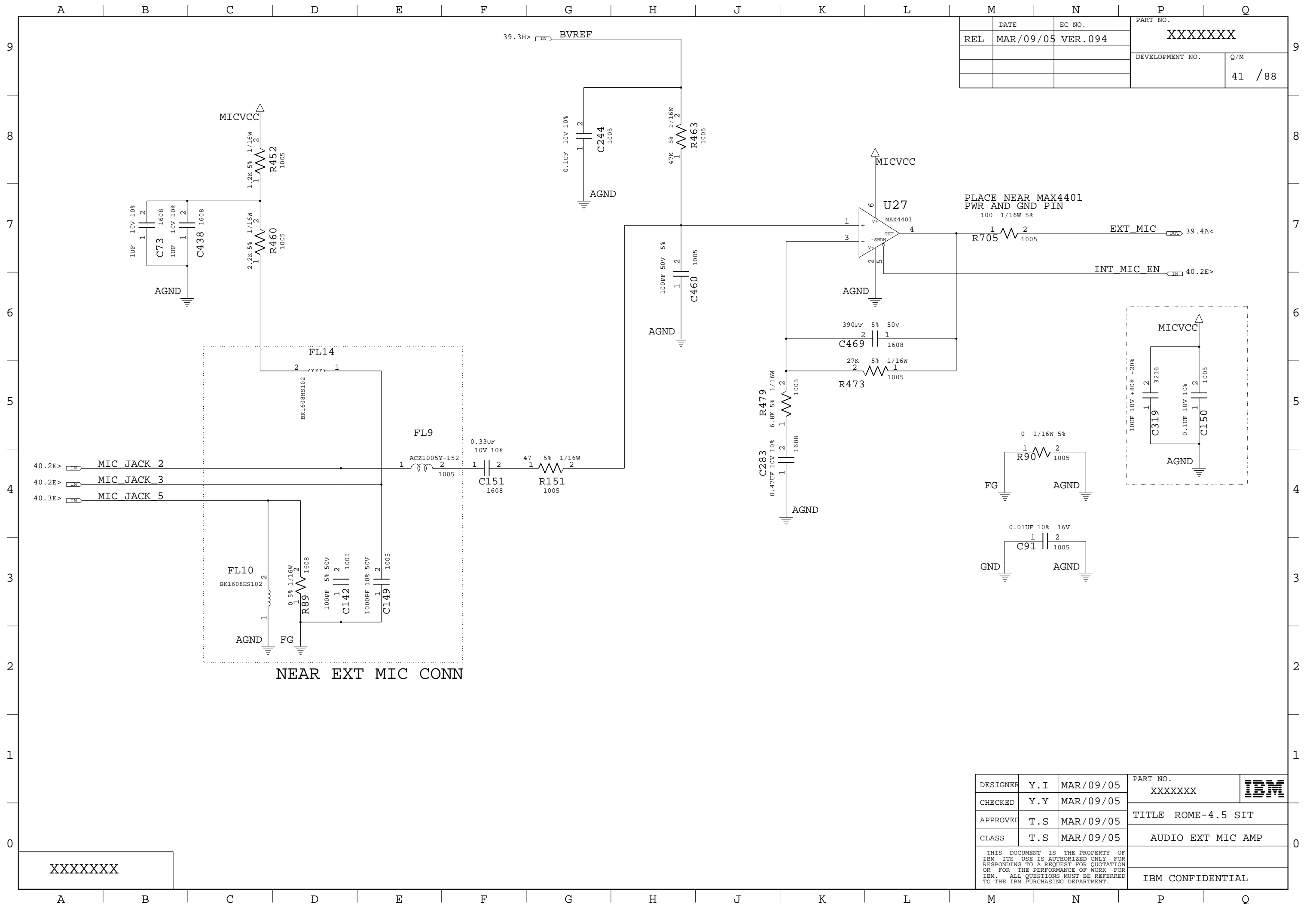
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DATE	EC NO.	PART NO.	
REL MAR/09/05	VER.094	XXXXXXXX	
		DEVELOPMENT NO.	Q/M
			40 / 88

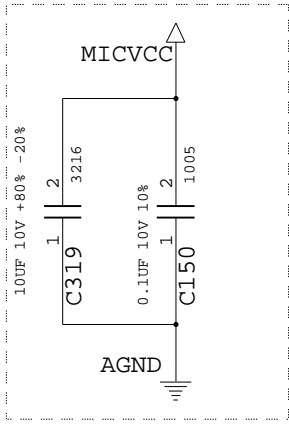
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DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	AUDIO HP & EXT MIC AMP		
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REL	DATE MAR/09/05	EC NO. VER.094	PART NO. XXXXXXXX
			DEVELOPMENT NO. Q/M 41 /88

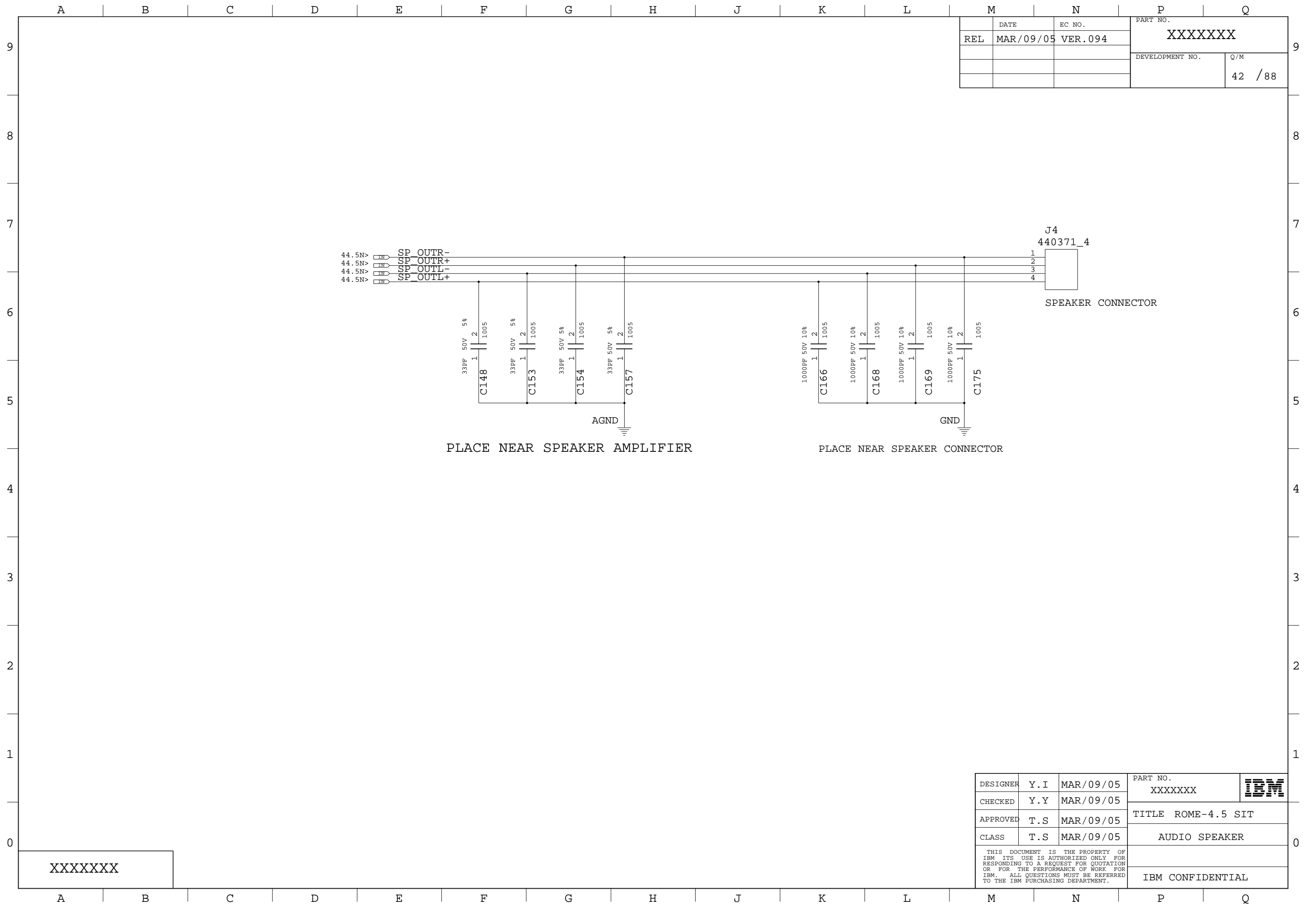
PLACE NEAR MAX4401
PWR AND GND PIN
100 1/16W 5%



NEAR EXT MIC CONN

XXXXXXXX

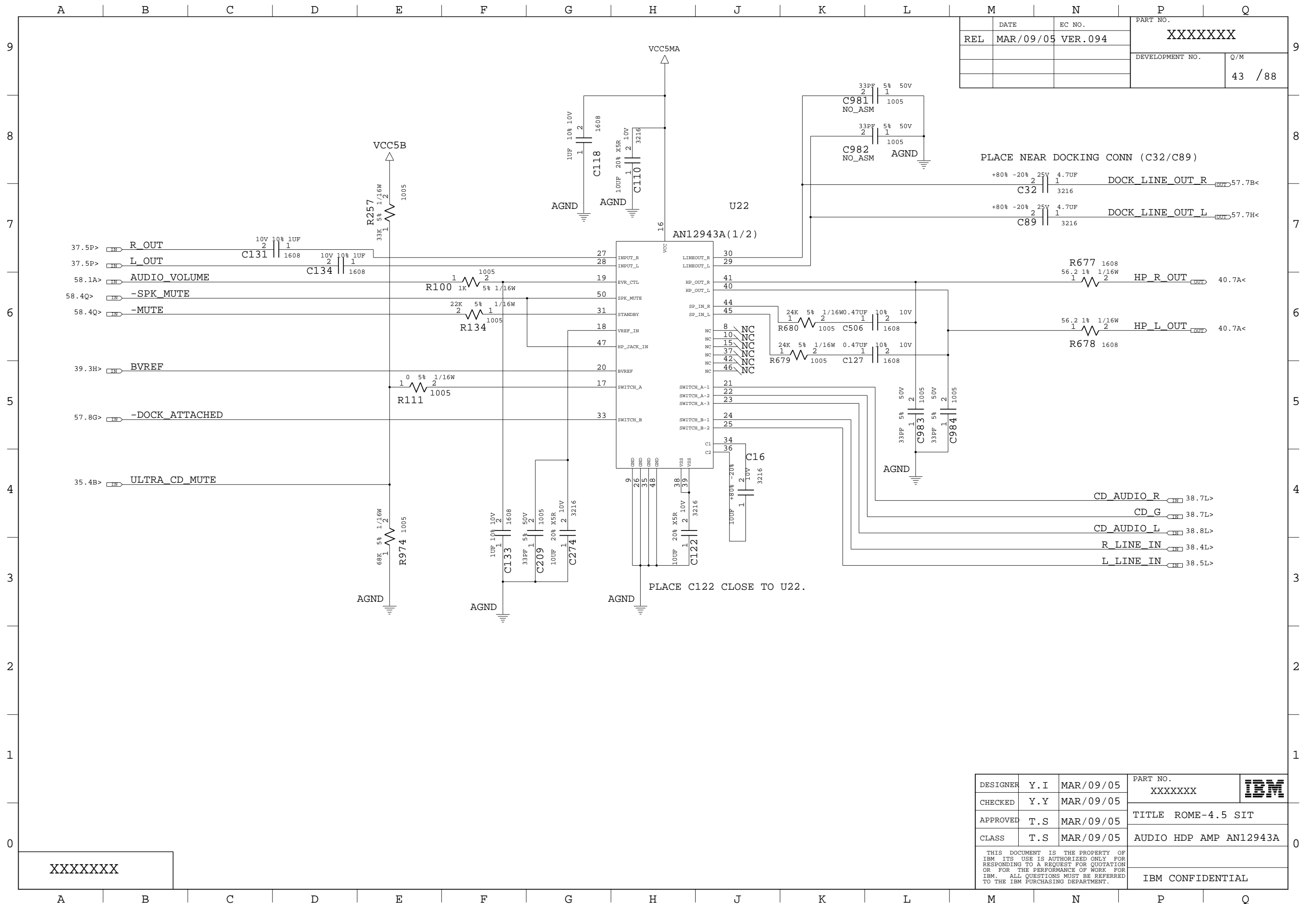
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CHECKED	Y.Y	MAR/09/05		
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT	
CLASS	T.S	MAR/09/05	AUDIO EXT MIC AMP	
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	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				42 / 88

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	AUDIO SPEAKER		
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DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		43 / 88

PLACE NEAR DOCKING CONN (C32/C89)

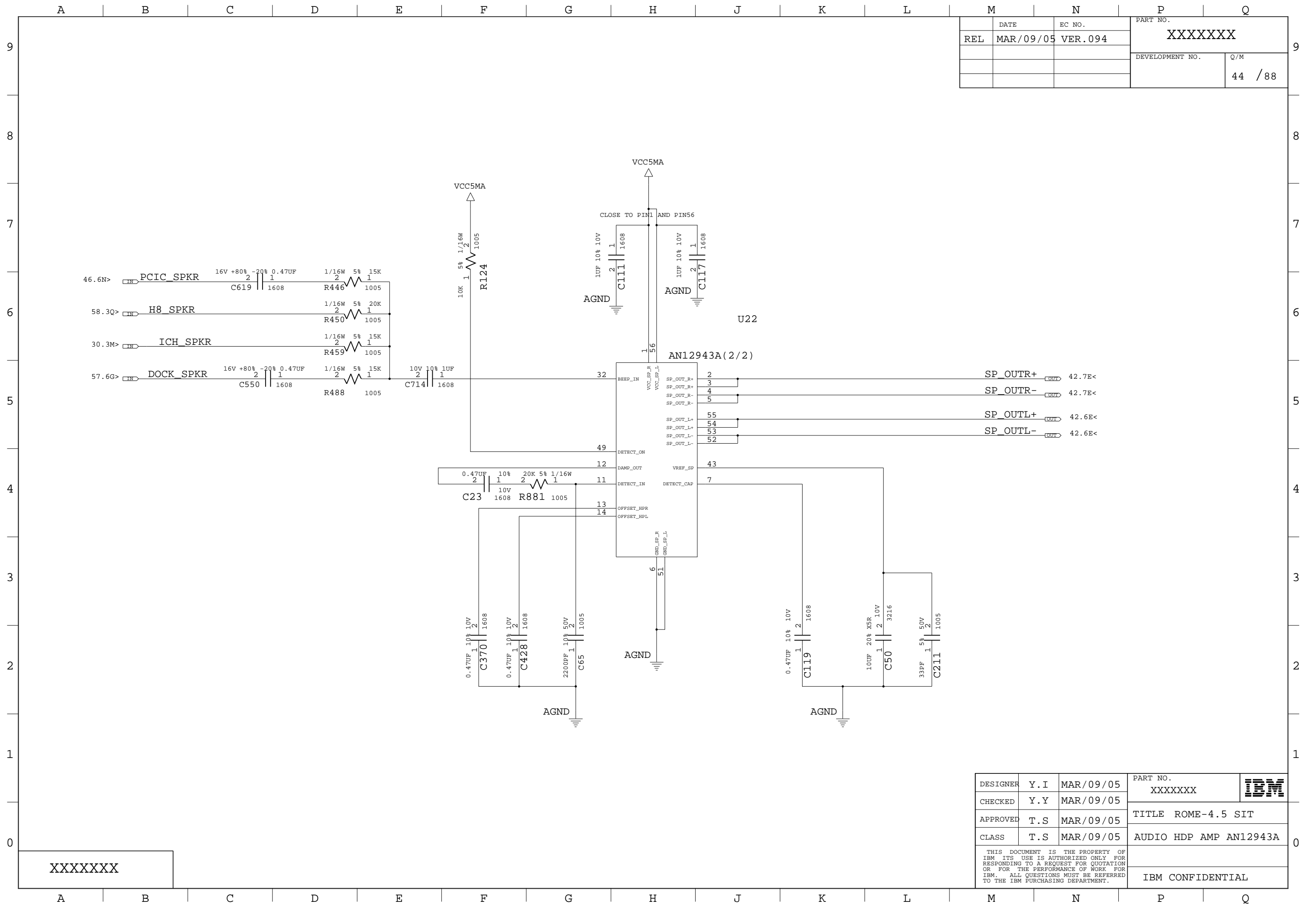
+80% -20% 25V 4.7UF DOCK LINE OUT R (OUT) 57.7B<

+80% -20% 25V 4.7UF DOCK LINE OUT L (OUT) 57.7H<

PLACE C122 CLOSE TO U22.

XXXXXXXX

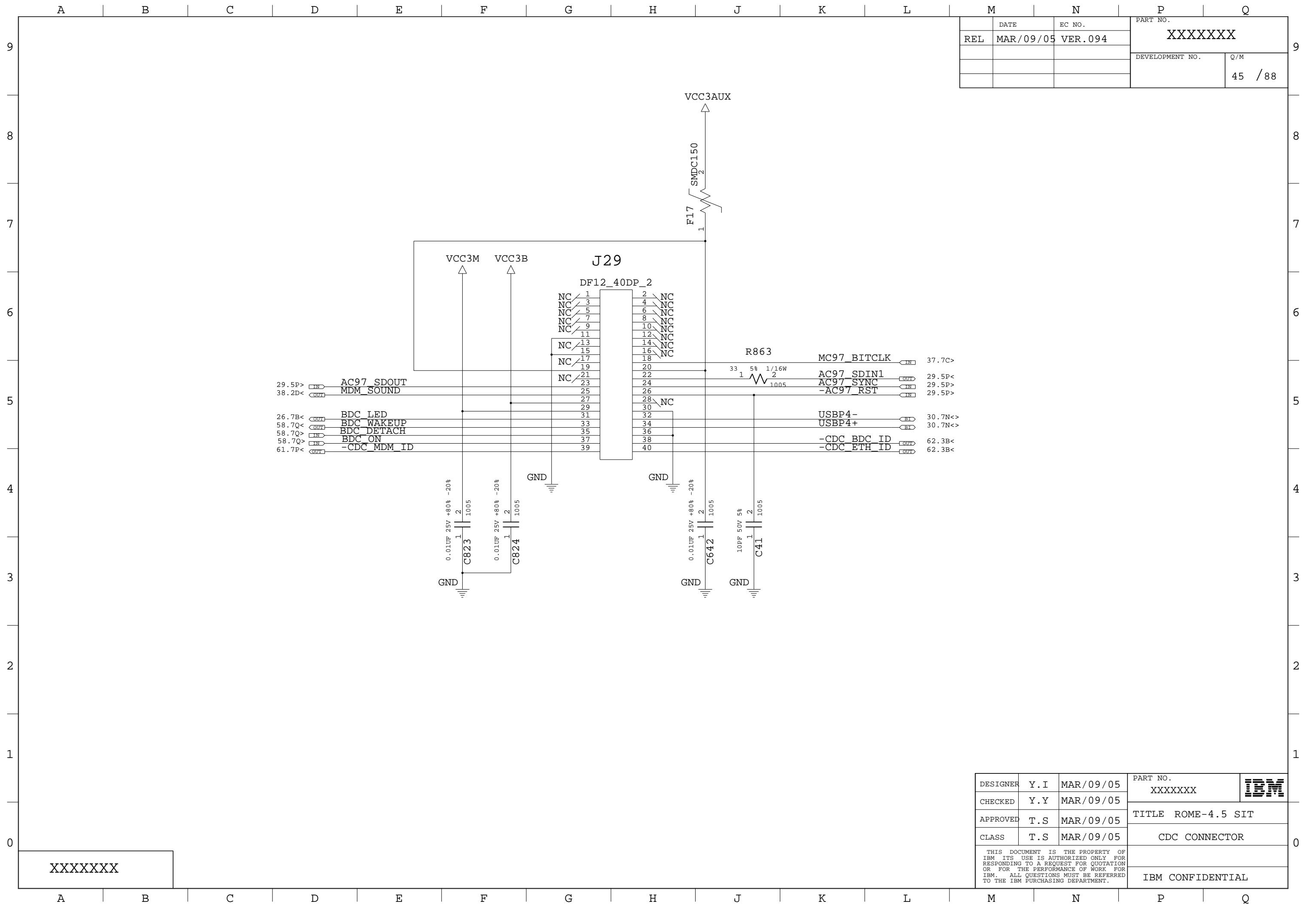
DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	AUDIO HDP AMP AN12943A		
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REL	DATE MAR/09/05	EC NO. VER.094	PART NO. XXXXXXXX
			DEVELOPMENT NO. Q/M 44 / 88

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO. XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05	TITLE ROME-4.5 SIT	
APPROVED	T. S	MAR/09/05	CLASS T. S	
			AUDIO HDP AMP AN12943A	
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REL	DATE MAR/09/05	EC NO. VER.094	PART NO. XXXXXXXX
			DEVELOPMENT NO. Q/M 45 / 88

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO. XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05	TITLE ROME-4.5 SIT	
APPROVED	T. S	MAR/09/05	CLASS CDC CONNECTOR	
CLASS	T. S	MAR/09/05	THIS DOCUMENT IS THE PROPERTY OF IBM. ITS USE IS AUTHORIZED ONLY FOR RESPONDING TO A REQUEST FOR QUOTATION OR FOR THE PERFORMANCE OF WORK FOR IBM. ALL QUESTIONS MUST BE REFERRED TO THE IBM PURCHASING DEPARTMENT.	
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REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			46 / 88

56.9A<> 55.8B<> 29.8C<> AD<31..0>

TABLE 1394 1/1
N-1394 Y-1394

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FL6	NO-ASM	ASM
C943	NO-ASM	ASM
C945	NO-ASM	ASM
R399	NO-ASM	ASM
C942	NO-ASM	ASM
R944	NO-ASM	ASM
C256	NO-ASM	ASM
R946	NO-ASM	ASM
R947	NO-ASM	ASM
R949	NO-ASM	ASM
R950	NO-ASM	ASM
C949	NO-ASM	ASM
R948	NO-ASM	ASM
C946	NO-ASM	ASM
C951	NO-ASM	ASM
J20	NO-ASM	ASM
C944	NO-ASM	ASM
R945	NO-ASM	ASM
Y7	NO-ASM	ASM
C947	NO-ASM	ASM
C948	NO-ASM	ASM

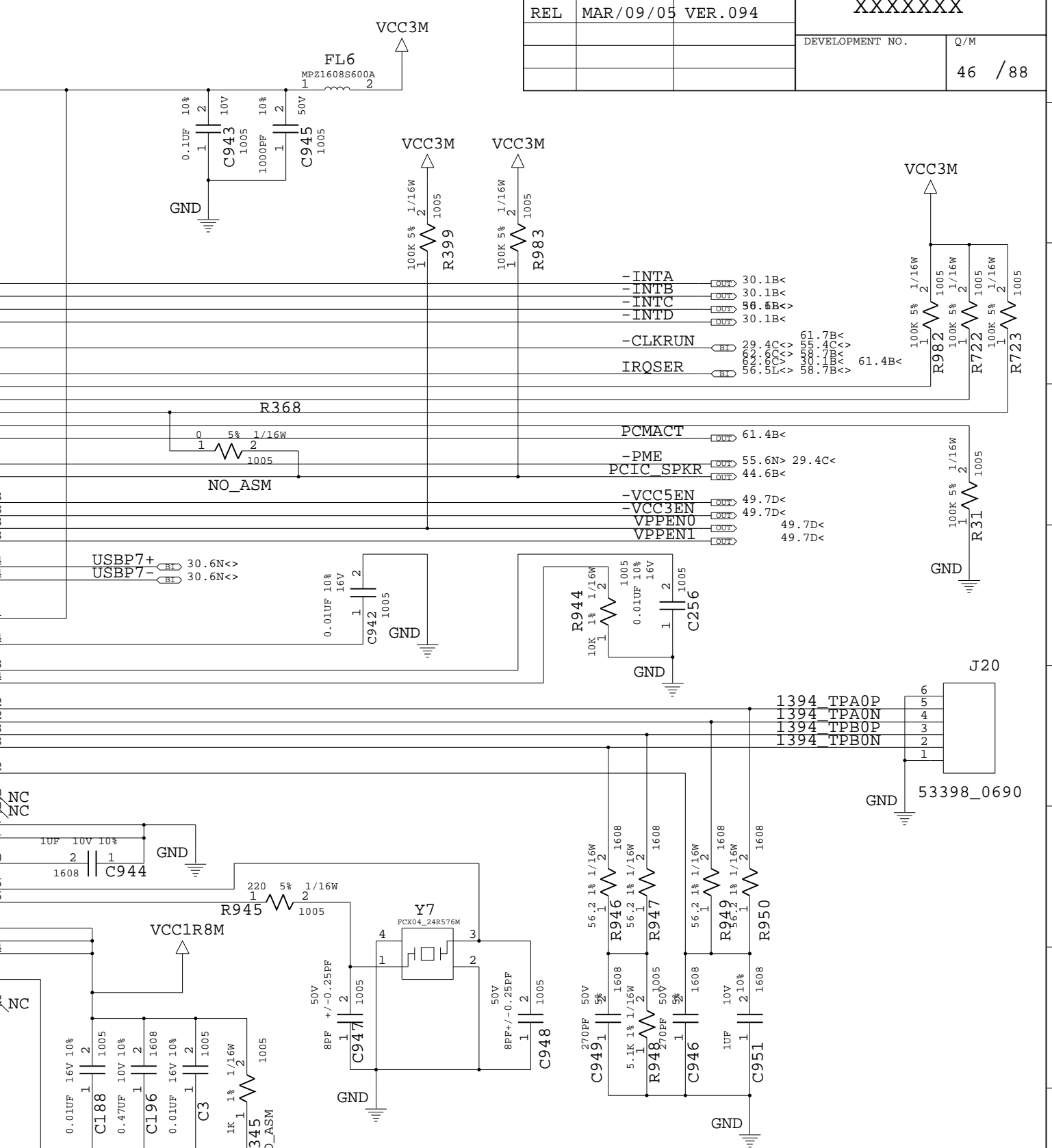
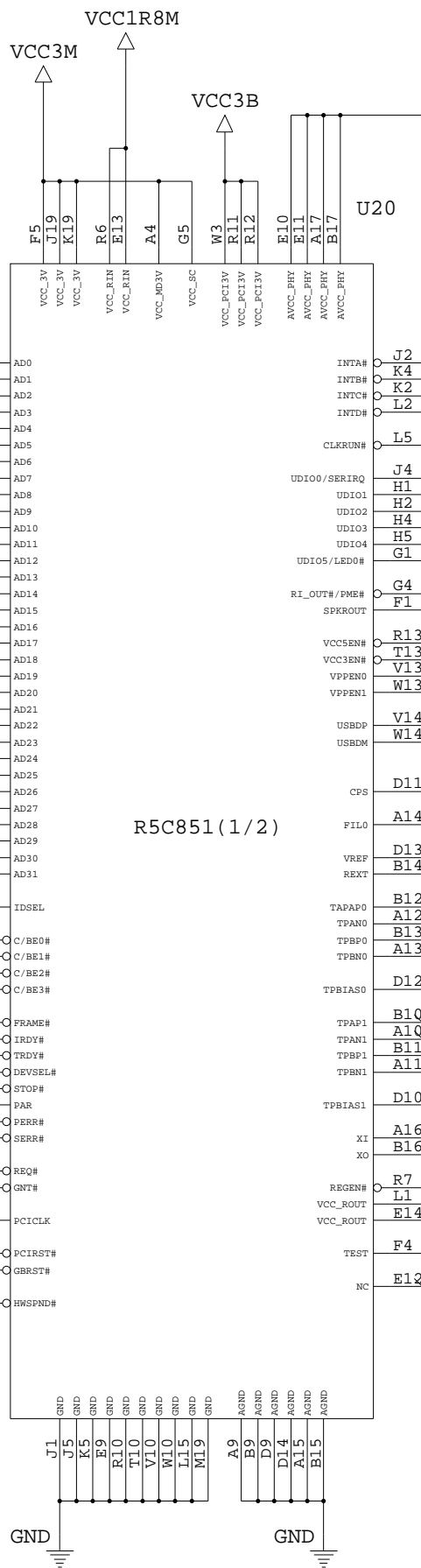
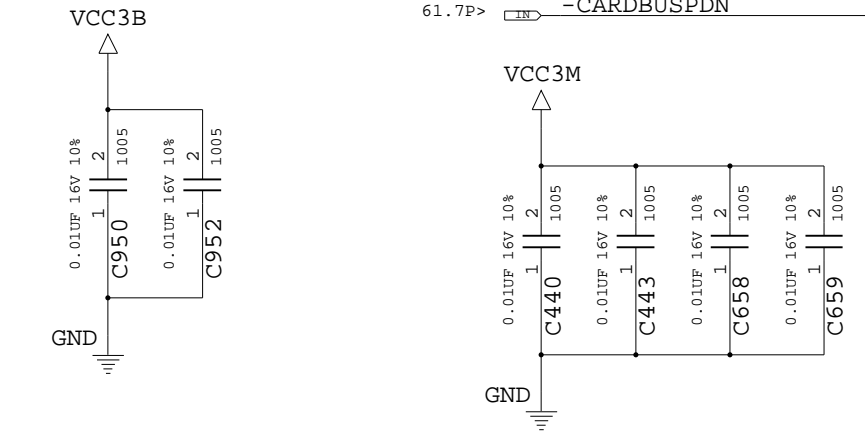
PAGE 62

LOGIC

56.8A<> 55.8B<> 29.9C<> C BE<3..0>

61.5B< 56.7L<> 55.4N<> 29.5C<> -FRAME V3 FRAME#
 61.5B< 56.7L<> 55.5C<> 29.5C<> -IRDY V4 IRDY#
 56.7L<> 55.4N<> 29.5C<> -TRDY W4 TRDY#
 56.6L<> 55.4N<> 29.5C<> -DEVSEL T5 DEVSEL#
 56.7L<> 55.4N<> 29.5C<> -STOP V5 STOP#
 56.6L<> 55.5N<> 29.5C<> -PAR V6 PAR
 56.5L<> 55.4C<> 29.5C<> -PERR W5 PERR#
 29.4C< 56.6L<> 55.4C<> -SERR T6 SERR#

29.4C< -REQ M4 REQ#
 29.3C< -GNT M5 GNT#
 19.2B> PCICLK CB 33M K1 PCICLK
 29.4C< -PCIRST L4 PCIRST#
 84.2K> 30.2M> MPWRG G2 GBRST#
 61.7P> -CARDBUSPDN F2 HWSPND#

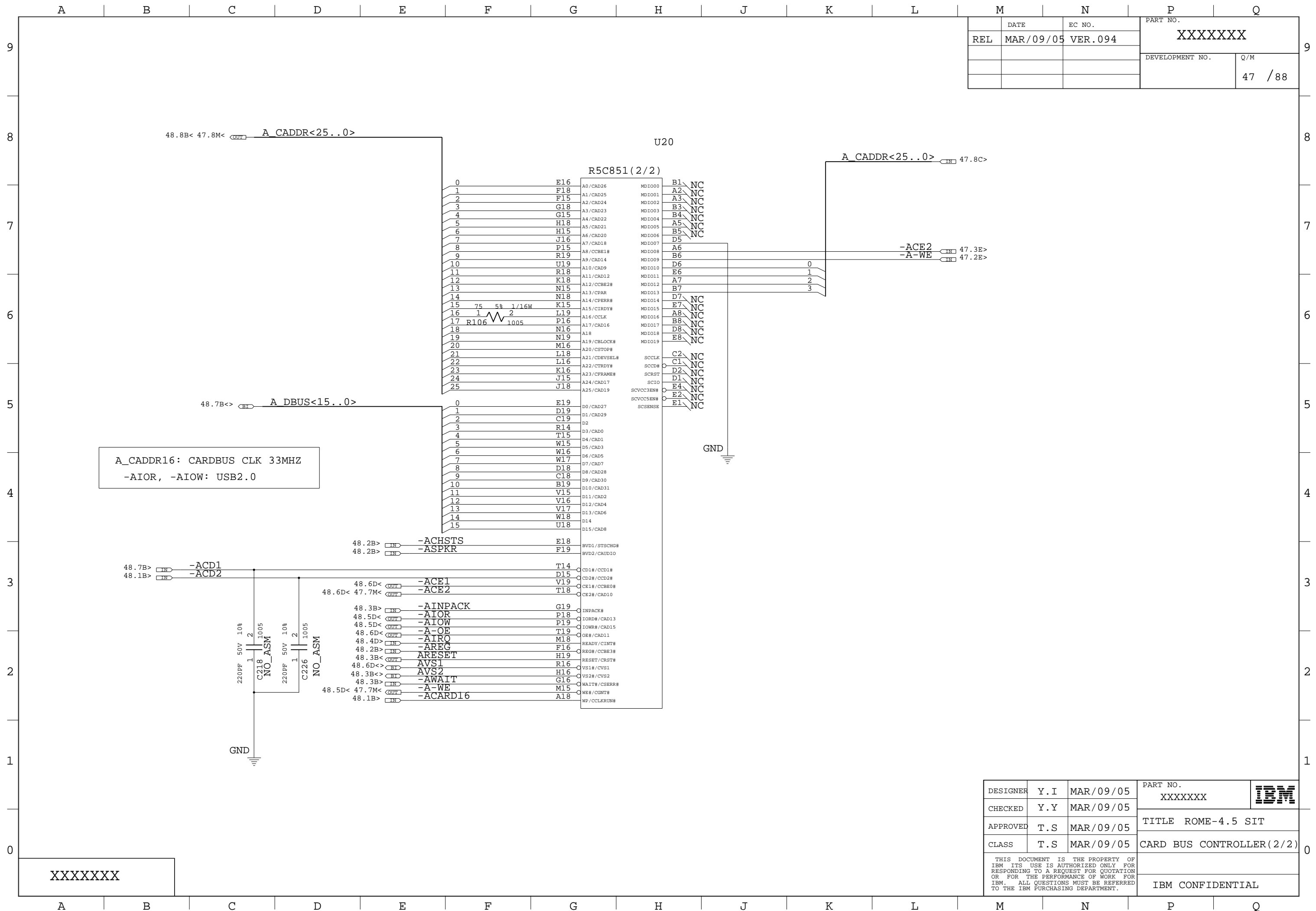


1394	TPA0P	6
1394	TPA0N	5
1394	TPB0P	4
1394	TPB0N	3
1394	TPB0N	2
1394	TPB0N	1

53398_0690

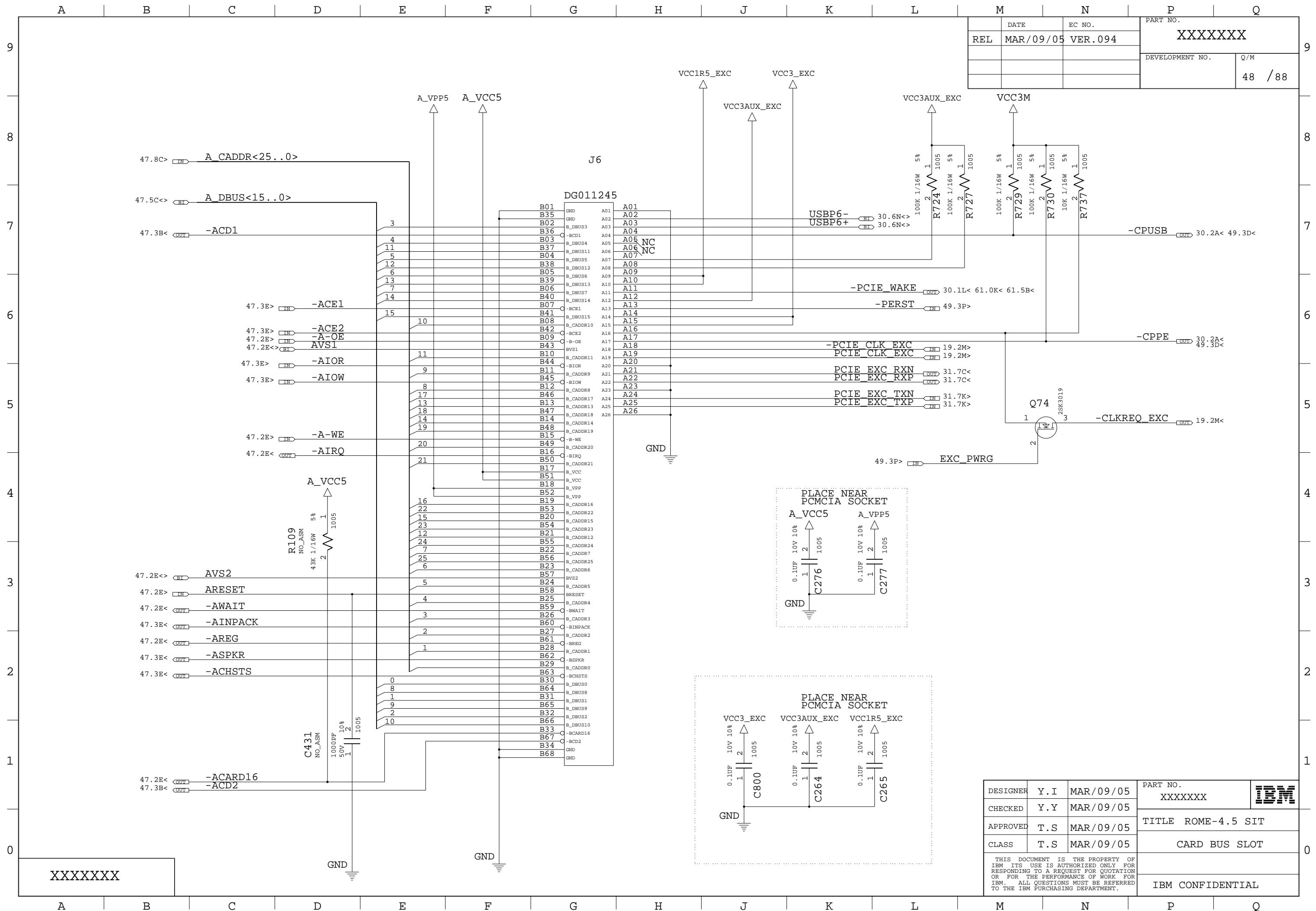
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APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	CARD BUS CONTROLLER(1/2)		
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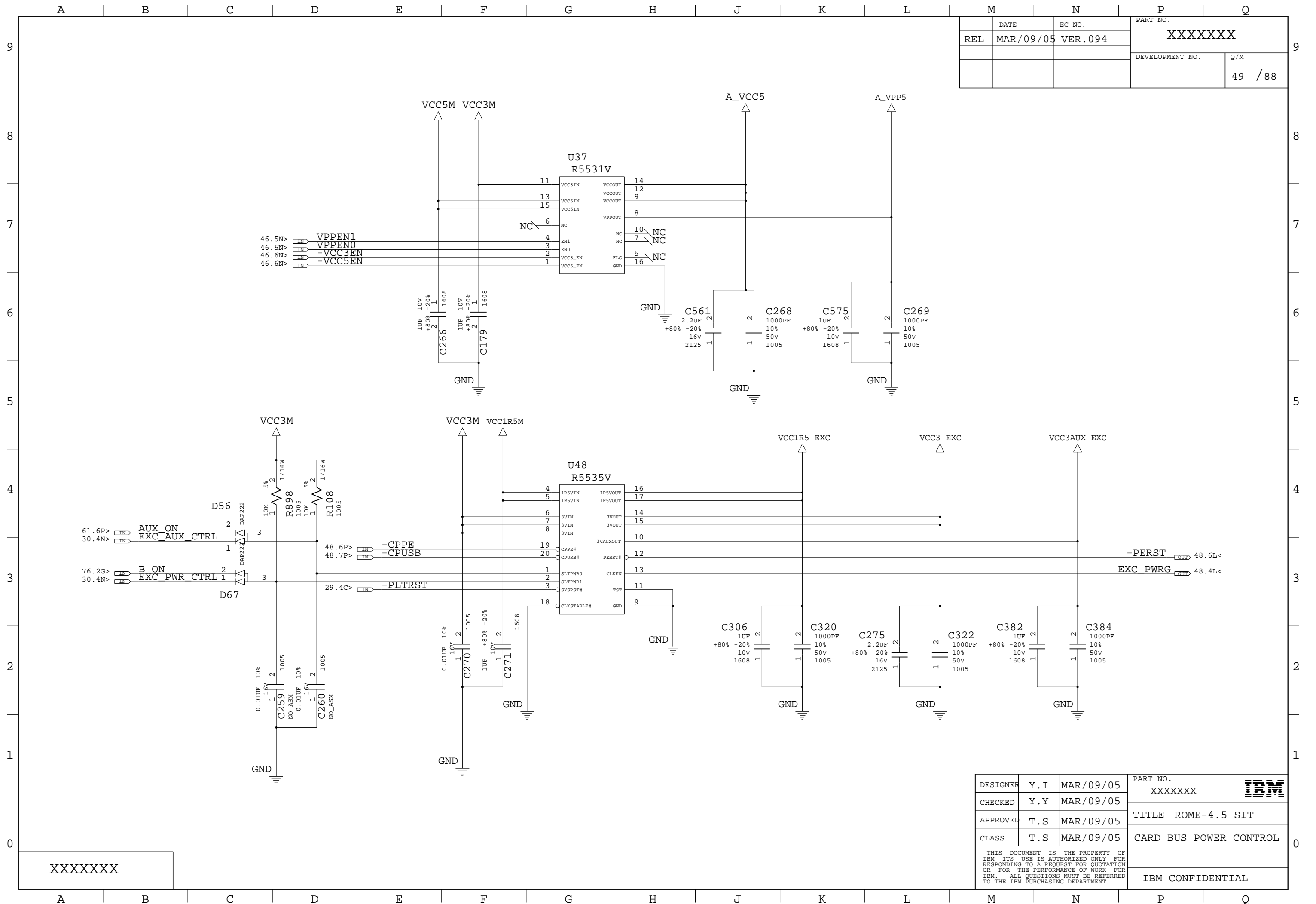
REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			47 / 88

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	CARD BUS CONTROLLER(2/2)		
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DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		48 / 88

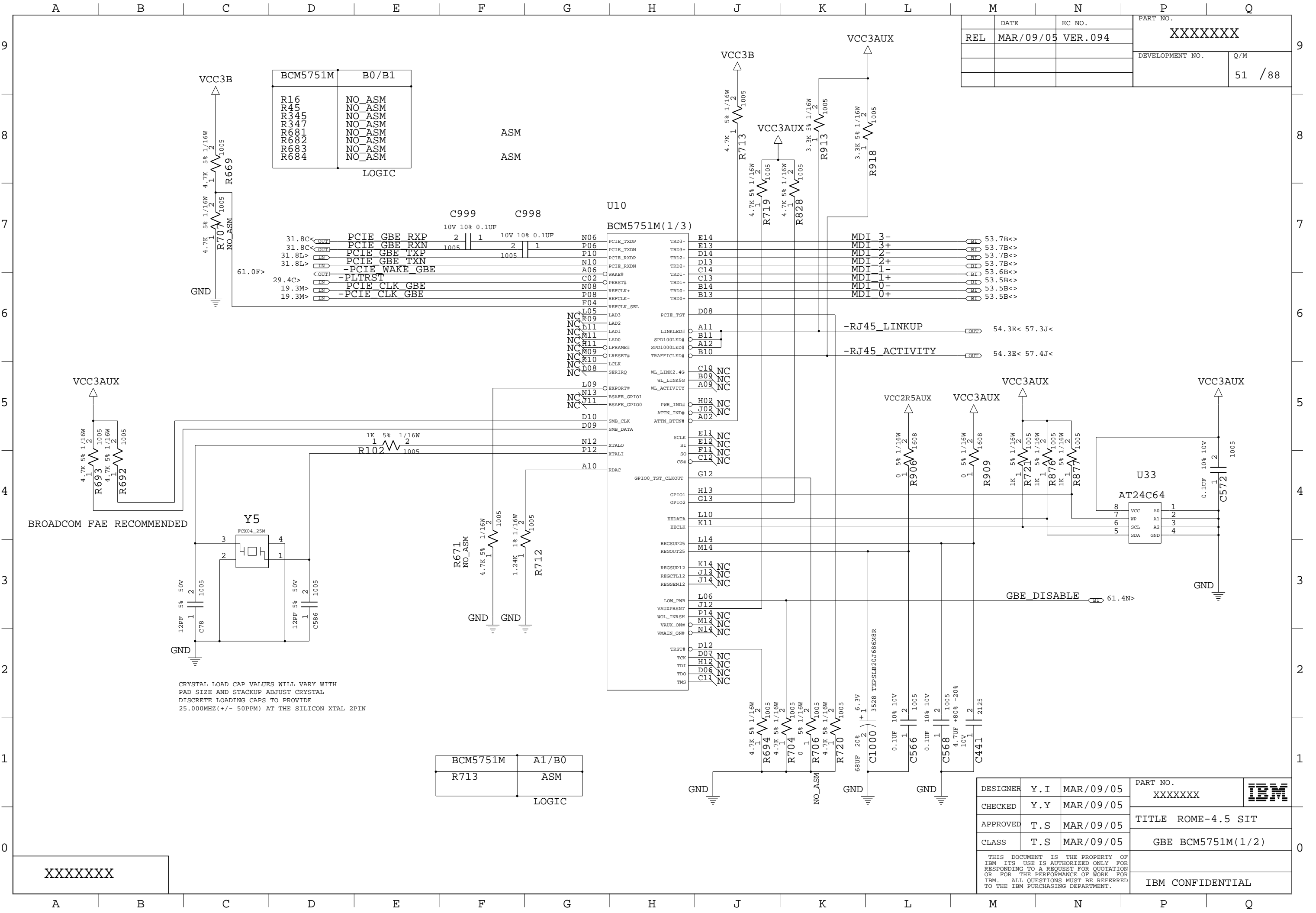
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APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	CARD BUS SLOT		
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	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				49 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	CARD BUS POWER CONTROL		
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REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			51 / 88

BCM5751M	B0/B1
R16	NO_ASM
R45	NO_ASM
R345	NO_ASM
R347	NO_ASM
R681	NO_ASM
R682	NO_ASM
R683	NO_ASM
R684	NO_ASM

ASM
ASM

LOGIC

C999	C998
10V 10% 0.1UF	10V 10% 0.1UF
2	1
1005	1005

U10	BCM5751M(1/3)
-----	---------------

31.8C<	PCIE_GBE_RXP	N06	PCIE_TXDP	TRD3-	E14	MDI_3-	BI	53.7B<>
31.8C<	PCIE_GBE_RXN	P06	PCIE_TXDN	TRD3+	E13	MDI_3+	BI	53.7B<>
31.8L>	PCIE_GBE_TXP	P10	PCIE_RXDP	TRD2-	D14	MDI_2-	BI	53.7B<>
31.8L>	PCIE_GBE_TXN	N10	PCIE_RXDN	TRD2+	D13	MDI_2+	BI	53.7B<>
	-PCIE_WAKE_GBE	A06	WAKE#	TRD1-	C14	MDI_1-	BI	53.6B<>
29.4C>	-PLTRST	C02	PERST#	TRD1+	C13	MDI_1+	BI	53.5B<>
19.3M>	PCIE_CLK_GBE	N08	REFCLK+	TRD0-	B14	MDI_0-	BI	53.5B<>
19.3M>	PCIE_CLK_GBE	P08	REFCLK-	TRD0+	B13	MDI_0+	BI	53.5B<>

BROADCOM FAE RECOMMENDED

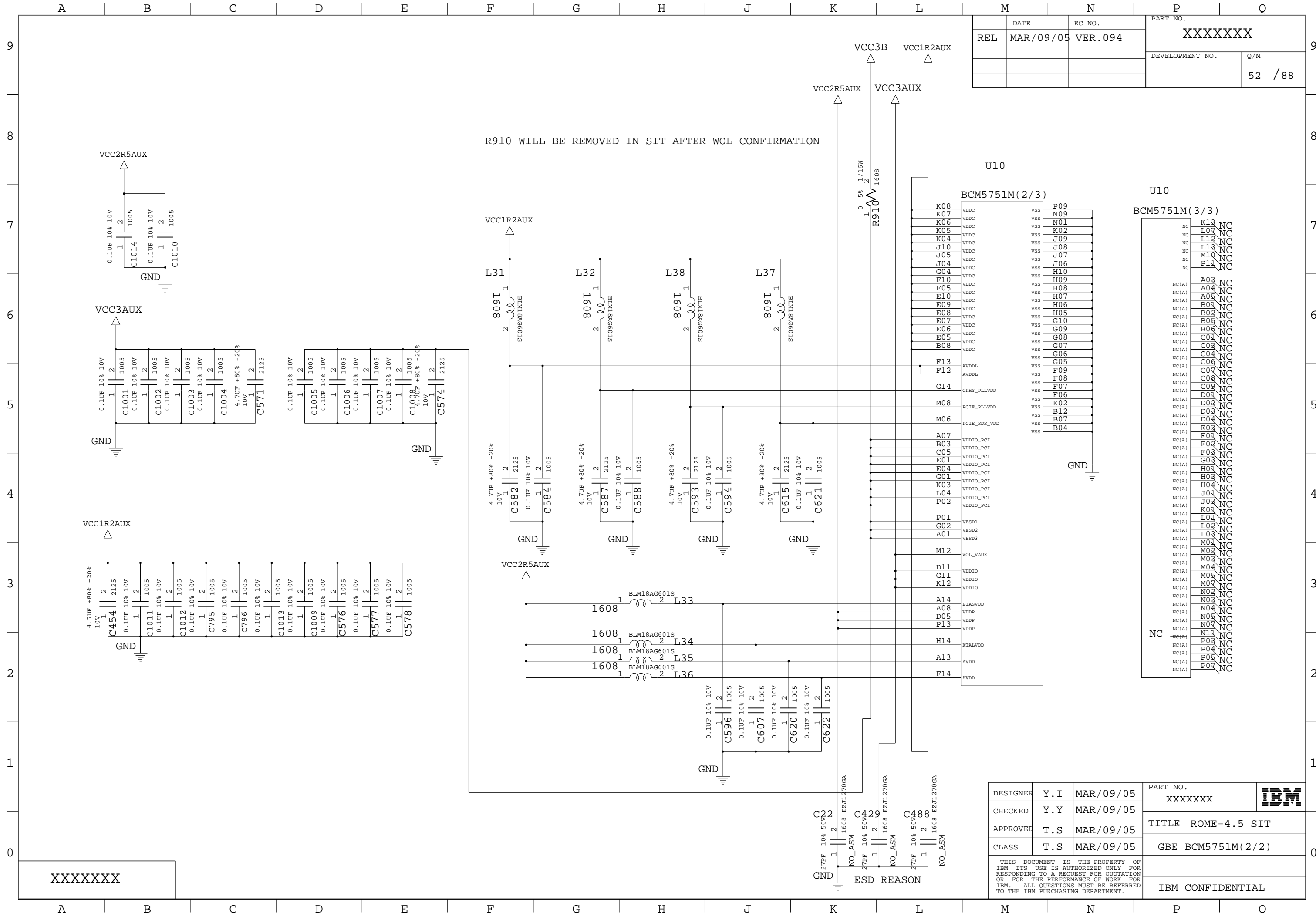
CRYSTAL LOAD CAP VALUES WILL VARY WITH
PAD SIZE AND STACKUP ADJUST CRYSTAL
DISCRETE LOADING CAPS TO PROVIDE
25.000MHZ(+/- 50PPM) AT THE SILICON XTAL 2PIN

BCM5751M	A1/B0
R713	ASM

LOGIC

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	GBE BCM5751M(1/2)		
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XXXXXXXX



DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		52 / 88

U10

BCM5751M(2/3)

K08	VDDC	P09	VSS
K07	VDDC	N09	VSS
K06	VDDC	N01	VSS
K05	VDDC	K02	VSS
K04	VDDC	J09	VSS
J10	VDDC	J08	VSS
J05	VDDC	J07	VSS
J04	VDDC	J06	VSS
G04	VDDC	H10	VSS
F10	VDDC	H09	VSS
F05	VDDC	H08	VSS
E10	VDDC	H07	VSS
E09	VDDC	H06	VSS
E08	VDDC	H05	VSS
E07	VDDC	G10	VSS
E06	VDDC	G09	VSS
E05	VDDC	G08	VSS
B08	VDDC	G07	VSS
F13	AVDDL	G06	VSS
F12	AVDDL	G05	VSS
G14	PHY_PLLVDD	F09	VSS
M08	PCIR_PLLVDD	F08	VSS
M06	PCIR_SDS_VDD	F07	VSS
A07	VDDIO_PCI	F06	VSS
B03	VDDIO_PCI	E02	VSS
C05	VDDIO_PCI	D01	VSS
E01	VDDIO_PCI	D02	VSS
E04	VDDIO_PCI	D03	VSS
G01	VDDIO_PCI	D04	VSS
K03	VDDIO_PCI	B07	VSS
L04	VDDIO_PCI	B07	VSS
P02	VDDIO_PCI	B04	VSS
P01	VESD1		
G02	VESD2		
A01	VESD3		
M12	WOL_VAUX		
D11	VDDIO		
G11	VDDIO		
K12	VDDIO		
A14	BIASVDD		
A08	VDDP		
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H14	XTALVDD		
A13	AVDD		
F14	AVDD		

U10

BCM5751M(3/3)

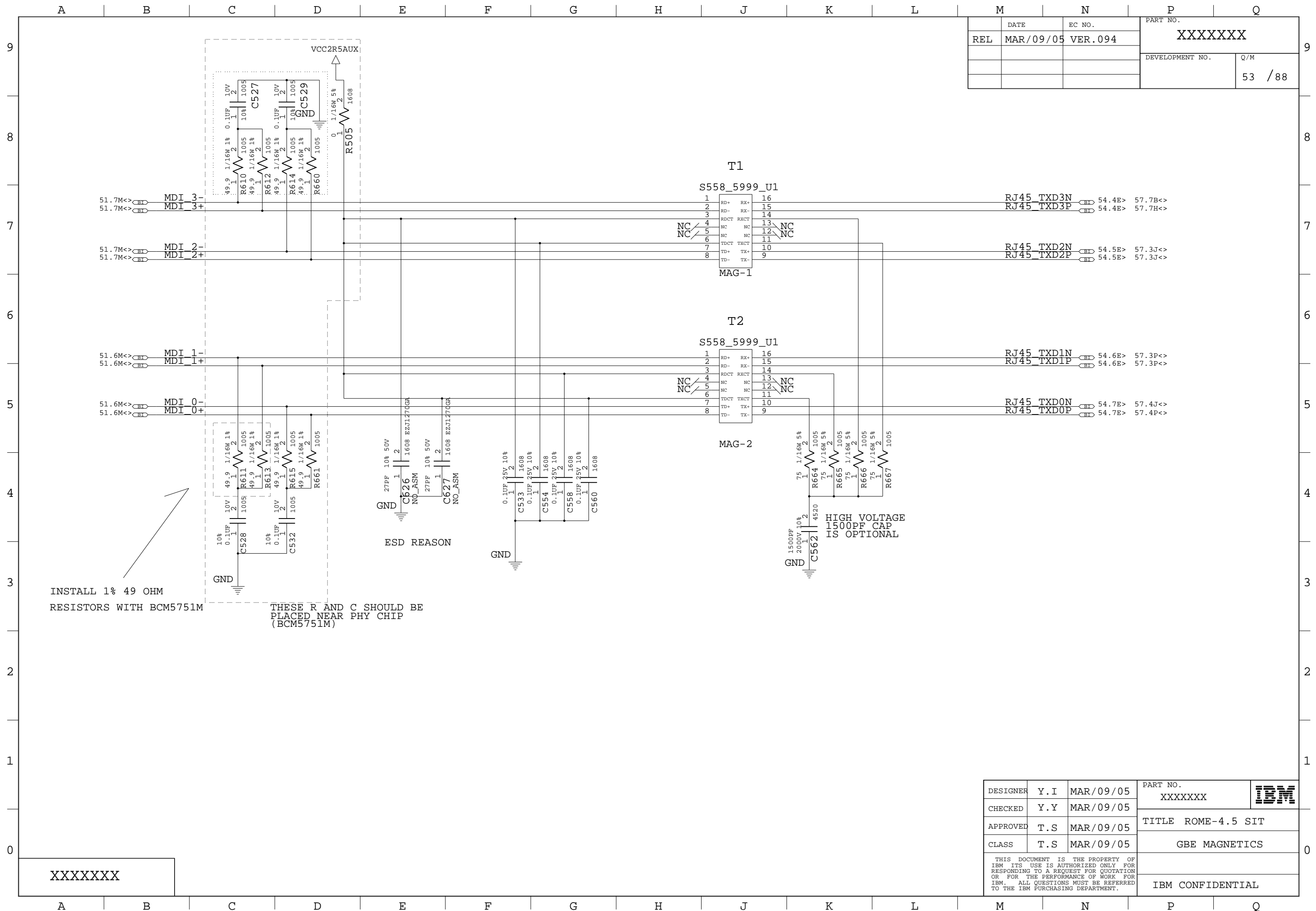
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L12	NC
L13	NC
M10	NC
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A04	NC(A)
A05	NC(A)
B01	NC(A)
B02	NC(A)
B05	NC(A)
B06	NC(A)
C01	NC(A)
C03	NC(A)
C04	NC(A)
C06	NC(A)
C07	NC(A)
F08	NC(A)
F09	NC(A)
F08	NC(A)
F07	NC(A)
C08	NC(A)
C09	NC(A)
D01	NC(A)
D02	NC(A)
D03	NC(A)
D04	NC(A)
B07	NC(A)
B04	NC(A)
E03	NC(A)
F01	NC(A)
F02	NC(A)
F03	NC(A)
G03	NC(A)
H01	NC(A)
H03	NC(A)
H04	NC(A)
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J03	NC(A)
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P04	NC(A)
P05	NC(A)
P07	NC(A)
NC	NC(A)

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	
CHECKED	Y. Y	MAR/09/05	TITLE ROME-4.5 SIT		
APPROVED	T. S	MAR/09/05	GBE BCM5751M(2/2)		
CLASS	T. S	MAR/09/05	IBM CONFIDENTIAL		

XXXXXXXX

ESD REASON

R910 WILL BE REMOVED IN SIT AFTER WOL CONFIRMATION



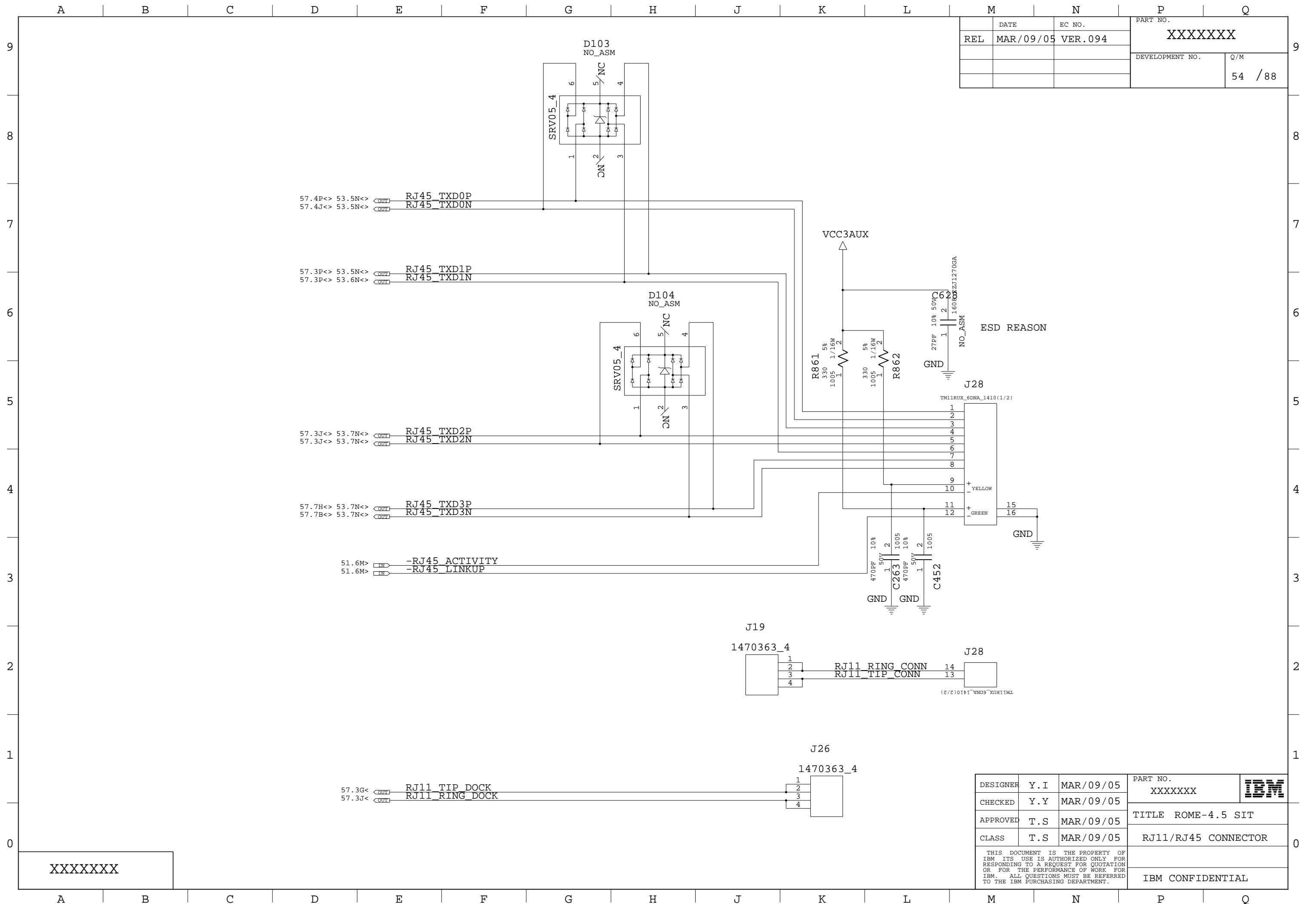
DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXX
DEVELOPMENT NO.		Q/M
53		/88

INSTALL 1% 49 OHM
RESISTORS WITH BCM5751M

THESE R AND C SHOULD BE
PLACED NEAR PHY CHIP
(BCM5751M)

HIGH VOLTAGE
1500PF CAP
IS OPTIONAL

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	GBE MAGNETICS		
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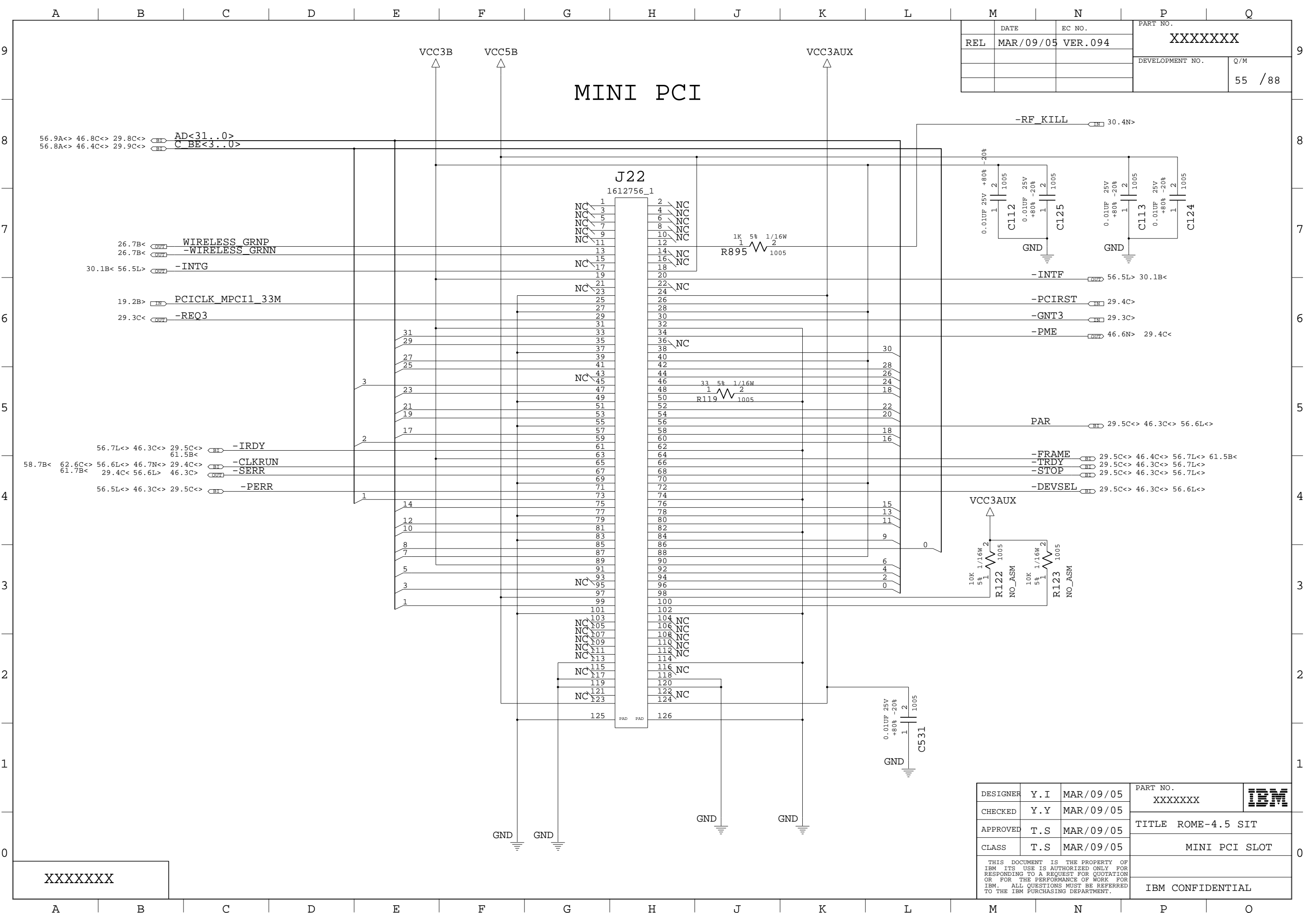


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REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		54 /88

ESD REASON

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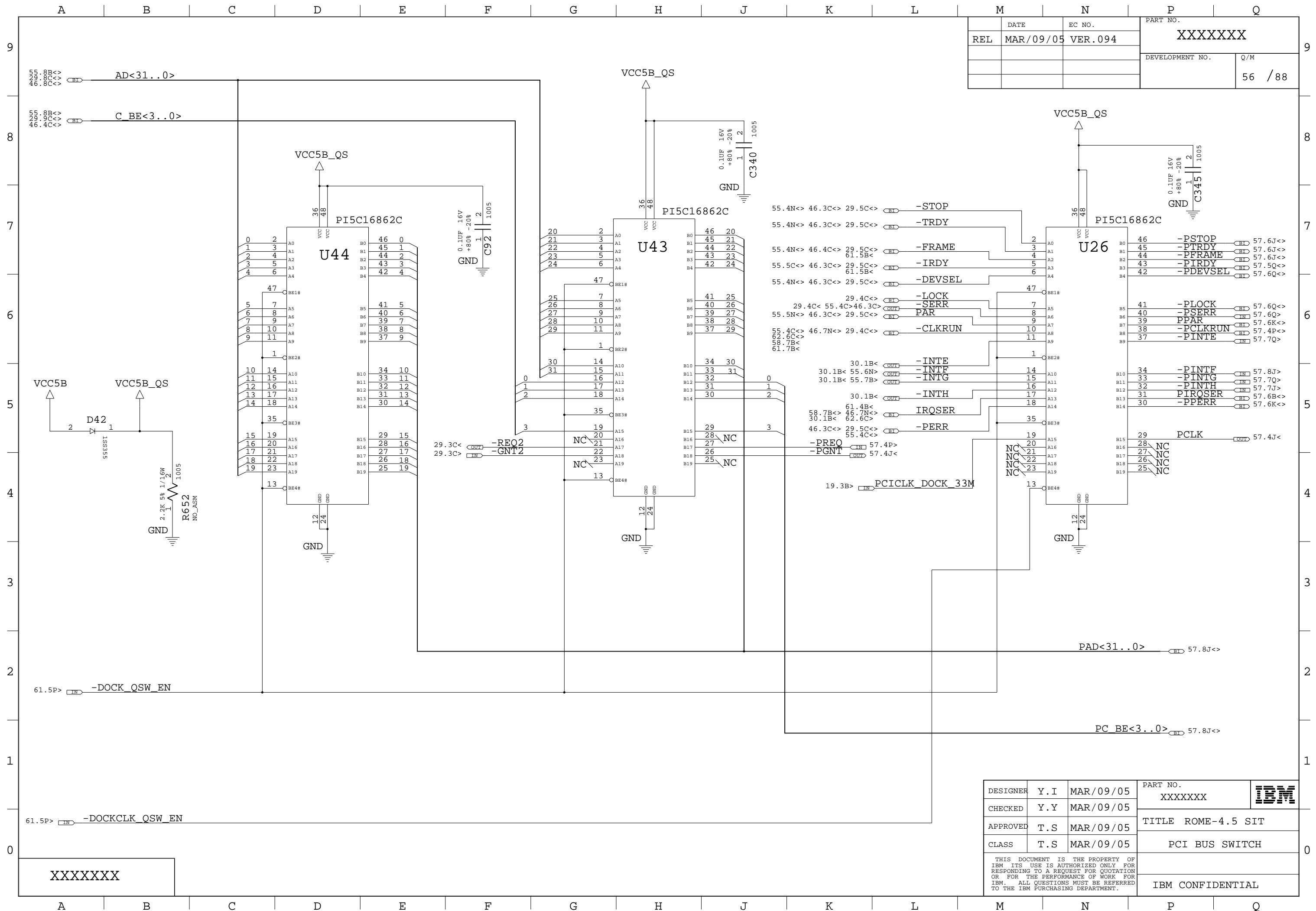
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CLASS	T. S	MAR/09/05	RJ11/RJ45 CONNECTOR		
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DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
55 / 88		

XXXXXXXX

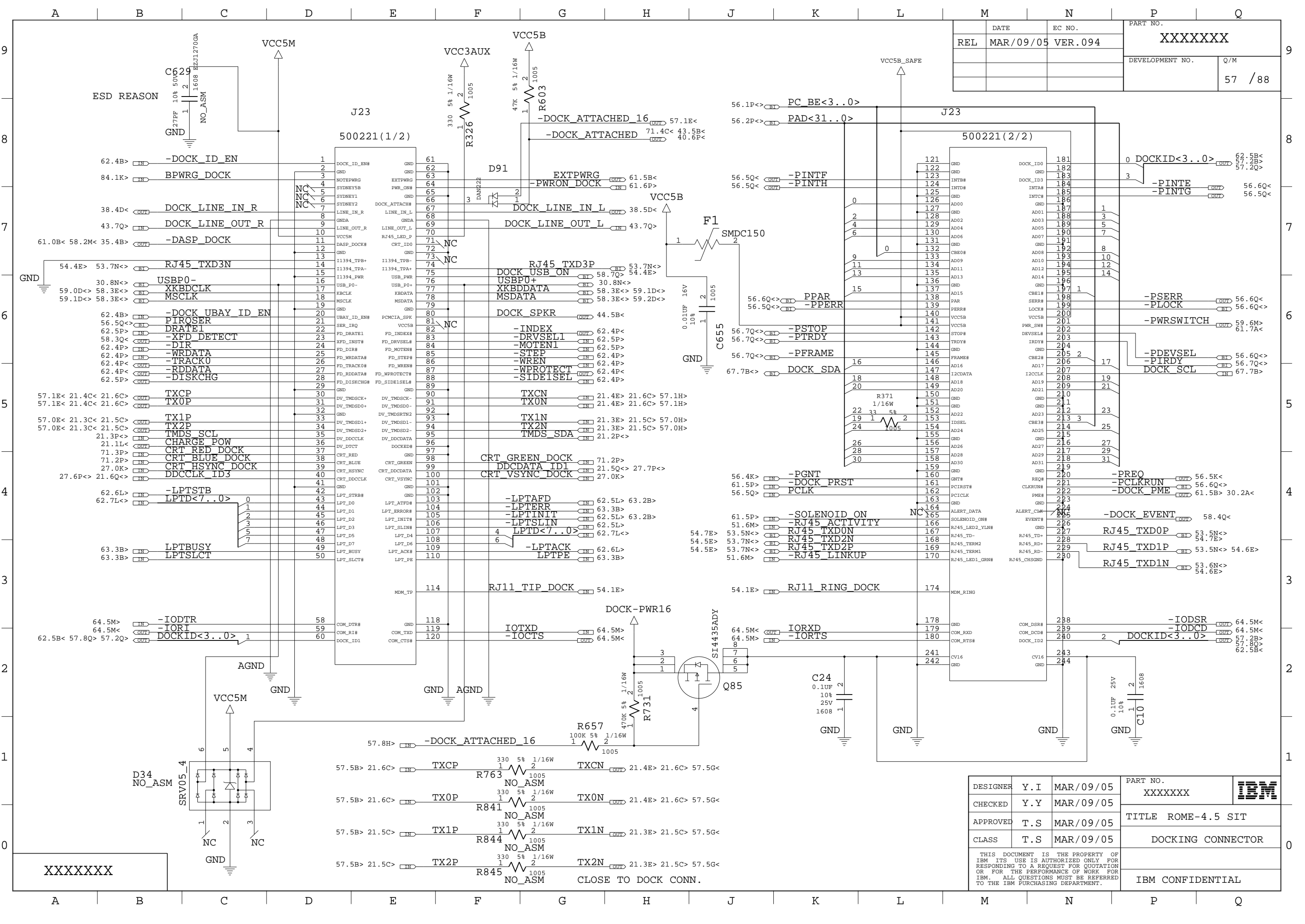
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CLASS	T. S	MAR/09/05	MINI PCI SLOT		
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DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		56 / 88

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y.Y	MAR/09/05			
APPROVED	T.S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T.S	MAR/09/05	PCI BUS SWITCH		
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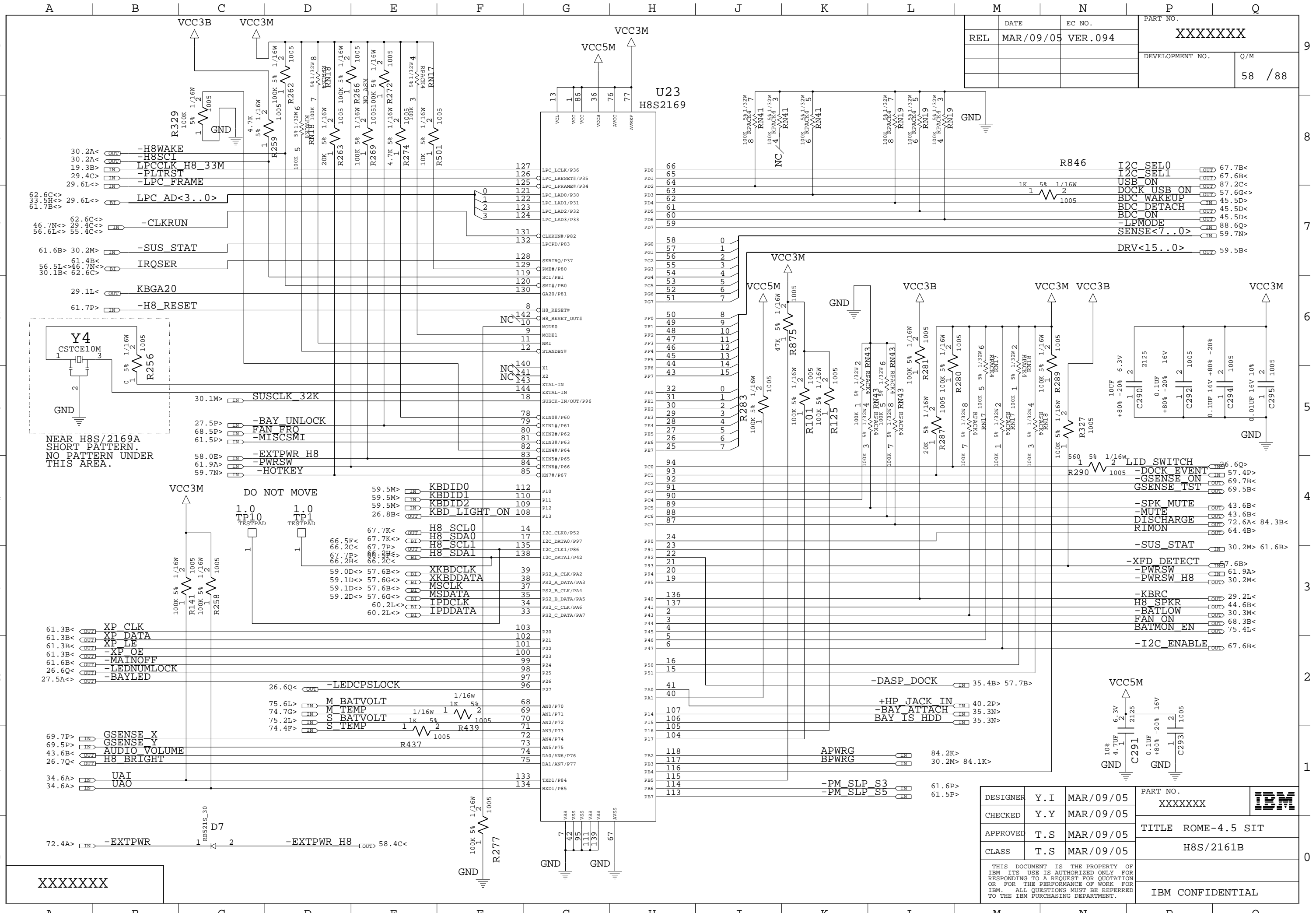
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REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXX
			DEVELOPMENT NO.
			Q/M
			57 / 88

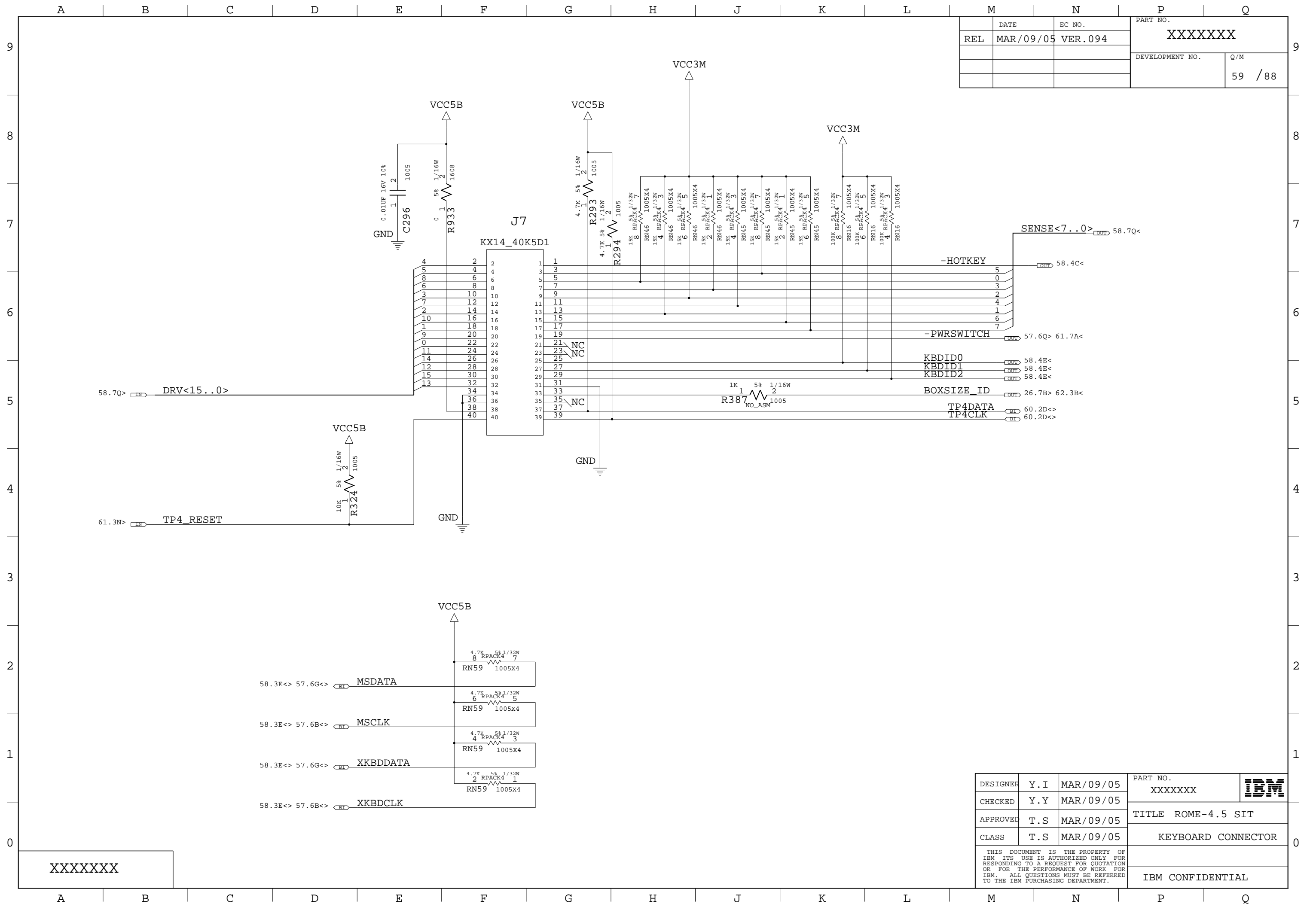
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REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			58 / 88



NEAR H8S/2169A
SHORT PATTERN.
NO PATTERN UNDER
THIS AREA.

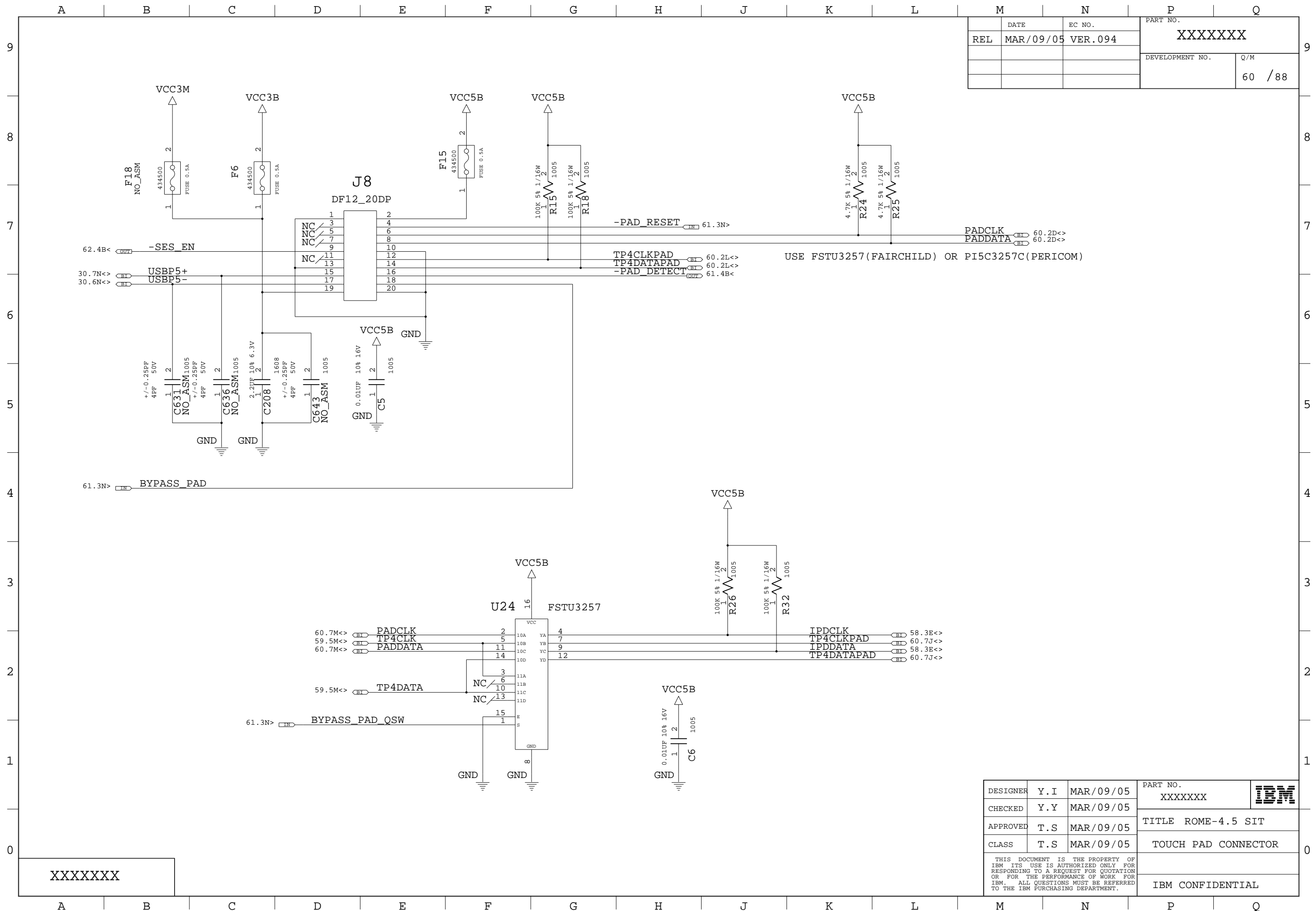
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DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		59 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
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APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	KEYBOARD CONNECTOR		
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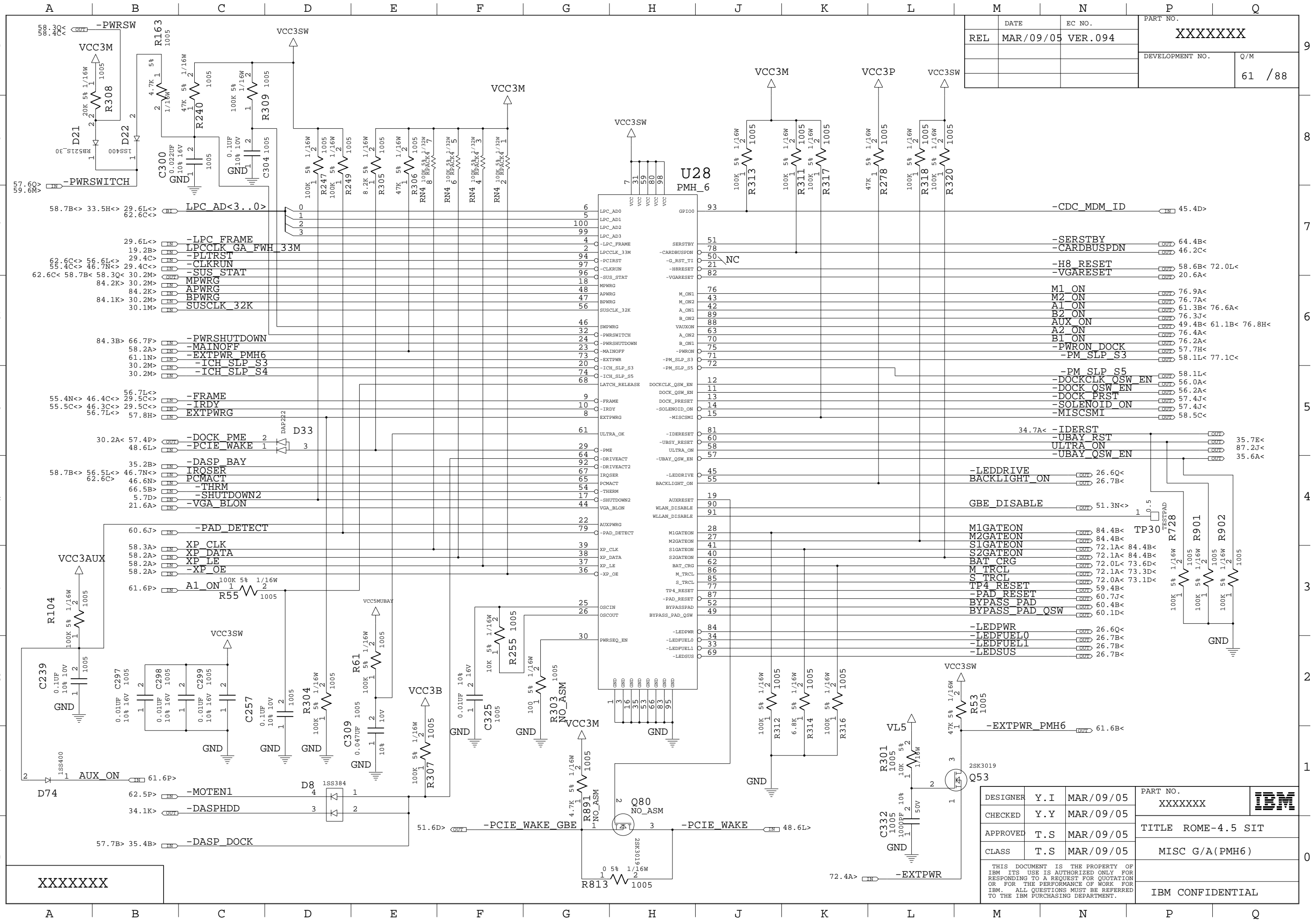
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DATE	EC NO.	PART NO.	
REL MAR/09/05	VER.094	XXXXXXXX	
		DEVELOPMENT NO.	Q/M
			60 / 88

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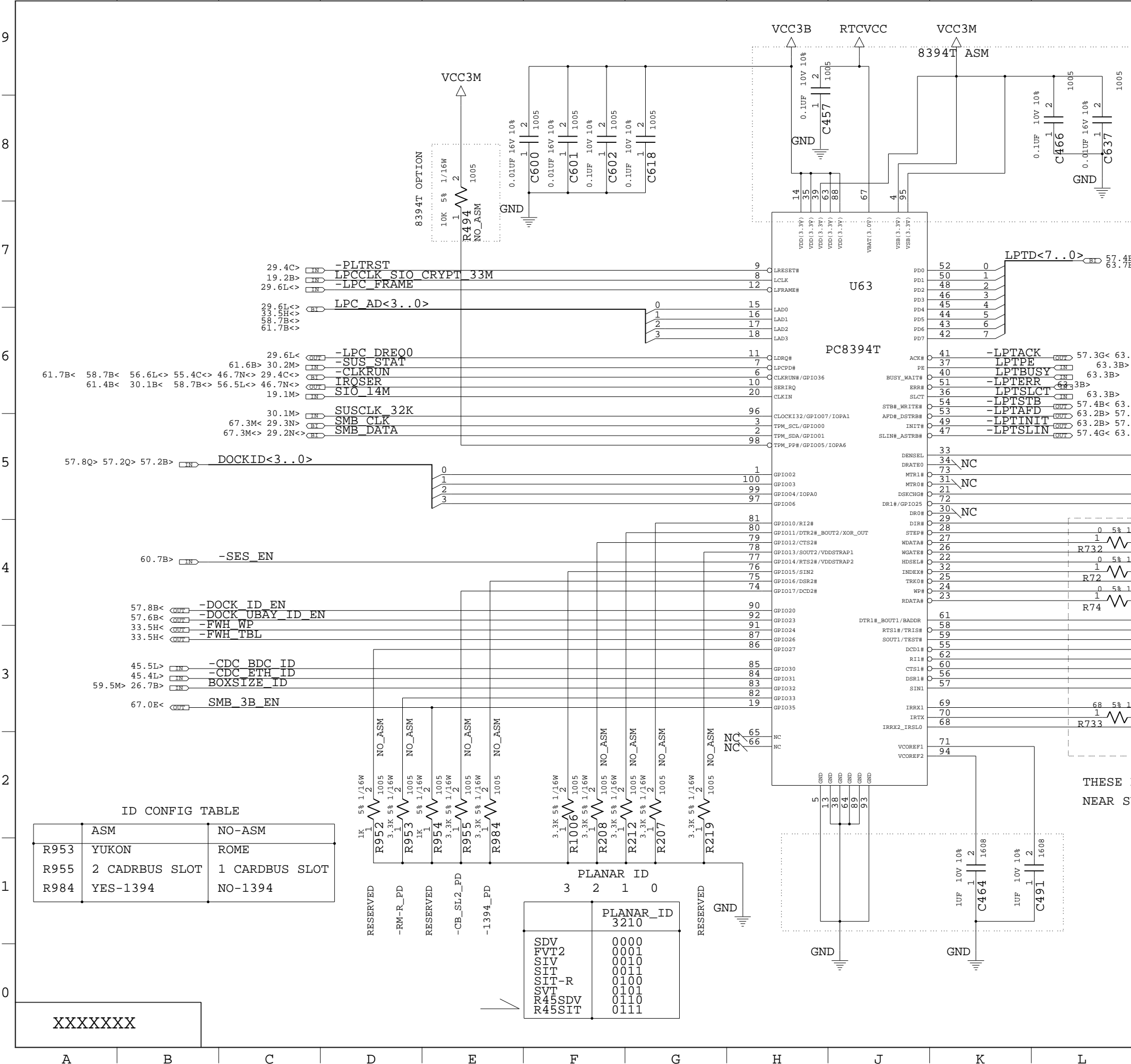
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CLASS	T. S	MAR/09/05	TOUCH PAD CONNECTOR		
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REL	DATE	EC NO.	PART NO.
	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			61 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	MISC G/A (PMH6)		
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DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		62 / 88



ID CONFIG TABLE

	ASM	NO-ASM
R953	YUKON	ROME
R955	2 CADRBUS SLOT	1 CADRBUS SLOT
R984	YES-1394	NO-1394

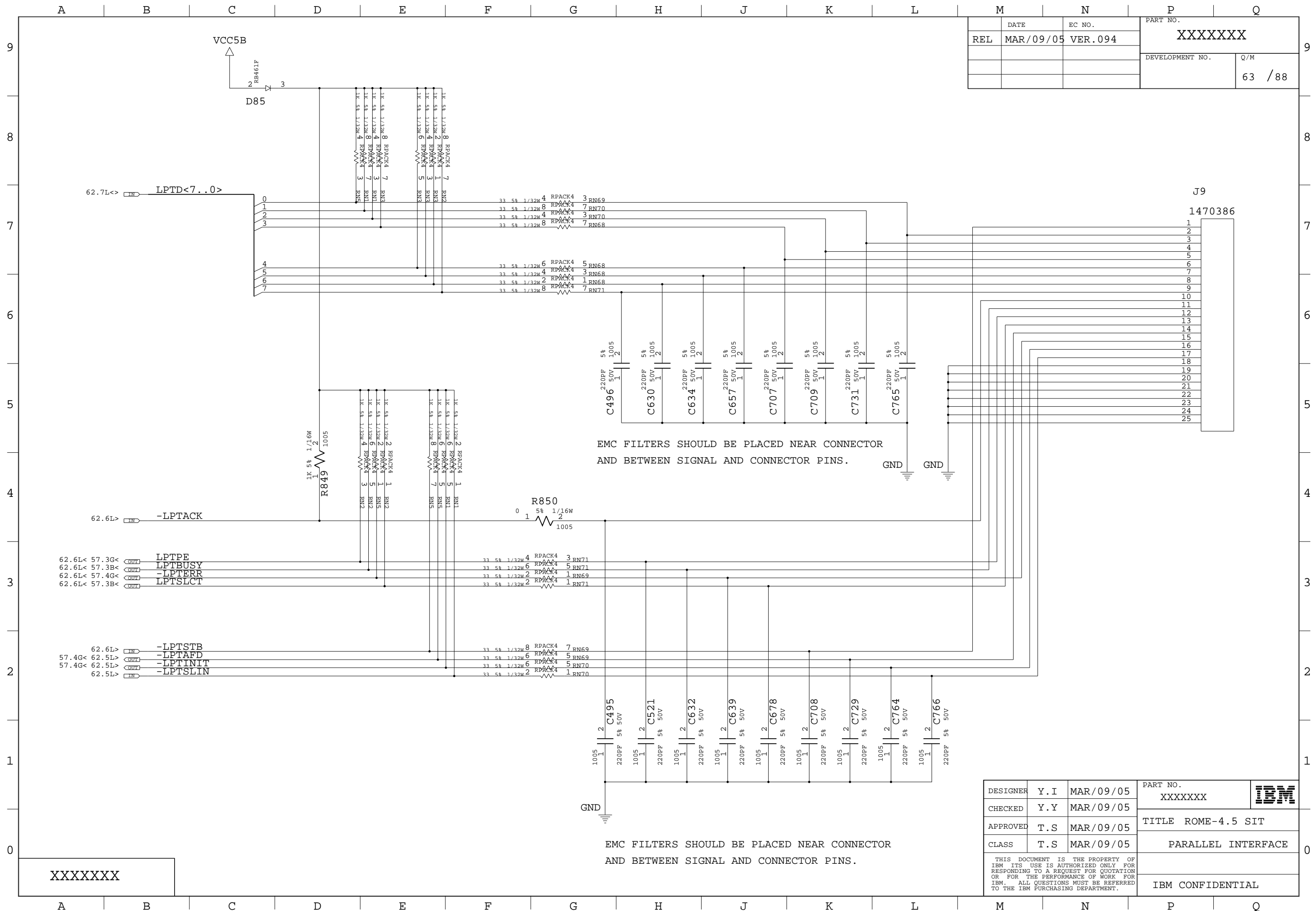
PLANAR ID	PLANAR_ID
3	0000
2	0001
1	0010
0	0011
	0100
	0101
	0110
	0111

THESE DUMPPERS SHOULD BE PLACED NEAR SUPER I/O OUTPUT.

BASE ADDRESS 2E-2FH

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	
CHECKED	Y.Y	MAR/09/05	TITLE ROME-4.5 SIT		
APPROVED	T.S	MAR/09/05	IO KEEPER (SUPER I/O TPM RFID)		
CLASS	T.S	MAR/09/05	100PIN PITCH=0.5MM		
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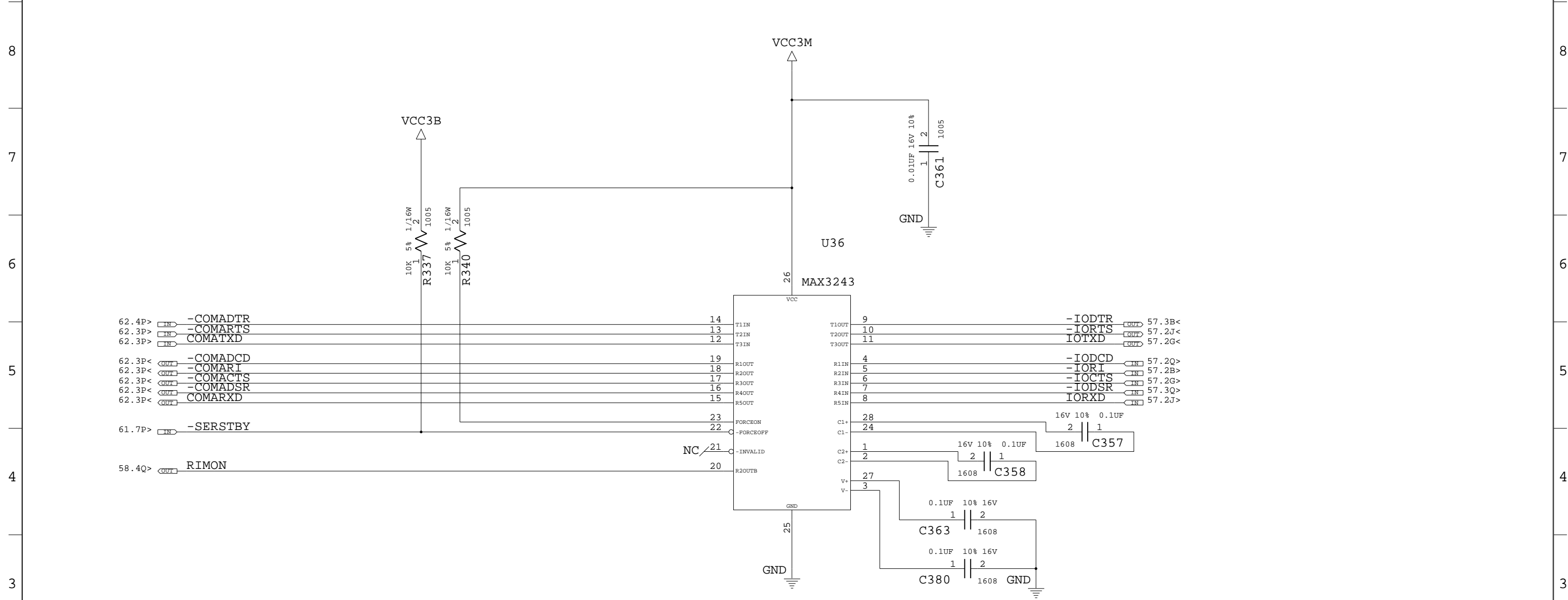
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	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			63 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	PARALLEL INTERFACE		
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DATE		EC NO.		PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX		
DEVELOPMENT NO.				Q/M	
				64 /88	

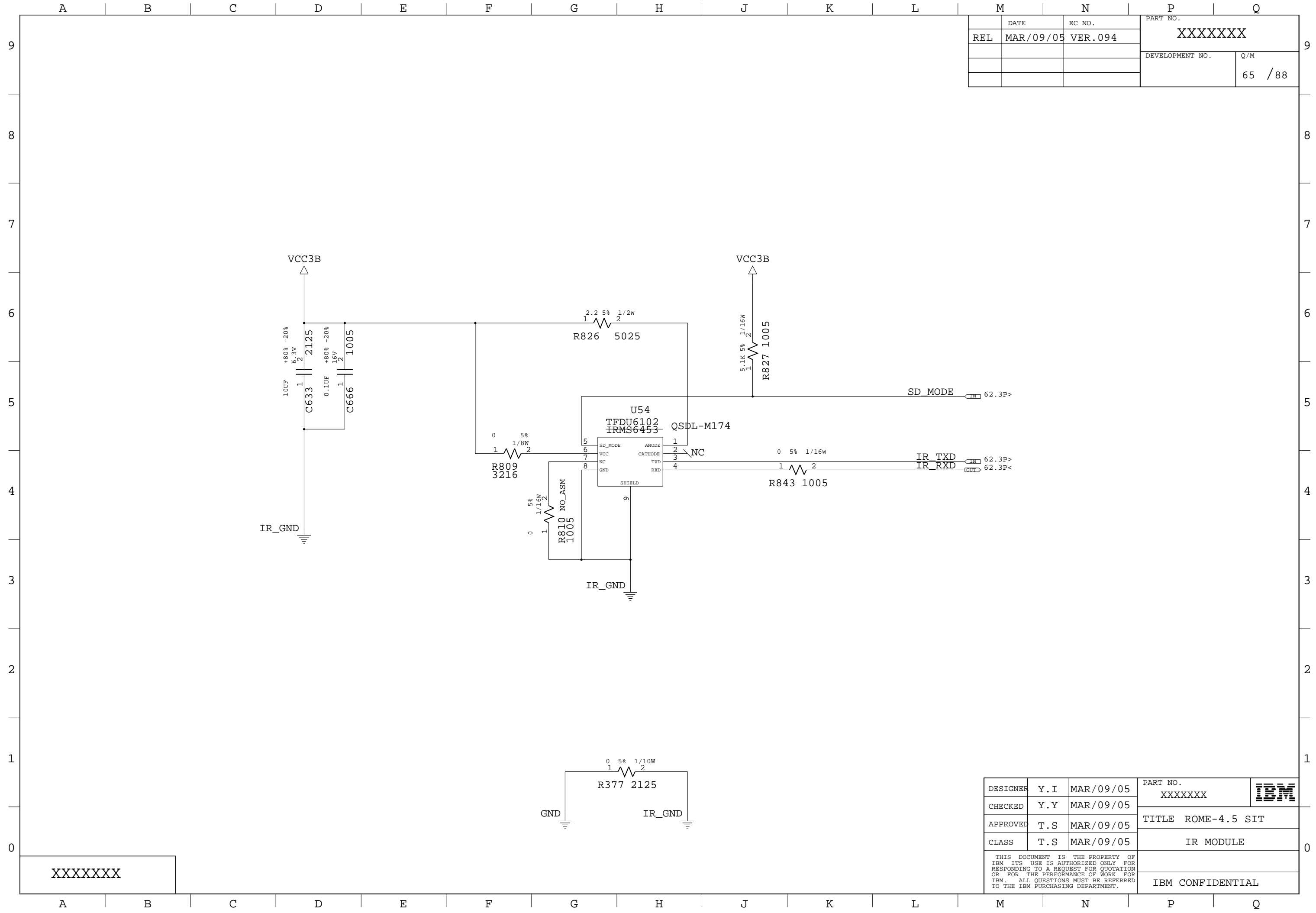


R1IN/R2IN/R3IN/R5IN HAVE INTERNAL PULLDOWN(5K OHM).
DO NOT WIRE SIGNALS UNDER PINS (1/2/3/24/25/26/27/28)
CHARGE PUMP CAPACITOR SHOULD BE PLACED NEAR PINS(1/2/3/24/27/28)
ADD GND SHILED UNDER CHARGE PUMP CIRCUIT TO
PROTECT POWER LINE NOISE
CAPACITORS FOR CHARGE PUMP SHOULD BE USED TYPE B AND LOW ESR TYPE.

	NORMAL MODE	POWER DOWN MODE	AUTO POWER DOWN MODE
FORCEON	HIGH	DO NOT CARE	LOW
FOCEOFF	HIGH	LOW	HIGH

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	SERIAL INTERFACE		
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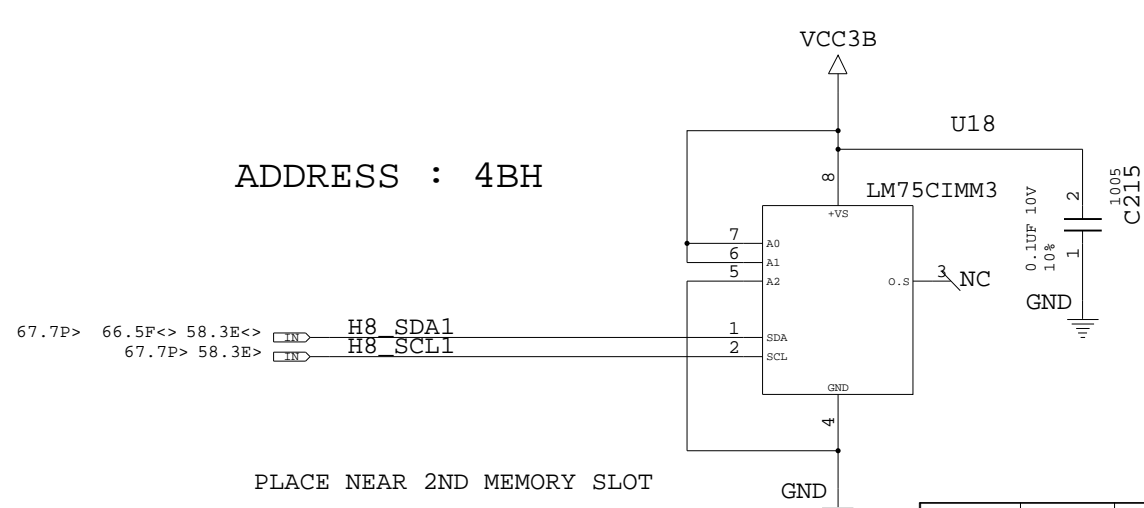
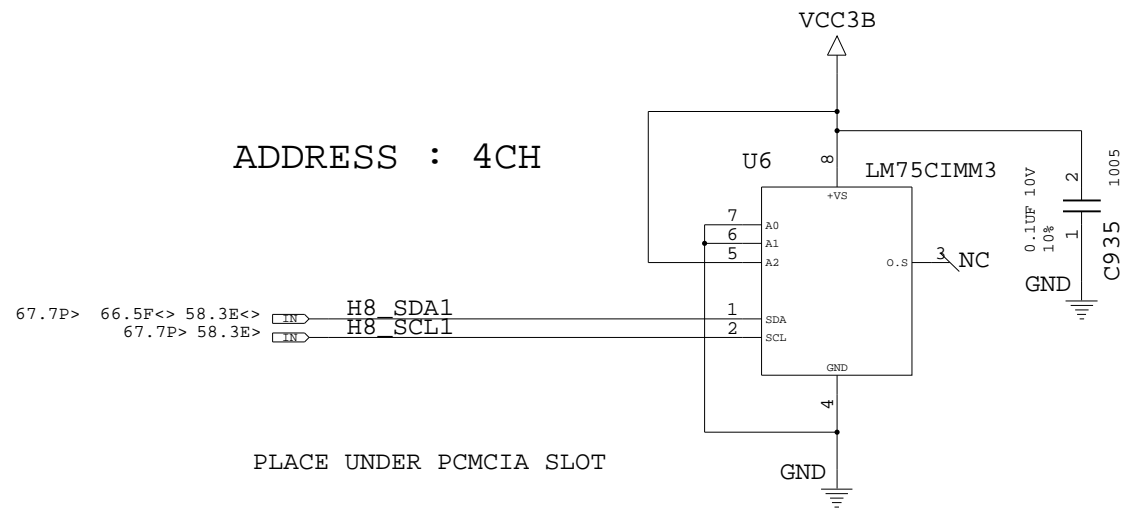
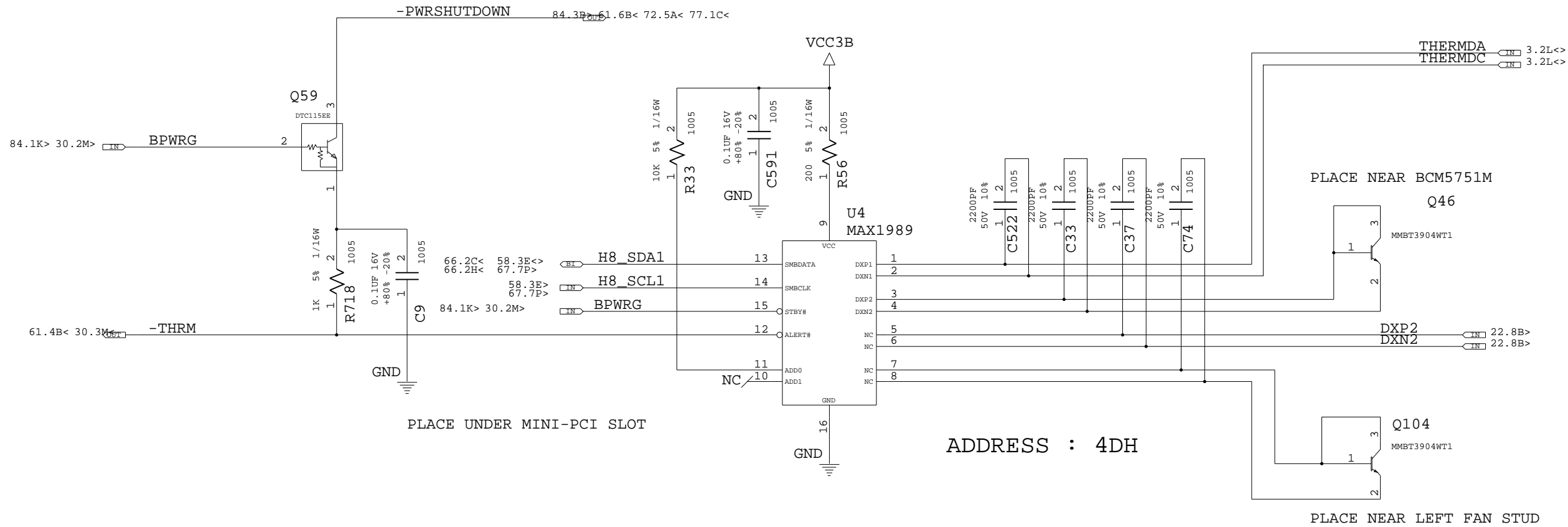


	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				65 /88

XXXXXXXX

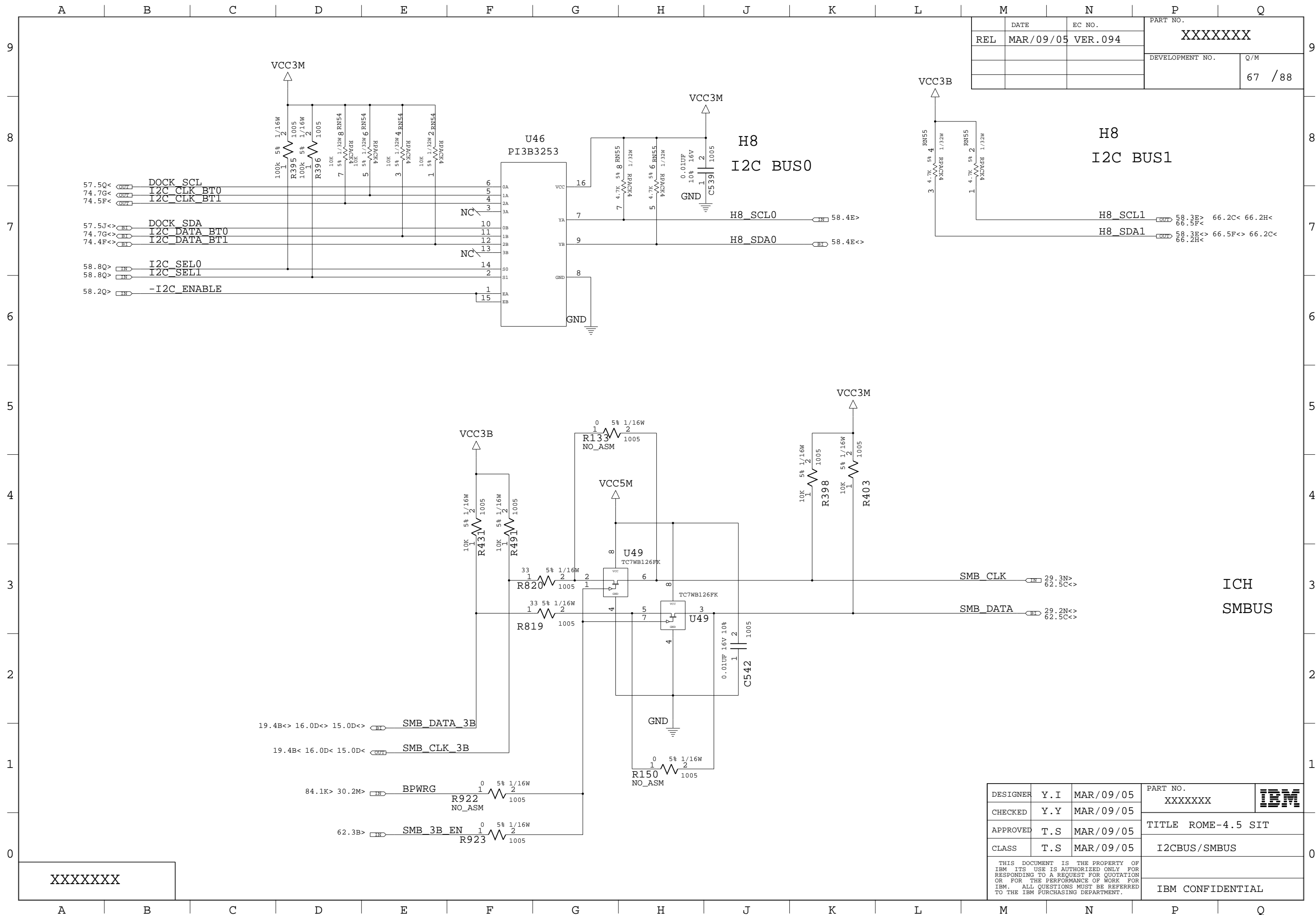
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CLASS	T. S	MAR/09/05	IR MODULE		
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DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		66 / 88



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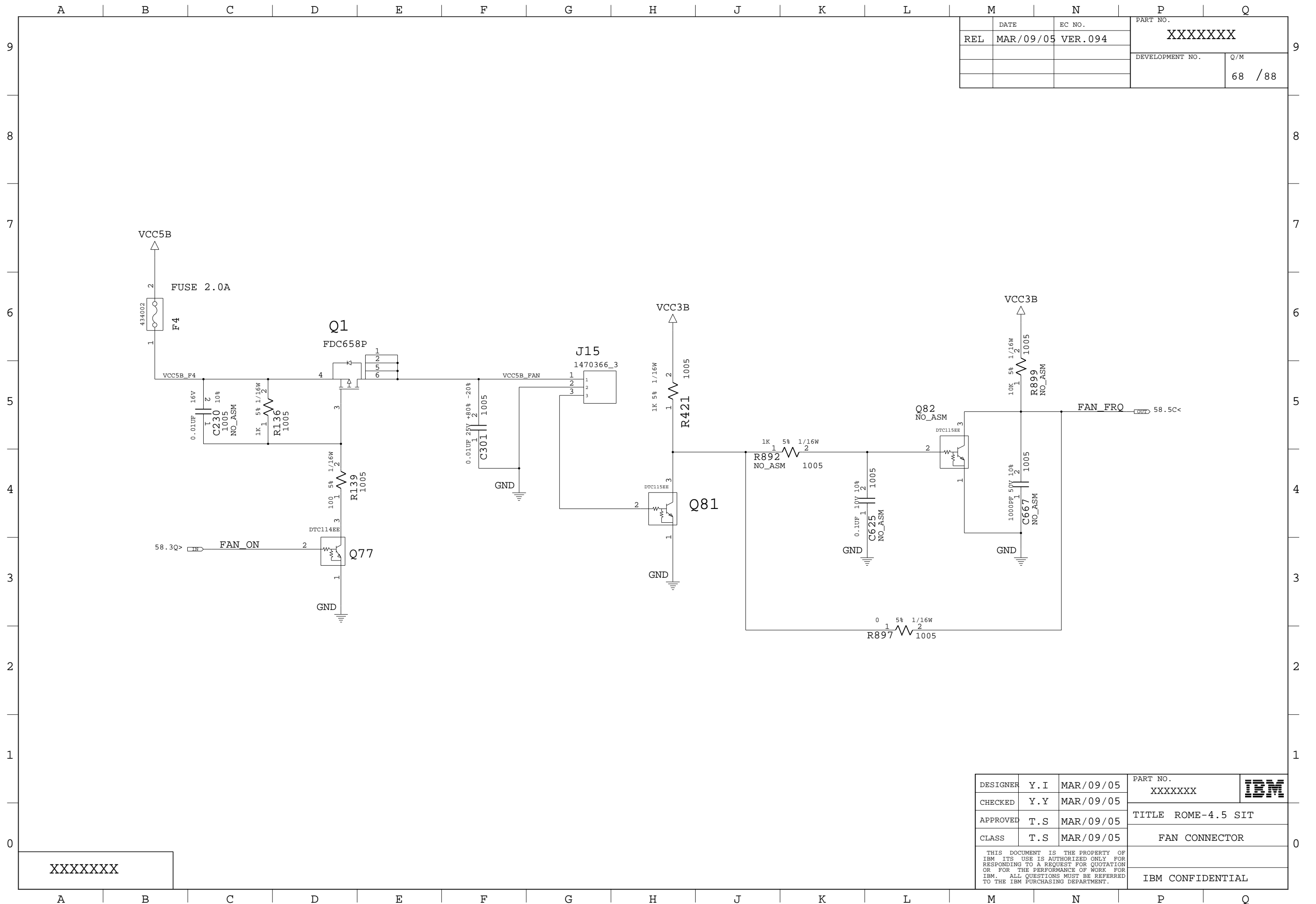
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CHECKED	Y. Y	MAR/09/05			
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CLASS	T. S	MAR/09/05	THERMAL SENSOR		
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	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				67 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	I2CBUS/SMBUS		
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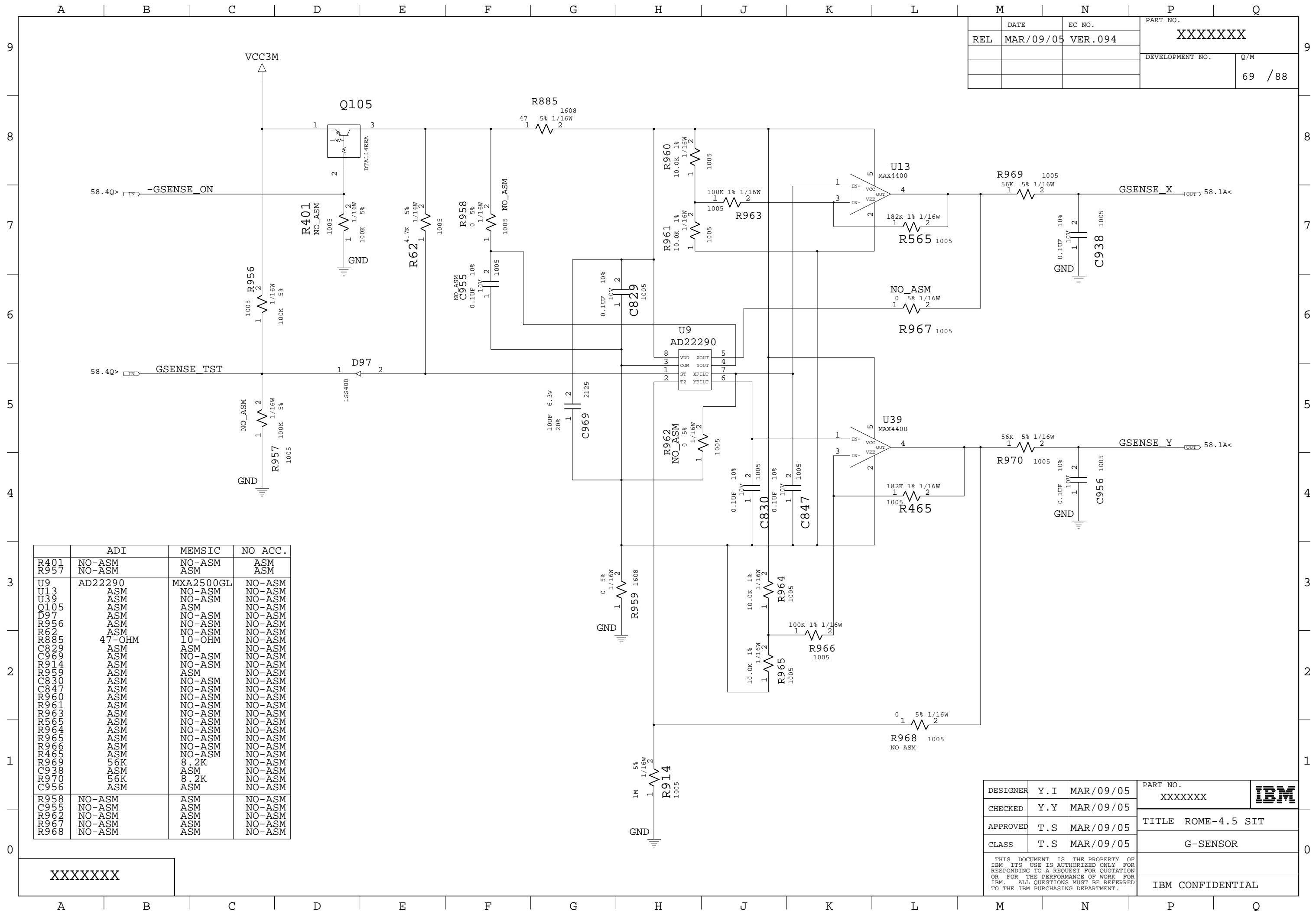
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REL	DATE	EC NO.	PART NO.	
	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				68 / 88

XXXXXXXX

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
APPROVED	T. S	MAR/09/05	TITLE ROME-4.5 SIT		
CLASS	T. S	MAR/09/05	FAN CONNECTOR		
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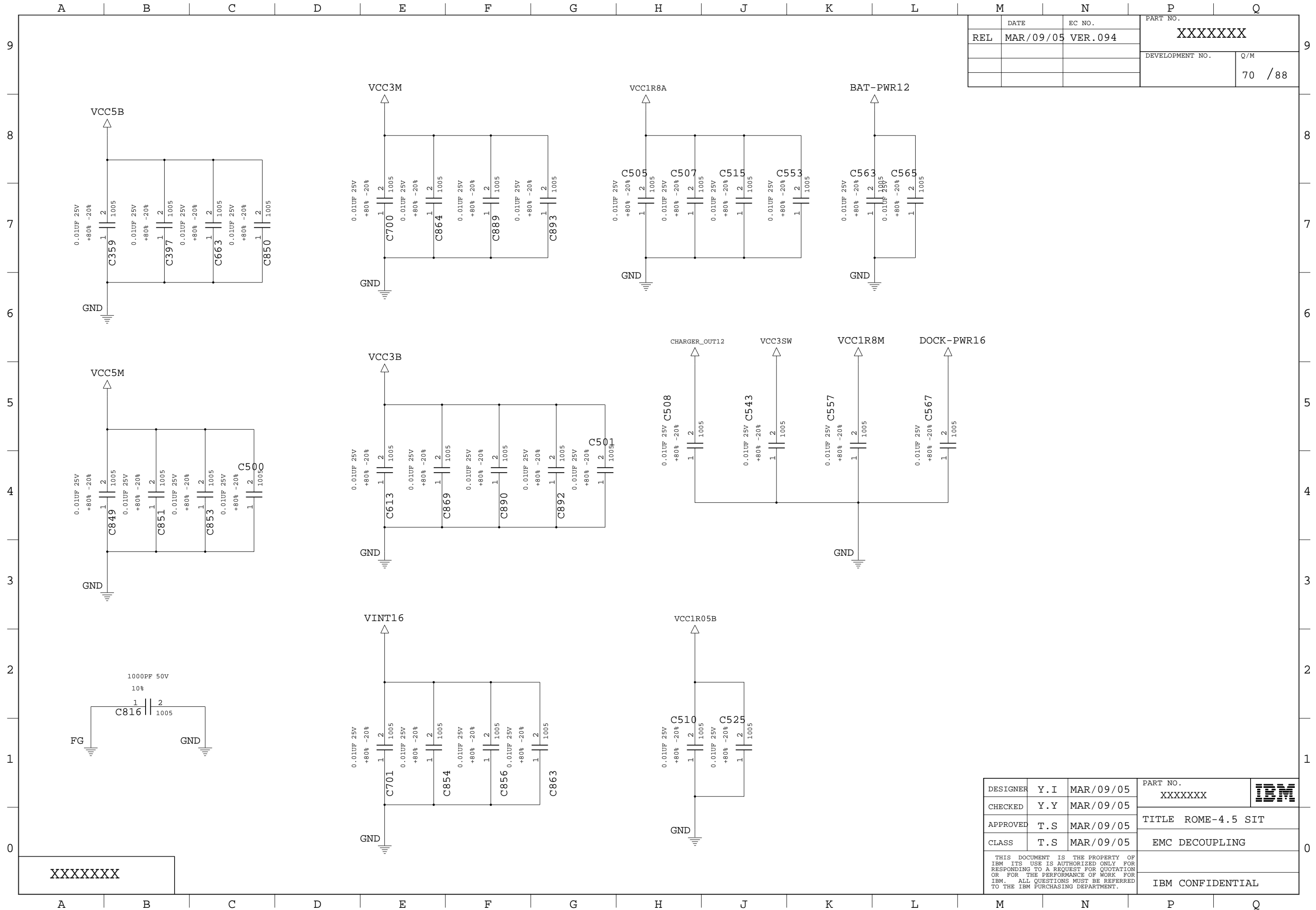


DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		69 / 88

	ADI	MEMSIC	NO ACC.
R401	NO-ASM	NO-ASM	ASM
R957	NO-ASM	ASM	ASM
U9	AD22290	MXA2500GL	NO-ASM
U13	ASM	NO-ASM	NO-ASM
U39	ASM	NO-ASM	NO-ASM
Q105	ASM	ASM	NO-ASM
D97	ASM	NO-ASM	NO-ASM
R956	ASM	NO-ASM	NO-ASM
R958	ASM	NO-ASM	NO-ASM
R885	47-OHM	10-OHM	NO-ASM
C829	ASM	ASM	NO-ASM
C955	ASM	NO-ASM	NO-ASM
C969	ASM	NO-ASM	NO-ASM
C830	ASM	NO-ASM	NO-ASM
C847	ASM	NO-ASM	NO-ASM
C956	ASM	NO-ASM	NO-ASM
C938	ASM	NO-ASM	NO-ASM
R961	ASM	NO-ASM	NO-ASM
R960	ASM	NO-ASM	NO-ASM
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R966	ASM	NO-ASM	NO-ASM
R968	ASM	NO-ASM	NO-ASM
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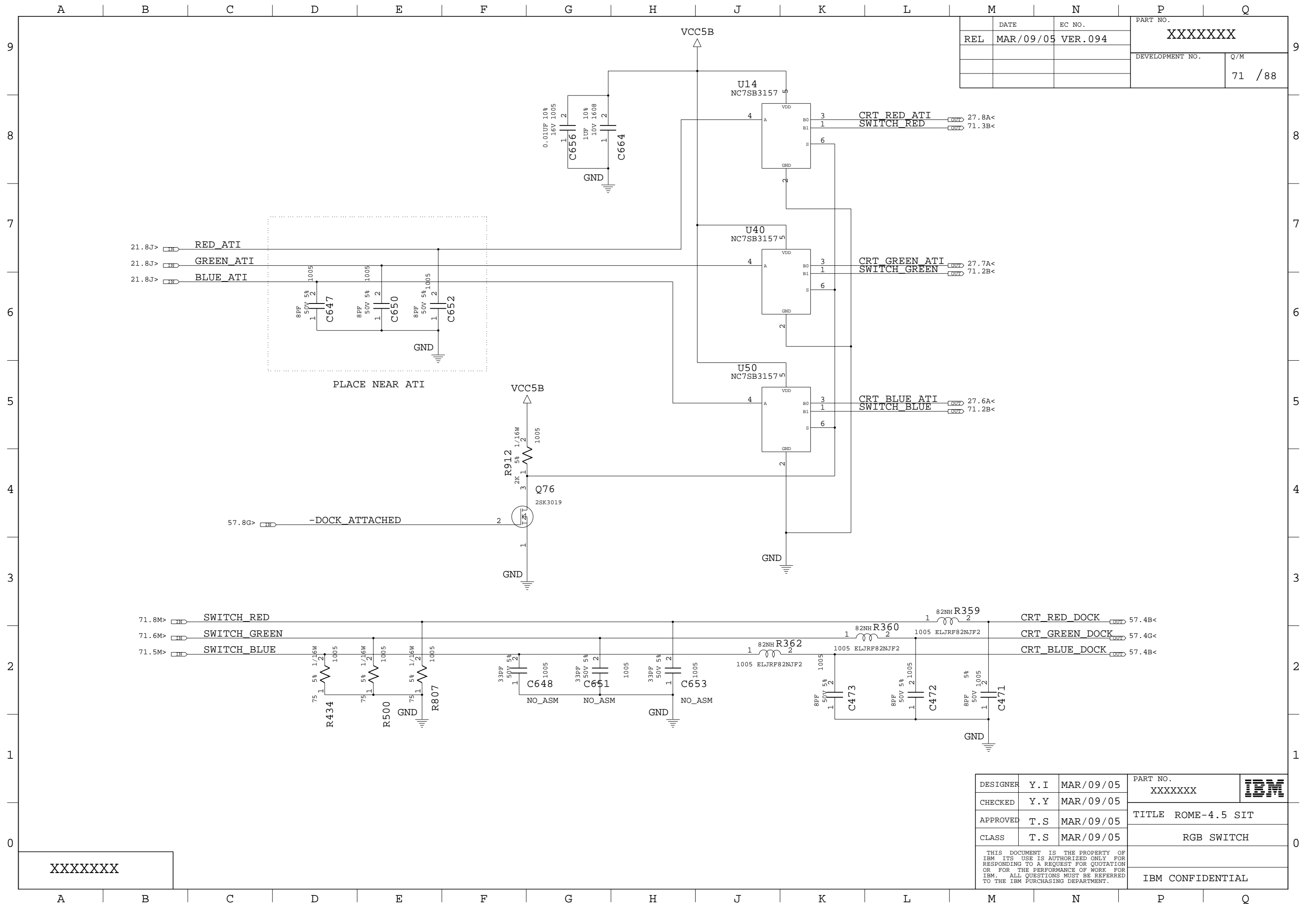
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REL	MAR/09/05	VER.094	XXXXXXX	
			DEVELOPMENT NO.	Q/M
			70	/88

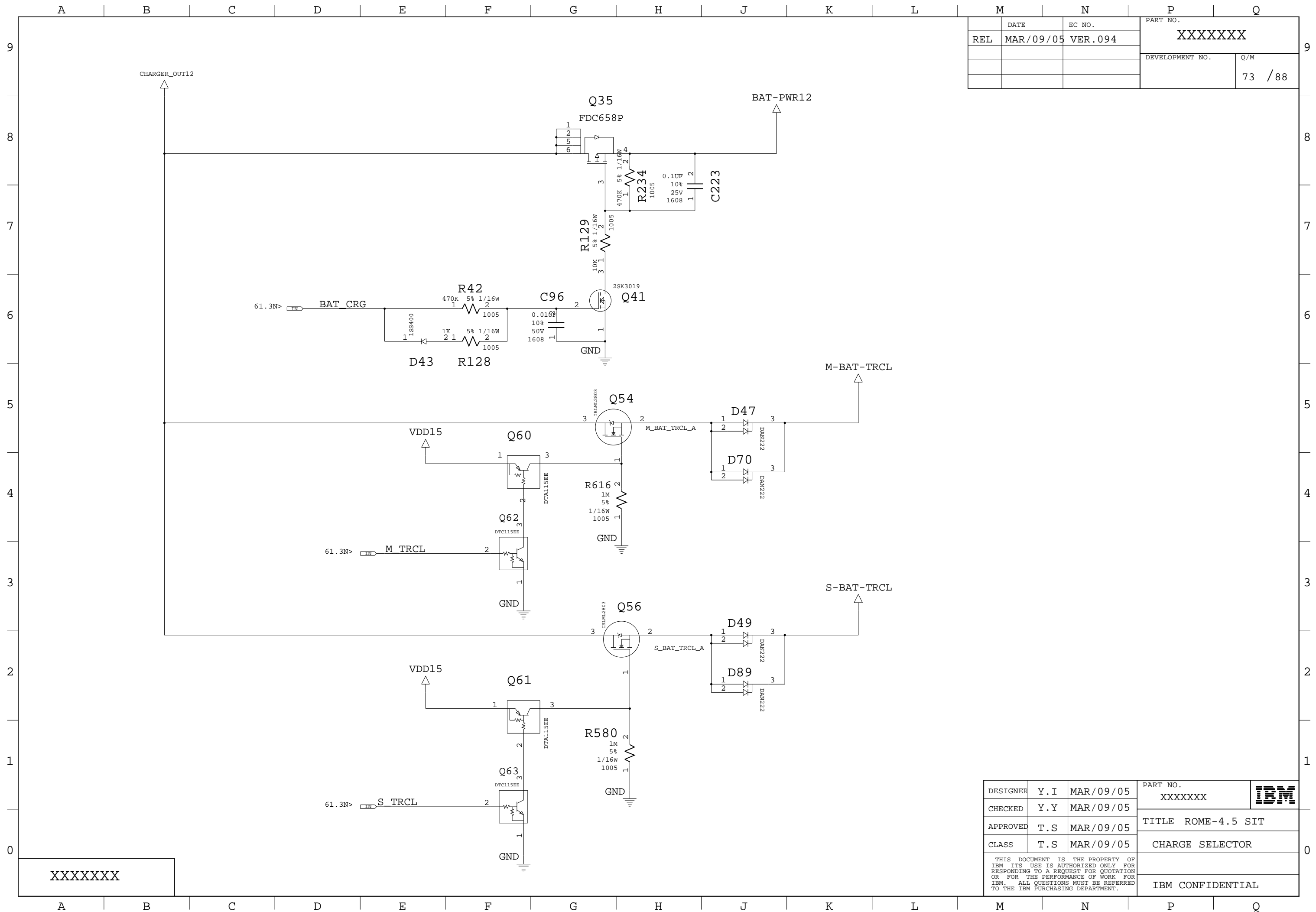
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CLASS	T. S	MAR/09/05	EMC DECOUPLING		
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	DATE	EC NO.	PART NO.
REL	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			71 / 88

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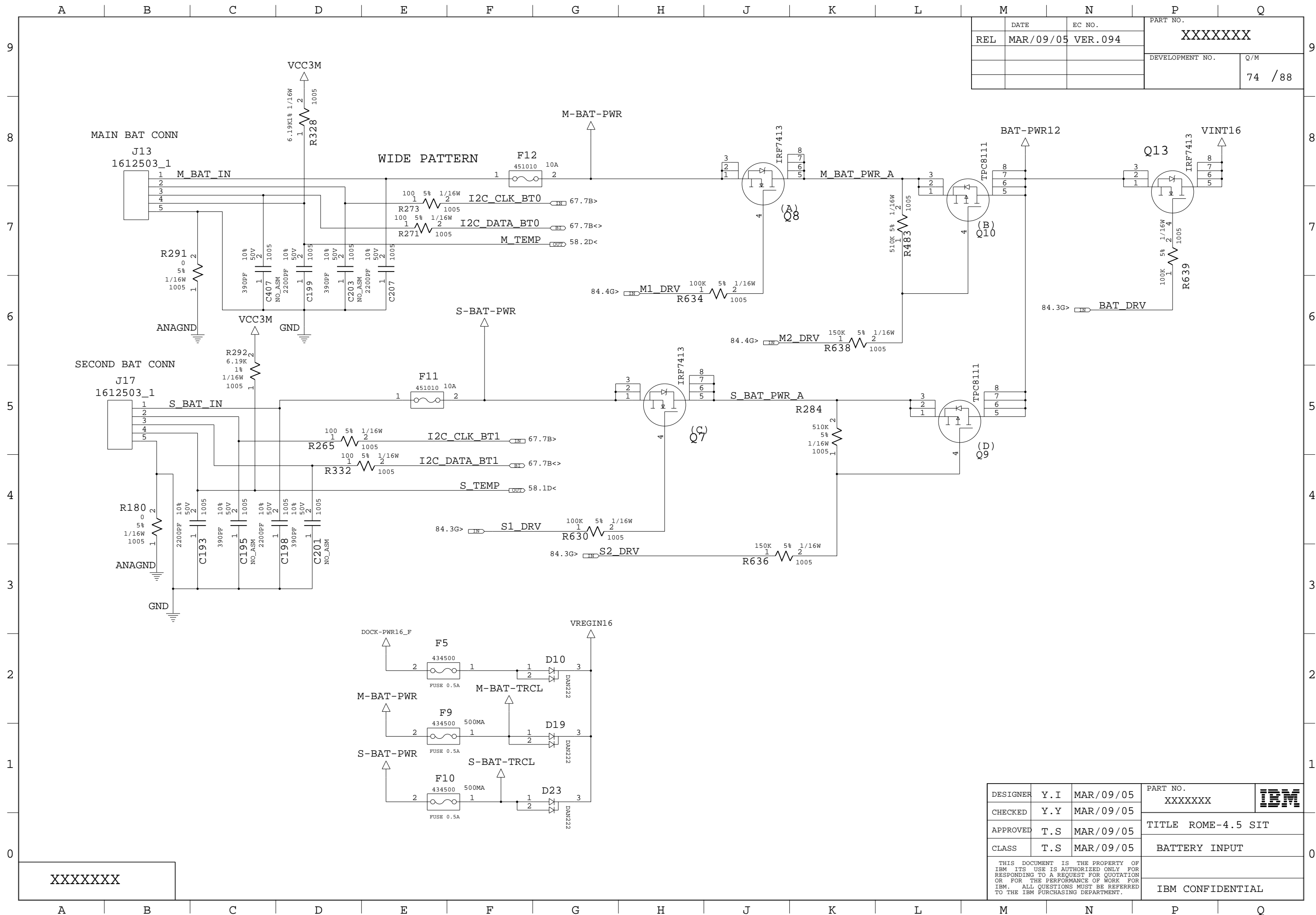
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CLASS	T. S	MAR/09/05	RGB SWITCH		
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REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				73 /88

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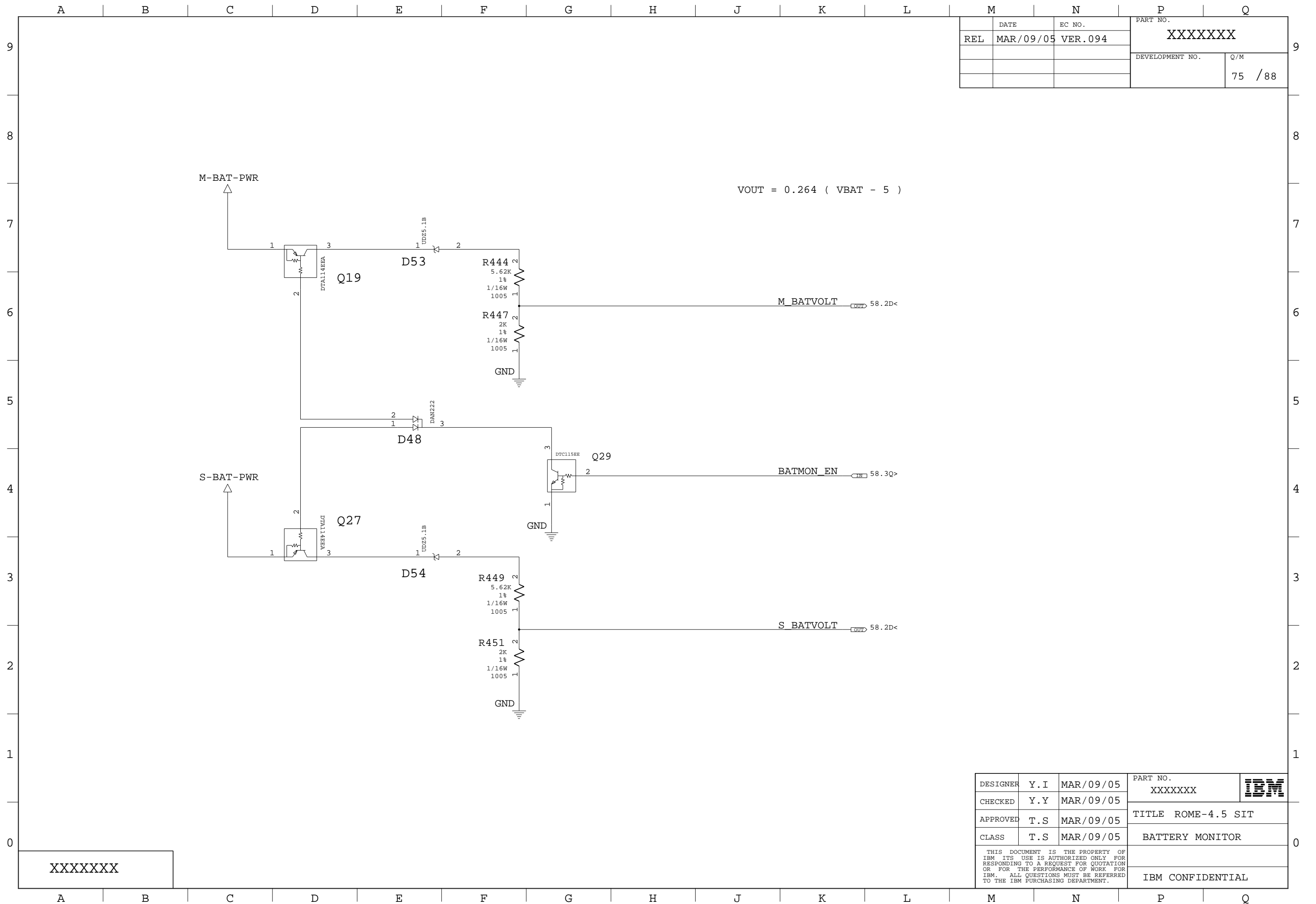
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DATE	EC NO.	PART NO.
MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		74 / 88

DESIGNER	Y. I	MAR/09/05	PART NO.	XXXXXXXX	IBM
CHECKED	Y. Y	MAR/09/05			
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CLASS	T. S	MAR/09/05	BATTERY INPUT		
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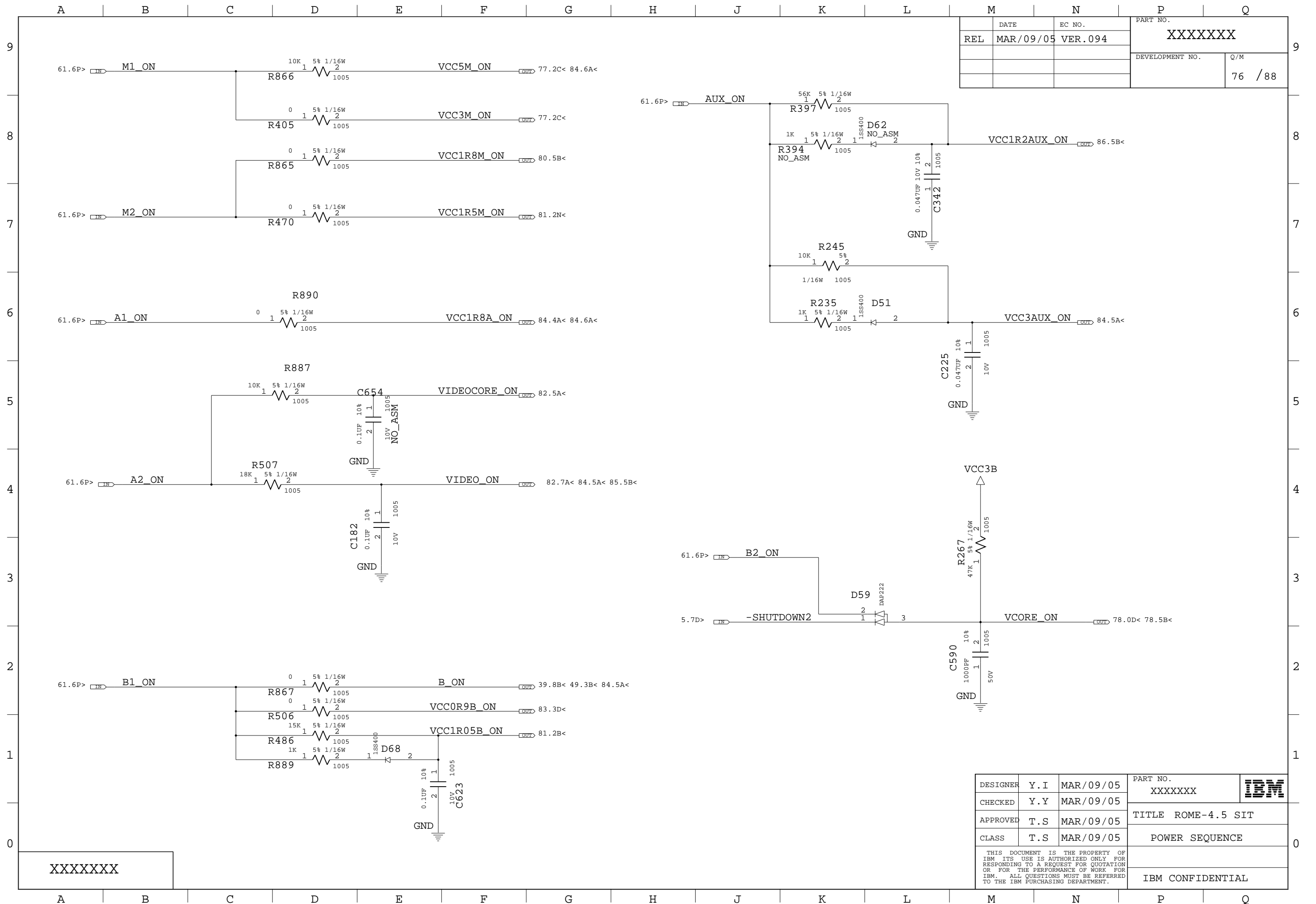
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	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				75 /88

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			DEVELOPMENT NO.	Q/M
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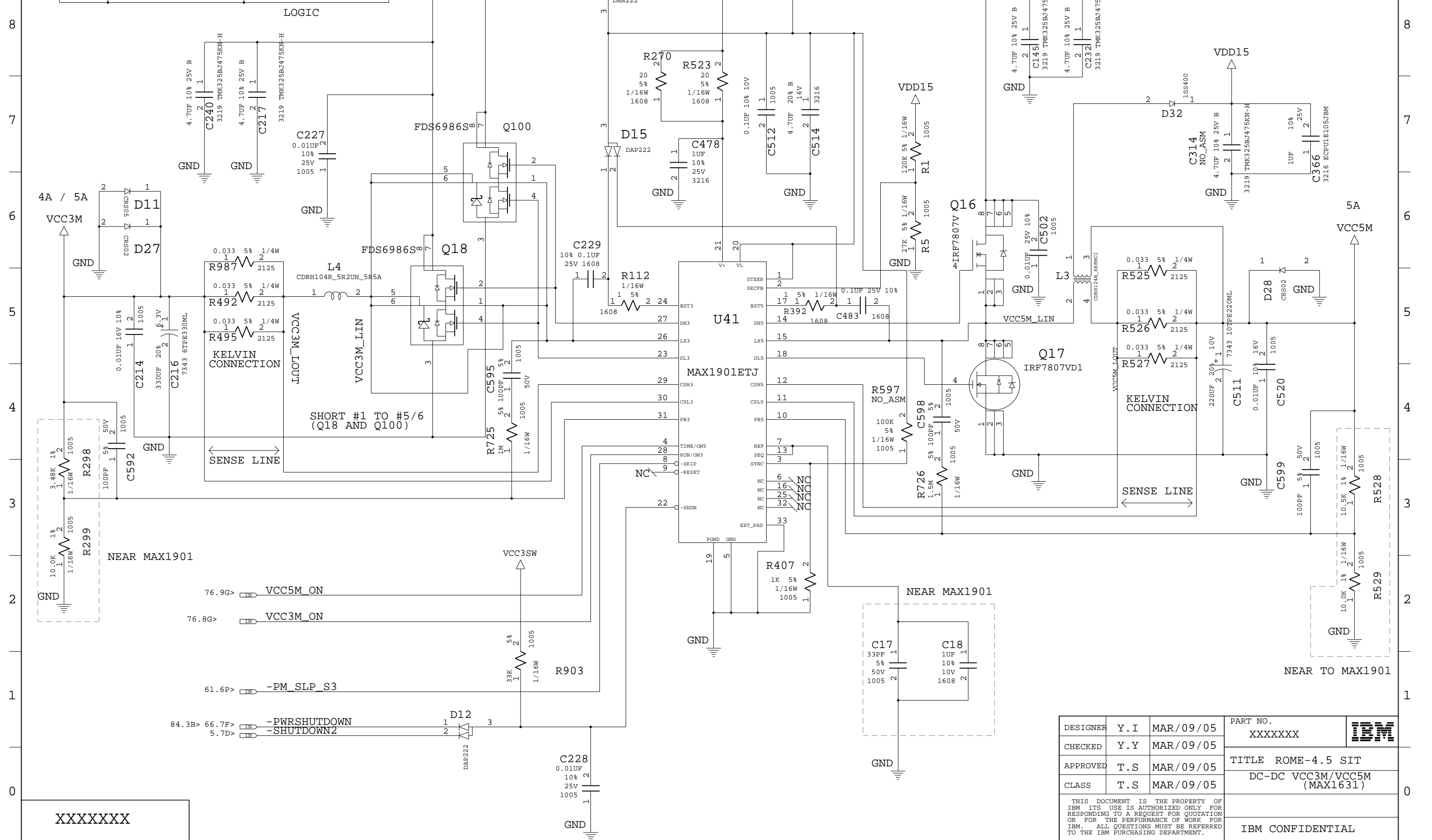
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A B C D E F G H J K L M N P Q

VCC3M TABLE 1/1

VCC3M	4.0A	5.0A
R987	NO-ASM	ASM
L4	CDRH104R_10UH_4R4A	CDRH104R_5R2UH_5R5A
Q100	NO-ASM	ASM
C217	NO-ASM	ASM

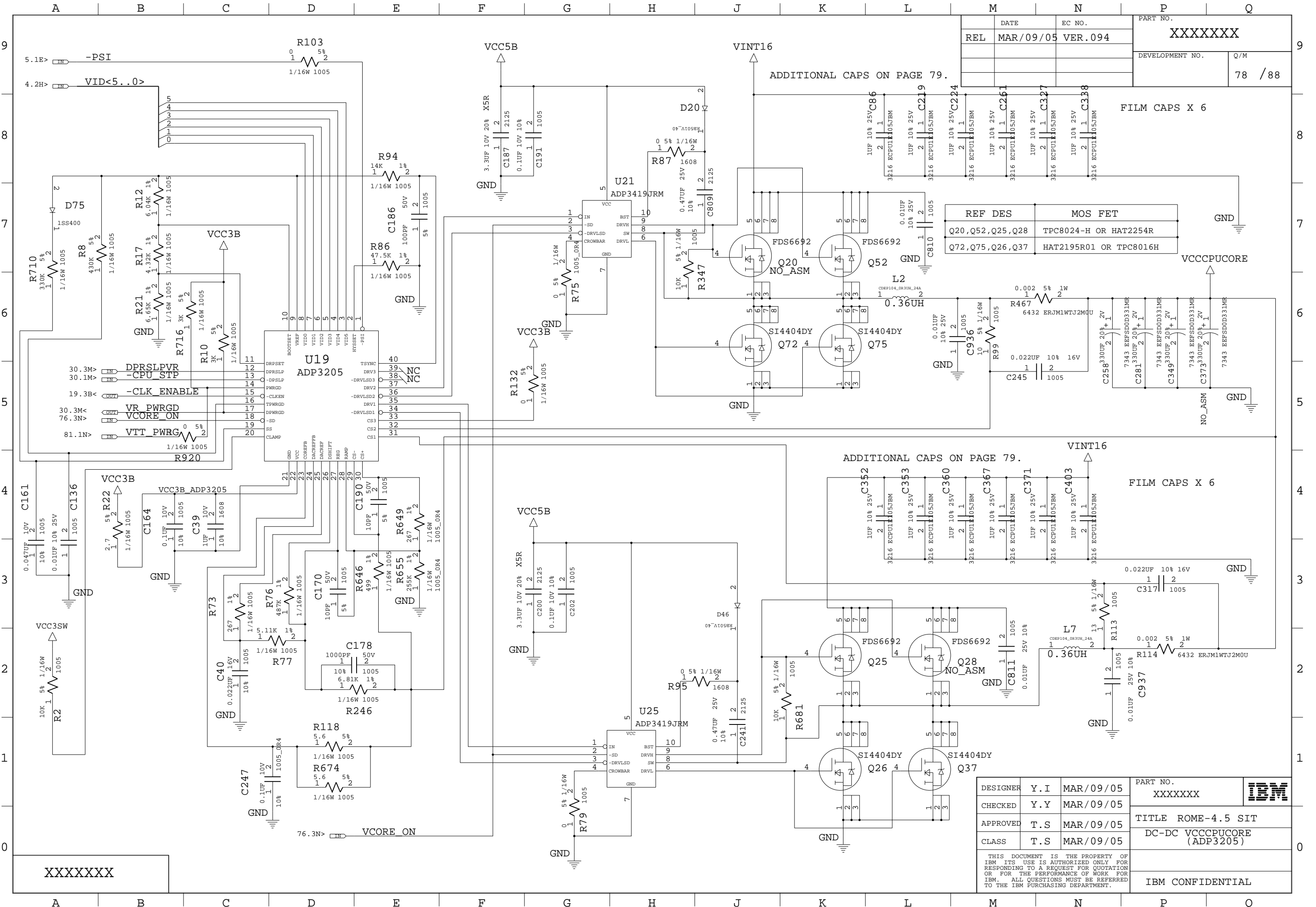
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	MAR/09/05	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			77 / 88



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CHECKED	Y. Y	MAR/09/05			
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CLASS	T. S	MAR/09/05	DC-DC VCC3M/VCC5M (MAX1631)		
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A B C D E F G H J K L M N P Q



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DEVELOPMENT NO.			Q/M
			78 / 88

REF DES	MOS FET	
Q20, Q52, Q25, Q28	TPC8024-H OR HAT2254R	
Q72, Q75, Q26, Q37	HAT2195R01 OR TPC8016H	

C256	330UF 20% 2V	
C281	330UF 20% 2V	
C349	330UF 20% 2V	
C373	330UF 20% 2V	
C734	EFDSD0331MR	
C734	EFDSD0331MR	
C734	EFDSD0331MR	
C734	EFDSD0331MR	

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CLASS	T. S	MAR/09/05	DC-DC VCCCPUCORE (ADP3205)

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FILM CAPS X 6

FILM CAPS X 6

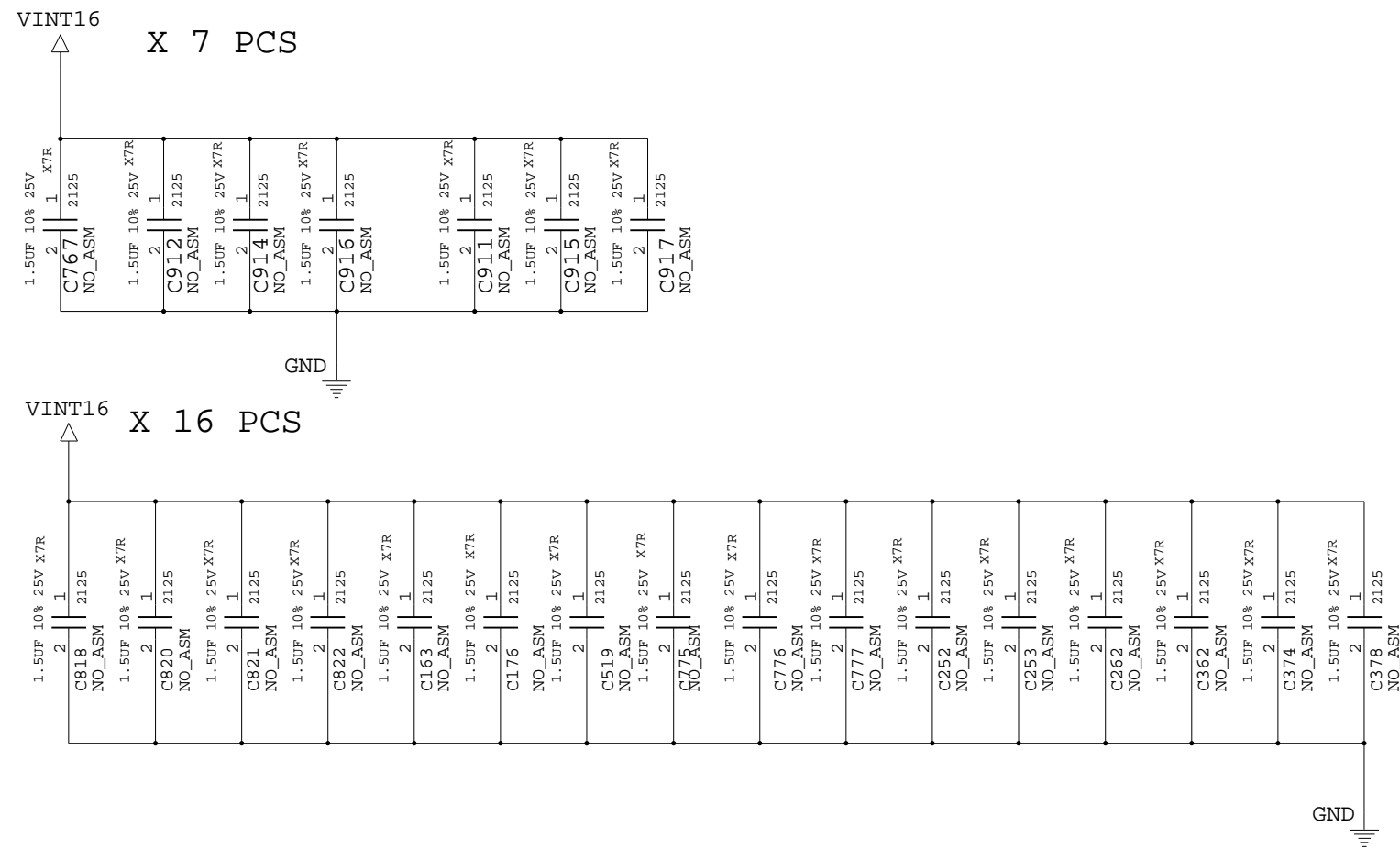
ADDITIONAL CAPS ON PAGE 79.

ADDITIONAL CAPS ON PAGE 79.

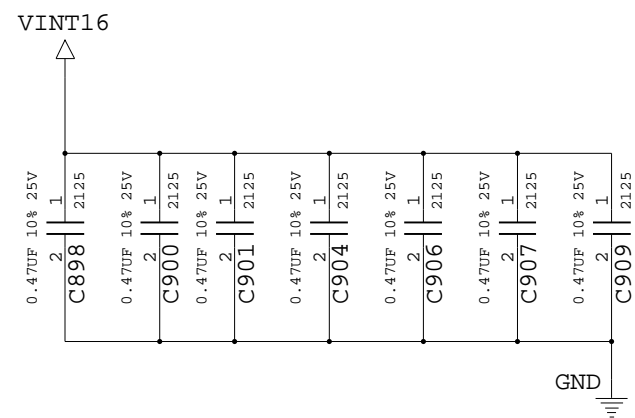
	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				79 /88

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FOLLOWING 23 PCS OF 1.5UF ARE NO-ASM FOR VCCCPUCORE.

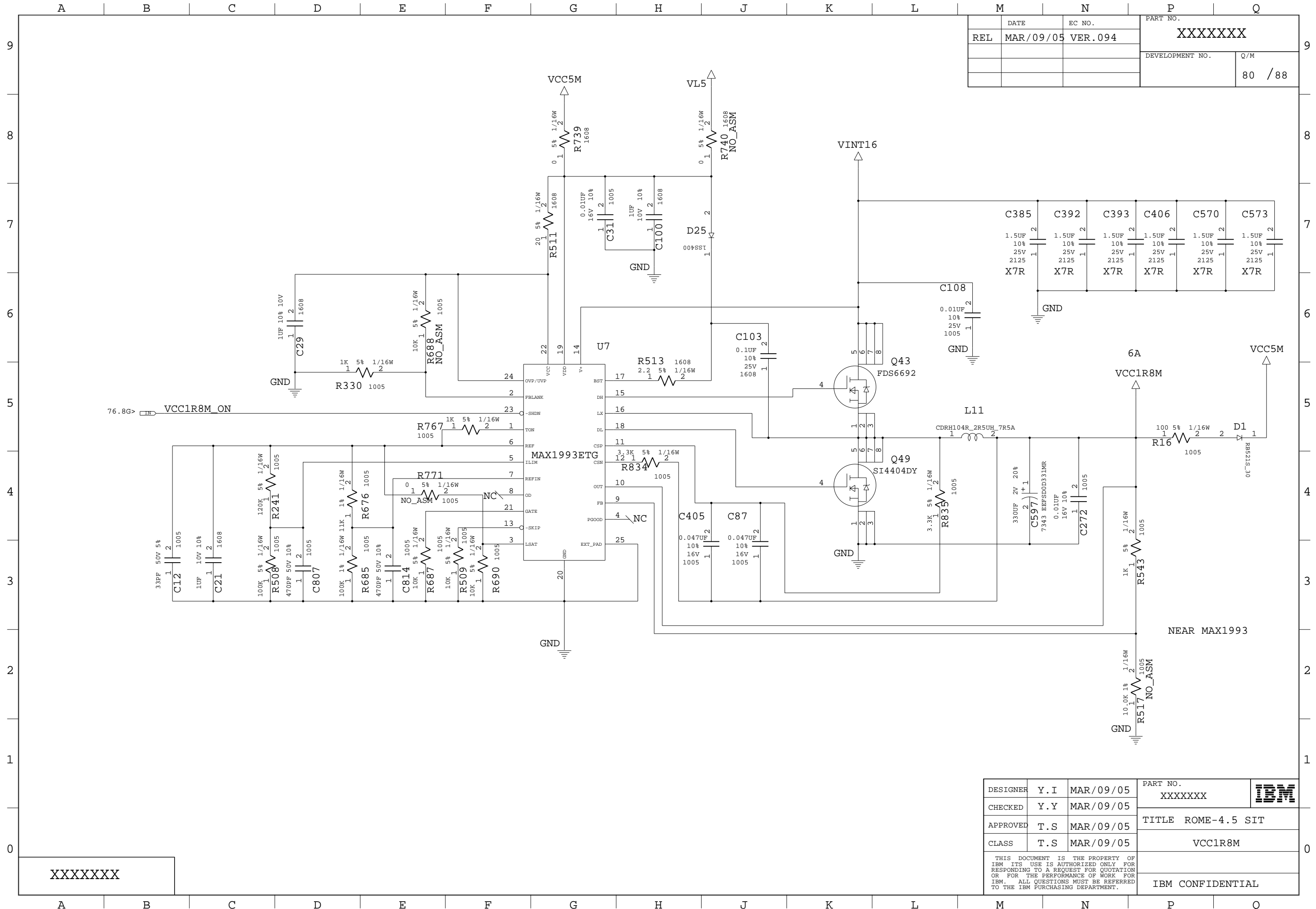


FOLLOWING 7 PCS OF 0.47UF AREA ASM FOR VCCCPUCORE TO REDUCE EMI.



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CLASS	T. S	MAR/09/05	DC-DC VCORE INPUT CAP		
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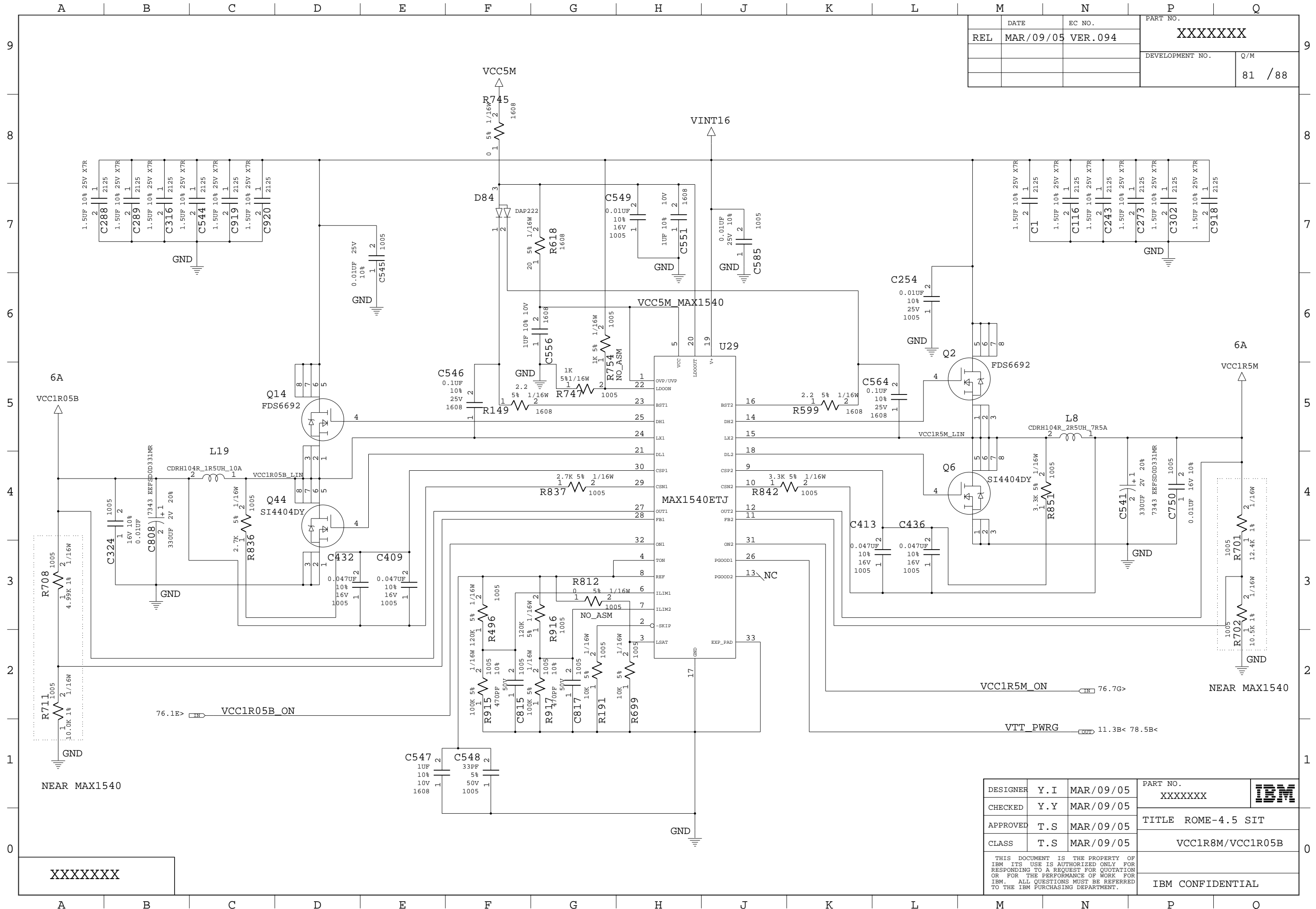


DATE	EC NO.	PART NO.
REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		80 / 88

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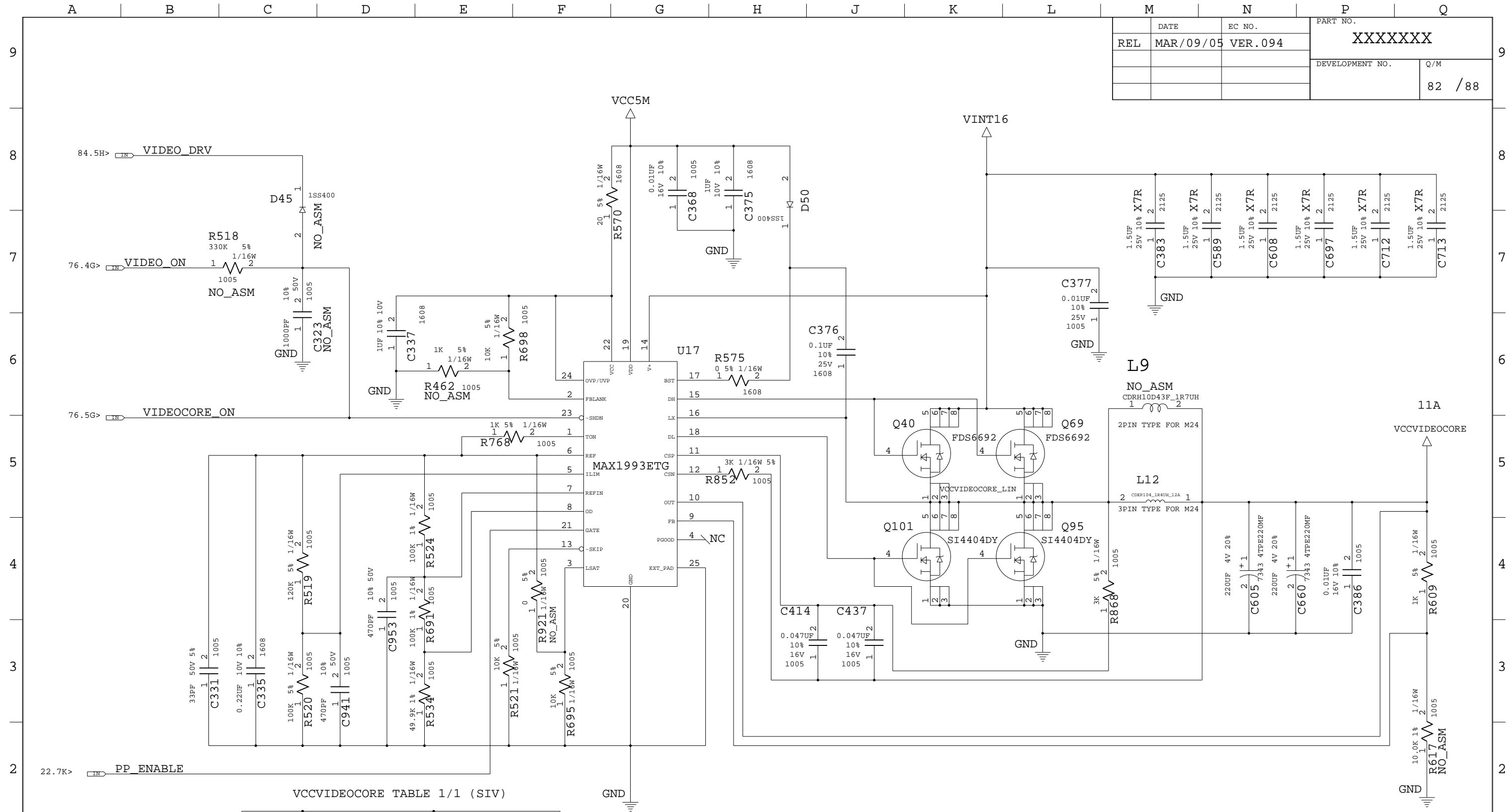
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REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		81 / 88



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CHECKED	Y. Y	MAR/09/05			
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REL MAR/09/05	VER.094	XXXXXXXX
DEVELOPMENT NO.		Q/M
		82 / 88



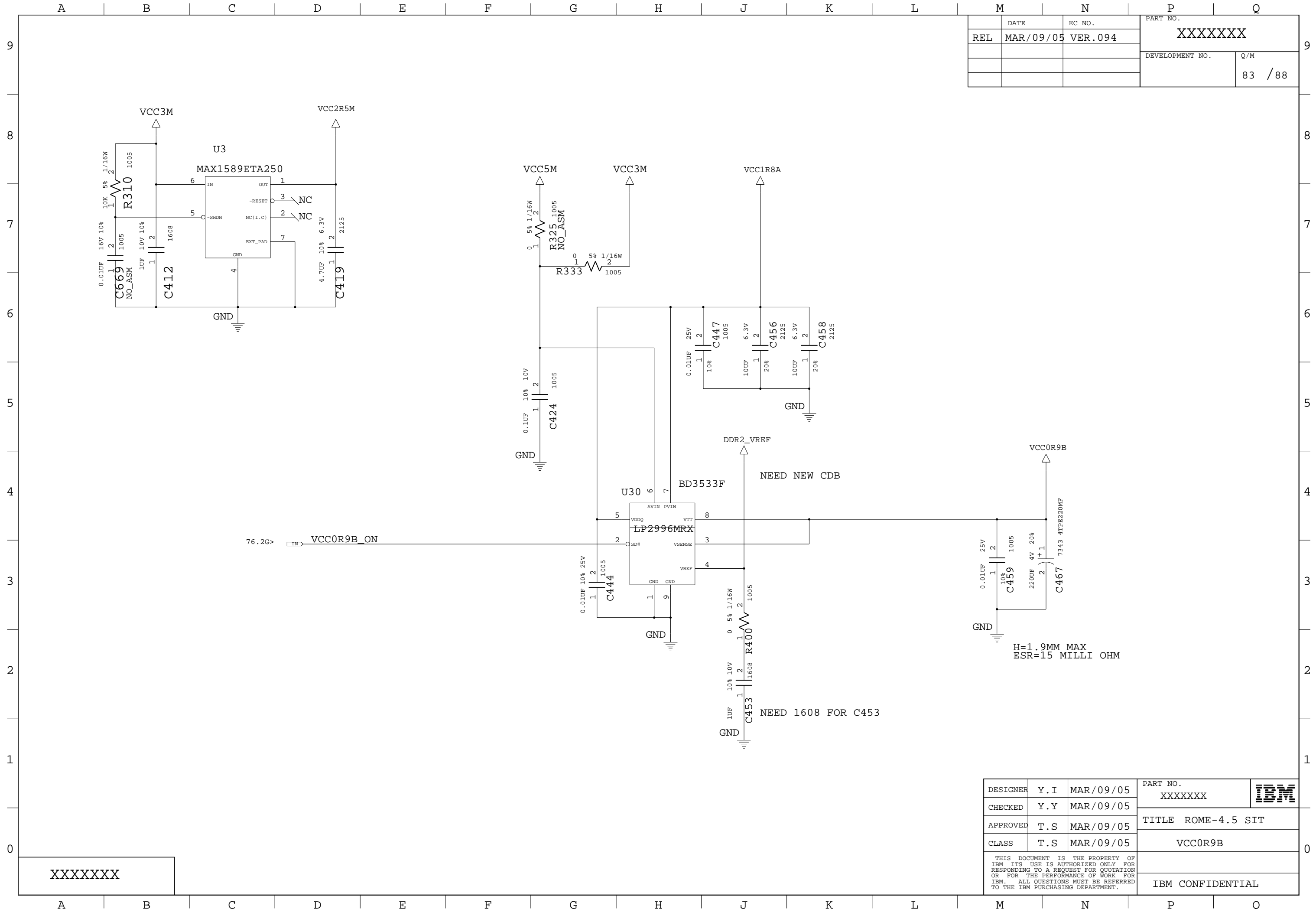
VCCVIDEOCORE TABLE 1/1 (SIV)

	M22 A12 (1.15V)	M24 A22 (1.2V)
R534	35.7K 1%	49.9K 1%

LOGIC

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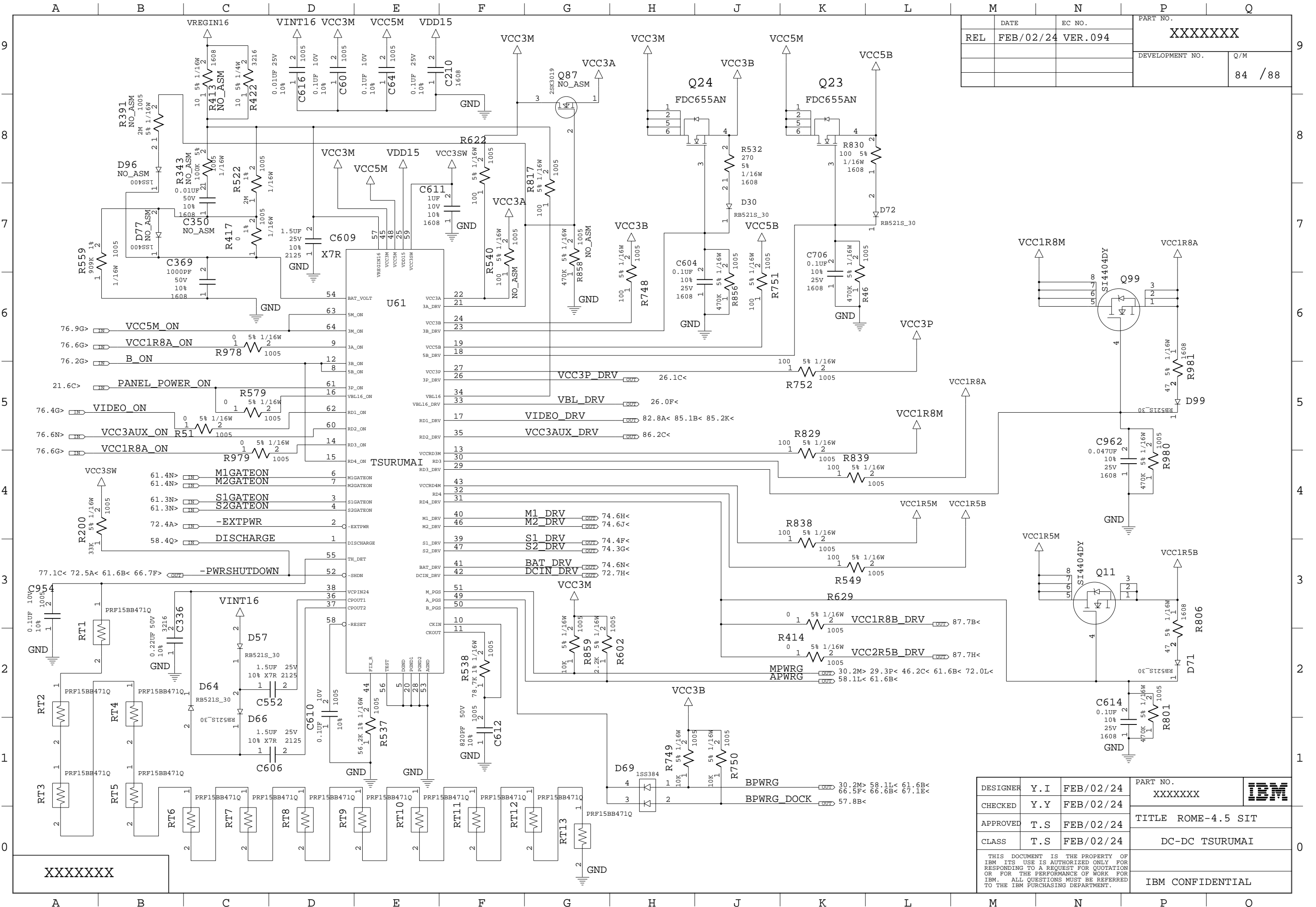
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			DEVELOPMENT NO.	Q/M
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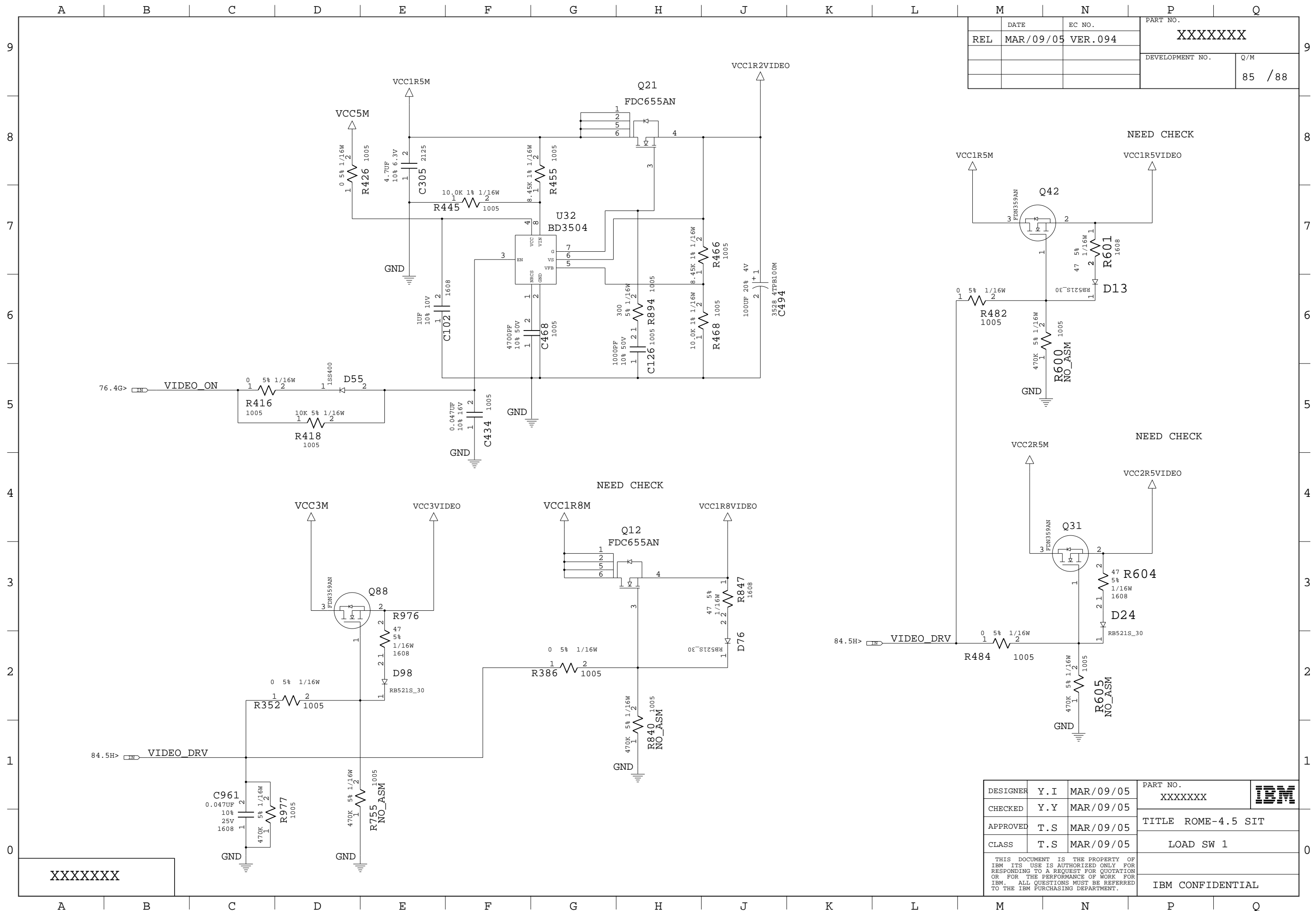
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	FEB/02/24	VER.094	XXXXXXXX
			DEVELOPMENT NO.
			Q/M
			84 / 88

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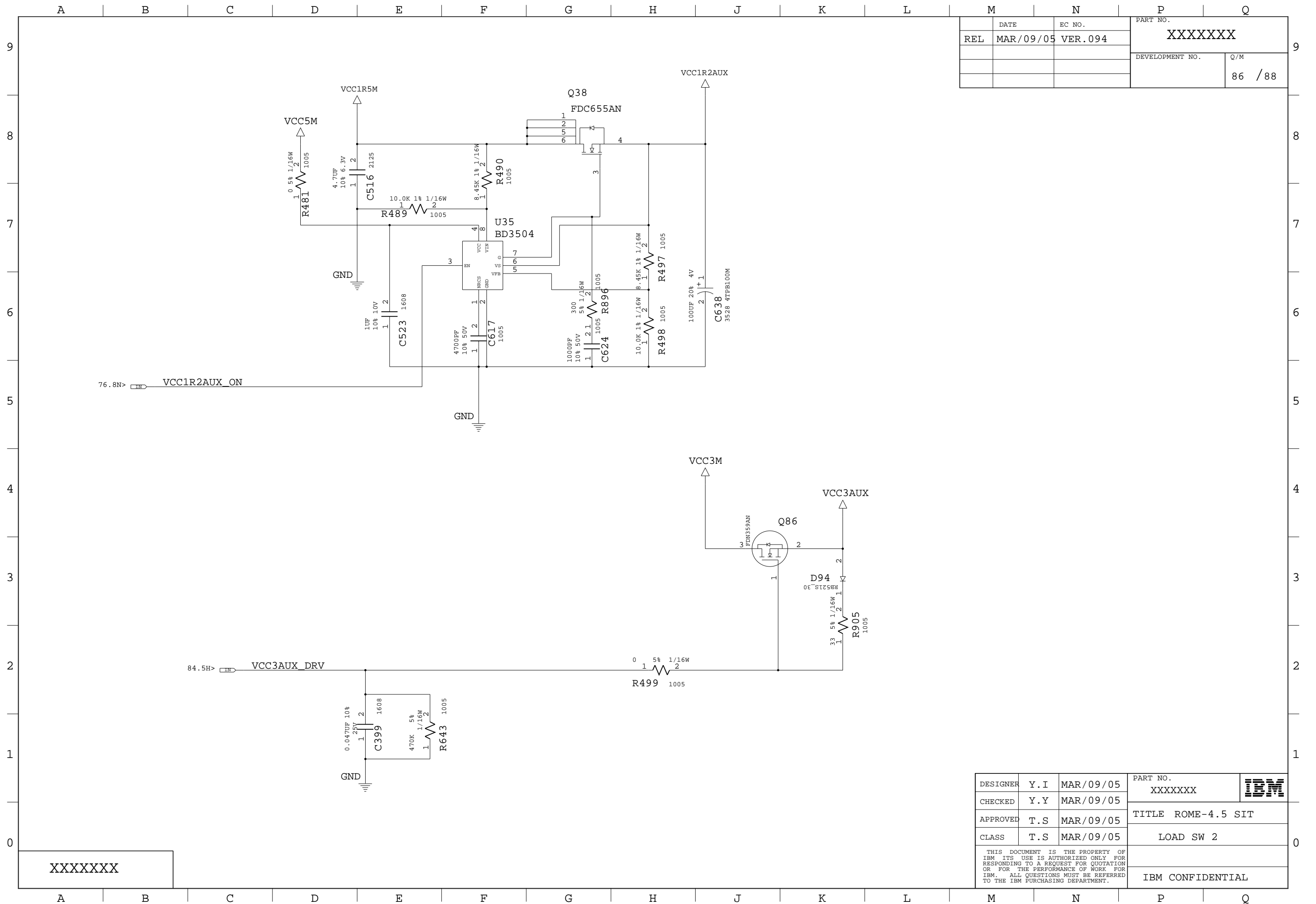
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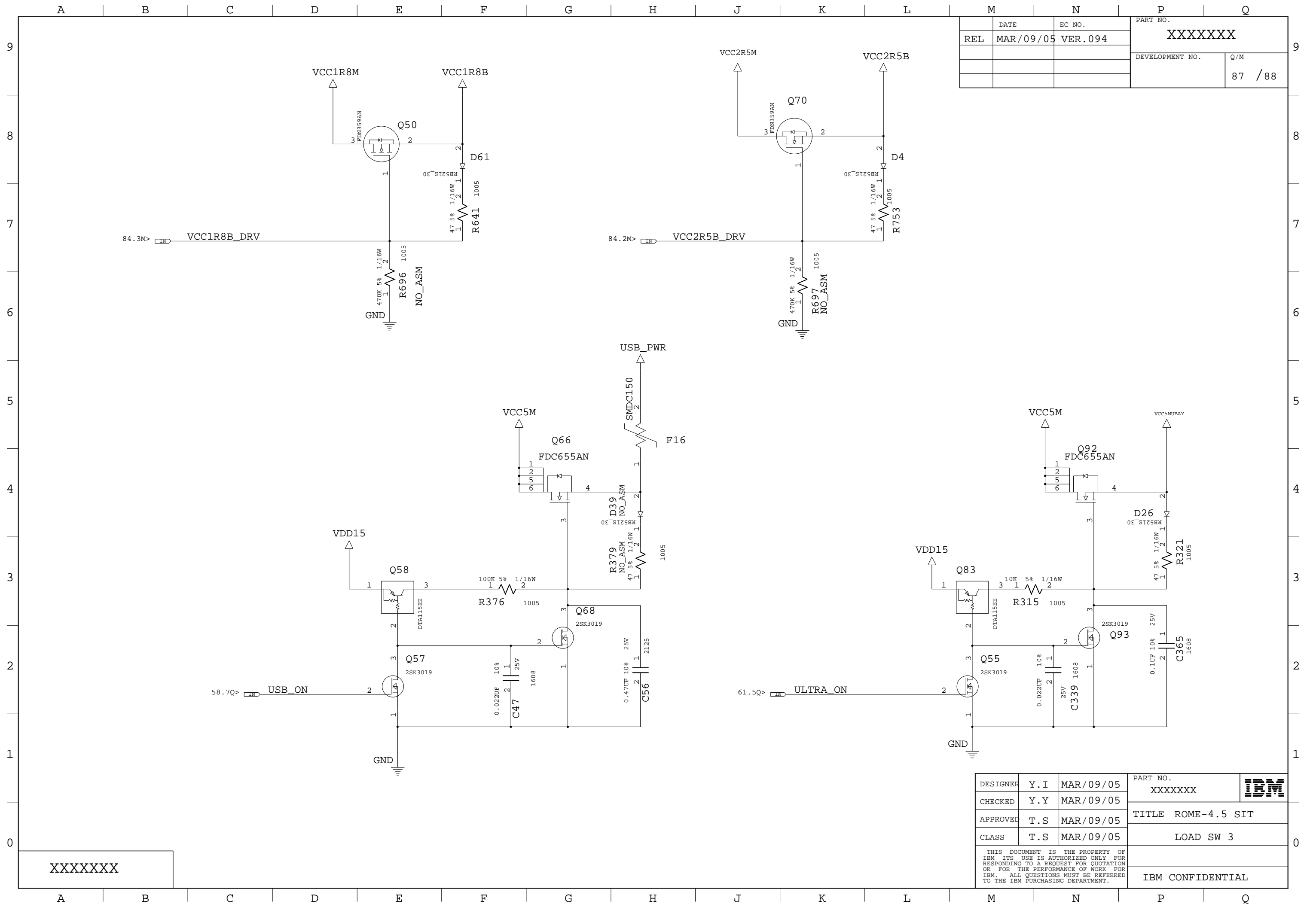


DATE	EC NO.	PART NO.	
MAR/09/05	VER.094	XXXXXXXX	
		DEVELOPMENT NO.	Q/M
			85 / 88

DESIGNER	Y.I	MAR/09/05	PART NO.	XXXXXXXX	IBM
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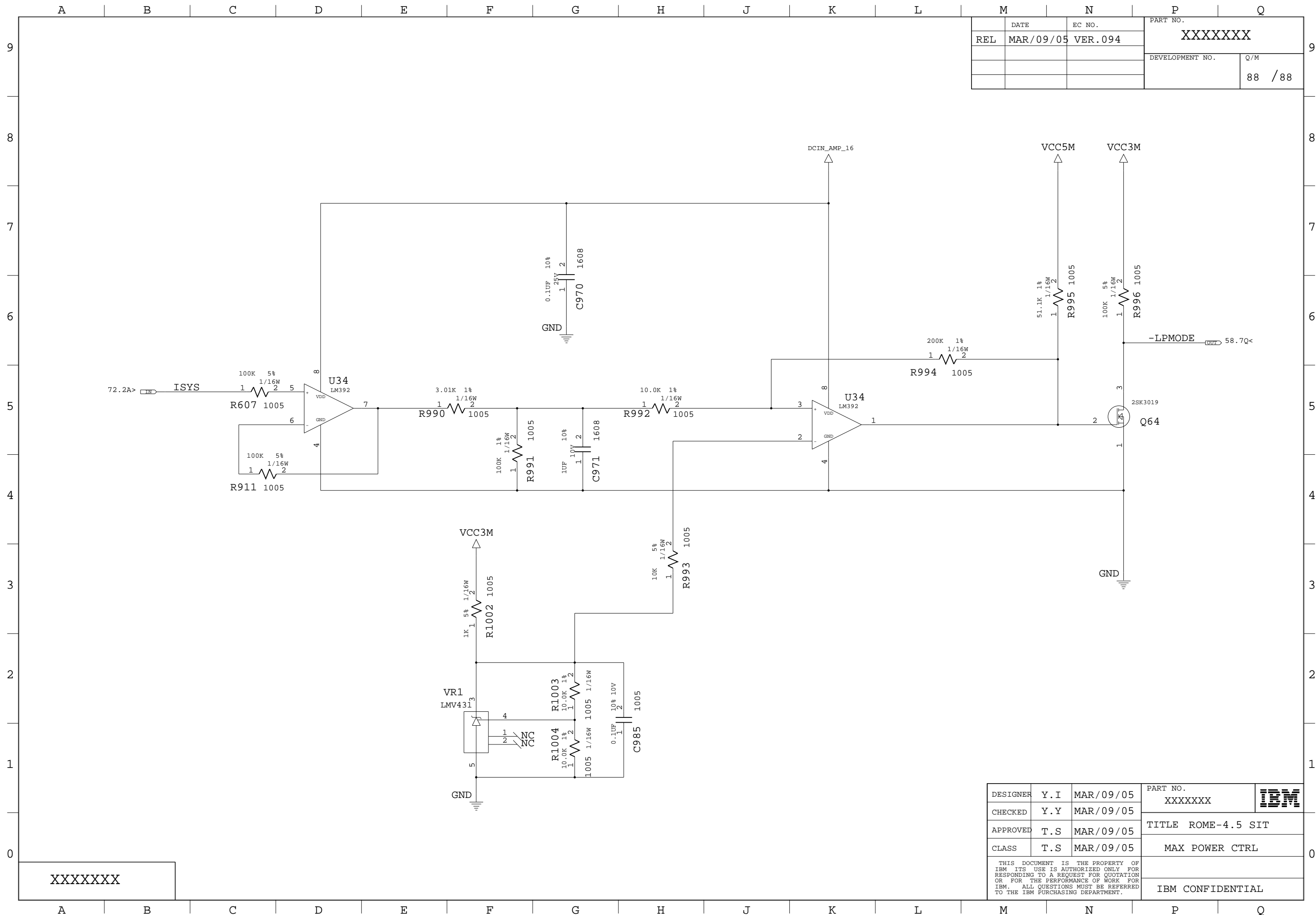




	DATE	EC NO.	PART NO.	
REL	MAR/09/05	VER.094	XXXXXXXX	
			DEVELOPMENT NO.	Q/M
				87 / 88

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			DEVELOPMENT NO. 88 / 88
			Q/M

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