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& HP & SPK)	2.0	08/24				
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P. Leader <i>廖育凱</i> 8/22/06	Check by <i>陳世祥</i> 8/22/06	Design by <i>劉新鈞</i> 8/22/06
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Schematics Subject: **MS70 Main Board** PCB P/N: **(FUBAI) 1P-0068100-6011**
(NAN YA) 1P-0068200-6011
(HANSTAR) 1P-0068500-6011

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

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28	Flash ROM/X-Bus	2.0	08/24				
29	LED/Touch PAD	2.0	08/24				
30	Mini-PCIE Card	2.0	08/24				
31	FAN	2.0	08/24				
32	OIDE	2.0	08/24				
33	AUDIO(CODEC & POWER)	2.0	08/24				
34	AUDIO(AMP & HP & SPK)	2.0	08/24				
35	AUDIO(EXTMIC)	2.0	08/24				

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P. Leader	Check by	Design by

Project Code & Schematics Subject: MS70 Main Board PCB P/N: (FUBAI) 1P-0068100-6011
 (NAN YA) 1P-0068200-6011
 (HANSTAR) 1P-0068500-6011

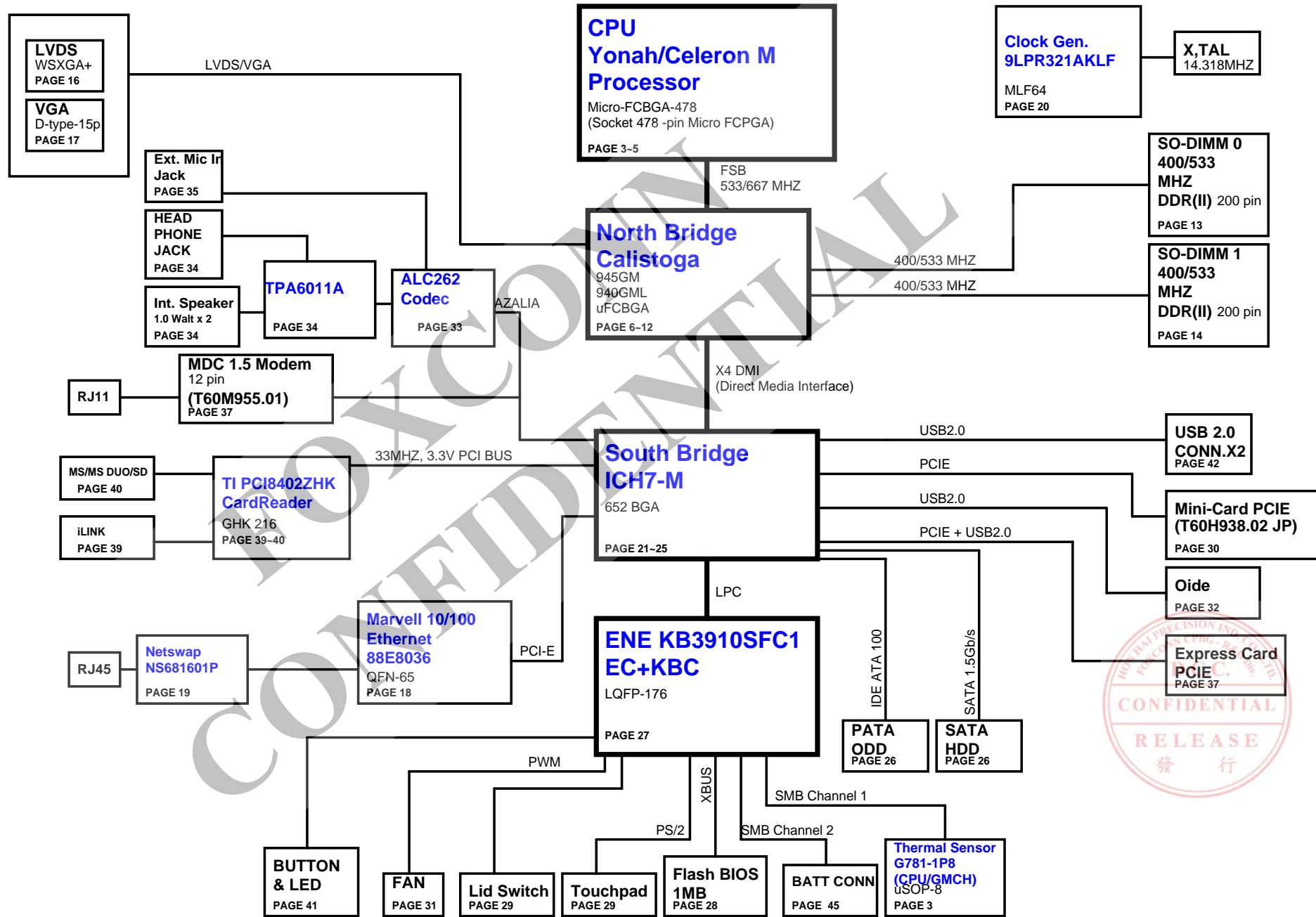
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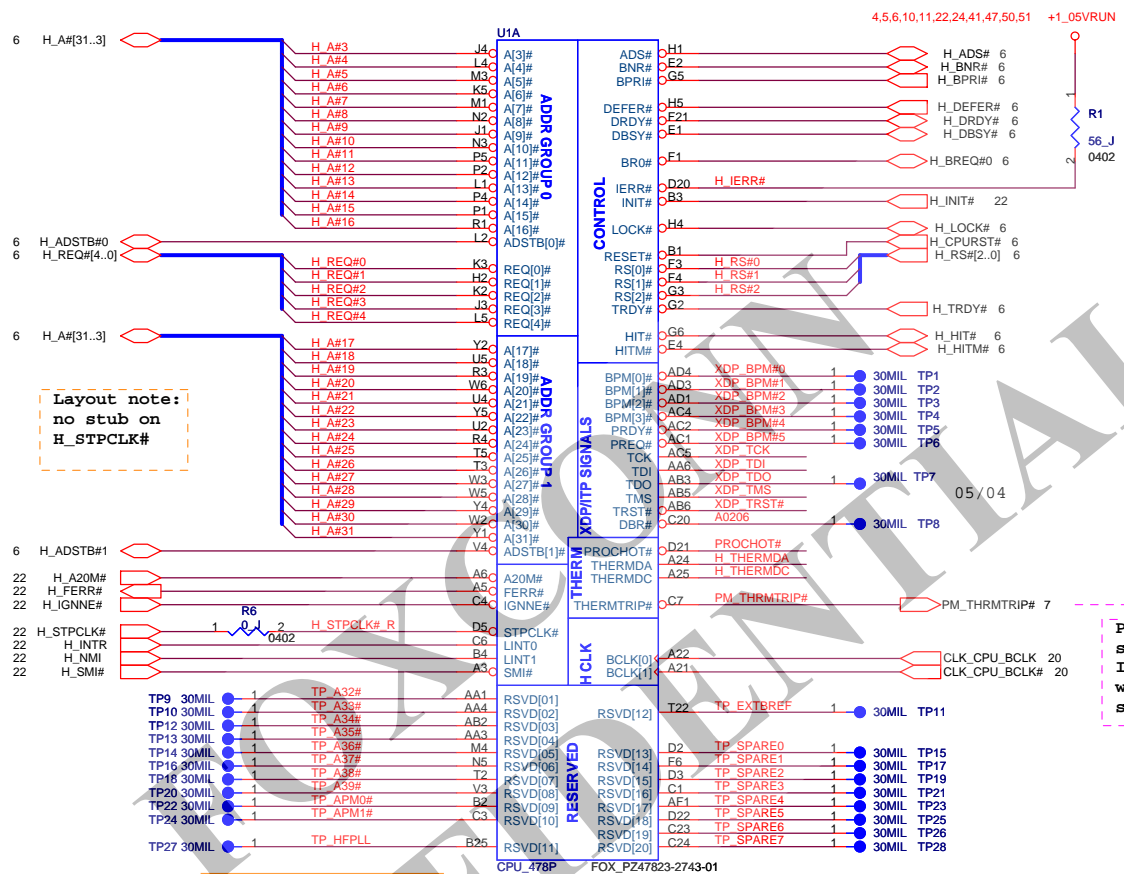
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RAPTOR/MS70(CALISTOGA GM/GML Block Diagram)

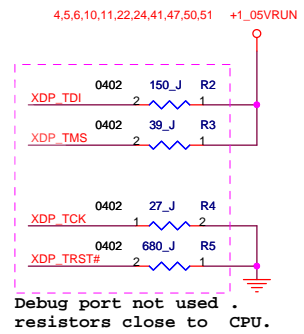




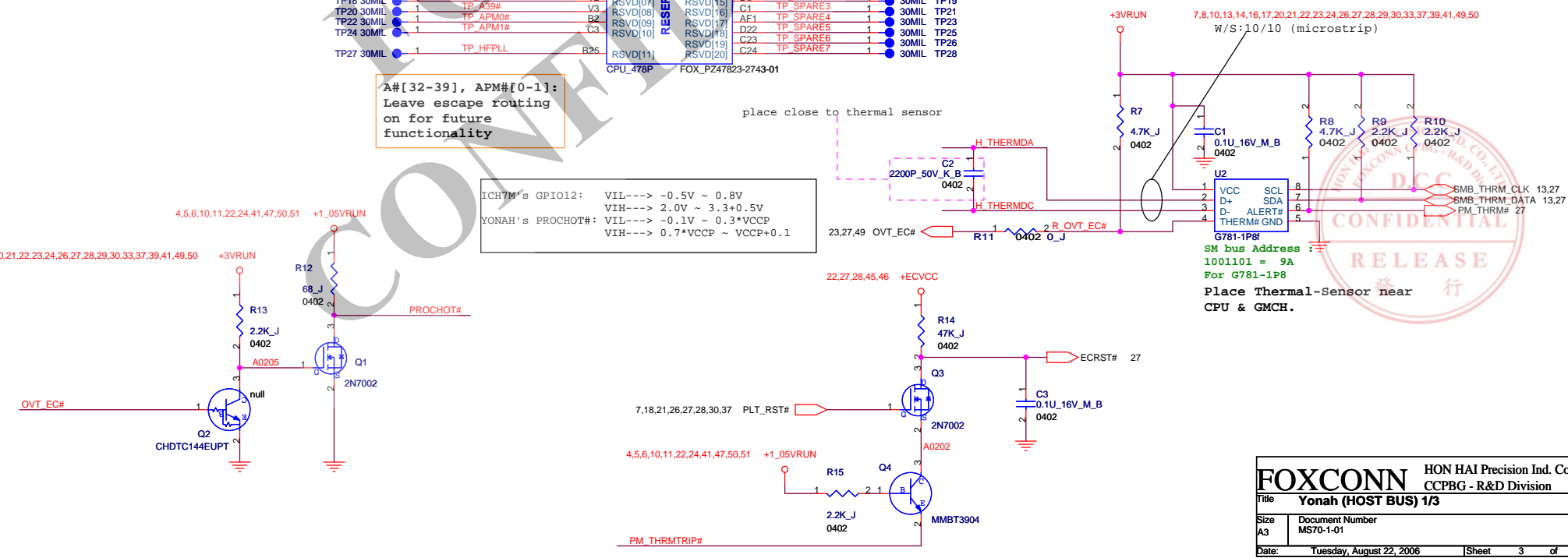
Layout note:
no stub on
H_STPCLK#

A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

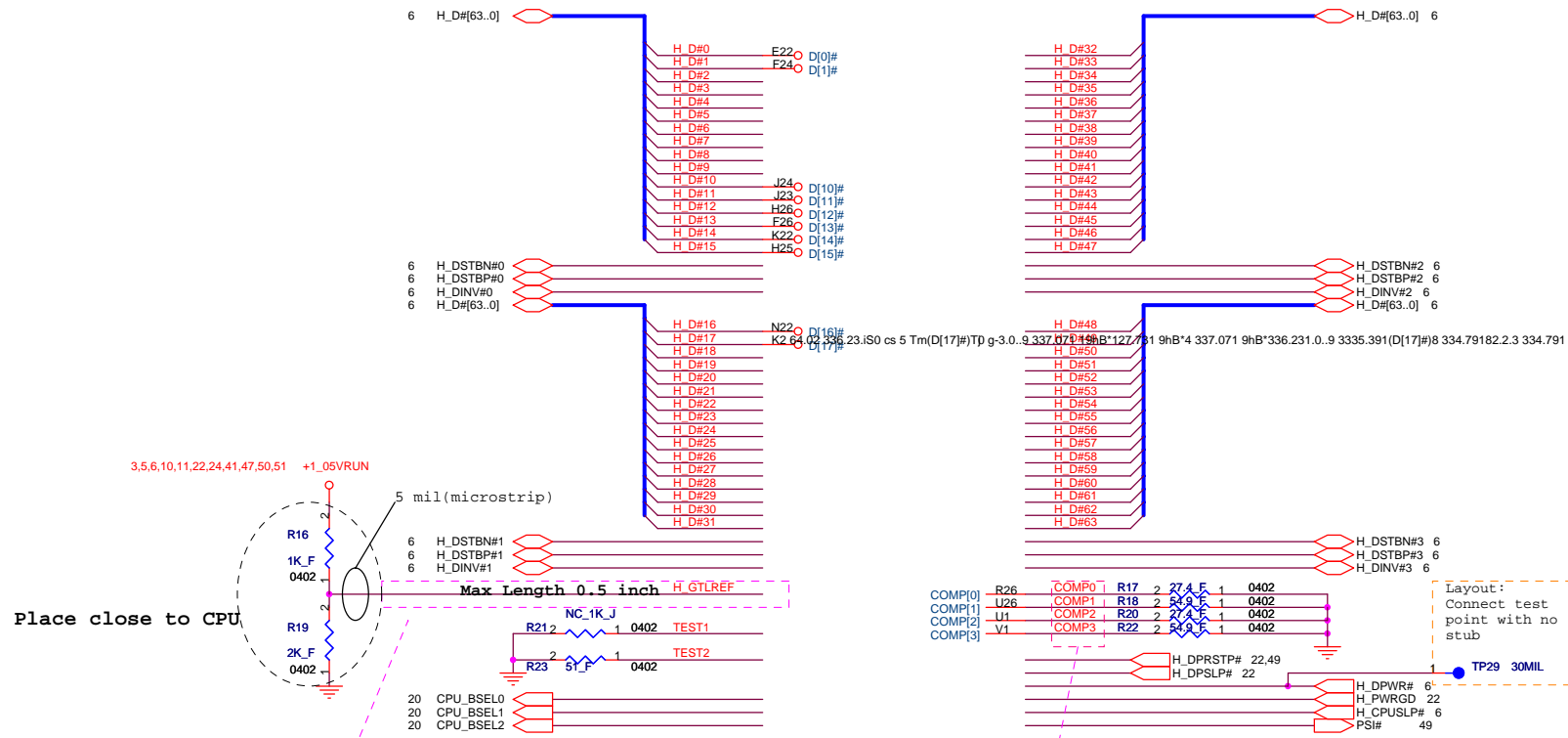
ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1



PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)



SM bus Address :
1001101 = 9A
For G781-1P8
Place Thermal-Sensor near
CPU & GMCH.

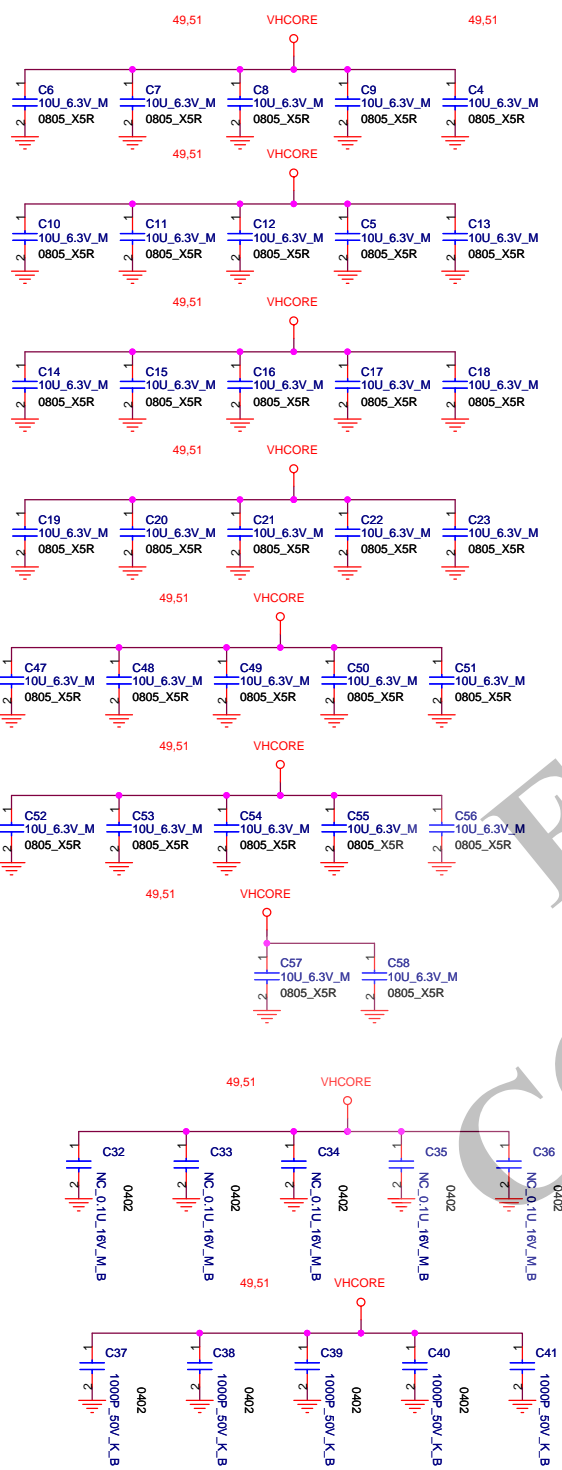


Place close to CPU

Layout Note:
 Zo=55 ohm, 0.5"
 max for GTLREF.

Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make
 trace length shorter then 0.5".
 Comp1,3 connect with Zo=55 ohm, make
 trace length shorter then 0.5".

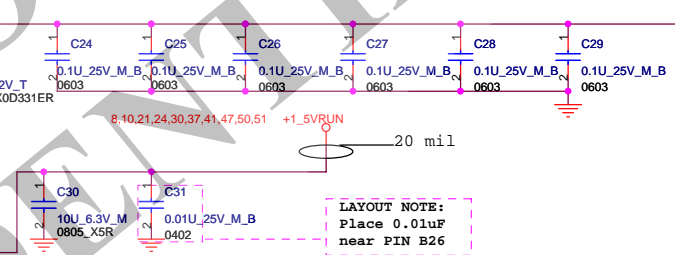
IMVP6 (max8736)
 cpu PSI# <-> max8736 PSI#
 max8736: VIHmin=0.67V
 VILmax=0.33V
 (ref. max8736 datasheet)



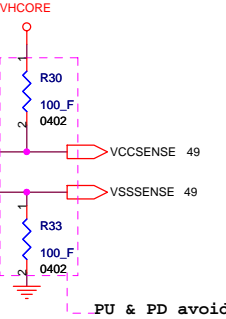
U1C

A7	VCC[001]	AB20
A9	VCC[002]	AB7
A10	VCC[003]	AC7
A12	VCC[070]	AC9
A13	VCC[004]	AC12
A15	VCC[005]	AC13
A17	VCC[006]	AC15
A18	VCC[007]	AC17
A20	VCC[008]	AC18
B7	VCC[009]	AD7
B9	VCC[010]	AD9
B10	VCC[011]	AD10
B12	VCC[012]	AD12
B14	VCC[013]	AD13
B15	VCC[014]	AD14
B17	VCC[015]	AD15
B18	VCC[016]	AD17
B20	VCC[017]	AD18
C9	VCC[018]	AE9
C10	VCC[019]	AE10
C12	VCC[021]	AE13
C13	VCC[022]	AE15
C15	VCC[023]	AE17
C17	VCC[024]	AE18
C18	VCC[025]	AE20
D9	VCC[026]	AF9
D10	VCC[027]	AF10
D12	VCC[028]	AF12
D14	VCC[029]	AF14
D15	VCC[030]	AF15
D17	VCC[031]	AF17
D18	VCC[032]	AF18
E7	VCC[033]	AF20
E9	VCC[034]	AF20
F10	VCC[035]	AG21
F12	VCC[036]	AG21
F13	VCC[037]	AG21
F15	VCC[038]	AG21
F17	VCC[039]	AG21
F18	VCC[040]	AG21
E20	VCC[041]	AG21
F7	VCC[042]	AG21
F9	VCC[043]	AG21
F10	VCC[044]	AG21
F12	VCC[045]	AG21
F14	VCC[046]	AG21
F15	VCC[047]	AG21
F18	VCC[048]	AG21
F20	VCC[049]	AG21
AA7	VCC[050]	AG21
AA9	VCC[051]	AG21
AA10	VCC[052]	AG21
AA12	VCC[053]	AG21
AA13	VCC[054]	AG21
AA15	VCC[055]	AG21
AA17	VCC[056]	AG21
AA18	VCC[057]	AG21
AA20	VCC[058]	AG21
AB9	VCC[059]	AG21
AC10	VCC[060]	AG21
AB10	VCC[061]	AG21
AB12	VCC[062]	AG21
AB14	VCC[063]	AG21
AB15	VCC[064]	AG21
AB17	VCC[065]	AG21
AB18	VCC[066]	AG21
AB18	VCC[067]	AG21

CPU_VCCA---->120mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A

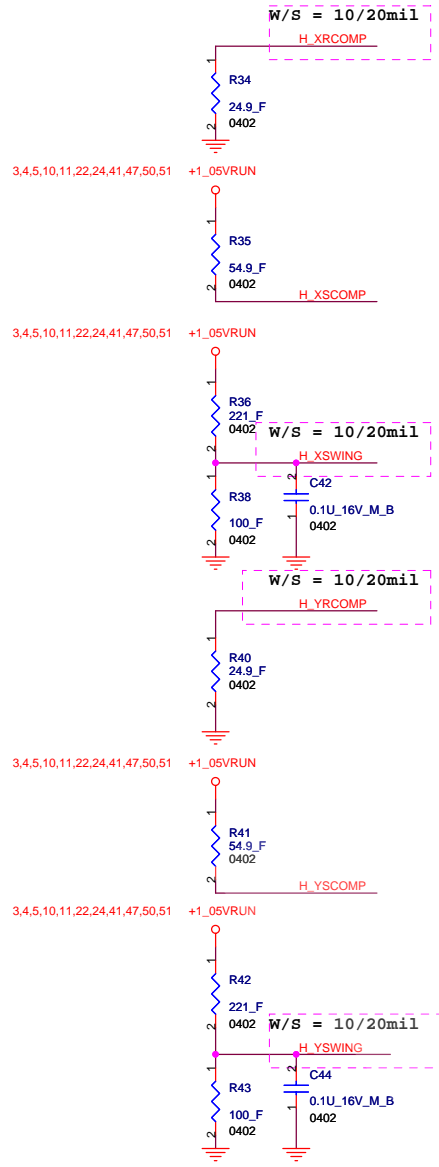


Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
 width=18 mil
 spacing=7 mil



U1D

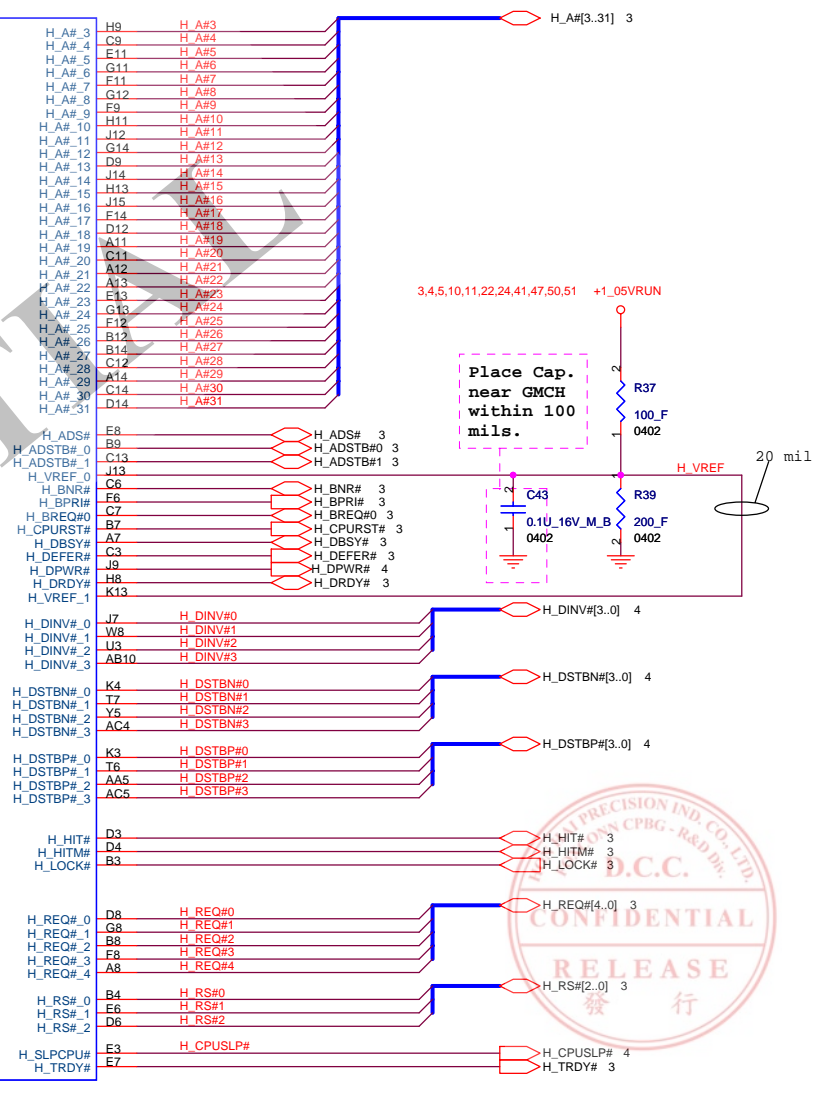
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
A26	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B16	VSS[012]	VSS[093]	U6
B19	VSS[013]	VSS[094]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C22	VSS[023]	VSS[104]	W26
C25	VSS[024]	VSS[105]	Y2
D1	VSS[025]	VSS[106]	Y6
D4	VSS[026]	VSS[107]	Y21
D8	VSS[027]	VSS[108]	Y24
D9	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA9
D19	VSS[031]	VSS[112]	AA11
D23	VSS[032]	VSS[113]	AA14
D26	VSS[033]	VSS[114]	AA16
E3	VSS[034]	VSS[115]	AA19
E6	VSS[035]	VSS[116]	AA22
E8	VSS[036]	VSS[117]	AA25
E11	VSS[037]	VSS[118]	AB1
E14	VSS[038]	VSS[119]	AB4
E16	VSS[039]	VSS[120]	AB8
E19	VSS[040]	VSS[121]	AB11
E21	VSS[041]	VSS[122]	AB13
E24	VSS[042]	VSS[123]	AB16
F2	VSS[043]	VSS[124]	AB19
F8	VSS[044]	VSS[125]	AB23
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC8
F19	VSS[048]	VSS[129]	AC11
F22	VSS[049]	VSS[130]	AC14
F25	VSS[050]	VSS[131]	AC16
G4	VSS[051]	VSS[132]	AC19
G1	VSS[052]	VSS[133]	AC21
G23	VSS[053]	VSS[134]	AC24
G26	VSS[054]	VSS[135]	AD2
H3	VSS[055]	VSS[136]	AD5
H6	VSS[056]	VSS[137]	AD8
H21	VSS[057]	VSS[138]	AD11
H24	VSS[058]	VSS[139]	AD13
J2	VSS[059]	VSS[140]	AD16
J5	VSS[060]	VSS[141]	AD19
J22	VSS[061]	VSS[142]	AD22
J25	VSS[062]	VSS[143]	AD25
K1	VSS[063]	VSS[144]	AE1
K4	VSS[064]	VSS[145]	AE4
K23	VSS[065]	VSS[146]	AE8
K26	VSS[066]	VSS[147]	AE11
L3	VSS[067]	VSS[148]	AE14
L6	VSS[068]	VSS[149]	AE19
L21	VSS[069]	VSS[150]	AE23
L24	VSS[070]	VSS[151]	AE26
M2	VSS[071]	VSS[152]	AF3
M5	VSS[072]	VSS[153]	AF6
M22	VSS[073]	VSS[154]	AF8
M25	VSS[074]	VSS[155]	AF11
N1	VSS[075]	VSS[156]	AF13
N4	VSS[076]	VSS[157]	AF16
N23	VSS[077]	VSS[158]	AF19
N26	VSS[078]	VSS[159]	AF21
P3	VSS[079]	VSS[160]	AF24
P3	VSS[080]	VSS[161]	AF24
P3	VSS[081]	VSS[162]	AF24



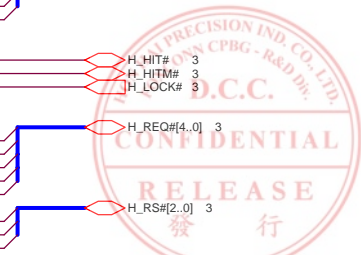
4 H_D#[63..0] H_D#[63..0]

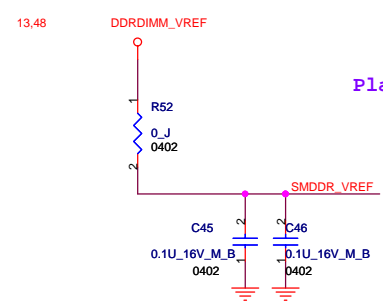
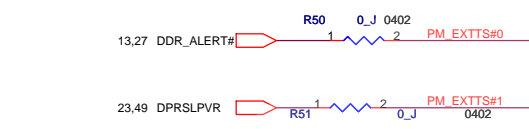
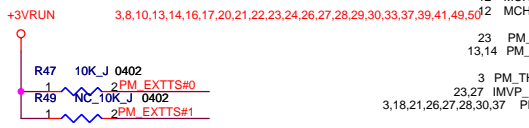
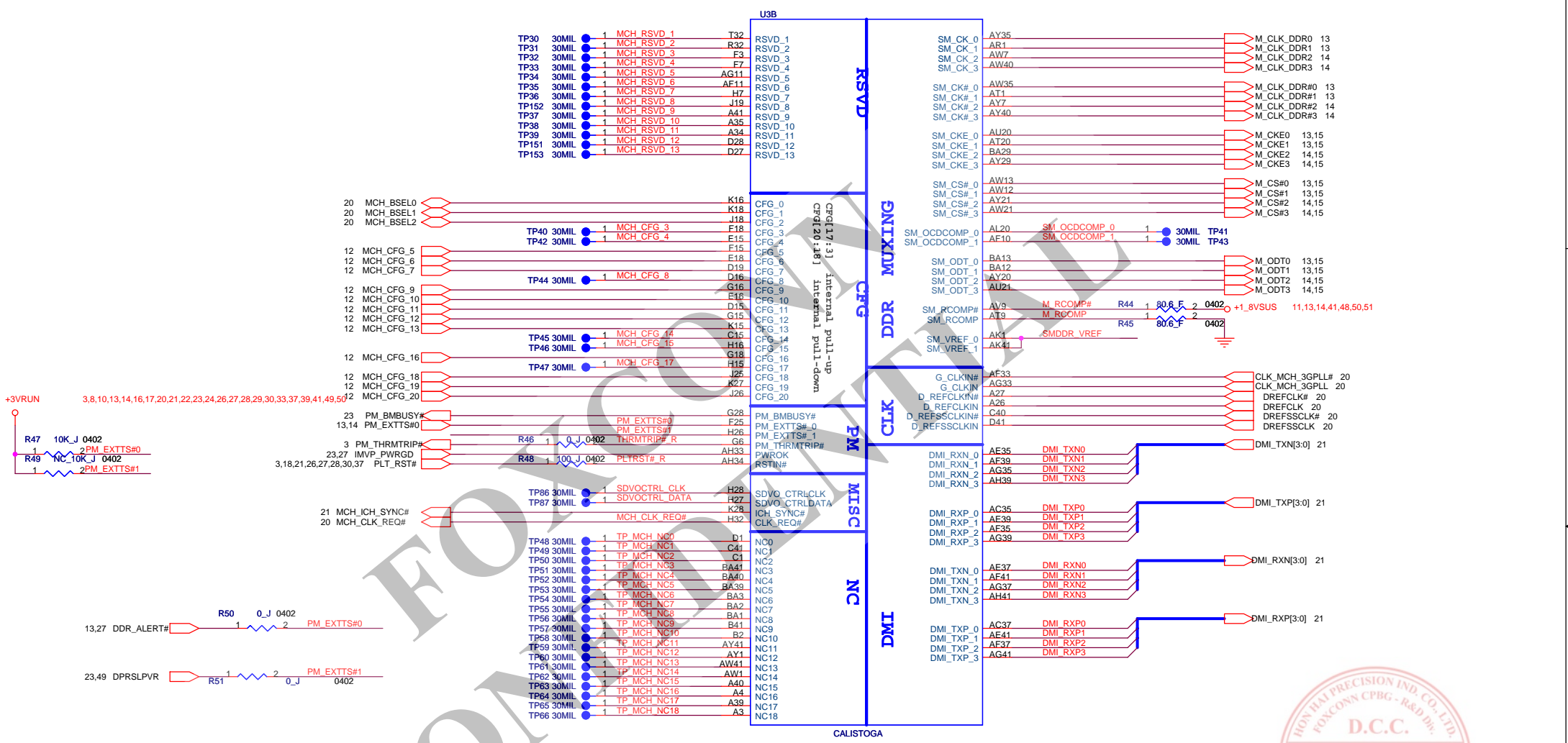
USA		HOST	
H_D#0	F1	H_AD#	3
H_D#1	J1	H_ADSTB#0	3
H_D#2	H1	H_ADSTB#1	3
H_D#3	J6	H_VREF_0	3
H_D#4	H3	H_BNR#	3
H_D#5	K2	H_BPR#	3
H_D#6	G1	H_BREQ#0	3
H_D#7	G2	H_CPURST#	3
H_D#8	K9	H_DBSY#	3
H_D#9	K1	H_DEFER#	3
H_D#10	K7	H_DPWR#	4
H_D#11	J8	H_DRDY#	3
H_D#12	H4	H_DIN#0	4
H_D#13	J3	H_DIN#1	4
H_D#14	K11	H_DIN#2	4
H_D#15	G4	H_DIN#3	4
H_D#16	L10	H_DSTBN#0	4
H_D#17	W11	H_DSTBN#1	4
H_D#18	T3	H_DSTBN#2	4
H_D#19	U7	H_DSTBN#3	4
H_D#20	U8	H_DSTBP#0	4
H_D#21	U11	H_DSTBP#1	4
H_D#22	T11	H_DSTBP#2	4
H_D#23	W9	H_DSTBP#3	4
H_D#24	T1	H_HIT#	3
H_D#25	T8	H_HITM#	3
H_D#26	T4	H_LOCK#	3
H_D#27	W7	H_REQ#0	3
H_D#28	U5	H_REQ#1	3
H_D#29	T9	H_REQ#2	3
H_D#30	W6	H_REQ#3	3
H_D#31	T5	H_REQ#4	3
H_D#32	AB7	H_RS#0	3
H_D#33	AA9	H_RS#1	3
H_D#34	W4	H_RS#2	3
H_D#35	W3	H_CPUSLP#	4
H_D#36	Y8	H_TRDY#	3
H_D#37	Y7		
H_D#38	W5		
H_D#39	Y10		
H_D#40	AB6		
H_D#41	W2		
H_D#42	AA4		
H_D#43	AA7		
H_D#44	AA2		
H_D#45	AA6		
H_D#46	AA10		
H_D#47	Y8		
H_D#48	AA1		
H_D#49	AB4		
H_D#50	AC9		
H_D#51	AB11		
H_D#52	AC11		
H_D#53	AB3		
H_D#54	AC2		
H_D#55	AD1		
H_D#56	AD9		
H_D#57	AC1		
H_D#58	AD7		
H_D#59	AC8		
H_D#60	AB5		
H_D#61	AD10		
H_D#62	AD4		
H_D#63	AC8		
H_D#63	AC8		
H_XRCOMP	E1	H_XRCOMP	E1
H_XSCOMP	E2	H_XSCOMP	E2
H_XSWING	E4	H_XSWING	E4
H_YRCOMP	Y1	H_YRCOMP	Y1
H_YSCOMP	U1	H_YSCOMP	U1
H_YSWING	W1	H_YSWING	W1
	AG2	H_CLKIN	AG2
	AG1	H_CLKIN#	AG1

20 CLK_MCH_BCLK#
20 CLK_MCH_BCLK#



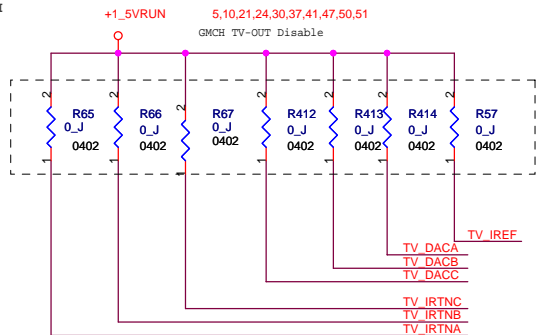
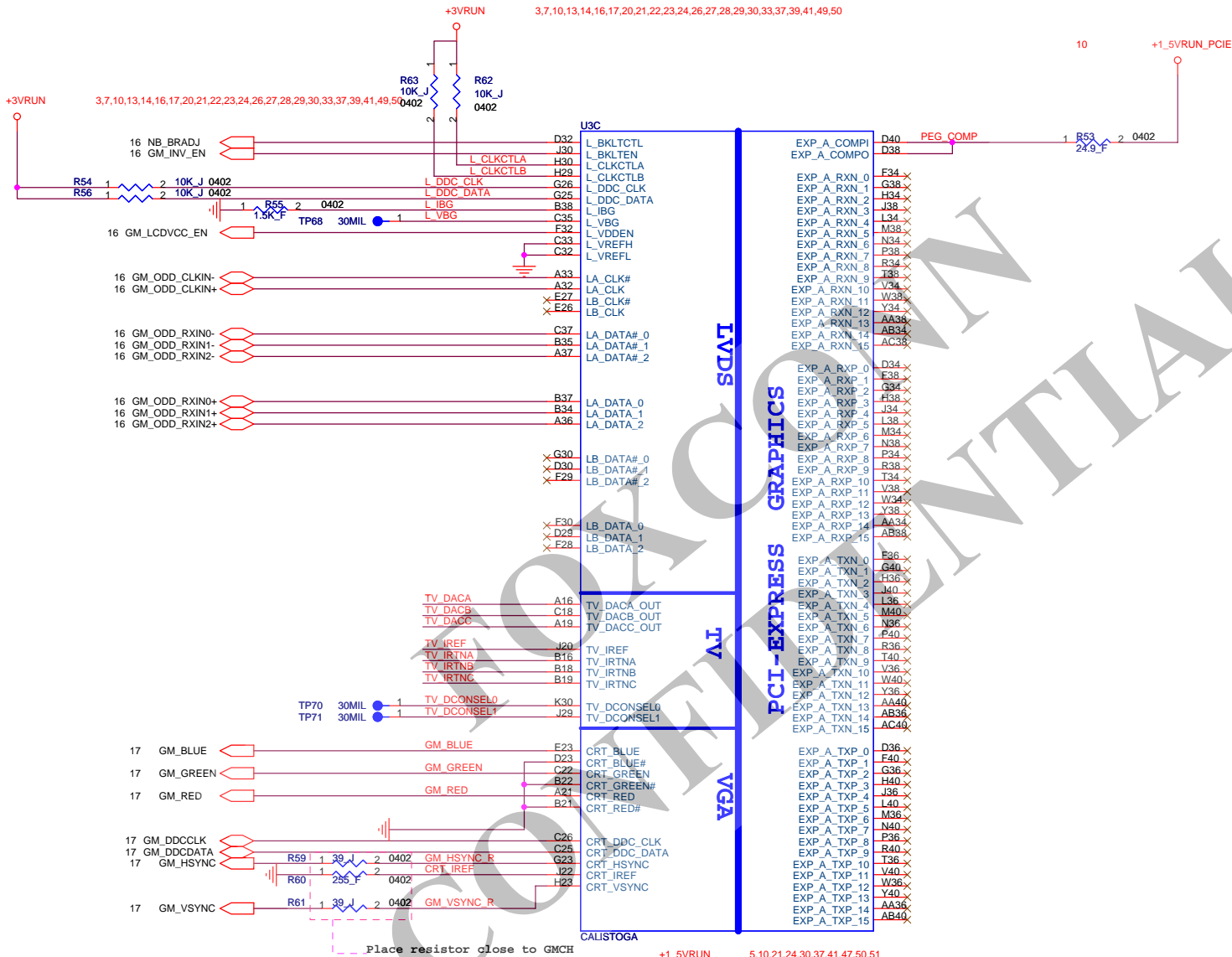
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Place close to chipset





U3C	L_BKLTCTL	EXP_A_COMP1	D40	PEG_COMP	1	R53	24.9_F	0402
	L_BKLTEN	EXP_A_COMP0	D38					
	L_CLKCTLA	EXP_A_RXN_0	F34					
	L_CLKCTLB	EXP_A_RXN_1	G38					
	L_CLKCTLC	EXP_A_RXN_2	H34					
	L_DDC_CLK	EXP_A_RXN_3	J38					
	L_DDC_DATA	EXP_A_RXN_4	K34					
	L_IBG	EXP_A_RXN_5	L34					
	L_IBG	EXP_A_RXN_6	M38					
	L_VBG	EXP_A_RXN_7	N34					
	L_VDDEN	EXP_A_RXN_8	P38					
	L_VREFH	EXP_A_RXN_9	R34					
	L_VREFL	EXP_A_RXN_10	S38					
	LA_CLK#	EXP_A_RXN_11	T34					
	LA_CLK	EXP_A_RXN_12	U38					
	LB_CLK#	EXP_A_RXN_13	V34					
	LB_CLK	EXP_A_RXN_14	W38					
	LA_DATA#_0	EXP_A_RXN_15	X34					
	LA_DATA#_1	EXP_A_RXN_16	AA38					
	LA_DATA#_2	EXP_A_RXN_17	AB34					
	LB_DATA#_0	EXP_A_RXN_18	AC38					
	LB_DATA#_1	EXP_A_RXP_0	D34					
	LB_DATA#_2	EXP_A_RXP_1	E38					
	LB_DATA#_3	EXP_A_RXP_2	F34					
	LB_DATA#_4	EXP_A_RXP_3	G38					
	LB_DATA#_5	EXP_A_RXP_4	H34					
	LB_DATA#_6	EXP_A_RXP_5	J38					
	LB_DATA#_7	EXP_A_RXP_6	K34					
	LB_DATA#_8	EXP_A_RXP_7	L38					
	LB_DATA#_9	EXP_A_RXP_8	M34					
	LB_DATA#_10	EXP_A_RXP_9	N38					
	LB_DATA#_11	EXP_A_RXP_10	P34					
	LB_DATA#_12	EXP_A_RXP_11	R38					
	LB_DATA#_13	EXP_A_RXP_12	S34					
	LB_DATA#_14	EXP_A_RXP_13	T38					
	LB_DATA#_15	EXP_A_RXP_14	U34					
	LB_DATA#_16	EXP_A_RXP_15	V38					
	LA_DATA_0	EXP_A_TXN_0	E36					
	LA_DATA_1	EXP_A_TXN_1	F40					
	LA_DATA_2	EXP_A_TXN_2	G36					
	LA_DATA_3	EXP_A_TXN_3	H40					
	LA_DATA_4	EXP_A_TXN_4	J36					
	LA_DATA_5	EXP_A_TXN_5	K40					
	LA_DATA_6	EXP_A_TXN_6	L36					
	LA_DATA_7	EXP_A_TXN_7	M40					
	LA_DATA_8	EXP_A_TXN_8	N36					
	LA_DATA_9	EXP_A_TXN_9	P40					
	LA_DATA_10	EXP_A_TXN_10	R36					
	LA_DATA_11	EXP_A_TXN_11	S40					
	LA_DATA_12	EXP_A_TXN_12	T36					
	LA_DATA_13	EXP_A_TXN_13	U40					
	LA_DATA_14	EXP_A_TXN_14	V36					
	LA_DATA_15	EXP_A_TXN_15	W40					
	TV_DACA_OUT	EXP_A_TXP_0	D36					
	TV_DACS_OUT	EXP_A_TXP_1	F40					
	TV_DACC_OUT	EXP_A_TXP_2	G36					
	TV_IRTNA	EXP_A_TXP_3	H40					
	TV_IRTNB	EXP_A_TXP_4	J36					
	TV_IRTNC	EXP_A_TXP_5	K40					
	TV_DCONSEL0	EXP_A_TXP_6	L40					
	TV_DCONSEL1	EXP_A_TXP_7	M36					
	CRT_BLUE	EXP_A_TXP_8	N40					
	CRT_BLUE#	EXP_A_TXP_9	P36					
	CRT_GREEN	EXP_A_TXP_10	R40					
	CRT_GREEN#	EXP_A_TXP_11	S40					
	CRT_RED	EXP_A_TXP_12	T36					
	CRT_RED#	EXP_A_TXP_13	U40					
	CRT_HS	EXP_A_TXP_14	V36					
	CRT_VS	EXP_A_TXP_15	W40					
	CRT_IR							
	CRT_IREF							



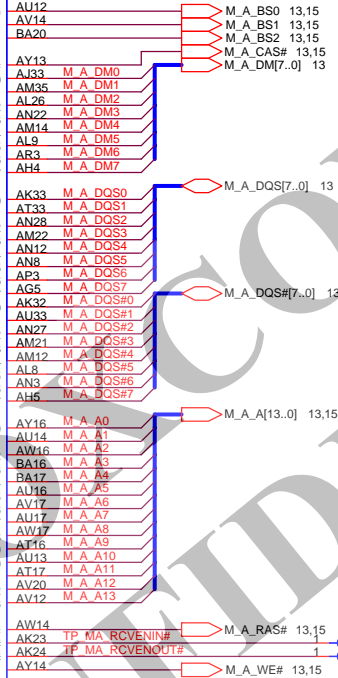
13 M_A_DQ[63.0]

M A DQ0	AJ35	SA_DQ0
M A DQ1	AJ34	SA_DQ1
M A DQ2	AM31	SA_DQ2
M A DQ3	AM33	SA_DQ3
M A DQ4	AJ36	SA_DQ4
M A DQ5	AK35	SA_DQ5
M A DQ6	AJ32	SA_DQ6
M A DQ7	AK31	SA_DQ7
M A DQ8	AN35	SA_DQ8
M A DQ9	AP33	SA_DQ9
M A DQ10	AR31	SA_DQ10
M A DQ11	AP31	SA_DQ11
M A DQ12	AN38	SA_DQ12
M A DQ13	AM36	SA_DQ13
M A DQ14	AM34	SA_DQ14
M A DQ15	AK26	SA_DQ15
M A DQ16	AL27	SA_DQ16
M A DQ17	AL28	SA_DQ17
M A DQ18	AM26	SA_DQ18
M A DQ19	AN24	SA_DQ19
M A DQ20	AK28	SA_DQ20
M A DQ21	AL28	SA_DQ21
M A DQ22	AM24	SA_DQ22
M A DQ23	AP26	SA_DQ23
M A DQ24	AP23	SA_DQ24
M A DQ25	AL22	SA_DQ25
M A DQ26	AP21	SA_DQ26
M A DQ27	AV20	SA_DQ27
M A DQ28	AL23	SA_DQ28
M A DQ29	AP24	SA_DQ29
M A DQ30	AP20	SA_DQ30
M A DQ31	AT21	SA_DQ31
M A DQ32	AR12	SA_DQ32
M A DQ33	AR14	SA_DQ33
M A DQ34	AP13	SA_DQ34
M A DQ35	AP12	SA_DQ35
M A DQ36	AT13	SA_DQ36
M A DQ37	AT12	SA_DQ37
M A DQ38	AL14	SA_DQ38
M A DQ39	AL12	SA_DQ39
M A DQ40	AK9	SA_DQ40
M A DQ41	AN7	SA_DQ41
M A DQ42	AK8	SA_DQ42
M A DQ43	AK7	SA_DQ43
M A DQ44	AP9	SA_DQ44
M A DQ45	AN9	SA_DQ45
M A DQ46	AT5	SA_DQ46
M A DQ47	AY2	SA_DQ47
M A DQ48	AW2	SA_DQ48
M A DQ49	AP1	SA_DQ49
M A DQ50	AN2	SA_DQ50
M A DQ51	AV2	SA_DQ51
M A DQ52	AT3	SA_DQ52
M A DQ53	AN1	SA_DQ53
M A DQ54	AL2	SA_DQ54
M A DQ55	AG7	SA_DQ55
M A DQ56	AF9	SA_DQ56
M A DQ57	AG4	SA_DQ57
M A DQ58	AF6	SA_DQ58
M A DQ59	AG9	SA_DQ59
M A DQ60	AH6	SA_DQ60
M A DQ61	AF4	SA_DQ61
M A DQ62	AF4	SA_DQ62
M A DQ63	AF8	SA_DQ63

U3D

DDR SYSTEM MEMORY A

SA_BS_0	AU12
SA_BS_1	AV14
SA_BS_2	BA20
SA_CAS#	AY13
SA_DM_0	AJ33 M A DM0
SA_DM_1	AM35 M A DM1
SA_DM_2	AL26 M A DM2
SA_DM_3	AM22 M A DM3
SA_DM_4	AM14 M A DM4
SA_DM_5	AL9 M A DM5
SA_DM_6	AR3 M A DM6
SA_DM_7	AH4 M A DM7
SA_DQS_0	AK33 M A DQS0
SA_DQS_1	AT33 M A DQS1
SA_DQS_2	AN28 M A DQS2
SA_DQS_3	AM22 M A DQS3
SA_DQS_4	AN12 M A DQS4
SA_DQS_5	AN8 M A DQS5
SA_DQS_6	AP3 M A DQS6
SA_DQS_7	AK32 M A DQS#0
SA_DQS#_0	AU33 M A DQS#1
SA_DQS#_1	AN27 M A DQS#2
SA_DQS#_2	AM21 M A DQS#3
SA_DQS#_3	AM12 M A DQS#4
SA_DQS#_4	AL8 M A DQS#5
SA_DQS#_5	AN3 M A DQS#6
SA_DQS#_6	AH5 M A DQS#7
SA_DQS#_7	
SA_MA_0	AY16 M A A0
SA_MA_1	AU14 M A A1
SA_MA_2	AW15 M A A2
SA_MA_3	BA16 M A A3
SA_MA_4	BA17 M A A4
SA_MA_5	AU16 M A A5
SA_MA_6	AV17 M A A6
SA_MA_7	AU17 M A A7
SA_MA_8	AW17 M A A8
SA_MA_9	AT16 M A A9
SA_MA_10	AU13 M A A10
SA_MA_11	AT17 M A A11
SA_MA_12	AV20 M A A12
SA_MA_13	AV12 M A A13
SA_RAS#	AW14
SA_RCVENIN#	AK23 TP MA RCVENIN#
SA_RCVENOUT#	AK24 TP MA RCVENOUT#
SA_WE#	AY14



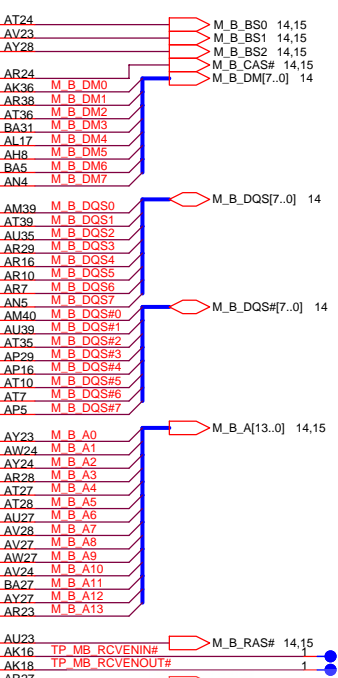
14 M_B_DQ[63.0]

M B DQ0	AK39	SB_DQ0
M B DQ1	AJ37	SB_DQ1
M B DQ2	AP32	SB_DQ2
M B DQ3	AR41	SB_DQ3
M B DQ4	AJ38	SB_DQ4
M B DQ5	AK38	SB_DQ5
M B DQ6	AN41	SB_DQ6
M B DQ7	AP41	SB_DQ7
M B DQ8	AT40	SB_DQ8
M B DQ9	AV41	SB_DQ9
M B DQ10	AU38	SB_DQ10
M B DQ11	AV38	SB_DQ11
M B DQ12	AP38	SB_DQ12
M B DQ13	AR40	SB_DQ13
M B DQ14	AY38	SB_DQ14
M B DQ15	AW38	SB_DQ15
M B DQ16	BA38	SB_DQ16
M B DQ17	AV36	SB_DQ17
M B DQ18	AR36	SB_DQ18
M B DQ19	AP36	SB_DQ19
M B DQ20	AU36	SB_DQ20
M B DQ21	AP35	SB_DQ21
M B DQ22	AP34	SB_DQ22
M B DQ23	AY33	SB_DQ23
M B DQ24	AY33	SB_DQ24
M B DQ25	BA33	SB_DQ25
M B DQ26	AT31	SB_DQ26
M B DQ27	AU29	SB_DQ27
M B DQ28	AU31	SB_DQ28
M B DQ29	AW31	SB_DQ29
M B DQ30	AV29	SB_DQ30
M B DQ31	AW29	SB_DQ31
M B DQ32	AM19	SB_DQ32
M B DQ33	AL19	SB_DQ33
M B DQ34	AP14	SB_DQ34
M B DQ35	AN14	SB_DQ35
M B DQ36	AN17	SB_DQ36
M B DQ37	AM16	SB_DQ37
M B DQ38	AP15	SB_DQ38
M B DQ39	AL15	SB_DQ39
M B DQ40	AJ11	SB_DQ40
M B DQ41	AH10	SB_DQ41
M B DQ42	AJ9	SB_DQ42
M B DQ43	AN10	SB_DQ43
M B DQ44	AK13	SB_DQ44
M B DQ45	AH11	SB_DQ45
M B DQ46	AJ8	SB_DQ46
M B DQ47	AJ8	SB_DQ47
M B DQ48	BA10	SB_DQ48
M B DQ49	AW10	SB_DQ49
M B DQ50	BA4	SB_DQ50
M B DQ51	AW4	SB_DQ51
M B DQ52	AY10	SB_DQ52
M B DQ53	AY9	SB_DQ53
M B DQ54	AW5	SB_DQ54
M B DQ55	AY5	SB_DQ55
M B DQ56	AV4	SB_DQ56
M B DQ57	AR5	SB_DQ57
M B DQ58	AK4	SB_DQ58
M B DQ59	AK3	SB_DQ59
M B DQ60	AT4	SB_DQ60
M B DQ61	AK5	SB_DQ61
M B DQ62	AJ5	SB_DQ62
M B DQ63	AJ3	SB_DQ63

U3E

DDR SYSTEM MEMORY B

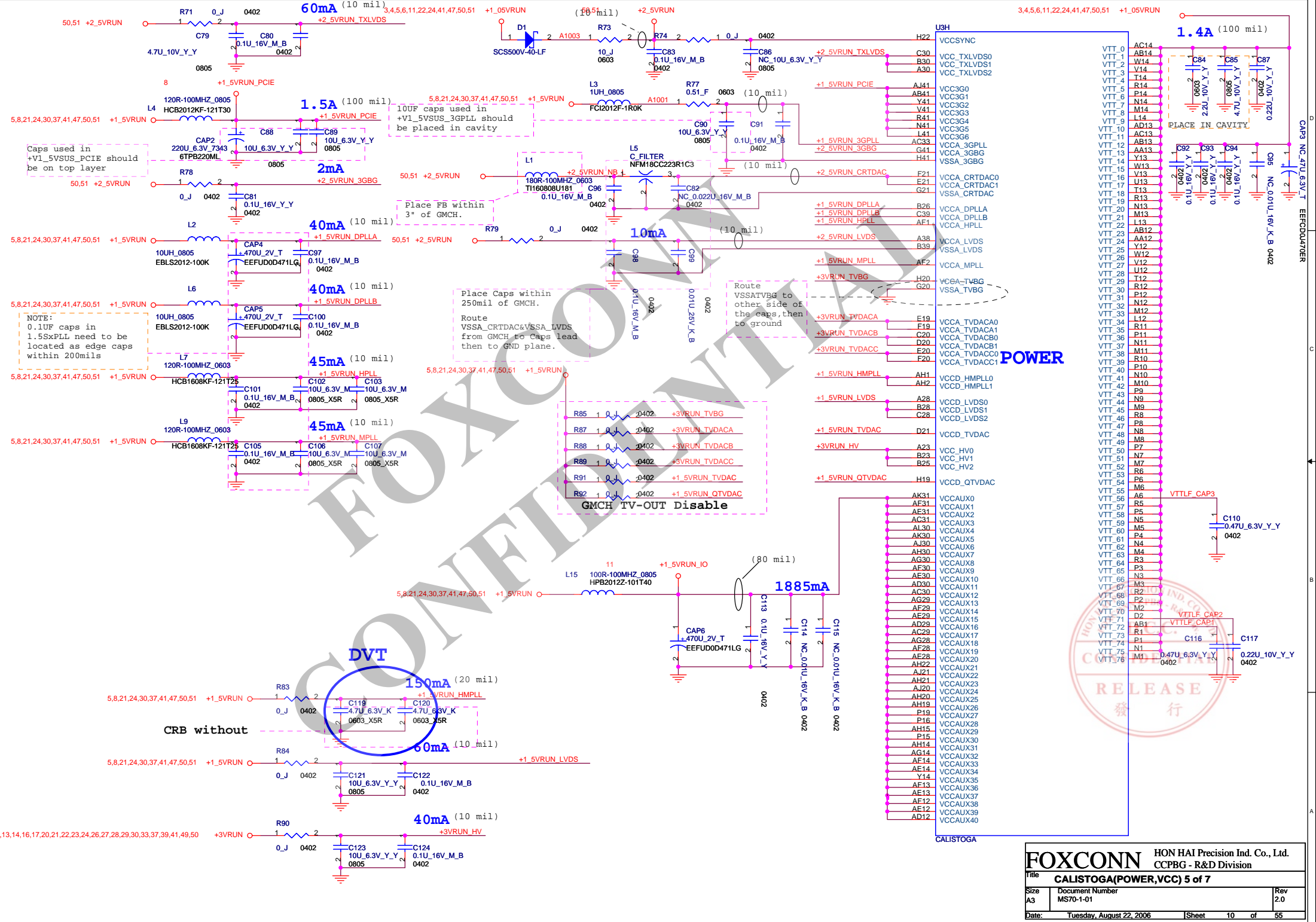
SB_BS_0	AT24
SB_BS_1	AV23
SB_BS_2	AY28
SB_CAS#	AR24
SB_DM_0	AK36 M B DM0
SB_DM_1	AR38 M B DM1
SB_DM_2	AT36 M B DM2
SB_DM_3	BA31 M B DM3
SB_DM_4	AL17 M B DM4
SB_DM_5	AH8 M B DM5
SB_DM_6	BA5 M B DM6
SB_DM_7	AN4 M B DM7
SB_DQS_0	AM39 M B DQS0
SB_DQS_1	AT39 M B DQS1
SB_DQS_2	AU35 M B DQS2
SB_DQS_3	AR29 M B DQS3
SB_DQS_4	AR16 M B DQS4
SB_DQS_5	AR10 M B DQS5
SB_DQS_6	AR7 M B DQS6
SB_DQS_7	AN5 M B DQS7
SB_DQS#_0	AM40 M B DQS#0
SB_DQS#_1	AU39 M B DQS#1
SB_DQS#_2	AT35 M B DQS#2
SB_DQS#_3	AP29 M B DQS#3
SB_DQS#_4	AP16 M B DQS#4
SB_DQS#_5	AT10 M B DQS#5
SB_DQS#_6	AT7 M B DQS#6
SB_DQS#_7	AP5 M B DQS#7
SB_MA_0	AY23 M B A0
SB_MA_1	AW24 M B A1
SB_MA_2	AY24 M B A2
SB_MA_3	AR28 M B A3
SB_MA_4	AT27 M B A4
SB_MA_5	AT28 M B A5
SB_MA_6	AU27 M B A6
SB_MA_7	AV28 M B A7
SB_MA_8	AW27 M B A8
SB_MA_9	AW27 M B A9
SB_MA_10	AV24 M B A10
SB_MA_11	BA27 M B A11
SB_MA_12	AY27 M B A12
SB_MA_13	AR23 M B A13
SB_RAS#	AU23
SB_RCVENIN#	AK16 TP MB RCVENIN#
SB_RCVENOUT#	AK18 TP MB RCVENOUT#
SB_WE#	AR27



CALISTOGA

CALISTOGA





Caps used in +V1_5VSUS_PCIE should be on top layer

NOTE:
0.1uF caps in 1.5SxPLL need to be located as edge caps within 200mils

10uF caps used in +V1_5VSUS_3GPLL should be placed in cavity

Place FB within 3" of GMCH.

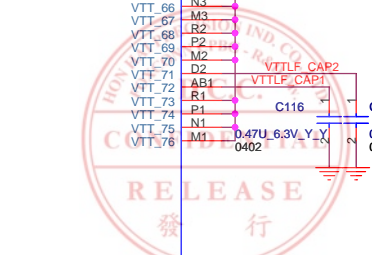
Place Caps within 250mil of GMCH.
Route VSSA_CRTDAC&VSSA_LVDS from GMCH to Caps lead then to GND plane.

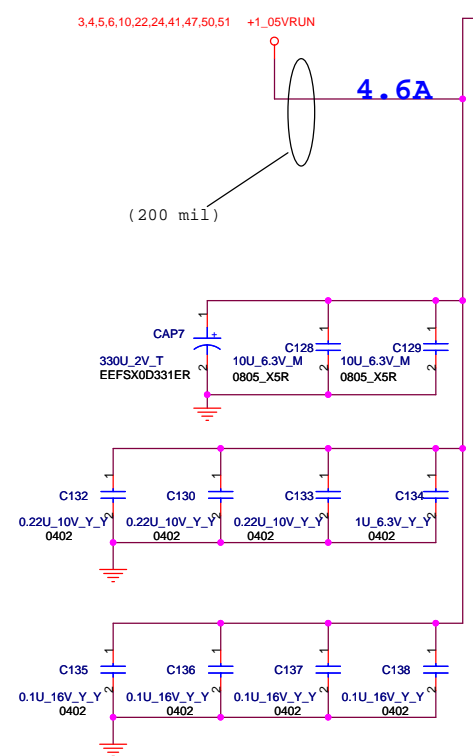
Route VSSATVBG to other side of the caps, then to ground

GMCH TV-OUT Disable

POWER

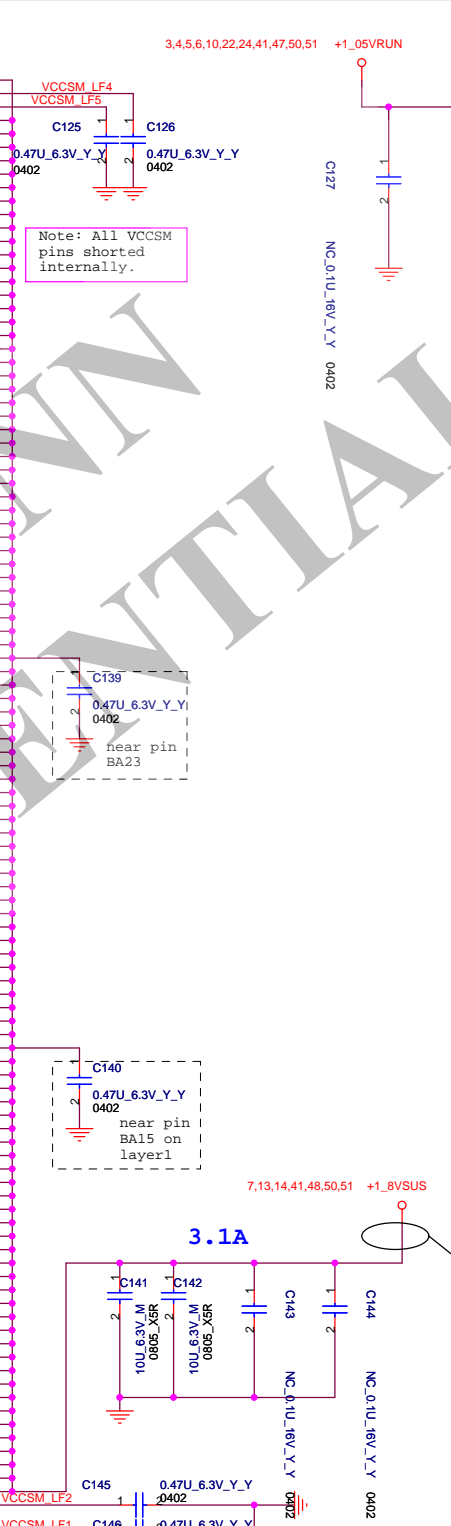
PLACE IN CAVITY





Pin	Signal
VCC_0	VCC_0
VCC_1	VCC_1
VCC_2	VCC_2
VCC_3	VCC_3
VCC_4	VCC_4
VCC_5	VCC_5
VCC_6	VCC_6
VCC_7	VCC_7
VCC_8	VCC_8
VCC_9	VCC_9
VCC_10	VCC_10
VCC_11	VCC_11
VCC_12	VCC_12
VCC_13	VCC_13
VCC_14	VCC_14
VCC_15	VCC_15
VCC_16	VCC_16
VCC_17	VCC_17
VCC_18	VCC_18
VCC_19	VCC_19
VCC_20	VCC_20
VCC_21	VCC_21
VCC_22	VCC_22
VCC_23	VCC_23
VCC_24	VCC_24
VCC_25	VCC_25
VCC_26	VCC_26
VCC_27	VCC_27
VCC_28	VCC_28
VCC_29	VCC_29
VCC_30	VCC_30
VCC_31	VCC_31
VCC_32	VCC_32
VCC_33	VCC_33
VCC_34	VCC_34
VCC_35	VCC_35
VCC_36	VCC_36
VCC_37	VCC_37
VCC_38	VCC_38
VCC_39	VCC_39
VCC_40	VCC_40
VCC_41	VCC_41
VCC_42	VCC_42
VCC_43	VCC_43
VCC_44	VCC_44
VCC_45	VCC_45
VCC_46	VCC_46
VCC_47	VCC_47
VCC_48	VCC_48
VCC_49	VCC_49
VCC_50	VCC_50
VCC_51	VCC_51
VCC_52	VCC_52
VCC_53	VCC_53
VCC_54	VCC_54
VCC_55	VCC_55
VCC_56	VCC_56
VCC_57	VCC_57
VCC_58	VCC_58
VCC_59	VCC_59
VCC_60	VCC_60
VCC_61	VCC_61
VCC_62	VCC_62
VCC_63	VCC_63
VCC_64	VCC_64
VCC_65	VCC_65
VCC_66	VCC_66
VCC_67	VCC_67
VCC_68	VCC_68
VCC_69	VCC_69
VCC_70	VCC_70
VCC_71	VCC_71
VCC_72	VCC_72
VCC_73	VCC_73
VCC_74	VCC_74
VCC_75	VCC_75
VCC_76	VCC_76
VCC_77	VCC_77
VCC_78	VCC_78
VCC_79	VCC_79
VCC_80	VCC_80
VCC_81	VCC_81
VCC_82	VCC_82
VCC_83	VCC_83
VCC_84	VCC_84
VCC_85	VCC_85
VCC_86	VCC_86
VCC_87	VCC_87
VCC_88	VCC_88
VCC_89	VCC_89
VCC_90	VCC_90
VCC_91	VCC_91
VCC_92	VCC_92
VCC_93	VCC_93
VCC_94	VCC_94
VCC_95	VCC_95
VCC_96	VCC_96
VCC_97	VCC_97
VCC_98	VCC_98
VCC_99	VCC_99
VCC_100	VCC_100
VCC_101	VCC_101
VCC_102	VCC_102
VCC_103	VCC_103
VCC_104	VCC_104
VCC_105	VCC_105
VCC_106	VCC_106
VCC_107	VCC_107
VCC_108	VCC_108
VCC_109	VCC_109
VCC_110	VCC_110

Pin	Signal
VCC_SM_0	VCC_SM_0
VCC_SM_1	VCC_SM_1
VCC_SM_2	VCC_SM_2
VCC_SM_3	VCC_SM_3
VCC_SM_4	VCC_SM_4
VCC_SM_5	VCC_SM_5
VCC_SM_6	VCC_SM_6
VCC_SM_7	VCC_SM_7
VCC_SM_8	VCC_SM_8
VCC_SM_9	VCC_SM_9
VCC_SM_10	VCC_SM_10
VCC_SM_11	VCC_SM_11
VCC_SM_12	VCC_SM_12
VCC_SM_13	VCC_SM_13
VCC_SM_14	VCC_SM_14
VCC_SM_15	VCC_SM_15
VCC_SM_16	VCC_SM_16
VCC_SM_17	VCC_SM_17
VCC_SM_18	VCC_SM_18
VCC_SM_19	VCC_SM_19
VCC_SM_20	VCC_SM_20
VCC_SM_21	VCC_SM_21
VCC_SM_22	VCC_SM_22
VCC_SM_23	VCC_SM_23
VCC_SM_24	VCC_SM_24
VCC_SM_25	VCC_SM_25
VCC_SM_26	VCC_SM_26
VCC_SM_27	VCC_SM_27
VCC_SM_28	VCC_SM_28
VCC_SM_29	VCC_SM_29
VCC_SM_30	VCC_SM_30
VCC_SM_31	VCC_SM_31
VCC_SM_32	VCC_SM_32
VCC_SM_33	VCC_SM_33
VCC_SM_34	VCC_SM_34
VCC_SM_35	VCC_SM_35
VCC_SM_36	VCC_SM_36
VCC_SM_37	VCC_SM_37
VCC_SM_38	VCC_SM_38
VCC_SM_39	VCC_SM_39
VCC_SM_40	VCC_SM_40
VCC_SM_41	VCC_SM_41
VCC_SM_42	VCC_SM_42
VCC_SM_43	VCC_SM_43
VCC_SM_44	VCC_SM_44
VCC_SM_45	VCC_SM_45
VCC_SM_46	VCC_SM_46
VCC_SM_47	VCC_SM_47
VCC_SM_48	VCC_SM_48
VCC_SM_49	VCC_SM_49
VCC_SM_50	VCC_SM_50
VCC_SM_51	VCC_SM_51
VCC_SM_52	VCC_SM_52
VCC_SM_53	VCC_SM_53
VCC_SM_54	VCC_SM_54
VCC_SM_55	VCC_SM_55
VCC_SM_56	VCC_SM_56
VCC_SM_57	VCC_SM_57
VCC_SM_58	VCC_SM_58
VCC_SM_59	VCC_SM_59
VCC_SM_60	VCC_SM_60
VCC_SM_61	VCC_SM_61
VCC_SM_62	VCC_SM_62
VCC_SM_63	VCC_SM_63
VCC_SM_64	VCC_SM_64
VCC_SM_65	VCC_SM_65
VCC_SM_66	VCC_SM_66
VCC_SM_67	VCC_SM_67
VCC_SM_68	VCC_SM_68
VCC_SM_69	VCC_SM_69
VCC_SM_70	VCC_SM_70
VCC_SM_71	VCC_SM_71
VCC_SM_72	VCC_SM_72
VCC_SM_73	VCC_SM_73
VCC_SM_74	VCC_SM_74
VCC_SM_75	VCC_SM_75
VCC_SM_76	VCC_SM_76
VCC_SM_77	VCC_SM_77
VCC_SM_78	VCC_SM_78
VCC_SM_79	VCC_SM_79
VCC_SM_80	VCC_SM_80
VCC_SM_81	VCC_SM_81
VCC_SM_82	VCC_SM_82
VCC_SM_83	VCC_SM_83
VCC_SM_84	VCC_SM_84
VCC_SM_85	VCC_SM_85
VCC_SM_86	VCC_SM_86
VCC_SM_87	VCC_SM_87
VCC_SM_88	VCC_SM_88
VCC_SM_89	VCC_SM_89
VCC_SM_90	VCC_SM_90
VCC_SM_91	VCC_SM_91
VCC_SM_92	VCC_SM_92
VCC_SM_93	VCC_SM_93
VCC_SM_94	VCC_SM_94
VCC_SM_95	VCC_SM_95
VCC_SM_96	VCC_SM_96
VCC_SM_97	VCC_SM_97
VCC_SM_98	VCC_SM_98
VCC_SM_99	VCC_SM_99
VCC_SM_100	VCC_SM_100
VCC_SM_101	VCC_SM_101
VCC_SM_102	VCC_SM_102
VCC_SM_103	VCC_SM_103
VCC_SM_104	VCC_SM_104
VCC_SM_105	VCC_SM_105
VCC_SM_106	VCC_SM_106
VCC_SM_107	VCC_SM_107



Pin	Signal
VCCSM_LF1	VCCSM_LF1
VCCSM_LF2	VCCSM_LF2
VCCSM_LF3	VCCSM_LF3
VCCSM_LF4	VCCSM_LF4
VCCSM_LF5	VCCSM_LF5

Pin	Signal
VSS_NCTF0	VSS_NCTF0
VSS_NCTF1	VSS_NCTF1
VSS_NCTF2	VSS_NCTF2
VSS_NCTF3	VSS_NCTF3
VSS_NCTF4	VSS_NCTF4
VSS_NCTF5	VSS_NCTF5
VSS_NCTF6	VSS_NCTF6
VSS_NCTF7	VSS_NCTF7
VSS_NCTF8	VSS_NCTF8
VSS_NCTF9	VSS_NCTF9
VSS_NCTF10	VSS_NCTF10
VSS_NCTF11	VSS_NCTF11
VSS_NCTF12	VSS_NCTF12
VSS_NCTF13	VSS_NCTF13
VSS_NCTF14	VSS_NCTF14
VSS_NCTF15	VSS_NCTF15
VSS_NCTF16	VSS_NCTF16
VSS_NCTF17	VSS_NCTF17
VSS_NCTF18	VSS_NCTF18
VSS_NCTF19	VSS_NCTF19
VSS_NCTF20	VSS_NCTF20
VSS_NCTF21	VSS_NCTF21
VSS_NCTF22	VSS_NCTF22
VSS_NCTF23	VSS_NCTF23
VSS_NCTF24	VSS_NCTF24
VSS_NCTF25	VSS_NCTF25
VSS_NCTF26	VSS_NCTF26
VSS_NCTF27	VSS_NCTF27
VSS_NCTF28	VSS_NCTF28
VSS_NCTF29	VSS_NCTF29
VSS_NCTF30	VSS_NCTF30
VSS_NCTF31	VSS_NCTF31
VSS_NCTF32	VSS_NCTF32
VSS_NCTF33	VSS_NCTF33
VSS_NCTF34	VSS_NCTF34
VSS_NCTF35	VSS_NCTF35
VSS_NCTF36	VSS_NCTF36
VSS_NCTF37	VSS_NCTF37
VSS_NCTF38	VSS_NCTF38
VSS_NCTF39	VSS_NCTF39
VSS_NCTF40	VSS_NCTF40
VSS_NCTF41	VSS_NCTF41
VSS_NCTF42	VSS_NCTF42
VSS_NCTF43	VSS_NCTF43
VSS_NCTF44	VSS_NCTF44
VSS_NCTF45	VSS_NCTF45
VSS_NCTF46	VSS_NCTF46
VSS_NCTF47	VSS_NCTF47
VSS_NCTF48	VSS_NCTF48
VSS_NCTF49	VSS_NCTF49
VSS_NCTF50	VSS_NCTF50
VSS_NCTF51	VSS_NCTF51
VSS_NCTF52	VSS_NCTF52
VSS_NCTF53	VSS_NCTF53
VSS_NCTF54	VSS_NCTF54
VSS_NCTF55	VSS_NCTF55
VSS_NCTF56	VSS_NCTF56
VSS_NCTF57	VSS_NCTF57
VSS_NCTF58	VSS_NCTF58
VSS_NCTF59	VSS_NCTF59
VSS_NCTF60	VSS_NCTF60
VSS_NCTF61	VSS_NCTF61
VSS_NCTF62	VSS_NCTF62
VSS_NCTF63	VSS_NCTF63
VSS_NCTF64	VSS_NCTF64
VSS_NCTF65	VSS_NCTF65
VSS_NCTF66	VSS_NCTF66
VSS_NCTF67	VSS_NCTF67
VSS_NCTF68	VSS_NCTF68
VSS_NCTF69	VSS_NCTF69
VSS_NCTF70	VSS_NCTF70
VSS_NCTF71	VSS_NCTF71
VSS_NCTF72	VSS_NCTF72

7 MCH_CFG_5 ← 1 ● 30MIL TP76

MCH_CFG_5
Low = DMIX2
High = DMIX4

7 MCH_CFG_6 ← 1 ● 30MIL TP77

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

7 MCH_CFG_7 ← 1 ● 30MIL TP78

MCH_CFG_7 (CPU Strap)
Low = RSVD
High = Mobile Yonah processor

7 MCH_CFG_9 ← 1 ● 30MIL TP81

MCH_CFG_9 (PCIe Graphics Lane)
Low = Reverse Lane operation
High = Normal operation

For layout convenience

7 MCH_CFG_10 ← 1 ● 30MIL TP82

MCH_CFG_10 (HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

7 MCH_CFG_11 ← 1 ● 30MIL TP83

MCH_CFG_11 (PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved



7 MCH_CFG_12 ← 1 ● 30MIL TP84

7 MCH_CFG_13 ← 1 ● 30MIL TP85

MCH_CFG_[13:12] (XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 ← 1 ● 30MIL TP160

MCH_CFG_16 (FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

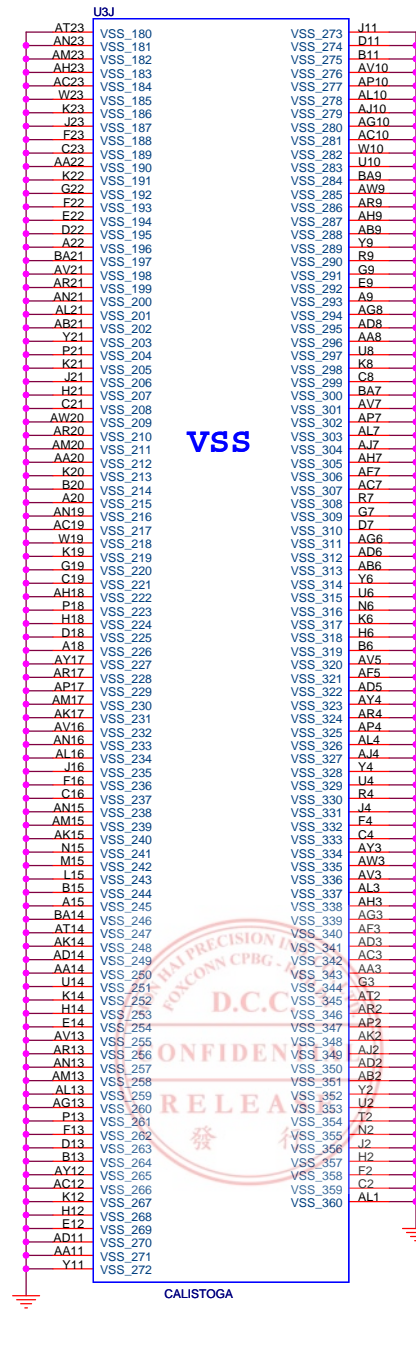
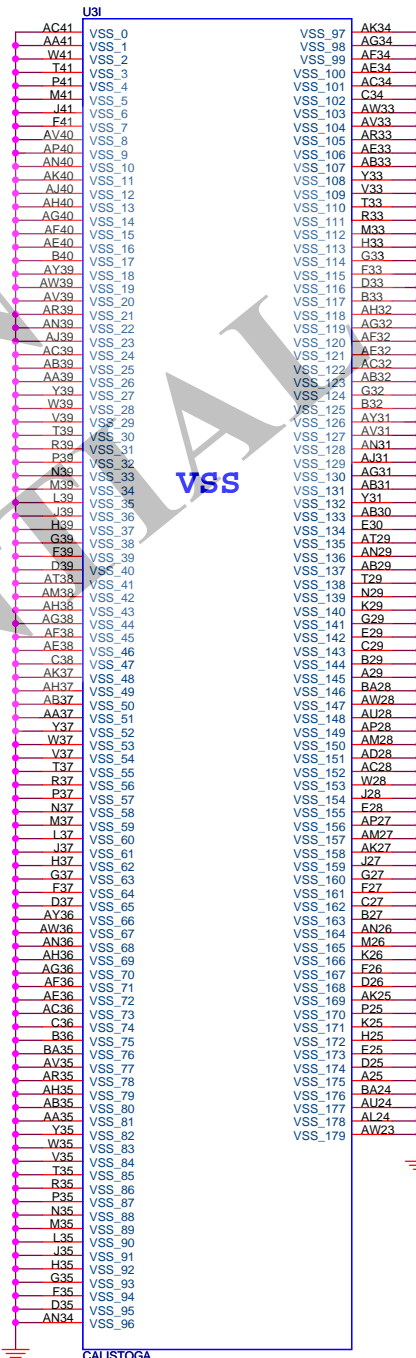
7 MCH_CFG_18 ← 1 ● 30MIL TP79

MCH_CFG_19 (DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

7 MCH_CFG_19 ← 1 ● 30MIL TP80

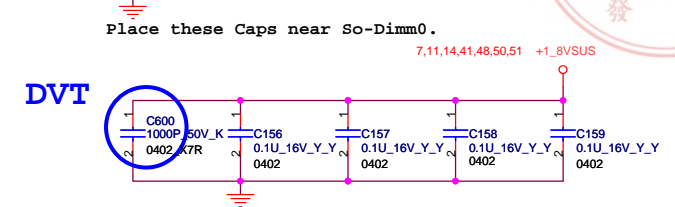
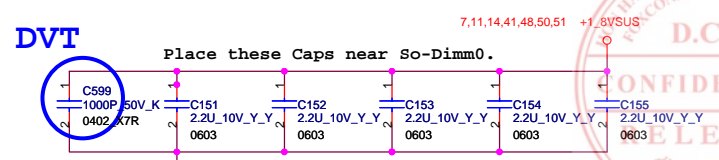
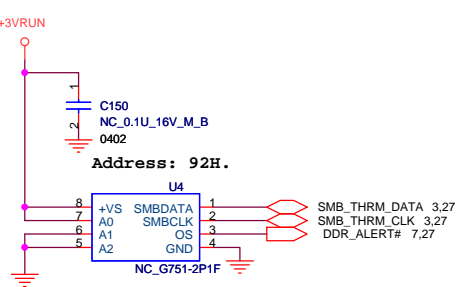
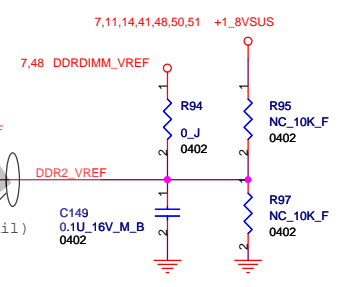
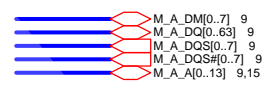
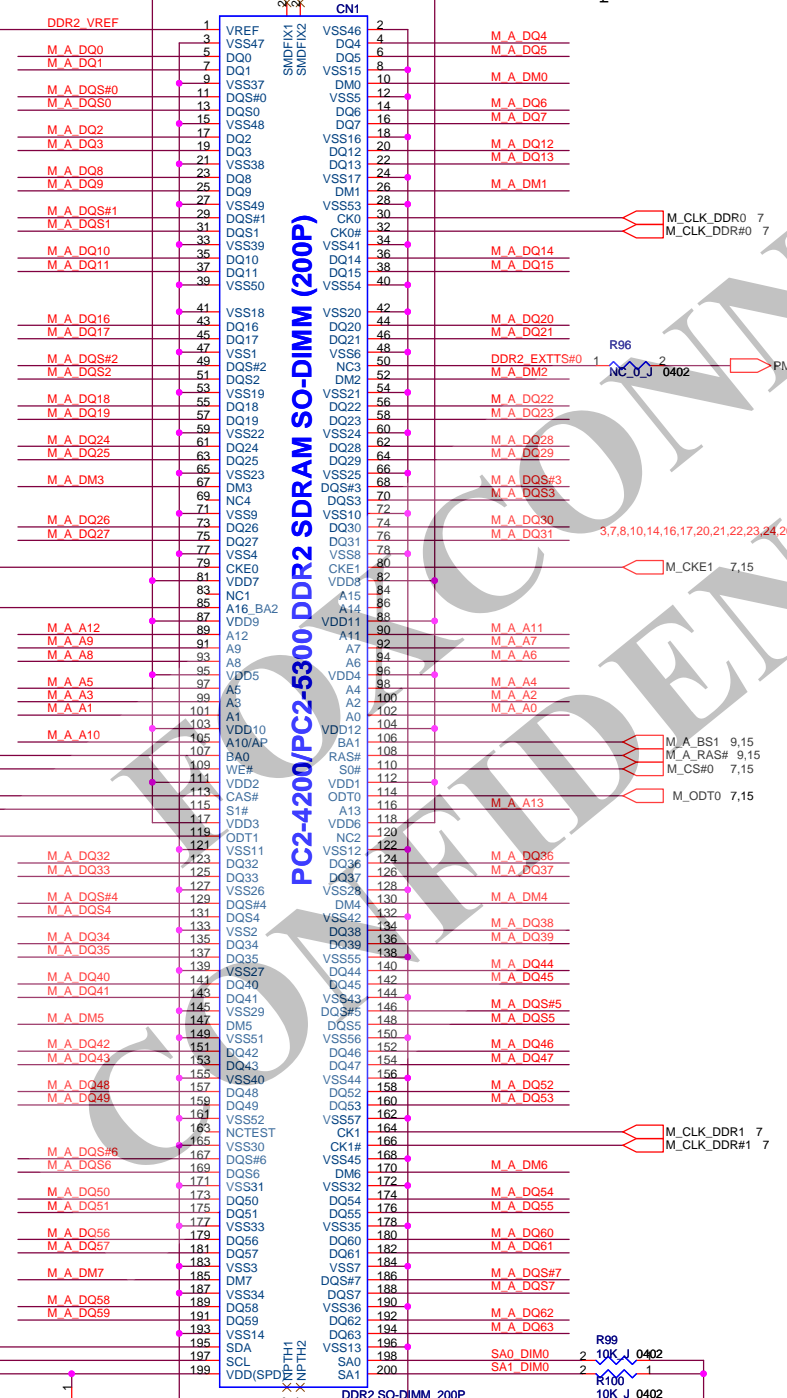
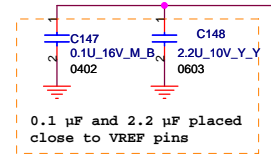
MCH_CFG_20 (PCIe Backward Interoperability mode)
Low = Only SDVO or PCIe x1 is operational (defaults)
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub



7,11,14,41,48,50,51 +1_8VSUS

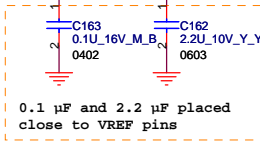
1.8V per DIMM=3.08A



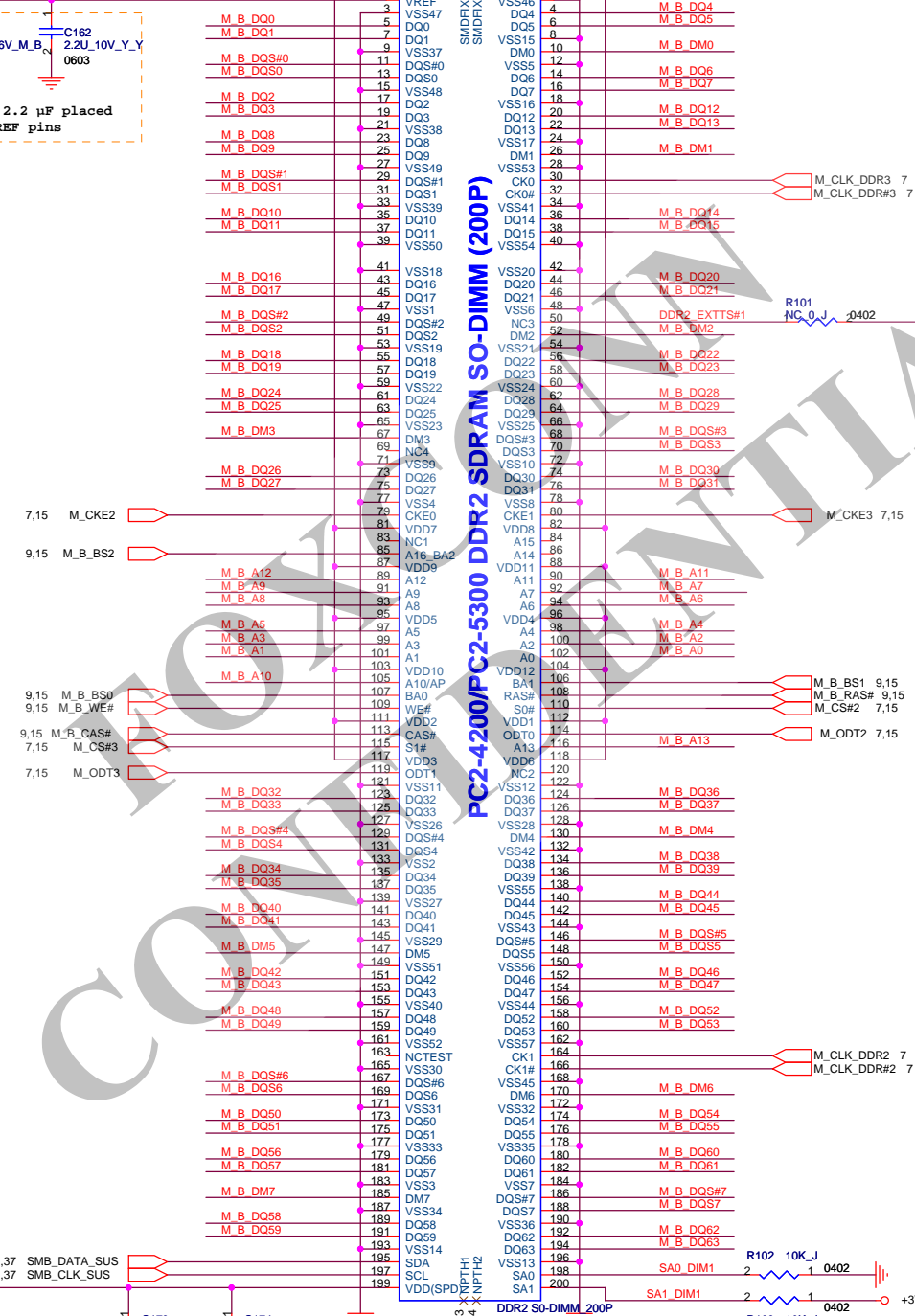
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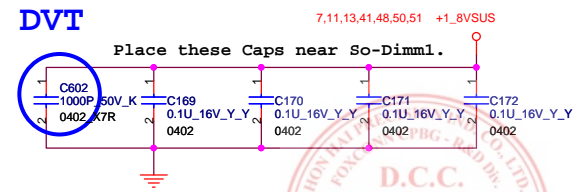
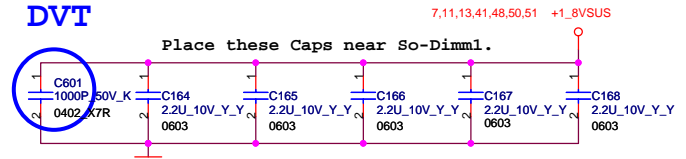
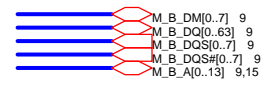
FOXCONN		
Title: DDR(H)SO-DIMM_0		
Size: A3	Document Number: MS70-1-01	Rev: 2.0
Date: Tuesday, August 22, 2006	Sheet: 13	of: 55



1.8V per DIMM=3.08A



PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)



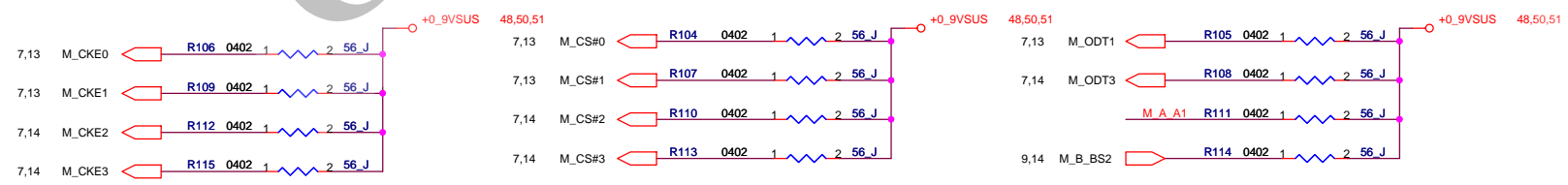
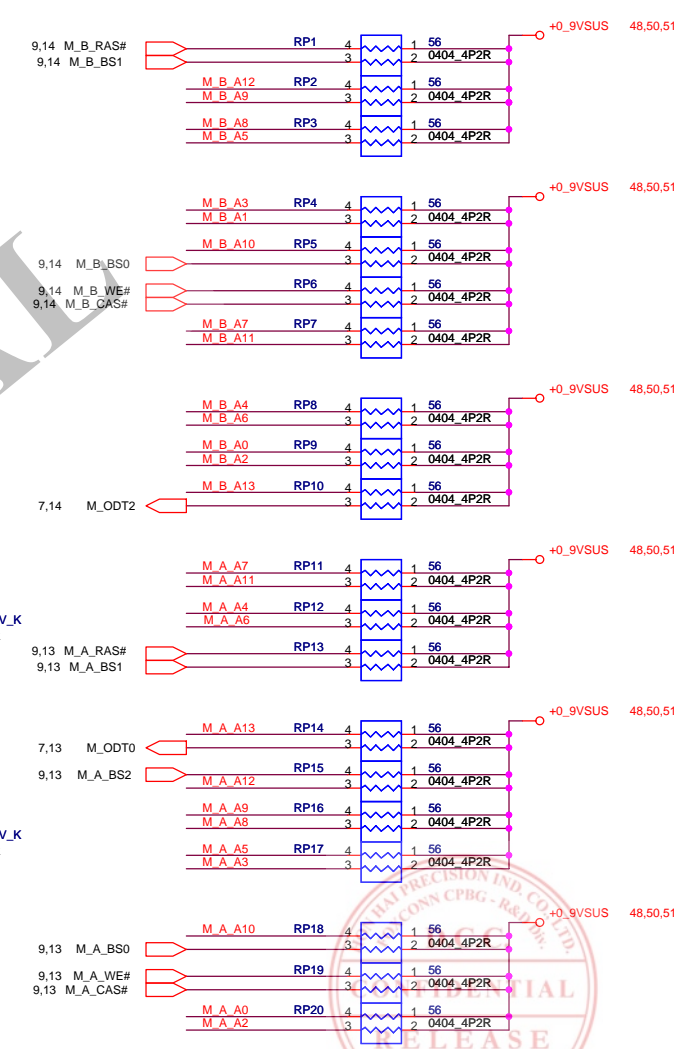
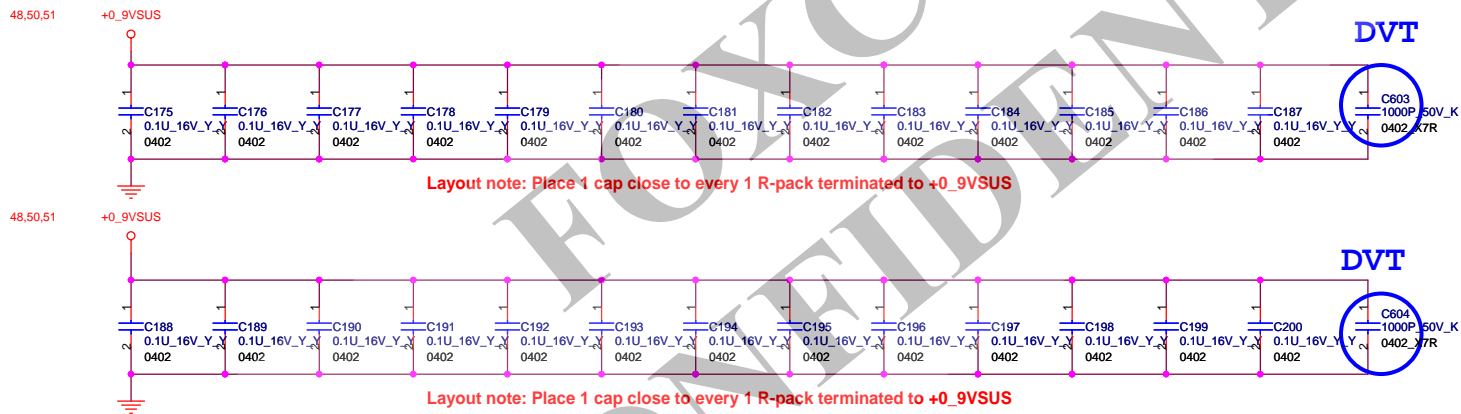
FOX_AS0A426_N4SC_4F

DIMM_1

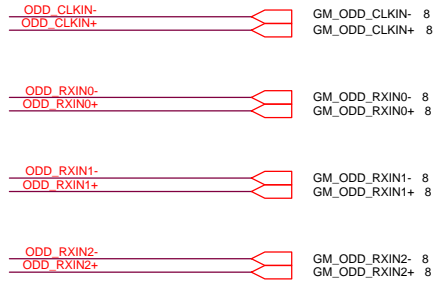
SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0

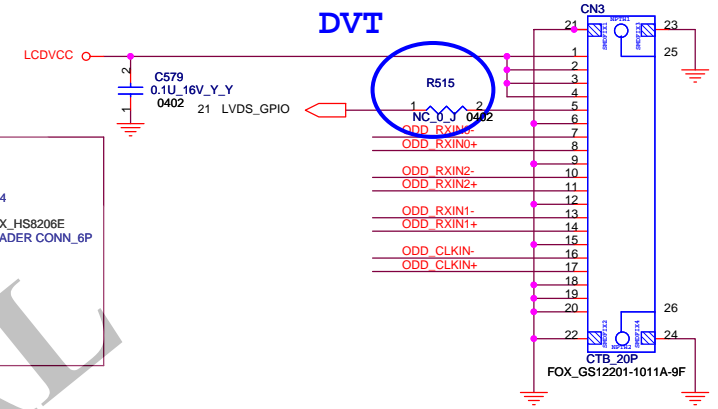
FOXCONN			HON HAI Precision Ind. Co., Ltd.		
Title DDR(I)SO-DIMM_1			CCPBG - R&D Division		
Size A3	Document Number MST0-1-01	Rev 2.0			
Date: Tuesday, August 22, 2006	Sheet 14	of 55			



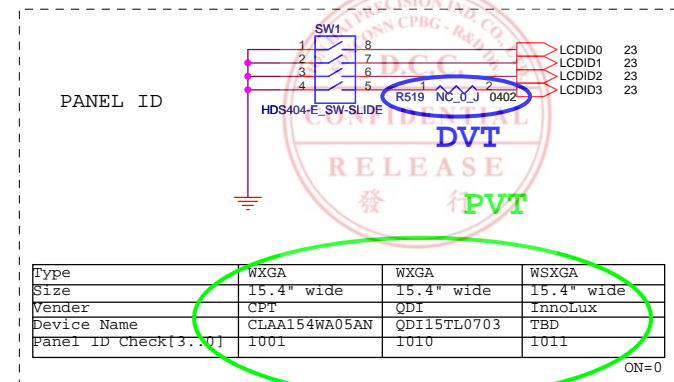
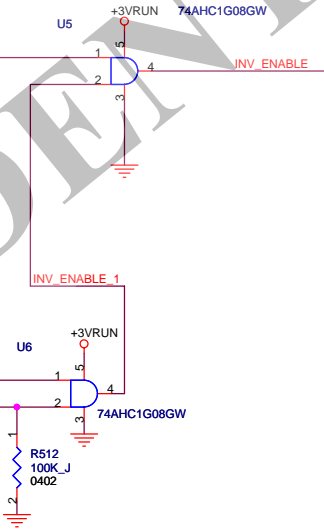
LVDS



LVDS CONNECTOR

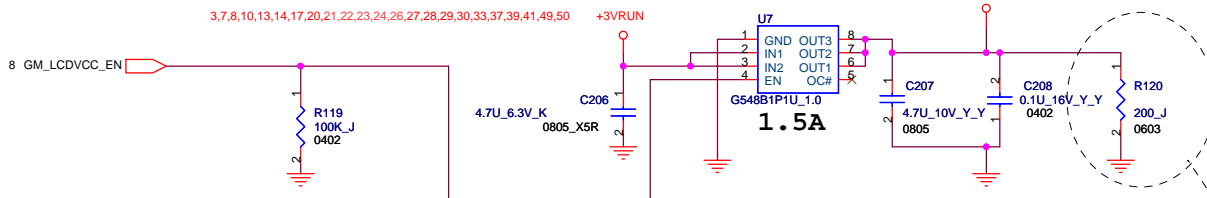


INVERTER CONNECTOR



Type	WXGA	WXGA	WSXGA
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	CPT	QDI	InnoLux
Device Name	CLAA154WA05AN	QDI15TL0703	TBD
Panel ID Check[3..0]	1001	1010	1011

ON=0

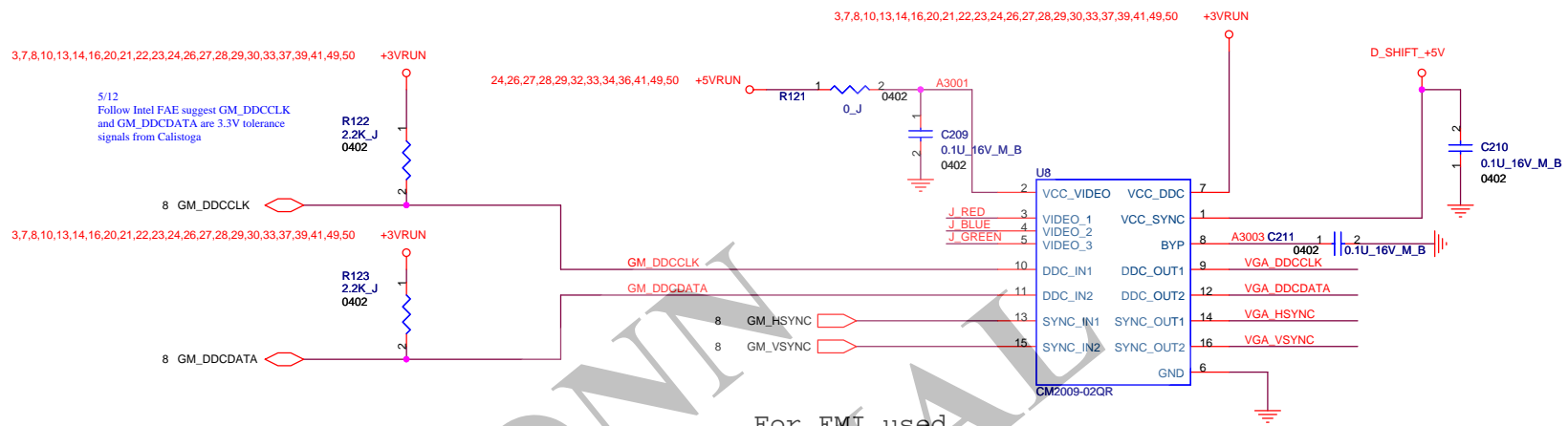


DISCHARGE
 The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

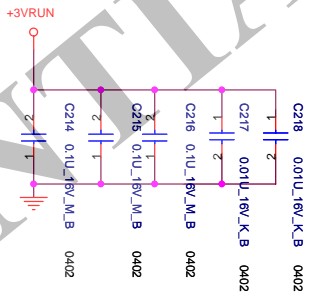
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title LVDS
Size A3 **Document Number** MS70-1-01 **Rev** 2.0
Date: Tuesday, August 22, 2006 **Sheet** 16 **of** 55

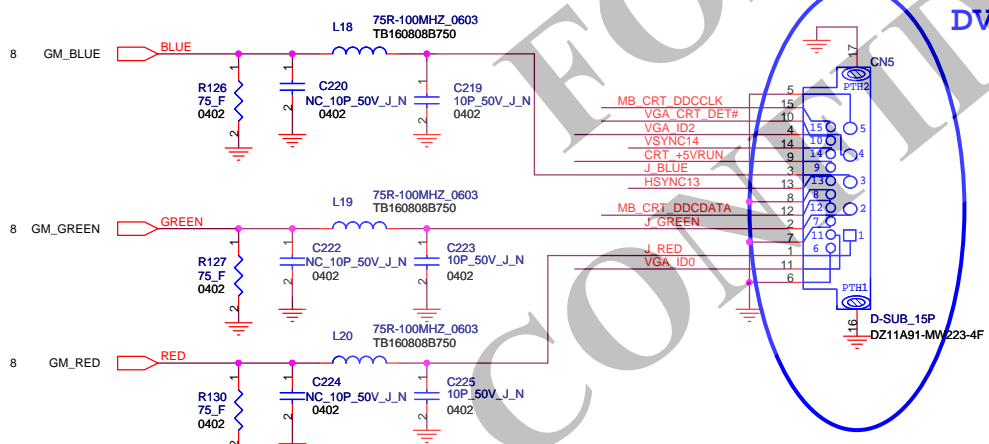
CONFIDENTIAL



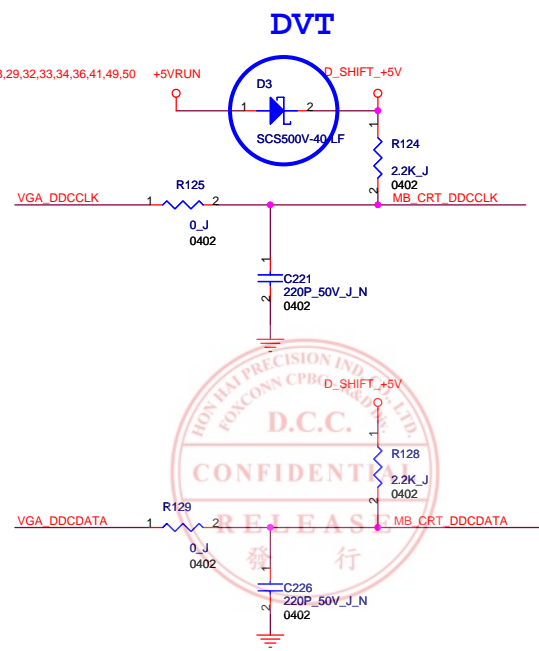
For EMI used



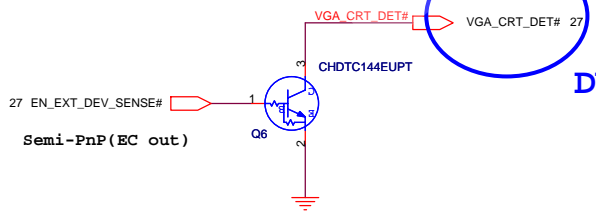
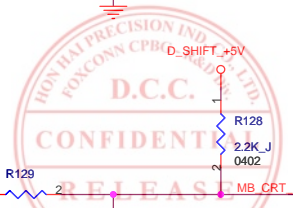
CRT CONNECTOR



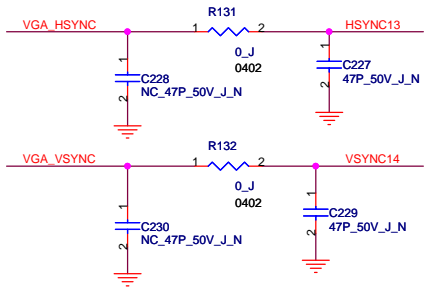
DVT



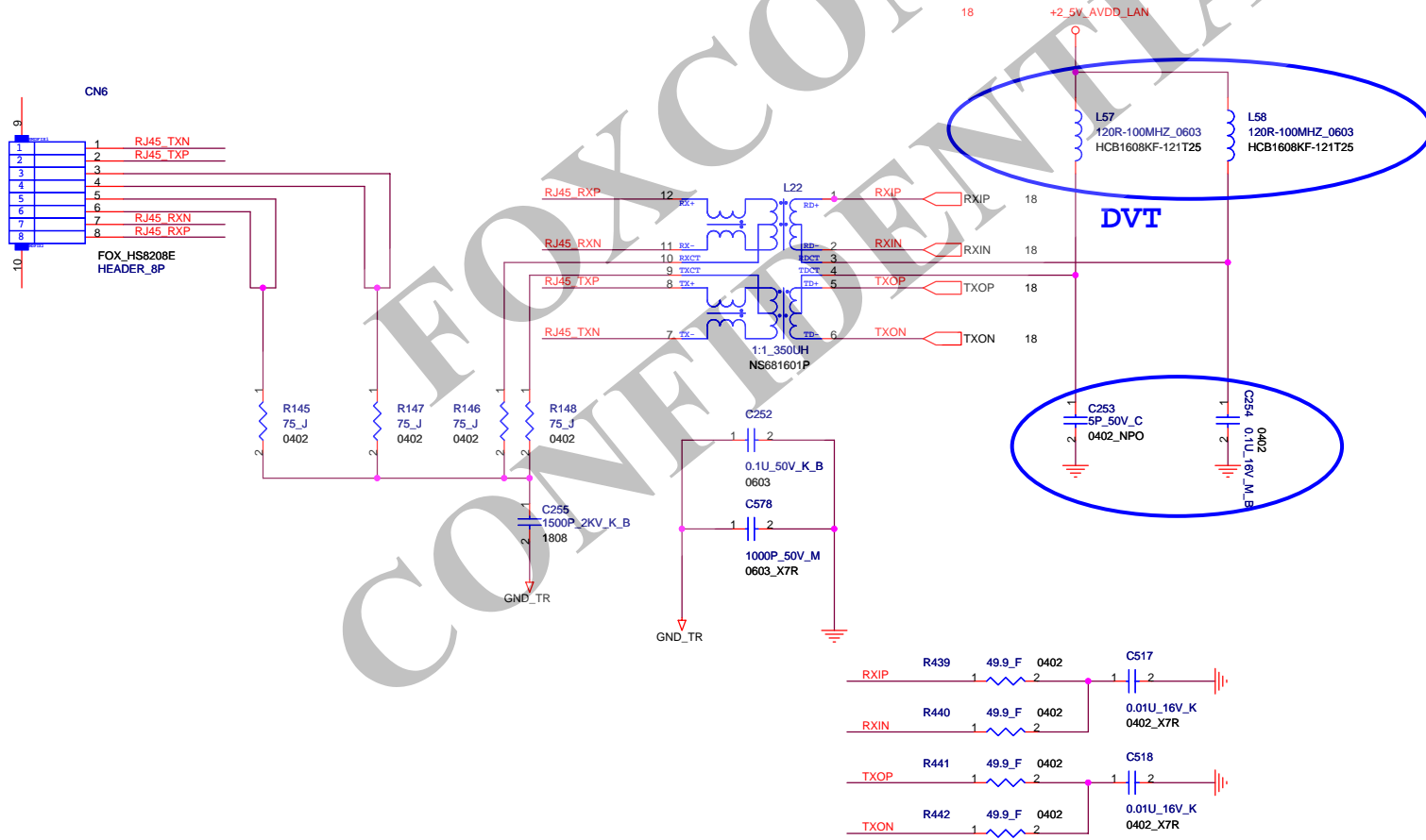
DVT



DVT



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
File	CRT	
Size	Document Number	Rev
A3	MS70-1-01	2.0
Date:	Tuesday, August 22, 2006	Sheet 17 of 55



CONFIDENTIAL



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title LAN Transformer		
Size A3	Document Number MS70-1-01	Rev 2.0
Date: Tuesday, August 22, 2006	Sheet 19	of 55

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	C256 0402
NC_10P_50V_E_N	2	1	C257 0402
NC_10P_50V_E_N	2	1	C258 0402
NC_10P_50V_E_N	2	1	C265 0402
NC_10P_50V_E_N	2	1	C266 0402
NC_10P_50V_E_N	2	1	C267 0402
NC_10P_50V_E_N	2	1	C268 0402
NC_10P_50V_E_N	2	1	C271 0402

close to clk gen (For EMI)

Length as short as possible.



ICH7 DMI

06/17
CLK_PCIE_ICH changed to SRCLK7
CLK_DOCK_LAN changed to SRCLK8
SW Note: datasheet page13 Byte8.1 => SRCLK7 should be configured as "Not Controlled"

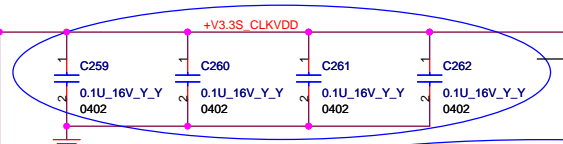
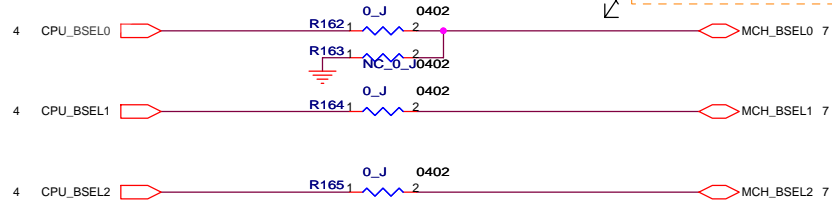
FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI	
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

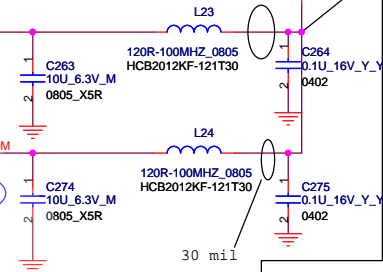
SM bus Address 96S9LPR321BKLF 1101001 (ICH7)
For clock generator

06/09
DEL pull-up resistor R80-82
pull-down resistor R85,R88
del R84,R87,R90

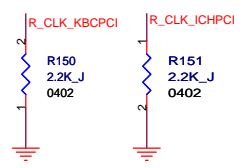
06/16
ICS have recognized, FSLA/FSLB setting is different from CK410M spec. But MS10 will not use 100MHz, For test purpose, please move R91 from MCH_BSEL2 to MCH_BSEL0, and mount R89.



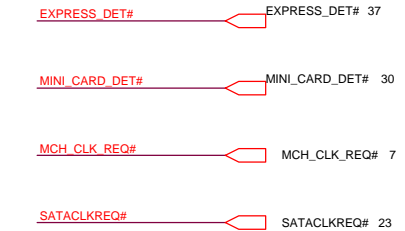
Layout note:
Place 1 cap close to each pin



Pin Straps	
Pin 53/59/60/64	100K ohm pull-up
pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCCLK1 (NV)



06/16
pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor



06/09
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor



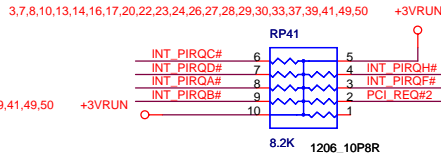
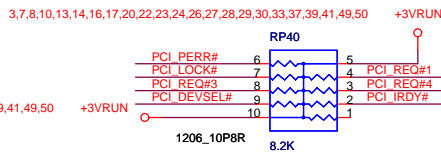
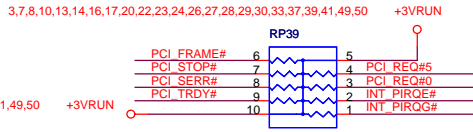
CALISTOGA Chip HOST

CPU

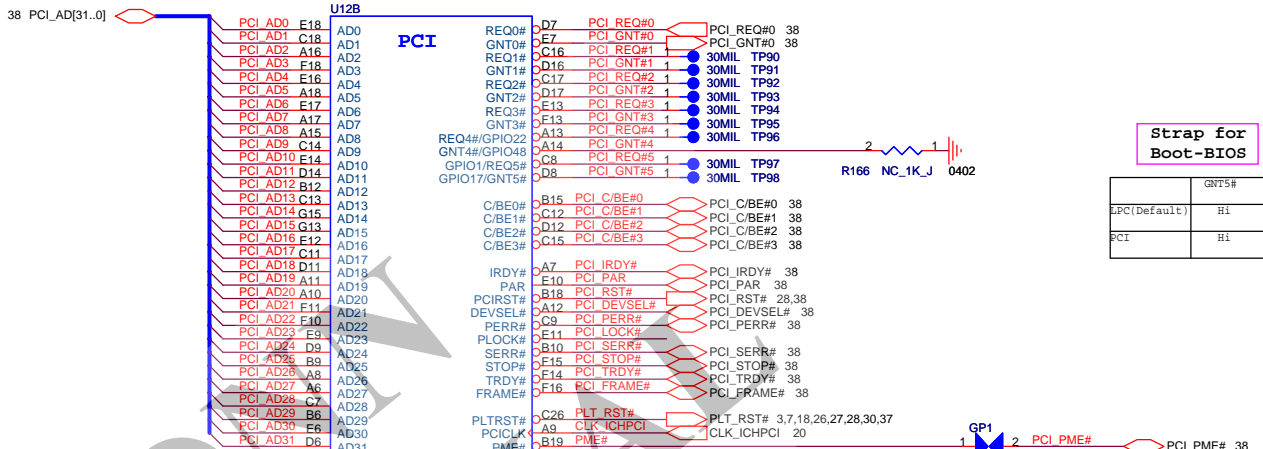
DVT

CALISTOGA SSSCK

CALISTOGA DOT96

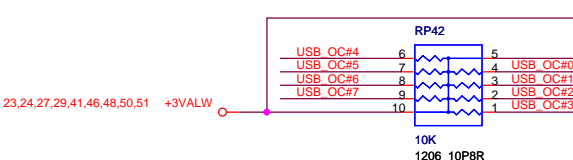
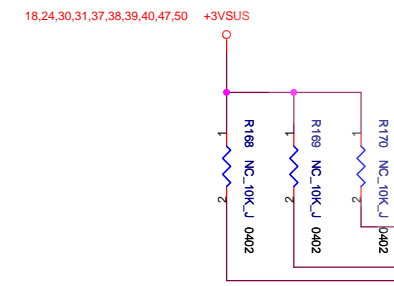
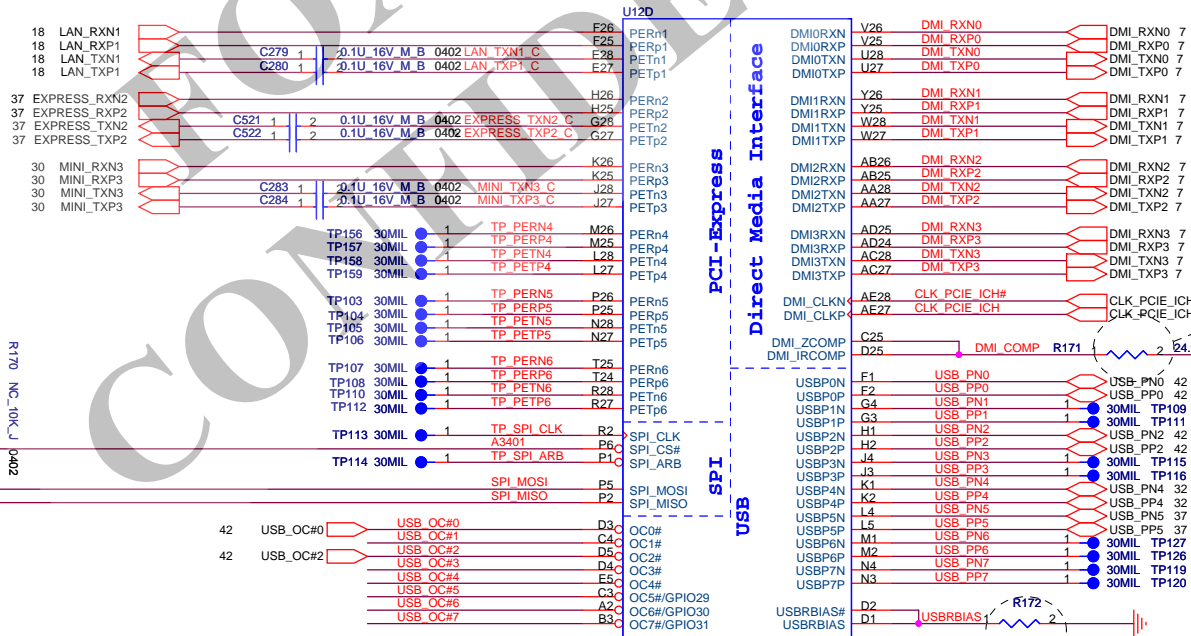
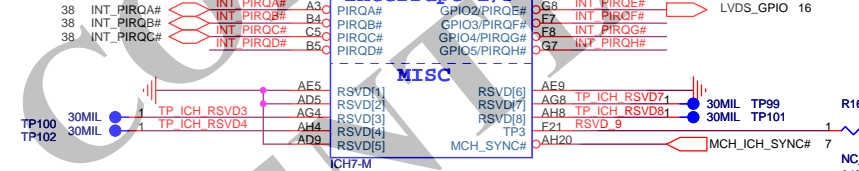


PCI Pullups

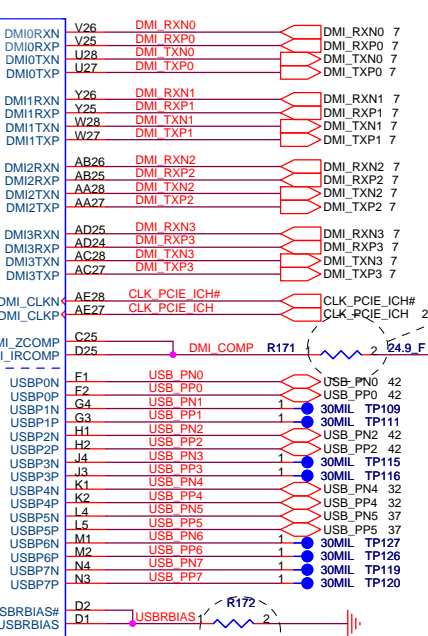


Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	HI	HI
PCI	HI	LOW

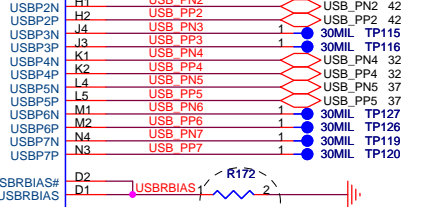


Direct Media Interface



Place within 500 mils of ICH

SPI



Place within 500 mils of ICH and don't routing next to high speed signals



FOXCONN HON HAI Precision Ind. Co., Ltd.

Title: ICH7-M(PCI/DMI/USB/PCIE) 1/5		
Size: A3	Document Number: MS70-1-01	Rev: 2.0
Date: Tuesday, August 22, 2006	Sheet: 21	of: 55

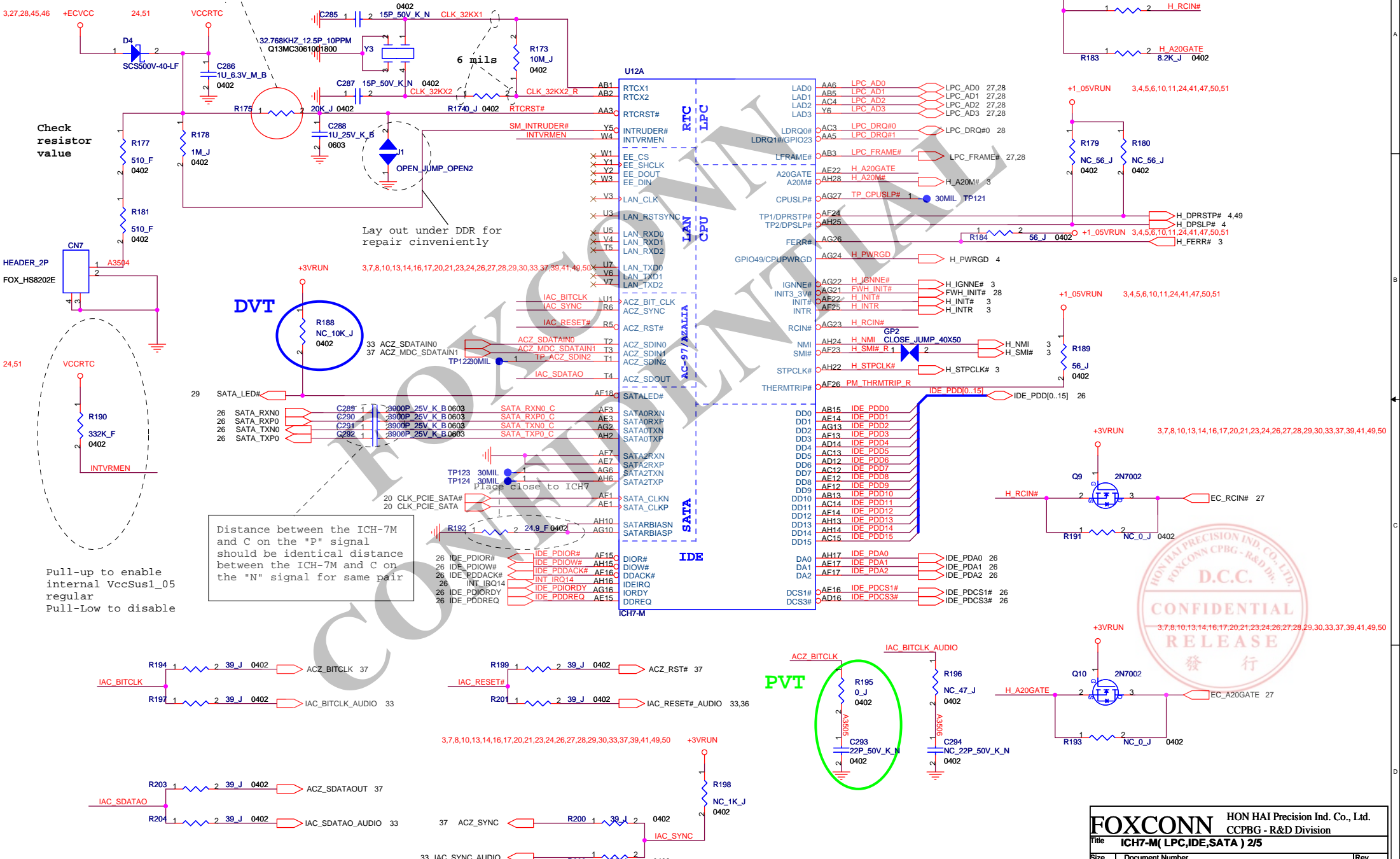
RTRCRST#

VccRTC

Min : 18ms

The traces inside this block should be wider. No digital signals routed under XTAL

+3VRUN 3,7,8,10,13,14,16,17,20,21,23,24,26,27,28,29,30,33,37,39,41,49,50



Check resistor value

Lay out under DDR for repair conveniently

Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for pair regular

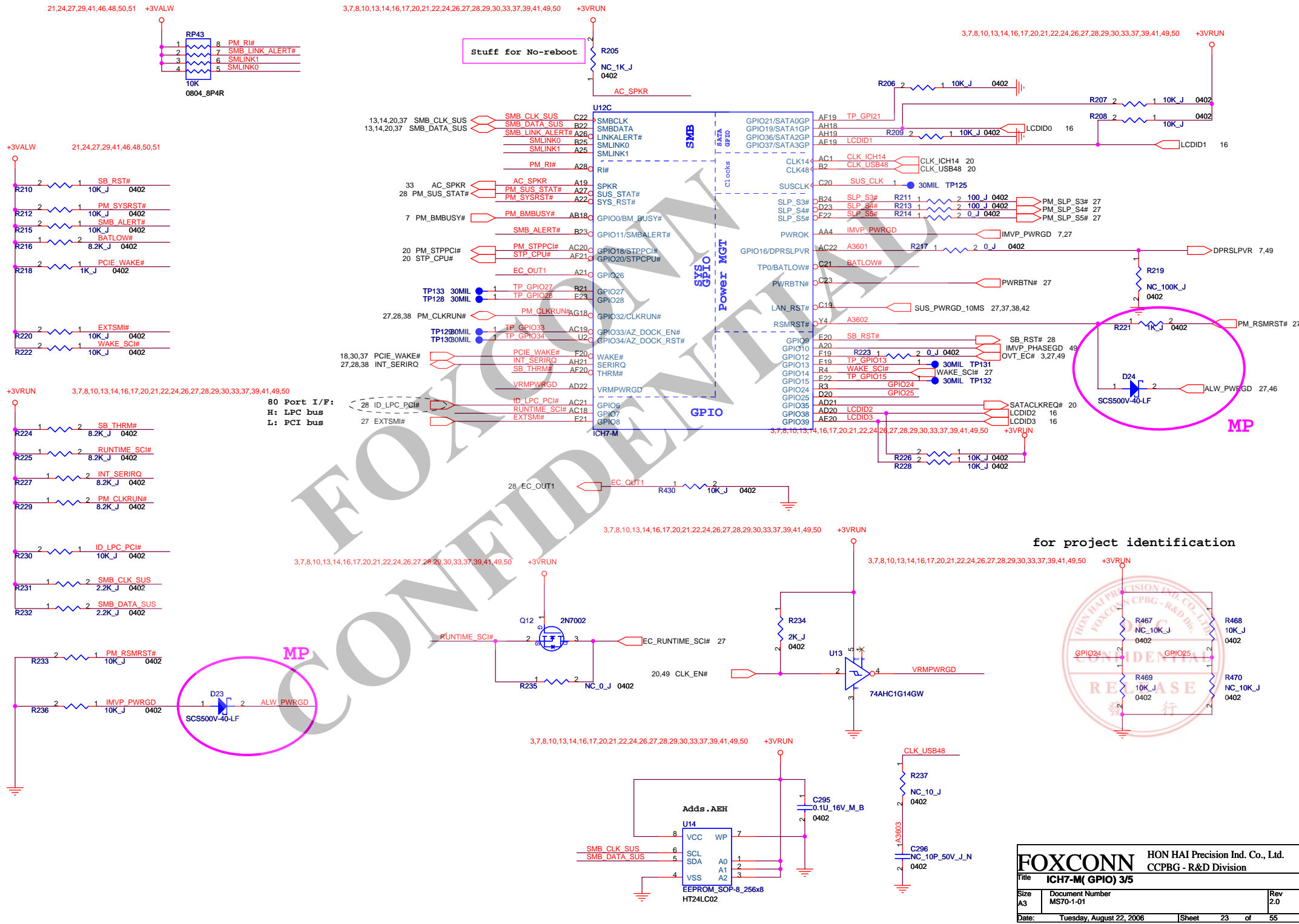
Pull-up to enable internal VccSus1_05 regular Pull-Low to disable

+3VRUN 3,7,8,10,13,14,16,17,20,21,23,24,26,27,28,29,30,33,37,39,41,49,50

+3VRUN 3,7,8,10,13,14,16,17,20,21,23,24,26,27,28,29,30,33,37,39,41,49,50



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CCPBG - R&D Division		
Title ICH7-M(LPC,IDE,SATA) 2/5		
Size A3	Document Number MS70-1-01	Rev 2.0
Date: Tuesday, August 22, 2006	Sheet 22	of 55

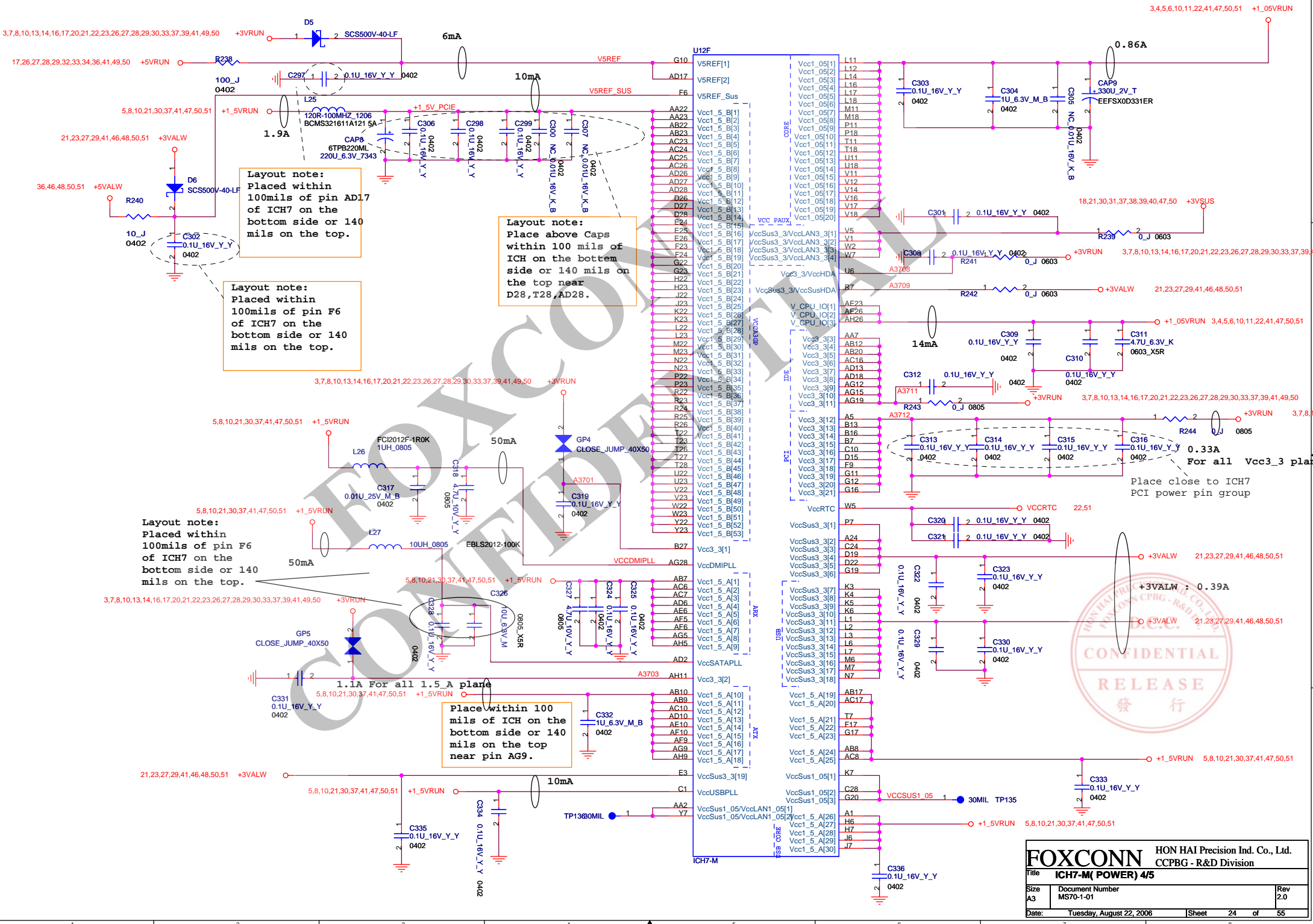


80 Port I/F:
 H: LPC bus
 L: PCI bus

for project identification

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title	ICH7-M (GPIO) 3/5		
Size	Document Number	Rev 2.0	
A3	MS70-1-01		
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Layout note:
Placed within 100mils of pin AD1.7 on the bottom side or 140 mils on the top.

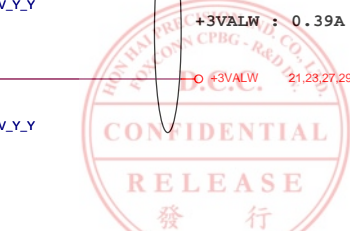
Layout note:
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

For all Vcc3_3 plane Place close to ICH7 PCI power pin group



FOXCONN HON HAI Precision Ind. Co., Ltd.		
Title ICH7-M (POWER) 4/5		
Size	Document Number	Rev
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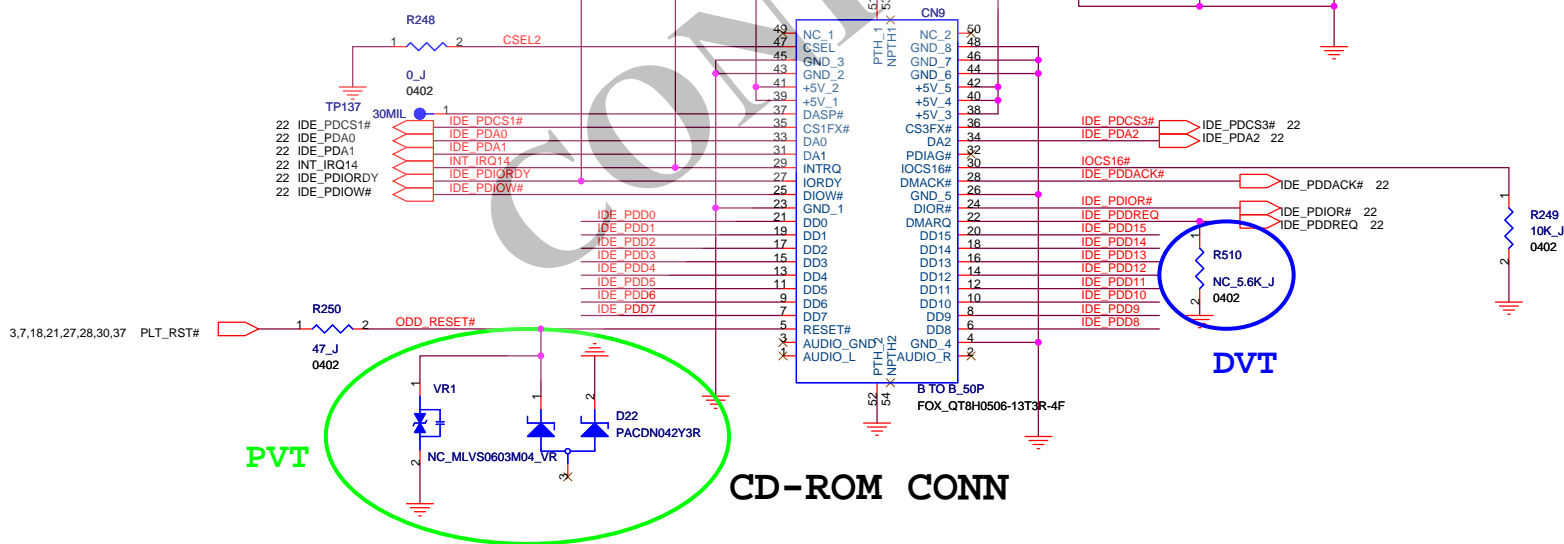
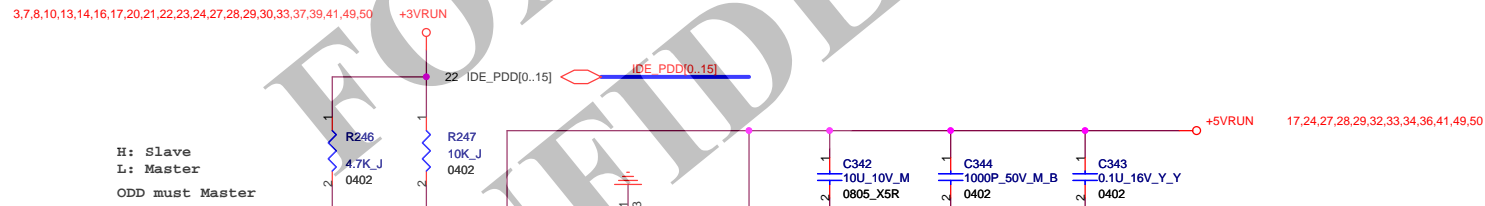
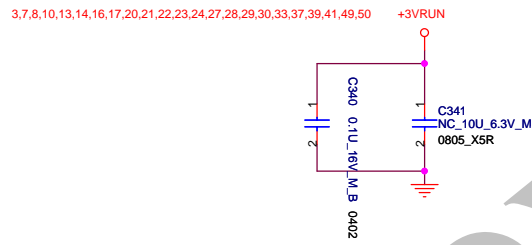
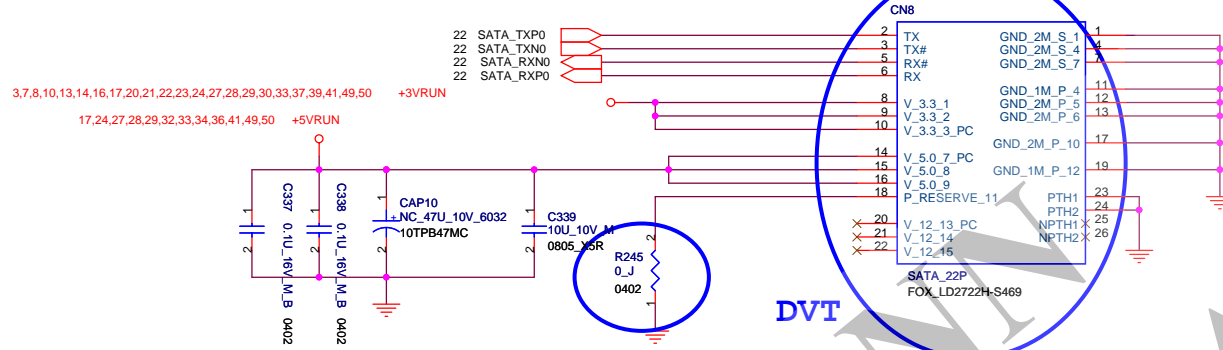
U12E		
A4	VSS11	VSS108
A23	VSS12	VSS109
B1	VSS13	VSS110
B8	VSS14	VSS111
B11	VSS15	VSS112
B14	VSS16	VSS113
B17	VSS17	VSS114
B20	VSS18	VSS115
B26	VSS19	VSS116
B28	VSS20	VSS117
C2	VSS21	VSS118
C6	VSS22	VSS119
C27	VSS23	VSS120
D10	VSS24	VSS121
D13	VSS25	VSS122
D18	VSS26	VSS123
D21	VSS27	VSS124
D24	VSS28	VSS125
E1	VSS29	VSS126
E2	VSS30	VSS127
E4	VSS31	VSS128
E8	VSS32	VSS129
E16	VSS33	VSS130
F3	VSS34	VSS131
F4	VSS35	VSS132
F5	VSS36	VSS133
F12	VSS37	VSS134
F27	VSS38	VSS135
F28	VSS39	VSS136
G1	VSS40	VSS137
G2	VSS41	VSS138
G5	VSS42	VSS139
G6	VSS43	VSS140
G9	VSS44	VSS141
G14	VSS45	VSS142
G18	VSS46	VSS143
G21	VSS47	VSS144
G24	VSS48	VSS145
G25	VSS49	VSS146
G26	VSS50	VSS147
H3	VSS51	VSS148
H4	VSS52	VSS149
H5	VSS53	VSS150
H24	VSS54	VSS151
H27	VSS55	VSS152
H28	VSS56	VSS153
J1	VSS57	VSS154
J2	VSS58	VSS155
J5	VSS59	VSS156
J24	VSS60	VSS157
J25	VSS61	VSS158
J26	VSS62	VSS159
K24	VSS63	VSS160
K27	VSS64	VSS161
K28	VSS65	VSS162
L13	VSS66	VSS163
L15	VSS67	VSS164
L24	VSS68	VSS165
L25	VSS69	VSS166
L26	VSS70	VSS167
M3	VSS71	VSS168
M4	VSS72	VSS169
M5	VSS73	VSS170
M12	VSS74	VSS171
M13	VSS75	VSS172
M14	VSS76	VSS173
M14	VSS77	VSS174
M15	VSS78	VSS175
M15	VSS79	VSS176
M16	VSS80	VSS177
M17	VSS81	VSS178
M24	VSS82	VSS179
M27	VSS83	VSS180
M28	VSS84	VSS181
N1	VSS85	VSS182
N2	VSS86	VSS183
N5	VSS87	VSS184
N6	VSS88	VSS185
N11	VSS89	VSS186
N12	VSS90	VSS187
N13	VSS91	VSS188
N14	VSS92	VSS189
N15	VSS93	VSS190
N16	VSS94	VSS191
N17	VSS95	VSS192
N24	VSS96	VSS193
N26	VSS97	VSS194
P3	VSS98	VSS195
P4	VSS99	VSS196
P12	VSS100	VSS197
P13	VSS101	VSS198
P14	VSS102	VSS199
P15	VSS103	VSS200
P16	VSS104	VSS201
P17	VSS105	VSS202
P24	VSS106	VSS203
P27	VSS107	VSS204
P28	VSS108	VSS205
R1	VSS109	VSS206
R11	VSS110	VSS207
R12	VSS111	VSS208
R13	VSS112	VSS209
R14	VSS113	VSS210
R15	VSS114	VSS211
R16	VSS115	VSS212
R17	VSS116	VSS213
R18	VSS117	VSS214
T6	VSS118	VSS215
T12	VSS119	VSS216
T13	VSS120	VSS217
T14	VSS121	VSS218
T15	VSS122	VSS219
T16	VSS123	VSS220
T17	VSS124	VSS221
U4	VSS125	VSS222
U12	VSS126	VSS223
U13	VSS127	VSS224
U14	VSS128	VSS225
U15	VSS129	VSS226
U16	VSS130	VSS227
U17	VSS131	VSS228
U24	VSS132	VSS229
U25	VSS133	VSS230
U26	VSS134	VSS231
V2	VSS135	VSS232
V13	VSS136	VSS233
V15	VSS137	VSS234
V24	VSS138	VSS235
V27	VSS139	VSS236
V28	VSS140	VSS237
W6	VSS141	VSS238
W24	VSS142	VSS239
W25	VSS143	VSS240
W26	VSS144	VSS241
Y3	VSS145	VSS242
Y24	VSS146	VSS243
Y27	VSS147	VSS244
Y28	VSS148	VSS245
AA1	VSS149	VSS246
AA24	VSS150	VSS247
AA25	VSS151	VSS248
AA26	VSS152	VSS249
AB4	VSS153	VSS250
AB6	VSS154	VSS251
AB11	VSS155	VSS252
AB14	VSS156	VSS253
AB16	VSS157	VSS254
AB19	VSS158	VSS255
AB21	VSS159	VSS256
AB24	VSS160	VSS257
AB27	VSS161	VSS258
AB28	VSS162	VSS259
AC2	VSS163	VSS260
AC5	VSS164	VSS261
AC9	VSS165	VSS262
AC11	VSS166	VSS263
AD1	VSS167	VSS264
AD3	VSS168	VSS265
AD4	VSS169	VSS266
AD7	VSS170	VSS267
AD8	VSS171	VSS268
AD11	VSS172	VSS269
AD15	VSS173	VSS270
AD19	VSS174	VSS271
AD23	VSS175	VSS272
AE2	VSS176	VSS273
AE4	VSS177	VSS274
AE8	VSS178	VSS275
AE11	VSS179	VSS276
AE13	VSS180	VSS277
AE18	VSS181	VSS278
AE21	VSS182	VSS279
AE24	VSS183	VSS280
AE25	VSS184	VSS281
AF4	VSS185	VSS282
AF8	VSS186	VSS283
AF11	VSS187	VSS284
AF27	VSS188	VSS285
AF28	VSS189	VSS286
AG1	VSS190	VSS287
AG3	VSS191	VSS288
AG7	VSS192	VSS289
AG11	VSS193	VSS290
AG14	VSS194	VSS291
AG17	VSS195	VSS292
AG20	VSS196	VSS293
AG25	VSS197	VSS294
AH1	VSS198	VSS295
AH3	VSS199	VSS296
AH7	VSS200	VSS297
AH12	VSS201	VSS298
AH23	VSS202	VSS299
AH27	VSS203	VSS300

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FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title ICH7-M(GND) 5/5		
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SATA HDD CONN

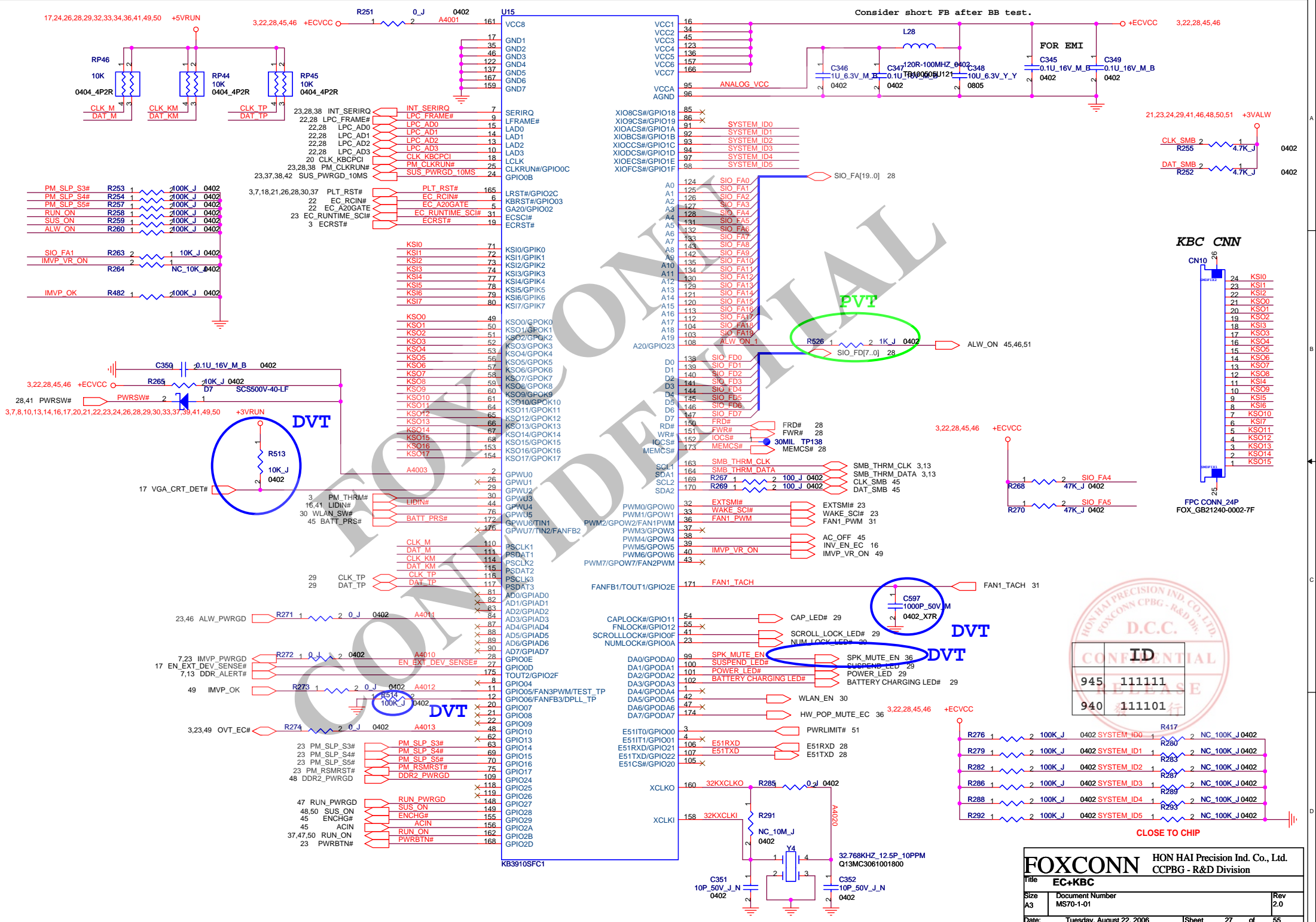


CD-ROM CONN

Follow Adoi san suggest ODD: Master/HDD:Slave

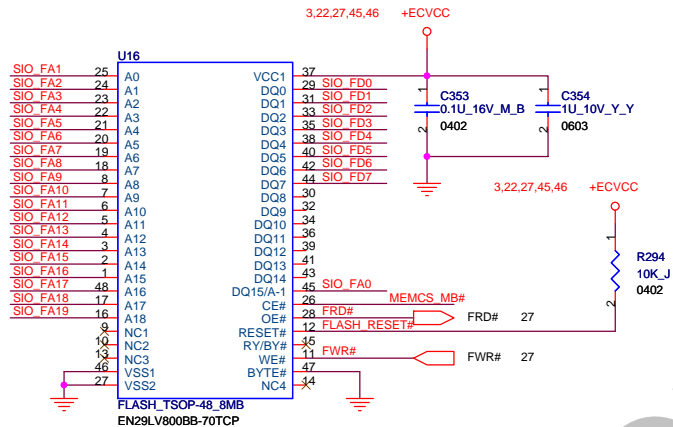


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title SATA HDD/CD-ROM		
Size A3	Document Number MS70-1-01	Rev 2.0
Date: Tuesday, August 22, 2006	Sheet 26	of 55



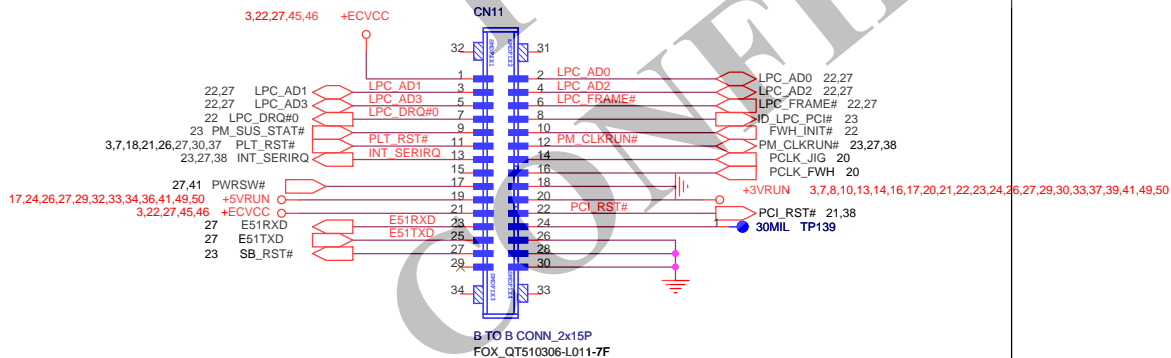
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title EC+KBC	
Size A3	Document Number MS70-1-01
Date: Tuesday, August 22, 2006	Sheet 27 of 55
Rev 2.0	

27 SIO_FA[19..0]
27 SIO_FD[7..0]

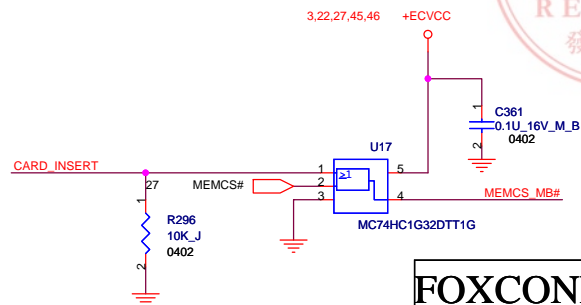
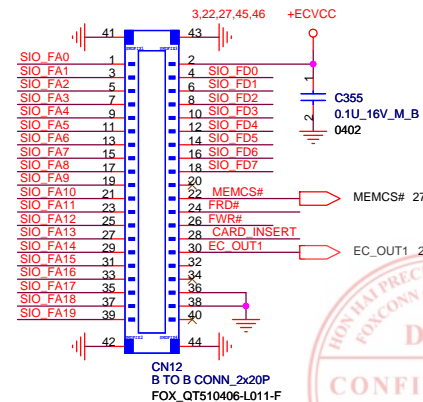


FLASH BIOS

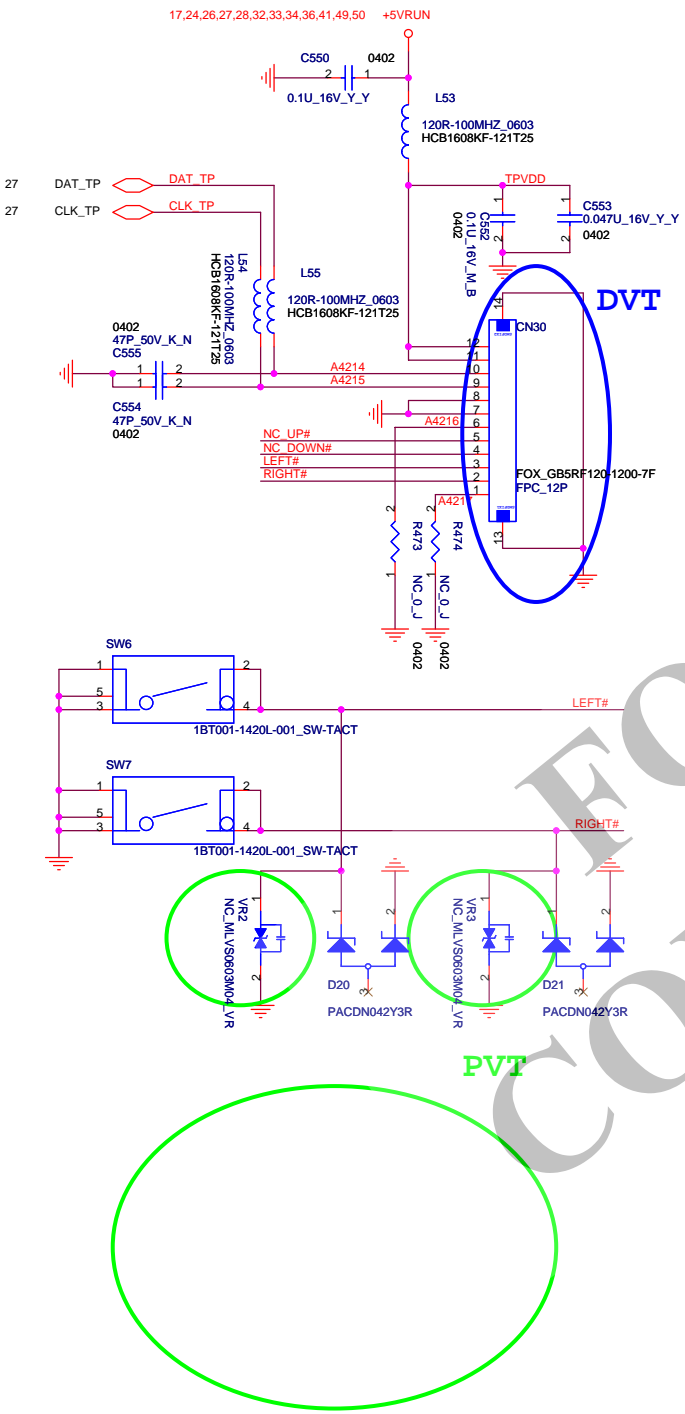
JIG-120



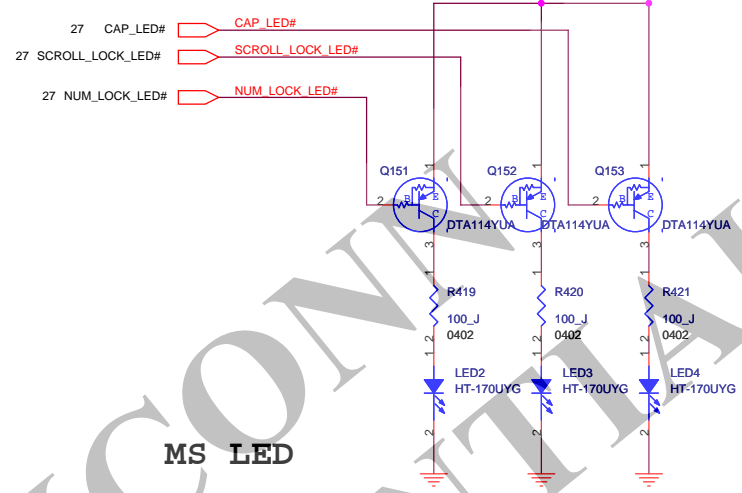
X-BUS



Touch Pad Board

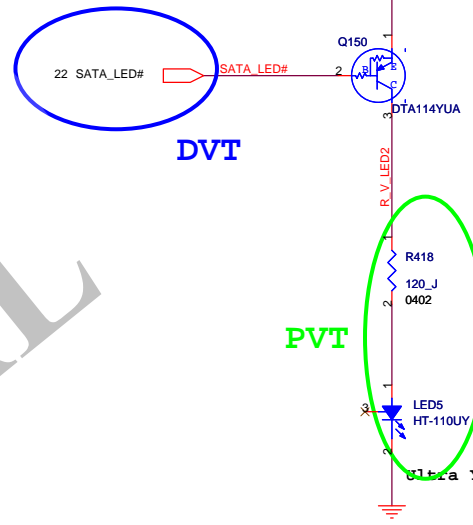


CAP_LED# SCROLL_LOCK_LED# NUM_LOCK_LED#



MS LED

HDD_LED#

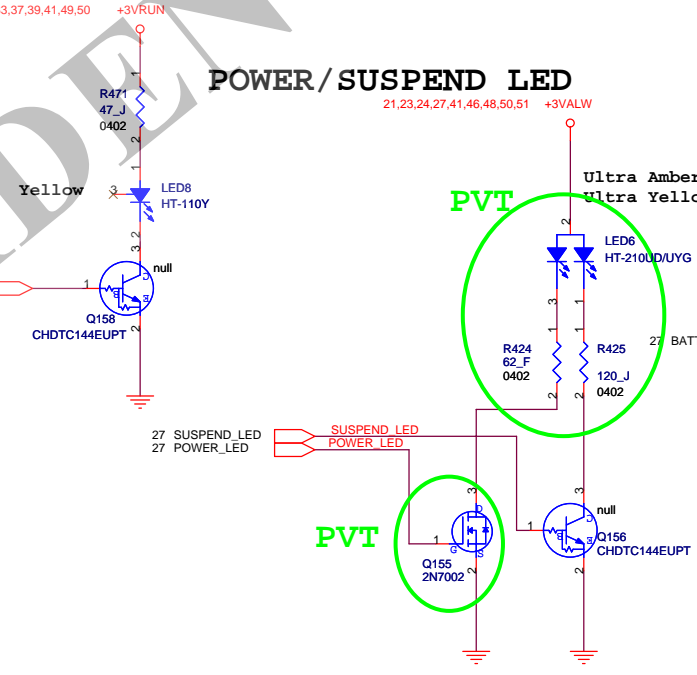


DVT

PVT

Ultra Yellow

POWER/SUSPEND LED



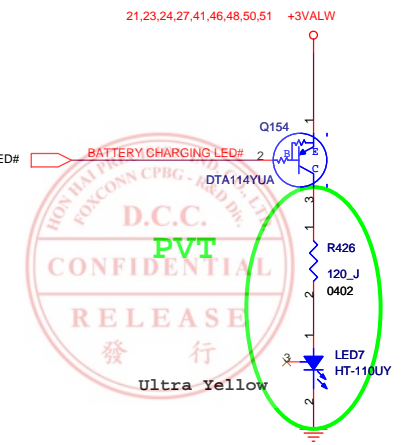
Yellow

PVT

Ultra Amber /
Ultra Yellow Green

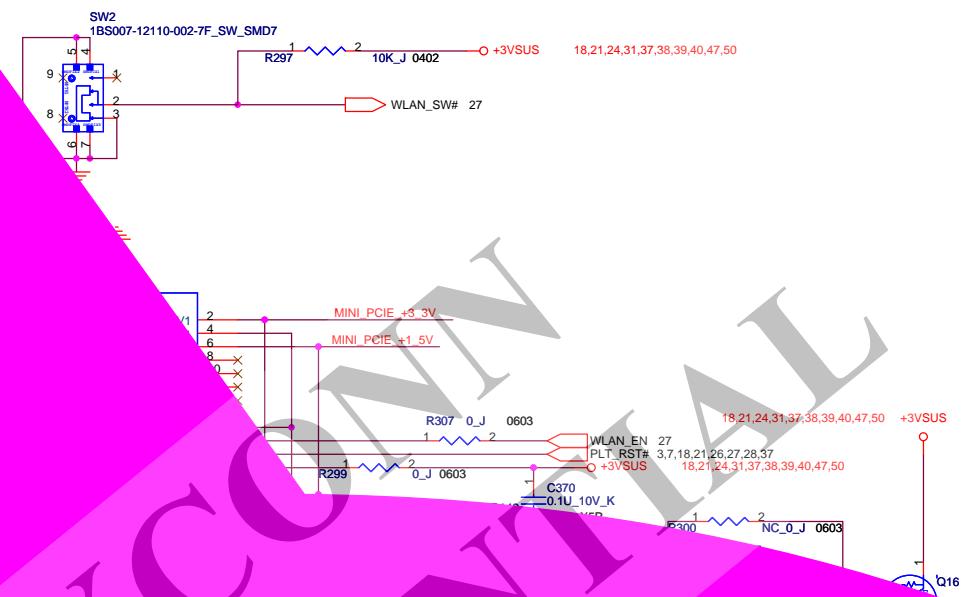
PVT

BATTERY CHARGING LED#



Ultra Yellow

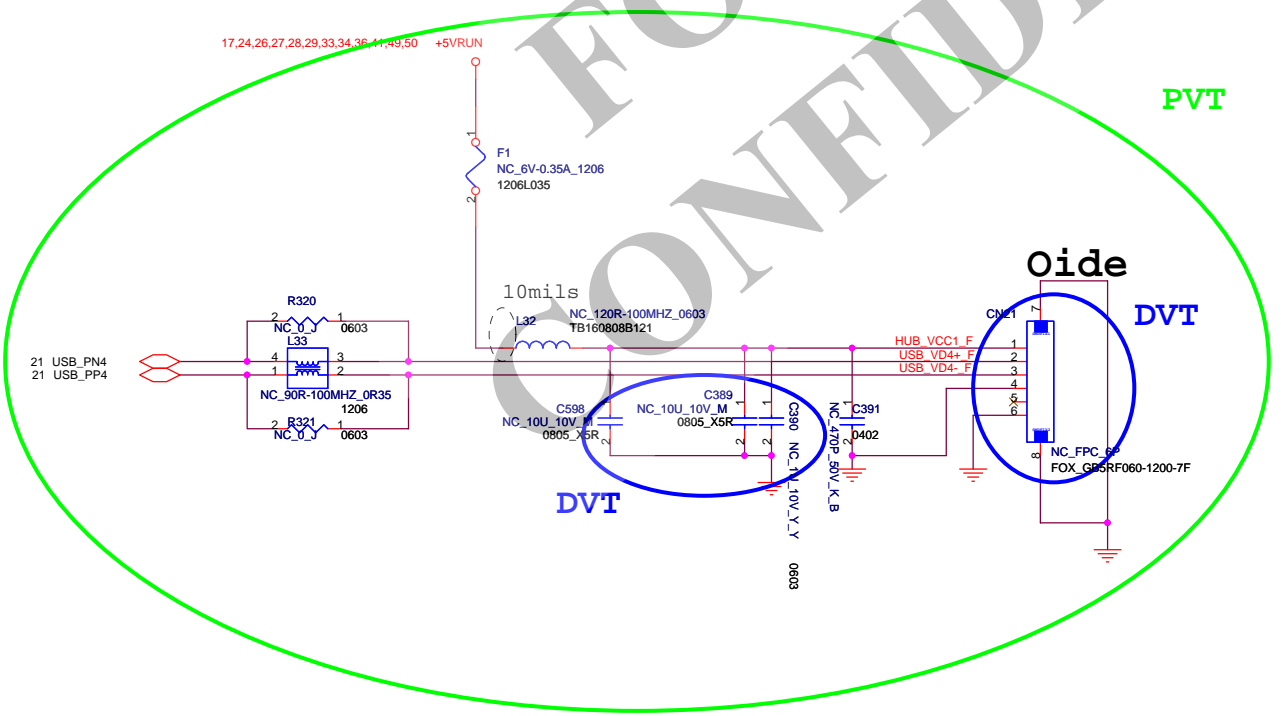
PVT



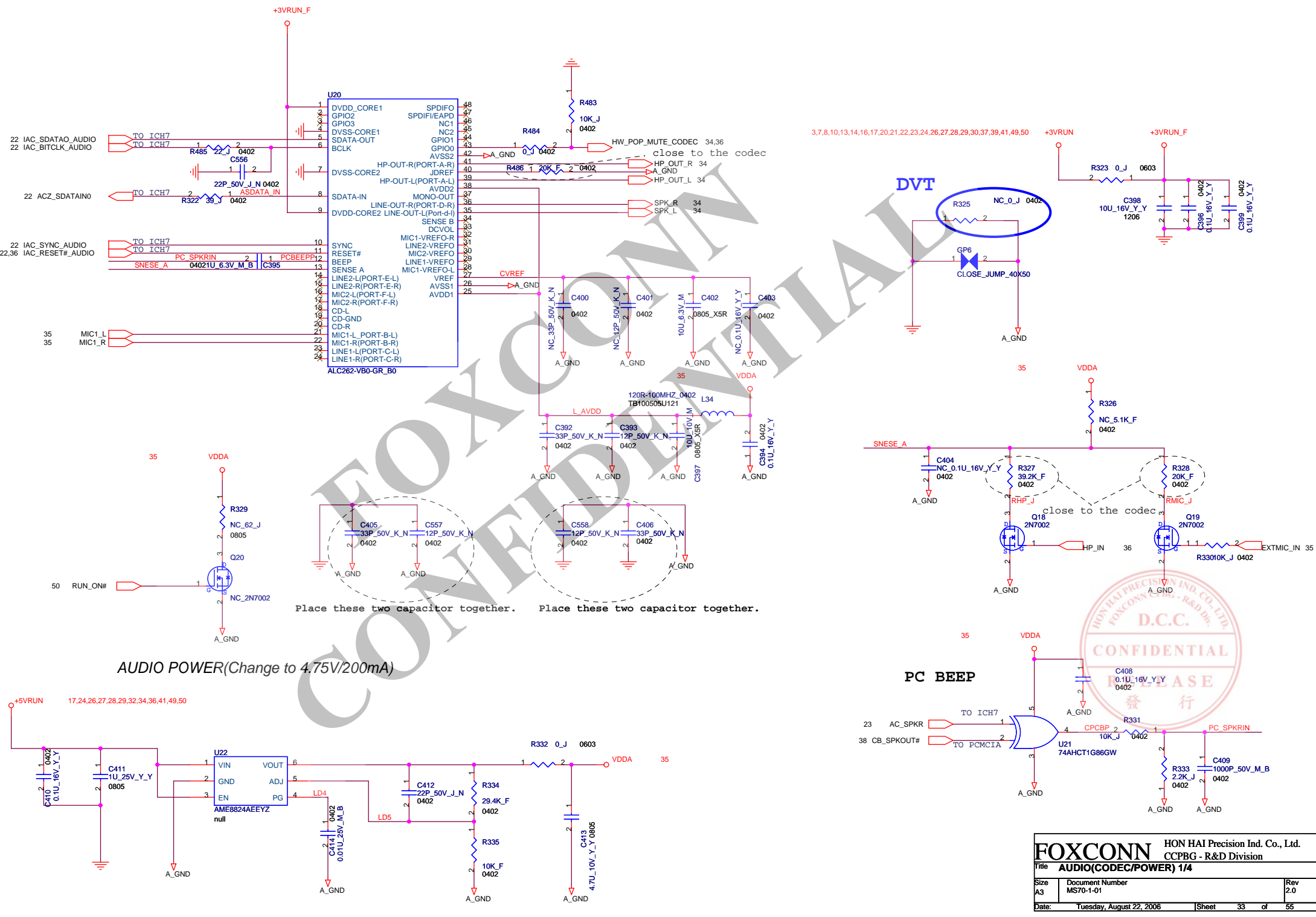
FOXC
 CONFIDENTIAL



FOXCONN CONFIDENTIAL



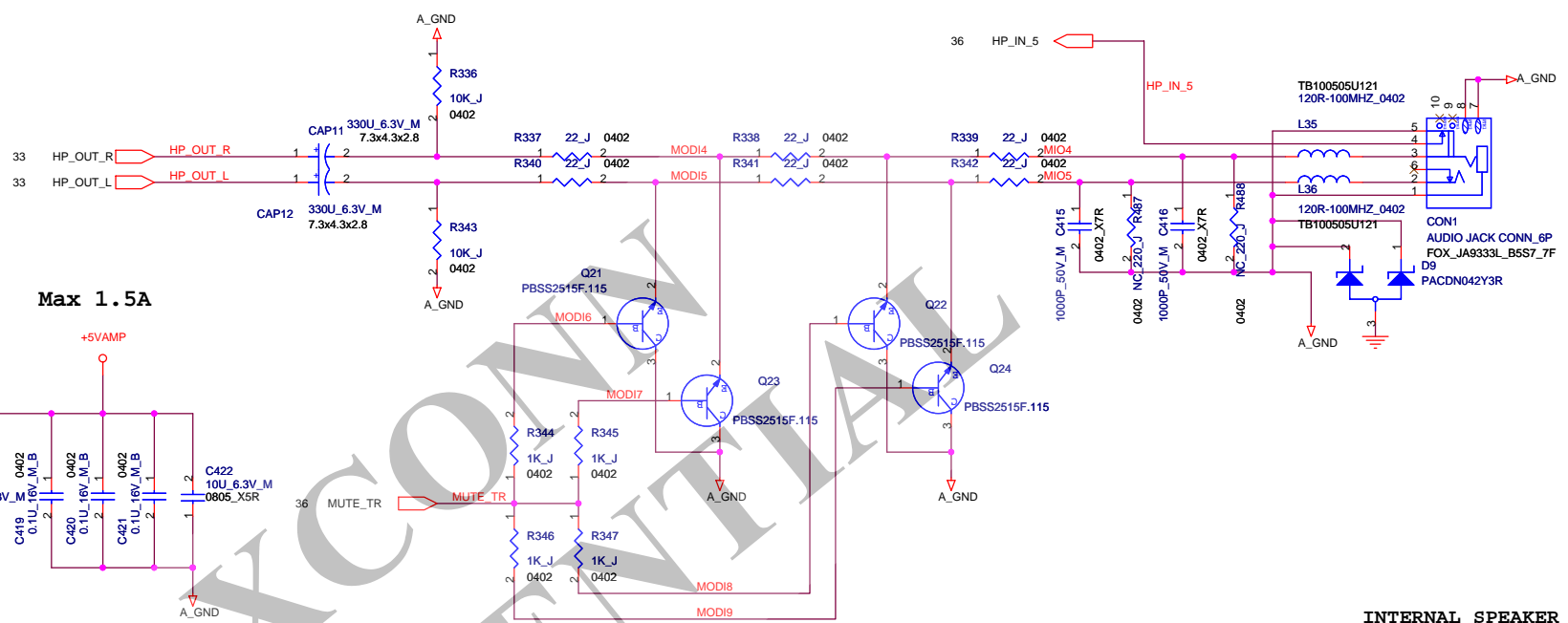
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title OIDE		CCPBG - R&D Division	
Size A3	Document Number MS70-1-01	Rev 2.0	
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Place these two capacitor together. Place these two capacitor together.

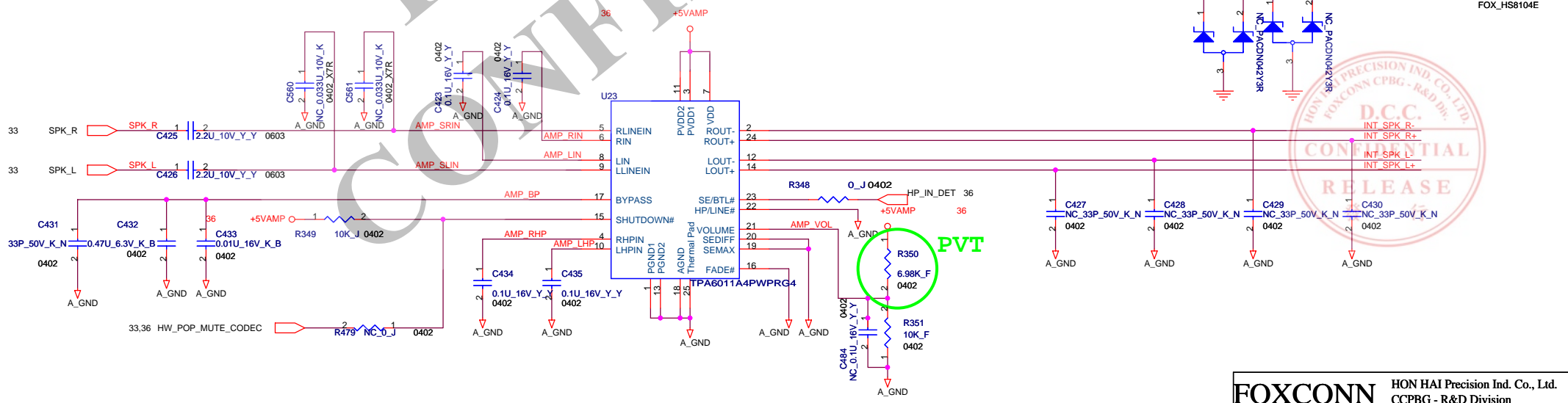
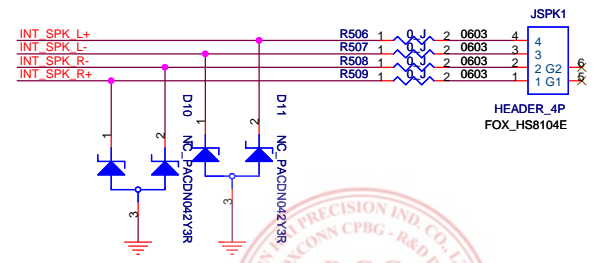
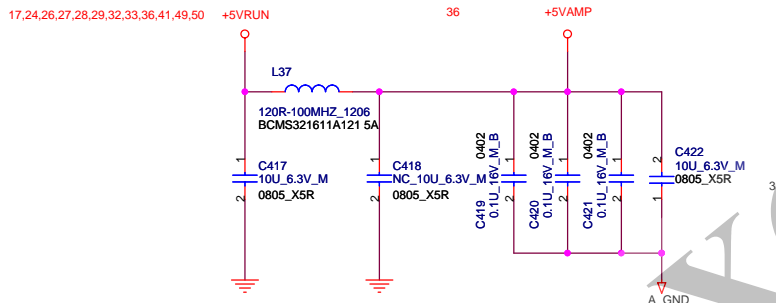
AUDIO POWER(Change to 4.75V/200mA)

PC BEEP

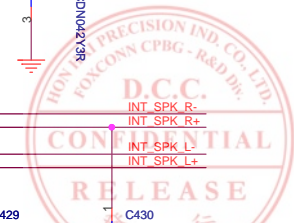


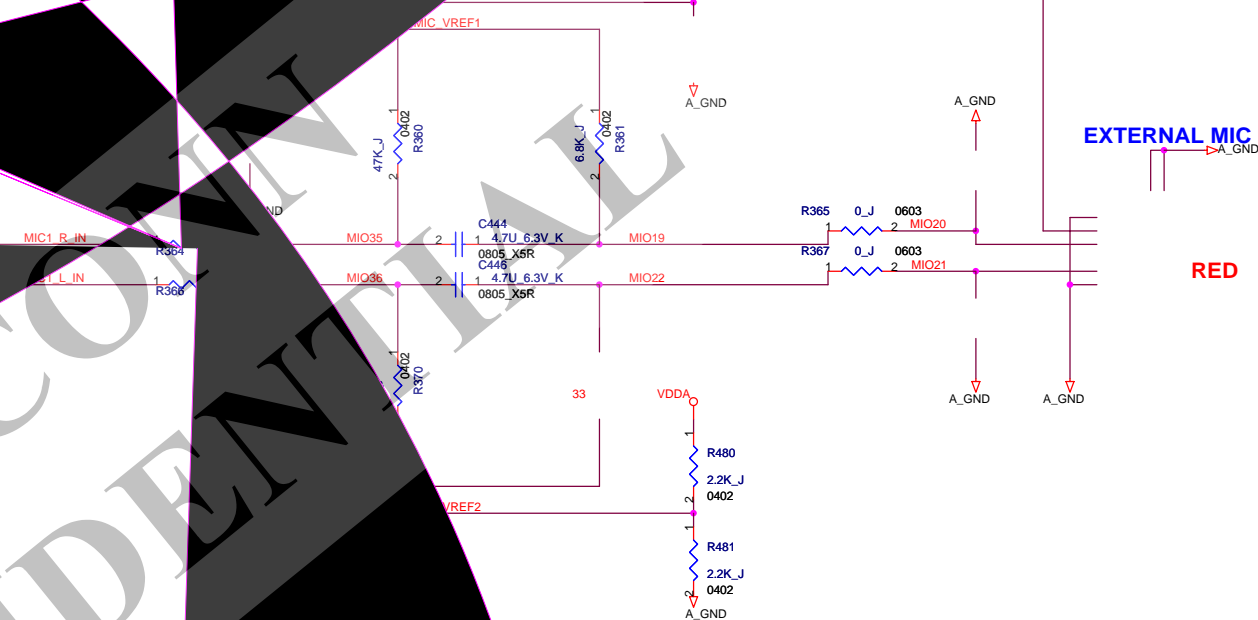
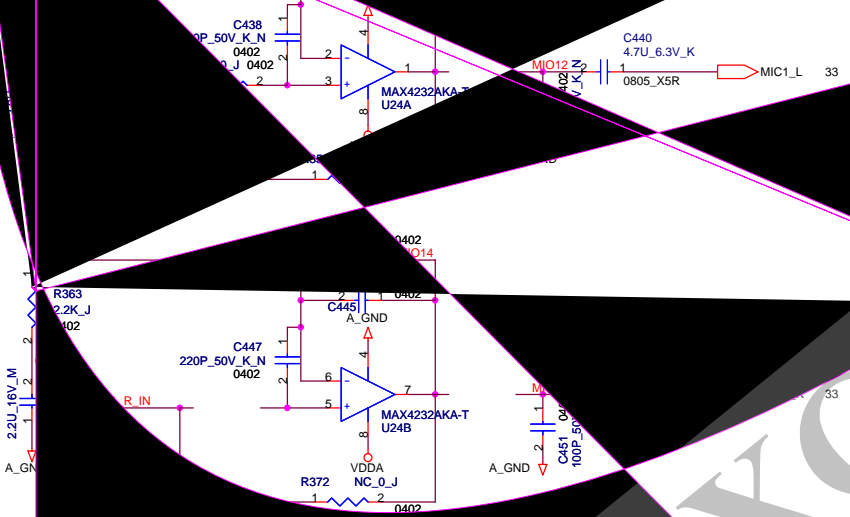
Max 1.5A

INTERNAL SPEAKER



PVT

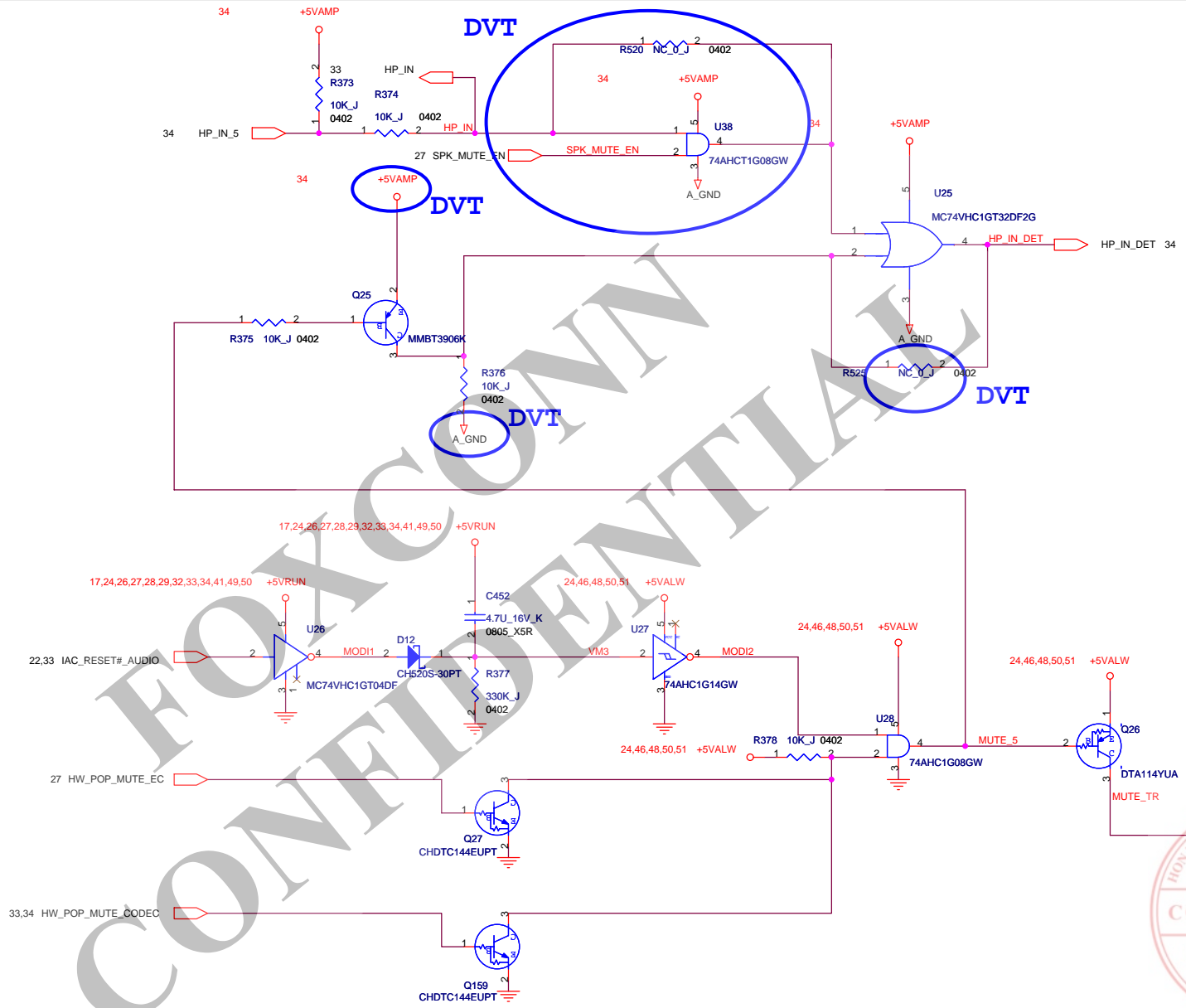




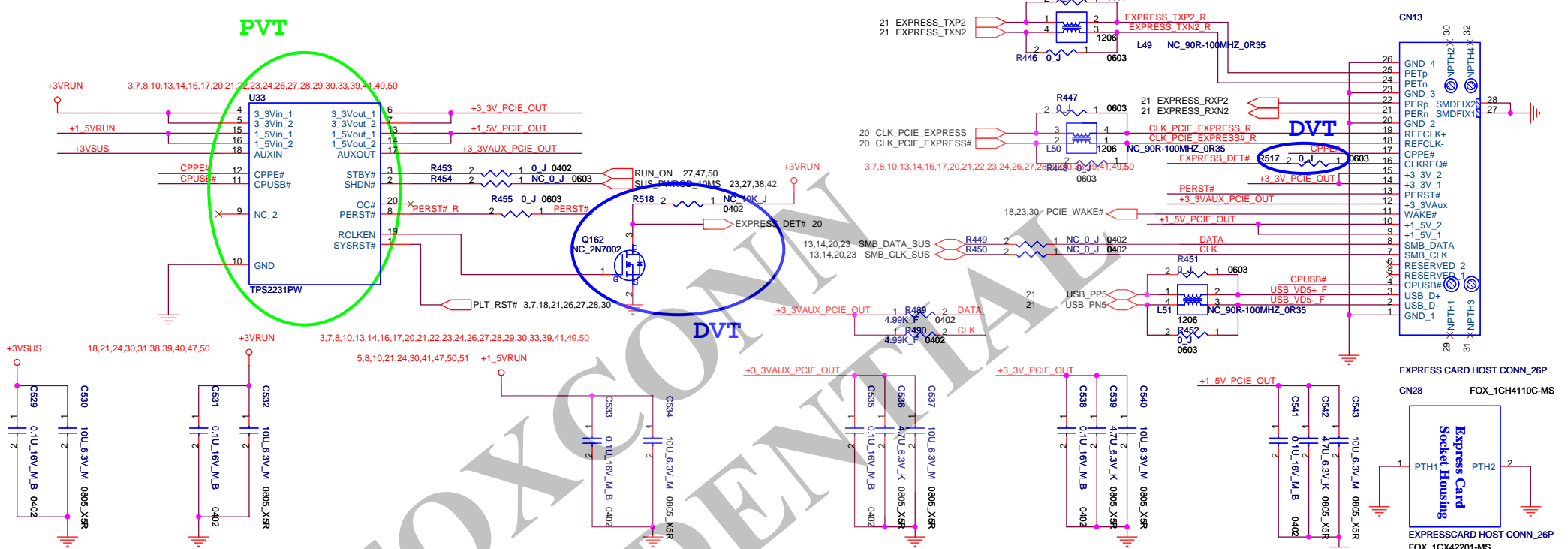
FOXCONN
CONFIDENTIAL



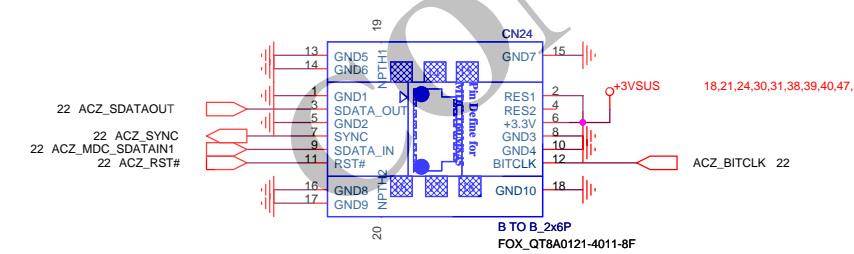
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title AUDIO(EXT MIC) 3/4		
Size A3	Document Number MS70-1-01	Rev 2.0
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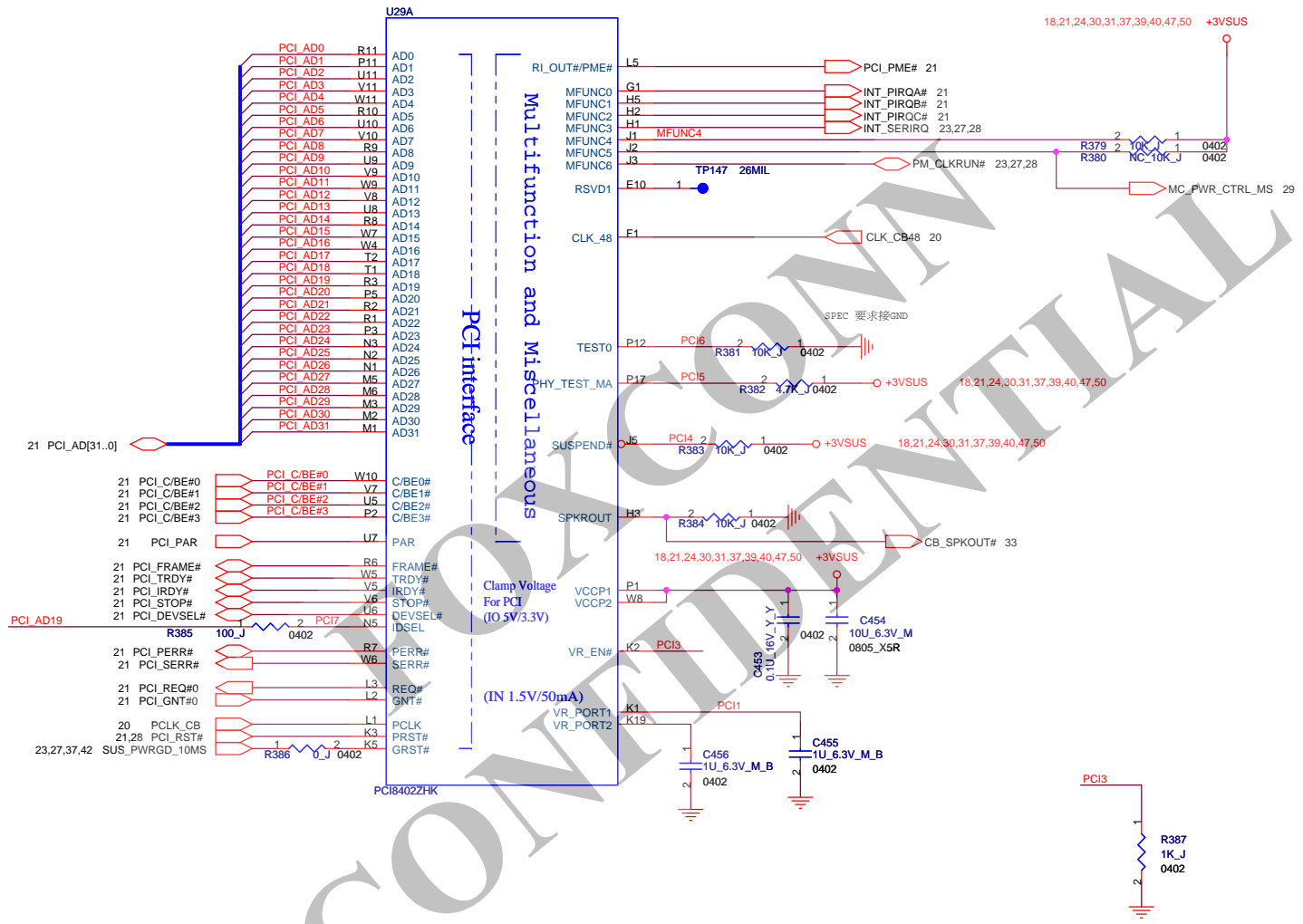


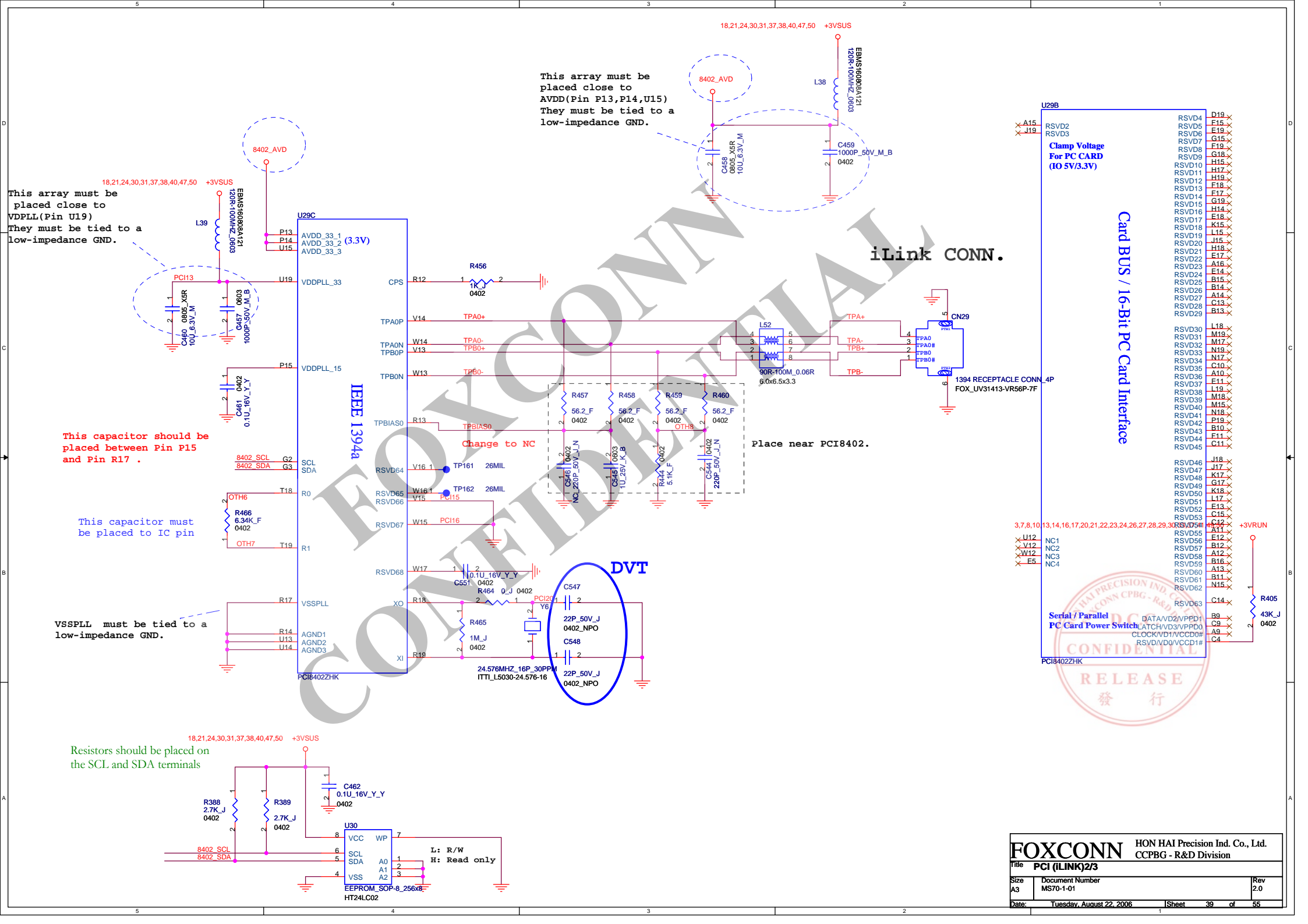
EXPRESS CONN



MDC CONN.







This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.

This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

Resistors should be placed on the SCL and SDA terminals

iLink CONN.

Place near PCI8402.

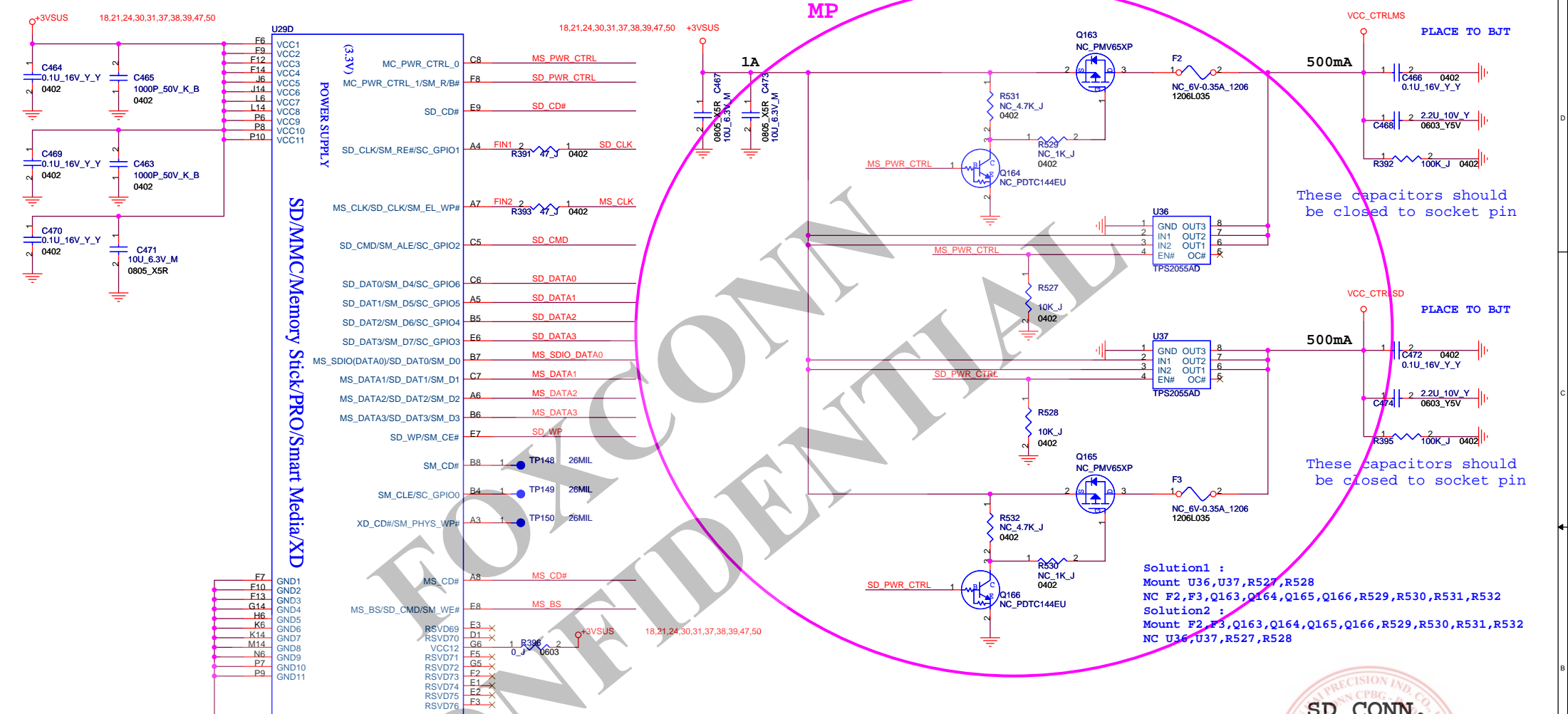
Clamp Voltage For PC CARD (IO 5V/3.3V)

Card BUS / 16-Bit PC Card Interface

Serial / Parallel PC Card Power Switch

RSVD2	RSVD4	D19
RSVD3	RSVD5	F15
	RSVD6	F19
	RSVD7	F19
	RSVD8	G18
	RSVD9	G18
	RSVD10	H15
	RSVD11	H17
	RSVD12	H19
	RSVD13	F18
	RSVD14	F17
	RSVD15	H14
	RSVD16	G19
	RSVD17	F18
	RSVD18	K15
	RSVD19	L15
	RSVD20	H18
	RSVD21	E17
	RSVD22	A16
	RSVD23	E14
	RSVD24	B15
	RSVD25	B15
	RSVD26	A14
	RSVD27	C13
	RSVD28	C13
	RSVD29	B13
	RSVD30	L18
	RSVD31	M19
	RSVD32	M19
	RSVD33	N17
	RSVD34	C10
	RSVD35	C10
	RSVD36	A10
	RSVD37	E11
	RSVD38	L19
	RSVD39	M18
	RSVD40	M15
	RSVD41	N18
	RSVD42	P19
	RSVD43	B10
	RSVD44	F11
	RSVD45	C11
	RSVD46	J18
	RSVD47	K17
	RSVD48	K17
	RSVD49	G17
	RSVD50	L17
	RSVD51	L17
	RSVD52	E13
	RSVD53	C15
	RSVD54	C12
	RSVD55	A11
	RSVD56	E12
	RSVD57	A12
	RSVD58	B16
	RSVD59	A13
	RSVD60	A13
	RSVD61	B11
	RSVD62	N15
	RSVD63	C14
	RSVD64	A11
	RSVD65	B9
	RSVD66	C9
	RSVD67	A9
	RSVD68	C4
	RSVD69	C4
	RSVD70	C4



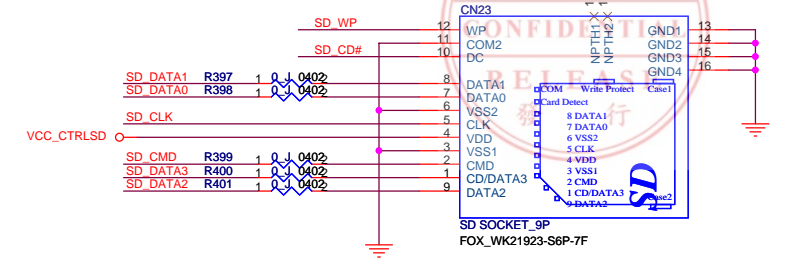
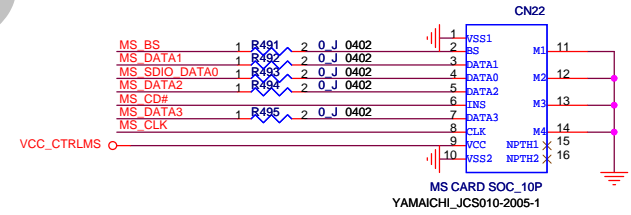
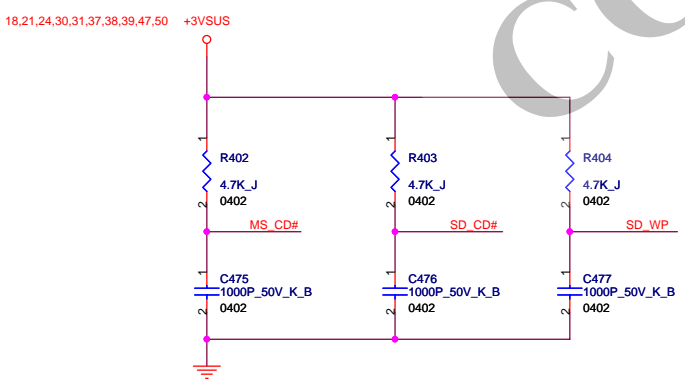


These capacitors should be closed to socket pin

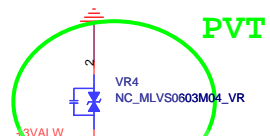
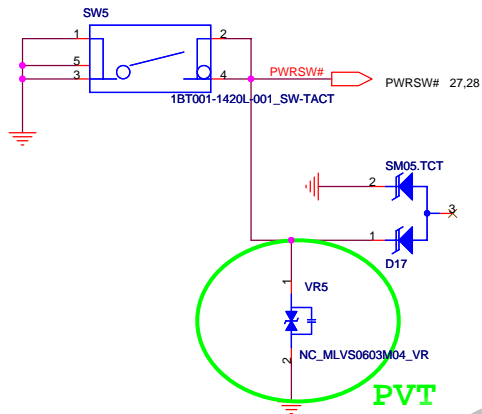
These capacitors should be closed to socket pin

Solution1 :
Mount U36, U37, R527, R528
NC F2, F3, Q163, Q164, Q165, Q166, R529, R530, R531, R532
Solution2 :
Mount F2, F3, Q163, Q164, Q165, Q166, R529, R530, R531, R532
NC U36, U37, R527, R528

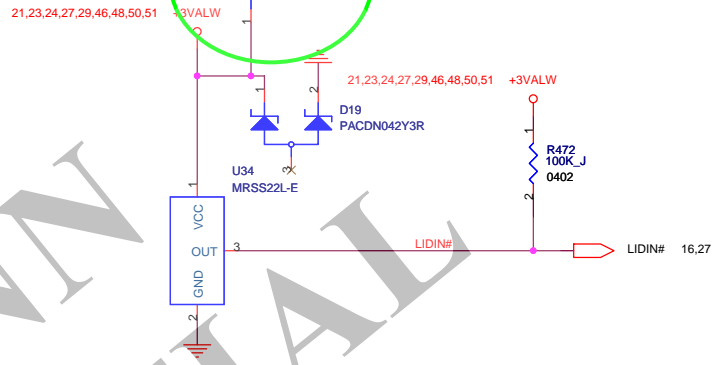
MS STD/DUO CONN.



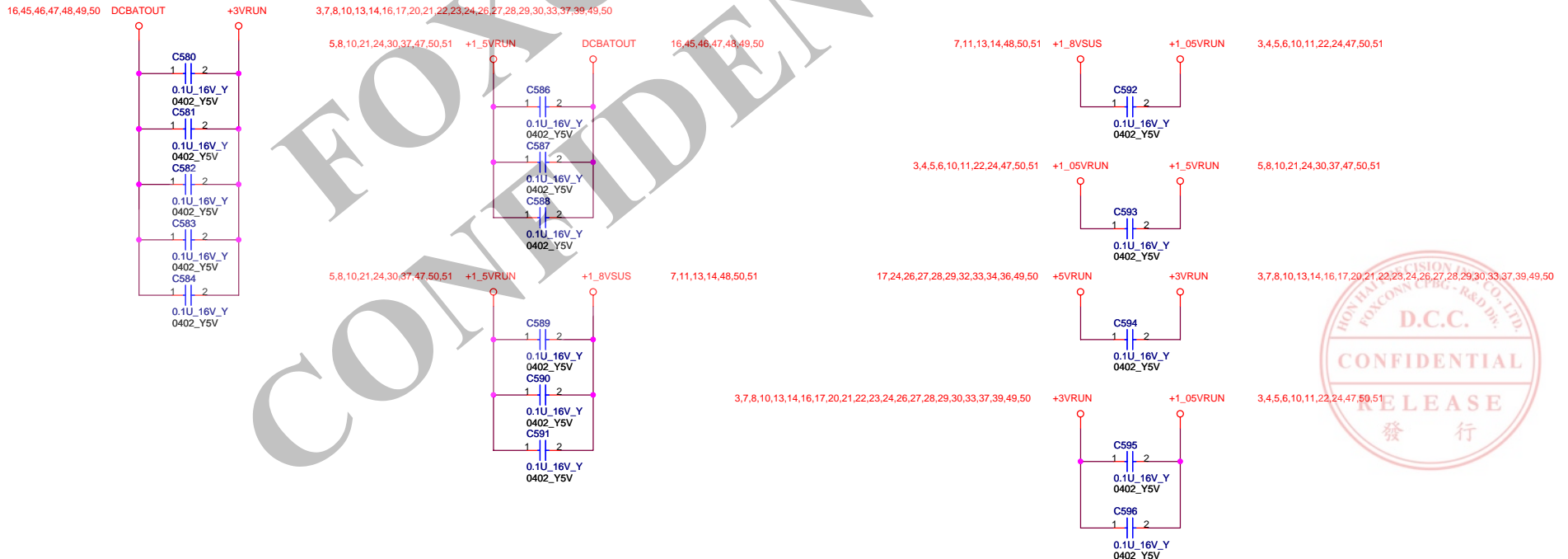
POWER BUTTON



LID Switch



EMI CAP



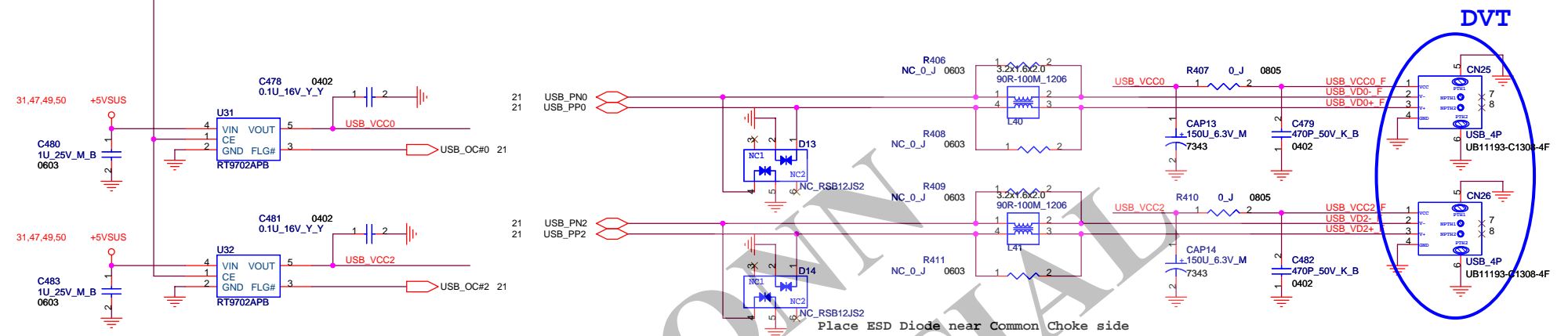
CONFIDENTIAL



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		Button/LID Switch/EMI CAP	
Size	Document Number	Rev	
A3	MS70-1-01	2.0	
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USB CONN X 2

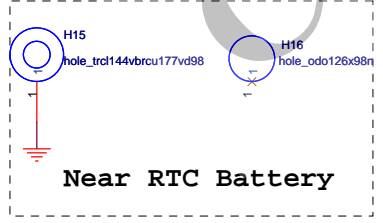
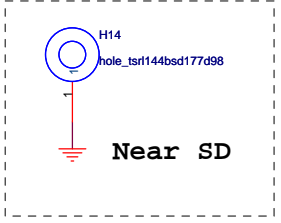
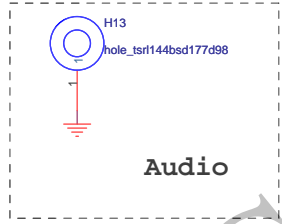
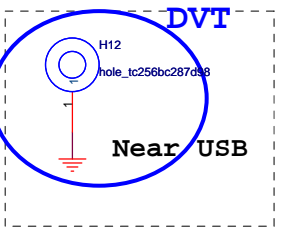
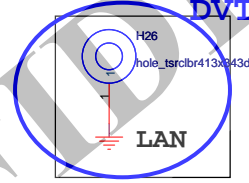
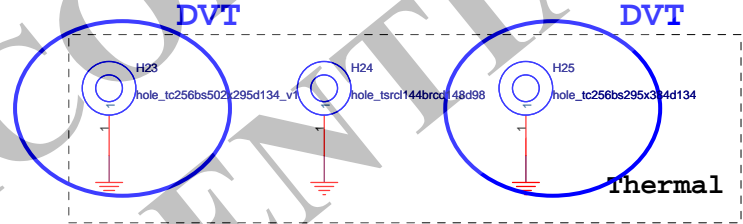
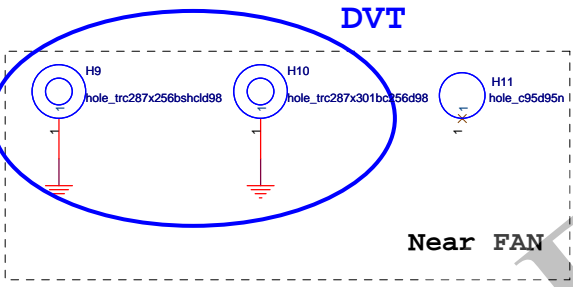
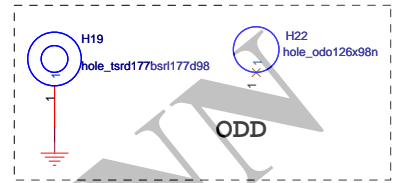
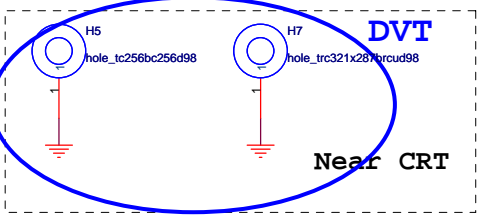
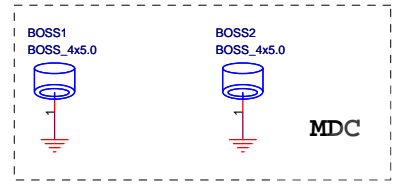
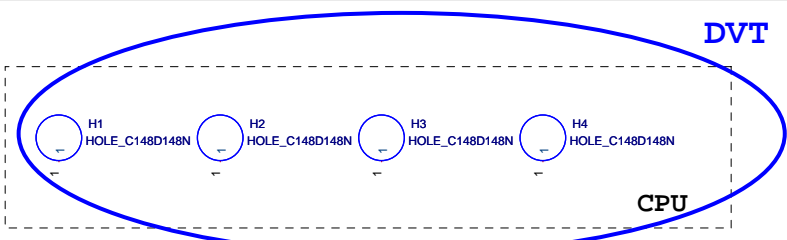
23,27,37,38 SUS_PWRGD_10MS



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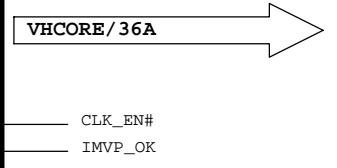
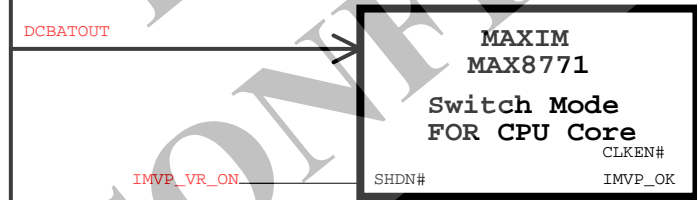
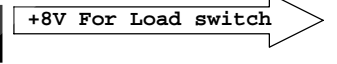
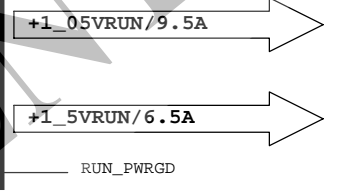
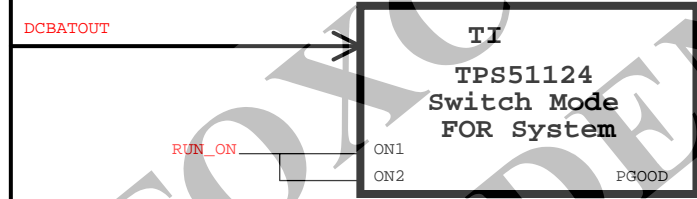
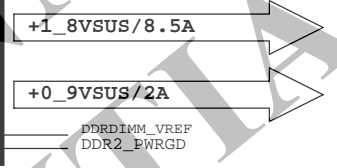
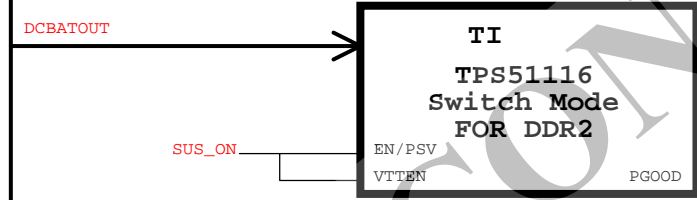
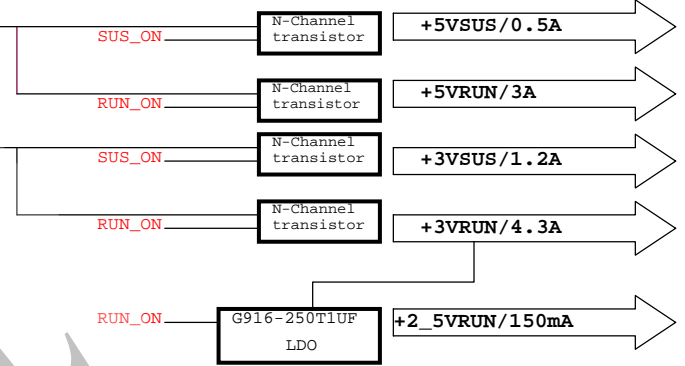
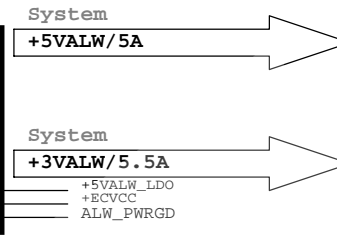
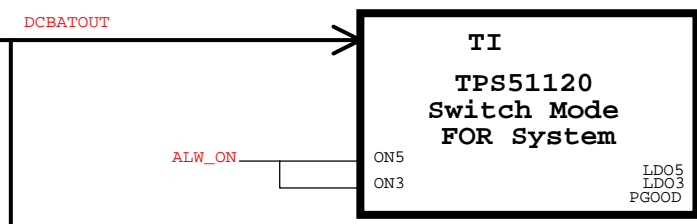
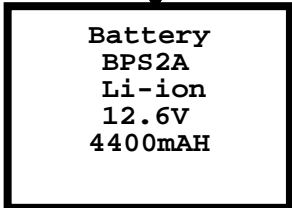
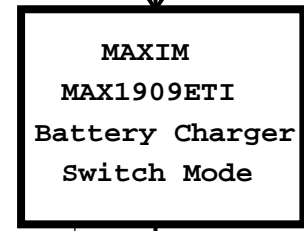
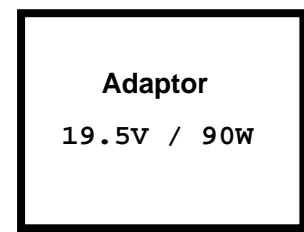
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title USB2.0		CCPBG - R&D Division	
Size A3	Document Number MS70-1-01	Rev 2.0	
Date:	Tuesday, August 22, 2006	Sheet	42 of 55



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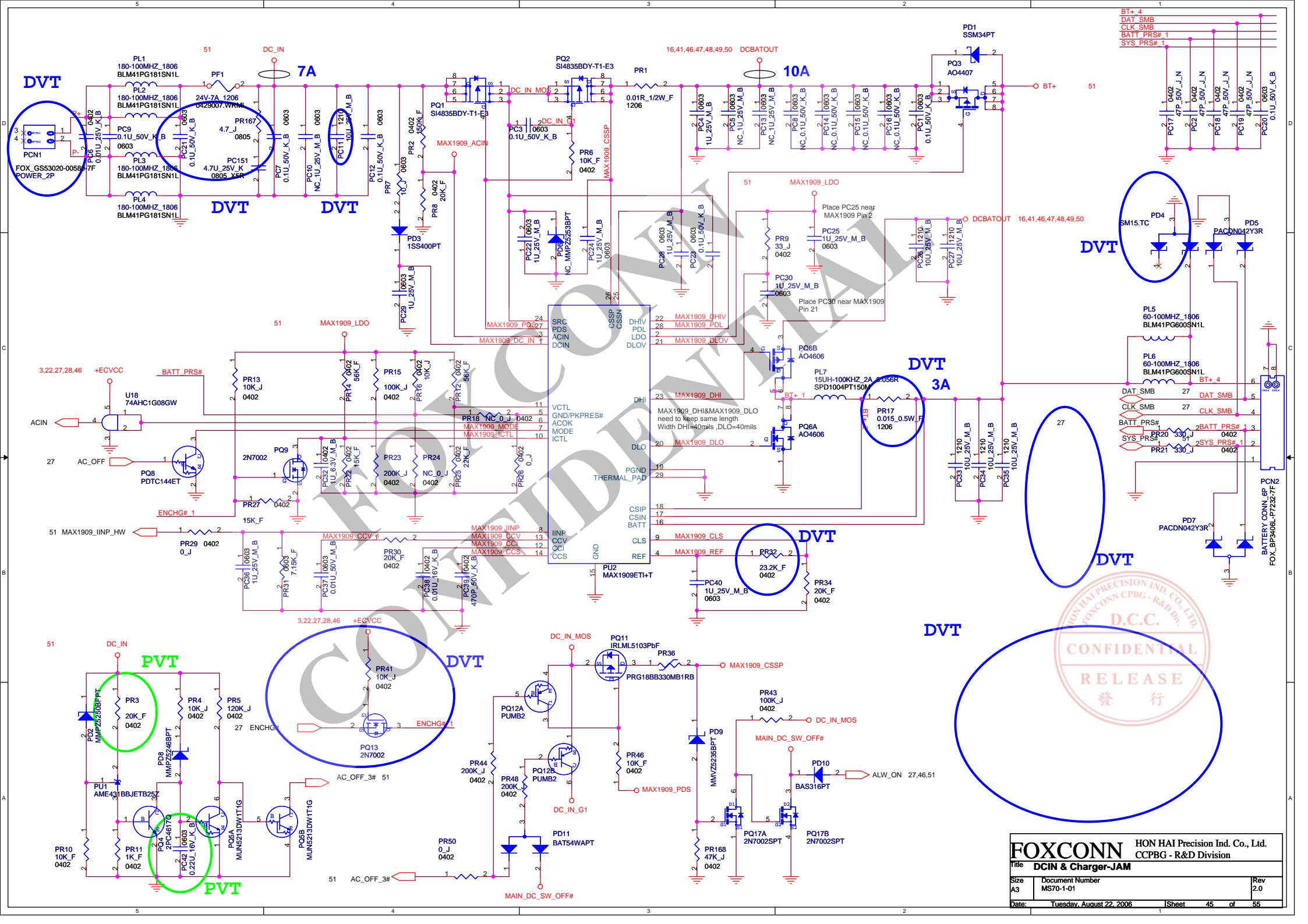
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title HOLE			
Size A3	Document Number MS70-1-01	Rev 2.0	
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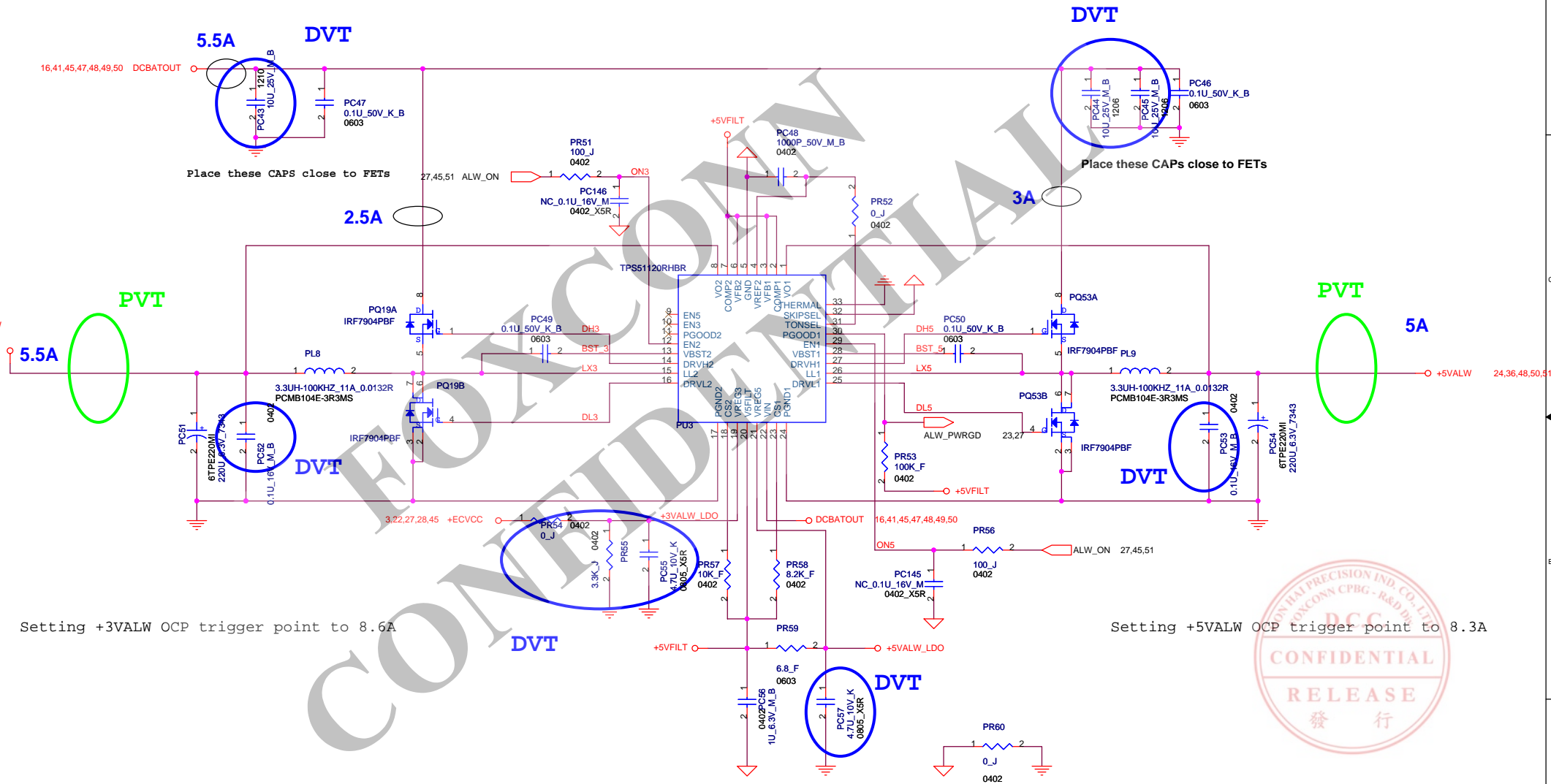


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Power Design Diagram-ZG			
Size A3	Document Number MS70-1-01	Rev 2.0	
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BT+ 4
 DAT SMB
 CLK SMB
 BATT_PRS# 1
 SYS_PRS# 1



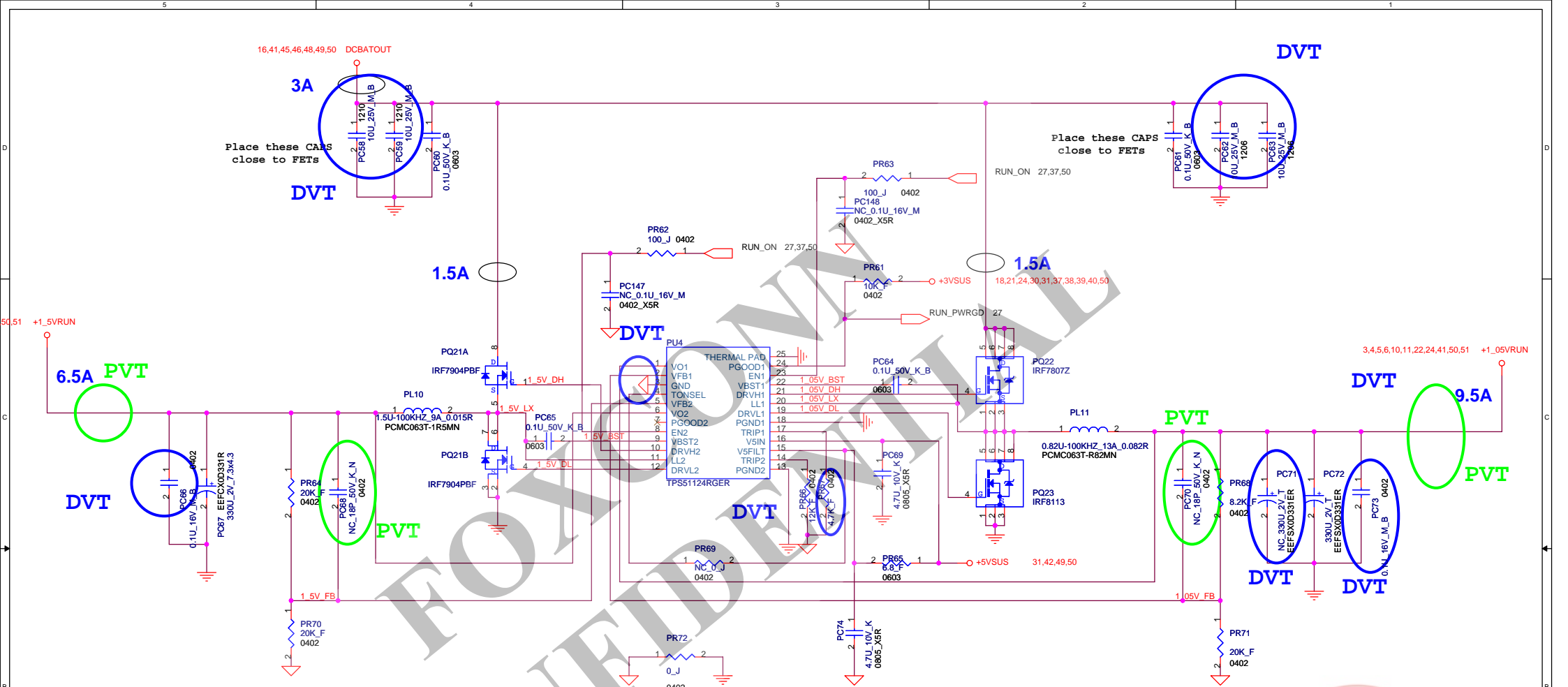


Setting +3VALW OCP trigger point to 8.6A

Setting +5VALW OCP trigger point to 8.3A



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title D/D Power-JAM		CCPBG - R&D Division	
Size A3	Document Number MS70-1-01	Rev 2.0	
Date: Tuesday, August 22, 2006	Sheet 46	of 55	

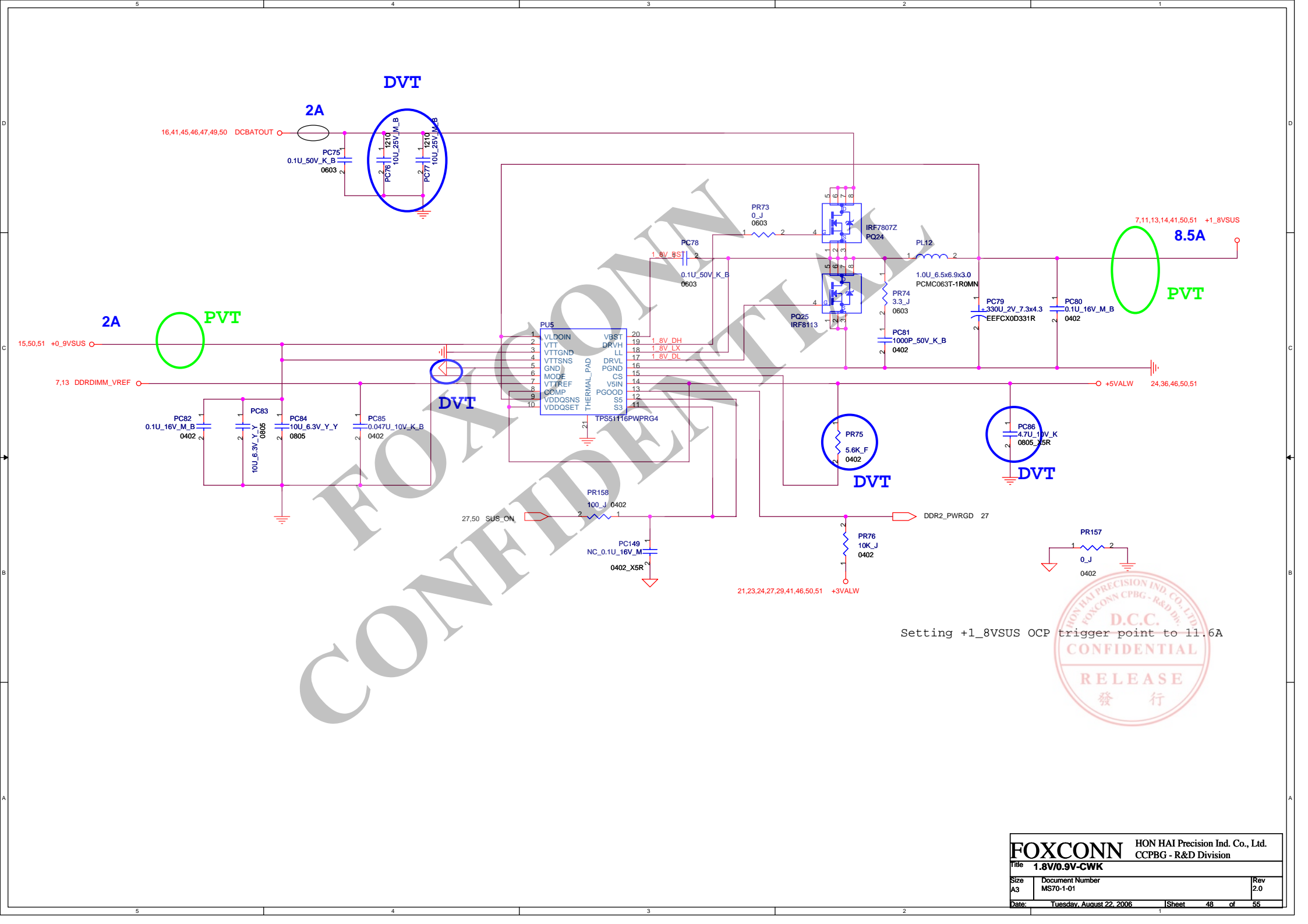


Setting +1_5VRUN OCP trigger point to 10.5A

Setting +1_05VRUN OCP trigger point to 12.8A



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title 1.5V/1.05V-JAM		
Size A3	Document Number MS70-1-01	Rev 2.0
Date Tuesday, August 22, 2006	Sheet 47	of 55

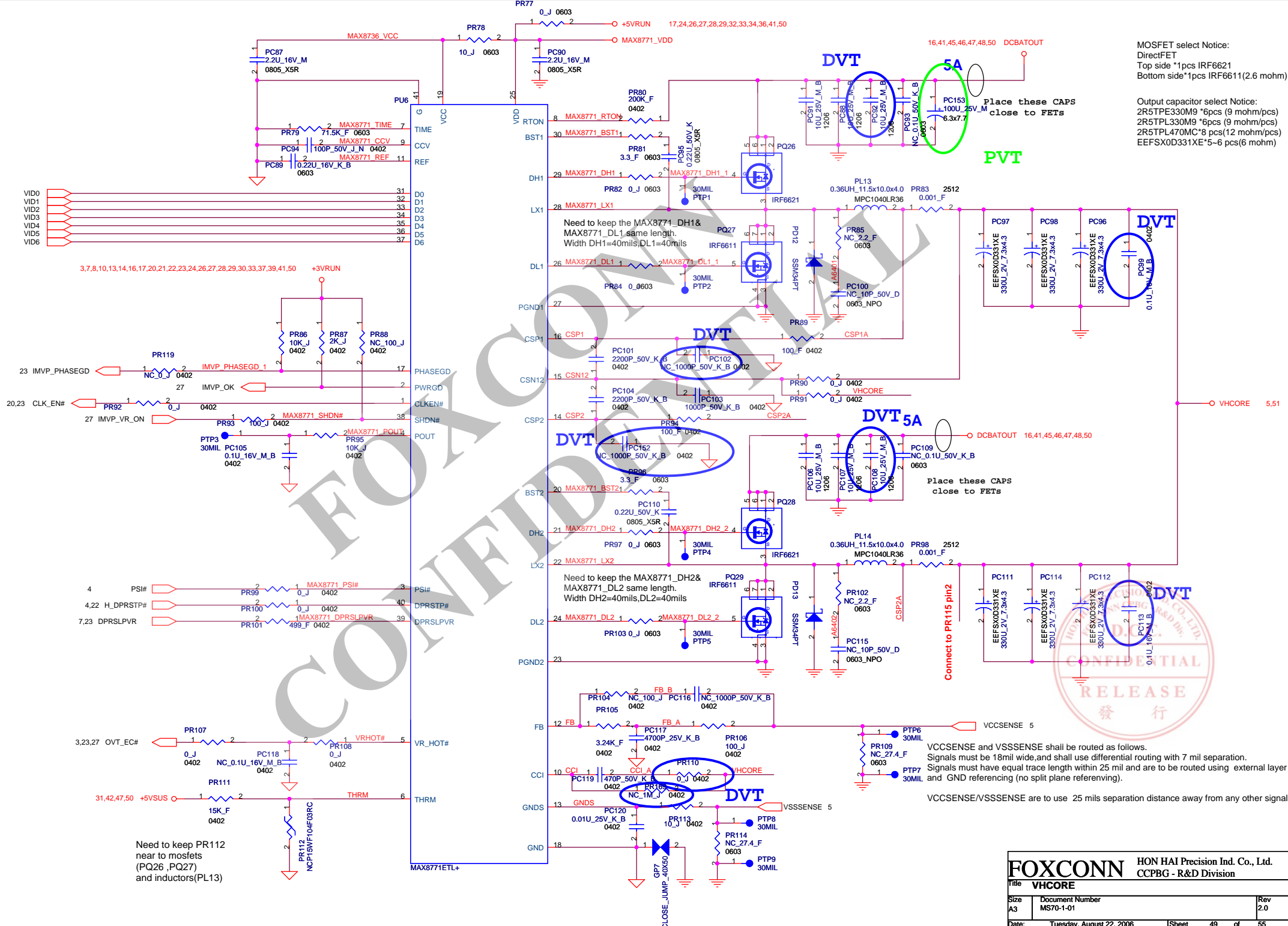


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Setting +1_8VSUS OCP trigger point to 11.6A



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title 1.8V/0.9V-CWK		
Size A3	Document Number MS70-1-01	Rev 2.0
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MOSFET select Notice:
 DirectFET
 Top side *1pcs IRF6621
 Bottom side *1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:
 2R5TPE330M9 *6pcs (9 mohm/pcs)
 2R5TPL330M9 *6pcs (9 mohm/pcs)
 2R5TPL470MC *8 pcs(12 mohm/pcs)
 EEFSXOD331XE*5-6 pcs(6 mohm)

Place these CAPS close to FETs

PVT

DVT

DVT

DVT 5A

Place these CAPS close to FETs

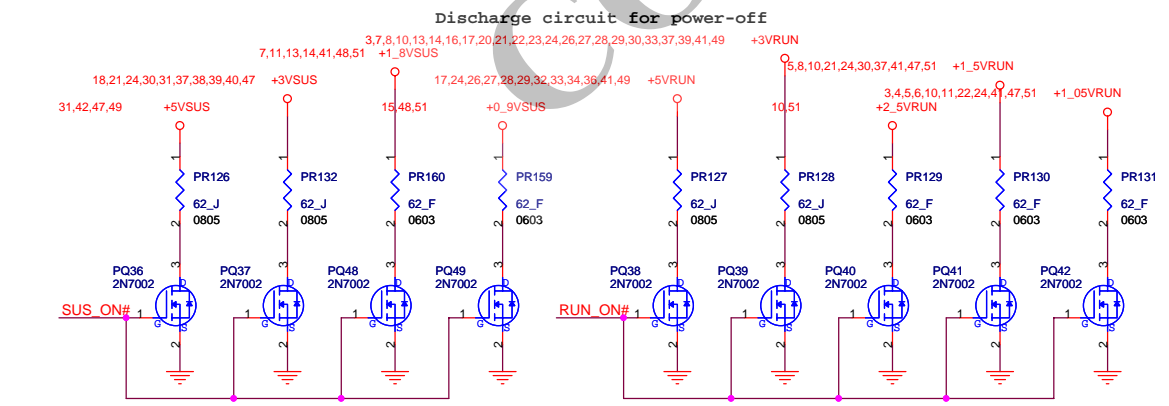
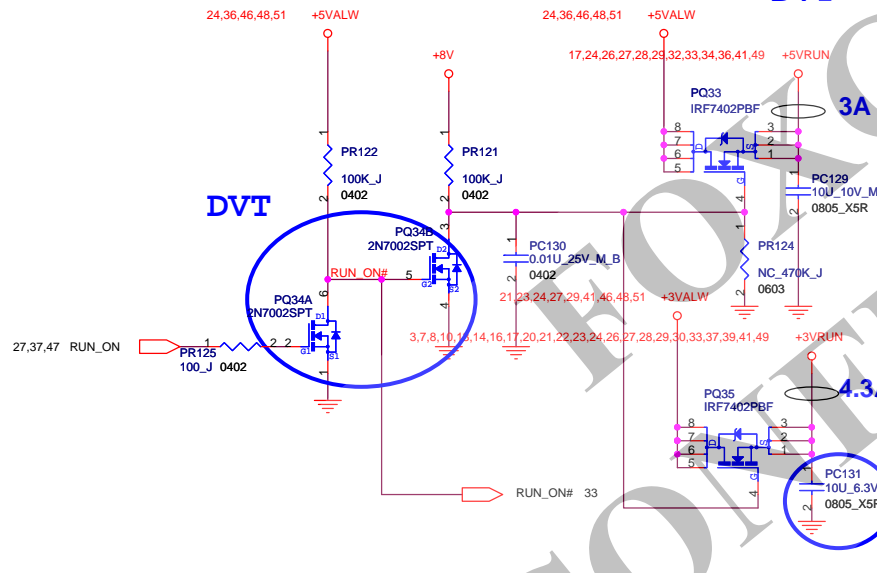
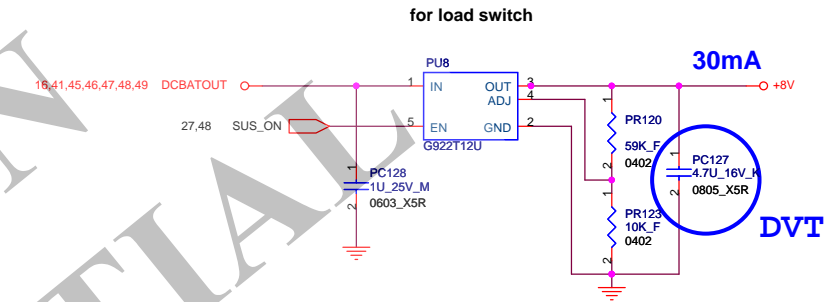
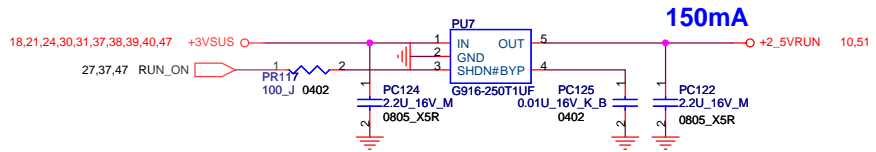
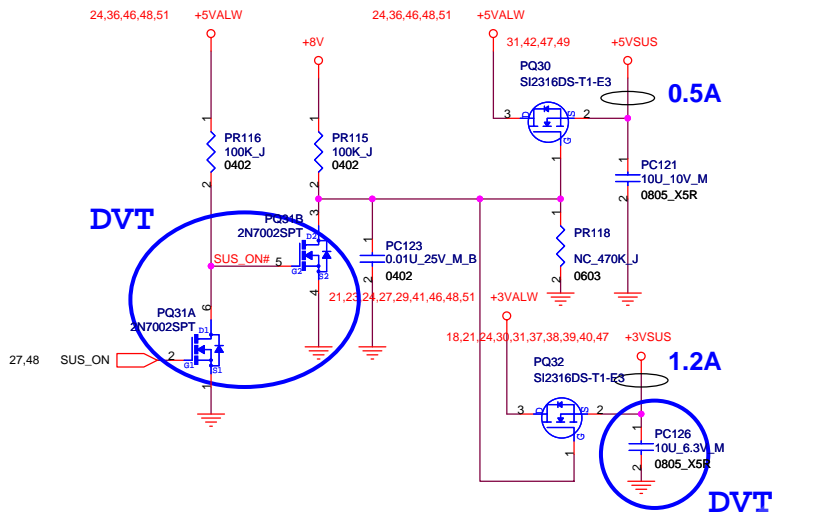
DVT

VCCSENSE and VSSSENSE shall be routed as follows.
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
 Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referencing).

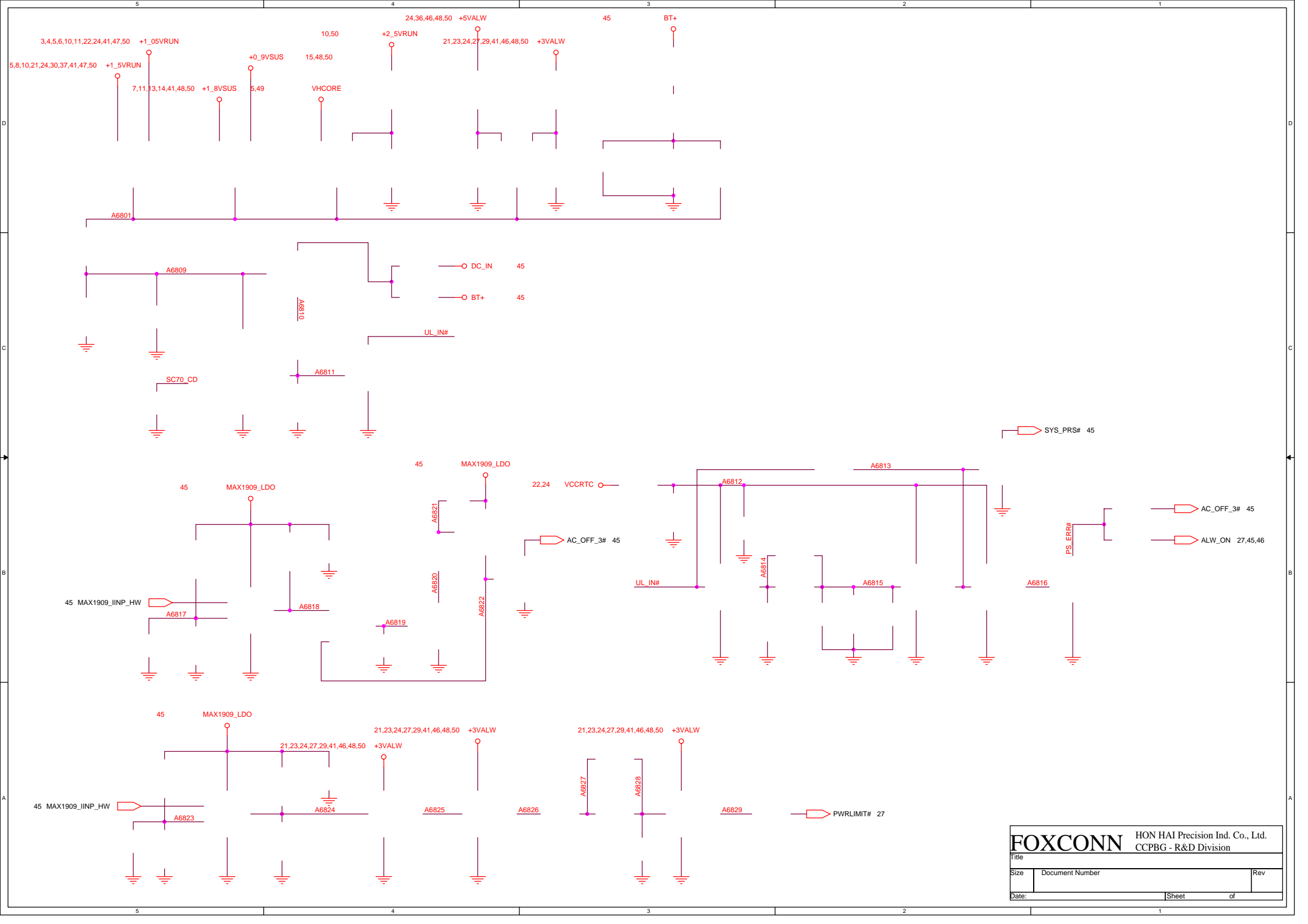
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

Need to keep PR112 near to mosfets (PQ26, PQ27) and inductors(PL13)

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
		Title VHCORE
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FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title Other power plan-ZG		
Size A3	Document Number MS70-1-01	Rev 2.0
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HISTORY (1)

(2006/04/25)

P.16 CN3 pin5 Add R515 0ohm for QDI LCD Panel doesn't support gamma correction issue.
P.17 Add VGA_CRT_DET# connect to U15 pin29 for Semi-PnP function fail issue.
P.20 U11 pin57 add R516 10Kohm pull down for LAN can't be recognized issue.
P.27 U15 pin29 add R513 10Kohm pull up for Semi-PnP function fail issue.
P.27 U15 pin12 add R514 100Kohm pull down for EC hardware strap pin.
P.27 U15 pin171 add C597 1000pF to ground for FAN can't be controlled issue.
P.31 R304 change from 4.7k to 10k for FAN can't be controlled issue.

(2006/05/03)

P.49 Add netname(IMVP_PHASEGD_1) on the right side of PR119 for application modification.
P.45 PC11, PC21, PC151, PR167 change from DNI to mount for DC_IN spike issue
P.45 PD4 pin1 and pin3 exchange for application modification
P.46 PR54 change from 100 ohm to 0 ohm for PU3 output abnormal issue
P.46 PR55 change from DNI to mount for can't boot up issue
P.47 PU4 pin3 change from GND to GND_SIGNAL_1D5V for application modification
P.48 PU5 pin5 change from GND to GND_SIGNAL_1D8V for application modification
P.49 Add PR169 NC_1M ohm for MAX8771 CCI issue
P.49 PC96, PC97, PC98, PC111, PC112, PC114 change from SANYO 2R5TPL330M9 to Panasonic EEPFX0D331XE for purchase difficult

(2006/05/04)

P.37 Add Q162(NC), R517, R518(NC) for Express card power sequence issue

(2006/05/15)

P.45 PR32 change from 22K_F to 23.2K_F for ACIN Vcls function trigger point correct to 3.4A
P.47 PR67 change from 8.2K_F to 4.7K_F for +1_05VRUN OCP trigger point correct to 12.8A
P.48 PR75 change from 6.8K_F to 5.6K_F for +1_8VSUS OCP trigger point correct to 11.6A
P.51 PR146 change from 51K_F to 46.4K_F for DCBATOUT OCP trigger point correct to 4.2A
P.51 PR150 change from 62K_F to 56K for PWRLIMIT# function trigger point correct to 3.6A
P.46 Delete PJ1, PJ2
P.47 Delete PJ3, PJ4, PJ5, PJ6
P.48 Delete PJ7, PJ8, PJ9

(2006/05/17)

P.45 Add PR41 10K_J_0402 and PQ13 2N7002 for preventing leakage current
P.45 PR17 change from 0.015_J 0805 to 0.015_F 1206 for application modification
P.46 PR55 change from 1K_J to 3.3K_J and PC55, PC57 change from 10u_25V_X5R 1206 to 4.7u_10V_X5R 0805 for reducing +ECVCC static current
P.47 PC71 change from mount to DNI for application modification
P.49 PR110 change from 20K_J to 0_J and PC102 change from DNI to mount for MAX8771 CCI issue
P.45 Delete PR19, PR28, PR33, PR35, PR37, PR38, PR39, PR40, PC31, PQ7, PQ10, PQ14, PQ16 For +ECVCC needed to work in battery only mode
P.51 Delete PD36, PD37 for +ECVCC needed to work in battery only mode
P.51 The net of VSOURCE (PQ43 pin3) change to DCBATOUT for +ECVCC needed to work in battery only mode
P.51 The net of BATT_EN (PD38 pin2) change to ALW_ON for +ECVCC needed to work in battery only mode

(2006/05/19)

P.13 C155 change from 2.2U_10V_Y_Y to 1000P_16V_K ; C159 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.14 C168 change from 2.2U_10V_Y_Y to 1000P_16V_K ; C172 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.15 C177,C179,C181,C191,C192,C196 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.39 C547,C548 change from 18P_50V_J_N to 22P_50V_J for PC18402's Crystal issue
P.30 LED1 change from HT-110Y to HT-110UYG for LED color requirement
P.45 PCN1 change from MOLEX_53259-0229 to FOX_GS53020-00580-7F
P.45 PC11 change from 10U_25V_M_1206 to 10U_25V_M_B_1210 for purchase convenient
P.46 PC43,PC44,PC45 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.47 PC58,PC59,PC62,PC63 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.48 PC76,PC77 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.48 PC86 change from 4.7U_10V_K_B_1206 to 4.7U_10V_K_0805 for purchase convenient
P.50 PC126,PC131 change from 10U_10V_M to 10U_6.3V_M for purchase convenient
P.50 PC127 change from 4.7U_25V_K_B_1206 to 4.7U_16V_K_0805 for purchase convenient

(2006/05/22)

P.32 CN21 change from FOXCONN_GB11060_0221_7F to FOXCONN_GB5RF060_1200_7F for ME's requirement
P.29 CN30,CN31 change from foxconn_gb11120_0221_7F to FOXCONN_GB5RF120_1200_7F for ME's requirement
P.29 CN31 change from mount to DNI for ME's requirement
P.50 PQ31,PQ34 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient
P.51 PQ45 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient
P.27 Q149 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient

(2006/05/23)

P.47 PC62,PC63 change from 10U_25V_M_B_1210 to 10U_25V_M_B_1206 for ME limit of height
P.46 PC44,PC45 change from 10U_25V_M_B_1210 to 10U_25V_M_B_1206 for ME limit of height
P.46 Add PJ1,PJ2 for test request
P.47 Add PJ3,PJ4 for test request
P.48 Add PJ7,PJ9 for test request

(2006/05/24)

P.42 CN25,CN26(USB CONN) change from FOX_UB11193_C1301_4F to UB11193-C1308-4F for ME's requirement
P.17 CN5(VGA CONN) change from FOX_DZ11A91_MB221_4F to DZ11A91-MW223-4F for ME's requirement

(2006/05/25)

P.47 Add PJ6 for test request
P.26 CN8 footprint change from FOXCONN_LD2722H_S469 to FOXCONN_LD2722H_S469_MS70 for ME PAD request
P.32 C389 change from 22U_10V_Y_Y_1206 to 10U_10V_M_0805 and add C598 10U_10V_M_0805 for limit of ME
P.43 H1,H2,H3,H4 change from hole_c158d158n to HOLE_C148D148N for ME request
P.43 H7 change from hole_tsru144bsru177d98 to hole_trc321x287brud98 for ME request
P.43 H26 change from hole_c120d100 to hole_tsrlbr413x343d98 for ME request
P.43 H23 change from hole_tc256brcl295d98_v1 to hole_tc256bs502x295d134_v1 for ME request
P.43 H25 change from hole_tc256brcl148d98 to hole_tc256bs295x384d134 for ME request
P.43 H5 change from hole_tc256bc315d98 to hole_tc256bc256d98 for ME request
P.43 H10 change from hole_tshrd144bc315d98 to hole_trc287x301bc256d98 for ME request
P.43 H9 change from hole_trcd144brcl177d98 to hole_trc287x321brcd98 for ME request
P.43 H12 change from hole_tc256bsrcu144d98 to hole_tc256bc287d98 for ME request

(2006/05/26)

P.42 CN25,CN26 change from FOXCONN_UB11193_C1308_4F to FOXCONN_UB11193_C1308_4F_HM for solder issue
P.43 H9 change from hole_trc287x321brcd98 to hole_trc287x256bshcd98 for ME request
P.17 D3 change from 16-CH500H4-0P00 to 16-SCS500V-4000 for purchase convenient
P.10 C119 change from 1C-2B30105-K000 to 1C-2B30475-K100 ;
C120 change from 1C-2B20103-K001(0402) to 1C-2B30475-K100(0603) for +1_5VRUN_HMPLL noise issue
P.48 Add PJ8 for test request
(2006/06/01)
P.16 Add R519(0ohm 0402) for desinger set "LCDID3" to "0" by mistake.
P.49 PC102 change from mount to NC for application modification
P.46 PC52,PC53 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.47 PC66,PC73 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.49 PC99,PC113 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.36 Q25 pin2 netname change from +5VRUN to +5VAMP
P.36 R376 pin2 netname change from GND to A_GND
P.36 Add U38,R520(NC) for SPK_MUTE_EN for Vista requirement
P.36 Add NET "SPK_MUTE_EN" from U38 pin2 to U15 pin99 for Vista requirement
P.40 Change U36,U37 from RT9702 to RT9703, Add R521-R524.
P.27 Delete Q149.

(2006/06/02)

P.16 R515,R519 change from mount to NC
P.36 Add R525(NC) for Audio mute option
P.49 Add PC152 for application modification
P.26 R510 change from mount to NC for application modification
P.22 R188 change from mount to NC for application modification

(2006/06/05)

P.49 PC92,PC108 change from NC to mount for design rating
P.40 U36,U37 change from RT9703 to RT9702, Del R521-R524 for RT9703 phase out issue
P.49 Add PC153 for solving audible noise
P.19 Add R526 for LAN application modification

(2006/06/06)

P.13 Add C599,C600(1000P_50V_K) ; C155 change from 1000P_16V_K to 2.2U_10V_Y_Y ; C159 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.14 Add C601,C602(1000P_50V_K) ; C168 change from 1000P_16V_K to 2.2U_10V_Y_Y ; C172 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.15 Add C603,C604(1000P_50V_K) ; C177,C179,C181,C191,C192,C196 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.51 Add PD36,PD37 for application modification
P.19 C253 change form 0.1U_16V_M_B to 5P_50V_C ; C254 change from 5P_50V_C to 0.1U_16V_M_B ; Add L58 ; Del R526 for LAN application modification



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title History (1)		
Size	Document Number	Rev
C	H570-1-01	2.0
Date:	Tuesday, August 22, 2006	Sheet 52 of 55

HISTORY (2)

(2006/06/07)

P.26 R245 change from NC to mount for application modification

(2006/06/13)

P.33 R325 change from mount to NC for acoustic noise.

P.36 U38 change from 74AHCT1G08GW to 74AHCT1G08GW for Vih can't meet EC spec.

PVT

(2006/07/12)

P.47 Change PC68, PC70 from mount to NC for TPS51124 OVP issue.

P.27 Add R526 (1K ohm) series on ALW_ON net to prevent EC damage issue.

P.46 Delete PJ1, PJ2

P.47 Delete PJ3, PJ4, PJ6

P.48 Delete PJ7, PJ8, PJ9

P.32 F1,R320,R321,L32,C598,C389,C390,C391,CN21 change from mount to NC for cancel Oide function

P.37 U33 change from 15-TPS2231-0000(24pin) to 15-TPS2231-0002(20pin) for purchase convenient

P.40 U36,U37 change from 15-RT9702A-0000 to 15-TPS2055-0000 ;

Add R527,R528 for MS_PWR_CTRL and SD_PWR_CTRL are recognized to be high level by accident

(2006/07/20)

P.26 CN9 vendor part number change from QT8H0506-13T3R-7F to QT8H0506-13T3R-4F for packing type change.

P.49 PC153 change from 1C-10X0107-M403 to 1C-1XX0107-M400 for purchase convenient.

P.29 Delete CN31 for touch pad application modification.

P.22 R195 change from 47ohm to 0ohm ; C293 change from NC to mount for EMI solution.

P.29 LED6 change from 16-HT210DY-G000 to 16-HT210UD-UY00 for ME brightness issue.

LED5,LED7 change from 16-HT110Y0-0000 to 16-HT110UY-0000 for ME brightness issue.

(2006/07/21)

P.26 Add D22(NC) for ESD solution

P.30 R301 change from 120ohm to 47ohm for ME brightness issue

(2006/07/25)

P.30 C365 change from NC to mount for WLAN power ripple noise issue

P.26 Add VR1 for ESD solution

P.29 Add VR2,VR3(NC) for ESD solution

P.41 Add VR4,VR5(NC) for ESD solution

(2006/07/28)

P.29 Q155 change from 17-CHDTC14-4E01 to 17-2N70020-0000 for ME brightness issue.

(2006/07/31)

P.30 R301 change from 47ohm to 120ohm (LED1 is 10mA) for ME brightness issue

P.29 R418 change from 47ohm to 62ohm (LED5 is 18.75mA) for ME brightness issue

P.29 R424 change from 47ohm to 62ohm (LED6 is 19.5mA)

R425 change from 47ohm to 120ohm (LED6 is 10mA)for ME brightness issue

P.29 R426 change from 47ohm to 62ohm (LED7 is 18.9mA)

(2006/08/01)

P.31 Q17 change from 17-ME2301T-1000 to 17-S12301B-DS00 for Fan rotational speed issue

-----PVT schematic released

(2006/08/07)

P.45 PC42 change from 1C-2B30104-K000(0.1u) to 1C-2B30224-K000(0.22u) and mount PC42 for solving AC_OFF_3# abnormal issue

P.34 R350 change from 6.2kohm to 6.98kohm for adjust the gain of speaker amp

P.26 VR1 change from mount to NC ; D22 change from NC to mount for purchase convenient.

P.29 R418,R426 change from 62ohm to 120ohm for LED brightness issue

(2006/08/13)

P.45 PR3 change from 1kohm to 20kohm for power circuit design improvement plan which is DC_IN OVP circuit.

-----PVT SMT

MP

(2006/08/16)

P.23 Add D23 from IMVP_PWRGD to ALW_PWRGD for RTC stop issue backup (D23 is NC)

Add D24 from PM_RSMRST#(A3602) to ALW_PWRGD for RTC stop issue backup (D24 is NC)

(2006/08/17)

P.40 Add Q163,Q164,R529,F2(MS_PWR) for purchase convenient

Add Q165,Q166,R530,F3(SD_PWR) for purchase convenient

(2006/08/18)

P.40 R392,R395 change from 1Mohm to 100Kohm
F2,F3 move to pin3 side of Q163,Q165

P.40 Q163,Q165 change from PMBT2907A(PNP) to SI2301BDS-T1-E3(P-MOS)
R529,R530 change from 1.5kohm to 1kohm
Add R531,R532 4.7kohm

P.23 R221 change from 100ohm to 1kohm

D23,D24 change from BAS316PT to SCS500V-40-LF

D23,D24 change from NC to mount for RTC stop issue

(2006/08/23)

P.40 Q163,Q165 change from VISHAY_SI2301BDS-T1-E3 to Philips_PMV65XP for purchase convenient.

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