





## 8. Block Diagram and Schematic

**BOARD INFORMATION**

### SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

#### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
<b>ICH9M</b>	<b>Master</b>		<b>SMBUS Master</b>
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	
SODIMM1	1010 001X	A4h	
<b>MICOM</b>	<b>Master</b>		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

#### USB PORT Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	1 USB PORT (RIGHT, SUB)	UHCL_3	7 USB PORT (RIGHT, SUB)
UHCL_1	2 USB PORT (LEFT)	UHCL_4	8 CAMERA(17*)
UHCL_2	3, 4 CARD READER(AU8336)	UHCL_9	9 CAMERA(15*)
	5 BLUETOOTH(TBD)	UHCL_5	11

#### SATA Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

#### PCI EXPRESS Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCle1	WLAN	PCle2	Wired LAN
PCle3	-	PCle4	-

#### Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	

#### Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
<b>VDC_ADPT</b>	Primary DC system power supply (9 to 19V)	<b>P1.05V_PEG</b>	P1.05V (Direct Media Interface Compensation)
<b>VDC</b>	Charger Reference Voltage Source	<b>P5.0V</b>	5.0V Power Rail (off in S3-S5)
<b>VDC_CHG</b>	Charger Reference Voltage Source	<b>P3.3V</b>	3.3V Power Rail (off in S3-S5)
<b>PRTC_BAT</b>	3.3V supply for the RTC well.	<b>P1.05</b>	1.05V Power Rail (off in S3-S5)
<b>P5.0V_ALW</b>	5.0V always power well	<b>P0.9V</b>	DDR2 Termination
<b>P12.0V_ALW</b>	12.0V always power well	<b>P5.0V_AUX</b>	5.0V Power Rail (off in S4-S5)
<b>P1.7V_VREF</b>	Power Chip Reference	<b>P3.3V_AUX</b>	3.3V Power Rail (off in S4-S5)
<b>P2.0V_VREF</b>	Power Chip Reference	<b>P1.8V_AUX</b>	1.8V Power Rail (off in S4-S5)
<b>P5.0V_VREF_FLT</b>	Power Chip Reference	<b>GPU_CORE</b>	Core Voltage for GPU
<b>P3.3V_MICOM</b>	Output voltage of RT8205AGQW (if VDC is removed, it will be off)	<b>AUD_P5V</b>	5.0V supply for Audio
<b>LCD_VDD3V</b>	3.3V (LED LCD)	<b>P4.75V_AUD</b>	Audio Analog Voltage
<b>KBC3_CHG4.2V</b>	To charge battery	<b>P5.0V_STB</b>	To charge USB device at sleep status
<b>P1.2V_LAN</b>	Internal Regulator's Power of LAN Controller	<b>P5.0V_ODD</b>	5.0V supply at SUB_ODD Board
<b>P2.5V_LAN</b>	Internal Regulator's Power of LAN Controller	<b>EGFX_CORE</b>	nVidia Graphic Chip power
<b>P3.3V_MCD</b>	3.3V (3-in-1 Socket)	<b>P1.5V</b>	1.5V Power Rail (off in S3-S5)
		<b>P1.5V_AUX</b>	1.5V Power Rail (off in S4-S5)
		<b>P1.8V</b>	1.8V Power Rail (off in S3-S5)

} Power source of External

### REVISION HISTORY

See rev notes for more information.

DRAW	Jun PARK	DATE	9/23/2008	TITLE	<b>Bremen-L3</b>		<b>SAMSUNG</b> ELECTRONICS
CHECK	YMAHN	DEV. STEP	PV	MAIN		PART NO.	
APPROVAL	HJKIM	REV	1.0	BOARD INFO		BA41-xxxxxA	
MODULE CODE	undefined	LAST EDIT	October 27, 2009 14:27:43 PM	PAGE	3	OF	59

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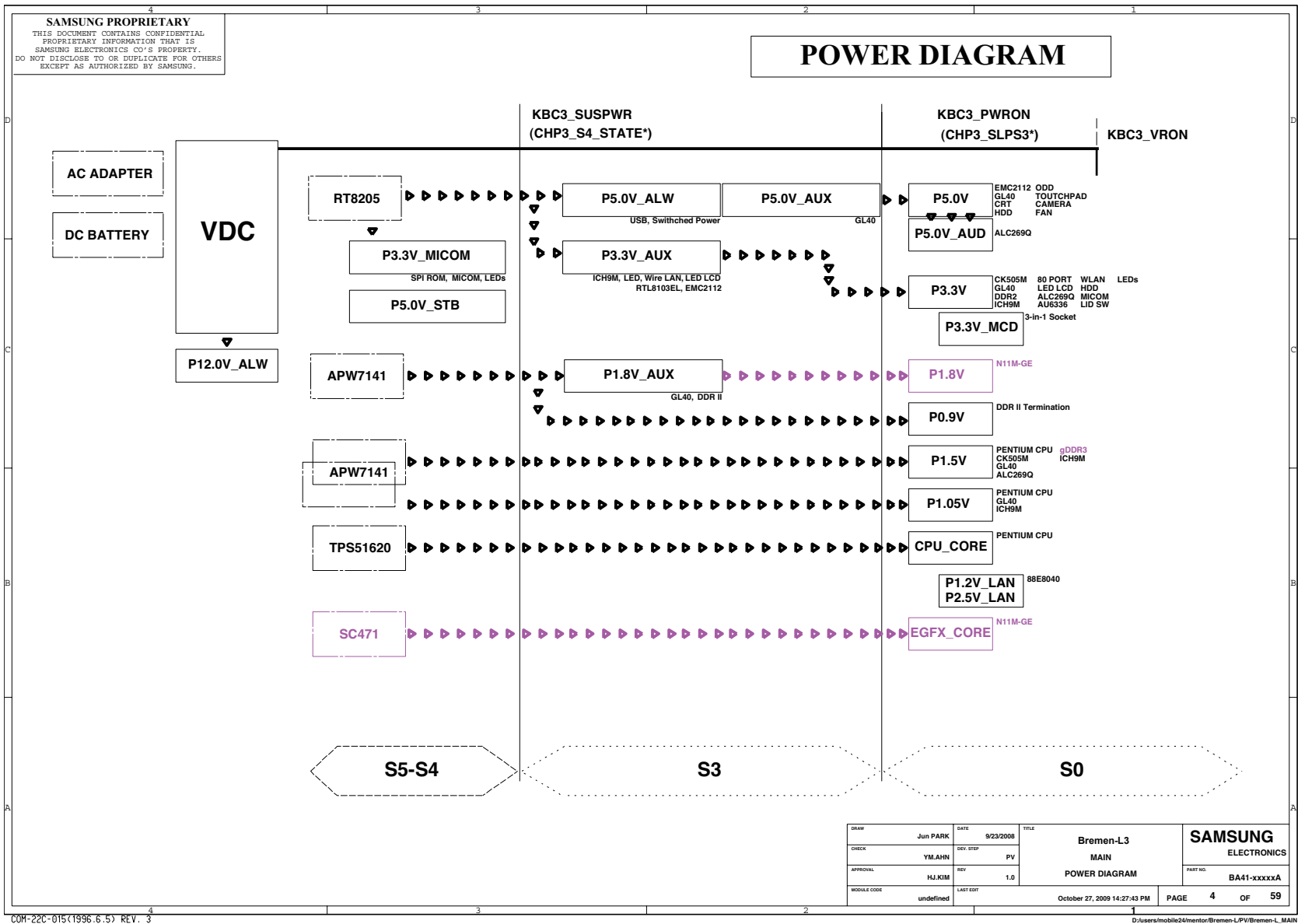
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R530/R730

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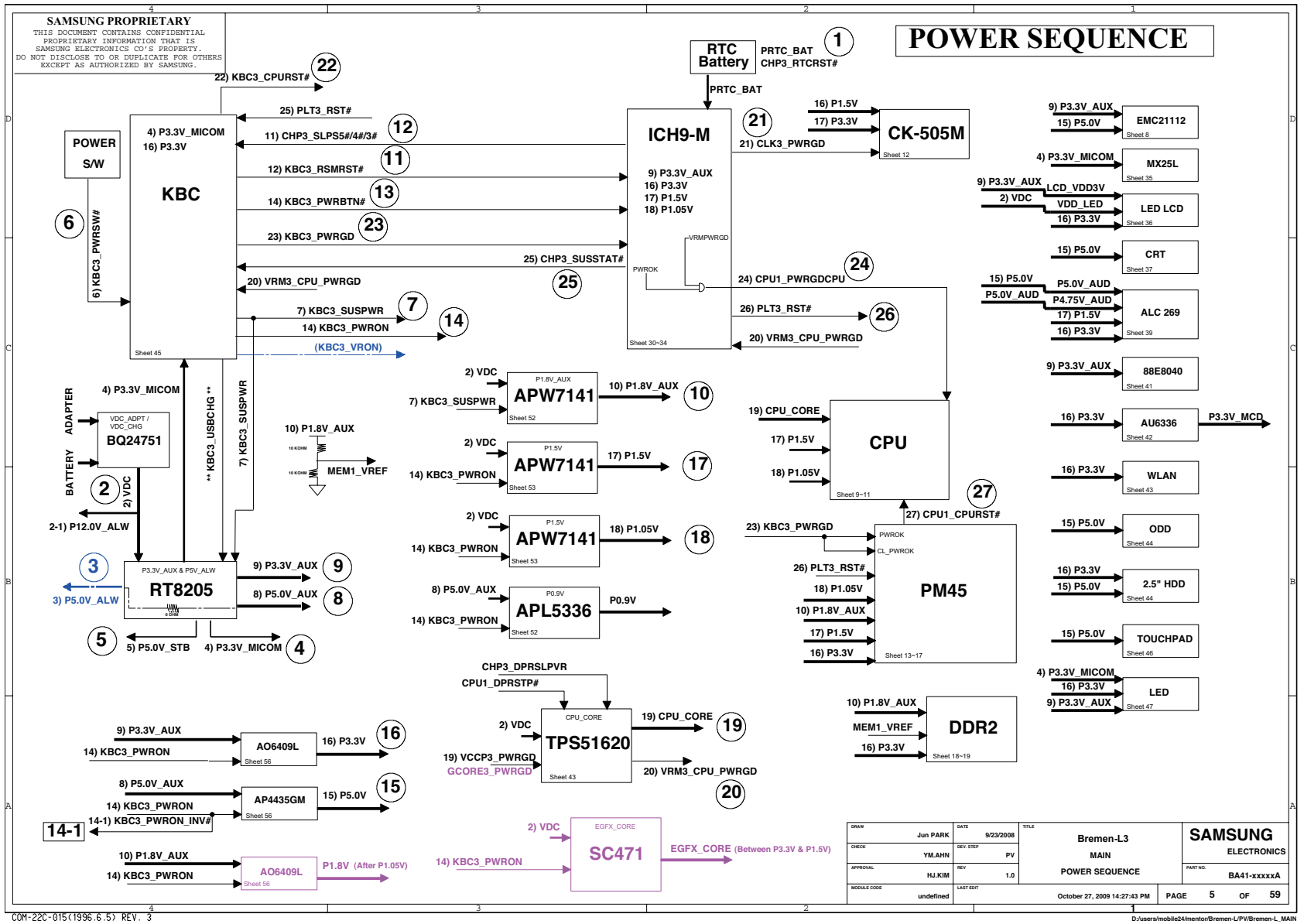
## 8. Block Diagram and Schematic



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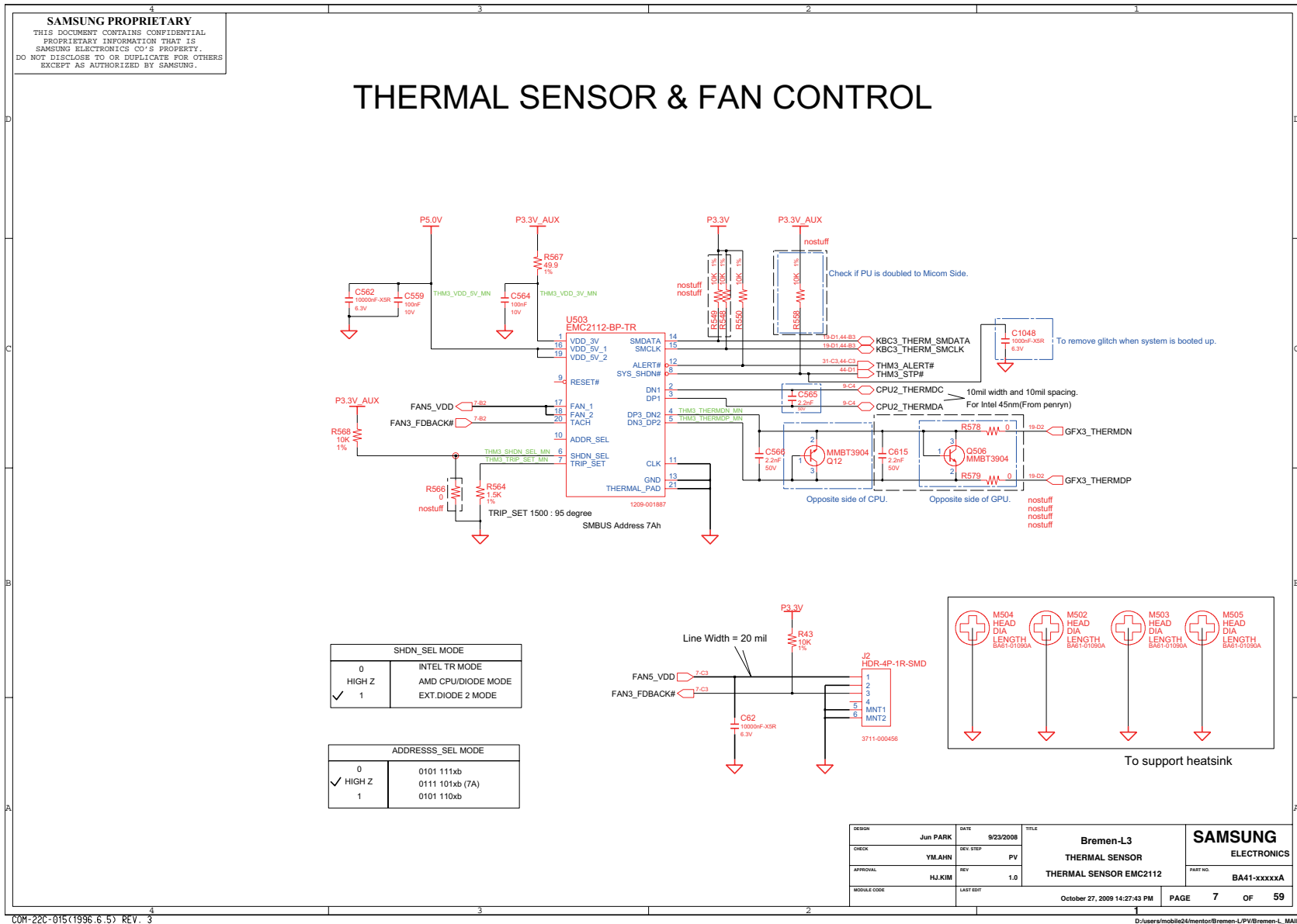
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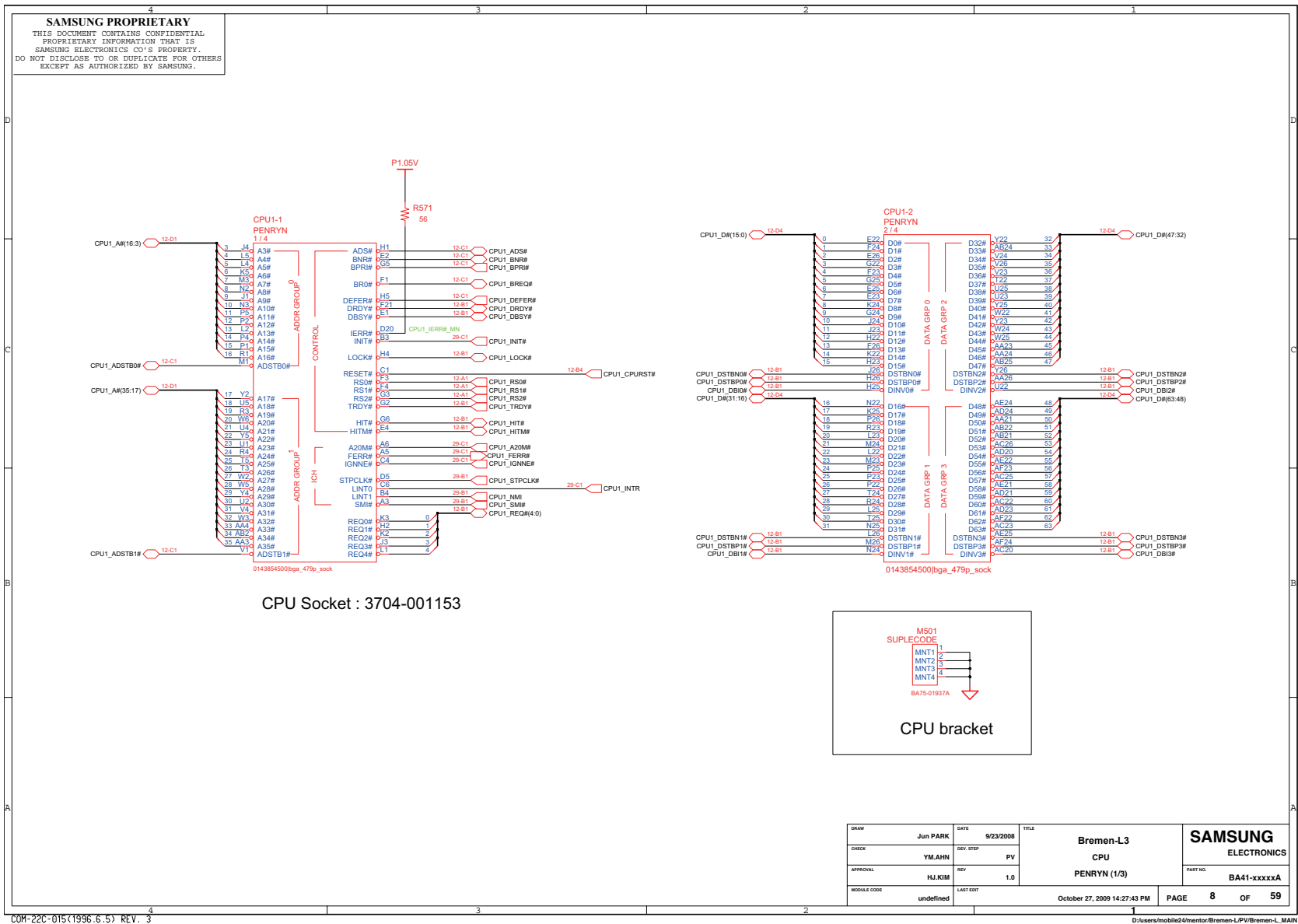


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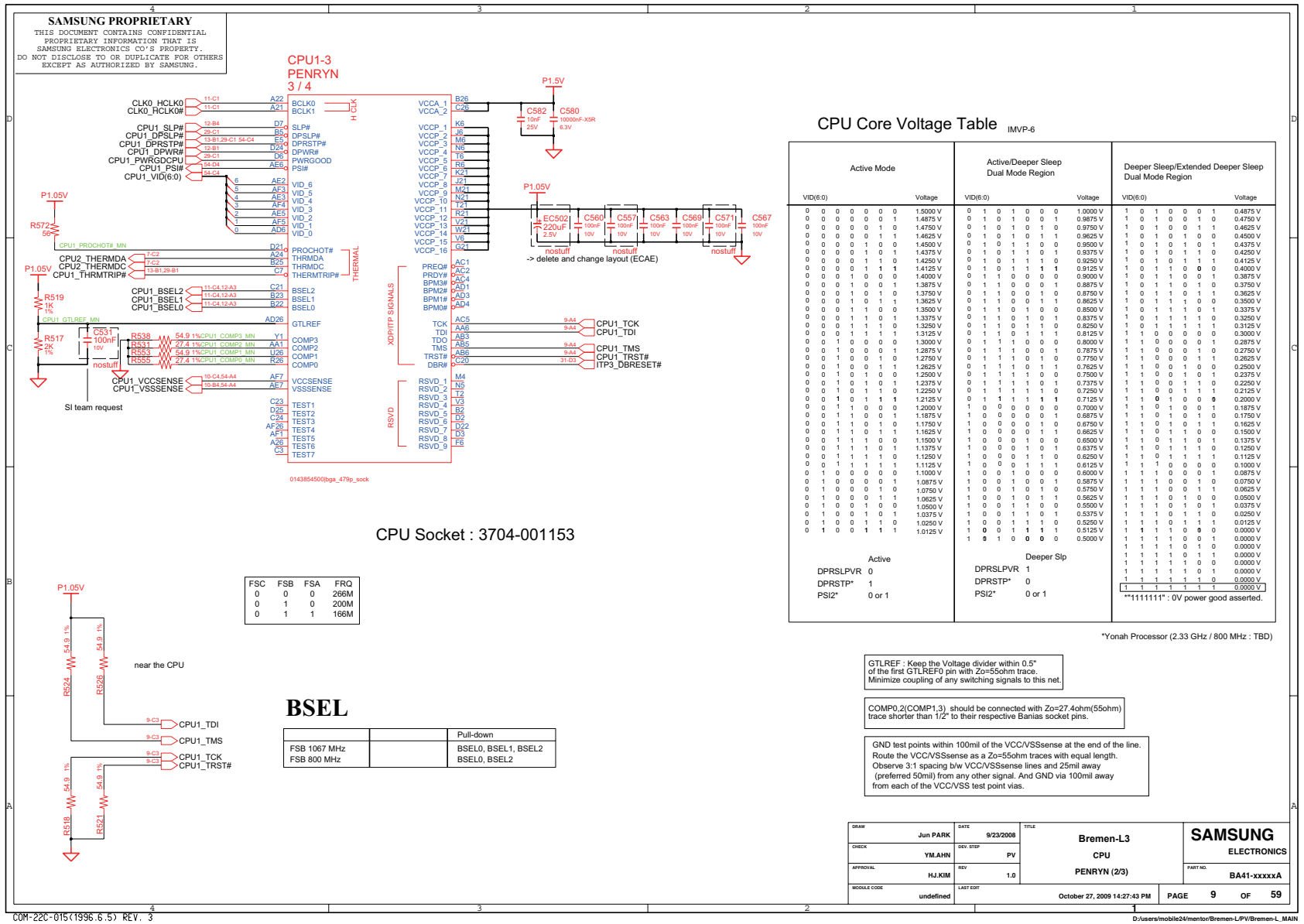
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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 0	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 0 1 1 1 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 0	0.8875 V	1 0 1 1 0 0 1	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 0 1	0.8750 V	1 0 1 1 0 1 0	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 0	0.8625 V	1 0 1 1 0 1 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 0 1 1	0.8500 V	1 0 1 1 1 0 0	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 0	0.8375 V	1 0 1 1 1 0 1	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 0 1	0.8250 V	1 0 1 1 1 1 0	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 0 1 1 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 0 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 0 1 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 0	0.7375 V	1 1 0 0 1 0 1	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 0 1	0.7250 V	1 1 0 0 1 1 0	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 0	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	0 1 1 1 1 1 1	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 0	0.6875 V	1 1 0 1 0 0 1	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 0 1	0.6750 V	1 1 0 1 0 1 0	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 0	0.6625 V	1 1 0 1 0 1 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 1 1	0.6500 V	1 1 0 1 1 0 0	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 0	0.6375 V	1 1 0 1 1 0 1	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 0 1	0.6250 V	1 1 0 1 1 1 0	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 0	0.6125 V	1 1 0 1 1 1 1	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 0	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 0 1	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 0	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 0 1 0	0.0500 V
0 1 0 1 0 0 0	1.0500 V	1 0 0 1 1 0 1	0.5500 V	1 1 1 0 0 1 1	0.0375 V
0 1 0 1 0 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 0 0	0.0250 V
0 1 0 1 0 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 0 1	0.0125 V
0 1 0 1 0 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 1 0 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
0 1 1 1 0 0 0	1.0000 V	1 0 1 1 0 0 0	0.5000 V	1 1 1 1 0 1 0	0.0000 V
0 1 1 1 0 0 1	1.0000 V	1 0 1 1 0 0 1	0.5000 V	1 1 1 1 1 0 0	0.0000 V
0 1 1 1 0 0 1	1.0000 V	1 0 1 1 0 0 1	0.5000 V	1 1 1 1 1 0 1	0.0000 V
0 1 1 1 0 0 1	1.0000 V	1 0 1 1 0 0 1	0.5000 V	1 1 1 1 1 1 0	0.0000 V
0 1 1 1 0 0 1	1.0000 V	1 0 1 1 0 0 1	0.5000 V	1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP\* 1, PSi2\* 0 or 1  
 Deeper Slp: DPRSLPVR 1, DPRSTP\* 0, PSi2\* 0 or 1

\*\*11111111\*: 0V power good asserted.

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

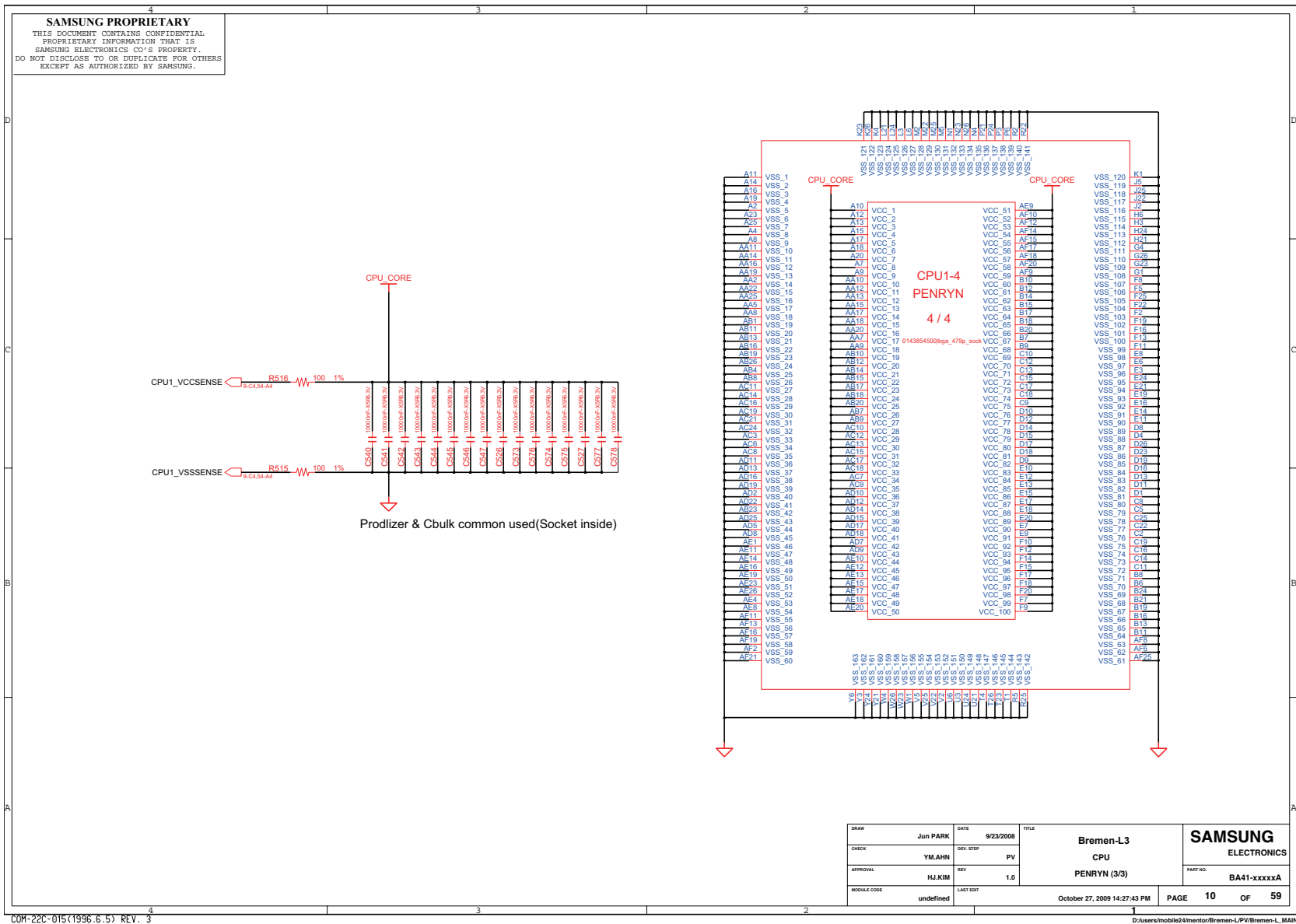
COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm trace with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

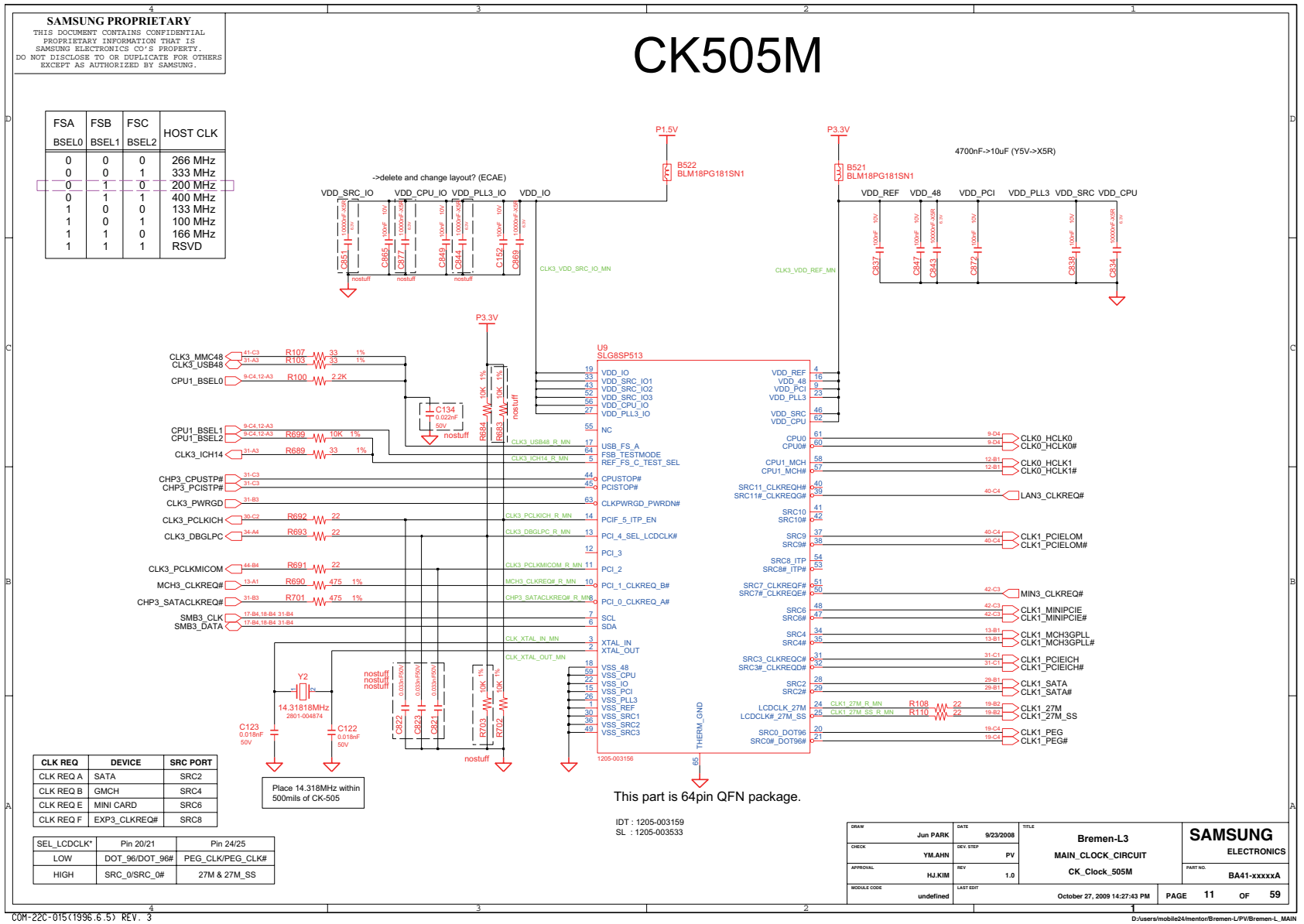
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	Bremen-L3	SAMSUNG ELECTRONICS
CHECK	YM.AHN	DEV. STEP	PV		CPU	
APPROVAL	HJ.KIM	REV	1.0		PENRYN (2/3)	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 27, 2009 14:27:43 PM	PAGE	9	OF 59

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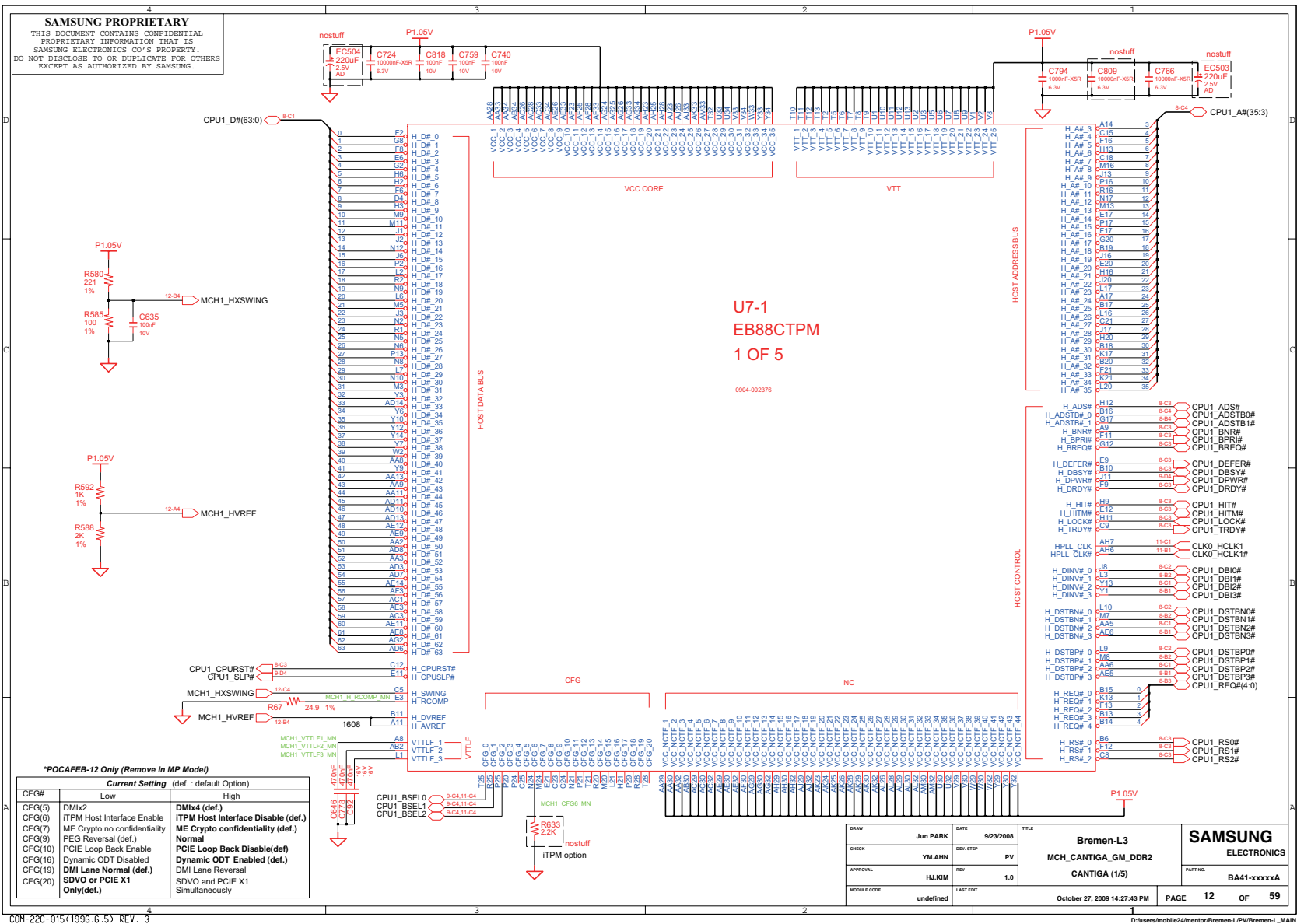
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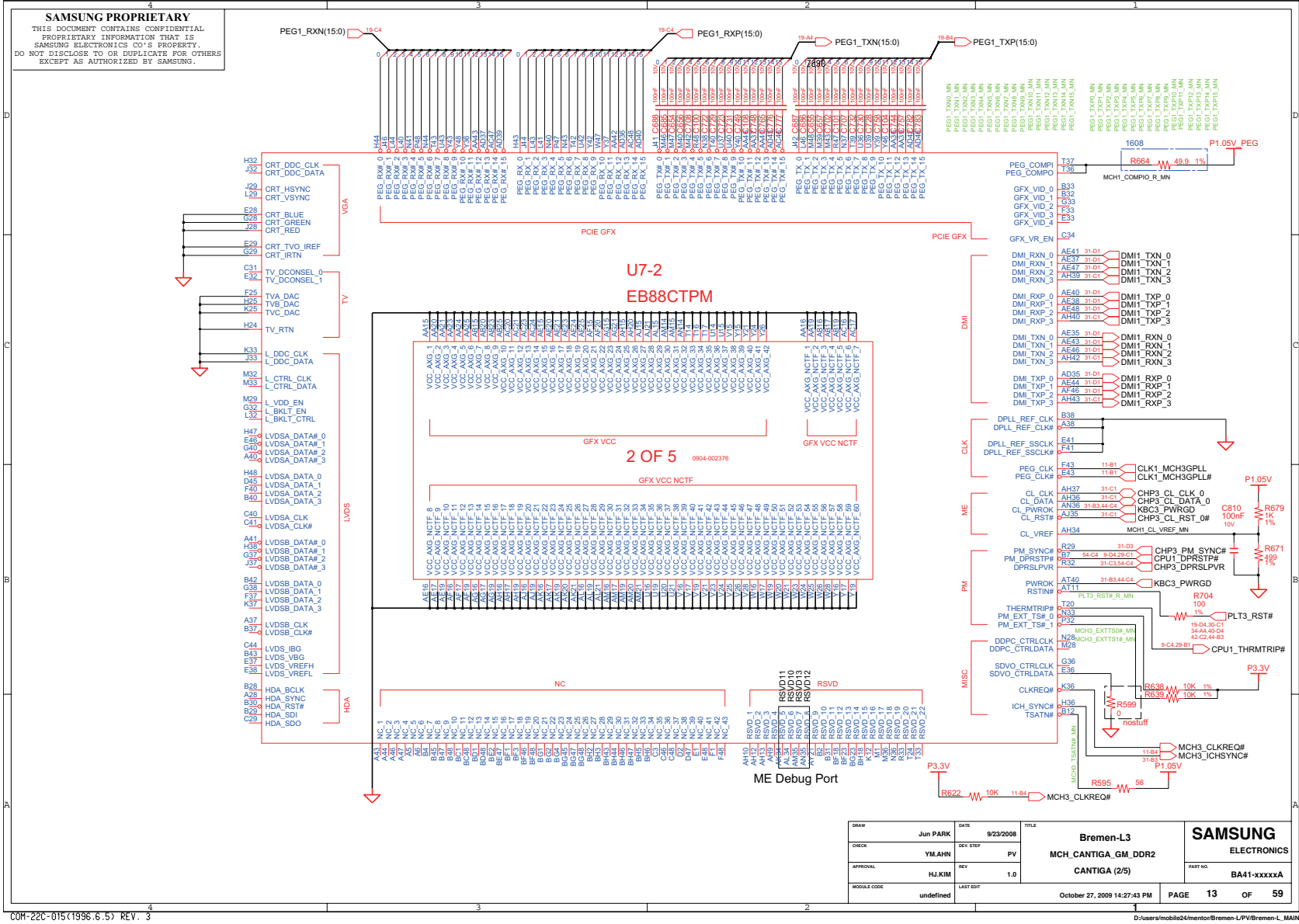
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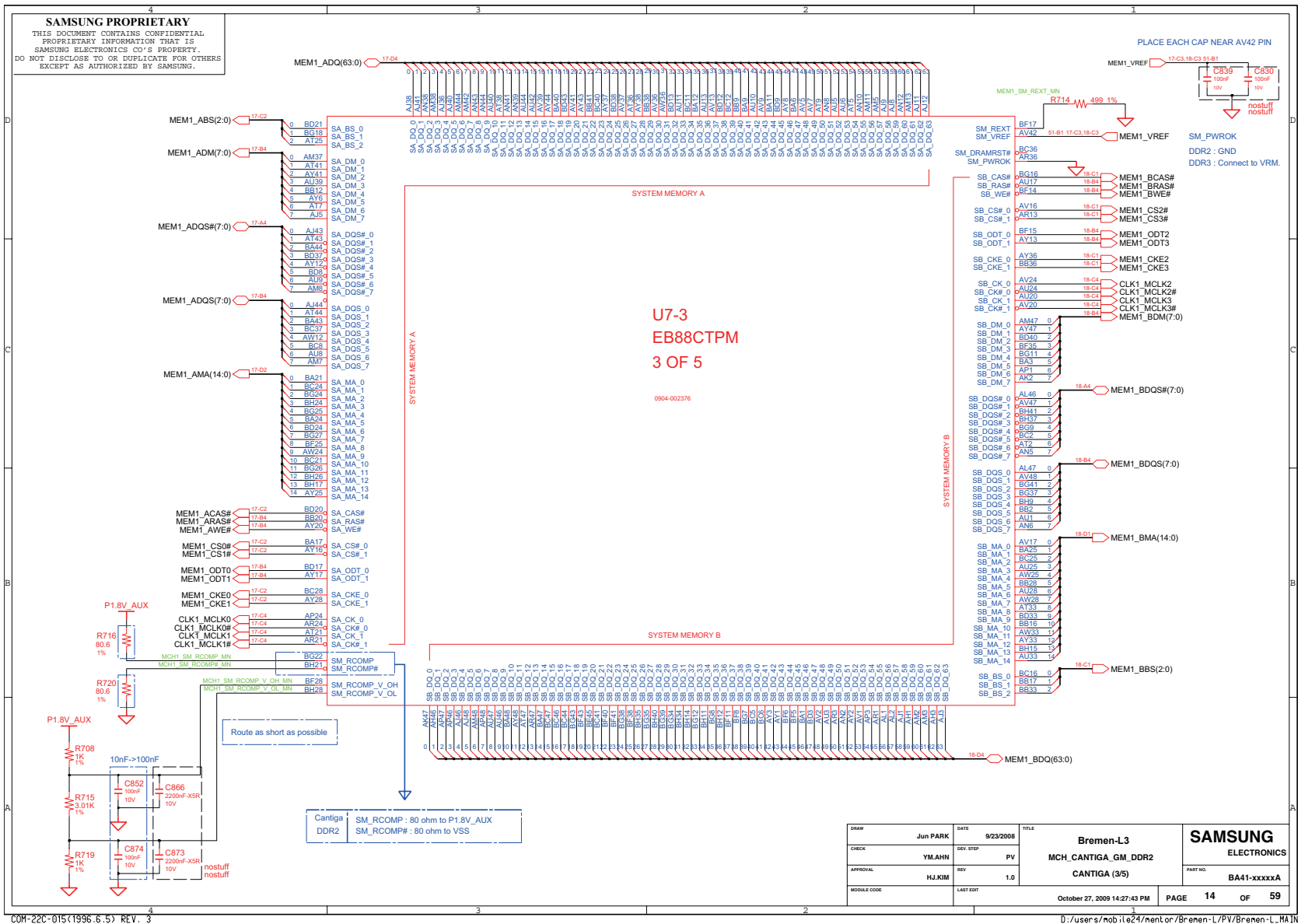
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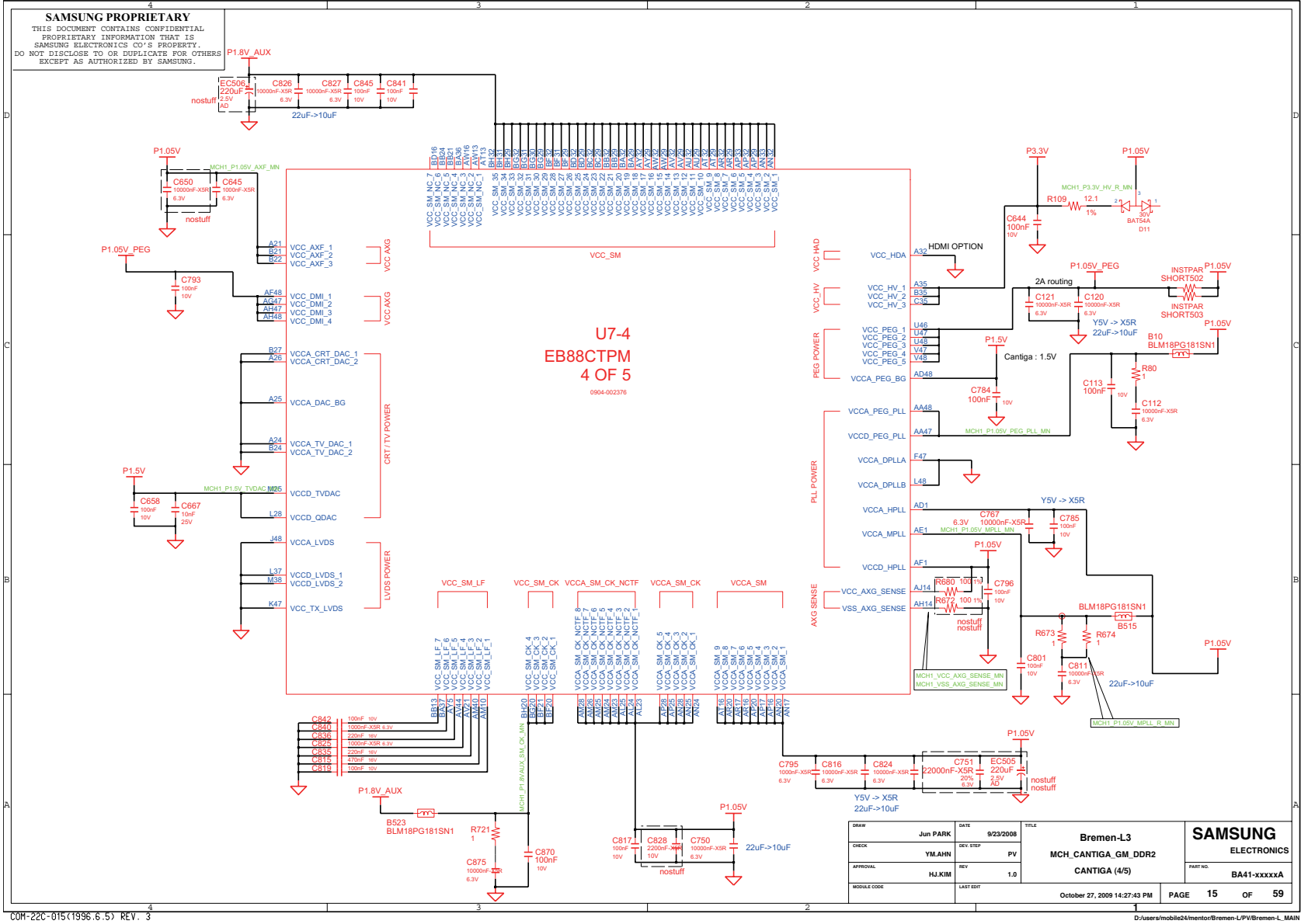
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CHECK	YMAHN	DEV STEP	PV		MCH_CANTIGA_GM_DDR2	
APPROVAL	HJKIM	REV	1.0		CANTIGA (2/5)	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 27, 2009 14:27:43 PM	PAGE	13	OF 59

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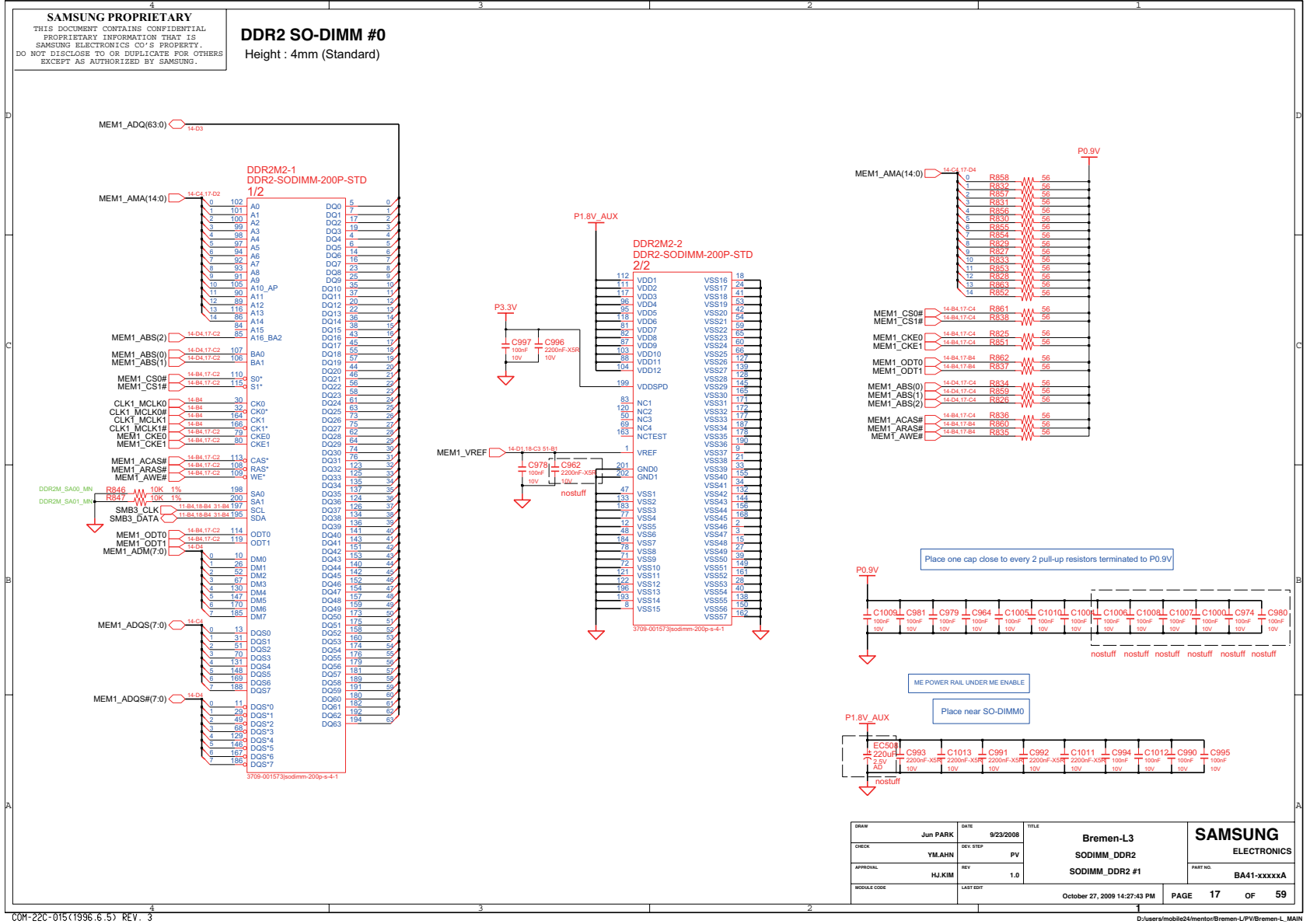
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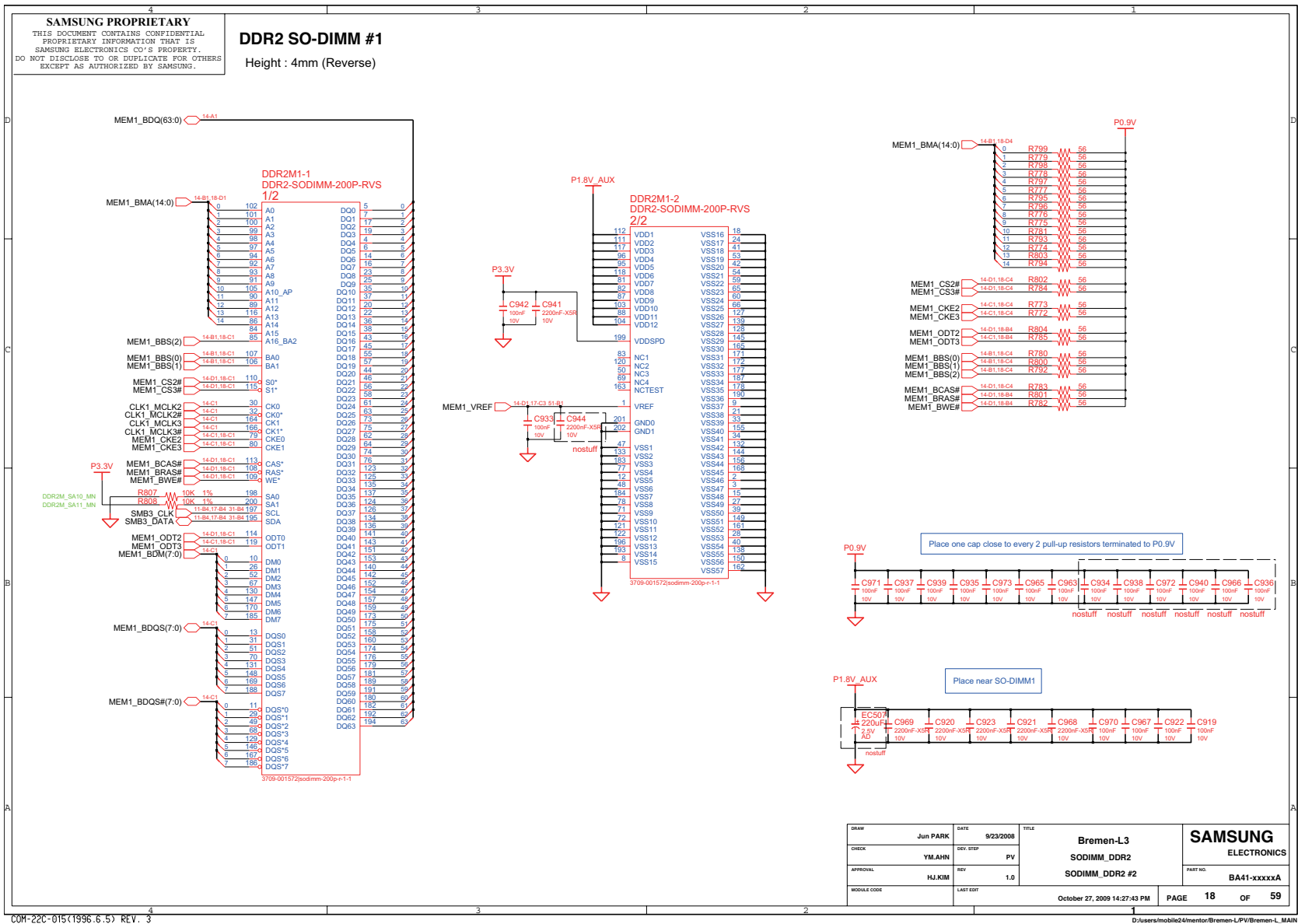


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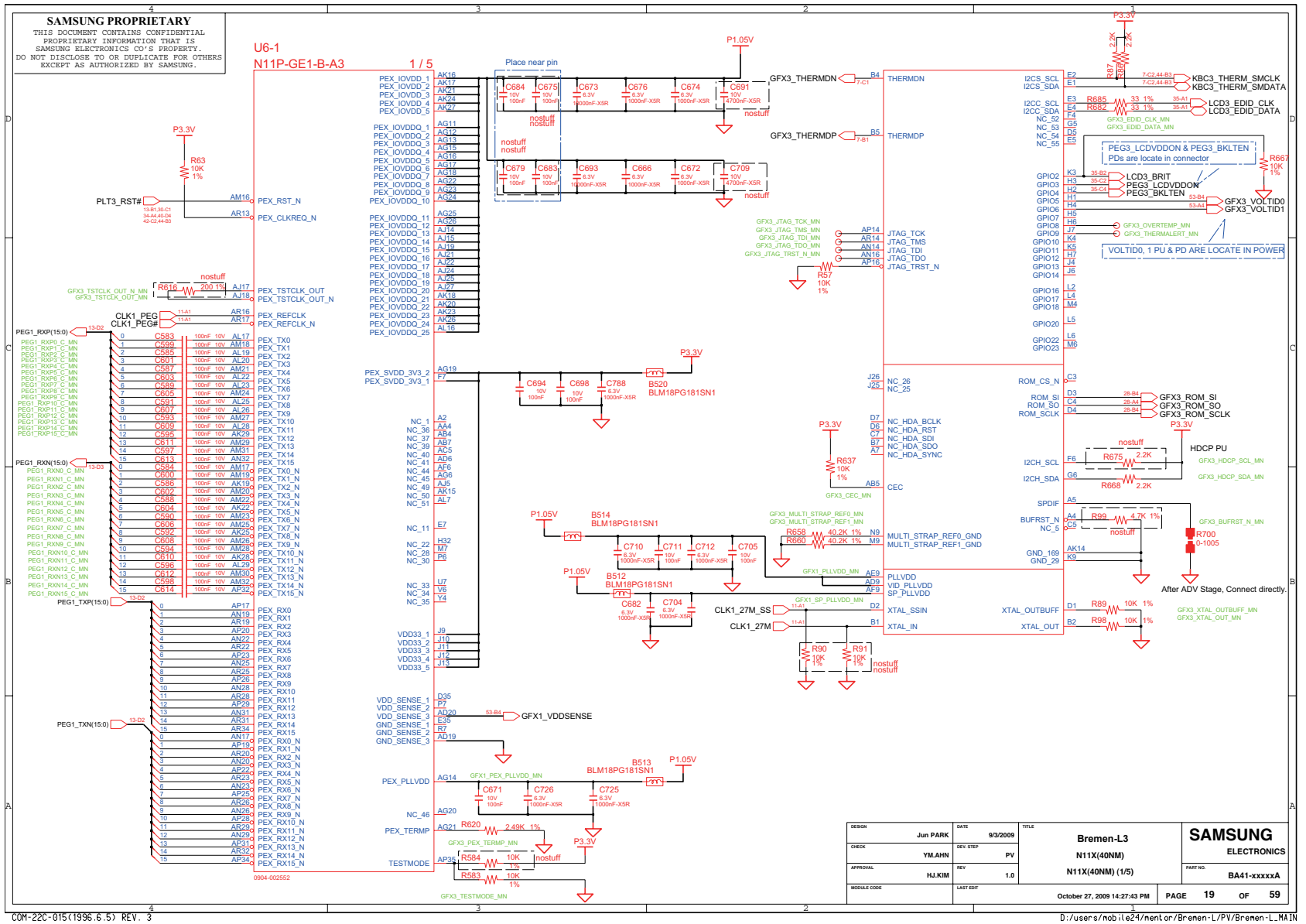
COM-22C-015(1996.6.5) REV. 3

DRAW	Jun PARK	DATE	9/23/2008	TITLE	Bremen-L3	<b>SAMSUNG</b> ELECTRONICS
CHECK	YJ.AHN	DEV. STEP	PV	SODIMM_DDR2		
APPROVAL	HJ.KIM	REV	1.0	SODIMM_DDR2 #2	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		October 27, 2009 14:27:43 PM	PAGE	18 OF 59

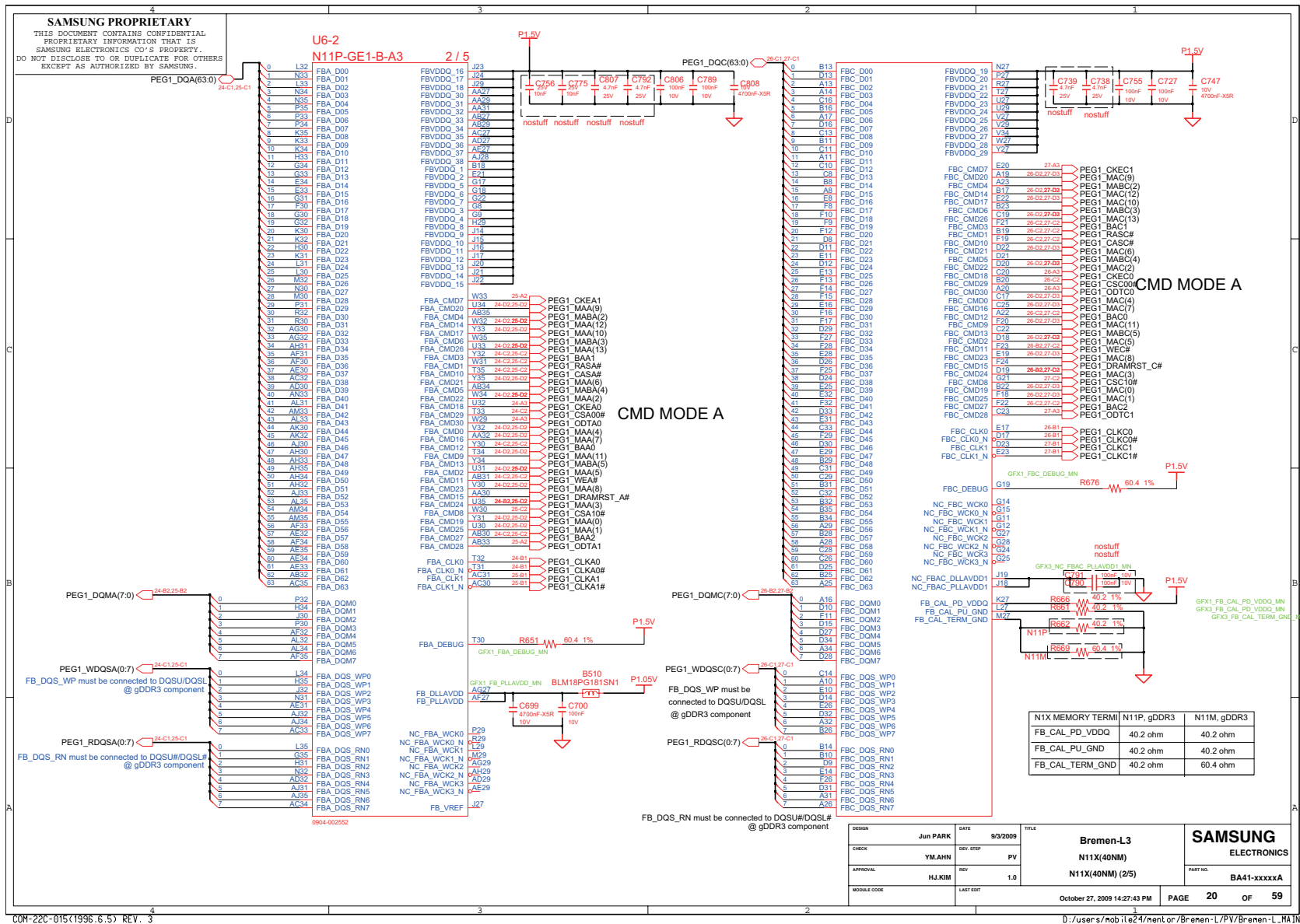
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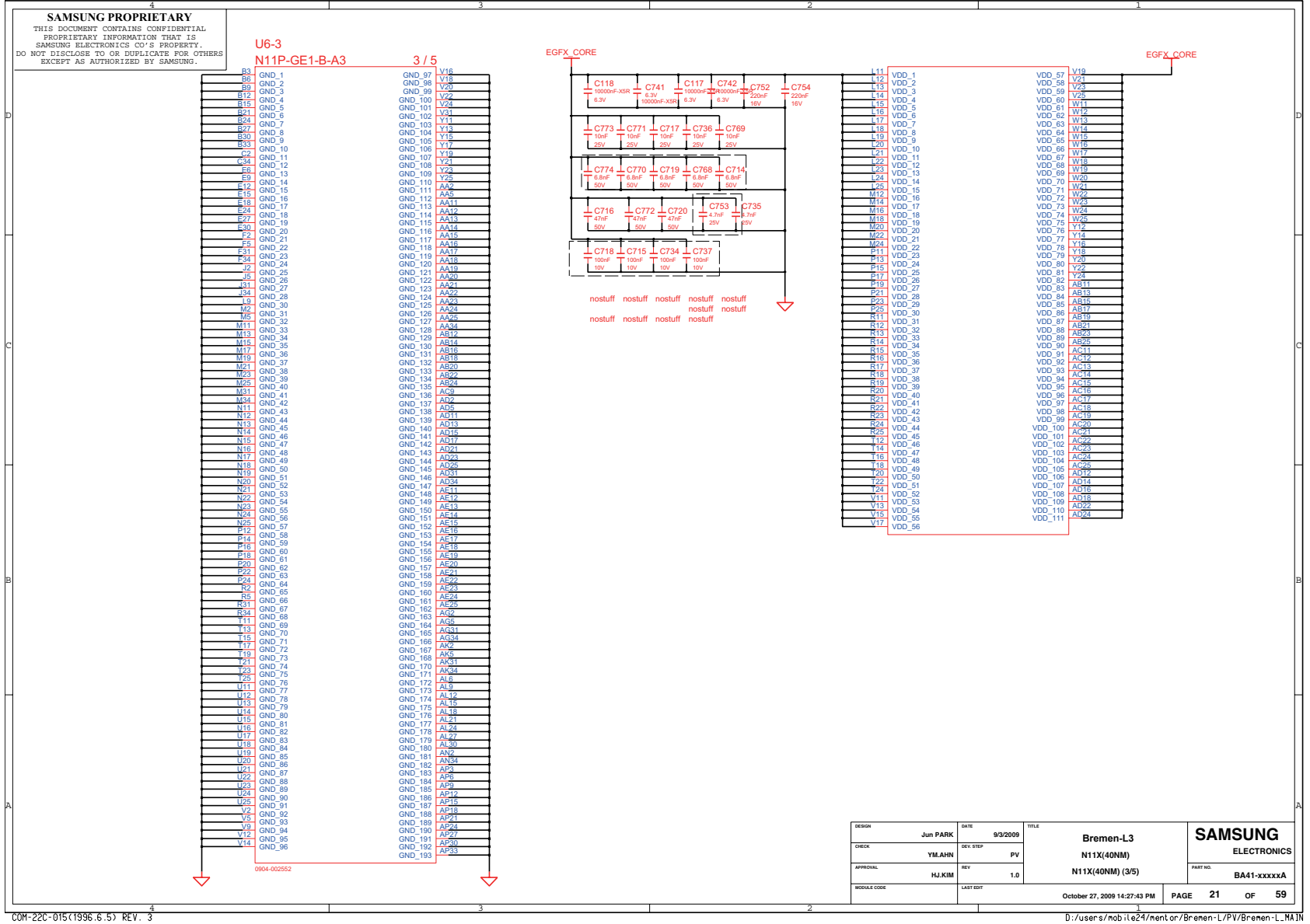
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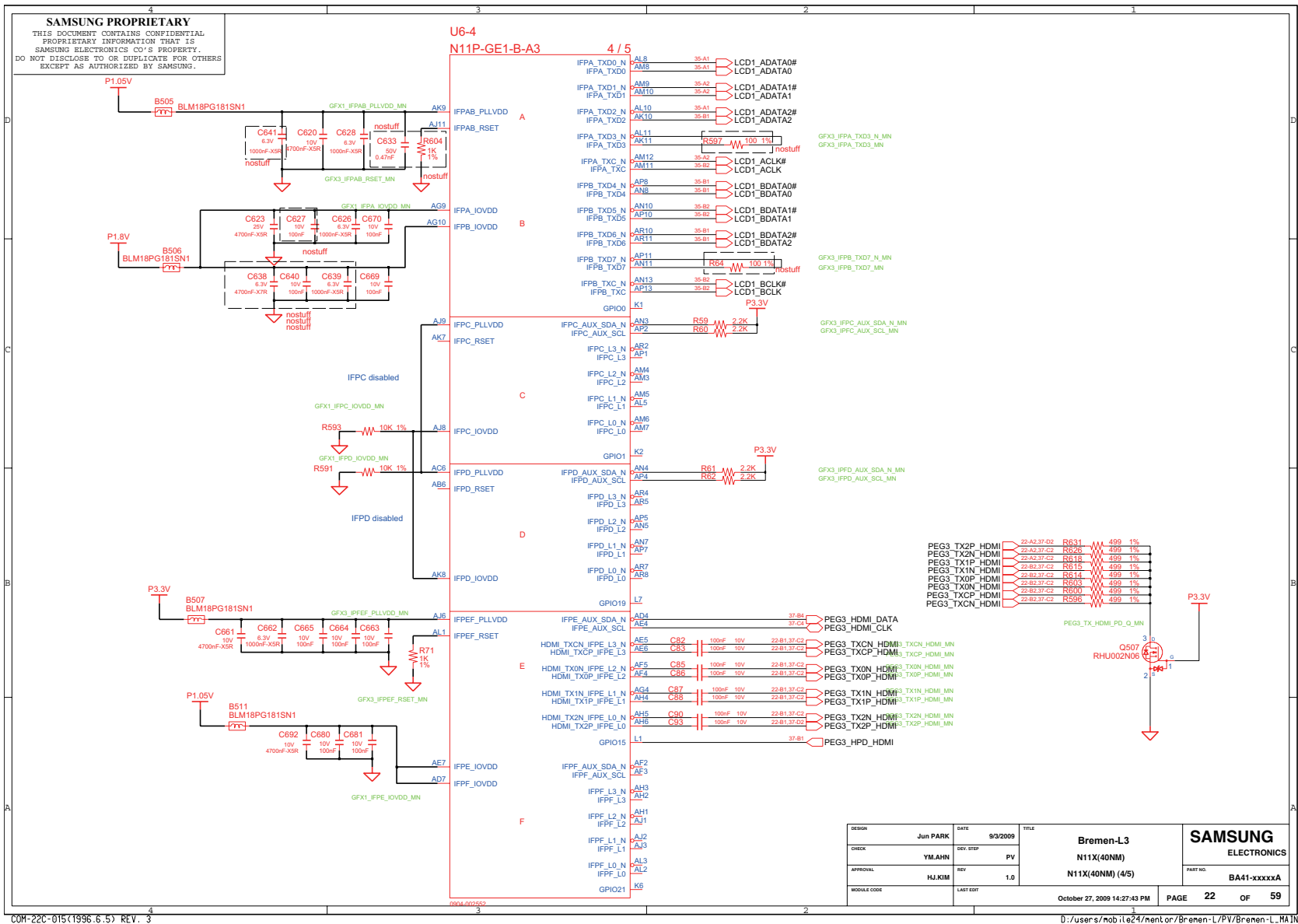
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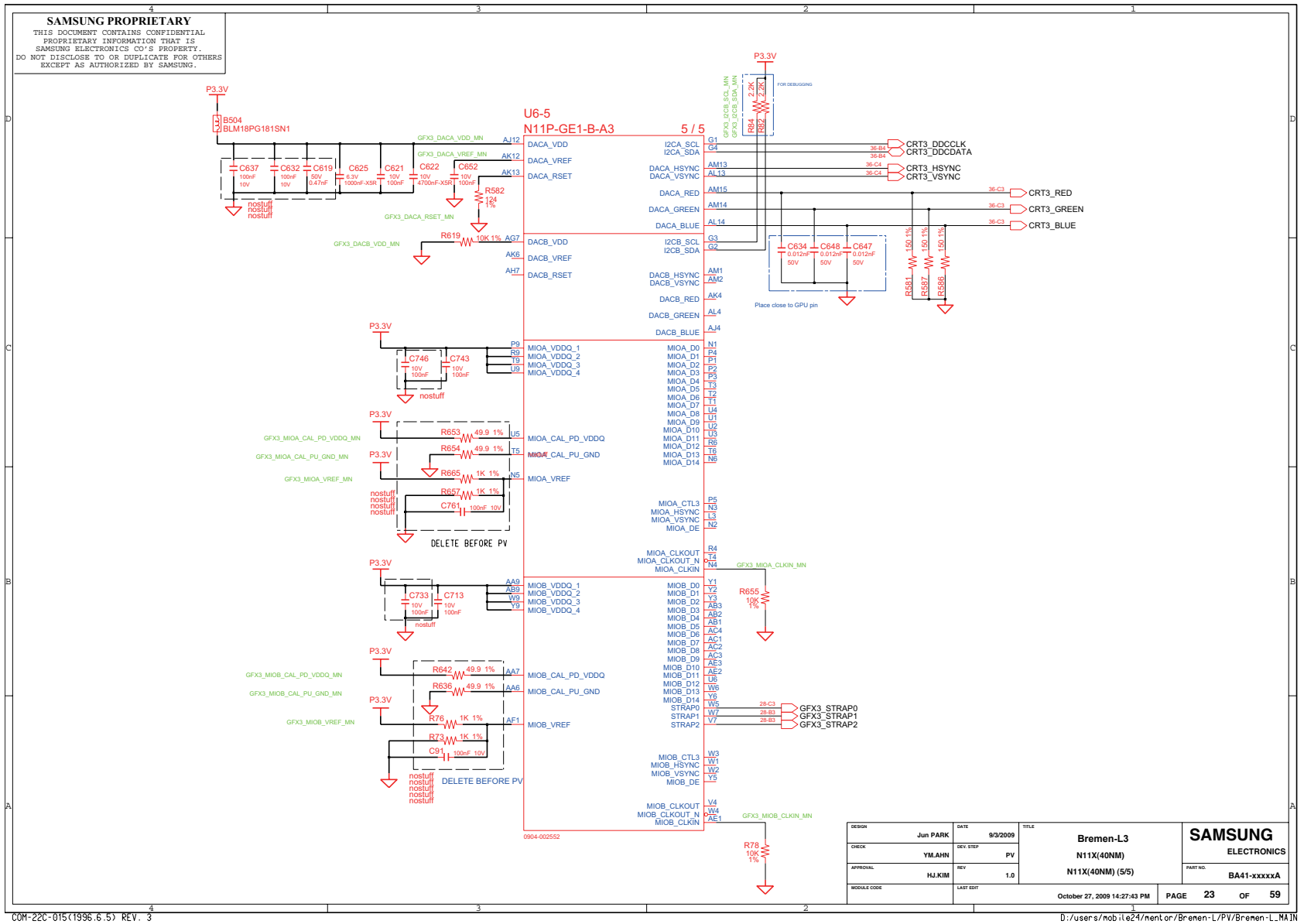
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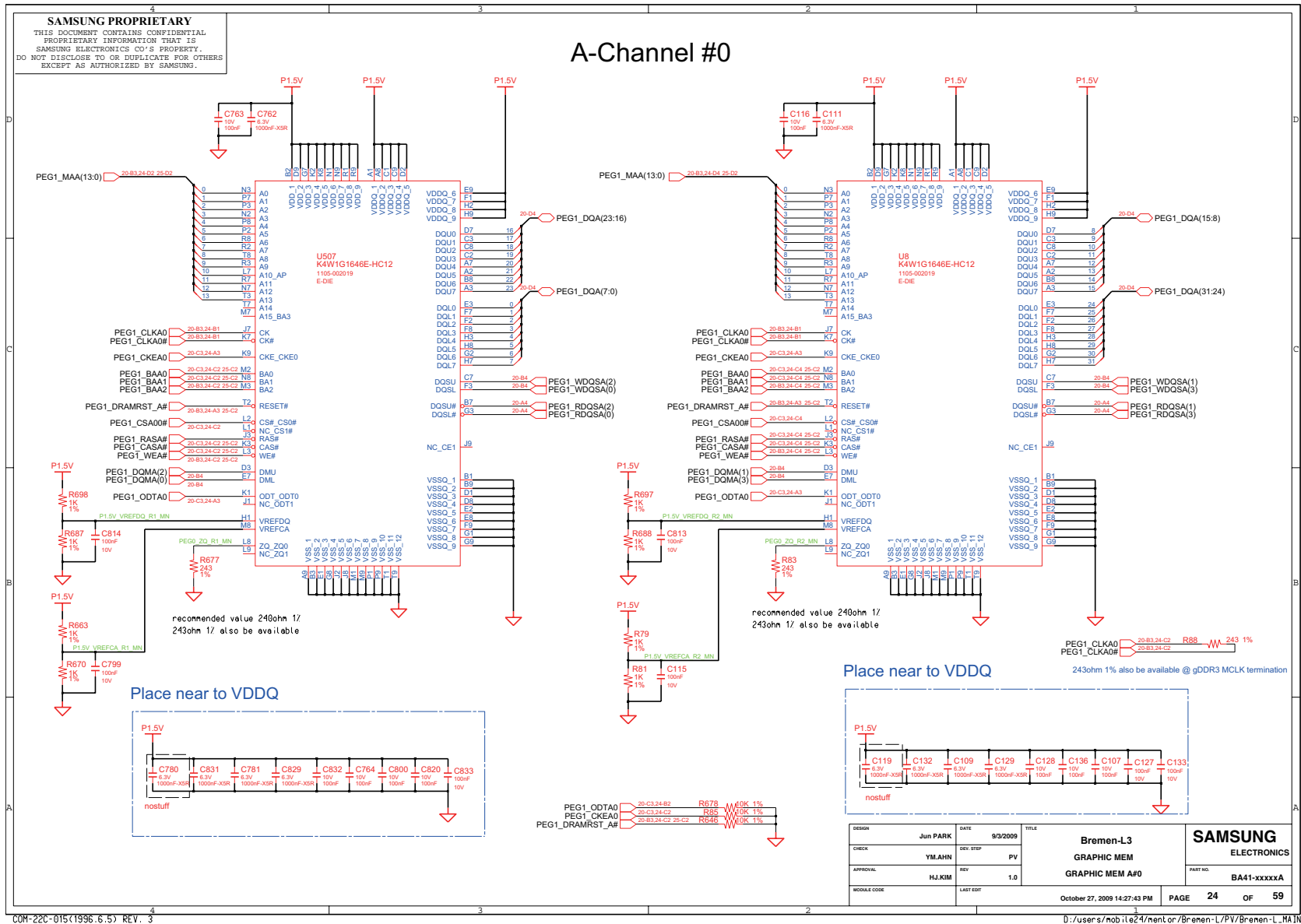
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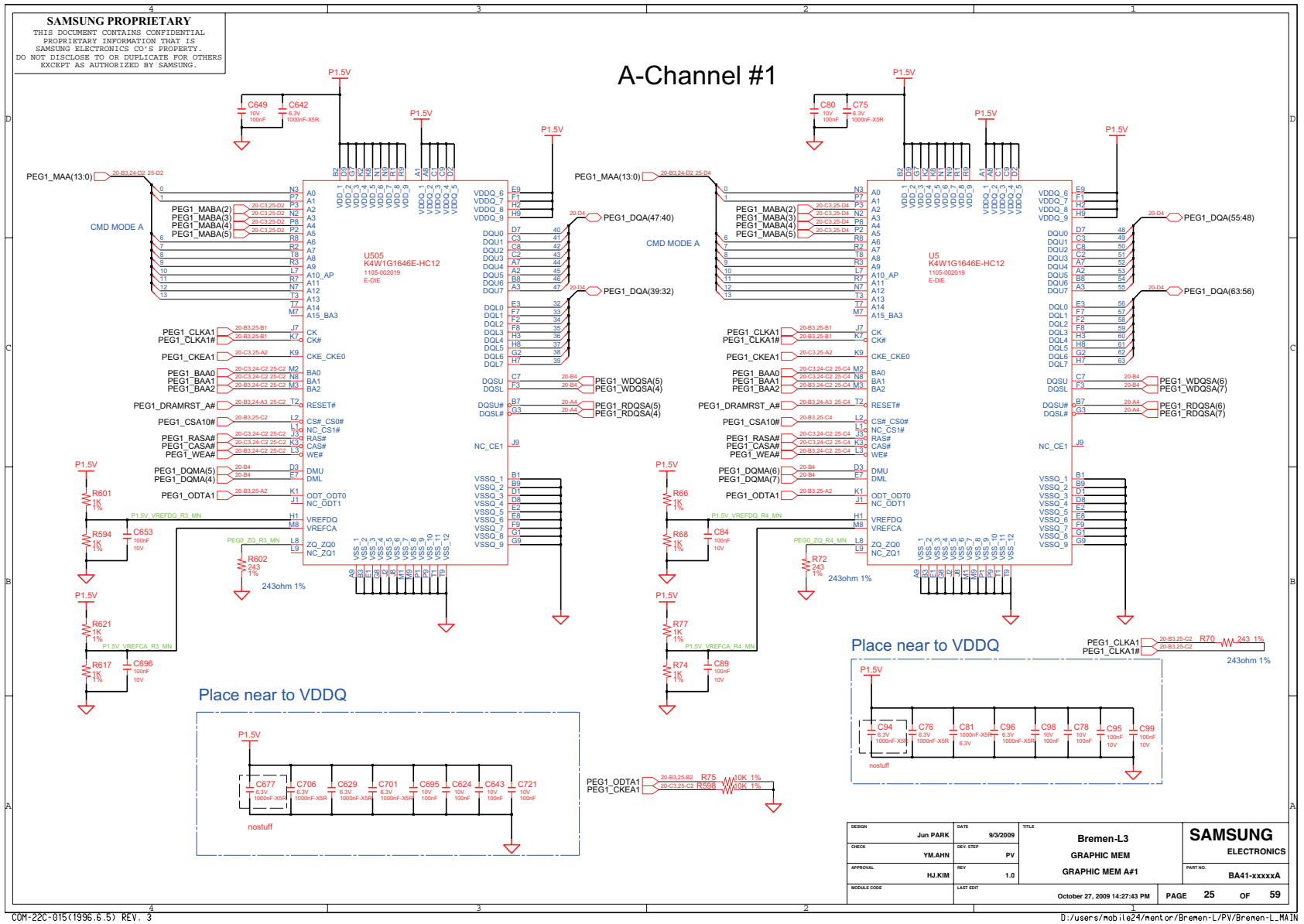
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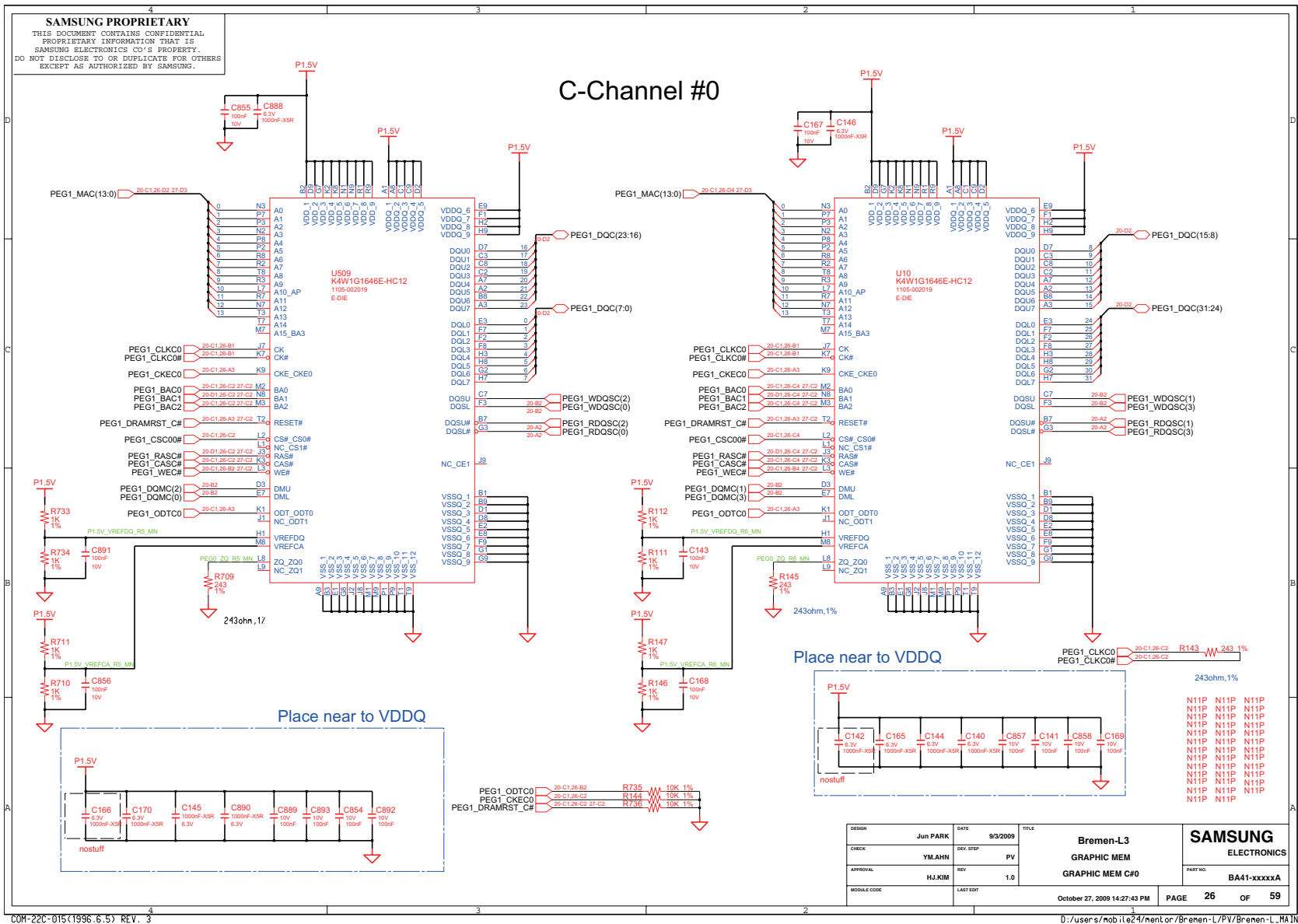


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# 8. Block Diagram and Schematic

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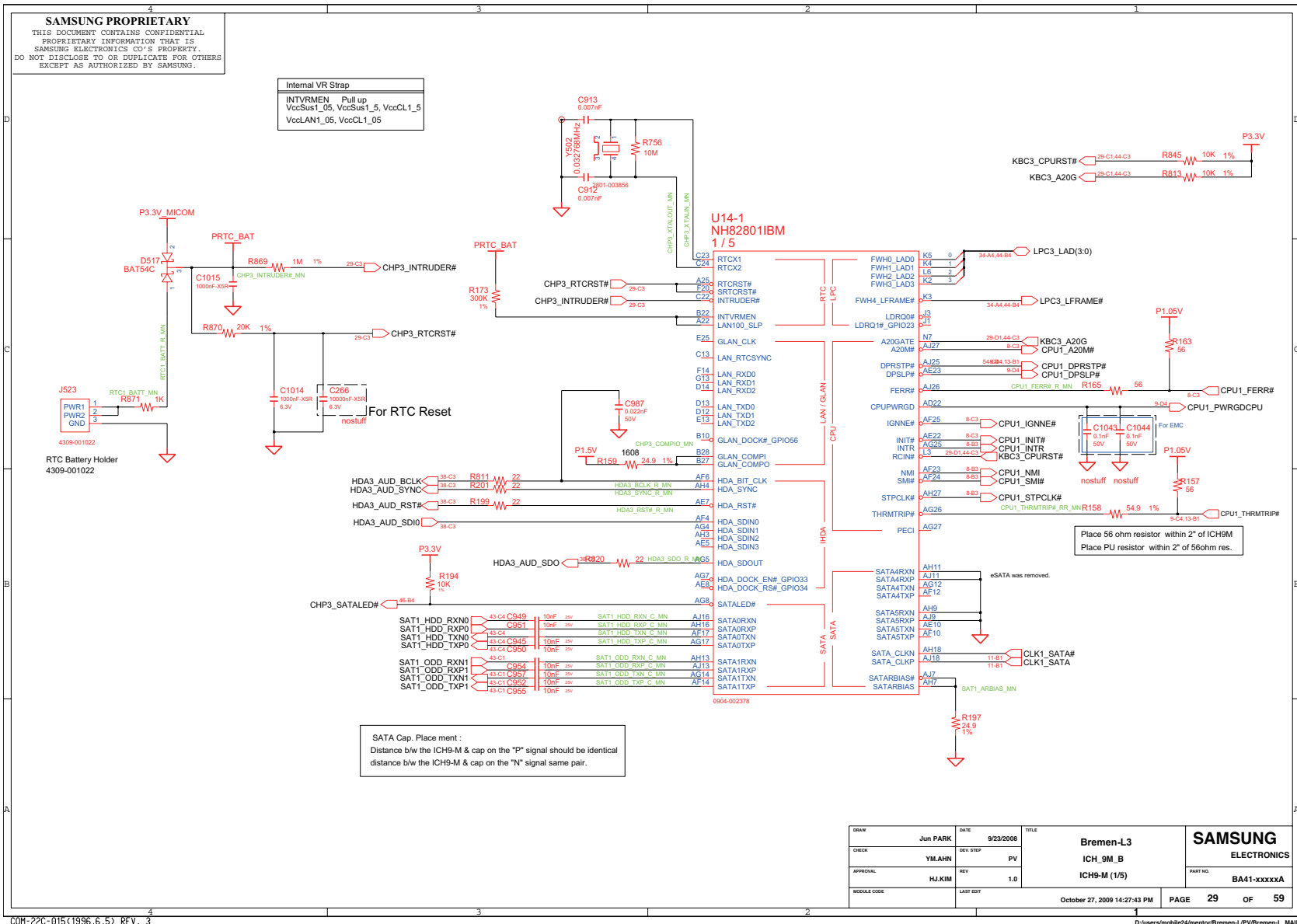
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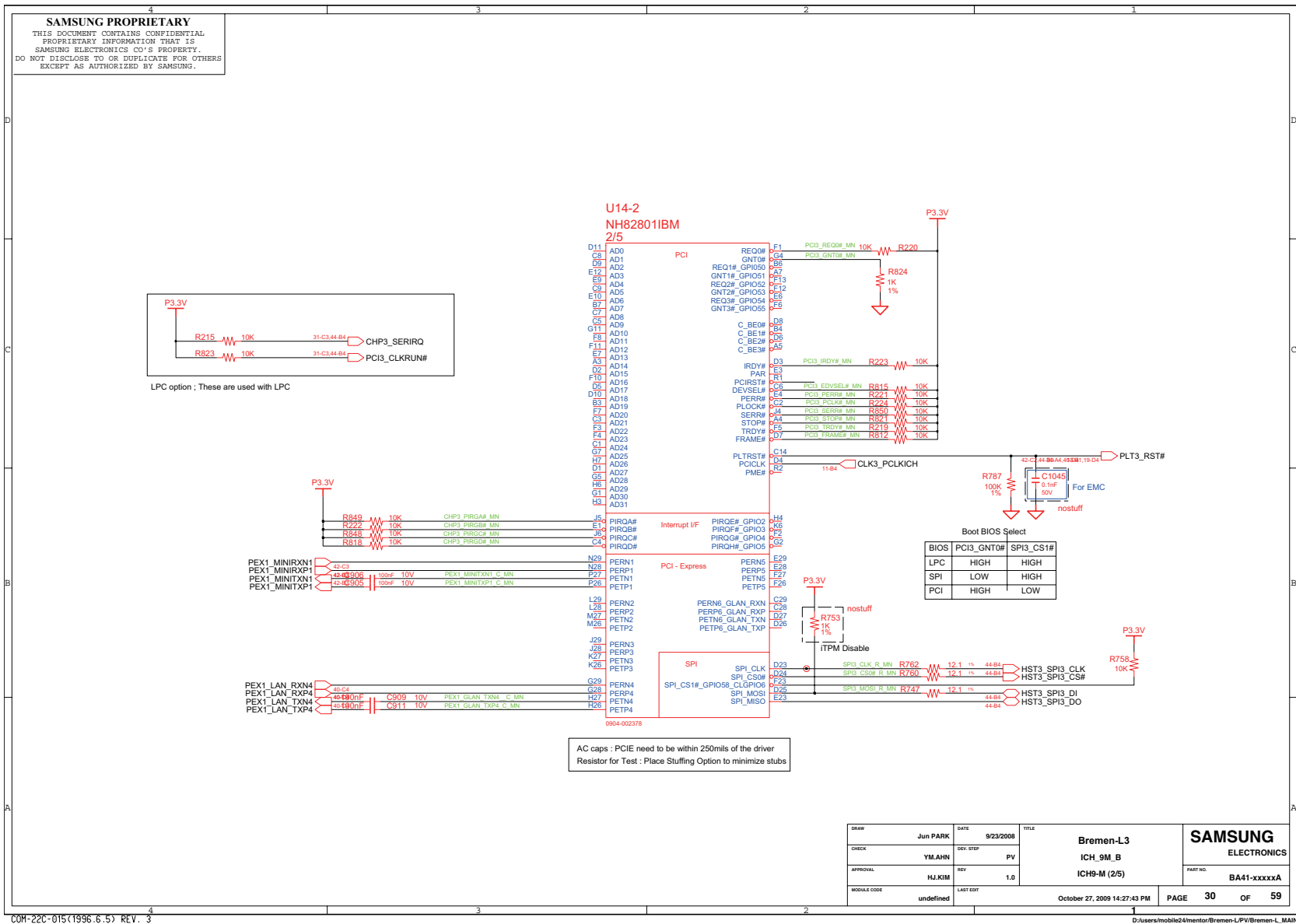
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# 8. Block Diagram and Schematic



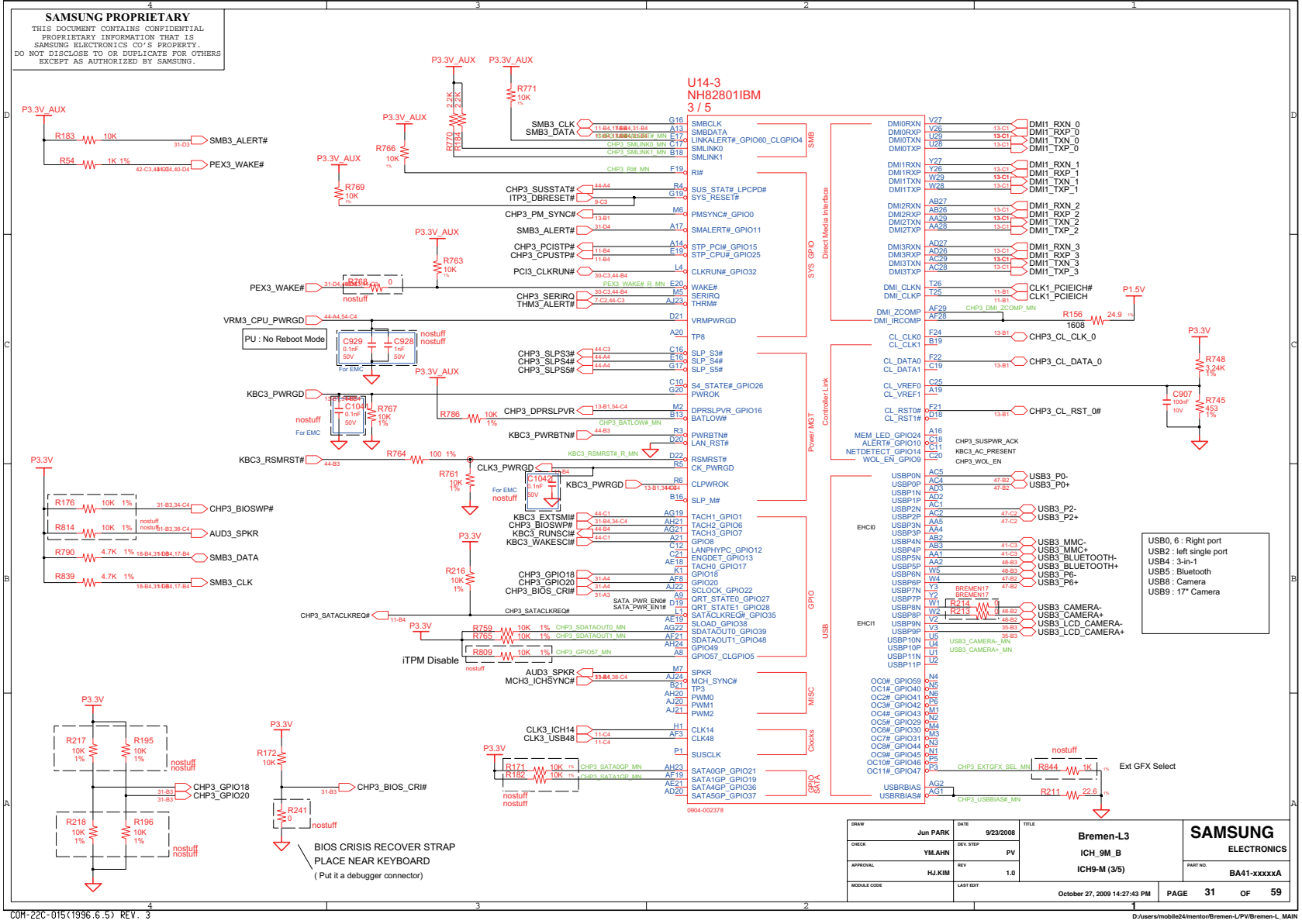
# 8. Block Diagram and Schematic



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APPROVAL	HJ.KIM	REV	1.0	ICH9-M (Z/5)	PART NO.	BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 27, 2009 14:27:43 PM	PAGE	30	OF 59

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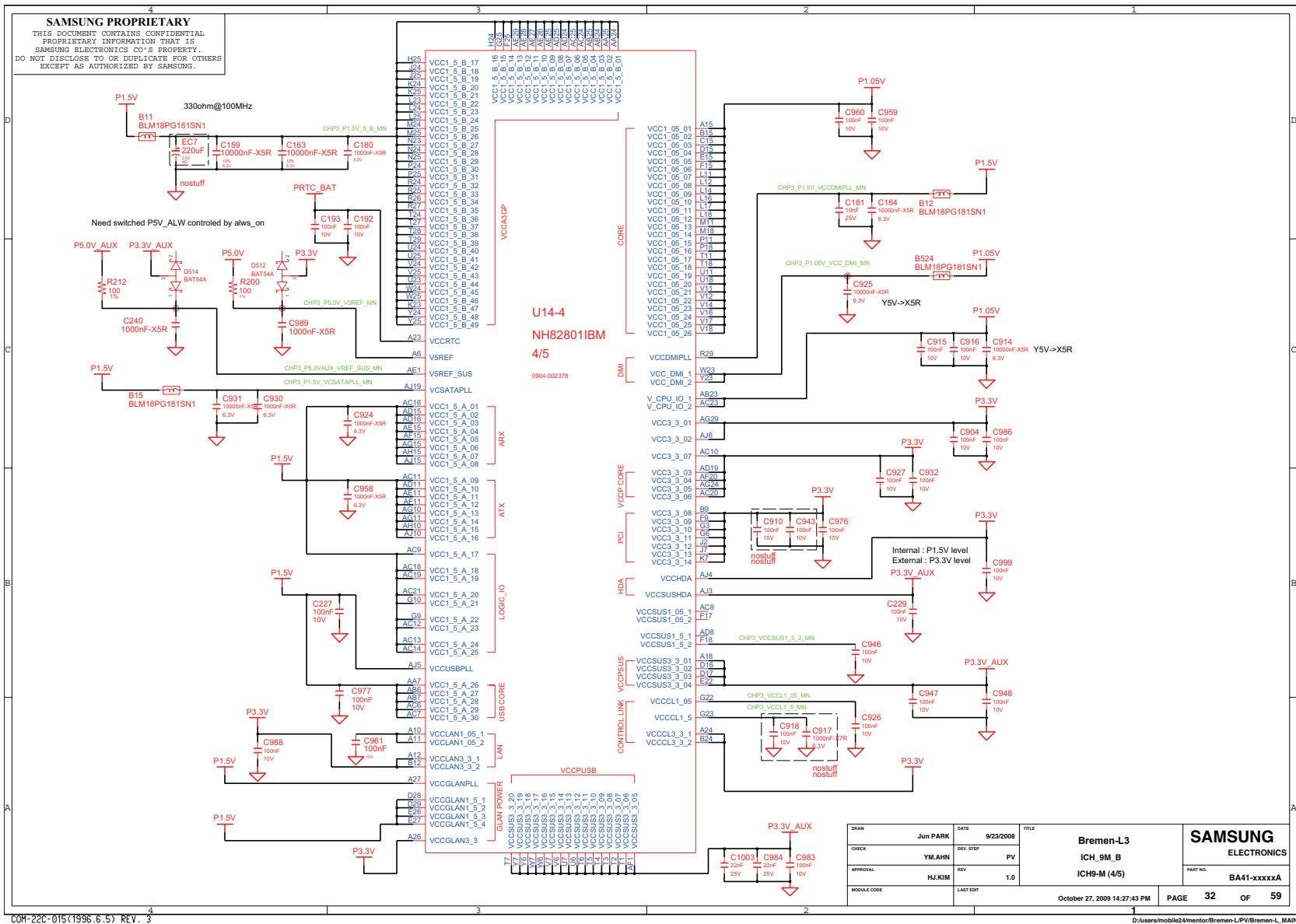
### 8. Block Diagram and Schematic



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APPROVAL	HJKIM	REV.	1.0		ICH9M (3/5)	PART NO. BA41-xxxxxA
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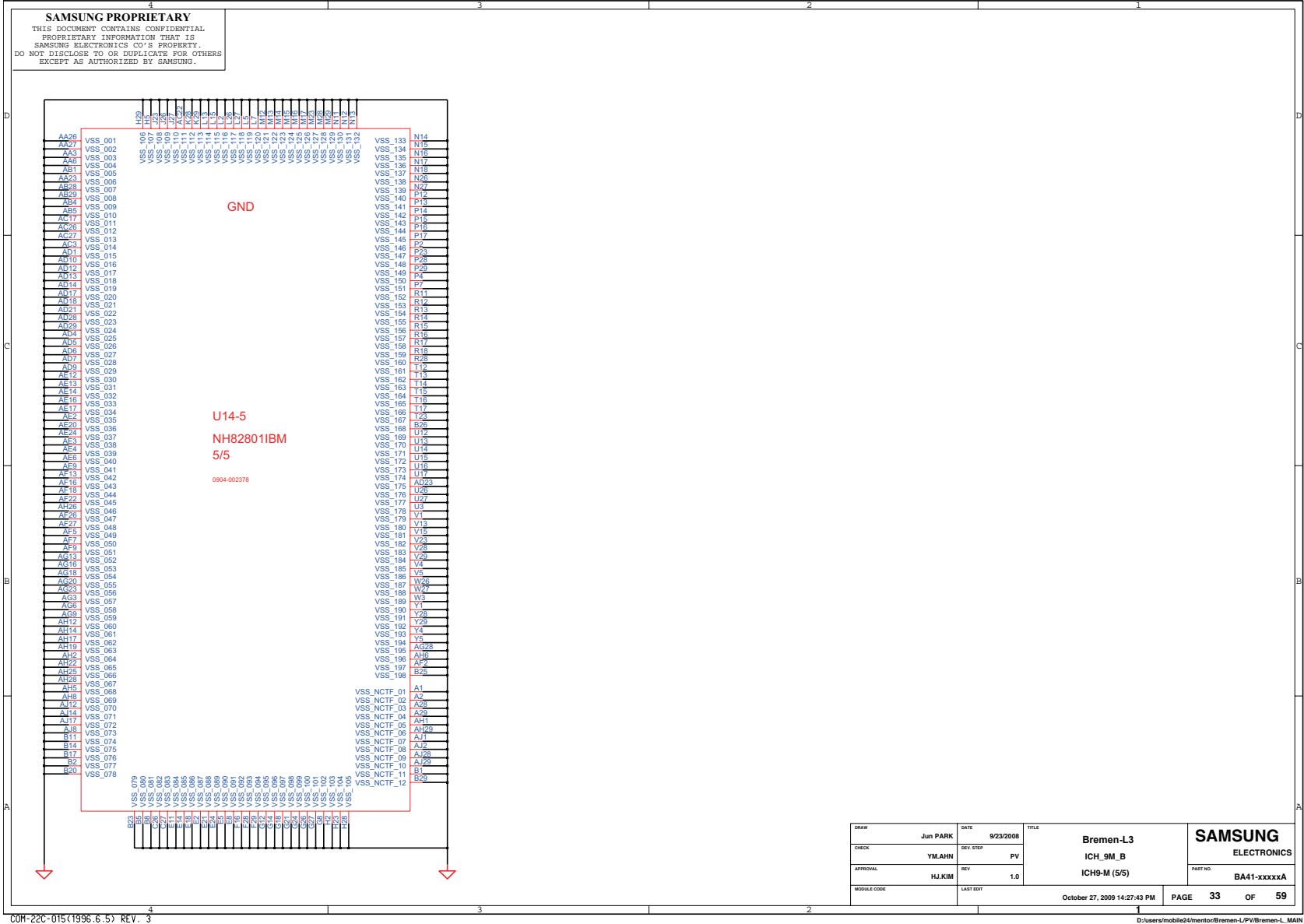
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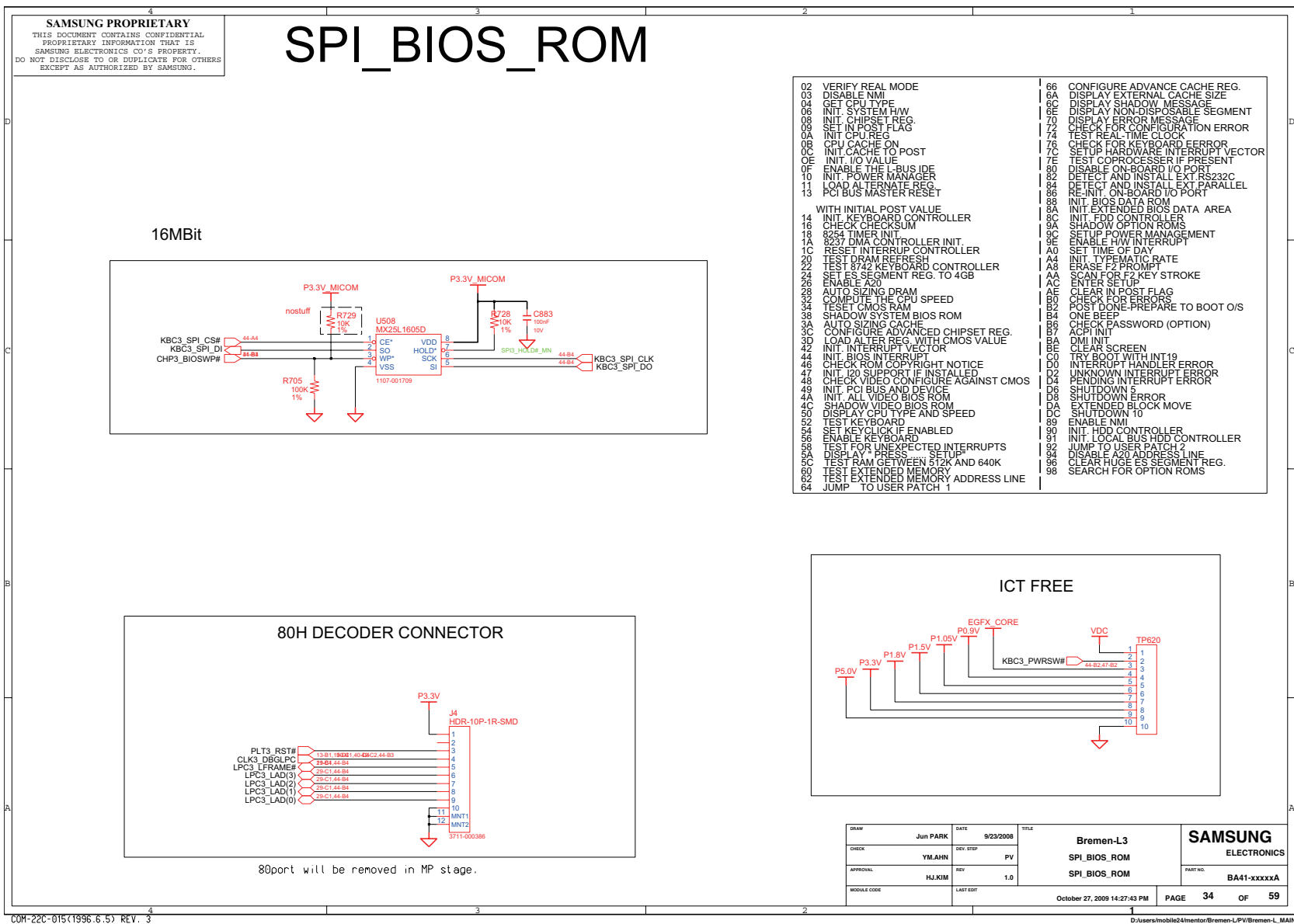


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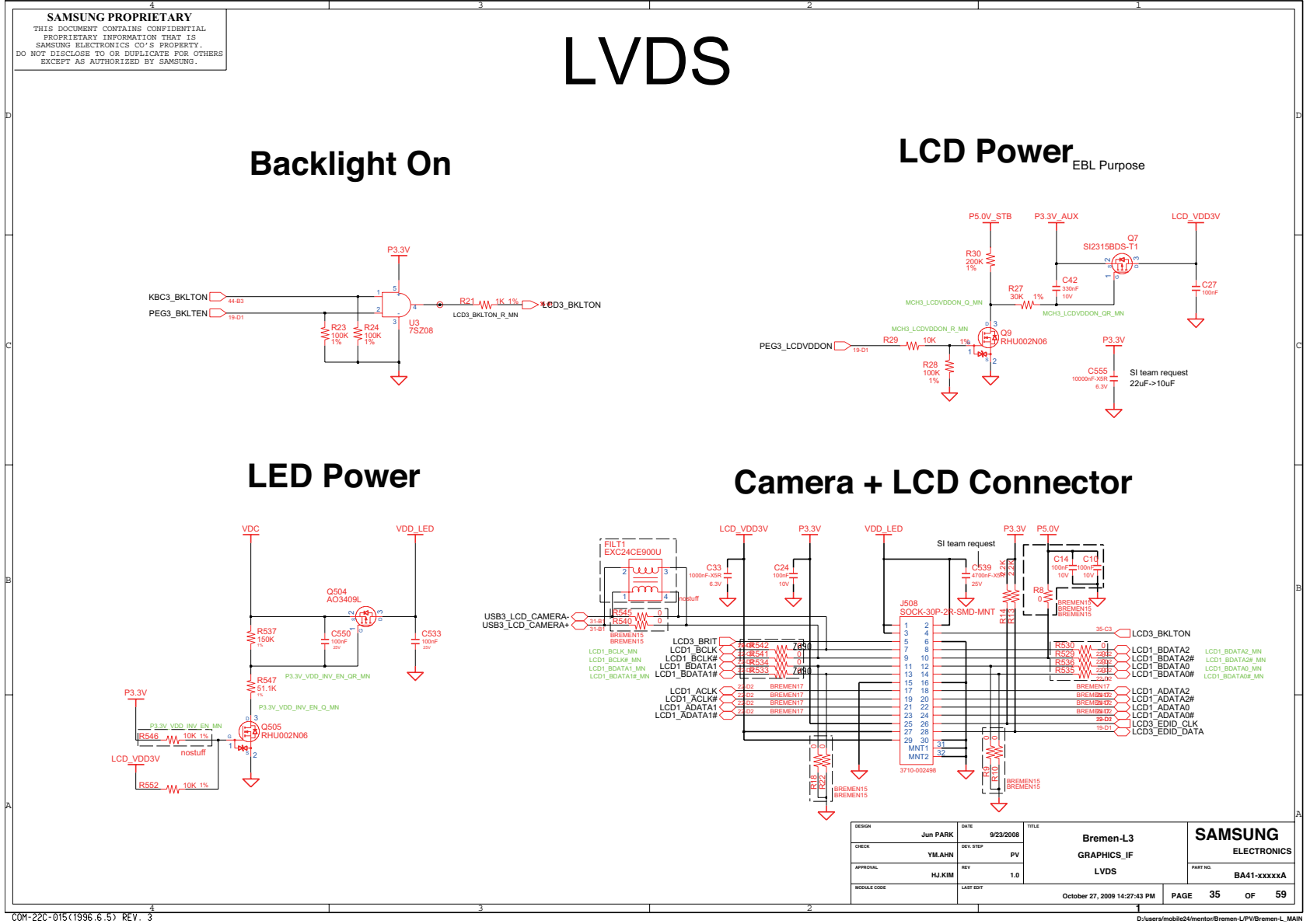
## 8. Block Diagram and Schematic



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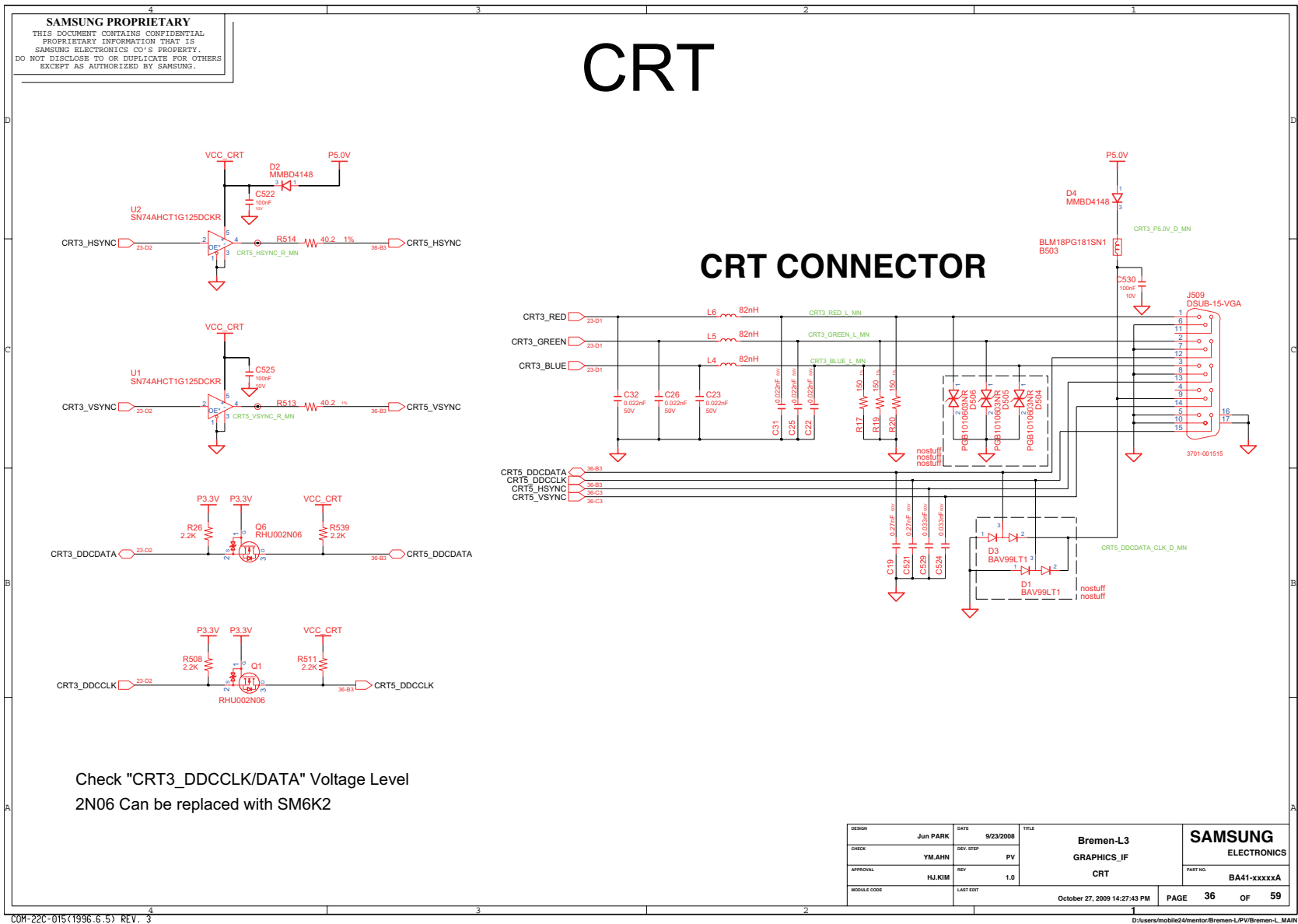


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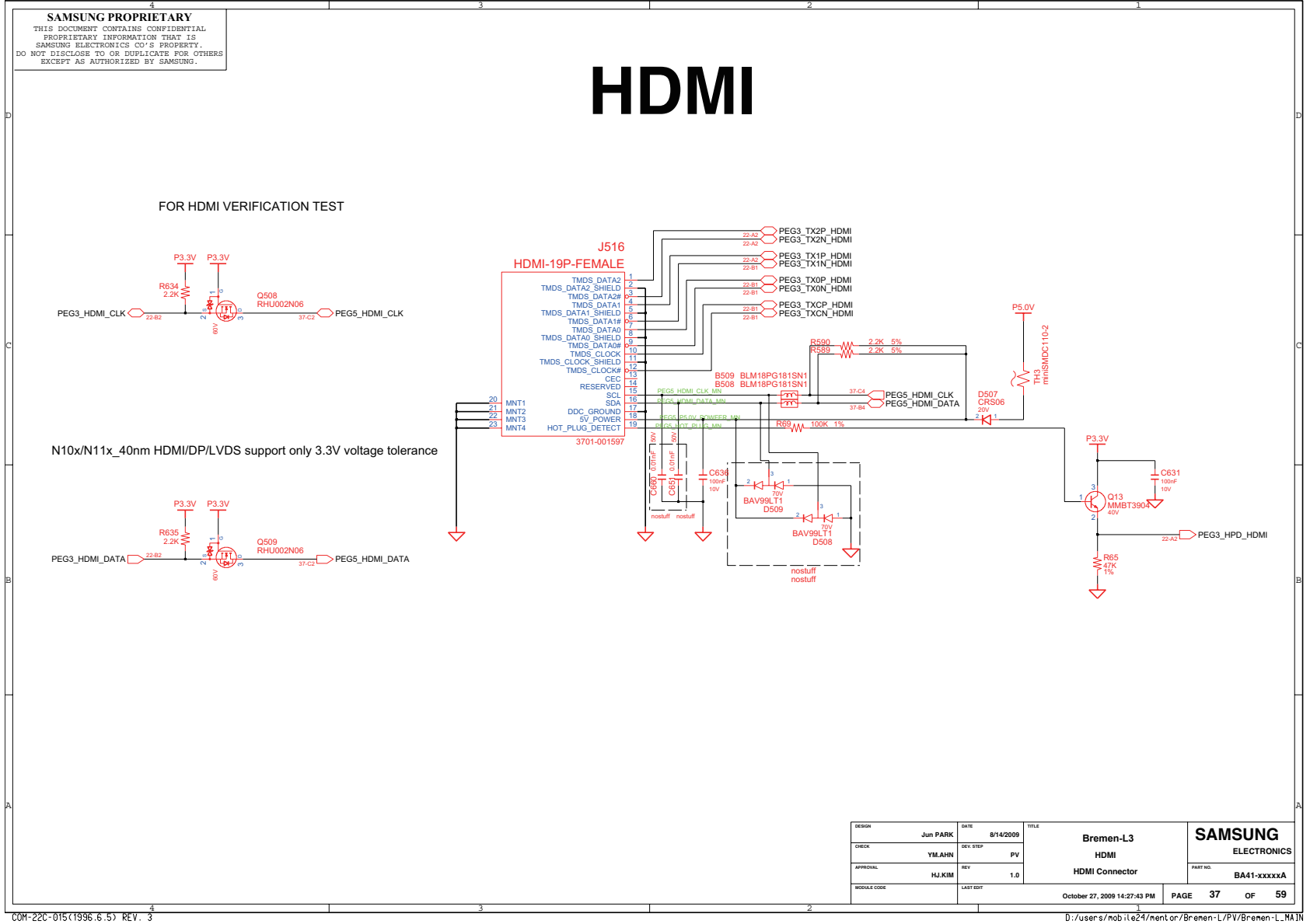


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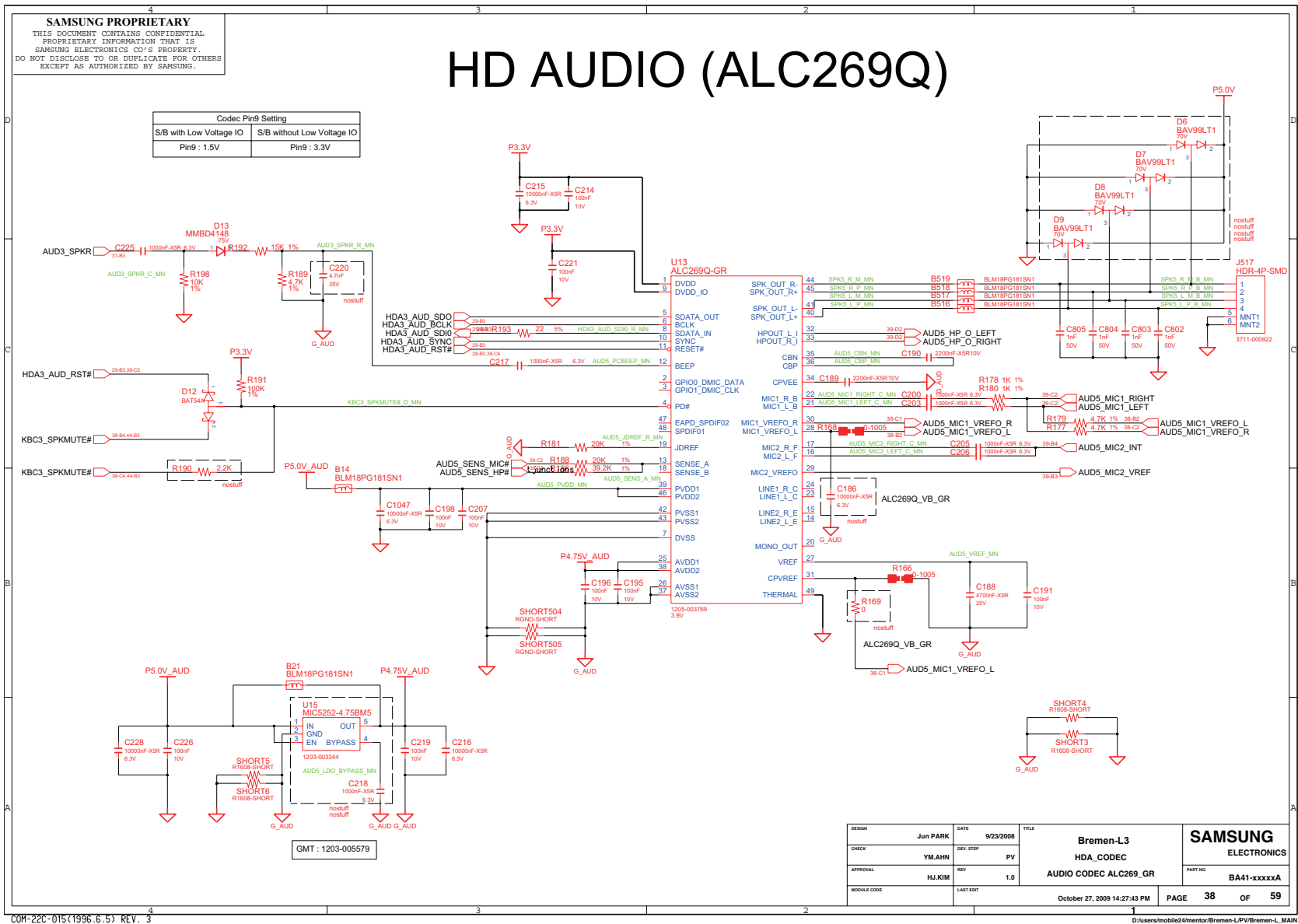
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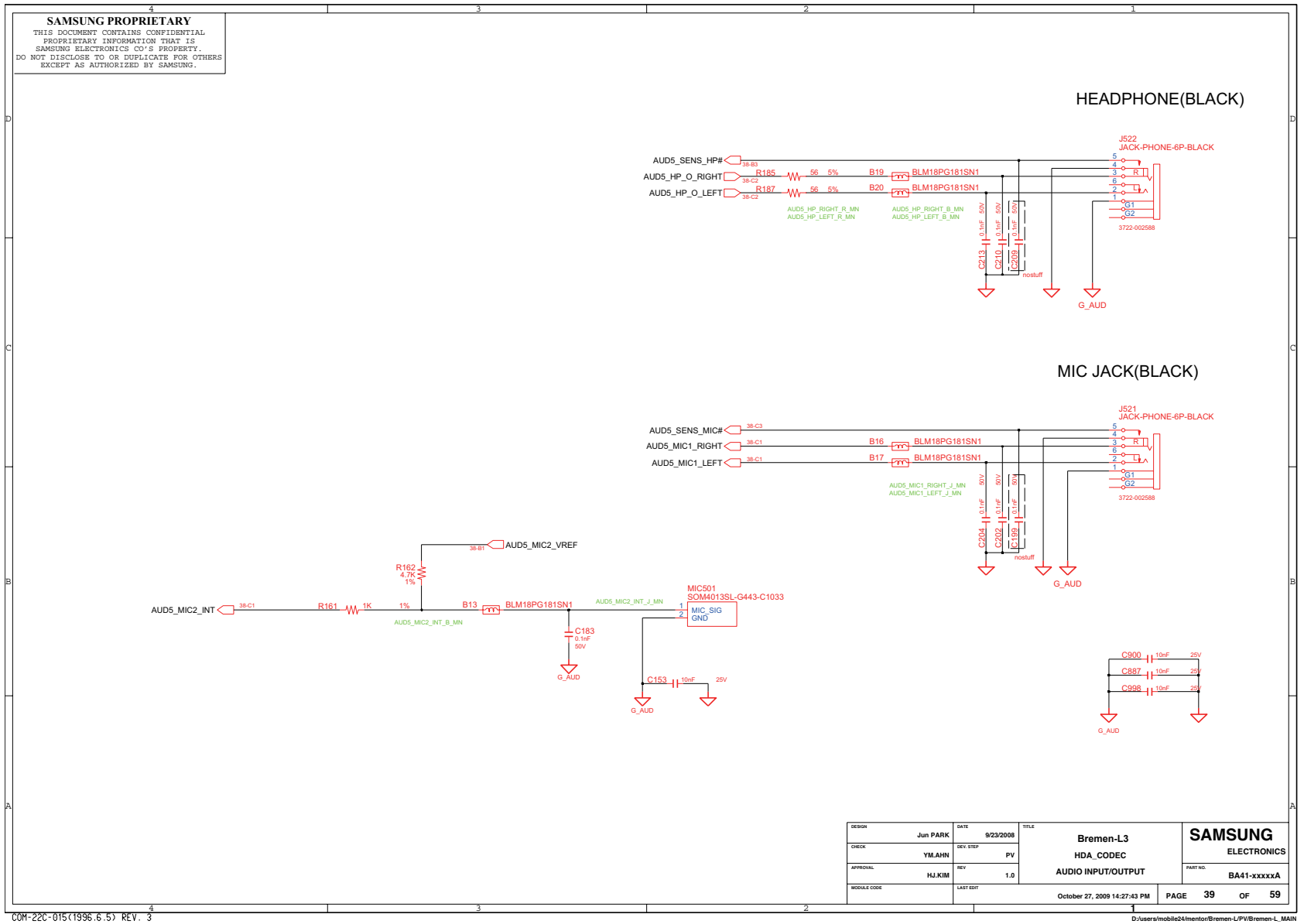
## 8. Block Diagram and Schematic



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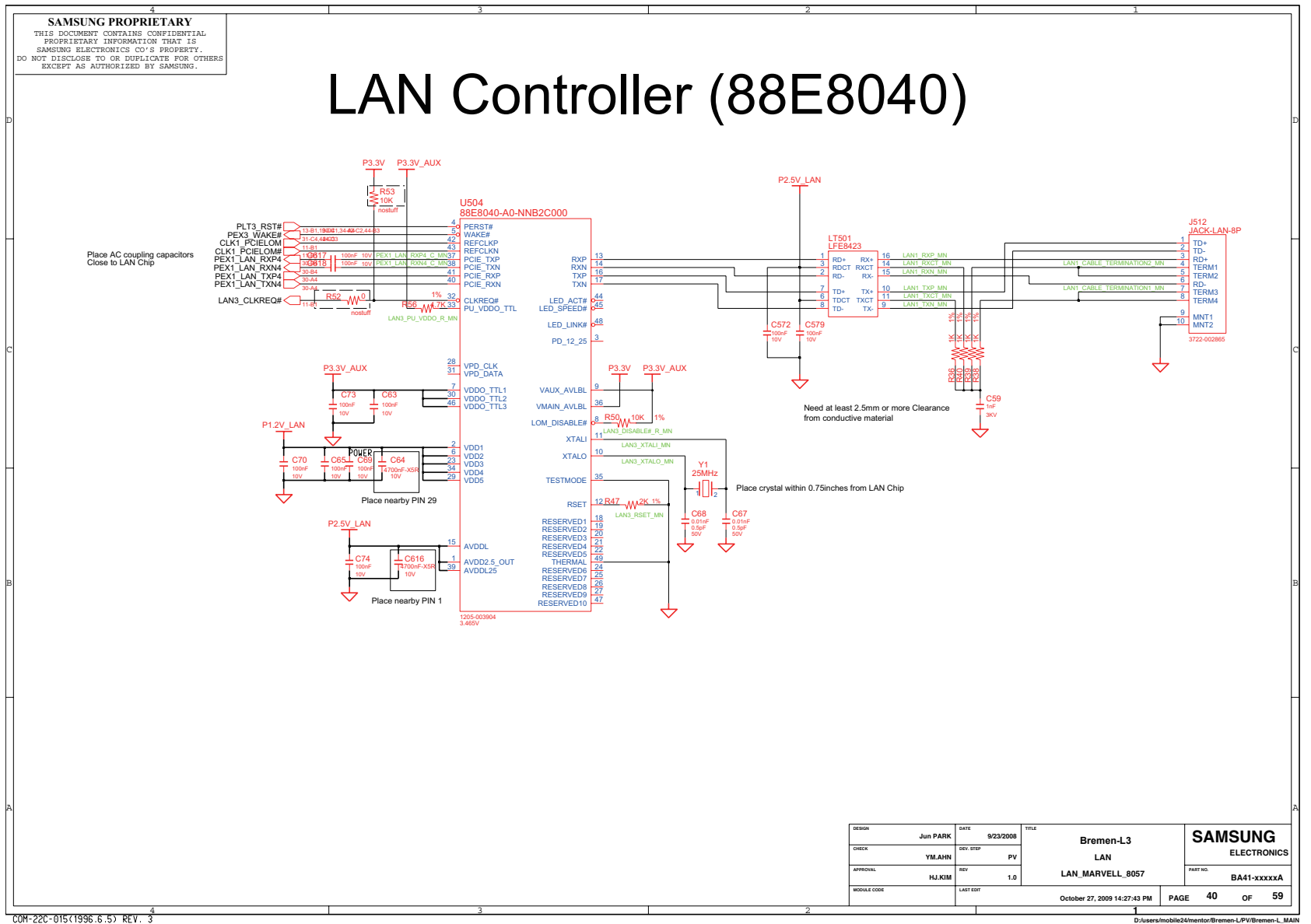


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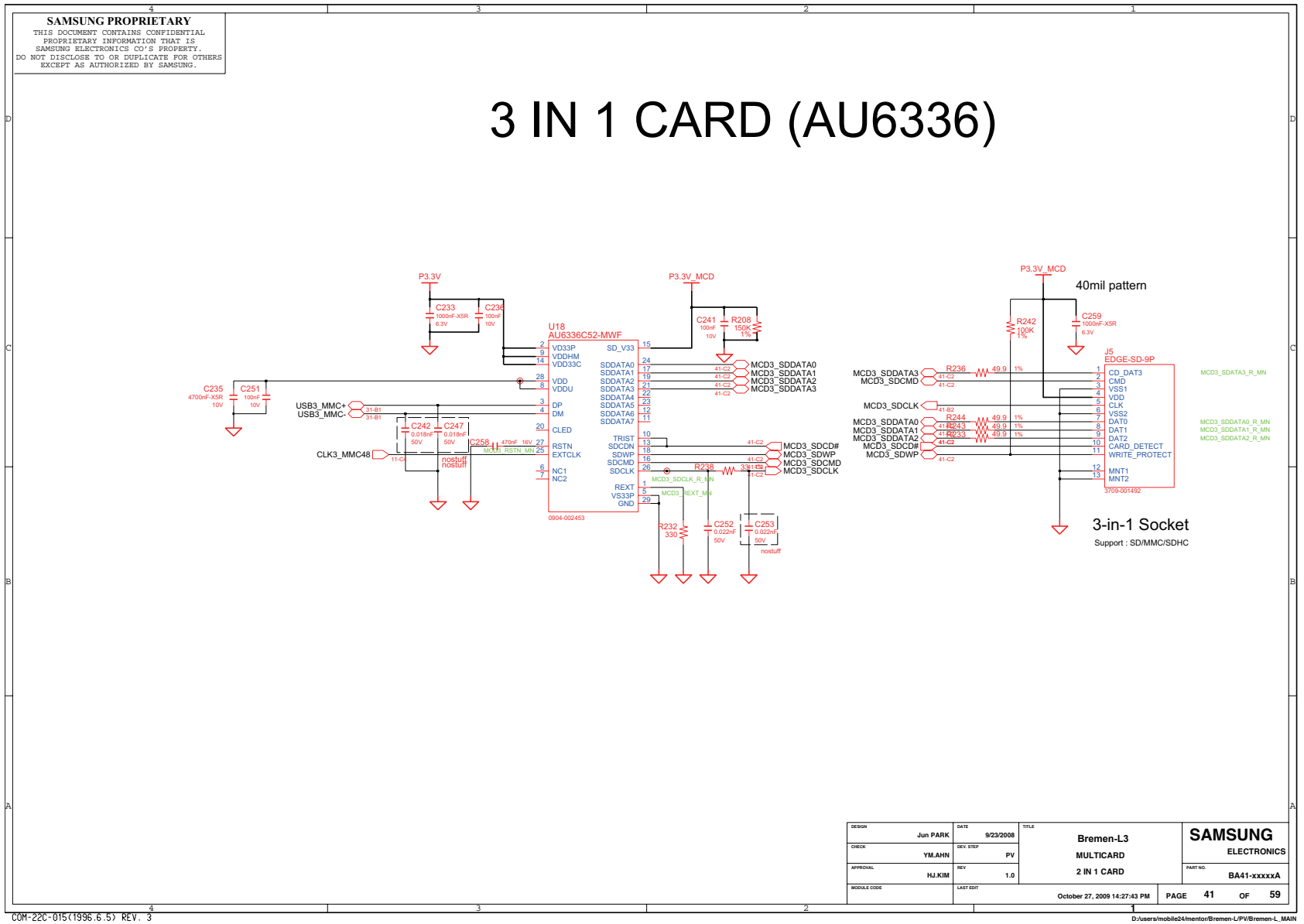
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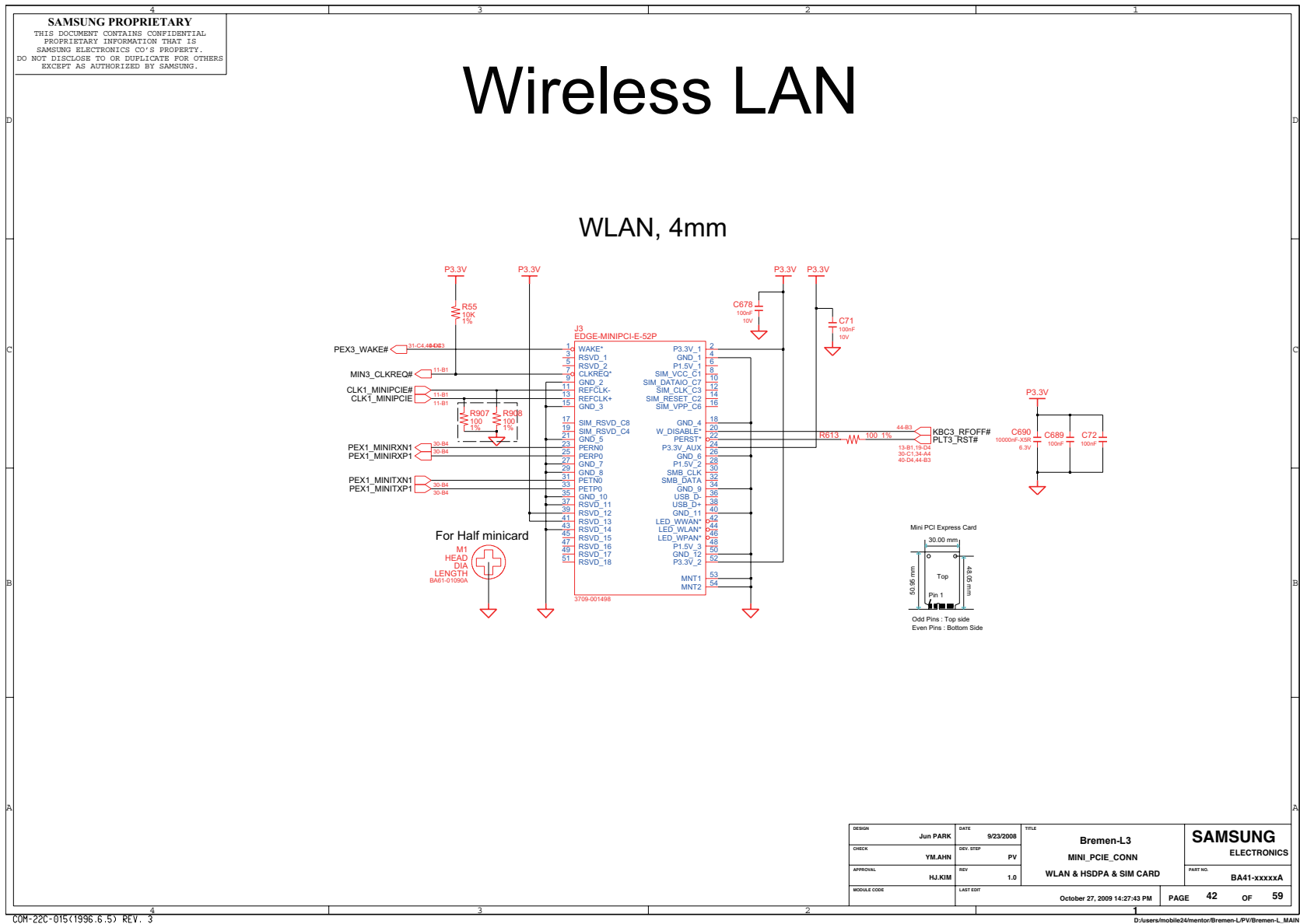


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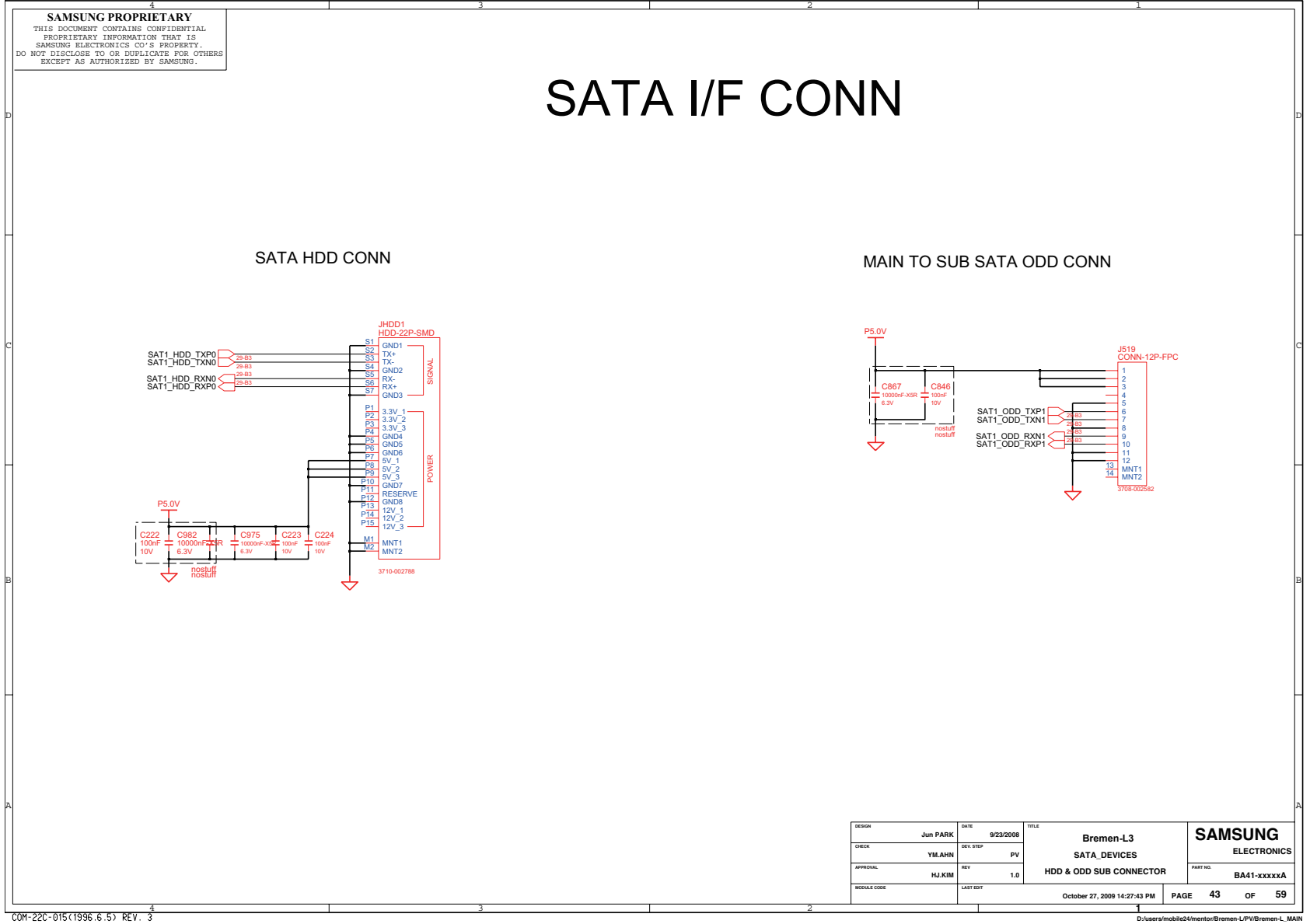


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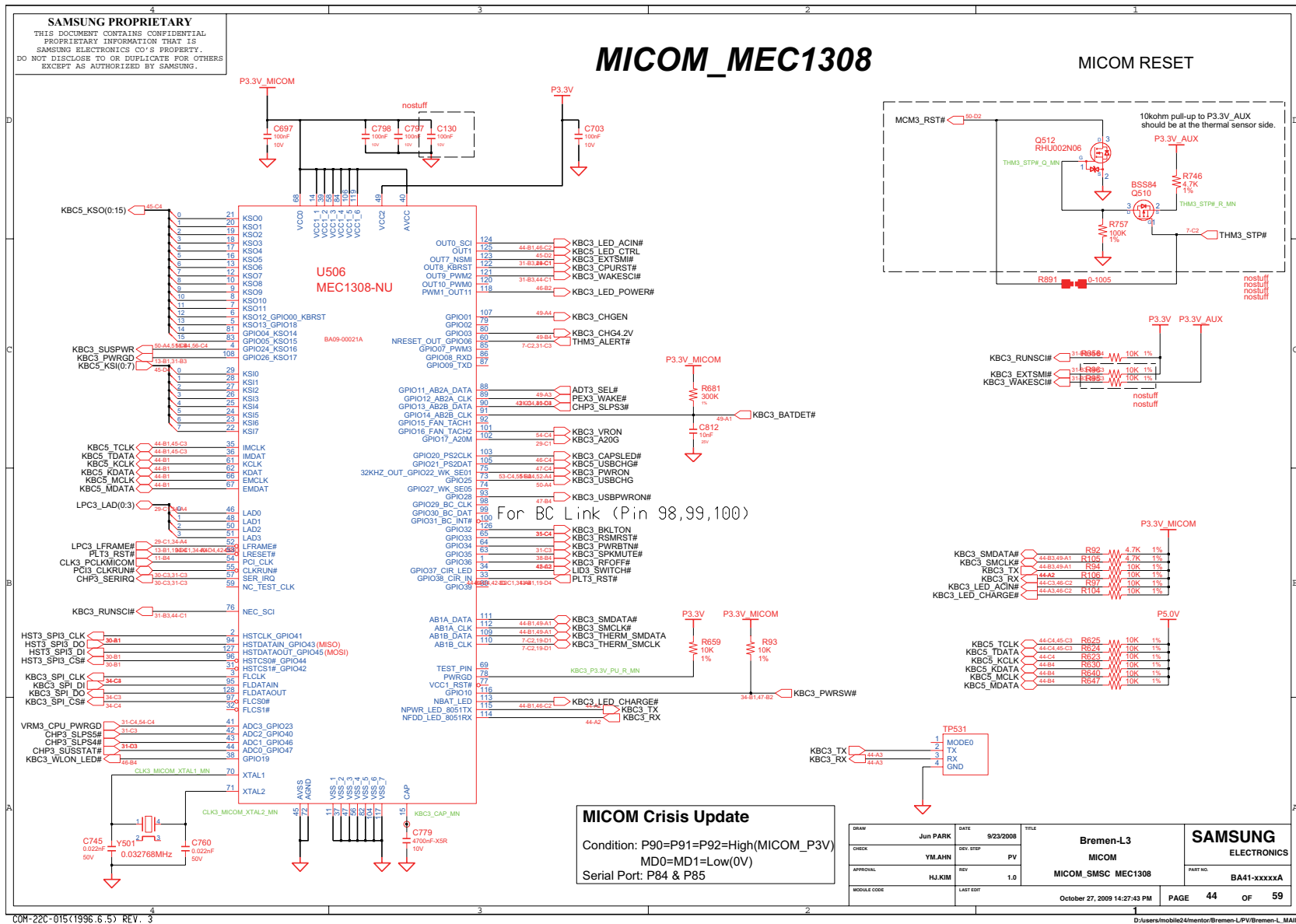
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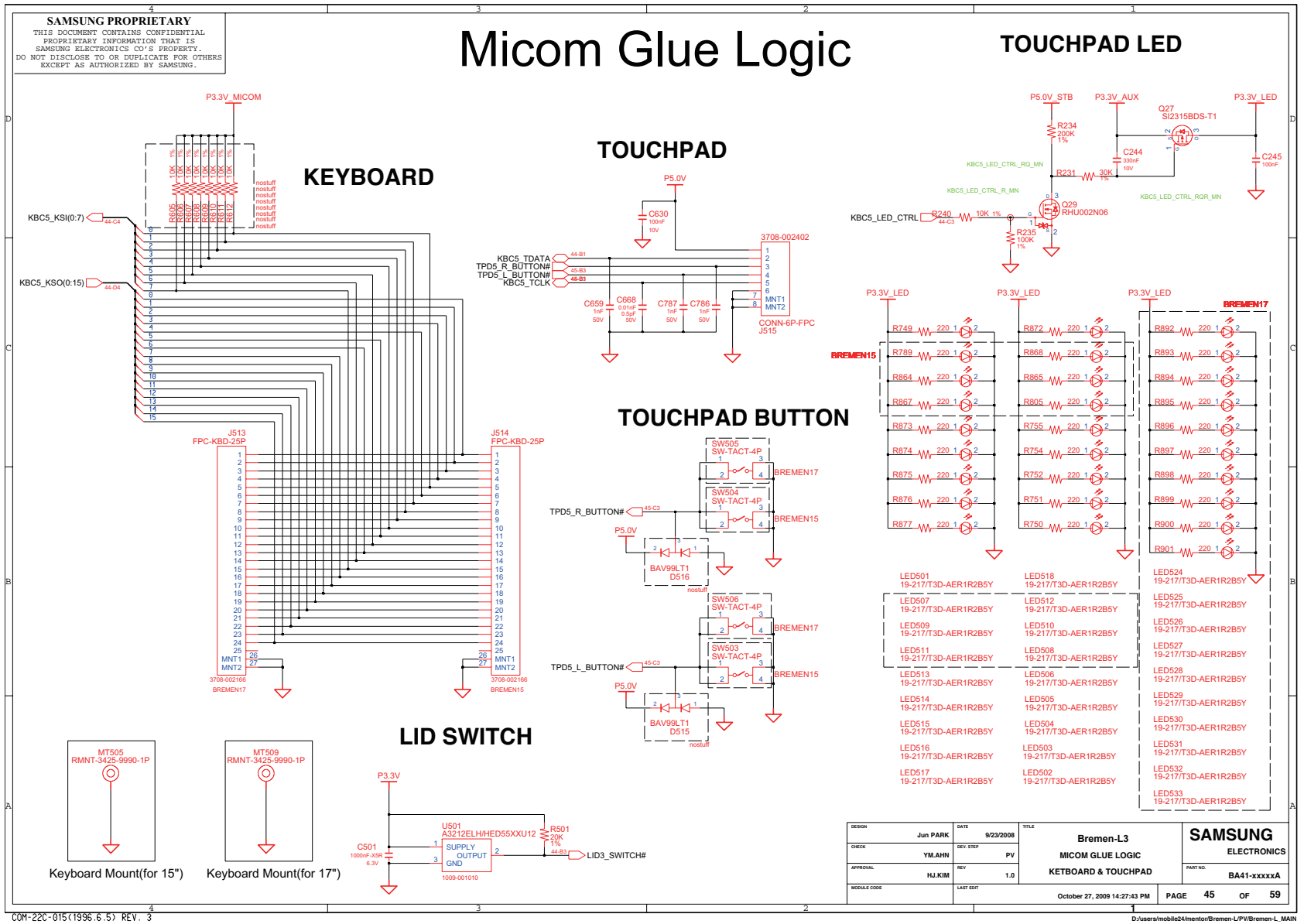
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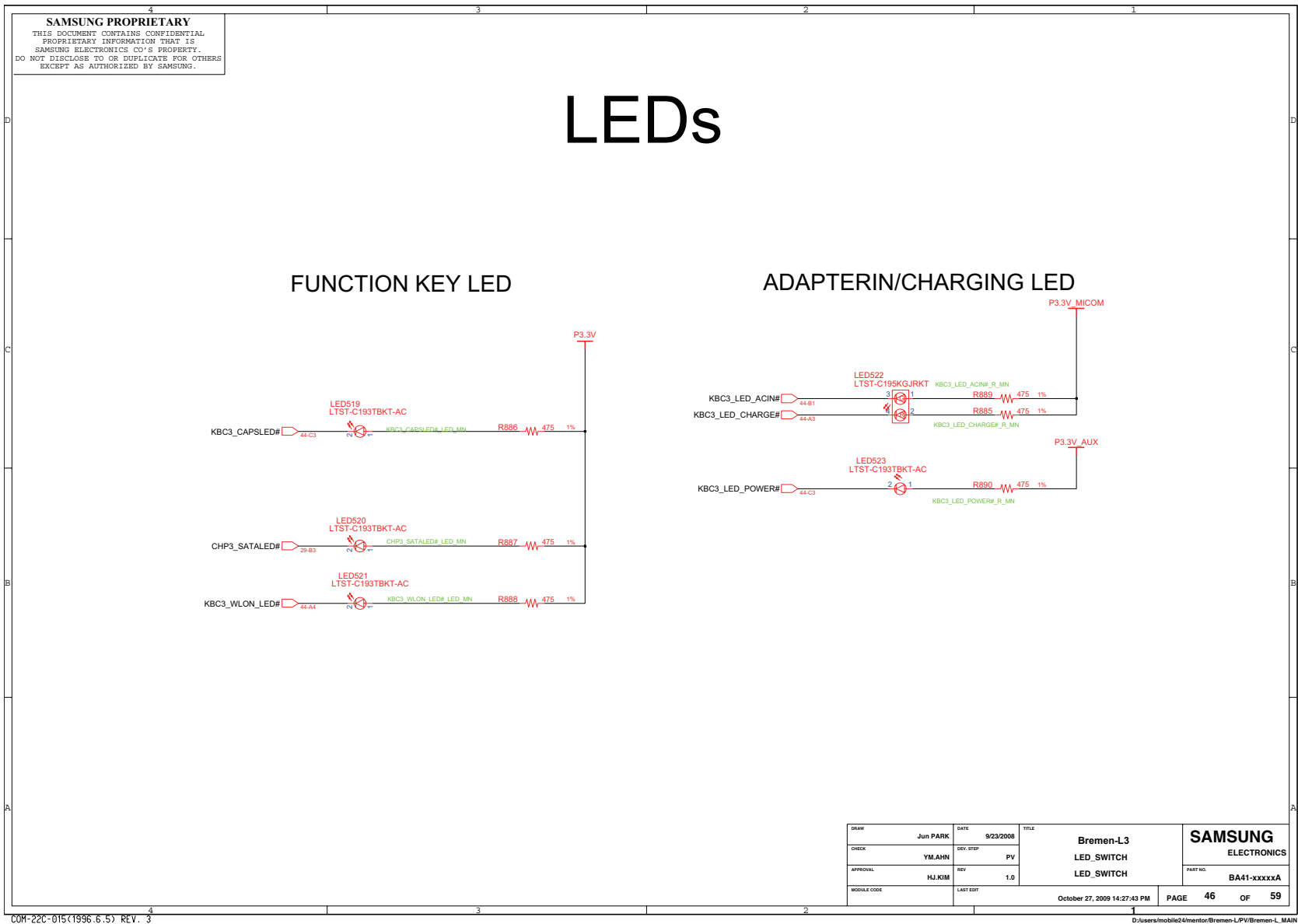
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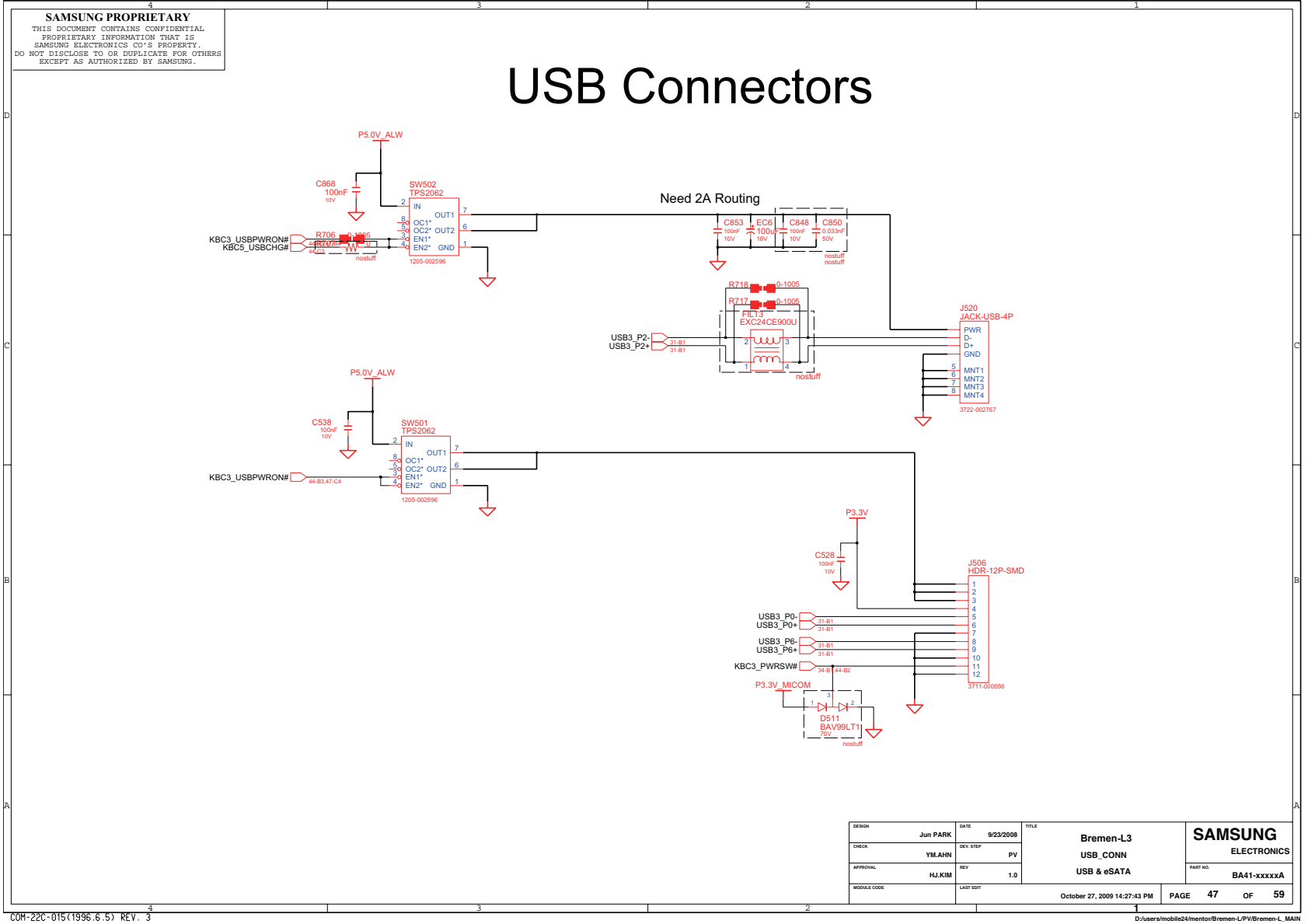
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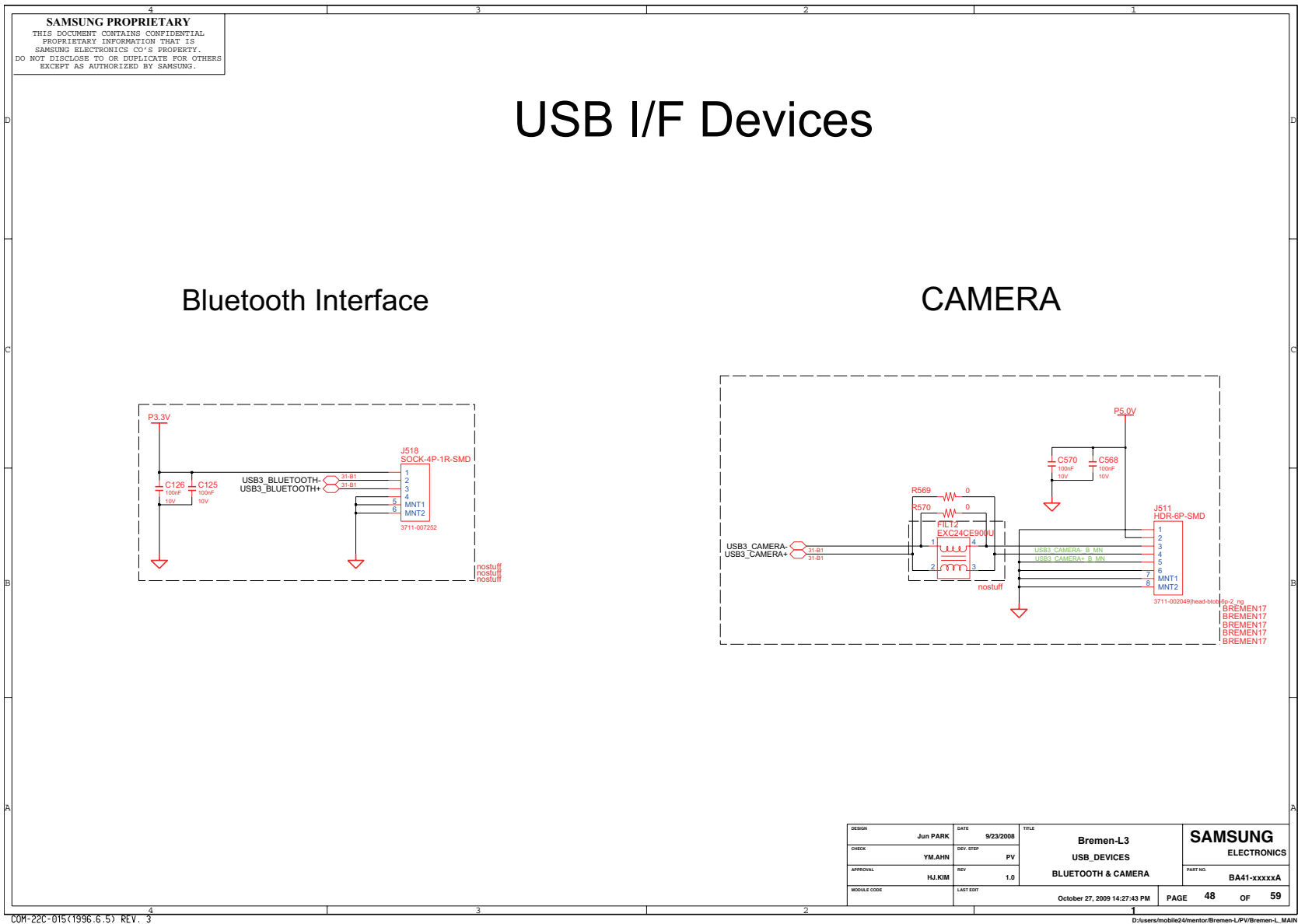
## 8. Block Diagram and Schematic



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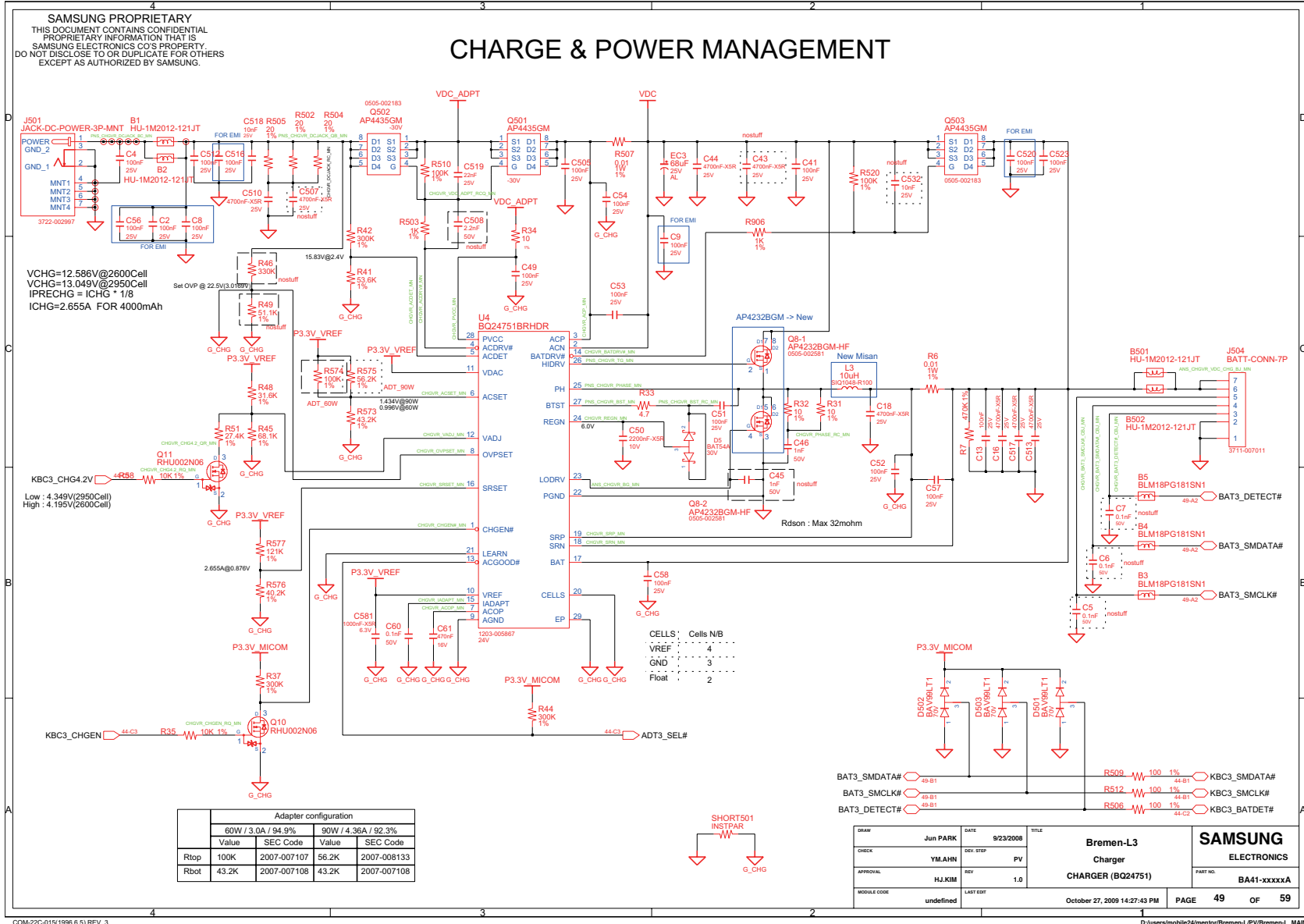


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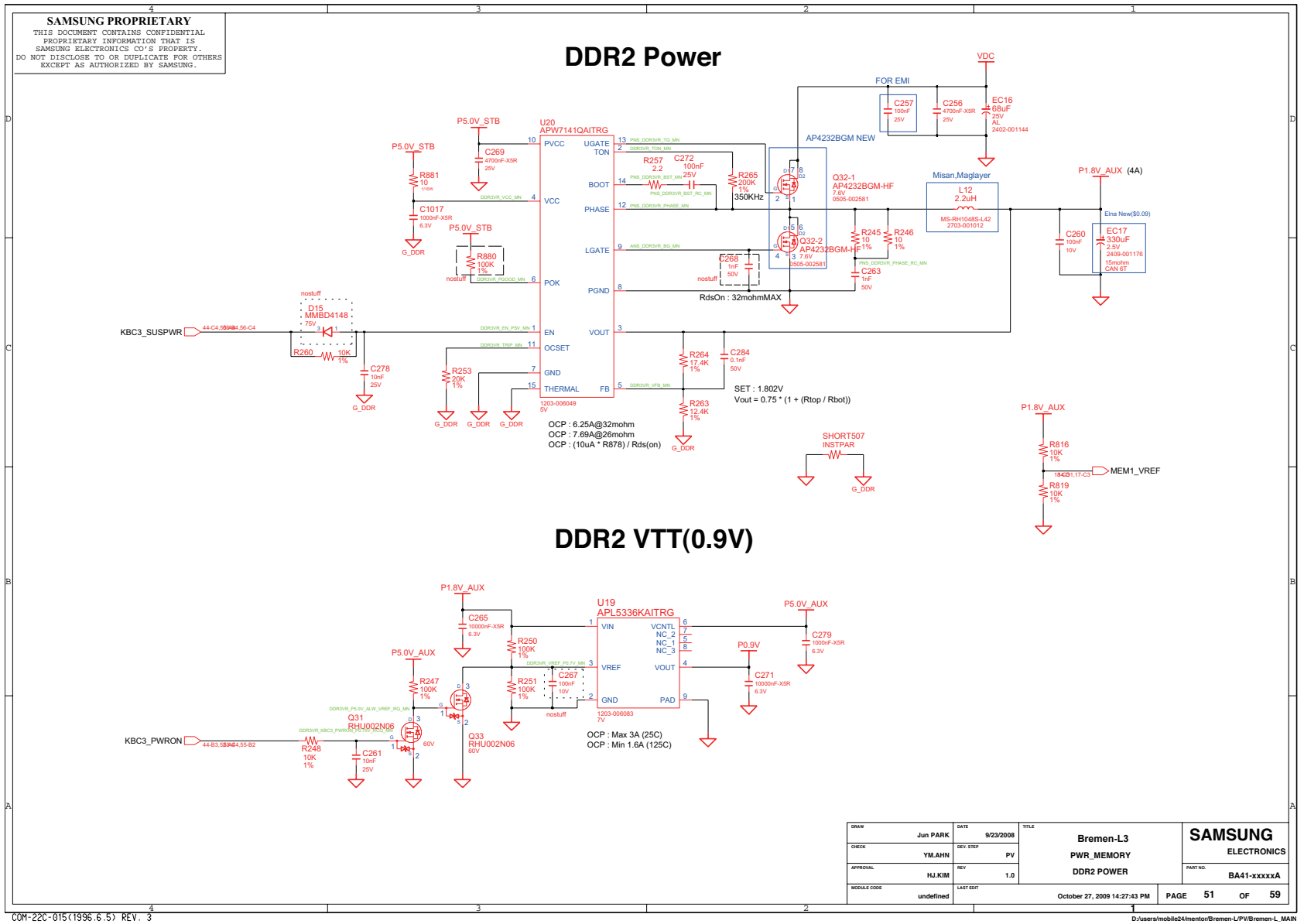


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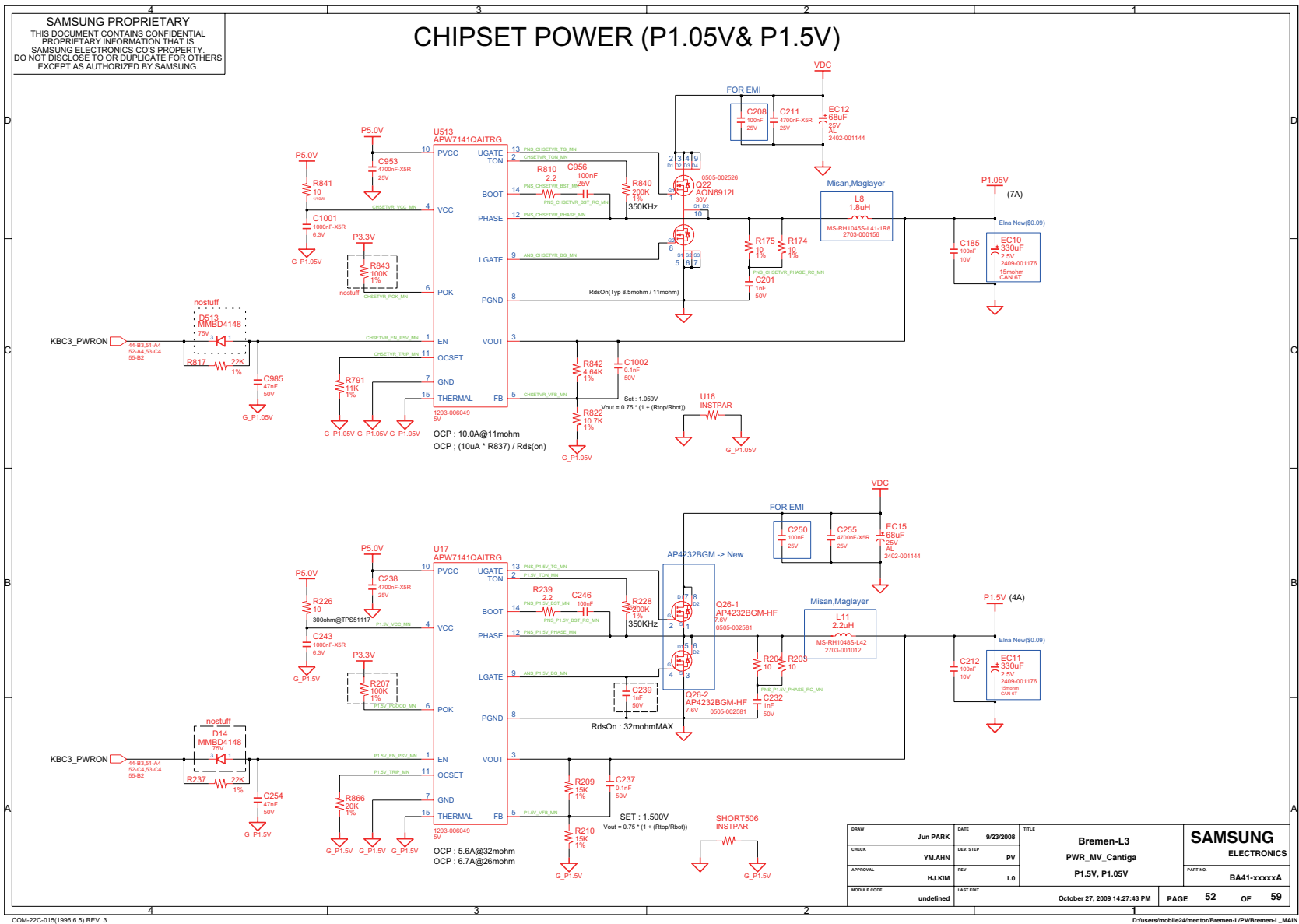
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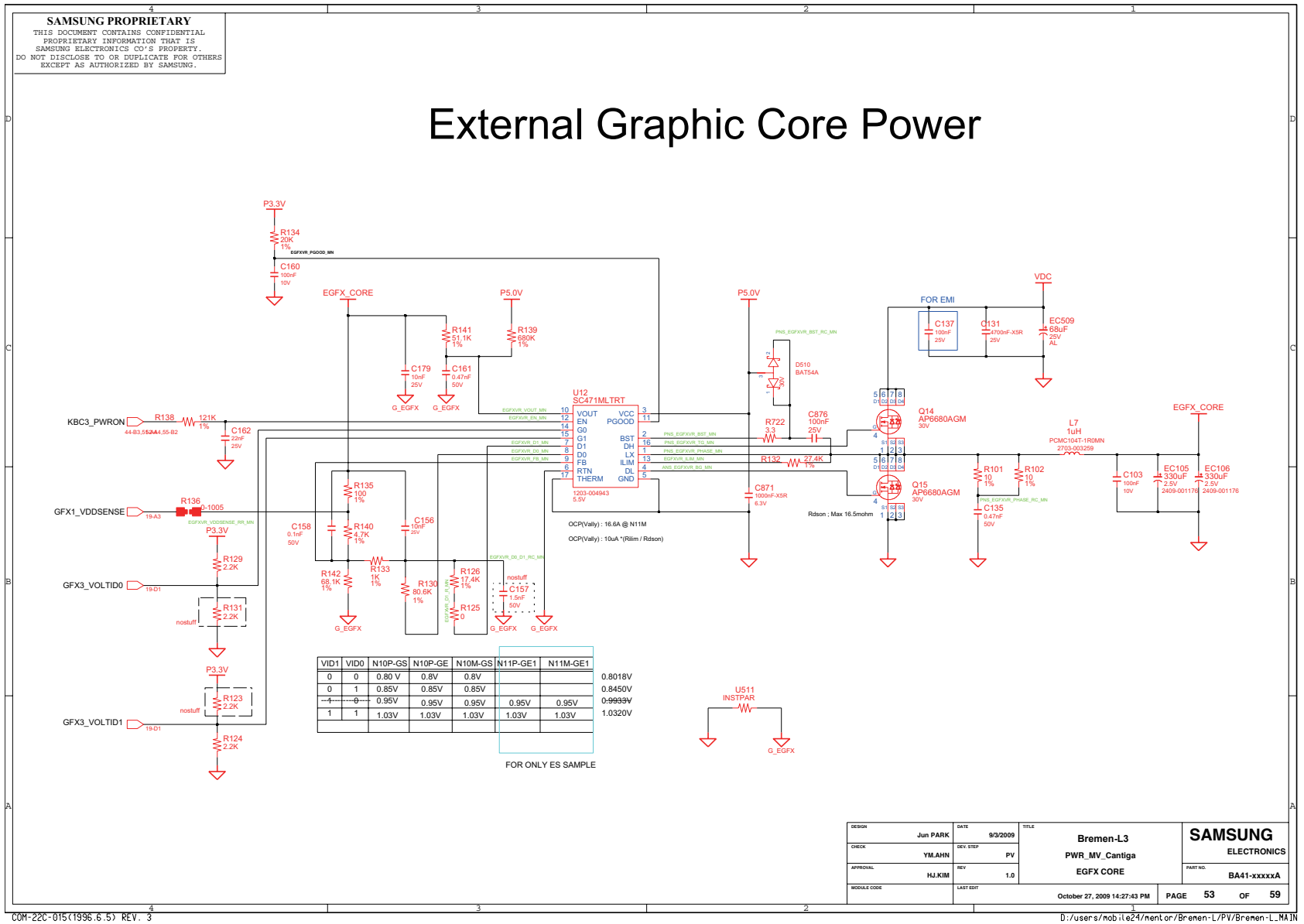
## 8. Block Diagram and Schematic



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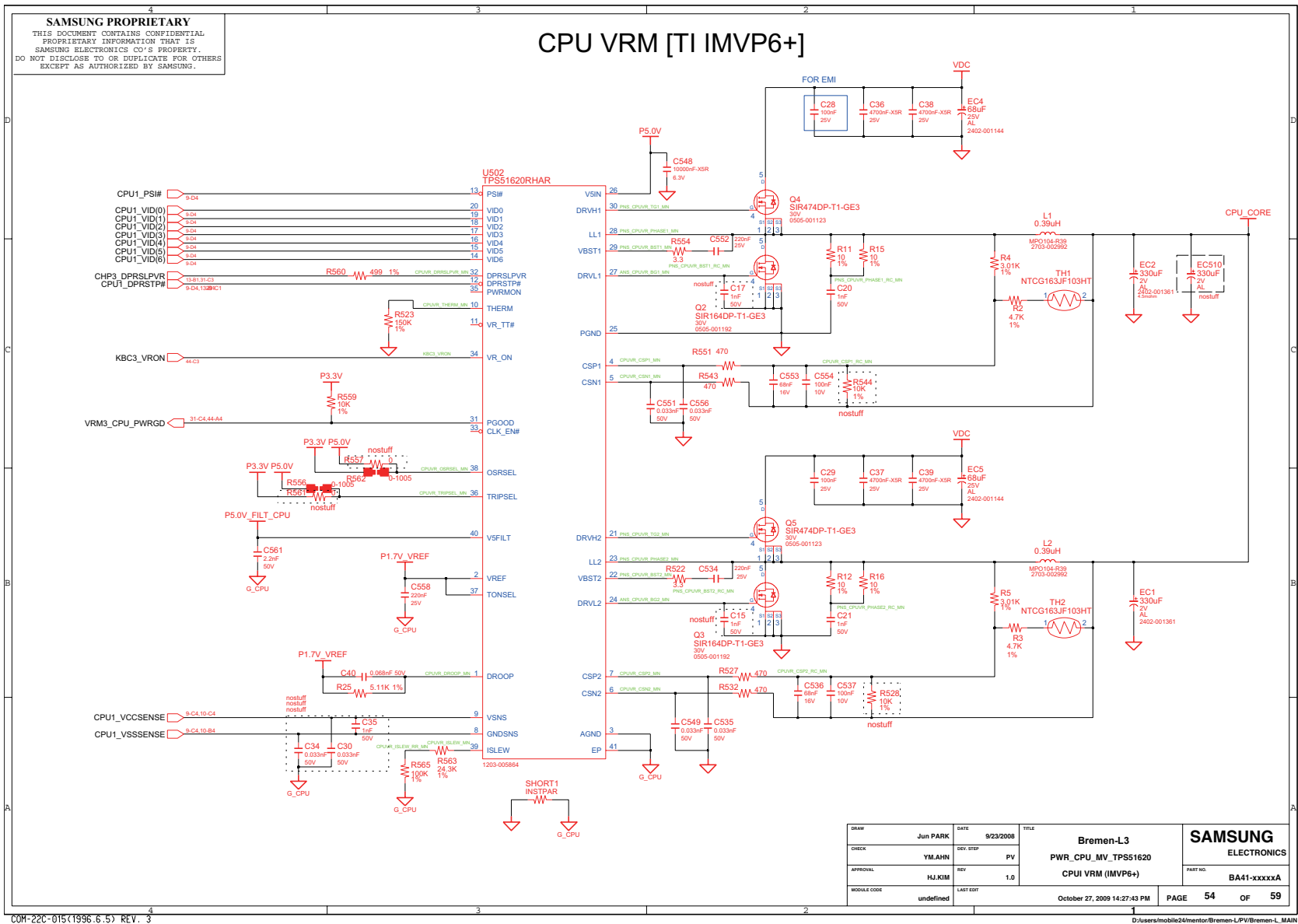


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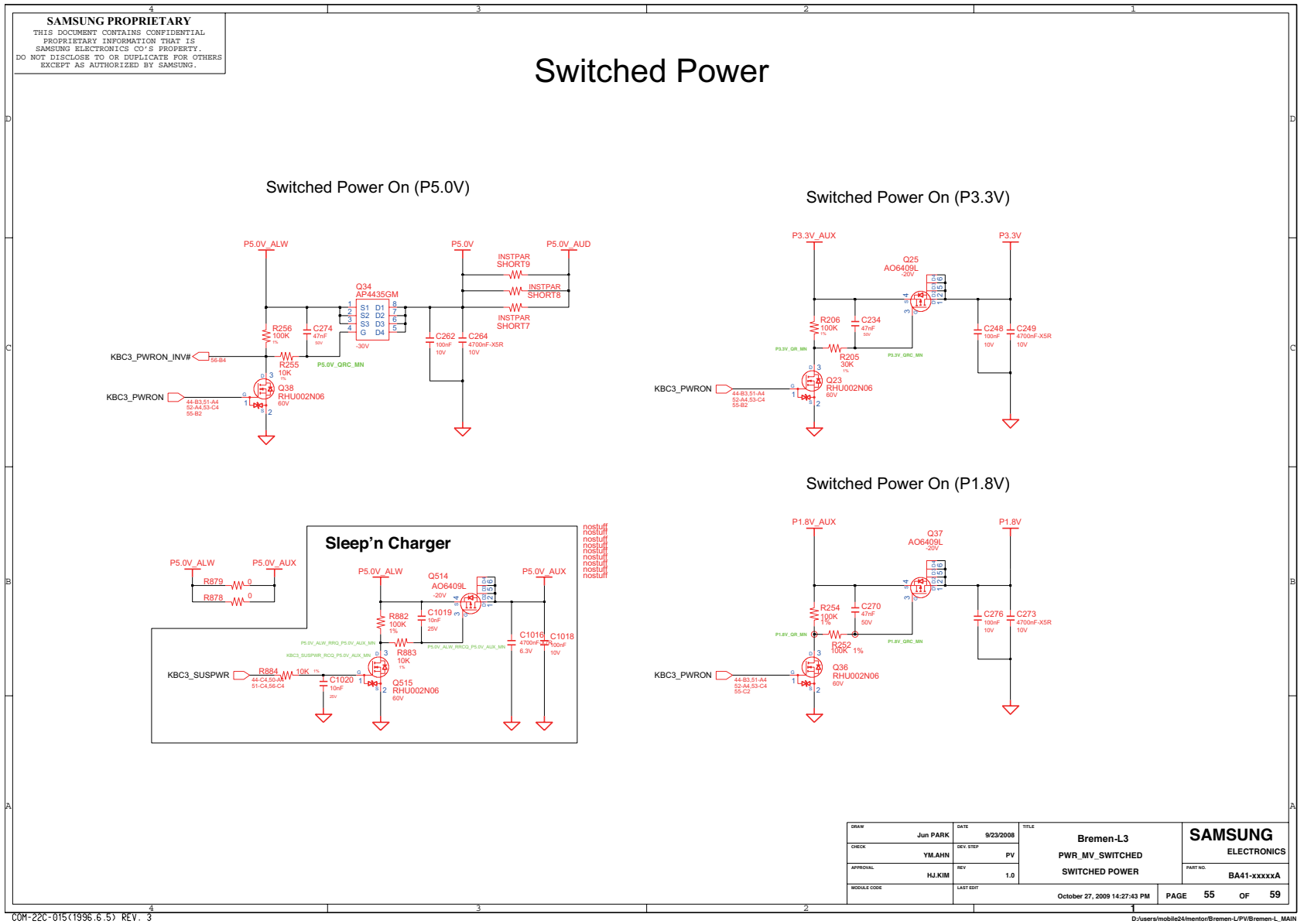
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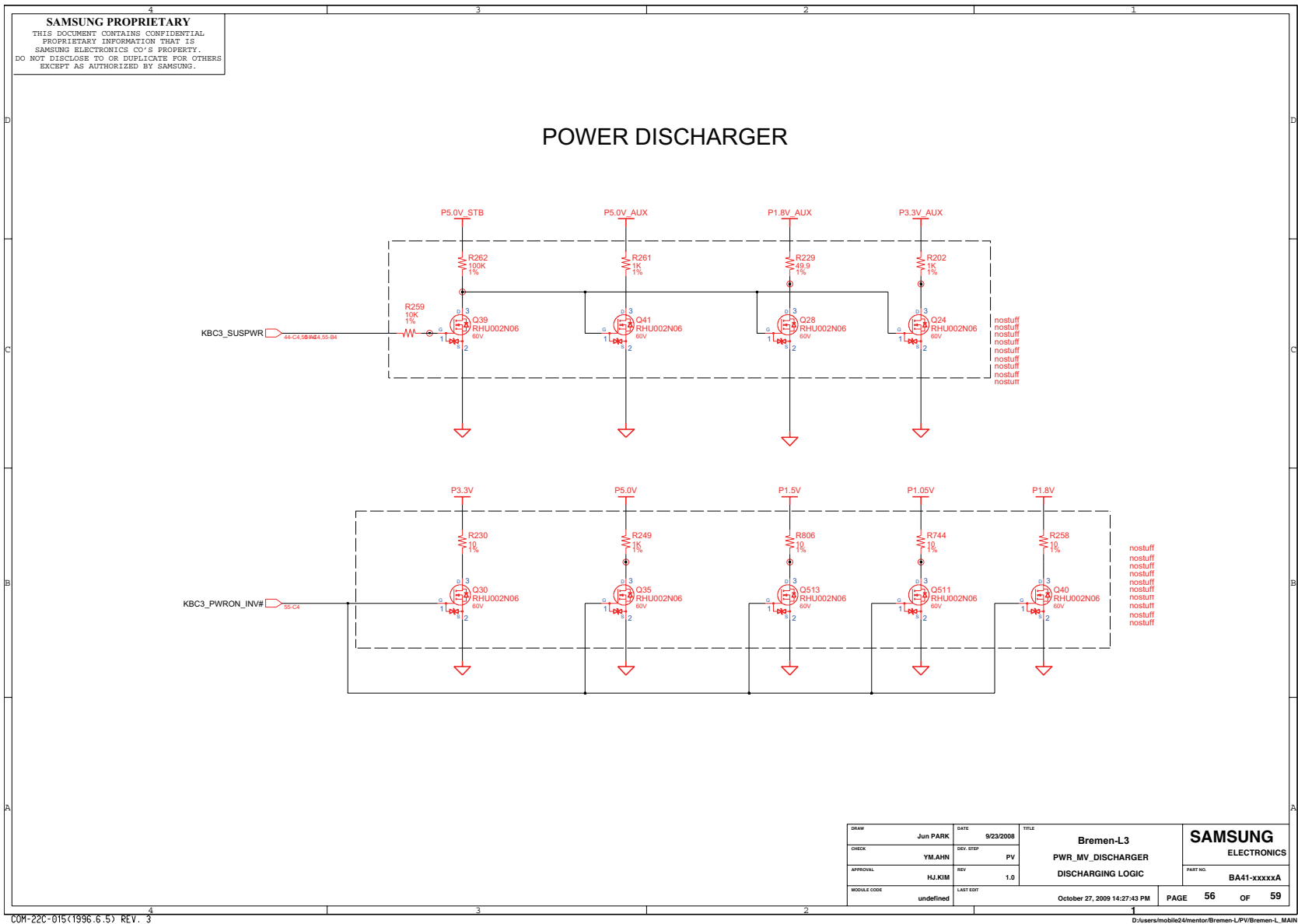
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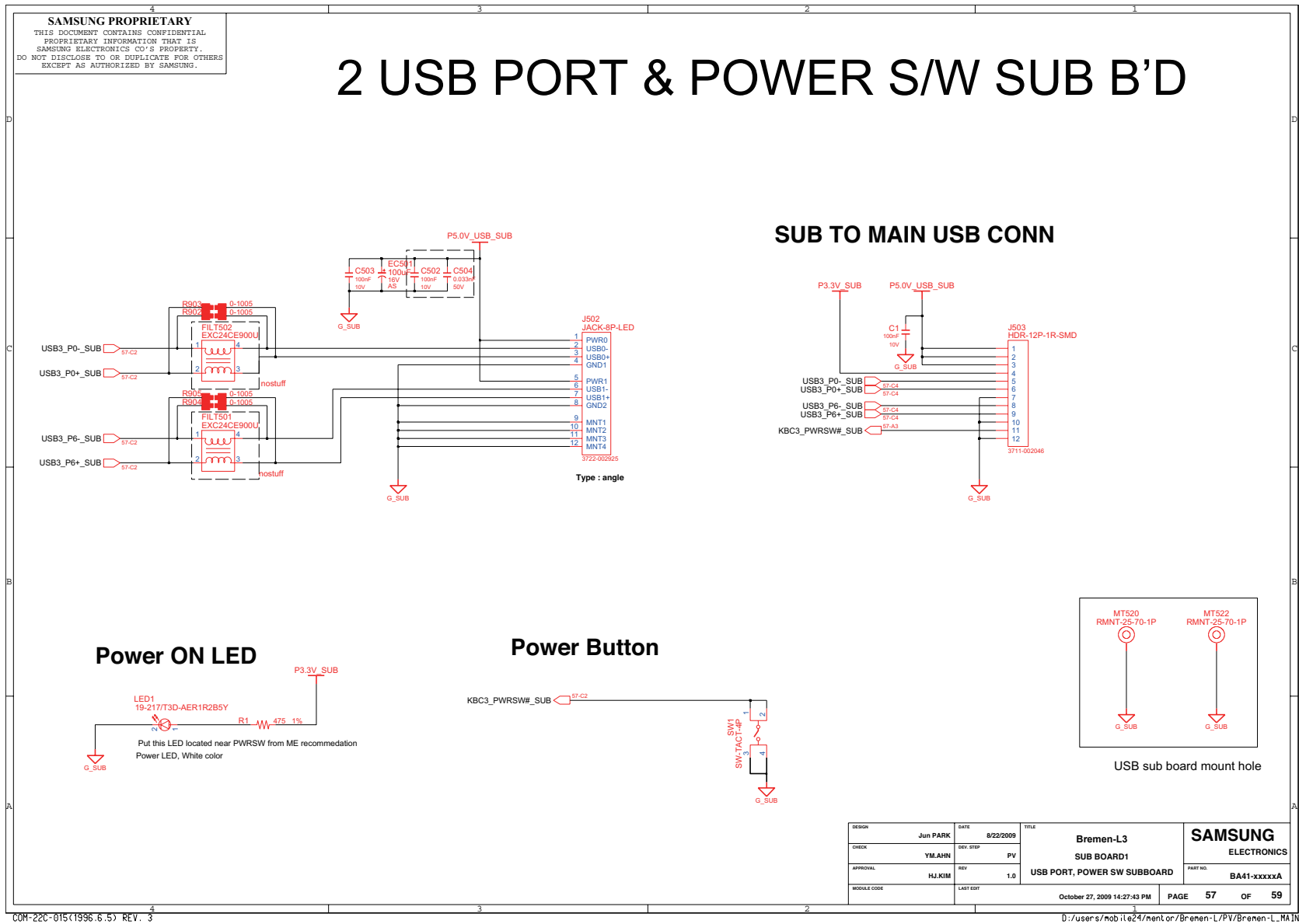
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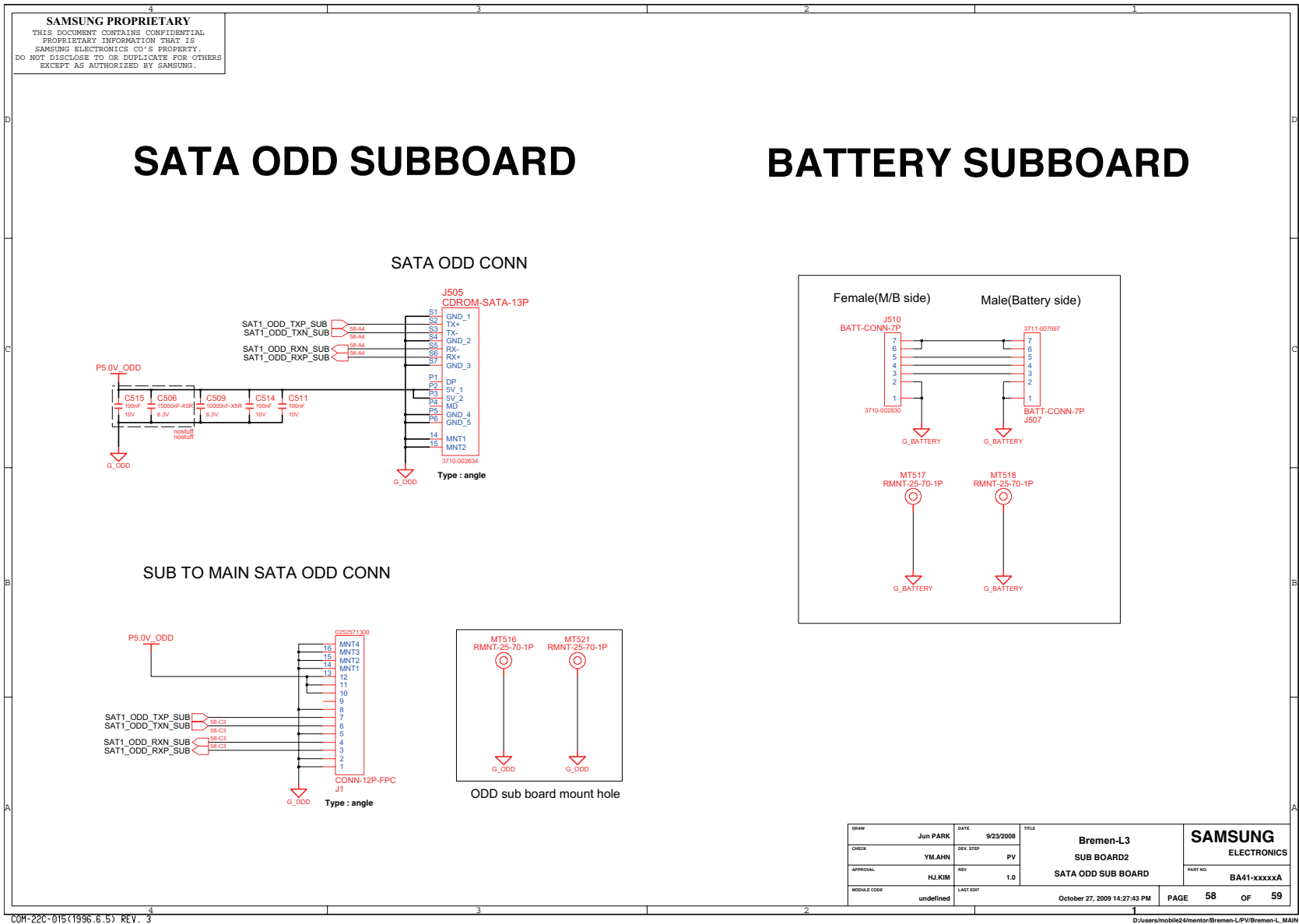




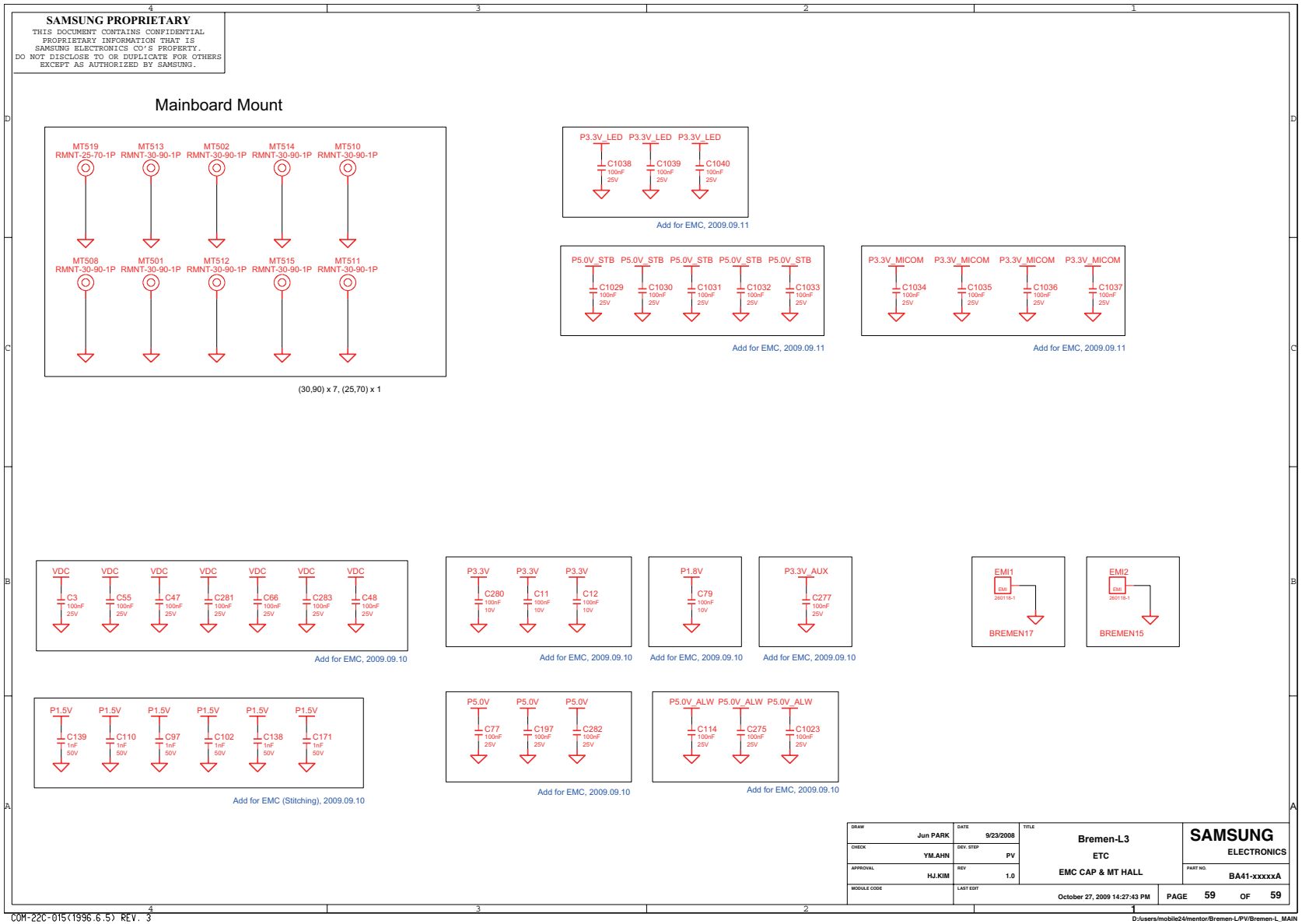
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