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# Jinmao

CPU : Arrandale PGA  
Chip Set : Intel Ibex Peak  
GFX : N12M / INT.GFX  
Remarks : Calpella Platform

Model Name : Jinmao  
PBA Name : MAIN  
PCB Code : BA41-01432A (GCE)  
BA41-01433A (NY)  
BA41-01434A (HAN)  
BA41-01435A (GBM)  
Dev. Step : PR  
Revision : 1.0  
T.R. Date : 2010.11.26

Design	CHECK	APPROVAL
MS YANG	MK KIM	BL LEE

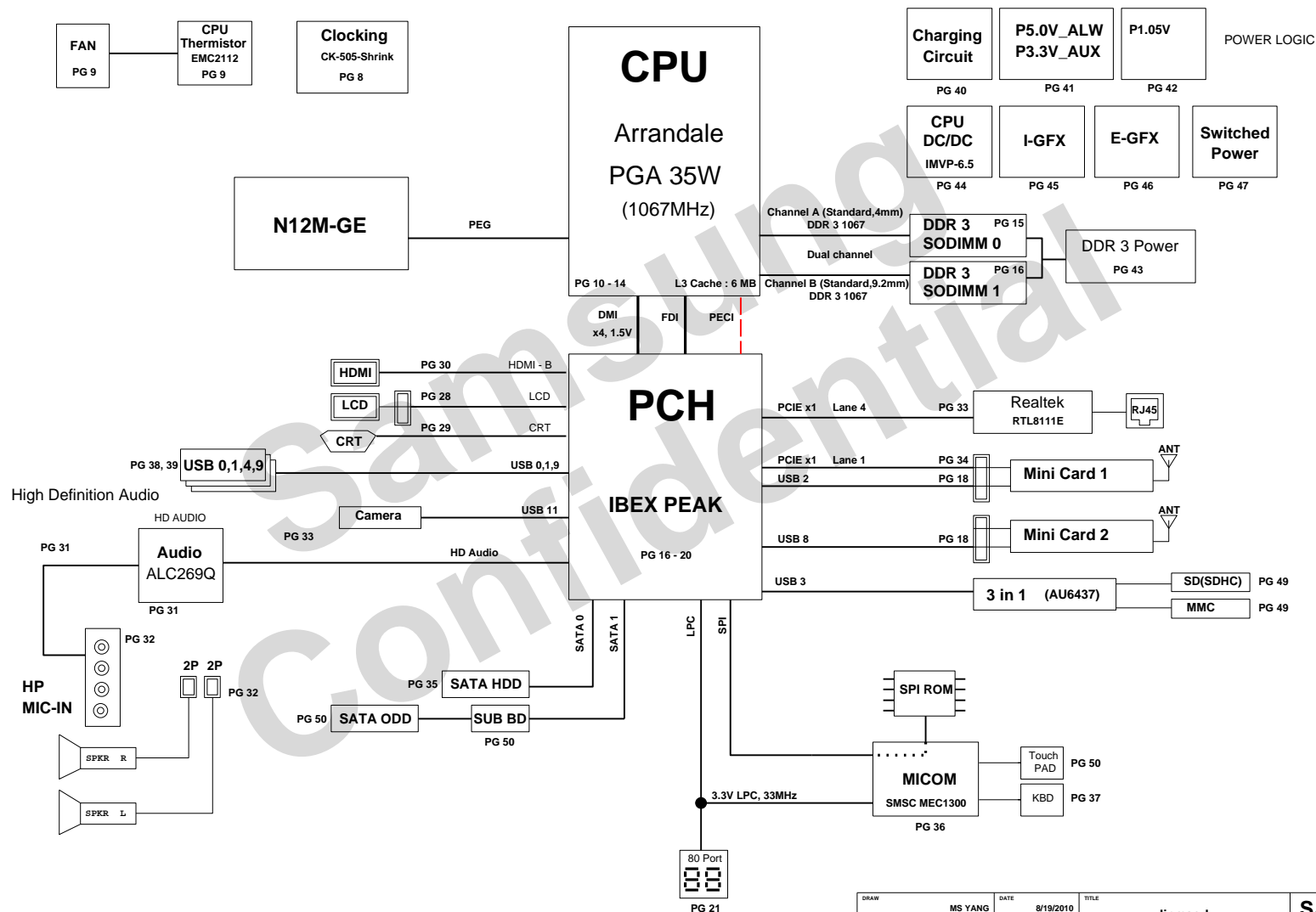
Owner : SEC IT Solution N/P LAB Signature : mansu

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sheet52 : Power - Switched Power 2

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	COVER	PART NO.	BA41-01432A
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	1	OF 52

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# BLOCK DIAGRAM



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
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## BOARD INFORMATION

### SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails		Active in
VDC P12.0V_ALW P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 12.0V always power rail 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail	S4 - S5
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)	
P5.0V P3.3V P1.8V P1.5V P1.05V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 1.05V power rail for chipset (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)	
VCC_CORE IGFX_CORE EGFX_CORE P1.05V (VCCP)	Core Voltage for CPU Core Voltage for IGFX Core Voltage for GPU VCC for Arrandale & IBEX Peak	

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express	3	NC
3	Multi Memory Card Controller	4	LAN CONTROLLER
4	NC	5	NC
5	NC	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	NC		
9	SYSTEM PORT 2 (SUB BOARD)		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	
5	

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

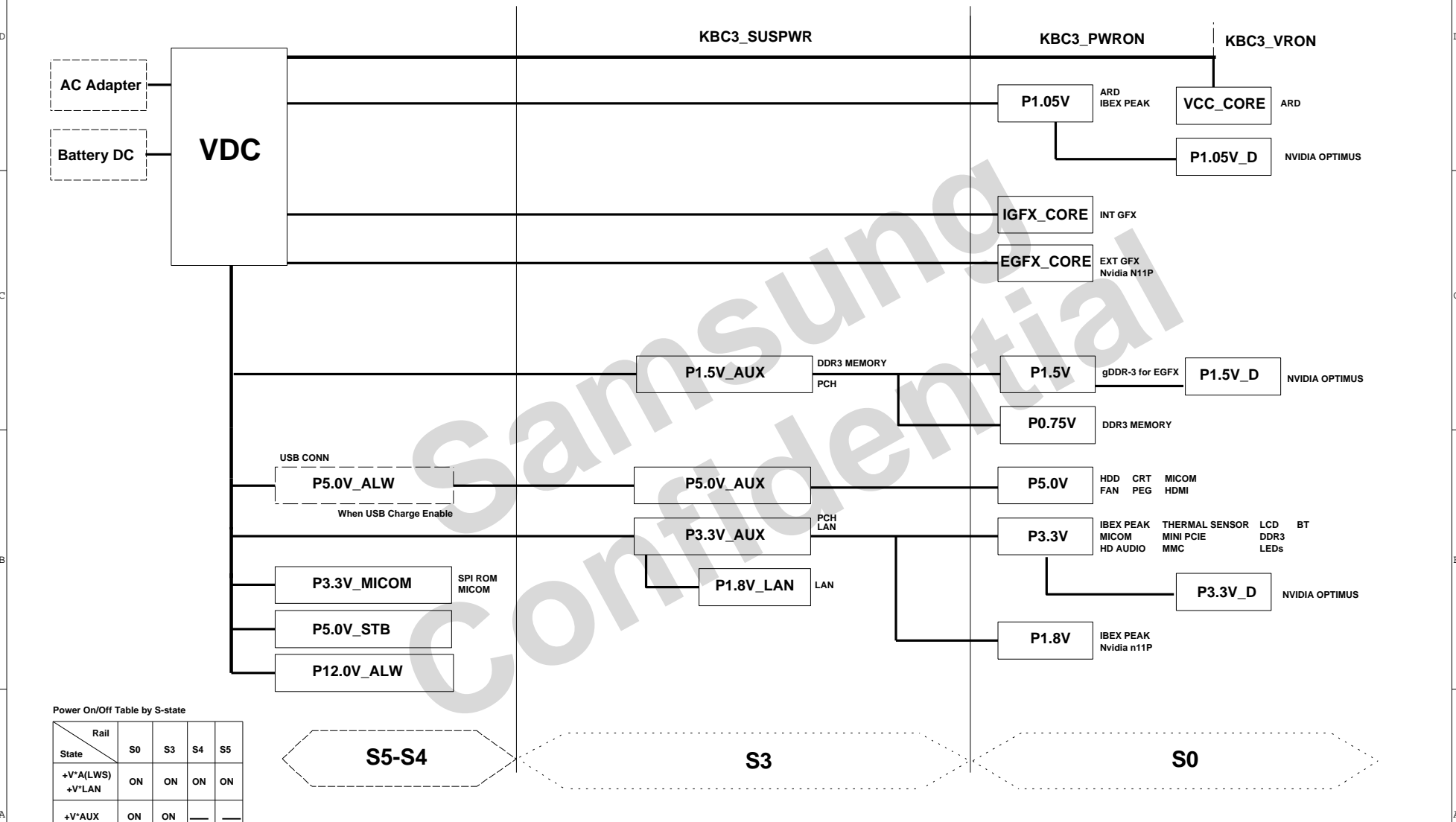
LCD Pannel Detect		
Devices	Resolution	PANNEL_DETECT_0
LTN140AT17	HD(1366x768)	SEC3250

I <sup>2</sup> C / SMB Address			
Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	
SODIMM0	1010 000x	A0h	Thermal Sensor
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L MAIN BOARD INFO	SAMSUNG ELECTRONICS PART NO. BA41-01432A
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APPROVAL	BL LEE	REV	rev. 1.0			
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# POWER DIAGRAM



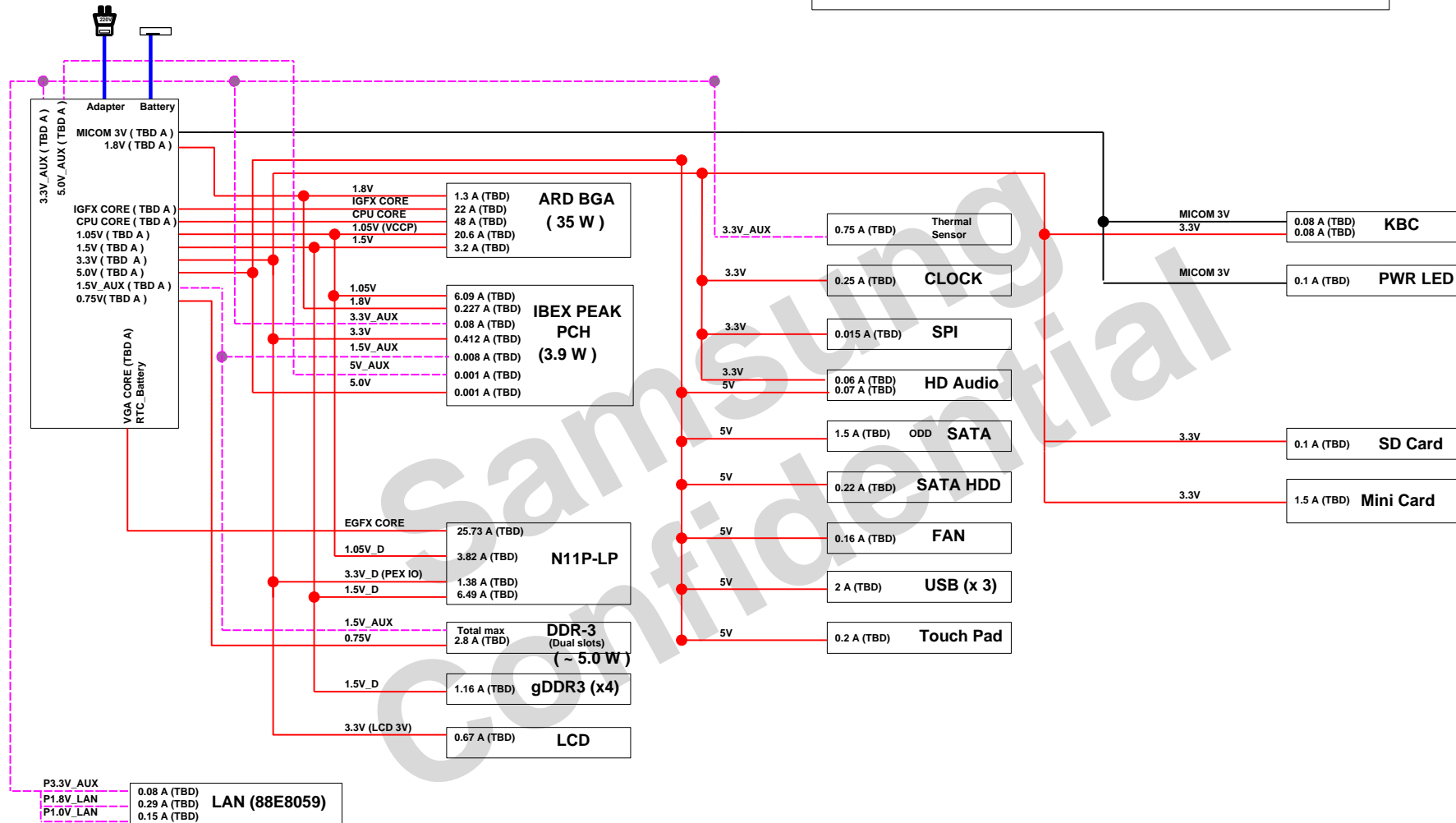
Power On/Off Table by S-state

Rail	S0	S3	S4	S5
+V*A(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	ON	ON
+V*AUX	ON	ON	ON	ON
+V	ON	ON	ON	ON
+V* (CORE)	ON	ON	ON	ON

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
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## POWER RAILS ANALYSIS

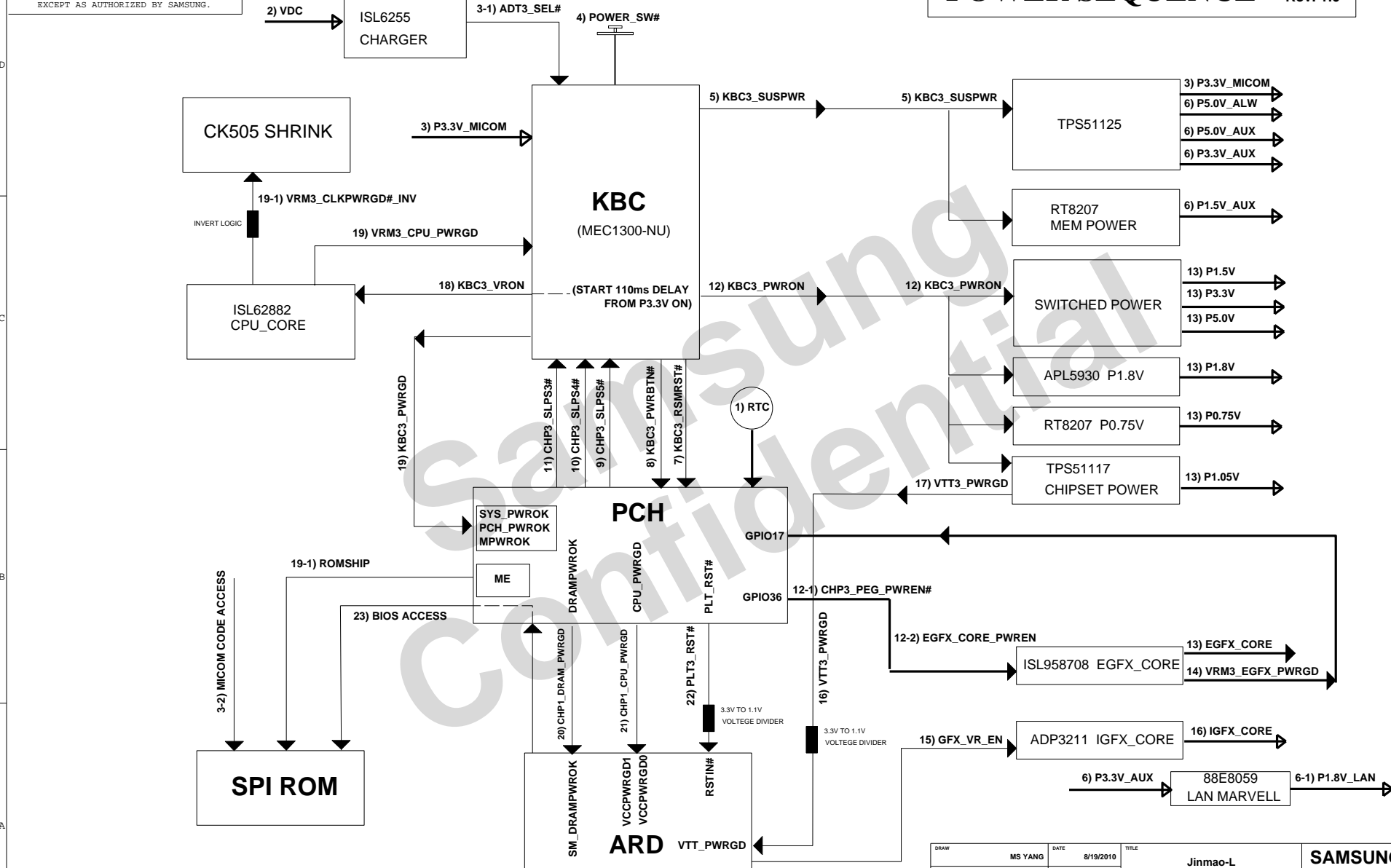


DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
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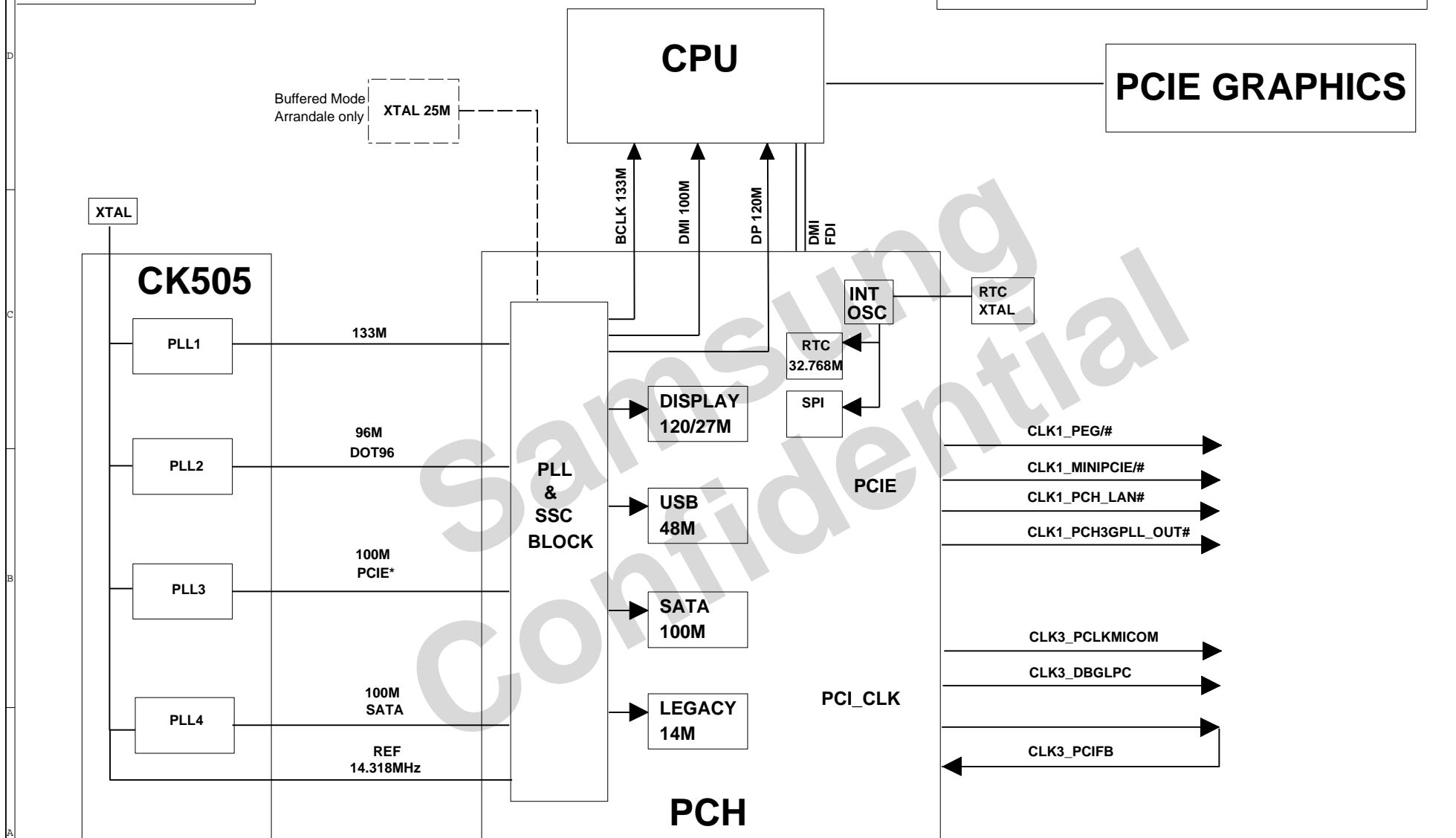
# POWER SEQUENCE

Rev. 1.0



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	6	OF 52

## Rev. 1.0



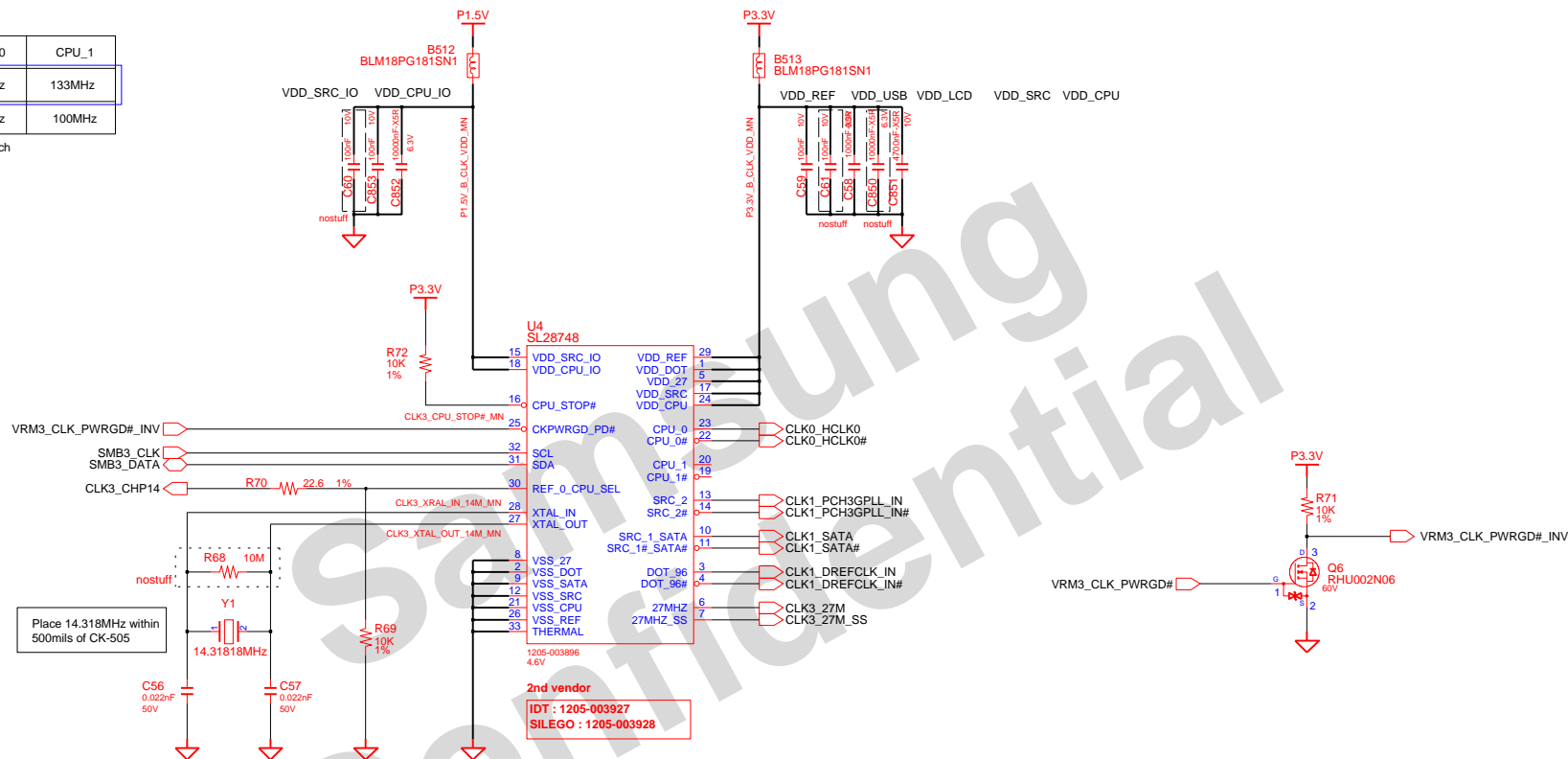
DRAW	MS YANG	DATE	8/19/2010	Jinmao-L MAIN CLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM		
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## CPU\_MODE\_SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

\*CPU SEL During CK PWRGD Latch




DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L CLOCK CK505-SHRINK	SAMSUNG ELECTRONICS		
CHECK	MK KIM	DEV. STEP	PR				
APPROVAL	BL LEE	REV	rev. 1.0			PART NO.	BA41-01432A
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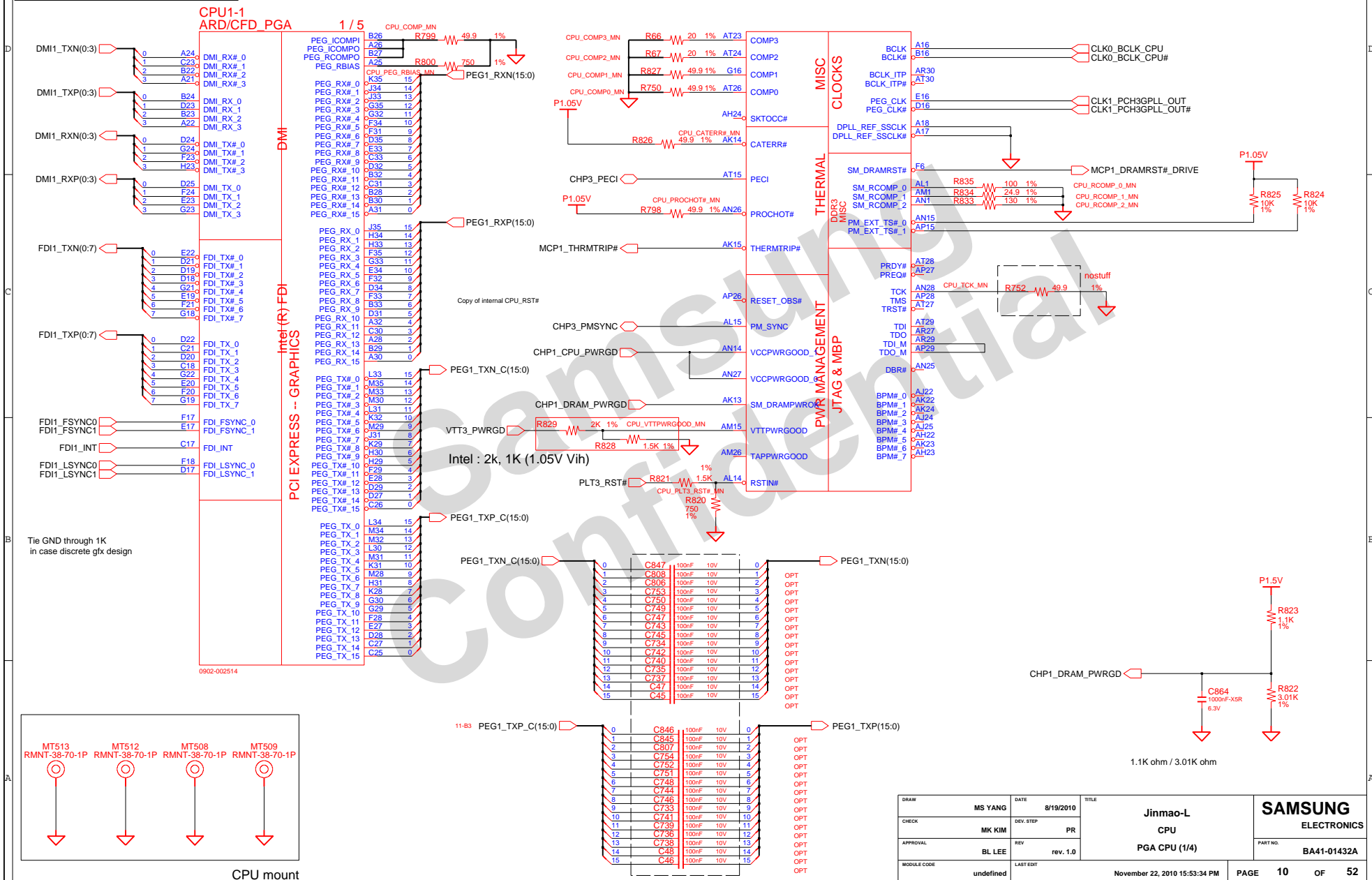
ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

SHDN_SEL MODE	
0 HIGH Z	INTEL TR MODE AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

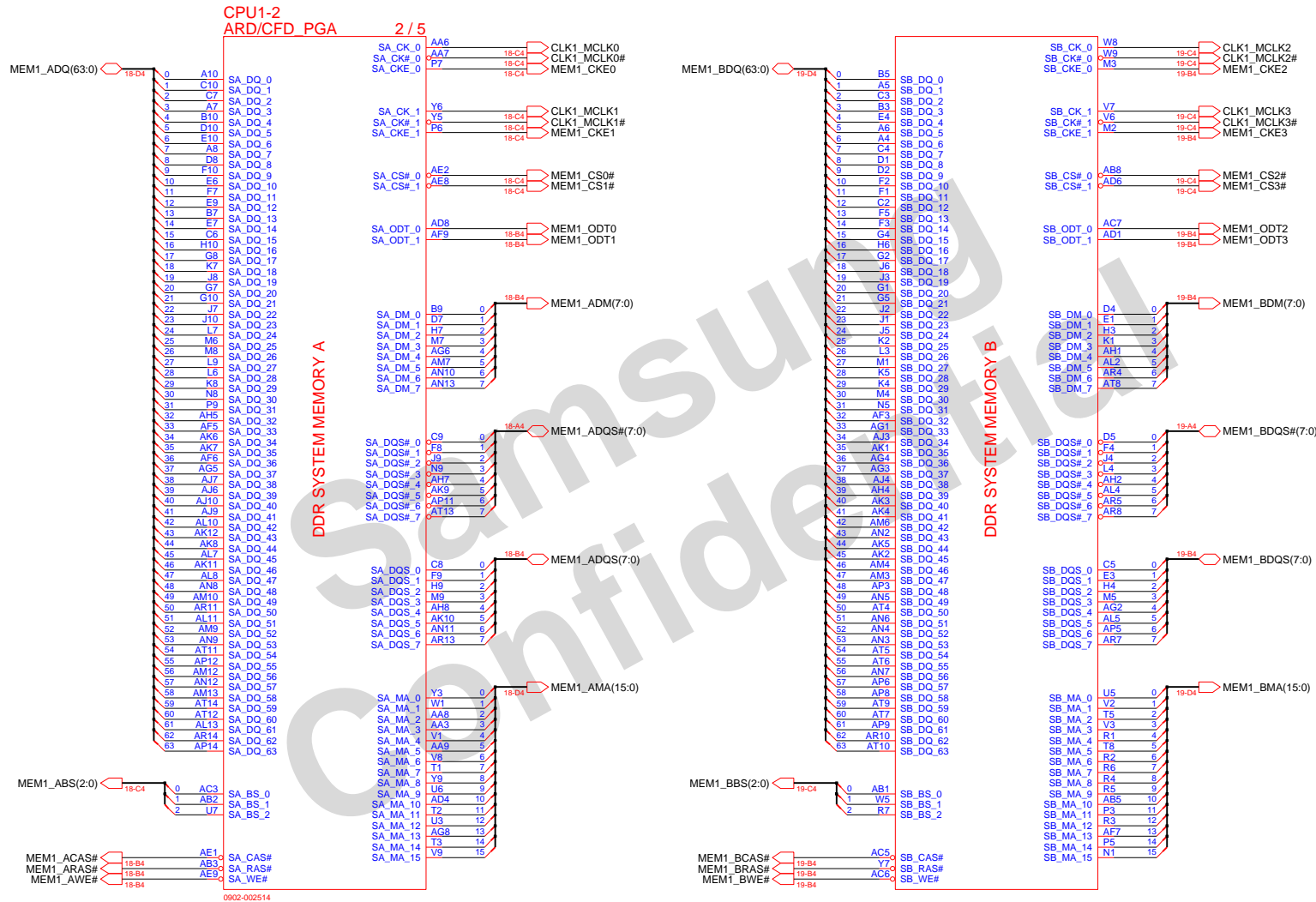
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L		
CHECK	MK KIM	DEV. STEP	PR	THERMAL SENSOR			
APPROVAL	BL LEE	REV	rev. 1.0	THERMAL SENSOR EMC2112		PART NO.	BA41-01432A
MODULE CODE	LAST EDIT		November 22, 2010 15:53:34 PM			PAGE	9 OF 52

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## ARRANDALE PROCESSOR (DMI,PEG, FDI)

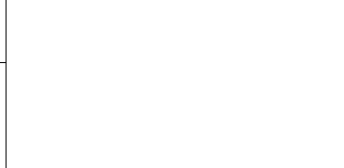
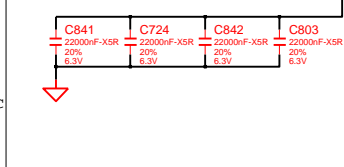
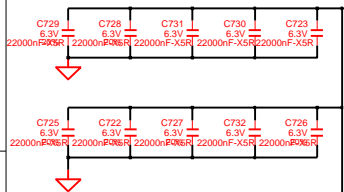


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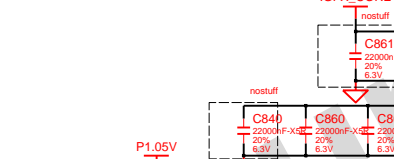
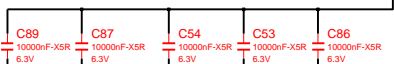
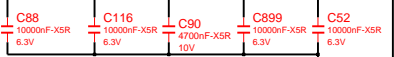
0902-002514

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L CPU	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01432A
CHECK	MK KIM	DEV. STEP	PR			
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM			
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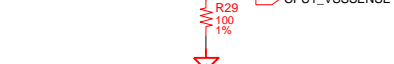
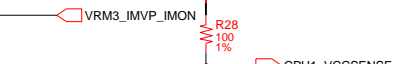
AG35	VC01
AG34	VC02
AG33	VC03
AG32	VC04
AG31	VC05
AG30	VC06
AG29	VC07
AG28	VC08
AG27	VC09
AG26	VC10
AF35	VC11
AF34	VC12
AF33	VC13
AF32	VC14
AF31	VC15
AF30	VC16
AF29	VC17
AF28	VC18
AF27	VC19
AD35	VC20
AD34	VC21
AD33	VC22
AD32	VC23
AD31	VC24
AD30	VC25
AD29	VC26
AD28	VC27
AD27	VC28
AC35	VC29
AC34	VC30
AC33	VC31
AC32	VC32
AC31	VC33
AC30	VC34
AC29	VC35
AC28	VC36
AC27	VC37
AC26	VC38
AC25	VC39
AC24	VC40
AC23	VC41
AC22	VC42
AC21	VC43
AC20	VC44
AC19	VC45
AC18	VC46
AC17	VC47
AC16	VC48
AC15	VC49
AC14	VC50
AC13	VC51
AC12	VC52
Y35	VC53
Y34	VC54
Y33	VC55
Y32	VC56
Y31	VC57
Y30	VC58
Y29	VC59
Y28	VC60
Y27	VC61
Y26	VC62
Y25	VC63
Y24	VC64
Y23	VC65
Y22	VC66
Y21	VC67
Y20	VC68
Y19	VC69
Y18	VC70
Y17	VC71
Y16	VC72
Y15	VC73
Y14	VC74
Y13	VC75
Y12	VC76
Y11	VC77
Y10	VC78
Y09	VC79
Y08	VC80
Y07	VC81
Y06	VC82
Y05	VC83
Y04	VC84
Y03	VC85
Y02	VC86
Y01	VC87
R35	VC88
R34	VC89
R33	VC90
R32	VC91
R31	VC92
R30	VC93
R29	VC94
R28	VC95
R27	VC96
R26	VC97
R25	VC98
R24	VC99
R23	VC100

3/5	
VT1	AH14
VT2	AH12
VT3	AH11
VT4	AH10
VT5	J14
VT6	J13
VT7	H14
VT8	H12
VT9	G14
VT10	G13
VT11	G12
VT12	F11
VT13	F14
VT14	F13
VT15	F12
VT16	F11
VT17	E14
VT18	E12
VT19	D14
VT20	D13
VT21	D12
VT22	D11
VT23	C14
VT24	C13
VT25	C12
VT26	C11
VT27	B14
VT28	B12
VT29	B11
VT30	A13
VT31	A12
	A11

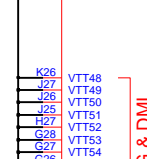
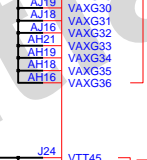
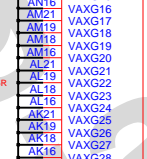
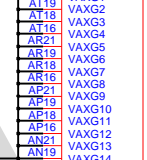
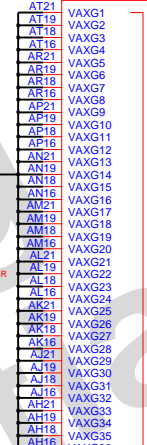


VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD


VTT\_SEL signal (for CFD/ARD shared) CPU\_CORE



VTT_SEL	VOLTAGE	CPU
<b>1</b>	<b>P1.05V</b>	<b>ARRANDALE</b>
0	P1.1V	CLARKS FIELD



	1uF	10uF	22uF	330uF
<b>w Proddizer</b>	25 pcs	0 pcs	16 pcs	0 pcs
<b>w/o Proddizer</b>	25 pcs	16 pcs	12 pcs	4 pcs

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L CPU PGA CPU (3/4)	
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
					PART NO.
					BA41-0143
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE 12 OF

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CPU1-5  
ARD/CFD\_PG5/5

AT20	VSS1	VSS81	AE34
AT17	VSS2	VSS82	AE33
AR3	VSS3	VSS83	AE32
AR28	VSS4	VSS84	AE31
AR26	VSS5	VSS85	AE30
AR24	VSS6	VSS86	AE29
AR23	VSS7	VSS87	AE28
AR20	VSS8	VSS88	AE27
AR17	VSS9	VSS89	AE26
AR15	VSS10	VSS90	AE6
AR12	VSS11	VSS91	AD10
AR9	VSS12	VSS92	AC9
AR6	VSS13	VSS93	AC2
AR3	VSS14	VSS94	AC1
AP20	VSS15	VSS95	AB35
AP17	VSS16	VSS96	AB34
AP13	VSS17	VSS97	AB33
AP10	VSS18	VSS98	AB32
AP7	VSS19	VSS99	AB31
AP4	VSS20	VSS100	AB30
AP2	VSS21	VSS101	AB29
AN34	VSS22	VSS102	AB28
AN31	VSS23	VSS103	AB27
AN23	VSS24	VSS104	AB26
AN20	VSS25	VSS105	AB25
AN17	VSS26	VSS106	AB24
AM29	VSS27	VSS107	AB23
AM27	VSS28	VSS108	AB22
AM25	VSS29	VSS109	AB21
AM20	VSS30	VSS110	AB20
AM17	VSS31	VSS111	AB19
AM14	VSS32	VSS112	AB18
AM11	VSS33	VSS113	AB17
AM8	VSS34	VSS114	AB16
AM5	VSS35	VSS115	AB15
AM2	VSS36	VSS116	AB14
AL34	VSS37	VSS117	AB13
AL31	VSS38	VSS118	AB12
AL23	VSS39	VSS119	AB11
AL20	VSS40	VSS120	AB10
AL17	VSS41	VSS121	AB9
AL12	VSS42	VSS122	AB8
AL9	VSS43	VSS123	AB7
AL6	VSS44	VSS124	AB6
AL3	VSS45	VSS125	AB5
AK29	VSS46	VSS126	AB4
AK27	VSS47	VSS127	AB3
AK25	VSS48	VSS128	AB2
AK20	VSS49	VSS129	AB1
AK17	VSS50	VSS130	AB0
AK13	VSS51	VSS131	AB0
AK10	VSS52	VSS132	AB0
AK7	VSS53	VSS133	AB0
AK4	VSS54	VSS134	AB0
AK1	VSS55	VSS135	AB0
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AK0	VSS79	VSS159	AB0
AK0	VSS80	VSS160	AB0

K27	VSS161	AE34
K9	VSS162	AE33
K6	VSS163	AE32
K3	VSS164	AE31
J32	VSS165	AE30
J30	VSS166	AE29
J21	VSS167	AE28
J19	VSS168	AE27
H35	VSS169	AE26
H32	VSS170	AE6
H28	VSS171	AD10
H26	VSS172	AC9
H24	VSS173	AC2
H22	VSS174	AC1
H18	VSS175	AB35
H15	VSS176	AB34
H13	VSS177	AB33
H11	VSS178	AB32
H8	VSS179	AB31
H5	VSS180	AB30
H2	VSS181	AB29
G34	VSS182	AB28
G31	VSS183	AB27
G20	VSS184	AB26
G9	VSS185	AB25
G6	VSS186	AB24
G3	VSS187	AB23
F30	VSS188	AB22
F27	VSS189	AB21
F25	VSS190	AB20
F22	VSS191	AB19
F19	VSS192	AB18
F16	VSS193	AB17
E32	VSS194	AB16
E35	VSS195	AB15
E29	VSS196	AB14
E24	VSS197	AB13
E21	VSS198	AB12
E18	VSS199	AB11
E13	VSS200	AB10
E11	VSS201	AB9
E8	VSS202	AB8
E5	VSS203	AB7
E2	VSS204	AB6
D33	VSS205	AB5
D30	VSS206	AB4
D26	VSS207	AB3
D9	VSS208	AB2
D6	VSS209	AB1
D3	VSS210	AB0
C34	VSS211	AB0
C32	VSS212	AB0
C29	VSS213	AB0
C28	VSS214	AB0
C24	VSS215	AB0
C22	VSS216	AB0
C19	VSS217	AB0
C16	VSS218	AB0
B31	VSS219	AB0
B25	VSS220	AB0
B21	VSS221	AB0
B18	VSS222	AB0
B17	VSS223	AB0
B13	VSS224	AB0
B11	VSS225	AB0
B8	VSS226	AB0
B6	VSS227	AB0
B4	VSS228	AB0
A29	VSS229	AB0
A27	VSS230	AB0
A23	VSS231	AB0
A9	VSS232	AB0
	VSS233	AB0

NCTF  
-VSS\_NCTF1  
AT35  
AT1  
AR34  
B34  
B2  
B1  
A35  
-VSS\_NCTF7

AP25	RSVD1	RSVD32	AJ13
AL25	RSVD2	RSVD33	AJ12
AL24	RSVD3	RSVD34	AH25
AL22	RSVD4	RSVD35	AK26
AJ33	RSVD5	RSVD36	AL26
AG9	RSVD6	RSVD_NCTF_37	AR2
M27	RSVD7	RSVD38	AJ26
L28	RSVD8	RSVD39	AJ27
H17	SA_DIMM_VREFDQ		
H17	SB_DIMM_VREFDQ		
G25	RSVD11		
G17	RSVD12	RSVD_NCTF_40	AP1
E31	RSVD13	RSVD_NCTF_41	AT2
E30	RSVD14	RSVD_NCTF_42	AT3
		RSVD_NCTF_43	AR1
AM30	CFG_0	RSVD45	AL28
AM28	CFG_1	RSVD46	AL29
AP31	CFG_2	RSVD47	AP30
AL32	CFG_3	RSVD48	AP32
AL30	CFG_4	RSVD49	AL27
AM31	CFG_5	RSVD50	AT31
AM29	CFG_6	RSVD51	AP33
AM32	CFG_7	RSVD52	AR33
AK32	CFG_8	RSVD53	AT33
AK31	CFG_9	RSVD_NCTF_54	AT34
AK28	CFG_10	RSVD_NCTF_55	AP35
AJ28	CFG_11	RSVD_NCTF_56	AR35
AN30	CFG_12	RSVD_NCTF_57	AR32
AN32	CFG_13	RSVD58	
AJ32	CFG_14		
AJ29	CFG_15	RSVD_TP_59	E15
AJ30	CFG_16	RSVD_TP_60	F15
AK30	CFG_17	KEY	A2
H16	RSVD_TP_86	RSVD82	D15
		RSVD83	C15
		RSVD84	AJ15
		RSVD85	AH15
B19	RSVD15		
A19	RSVD16		
A20	RSVD17		
B20	RSVD18		
U9	RSVD19	RSVD_TP_66	AA5
T9	RSVD20	RSVD_TP_67	AA4
AC9	RSVD21	RSVD_TP_68	R8
AB9	RSVD22	RSVD_TP_69	AD3
		RSVD_TP_70	AD2
		RSVD_TP_71	AA2
		RSVD_TP_72	AA1
		RSVD_TP_73	R9
		RSVD_TP_74	AG7
		RSVD_TP_75	AE3
C1	RSVD_NCTF_23		
A3	RSVD_NCTF_24		
		RSVD_TP_76	V4
		RSVD_TP_77	V5
		RSVD_TP_78	N2
		RSVD_TP_79	AD5
		RSVD_TP_80	AD7
		RSVD_TP_81	W3
		RSVD_TP_82	W2
		RSVD_TP_83	N3
		RSVD_TP_84	AE5
		RSVD_TP_85	AD9
J29	RSVD26		
J28	RSVD27		
A34	RSVD_NCTF_28		
A33	RSVD_NCTF_29		
C35	RSVD_NCTF_30		
B35	RSVD_NCTF_31		

(VSS) RSVD86

CRB is NC  
EDS/DG is GND recommend

Clarksfield : SA\_DIMM\_VRREFDQ, 100K PD  
SB\_DIMM\_VRREFDQ, 100K PD  
Arrandale : SA\_DIMM\_VRREFDQ, NC  
SB\_DIMM\_VRREFDQ, NC

## CFG Straps for Processor

PCI Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifunction enabled

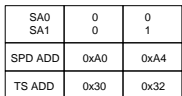
PCI Express Static Lane Reversal	
CFG3	1 : Normal operation 0 : Lane Reversed

Display Port Presence	
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP

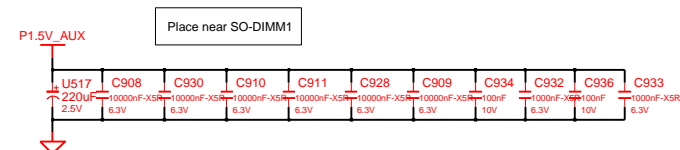
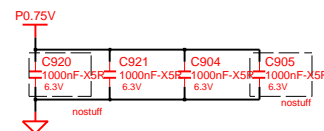
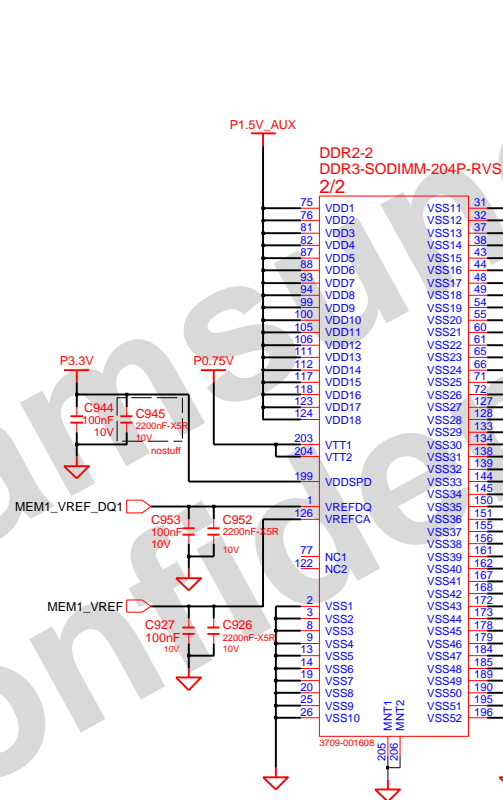
PCIe 2.0 SUPPORT	
CFG7	1 : Normal operation 0 : PCIe2.0 Jitter support

DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		CPU	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		PGA CPU (4/4)	PART NO.
MODULE CODE		LAST EDIT				BA41-01432A
November 22, 2010 15:53:34 PM						PAGE 13 OF 52

P/N : 3709-001609 (CONCRAFT)

D:/users/mobile39/mentor/Jinmac-L/Main/PR/Jinmac-L MAIN

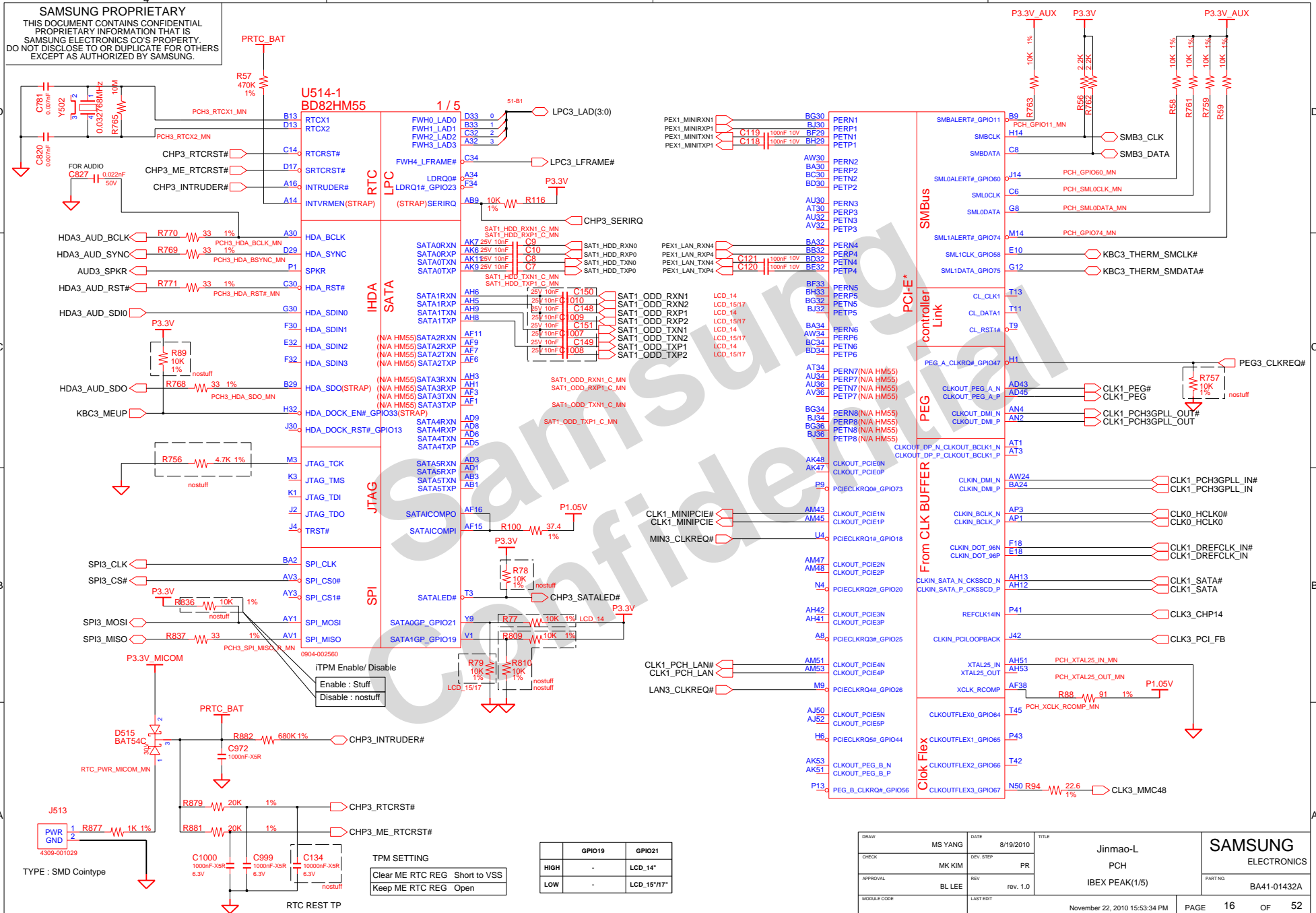
**DDR SO-DIMM #1**  
Height : 4 mm (REVERSE)

[illegible]

DRAW	MS YANG	DATE	8/19/2010	TITLE  Jinmao-L SODIMM B DDR3	<b>SAMSUNG</b> ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE	LAST EDIT				
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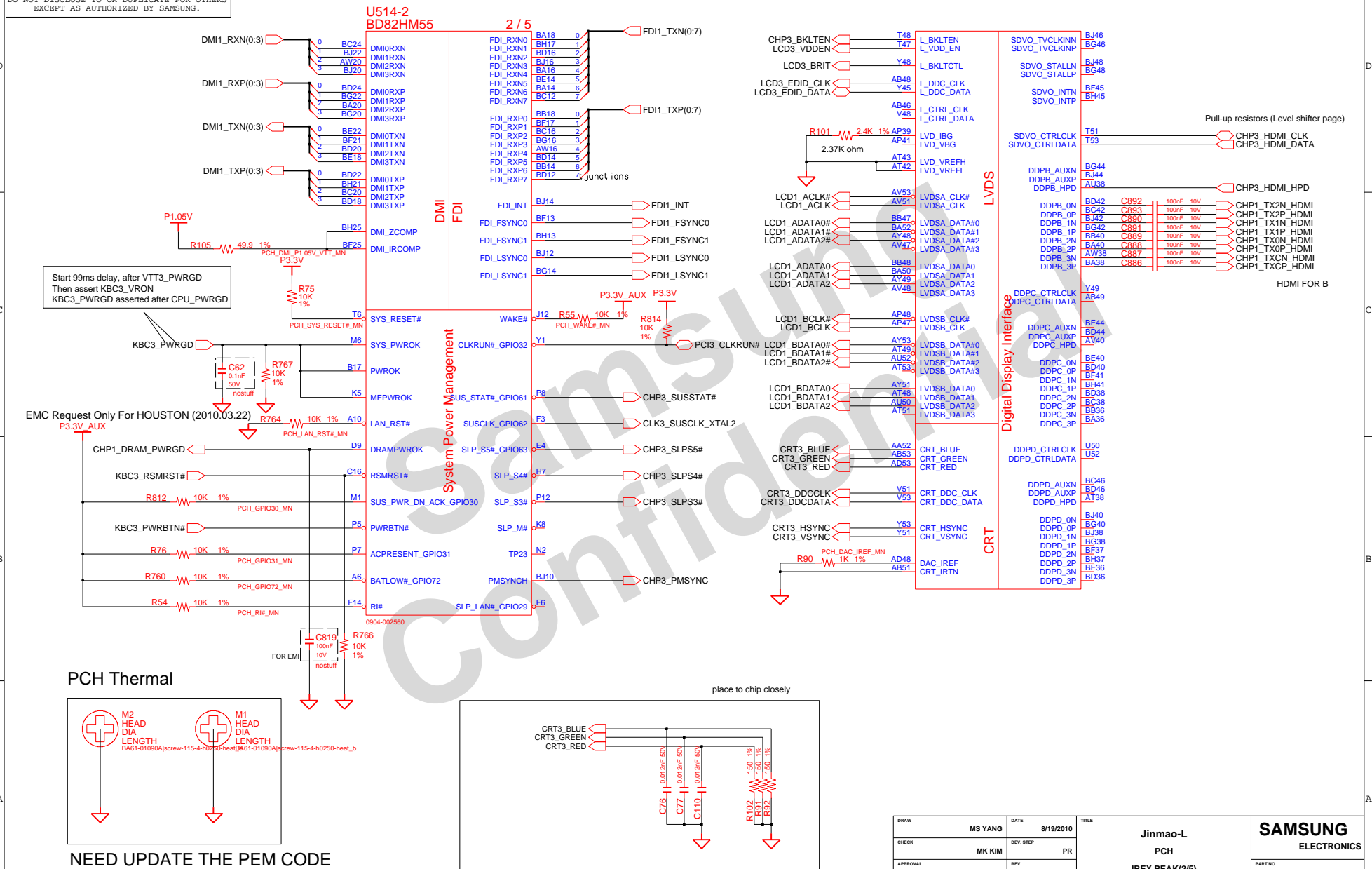


	GPIO19	GPIO21
HIGH	-	LCD_14"
LOW	-	LCD_15"/17"

DRAWN	MS YANG	DATE	8/19/2010	<div style="text-align: center;"> <b>Jinmao-L</b>  <b>PCH</b>  <b>IBEX PEAK(1/5)</b> </div>	<div style="text-align: center;"> <b>SAMSUNG</b>  <b>ELECTRONICS</b> </div>	
CHECK	MK KIM	DEV. STEP	PR			
APPROVAL	BL LEE	REV	rev. 1.0		PART NO.	BA41-01432A
MODULE CODE	LAST EDIT				<div style="text-align: center;"> November 22, 2010 15:53:34 PM </div>	<div style="display: flex; justify-content: space-between;"> PAGE 16 OF 52 </div>

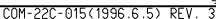


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DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		PCH	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		IBEX PEAK(2/5)	PART NO.
MODULE CODE		LAST EDIT				BA41-01432A
				November 22, 2010 15:53:34 PM	PAGE	17 OF 52

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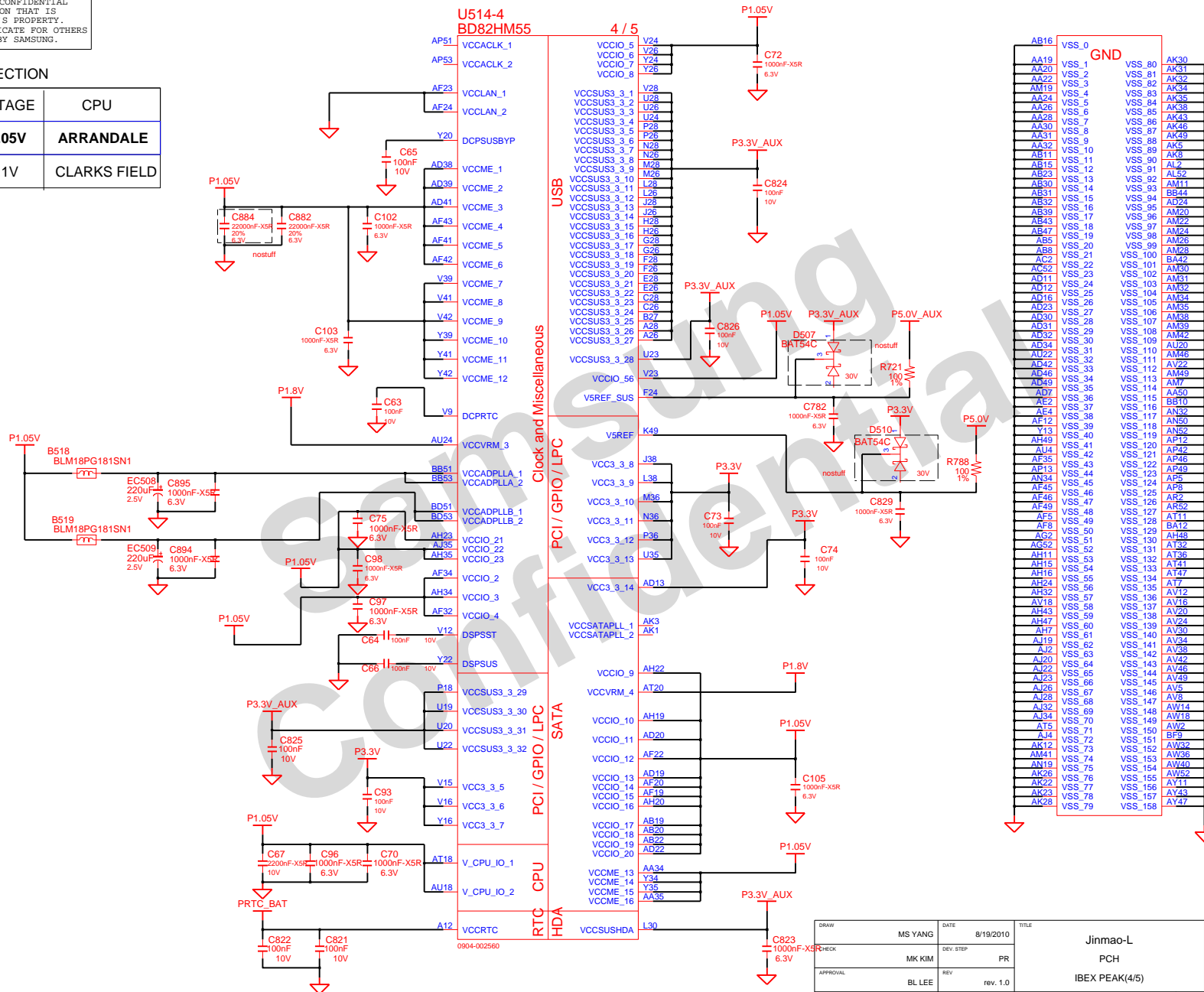


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## \*\*VTT POWER SELECTION

VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD



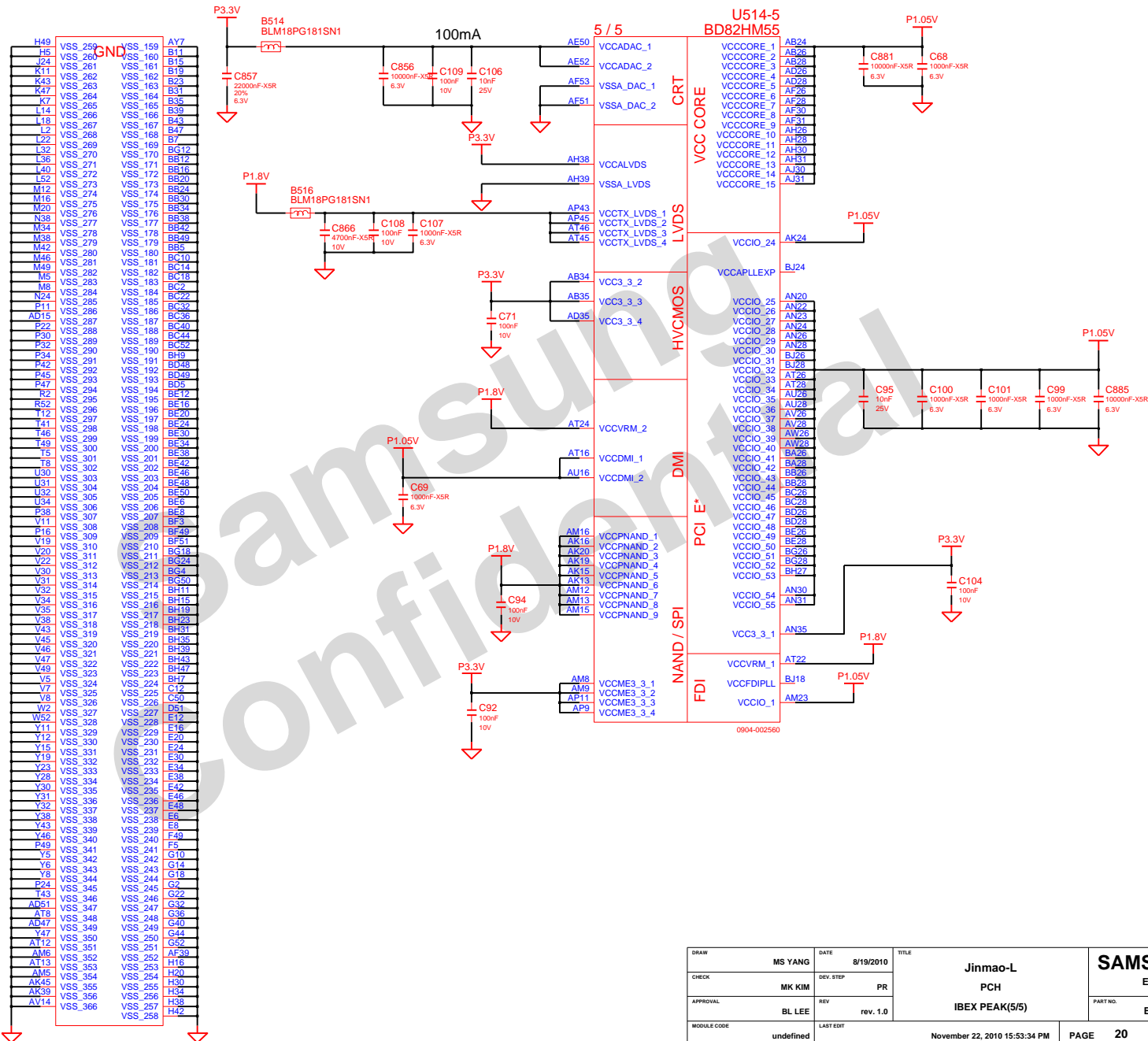
DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L
CHECK	MK KIM	DEV. STEP	PR		PCH
APPROVAL	BL LEE	REV	rev. 1.0		IBEX PEAK(4/5)
MODULE CODE	52	LAST EDIT			
November 22, 2010 15:53:34 PM					PAGE 19 OF 60

SAMSUNG  
 ELECTRONICS

PART NO. BA41-01432A

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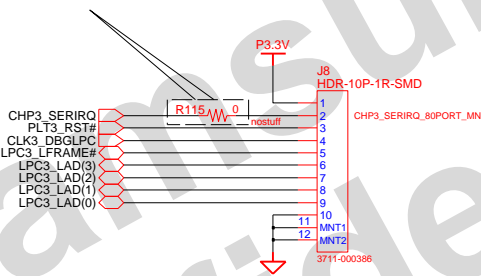
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DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		PCH	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		IBEX PEAK(5/5)	PART NO.
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM			BA41-01432A
					PAGE	20 OF 52

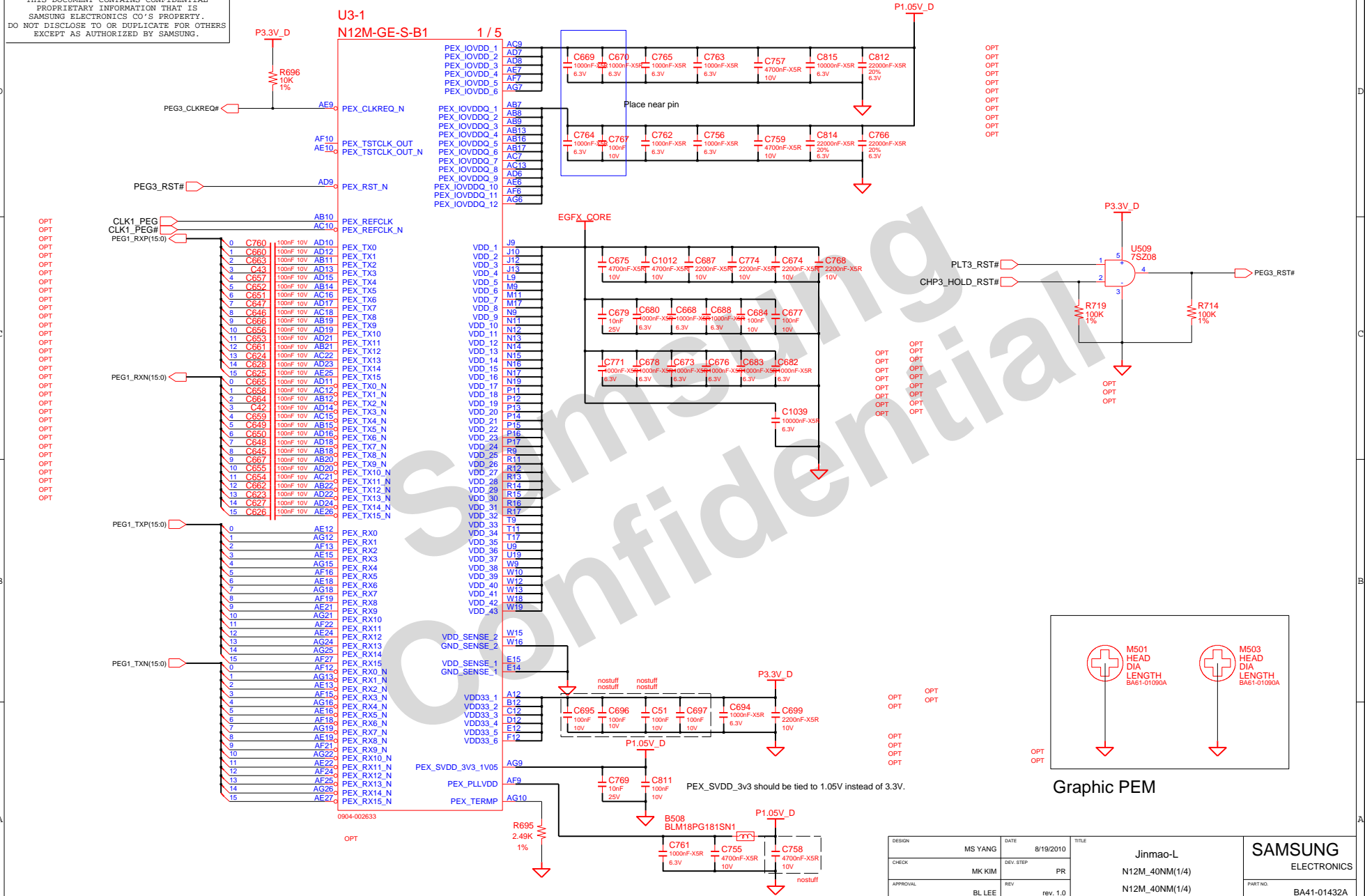
80H PORT DEBUG

For MICOM 80H Debug Port Test



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	DEBUG PORT		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	80H DECODER	PART NO.	BA41-01432A
MODULE CODE	LAST EDIT			November 22, 2010 15:53:34 PM	PAGE	21 OF 52

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DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		N12M_40NM(1/4)	
APPROVAL	BL LEE	REV	rev. 1.0		N12M_40NM(1/4)	
MODULE CODE		LAST EDIT				PART NO. BA41-01432A
November 22, 2010 15:53:34 PM						PAGE 22 OF 52

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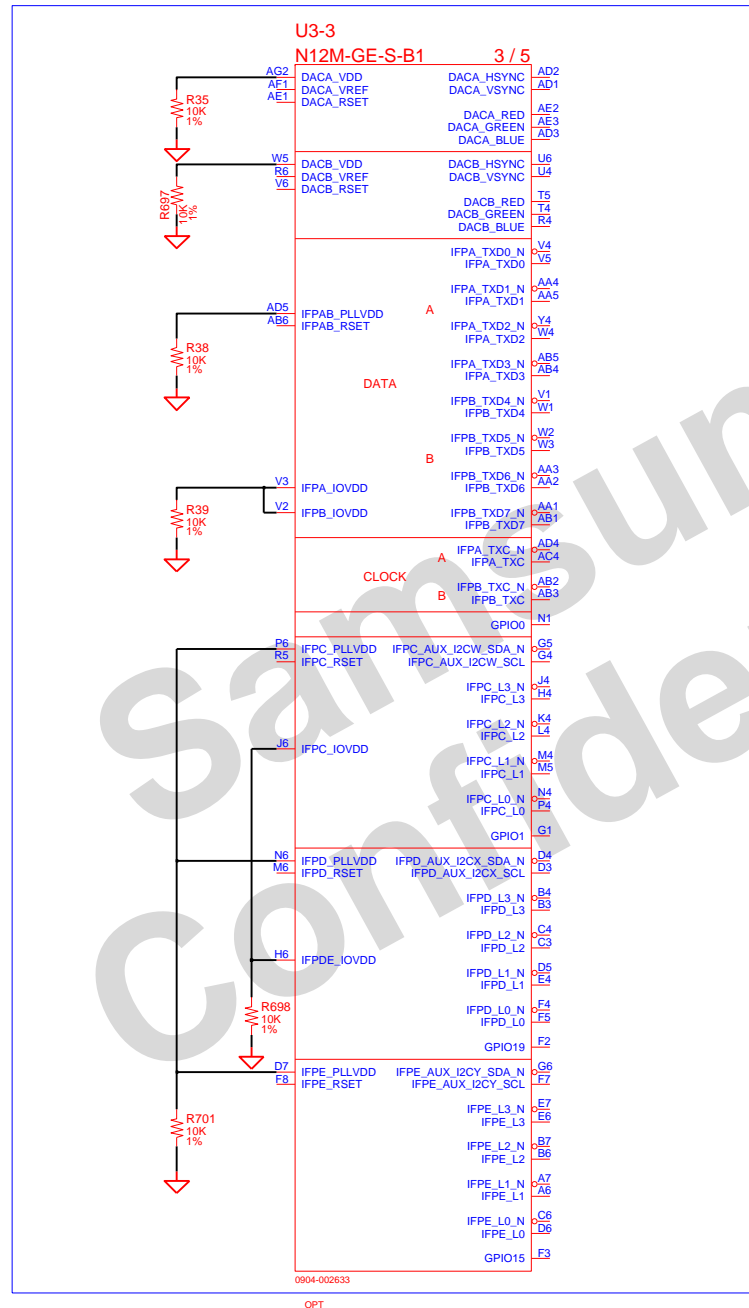
## CMD MODE A

OPT	OPT
OPT	OPT
OPT	OPT

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L N12M_40NM(2/4) N12M_40NM(2/4)	SAMSUNG ELECTRONICS			
CHECK	DRY STEP	PR						
APPROVAL	REV	REV. 1.0	PART NO.		BA41-01432A			
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE	23	OF



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DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		N12M_40NM(3/4)	
APPROVAL	BL LEE	REV	rev. 1.0		N12M_40NM(3/4)	
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	24	OF 52



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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCDD_BL_PWM	High
GPIO(3)	LCDD_VDD	High
GPIO(4)	LCDD_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V 10 0.95V
GPIO(6)	GPU VID1	01 0.85V 11 1.03V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

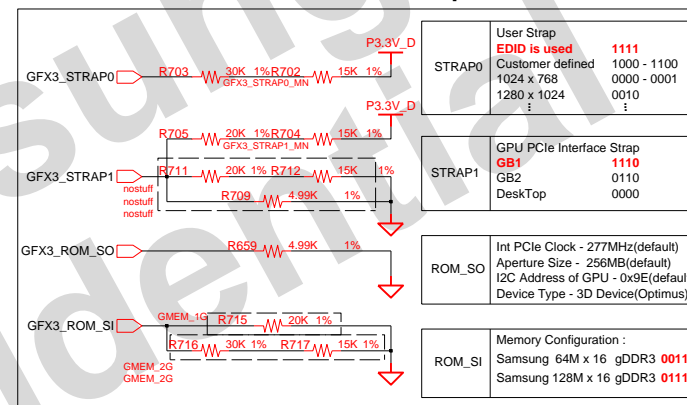
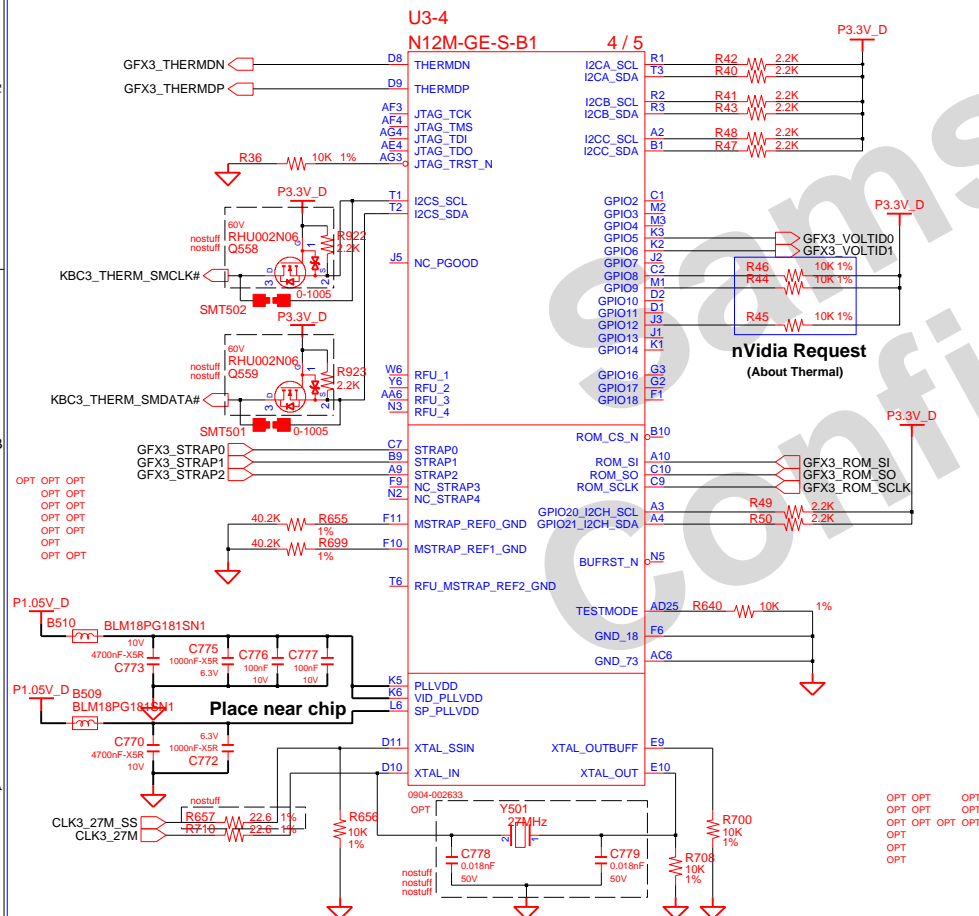
Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK417 = 0.27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 gDDR3 1Gb	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0110 for N	
25K ohm	1100	0100		
30K ohm	1101	0101		
35K ohm	1110	0110		
45K ohm	1111	0111		

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	0	27M
SCLK	1	0	1	0	N11M-GE GFX TPYE
	0	0	1	0	N11M-LP1
SI	0	0	1	1	gDDR3 1Gb
SI	0	1	1	1	gDDR3 2Gb
Strap2	0	0	0	0	N11M-GE2
Strap2	0	1	0	1	N11M-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIe swing level
Strap0	1	1	1	1	EDID_EN

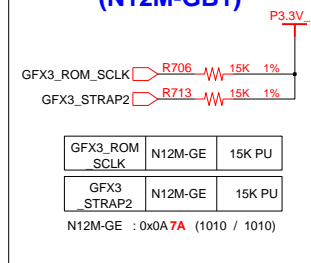
NC 1 C15

5 / 5

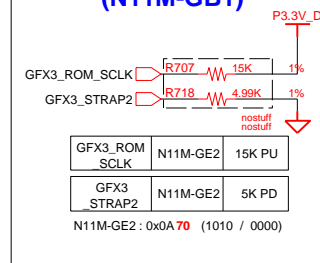
## Function Straps




### Chip Select Straps (N12M-GB1)



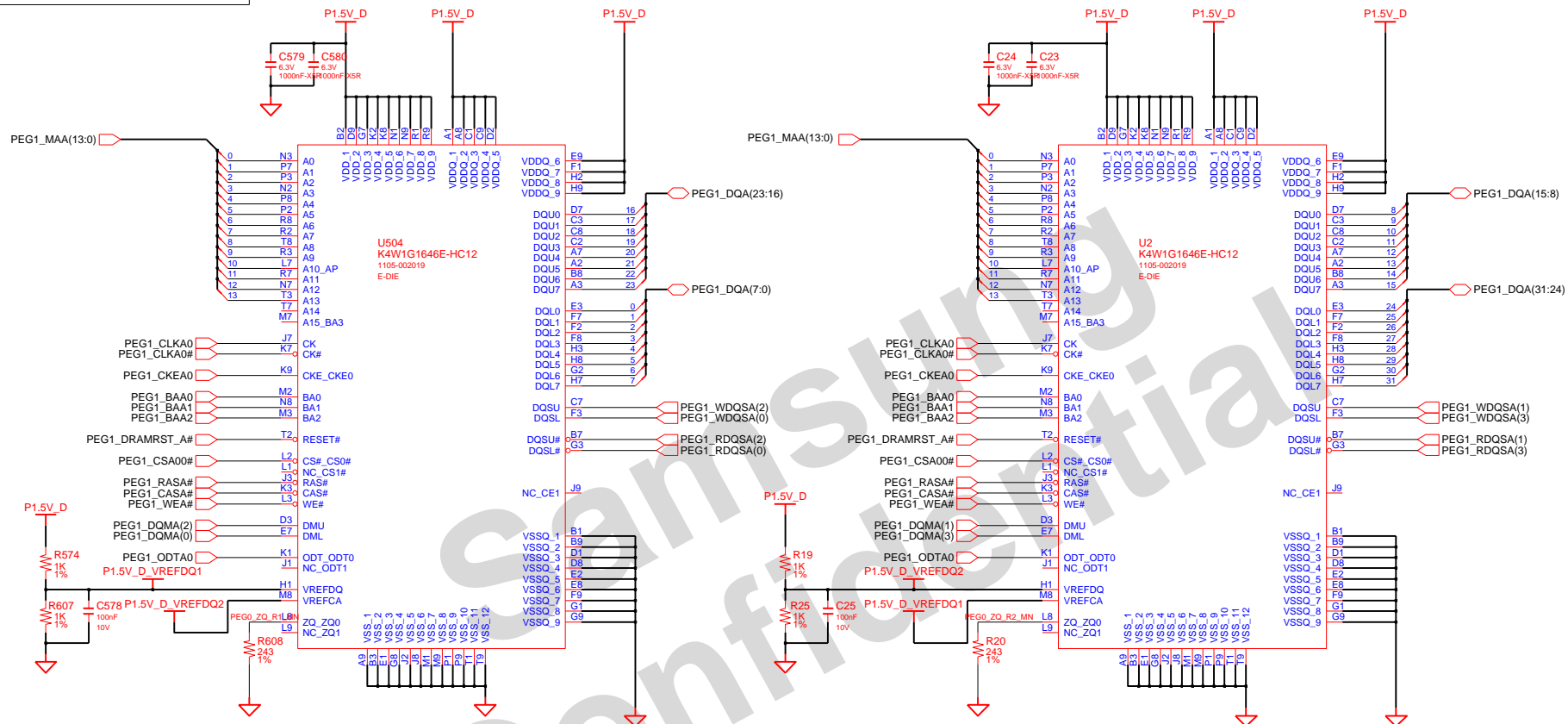
### Chip Select Straps (N11M-GB1)



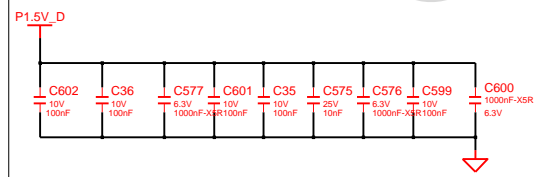
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L		
CHECK	MM KIM	DEV. STEP	PR		N12M_40NM(4/4)		
APPROVAL	BL LEE	REV	REV. 1.0		N12M_40NM(4/4)	PART NO.	BA41-01432A
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE	25 OF 52

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## A-Channel #0



Place near to VDDQ



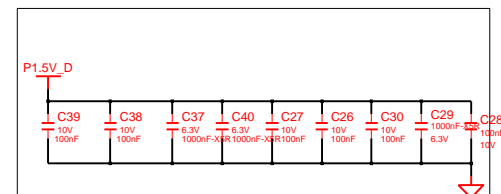
PEG1\_CLKA0 (R573) 243 1%

PEG1\_ODTA0 (R24) 10K 1%

PEG1\_CKEA0 (R609) 10K 1%

PEG1\_DRAMRST\_A# (R572) 10K 1%

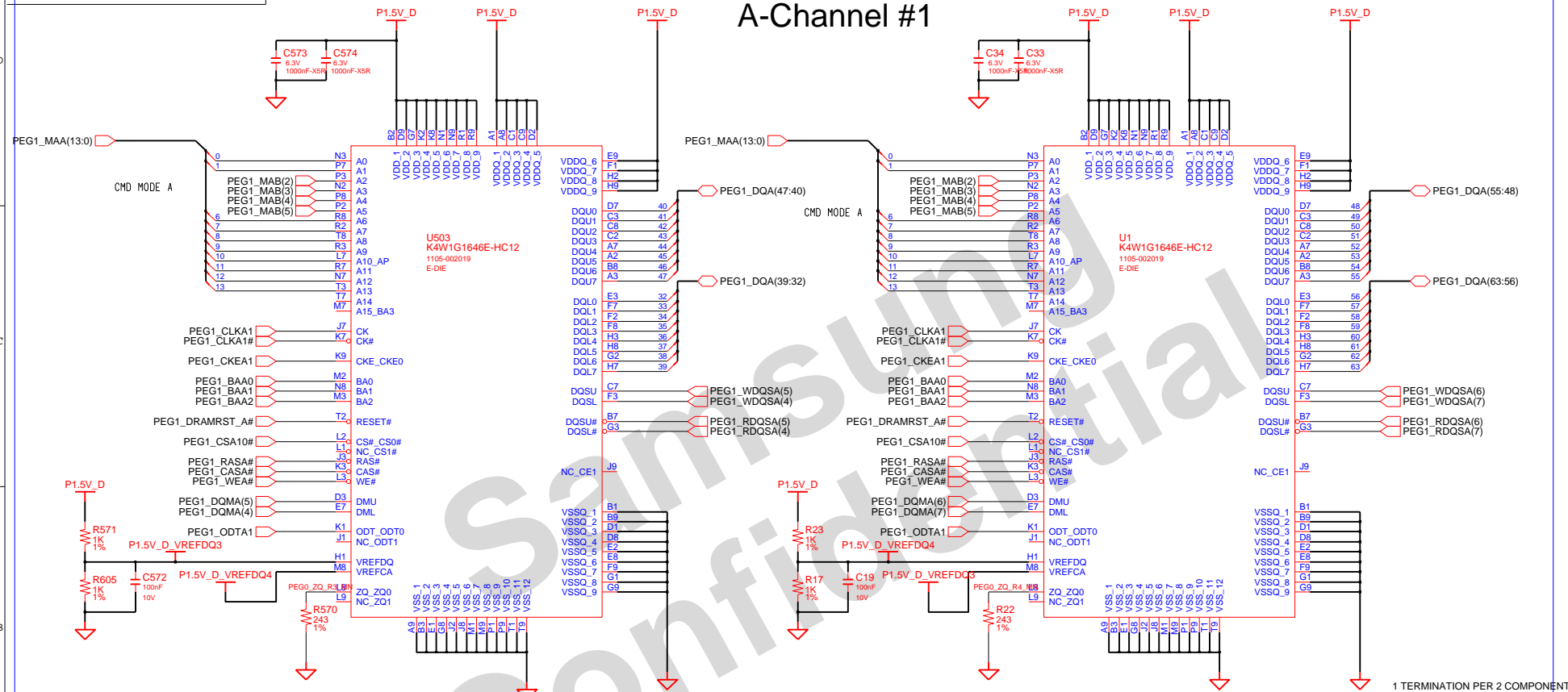
Place near to VDDQ



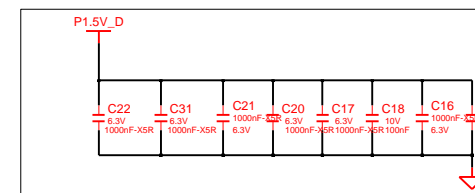
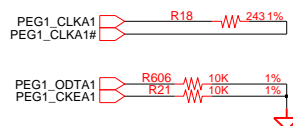
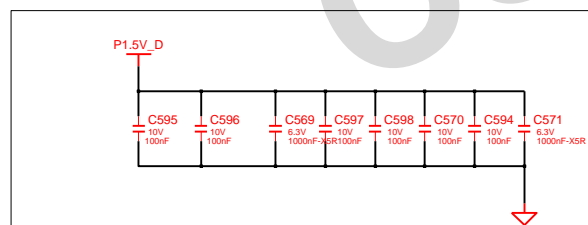
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT  
OPT  
OPT

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L  GRAPHIC_MEM A#0  GRAPHIC_MEM A#0	SAMSUNG  ELECTRONICS
CHECK	MK KM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
				PART NO.	BA41-01432A
MODULE CODE	LAST EDIT			November 22, 2010 15:53:34 PM	PAGE 26 OF 52

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Place near to VDDQ



1 TERMINATION PER 2 COMPONENT

OPT  
OPT  
OPT  
OPT  
OPT  
OPT  
OPT  
OPT

OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT

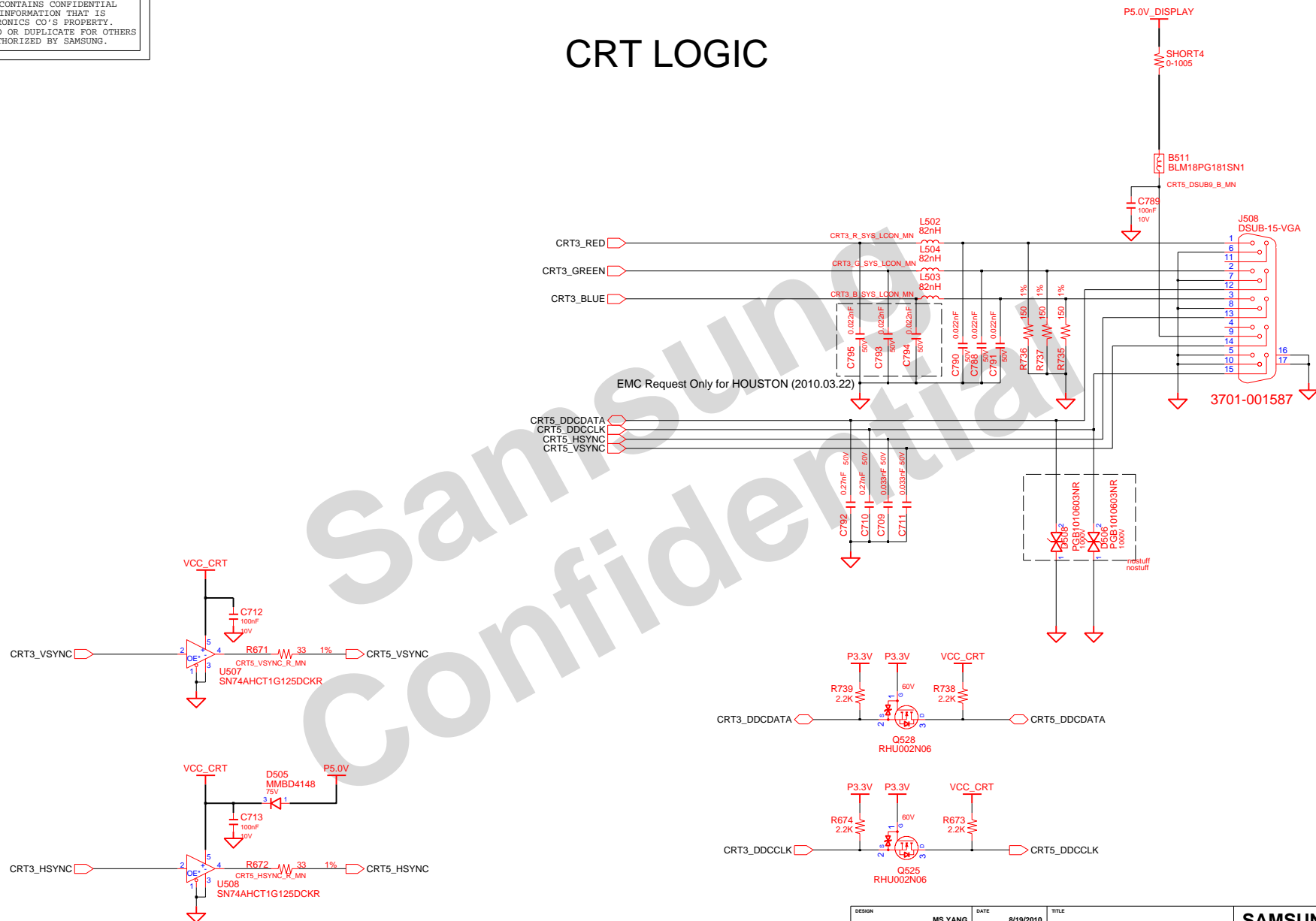
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG	
CHECK	MK KIM	DEV. STEP	PR	GRAPHIC_MEM A#1		ELECTRONICS	
APPROVAL	BL LEE	REV	rev. 1.0	GRAPHIC_MEM A#1		PART NO.	BA41-01432A
MODULE CODE	LAST EDIT			November 22, 2010 15:53:34 PM	PAGE	27	OF 52



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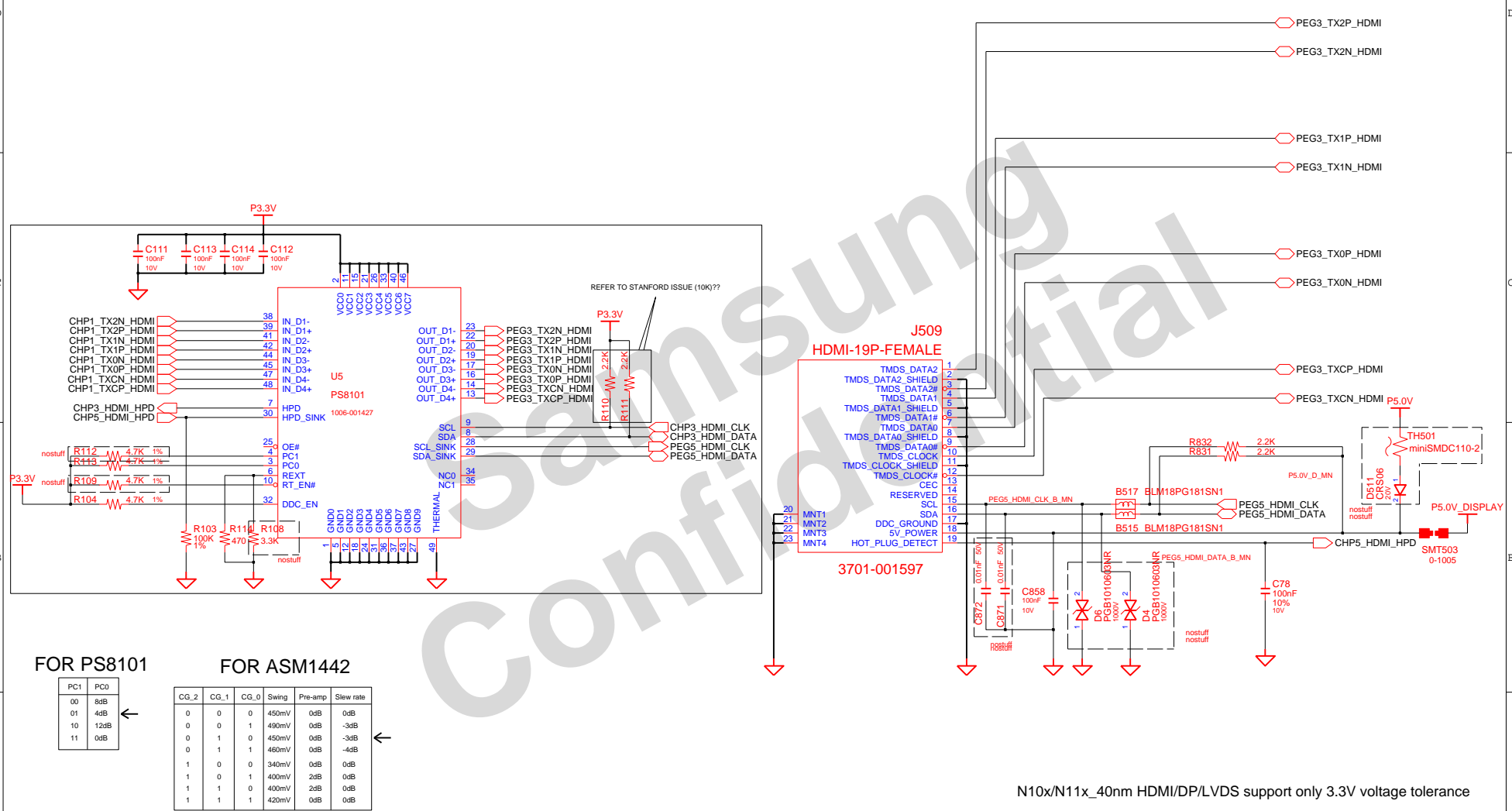
## CRT LOGIC



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		GRAPHICS_IF	
APPROVAL	BL LEE	REV	rev. 1.0		CRT	
MODULE CODE		LAST EDIT				
November 22, 2010 15:53:34 PM						PAGE 29 OF 52

(EMC request at 2010.04.15)

## HDMI Graphic



FOR PS8101

PC1	PC0
00	8dB
01	4dB
10	12dB
11	0dB

FOR ASM1442

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB

HDMI Level Shifter	EXT_Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note	4-6 CODE
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC		1006-001427
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PU/PD exist CGs nostuff is 450mV swing	1006-001471

FOR ASM1442

EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

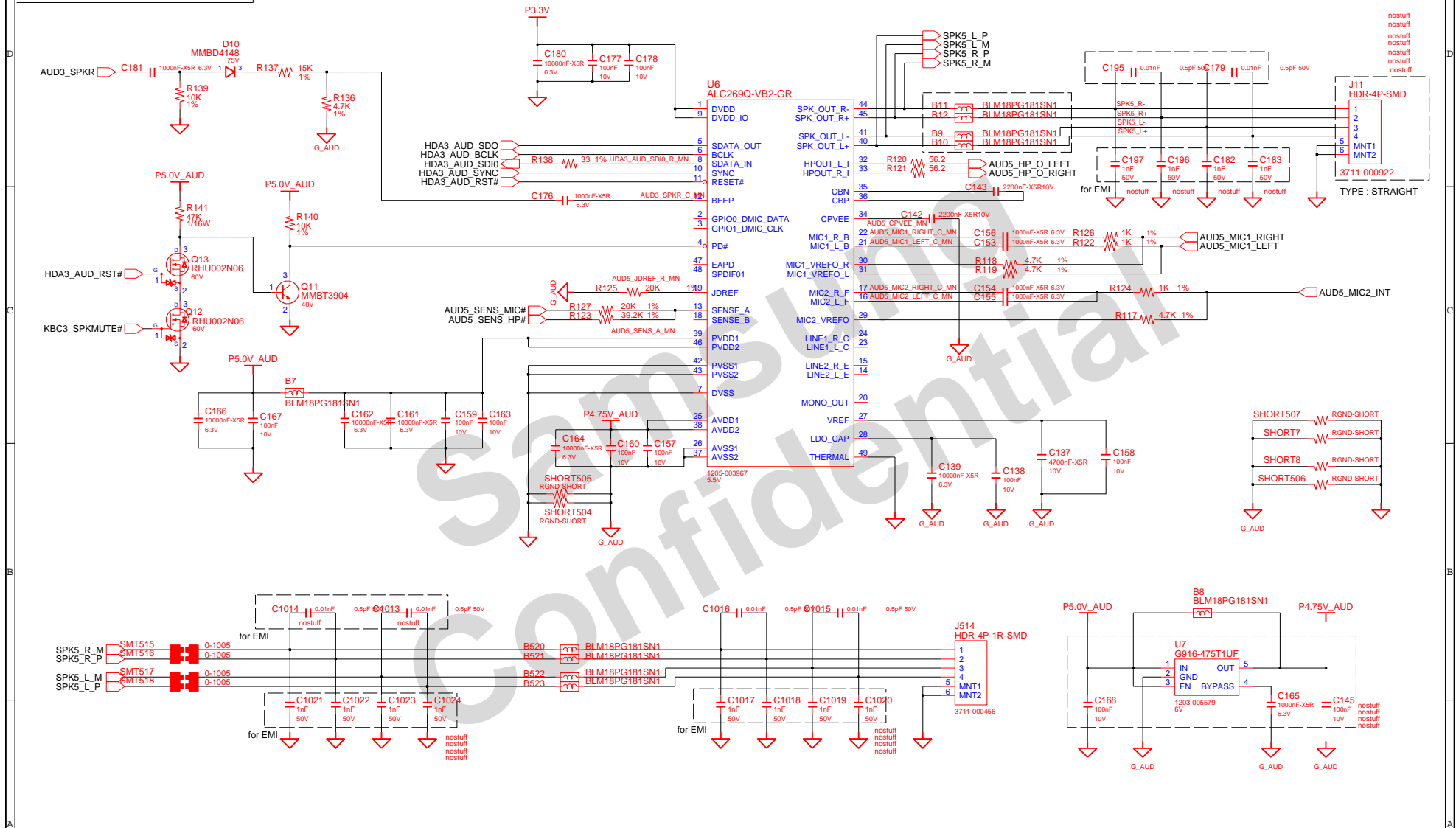
Internal Default Value

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L GRAPHICS_IF HDMI	<b>SAMSUNG</b> ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE	LAST EDIT				
November 22, 2010 15:53:34 PM				PAGE	30 OF 52

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# HD AUDIO

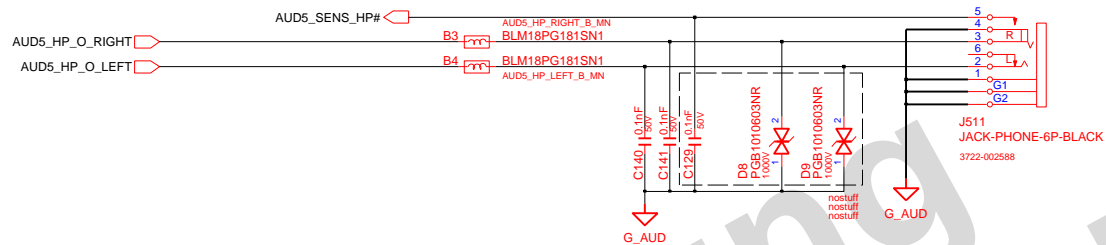


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		HDA_CODEC SUB	
APPROVAL	BL LEE	REV	rev. 1.0		AUDIO CODEC ALC269 SUB	
MODULE CODE		LAST EDIT				
November 22, 2010 15:53:34 PM						PAGE 31 OF 52

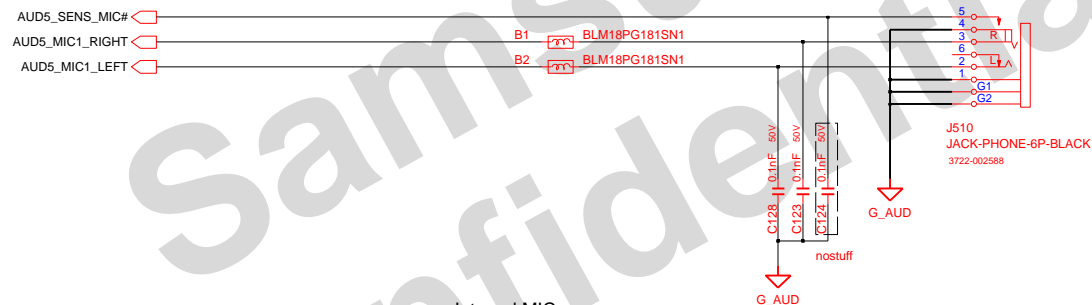
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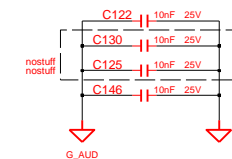
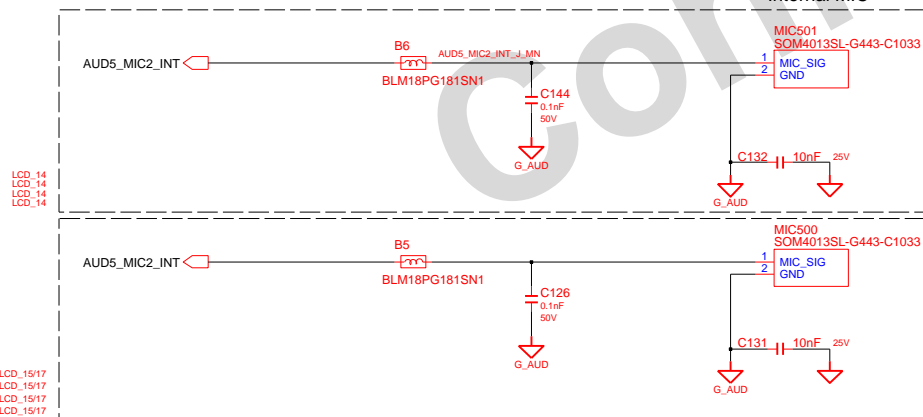
## HEADPHONE



## MIC JACK



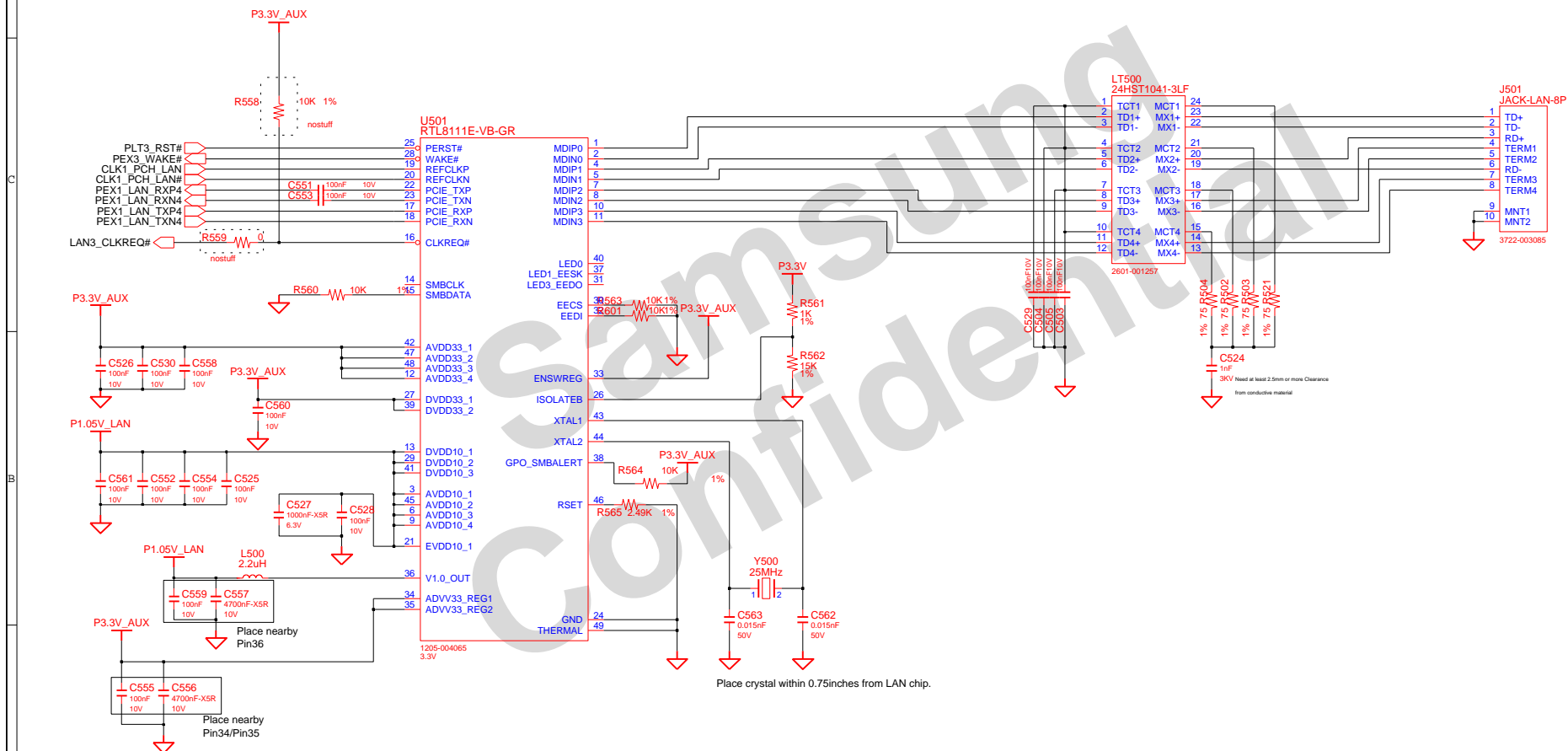
## Internal MIC



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	HDA_CODEC & LED SUB		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	AUDIO JACK & LED SUB	PART NO.	BA41-01432A
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE	32 OF 52



# Reatek RTL8111E



Place crystal within 0.75inches from LAN chip.

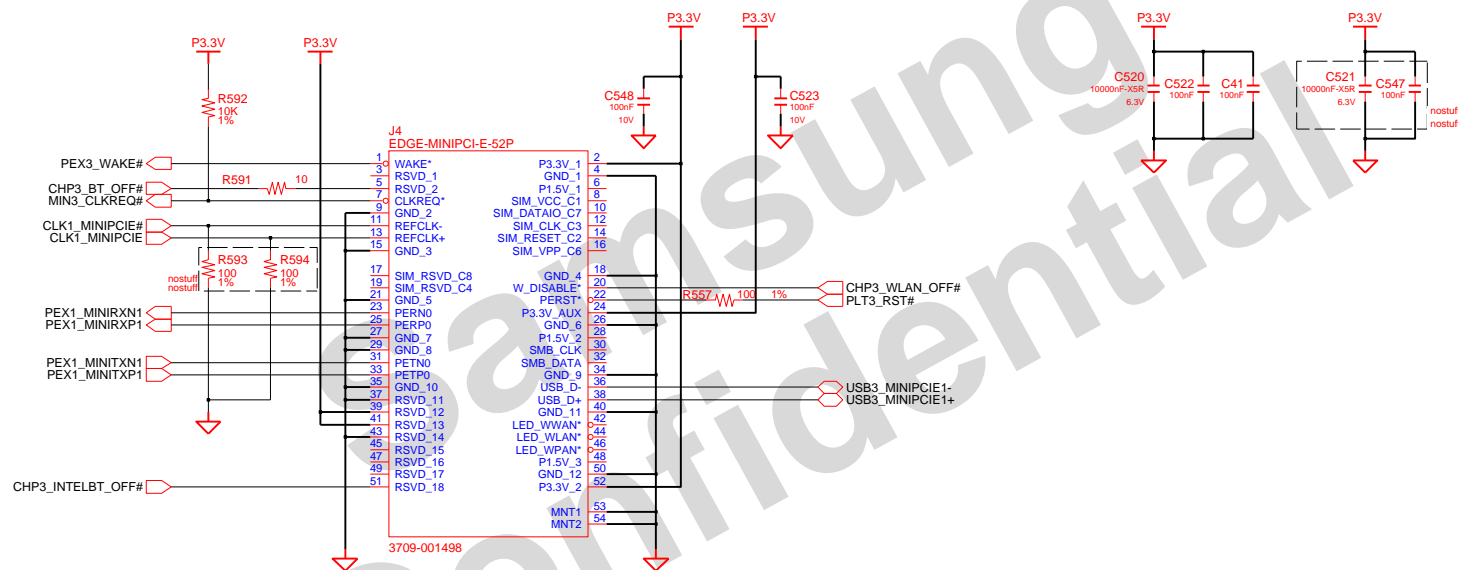
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L
CHECK	MK KIM	DEV. STEP	PR		LAN
APPROVAL	BL LEE	REV	rev. 1.0		LAN_Realttek_RTL8111
MODULE CODE		LAST EDIT			
				November 22, 2010 15:53:34 PM	PAGE 33 OF 52

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## WLAN

Height : 4.0mm



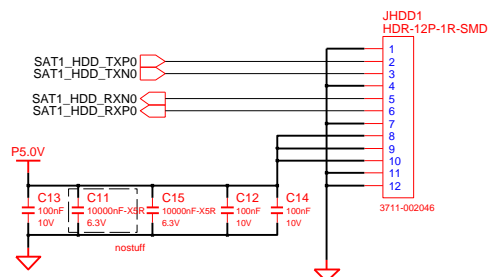
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L WLAN WLAN	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	34	OF 52

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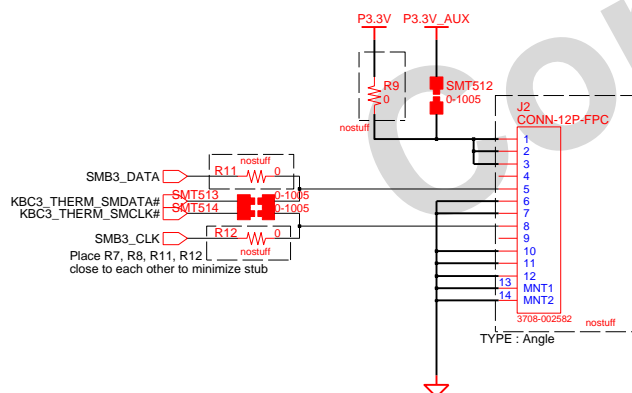
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## SATA HDD CONN

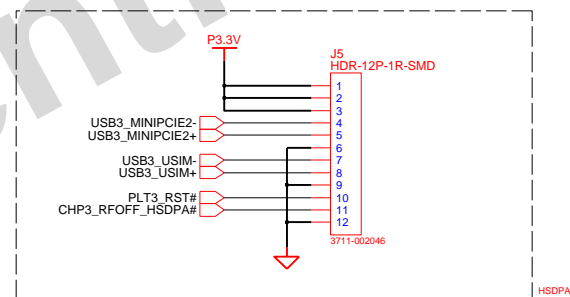
Cable Connector Type



FOR IR



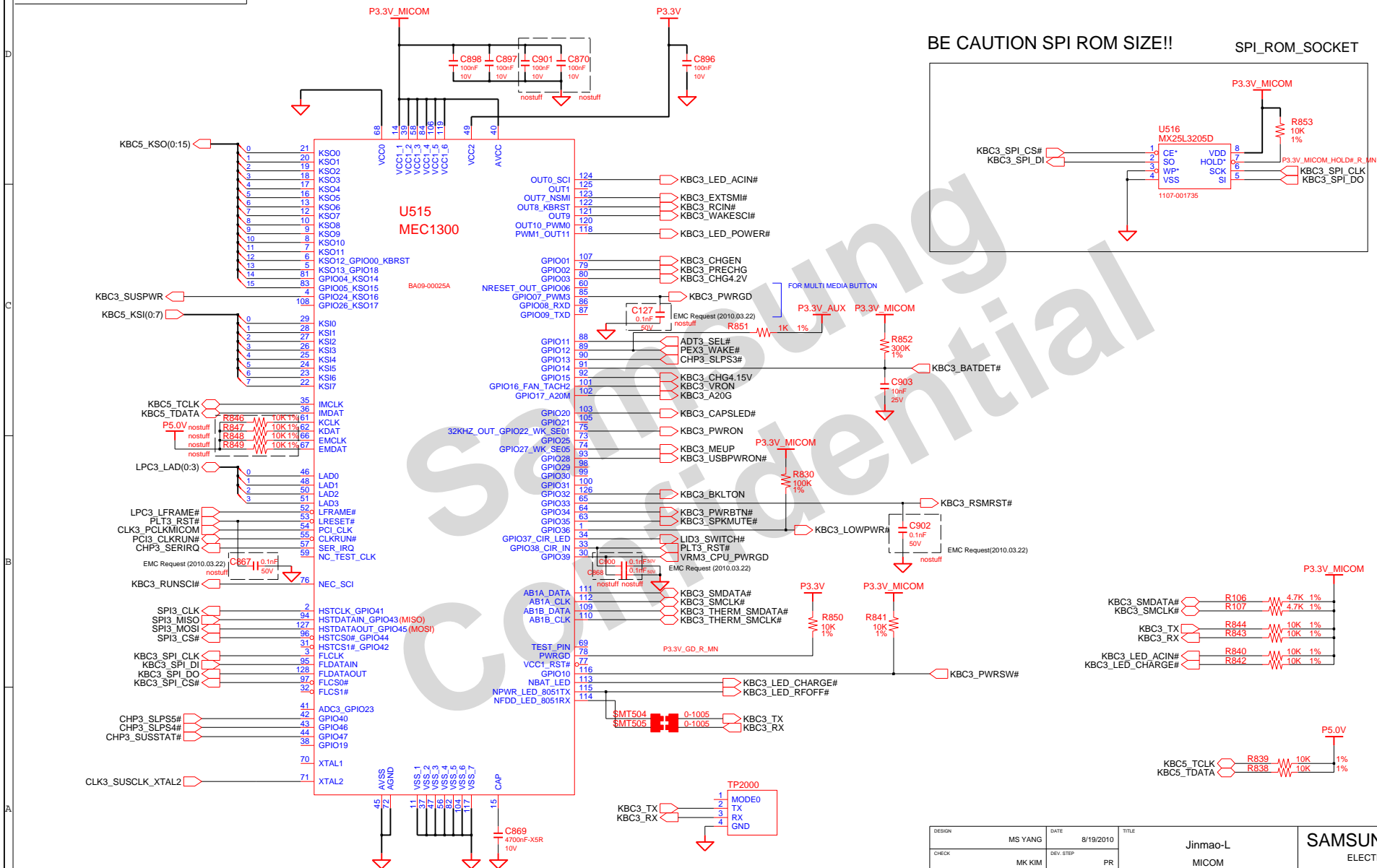
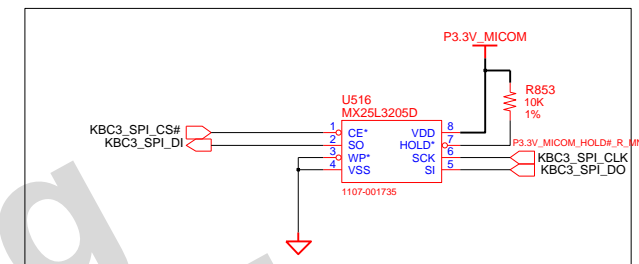
## MAIN to HSDPA SUB



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		SATA HDD & IR	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		SATA HDD & IR	PART NO.
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM			BA41-01432A
				PAGE	35	OF 52

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SPI ROM SOCKET

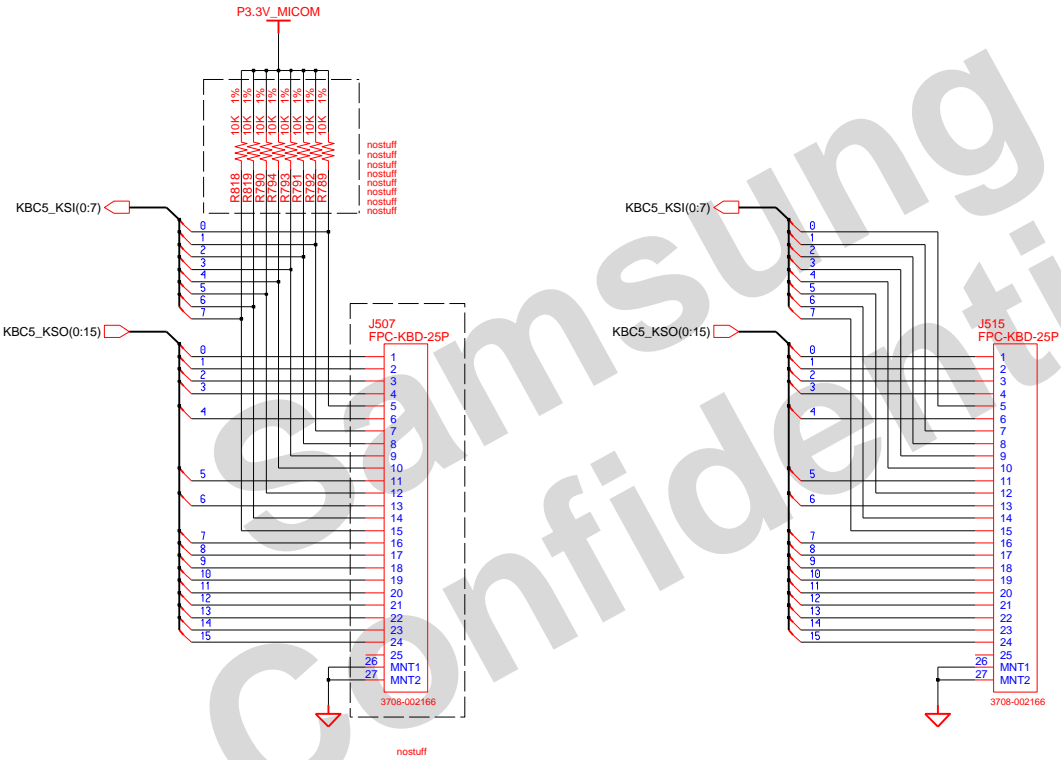


DESIGN	MS YANG	DATE	8/19/2010	TITLE  Jinmao-L MICOM SMSC MEC1300	PART NO.  BA41-01432A	<b>SAMSUNG</b> ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE	LAST EDIT					
				November 22, 2010 15:53:34 PM	PAGE	36
					OF	52

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# Micom Glue Logic

## KEYBOARD



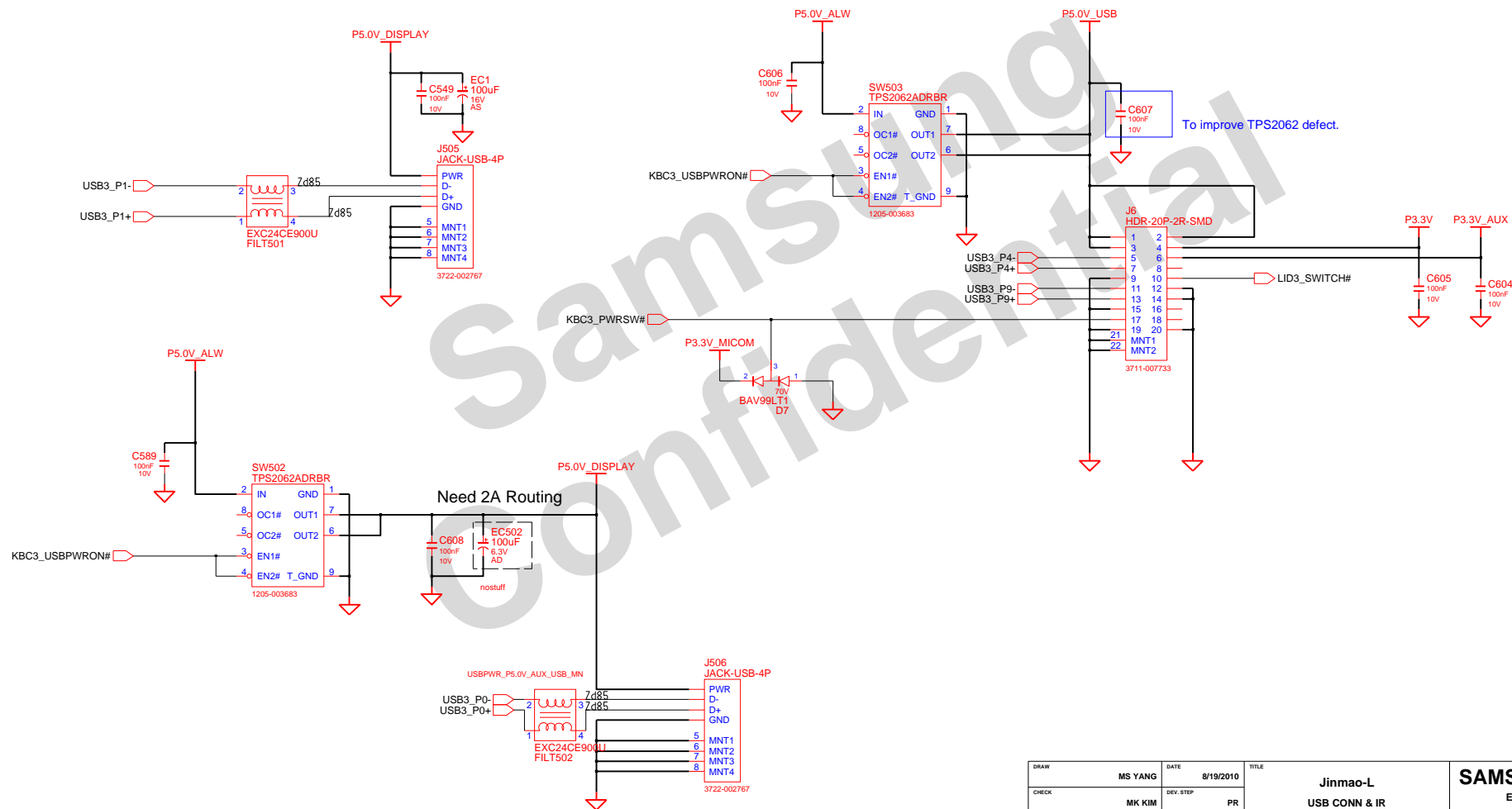
DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	MICOM GLUE LOGIC		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	MICOM GLUE LOGIC	PART NO.	BA41-01432A
MODULE CODE	LAST EDIT			November 22, 2010 15:53:34 PM	PAGE	37 OF 52

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# POWER S/W SUB B'D CONNECTOR

## MAIN to SUB



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	USB CONN & IR		
APPROVAL	BL LEE	REV	rev. 1.0	USB & IR	PART NO. BA41-01432A	
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE	38 OF 52

**VCHG Table:**

KBC3_CHG4.2V	KBC3_CHG4.15V	VCHG
0	0	12.597V
1	0	12.509V
0	1	12.443V
1	1	12.391V

**ICHG=2.561A FOR 5200mAh & 4400mAh**

**Adapter configuration Table:**

Adapter configuration			
60W / 3.03A / 96%		90W / 4.32A / 91.2%	
Value	SEC Code	Value	SEC Code
Rtop 200K	2007-007334	10K	2007-007142
Rbot 27.4K	2007-007274	30K	2007-008275

**Component List:**

- Q501: AP4435GM
- Q502: AP4435GM
- Q503: AP4435GM
- Q504: BAT54C
- Q505: ISL6255AHRZ-T
- Q506-1: AP4232BGM-HF
- Q506-2: AP4232BGM-HF
- Q507: BSS84
- Q508: RHU002N06
- Q509: RHU002N06
- Q510: RHU002N06
- Q511: RHU002N06
- Q512: RHU002N06
- Q513: RHU002N06
- Q514: RHU002N06
- Q515: RHU002N06
- Q516: RHU002N06
- Q517: RHU002N06
- Q518: RHU002N06
- Q519: RHU002N06
- Q520: RHU002N06
- Q521: RHU002N06
- Q522: RHU002N06
- Q523: RHU002N06
- Q524: RHU002N06
- Q525: RHU002N06
- Q526: RHU002N06
- Q527: RHU002N06
- Q528: RHU002N06
- Q529: RHU002N06
- Q530: RHU002N06
- Q531: RHU002N06
- Q532: RHU002N06
- Q533: RHU002N06
- Q534: RHU002N06
- Q535: RHU002N06
- Q536: RHU002N06
- Q537: RHU002N06
- Q538: RHU002N06
- Q539: RHU002N06
- Q540: RHU002N06
- Q541: RHU002N06
- Q542: RHU002N06
- Q543: RHU002N06
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- Q596: RHU002N06
- Q597: RHU002N06
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- Q600: RHU002N06

## P3.3V\_AUX & P5.0V\_AUX

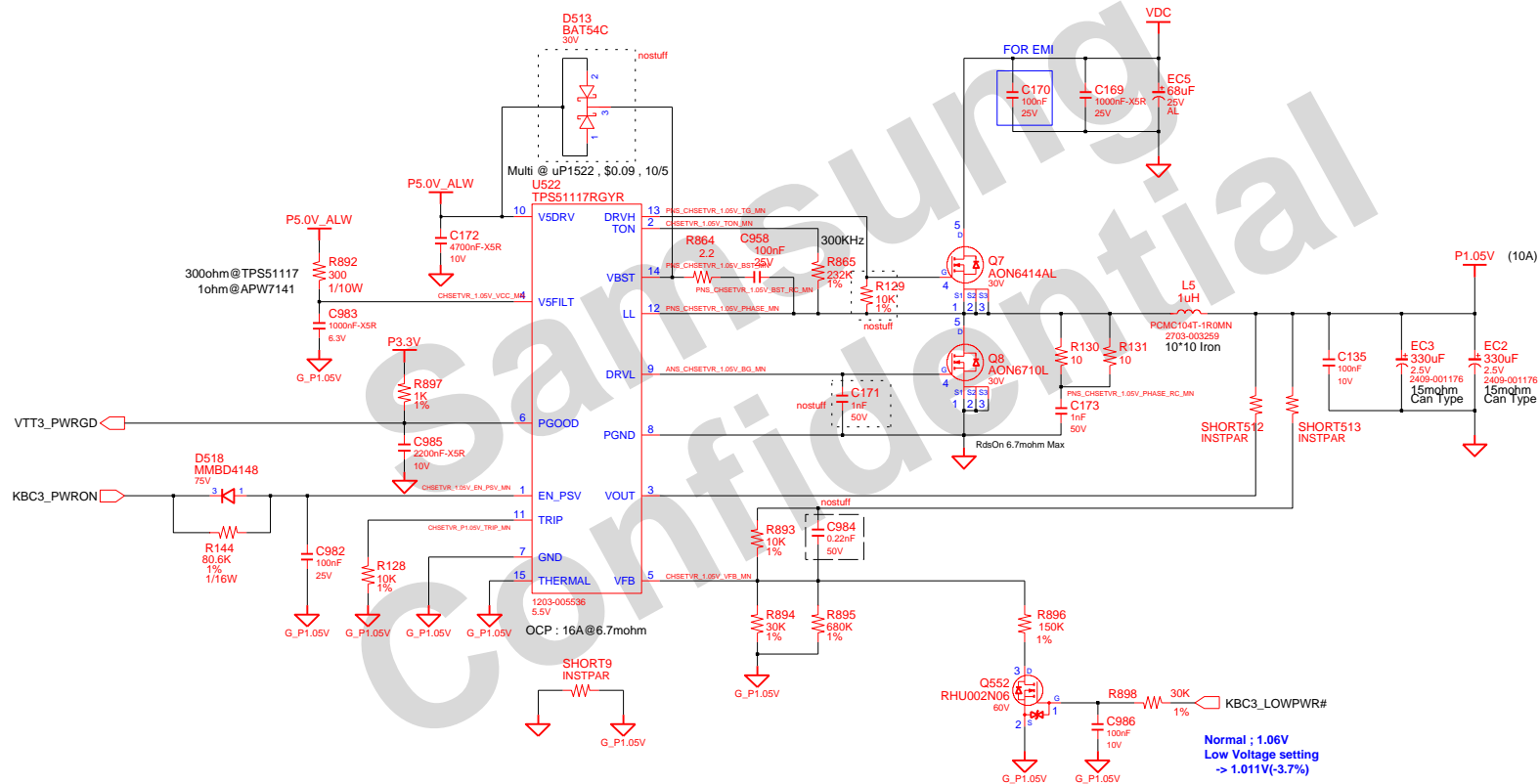
D:/users/mobile39/mentor/Jinmao-L/Main/PR/Jinmao-L MAIN



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## CHIPSET POWER(P1.05V)

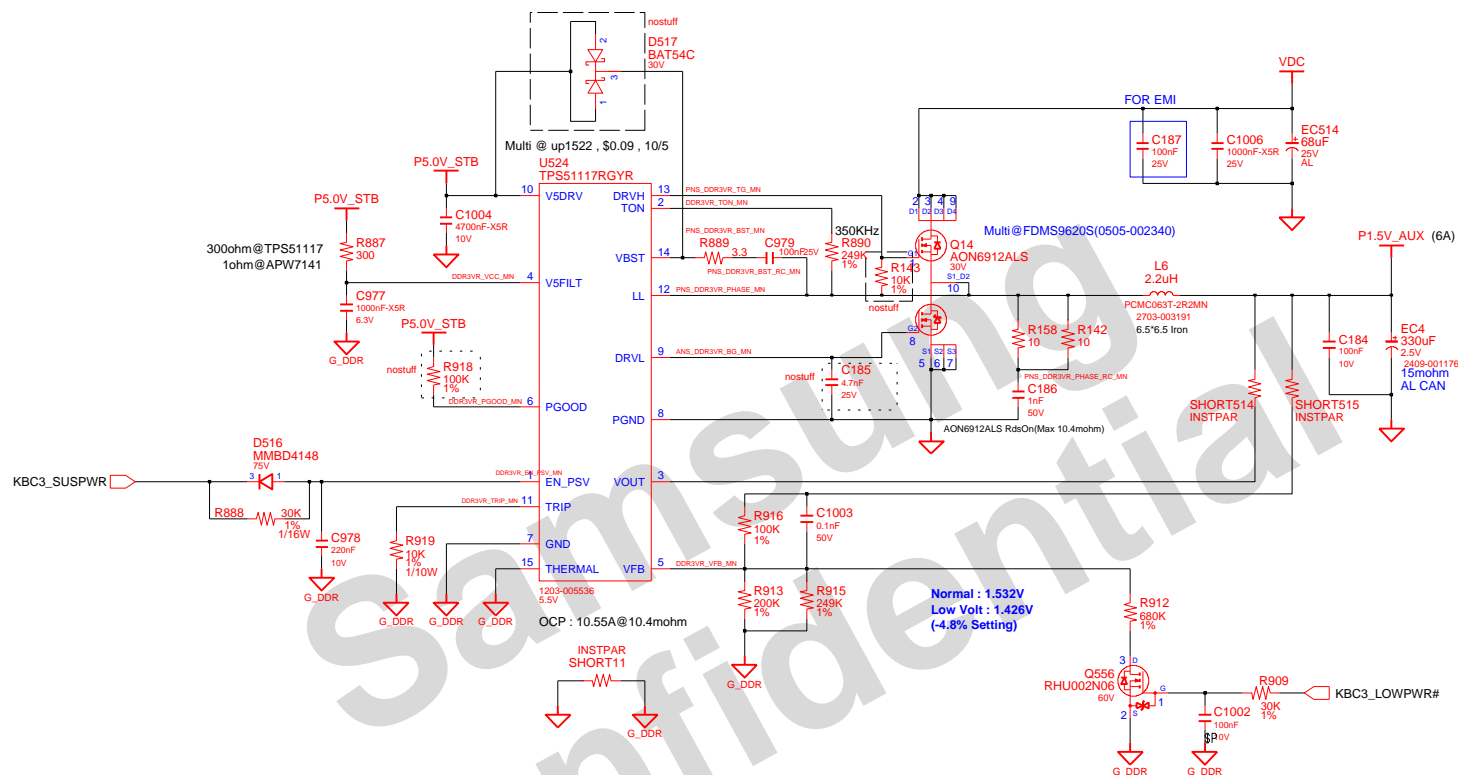


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		P1.05V	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		TI TPS51117R	PART NO.
MODULE CODE		LAST EDIT				BA41-01432A
				November 22, 2010 15:53:34 PM	PAGE	41 OF 52

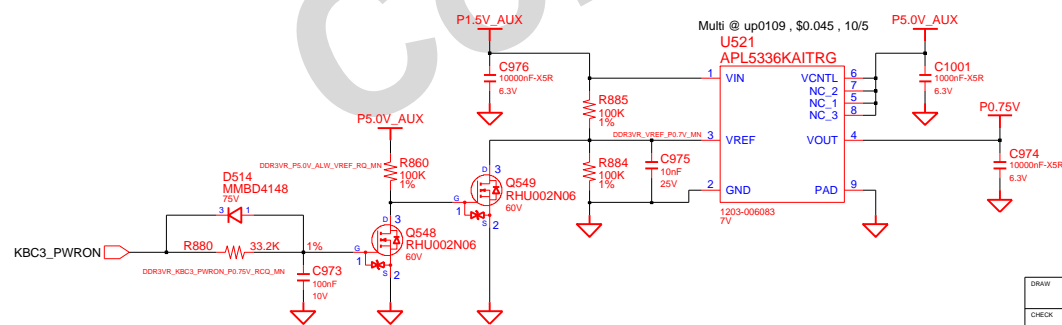
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## DDR3 Power



## DDR3 VTT(0.75V)

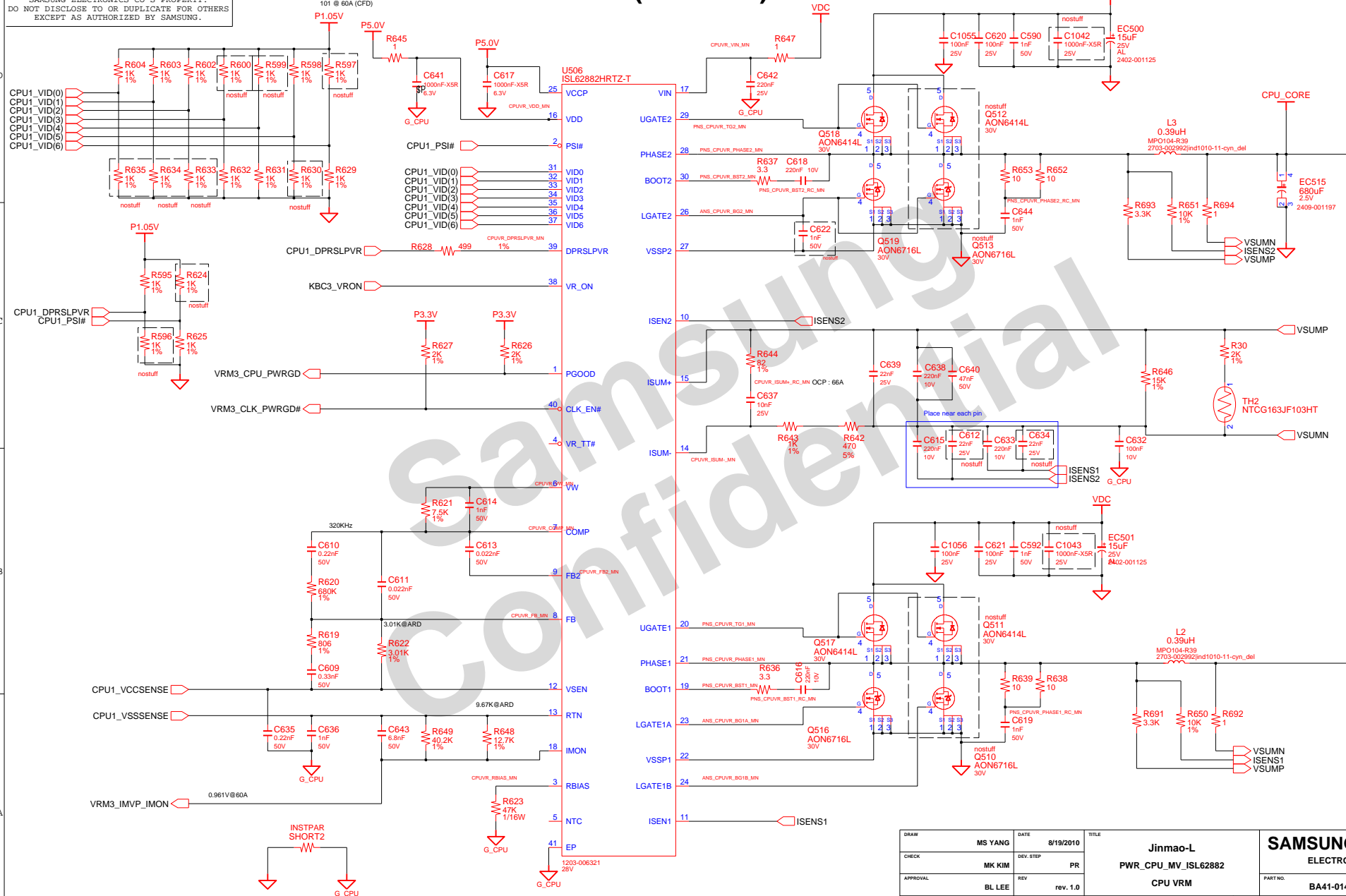


DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	PWR MEMORY		
APPROVAL	BL LEE	REV	rev. 1.0	RT8207		
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	42	OF 52

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## CPU VRM (IMVP-6.5)



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L
CHECK	MK KIM	DEV. STEP	PR		PWR_CPU_MV_ISL62882
APPROVAL	BL LEE	REV	rev. 1.0		CPU VRM
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	43 OF 52

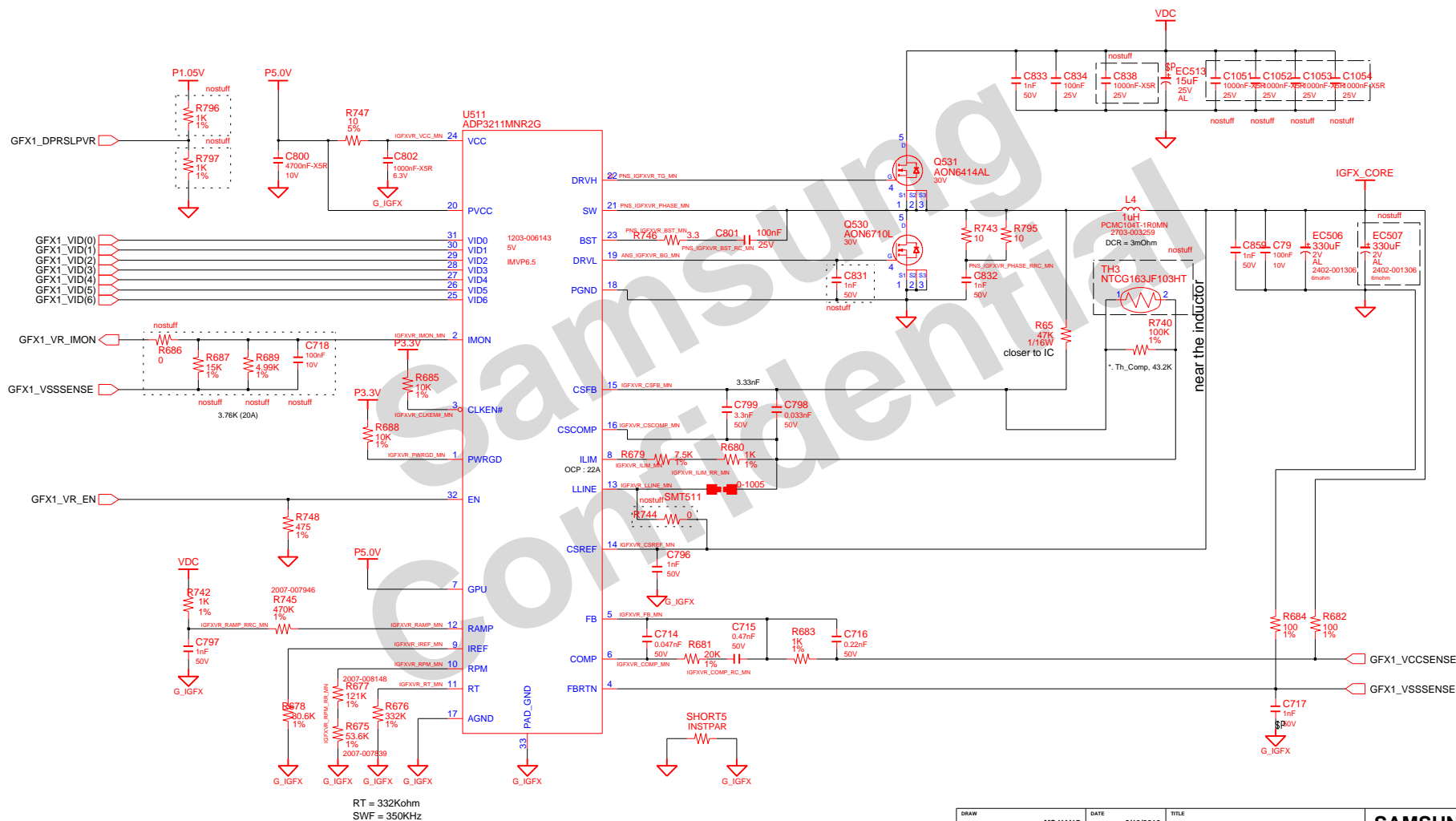
SAMSUNG

ELECTRONICS

PART NO. BA41-01432A

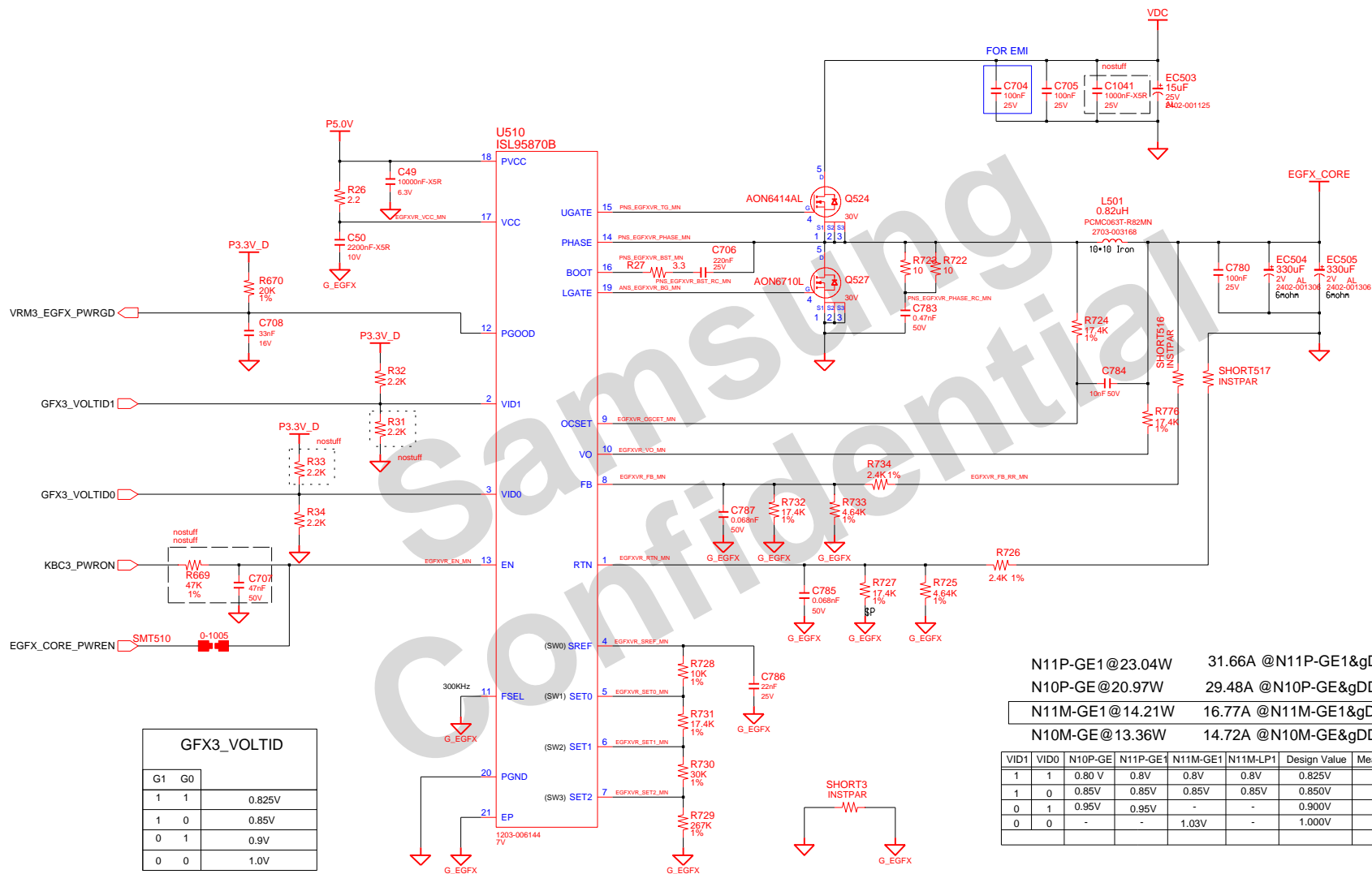
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## Internal GFX Core Power



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	<b>SAMSUNG</b>	
CHECK	MK KIM	DEV. STEP	PR	PWR GFX_INT_	Internal Graphic Power	ELECTRONICS	
APPROVAL	BL LEE	REV	rev. 1.0			PART NO.	BA41-01432A
MODULE CODE	undefined	LAST EDIT			November 22, 2010 15:53:34 PM	PAGE	44 OF 52

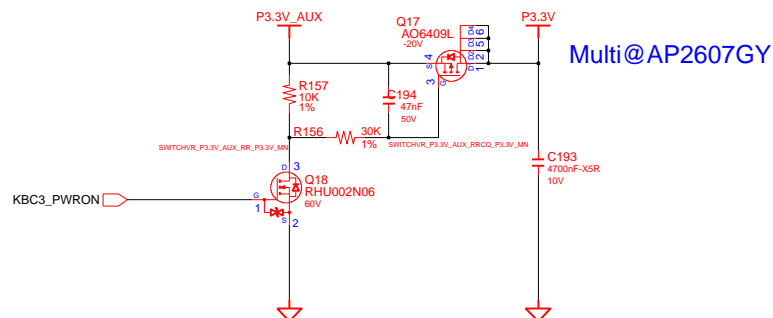
## External GFX Core Power



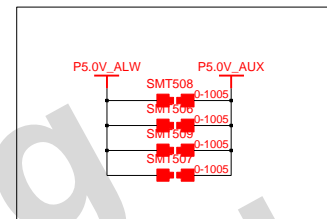
VID1	VID0	N10P-GE	N11P-GE	N11M-GE1	N11M-LP1	Design Value	Measured Value
1	1	0.80 V	0.8V	0.8V	0.8V	0.825V	
1	0	0.85V	0.85V	0.85V	0.85V	0.850V	
0	1	0.95V	0.95V	-	-	0.900V	
0	0	-	-	1.03V	-	1.000V	

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L PWR_GFX_MV_EXT External Graphic Power	SAMSUNG ELECTRONICS	
CHECK	MK KIM	DEV. STEP	PR		PART NO.	BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE 45 OF 52

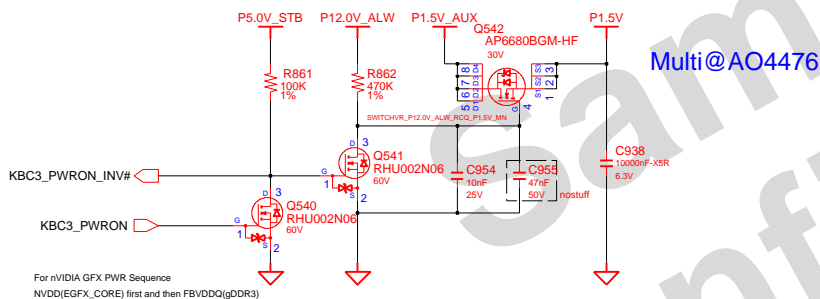
### Switched Power On (P3.3V)



## P5.0V\_AUX

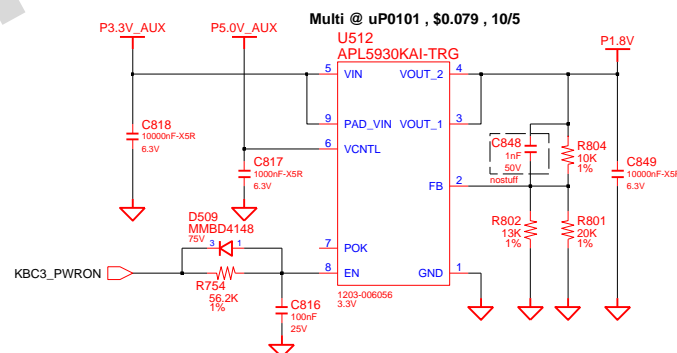


### Switched Power On (P1.5V)

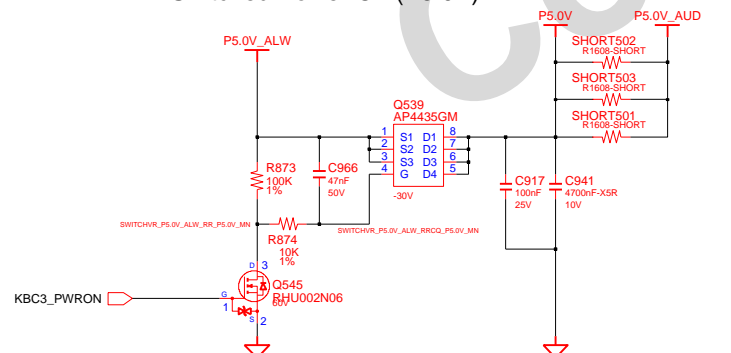


For nVIDIA GFX PWR Sequence  
NVDD(EGFX\_CORE) first and then FBVDDQ(gDDR3)

P1.8V(LDO)



## Switched Power On (P5.0V)

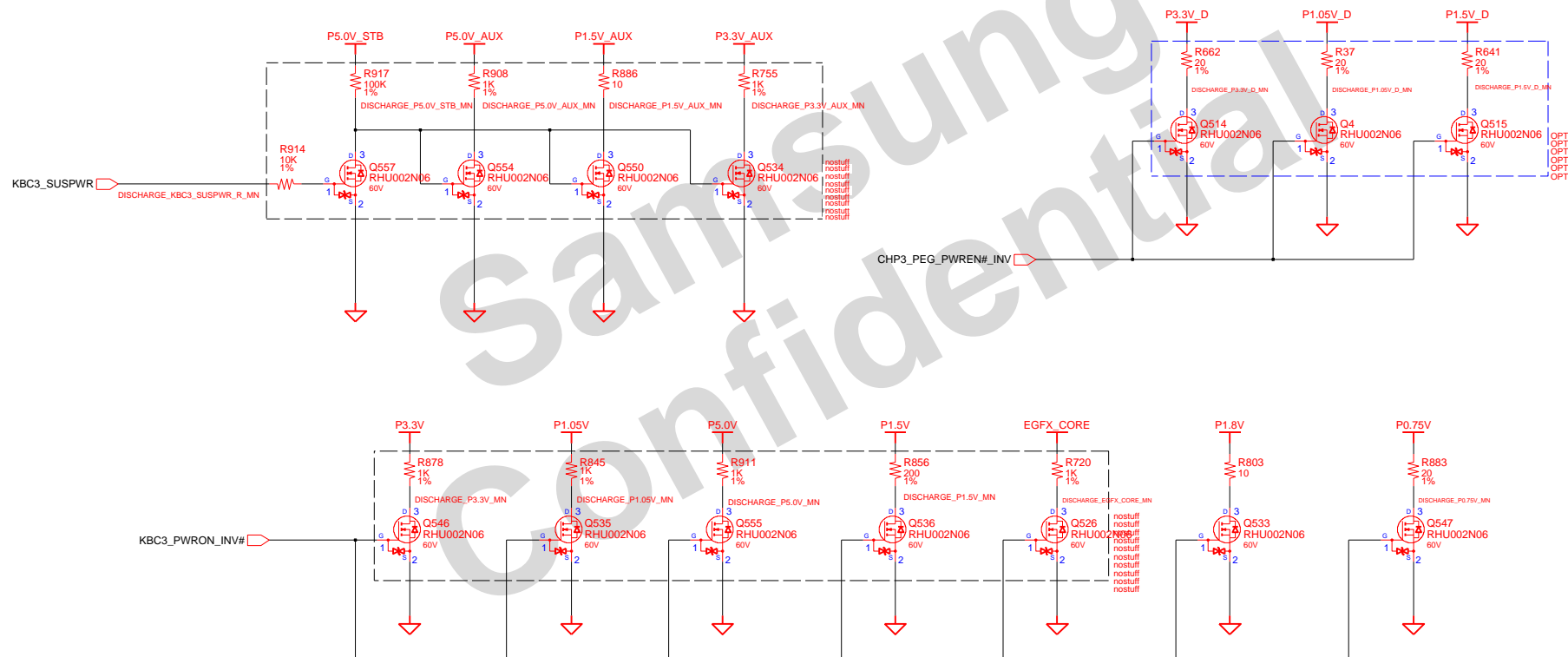


DRAW	MS YANG	DATE	8/19/2010	Jinmao-L PWR_MV_SWITCHED SWITCHED POWER	SAMSUNG ELECTRONICS	
CHECK	MK KIM	DEV. STEP	PR			
APPROVAL	BL LEE	REV	rev. 1.0			
PART NO.						BA41-01432A
MODULE CODE		LAST EDIT			November 22, 2010 15:53:34 PM	PAGE 46 OF 52

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# POWER DISCHARGER

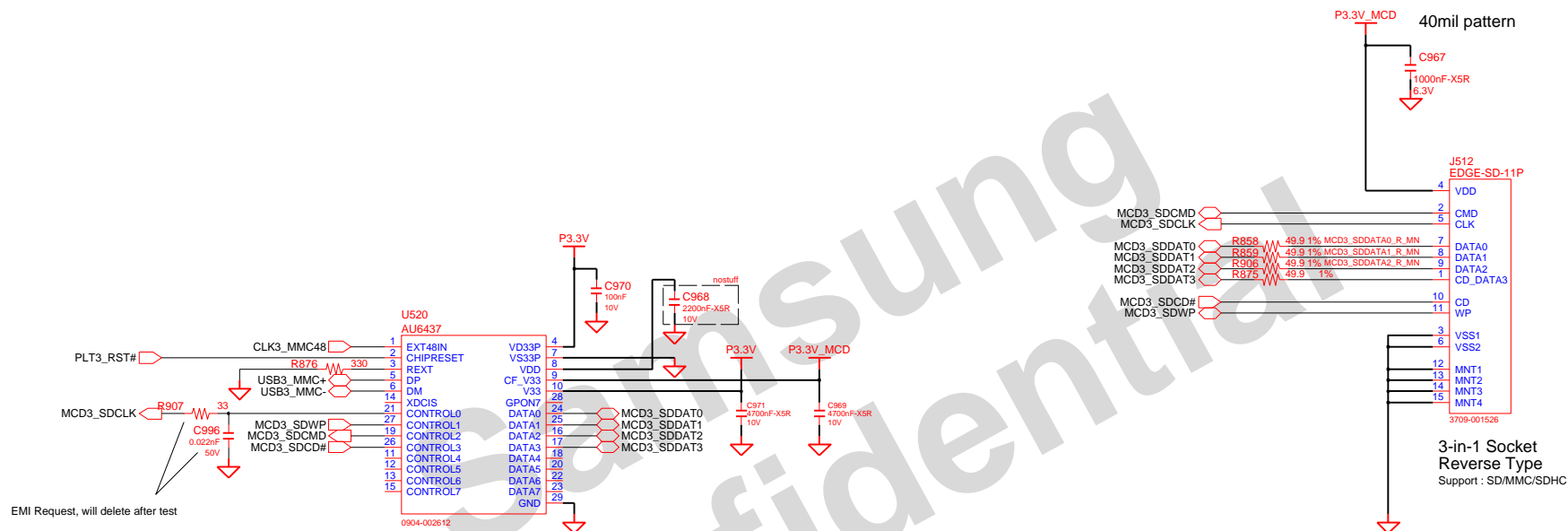


DRAW	MS YANG	DATE	8/19/2010	Jinmao-L  PWR_MV_DISCHARGER  DISCHARGING LOGIC		SAMSUNG ELECTRONICS					
CHECK	MK KIM	DEV. STEP	PR								
APPROVAL	BL LEE	REV	rev. 1.0	PART NO.				BA41-01432A			
MODULE CODE		undefined		LAST EDIT		November 22, 2010 15:53:34 PM		PAGE	47	OF	52

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## AU6437 (4-in-1)



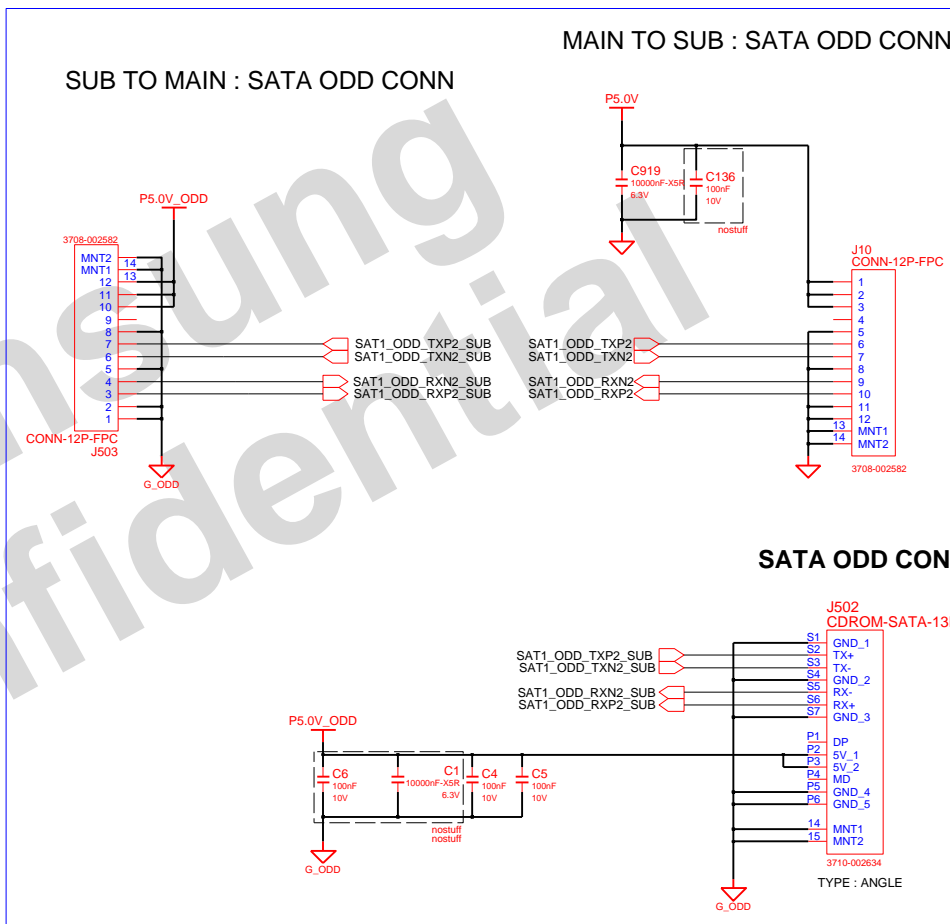
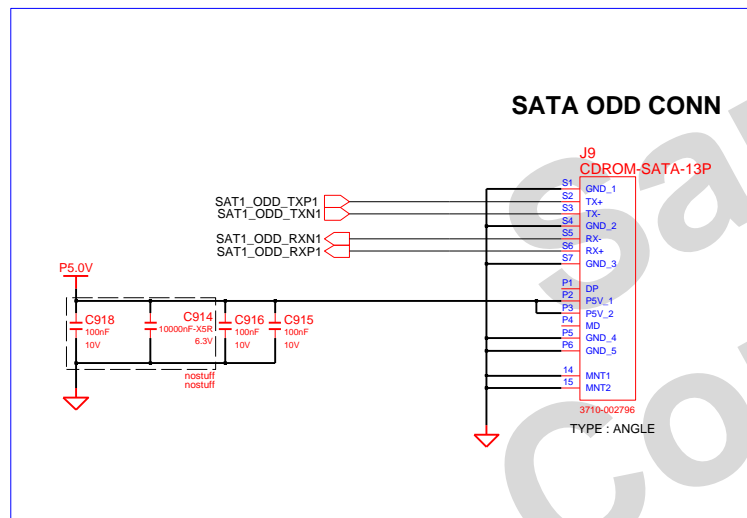
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	AU 6437	BA41-01432A	
APPROVAL	BL LEE	REV	rev. 1.0	AU 6437		
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE 48 OF 52	



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# SATA ODD SUB BOARD

**15.6" & 17.3"****MAIN TO SUB : SATA ODD CONN****SUB TO MAIN : SATA ODD CONN****14"****SATA ODD CONN****MT505  
RMNT-25-65-1P****G\_ODD**

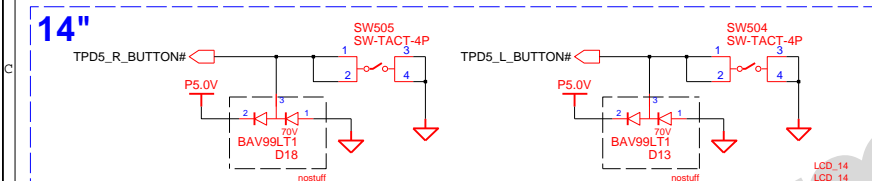
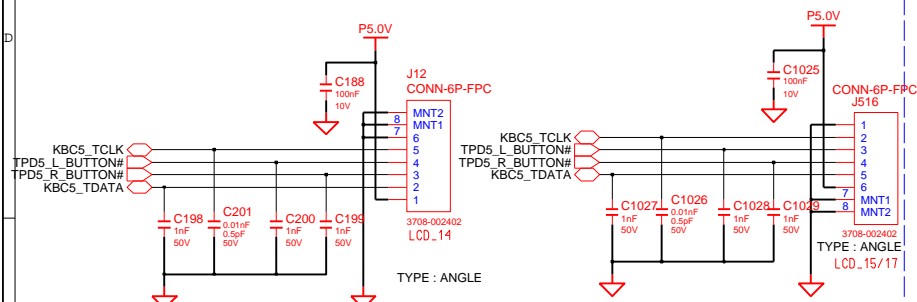
ODD sub board mount hole

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01432A
CHECK	MK KIM	DEV. STEP	PR	SATA ODD	SATA ODD	
APPROVAL	BL LEE	REV	rev. 1.0	SATA ODD		
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE	49 OF 52

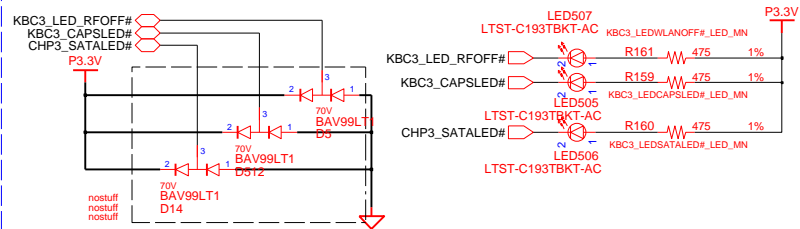
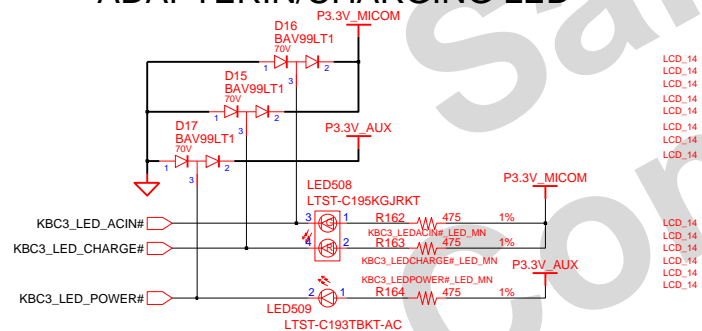
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## TOUCHPAD

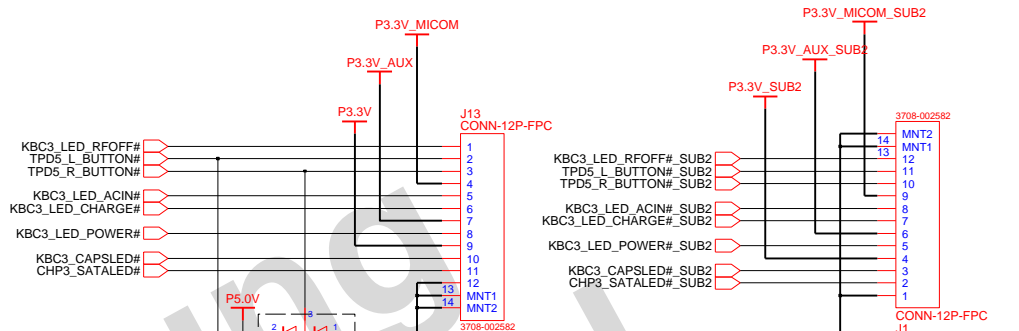


## ADAPTERIN/CHARGING LED

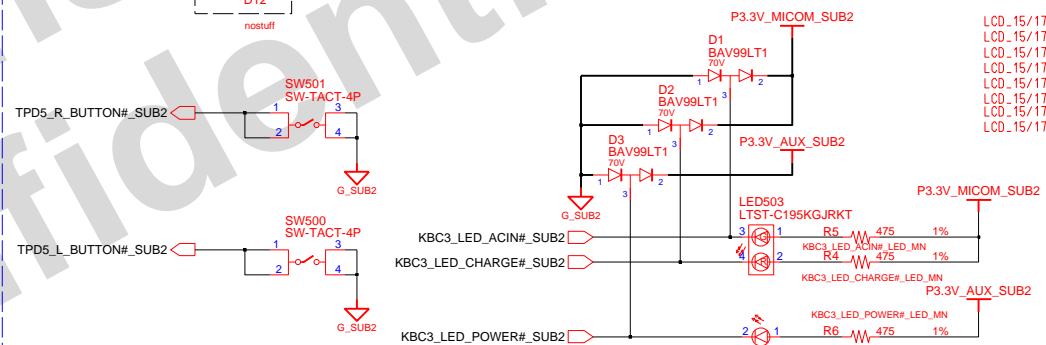


## 15.6" & 17.3"

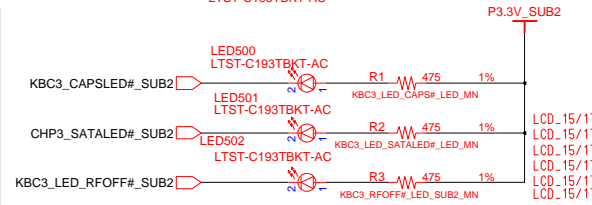
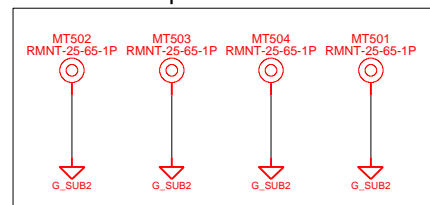
## TOUCHPAD MAIN TO SUB TOUCHPAD SUB TO MAIN



## ADAPTERIN/CHARGING LED



## Touchpad Mount Hole

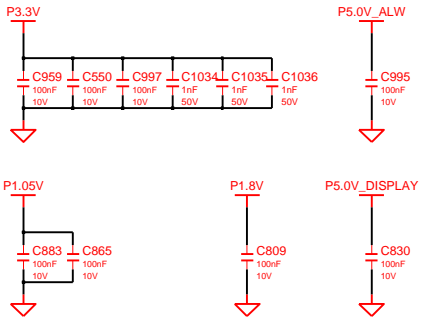
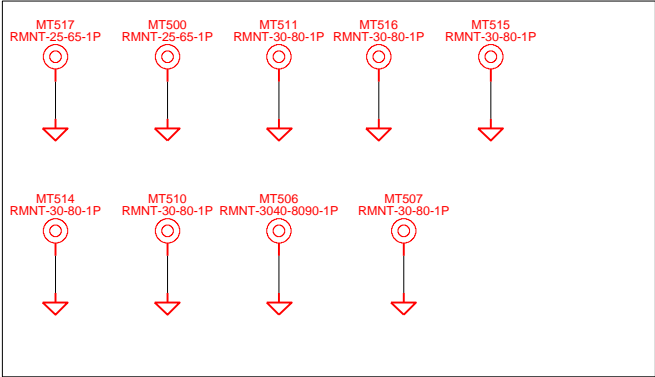


DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L
CHECK	MK KIM	DEV. STEP	PR		Touchpad
APPROVAL	BL LEE	REV	rev. 1.0		Touchpad
MODULE CODE		LAST EDIT			
November 22, 2010 15:53:34 PM				PAGE	50 OF 52

**SAMSUNG**  
ELECTRONICS  
PART NO.  
BA41-01432A

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Mainboard Mount ((25-65)X2EA, (30-80)X7EA)



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	MNT hole		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	MNT hole	PART NO.	BA41-01432A
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE 51 OF 52

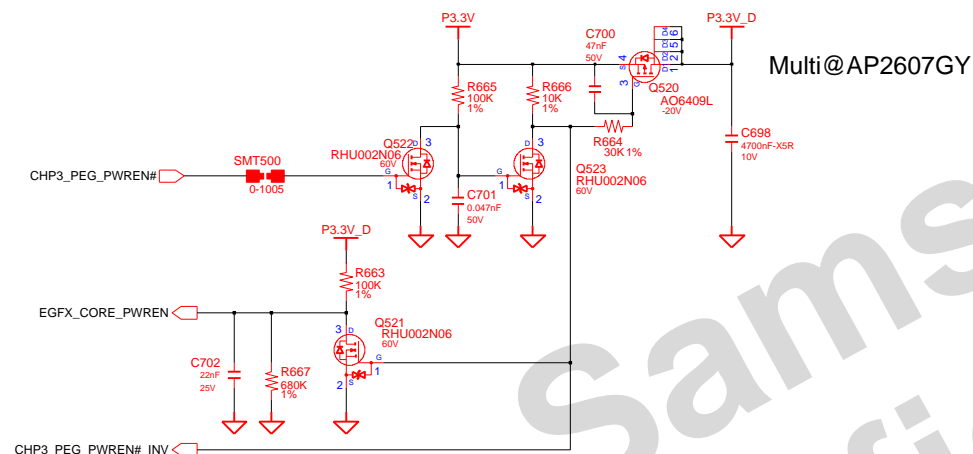
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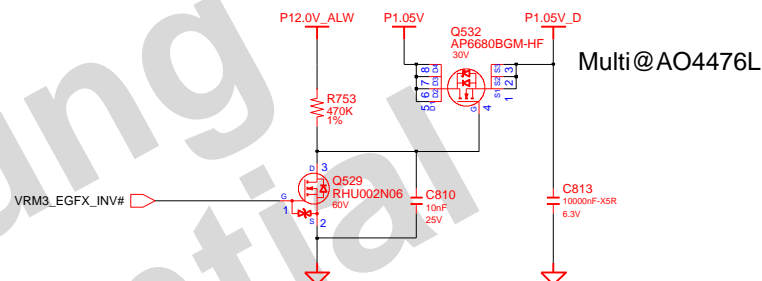
## Switched Power 2 (For nVidia GFX Power Sequence)

Sequence (D3.3V -> GFX Core -> D1.8V -> D1.5V -> D1.05V)

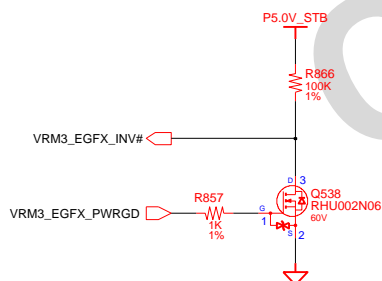
Discrete Switched Power (D3.3V : Max\_1.2A)



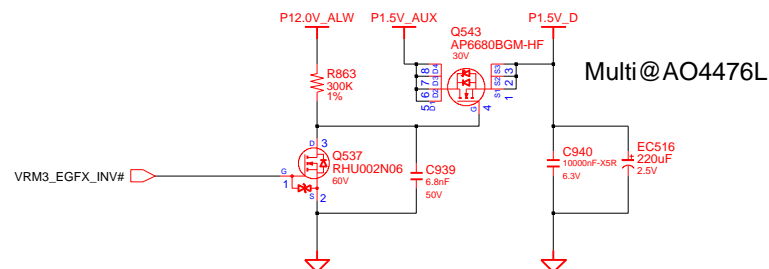
Discrete Switched Power (D1.05V : Max 3.6A)



Discrete Switched Power (D1.8V : Max 0.5A)



Discrete Switched Power (D1.5V : Max 5.0A)



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DRAW	MS YANG	DATE	5/10/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	Switched PWR 2		
APPROVAL	BL LEE	REV	rev. 1.0	FOR OPTIMUS PWR	PART NO.	
MODULE CODE		LAST EDIT			BA41-01432A	
November 22, 2010 15:53:34 PM						PAGE 52 OF 52