Schematics Page Index (Title / Revision / Change Date)

P. Leader	Check by	Design by

Project Code & Schematics Subject: MS10 Main Board

PCB P/N: 1P-005C100-8011(FUBAI)
1P-005C500-8011(HANSTAR)
1P-005C200-8011(NAB YA)

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

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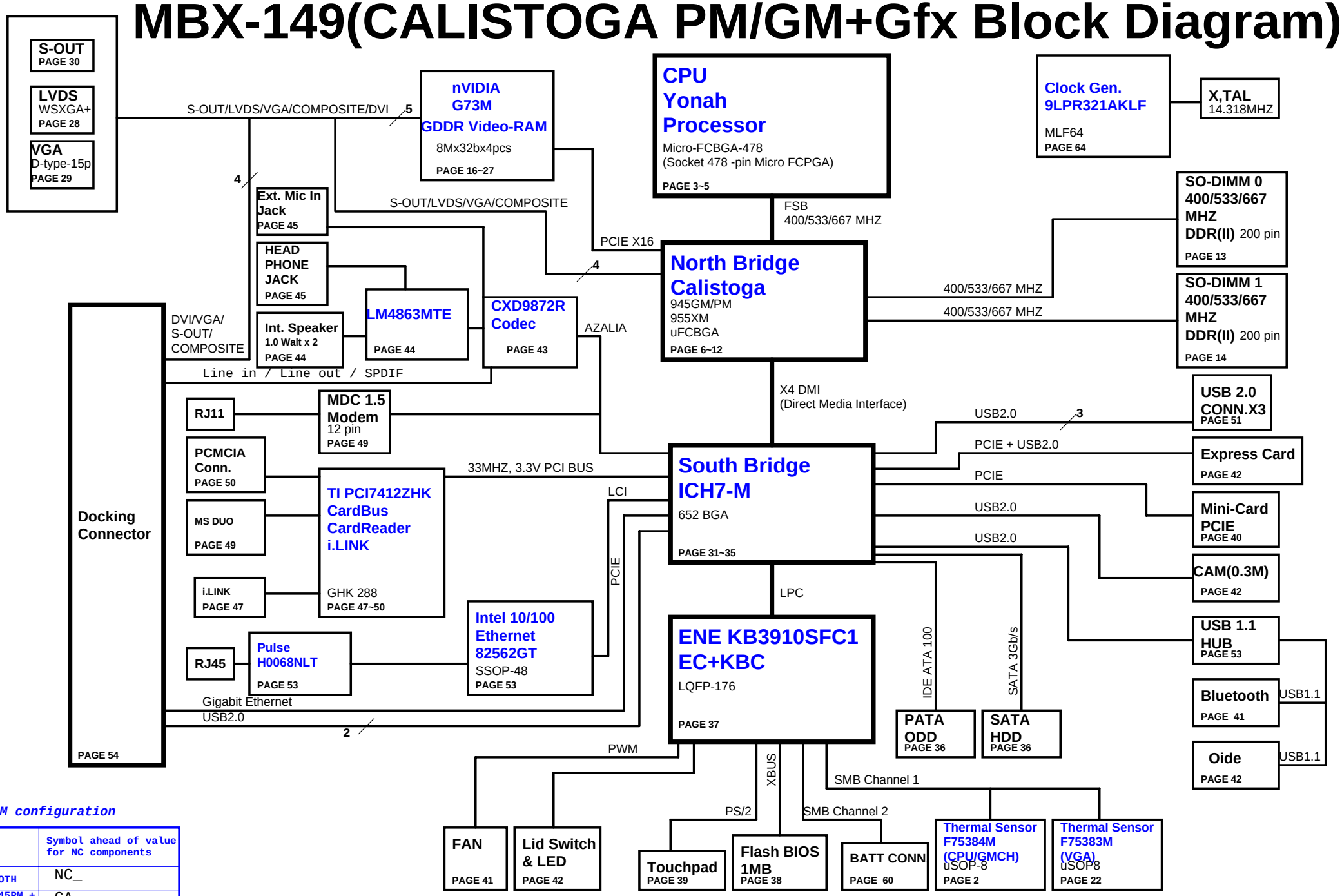
MBX-149(CALISTOGA PM/GM+Gfx Block Diagram)



BOM configuration

	Symbol ahead of value for NC components
BOTH	NC_
945PM + NV43M	CA_
945GM	NV_

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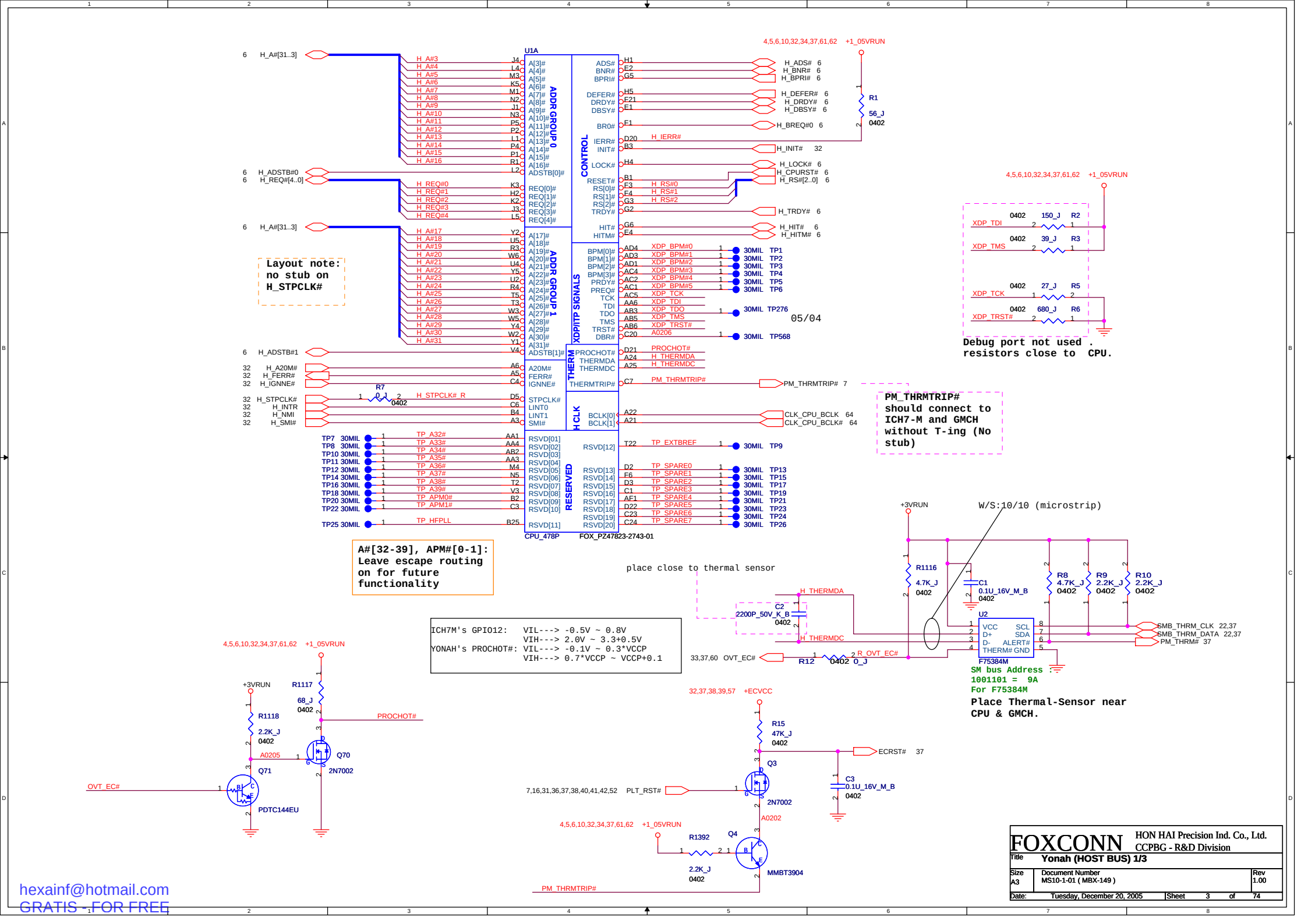

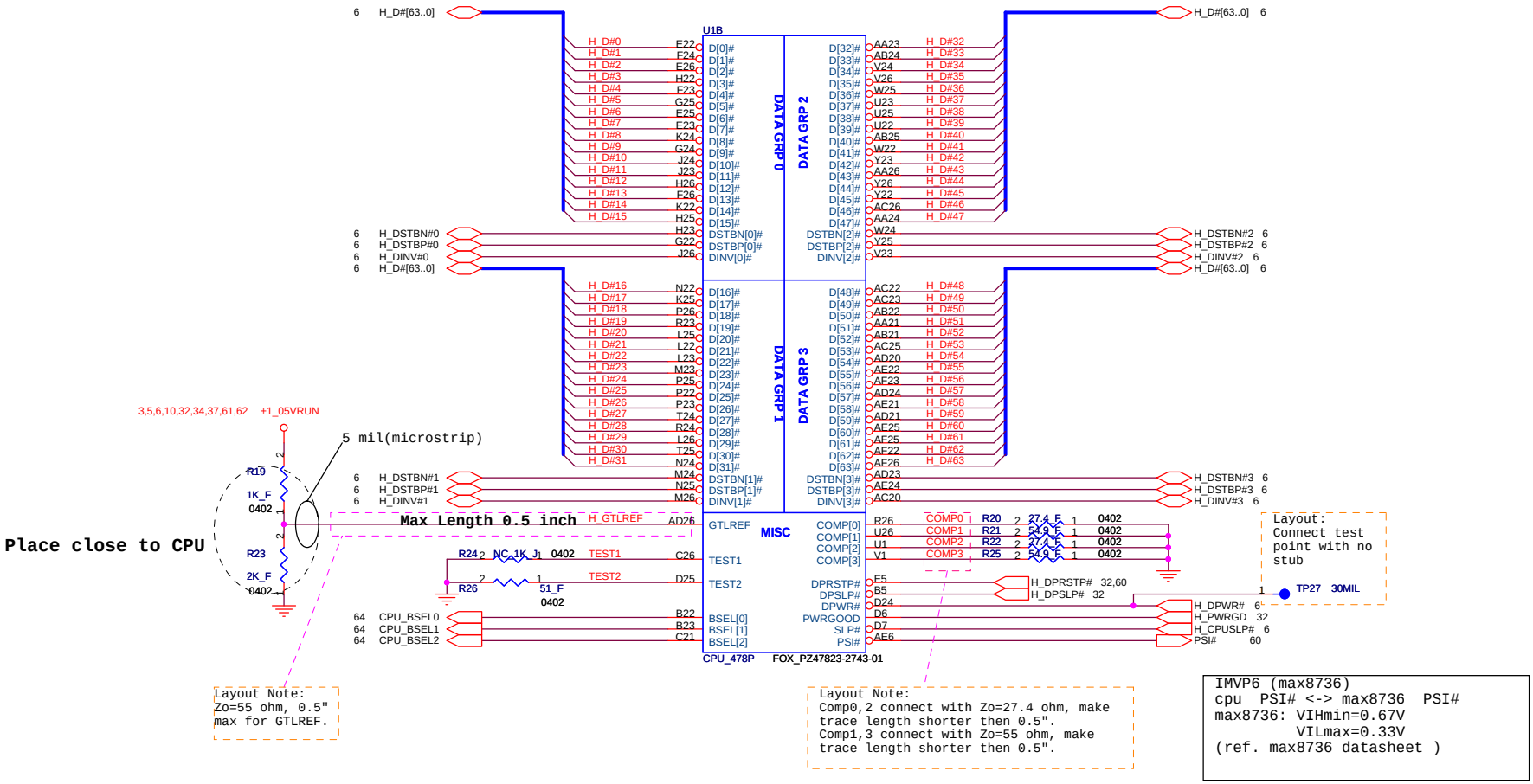

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Yonah (HOST BUS) 2/3		
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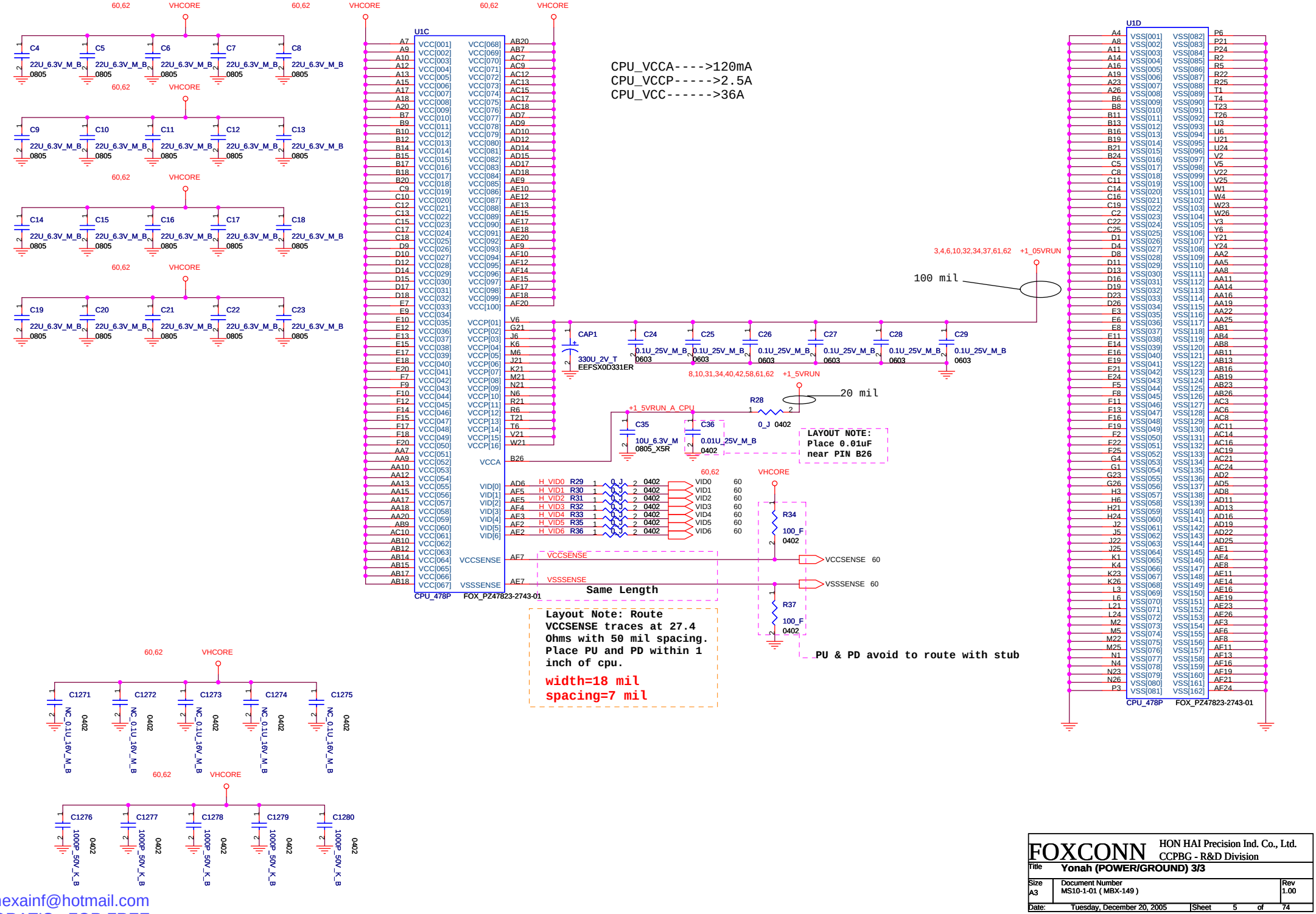

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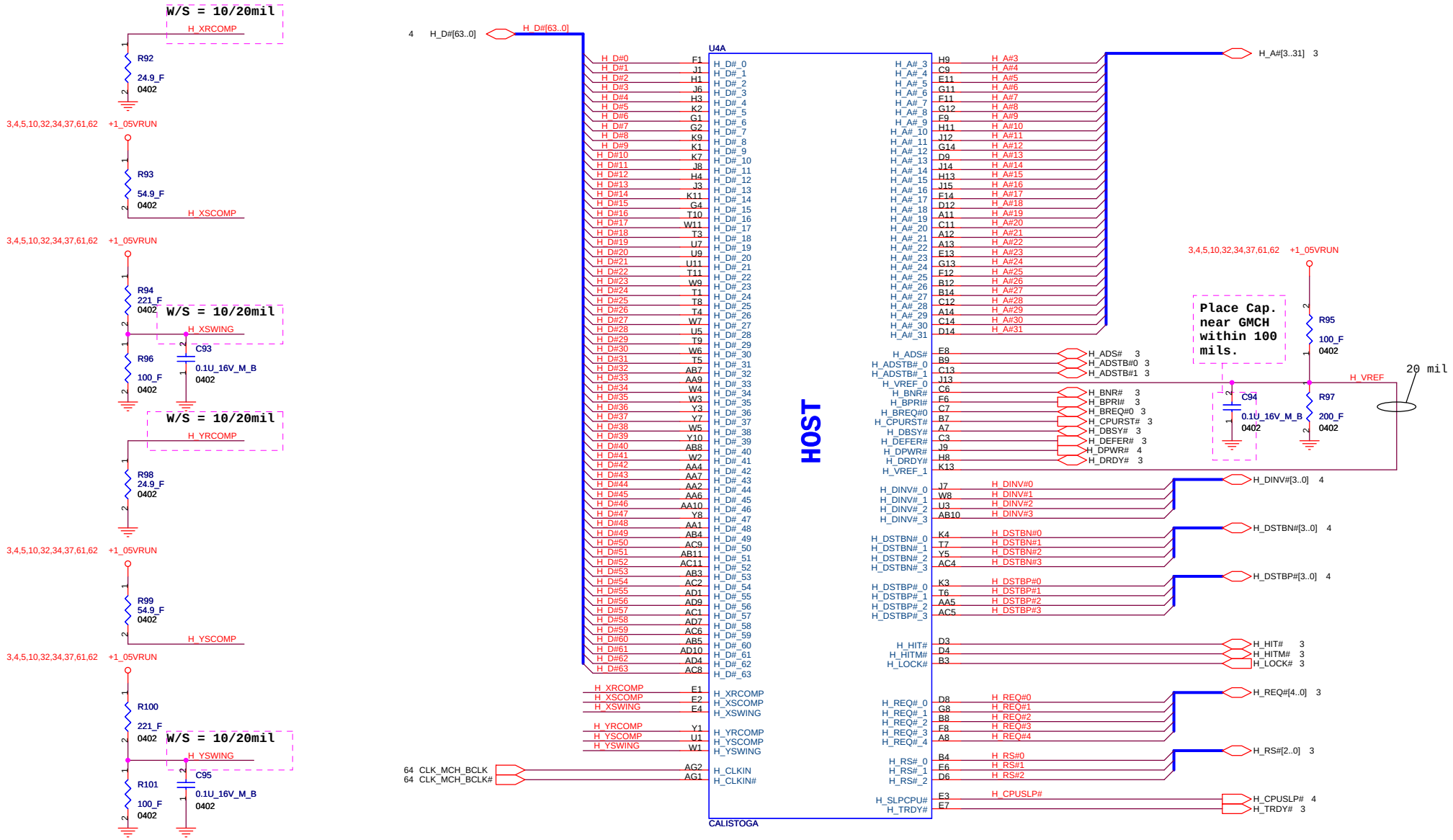

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Title	CALISTOGA (HOST) 1 of 7	
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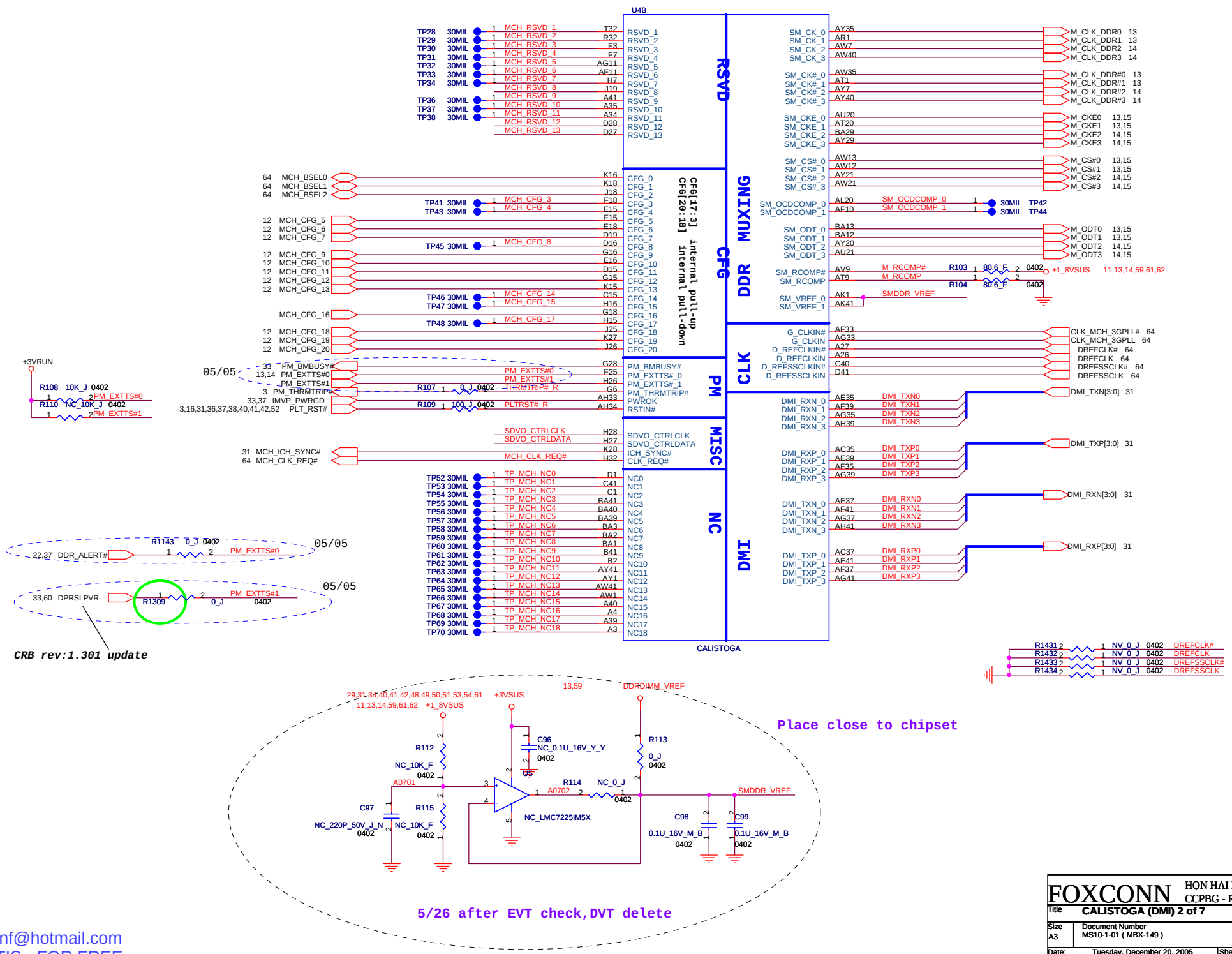

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Title	CALISTOGA (DMI) 2 of 7		
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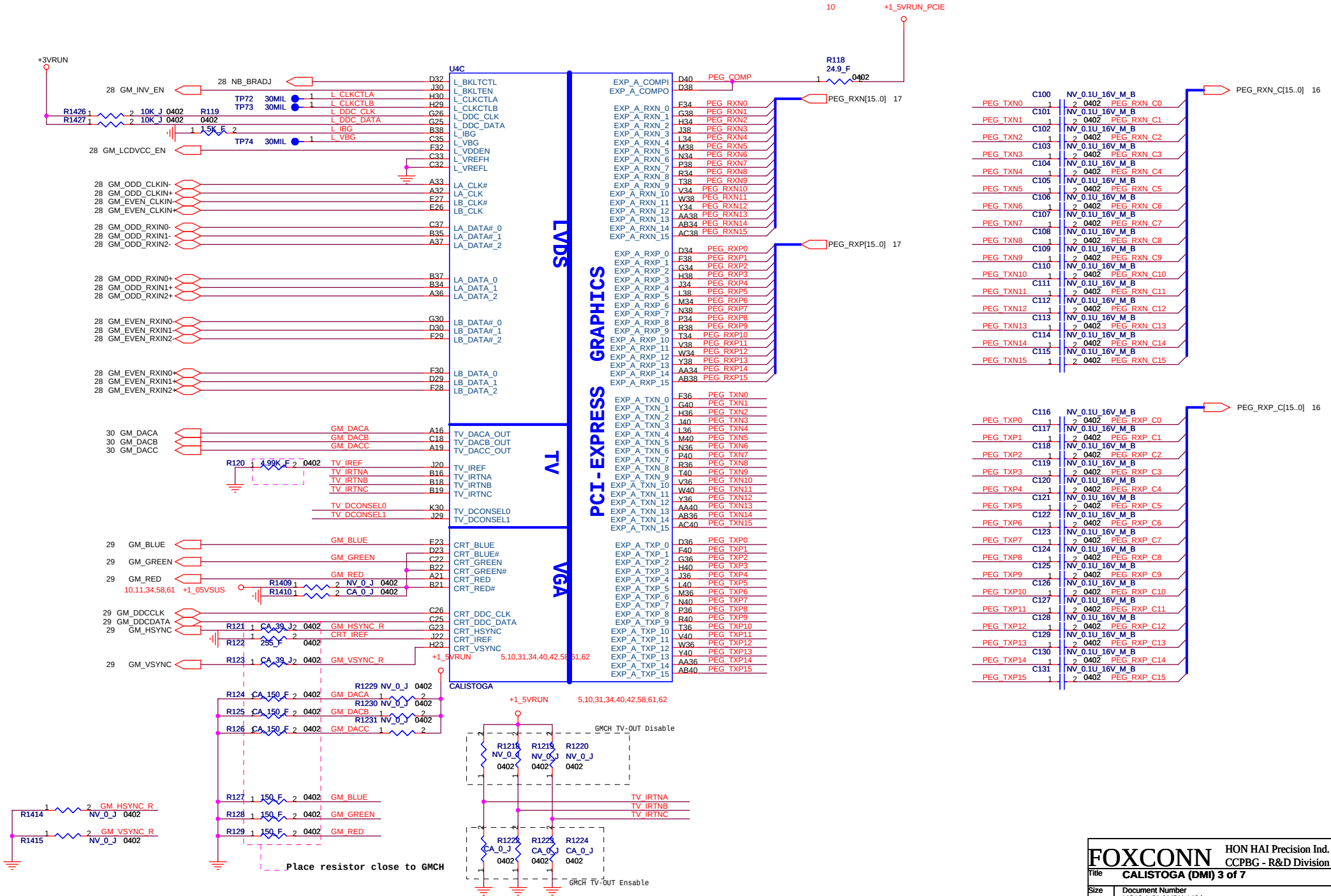

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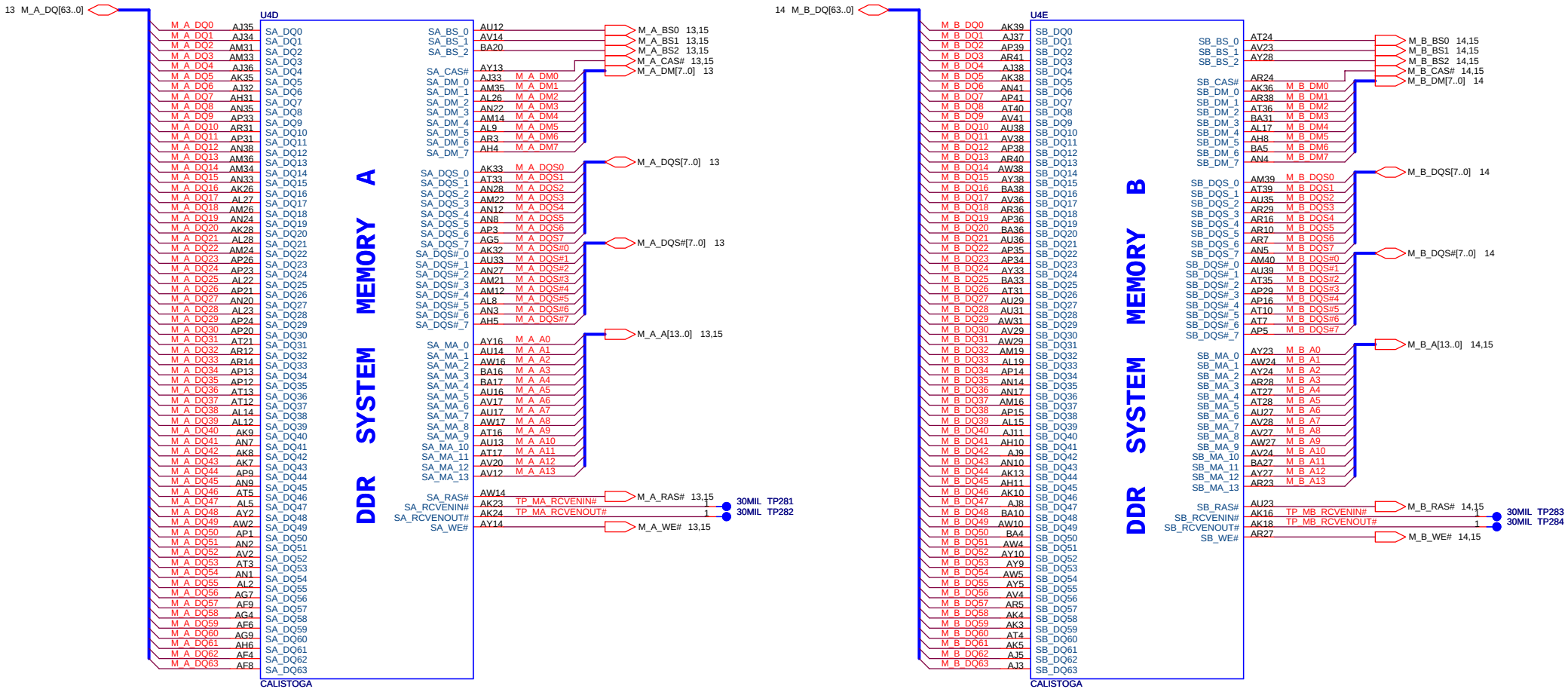

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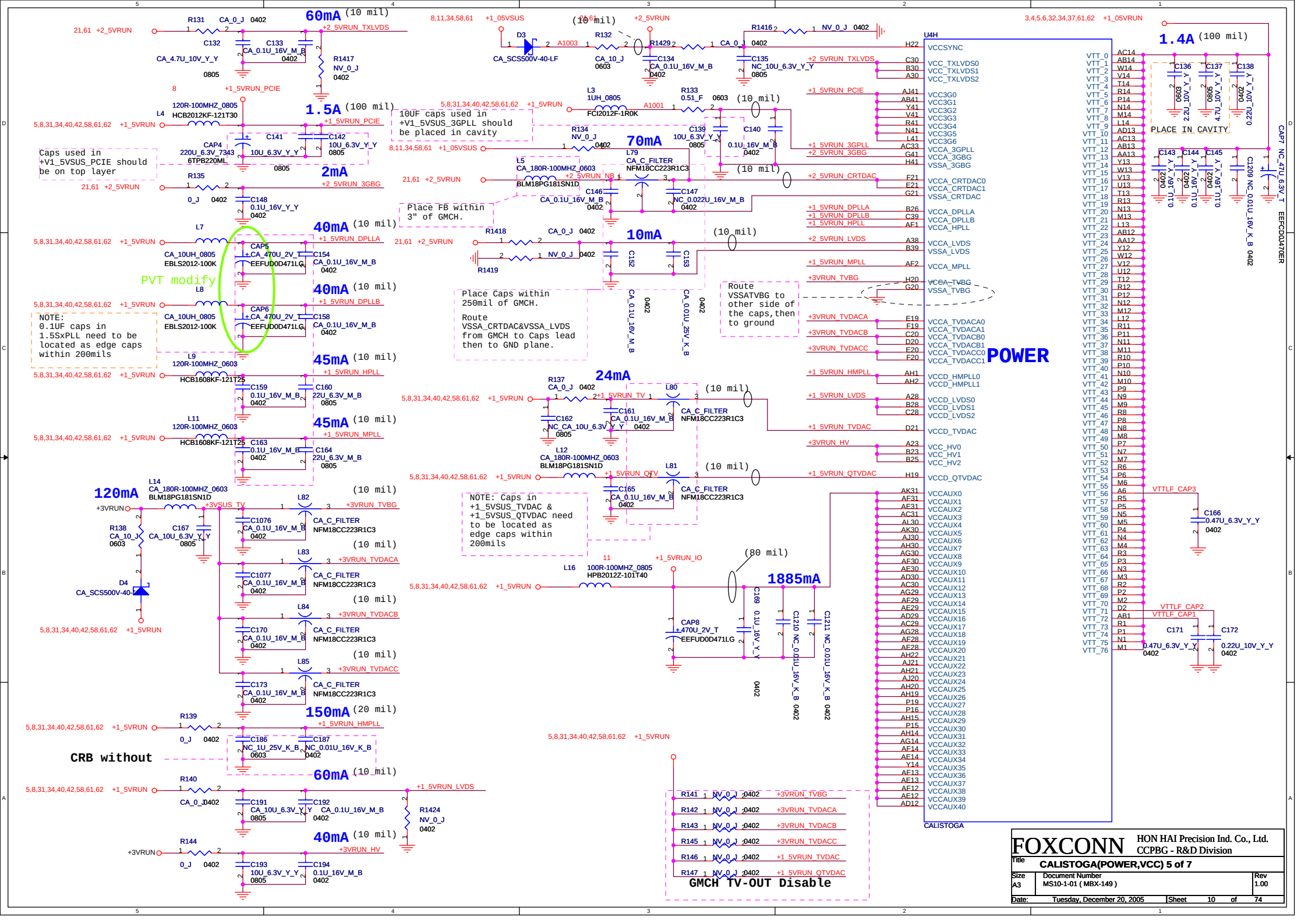
60mA (10 mil)
1.5A (100 mil)
2mA
40mA (10 mil)
40mA (10 mil)
45mA (10 mil)
45mA (10 mil)
120mA
(10 mil)
(10 mil)
(10 mil)
(10 mil)
150mA (20 mil)
CRB without
60mA (10 mil)
40mA (10 mil)
70mA
(10 mil)
(10 mil)
10mA
(10 mil)
24mA
(10 mil)
(10 mil)
(80 mil)
1885mA
1.4A (100 mil)
PLACE IN CAVITY
GMCH TV-OUT Disable
POWER
CALISTOGA
10UF caps used in +V1_5VSUS_3GPLL should be placed in cavity
Caps used in +V1_5VSUS_PCIE should be on top layer
Place FB within 3" of GMCH.
Place Caps within 250mil of GMCH.
Route VSSA_CRTDAC&VSSA_LVDS from GMCH to Caps lead then to GND plane.
Route VSSATVBG to other side of the caps,then to ground
PVT modify
NOTE: 0.1UF caps in 1.5SxPLL need to be located as edge caps within 200mils
NOTE: Caps in +1_5VSUS_TVDAC & +1_5VSUS_QTVDAC need to be located as edge caps within 200mils
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Title: CALISTOGA(POWER,VCC) 5 of 7
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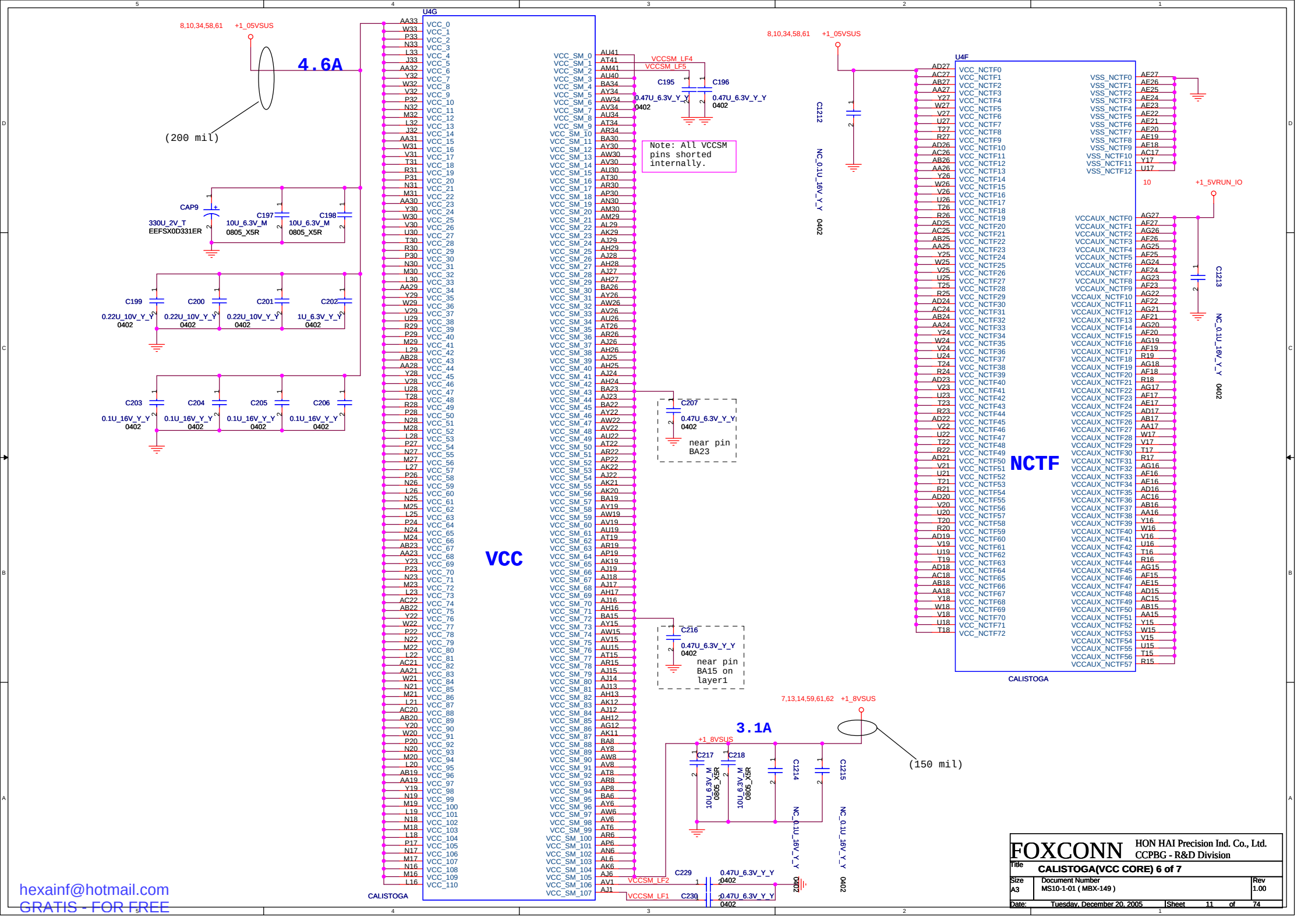

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Title	CALISTOGA(VCC CORE) 6 of 7	
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7 MCH_CFG_5 — 1 — 30MIL TP554

MCH_CFG_5	Low = DMIx2 High = DMIx4

7 MCH_CFG_6 — 1 — 30MIL TP556

MCH_CFG_6	Low = Moby Dick High = Calistoga

DDR2 select (default high)

7 MCH_CFG_7 — 1 — 30MIL TP557

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor

7 MCH_CFG_9 — 1 — 30MIL TP559

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

7 MCH_CFG_10 — 1 — 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY

7 MCH_CFG_11

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Calistoga High = Reserved

R162 NC_2.2K_J 0402

7 MCH_CFG_12 — 1 — 30MIL TP562
7 MCH_CFG_13 — 1 — 30MIL TP563

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

7 MCH_CFG_16

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V

7 MCH_CFG_18 — 1 — 30MIL TP555

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED

7 MCH_CFG_19 — 1 — 30MIL TP558

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 — 1 — 30MIL TP561

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

U4I

VSS

CALISTOGA

U4J

VSS

CALISTOGA

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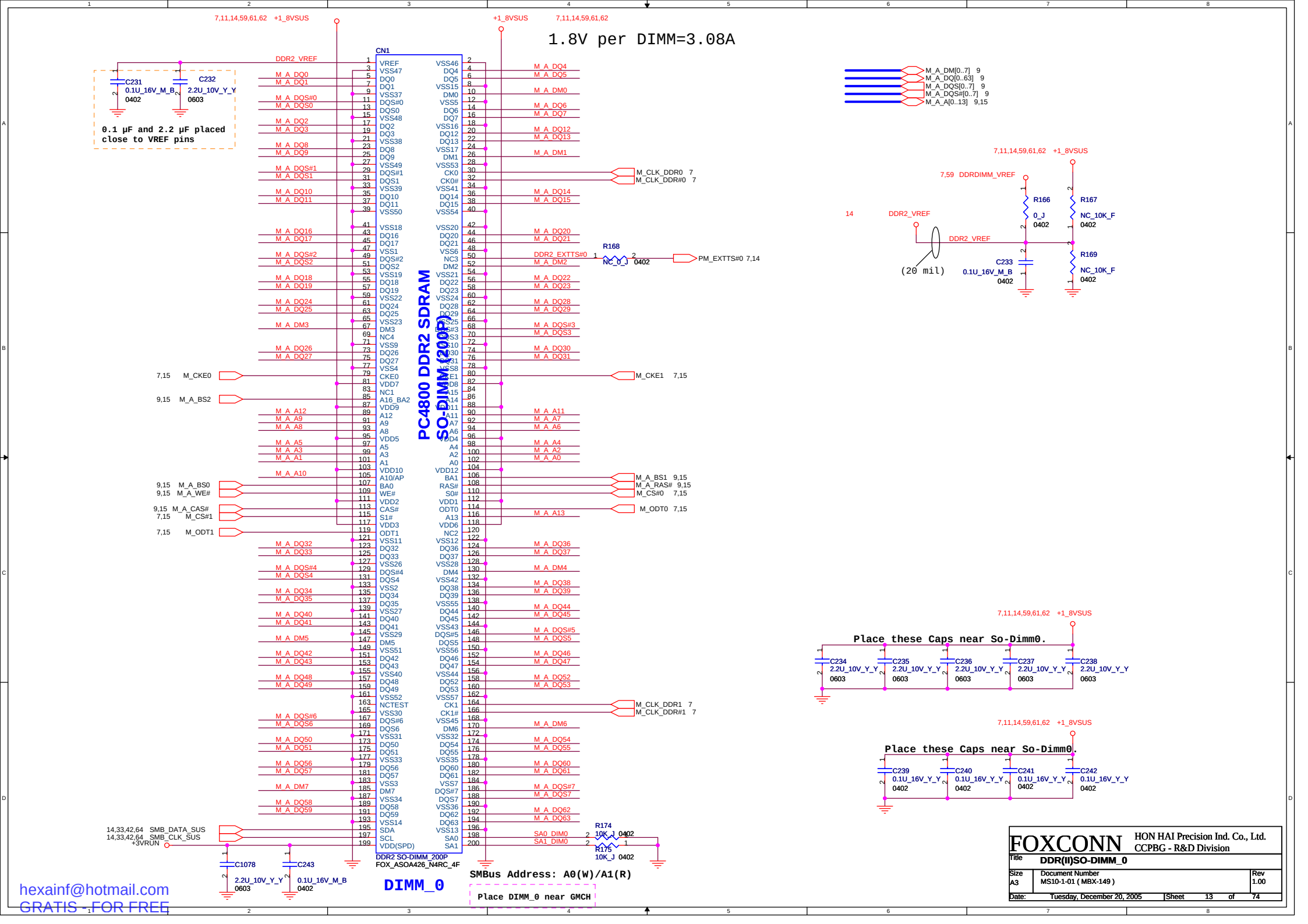

13

DDR2_VREF

7,11,13,59,61,62 +1_8VSUS

+1_8VSUS 7,11,13,59,61,62

1.8V per DIMM=3.08A

C244 0.1U_16V_M_B 0402

C245 2.2U_10V_Y_Y 0603

0.1 µF and 2.2 µF placed close to VREF pins

CN2

PC4800 DDR2 SDRAM SO-DIMM (200P)

1	VREF	VSS46	2				
3	VSS47	DQ4	4	M_B_DQ0	M_B_DQ4		
5	DQ0	DQ5	6	M_B_DQ1	M_B_DQ5		
7	DQ1	VSS15	8				
9	VSS37	DM0	10		M_B_DM0		
11	DQS#0	VSS5	12	M_B_DQS#0	M_B_DQ6		
13	DQS0	DQ6	14	M_B_DQS0	M_B_DQ7		
15	VSS48	DQ7	16				
17	DQ2	VSS16	18	M_B_DQ2	M_B_DQ12		
19	DQ3	DQ12	20	M_B_DQ3	M_B_DQ13		
21	VSS38	DQ13	22				
23	DQ8	VSS17	24	M_B_DQ8	M_B_DM1		
25	DQ9	DM1	26	M_B_DQ9			
27	VSS49	VSS53	28				
29	DQS#1	CK0	30	M_B_DQS#1	M_CLK_DDR3 7		
31	DQS1	CK0#	32	M_B_DQS1	M_CLK_DDR#3 7		
33	VSS39	VSS41	34				
35	DQ10	DQ14	36	M_B_DQ10	M_B_DQ14		
37	DQ11	DQ15	38	M_B_DQ11	M_B_DQ15		
39	VSS50	VSS54	40				
41	VSS18	VSS20	42				
43	DQ16	DQ20	44	M_B_DQ16	M_B_DQ20		
45	DQ17	DQ21	46	M_B_DQ17	M_B_DQ21		
47	VSS1	VSS6	48				
49	DQS#2	NC3	50	M_B_DQS#2	DDR2_EXTTS#1	R176 NC_0_J 0402	PM_EXTTS#0 7,13
51	DQS2	DM2	52	M_B_DQS2	M_B_DM2		
53	VSS19	VSS21	54				
55	DQ18	DQ22	56	M_B_DQ18	M_B_DQ22		
57	DQ19	DQ23	58	M_B_DQ19	M_B_DQ23		
59	VSS22	VSS24	60				
61	DQ24	DQ28	62	M_B_DQ24	M_B_DQ28		
63	DQ25	DQ29	64	M_B_DQ25	M_B_DQ29		
65	VSS23	VSS25	66				
67	DM3	DQS#3	68	M_B_DM3	M_B_DQS#3		
69	NC4	DQS3	70		M_B_DQS3		
71	VSS9	VSS10	72				
73	DQ26	DQ30	74	M_B_DQ26	M_B_DQ30		
75	DQ27	VSS31	76	M_B_DQ27	M_B_DQ31		
77	VSS4	VSS8	78				
79	CKE0	CKE1	80	7,15 M_CKE2	M_CKE3 7,15		
81	VDD7	VDD8	82				
83	NC1	A15	84				
85	A16_BA2	A14	86	9,15 M_B_BS2			
87	VDD9	A11	88				
89	A12	A11	90	M_B_A12	M_B_A11		
91	A9	A7	92	M_B_A9	M_B_A7		
93	A8	A6	94	M_B_A8	M_B_A6		
95	VDD5	VDD4	96				
97	A5	A4	98	M_B_A5	M_B_A4		
99	A3	A2	100	M_B_A3	M_B_A2		
101	A1	A0	102	M_B_A1	M_B_A0		
103	VDD10	VDD12	104				
105	A10/AP	BA1	106	M_B_A10	M_B_BS1 9,15		
107	BA0	RAS#	108	9,15 M_B_BS0	M_B_RAS# 9,15		
109	WE#	S0#	110	9,15 M_B_WE#	M_CS#2 7,15		
111	VDD2	VDD1	112				
113	CAS#	ODT0	114	9,15 M_B_CAS#	M_ODT2 7,15		
115	S1#	A13	116	7,15 M_CS#3	M_B_A13		
117	VDD3	VDD6	118				
119	ODT1	NC2	120	7,15 M_ODT3			
121	VSS11	VSS12	122				
123	DQ32	DQ36	124	M_B_DQ32	M_B_DQ36		
125	DQ33	DQ37	126	M_B_DQ33	M_B_DQ37		
127	VSS26	VSS28	128				
129	DQS#4	DM4	130	M_B_DQS#4	M_B_DM4		
131	DQS4	VSS42	132	M_B_DQS4			
133	VSS2	DQ38	134		M_B_DQ38		
135	DQ34	DQ39	136	M_B_DQ34	M_B_DQ39		
137	DQ35	VSS55	138	M_B_DQ35			
139	VSS27	DQ44	140		M_B_DQ44		
141	DQ40	DQ45	142	M_B_DQ40	M_B_DQ45		
143	DQ41	VSS43	144	M_B_DQ41			
145	VSS29	DQS#5	146		M_B_DQS#5		
147	DM5	DQS5	148	M_B_DM5	M_B_DQS5		
149	VSS51	VSS56	150				
151	DQ42	DQ46	152	M_B_DQ42	M_B_DQ46		
153	DQ43	DQ47	154	M_B_DQ43	M_B_DQ47		
155	VSS40	VSS44	156				
157	DQ48	DQ52	158	M_B_DQ48	M_B_DQ52		
159	DQ49	DQ53	160	M_B_DQ49	M_B_DQ53		
161	VSS52	VSS57	162				
163	NCTEST	CK1	164		M_CLK_DDR2 7		
165	VSS30	CK1#	166		M_CLK_DDR#2 7		
167	DQS#6	VSS45	168	M_B_DQS#6			
169	DQS6	DM6	170	M_B_DQS6	M_B_DM6		
171	VSS31	VSS32	172				
173	DQ50	DQ54	174	M_B_DQ50	M_B_DQ54		
175	DQ51	DQ55	176	M_B_DQ51	M_B_DQ55		
177	VSS33	VSS35	178				
179	DQ56	DQ60	180	M_B_DQ56	M_B_DQ60		
181	DQ57	DQ61	182	M_B_DQ57	M_B_DQ61		
183	VSS3	VSS7	184				
185	DM7	DQS#7	186	M_B_DM7	M_B_DQS#7		
187	VSS34	DQS7	188		M_B_DQS7		
189	DQ58	VSS36	190	M_B_DQ58			
191	DQ59	DQ62	192	M_B_DQ59	M_B_DQ62		
193	VSS14	DQ63	194		M_B_DQ63		
195	SDA	VSS13	196	13,33,42,64 SMB_DATA_SUS			
197	SCL	SA0	198	13,33,42,64 SMB_CLK_SUS	SA0_DIM1	R177 10K_J 0402	
199	VDD(SPD)	SA1	200	+3VRUN	SA1_DIM1	0402	+3VRUN

DDR2 S0-DIMM_200P

FOX_ASOA426_N4SC_4F

R178 10K_J

C1079 2.2U_10V_Y_Y 0603

C255 0.1U_16V_M_B 0402

DIMM_1

SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0

M_B_DM[0..7] 9
M_B_DQ[0..63] 9
M_B_DQS[0..7] 9
M_B_DQS#[0..7] 9
M_B_A[0..13] 9,15

7,11,13,59,61,62 +1_8VSUS

Place these Caps near So-Dimm1.

C246 2.2U_10V_Y_Y 0603
C247 2.2U_10V_Y_Y 0603
C248 2.2U_10V_Y_Y 0603
C249 2.2U_10V_Y_Y 0603
C250 2.2U_10V_Y_Y 0603

7,11,13,59,61,62 +1_8VSUS

Place these Caps near So-Dimm1.

C251 0.1U_16V_Y_Y 0402
C252 0.1U_16V_Y_Y 0402
C253 0.1U_16V_Y_Y 0402
C254 0.1U_16V_Y_Y 0402

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Title: DDR(II)SO-DIMM_1

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9,13 M_A_A[0..13]

9,14 M_B_A[0..13]

59,62 +0_9VSUS

C257 C258 C259 C260 C261 C262 C263 C264 C265 C266 C267 C268 C269
0.1U_16V_Y_X
0402

Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

59,62 +0_9VSUS

C270 C271 C272 C273 C274 C275 C276 C277 C278 C279 C280 C281 C282
0.1U_16V_Y_X
0402

Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

9,14 M_B_RAS#
9,14 M_B_BS1
RP12 4 3 1 2 56 0404_4P2R
M_B_A12 M_B_A9 RP13 0404_4P2R
M_B_A8 M_B_A5 RP14 0404_4P2R

+0_9VSUS 59,62

M_B_A3 M_B_A1 RP15 0404_4P2R
M_B_A10 RP16 0404_4P2R
9,14 M_B_BS0
9,14 M_B_WE#
9,14 M_B_CAS#
RP17 0404_4P2R
M_B_A7 M_B_A11 RP18 0404_4P2R

+0_9VSUS 59,62

M_B_A4 M_B_A6 RP19 0404_4P2R
M_B_A0 M_B_A2 RP20 0404_4P2R
7,14 M_ODT2
M_B_A13 RP21 0404_4P2R

+0_9VSUS 59,62

M_A_A7 M_A_A11 RP22 0404_4P2R
M_A_A4 M_A_A6 RP23 0404_4P2R
9,13 M_A_RAS#
9,13 M_A_BS1
RP24 0404_4P2R

+0_9VSUS 59,62

M_A_A13 RP25 0404_4P2R
7,13 M_ODT0
9,13 M_A_BS2
RP26 0404_4P2R
M_A_A12
M_A_A9 M_A_A8 RP27 0404_4P2R
M_A_A5 M_A_A3 RP28 0404_4P2R

+0_9VSUS 59,62

M_A_A10 RP29 0404_4P2R
9,13 M_A_BS0
9,13 M_A_WE#
9,13 M_A_CAS#
RP30 0404_4P2R
M_A_A0 M_A_A2 RP31 0404_4P2R

+0_9VSUS 59,62

7,13 M_CKE0 R183 0402 56_J
7,13 M_CKE1 R186 0402 56_J
7,14 M_CKE2 R189 0402 56_J
7,14 M_CKE3 R192 0402 56_J

+0_9VSUS 59,62

7,13 M_CS#0 R181 0402 56_J
7,13 M_CS#1 R184 0402 56_J
7,14 M_CS#2 R187 0402 56_J
7,14 M_CS#3 R190 0402 56_J

+0_9VSUS 59,62

7,13 M_ODT1 R182 0402 56_J
7,14 M_ODT3 R185 0402 56_J
M_A_A1 R188 0402 56_J
9,14 M_B_BS2 R191 0402 56_J

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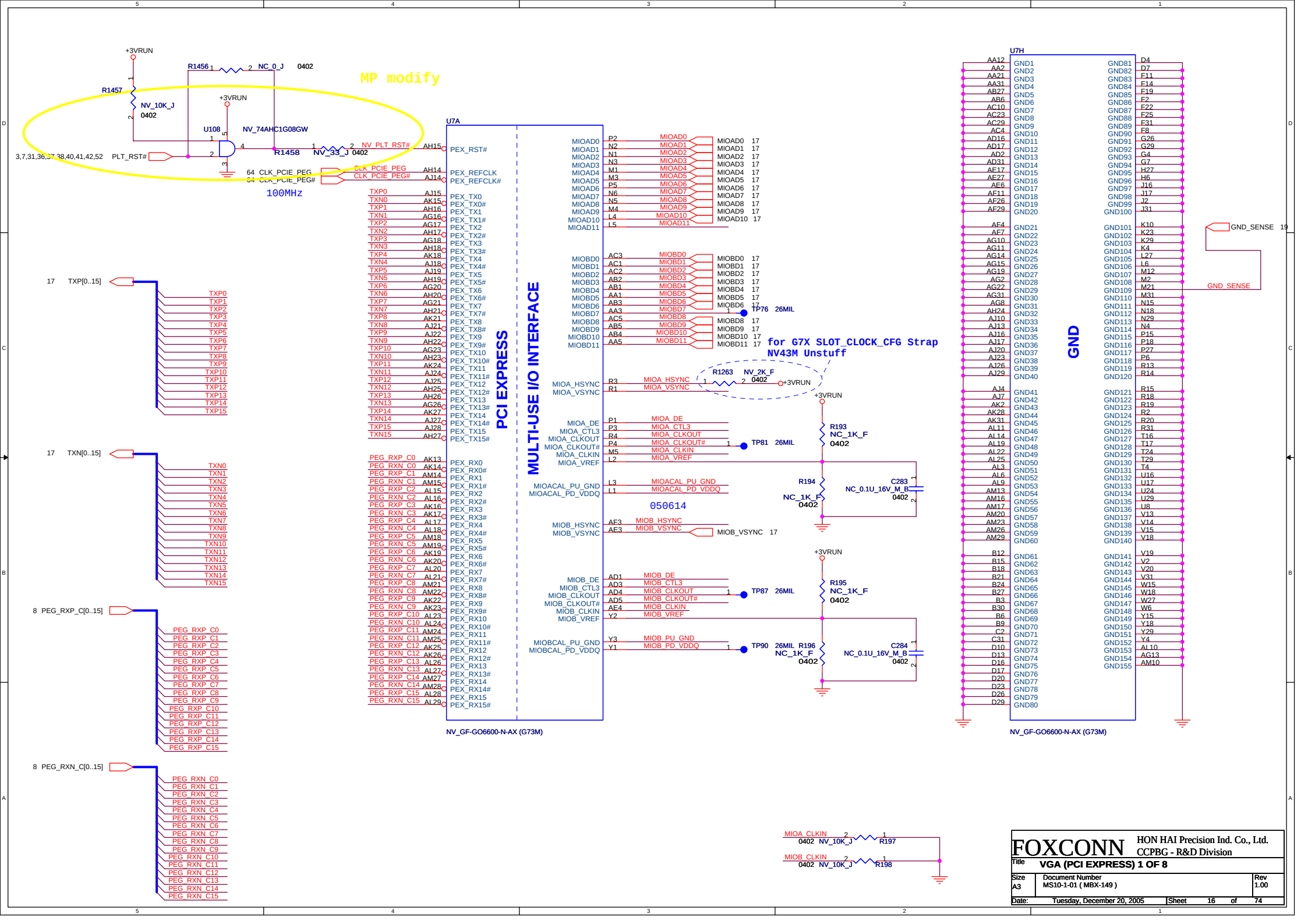

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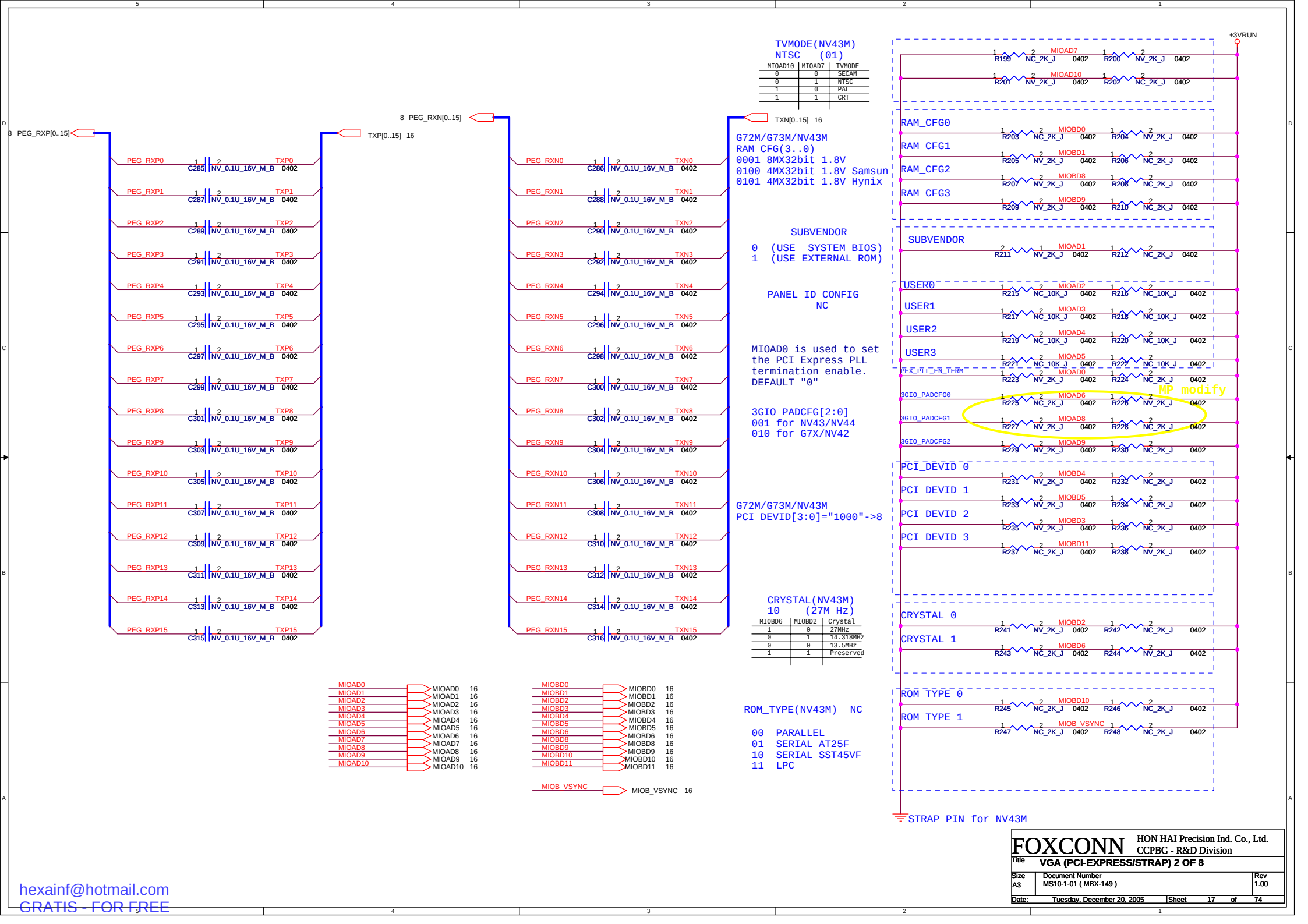

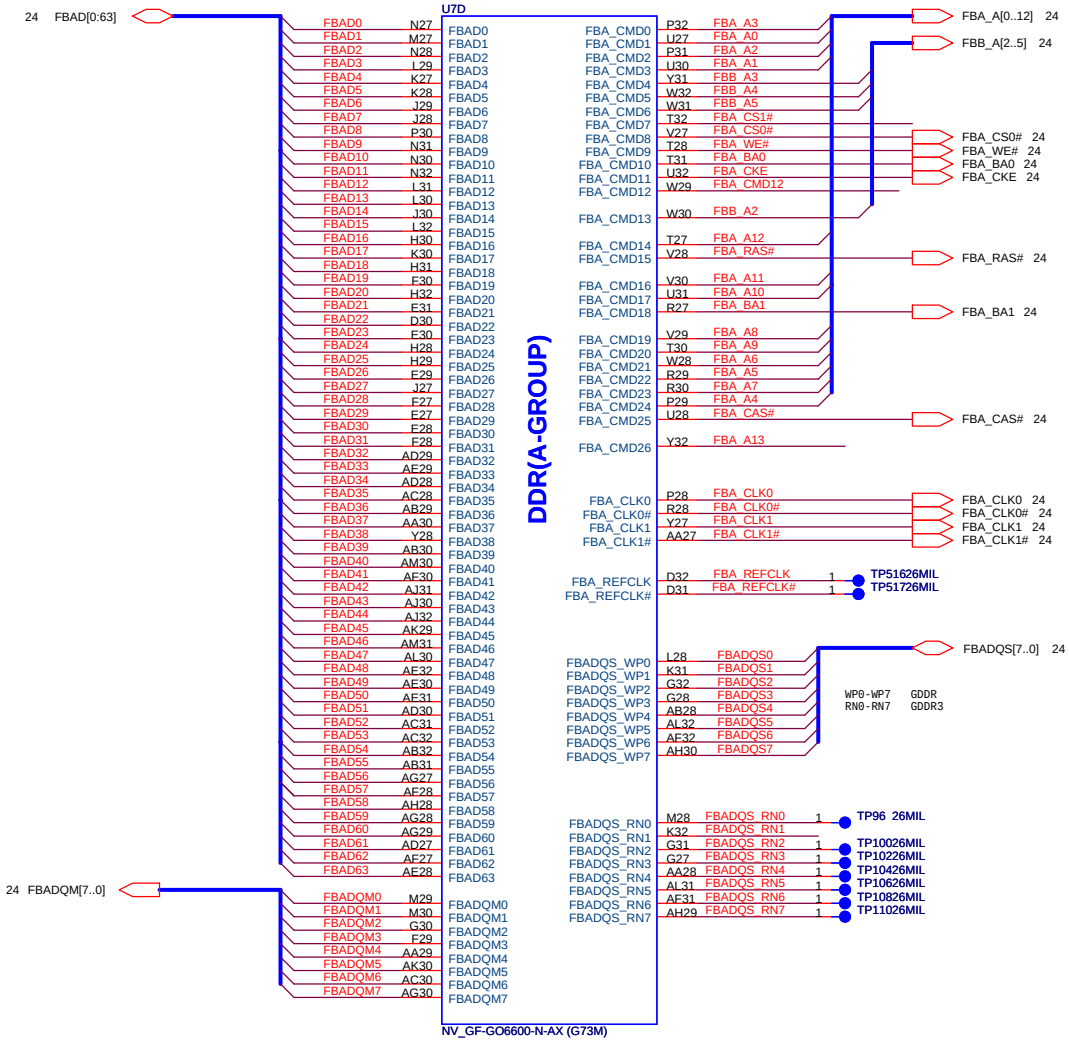

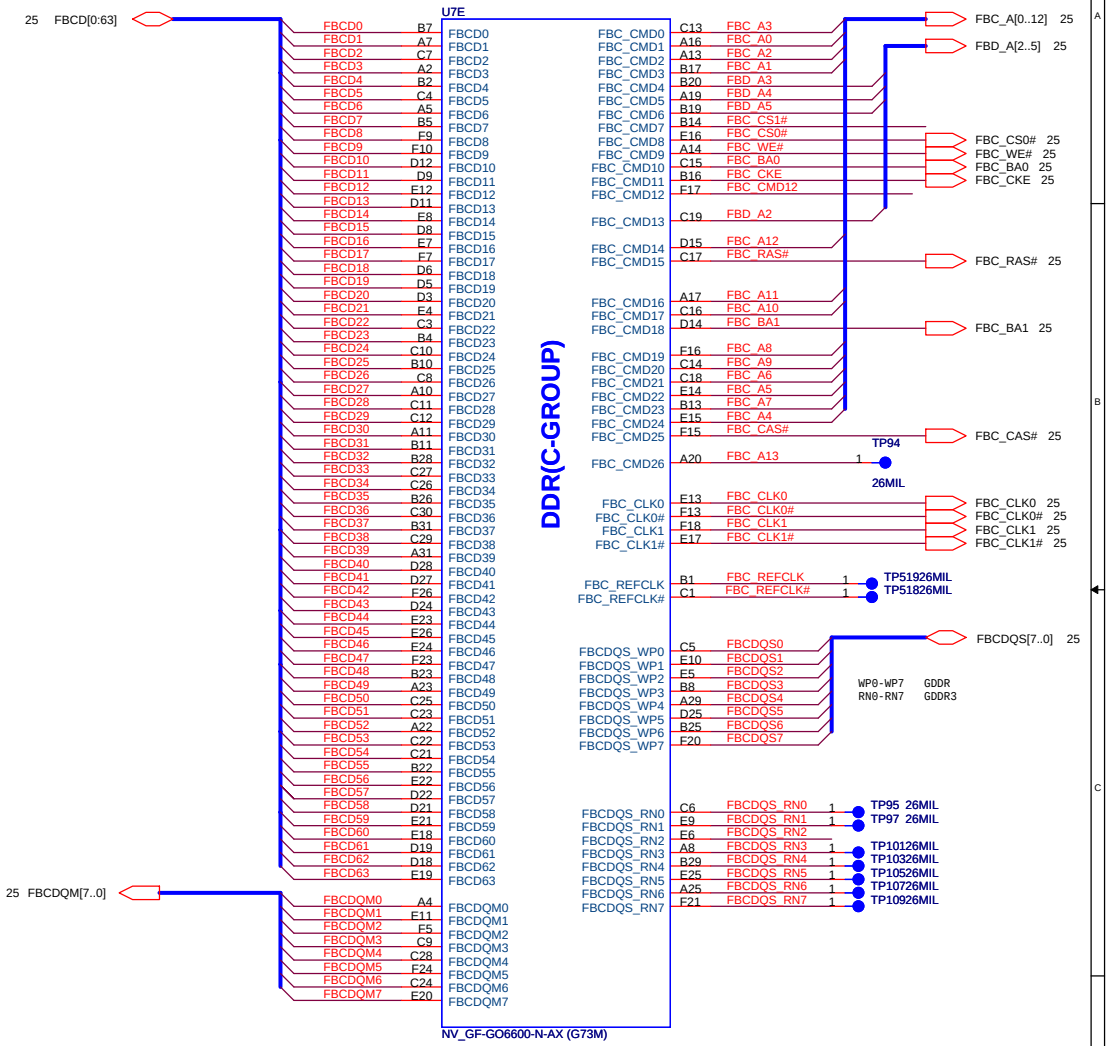

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	VGA (GDDR) 3 OF 8		
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
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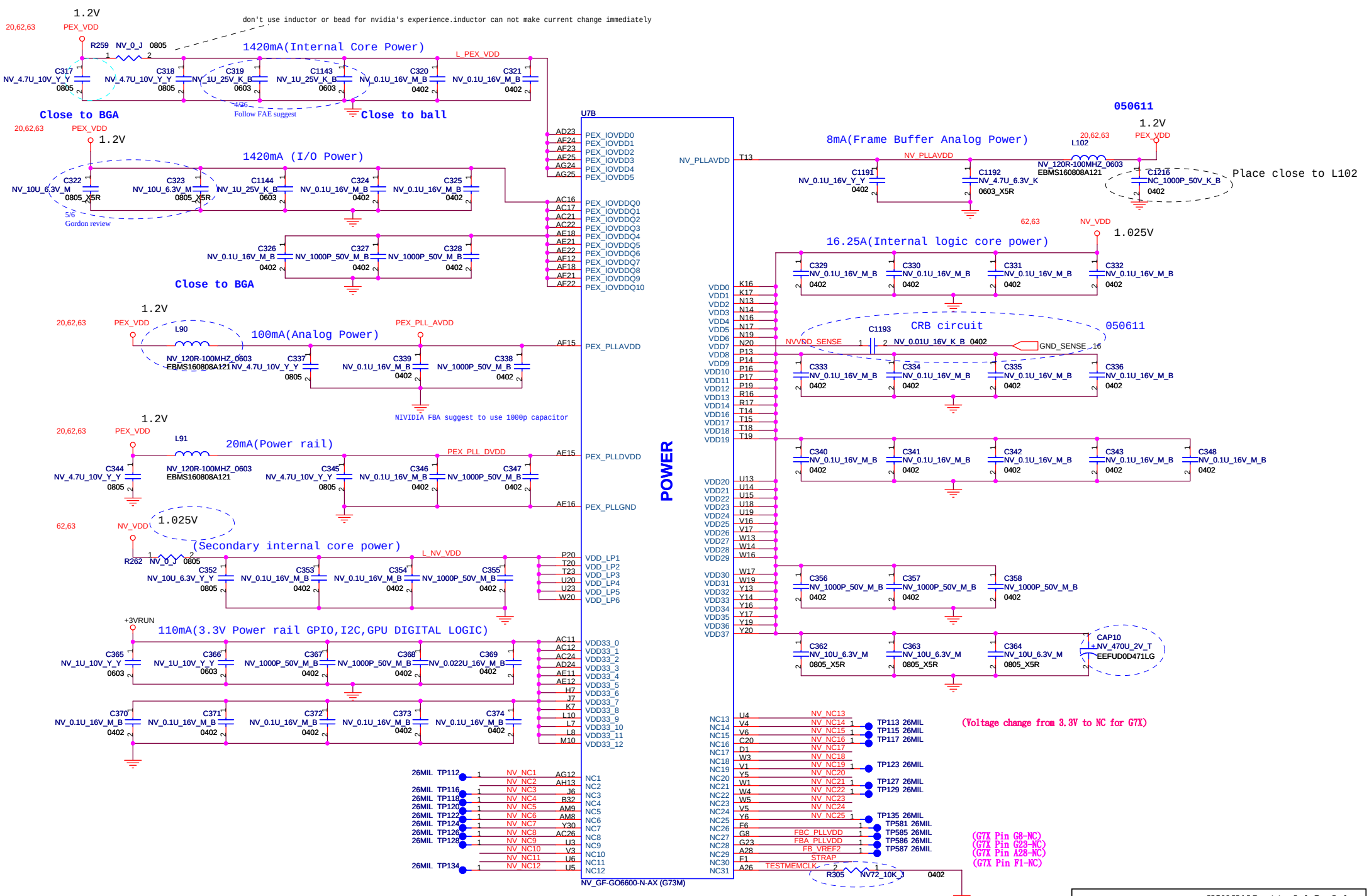
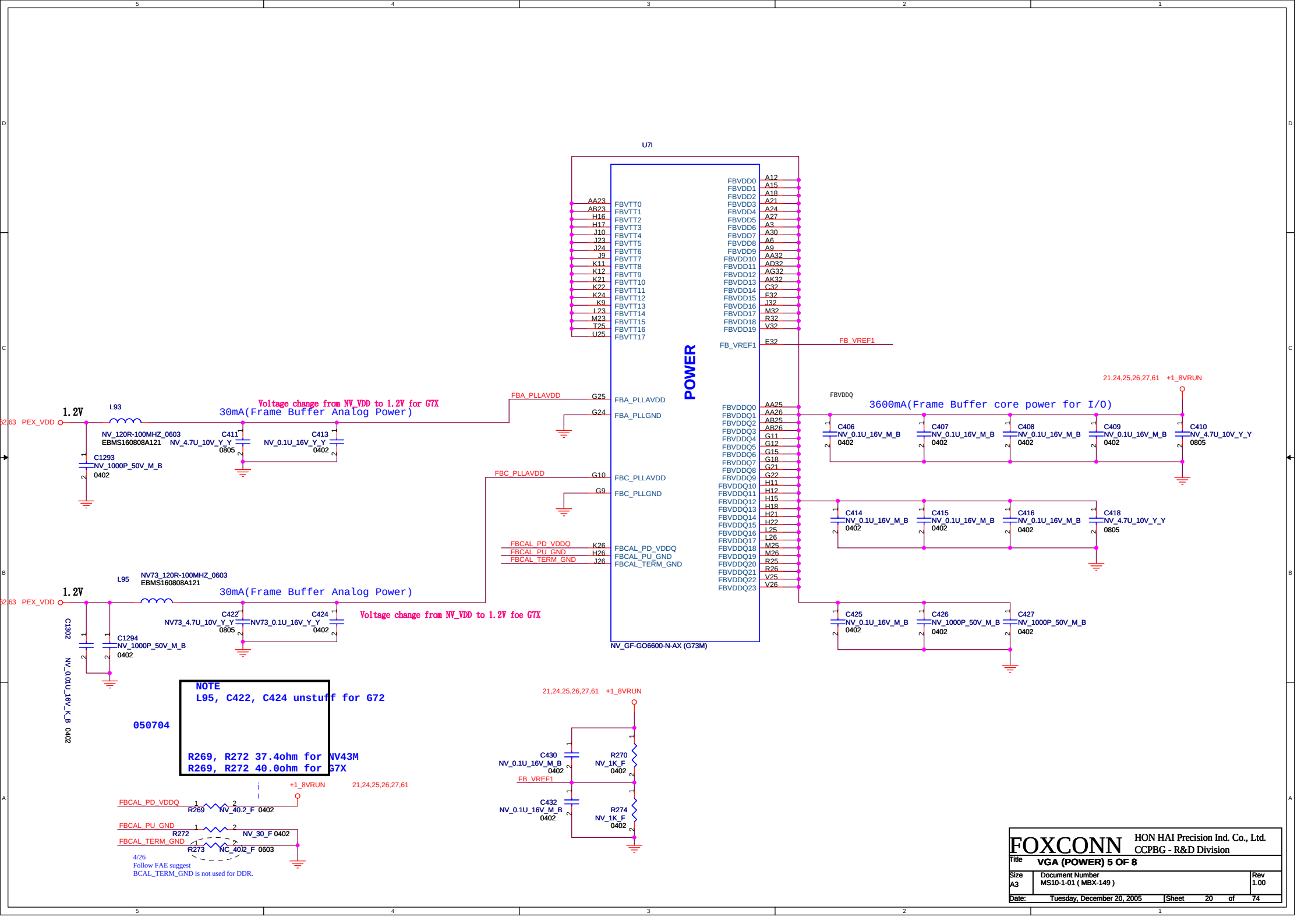


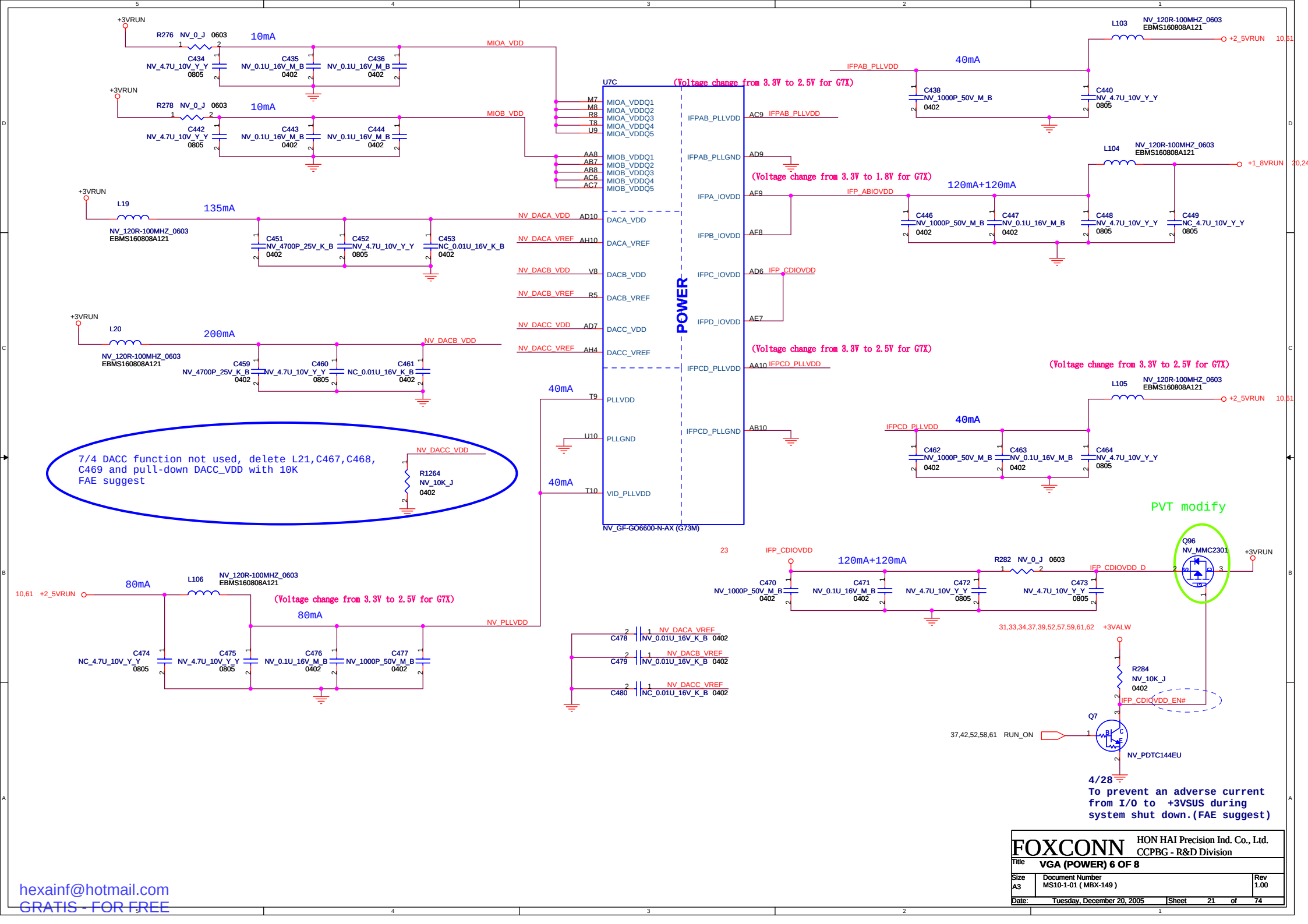
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VGA (GDDR/I2C/ROM) 4 OF 8	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 19 of 74	



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VGA (POWER) 5 OF 8	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 20 of 74	


+3VRUN
R276 NV_0_J 0603
10mA
C434 NV_4.7U_10V_Y_Y 0805
C435 NV_0.1U_16V_M_B 0402
C436 NV_0.1U_16V_M_B 0402
MIOA_VDD
R278 NV_0_J 0603
10mA
C442 NV_4.7U_10V_Y_Y 0805
C443 NV_0.1U_16V_M_B 0402
C444 NV_0.1U_16V_M_B 0402
MIOB_VDD
L19
135mA
NV_120R-100MHZ_0603 EBMS160808A121
C451 NV_4700P_25V_K_B 0402
C452 NV_4.7U_10V_Y_Y 0805
C453 NC_0.01U_16V_K_B 0402
NV_DACA_VDD
L20
200mA
NV_120R-100MHZ_0603 EBMS160808A121
C459 NV_4700P_25V_K_B 0402
C460 NV_4.7U_10V_Y_Y 0805
C461 NC_0.01U_16V_K_B 0402
NV_DACB_VDD
7/4 DACC function not used, delete L21,C467,C468, C469 and pull-down DACC_VDD with 10K FAE suggest
NV_DACC_VDD
R1264 NV_10K_J 0402
U7C
M7 M8 R8 T8 U9 MIOA_VDDQ1 MIOA_VDDQ2 MIOA_VDDQ3 MIOA_VDDQ4 MIOA_VDDQ5
AA8 AB7 AB8 AC6 AC7 MIOB_VDDQ1 MIOB_VDDQ2 MIOB_VDDQ3 MIOB_VDDQ4 MIOB_VDDQ5
NV_DACA_VDD AD10 DACA_VDD
NV_DACA_VREF AH10 DACA_VREF
NV_DACB_VDD V8 DACB_VDD
NV_DACB_VREF R5 DACB_VREF
NV_DACC_VDD AD7 DACC_VDD
NV_DACC_VREF AH4 DACC_VREF
T9 PLLVDD
U10 PLLGND
T10 VID_PLLVDD
POWER
(Voltage change from 3.3V to 2.5V for G7X)
IFPAB_PLLVDD AC9 IFPAB_PLLVDD
IFPAB_PLLGND AD9
(Voltage change from 3.3V to 1.8V for G7X)
IFPA_IOVDD AF9 IFP_ABIOVDD
IFPB_IOVDD AF8
IFPC_IOVDD AD6 IFP_CDIOVDD
IFPD_IOVDD AE7
(Voltage change from 3.3V to 2.5V for G7X)
IFPCD_PLLVDD AA10 IFPCD_PLLVDD
IFPCD_PLLGND AB10
NV_GF-GO6600-N-AX (G73M)
40mA
40mA
40mA
L103 NV_120R-100MHZ_0603 EBMS160808A121
+2_5VRUN 10,61
IFPAB_PLLVDD
40mA
C438 NV_1000P_50V_M_B 0402
C440 NV_4.7U_10V_Y_Y 0805
L104 NV_120R-100MHZ_0603 EBMS160808A121
+1_8VRUN 20,24
120mA+120mA
C446 NV_1000P_50V_M_B 0402
C447 NV_0.1U_16V_M_B 0402
C448 NV_4.7U_10V_Y_Y 0805
C449 NC_4.7U_10V_Y_Y 0805
(Voltage change from 3.3V to 2.5V for G7X)
L105 NV_120R-100MHZ_0603 EBMS160808A121
+2_5VRUN 10,61
IFPCD_PLLVDD
40mA
C462 NV_1000P_50V_M_B 0402
C463 NV_0.1U_16V_M_B 0402
C464 NV_4.7U_10V_Y_Y 0805
PVT modify
Q96 NV_MMC2301
+3VRUN
23 IFP_CDIOVDD
120mA+120mA
C470 NV_1000P_50V_M_B 0402
C471 NV_0.1U_16V_M_B 0402
C472 NV_4.7U_10V_Y_Y 0805
C473 NV_4.7U_10V_Y_Y 0805
R282 NV_0_J 0603
IFP_CDIOVDD_D
31,33,34,37,39,52,57,59,61,62 +3VALW
R284 NV_10K_J 0402
IFP_CDIOVDD_EN#
Q7
37,42,52,58,61 RUN_ON
NV_PDTC144EU
4/28
To prevent an adverse current from I/O to +3VSUS during system shut down.(FAE suggest)
10,61 +2_5VRUN
80mA
L106 NV_120R-100MHZ_0603 EBMS160808A121
(Voltage change from 3.3V to 2.5V for G7X)
80mA
C474 NC_4.7U_10V_Y_Y 0805
C475 NV_4.7U_10V_Y_Y 0805
C476 NV_0.1U_16V_M_B 0402
C477 NV_1000P_50V_M_B 0402
NV_PLLVDD
C478 NV_0.01U_16V_K_B 0402 NV_DACA_VREF
C479 NV_0.01U_16V_K_B 0402 NV_DACB_VREF
C480 NC_0.01U_16V_K_B 0402 NV_DACC_VREF
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title VGA (POWER) 6 OF 8
Size A3
Document Number MS10-1-01 (MBX-149)
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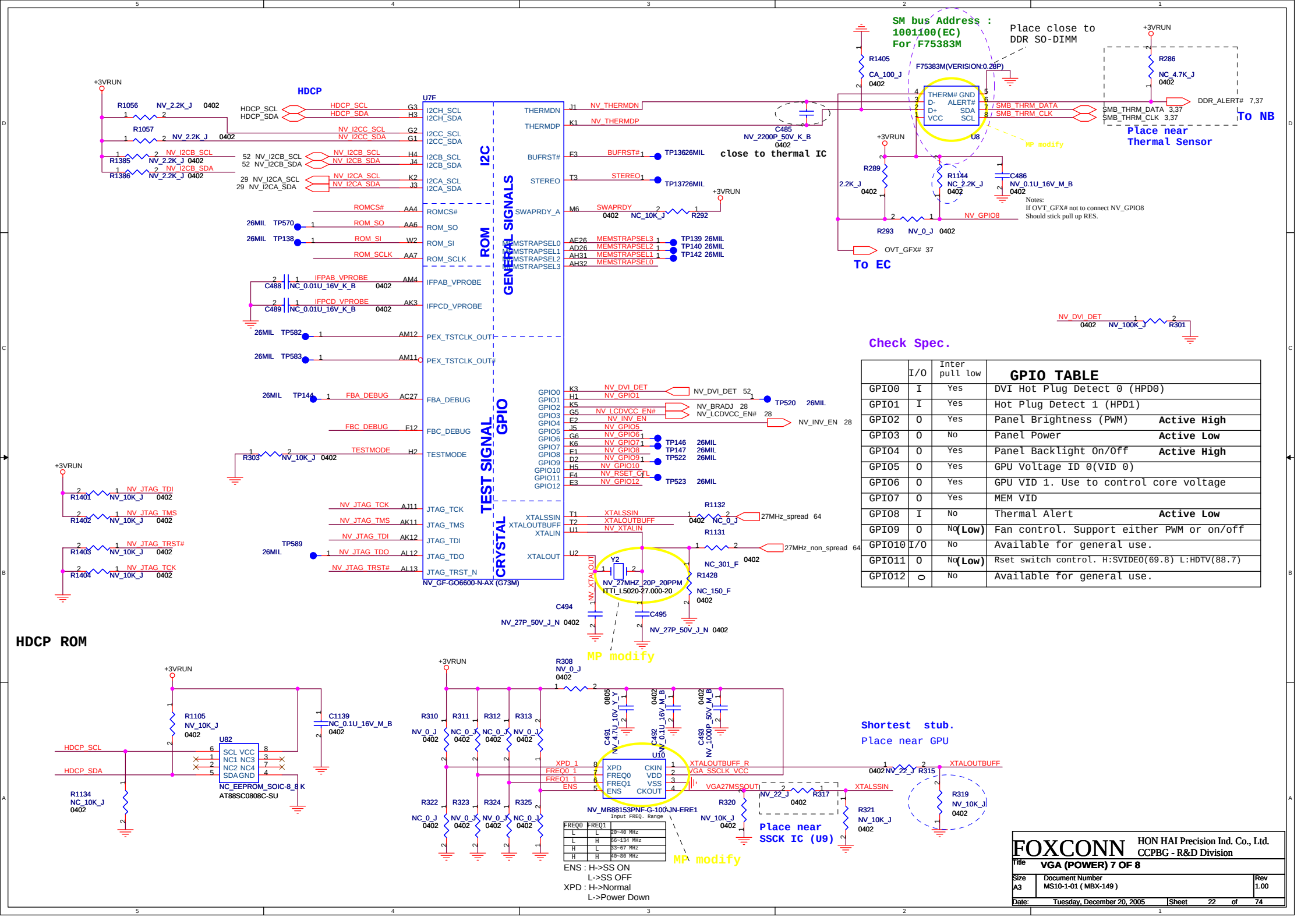
hexainf@hotmail.com
GRATIS - FOR FREE


SM bus Address :
1001100(EC)
For F75383M
Place close to
DDR SO-DIMM
F75383M(VERISION:0.28P)
HDCP
U7F
I2C
ROM
GENERAL SIGNALS
GPIO
TEST SIGNAL
CRYSTAL
close to thermal IC
To NB
Place near
Thermal Sensor
To EC
Notes:
If OVT_GFX# not to connect NV_GPIO8
Should stick pull up RES.
Check Spec.
GPIO TABLE
GPIO0 I Yes DVI Hot Plug Detect 0 (HPD0)
GPIO1 I Yes Hot Plug Detect 1 (HPD1)
GPIO2 O Yes Panel Brightness (PWM) Active High
GPIO3 O No Panel Power Active Low
GPIO4 O Yes Panel Backlight On/Off Active High
GPIO5 O Yes GPU Voltage ID 0(VID 0)
GPIO6 O Yes GPU VID 1. Use to control core voltage
GPIO7 O Yes MEM VID
GPIO8 I No Thermal Alert Active Low
GPIO9 O No(Low) Fan control. Support either PWM or on/off
GPIO10 I/O No Available for general use.
GPIO11 O No(Low) Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12 O No Available for general use.
HDCP ROM
MP modify
Shortest stub.
Place near GPU
Place near
SSCK IC (U9)
ENS : H->SS ON
L->SS OFF
XPD : H->Normal
L->Power Down
FOXCONN
HON HAI Precision Ind. Co., Ltd.
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Title VGA (POWER) 7 OF 8
Size A3
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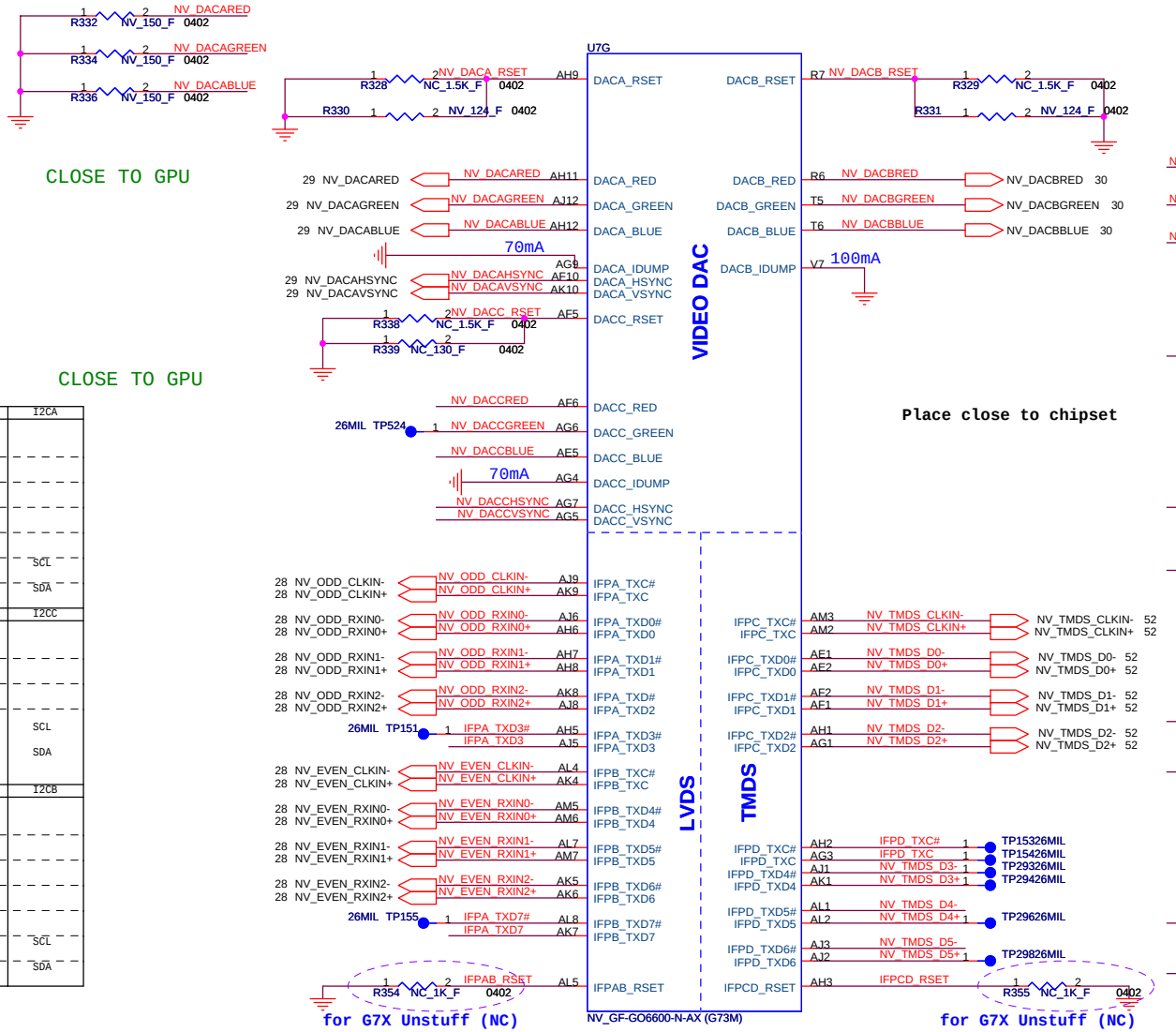

DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCCLK			SCL
	VGA-DDCDATA			SDA
DACB	**S-VIDEO**	**COMPOSITE**	**D-CONNECTOR**	**I2CC**
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITEPB		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	**DVI-I**			**I2CB**
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCCLK			SCL
	DVI-DDCDATA			SDA

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: VGA (POWER) 8 OF 8

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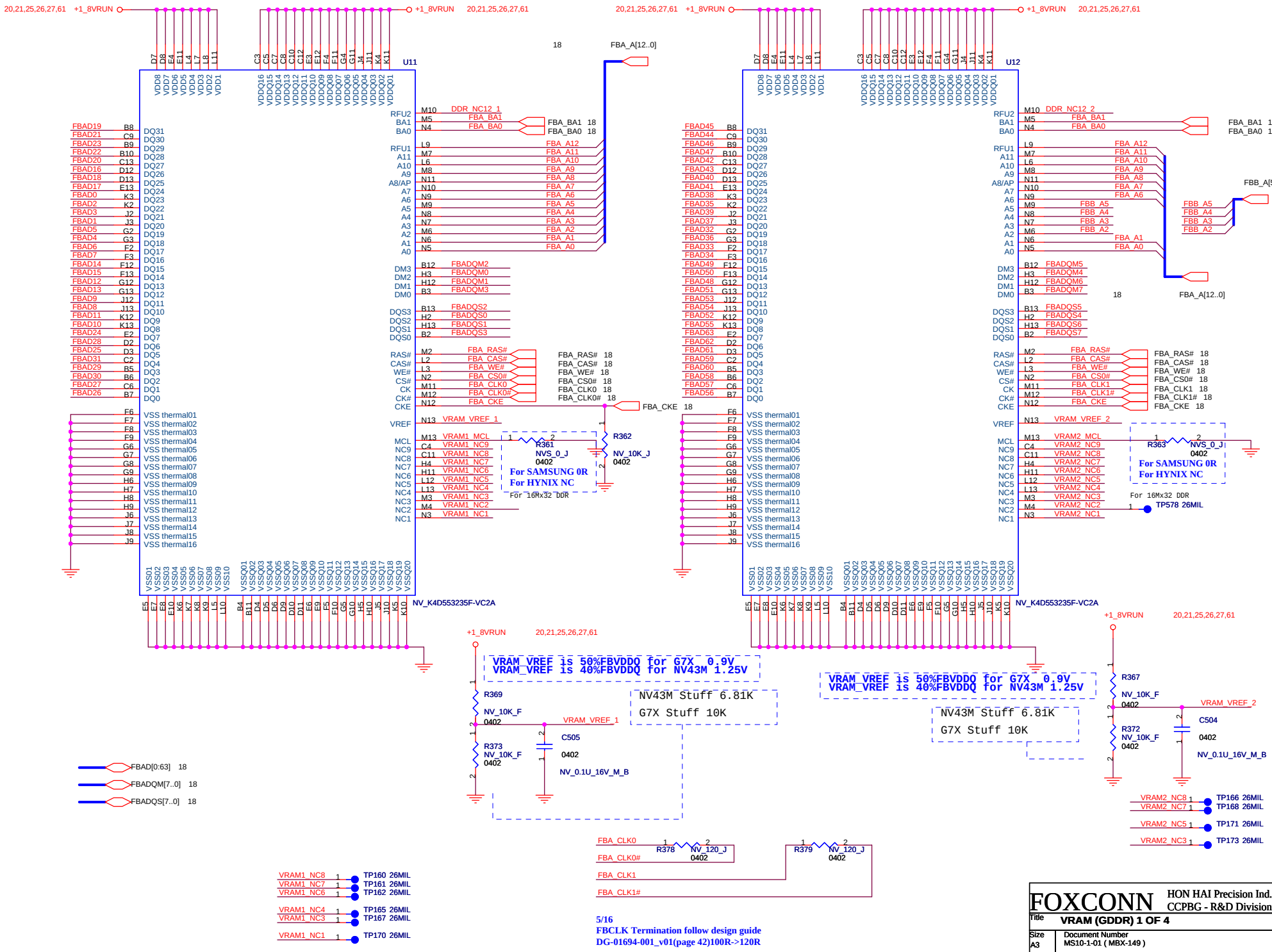
U11
U12
NV_K4D553235F-VC2A
FBA_A[12..0]
FBB_A[5..2]
FBA_A[12..0]
FBAD[0:63] 18
FBADQM[7..0] 18
FBADQS[7..0] 18
+1_8VRUN
20,21,25,26,27,61
VRAM_VREF is 50%FBVDDQ for G7X 0.9V
VRAM_VREF is 40%FBVDDQ for NV43M 1.25V
NV43M Stuff 6.81K
G7X Stuff 10K
For SAMSUNG 0R
For HYNIX NC
For 16Mx32 DDR
R361 NVS_0_J 0402
R362 NV_10K_J 0402
R363 NVS_0_J 0402
R367 NV_10K_F 0402
R369 NV_10K_F 0402
R372 NV_10K_F 0402
R373 NV_10K_F 0402
C504 0402 NV_0.1U_16V_M_B
C505 0402 NV_0.1U_16V_M_B
R378 NV_120_J 0402
R379 NV_120_J 0402
TP578 26MIL
TP160 26MIL
TP161 26MIL
TP162 26MIL
TP165 26MIL
TP167 26MIL
TP170 26MIL
TP166 26MIL
TP168 26MIL
TP171 26MIL
TP173 26MIL
5/16
FBCLK Termination follow design guide
DG-01694-001_v01(page 42)100R->120R
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title VRAM (GDDR) 1 OF 4
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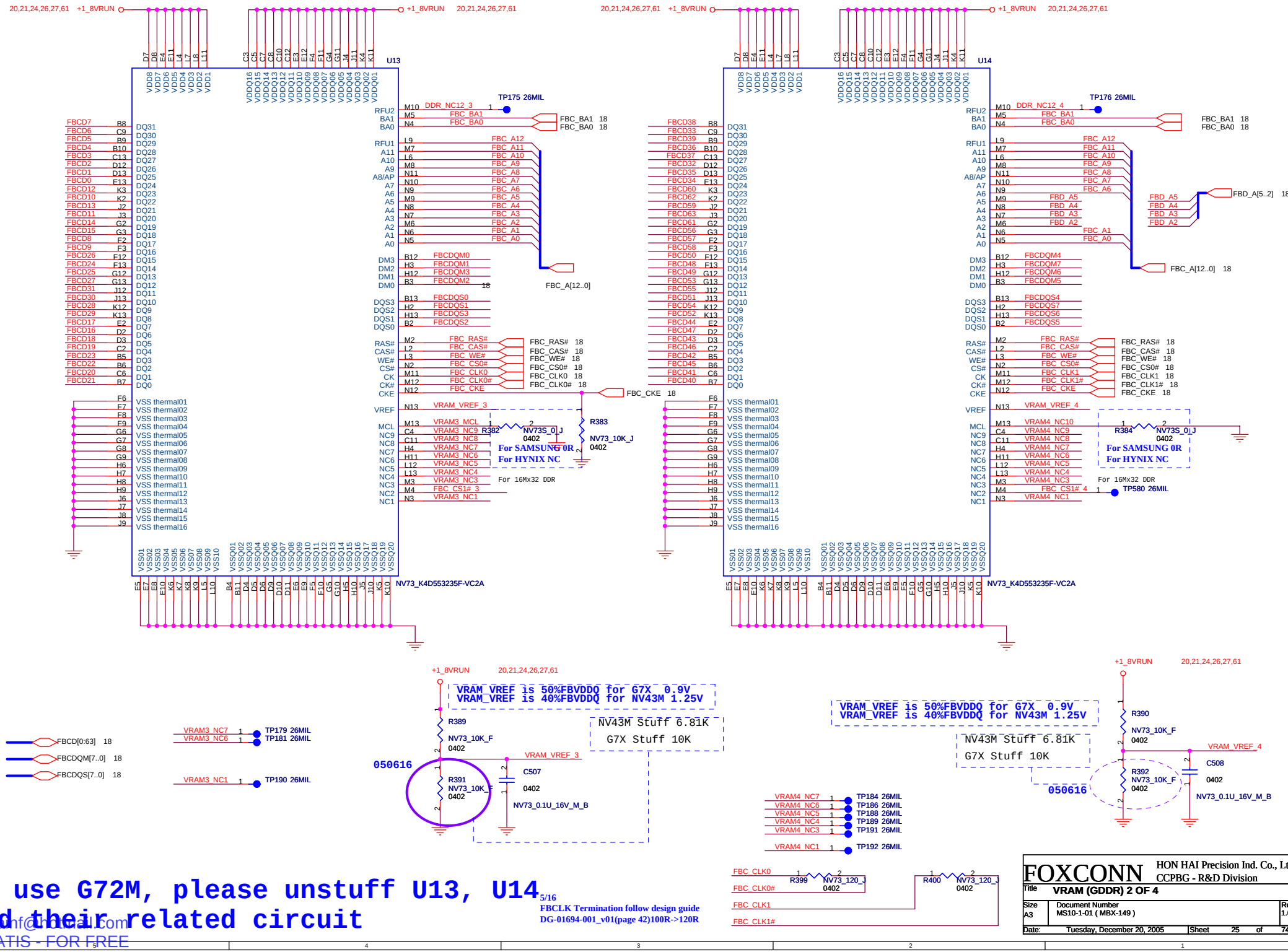

Decoupling for right MEMORY

Place around the MEM

+1_8VRUN 20,21,24,25,27,61

5/6
4.7u->10u

C510 NV73_10U_6.3V_M 0805_X5R
C511 NV73_0.1U_16V_M_B 0402
C512 NV73_0.1U_16V_M_B 0402
C513 NV73_0.1U_16V_M_B 0402
C514 NV73_0.1U_16V_M_B 0402
C515 NV73_0.1U_16V_M_B 0402
C516 NV73_0.1U_16V_M_B 0402
C517 NV73_0.1U_16V_M_B 0402
C518 NV73_0.1U_16V_M_B 0402
C519 NV73_0.1U_16V_M_B 0402
C520 NV73_0.1U_16V_M_B 0402

+1_8VRUN 20,21,24,25,27,61

1.2A

Place under the MEM

C521 NV73_0.1U_16V_M_B 0402
C522 NV73_0.1U_16V_M_B 0402
C523 NV73_0.1U_16V_M_B 0402
C524 NV73_1000P_50V_M_B 0402
C525 NV73_1000P_50V_M_B 0402
C526 NV73_1000P_50V_M_B 0402
C527 NV73_1000P_50V_M_B 0402
C528 NV73_1000P_50V_M_B 0402

Decoupling for left MEMORY

Place around the MEM

+1_8VRUN 20,21,24,25,27,61

5/6
4.7u->10u

C540 NV73_10U_6.3V_M 0805_X5R
C541 NV73_0.1U_16V_M_B 0402
C542 NV73_0.1U_16V_M_B 0402
C543 NV73_0.1U_16V_M_B 0402
C544 NV73_0.1U_16V_M_B 0402
C545 NV73_0.1U_16V_M_B 0402
C546 NV73_0.1U_16V_M_B 0402
C547 NV73_0.1U_16V_M_B 0402
C548 NV73_0.1U_16V_M_B 0402
C549 NV73_0.1U_16V_M_B 0402
C550 NV73_0.1U_16V_M_B 0402

+1_8VRUN 20,21,24,25,27,61

Place under the MEM

C551 NV73_0.1U_16V_M_B 0402
C552 NV73_0.1U_16V_M_B 0402
C553 NV73_0.1U_16V_M_B 0402
C554 NV73_1000P_50V_M_B 0402
C555 NV73_1000P_50V_M_B 0402
C556 NV73_1000P_50V_M_B 0402
C557 NV73_1000P_50V_M_B 0402
C558 NV73_1000P_50V_M_B 0402

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: VRAM (GDDR) 3 OF 4

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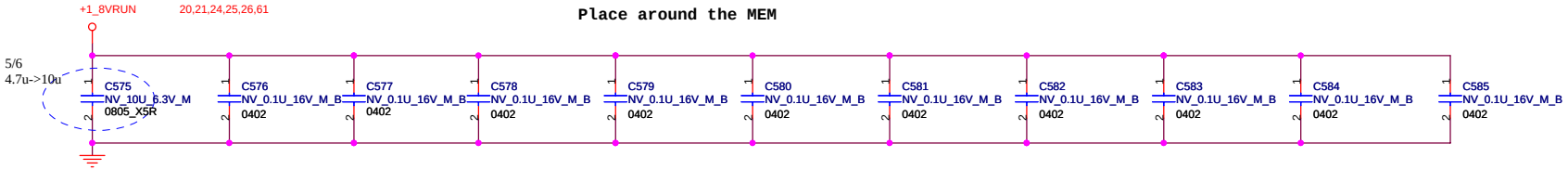
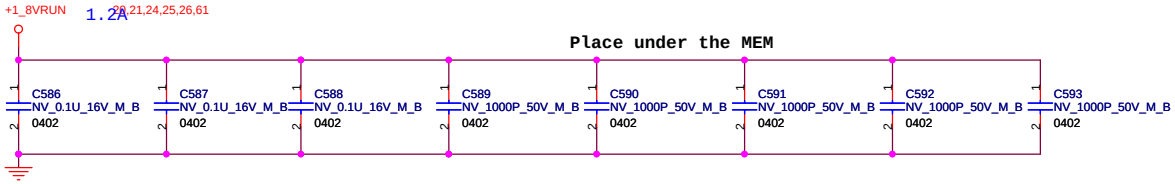
Decoupling for right MEMORY

Place around the MEM

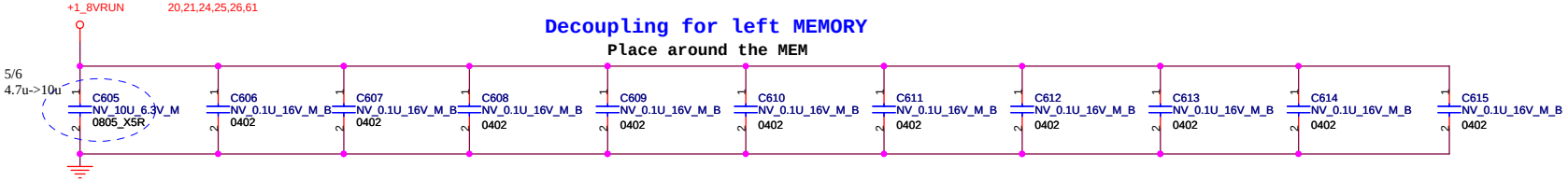


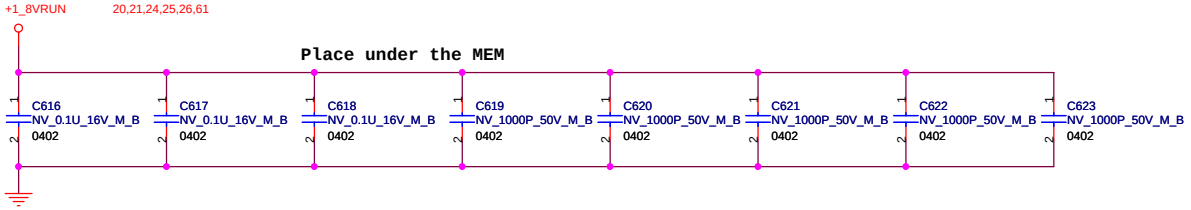


NO USE

Decoupling for left MEMORY

Place around the MEM





Place under the MEM

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VRAM (POWERBYPASS) 4 OF 4	
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LVDS

Group1,Group1 should be close

Group1 / Group2

	Group1	Group2
23 NV_ODD_CLKIN- / 23 NV_ODD_CLKIN+	0404_4P2R NV_0 RP76	0404_4P2R CA_0 RP77
23 NV_ODD_RXIN0- / 23 NV_ODD_RXIN0+	0404_4P2R NV_0 RP78	0404_4P2R CA_0 RP79
23 NV_ODD_RXIN1- / 23 NV_ODD_RXIN1+	0404_4P2R NV_0 RP80	0404_4P2R CA_0 RP81
23 NV_ODD_RXIN2- / 23 NV_ODD_RXIN2+	0404_4P2R NV_0 RP82	0404_4P2R CA_0 RP83
23 NV_EVEN_CLKIN- / 23 NV_EVEN_CLKIN+	0404_4P2R NV_0 RP84	0404_4P2R CA_0 RP85
23 NV_EVEN_RXIN0- / 23 NV_EVEN_RXIN0+	NV_0 RP86 0404_4P2R	CA_0 RP87 0404_4P2R
23 NV_EVEN_RXIN1- / 23 NV_EVEN_RXIN1+	NV_0 RP88 0404_4P2R	CA_0 RP89 0404_4P2R
23 NV_EVEN_RXIN2- / 23 NV_EVEN_RXIN2+	0404_4P2R NV_0 RP90	0404_4P2R CA_0 RP91

ODD_CLKIN- / ODD_CLKIN+ / ODD_RXIN0- / ODD_RXIN0+ / ODD_RXIN1- / ODD_RXIN1+ / ODD_RXIN2- / ODD_RXIN2+ / EVEN_CLKIN- / EVEN_CLKIN+ / EVEN_RXIN0- / EVEN_RXIN0+ / EVEN_RXIN1- / EVEN_RXIN1+ / EVEN_RXIN2- / EVEN_RXIN2+

GM_ODD_CLKIN- 8 / GM_ODD_CLKIN+ 8
GM_ODD_RXIN0- 8 / GM_ODD_RXIN0+ 8
GM_ODD_RXIN1- 8 / GM_ODD_RXIN1+ 8
GM_ODD_RXIN2- 8 / GM_ODD_RXIN2+ 8
GM_EVEN_CLKIN- 8 / GM_EVEN_CLKIN+ 8
GM_EVEN_RXIN0- 8 / GM_EVEN_RXIN0+ 8
GM_EVEN_RXIN1- 8 / GM_EVEN_RXIN1+ 8
GM_EVEN_RXIN2- 8 / GM_EVEN_RXIN2+ 8

LVDS CONNECTOR

CN3
FPC RECEPTCAL CONN_30P
FOX_GS12301-1011A-9F

LCDVCC
37 LVDS_GPIO
EVEN_RXIN0+ / EVEN_RXIN0-
EVEN_RXIN1+ / EVEN_RXIN1-
EVEN_RXIN2- / EVEN_RXIN2+
EVEN_CLKIN+ / EVEN_CLKIN-
ODD_CLKIN+ / ODD_CLKIN-
ODD_RXIN2+ / ODD_RXIN2-
ODD_RXIN1+ / ODD_RXIN1-
ODD_RXIN0+ / ODD_RXIN0-

56,57,58,59,60,61,63 DCBATOUT

C640 0.1U_50V_K_B 0603

2A

CN49
B TO B HEADER CONN_6P
FOX_HS8106E

8 NB_BRADJ — 0402 CA_0_J R1268 — INV_BRADJ

INV_ENABLE

+3VRUN

PVT modify

U106 NV_74AHC1G08GW

27 INV_EN_EC — 0402 — 1
22 NV_BRADJ — NV_0_J R1269 — BRADJPWM_LPF — 2

R1393 10K_J 0402

INVERTER CONNECTOR

PVT modify

U15 74AHC1G08GW +3VRUN

37 INV_EN_EC — INV_ENABLE

R1394 10K_J 0402

INV_ENABLE_1

U16 74AHC1G08GW +3VRUN

37,39 LIDIN#
22 NV_INV_EN
(3.3V tolerant)

8 GM_INV_EN — R457 CA_0_J 0402 — R458 CA_100K_J 0402

LCDVCC

+3VRUN — R459 10K_J 0402 — Q10 — CA_PDTC144EU

8 GM_LCDVCC_EN

+3VRUN — C647 4.7U_6.3V_K 0805_X5R

U17 G548B2P1U
IN1 IN2 OUT3 OUT2 OUT1 EN GND OC

C649 4.7U_10V_Y_Y 0805

C650 0.1U_16V_Y_Y 0402

R461 200_J 0603

22 NV_LCDVCC_EN#

C1151 0402 NV_0.1U_16V_Y_Y

DISCHARGE

The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

C641 NC_10P_50V_J_N ODD_CLKIN- 0402
C643 NC_10P_50V_J_N ODD_CLKIN+ 0402
C644 NC_10P_50V_J_N EVEN_CLKIN- 0402
C645 NC_10P_50V_J_N EVEN_CLKIN+ 0402

For EMI

PANEL ID

SW1 HDS404-E_SW-SLIDE

LCDID0 33
LCDID1 33
LCDID2 33
LCDID3 33

ON=0

Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vender	Hitach	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID Check[3..0]	1000	1000	1100

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: LVDS
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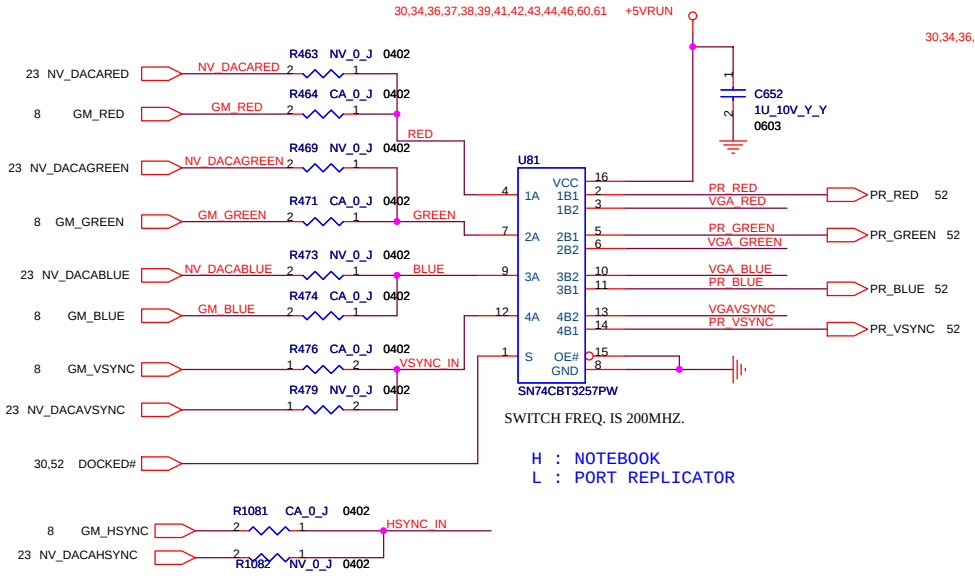
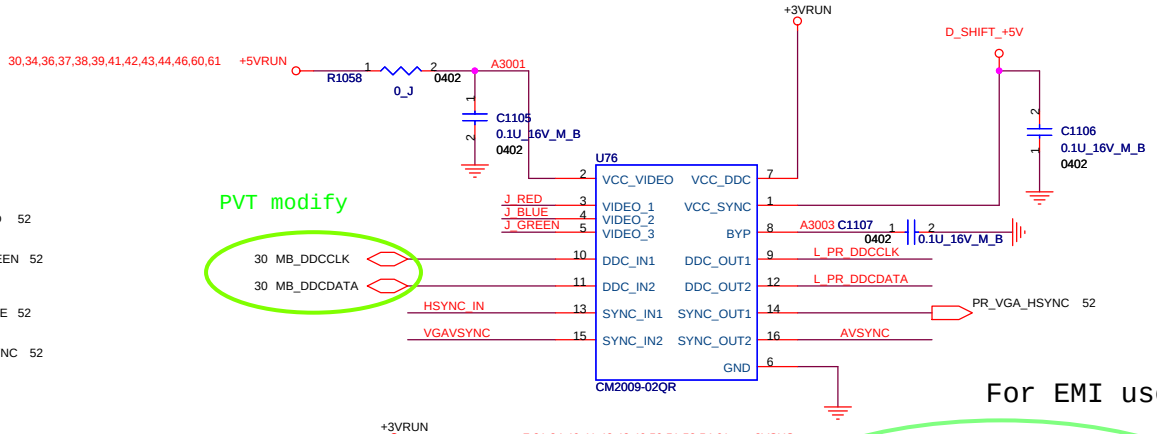
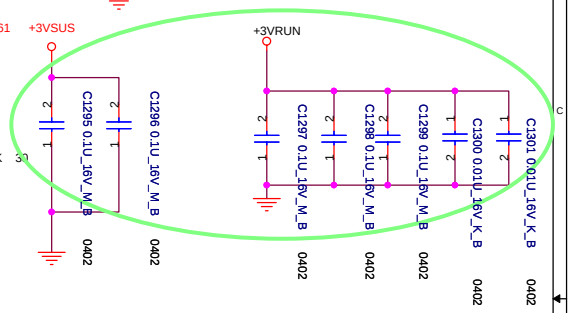
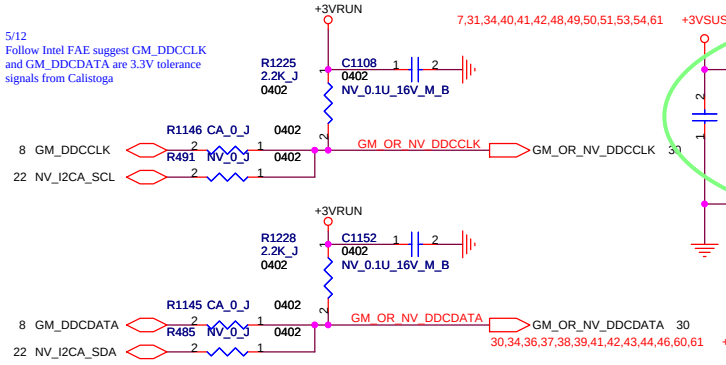
CRT ANALOG SWITCH



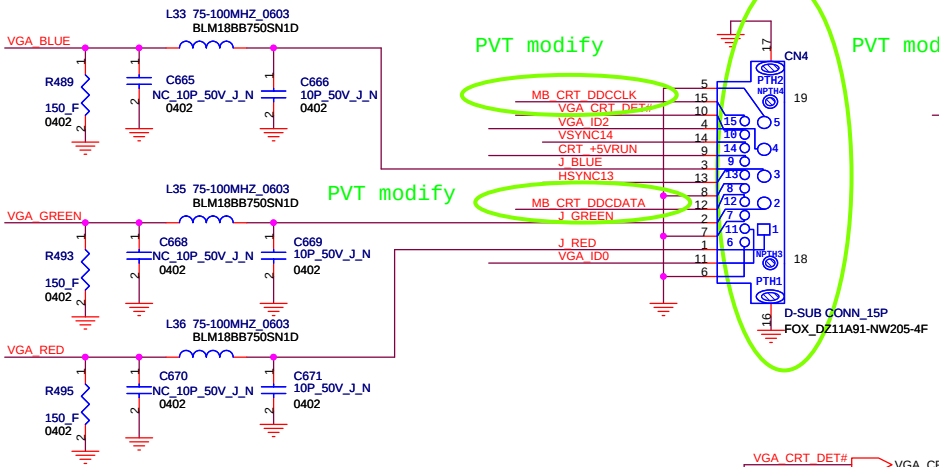


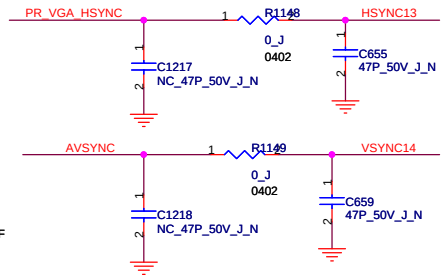
For EMI used

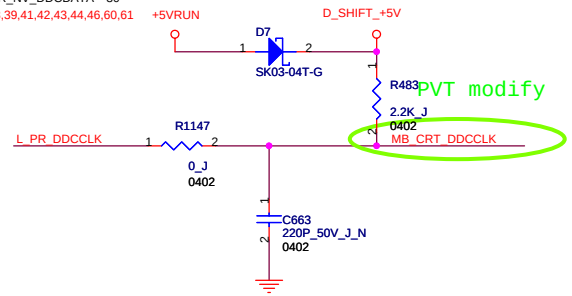


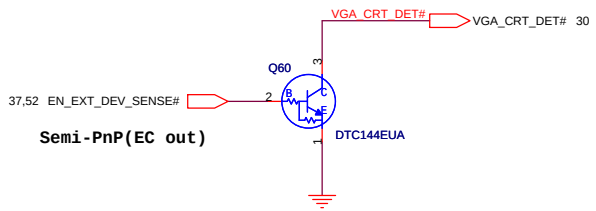


CRT CONNECTOR







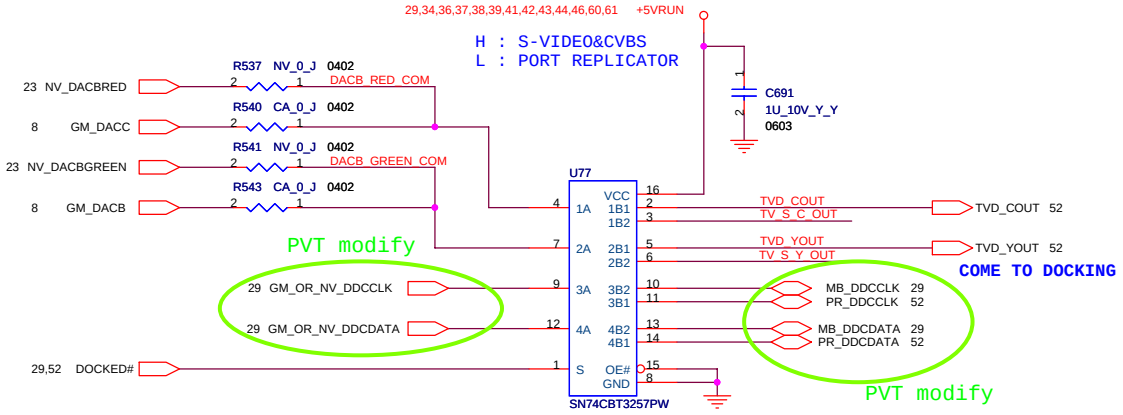


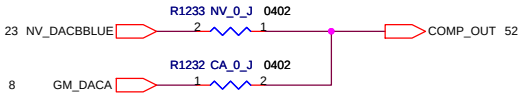
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: MS10-1-01 (MBX-149)	Rev: 1.00
Date: Tuesday, December 20, 2005	Sheet 29 of 74	

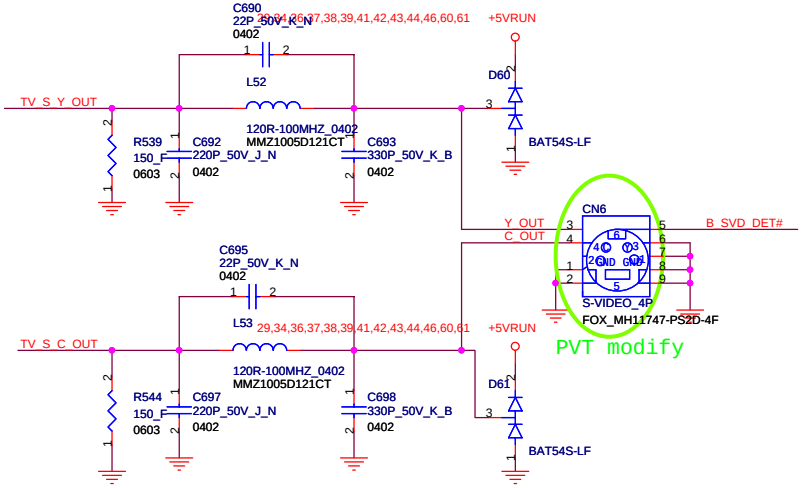
S-VIDEO

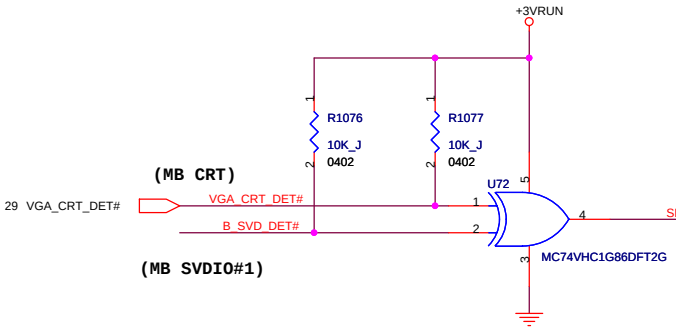
These compoent close to S-Video connector within 700 mil

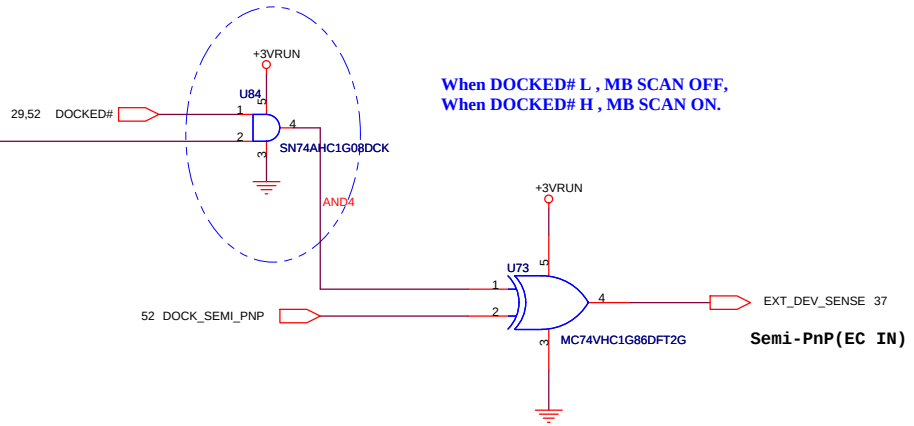
S-VIDEO ANALOG SWITCH





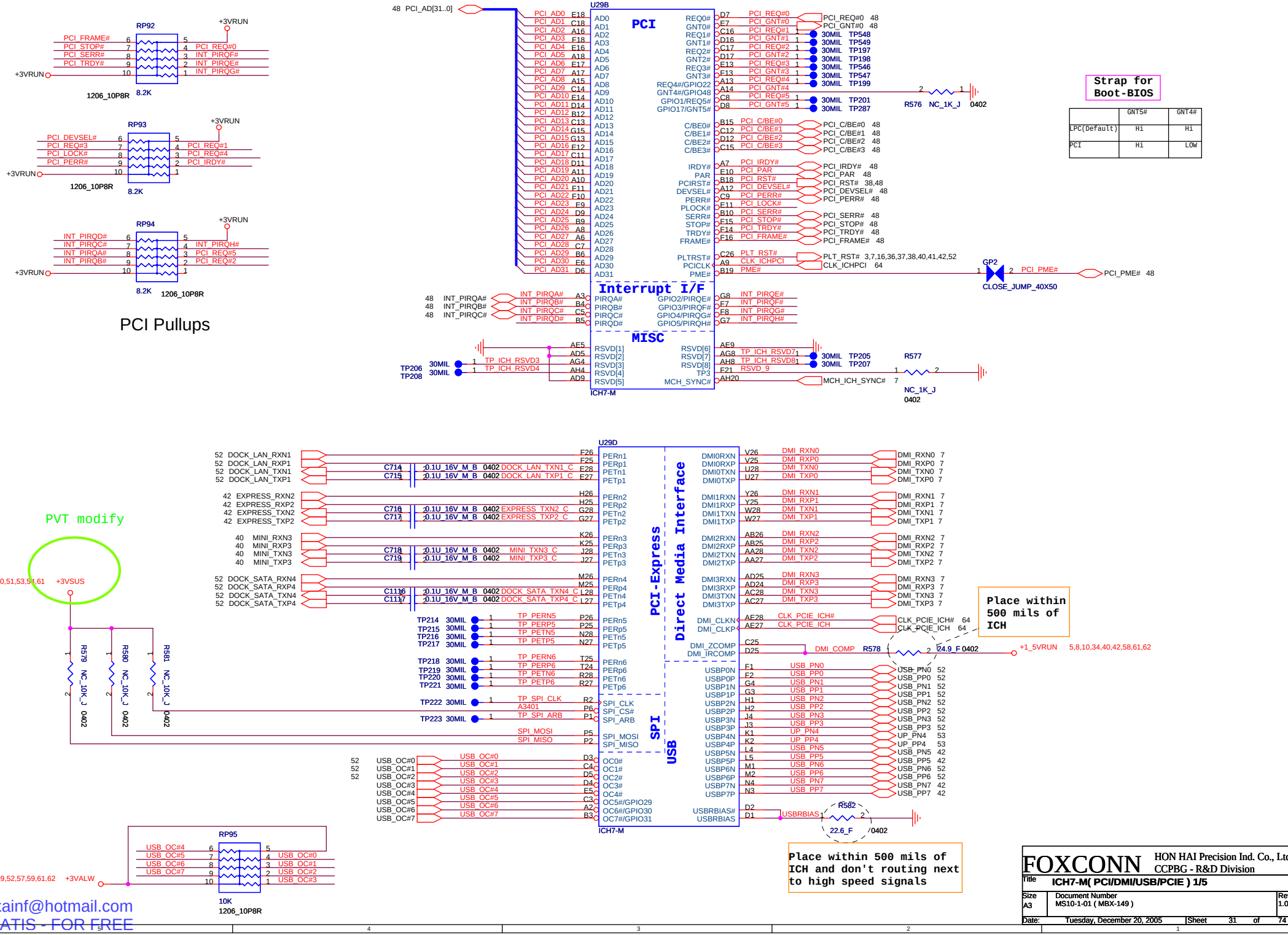


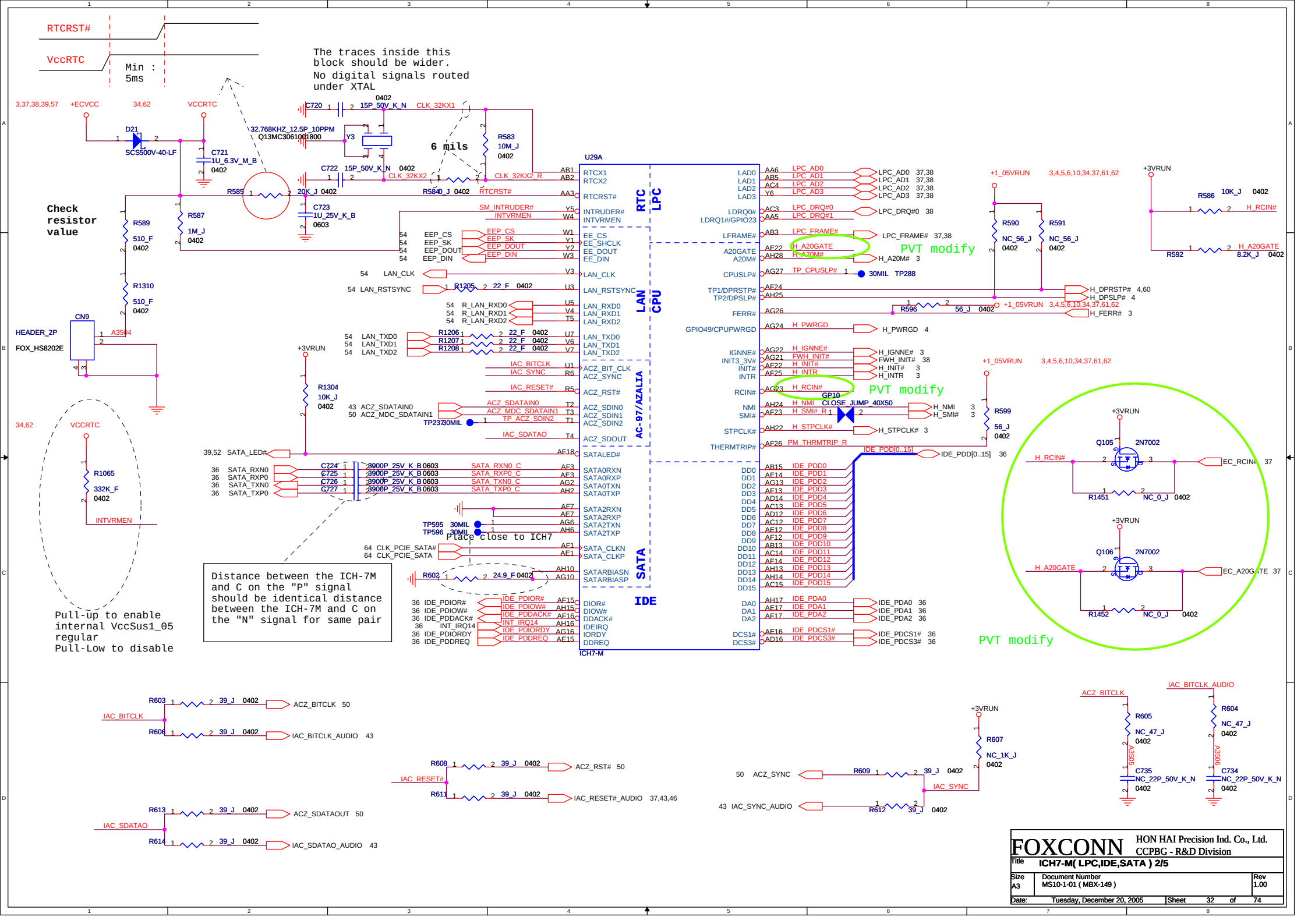




Semi-PnP

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	S-VIDEO/Semi-PnP	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 30 of 74	


RP92
PCI_FRAME#
PCI_STOP#
PCI_SERR#
PCI_TRDY#
+3VRUN
PCI_REQ#0
INT_PIRQF#
INT_PIRQE#
INT_PIRQG#
1206_10P8R
8.2K
RP93
PCI_DEVSEL#
PCI_REQ#3
PCI_LOCK#
PCI_PERR#
PCI_REQ#1
PCI_REQ#4
PCI_IRDY#
RP94
INT_PIRQD#
INT_PIRQC#
INT_PIRQA#
INT_PIRQB#
INT_PIRQH#
PCI_REQ#5
PCI_REQ#2
PCI Pullups
U29B
PCI
48 PCI_AD[31..0]
PCI_AD0 E18
PCI_AD1 C18
PCI_AD2 A16
PCI_AD3 F18
PCI_AD4 E16
PCI_AD5 A18
PCI_AD6 E17
PCI_AD7 A17
PCI_AD8 A15
PCI_AD9 C14
PCI_AD10 E14
PCI_AD11 D14
PCI_AD12 B12
PCI_AD13 C13
PCI_AD14 G15
PCI_AD15 G13
PCI_AD16 E12
PCI_AD17 C11
PCI_AD18 D11
PCI_AD19 A11
PCI_AD20 A10
PCI_AD21 F11
PCI_AD22 F10
PCI_AD23 E9
PCI_AD24 D9
PCI_AD25 B9
PCI_AD26 A8
PCI_AD27 A6
PCI_AD28 C7
PCI_AD29 B6
PCI_AD30 E6
PCI_AD31 D6
REQ0# D7 PCI_REQ#0
GNT0# E7 PCI_GNT#0
REQ1# C16 PCI_REQ#1
GNT1# D16 PCI_GNT#1
REQ2# C17 PCI_REQ#2
GNT2# D17 PCI_GNT#2
REQ3# E13 PCI_REQ#3
GNT3# F13 PCI_GNT#3
REQ4#/GPIO22 A13 PCI_REQ#4
GNT4#/GPIO48 A14 PCI_GNT#4
GPIO1/REQ5# C8 PCI_REQ#5
GPIO17/GNT5# D8 PCI_GNT#5
C/BE0# B15 PCI_C/BE#0
C/BE1# C12 PCI_C/BE#1
C/BE2# D12 PCI_C/BE#2
C/BE3# C15 PCI_C/BE#3
IRDY# A7 PCI_IRDY#
PAR E10 PCI_PAR
PCIRST# B18 PCI_RST#
DEVSEL# A12 PCI_DEVSEL#
PERR# C9 PCI_PERR#
PLOCK# E11 PCI_LOCK#
SERR# B10 PCI_SERR#
STOP# F15 PCI_STOP#
TRDY# F14 PCI_TRDY#
FRAME# F16 PCI_FRAME#
PLTRST# C26 PLT_RST#
PCICLK A9 CLK_ICHPCI
PME# B19 PME#
PCI_REQ#0 48
PCI_GNT#0 48
30MIL TP548
30MIL TP549
30MIL TP197
30MIL TP198
30MIL TP546
30MIL TP547
30MIL TP199
30MIL TP201
30MIL TP287
R576 NC_1K_J 0402
PLT_RST# 3,7,16,36,37,38,40,41,42,52
CLK_ICHPCI 64
GP2
CLOSE_JUMP_40X50
PCI_PME# 48
Strap for Boot-BIOS
GNT5# GNT4#
LPC(Default) Hi Hi
PCI Hi LOW
Interrupt I/F
48 INT_PIRQA#
48 INT_PIRQB#
48 INT_PIRQC#
PIRQA# A3 INT_PIRQA#
PIRQB# B4 INT_PIRQB#
PIRQC# C5 INT_PIRQC#
PIRQD# B5 INT_PIRQD#
GPIO2/PIRQE# G8 INT_PIRQE#
GPIO3/PIRQF# E7 INT_PIRQF#
GPIO4/PIRQG# F8 INT_PIRQG#
GPIO5/PIRQH# G7 INT_PIRQH#
MISC
RSVD[1] AE5
RSVD[2] AD5
RSVD[3] AG4
RSVD[4] AH4
RSVD[5] AD9
RSVD[6] AE9
RSVD[7] AG8 TP_ICH_RSVD7
RSVD[8] AH8 TP_ICH_RSVD8
TP3 F21 RSVD_9
MCH_SYNC# AH20 MCH_ICH_SYNC# 7
TP206 30MIL TP_ICH_RSVD3
TP208 30MIL TP_ICH_RSVD4
30MIL TP205
30MIL TP207
R577 NC_1K_J 0402
ICH7-M
PVT modify
41,42,48,49,50,51,53,54,61 +3VSUS
R579 NC_10K_J 0402
R580 NC_10K_J 0402
R581 NC_10K_J 0402
U29D
PCI-Express
Direct Media Interface
SPI
USB
52 DOCK_LAN_RXN1
52 DOCK_LAN_RXP1
52 DOCK_LAN_TXN1
52 DOCK_LAN_TXP1
C714 0.1U_16V_M_B 0402 DOCK_LAN_TXN1_C
C715 0.1U_16V_M_B 0402 DOCK_LAN_TXP1_C
PERn1 F26
PERp1 F25
PETn1 E28
PETp1 E27
42 EXPRESS_RXN2
42 EXPRESS_RXP2
42 EXPRESS_TXN2
42 EXPRESS_TXP2
C716 0.1U_16V_M_B 0402 EXPRESS_TXN2_C
C717 0.1U_16V_M_B 0402 EXPRESS_TXP2_C
PERn2 H26
PERp2 H25
PETn2 G28
PETp2 G27
40 MINI_RXN3
40 MINI_RXP3
40 MINI_TXN3
40 MINI_TXP3
C718 0.1U_16V_M_B 0402 MINI_TXN3_C
C719 0.1U_16V_M_B 0402 MINI_TXP3_C
PERn3 K26
PERp3 K25
PETn3 J28
PETp3 J27
52 DOCK_SATA_RXN4
52 DOCK_SATA_RXP4
52 DOCK_SATA_TXN4
52 DOCK_SATA_TXP4
C1116 0.1U_16V_M_B 0402 DOCK_SATA_TXN4_C
C1117 0.1U_16V_M_B 0402 DOCK_SATA_TXP4_C
PERn4 M26
PERp4 M25
PETn4 L28
PETp4 L27
PERn5 P26
PERp5 P25
PETn5 N28
PETp5 N27
PERn6 T25
PERp6 T24
PETn6 R28
PETp6 R27
DMI0RXN V26 DMI_RXN0
DMI0RXP V25 DMI_RXP0
DMI0TXN U28 DMI_TXN0
DMI0TXP U27 DMI_TXP0
DMI1RXN Y26 DMI_RXN1
DMI1RXP Y25 DMI_RXP1
DMI1TXN W28 DMI_TXN1
DMI1TXP W27 DMI_TXP1
DMI2RXN AB26 DMI_RXN2
DMI2RXP AB25 DMI_RXP2
DMI2TXN AA28 DMI_TXN2
DMI2TXP AA27 DMI_TXP2
DMI3RXN AD25 DMI_RXN3
DMI3RXP AD24 DMI_RXP3
DMI3TXN AC28 DMI_TXN3
DMI3TXP AC27 DMI_TXP3
DMI_CLKN AE28 CLK_PCIE_ICH#
DMI_CLKP AE27 CLK_PCIE_ICH
DMI_ZCOMP C25
DMI_IRCOMP D25
DMI_COMP R578 24.9_F 0402
+1_5VRUN 5,8,10,34,40,42,58,61,62
Place within 500 mils of ICH
TP214 30MIL TP_PERN5
TP215 30MIL TP_PERP5
TP216 30MIL TP_PETN5
TP217 30MIL TP_PETP5
TP218 30MIL TP_PERN6
TP219 30MIL TP_PERP6
TP220 30MIL TP_PETN6
TP221 30MIL TP_PETP6
TP222 30MIL TP_SPI_CLK
A3401
TP223 30MIL TP_SPI_ARB
SPI_CLK R2
SPI_CS# P6
SPI_ARB P1
SPI_MOSI P5
SPI_MISO P2
USBP0N F1 USB_PN0
USBP0P F2 USB_PP0
USBP1N G4 USB_PN1
USBP1P G3 USB_PP1
USBP2N H1 USB_PN2
USBP2P H2 USB_PP2
USBP3N J4 USB_PN3
USBP3P J3 USB_PP3
USBP4N K1 UP_PN4
USBP4P K2 UP_PP4
USBP5N L4 USB_PN5
USBP5P L5 USB_PP5
USBP6N M1 USB_PN6
USBP6P M2 USB_PP6
USBP7N N4 USB_PN7
USBP7P N3 USB_PP7
USBRBIAS# D2
USBRBIAS D1
R582 22.6_F /0402
52 USB_OC#0
52 USB_OC#1
52 USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
OC0# D3
OC1# C4
OC2# D5
OC3# D4
OC4# E5
OC5#/GPIO29 C3
OC6#/GPIO30 A2
OC7#/GPIO31 B3
ICH7-M
Place within 500 mils of ICH and don't routing next to high speed signals
RP95
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
10K
1206_10P8R
21,33,34,37,39,52,57,59,61,62 +3VALW
hexainf@hotmail.com
GRATIS - FOR FREE
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title ICH7-M(PCI/DMI/USB/PCIE) 1/5
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 31 of 74


RTCRST#
VccRTC
Min : 5ms
The traces inside this block should be wider.
No digital signals routed under XTAL
6 mils
Check resistor value
Pull-up to enable internal VccSus1_05 regular
Pull-Low to disable
Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair
Place close to ICH7
PVT modify
PVT modify
PVT modify
U29A
ICH7-M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
ICH7-M(LPC,IDE,SATA) 2/5
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
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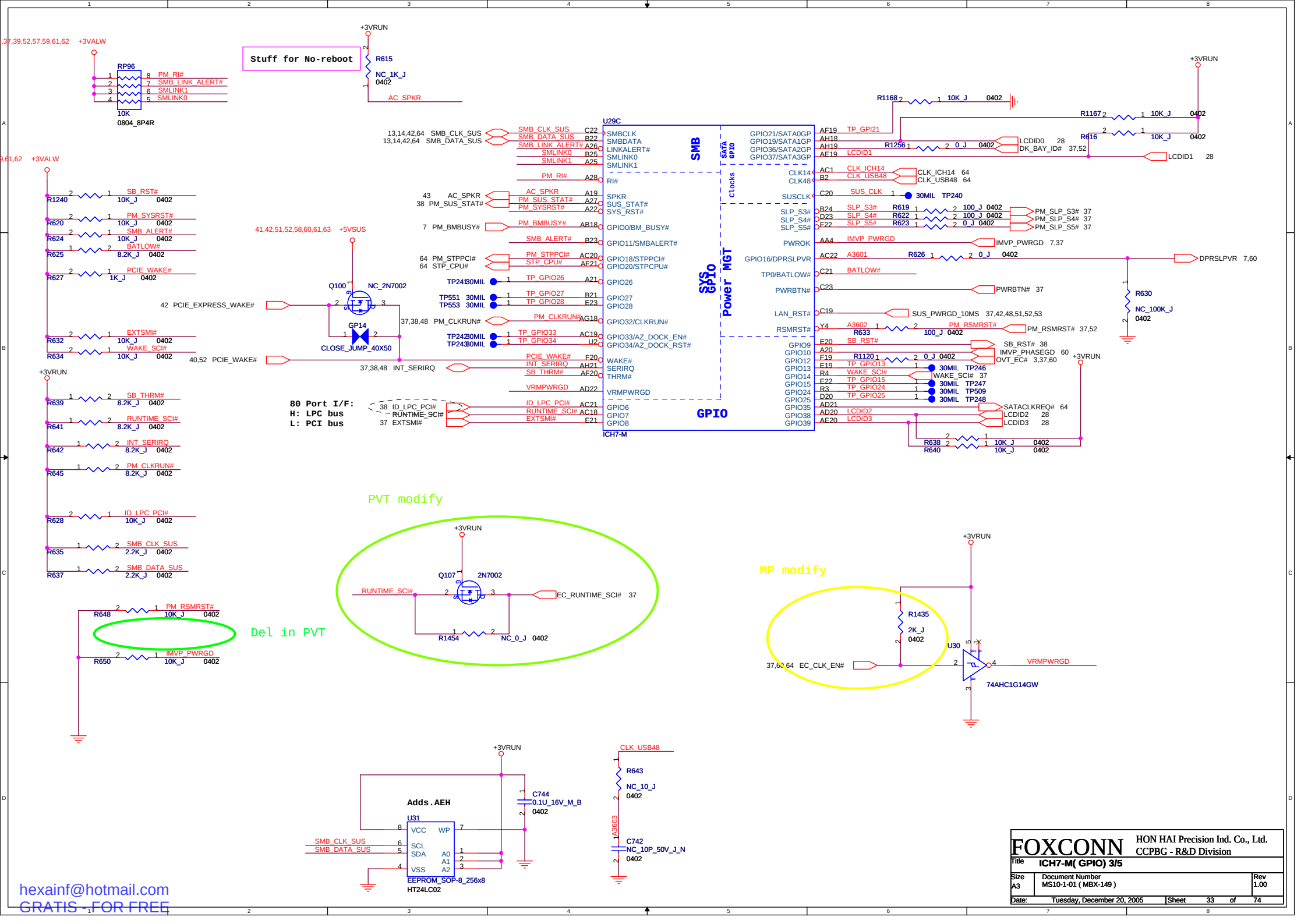
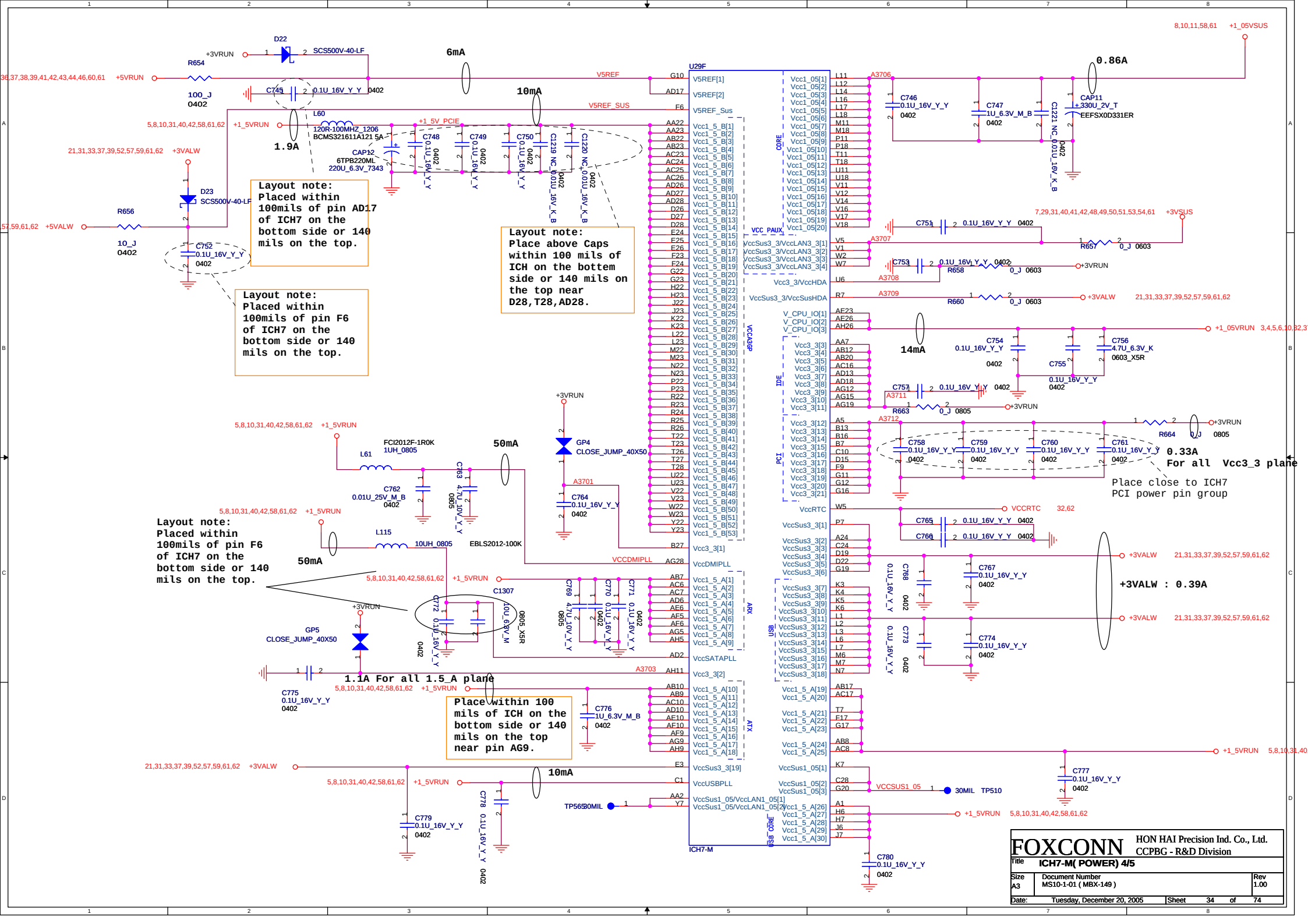
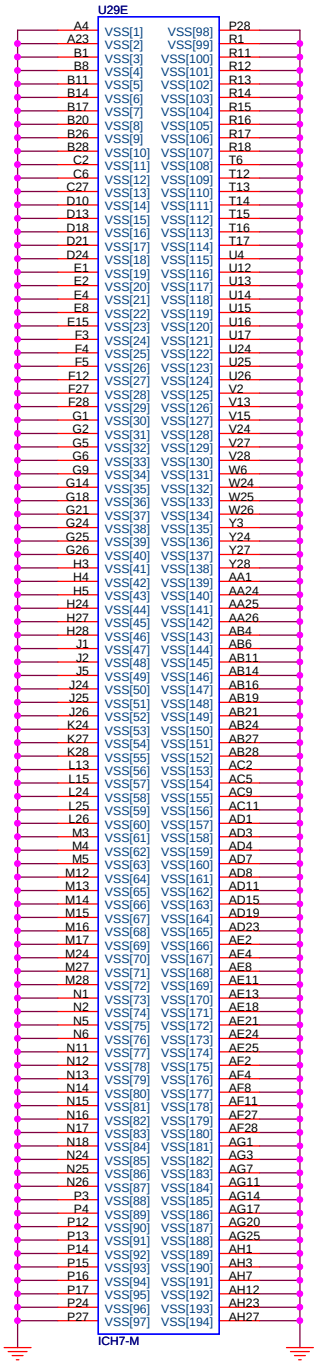
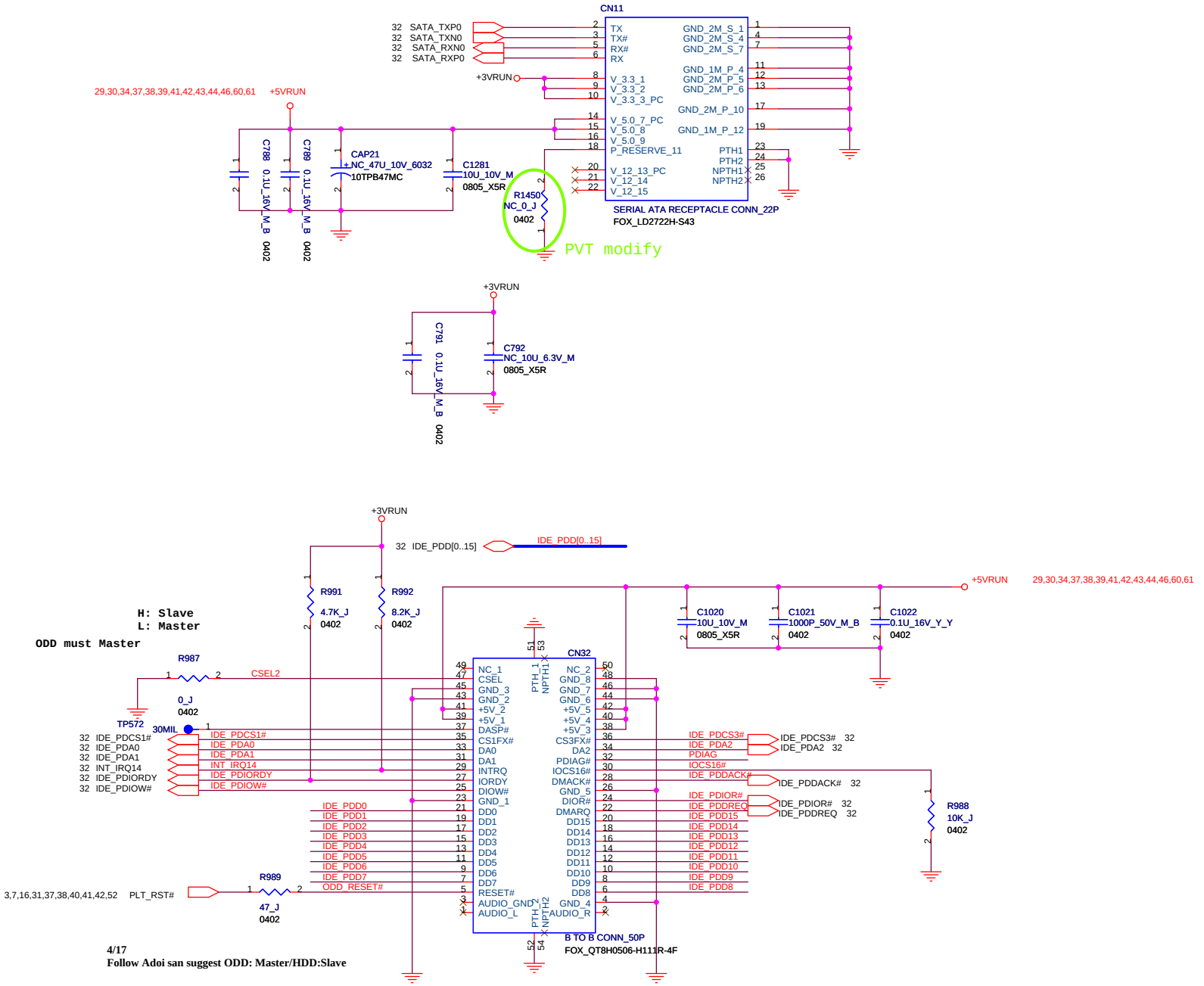



Layout note: Placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top.
Layout note: Place above Caps within 100 mils of ICH on the bottem side or 140 mils on the top near D28,T28,AD28.
Layout note: Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.
Layout note: Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.
Place close to ICH7 PCI power pin group
0.33A For all Vcc3_3 plane
+3VALW : 0.39A
1.1A For all 1.5_A plane
0.86A
1.9A
6mA
10mA
14mA
50mA
ICH7-M
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title ICH7-M(POWER) 4/5
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 34 of 74

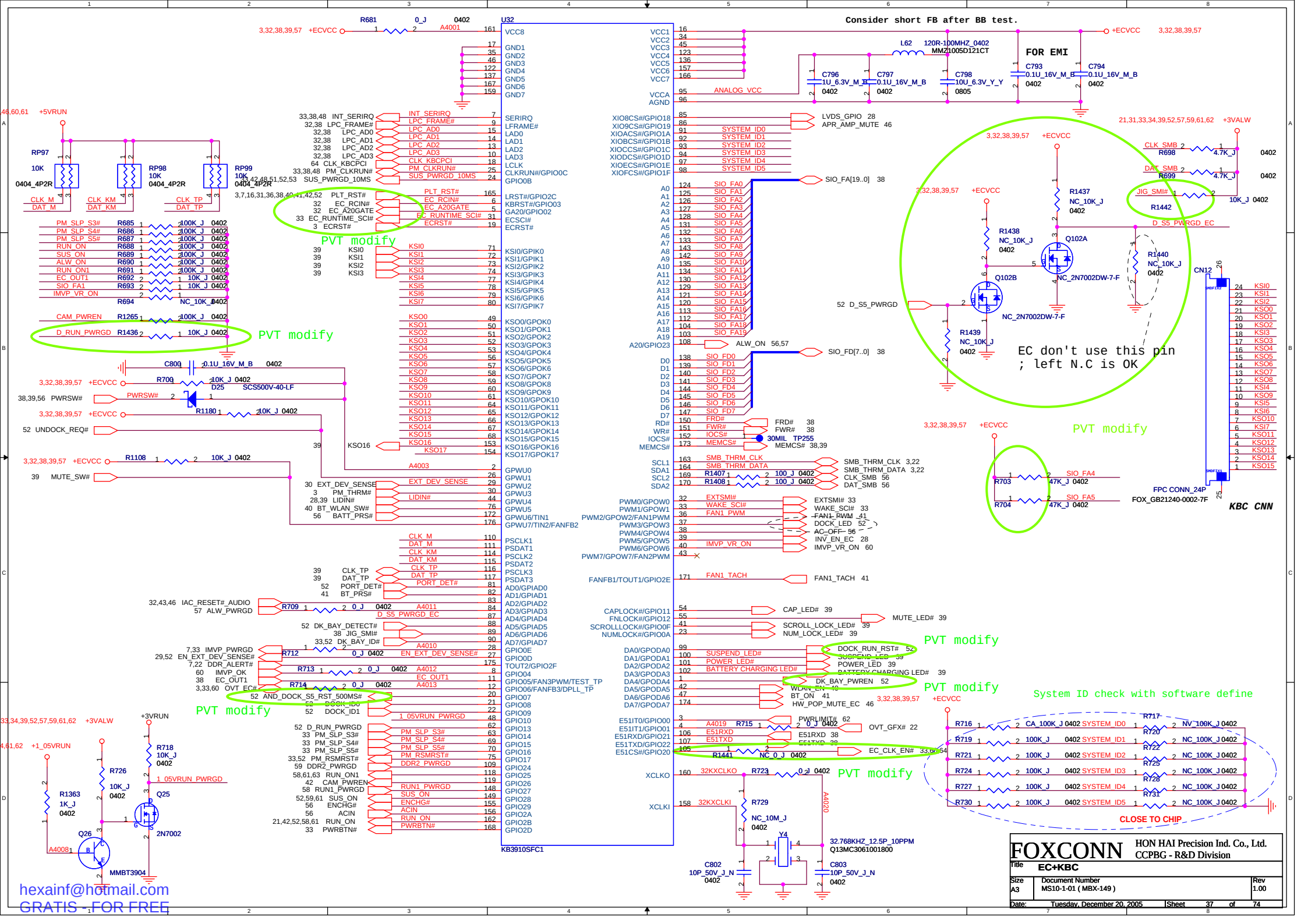


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ICH7-M(GND) 5/5	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 35 of 74	



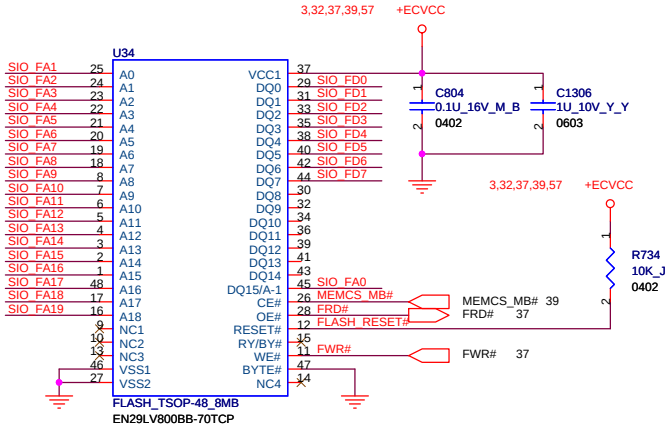
CD-ROM CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA HDD/CD-ROM	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 36 of 74	


Consider short FB after BB test.
U32
KB3910SFC1
FOR EMI
PVT modify
EC don't use this pin ; left N.C is OK
System ID check with software define
CLOSE TO CHIP
KBC CNN
FPC CONN_24P
FOX_GB21240-0002-7F
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title EC+KBC
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 37 of 74
hexainf@hotmail.com
GRATIS - FOR FREE

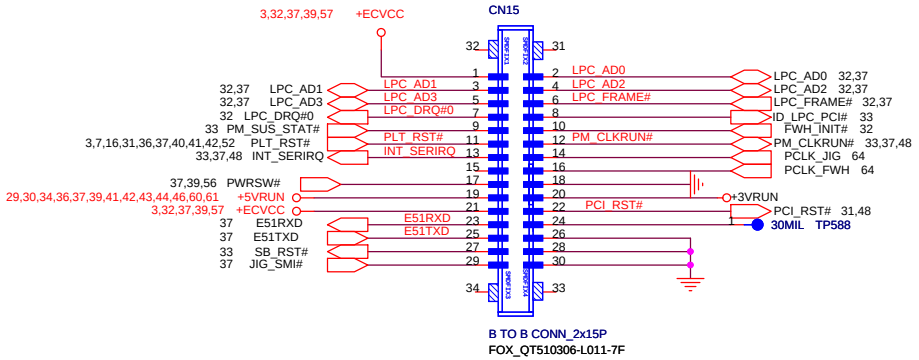
37 SIO_FA[19..0]

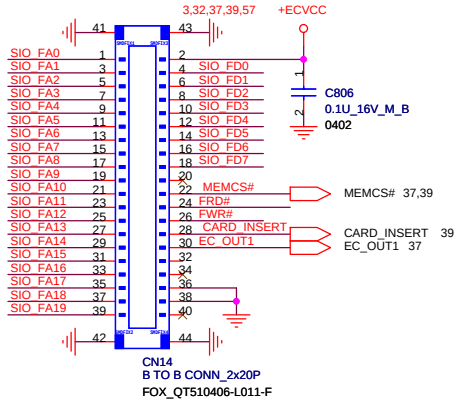
37 SIO_FD[7..0]



FLASH BIOS

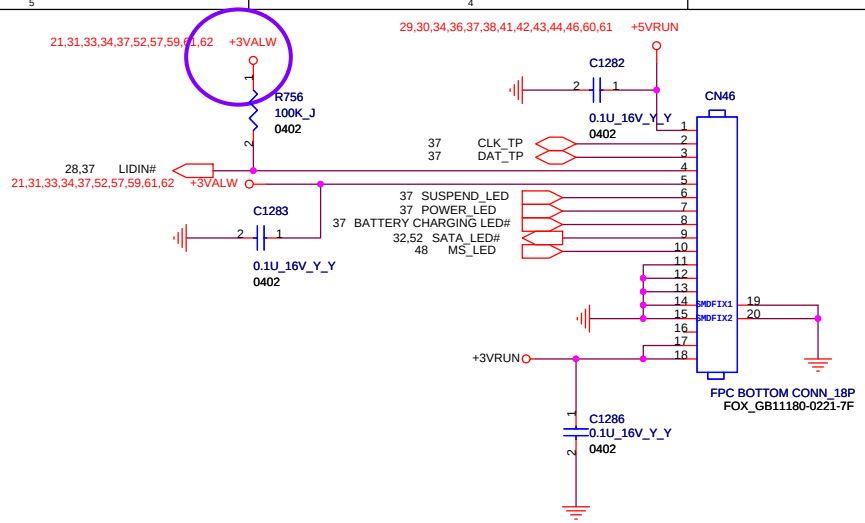
JIG-120

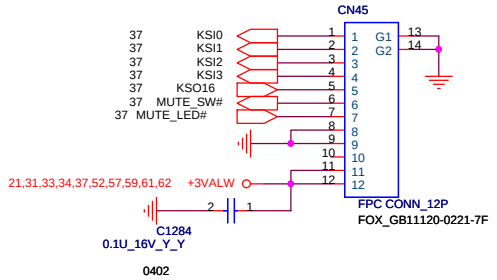


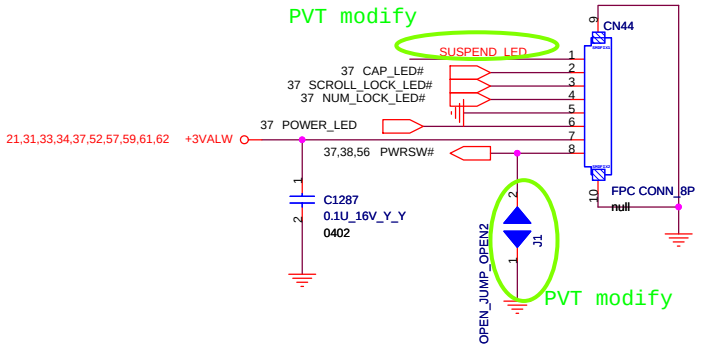


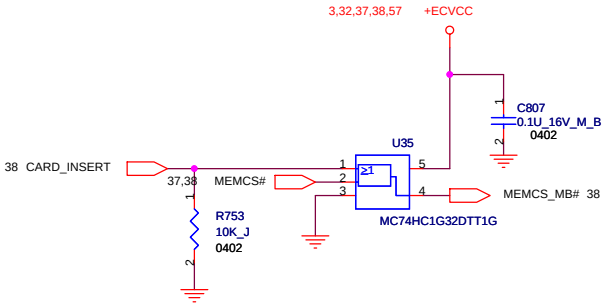
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

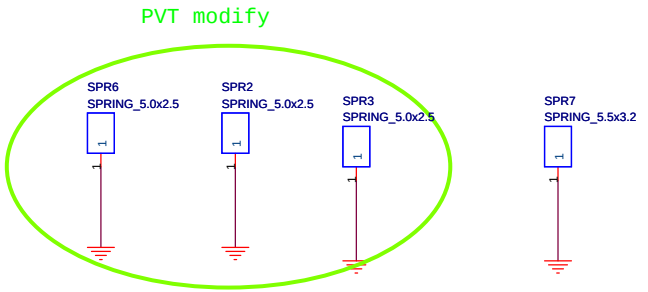
Title	Flash ROM/X-Bus CONN	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 38 of 74	



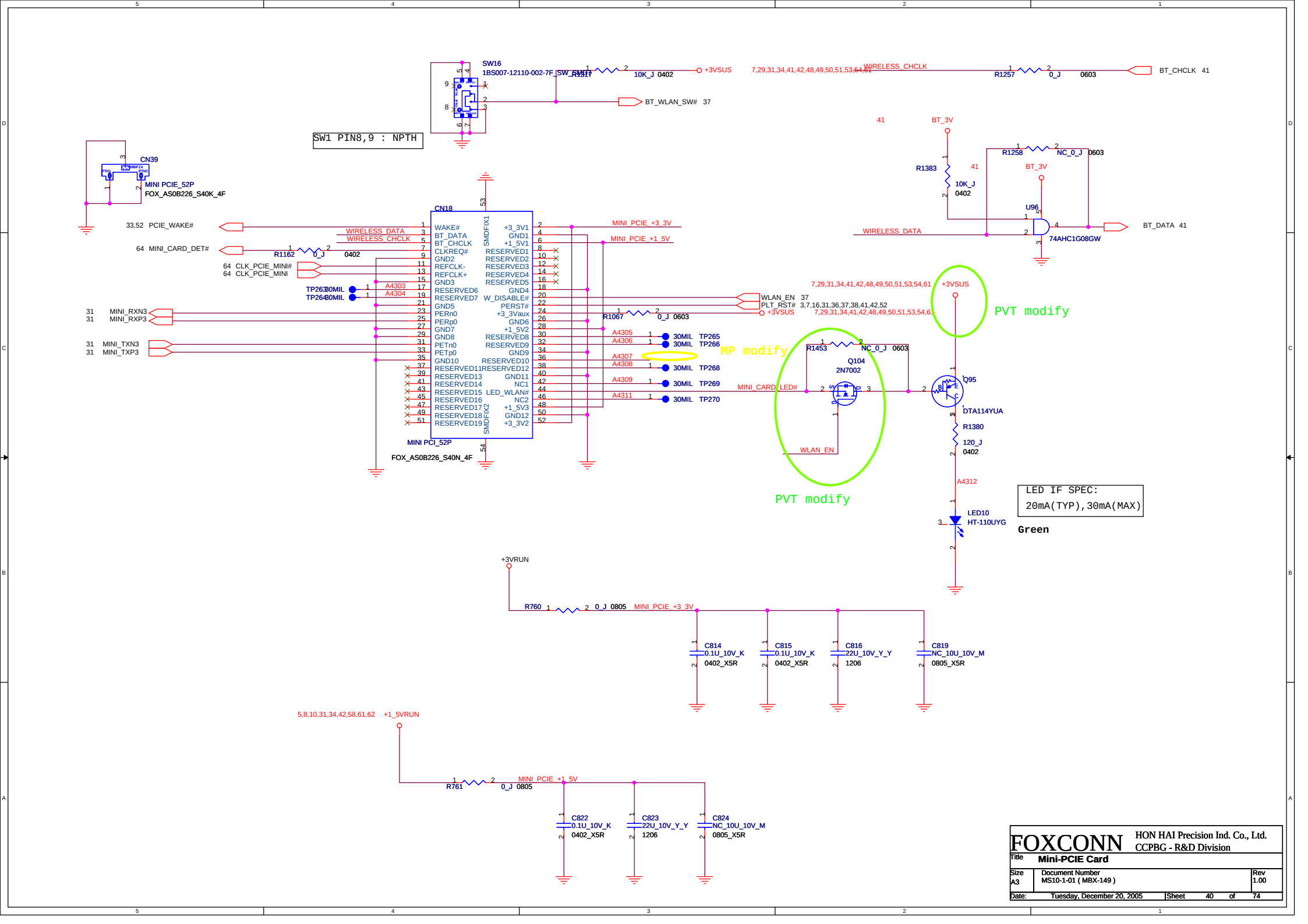


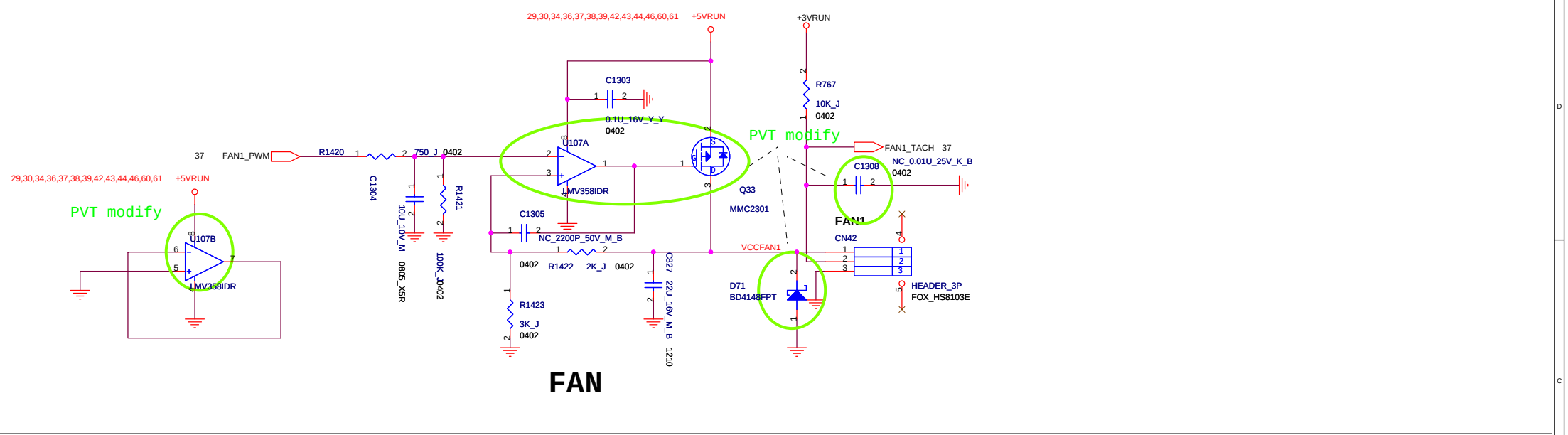


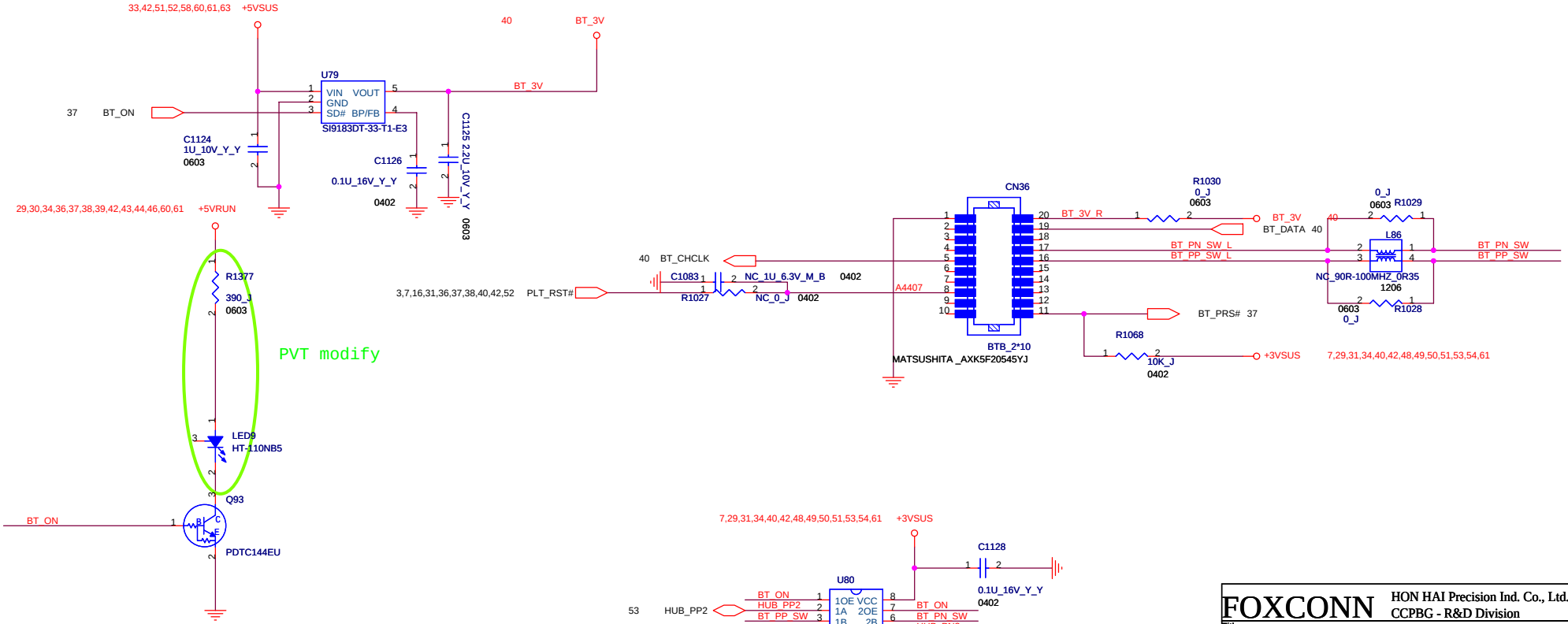




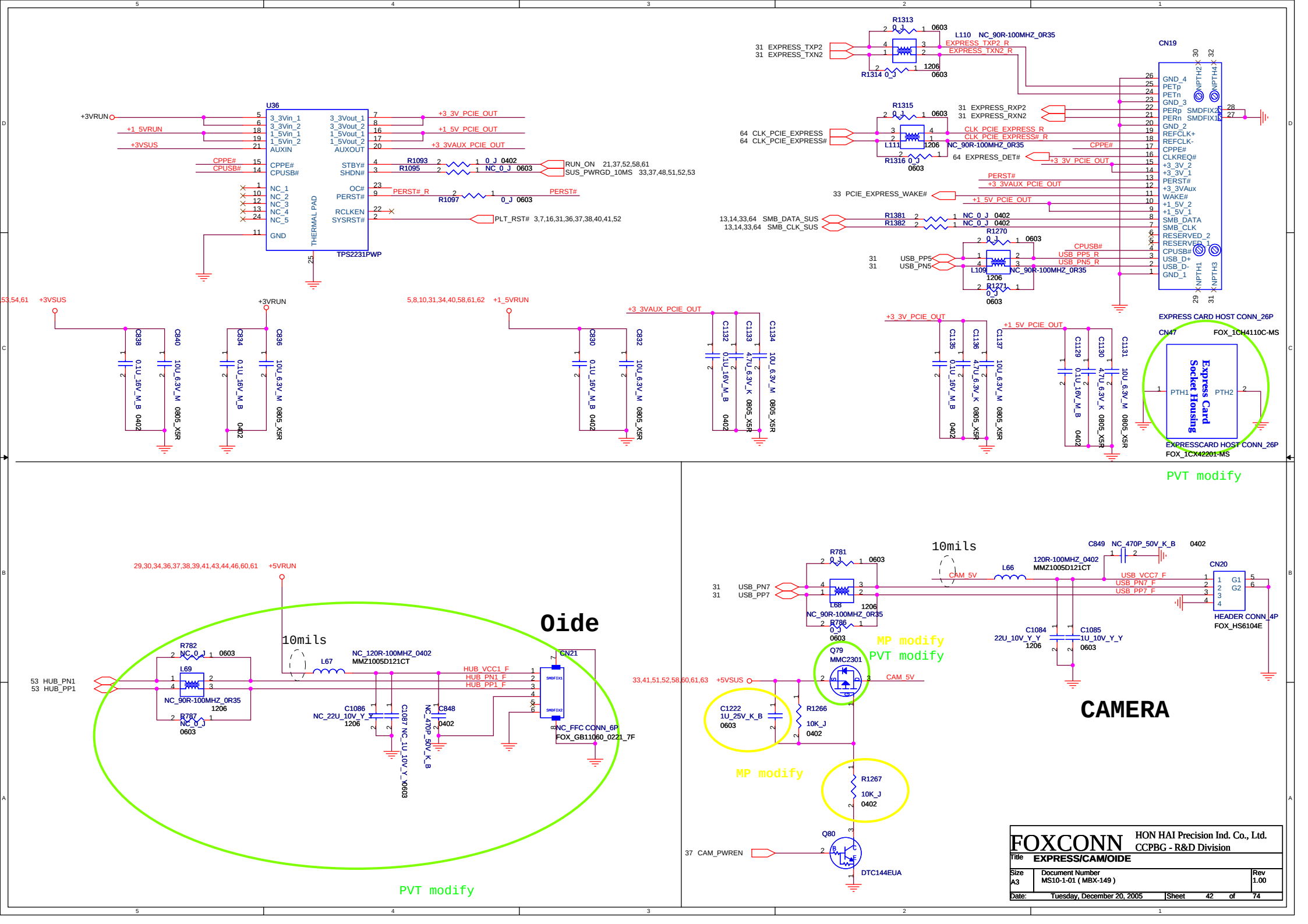
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	LED/LID SW#/Touch PAD		
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 39 of 74		

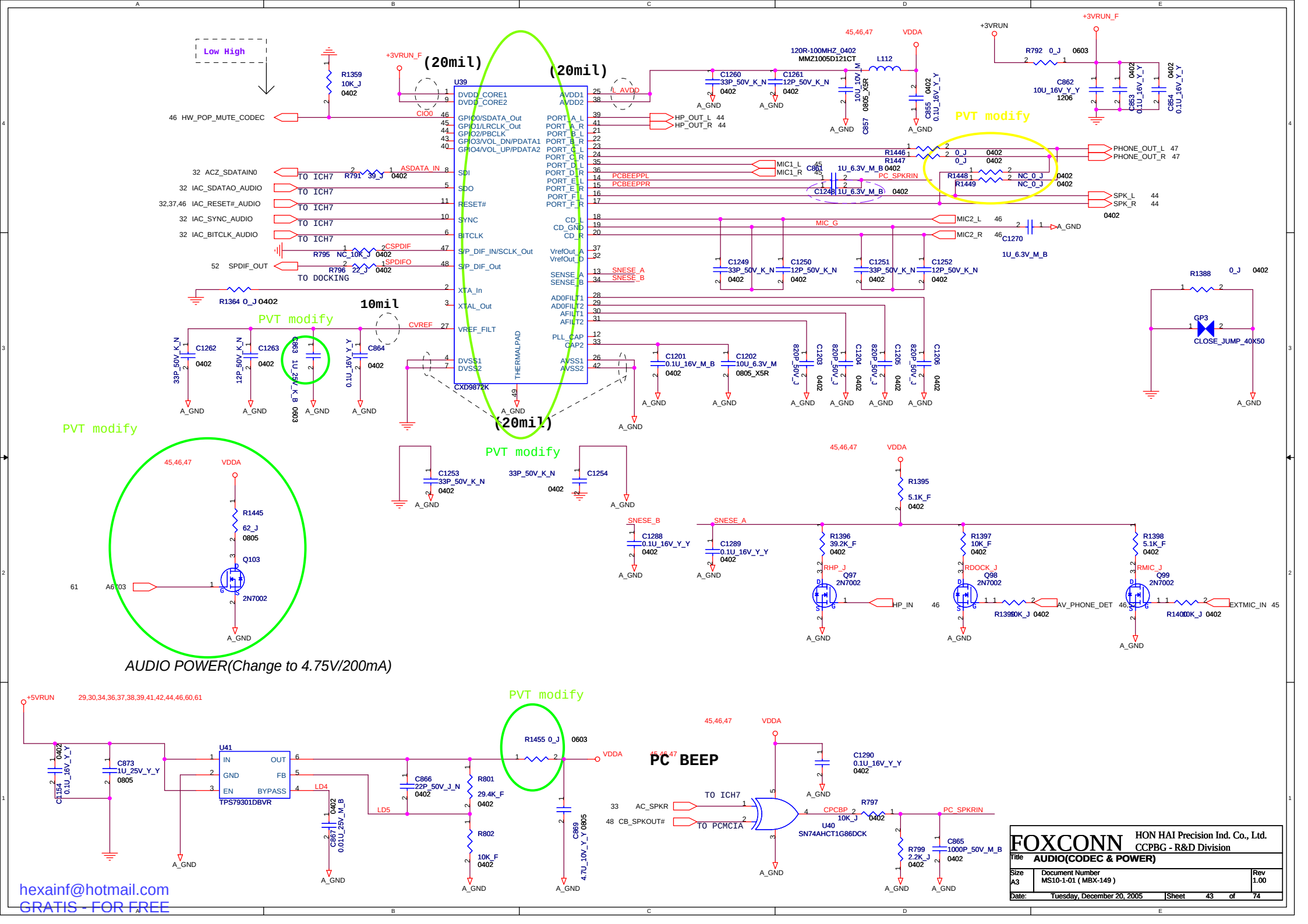

SW16
1BS007-12110-002-7F_SW_SMD
10K_J 0402
+3VSUS
BT_WLAN_SW# 37
SW1 PIN8,9 : NPTH
7,29,31,34,41,42,48,49,50,51,53,54,61
WIRELESS_CHCLK
R1257
0_J 0603
BT_CHCLK 41
41
BT_3V
R1258
NC_0_J 0603
R1383
10K_J
0402
U96
74AHC1G08GW
WIRELESS_DATA
BT_DATA 41
CN39
MINI PCIE_52P
FOX_AS0B226_S40K_4F
CN18
33,52 PCIE_WAKE#
64 MINI_CARD_DET#
R1162
0_J 0402
64 CLK_PCIE_MINI#
64 CLK_PCIE_MINI
TP263 30MIL
TP264 30MIL
A4303
A4304
31 MINI_RXN3
31 MINI_RXP3
31 MINI_TXN3
31 MINI_TXP3
WAKE#
BT_DATA
BT_CHCLK
CLKREQ#
GND2
REFCLK-
REFCLK+
GND3
RESERVED6
RESERVED7
GND5
PERn0
PERp0
GND7
GND8
PETn0
PETp0
GND10
RESERVED11
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18
RESERVED19
+3_3V1
GND1
+1_5V1
RESERVED1
RESERVED2
RESERVED3
RESERVED4
RESERVED5
GND4
W_DISABLE#
PERST#
+3_3Vaux
GND6
+1_5V2
RESERVED8
RESERVED9
GND9
RESERVED10
RESERVED12
GND11
NC1
LED_WLAN#
NC2
+1_5V3
GND12
+3_3V2
SMDFIX1
SMDFIX2
MINI PCI_52P
FOX_AS0B226_S40N_4F
MINI_PCIE_+3_3V
MINI_PCIE_+1_5V
R1067
0_J 0603
WLAN_EN 37
PLT_RST# 3,7,16,31,36,37,38,41,42,52
+3VSUS
7,29,31,34,41,42,48,49,50,51,53,54,61
A4305
A4306
A4307
A4308
A4309
A4311
30MIL TP265
30MIL TP266
30MIL TP268
30MIL TP269
30MIL TP270
MP modify
R1453
NC_0_J 0603
Q104
2N7002
MINI_CARD_LED#
WLAN_EN
Q95
DTA114YUA
R1380
120_J
0402
A4312
LED10
HT-110UYG
Green
LED IF SPEC:
20mA(TYP),30mA(MAX)
PVT modify
PVT modify
+3VRUN
R760
0_J 0805
MINI_PCIE_+3_3V
C814
0.1U_10V_K
0402_X5R
C815
0.1U_10V_K
0402_X5R
C816
22U_10V_Y_Y
1206
C819
NC_10U_10V_M
0805_X5R
5,8,10,31,34,42,58,61,62 +1_5VRUN
R761
0_J 0805
MINI_PCIE_+1_5V
C822
0.1U_10V_K
0402_X5R
C823
22U_10V_Y_Y
1206
C824
NC_10U_10V_M
0805_X5R
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
Mini-PCIE Card
Size
A3
Document Number
MS10-1-01 (MBX-149)
Rev
1.00
Date:
Tuesday, December 20, 2005
Sheet
40
of
74

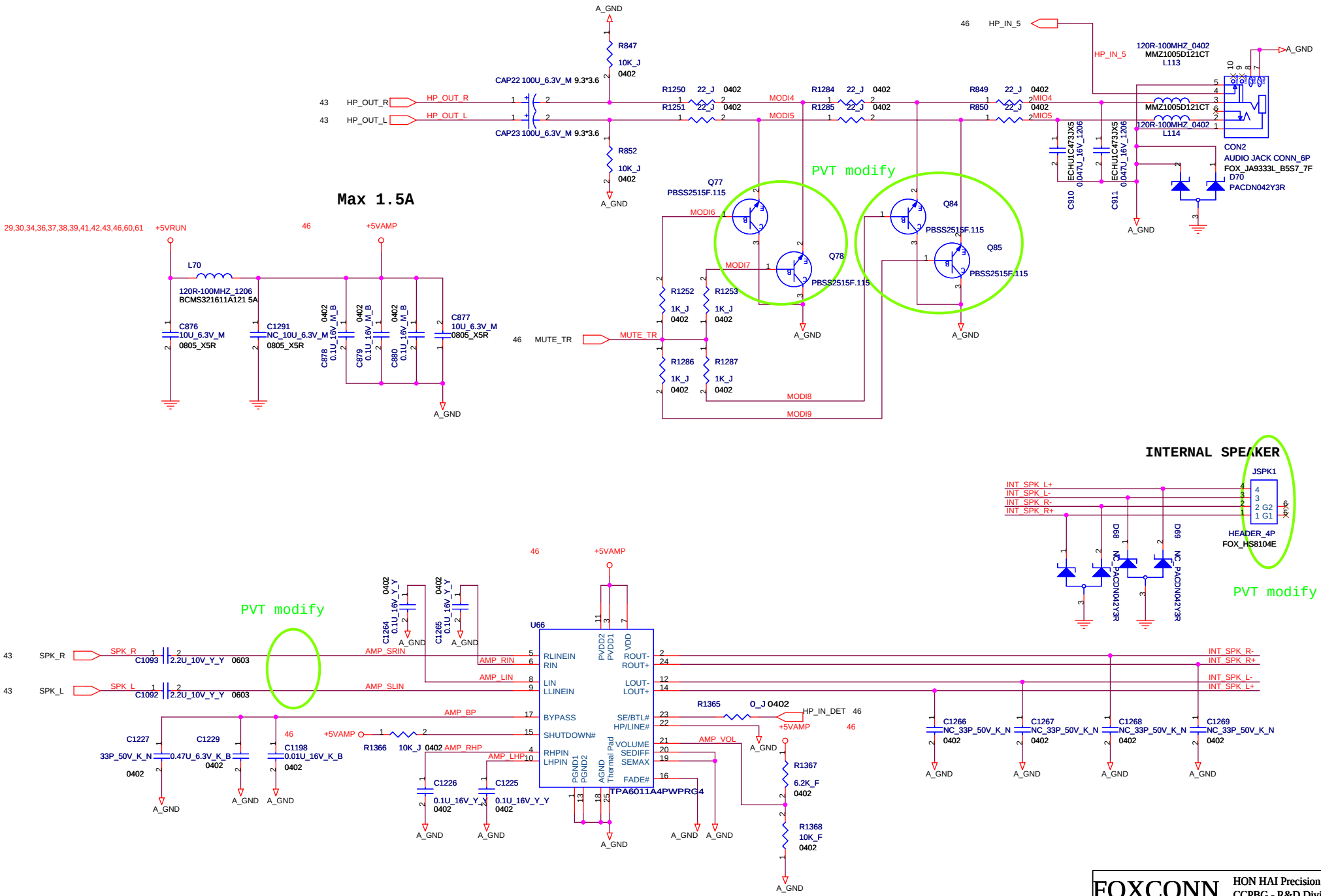




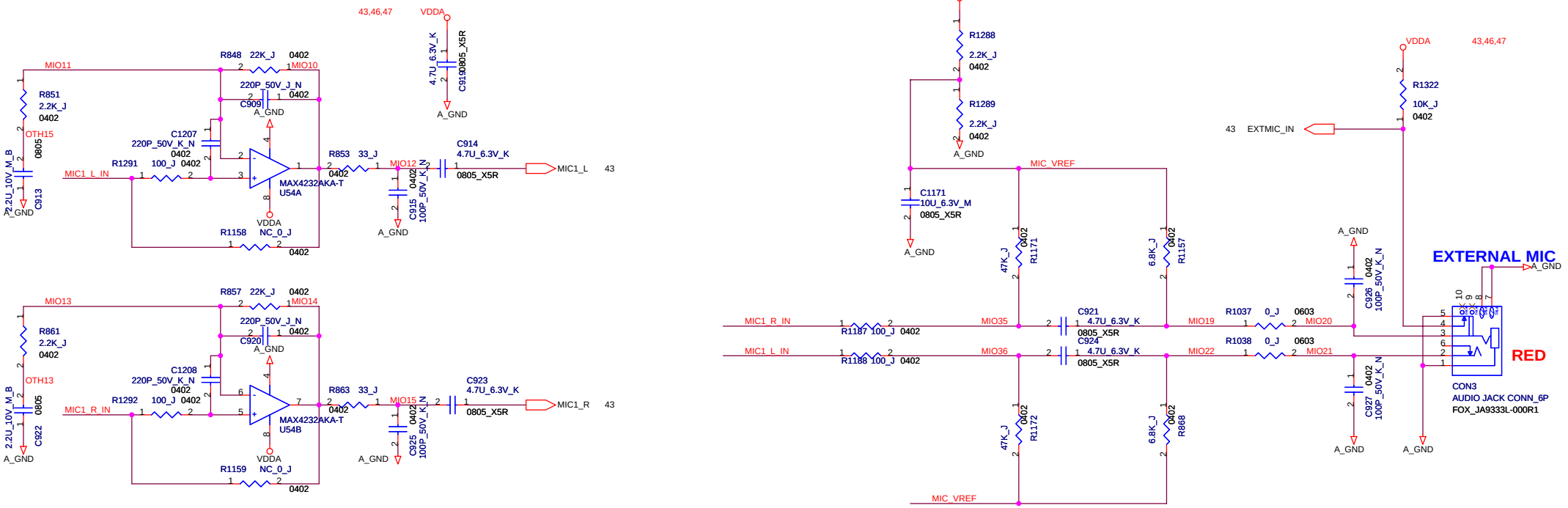
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN/Bluetooth	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 41 of 74	


U36
TPS2231PWP
+3VRUN
+1_5VRUN
+3VSUS
+3_3V_PCIE_OUT
+1_5V_PCIE_OUT
+3_3VAUX_PCIE_OUT
CPPE#
CPUSB#
STBY#
SHDN#
OC#
PERST#
RCLKEN
SYSRST#
THERMAL PAD
RUN_ON 21,37,52,58,61
SUS_PWRGD_10MS 33,37,48,51,52,53
PERST# R
PLT_RST# 3,7,16,31,36,37,38,40,41,52
CN19
EXPRESS_TXP2
EXPRESS_TXN2
EXPRESS_RXP2
EXPRESS_RXN2
CLK_PCIE_EXPRESS
CLK_PCIE_EXPRESS#
EXPRESS_DET#
PCIE_EXPRESS_WAKE#
SMB_DATA_SUS
SMB_CLK_SUS
USB_PP5
USB_PN5
EXPRESS CARD HOST CONN_26P
CN47
FOX_1CH4110C-MS
Express Card Socket Housing
EXPRESSCARD HOST CONN_26P
FOX_1CX42201-MS
PVT modify
10mils
L67
NC_120R-100MHZ_0402
MMZ1005D121CT
HUB_VCC1_F
HUB_PN1_F
HUB_PP1_F
CN21
NC_FFC CONN_6P
FOX_GB11060_0221_7F
HUB_PN1
HUB_PP1
PVT modify
Oide
10mils
L66
120R-100MHZ_0402
MMZ1005D121CT
CAM_5V
USB_VCC7_F
USB_PN7_F
USB_PP7_F
CN20
HEADER CONN_4P
FOX_HS6104E
MP modify
PVT modify
Q79
MMC2301
MP modify
Q80
DTC144EUA
CAM_PWREN
CAMERA
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title EXPRESS/CAM/OIDE
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 42 of 74

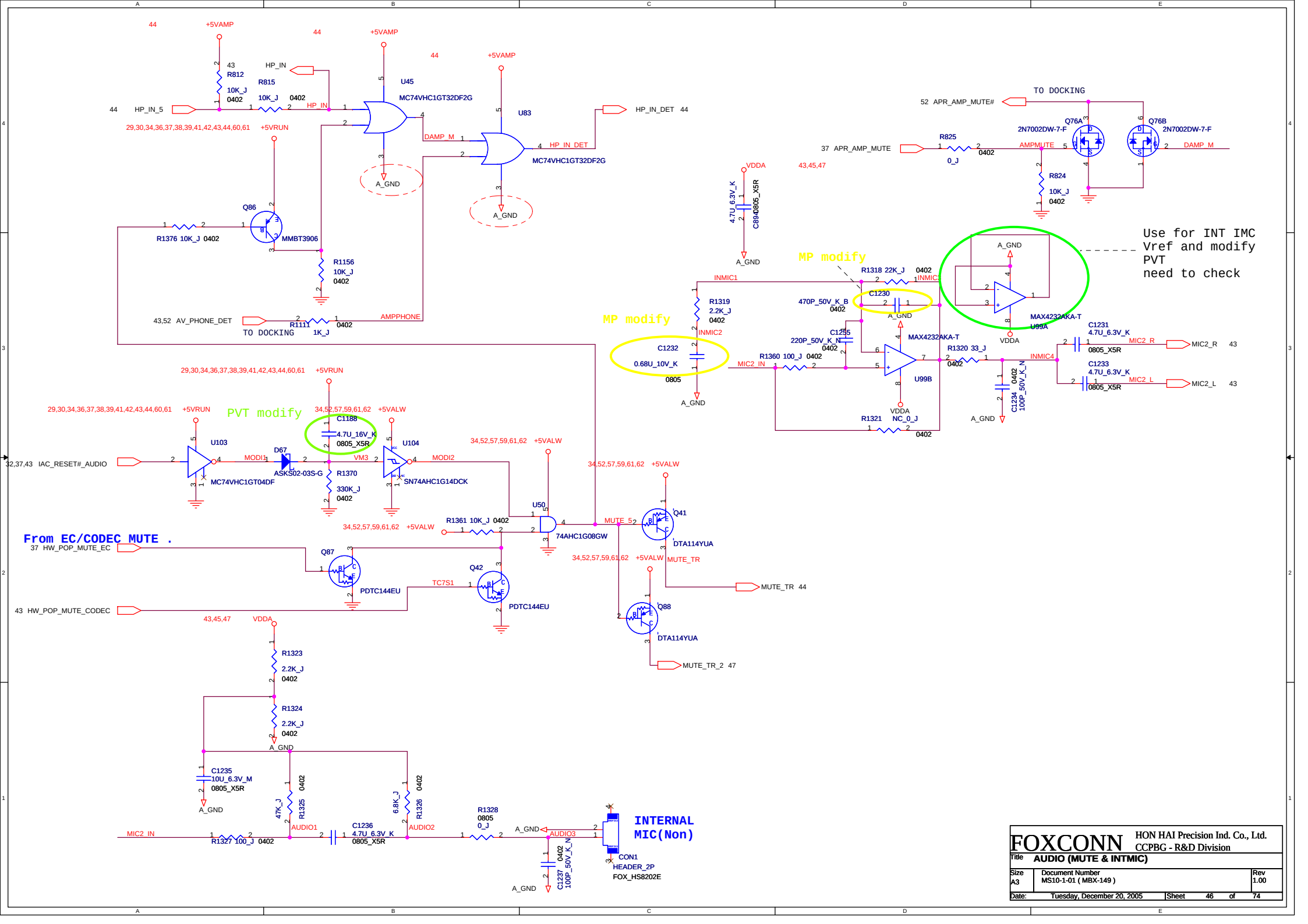

Low High
R1359 10K_J 0402
46 HW_POP_MUTE_CODEC
+3VRUN_F
(20mil)
CI00
U39
CXD9872K
DVDD_CORE1
DVDD_CORE2
GPIO0/SDATA_Out
GPIO1/LRCLK_Out
GPIO2/PBCLK
GPIO3/VOL_DN/PDATA1
GPIO4/VOL_UP/PDATA2
SDI
SDO
RESET#
SYNC
BITCLK
S/P_DIF_IN/SCLK_Out
S/P_DIF_Out
XTA_In
XTAL_Out
VREF_FILT
DVSS1
DVSS2
THERMALPAD
AVDD1
AVDD2
PORT_A_L
PORT_A_R
PORT_B_L
PORT_B_R
PORT_C_L
PORT_C_R
PORT_D_L
PORT_D_R
PORT_E_L
PORT_E_R
PORT_F_L
PORT_F_R
CD_L
CD_GND
CD_R
VrefOut_A
VrefOut_D
SENSE_A
SENSE_B
AD0FILT1
AD0FILT2
AFILT1
AFILT2
PLL_CAP
CAP2
AVSS1
AVSS2
L_AVDD
32 ACZ_SDATAIN0
32 IAC_SDATAO_AUDIO
32,37,46 IAC_RESET#_AUDIO
32 IAC_SYNC_AUDIO
32 IAC_BITCLK_AUDIO
52 SPDIF_OUT
TO ICH7
TO DOCKING
ASDATA_IN
R791 33_J 0402
R795 NC_10K_J 0402
R796 22_J 0402
CSPDIF
SPDIFO
R1364 0_J 0402
10mil
PVT modify
CVREF
C1262 33P_50V_K_N 0402
C1263 12P_50V_K_N 0402
C863 1U_25V_K_B 0603
C864 0.1U_16V_Y_Y 0402
A_GND
(20mil)
L_AVDD
45,46,47
VDDA
120R-100MHZ_0402
MMZ1005D121CT
L112
C1260 33P_50V_K_N 0402
C1261 12P_50V_K_N 0402
C857 10U_10V_M 0805_X5R
C855 0.1U_16V_Y_Y 0402
HP_OUT_L 44
HP_OUT_R 44
+3VRUN
+3VRUN_F
R792 0_J 0603
C862 10U_16V_Y_Y 1206
C853 0.1U_16V_Y_Y 0402
C854 0.1U_16V_Y_Y 0402
PVT modify
R1446 0_J 0402
R1447 0_J 0402
PHONE_OUT_L 47
PHONE_OUT_R 47
MIC1_L
MIC1_R
C861 1U_6.3V_M_B 0402
PCBEEPPL
PCBEEPPR
PC_SPKRIN
C1248 1U_6.3V_M_B 0402
R1448 NC_0_J 0402
R1449 NC_0_J 0402
SPK_L 44
SPK_R 44
MIC_G
MIC2_L 46
MIC2_R 46
C1270 1U_6.3V_M_B
C1249 33P_50V_K_N 0402
C1250 12P_50V_K_N 0402
C1251 33P_50V_K_N 0402
C1252 12P_50V_K_N 0402
SNESE_A
SNESE_B
R1388 0_J 0402
GP3
CLOSE_JUMP_40X50
C1201 0.1U_16V_M_B 0402
C1202 10U_6.3V_M 0805_X5R
820P_50V_J 0402
C1203
C1204
C1205
C1206
PVT modify
45,46,47
VDDA
R1445 62_J 0805
Q103
61 A6703
2N7002
C1253 33P_50V_K_N 0402
C1254 33P_50V_K_N 0402
R1395 5.1K_F 0402
C1288 0.1U_16V_Y_Y 0402
C1289 0.1U_16V_Y_Y 0402
R1396 39.2K_F 0402
R1397 10K_F 0402
R1398 5.1K_F 0402
RHP_J
RDOCK_J
RMIC_J
Q97 2N7002
Q98 2N7002
Q99 2N7002
HP_IN 46
AV_PHONE_DET 46
EXTMIC_IN 45
R1399 10K_J 0402
R1400 10K_J 0402
AUDIO POWER(Change to 4.75V/200mA)
+5VRUN
29,30,34,36,37,38,39,41,42,44,46,60,61
C1154 0.1U_16V_Y_Y 0402
C873 1U_25V_Y_Y 0805
U41
TPS79301DBVR
IN
GND
EN
OUT
FB
BYPASS
LD4
LD5
C867 0.01U_25V_M_B 0402
C866 22P_50V_J_N 0402
R801 29.4K_F 0402
R802 10K_F 0402
PVT modify
R1455 0_J 0603
VDDA
C869 4.7U_10V_Y 0805
PC BEEP
45,46,47
VDDA
C1290 0.1U_16V_Y_Y 0402
TO ICH7
TO PCMCIA
33 AC_SPKR
48 CB_SPKOUT#
CPCBP
R797 10K_J 0402
U40
SN74AHCT1G86DCK
PC_SPKRIN
R799 2.2K_J 0402
C865 1000P_50V_M_B 0402
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title AUDIO(CODEC & POWER)
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 43 of 74
hexainf@hotmail.com
GRATIS - FOR FREE



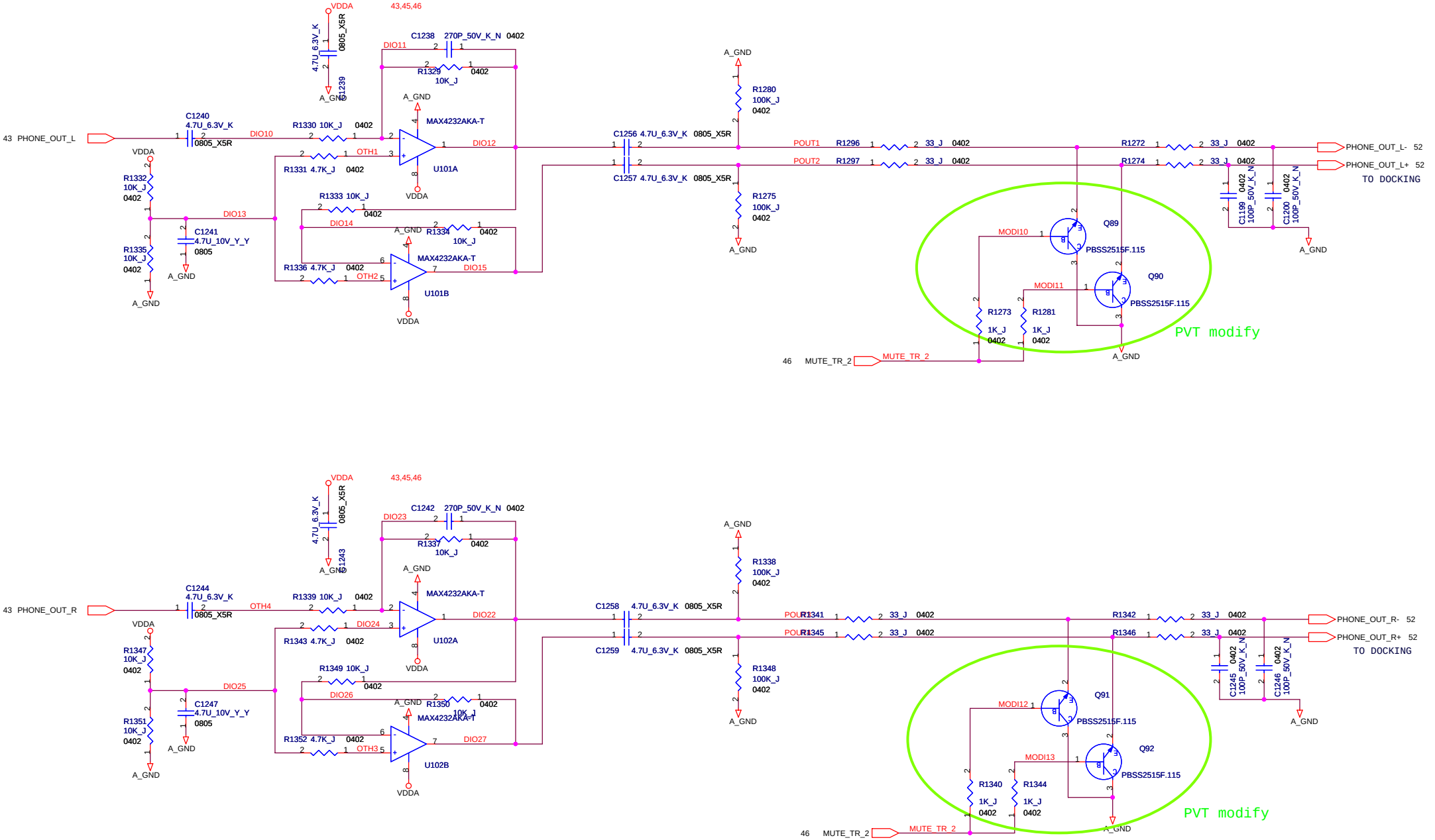
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO(AMP & HP & SPK)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 44 of 74	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO(EXT MIC & PHONE OUT)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 45 of 74	

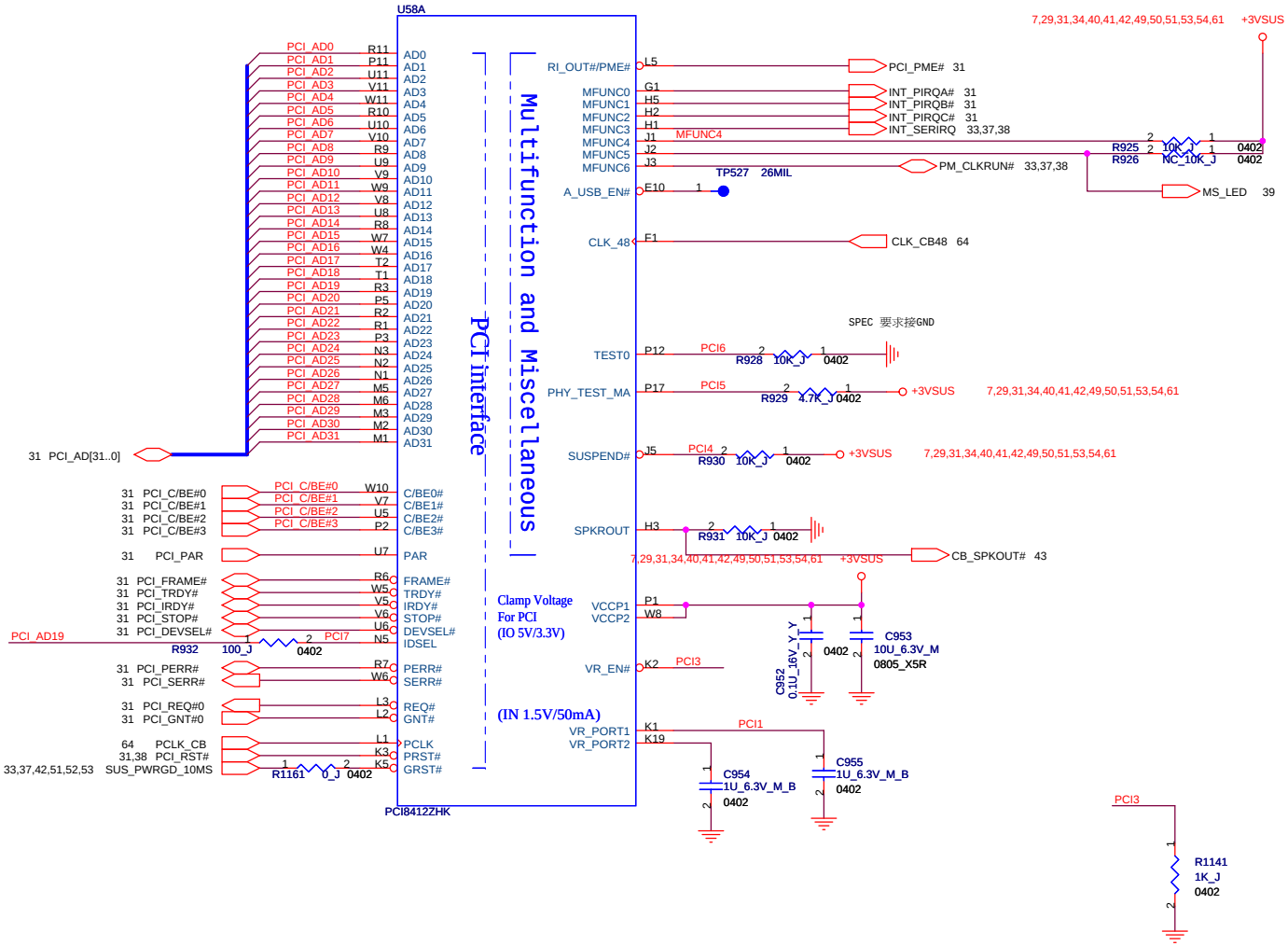


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	AUDIO (MUTE & INTMIC)
Size A3	Document Number MS10-1-01 (MBX-149) Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 46 of 74

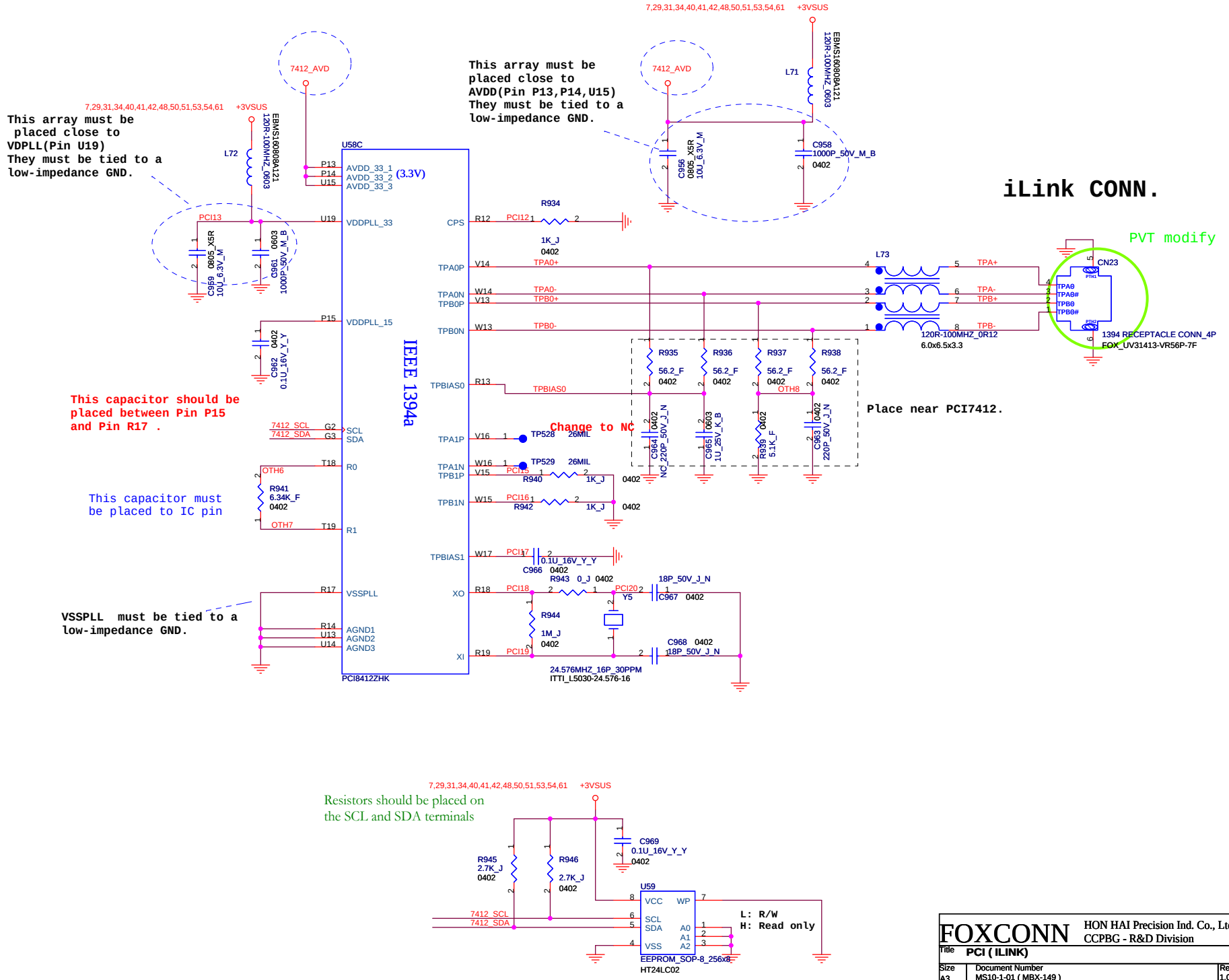


FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

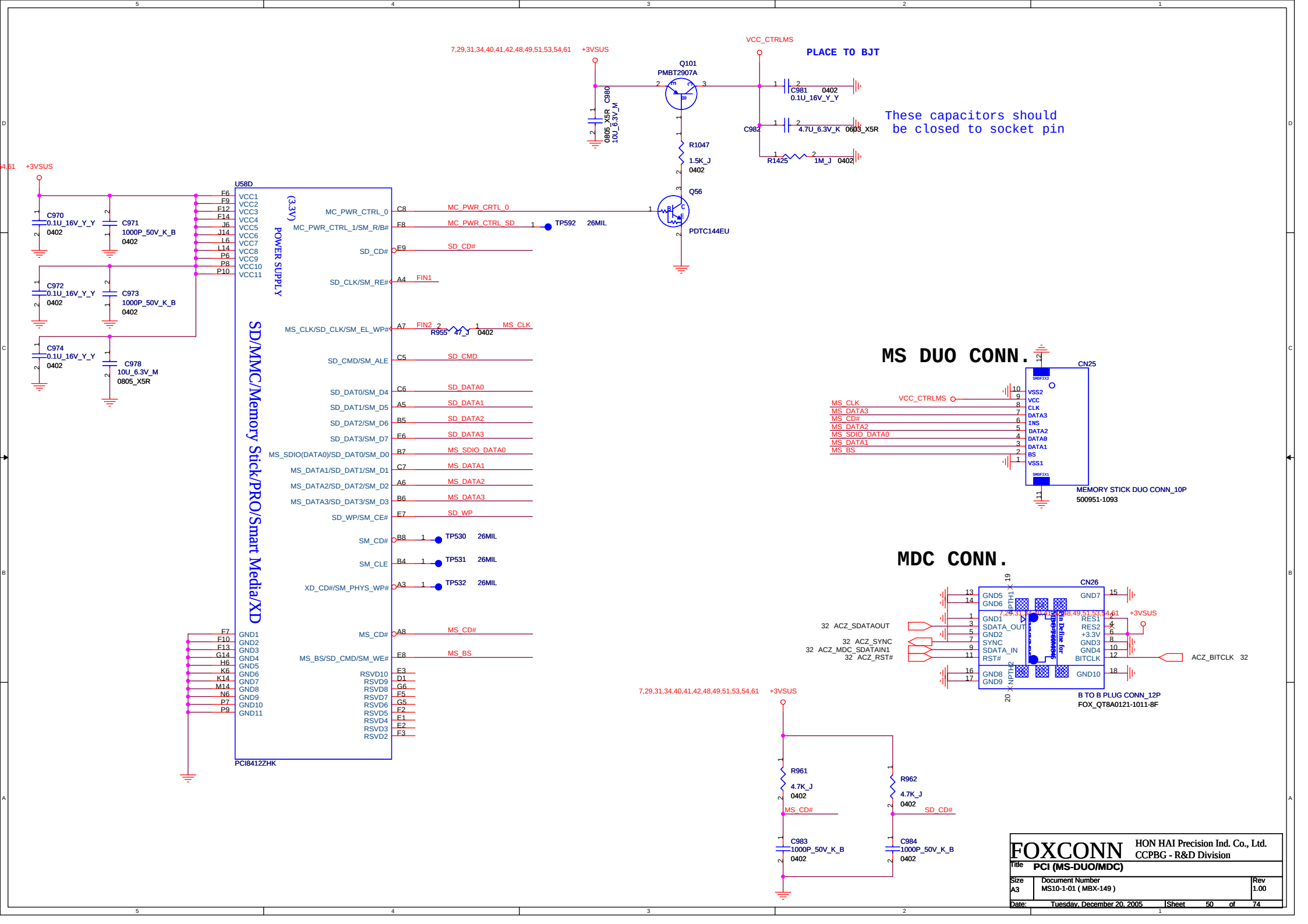
Title	AUDIO (PHONE OUT)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 47 of 74	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (PCI BUS)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 48 of 74	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (ILINK)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 49 of 74	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (MS-DUO/MDC)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
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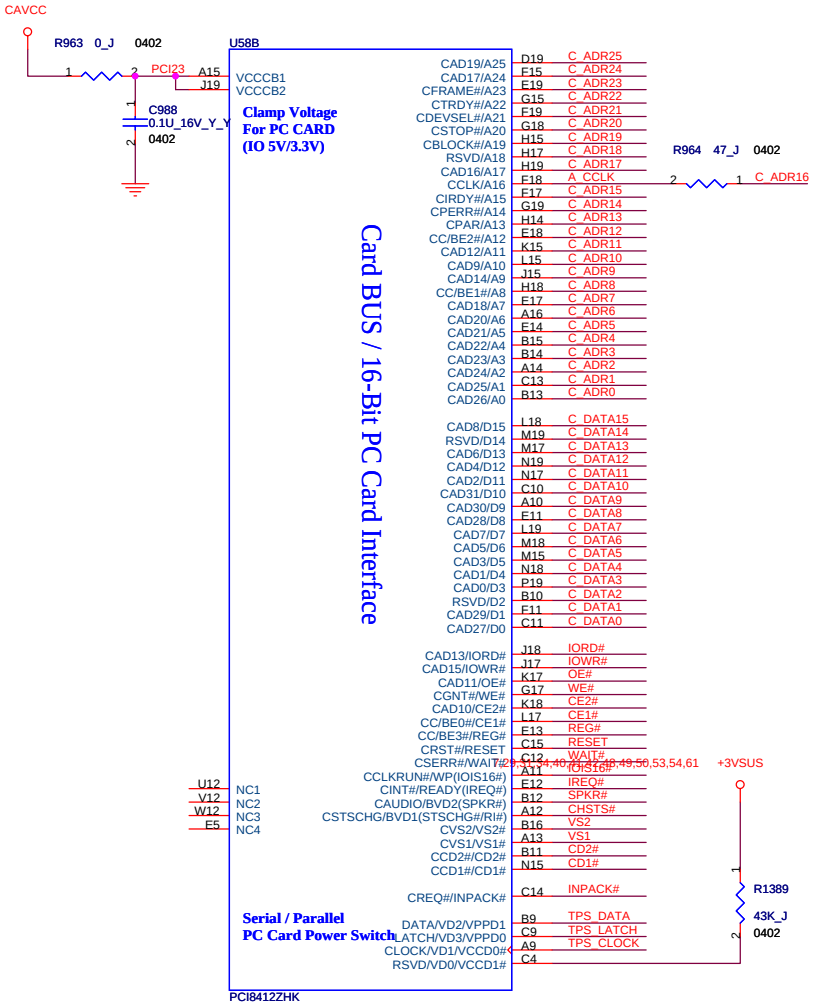
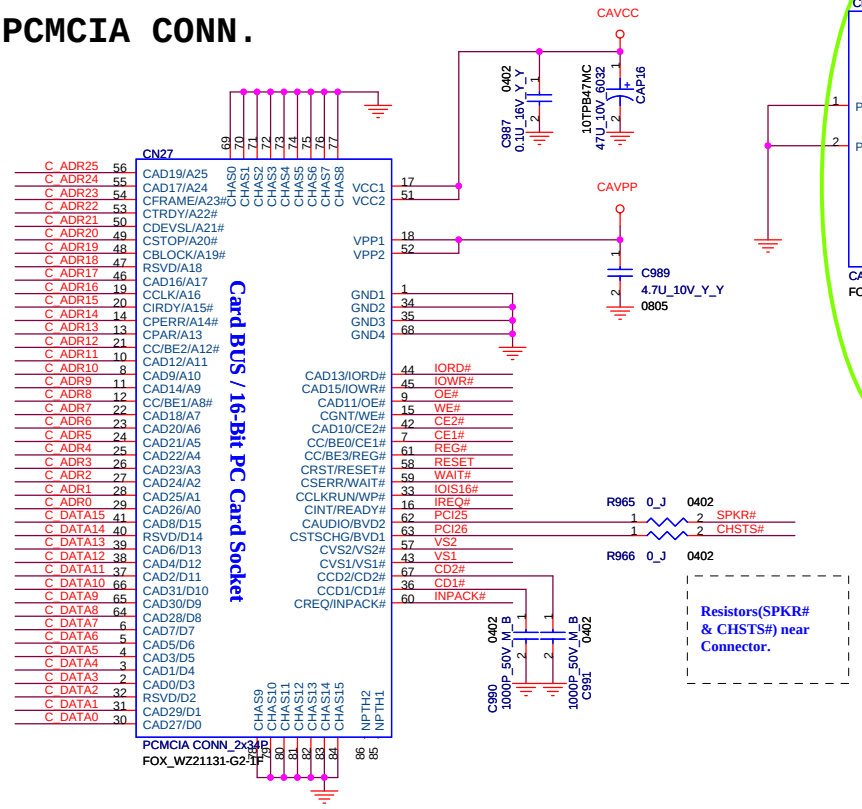
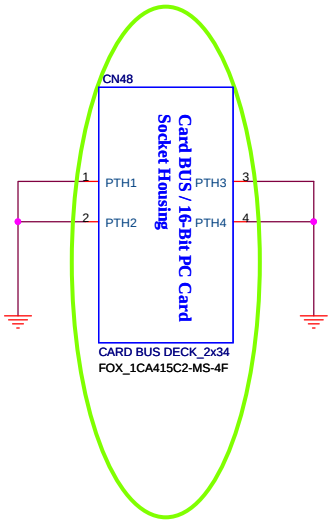
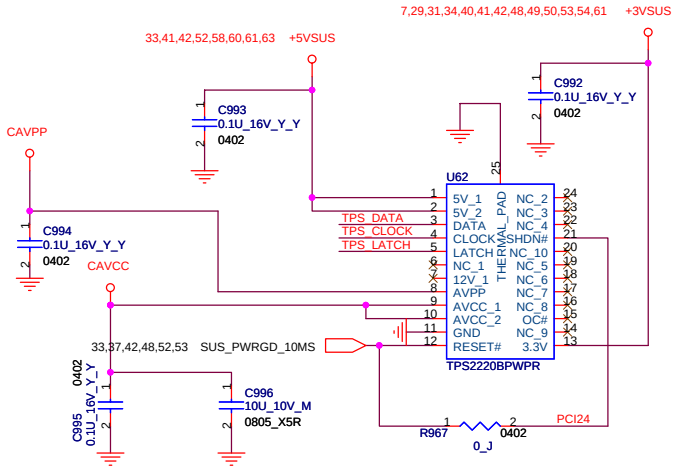
PVT modify

PCMCIA CONN.



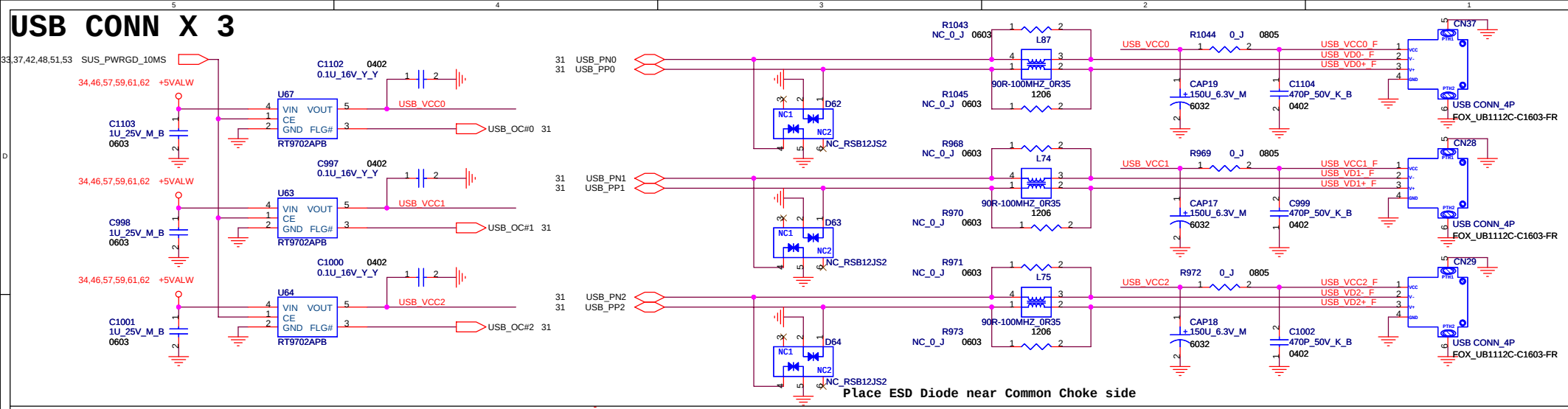


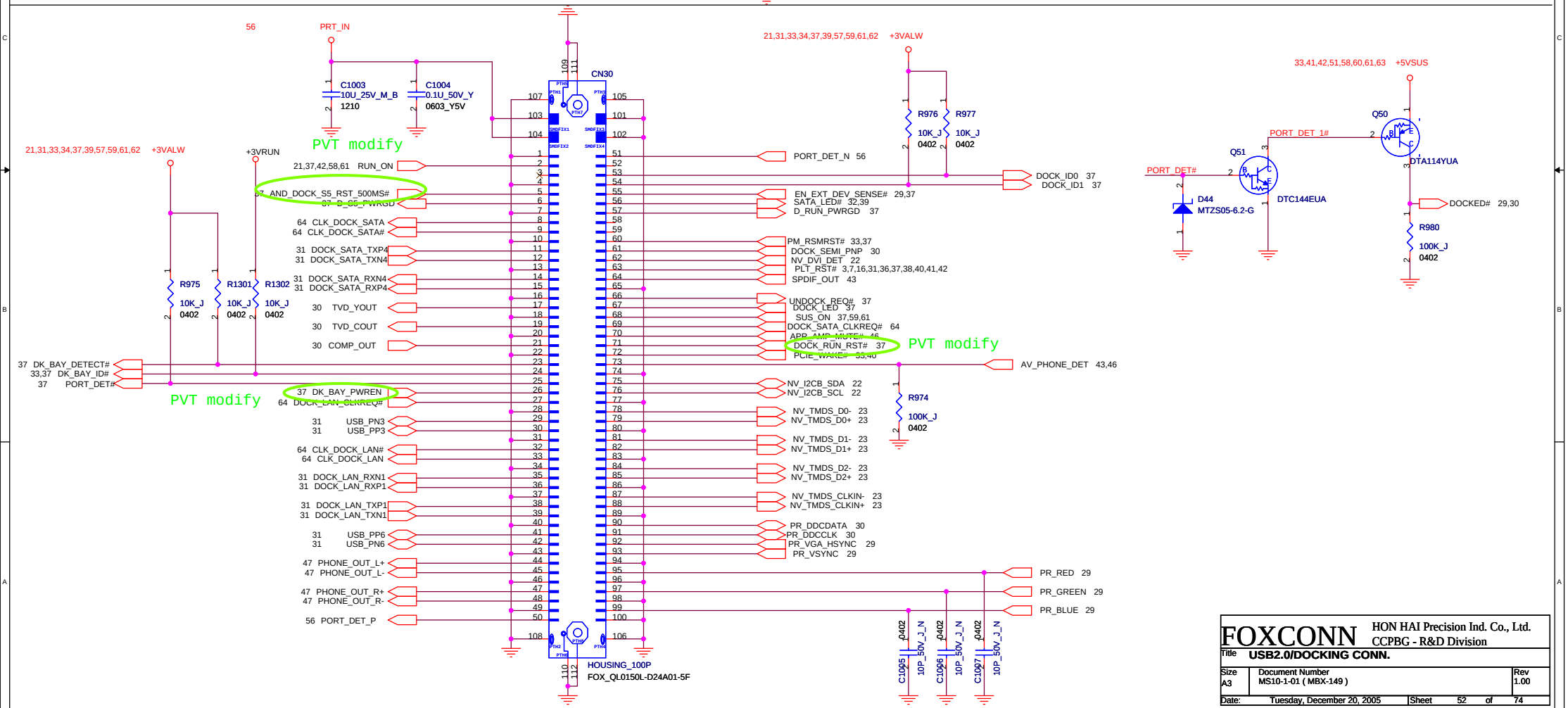




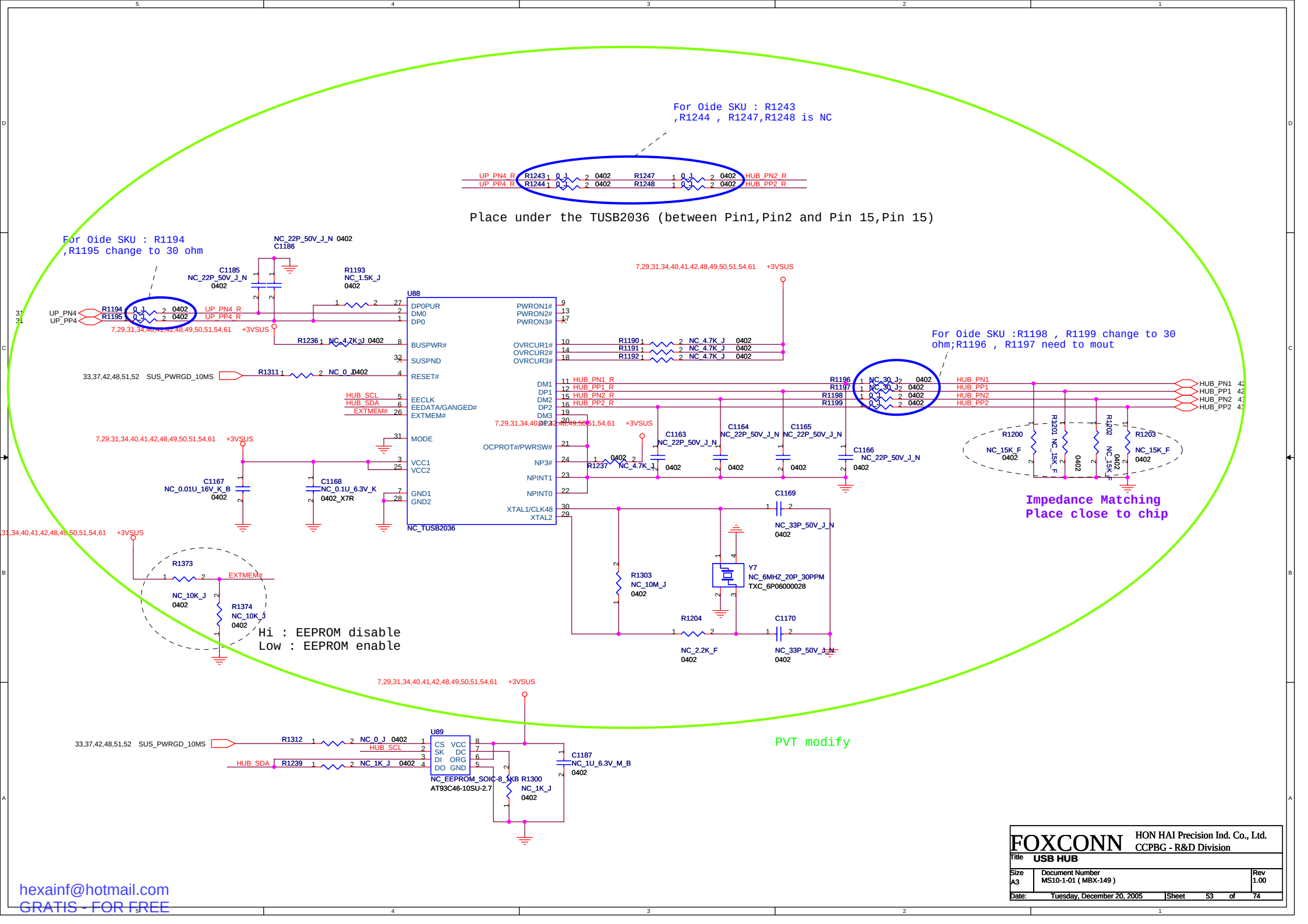
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (PCMCIA)	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 51 of 74	

USB CONN X 3





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB2.0/DOCKING CONN.	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 52 of 74	


For Oide SKU : R1243
,R1244 , R1247,R1248 is NC
Place under the TUSB2036 (between Pin1,Pin2 and Pin 15,Pin 15)
For Oide SKU : R1194
,R1195 change to 30 ohm
For Oide SKU :R1198 , R1199 change to 30 ohm;R1196 , R1197 need to mout
Impedance Matching
Place close to chip
Hi : EEPROM disable
Low : EEPROM enable
PVT modify
U88
NC_TUSB2036
U89
NC_EEPROM_SOIC-8_1KB
AT93C46-10SU-2.7
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title USB HUB
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 53 of 74
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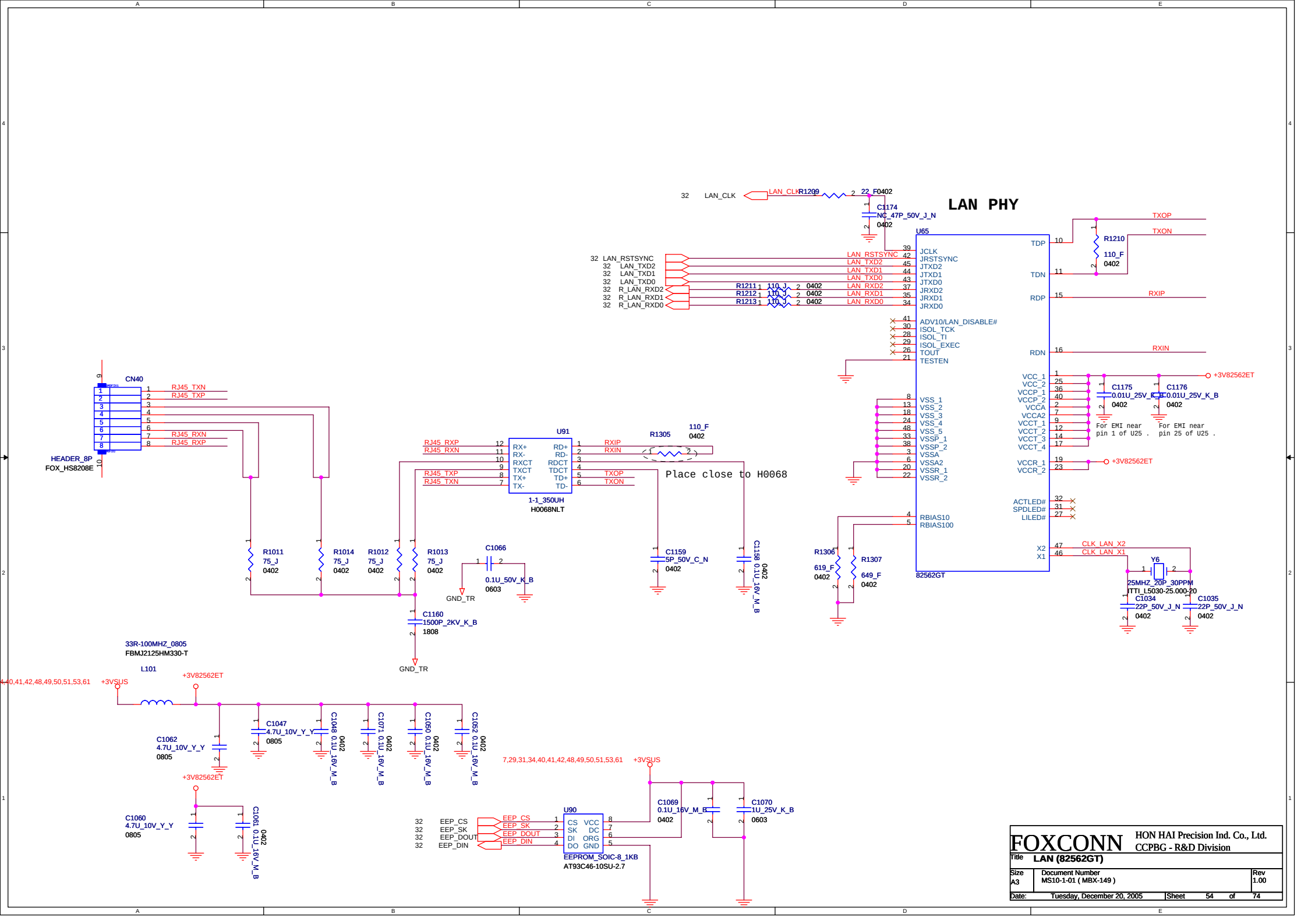
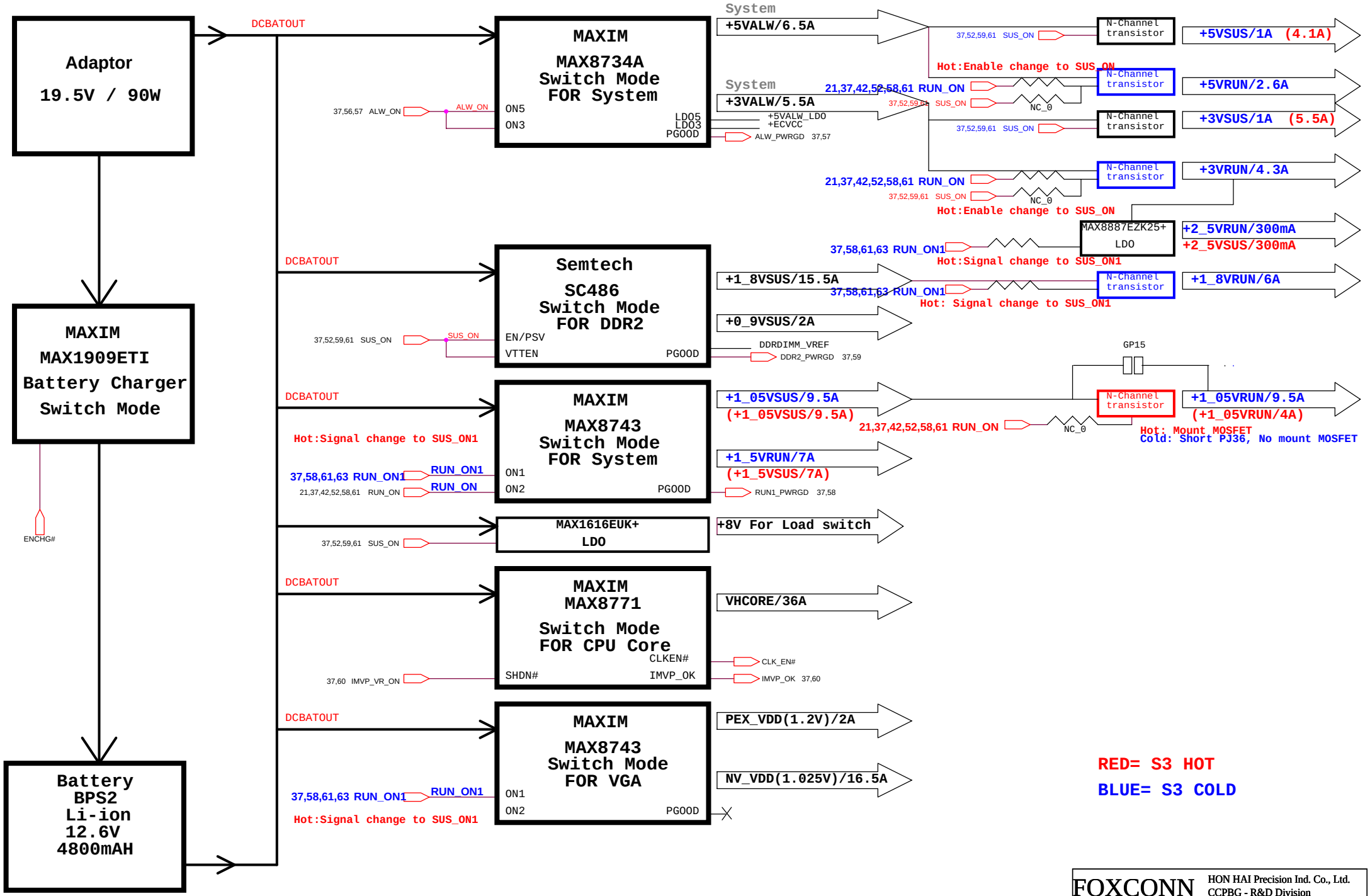


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	LAN (82562GT)		
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 54 of 74		



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Power Design Diagram-ZG		
Size A3	Document Number MBX-149		Rev 1.00
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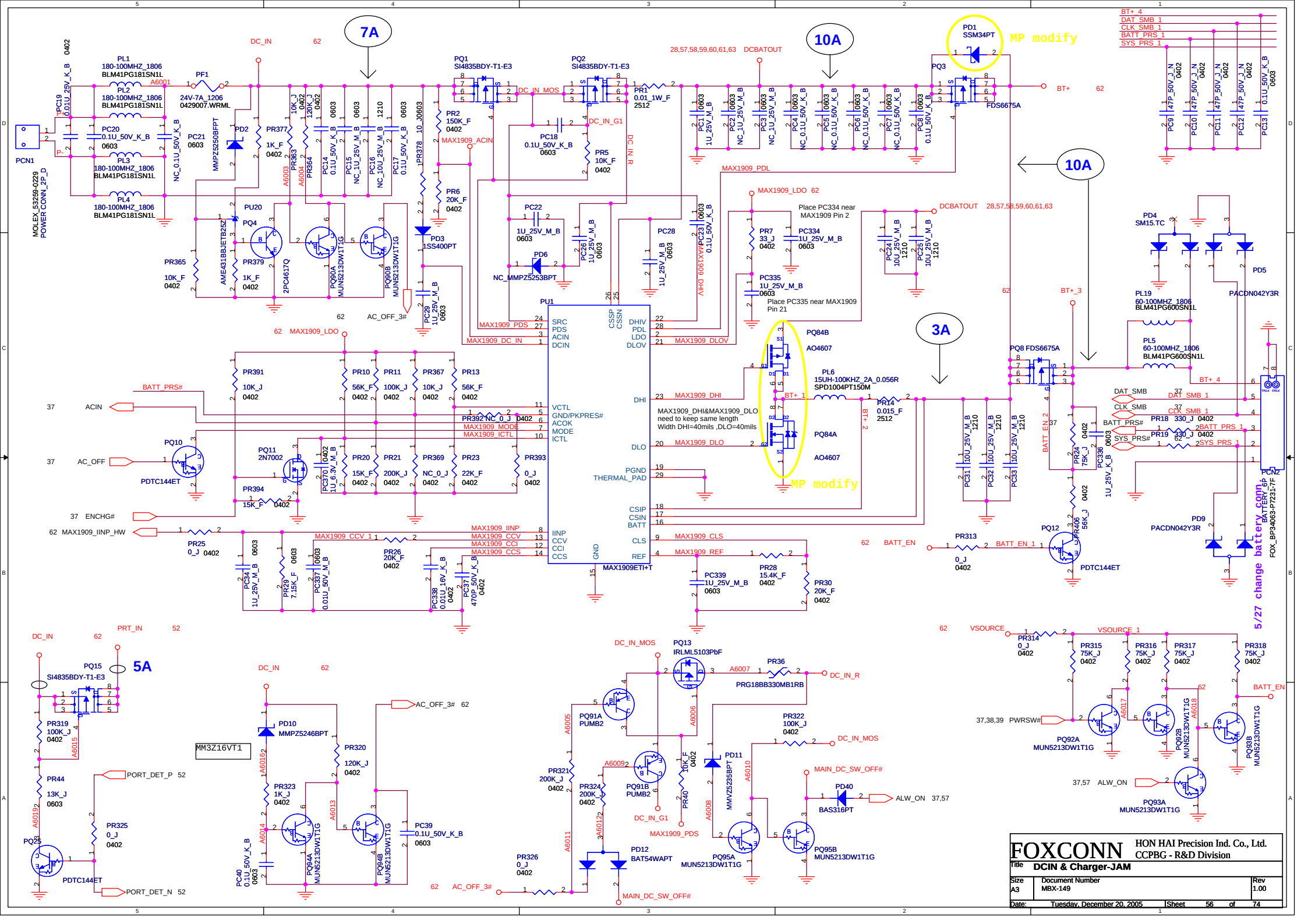
7A
10A
10A
3A
5A
DC_IN
PRT_IN
PCN1
MOLEX_53259-0229
POWER CONN_2P_D
PL1
180-100MHZ_1806
BLM41PG181SN1L
PL2
PL3
PL4
PF1
24V-7A_1206
0429007.WRML
PD2
MMPZ5250BFPT
PU20
AME4311BBJETB25Z
PQ4
2PC4617Q
PQ90A
MUN5213DW1T1G
PQ90B
PR365
10K_F
0402
PR379
1K_F
0402
PR377
1K_F
0402
PR378
10_J
0603
PR2
150K_F
0402
PR6
20K_F
0402
PD3
1SS400PT
PC29
1U_25V_M_B
0603
AC_OFF_3#
PQ1
SI4835BDY-T1-E3
PQ2
SI4835BDY-T1-E3
DC_IN_MOS
PR1
0.01_1W_F
2512
DC_IN_G1
PC18
0.1U_50V_K_B
0603
PR5
10K_F
0402
MAX1909_ACIN
MAX1909_PDS
MAX1909_DC_IN
MAX1909_LDO
MAX1909_PDL
PC22
1U_25V_M_B
0603
PD6
NC_MMPZ5253BPT
PC28
1U_25V_M_B
0603
PC23
0.1U_50V_K_B
0603
PU1
SRC
PDS
ACIN
DCIN
CSSP
CSSN
DHIV
PDL
LDO
DLOV
VCTL
GND/PKPRES#
ACOK
MODE
ICTL
DHI
DLO
PGND
THERMAL_PAD
CSIP
CSIN
BATT
CLS
REF
IINP
CCV
CCI
CCS
GND
MAX1909ETI+T
MAX1909_DHI
MAX1909_DLO
MAX1909_DLOV
MAX1909_DHI&MAX1909_DLO
need to keep same length
Width DHI=40mils ,DLO=40mils
MAX1909_MODE
MAX1909_ICTL
MAX1909_IINP
MAX1909_CCV
MAX1909_CCI
MAX1909_CCS
MAX1909_CLS
MAX1909_REF
MAX1909_IINP_HW
Place PC334 near
MAX1909 Pin 2
PC334
1U_25V_M_B
0603
PR7
33_J
0402
PC335
1U_25V_M_B
0603
Place PC335 near MAX1909
Pin 21
PQ84B
AO4607
PQ84A
AO4607
PL6
15UH-100KHZ_2A_0.056R
SPD1004PT150M
PR14
0.015_F
2512
MP modify
PD1
SSM34PT
MP modify
PQ3
FDS6675A
PQ8 FDS6675A
PD4
SM15.TC
PD5
PACDN042Y3R
PL19
60-100MHZ_1806
BLM41PG600SN1L
PL5
60-100MHZ_1806
BLM41PG600SN1L
PD9
PACDN042Y3R
PCN2
BATTERY_6P
FOX_BP34063-P7231-7F
PR391
10K_J
0402
PR10
56K_F
0402
PR11
100K_J
0402
PR367
10K_J
0402
PR13
56K_F
0402
PR392 NC_0_J 0402
PR20
15K_F
0402
PR21
200K_J
0402
PR369
NC_0_J
0402
PR23
22K_F
0402
PR393
0_J
0402
PR394
15K_F
0402
PR25
0_J 0402
PR26
20K_F
0402
PR28
15.4K_F
0402
PR30
20K_F
0402
PC339
1U_25V_M_B
0603
PC34
1U_25V_M_B
0603
PR29
7.15K_F
0603
PC337
0.01U_50V_M_B
0603
PC338
0.01U_16V_K_B
0402
PC371
470P_50V_K_B
0402
PC370
1U_6.3V_M_B
0402
PQ10
PDTC144ET
PQ11
2N7002
BATT_PRS#
ACIN
AC_OFF
ENCHG#
PR313
0_J
0402
BATT_EN_1
PQ12
PDTC144ET
BATT_EN
PR24
75K_J
0402
PC336
1U_25V_K_B
0603
PC31
10U_25V_M_B
1210
PC32
10U_25V_M_B
1210
PC33
10U_25V_M_B
1210
BATT_EN_2
PR18 330_J 0402
PR19 330_J 0402
DAT_SMB
CLK_SMB
BATT_PRS_1
SYS_PRS_1
BT+_3
BT+_4
BT+_2
BT+_1
BT+
DCBATOUT
28,57,58,59,60,61,63
PQ15
SI4835BDY-T1-E3
PR319
100K_J
0402
PR44
13K_J
0603
PR325
0_J
0402
PQ25
PDTC144ET
PORT_DET_P
PORT_DET_N
PD10
MMPZ5246BPT
MM3Z16VT1
PR320
120K_J
0402
PR323
1K_J
0402
PC39
0.1U_50V_K_B
0603
PC40
0.1U_50V_K_B
0603
PQ94A
MUN5213DW1T1G
PQ94B
MUN5213DW1T1G
PR326
0_J
0402
AC_OFF_3#
MAIN_DC_SW_OFF#
PQ13
IRLML5103PbF
PR36
PRG18BB330MB1RB
DC_IN_R
PQ91A
PUMB2
PQ91B
PUMB2
PR321
200K_J
0402
PR324
200K_J
0402
PR322
100K_J
0402
PD11
MMVZ5235BPT
PD12
BAT54WAPT
PD40
BAS316PT
ALW_ON
PQ95A
MUN5213DW1T1G
PQ95B
MUN5213DW1T1G
VSOURCE
VSOURCE_1
PR314
0_J
0402
PR315
75K_J
0402
PR316
75K_J
0402
PR317
75K_J
0402
PR318
75K_J
0402
PWRSW#
PQ92A
MUN5213DW1T1G
PQ92B
MUN5213DW1T1G
PQ93A
MUN5213DW1T1G
PQ93B
MUN5213DW1T1G
ALW_ON
5/27 change battery conn.
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
DCIN & Charger-JAM
Size
A3
Document Number
MBX-149
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1.00
Date:
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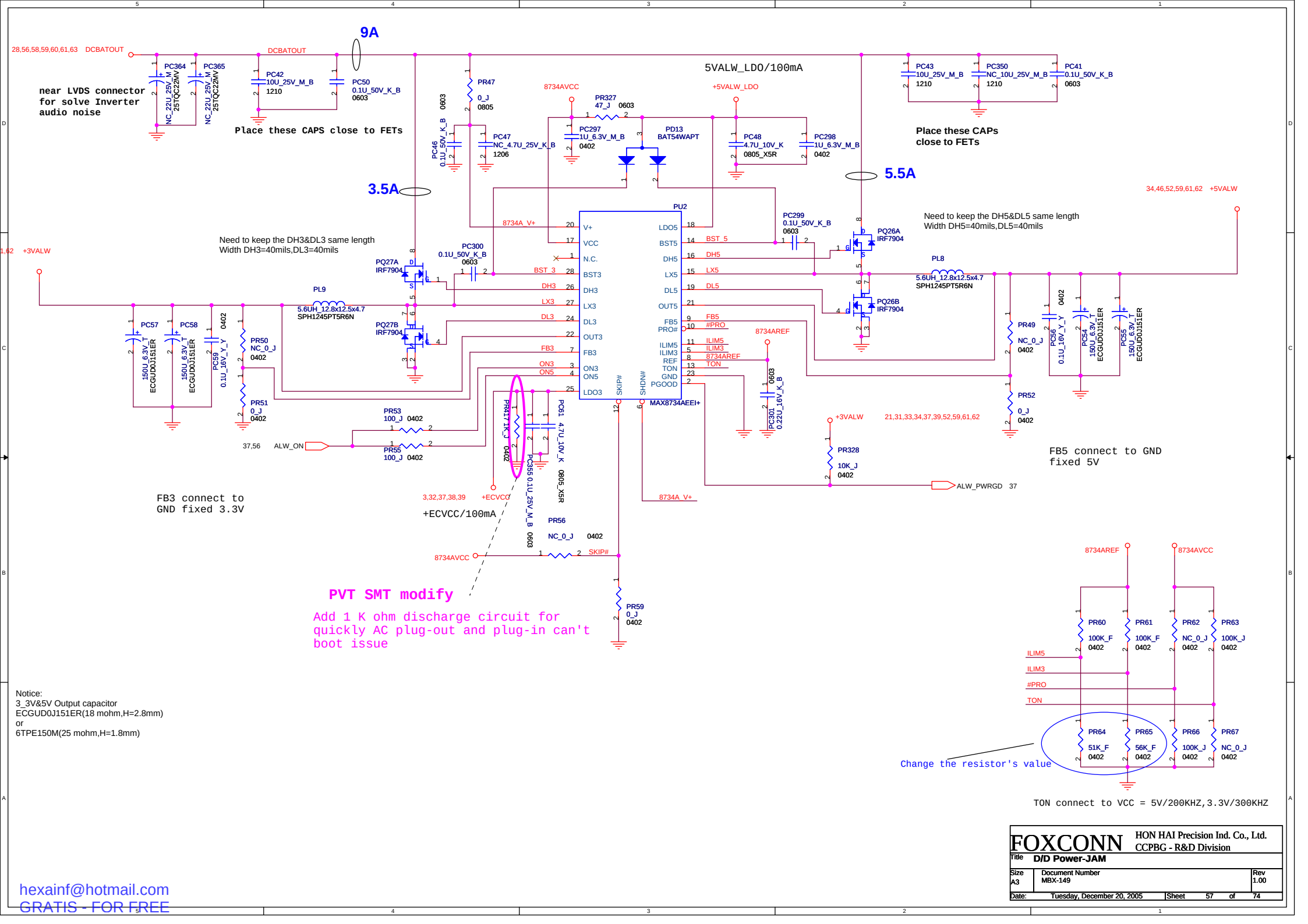
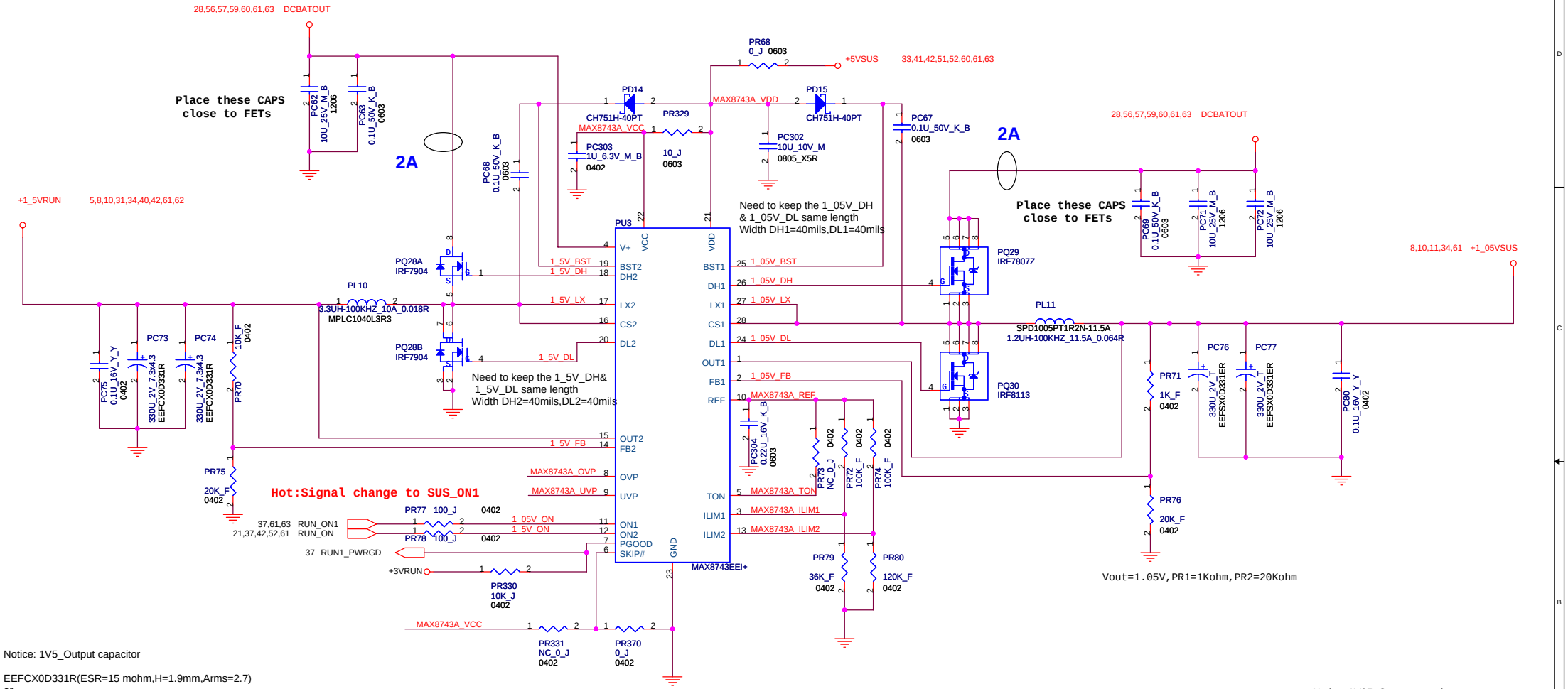
of
74


9A
28,56,58,59,60,61,63 DCBATOUT
DCBATOUT
near LVDS connector for solve Inverter audio noise
Place these CAPS close to FETs
5VALW_LDO/100mA
Place these CAPs close to FETs
3.5A
5.5A
34,46,52,59,61,62 +5VALW
Need to keep the DH3&DL3 same length
Width DH3=40mils,DL3=40mils
Need to keep the DH5&DL5 same length
Width DH5=40mils,DL5=40mils
PU2
MAX8734AEEI+
5.6UH_12.8x12.5x4.7 SPH1245PT5R6N
PQ26A IRF7904
PQ26B IRF7904
PQ27A IRF7904
PQ27B IRF7904
37,56 ALW_ON
21,31,33,34,37,39,52,59,61,62
ALW_PWRGD 37
FB5 connect to GND fixed 5V
FB3 connect to GND fixed 3.3V
3,32,37,38,39 +ECVCC
+ECVCC/100mA
PVT SMT modify
Add 1 K ohm discharge circuit for quickly AC plug-out and plug-in can't boot issue
Change the resistor's value
TON connect to VCC = 5V/200KHZ,3.3V/300KHZ
Notice:
3_3V&5V Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
or
6TPE150M(25 mohm,H=1.8mm)
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title D/D Power-JAM
Size A3
Document Number MBX-149
Rev 1.00
Date: Tuesday, December 20, 2005
Sheet 57 of 74
hexainf@hotmail.com
GRATIS - FOR FREE



Notice: 1V5_Output capacitor

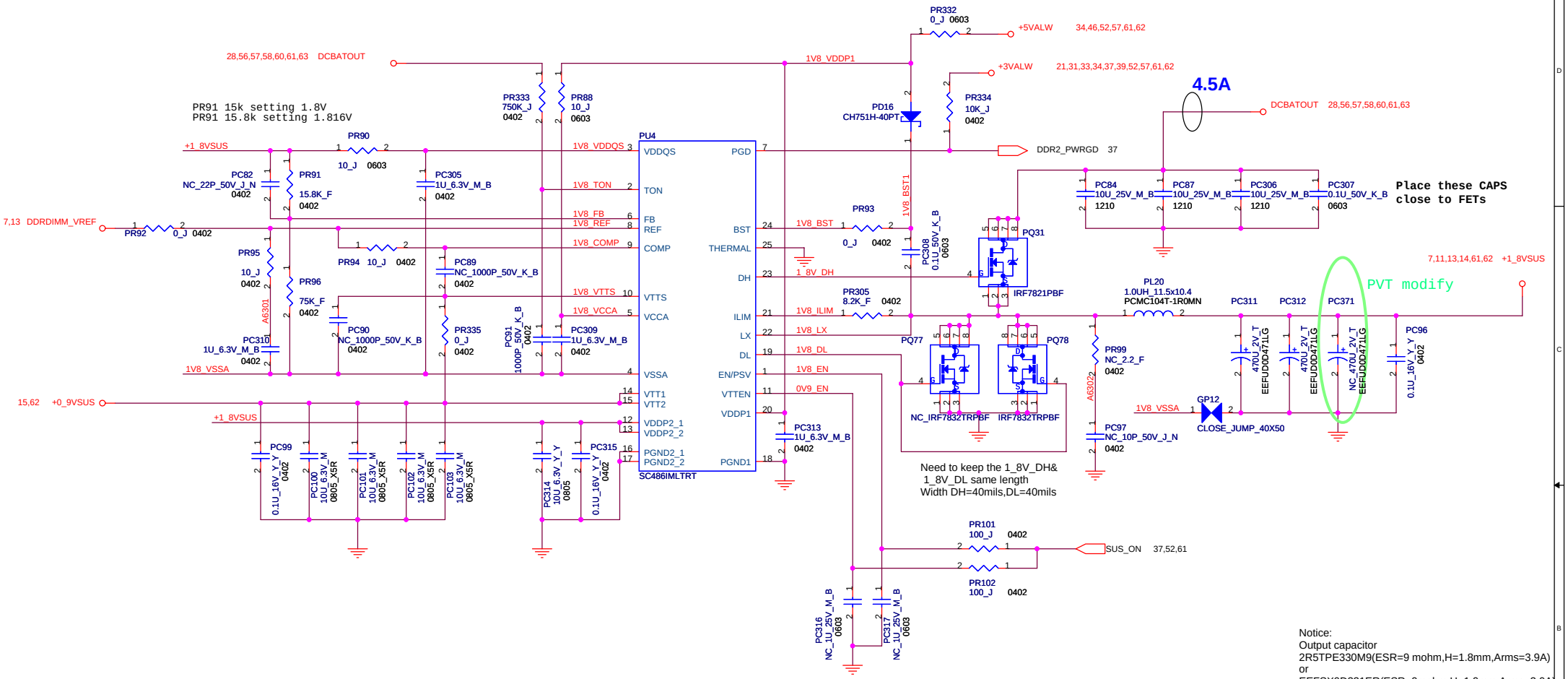
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)
or
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)

Notice: 1V05_Output capacitor usage

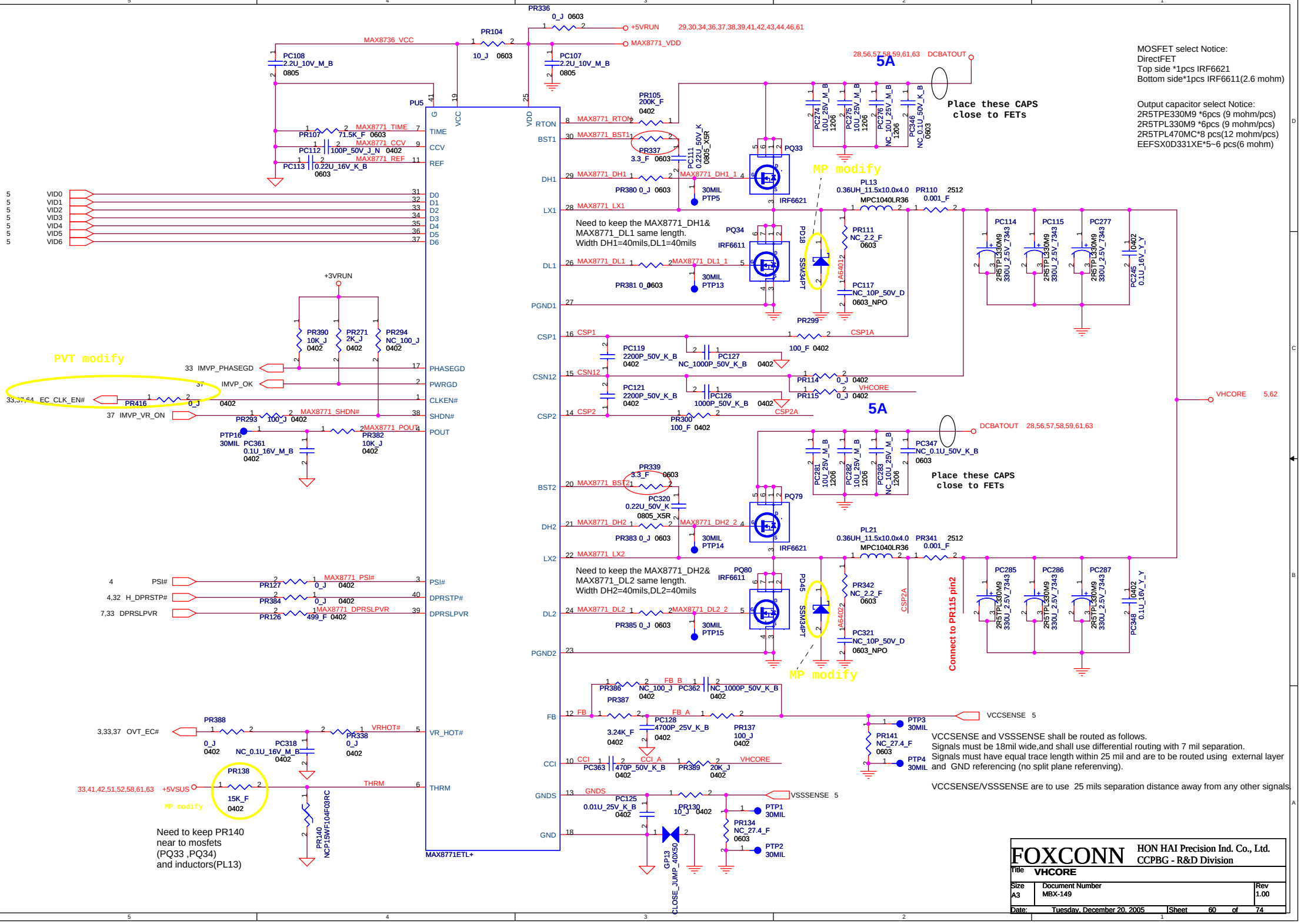
POWER side*2 pcs,Device side*3pcs

EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
or
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	1.5V/1.05V-JAM	
Size A3	Document Number MBX-149	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 58 of 74	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	1.8V/0.9V-CWK	
Size A3	Document Number MBX-149	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 59 of 74	


MOSFET select Notice:
DirectFET
Top side *1pcs IRF6621
Bottom side*1pcs IRF6611(2.6 mohm)
Output capacitor select Notice:
2R5TPE330M9 *6pcs (9 mohm/pcs)
2R5TPL330M9 *6pcs (9 mohm/pcs)
2R5TPL470MC*8 pcs(12 mohm/pcs)
EEFSX0D331XE*5~6 pcs(6 mohm)
PVT modify
MP modify
Place these CAPS close to FETs
Need to keep the MAX8771_DH1& MAX8771_DL1 same length. Width DH1=40mils,DL1=40mils
Need to keep the MAX8771_DH2& MAX8771_DL2 same length. Width DH2=40mils,DL2=40mils
Connect to PR115 pin2
Need to keep PR140 near to mosfets (PQ33 ,PQ34) and inductors(PL13)
VCCSENSE and VSSSENSE shall be routed as follows.
Signals must be 18mil wide,and shall use differential routing with 7 mil separation.
Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referenving).
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.
MAX8771ETL+
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title VHCORE
Size A3
Document Number MBX-149
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Date: Tuesday, December 20, 2005
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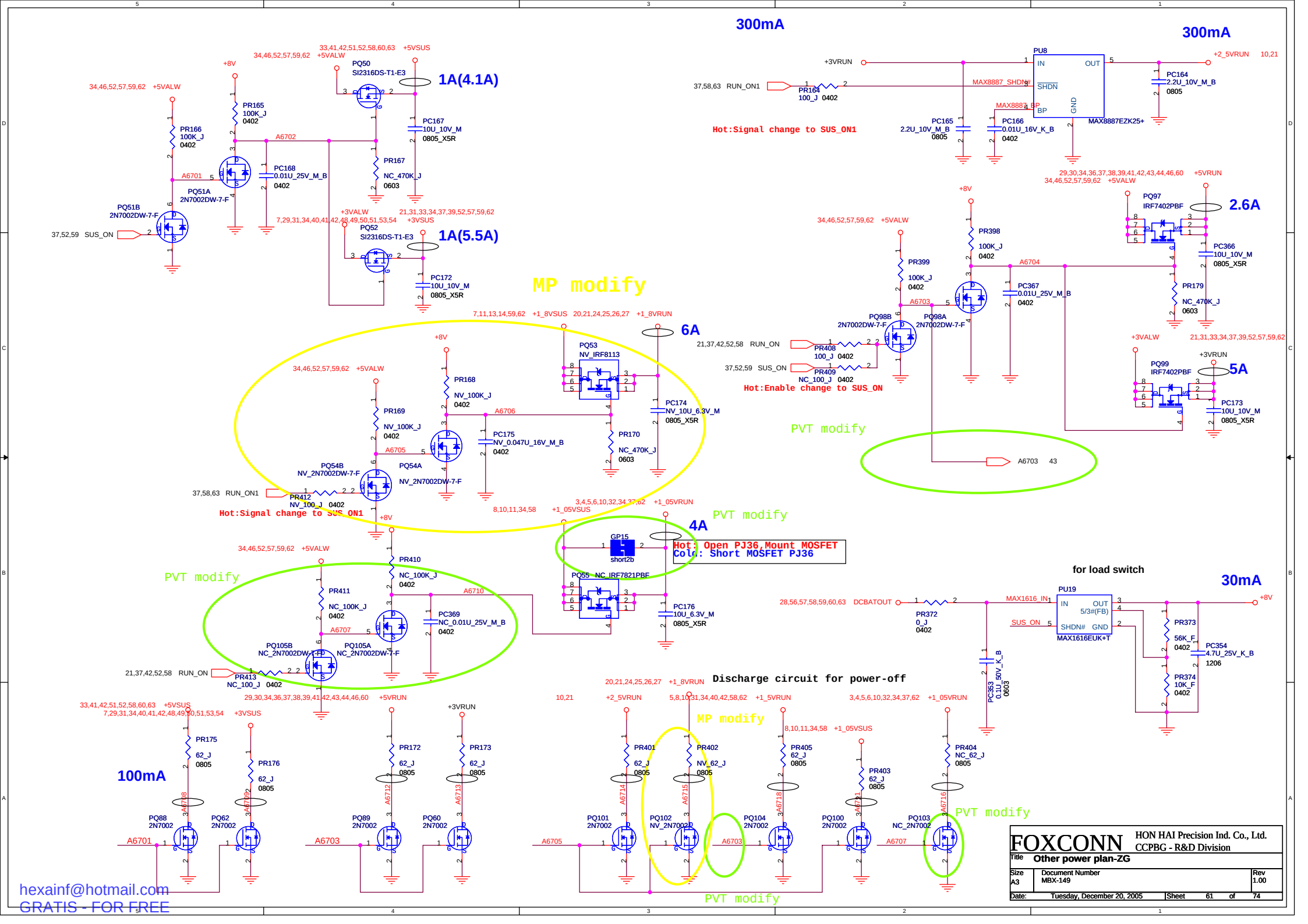

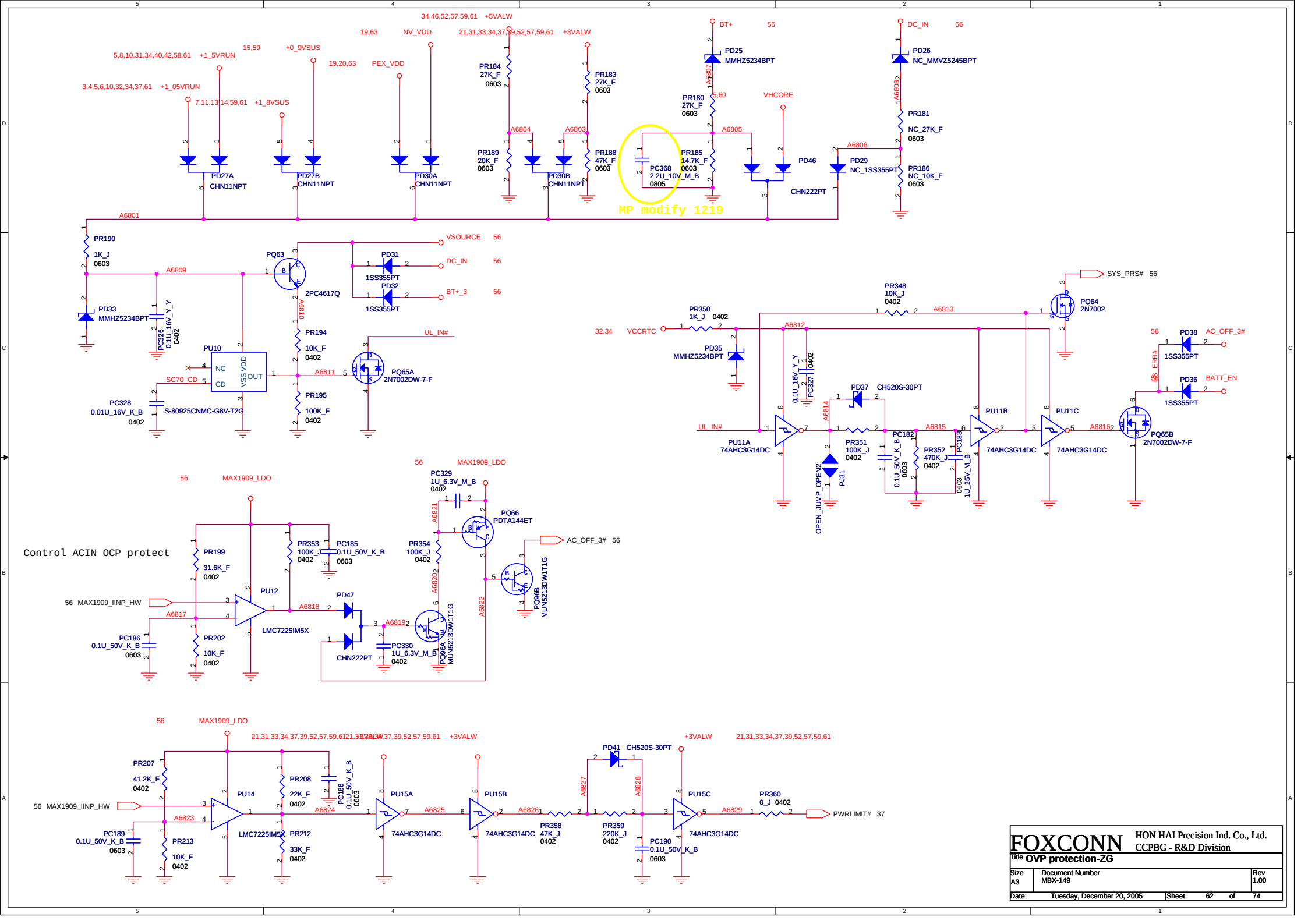
34,46,52,57,59,61 +5VALW
19,63 NV_VDD
21,31,33,34,37,39,52,57,59,61 +3VALW
BT+ 56
DC_IN 56
5,8,10,31,34,40,42,58,61 +1_5VRUN
15,59 +0_9VSUS
19,20,63 PEX_VDD
3,4,5,6,10,32,34,37,61 +1_05VRUN
7,11,13,14,59,61 +1_8VSUS
PR184 27K_F 0603
PR183 27K_F 0603
PR180 27K_F 0603
5.60
VHCORE
PD25 MMHZ5234BPT
PD26 NC_MMVZ5245BPT
PR181 NC_27K_F 0603
PR186 NC_10K_F 0603
PD27A CHN11NPT
PD27B CHN11NPT
PD30A CHN11NPT
PD30B CHN11NPT
PR189 20K_F 0603
PR188 47K_F 0603
PC368 2.2U_10V_M_B 0805
PR185 14.7K_F 0603
PD46
CHN222PT
PD29 NC_1SS355PT
A6804
A6803
A6805
A6806
A6807
A6808
A6801
MP modify 1219
PR190 1K_J 0603
PD33 MMHZ5234BPT
PC326 0.1U_16V_Y_Y 0402
A6809
PQ63 2PC4617Q
VSOURCE 56
DC_IN 56
BT+_3 56
PD31 1SS355PT
PD32 1SS355PT
A6810
PR194 10K_F 0402
PU10 S-80925CNMC-G8V-T2G
SC70_CD
PC328 0.01U_16V_K_B 0402
PR195 100K_F 0402
A6811
PQ65A 2N7002DW-7-F
UL_IN#
SYS_PRS# 56
PR348 10K_J 0402
PR350 1K_J 0402
32,34 VCCRTC
PD35 MMHZ5234BPT
PC327 0.1U_16V_Y_Y 0402
A6812
A6813
PQ64 2N7002
PD37 CH520S-30PT
A6814
PU11A 74AHC3G14DC
PU11B 74AHC3G14DC
PU11C 74AHC3G14DC
PR351 100K_J 0402
PC182 0.1U_50V_K_B 0603
PR352 470K_J 0402
PC183 1U_25V_M_B 0603
A6815
A6816
PQ65B 2N7002DW-7-F
PD38 AC_OFF_3#
PD36 BATT_EN
1SS355PT
56 PD38 AC_OFF_3#
56 PD36 BATT_EN
OPEN_JUMP_OPEN2
PJ31
56 MAX1909_LDO
PC329 1U_6.3V_M_B 0402
PQ66 PDTA144ET
AC_OFF_3# 56
PR353 100K_J 0402
PC185 0.1U_50V_K_B 0603
PR354 100K_J 0402
PQ96B MUN5213DW1T1G
Control ACIN OCP protect
PR199 31.6K_F 0402
56 MAX1909_IINP_HW
PU12 LMC7225IM5X
A6817
A6818
A6819
A6820
A6821
A6822
PD47
CHN222PT
PC330 1U_6.3V_M_B 0402
PQ96A MUN5213DW1T1G
PC186 0.1U_50V_K_B 0603
PR202 10K_F 0402
56 MAX1909_LDO
21,31,33,34,37,39,52,57,59,61 +3VALW
PR207 41.2K_F 0402
56 MAX1909_IINP_HW
PU14 LMC7225IM5X
A6823
A6824
PR208 22K_F 0402
PC188 0.1U_50V_K_B 0603
PR212 33K_F 0402
PC189 0.1U_50V_K_B 0603
PR213 10K_F 0402
PU15A 74AHC3G14DC
A6825
PU15B 74AHC3G14DC
A6826
PR358 47K_J 0402
PD41 CH520S-30PT
A6827
A6828
PR359 220K_J 0402
PC190 0.1U_50V_K_B 0603
PU15C 74AHC3G14DC
A6829
PR360 0_J 0402
PWRLIMIT# 37
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title OVP protection-ZG
Size A3
Document Number MBX-149
Rev 1.00
Date: Tuesday, December 20, 2005
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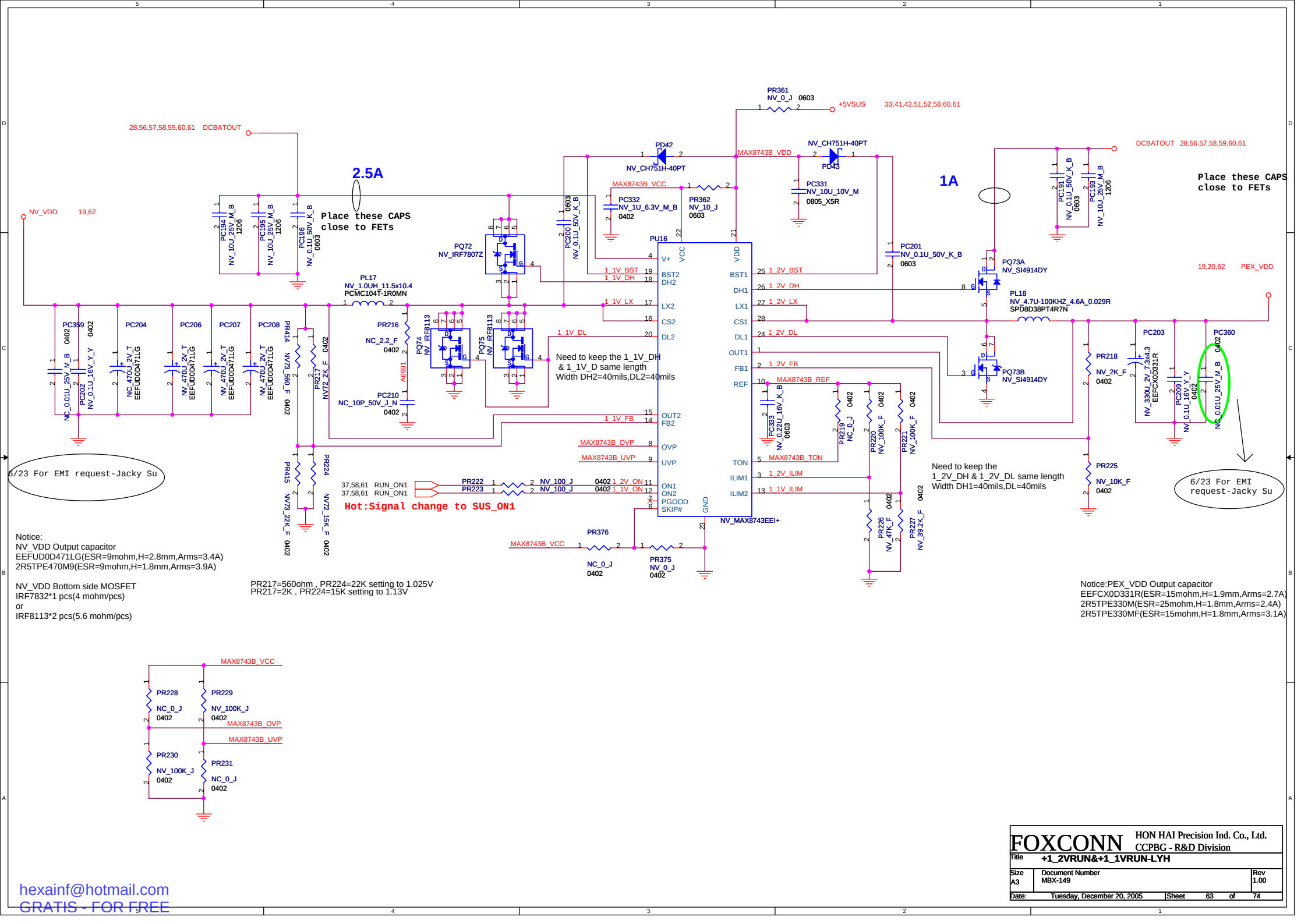


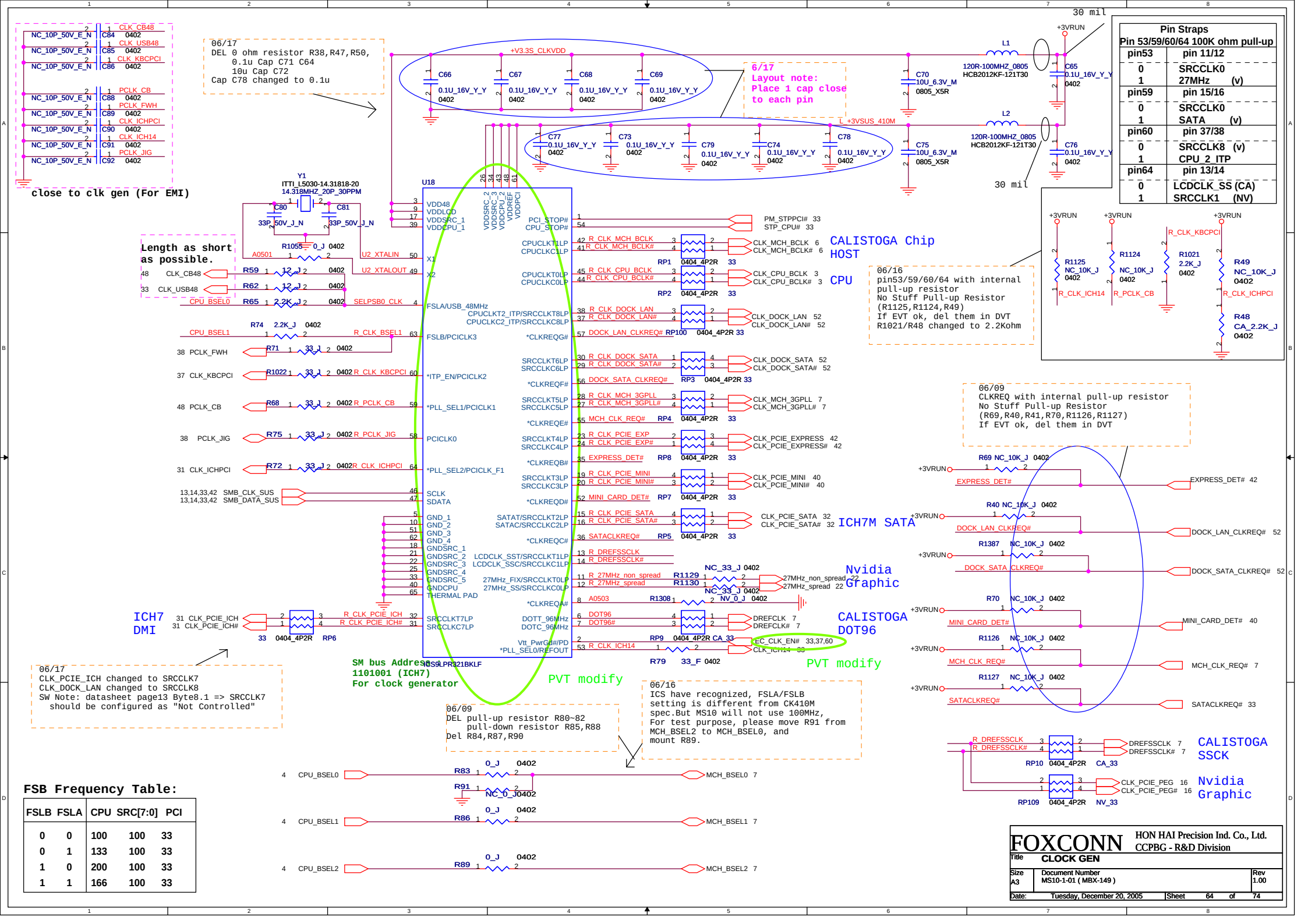
Notice:
NV_VDD Output capacitor
EEFUD0D471LG(ESR=9mohm,H=2.8mm,Arms=3.4A)
2R5TPE470M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

NV_VDD Bottom side MOSFET
IRF7832*1 pcs(4 mohm/pcs)
or
IRF8113*2 pcs(5.6 mohm/pcs)

PR217=560ohm , PR224=22K setting to 1.025V
PR217=2K , PR224=15K setting to 1.13V

Notice:PEX_VDD Output capacitor
EEFCX0D331R(ESR=15mohm,H=1.9mm,Arms=2.7A)
2R5TPE330M(ESR=25mohm,H=1.8mm,Arms=2.4A)
2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	+1_2VRUN&+1_1VRUN-LYH		
Size A3	Document Number MBX-149		Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 63 of 74		


close to clk gen (For EMI)
06/17
DEL 0 ohm resistor R38,R47,R50,
0.1u Cap C71 C64
10u Cap C72
Cap C78 changed to 0.1u
6/17
Layout note:
Place 1 cap close
to each pin
30 mil
Pin Straps
Pin 53/59/60/64 100K ohm pull-up
pin53
0 SRCCLK0 27MHz (v)
pin59
0 SRCCLK0 SATA (v)
pin60
0 SRCCLK8 (v) CPU_2_ITP
pin64
0 LCDCLK_SS (CA)
1 SRCCLK1 (NV)
Length as short as possible.
CALISTOGA Chip HOST CPU
06/16
pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor (R1125,R1124,R49)
If EVT ok, del them in DVT
R1021/R48 changed to 2.2Kohm
06/09
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor
(R69,R40,R41,R70,R1126,R1127)
If EVT ok, del them in DVT
ICH7M SATA
Nvidia Graphic
CALISTOGA DOT96
ICH7 DMI
06/17
CLK_PCIE_ICH changed to SRCCLK7
CLK_DOCK_LAN changed to SRCCLK8
SW Note: datasheet page13 Byte8.1 => SRCCLK7
should be configured as "Not Controlled"
SM bus Address
1101001 (ICH7)
For clock generator
PVT modify
PVT modify
06/09
DEL pull-up resistor R80~82
pull-down resistor R85,R88
Del R84,R87,R90
06/16
ICS have recognized, FSLA/FSLB setting is different from CK410M spec.But MS10 will not use 100MHz, For test purpose, please move R91 from MCH_BSEL2 to MCH_BSEL0, and mount R89.
CALISTOGA SSCK
Nvidia Graphic
FSB Frequency Table:
FSLB FSLA CPU SRC[7:0] PCI
0 0 100 100 33
0 1 133 100 33
1 0 200 100 33
1 1 166 100 33
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title CLOCK GEN
Size A3
Document Number MS10-1-01 (MBX-149)
Rev 1.00
Date: Tuesday, December 20, 2005
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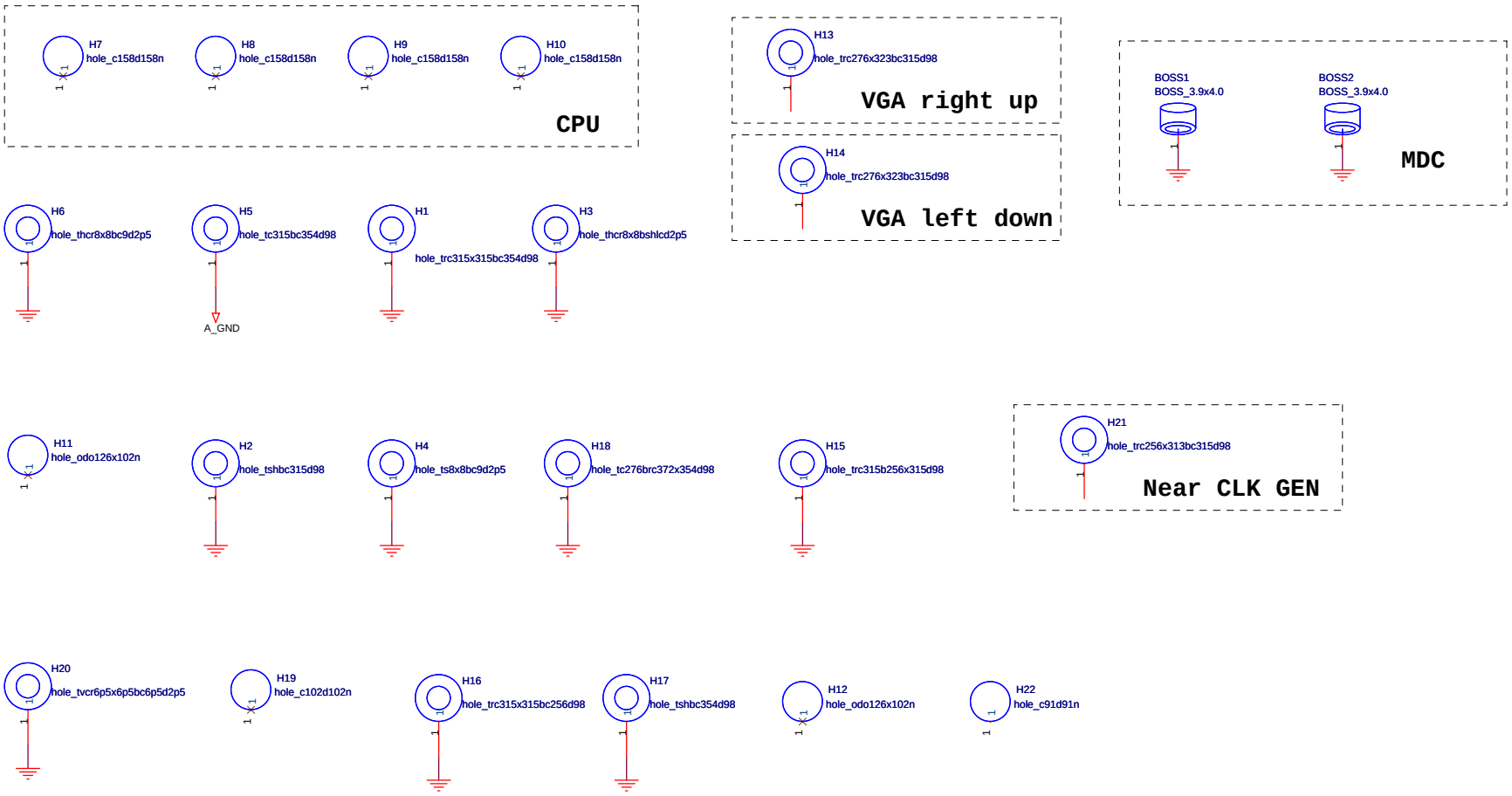

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	HOLE	
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 65 of 74	

HISTORY (Before 2005/06/20)

P.2 Change Q71 , Q4 from MMBT3904 to PDTC144EU to improvement quality
P.4 Reduce CPU VHCOR's capacitor(22uF * 12 PCS ; 0.1uF *10 PCS ; 1000p *10 PCS)
P.5 del C64,C71,C72,C82,C87,C1075
P.5 change C78 from 10U_6.3V_Y_Y to 0.1U_16V_Y_Y ; del D1 BAT54S-LF
P.5 del R38,R47,R50,R67,R77,R80,R81,R82,R84,R85,R87,R88,R90,R1128
P.5 del SRC 49.9ohm termination resistor : R1053,R1054,R39,R42,R43,R44,R45,R46, R51,R52,R53,R54,R55,R56,R57,R58,R60,R61,R63,R64
P.5 del TestPad TP512,TP513,TP514,TP515
P.5 Add R74 2.2K_J ; Add R1308 NV_0_J ; change R1021 from 33_J to 2.2K_J
P.5 change R1124 from NV_10K_J to NC_10K_J ; change R1125 from CA_10K_J to NC_10K_J
P.5 change R1126,R1127 from 10K_J to NC_10K_J
P.5 change R48 from 49.9_F to CA_2.2K_J
P.5 change R49 from 49.9_F to NC_10K_J ; change R40,R41 from 49.9_F to NC_10K_J
P.5 change R69,R70 from 10K_J to NC_10K_J
P.5 change U18 Clkgen from Cypress_28445-5(68-pin MLF) to ICS_9LPR321AKLF (64pinMLF)
P.8 Add R1229~R1231
P.10 Reduce NB VTT plane's capacitor (C149~C157) adn change power plane from SUS to RUN plane
P.10 Reduce NB VCCAUX power plane 's capacitor C174~C190
P.10 Reduce NB VCC plane capacitor C208~C215 & del R148~R150
P.12 Del R154~R161 ,R163,R164 MCH_CFG's strap resistor
P.13,P.14 Del R170~R173 and change 1_8VSUS_DDR2 net name to 1_8VSUS;3VSUS_DDR2_SPD to 3VSUS
P.28 Connect LVDS signals directly to LVDS connector withour choke
P.28 Del brightness PWM circuit and add R1268 , R1269
P.28 Change CN3.38~40 net name to DCBATOUT
P.28 Add GP11 R771 for BIOS_CRISIS# function
P.29 Modify GM_OR_NV_DDCCLK & GM_OR_NV_DDCDATA circuit
P.29 Del C1109 ,C1110 ,R1136 EMI's component and Del DVI function
P.30 Del TV-OUT composite connector ; add D60 ,D61 for ESD protection
P.30 Add R1233 ,R1232 and del DVI's ESD protection circuit
P.30 Modify Semi-PNP circuit and del S-Video 2 circuit
P.31 Modify U29 USB channel 4 net name for HUB
P.32 Del AZALIA interface 8 capacitor for EMI reserved
P.32 Connect SB's LAN interface to INTEL's FHY(change LAN solution)
P.33 Add R124 for JIG borard ; del R618 , R621 ,R646 ,R651 , R653
P.33 Change R1184 to NC and mount R1183 for power sequence unstable issue
P.33 Modify LCDID0 ,1 to GPIO 19 &37; add R1256 for Dock_BAY ;Del R738 , R659 ,R661
P.36 Del SATA2(CN10) for EVT SPEC
P.37 Add R1265 pull low for CAM power on-off function
P.37 Add signal DK_BAY_DETECT# , CAM_PWREN , DK_BAYPWEN ; del R701 and drop FAN2_DAC function
P.37 Change Q24 ,Q26 from MMBT3904 to PDTC144EU to improvement quality
P.38 Del BIOS socket ; del TPM function(CN35) J1 CN36(PS2 function)
P.39 Make SW and LED to D/B(including LID SW , Touch Pad) add SPR2 ,SPR6 for EMI request
P.40 Move LED to D/B ; del C818~C821 , C824 ,C825 reserved capacitor
P.41 Del Fane circuit and change FAN connector from 4 pin to 3 pin
P.41 Move BT's LED circuit to D/B
P.42 Reduce Express Card power SW's capacitor and combin U36 pin 56 & 21 net name
P.42 Change Q35 part , and make Q35 & R772 to NC
P.42 Change Oide USB interface connet to USB HUB "TUSB2036"
P.48 Del R993 ,R1140 and mount R1141 for TI7412's ERRATA
P.49 Del R1174 , C1146~C1150 for TI7412's ERRATA
P.50 Del SD function and move MS's LED to D/B ; change CN25 , CN26 connector
P.52 Change CN37 , CN28 ,CN29 connector
P.53 Del Mini-PCI function and add USB TUB2036 HUB
P. 36 Del PATA HDD function and move HDD's LED to D/B
P.54 Change LAN solution to INTEL 82562GT
P.16 Add R1263 2K ohm pull up +3_3VSUS to U7A " R3 " pin, for G7X " SLOT_CLOCK_CFG " strap.
P.17 Unstuff R226, R227 and stuff R225, R228 change from " 3GIO_PADCFG[2:0] " 001 to 010 for G7X series.
P.19 Change R305 Unstuff to Stuff for G7X.
P.19 Add R1262 for G7X/ NV34M co-layout and R1262 no need stuff for G7X.
P.19 Chipset U7 Pin "F6","G8","G23","A28","F1" change to NC pin and C490 CAP no need stuff for G7X.
P.19 Add L102,C1191,C1192 on U7 Pin "T13" Voltage change from NV_VDD(1.1V) to PEX_VDD(1.2V), and add R1261 for G7X/ NV34M co-layout but R1261no need stuff for G7X
P.19 Add C1193 series connect U7 pin "M21"and "N20", is a nVIDIA CRB circuit suggest.
P.20 Delete power " FBVTT/ FBVDD " all Caps and FBVTT/FBVDDQ/FBVDD connect together.
P.20 Parts L92,L94,C402,C403,C405,C419,C421,C431,C433,R271,R275 unstuff for G7X
P.20 Delete L107,L108 and add L93,L95 for power "FAB_PLLAVDD/ FBC_PLLAVDD" from NV_VDD(1.1V) to PEX_VDD(1.2V) for G7X,
P.20 Change R269,R272 from 37.4ohm to 40ohm

P.21 Parts L21,C467,C468,C469 unstuff for G7X
P.21 Add R1264 10K pull low , when DACC is not used
P.21 Delete L96,L98 and add L103,L105 on power " IFPAB_PLLVDD/ IFPCD_PLLVDD " from +3VSUS to +2_5VSUS for G7X.
P.21 Delete L97 and add L104 on power " IFP_ABIOVDD " from LCDVCC to +1_8VSUS for G7X.
P.22 Delete R291,R294 if ROM interface no used.
P.22 Parts C488,C489,C487,R299,R300,R302,R304,R306,R307,R297,R1104 unstuff for G7X
P.23 Parts R339,R354,R355 unstuff for G7X
P.24 Parts R372,R373 change 6.81K ohm to 10K ohm for G7X
P.25 Parts R391,R392 change 6.81K ohm to 10K ohm for G7X

REV 0.A: (2005/06/21)

P.52 Change value U89 , C1187 , R1239 and add R1300
Del U87 , C1162 ,C1161 and change value R1191 , R1192
P.41 change net HUB_VCC1 to +5VSUS
P.37 Add R1282 0 ohm R
P.43 Add R1283 0ohm
P.43 NC R795 10K
P.43 Add C1201,C1202,C1203,C1204,C1205,C1206
P.44 Add R1284,R1285,Q84,Q85 for HP-OUT muting circuit
P.45 Add R1291,R1292,C1207,C1208
P.45 Add R1288,1289,1294,1295,C1171,C1172 for MIC1_VREF
P.45 Add R1296,R1297,Q86,Q87 for PHONE-OUT muting circuit

(2005/06/22)

P.2 del R1142 and change to test point
P.5 add R1308 to GND
P.7 Change GP11 to R1309 NC
P.32 Change R589 to 510 ohm and add R1310 510 ohm
P.33 change net name U29 pin AH19 to from DK_BAY_DETECT# to DK_BAY_ID#
P.33 Mount R1183 and change R1184 to NC
P.41 change CN42 from 4 pin to 3pin and del FAN2_DAC net name

P.47 Del R933 , R1140 and mount R1141
P.48 del R114 , C1146 ,C1147 , C1148 , C1149 , C1150
P.52 Add R1303 for crystal feelback resister ; Add R1311 , R1312 change net name from PLT_RST# to SUS_PWRGD_10MS
P.36 Add R1304 pull high and del D45
P.53 Add R1305 , R1306, R1307 ; del R1238 and modify U65's pin 21 to GND
P.51 add pull high R1301,R1302

(2005/06/23)

P.10 Add C1209 0.01uF , C1210 ,C1211reserve capicitor for EMI
P.11 Add C1212 ,C1213,C1214,C1215 0.1uF reserve capicitor for EMI
P.16 Del BOSS3,BOSS4 (only BB use)
P.19 Add C1216 1000pF reserve capicitor for EMI
P.29 Add C1217,C1218 47pF reserve capicitor for EMI
P.34 Add C1219,C1220,C1221 0.01upF reserve capicitor for EMI
P.37 Change net name U32.37 from DOCK_LED# to DOCK_LED
P.51 Change net name U30.92 from DOCK_LED# to DOCK_LED
P.52 Move R1243 , R1244 ,R1247 ,R1248 from ICH7 to USB HUB side and del R1241 ,R1242(P.34) ; Mount U89 , R1300 ,C1187
P.41 short R1245 , R1246
P.30 Change CN6 from FOX_MH11741-0001 to FOX_MH11747-BS2D-4F
P.50 Change CN27 library for footprint change and add CN48 for PCMCIA hoswing portion
P.37 U32.62 pin net name from HW_POP_MUTE to HW_POP_MUTE_EC and del R1282
P.43 Delete R1283
P.43 Change net HW_POP_MUTE to HW_POP_MUTE_CODEC
P.46 Add U97 for HW_POP_MUTE
P.42 Add R1313~R1316,L110,L111 for EMI reserve and add CN47 for EXPRESS Card's hoswing portion

(2005/06/24)

P.32 Short C1177 ~C1180

P.42 Update CN19 library for layout footprint

Arrange schematics :
1. Del original page 26 ,31
2.Move orginal P33 Semi-PNP circuit to P30 and del original P33
3.Move orginal P56 CD-ROM circuit to P36 and del original P56
4.rename all page nember

(2005/06/24) Power circuit modify

P.56 Change PD1,3,10,11,12,40 for second source test in EVT.
P.56 Modify PD4 connect to BT+_4 (EMI [Jacjk Su] request)
P.57 Modify PJ1,3,2,4 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.57 Change PL9 from SPD1005PT3R8N-7A to SPH1245PT5R6N
P.57 Change PL8 from RLF12545T-5R6N6R1 to SPH1245PT5R6N
P.57 Change PD13 from LASM02-03T4-G to BAT54WAPT for seconf source test
P.57 Change PU2 from MAX1999EEI+ to MAX8734AEEI+
P.58 Modify PJ5,6,7,8 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.58 Change PD14,15 from SK0003-03T-G to CH751H-40PT for seconf source test
P.58 Change PL10 from SPD1005PT3R8N-7A to MPLC1040L3R3
P.58 Change PL11 from SPD1005PT1R5N-10A to MPLC1040L1R5
P.58 Change PQ28 from Dual mosfet IRF7904 to IRF7807Z
P.58 Add PQ97 IRF8113 for power budget change
P.58 Change PU3 from MAX1845EEI+ to MAX8743EEI+

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(2005/06/24) **Power circuit modify**

P.59 Change PD16 from SK0003-03T-G to CH751H-40PT for seconf source test
P.59 Del PR100 0_J 0402 , Add GP12 close jump for separate A GND and P GND
P.59 Modify PJ9,10,11,37 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.60 Del PR120 470_J 0402 and PQ36 and H_DPRSTP# signal & PJ41
P.60 Change PD17 from SK0003-03T-G to CH751H-40PT for seconf source test
P.60 Change PD18 from SKS30-04AT-G to SSM34APT for seconf source test
P.60 Del PR133 0_J 0603 , Add GP13 close jump for separate A GND and P GND
P.61 Change PD44 from SK0003-03T-G to CH751H-40PT for seconf source test
P.61 Change PD45 from SKS30-04AT-G to SSM34APT for seconf source test
P.62 Change PQ50,52 from FDC653N to IRF7402PBF for power budget change
P.62 Del PR344 0_J 0402 ,PJ36 (cause H/W request in EVT need use +1_5VRUN and +1_05VRUN) So mount parts of PQ53,55
P.62 Change PU19 from MAX1615EUK+ to MAX1616EUK+ make 8V for load switch turn on
P.62 Del +1_5ALW circuit of PU9,PJ29,PC171,PC173,PC170,PJ30

P.63 Change PD25,26,27,28,29,30,31,32,33,35,36,37,38,39,41 for second source test in EVT.
P.64 Modify PJ32,33,34,35 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.64 Add PC359,360 for EMI (6/23 Jacky Su request)
P.64 Change PD42,43 from SK0003-03T-G to CH751H-40PT for seconf source test
P.64 Change PU16 from MAX1845EEI+ to MAX8743EEI+

(2005/06/27) **Power circuit modify**

P.58 Change PR68 from 0_J 0402 to 0_J 0603
P.59 Change PR332 from 0_J 0402 to 0_J 0603
P.63 Change PR361 from 0_J 0402 to 0_J 0603
P.60 P.61 Del MAX8736ETL+ and MAX8552ETB+ solution then add P.60 Change to MAX8771ETL+ for new two phase power controller.
P.62 Del PJ27

(2005/06/27)

P.33 Del R636 for thermal SPEC change
P.42 Add C1222 for CAM power drop issue
P.52 Change Y7 part value to 6MHZ_20P_30PPMM
P.51. Del RUN_ON net name (primily reserved)
P.52 Change U89,R1312,R1239,R1300,C1187 TO NC(do not install)
P.28 Del net name BRADJ_EC and del R445 reserved
P.37 Change pin U32.43 net name from BRADJ_EC to tast point
P.36 Move R1304 to P32 and change net name from PATAODD_LED# to SATA_LED# & change CN32 to NC pin
P.40 Modify CN18.18pin connect to GND ; connect CN18.44 pin to MINI_CARD_LED
P.40 Add R1317 and SW16 for BT & WLAN function SW
P.39 CN44 ,CN45 ,CN46 pin define modify , still need to confirm ID status
P.49 Change CN26 connect to FOX_QT8A0121-1011-8F
P.24, P25 Change U11,U12,U13,U14 for 350 MHZ VRAM

(2005/06/28)

P.42 Change R772 to NC(do not install)
P.41 Del R1098 reserved resister

Audio circuit modify

PS : Remove orginal P54 (HOLE) to P64 ; add one audio page and also arrange PCMCIA , power circuit page number
P.43 Change C1203,C1204,C1205,C1206 to 820pF
P.43 Change net HP_SPK_L,HP_SPK_R to HP_OUT_L,HP_OUT_R
P.44 Change net HP_SPK_L,HP_SPK_R to HP_OUT_L,HP_OUT_R
P.43 Add net SPK_L,SPK_R from U39 PIN16,PIN17
P.44 Change net HP_SPK_L,HP_SPK_R to SPK_L,SPK_R
P.46 Add INT MIC amp circuit block
P.46 Add Mechanical selecter block
P.47 PHONE-OUT change from signal-ends to differential , add PHONE-OUT differential block
P.44 Add C1223,C1224,C1225,C1226,C1227,C1228,C1229 33pF capacitor for RF noise
P.45 Change R1288,R1289,R1294,R1295 from 1K to 2.2K

(2005/06/29) **Power circuit modify**

P.60 Add PR390 NC_0_J 0402 resister

(2005/06/29)

P.32 Change R1206~R1208 from 110 ohm to 22 ohm same as MS01's value
P.37 Connect U32.99 "DOCK_RST_100MS#" to P.52 CN30.98
P.33 Change R1256 value from 100 ohm to 0 ohm
P.37 Del U32.174 pin EC_DOCK_MUTE and del CN30.97 EC_DOCK_MUTE
P.40 Add R1357 pull high to +3VSUS and change net name from MINI_CARD_LED to MINI_CARD_LED#
P.32 Modify R608 to 61.9 ohm 1% and add R1358 parallel R608 for SATA amplitudel over SPEC
P.32 Change R585 from 100K ohm to 20 K ohm for RTCRST# tming verify
P.31 Swrap RP92 , RP94,RP93 pull high net name for layout routing convenience
P.24 ,25 short R359 ,R360 ,R380,R381
P.24 ,25 Del R364 , R365, R382, R386 two BANK VRAM reserved

(2005/06/30) **Audio circuit modify**

P.43 Add R1359 10K_J 0402 resister
P.43 Add C1253, C1254,C1249, C1251 33P_50V_K_N 0402 capacitor
P.43 Add C1250, C1252 12P_50V_K_N 0402 capacitor
P.43 Add C1248 1U_6.3V_M_B 0402 capacitor
P.44 Add D70 PACDN042Y3R ESD Diode
P.45 Change R851,R861 to 2.2K_J 0402 resistor
P.45 Change R848,R857 to 22K_J 0402 resistor
P.45 Change C913, C922 to 2.2U_10V_M_B 0805 capacitor
P.46 del R1112
P.46 del U70
P.46 del Testpad TP304
P.46 Change C1232 to 2.2U_10V_M_B 0805 capacitor
P.46 Change R1319 to 2.2K_J 0402 resistor
P.46 Change R1318 to 22K_J 0402 resistor
P.46 Add C1255 220P_50V_K_N 0402 capacitor
P.46 Change R1318 to 22K_J 0402 resistor
P.46 del U98A,U94B, U95C
P.46 Add U103,U104, U50,U105
P.47 Change R1332,R1335,R1329,R1330,R1333,R1334 to 10K_J 0402 resistor
P.47 Change C1241 to 4.7U_10V_Y_Y 0805 capacitor
P.47 Change R134,R1351,R1337,R1339,R1349,R1350 to 10K_J 0402 resistor
P.47 Change C1247 to 4.7U_10V_Y_Y 0805 capacitor
P.47 del CAP24,CAP25,CAP26,CAP27
P.47 Add C1256,C1257,C1258,C1259 4.7U_6.3V_K 0805 X5R capacitor
P.47 del Q82,Q83,Q86,Q87,Q88,Q89,Q90,Q91
P.47 del R1276,R1277,R1298,R1299,R1353,R1354,R1355,R1356

(2005/06/30)

P.50 Change Q56 S & D connetion for voltage leakeage
P.19 Change C1216 location to L102 righ side
P.3 add JIG_SMI# in CN15.29 &U32.89 pin , add EC_BRADJ U32.43
P.37 Add R1362 ,R1363 and change Q24 ,Q26 for PWRGD fail issue

(2005/06/30) Audio change

P.45 Add R1369 0_J 0402 for mechanical switch solution
P.46 Add R1372 NC_0_J 0402
P.46 change U103 to TC7SET04FU
P.46 change U104 to SN74AHC1G14DCK
P.46 Add U105 TC7SET04FU
P.46 Del R1112
P.46 Del U70 TC7SET32FU

(2005/07/01) Audio change

P.43 Del R803
P.43 Del C872,C1194,C1195
P.43 Change C873 to 1U_25V_Y_Y 0805
P.43 Change C869 to 10U_10V_M 0805 X5R
P.43 Change U41 to MAX1818EUT50
P.43 Del Y6 Xtal
P.43 Add R1364 0_J 0402
P.43 Add C1262 33P_50V_K_N 0402
P.43 Add C1263 12P_50V_K_N 0402
P.44 Add C1264 0.1U_16V_M_B 0402
P.44 Add C1265 0.1U_16V_M_B 0402
P.44 Add C1263 12P_50V_K_N 0402
P.44 Change C1229 to 0.47U_6.3V_K_B 0402
P.44 Change C878 to 0.1U_16V_M_B 0402
P.44 Add R1336 10K_J 0402
P.44 Del C1197,C1224,C1196,C1223
P.44 Del R1278,R1279
P.44 Add R1368 10K_F 0402
P.44 Add R1367 5.6K_F 0402
P.44 Add R1365 0_J 0402
P.44 Change U66 to TPA6011A4PWPRG4
P.46 Change R1249 to 560K_J 0402
P.46 Add R1370 470K_J 0402
P.46 Add R1371 47K_J 0402

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(2005/07/04)

P.52 CN30 Docking pindefine change for Docking layout critical
P.19 Delete R1261 for NV43 reserved
P.20 Delete C402, L92, C403, C405, L94, C419, C421,C431, C433, R271, R275,L107, L108 for NV43M reserved
P.21 Delete L21, C467, C468, C469,C487, R299, R300, R297, R1104 for NV43M reserved
P.53 Change Y7 to AKER_CXB-006000-7X4X2 for small size ; add R1373 , R1374 for EEPROM select
P.30 Change CN6 pin 3 & pin 4 signal for S-Video fail issue
P.39 Del CN17 and make Touch Pad to D/B
P.64 Change screw hole size for new ME drawing
P.39 Change CN44 to 8 pin MOLEX _52893-0895 ; modify CN45 pin define

(2005/07/05) **Audio circuit modify**

P.43 Change C862 to 10U_10V_M_B 0805 X5R
P.44 Del C1228
P.44 Change C1092, C1093 to 2.2U_10V_Y_Y 0603
P.44 Change C1225,C1226 to 0.1U_16V_Y_Y 0402
P.45 Change R1290,R1293 to NC_0_J 0402
P.46 Del Q75
P.46 Del R1249,R1371
P.46 Del U97
P.46 Add Q87
P.46 Change Q81B to Q76B

(2005/07/05) **Power circuit modify**

P.57 Add PJ29 jump for ECVCC separate with system
P.57 Add PC 364 ,PC365 for solve Inverter audio noise.
P.57 Change PR64 from 147K_F 0402 to 47K_F 0402
P.57 Change PR65 from 100K_F 0402 to 56K_F 0402
P.58 Change PR80 from 75K_F 0402 to 33K_F 0402
P.58 Change PR79 from 61.9K_F 0402 to 39.2K_F 0402
P.59 Change PR305 from 5.1K_F 0402 to 5.6K_F 0402
P.59 Change PQ31 from IRF7807Z to IRF7821
P.59 Change PQ77,PQ78 from IRF7832 to IRF8113
P.60 Add PR115 0_J 0402 resister
P.60 Add PC126,PC127 1000P_50V_K_B
P.60 Change PR337,PR339 from 0_J 0402 to 3.3_F 0603
P.60 Del PR139 , PC247 same EVkit
P.60 Add PTP16
P.60 Add PR294 100_J 0402
P.60 Add PR390 10K_F 0402
P.60 Change PR272 form 2K_J 0402 to 100K_F 0402
P.60 Change PC113 form 0.1u_25V 0603 to 0.22u_16V 0603
P.60 Add IMVP_PHASEGD signal
P.61 Change PR373 from 80.6K_F 0402 to 56K_F 0402
P.61 Add PR344 NC_0_J
P.61 Add PJ36 OPEN_JUMP_OPEN2B
P.62 Del PC324 , 325 same MS03 setting
P.63 Change PR226 from 61.9K_F 0402 to 47K_F 0402
P.63 Change PR227 from 33.2K_F 0402 to 39.2K_F 0402
P.63 Change PR217 from 1.58K_F 0402 to 560_F 0402 for 1.025V setting
P.63 Change PR224 from 10K_F 0402 to 22K_F 0402 for 1.025V setting
P.63 Change PL18 from SPD8D28PT4R7N to SPD8D43PT100M
P.63 Change PQ74,PQ75 from IRF7832 to IRF8113
P.60 Change PL13,PL21 from MPC1040LR56 to MPC1040LR36

(2005/07/05)

P.24 Change net name U11.M4 to VRAM1_NC2 ,U12.M4 to VRAM2_NC2
P.32 Change net name R1206 , R1207 ,R1208 LAN signal to correct
P.44 Change CON2 to FOX_JA9333L-000G2 for ME issue
P.45.Change CON3 to FOX_JA9333L-000R1 for ME issue
P.42 Change CN20 to FOX_HS6104E
P.42 Change CN20 to FOX_HS6104E
P.30 Change CN6 pin 3 & pin 4 signal for S-Video footpring modify
P.29 Del R1135

(2005/07/06)

P.46 Change Q86 to MMBT3906(PNP)
P.46 Add R1376 10K_J_0402
P.46 Add Q86 NC_DTA114YUA
P.47 Add Q89,Q90,Q91,Q92 for reservation
P.47 Change R1296,R1297,R1272,R1274,R1341,R1342,R1345,R1346 to 33_J_0402
P.37 Change R698 ,R699 from 10k to 4.7K ohm
P.22 Mount U8 , R286 , R289 thermal sensor ; change R308R310 , R323 ,R324 ,R315, R317,R320,C491~493 to NV_0 condition

P41. Add R1377 , LED9 ,Q93 ,Q94 ,R1378 , R1379 for BT's LED on board
P40. Del R1357 ; add Q95 , R1380 , LED10 for WLAN on board and modify
P.39 CN46 connector pin define

P.37 Add RP99 10K for TOUCH PAD

(2005/07/07)

P.28 Add CN49 interver connector and change CN3 to 30 pin (for LVDS cable burn issue)
P.37 Move HW_POP_MUTE_EC to U32.174 pin ; add D_PWRGD netname in U32.62 & CN30.57 ; Del U32.87 BOOT_MODE# net name
P.52 Add HDCP_SCL,HDCP_SDA net name in CN30.58,59 and change U82 to NC
P.5 Change R65 ,R74 left side net name to CPU_BSEL0 ,CPU_BSEL1
P.5 Change C729 to NC_10U_6.3V_M
P.41 Del R769 reserved R
P.42 Change C849 , C848 to NC condition
P.44 Change C1266~1268's GND to analog GND
P.40 Change LED10 to HT-110UYG 90 degree for ID issue
P.41 Change LED9 to HT-110UYG 90 degree for ID issue

P.38 Del CN15's H_CPURST# signal for layout issue
P.42 Move R1315 ,R1316,L111 to EXPRESS CARD's CLK signal
P.42 Add R1381 , R1382 reserved R
P.10 Change CAP5,6,8 to EEFUD0D471LG
P.43 Add C1270 decoupling capacitor
P.43 Change U41 to TPS79301DBVR (Audio power 4.75V/200mA)
P.43 Change C887 to 0.01U_25V_M_B
P.43 Change R801 to 30K_F 0402
P.43 Change C869 to 4.7U_10V_Y_Y 0805
P.3 Add C1271~ C1280 decoupling capatitor for EMI reserved
P.46 Change U50 to 74AHC1G08GW
P.36 Add C1281 10 uF capacitor and change CAP21 to NC condition
P.39 Add C1282~ 7 0.1uF in D/B power source for EMI
P.40 Add R1283 to correct connection
P.40 Del C817 , C818 capacitor
P.52 SWAP PHONE_OUT_R+ ,PHONET_OUTR- in CN connector
P.54 U90 change to AT93C46-10SU-2.7
P.53 Change AKER_CXA-751 6MHz to 4 pin
P.29 Change D7 to BAS316 for small size
P.3 Change R26 to 51ohm for Intel document update
P.52 Add PM_RSMRST# in docking connector
P.41 Change Q93,Q94 to PDTC144EU and del R1154,R1155
P.21 Change U86 to Q96 MOSFET 2301
P.39 Add SPR3,SPR7 for EMI solution
P.43 SWAP pin U39.39,41 and U39.35,36 ;Add Gp14,L112 for EMI
P44 Add L113,L114 for EMI request

(2005/07/07) **Power circuit modify**

P.56 Change PD2 to MMPZ5250BFPT
P.58 Change PR79 to 47K_F 0402, PR80 to 120K_F 0402
P.58 Del PQ97
P.58 Change PQ28 to IRF7904
P.60 Mount PC245,PC248
P.62 Change PU10 to S-80925CNMC-G8V-T2G
P.60 Del PTP6,,8,9,10,11,12 reduce layout space

(2005/07/08)

P.42 SWAP L111 signals for layout routing smooth
P.64 Change H3 screw hole for ME request
P.50 Del C979 , C976 ,C975 ,C977 capacitor
P.52 Del docking connector netname " DOCK_SATA_CLKREQ#,PWRLIMIT# "
P.5 Del R41 for DOCK_SATA_CLKREQ# reserved R

(2005/07/09)

P.37 Add U106 ,R1348 for docking reset timing
P.39 Change SRP3,SRP7 type for EMI request

(2005/07/09) **Power circuit modify**

P.58 Change PR70,71,75,76 from 0603 to 0402
P.58 Change PR79 to 36K_F 0402
P.59 Change PQ77,78 to PQ77 mount IRF7832 , PQ78 NC
P.59 Change PR305 to 6.49K_F 0402
P.63 Change PR227 to 36k_F 0402

(2005/07/11)

P.21 Q96 Swap for leakege voltage

(2005/07/12)

P.34 Add 0 ohm R for VccSATAPLL
P.22 Add R1385,R1386 pull high for DVI "I2CB "
P.43 Modify R801 to 29.4K ohm
P.53 Change U52 to AT93C46-10SU-2.7 for use the same BOM
P.38 Add PWRSW# signal to CN15

(2005/07/12) **Power circuit modify**

P.61 Change PQ53,PQ55 to IRF821PBF
P.63 Change PL18 to CDRH8D38NP-4R7NC

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(2005/07/12)

P.64 Add R1387 and net name DOCK_SATA_CLKREQ# to docking connector

P.41 LED9 change to HT-110NB

(2005/07/14) **Audio circuit modify**

P.43 Change C1154 from 0.1uF 50V to 0.1uF 16V

P.43 Add C1290 0.1uF 16V_Y_Y ; change C855 close codec side

P.43 Add C1288 0.1uF 16V_Y_Y : connect SENSE_A to GND

P.43 Add C1289 0.1uF 16V_Y_Y : connect SENSE_B to GND

P.43 Replace GP14 Close Jump with R1388 NC_0 ohm 0402

P.44 Replace CAP13 to C1291 NC_10uF 6.3V_X5R 0805 and connect to DGND for Test

P.44 Change C877 to 10uF 6.3V_X5R 0805

P.44 Change R1185, R1186 to 0hom 0402

P.44 Change CAP22,CAP23 to shoei Al CAP

P.65 Change H5's GND to CHASSIS_GND for EMI request

(2005/07/15)

P.44 Connect C1266, C1267, C1268 & C1269 to AGND

P.37 Change CN12 from FOX_GB20240-0001-7F to FOX_GB20240-0002-7F for KBC drop in SMT issue

(2005/07/19)

P.52 Change CAP19,17,18 from 7343 size to 6032 size

P.38 Del CN14.32 net name BOOT_MODE#

P.50 Del R950 47 ohm for SD fucntion drop

P.37 Change R698 , R699 to 10K ohm

P.52 Add R1389 pull high R for PCMCIA issue

(2005/07/20)

P.63 Del PC205 for layout space issue

P.59 Change net name from 1V8/15A to 1V8/15.5A

P.54 Change R1210,R1305 from 100ohm to 110ohm for INTEL FAE suggest

(2005/07/21)

P.64 Change H15 screw hole for ME request

P.28 Add U106,R1390 for voltage level shift

P.37 Change net name SUSPEND_LED# & POWER_LED to SUSPEND_LED & POWER_LED

P.56 PD5,9 Change to PACDN042Y3R

(2005/07/24)

P.37 Del CN12 Pin 25,26 connect to GND ; Del TP114

(2005/07/25)

P.52 Change R1301 pull high from +3VSUS to +3VALW

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DVT (2005/09/05)

PS : For S3 hot change to S3 cold :

Change all power plane form +1_5VSUS ,+1_05VSUS to +1_5VRUN and +1_05VRUN power plane

Change VGA & VRAM's power source from +1_8VSUS to +1_8RUN

Change most of power source from +3VSUS to +3VRUN expect chip TI7412 and other small portion

Change most of power source from +5VSUS to +3VSUS , but not all

P.27 Change C575 , C605 to NV_10U_6.3V_M
P.48 Seraprate C954 ,C955 to the different U58's pin
P.49 R934,R940,R955 change to 1K ohm for TI's reference denign update
P.10 Del A1001 conection from R138 to D4 ; change L4 to HCB2012KF-121T30 for +1_5V drop issue
P.40 Change R1067 from MINI_PCIE_+3_3V to +3VALW for support WOL S4
P.34 Change R657 's power from +3VSUS to +3VALW for support WOL S4
P.54 Change L101,U90's power source from +3VSUS to +3VALW
P.33 Change U29 pin C29 to PM_RSMRST# for support S4 WOL and add R1391 0 ohm R
P.3 Change Q4 to MMB3904 and add R1392 (2.2K ohm)for PM_THRMTRIP# can't turn on issue
P.64 Swap U18 pin 58 & pin 64 connection for ICH clock free run
P.50 Short CN26's pin 2 & pin 6
P.29 Add R1394,R1394 pull down R for S4/S5 float issue
P.7 Add R1309 for intel reference denign update
P.12 Del R162 for Intel's A02 CPU update
P.23 Change R330 , R331 to 124 ohm for Nvidia's suggestion
P.22 Add R1401~R1404 for Nvidia's JTAG can't floating issue
P.37 Del R718,Q25,R726,Q26,R1363,R706,Q23,R707,R1363,Q24 for S3 hot extra power good
Add NV_ mount condition to correct for U7,U11,U12,U13,U14,R1263,C322,C323,CAP10,Q7.
P.10 Change C141,C142 to 10uF C
P.23 Modify R354,R355 to NC
P.37 Change U32.118 pin ,R691 from SUS_ON1 to RUN_ON1
P.37 Change U32.48's net name to RUN1_PWRGD
P.20 Add C1293 ,C1294 for EMI request
P.22 Add R1405 100 ohm pull-down R to solve DDE_ALERT# always keep low issue
P.34 Short U29.AB17,AC17,T7,F17,G17,AB8,AC8 and del GP6,GP7,GP8 for progress power plane
P.33 Del R1184 for power sequence verify
P.29 Add C1295~C1301 for EMI request
P.65 Change H5's GND to A_GND
P.54 Del CN40 pin 8,9 GND
P.39 Change CN44 to foxconn vendor but pin to pin compitable with MOLEX
P.14 change R176 net name from PM_EXTTS#1 to PM_EXTTS#0
P.22 Change C1139 to NC condition
P.52 Change CN30 to FOX_QL0150L-D24A01-5F (add GND pad)
P.10 Change L4 to HCB2012KF-121T30 for voltage drop issue
P.28 Change R1268 , U106,R1390 mont condition

Audio circuit modify

P.43 Change C863 from 1uF 10V to 10uF 10V (Sigmatel: For anti-pop noise)
P.43 Change C857 from 4.7uF 6.3V to 10uF 10V (Sigmatel: For better performance)
P.43 Add C? 0.1uF 16V_Y_Y on Port-B (Non use Input port should connect to GND through 0.1uF)
P.43 Add Q?, Q? & Q? for Jack sense circuit.
P.43 Add R? 39.2K_F 0402; R? 10K_F 0402; R? & R?10K_J 0402; R? & R? 5.1K_F 0402 for Jack sense circuit.
P.44 Change R1367 5.6K_F to 6.2K_F (Set AMP gain = 10dB)
P.45 Del R1290, R1293, R1369, R1294, R1295 & C1172 (One Verf for MIC is enough)
P.46 Del U105 (HW_POP_MUTE_CODEC change to Active High)
P.46 Del R1375 (One MIC Verf is enough)
P.46 Del U100 & R1372 (MIC Switch is not needed)
P.44 Change CON2 connector to black color

(2005/09/12)

P.52 Change CN30 to FOX_QL0150L-D24A01-5F (add GND pad)
P.36 Change CN32 to FOX_QT8H0506-H111R-4F
P.39 Change CN15 to FOX_QT510306-L011-7F for connector easy breaken issue
P.42 Modify CN19 layout symbol(add 2 fixed GND for connector easy drop issue during SMT re-flow
P.28 Change U17 to G548
P.43 Del C1292 and del U39.21,U39.22 connection
P.43 Change U39 to co-lay packeage
P.49 Change CN23 to FOX_UV31413-WR56P-7F for reserve type
P.37 Add R718 , R726 , R1363 for S3 hot reserve
P.50 Change C982 from 10uF to 4.7uF and add R1406 for dischage
P.37 Change R698 , R699 from 10K ohm to 4.7K ohm and add R1407 , R1408 for SM Bus measurement fail issue
P.32 Del U29 SATA2 connection to docking
P.65 Modify H17 , H22 ,H1,H2,H18,H15,H14,H13,H21,H5,H16
P.20 Add C1302 for EMI request
P.28 Change R461 from 330 to 200 ohm
P.52 Add CN30 pin2 connection RUN_ON

(2005/09/13)

P.19 Change C1192 to 0603 size
P.10 Bypass R130 ,R136 0 ohm R
P.22 Del R1133 pull-low R and move R458 from R457pin1 to R457 pin2 location
P.34 Del R655 0ohm R
P.40 Change R1317 and R1067's power source to +3VSUS
P.41 Change R1377's power source to +5VRUN and del Q94
P.42 Del R772,Q35,R774 reserve circuit ; bypass R1096 0 ohm R

(2005/09/14)

P.33 Del R1183 0ohm R
P.52 Del CN30 pin 58,59 connection
P.37 Del U32 " BIOS_CRISIS# " , U32.20 " FWH_BOOT" connection
P.38 Del CN15 FWH_BOOT connection and del R735
P.28 Del GP11 and R771
P.39 Swap CN44's pin 6 and pin8 connection
P.40 Change SW16 vendor to Foxconn
P.42 Change Q79's power to +5VSUS
P.42 CN19 pin 11 name to PCIE_EXPRESS_WAKE# and connection
P.33 Add Q100 , GP14 for EXPRESS wake pin lekage voltage prevent
P.39 Change CN46 conection to U58.F8 pin
P.50 Modify U58.C8 , Q56 net name to MC_PWR_CRT_0
P.32 Change R602 value to 24.9ohm and del R1358 for SATA SI measurement

(2005/09/16)

P.33 U29.C19 net name to SUS_PWRGD_10MS for LAN don't not support S4 WOL
P.34 Modify R657's power to +3VSUS for LAN don't support S4 WOL
P.54 Change L101 , U90's power source to +3VSUS for LAN don't support S4 WOL
P.37 Change CN12 to FOX_GB21240-0002-7F
P.53 Change Y7 to TXC vendor

(2005/09/19)

P.8 Modify R120 mount condition
P.8Add R1409~R1415 for Intel's update
P.10 Modify R131,C132,C133,D3,R132,R136,C152,C153;and Add R1416,R1419
P.50 Modify MS's power circuit add Q101 ;modify R1047 ,Q56 value and del R1406
P.5 Del R27 0ohm R
P.37 Change R718,R726's power source to +3VSUS

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P.22 Change R286 mount condition to NC
P.28 Del R445 and BRADJ_EC line
P.34 Del GP9 ,R670,R667,R1384,R676,R674,R668,R666,R662

(2005/09/20) DVT power modify

P.56 Change PR379 to 1K_F 0402
P.56 Change PR363 to 10K_J 0402
P.56 Add PR392 to NC_0_J 0402 ,PR393 to 0_J 0402
P.56 Add PR391 22k_J 0402 ,PR394 33k_J 0402
P.56 Change PC337 to 0.01U_50V 0603
P.56 Change PR26 to 20k_F 0402
P.56 Change PC37 to 470p_50V 0603
P.56 Change PD11 to MMVZ5235BPT
P.56 Add PR406 56k_J 0402
P.56 Change PC336 to 1U_25V 0603
P.56 Del PR15,16 ,move to H/W side/ close KBC
P.56 Change PC9 to 47p_50V 0402
P.57 Change PR47 to 0_J 0805
P.57 Change PC47 to NC_4.7U_25V
P.57 Del PJ1,3,2,4,29
P.58 Change PR68 source to +5VSUS
P.58 Del PC78,79
P.58 PGOOD pull high source change to +3VRUN
P.59 Del PC349
P.59 Change PC311,312 to EEFUD0D471LG
P.59 Del PJ9,10,37,11
P.59 PGOOD pull high source change to +3VSUS
P.60 Change PC112 to 100p 50V 0402
P.60 Change PR272 to 2k_J 0402
P.60 Change PC125 to 0.01U_25V 0402
P.60 Change PR130 to 10_J 0402
P.60 Change PR336 source to +5VRUN
P.61 Change PQ50,52 to SI2316DS
P.61 Change PQ53 D ans S to +1_8VSUS and +1_8VRUN
P.61 Change PQ55 D ans S to +1_05VSUS and +1_05VRUN
P.61 Add PR410,411,412,413,399,398,408,409, PQ105,98,97,99
P.61 Del PJ28,40
P.61 Change PU8 enable signal to RUN_ON1
P.63 Change PR361 source to +5VSUS
P.63 Change PU16 enable signal to RUN_ON1
P.60 Change PR387 to 3k_F 0402

(2005/09/20)

P.20 Change R272 to 30 ohm for nVIDIA's suggestion
P.41 Change R1377 to 200 ohm
P.41 Add U107 , R1420 ,R1421,R1422,R1423,C1304,C1305,C1303 and change Q33 ,C827
P.38 Change U34 to EN29LV800BB-70TCP
P.37 Modify R726's power source to +3VALW
P.37 Change R698,R699,R1180's power source to +3VALW
P.39 Change R756's power source to +3VSUS
P.39 Change SPR2,SPR3,SPR6
P.21 Modify C474 mount condition to NC
P.22 Modify C488 ,C489,R292 mount condition to NC_
P.23 Change R339 mount condition to NC

P.19 Modify R305 mount condition to NV72_
P.20 Modify L95 ,C422,C424 mount condition to NV73_
P.25Modify U13 ,U14,R383 ,R389 ,R391 , C507,R399,R400 , R390,R392,C508 to NV73_
P.26 Modify mount condition to NV_73 all page
P.24 Modify R361 ,R363 mount condition to NVS_
P.25Modify R383 , R384 mount condition to NV73S
P63 Add PR414 , PR415 and modify PR217 ,PR224 mount condition

P.38 Add C1306

(2005/09/21)

P.50 Swap Q101 pin E & C and add R1425

P.54 Change R1307 to 620 ohm
P.8 Add R1426 ,R1427 pull high R
P.43 Modify R1359 to pll low
P.44 Change R847 ,R852 to 10K
P.52 Add U30 pin 5 ,pin 6 connection to U32.20,87
Modify PR64 to 51K ,PR305 to 8.2K,PR387 to 3.24k
P.37 Change R718's power source to +3VRUN ; R1180 to ECVCC
P.52 Modify CN30.71 & U32.99 net nace to DOCK_RUN_RST
P.52 Modify CN30.5 & U32.20 net name to AND_DOCK_S5_RST_100MS#
P.37 Add IAC_RESET#_AUDIO net to U32.83
P.22 Add R1428 and modify R1131
P.43 Change C1270 to 1uF
P.47 Change C1238 ,C1242 to 270pF
P.62 PR207 change to 1R-0006342-F200(63.4K)

Final BOM until above

Need to release E-ECN to factory
P.10 Add R1429 0 ohm
P.43 Add R1388 0 ohm to BOM
P.8 Add R1430 ohm
P.31 Connect U29.AE5,AD5,AD9,AE9 to GND
P.21 Change C480 to NC
P.7 Add R1431 ,R1432 ,1433 , R1434 NV_ for Intel's seggestion
P.64 Change R1129 ,R1130 to NC condition
P.34 Del R1384 0 ohm ; add L115 (10uH) , C1307 (10uF)

(2005/09/23)

P.48 Change R926 mount to NC
p.36 Add CN32.51 to GND
P.8 Del R1221 , R1411 ,R1412 ,R1413 R1430

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PVT start

(2005/10/12)

P.62 Change PR207 to 41.2K ohm
P.61 change PC175 to 0.047uF
P.46 Mount Q88 for pop-noise
P.47 Mount Q91,Q92 ,R1340,R1344 ,Q89,Q90,R1273,R1281 for pop-noise
P.30 Change U72 , U73 to MC74VHC1G86DFT2G
P.7 Change R110 mont condition to NC
P.29 Change D7 to SK03-04T-G for D_SHIFT_+5V drop issue
P.58 Change +1_5VRUN's enable singal from RUN_ON1 to RUN_ON
P.22 Change Y2 27MHz from 30 PPMto 20 PPM
P.10 Change L7,L8 ,L115(P.34) to MAX ECHO vendor
P.39 Change U35 to MC74HC1G32DTT1G
P.46 Change U45 , U83 to MC74VHC1GT32DF2G
P.46 Change U103 to MC74VHC1GT04DF
P.49 Change L71,L72,L19,L20,L90,L91,L93,L95,L102,L103,L104,L105,L106 to EBMS160808A121
P.34 L60 ,L70(44) change to BCMS321611A121 5A
P.41 U107 pin 8 change from 8V to DCBATOUT for FAN can't full on issue for DVT short term solution
P.54 Change R1307 to 649 ohm
P.61 PQ53 change to IRF8113
P.37 Change R703 , R704 from 47K ohm to 470K ohm

(2005/10/29)

P.41 Change U107 to rail to rail type and swap pin2 & pin3 connection ; change Q33 to P-MOS
P.10 Change CAP5 , CAP6 mount condition to CA_
P.33 Change U30 pin 2 conection to EC_CLKEN# and add R1435 pull up R
P.37 Add U32 pin 105 EC_CLK_EN#
P.40 Change Q95 pin1 power source from +3VRUN to+3VSUS
P.64 Change Clock GEN's pin2 to EC_CLK_EN#
P.44 Swap JSPK1's pin define

(2005/11/03)

P.21 Q96, P41 Q33 ,P42 Q79 update MMC2301 layout footprint
P.39 Add J1 for factory request
P.29 Change CN4 to FOX_DZ11A91-NW205-4F for ID request
P.51 modify CN48's part number
P.42 Change CN47's part number

(2005/11/07)

P.52 Mount R1243,R1244,R1247,R1248 and change R1194 ,R1195 , R1198,R1199 to 0ohm R for no Oide SKU ; change the others to NC on this page
P.42Change CN21 , L67 ,C1086 ,R782 ,R787 to NC for no Oide SKU
P.41 Change C827 to 22uF for FAN VCC quality ; add D71
P.64 Change U18 to B version
P.52 Change CN29,CN28,CN37 to FOX_UB1112C-C1603-FR for ID request
P.30 Change CN6 to FOX_MH11747-PS2D-4F for ID request
P.49 Chagne CN23 to FOX_UV31413-VR56P-7F for ID request
P.28 Modify CN3 connector (add two dummy pad)
P.37 Add R1436 pull down R
P.41 Add C1308 reserve C

(2005/11/10)

P.37 Reserved R1438 ,R1437 , R1439 ,R1440 ,Q102 for RS11 reserve
P.39 Change SPR2,3,6 to 5.0X2.5

(2005/11/12)

P.39 Change CN44 pin1 to SUSPEND_LED and del C1285
P.37 Add R1441 0 ohm R on U32 pin 105 ; change R703 ,R704 to 470K ohm
P.37 Change U32.99 pin & CN30.71 pin net name to DOCK_RUN_RST#
P.37 Add R1442 pull up R ; change R703 , R704 to 47 K ohm

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(2005/11/14)

P.64 Add R1443 ,R1444 2.2ohm R
P.43 Change U39 to Kversion
P.52 Change CN30.5 name to AND_DOCK_S5_RST_500
P.52 Change CN30.26 name to DK_BAY_PWREN
P.43 Change C863 to 1uF for pop noise
P.46 Change C1188 to 4.7uF for pop noise
P.44 Change Q77 , Q78 ,Q84, Q85 to PBSS2515 for procurement issue
P.47 Change Q89 , Q90 ,Q91, Q92 to PBSS2515 for procurement issue
P.33 Del R649
P.48 Change U58 pin j2 CN46 pin 10 net name to MS_LED
P.31 Change R579,R580,R581's power souce to +3VSUS

(2005/11/14) Power modify

P.56 Add PC370 connect PQ11 pin3
P.56 Change PR391 to 10K_J ,PR349 to 15K_F same MS20 setting
P.59 Add PC371 connect to +1_8VSUS back up for output ,no mount
P.60 Add PR416 0ohm R and del PR272 pull up R
P.61 Change PR410 , PC369 , PQ105 , PR411 , PR413 to NC condition
P.61 Change PQ104 pin1 net name to A6703

(2005/11/15)

P.44 Bypass R1186 , R1185
P.43 Add R1445 , Q103 and add P.61 A603 port
P.43 Add R1446 , R1447 , R1448 ,R1449 mount option
P.36 Add R1450 reserved R
P.64 Del R1443 , R1444 to 0ohm R
P.40 Add Q104 for WLAN LED issue
P.32 Add Q105 , Q106 , R1451 ,R1452 for leakage voltage
P.41 Change R1377 to 390 ohm for ME request

(2005/11/16)

P.41 Change LED9 to HT-110NB5 for ME request
P.40 Add R1453 reserved R
P.29 Change U76 pin 10 , 11 net name to MB_DDCCLK & MB_DDCDATA
P.29 Change CN4 pin 15,12 & R483 pin2 , R487 pin2 netname to MB_CRT_DDCLK ,MB_CRT_DDCDATA
P.30 Del R1060 , R1059 and connect U77 pin 9 to GM_OR_NV_DDCCLK ; connect U77 pin 12 to GM_OR_NV_DDCDATA
P.30 Connect U77 pin 10 , 11,13,14 to MB side and docking's CRT DDC CLK and DATA signal
P.33 Add Q107 and R1454 for RUNTIME_SCI# leakage current

(2005/11/18)

P.23 Change R340,R344,R347,R348,R351,R352,R357,R358,C499,C501 to NC condition
P.28 Del R1390 and connect U106 pin 1 to INV_EN_EC
P.43 Add R1455 0 ohm R
P.16 Add R1457 , U108 , R1456 for Nvidia reset glith issue
P.16 Add R1458 33ohm

(2005/11/18) Power modify

P.61 Del PJ36 then add GP15 at PJ36 location for short +1_05VSUS with +1_05VRUN
P.61 No mount PQ103

Any change need to modify BOM by manual

(2005/11/19)

P.42 C1222 change to 2,2uF

MP schematics modify

PVT released ECR to modify BOM as below list :

(2005/12/03)

P.42 Change C1222 from 2.2uF to 1uF ; R1267 change to 10K ohm
P.33 R1435 change from 10Kohm to 2K ohm
P.43 Add R1446 and R1447 ; Del R1448 , R1449 at BOM
P.37 Del R1441 and add PR416 for CLK_EN# control by Max8771
P.17 Del R225,R228 and add R226 , R227 for 3GIO_PADCFG setting
P.22 Change U8 from 0.26p to 0.28p version
P.22 Change Y2 mount condition to NV_

Power modify

P.56 PD1 change to SSM34PT
P.60 Change PR138 to 15K ohm
P.60 PD18,PD45 change to SSM34PT
P.56 Change PQ84 to AO4607

New modify for MP stage (including BOM and schematics)

(2005/12/09)

P.57 Add PR417 1K ohm pull-low for +ECVCC discharge circuit (modify layout)
P.42 Add R1459 , R1460 pull up resistor for ExpressCard logo apply (modify la
P.43 Change U39 footprint to QFN package only (modify layout)

P.40 Del TP267 for layout space tight issue

(2005/12/12)

P.16 Change R1457 , U108 , R1458 to NV_ condition

(2005/12/13)

P.42 Change R1459 , R1460's power source to +3VAUX_PCIE_OUT (modify layout)

(2005/12/14)

P.42 Del R1459 , R1460 for layout space critital issue (modify layout)

P.22 Change U10 to G-100(down scale 1%) for G72M can accept 1.25% issue

(2005/12/15)

P.46 Change C1232 to 0.68uF and C1230 change to 470pF for bandwidth change
P.61 Change PQ54 , PR412 , PR169 , PR168 , PC175 , PQ53 PC174 to NV_ condition
P.42 Add C1309 for CAM quality progress
P.61 Change PR402 , PQ102 to NV_ mount condition

(2005/12/16)

P.42 Delete C1309.

(2005/12/19)

P.62 For UL_IN# lock issue

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