



PCB

DA8000B000

Compal Confidential

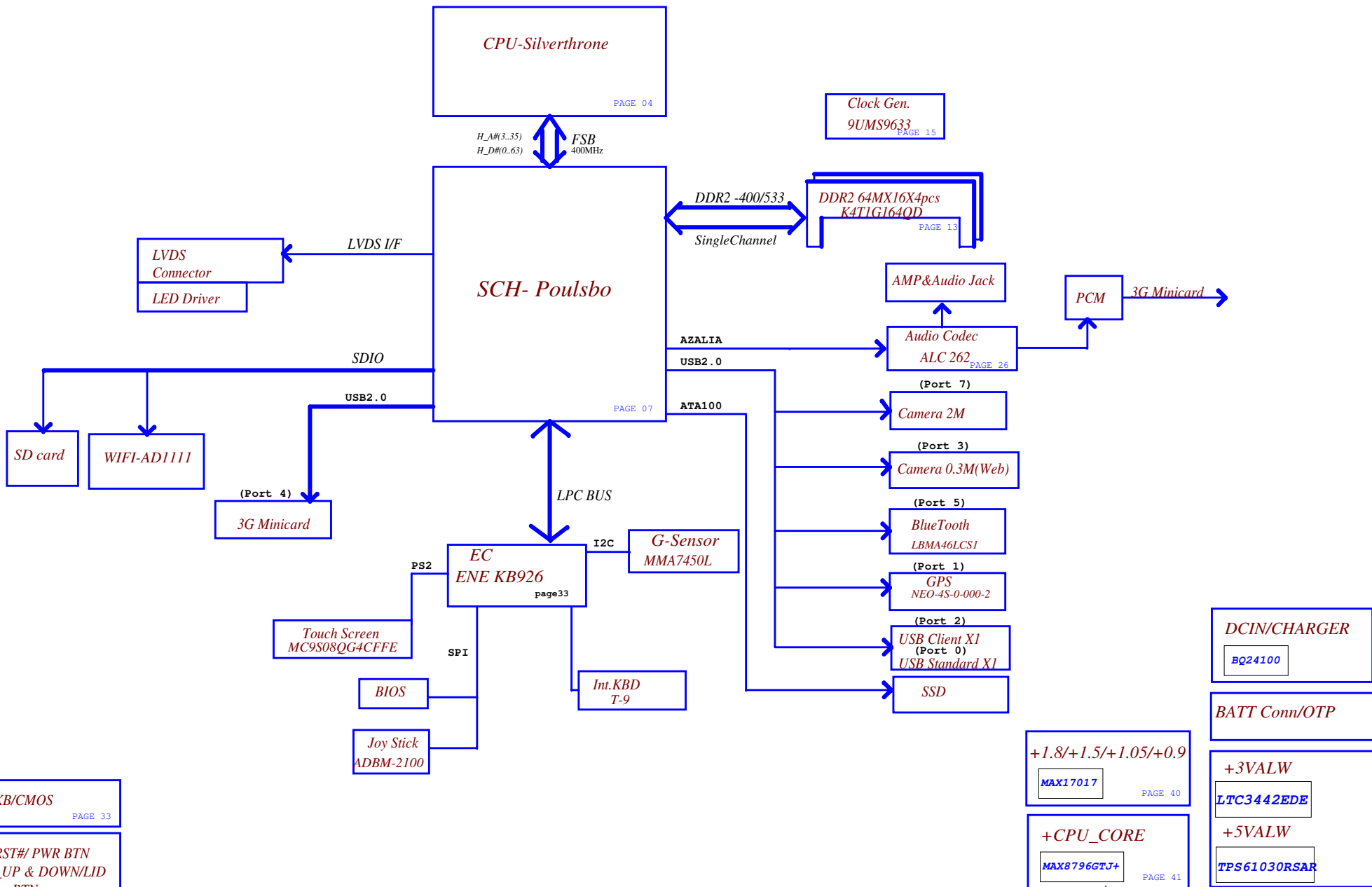
Amazon Schematics Document

Menlow-Silverthorne with Poulsbo

Monday, April 28, 2008

REV: 0.2

| | | | | | |
|---|------------|--------------------|------------|---------------------------------|---------|
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| Issued Date | 2006/08/04 | Deciphered Date | 2006/10/06 | Compal Electronics, Inc. | |
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| | | | | Document Number | Rev |
| | | | | Amazon(Menlow) | 0.2 |
| Date: | | | | Sheet | 1 of 43 |



INT KB/CMOS
PAGE 33

RTCRST#/ PWR BTN
VOL_UP & DOWN/LID
Shutter BTN
PAGE 33

| | | | | | |
|---|------------|--------------------|------------|------------------------------|-----------------|
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| Issued Date | 2006/08/04 | Deciphered Date | 2006/10/06 | Block Diagram | |
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| | | | | Sheet | 2 of 43 |

Voltage Rails O MEANS ON X MEANS OFF

| power plane / State | +VBAT | +5VALW +3VALW | +1.8V +0.9V | +5VS +3VS +1.8VS +1.5VS +CPU_CORE +VCCP | CLOCK |
|--------------------------------|-------|------------------|----------------|--|-------|
| S0 | O | O | O | O | O |
| S3 | O | O | O | X | X |
| S5 S4/AC | O | O | X | X | X |
| S5 S4/ Battery only | O | X | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X | X |

O MEANS ON S3 : STR
X MEANS OFF S4 : STD
 S5 : SOFT OFF

SKU ID Table

| Vcc | 3.3V +/- 5% | | | |
|----------|-------------|-------------------------|-------------------------|-------------------------|
| Ra | 100K +/- 5% | | | |
| Board ID | Rb | V _{AD_BID} min | V _{AD_BID} typ | V _{AD_BID} max |
| * 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

| SKU ID | MB ID (H) | MB ID (L) |
|--------|-----------|-----------|
| 0 | | |
| * 1 | IEL10 | |
| 2 | IDL11 | IDL01 |
| 3 | HDL10 | HDL00 |
| 4 | | HDL20 |
| 5 | IDL12 | HDL30 |
| 6 | | |
| 7 | | |

| | MB ID |
|---|-------|
| H | JAX10 |
| L | JAX60 |

TBD

BOM Structure

| MARK | FUNCTION |
|------|------------|
| @ | NC FOR ALL |
| | |
| | |
| | |

Address

USB PORT LIST

| PORT | DEVICE |
|------|---------|
| 0 | SPR |
| 1 | Client |
| 2 | SPR |
| 3 | CMOS |
| 4 | 3G, GPS |
| 5 | BT |
| 6 | |
| 7 | |

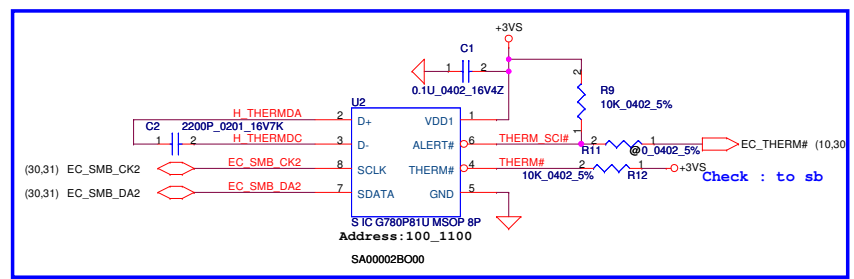
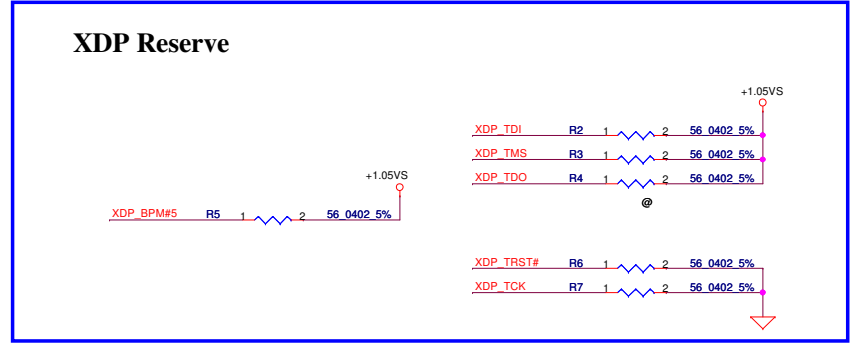
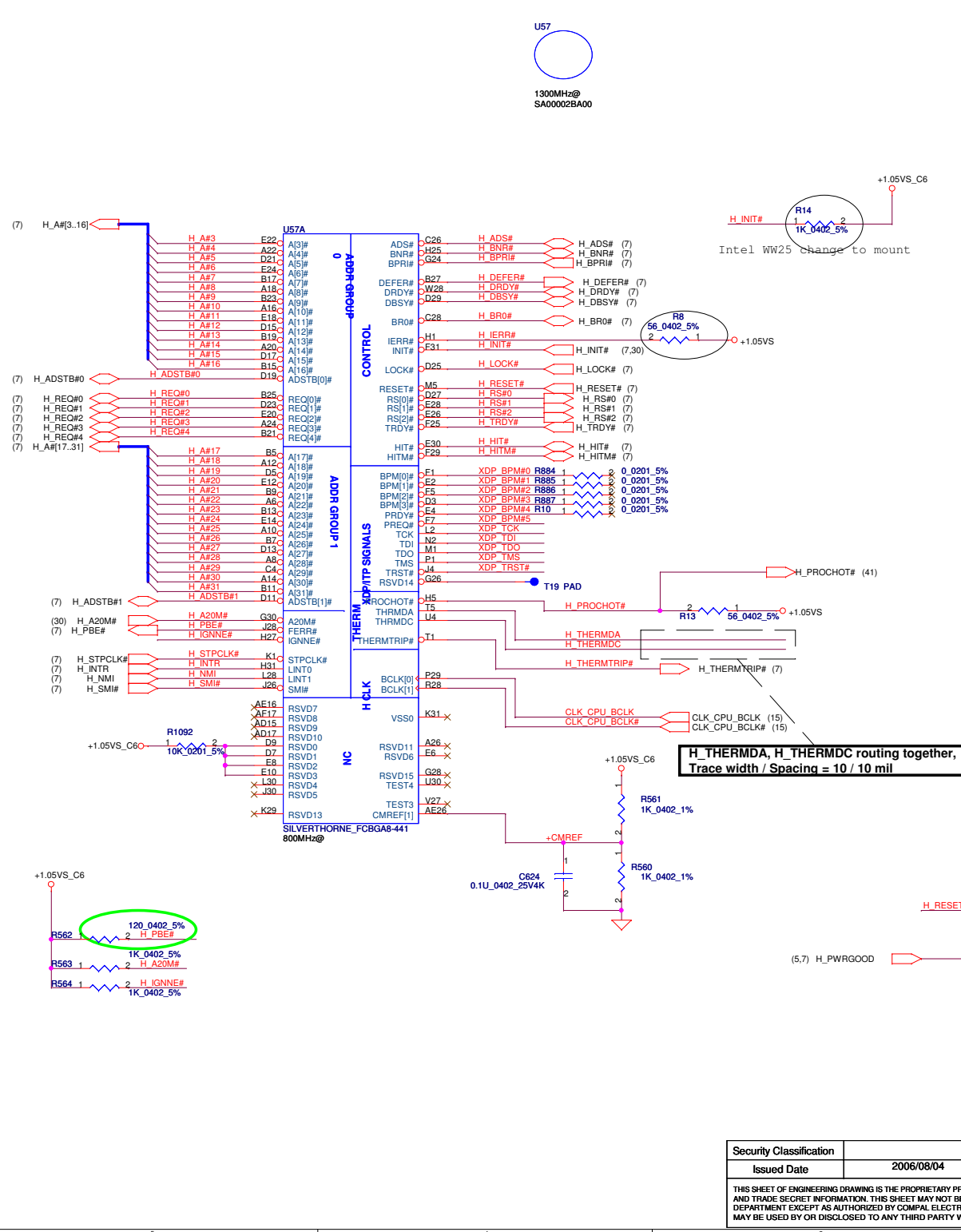
EC SM Bus1 address

EC SM Bus2 address

| Device | Address | Device | Address |
|------------------|-------------|---------|-------------|
| EEPROM(24C16/02) | 1010 000X b | ADM1032 | 1001 100X b |

Poulsbo SM Bus address

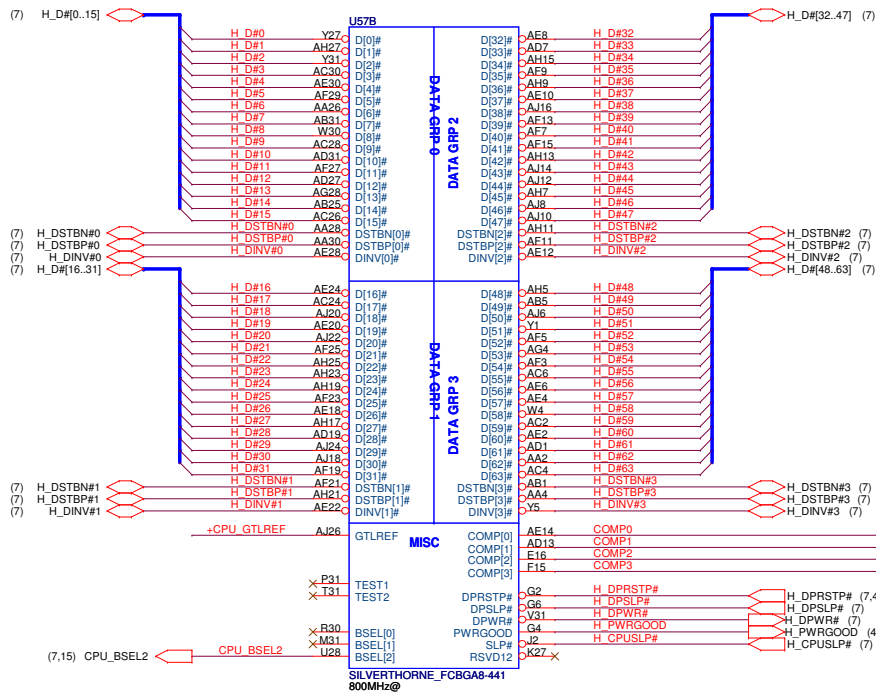
| Device | Address |
|-----------------------------|------------|
| Clock Generator (ICS954226) | 1101 001Xb |



**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

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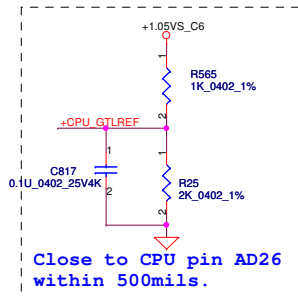
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|----------------------------|------------------------|---------------|
| Title | | |
| Silverthorne(1/3)-AGTL+XDP | | |
| Size | Document Number | Rev |
| Custom | JAX60 | 0.2 |
| Date: | Monday, April 28, 2008 | Sheet 4 of 43 |

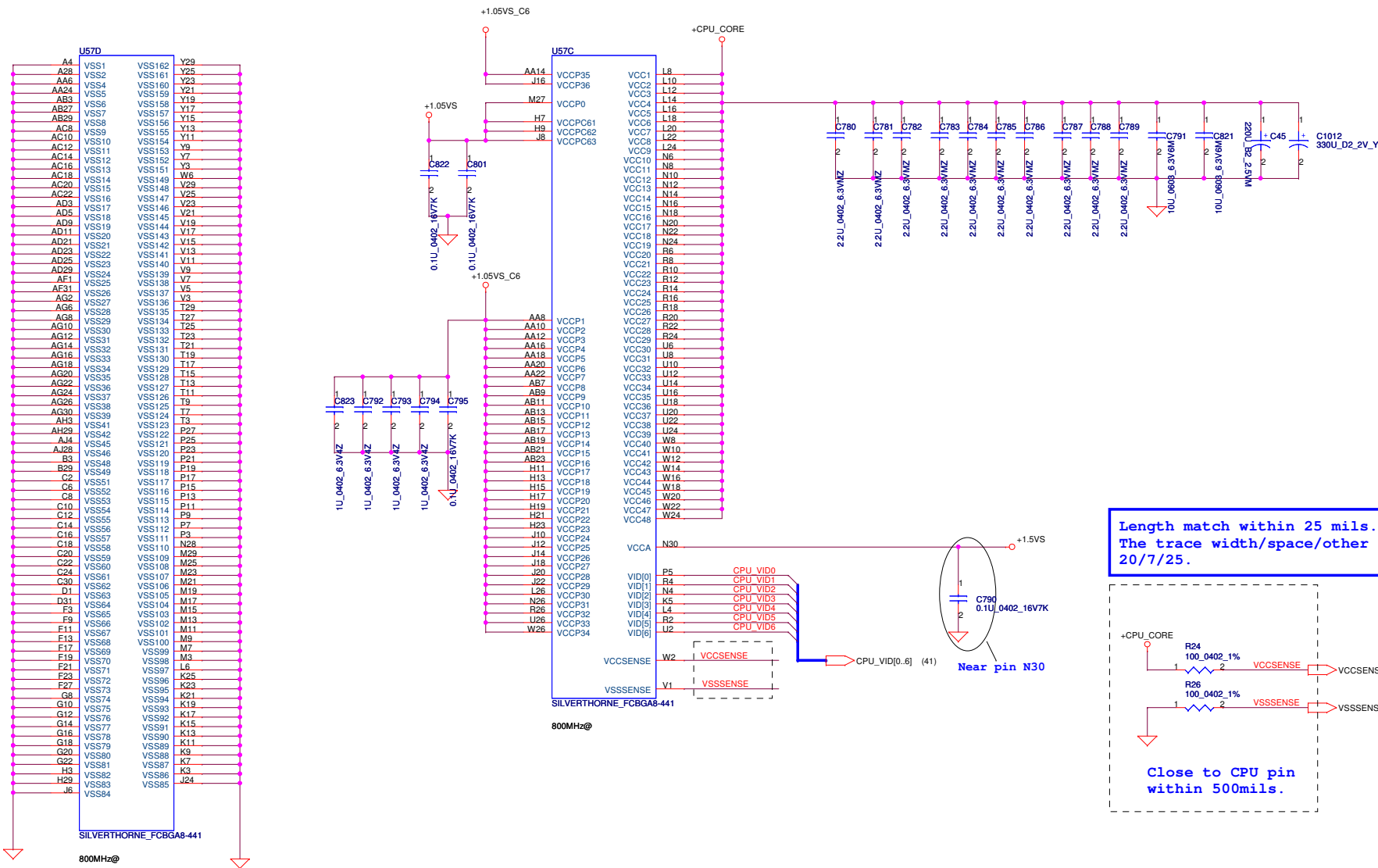


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

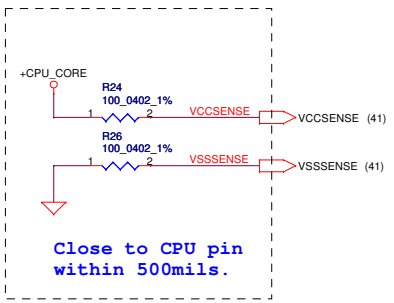
| CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0 |
|----------|-----------|-----------|-----------|
| 100 | 1 | 0 | 1 |
| 133 | 0 | 0 | 1 |

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

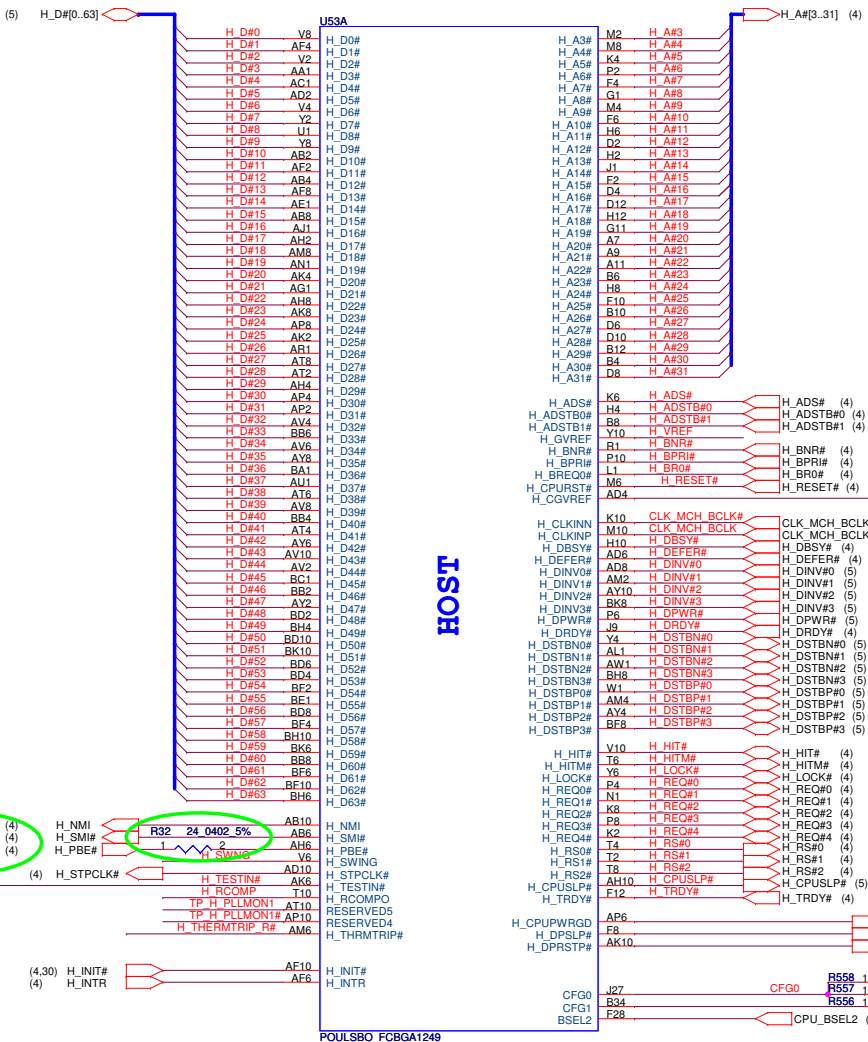




Length match within 25 mils.
The trace width/space/other is 20/7/25.



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| Size | Document Number | Date: | Monday, April 28, 2006 | Sheet | 6 of 43 |
| Custom | JAX60 | | | | Rev 0.2 |

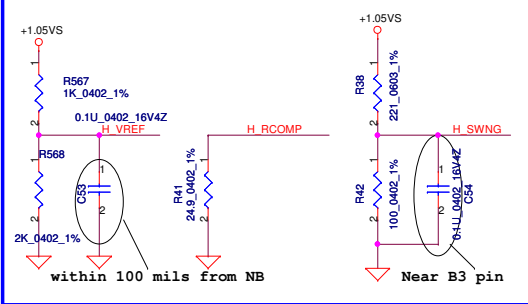


HOST

In pre-ES R571=2k H_CGVPREF=2/3VCCP
In ES R571 choose 1k

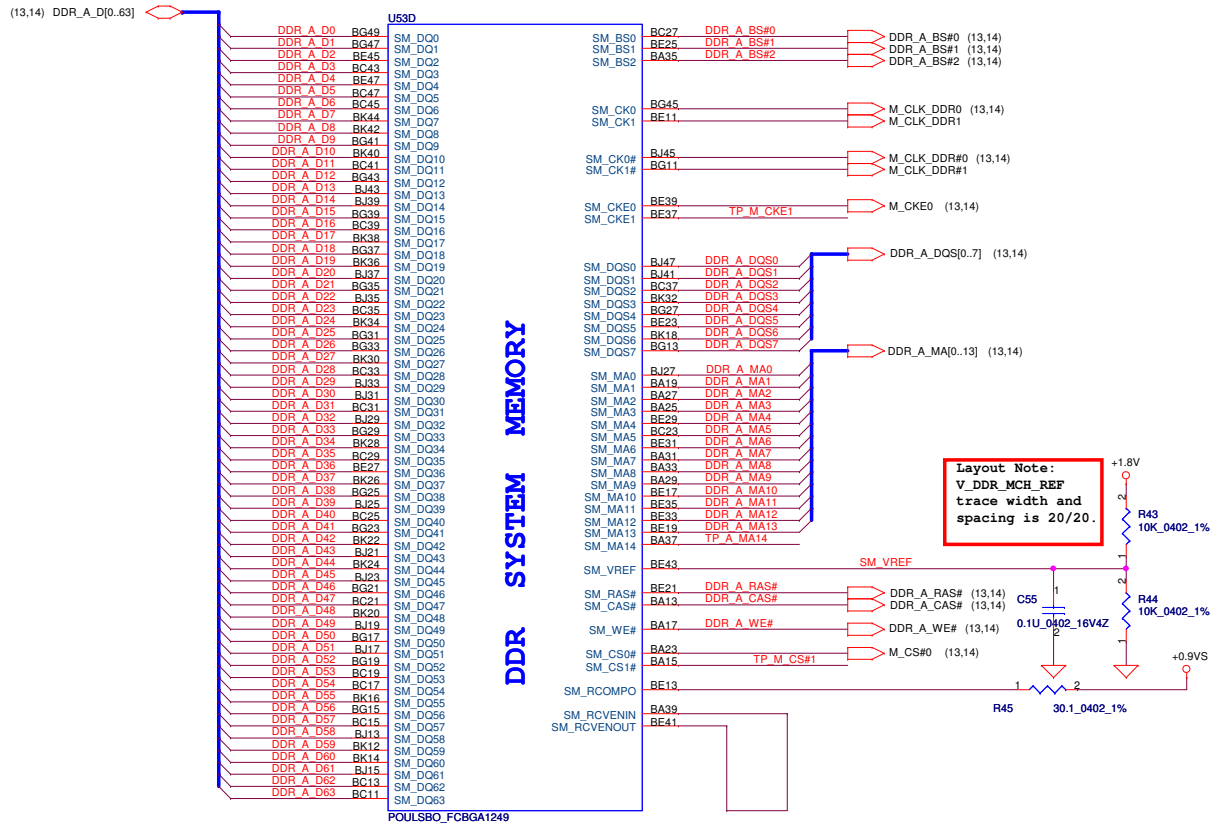
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

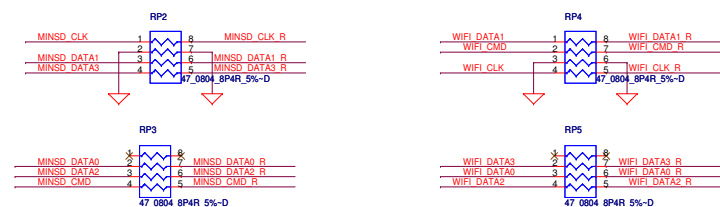
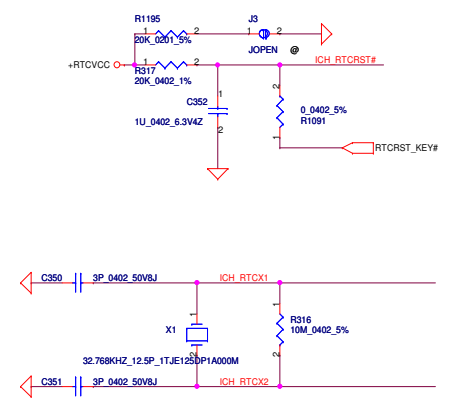
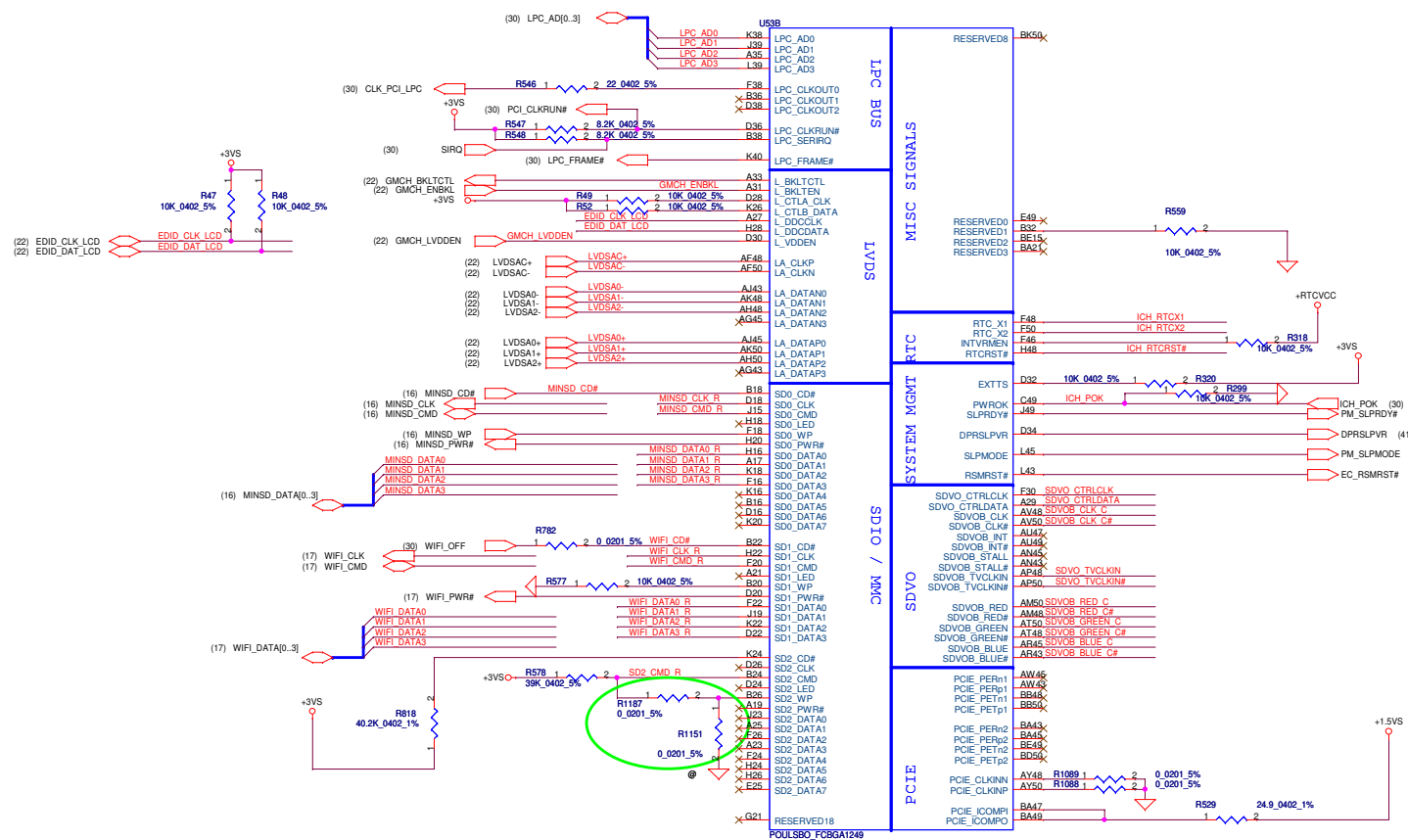


| FSB | BSEL2 | CFG1 | CFG0 | FSB DDR |
|-----|-------|------|------|---------|
| 100 | 1 | 0 | 0 | 100 |
| 133 | 0 | 0 | 1 | 133 |

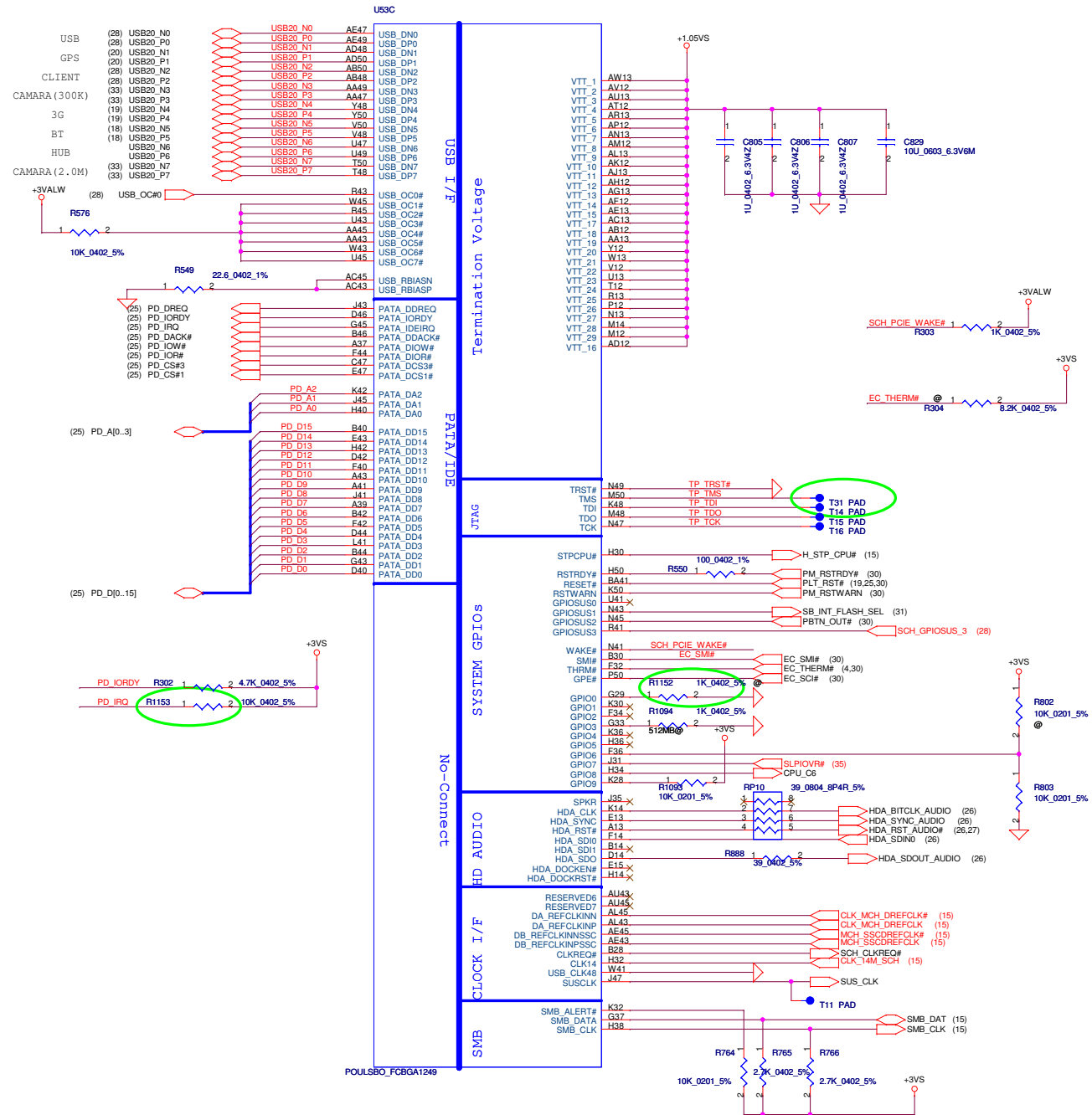
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| Date: | Monday, April 28, 2008 | Sheet | 7 | of | 43 | |



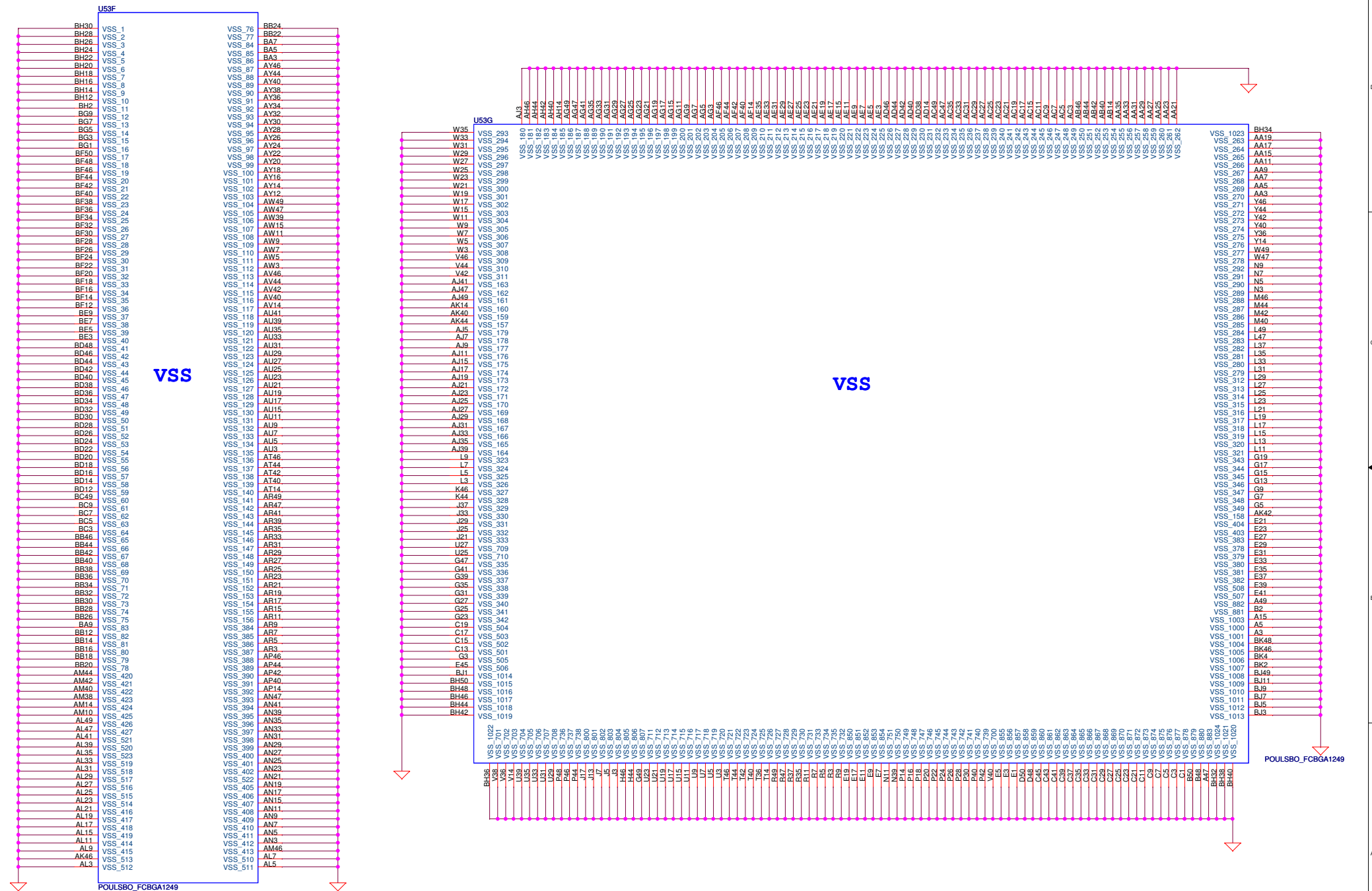
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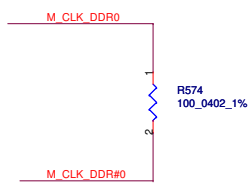
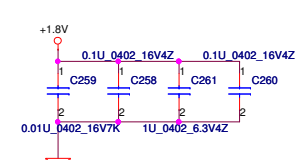
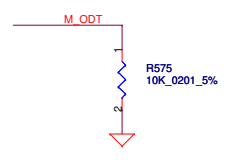
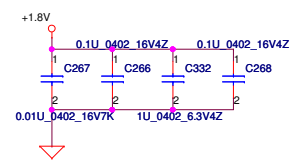
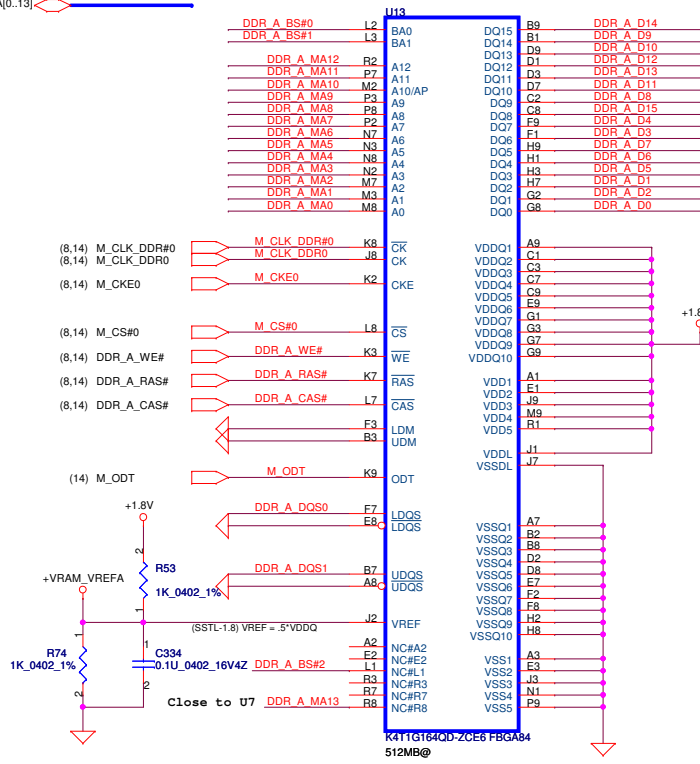


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| JAX60 | | Monday, April 28, 2008 | | 10 | 0.2 |
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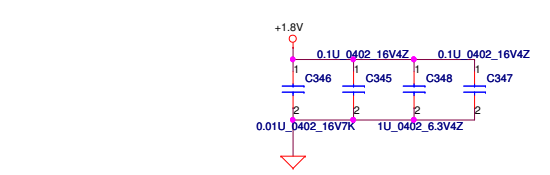
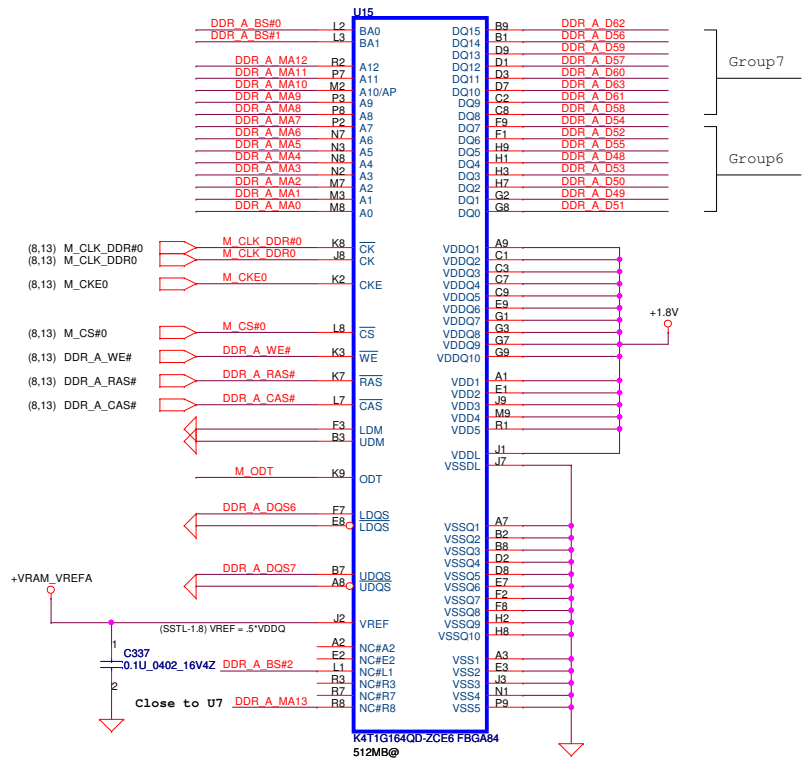
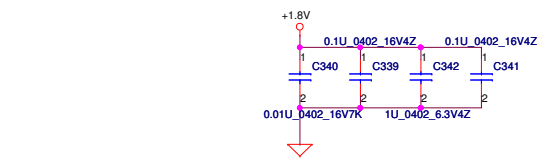
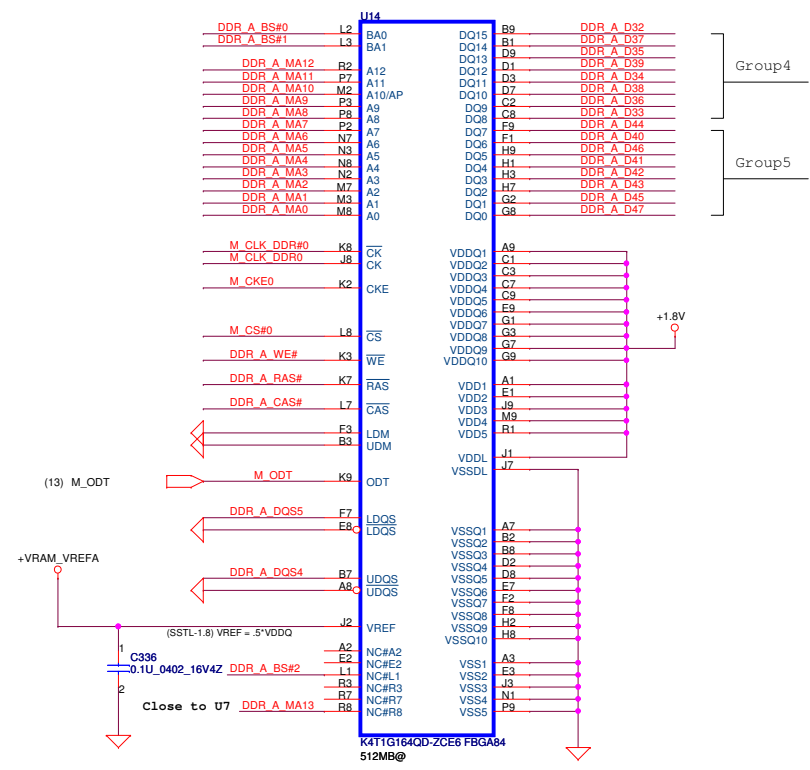
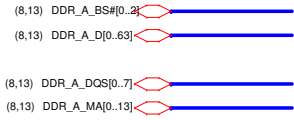


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| Sheet 12 of 43 | | | | Rev 0.2 |

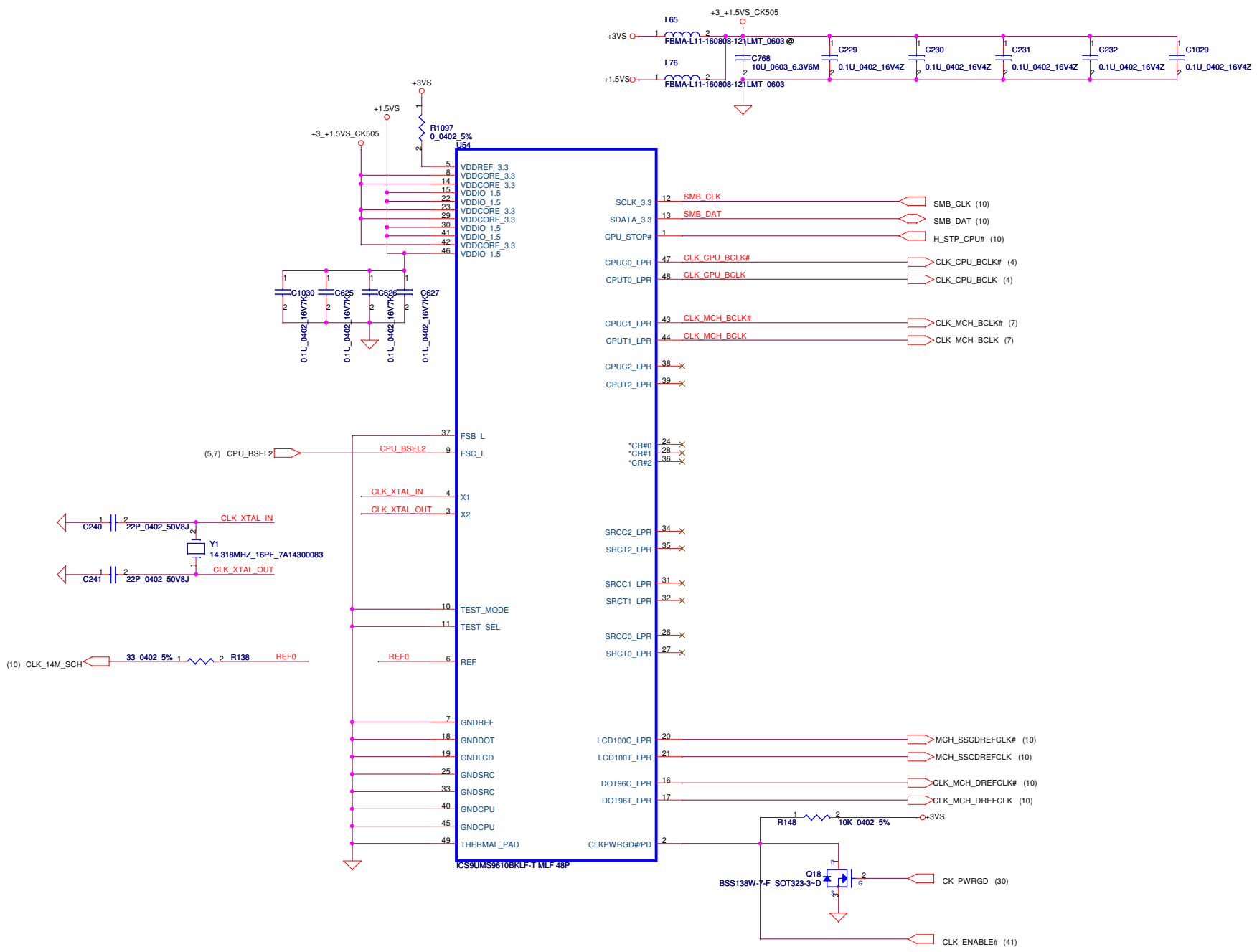
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 (8,14) DDR_A_DQS[0..7]
 (8,14) DDR_A_MA[0..13]



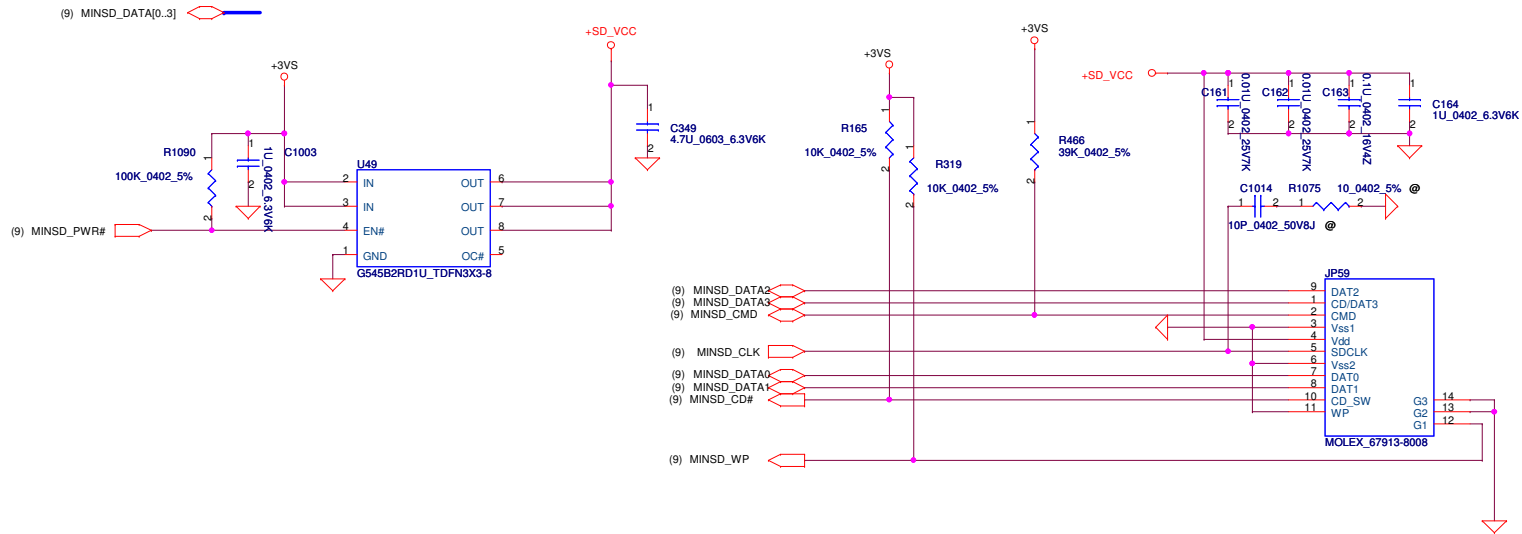
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| Date: | Monday, April 28, 2008 | Sheet | 13 of 43 | Rev 0.2 |



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| | | | | Size | Document Number | Rev |
| | | | | JAX60 | | 0.2 |
| Date: | Monday, April 28, 2008 | Sheet | 15 | of 43 | | |



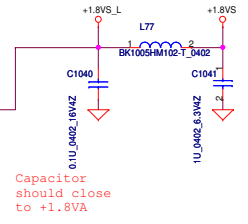
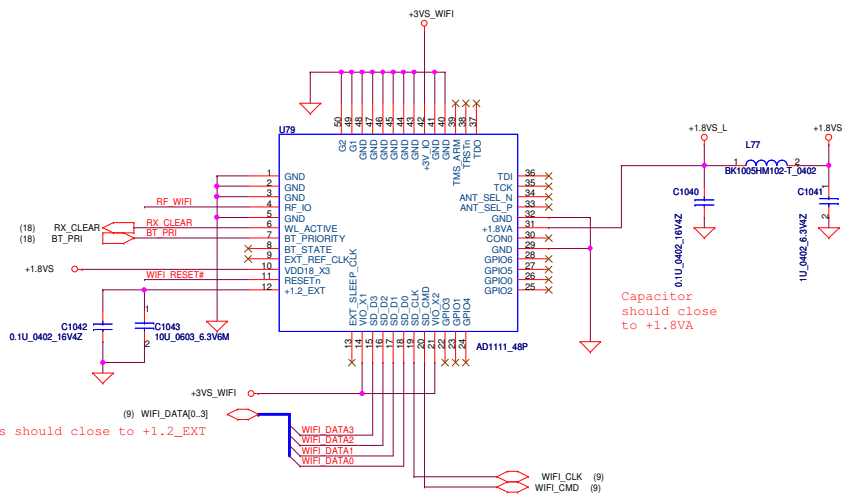
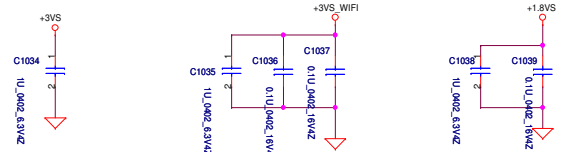
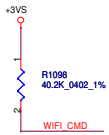
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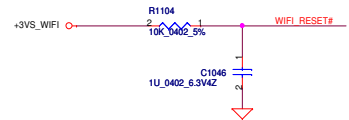
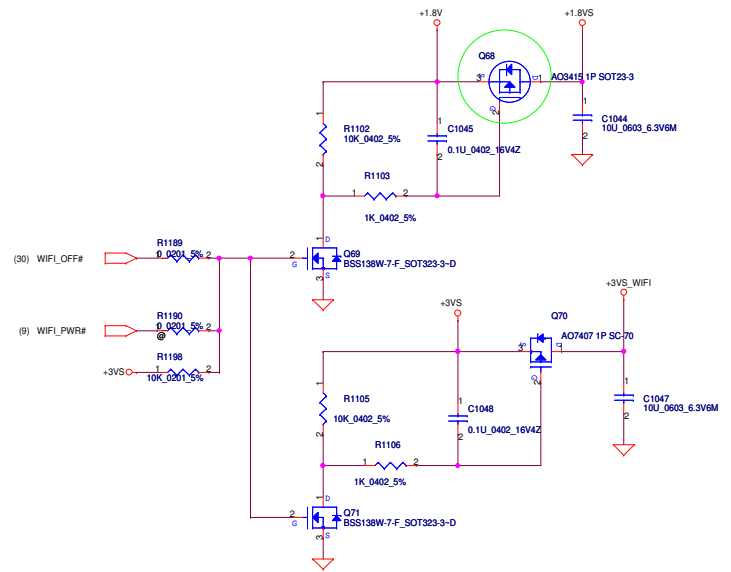
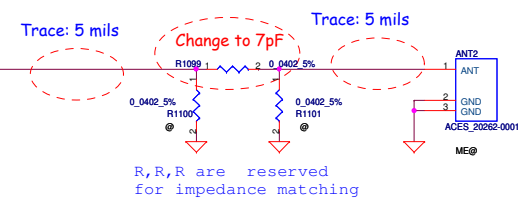
Monday, April 28, 2006

3.3V operation 120mA
 1.8V operation 200mA

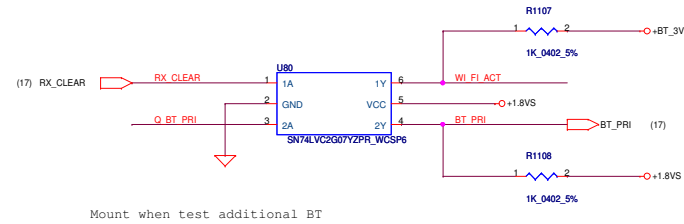
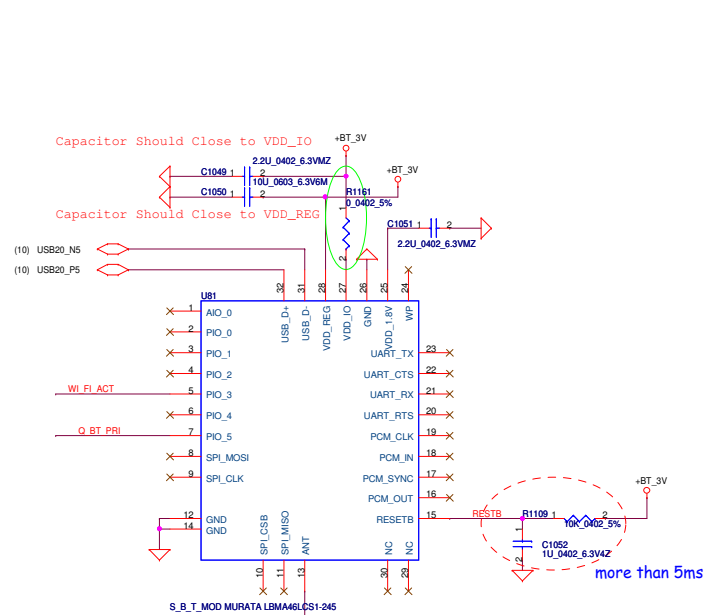
SDIO Signal Level



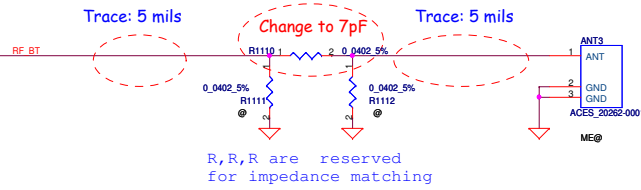
Capacitors should close to +1.2_EXT



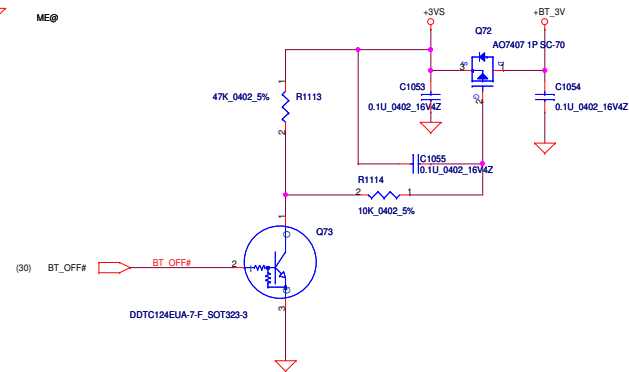
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| Date: Monday, April 28, 2008 | | | | Rev 0.2 |
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Mount when test additional BT

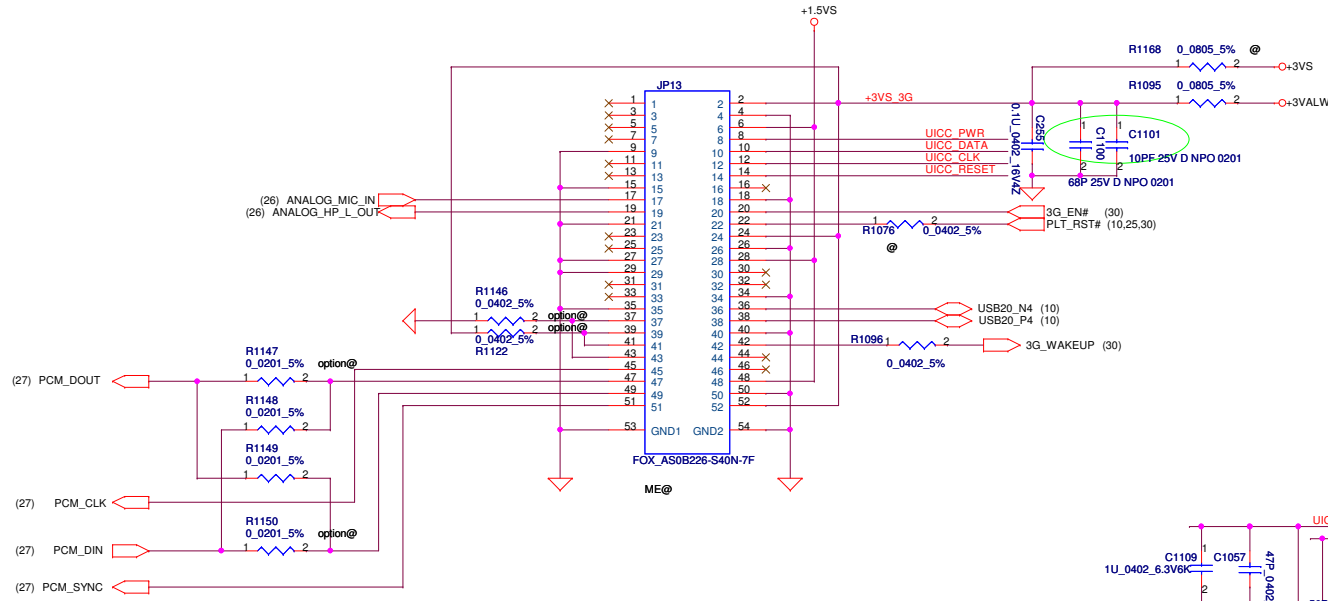


R,R,R are reserved for impedance matching

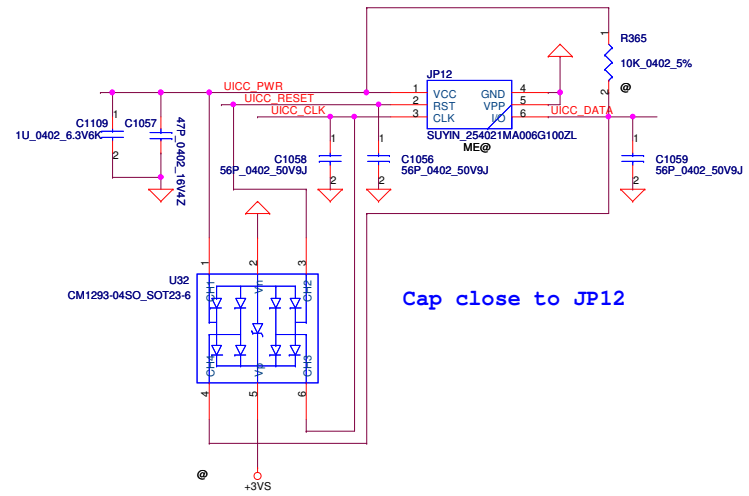


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| Size | | | Document Number | 0.2 |
| Date | | | JAX60 | Monday, April 28, 2008 |
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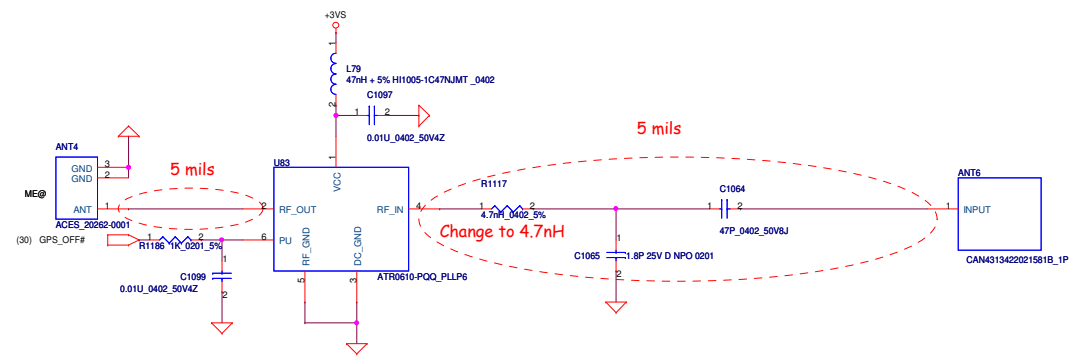
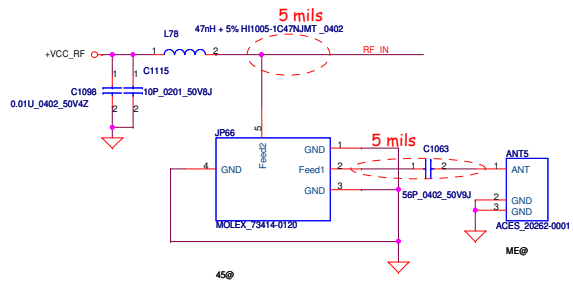
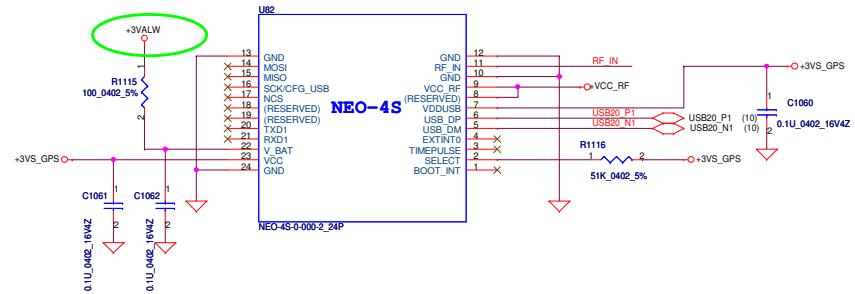
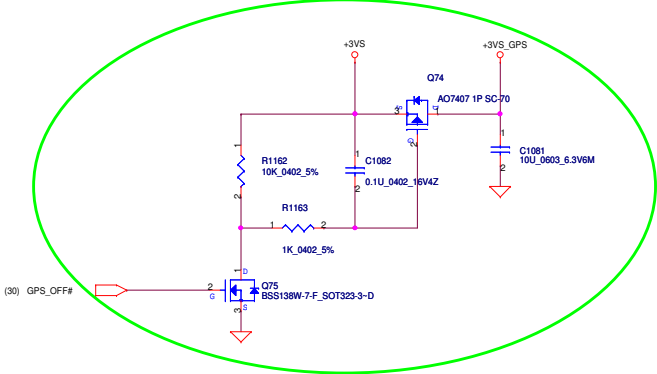
MINI-EXPRESS CARD



SIM Connector



| | | | | | | |
|---|--------------------|-----------------|------------|--------|------------------------|----------------|
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| | | | | Date: | Monday, April 28, 2006 | Sheet 19 of 43 |



| | | | | | |
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| | | | | JAX60 | 0.2 |
| | | | | Date: Monday, April 28, 2008 | Sheet 20 of 43 |

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| Date: | Monday, April 28, 2008 | Sheet | 21 | of 43 |

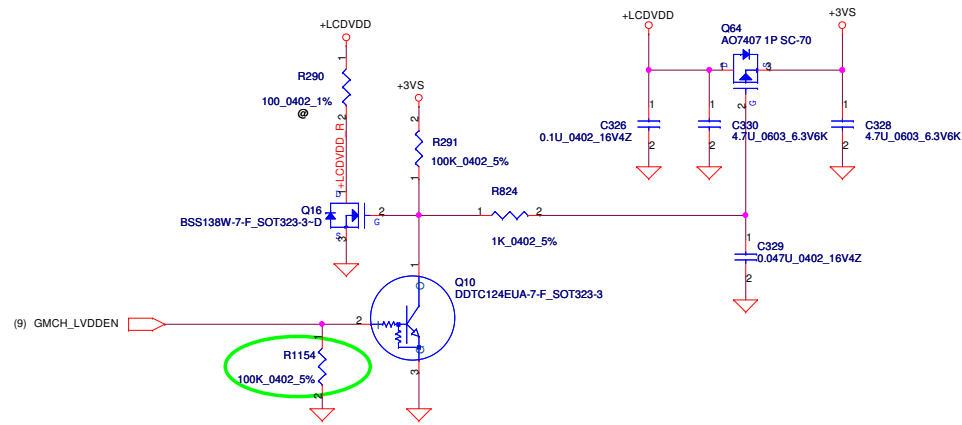
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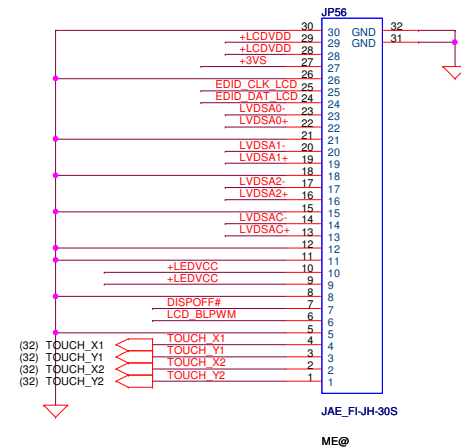
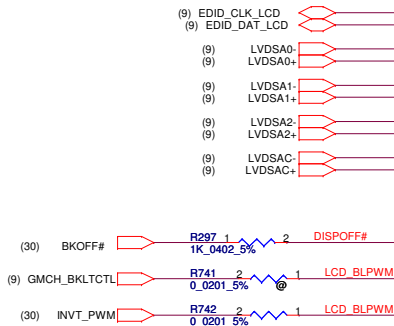
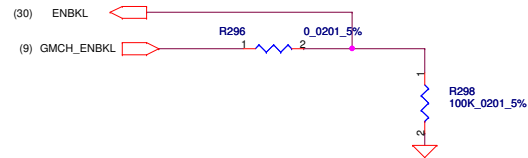
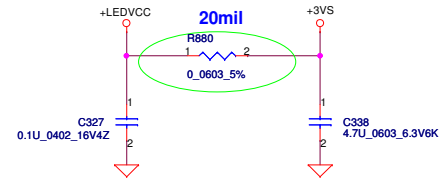
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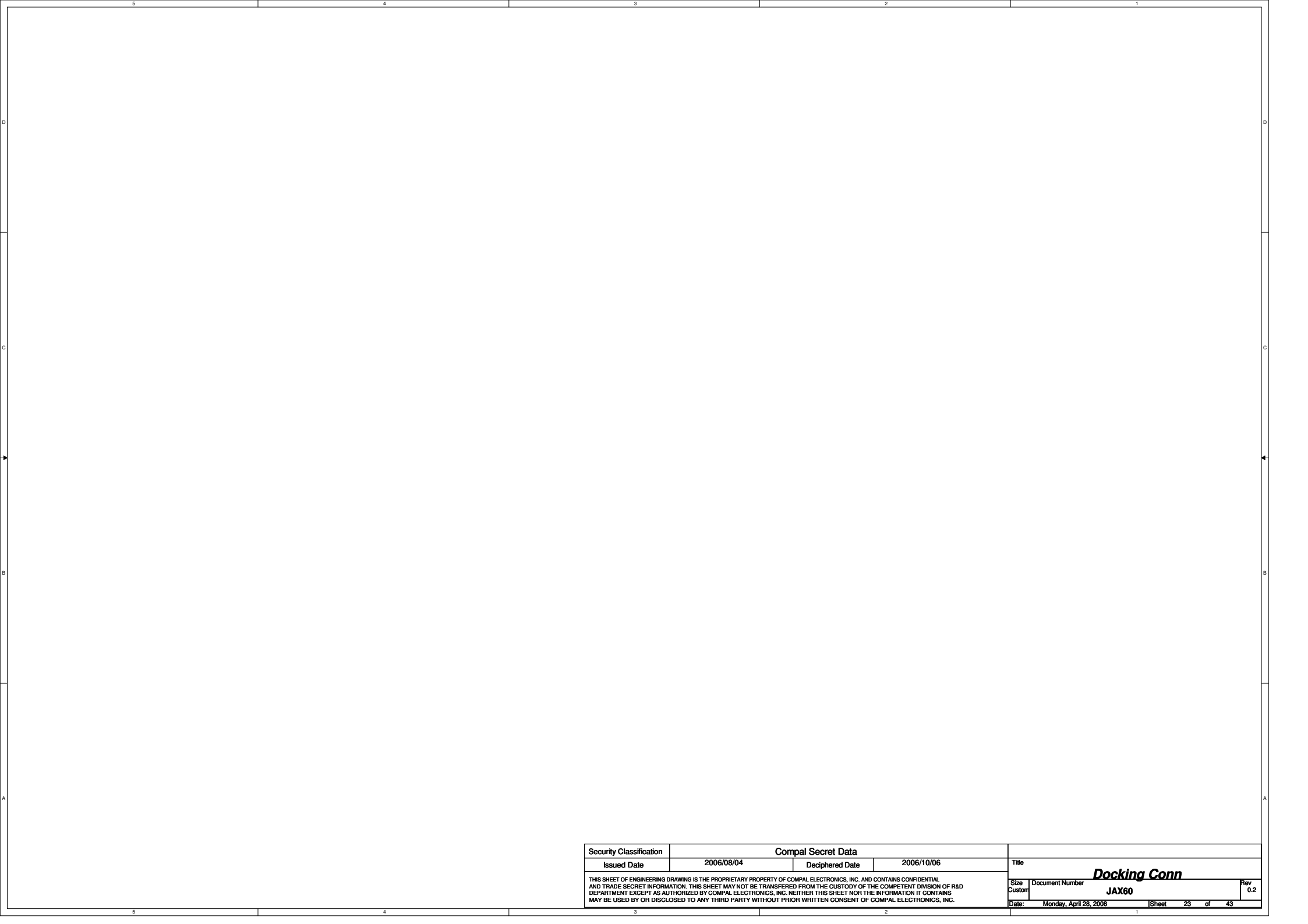


**LED Driving 2 parallel string of 6 serial
power consumption 1.6W 0.5A max**



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| Size | | | Document Number | | |
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| | | | | Custom | JAX60 |
| | | | | Date: | Monday, April 28, 2008 |
| | | | | Sheet | 23 of 43 |

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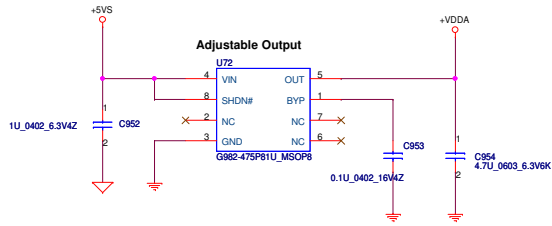
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Regulator for CODEC



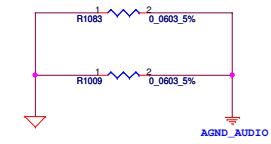
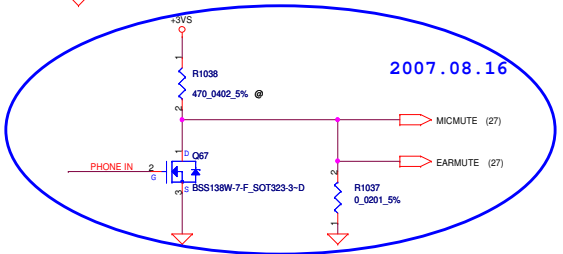
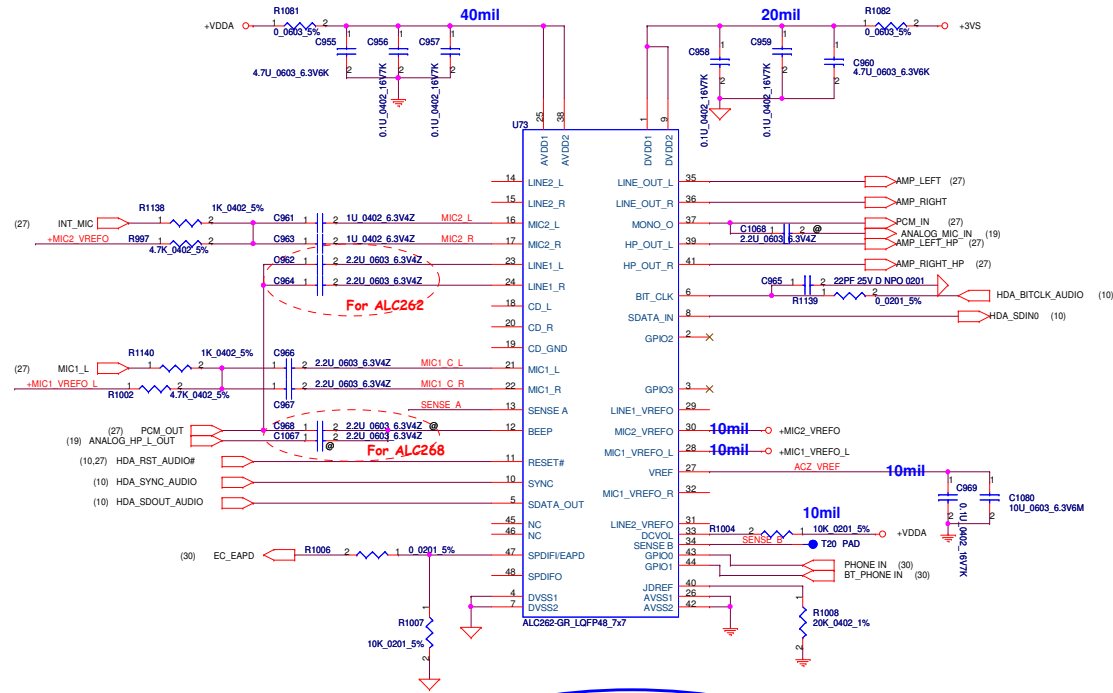
| | GPIO Low | GPIO High |
|------------|------------------------------|--|
| GPIO1 Low | codec phone call mode is off | codec phone call mode on |
| GPIO1 High | codec phone call mode is off | codec phone call mode on But Headphone/Speaker/Mic are off) Bluetooth is enabled |

HD Audio Codec

SENSE FOR Ext. Mic.

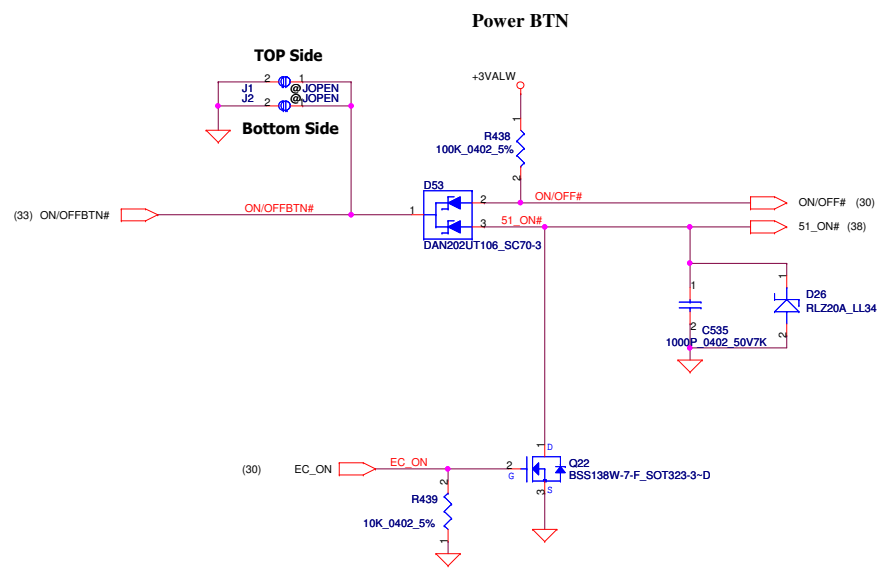


SENSE FOR HP

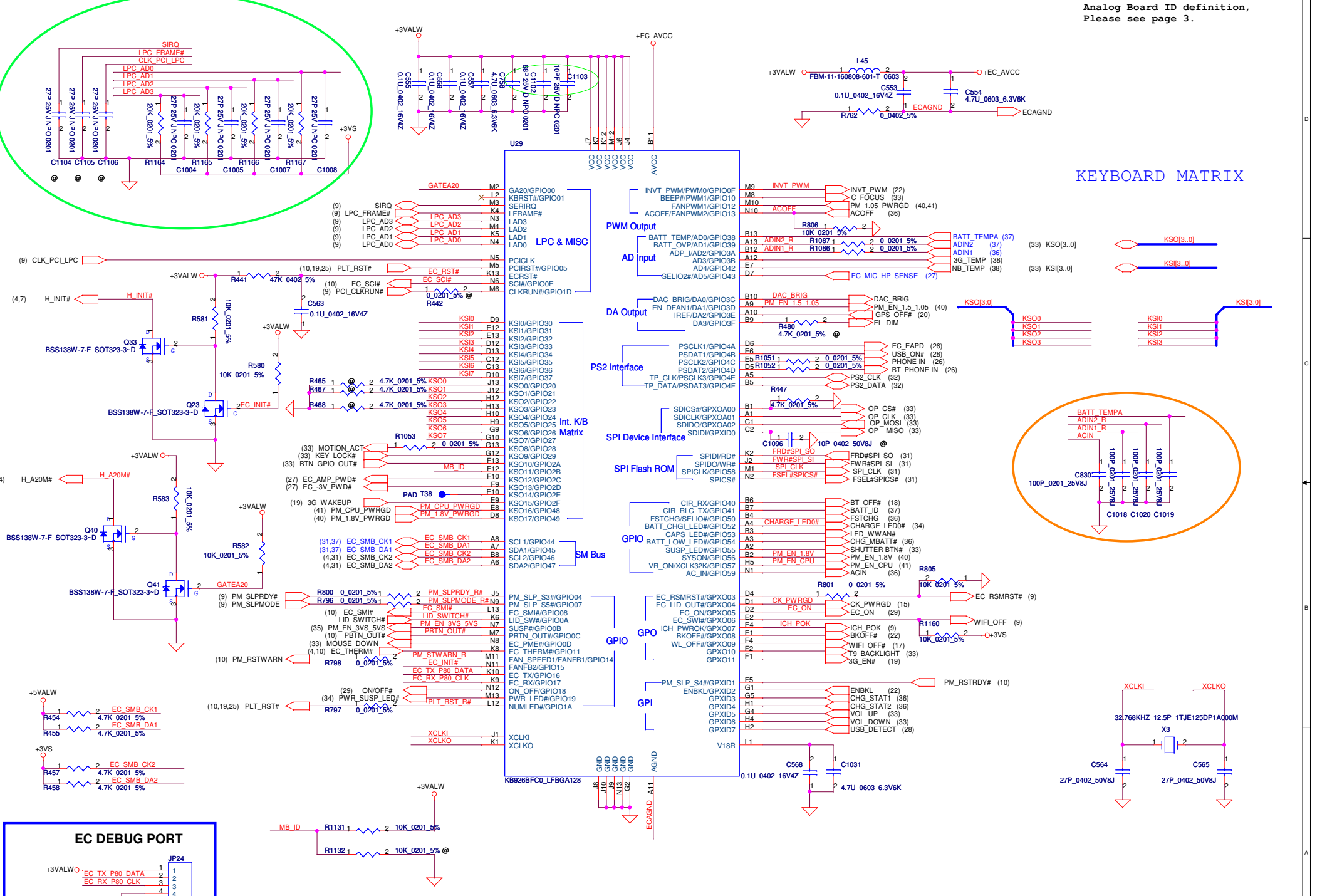


| Sense Pin | Impedance | Codec Signals |
|-----------|-----------|---------------------|
| SENSE A | 39.2K | PORT-A (PIN 39, 41) |
| | 20K | PORT-B (PIN 21, 22) |
| | 10K | PORT-C (PIN 23, 24) |
| | 5.1K | PORT-D (PIN 35, 36) |
| SENSE B | 39.2K | PORT-E (PIN 14, 15) |
| | 20K | PORT-F (PIN 16, 17) |
| | 10K | PORT-G (PIN 43, 44) |
| | 5.1K | PORT-H (PIN 45, 46) |

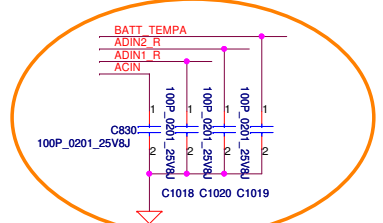
2007.08.16



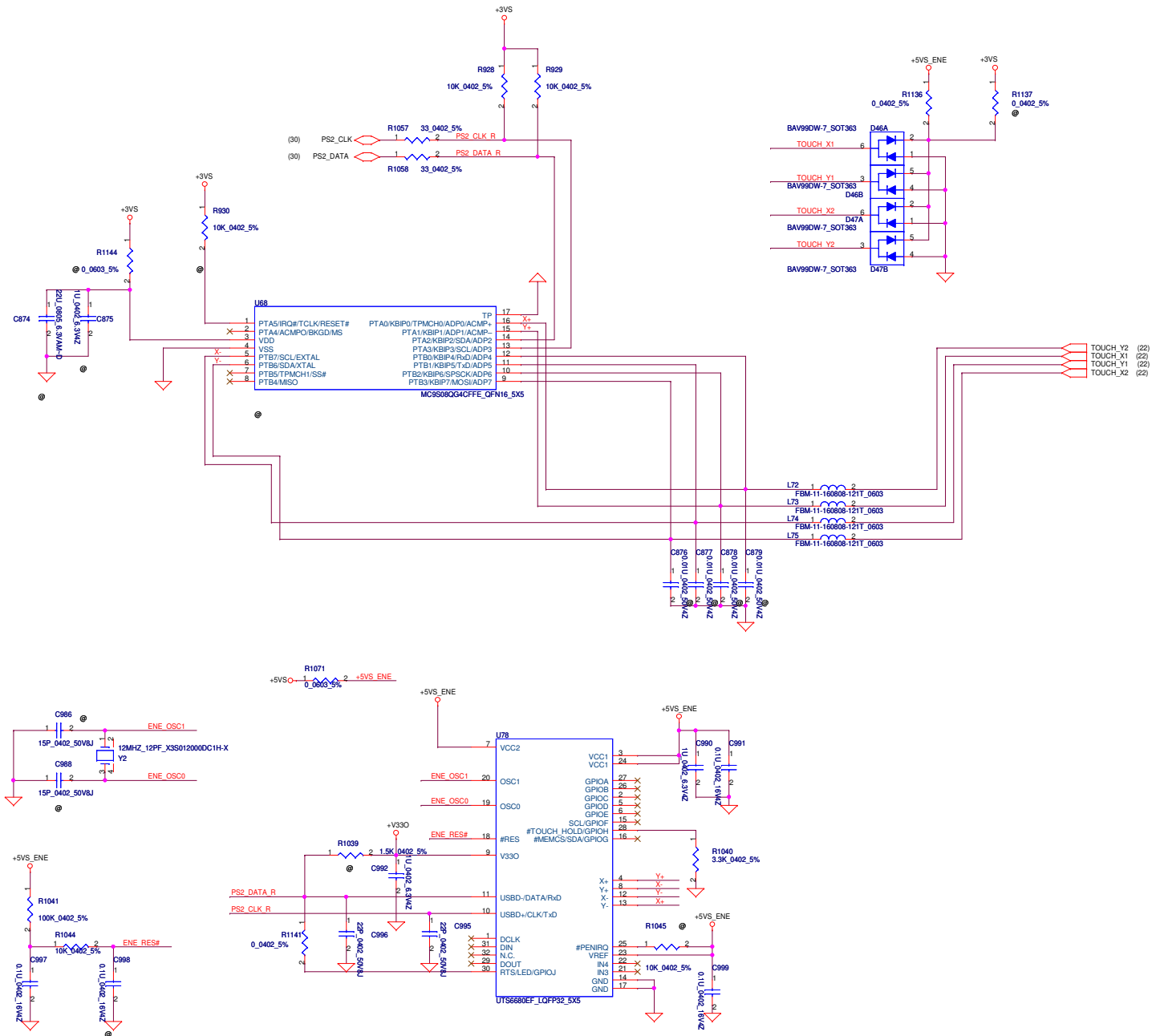
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
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| | | | | Date: Monday, April 28, 2006 | Sheet 29 of 43 |



KEYBOARD MATRIX



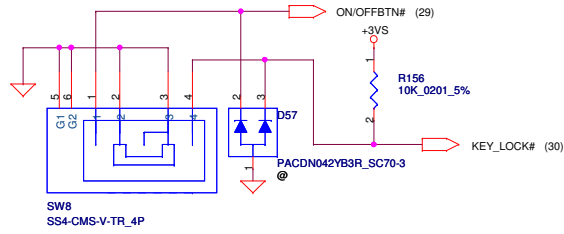
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| 2006/08/04 | | 2006/10/06 | | ENE-KB926 | |
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| JAX60 | | 30 | 43 | 0.2 | |
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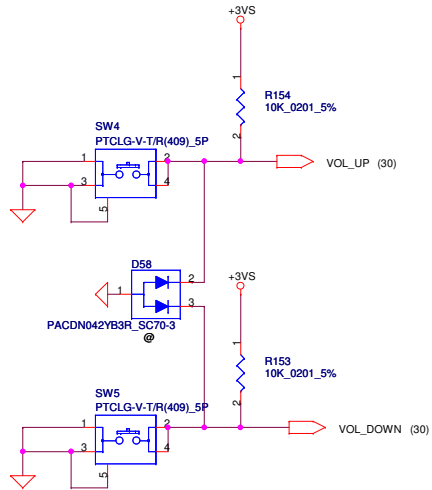
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| Issued Date | 2006/08/04 | Deciphered Date | 2006/10/06 |
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|---------------------------------|------------------------|
| Compal Electronics, Inc. | |
| TOUCH SCREEN | |
| Size | Document Number |
| C | JAX60 |
| Date | Monday, April 28, 2008 |
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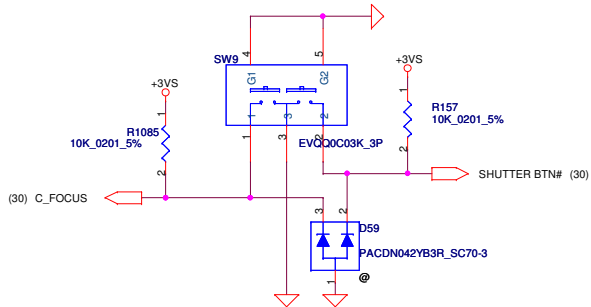
PWR SWITCH



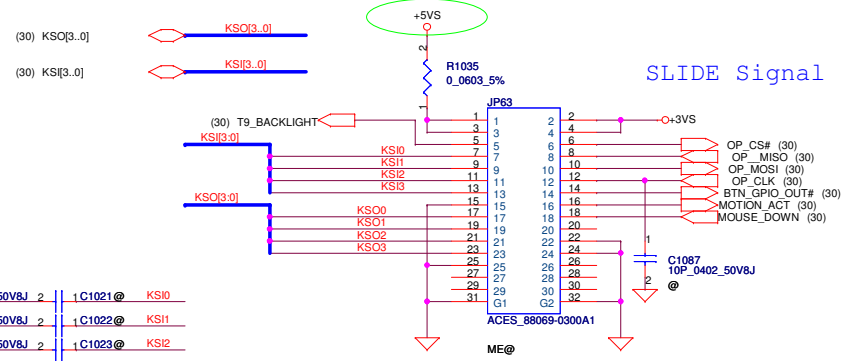
VOLUME ON/OFF



SHUTTER BUT

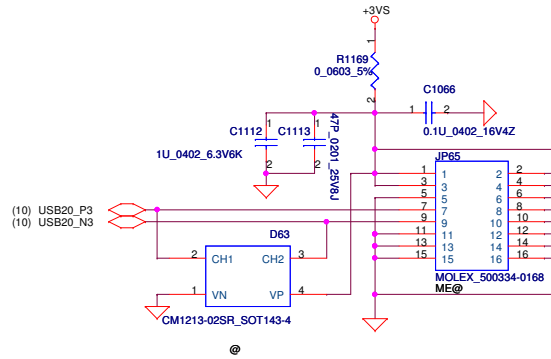


T9 Conn

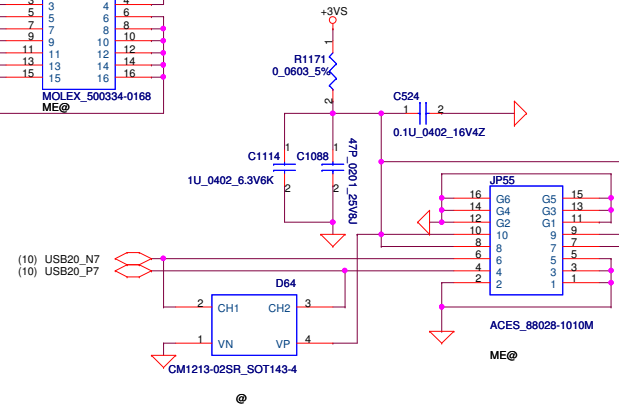


| | | | | |
|-----------------|---|---|--------|------|
| 100P_0402_50V8J | 2 | 1 | C1021@ | KSI0 |
| 100P_0402_50V8J | 2 | 1 | C1022@ | KSI1 |
| 100P_0402_50V8J | 2 | 1 | C1023@ | KSI2 |
| 100P_0402_50V8J | 2 | 1 | C1024@ | KSI3 |
| 100P_0402_50V8J | 2 | 1 | C1025@ | KSO0 |
| 100P_0402_50V8J | 2 | 1 | C1026@ | KSO1 |
| 100P_0402_50V8J | 2 | 1 | C1027@ | KSO2 |
| 100P_0402_50V8J | 2 | 1 | C1028@ | KSO3 |

0.3M Camera Conn



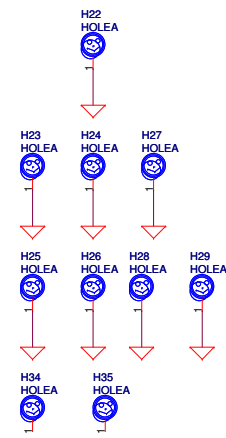
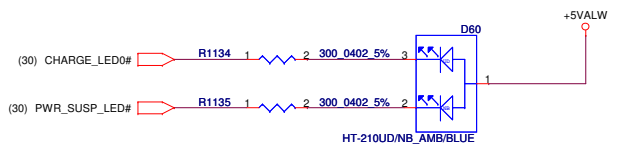
2.0M Camera Conn



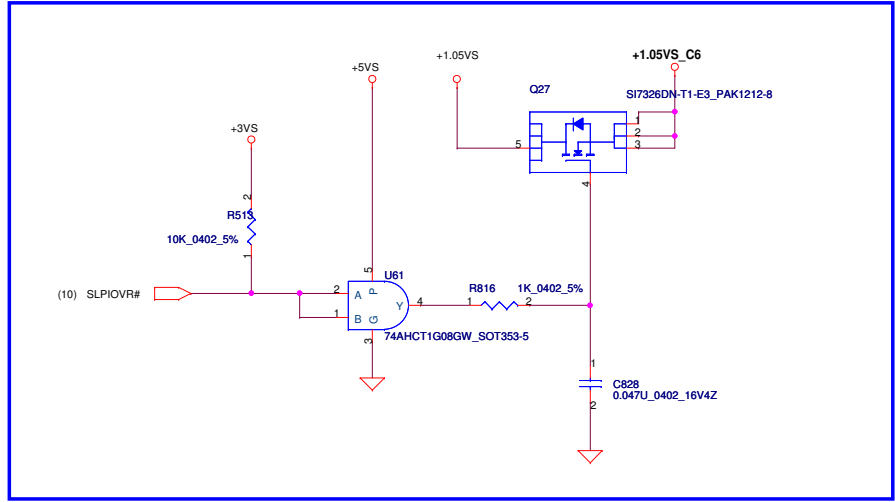
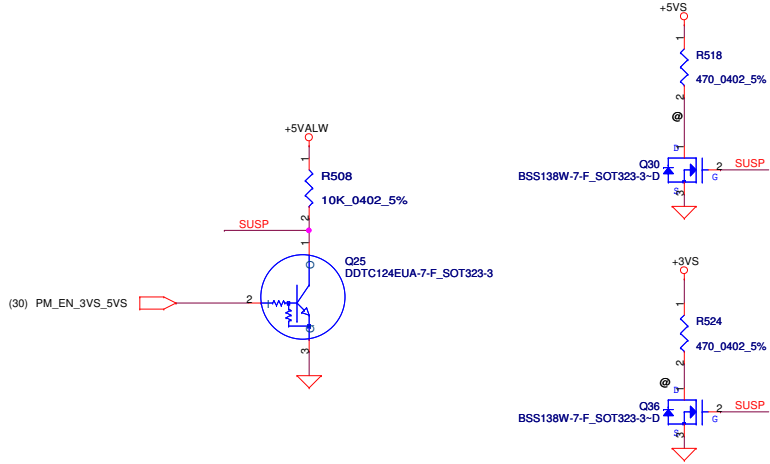
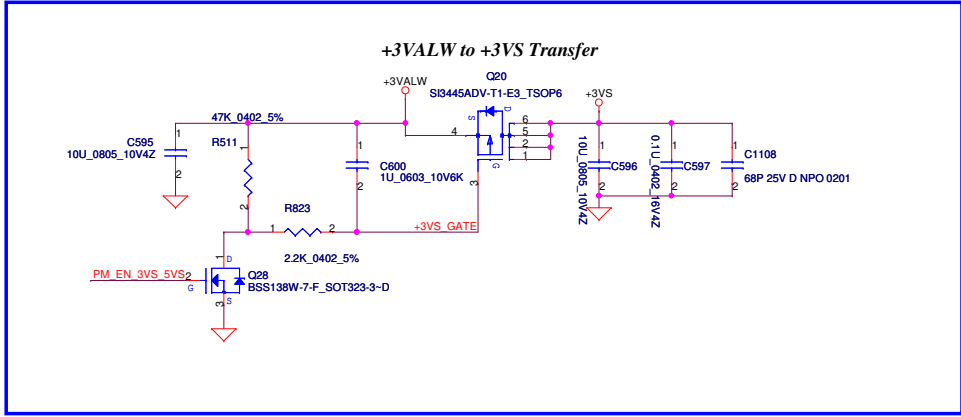
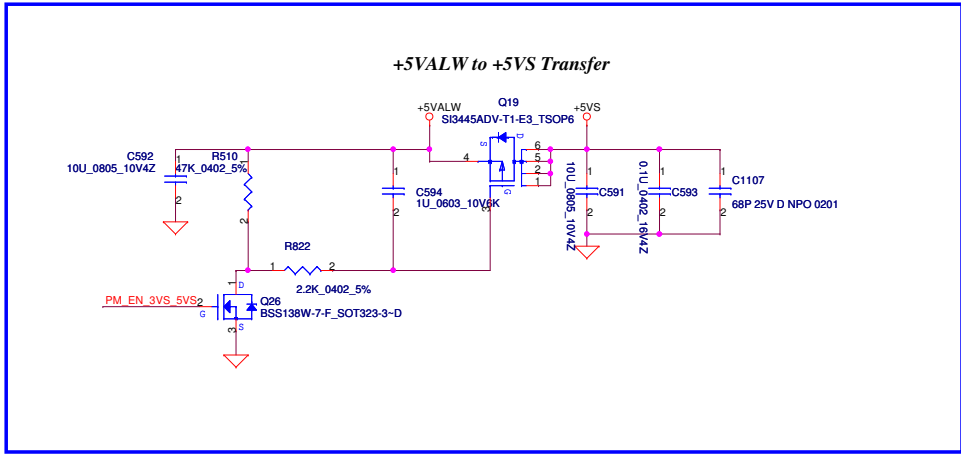
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| | | | | Date: | Monday, April 28, 2006 |
| | | | | Sheet | 33 of 43 |
| | | | | Rev | 0.2 |

Compal Electronics, Inc.

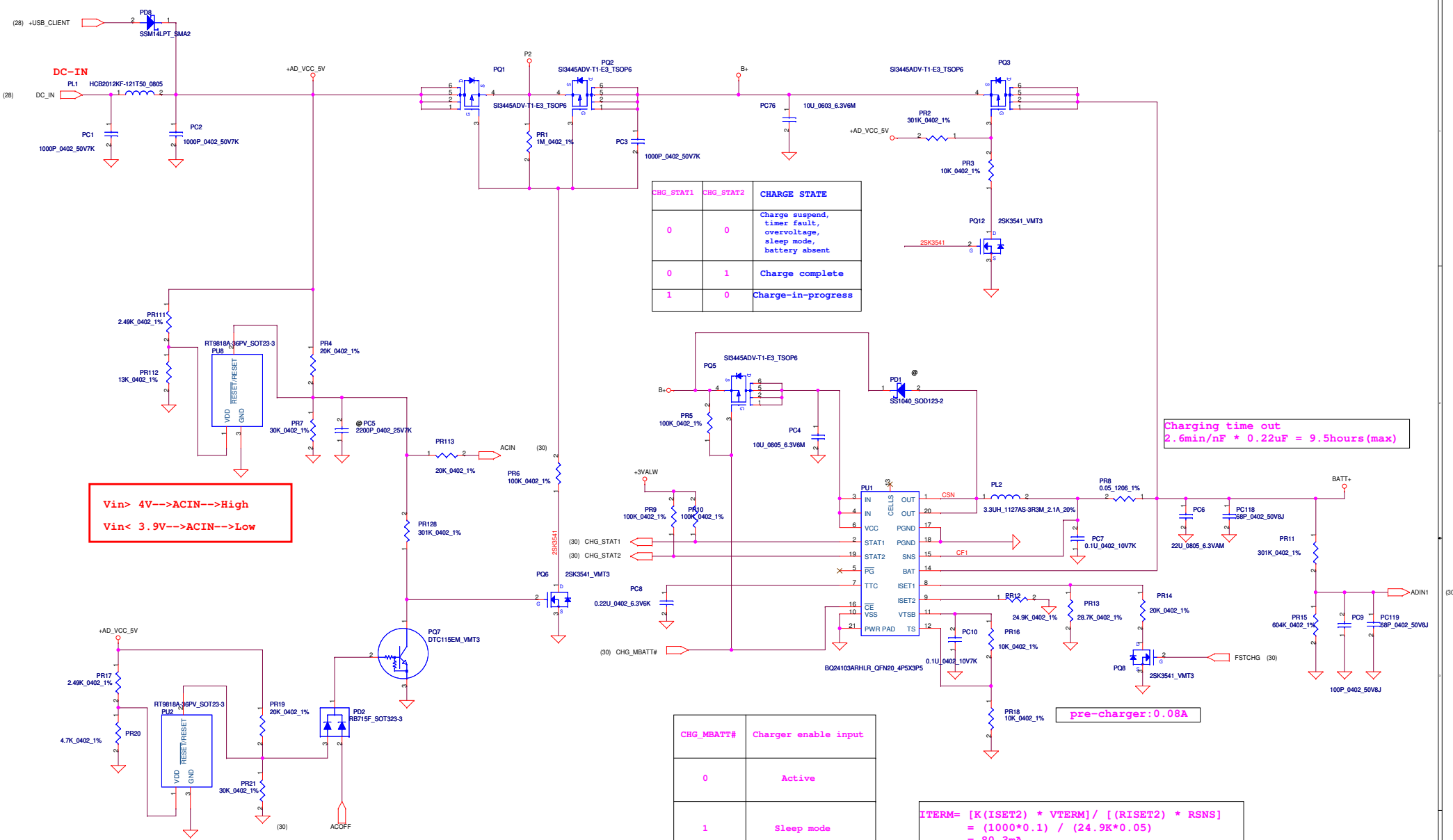
Front LEDs



| | | | | | |
|--|--------------------|-----------------|------------|------------------------------|----------------|
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| Issued Date | 2006/08/04 | Deciphered Date | 2006/10/06 | INDICATE LED | |
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| | | | | Date: Monday, April 28, 2006 | Sheet 34 of 43 |



| | | | | |
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| Issued Date | 2006/08/04 | Deciphered Date | | |
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| Size | Document Number | Rev | | 0.2 |
| Custom | JAX10 | Date: | | Monday, April 28, 2008 |
| Date: | | | Monday, April 28, 2008 | Sheet 35 of 43 |



Vin > 4V --> ACIN --> High
 Vin < 3.9V --> ACIN --> Low

Adapter OVP setting
 Vin > 5.5V --> ACIN --> Low
 Vin < 5.45V --> ACIN --> High

| CHG_STAT1 | CHG_STAT2 | CHARGE STATE |
|-----------|-----------|--|
| 0 | 0 | Charge suspend, timer fault, overvoltage, sleep mode, battery absent |
| 0 | 1 | Charge complete |
| 1 | 0 | Charge-in-progress |

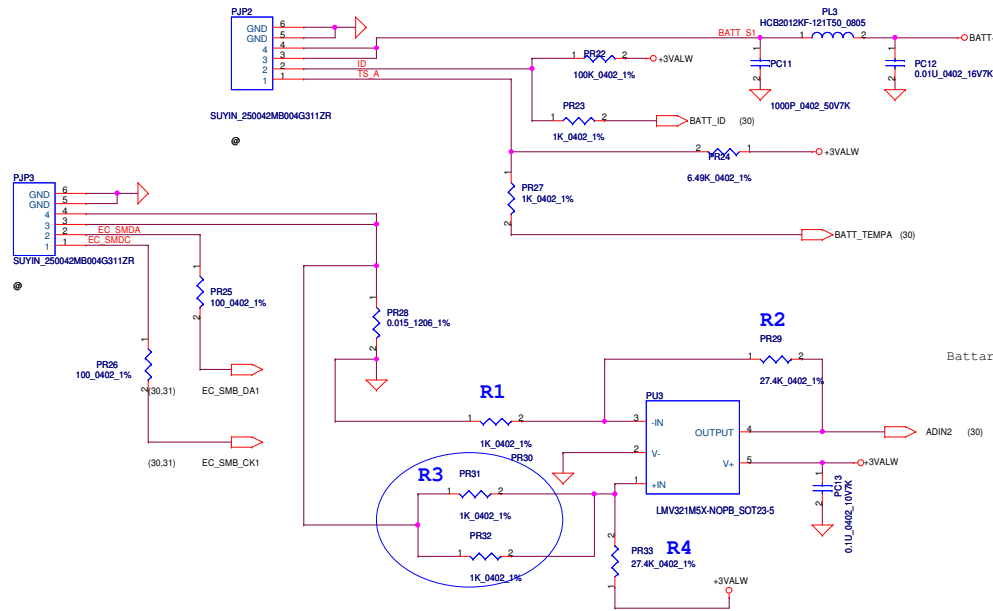
| CHG_MBATT# | Charger enable input |
|------------|----------------------|
| 0 | Active |
| 1 | Sleep mode |

$$I_{TERM} = \frac{K(I_{SET2}) * V_{TERM}}{[(R_{ISET2}) * R_{SNS}]} = \frac{(1000 * 0.1)}{(24.9K * 0.05)} = 80.3mA$$

Charging time out
 $2.6min/nF * 0.22uF = 9.5hours(max)$

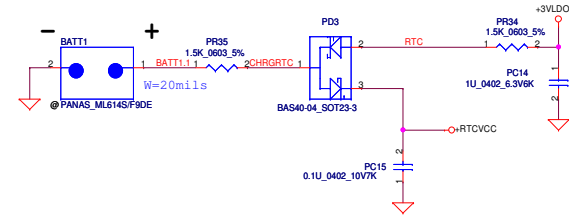
pre-charger: 0.08A

| FSTCHG | Charge Current |
|--------|--|
| 0 | 0.7A (System ON / USB IN but SYS OFF) |
| 1 | 1.7A (System Off) |

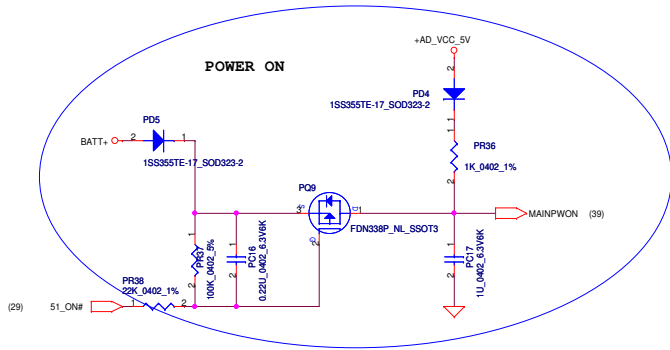
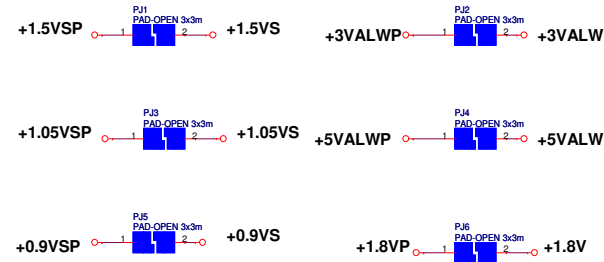
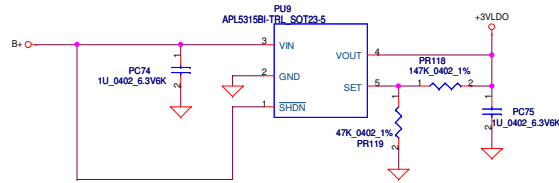


| For Discharging | | For charging | |
|---------------------|-----------|---------------------|-----------|
| Battery current (A) | ADIN2 (V) | Battery current (A) | ADIN2 (V) |
| 0A | 1.65V | 0A | 1.65V |
| 0.5A | 1.44V | 0.25A | 1.75V |
| 1A | 1.24V | 0.5A | 1.85V |
| 1.5A | 1.03V | 0.8A | 1.98V |
| 2A | 0.83V | 1A | 2.06V |
| 2.5A | 0.62V | 1.25A | 2.16V |
| 3A | 0.42V | 1.5A | 2.27V |
| 3.5A | 0.21V | 1.75A | 2.37V |
| 4A | 0.00V | 2A | 2.47V |

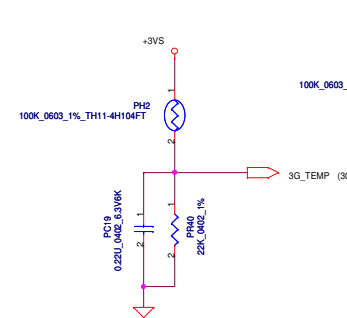
If $R1=R3$, $R2=R4$
 $V_o = (R2/R1) (V_2 - V_1) + (V_1/2)$



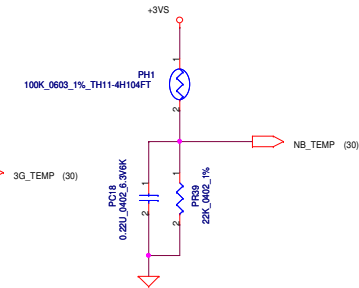
RTC BATTERY



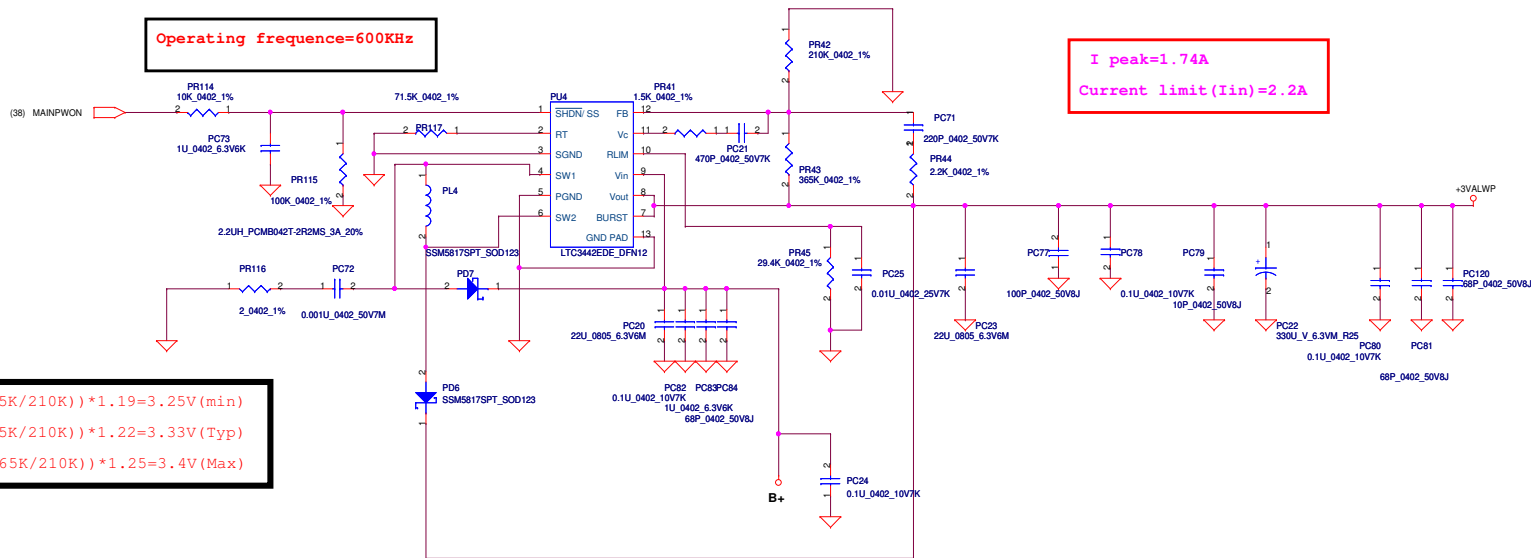
PH2 near 3G



PH1 under NB



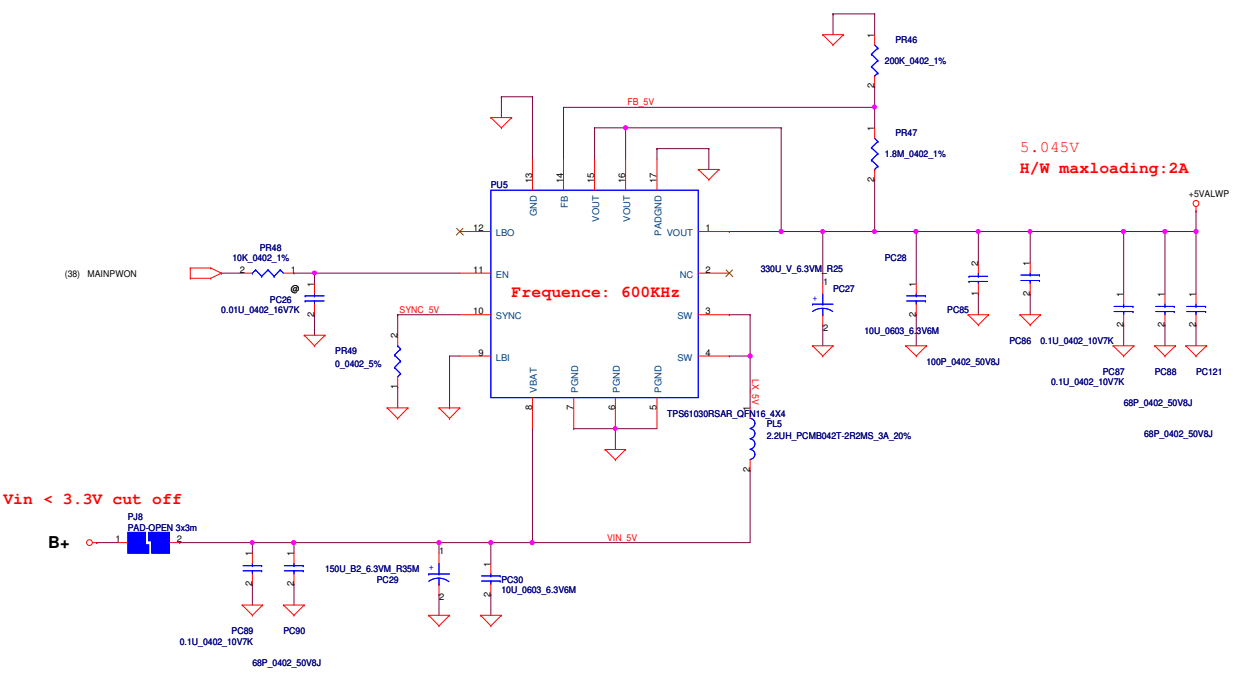
| | | | | |
|---|------------------------|-----------------|--------------------------|---|
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Operating frequency=600KHz

I peak=1.74A
Current limit (Iin)=2.2A

$(1 + (365K/210K)) * 1.19 = 3.25V (min)$
 $(1 + (365K/210K)) * 1.22 = 3.33V (Typ)$
 $(1 + (365K/210K)) * 1.25 = 3.4V (Max)$

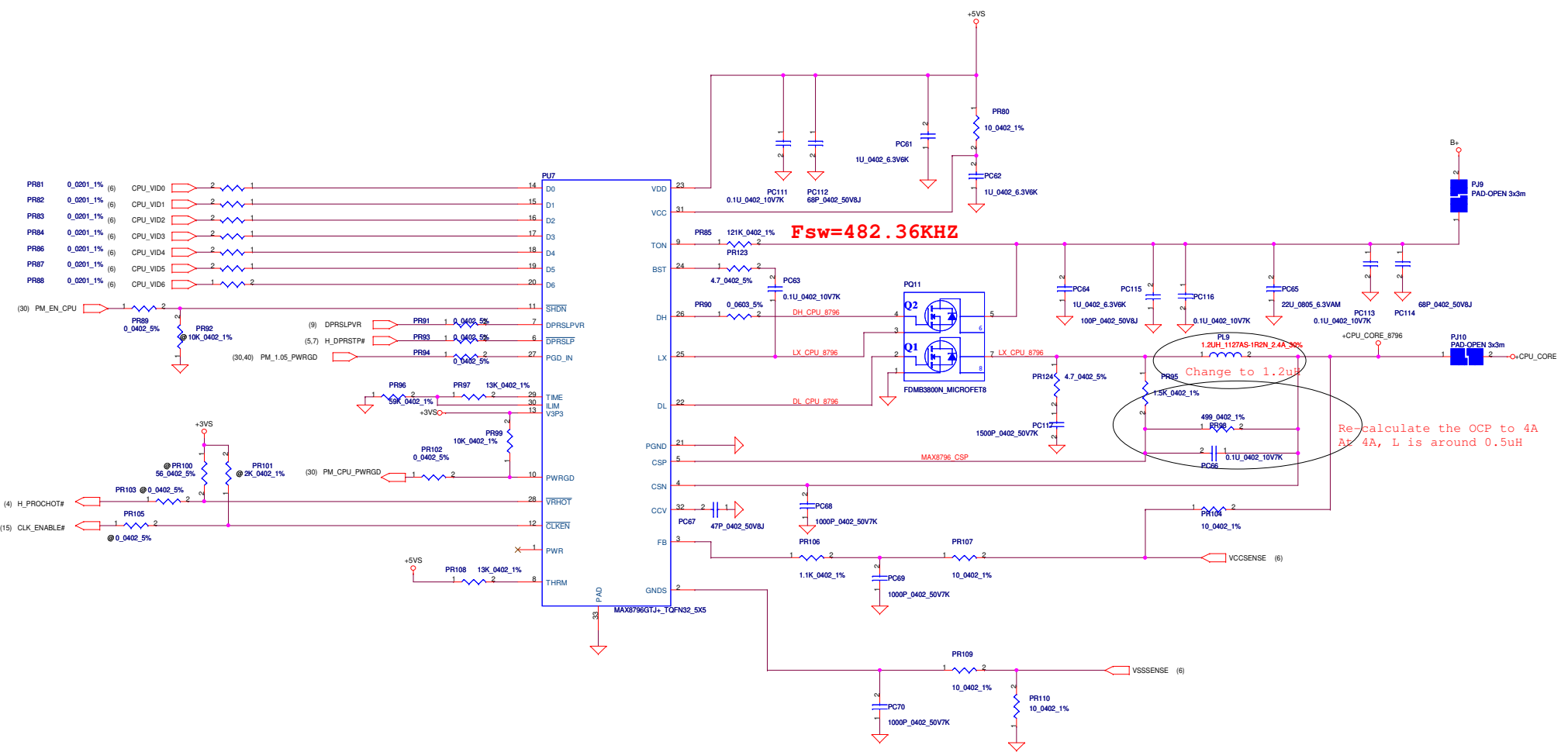


5.045V
H/W maxloading:2A

Frequency: 600KHz

Vin < 3.3V cut off

| | | | | |
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- PR81 0_0201_1% (6) CPU_VID0 2 1
- PR82 0_0201_1% (6) CPU_VID1 2 1
- PR83 0_0201_1% (6) CPU_VID2 2 1
- PR84 0_0201_1% (6) CPU_VID3 2 1
- PR86 0_0201_1% (6) CPU_VID4 2 1
- PR87 0_0201_1% (6) CPU_VID5 2 1
- PR88 0_0201_1% (6) CPU_VID6 1 2
- (30) PM_EN_CPU 1 2
- (9) DPRSLPVR 1 0.0402_5%
- (5,7) H_DPRSTP# 1 0.0402_5%
- (30,40) PM_1_05_PWRGD 1 0.0402_5%
- (30) PM_CPU_PWRGD 1 2
- (4) H_PROCHOT# 1 2
- (15) CLK_ENABLE# 1 2

| | | | | | |
|---|------------------------|--------------------|------------|--------------------------|-----------------------|
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DVT

1. RF noise solution

- (1) PU4 於PC22, PC23並聯PC79 (10PF濾波電容), 可改善2100MHz noise flow.
- (2) PU7 於PR90, 改為1.2ohm, 可改善5-15db noise flow.
- (3) 增加Snubber filter solution in PL6, PL7, PL8, PL9 (R=4.7ohm, c=1500pf)
PR120/PC100 in PL6 PR121/PC103 in PL7 PR122/PC108 in PL8 PR124/PC117 in PL9
- (4) 增加 .1uF and 100pf to PC23, PC28, PC64, PC32, and PC33
PC77/PC78 to PC23 PC87/PC85 to PC28 PC116/PC115 to PC64 PC94/PC93 to PC32 PC97/PC96 to PC33
- (5) B+ line inputs增加 10uF or 68uF --->PC76
- (6) Add PC82/PC83/PC84 to PC20
- (7) Add PC80/PC81 to PC23
- (8) Add PC89/PC90 to PC29
- (9) Add PC87/PC88 to PC28
- (10) Add PC91/PC92 to PC32
- (11) Add PC109/PC110 to PC59
- (12) Add PC106/PC107 to PC52
- (13) Add PC104/PC105 to PC48
- (14) Add PC101/PC102 to PC45
- (15) Add PC98/PC99 to PC37
- (16) Add PC113/PC114 to PC65
- (17) Add PC111/PC112 to PC61
- (18) Add PC95 to PC33

2. Solar bag circuit

Add PD8 to solar bag circuit.

PVT

1. Add PR128 to prevent ACIN to pull low in abnormal function
2. 不接ACOFF, PQ12.2連接到PQ6.1, 做開關動作
3. Charger 4.4UH change to 3.3UH for OCP concern
4. PC118/PC119/PC120/PC121 are used for RF noise

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EVT -----> DVT

PAGE04 R562 from 56 ohm change to 120 ohm & pull up +1.05VS_C6
PAGE07 R300 from 56 ohm change to 120 ohm
R32 from 0 ohm change to 24 ohm
PAGE09 Add R1151 0 ohm pull down
PAGE10 Add R1152 1K ohm pull down
R1153 10K ohm pull up +3VS
PAGE16 Del R321 0 ohm
PAGE17 Q68 change to AO3415(P/N:SB00000AP00)
PAGE18 Add R1161 0 ohm
PAGE19 C1056,C1058&C1059 from 10pF change to 56pF
RF solution add C1100 C1101
PAGE20 Add GPS_OFF# circuit
RF solution add L79 C1097 C1098 C1099
C1065 1.2pF change to 1.8pF
PAGE22 Add R1154 100K ohm pull down
PAGE25 Add R1155 0 ohm & MWP_PD# ,SWP_PD# net
PAGE27 R1029,R1034 change to 15.4K ohm
Add EC_-3V_PWD# net
Del EC_MIC_SENSE & EC_JACK_SENSE net
Change JP62 Connector & Reserve Speaker Amp circuit of WOLFSON
PAGE28 Add solar bag funtion(R1183 connect to EC)
PAGE30 Add R1167(LPC_AD0)
R1166(LPC_AD1)
R1165(LPC_AD2)
R1164(LPC_AD3) 20K ohm pull up +3VS
R1160 10K ohm pull up +3VS
RF solution add C1102 C1103
add USB_DETECT net
PAGE33 Reserve R1169 & R1171 pull up to +3VS
R1035 pull up from +5VALW change to +5VS
PAGE34 Del AN1,R1060,R1062,R1064&POGOPAD1,2
Change Size to 0201
PAGE27 R1139 R1004 R1006 R1007 C965
PAGE28 R1010 R1016 R1019 R1021 R1046 R1047 R1032
PAGE30 R442 R465 R467 R468 R800 R796 R798 R797
R454 R455 R457 R458 R1131 R1132 R1087 R1086
R480 R1051 R1052 R447 R801 R1160
C1004 C1005 C1007 C1008 C1096 C830 C1018
C1019 C1020
PAGE31 C1017 C1085 C1086 R1079

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