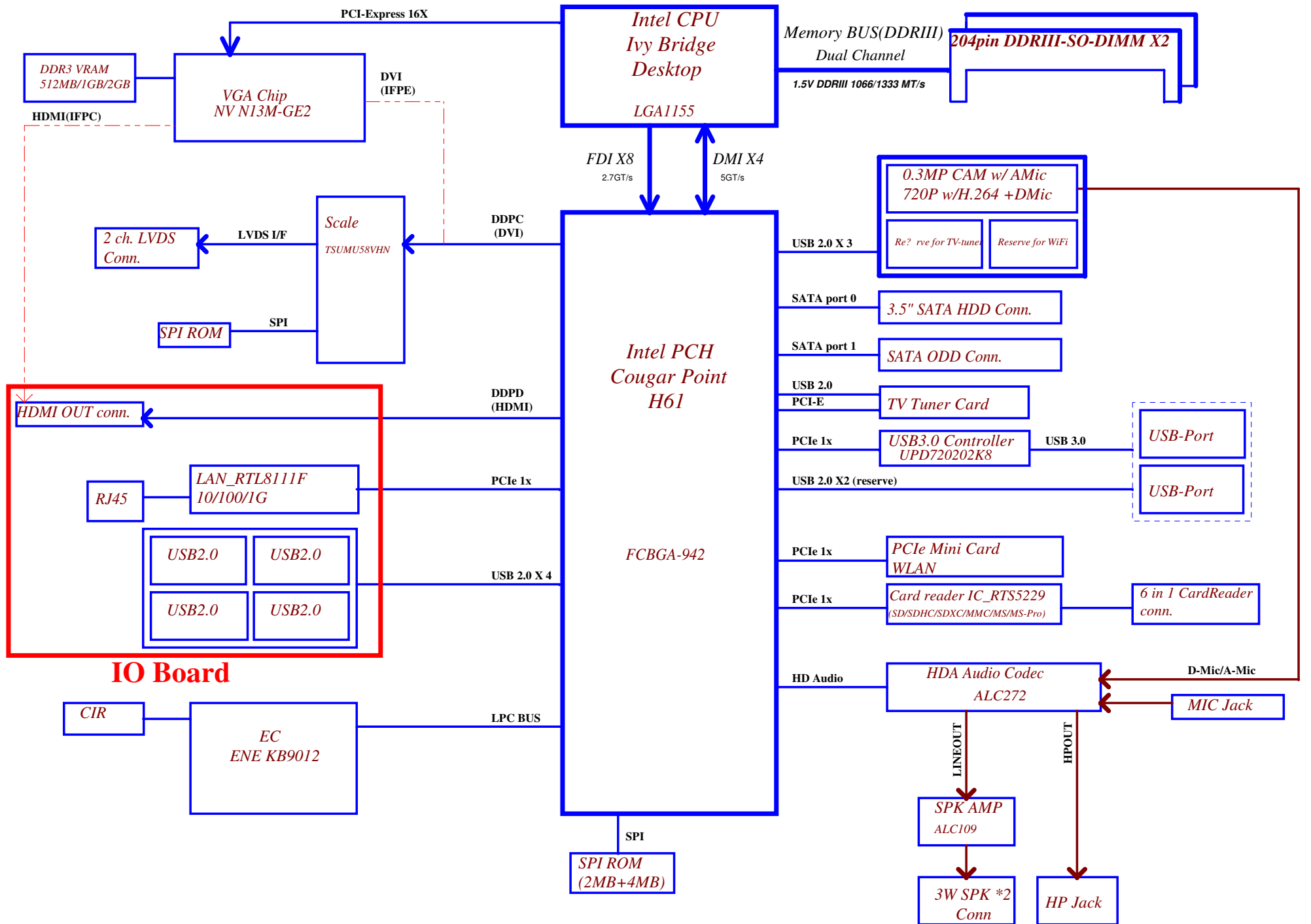


VBA00

LA-9301P REV 1.0 Schematic

Intel Processor(Ivy Bridge) / PCH(Cougar Point)
Friday, September 21, 2012 Rev 1.0

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USB Port Table			
USB 2.0	USB 1.1	Port	Device
RMH1	UHCI0	0	Rear IO USB20 Conn
		1	Rear IO USB20 Conn
		2	Co-lay w/USB30 PORT0
	UHCI1	3	Co-lay w/USB30 PORT1
		4	Web Camera
	UHCI2	5	NC
		6	Disabled on H61
RMH2	UHCI3	7	Disabled on H61
		8	Mini Card(TV Tuner)
		9	Mini Card(WiFi)
	UHCI4	10	Rear IO USB20 Conn
		11	Rear IO USB20 Conn
	UHCI5	12	Disabled on H61
		13	Disabled on H61

BOM Structure Table	
BTO Item	BOM Structure
ME components	CONN@
UMA Only	UMA@
DISCRETE ONLY	DIS@
USB30	USB30@
No USB30 SKU	USB20@
HDMI OUT from DIS	HDMIOD@
HDMI OUT from UMA	HDMI0U@
HDMI OUT	HDMI0@
Unpop	@
VRAM select	X76@
VRAM 4pcs	VRAM4@
VRAM 4pcs	VRAM8@
PCB	PCB@
VRAM 512M Samsung	S512M@
VRAM 512M Hynix	H512M@
VRAM 1G Samsung	S1G@
VRAM 1G Hynix	H1G@
VRAM 2G Samsung	S2G@
VRAM 2G Hynix	H2G@
SKU IO Select	GPIO69_H@
	GPIO69_L@
	GPIO70_H@
	GPIO70_L@
	GPIO71_H@
	GPIO71_L@

SATA Port Table		
Port	Device	
6G	0	ODD
	1	HDD
3G	2	Disabled on H61
	3	Disabled on H61
	4	NC
	5	NC

PCIe Port Table	
Port	Device
1	NC
2	USB30
3	WLAN
4	TV
5	Card reader
6	LAN
7	Disabled on H61
8	Disabled on H61

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	
2	
3	

SKU ID(Project) Table				
Project ID2 (GPIO69)	Project ID1 (GPIO70)	Project ID0 (GPIO71)	SKU	
0	0	0	UMA-USB30 4319KA38L01 4319KA38L02	UMA@ USB30@ HDMI0U@ GPIO69_L@ GPIO70_L@ GPIO71_L@ PCB@
0	0	1	UMA-USB20 4319KA38L03 4319KA38L04	UMA@ USB20@ HDMI0U@ GPIO69_L@ GPIO70_L@ GPIO71_H@ PCB@
0	1	0	DIS-512M USB30 4319KA38L05	DIS@ USB30@ HDMIOD@ GPIO69_L@ GPIO70_H@ GPIO71_L@ PCB@
0	1	1	DIS-512M USB20 4319KA38L06	DIS@ USB20@ HDMIOD@ GPIO69_L@ GPIO70_H@ GPIO71_H@ PCB@
1	0	0	DIS-1G USB30 4319KA38L07	DIS@ USB30@ HDMIOD@ GPIO69_H@ GPIO70_L@ GPIO71_L@ PCB@
1	0	1	DIS-1G USB20 4319KA38L08	DIS@ USB20@ HDMIOD@ GPIO69_H@ GPIO70_L@ GPIO71_H@ PCB@
1	1	0	DIS-2G USB30 4319KA38L09	DIS@ USB30@ HDMIOD@ GPIO69_H@ GPIO70_H@ GPIO71_L@ PCB@
1	1	1	DIS-2G USB20 4319KA38L10	DIS@ USB20@ HDMIOD@ GPIO69_H@ GPIO70_H@ GPIO71_H@ PCB@

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						Notes List				
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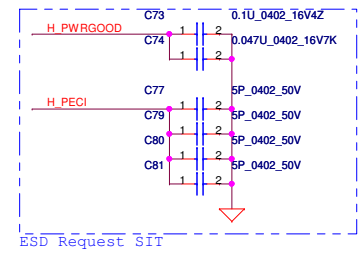
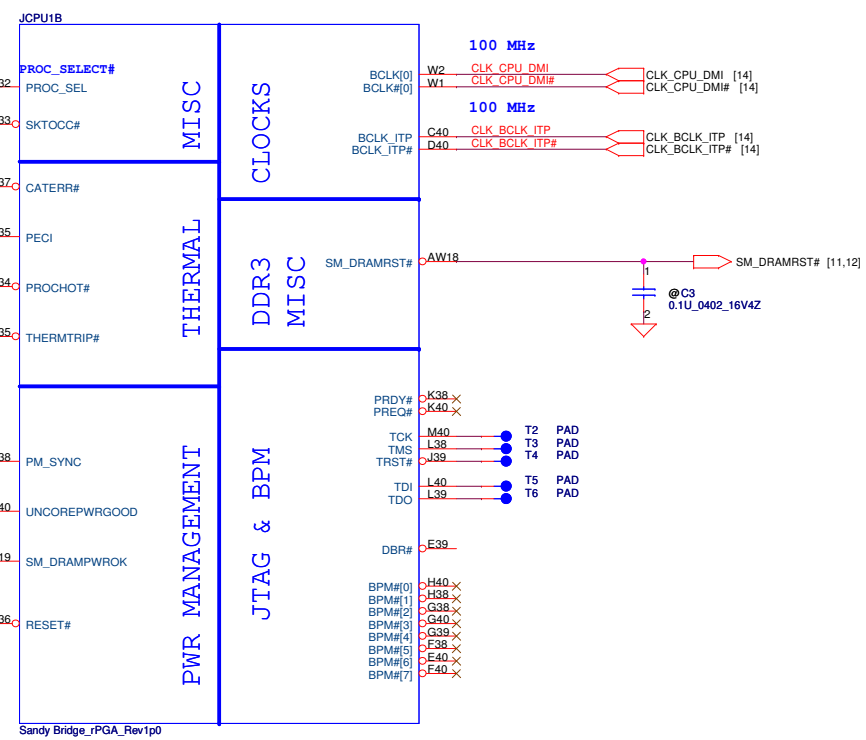
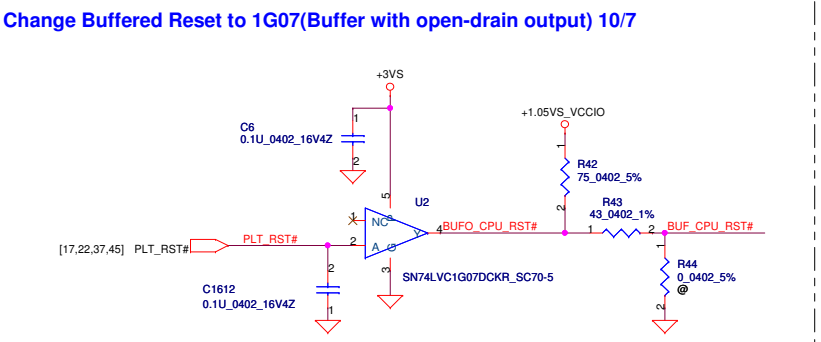
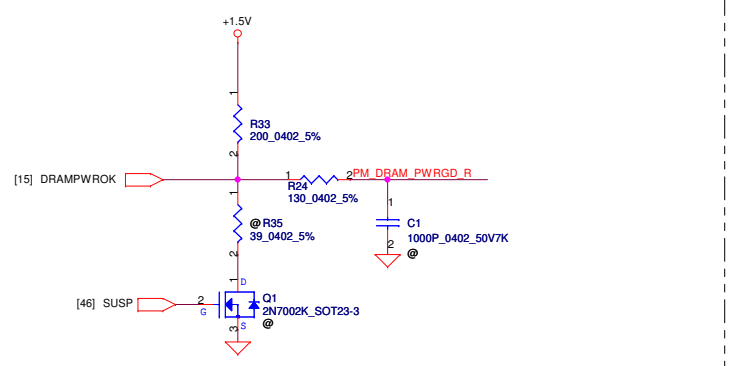
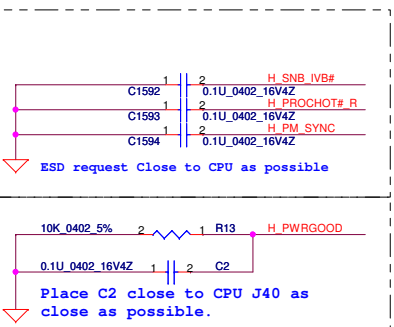
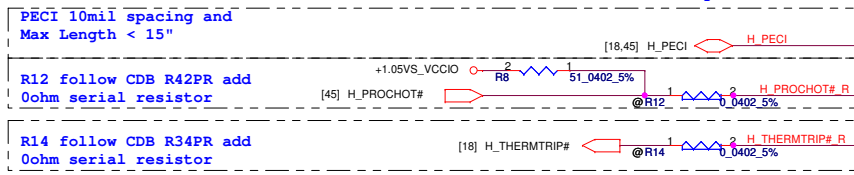
PCH SM Bus Address			
Power	Device	HEX	Address
+3VS	DDR(JDDR2)		1010 000X b
+3VS	DDR(JDDRH1)		1010 010X b

EC SM Bus1 Address			
Power	Device	HEX	Address
	ALC106	48H	0100_100xb

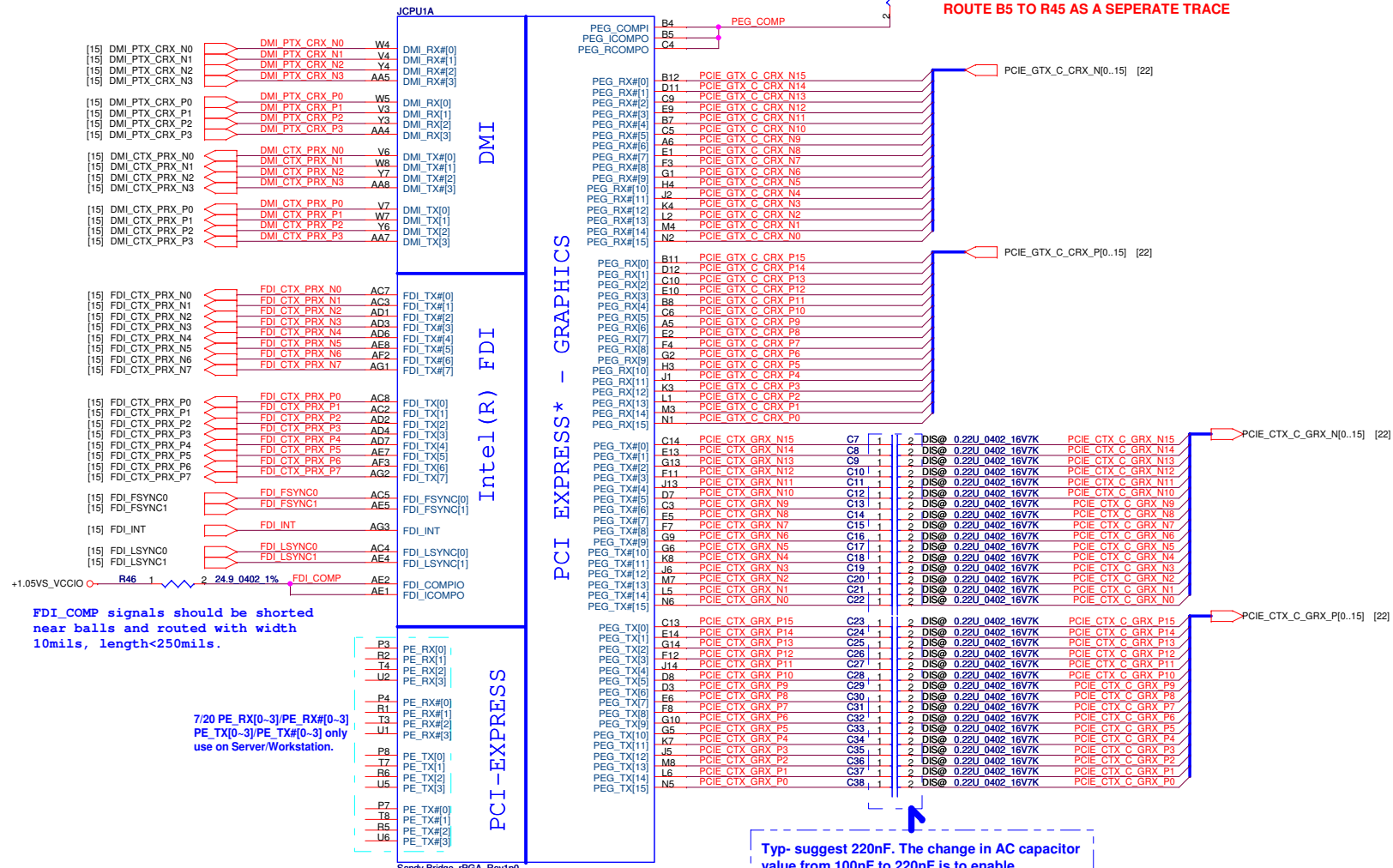
Board ID	Rb	V _{min}	V _{typ}	V _{max}	EC AD3
0	0	0 V	0 V	0.155 V	0x00 - 0x0C
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31 - 0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A - 0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A - 0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F - 0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC - 0xFF

PCH SML1 Bus Address			
Power	Device	HEX	Address
	VGA Ext. thermal sensor		1001_1010b
	VGA Int. thermal sensor (defaulta)		1001_1110b

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VS
Full ON		HIGH	HIGH	HIGH	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF



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PEG_ICOMPI and RCOMPO signals should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 m ohm (4 mils/15mils)
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 m ohm (12 mils/15mils)

SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLETRACE TO R45
ROUTE B5 TO R45 AS A SEPERATE TRACE

+CPU_CORE

POWER

JCPU1F

76A (Quad Core 65W)

8.5A

PEG AND DDR

SVID

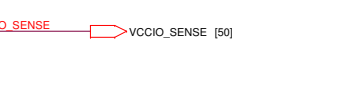
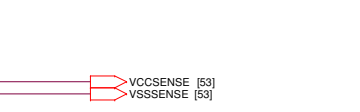
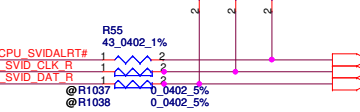
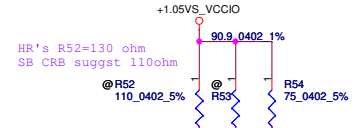
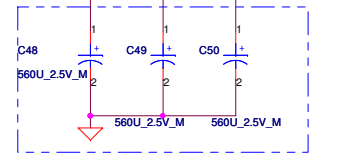
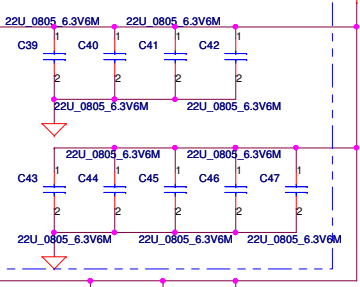
SENSE LINES

VSS_SENSE_VCCIO

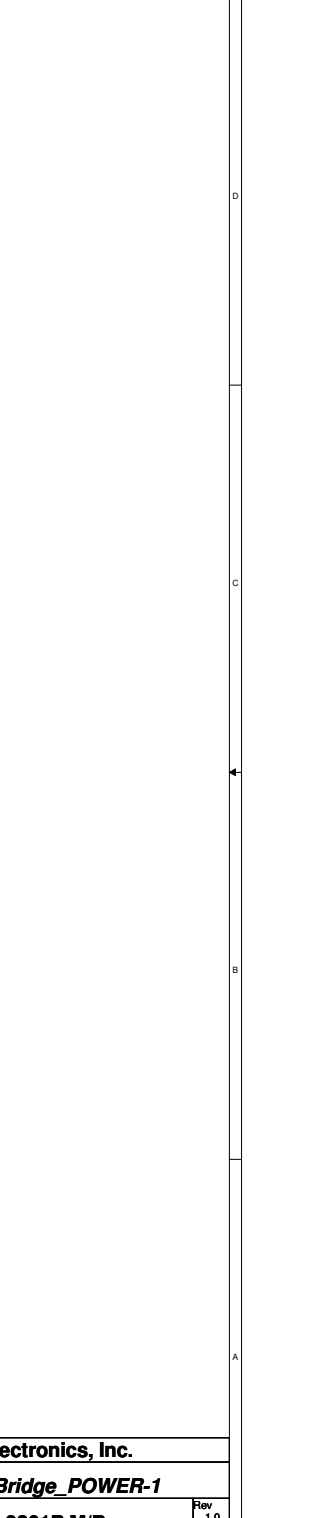
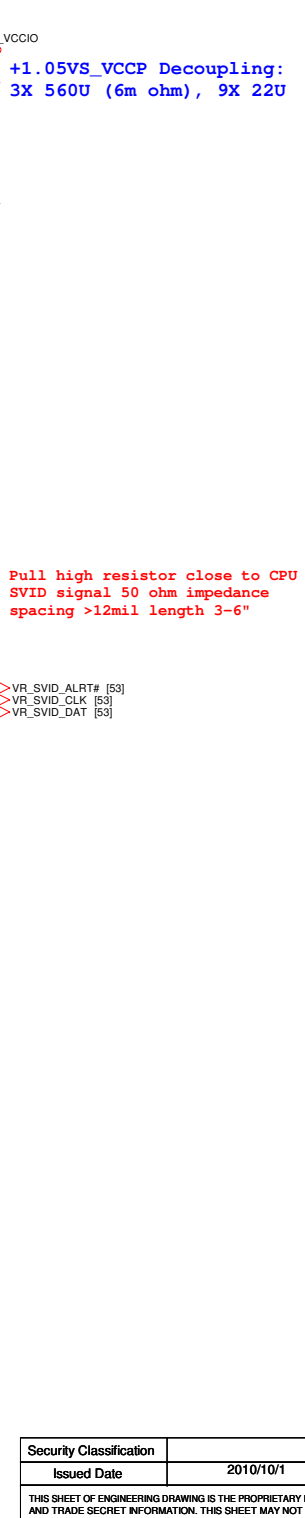
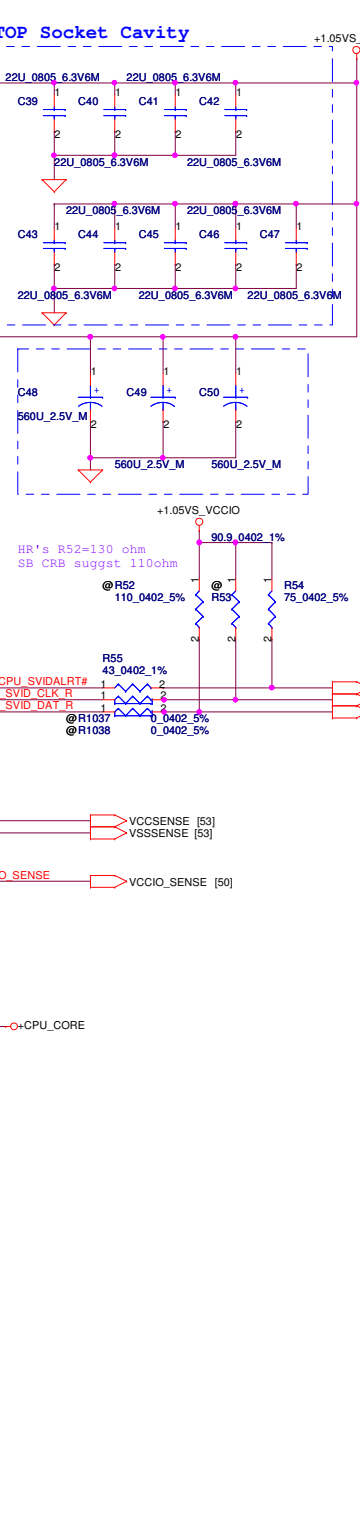
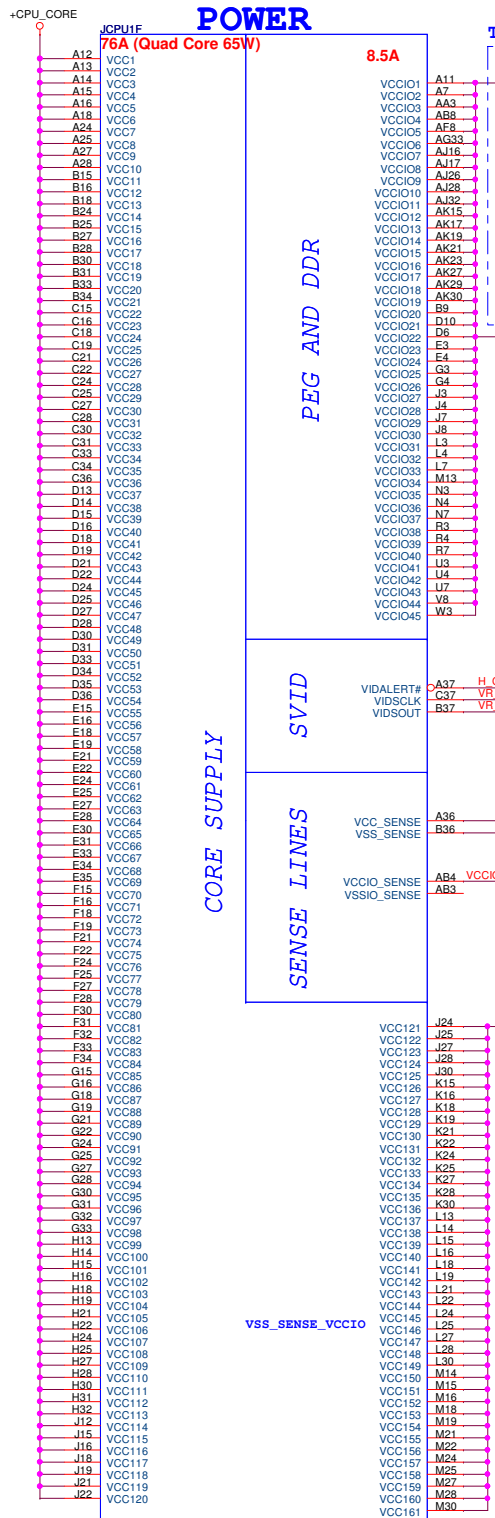
TOP Socket Cavity

+1.05VS_VCCIO

+1.05VS_VCCP Decoupling:
3X 560U (6m ohm), 9X 22U

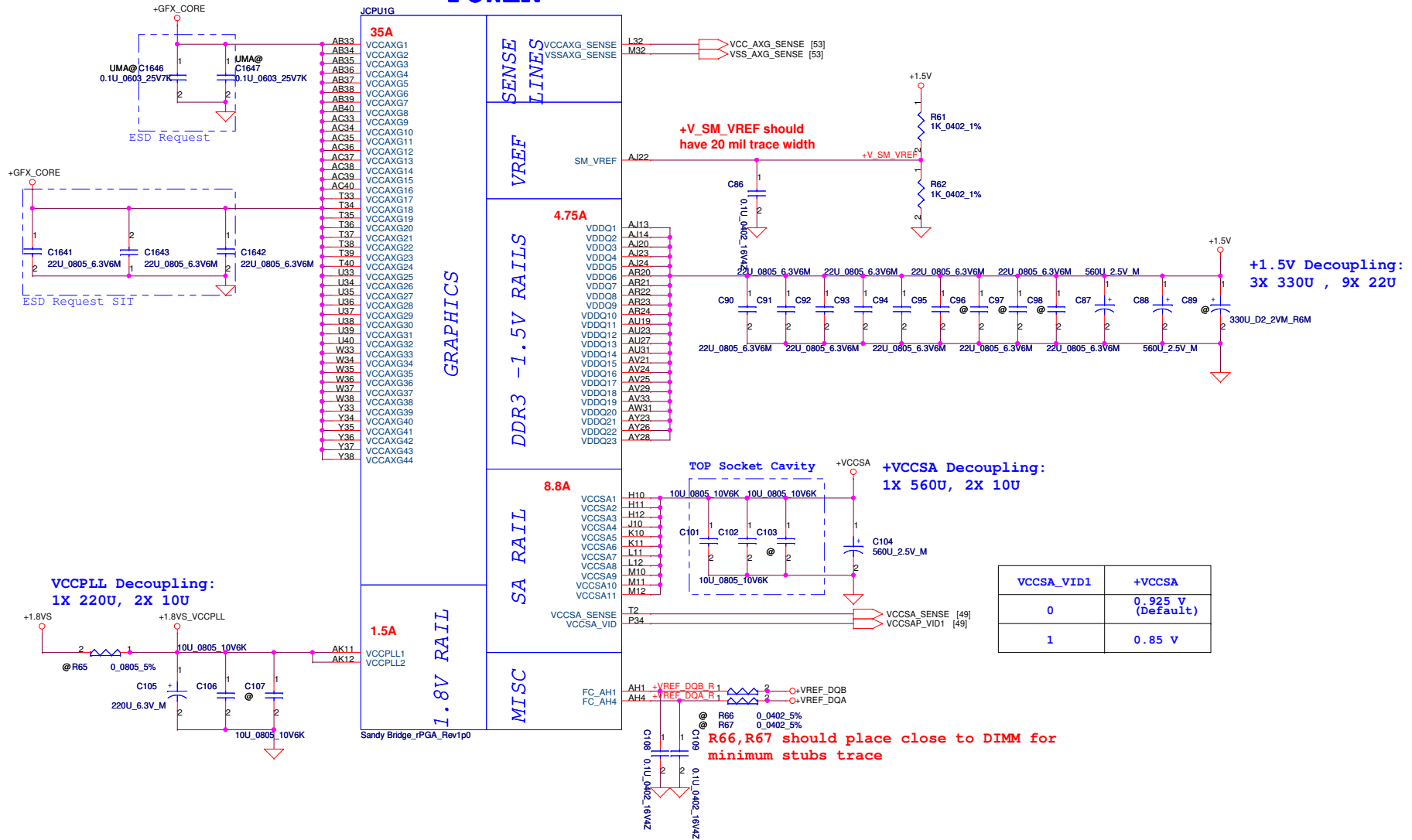


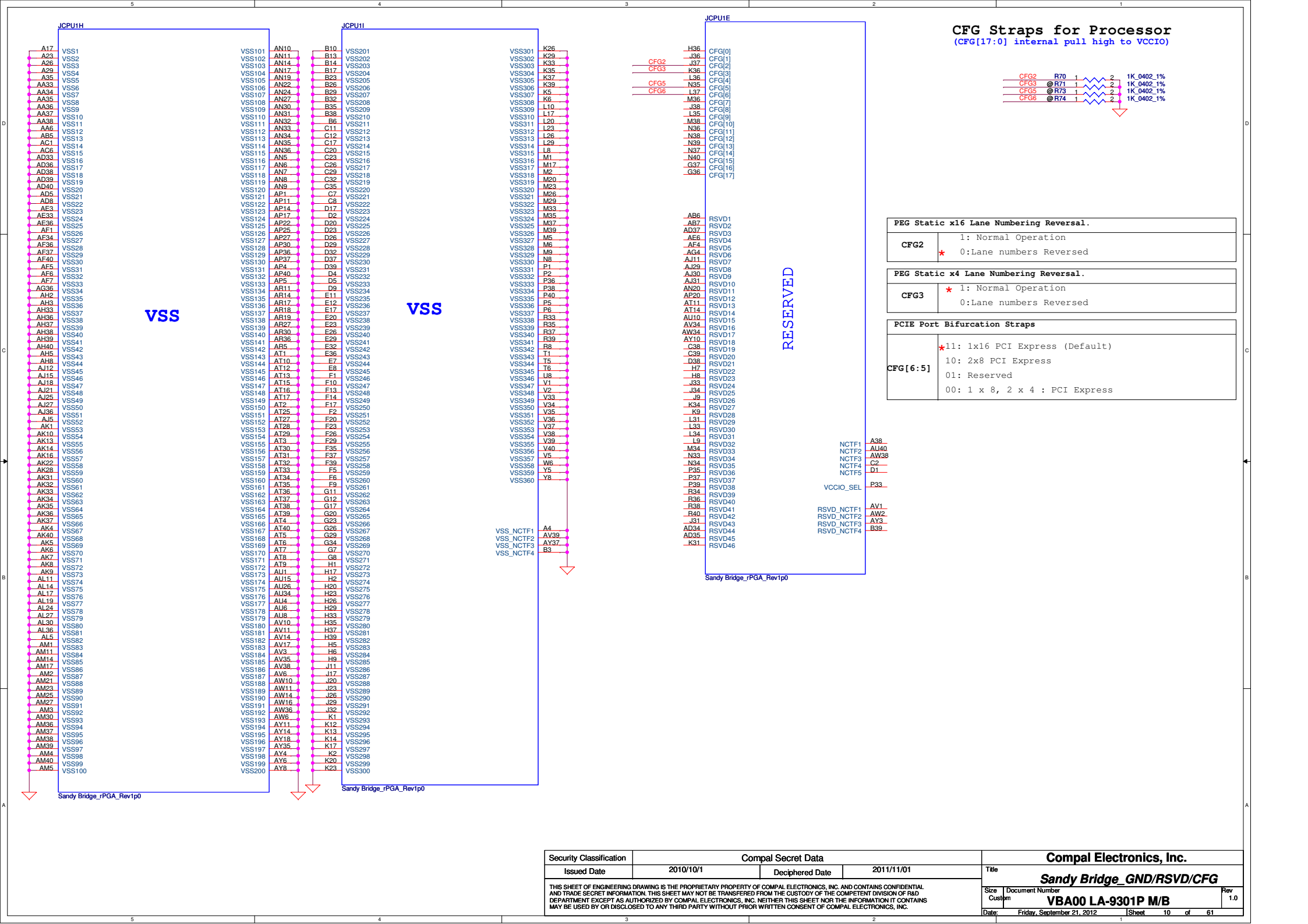
Pull high resistor close to CPU
SVID signal 50 ohm impedance
spacing >12mil length 3-6"



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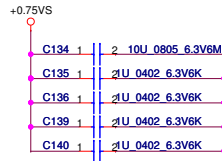
POWER





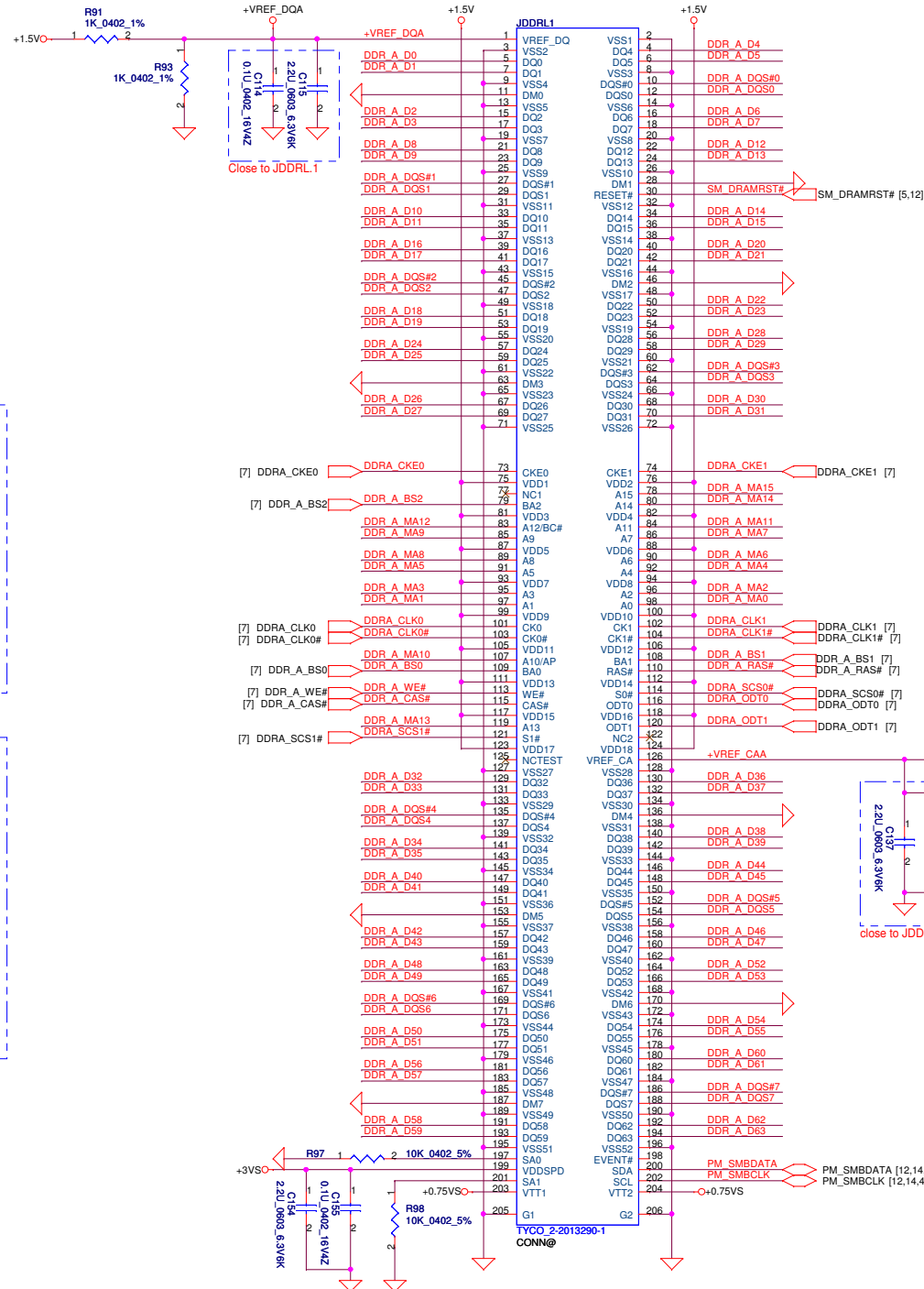
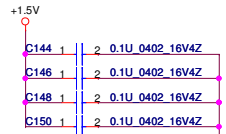
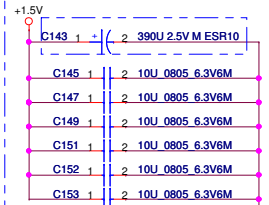
- [7] DDR_A_DQS[0..7]
- [7] DDR_A_DS# [0..7]
- [7] DDR_A_D[0..63]
- [7] DDR_A_MA[0..15]

Layout Note:
Place near JDDR1.203 and 204

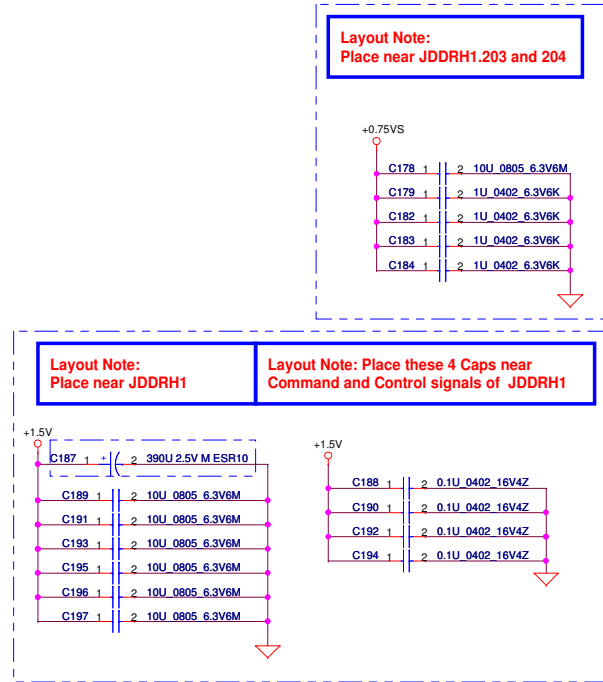


Layout Note:
Place near JDDR1

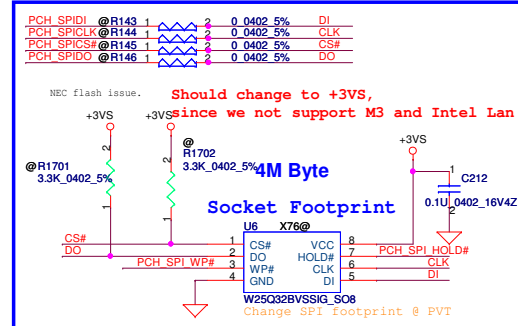
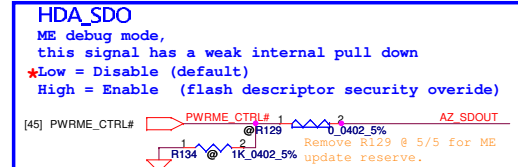
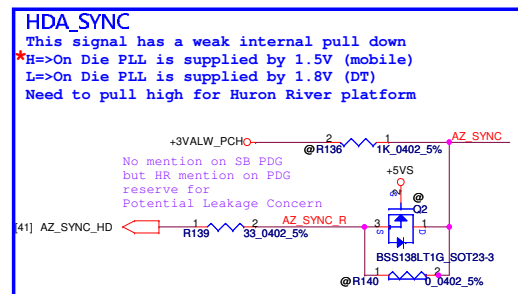
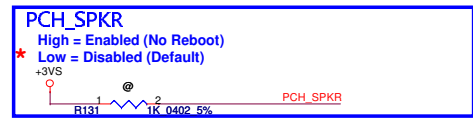
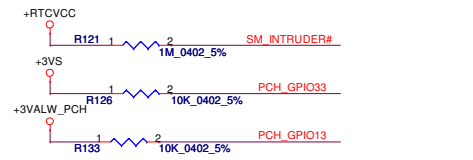
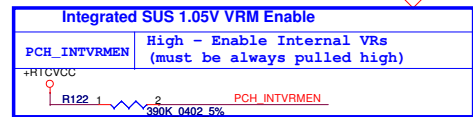
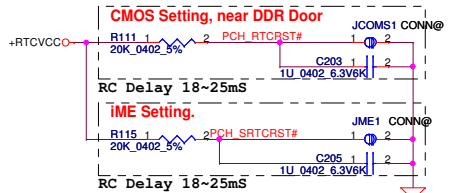
Layout Note: Place these 4 Caps near Command and Control signals of JDDR1



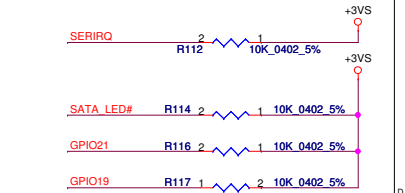
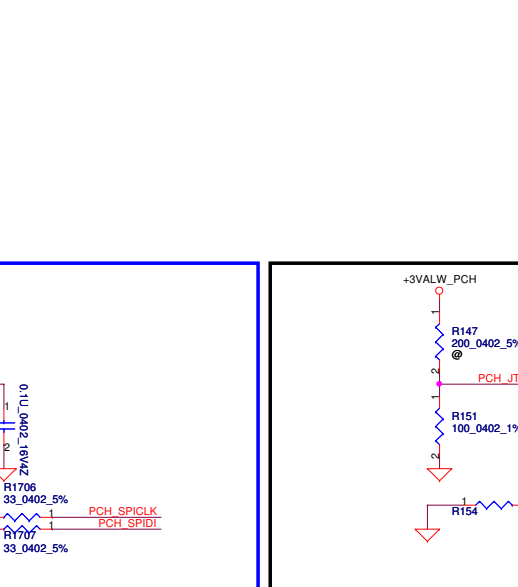
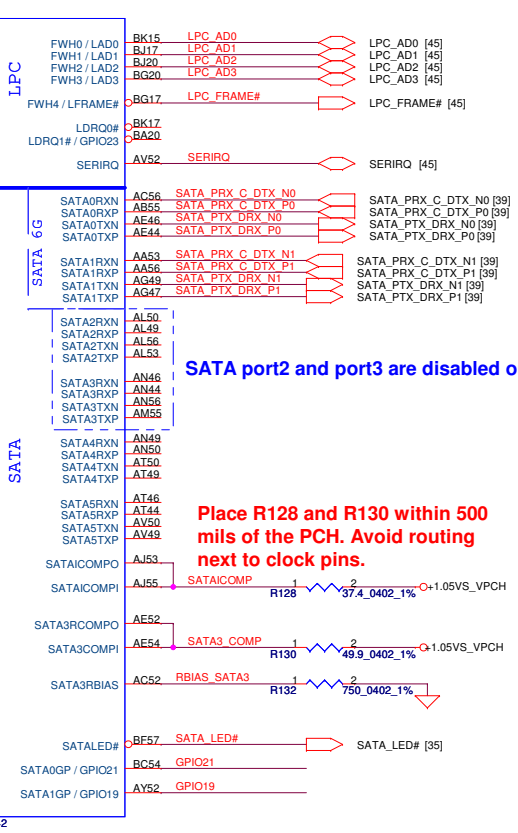
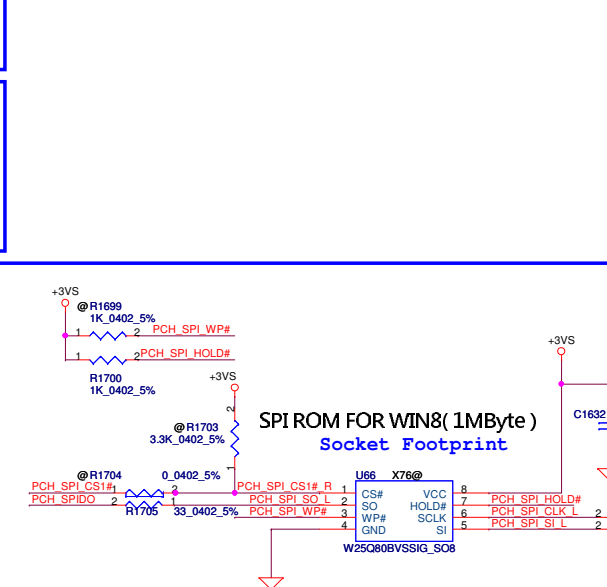
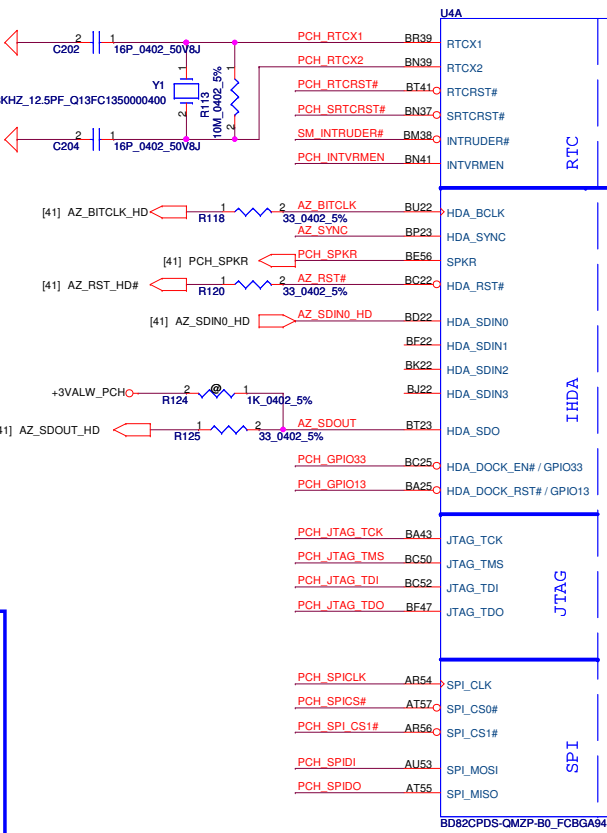
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Socket: SP07000F500/SP07000H900
Please close to U4 PCH

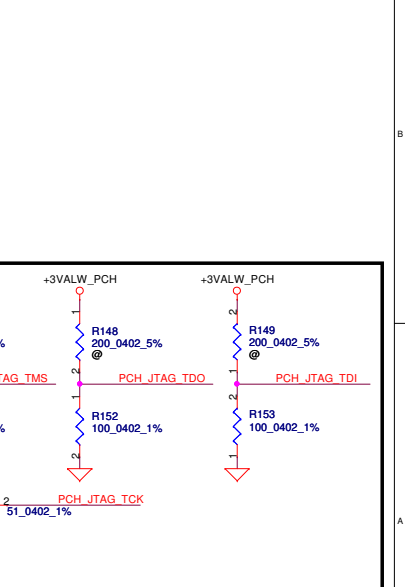


ODD

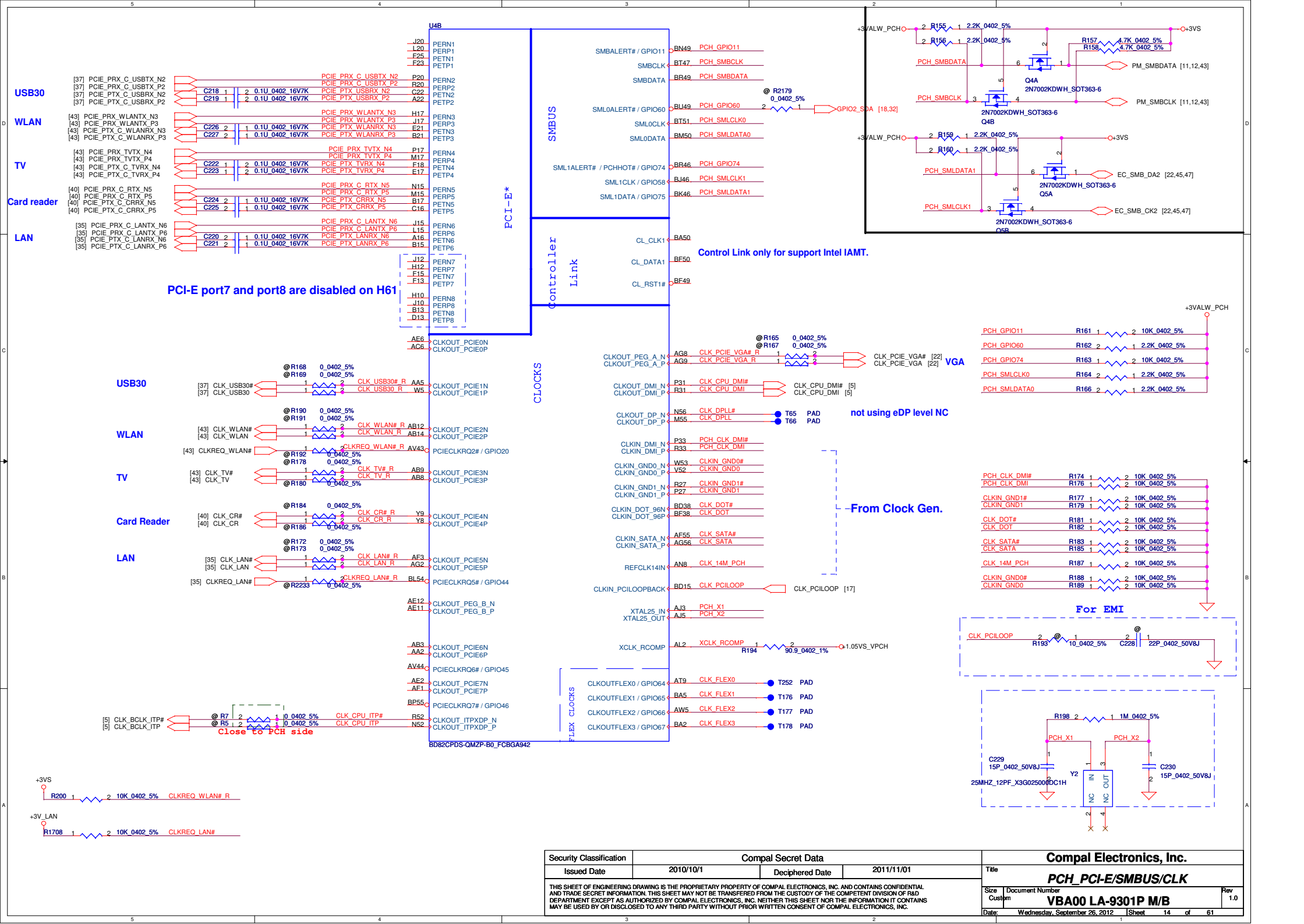
HDD

SATA port2 and port3 are disabled on H61

Place R128 and R130 within 500 mils of the PCH. Avoid routing next to clock pins.



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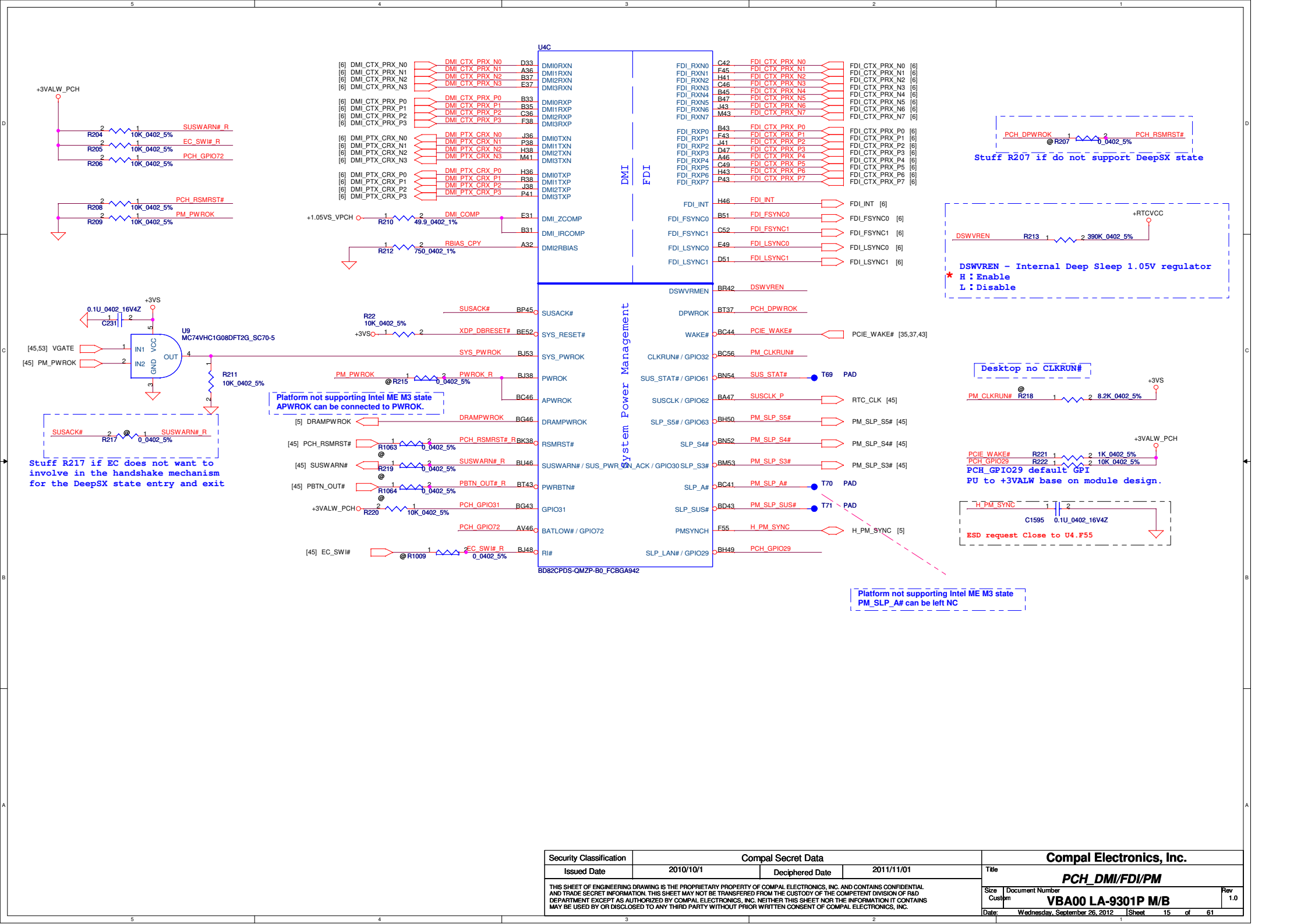
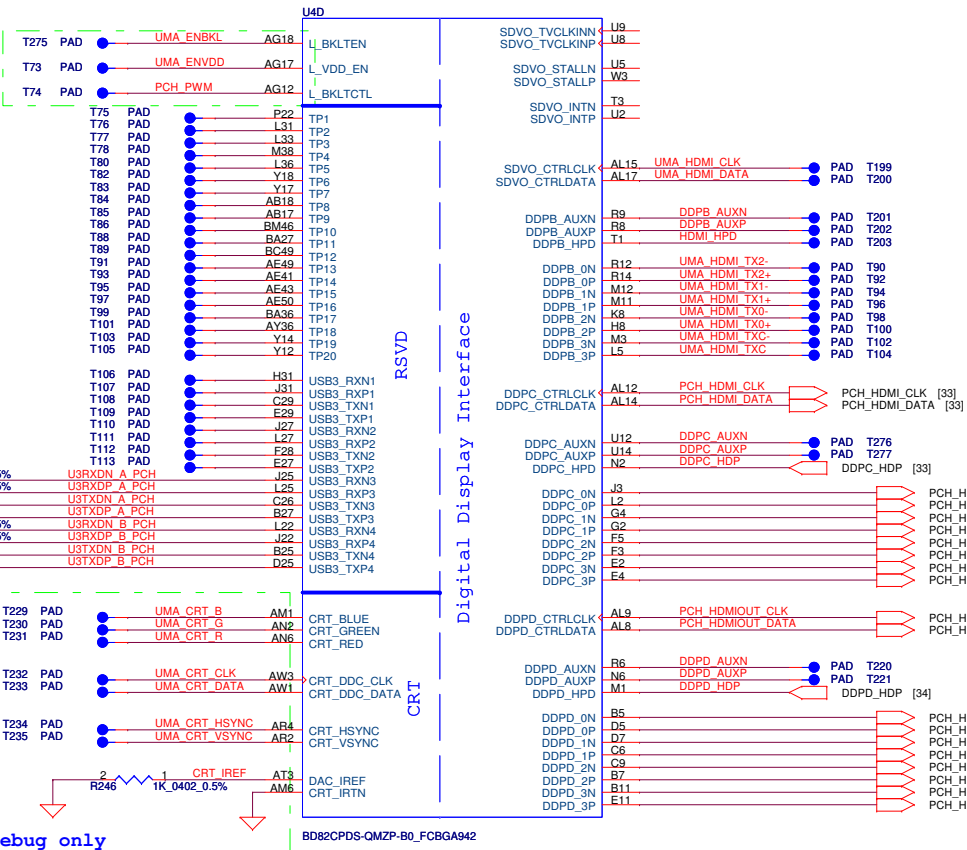
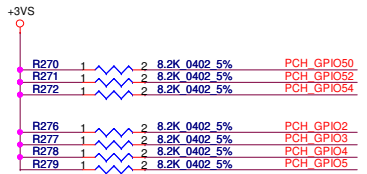
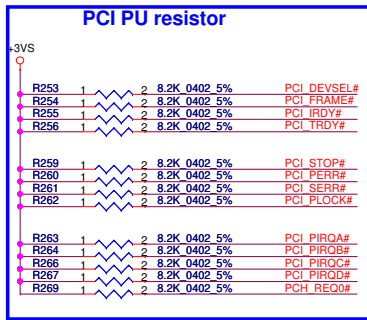


Table 13-1. Panther Point USB Port Mapping

	USB 2.0 Signals	SuperSpeed Signals
USB Port 0	USBP0P USBP0N	USB3Tp1
		USB3Tn1
		USB3Rn1
		USB3Rp1
USB Port 1	USBP1P USBP1N	USB3Tp2
		USB3Tn2
		USB3Rn2
		USB3Rp2
USB Port 2	USBP2P USBP2N	USB3Tp3
		USB3Tn3
		USB3Rn3
		USB3Rp3
USB Port 3	USBP3P USBP3N	USB3Tp4
		USB3Tn4
		USB3Rn4
		USB3Rp4

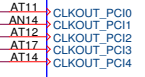
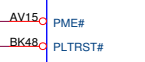
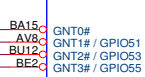
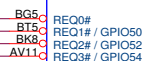
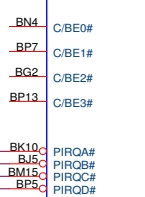
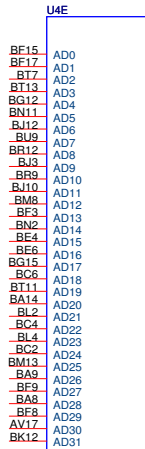
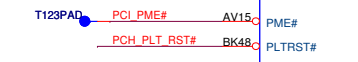
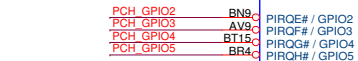
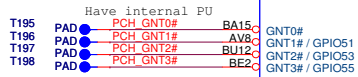
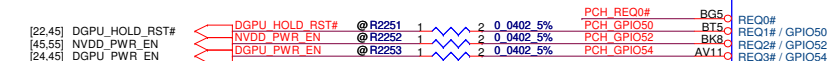
NOTE: PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.





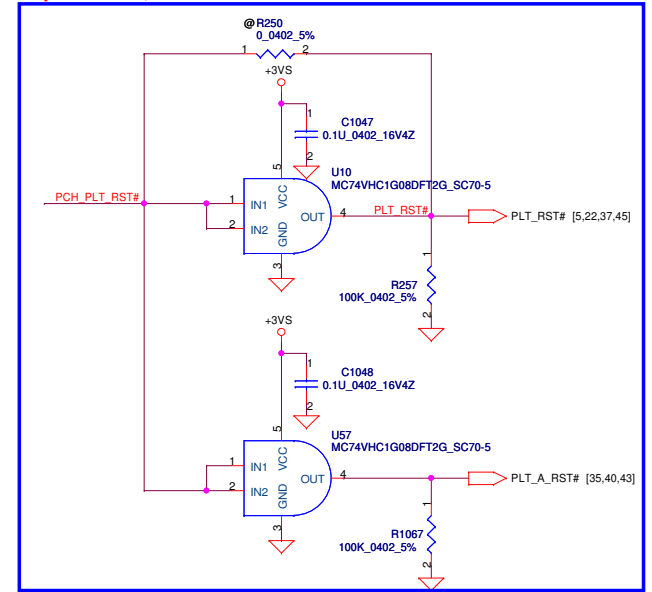
Intel confirm GPIO19 is correct.

PCH_GNT1#	GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★



BD82CPDS-QM2P-B0_FCBGA942

Seperate U10, U57 location



Rear IO USB 2.0 PORT

Reserve for USB30 PORT1@ CONN1

Place close to JUSB1/2

Reserve for USB30 PORT0@ CONN2

USB port6 and port7 are disabled on H61

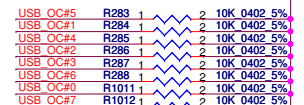
TV Tuner

WLAN

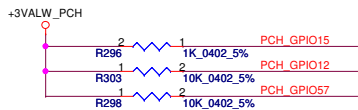
Rear IO USB 2.0 PORT

USB port12 and port13 are disabled on H61

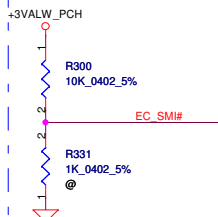
Layout Note:USB_BIAS WITH LENGTH NO MORE THAN 500 MILS TO RESISTOR.



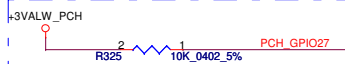
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				Size	Rev
				Custom	1.0
				Document Number	
				VBA00 LA-9301P M/B	
				Date	Wednesday, September 26, 2012
				Sheet	17 of 61



GPIO8
★ Integrated Clock Chip Enable (Removed)
H: Disable
L: Enable

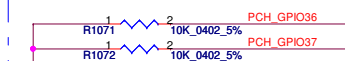
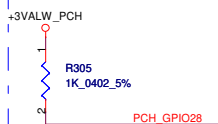


Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

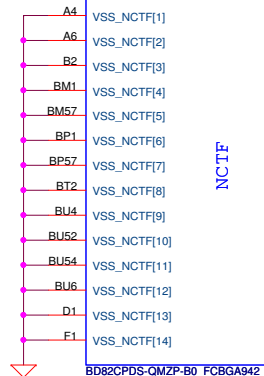
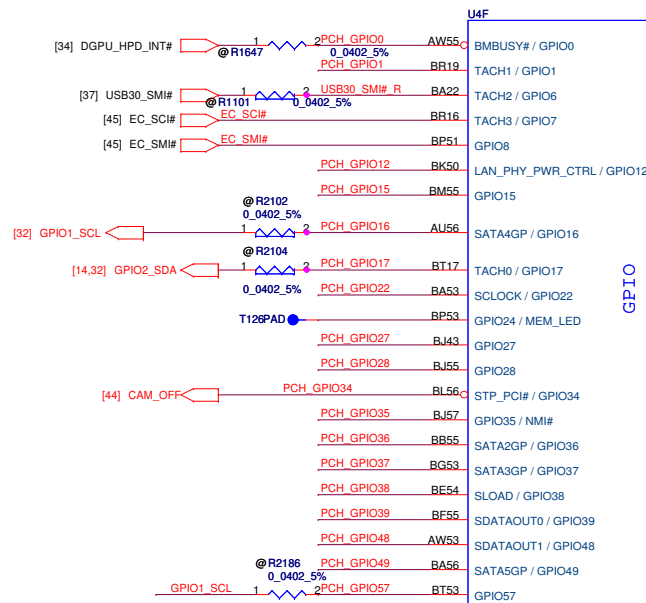
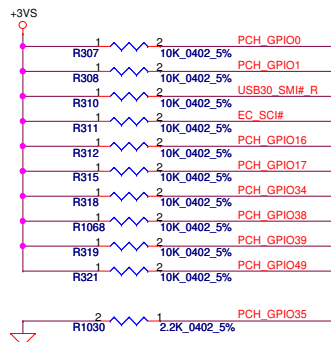
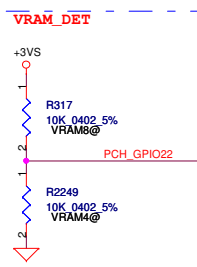
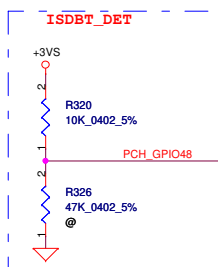


In Deep Sleep Power Well. Unmuxed.
Defaults to GPI.
Not used Weak pull-up 10kΩ to VccDSW3_3
-->Check list1.5 P402.
PD to GND for Huron River!!

GPIO28
★ On-Die PLL Voltage Regulator
H: Enable
L: Disable

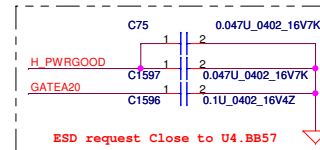
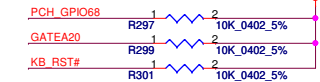
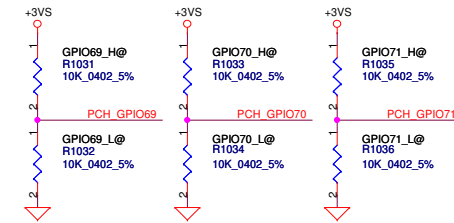


SATA2GP/GPIO36 & SATA3GP/GPIO37sampled at Rising edge of PWROK.Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

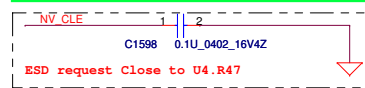
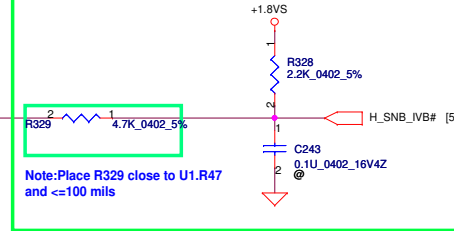


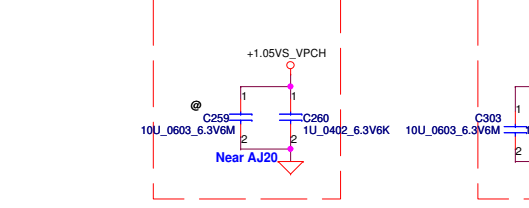
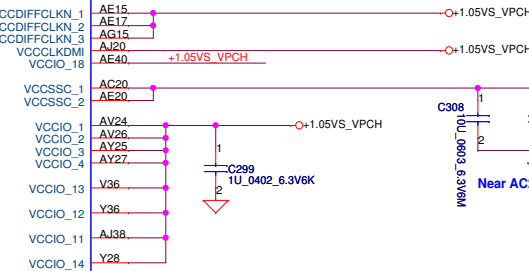
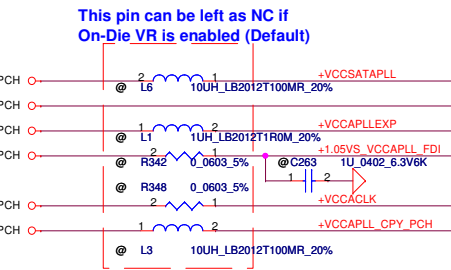
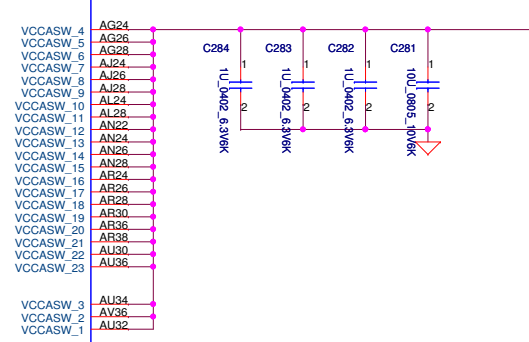
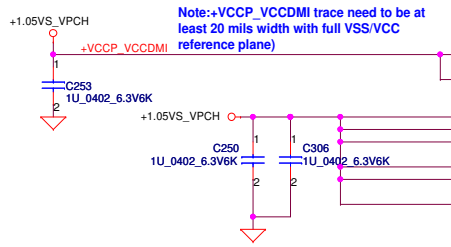
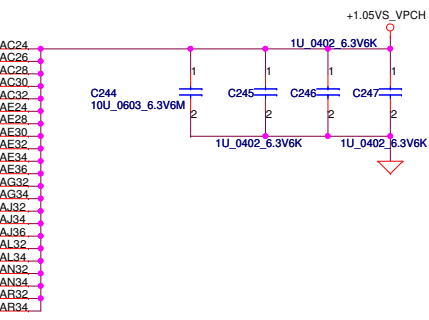
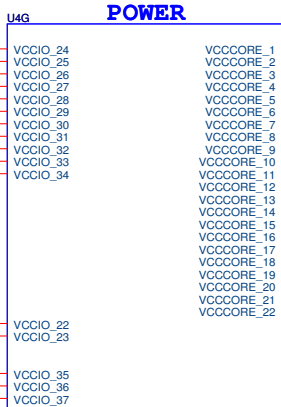
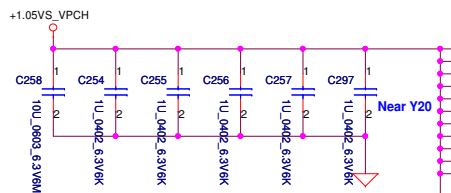
Project ID	GPIO69	GPIO70	GPIO71
SKU1	0	0	0
SKU2	0	0	1
SKU3	0	1	0
SKU4	0	1	1
SKU5	1	0	0
SKU6	0	0	1
SKU7	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

PROJECT ID TABLE

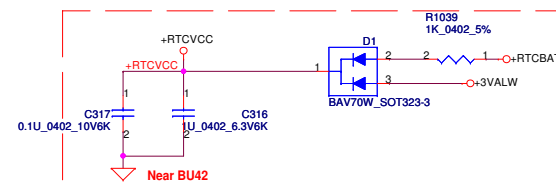
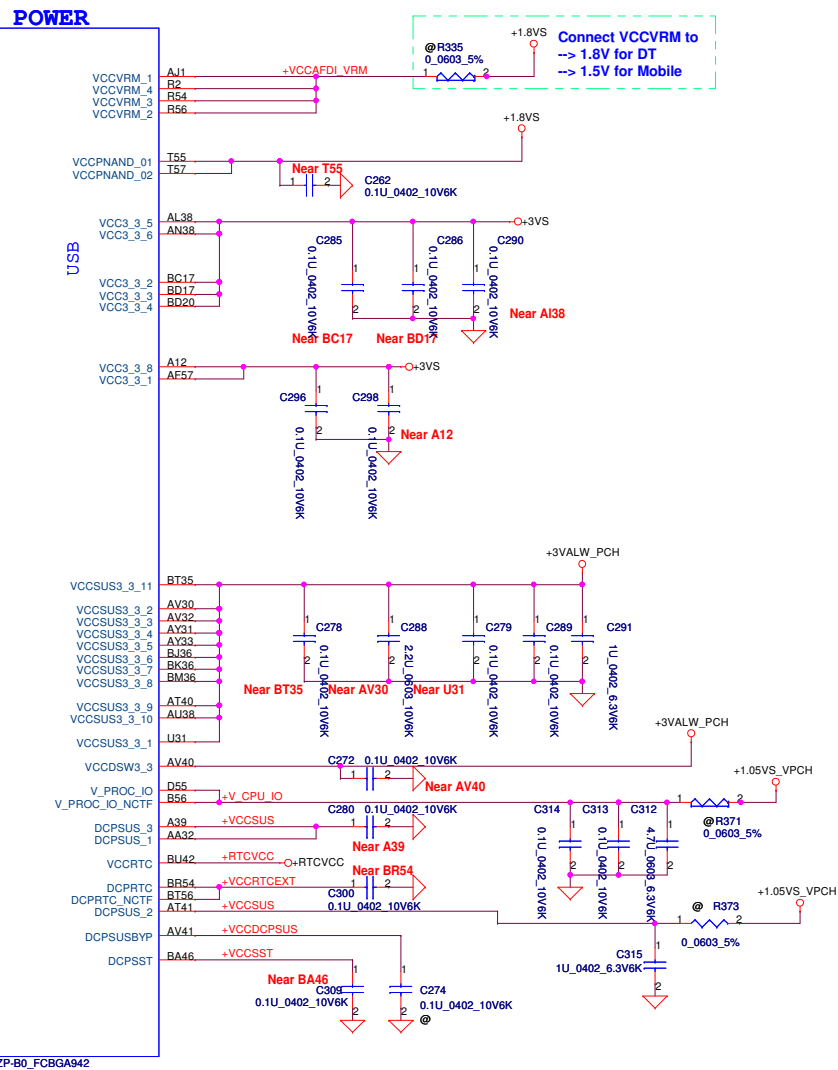
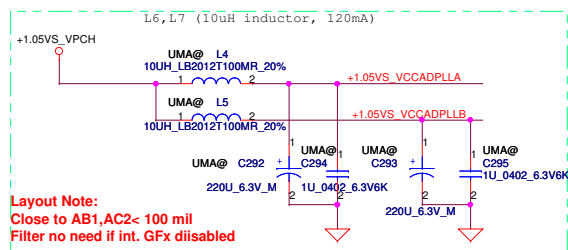
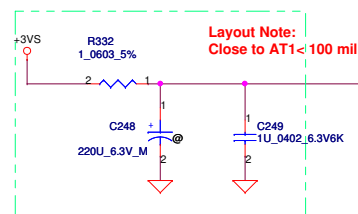
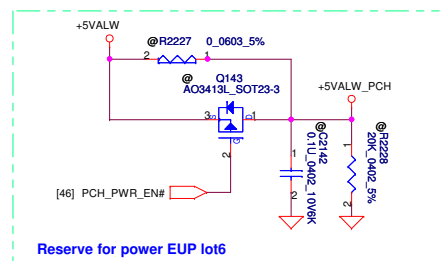


DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW

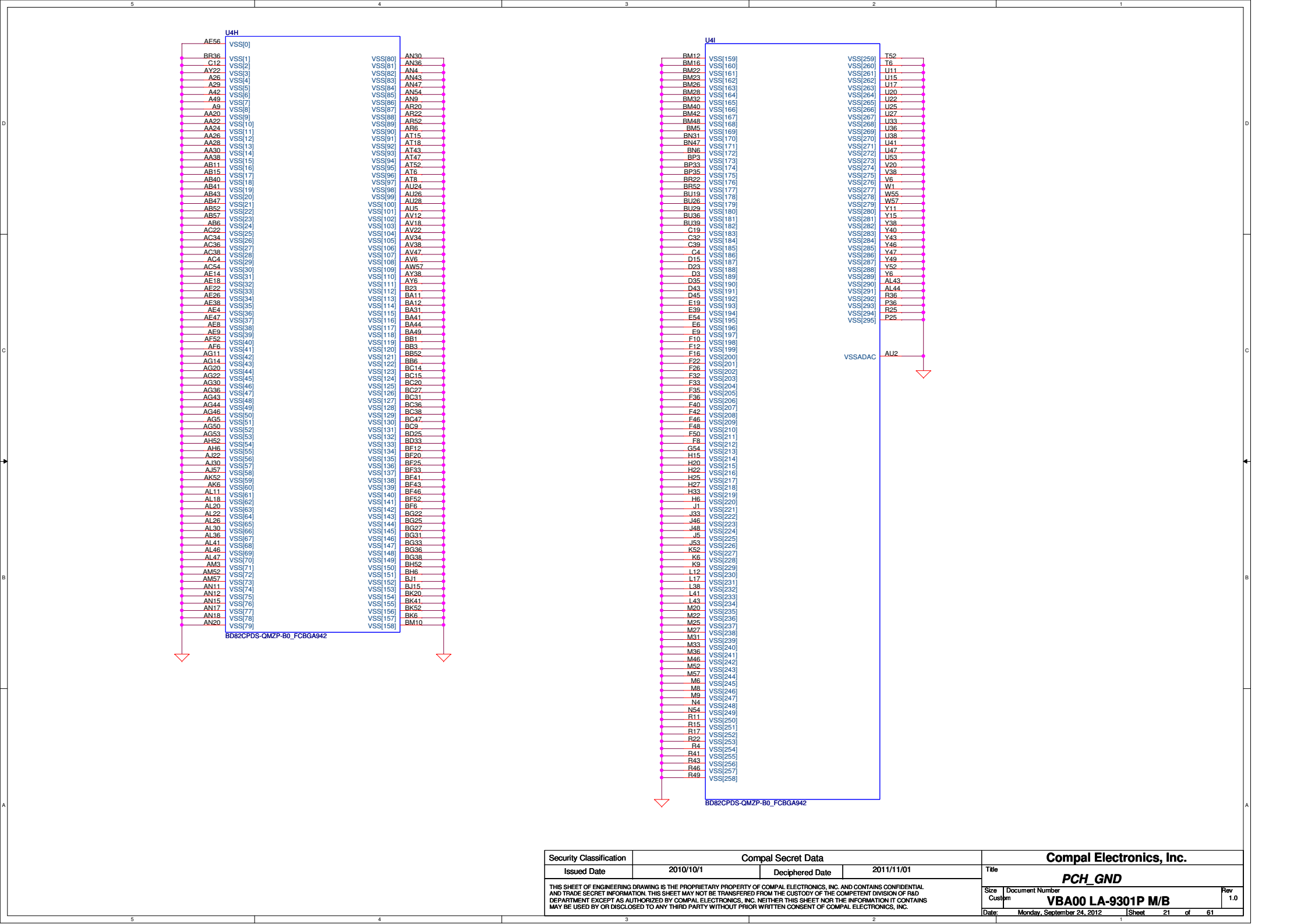




PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	1mA
V5REF	5	1mA
V5REF_SUS	5	1mA
VCC3_3	3.3	409mA
VCCADAC	3.3	68mA
VCCADPLLA	1.05	100mA
VCCADPLLB	1.05	100mA
VCCCORE	1.05	1600mA
VCCDMI	1.05	57mA
VCCIO	1.05	4070mA
VCCASW	1.05	1610mA
VCCSPI	3.3	20mA
VCCDSW	3.3	3mA
VCCDFTerm	1.8	200mA
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	97mA
VCCSUSHDA	3.3 / 1.5	10mA
VCCVRM	1.5	159mA
VCCCLKDMI	1.05	20mA
VCCSSC	1.05	105mA
VCCDIFFCLKN	1.05	55mA

[illegible]

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				Size	Document Number	Rev
				Custlsm	VBA00 LA-9301P M/B	1.0
				Date:	Wednesday, September 26, 2012	Sheet 20 of 61



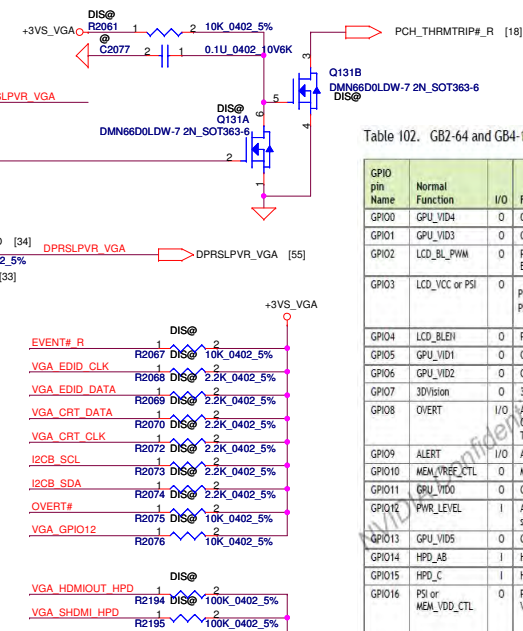
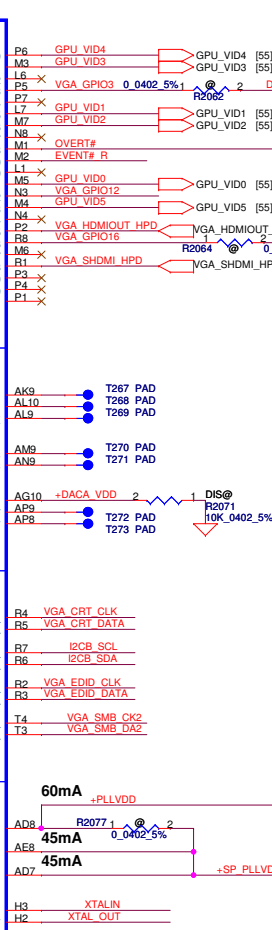
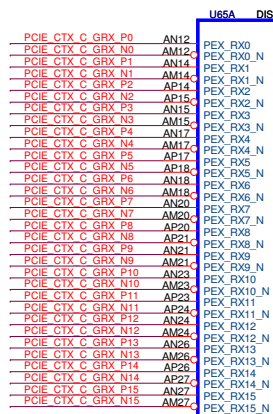
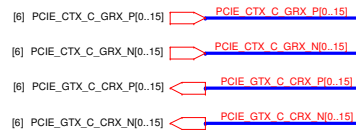
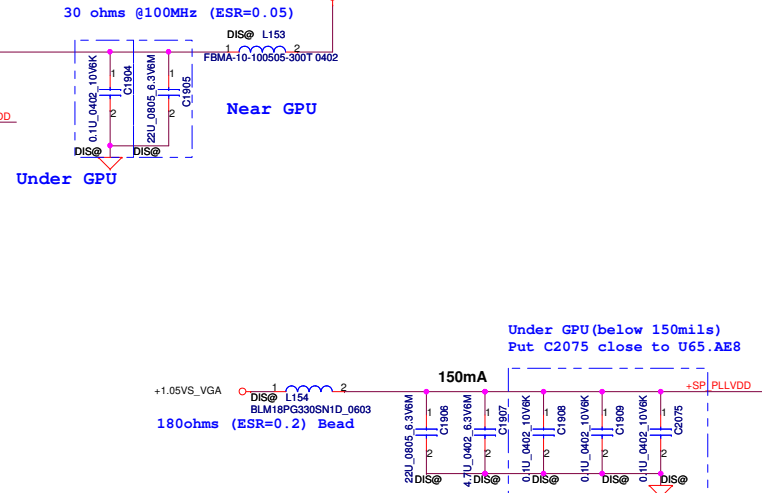
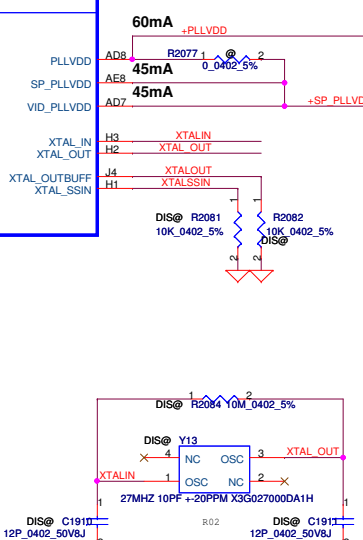
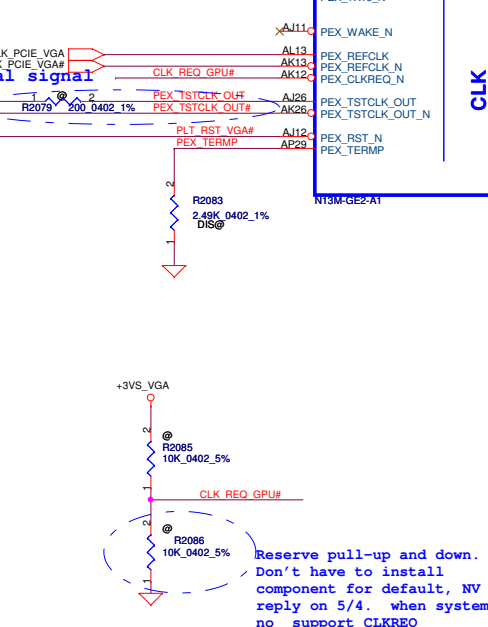
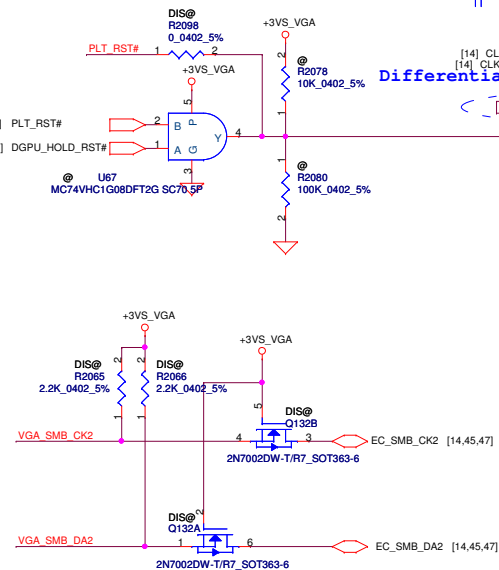
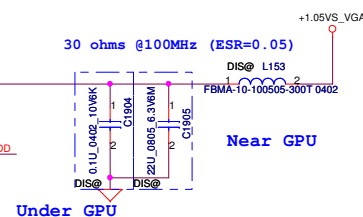


Table 102. GB2-64 and GB4-128 GPIO Description

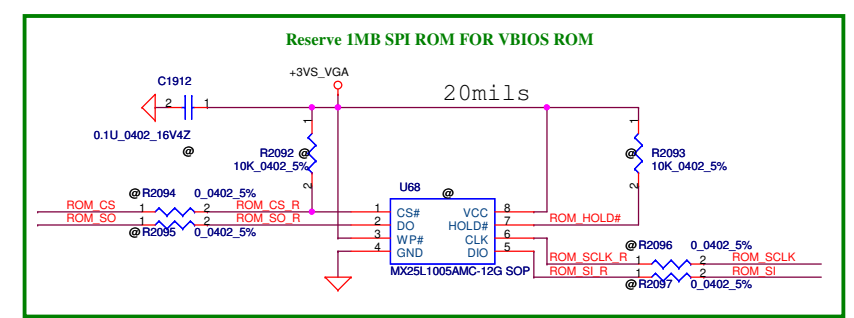
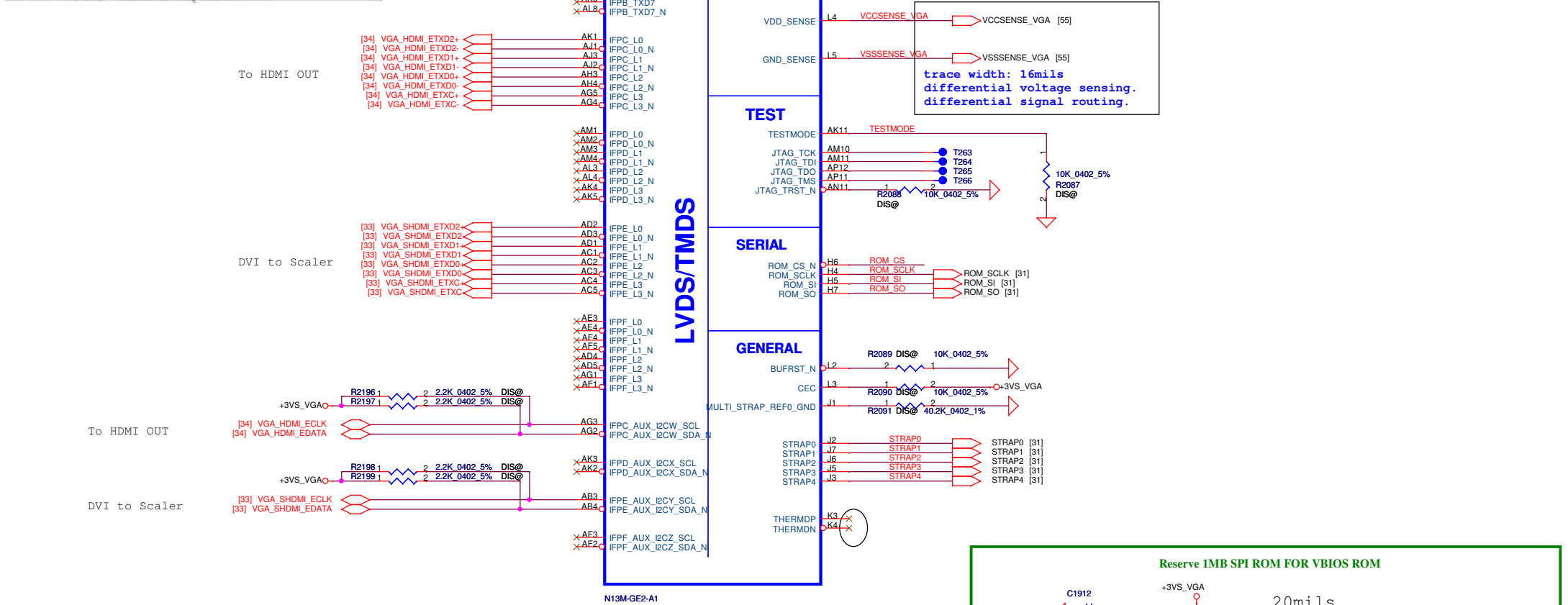
GPI0 pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPI00	GPU_VID4	0	GPU Core VDD VID4	Strap to boot HVDD
GPI01	GPU_VID3	0	GPU Core VDD VID3	Strap to boot HVDD
GPI02	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control	100 K pull-down
GPI03	LCD_VCC or PSI	0	Panel Power Enable or Phase Shedding	LCD_VCC: 100K pull-down PSI: 10K pull-up or pull-down stuff as needed to disable phase shedding by default
GPI04	LCD_BLE1	0	Panel Backlight Enable	100 K pull-down
GPI05	GPU_VID1	0	GPU Core VDD VID1	Strap to boot HVDD
GPI06	GPU_VID2	0	GPU Core VDD VID2	Strap to boot HVDD
GPI07	3D Vision	0	3D Vision Left/Right signal	100 K pull-down
GPI08	OV/ERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPI09	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPI10	MEM_VREF_CTL	0	Memory VREF Control	100 K pull-down
GPI11	GPU_VID0	0	GPU Core VDD VID0	Strap to boot HVDD
GPI12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPI13	GPU_VID5	0	GPU Core VDD VID5	Strap to boot HVDD
GPI14	HPD_AB	I	Hot Plug Detect for iFPAB	See Figure 76
GPI15	HPD_C	I	Hot Plug Detect for iFPAC	See Figure 76
GPI16	PSI or MEM_VDD_CTL	0	Phase Shedding or Memory VDD VID	PSI: 10K pull-up or pull-down stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPI17	HPD_D	I	Hot Plug Detect for iFPD	See Figure 76
GPI18	HPD_E	I	Hot Plug Detect for iFPE	See Figure 76
GPI19	HPD_F	I	Hot Plug Detect for iFPF	See Figure 76
GPI20	Reserved			
GPI21	Reserved			

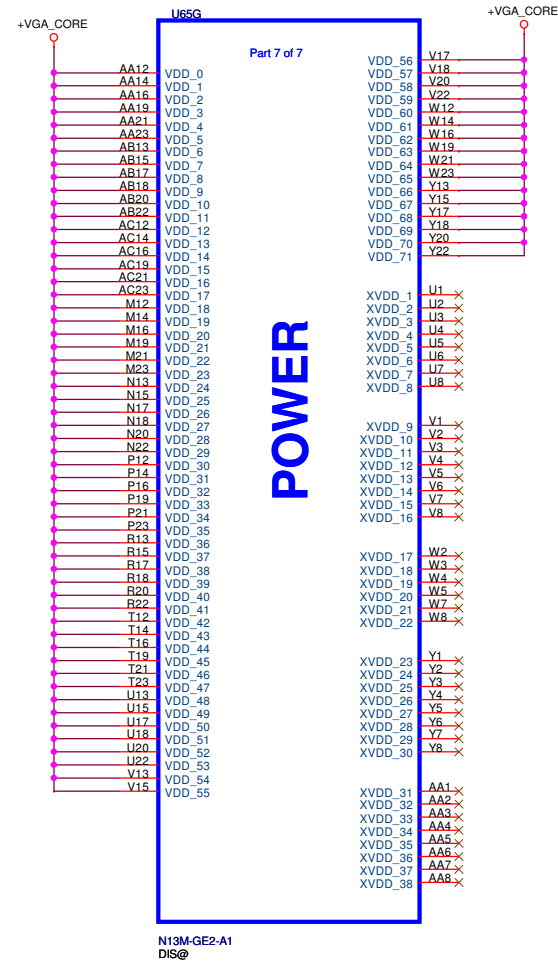
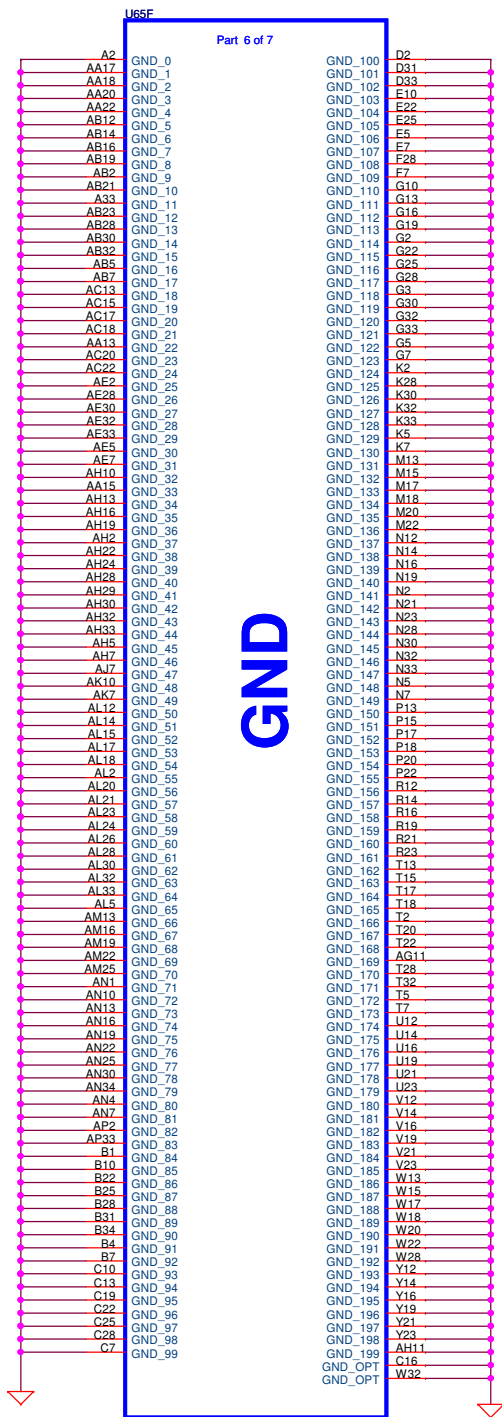


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				Size	Document Number	Rev
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Date:				Wednesday, September 26, 2012	Sheet	22 of 61

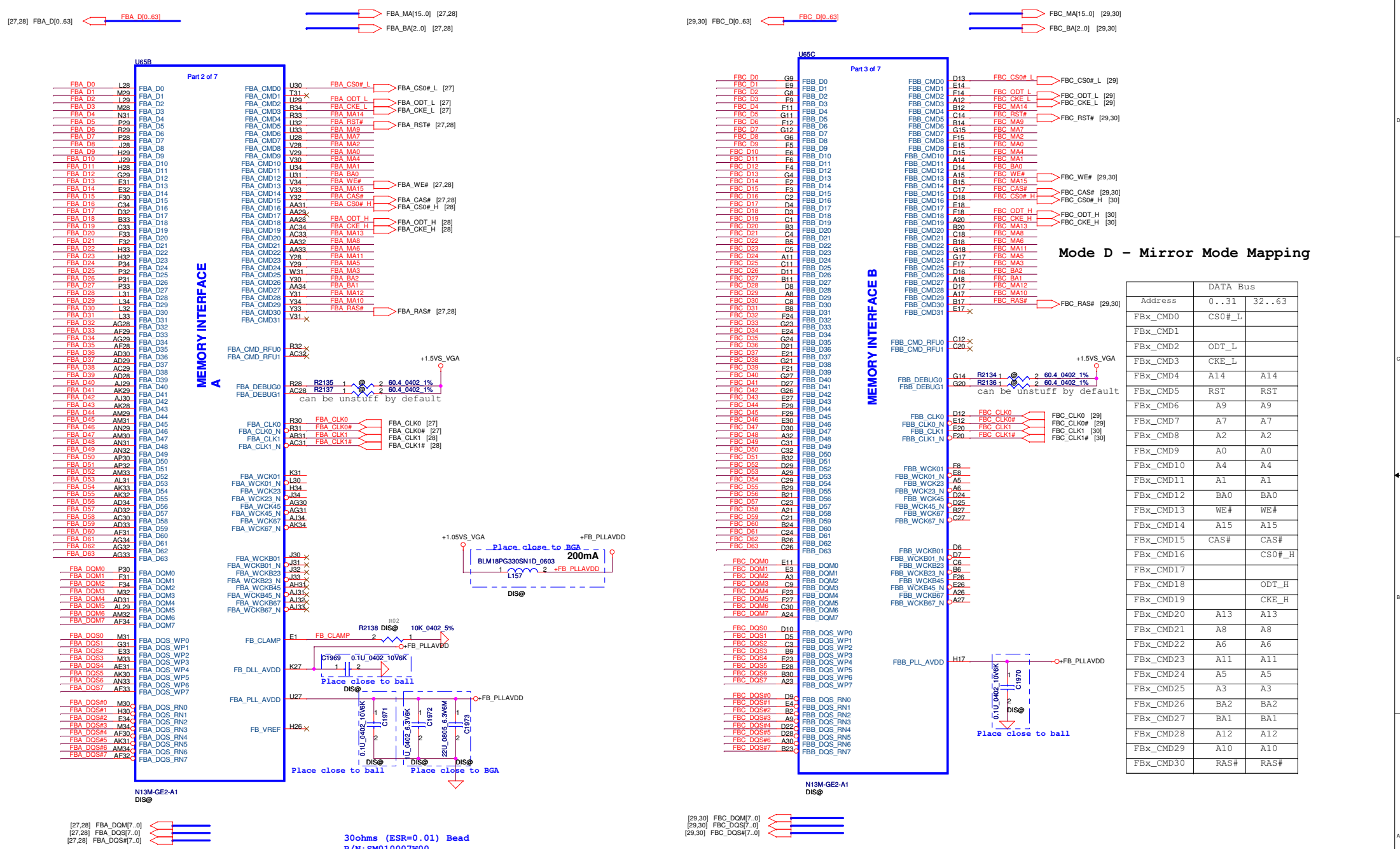
Table 66. N13x Family Display Link Summary

Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI





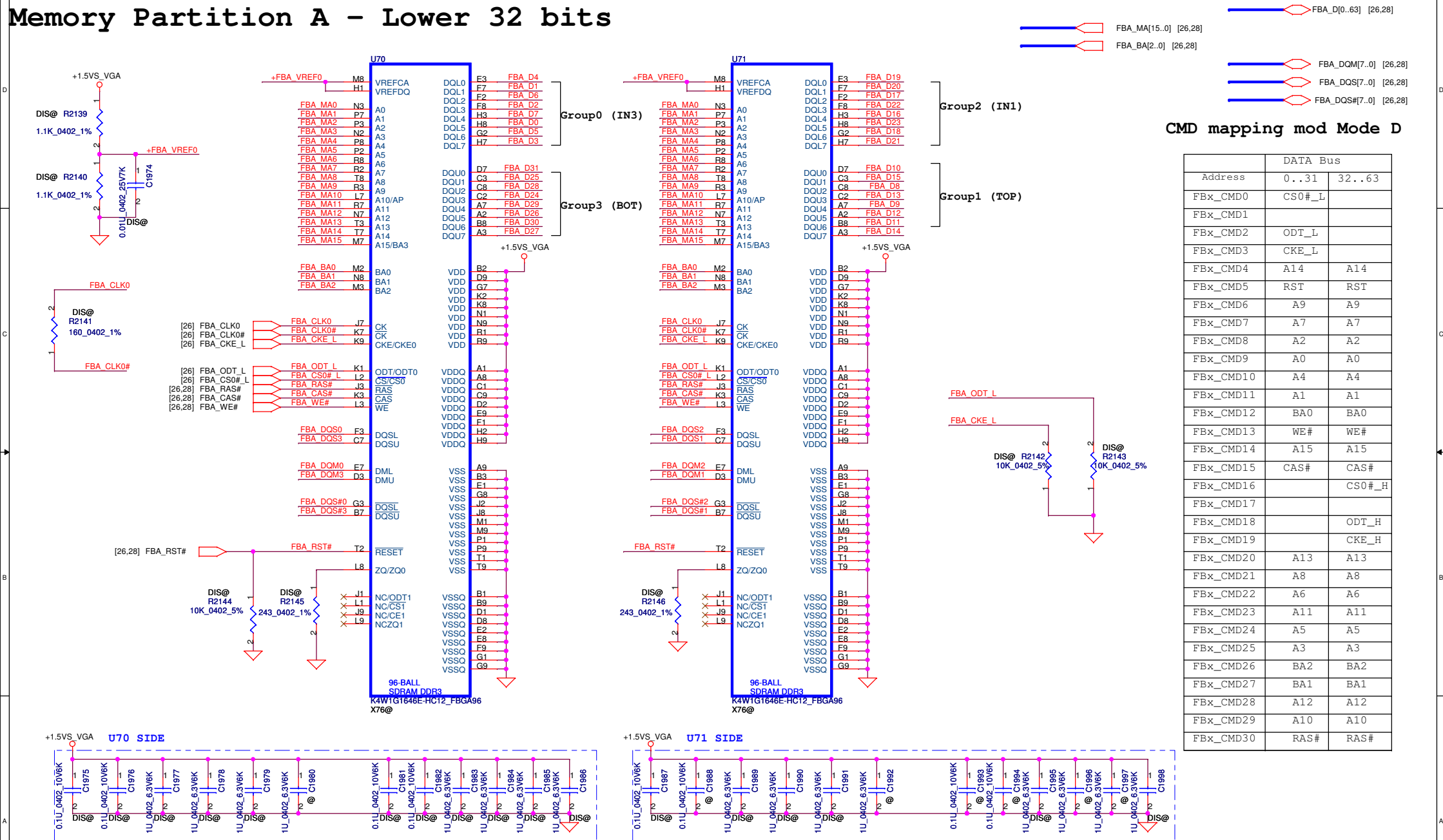
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						Size		Document Number		Rev	
								VBA00 LA-9301P M/B		1.0	
						Date:		Monday, September 24, 2012		Sheet 25 of 61	



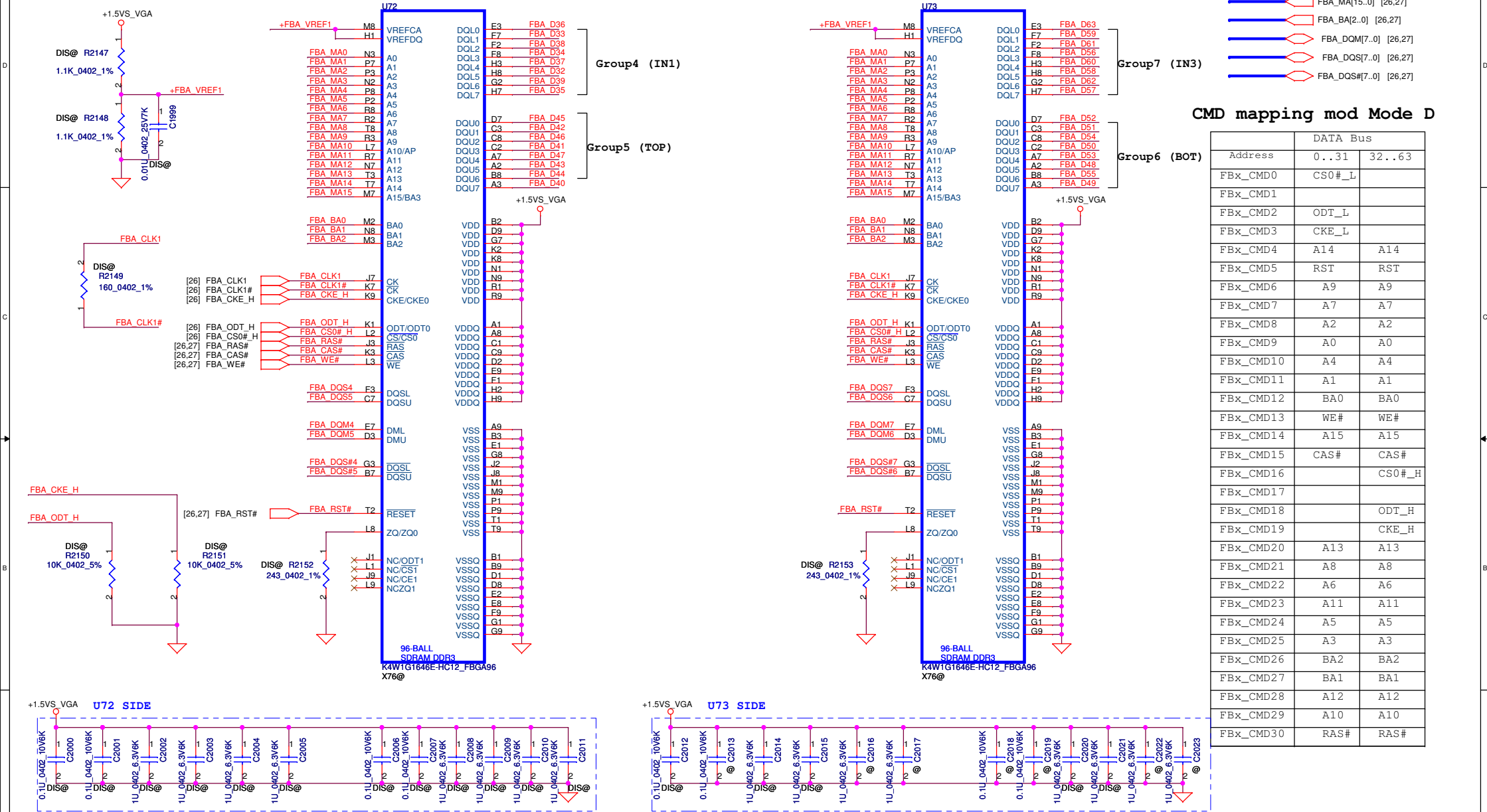
Mode D - Mirror Mode Mapping

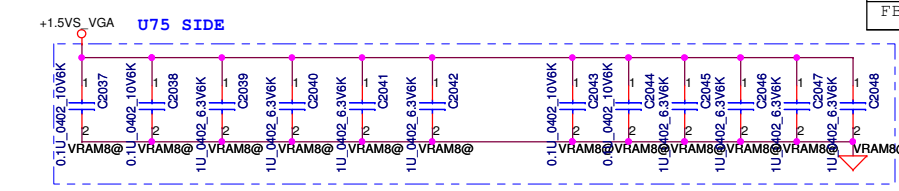
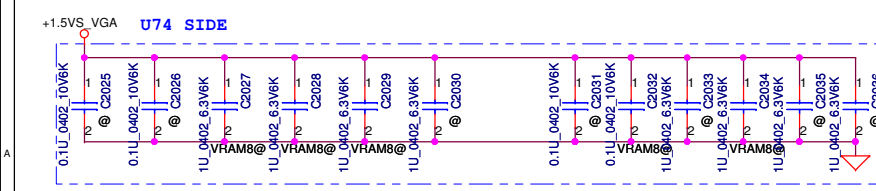
Address	DATA Bus
FBx_CMD0	CS0#_L
FBx_CMD1	ODT_L
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14
FBx_CMD5	RST
FBx_CMD6	A9
FBx_CMD7	A7
FBx_CMD8	A2
FBx_CMD9	A0
FBx_CMD10	A4
FBx_CMD11	A1
FBx_CMD12	BA0
FBx_CMD13	WE#
FBx_CMD14	A15
FBx_CMD15	CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13
FBx_CMD21	A8
FBx_CMD22	A6
FBx_CMD23	A11
FBx_CMD24	A5
FBx_CMD25	A3
FBx_CMD26	BA2
FBx_CMD27	BA1
FBx_CMD28	A12
FBx_CMD29	A10
FBx_CMD30	RAS#

Memory Partition A - Lower 32 bits



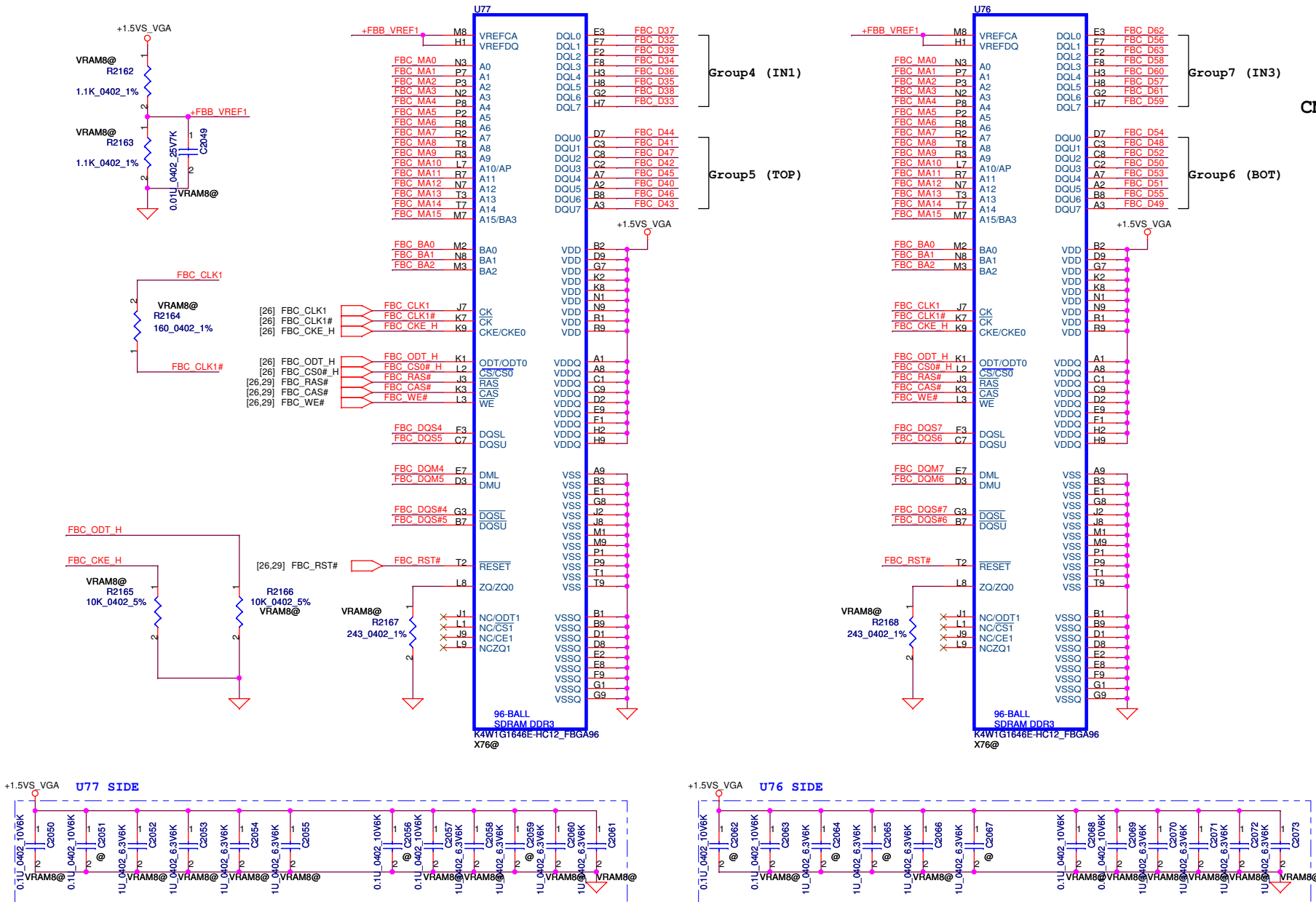
Memory Partition A - Upper 32 bits



[illegible]

	DATA Bus	
Address	0...31	32...63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Memory Partition C - Upper 32 bits



FBC_D[0..63] [26,29]

FBC_MA[15..0] [26,29]

FBC_BA[2..0] [26,29]

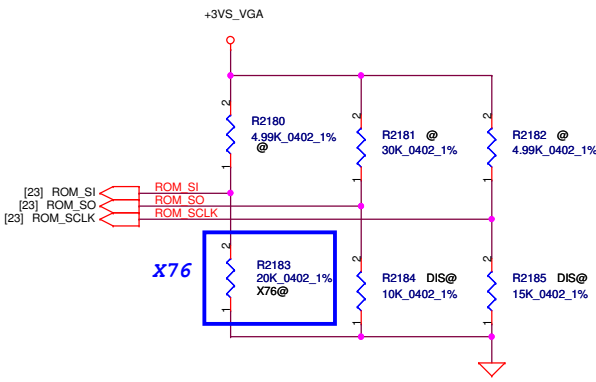
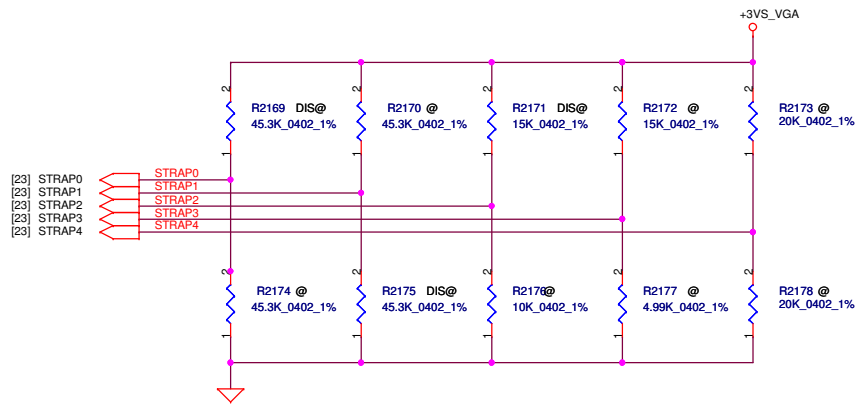
FBC_DQM[7..0] [26,29]

FBC_DQS[7..0] [26,29]

FBC_DQS# [7..0] [26,29]

CMD mapping mod Mode D

Address	DATA Bus
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14
FBx_CMD5	RST
FBx_CMD6	A9
FBx_CMD7	A7
FBx_CMD8	A2
FBx_CMD9	A0
FBx_CMD10	A4
FBx_CMD11	A1
FBx_CMD12	BA0
FBx_CMD13	WE#
FBx_CMD14	A15
FBx_CMD15	CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13
FBx_CMD21	A8
FBx_CMD22	A6
FBx_CMD23	A11
FBx_CMD24	A5
FBx_CMD25	A3
FBx_CMD26	BA2
FBx_CMD27	BA1
FBx_CMD28	A12
FBx_CMD29	A10
FBx_CMD30	RAS#



GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE2	900 MHz	64M* 16* 4 512MB	Hynix (0x2) H5TQ1G63DFR-11C SA000041S20	1111 R PU 45K	0111 R PD 45K	1001 R PU 10K	NC	NC	0010 R2138 PD 15K	0001 R PD 10K	0010 R PD 15K
N13M-GE2	900 MHz	64M* 16* 4 512MB	Samsung (0x3) K4W1G1646G-BC11 SA00004GS00	1111 R PU 45K	0111 R PD 45K	1001 R PU 10K	NC	NC	0011 R2138 PD 20K	0001 R PD 10K	0010 R PD 15K
N13M-GE2	900 MHz	64M* 16* 8 1GB	Hynix (0x2) H5TQ1G63DFR-11C SA000041S20	1111 R PU 45K	0111 R PD 45K	1001 R PU 10K	NC	NC	0010 R2138 PD 15K	0001 R PD 10K	0010 R PD 15K
N13M-GE2	900 MHz	64M* 16* 8 1GB	Samsung (0x3) K4W1G1646G-BC11 SA00004GS00	1111 R PU 45K	0111 R PD 45K	1001 R PU 10K	NC	NC	0011 R2138 PD 20K	0001 R PD 10K	0010 R PD 15K
N13M-GE2	900 MHz	128M* 16* 8 2GB	Hynix (0x5) H5TQ2G63DFR-11C SA00003YO70	1111 R PU 45K	0111 R PD 45K	1001 R PU 10K	NC	NC	0101 R2138 PD 30K	0001 R PD 10K	0010 R PD 15K
N13M-GE2	900 MHz	128M* 16* 8 2GB	Samsung (0x1) K4W2G1646E-BC11 SA00005SH00	1111 R PU 45K	0111 R PD 45K	1001 R PU 10K	NC	NC	0001 R2138 PD 10K	0001 R PD 10K	0010 R PD 15K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

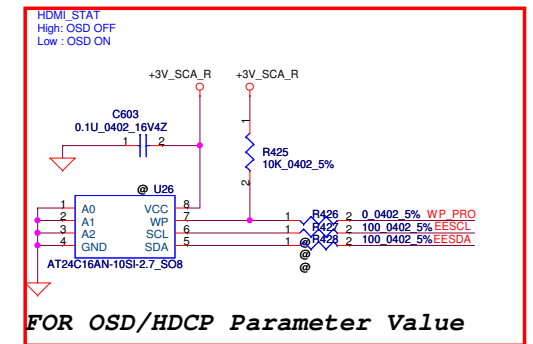
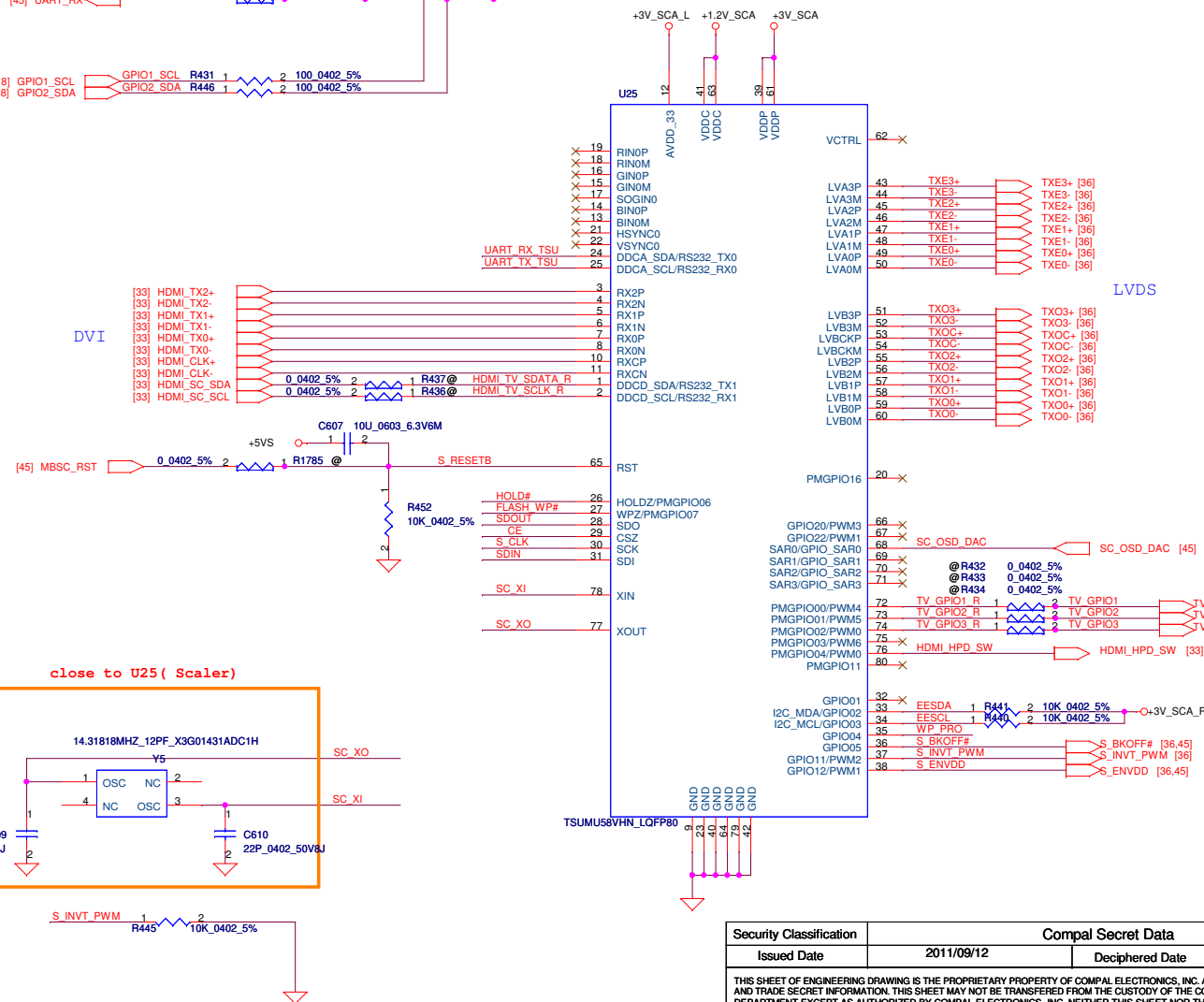
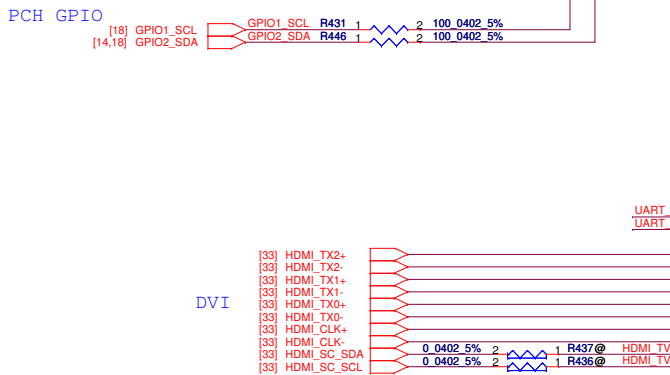
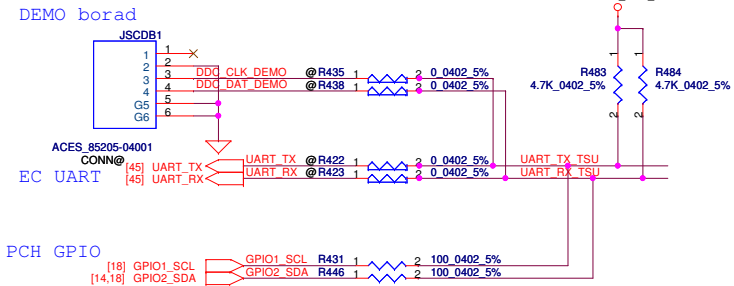
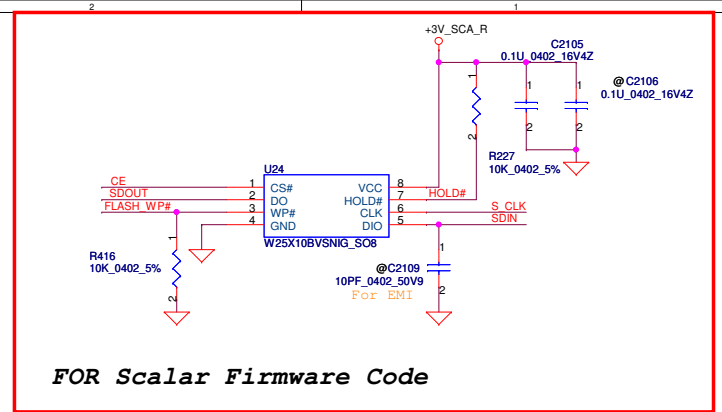
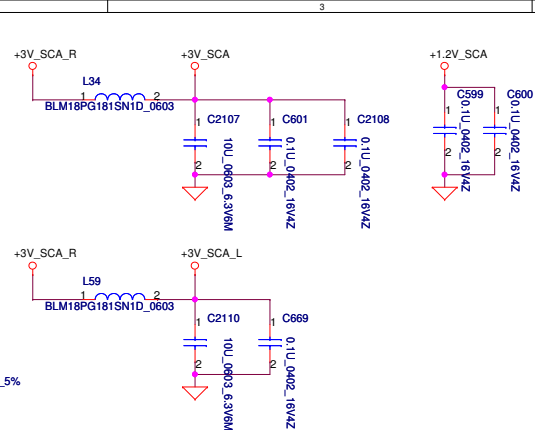
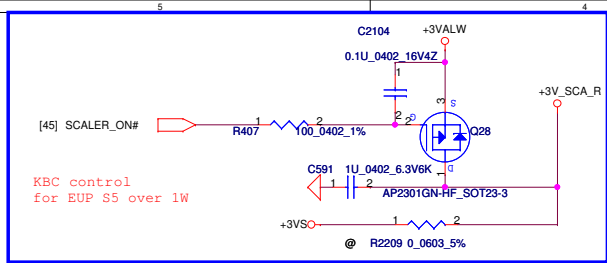
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

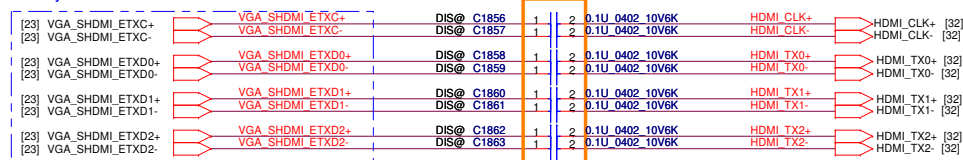
PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

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				Size Custom	Document Number	Rev
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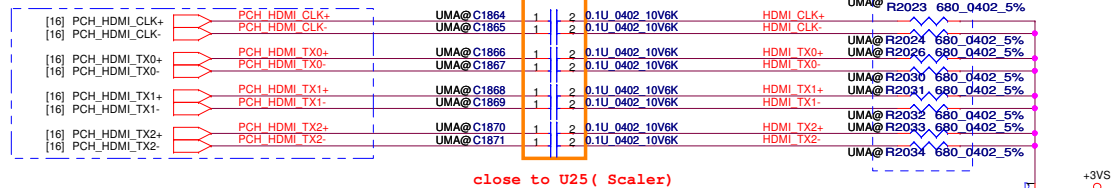


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Size	Document Number	VBA00 LA-9301P M/B		Rev	1.0
Date:	Wednesday, September 26, 2012	Sheet	32	of 61	

DIS only

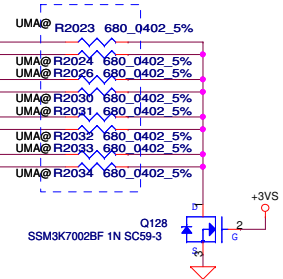


UMA only

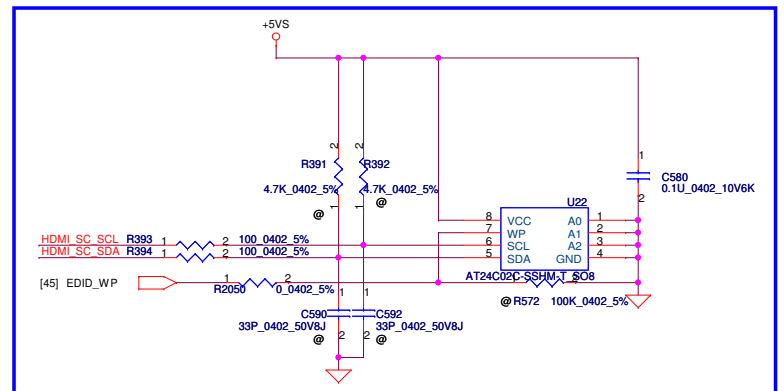
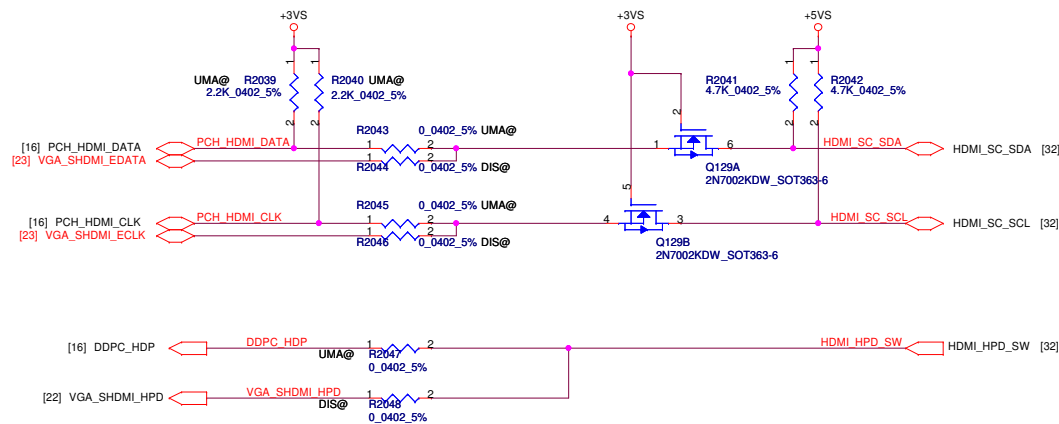
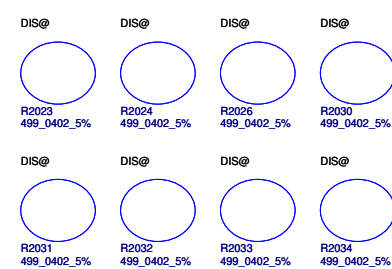


close to U25 (Scaler)

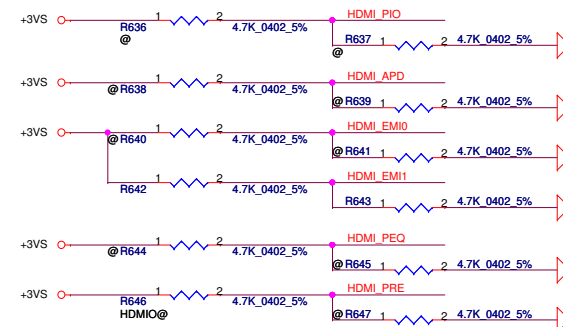
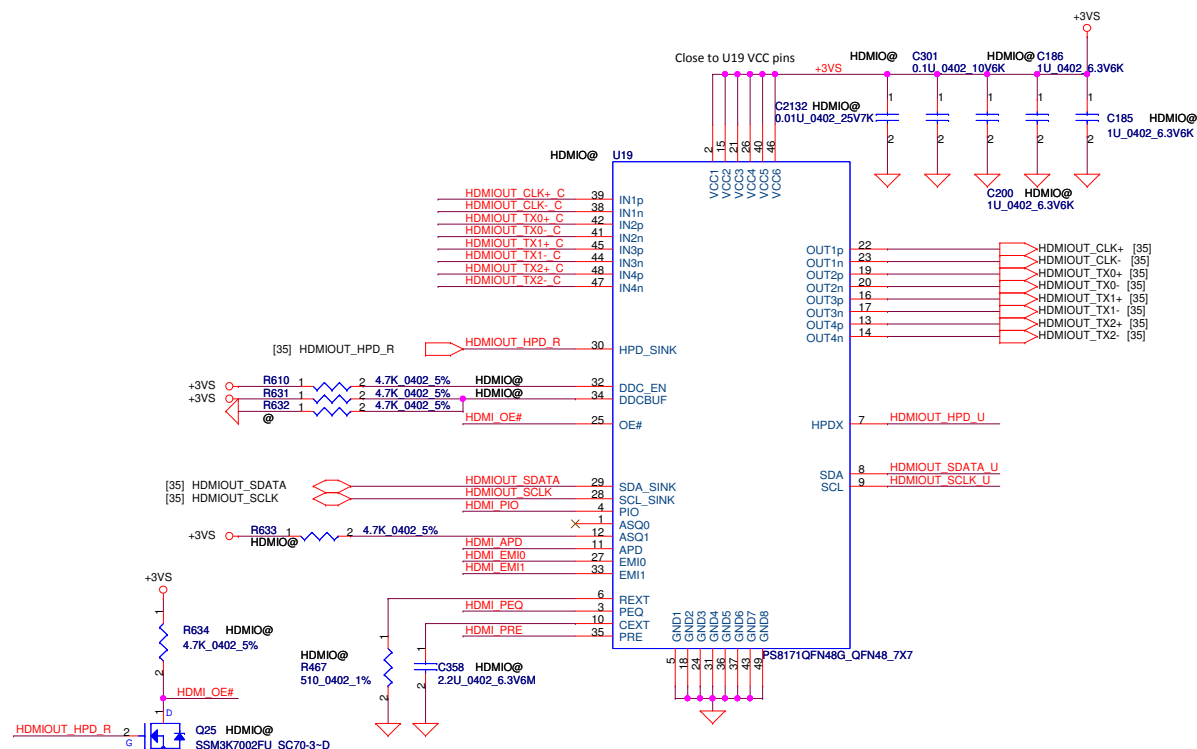
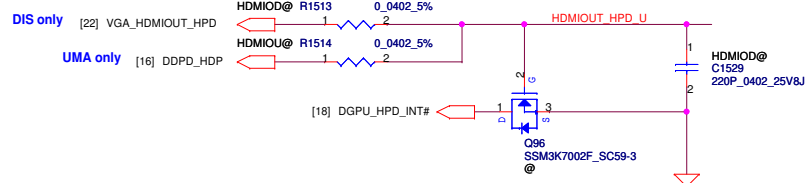
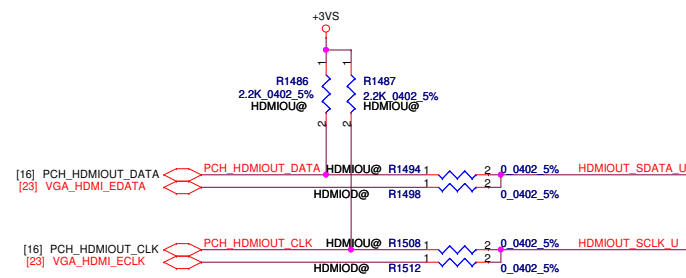
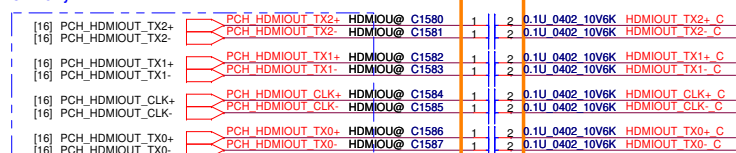
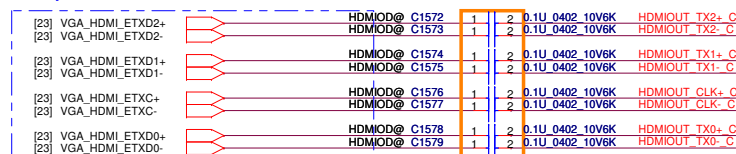
INTEL use 680 Ohm for termination



NV use 499 Ohm for termination



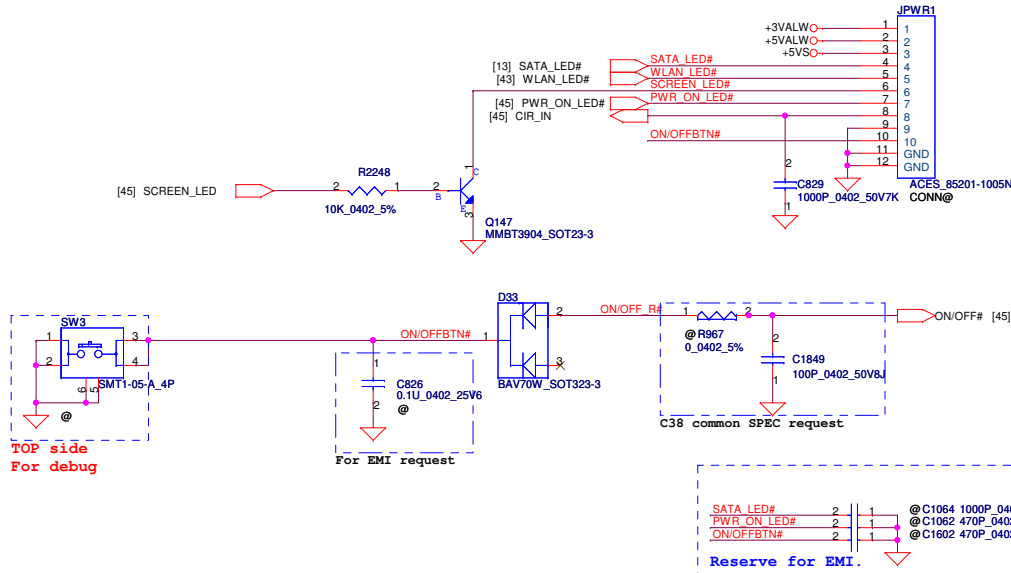
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Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title	
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	HIGH	LOW	MID
DDCBUF (Active Buffer)	Setting1	No	Setting2
PIO (HPD setting)	HPD=HPD_SINK#	HPD=HPD_SINK	
APD (Auto power down)	Enable	Disable	
PEQ (level of EQ)	High level	Mid level	Low level
PRE (pre-emphasis)	Low level	No	High level

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								Size	Document Number	Rev
								Custom	VBA00 LA-9301P M/B	1.0
								Date:	Wednesday, September 26, 2012	Sheet 34 of 61

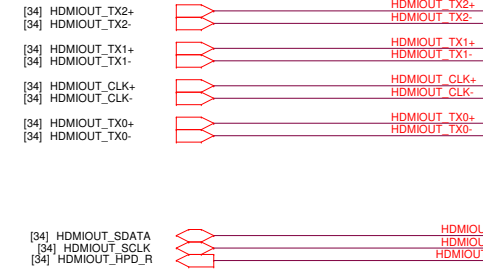
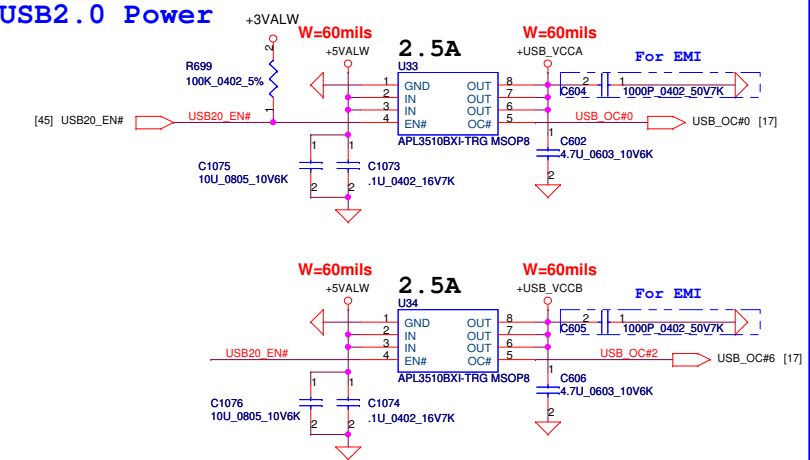
Power/B Connector



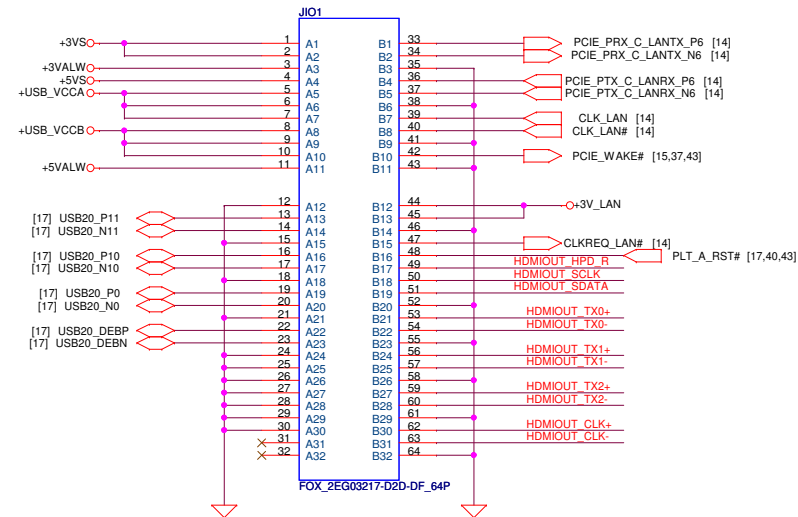
Function/B Connector



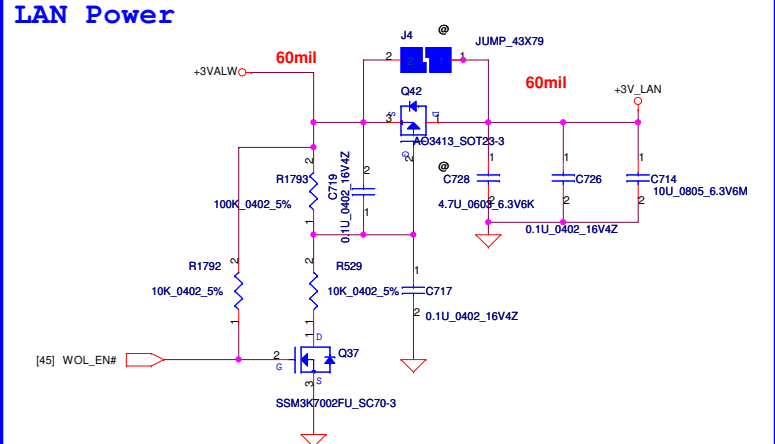
USB2.0 Power



PCIE_X4 Gold Finger(64 Pins)

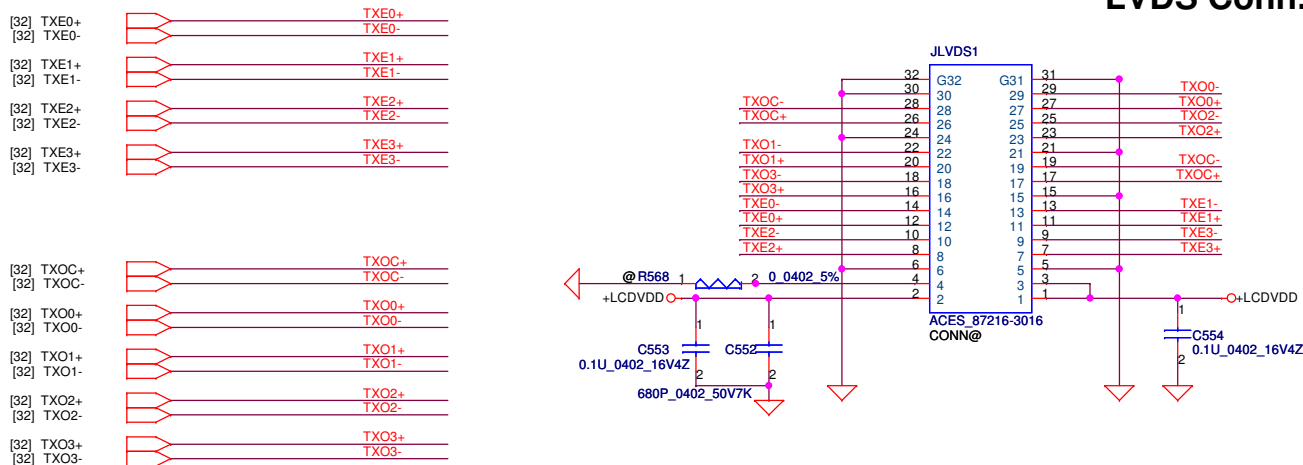


LAN Power

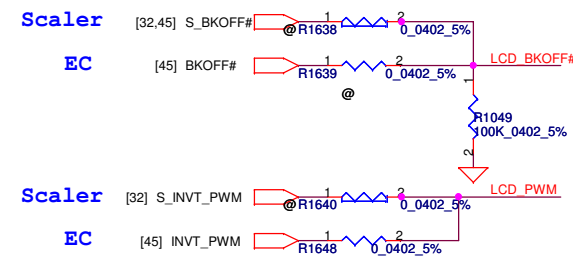
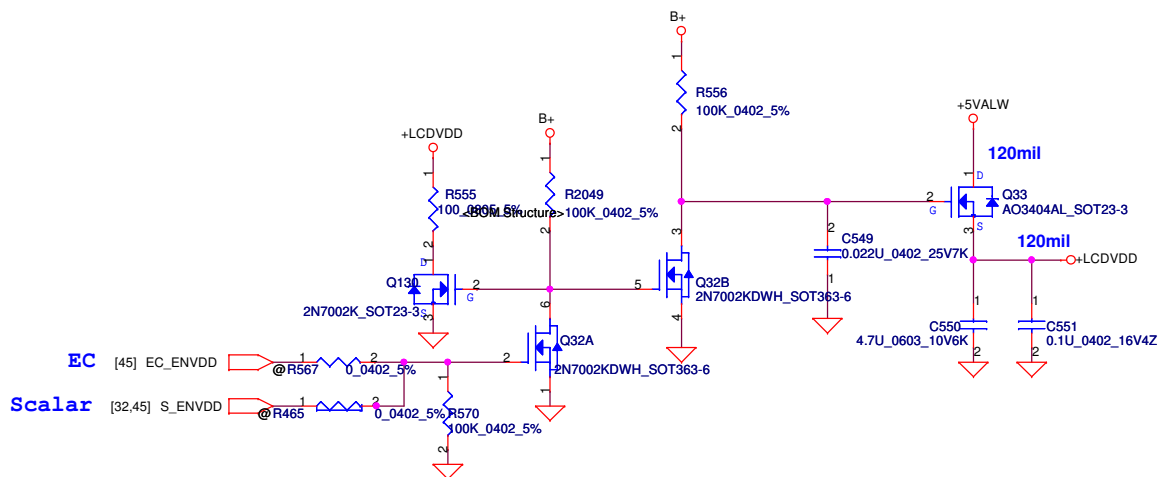
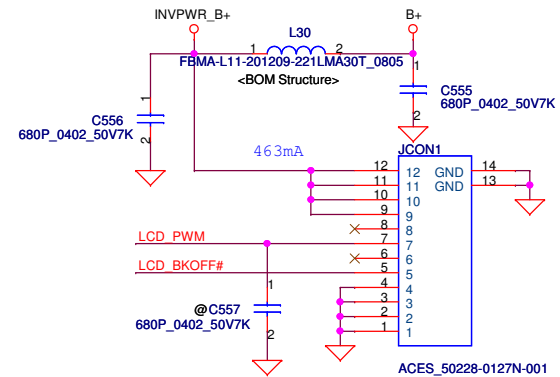


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LVDS Conn.

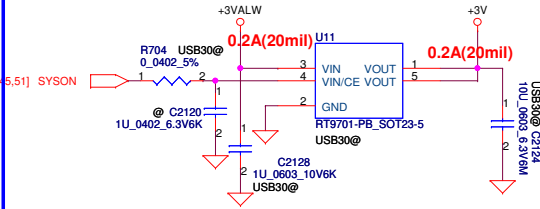


Converter

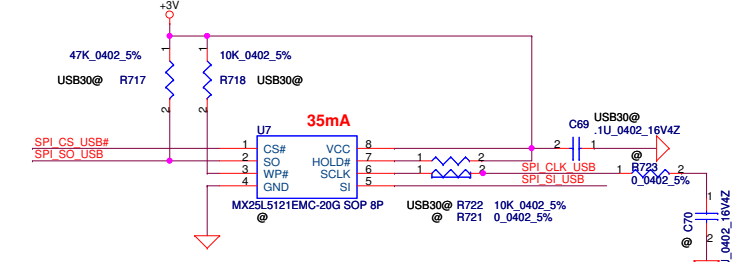
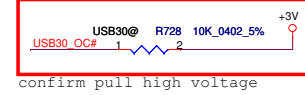
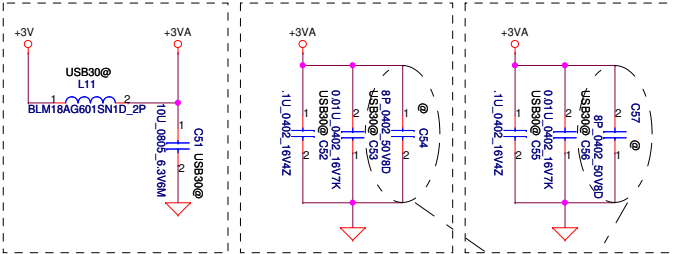
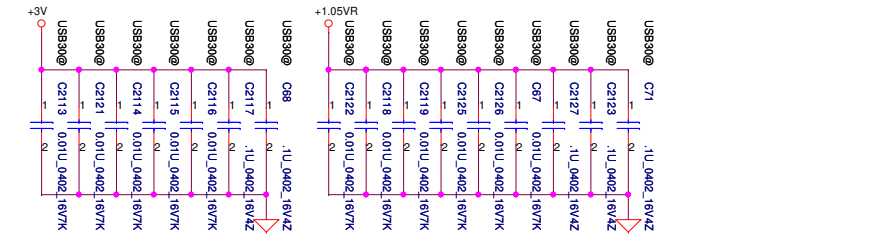
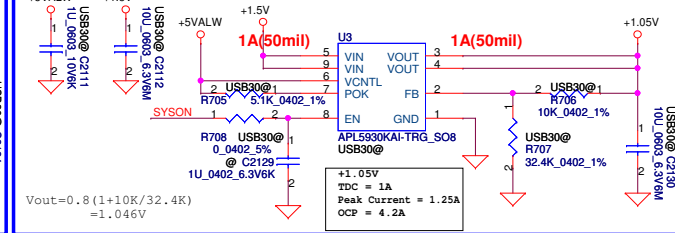


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				Date: Friday, September 21, 2012	Sheet 36 of 61	

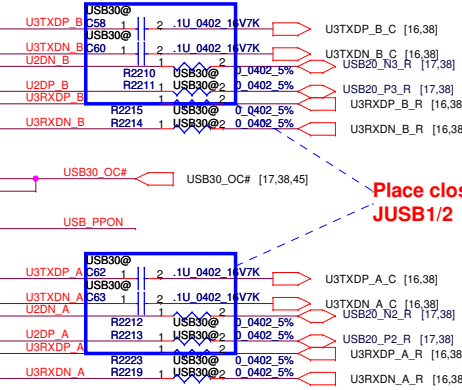
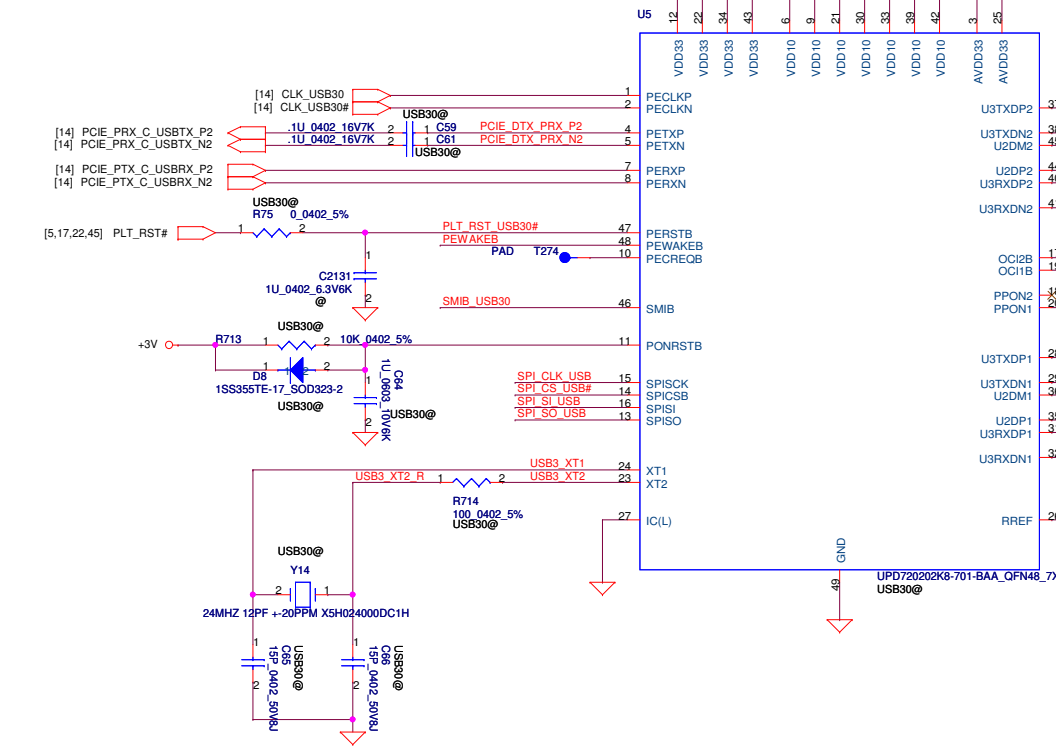
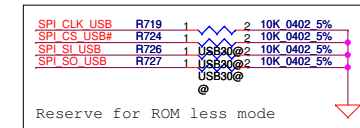
+3VALW to +3V Transfer



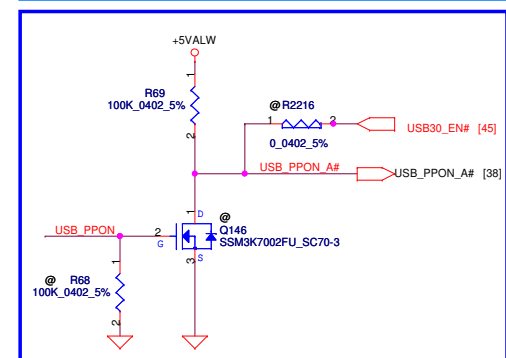
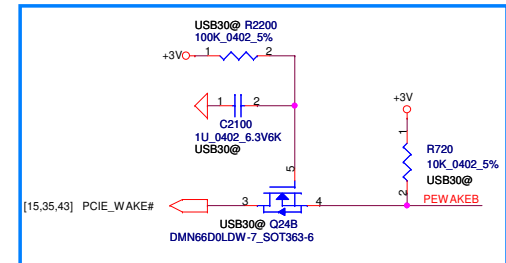
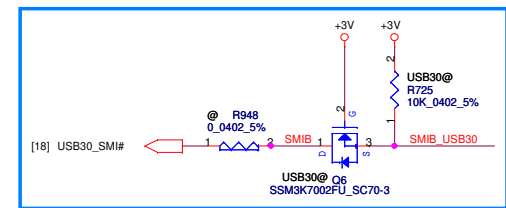
+1.5V to +1.05V Transfer



Follow Vendor recommend.



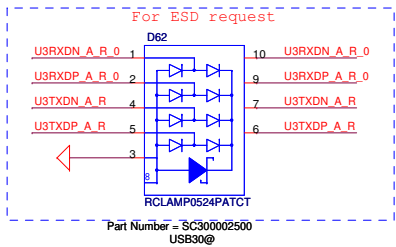
Place close to JUSB1/2



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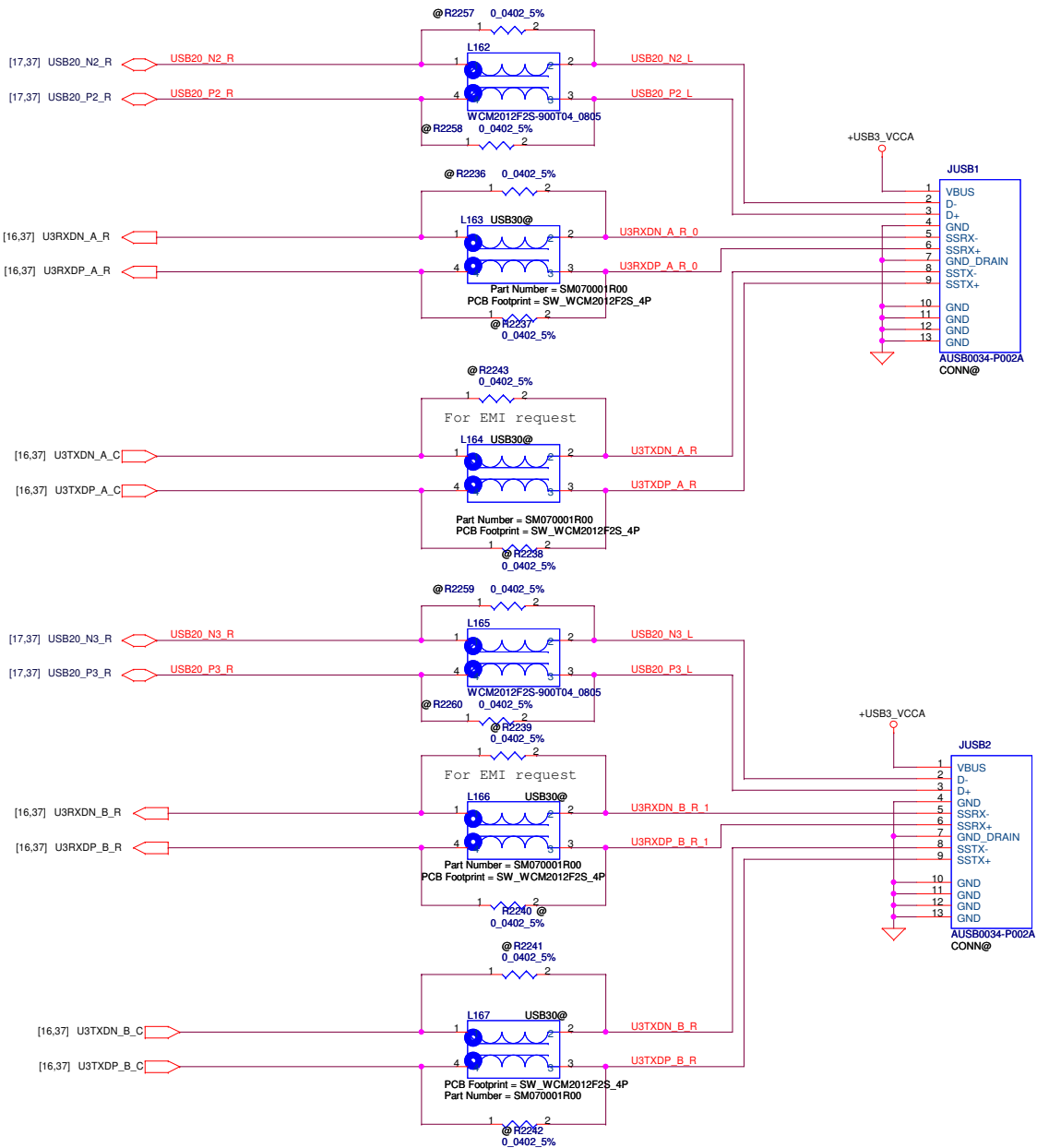
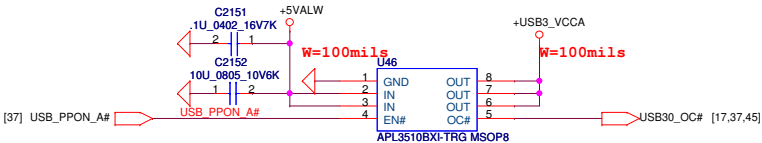
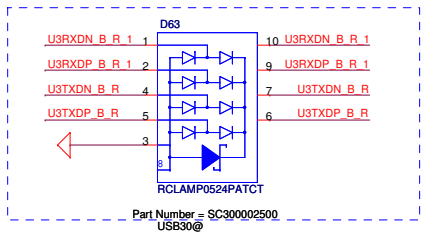
20101118 modify
BOM USB30@->
Normal (EMI part)

V0.4 : SC300000T10 change to SC300002500

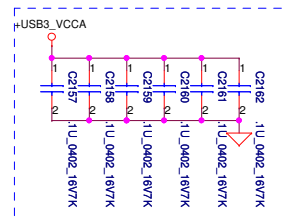


20101118 modify
BOM USB30@->
Normal (EMI part)

V0.4 : SC300000T10 change to
SC300002500 For ESD request

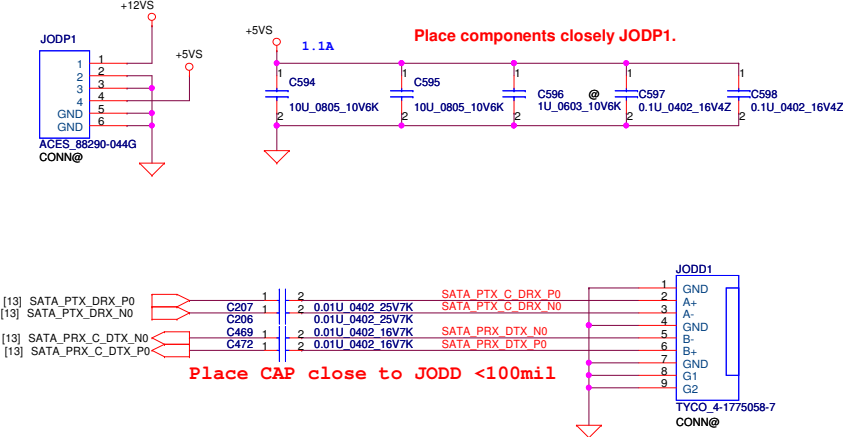


For EMC request 0627

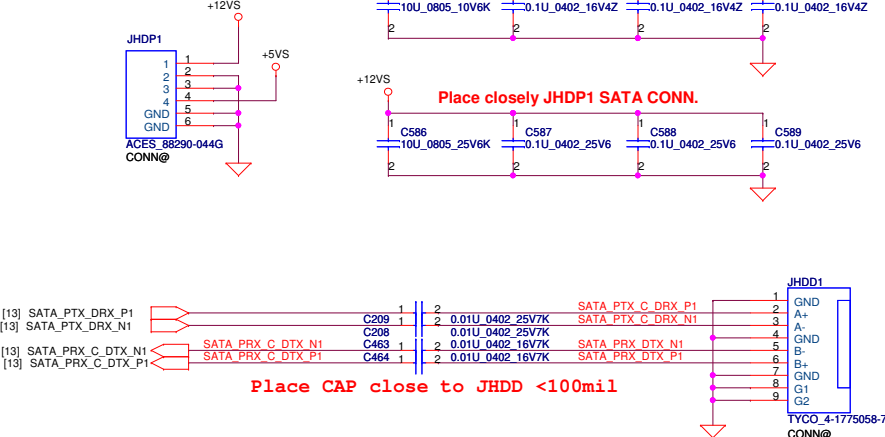


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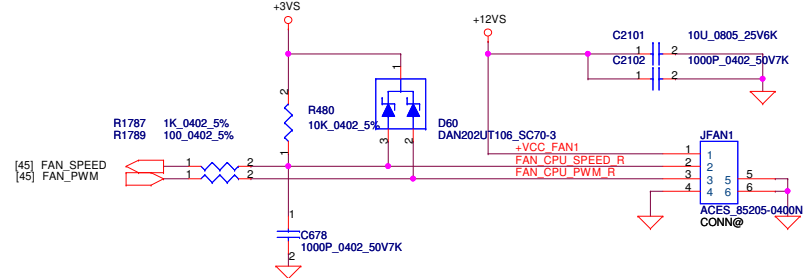
SATA ODD Conn

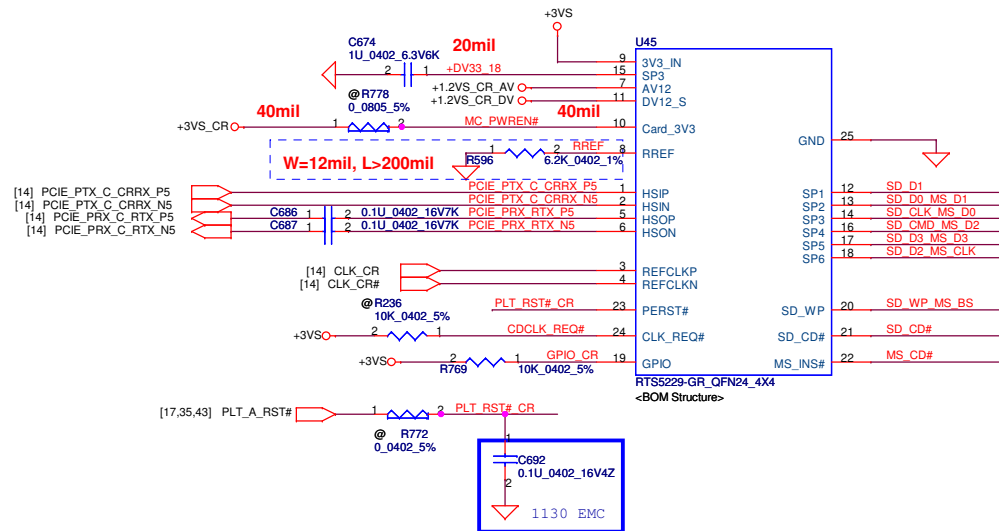
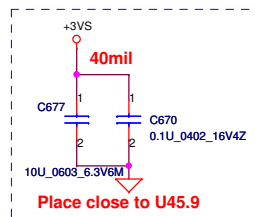
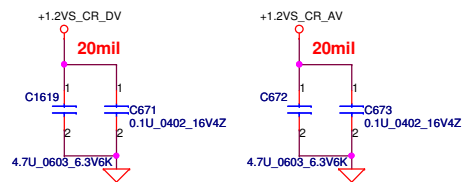


SATA HDD Conn.

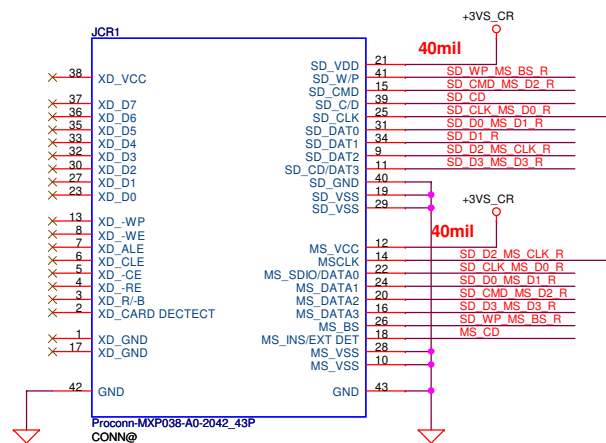
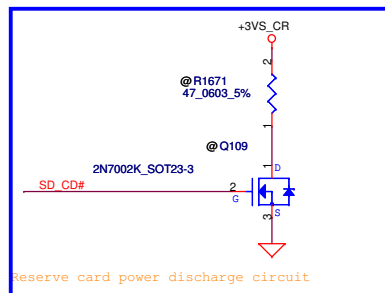
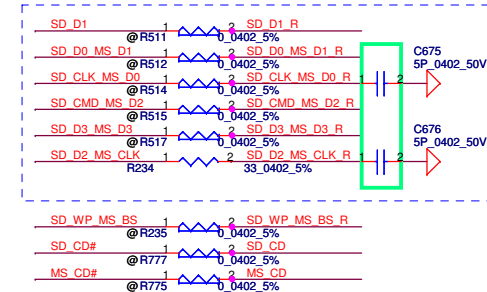


FAN Control Circuit

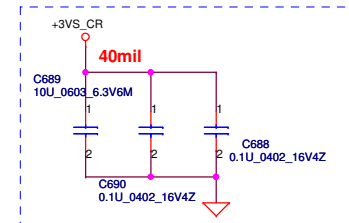




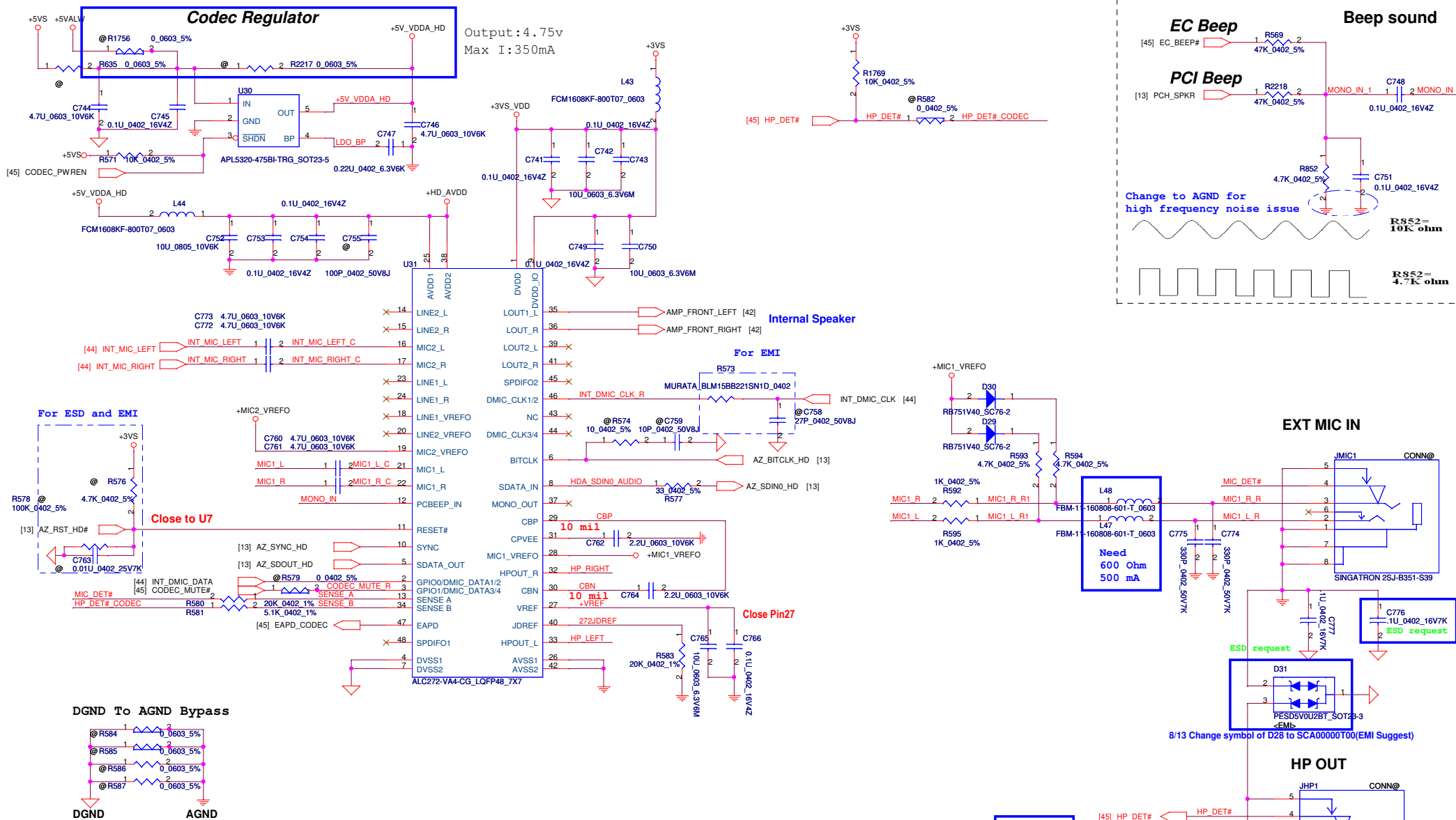
Length of per trace 2inch no more 2 via mismatch trace length <100mil 50ohm +-15% impedance.



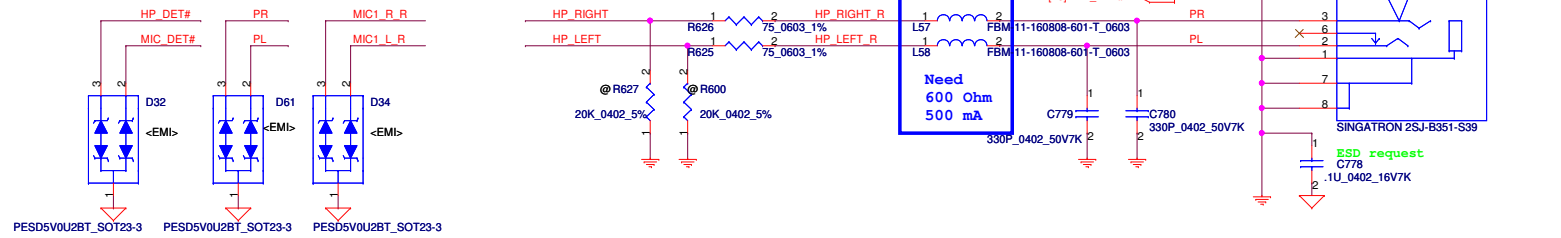
Place close to JCR1



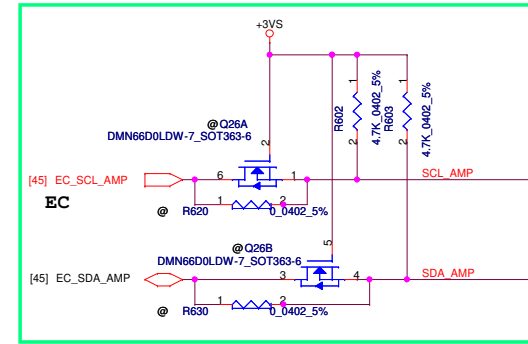
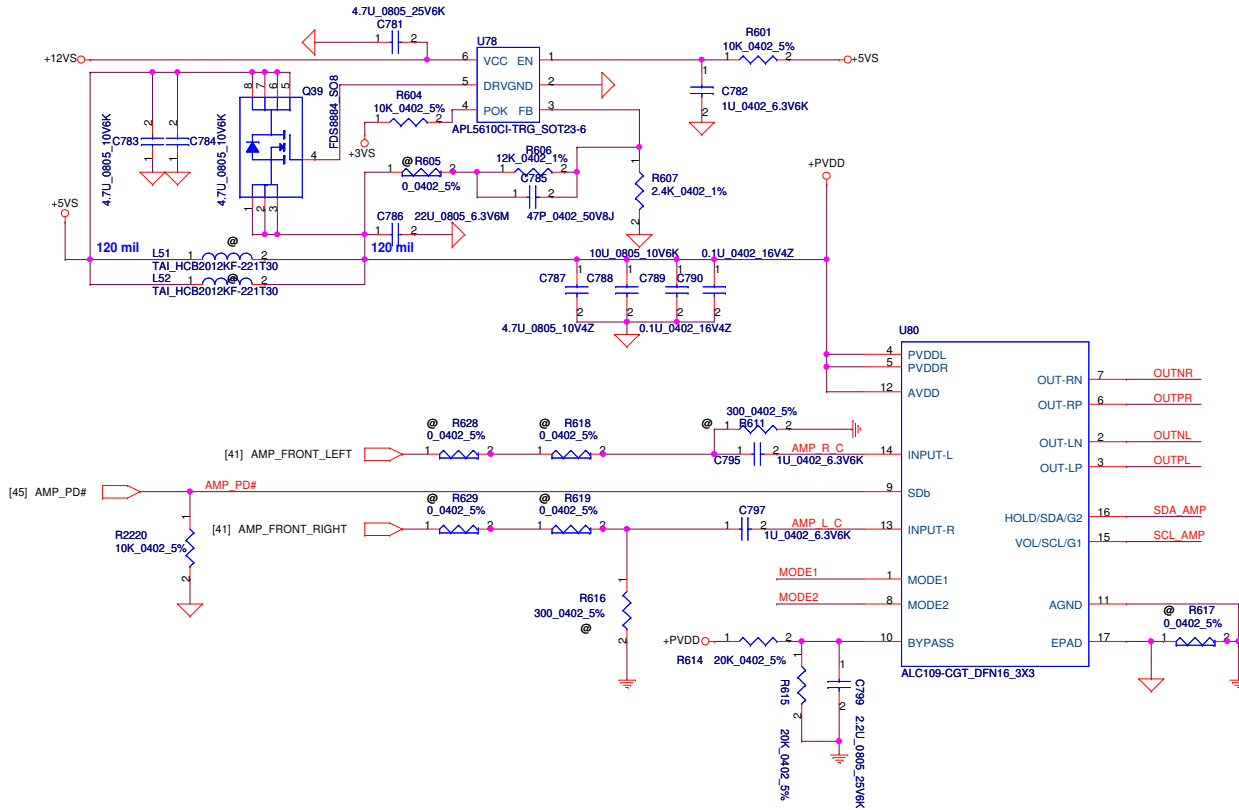
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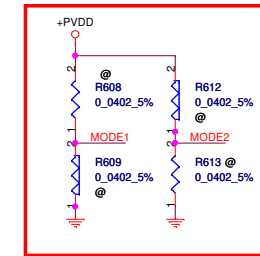
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	LOUT2 (PIN 39, 41)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	10K	
	5.1K	HP-OUT (PIN 32,33)



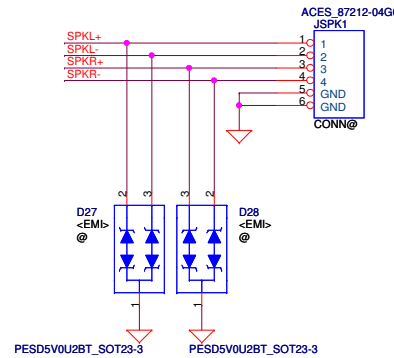
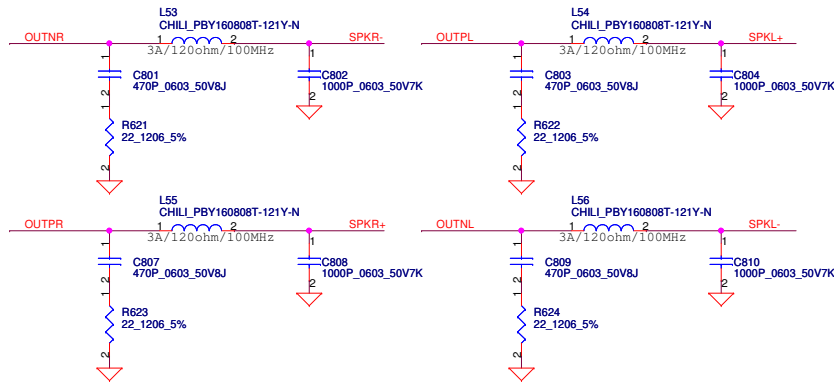
Vo=0.8 (1+R606/R607)
Output:4.8V
Max I:7.5A



Mode selet: I2C

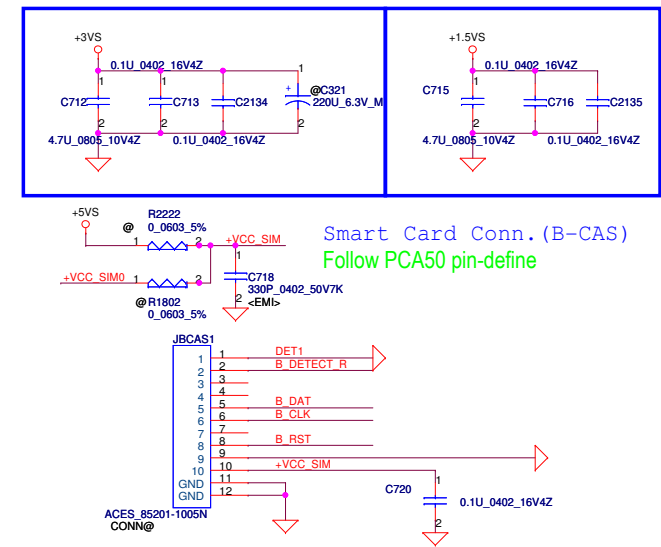
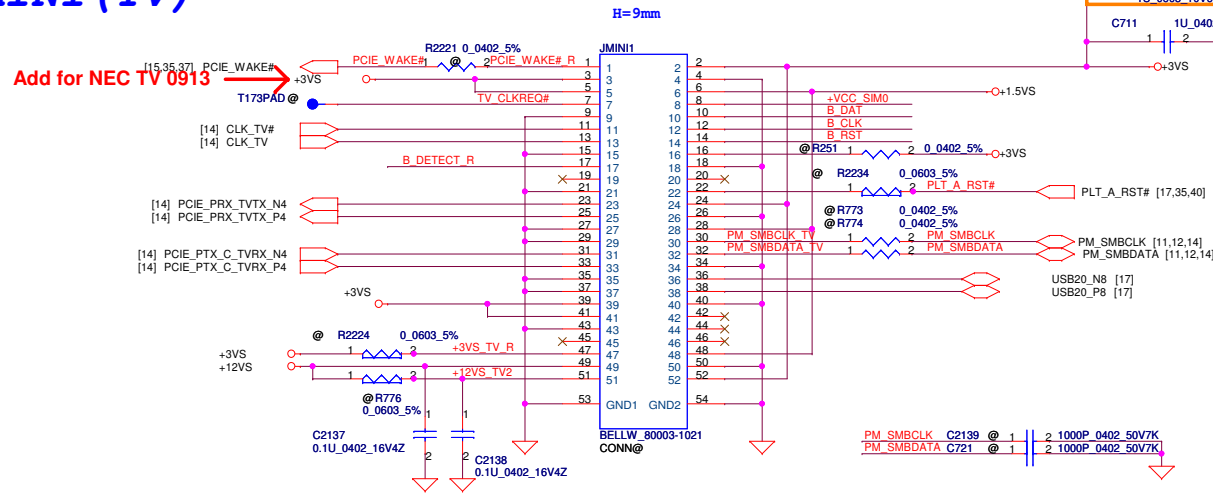


Model1	Model2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold



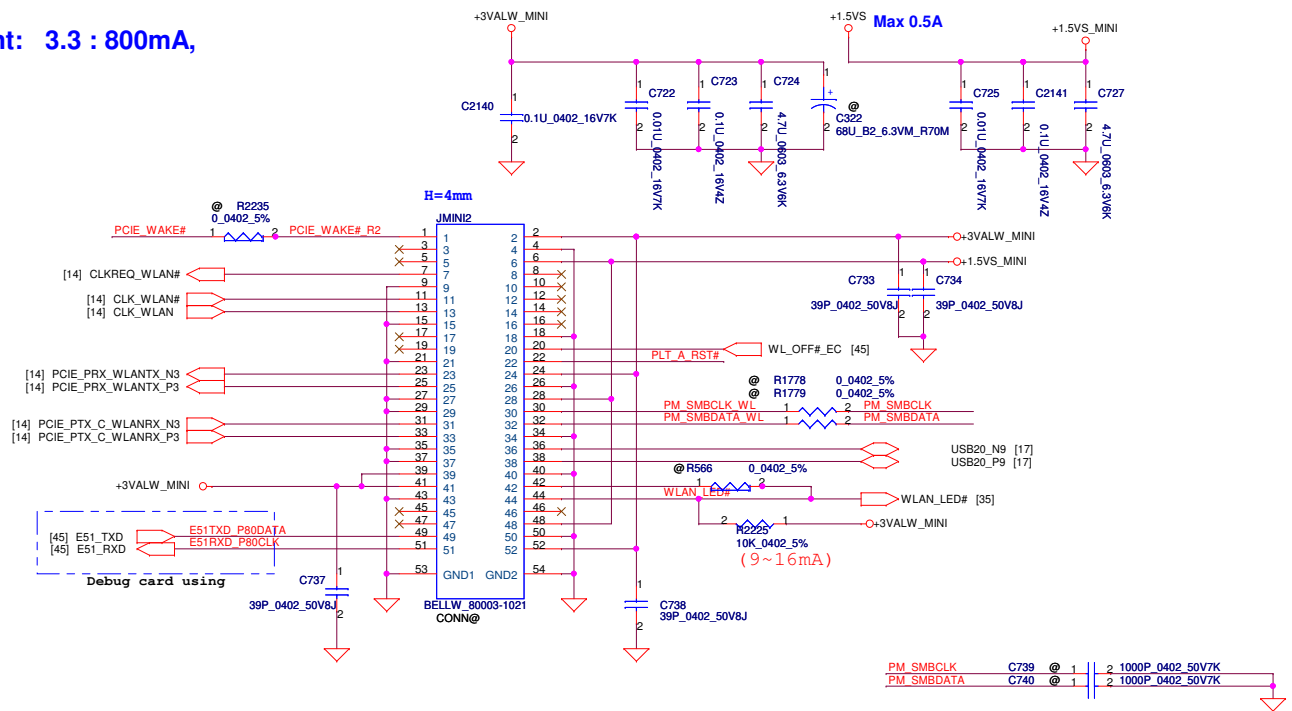
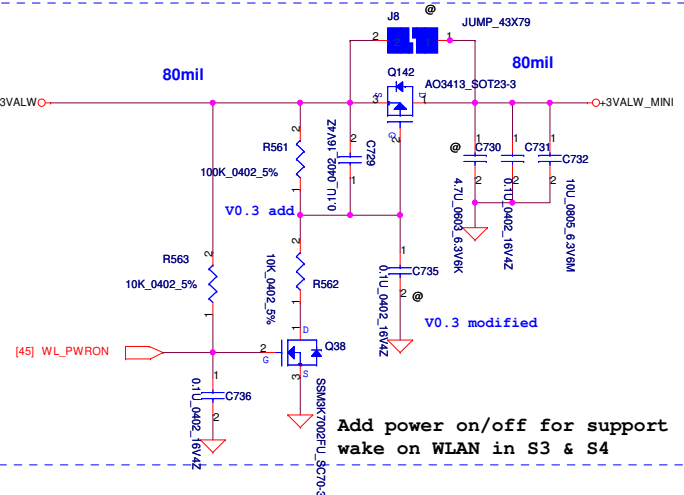
MINI (TV)

Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA



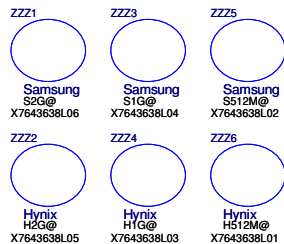
WLAN

Mini Card Slot 2--- WLAN Current: 3.3 : 800mA,

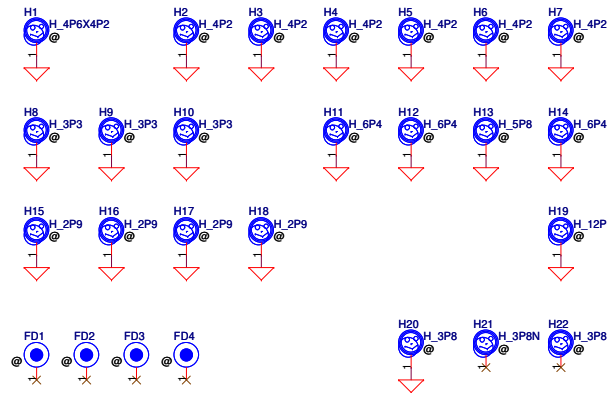


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				PCle-WLAN/TV_B-CAS					
				Size		Document Number		Rev	
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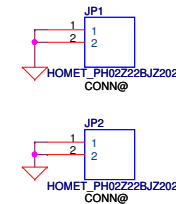
ISPD



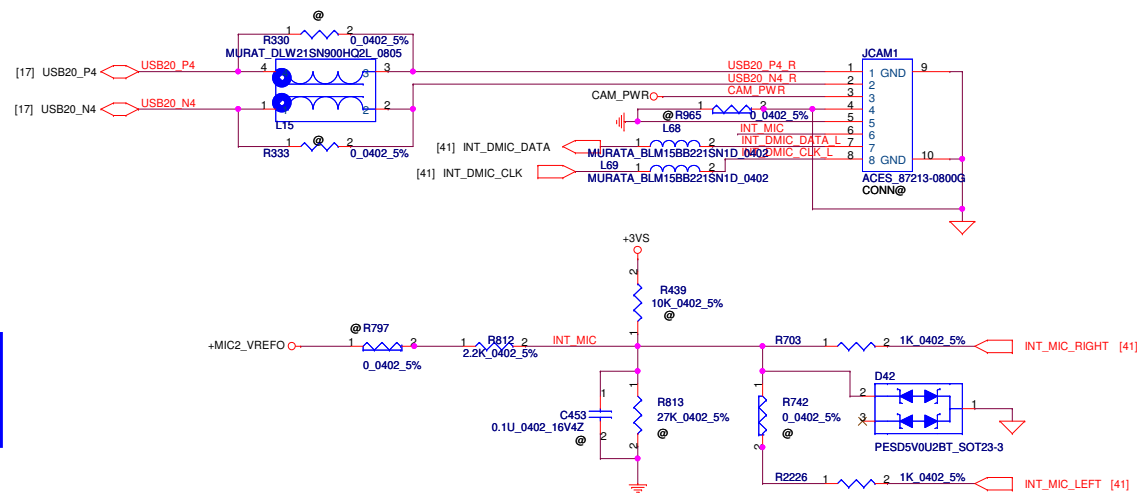
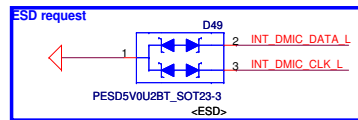
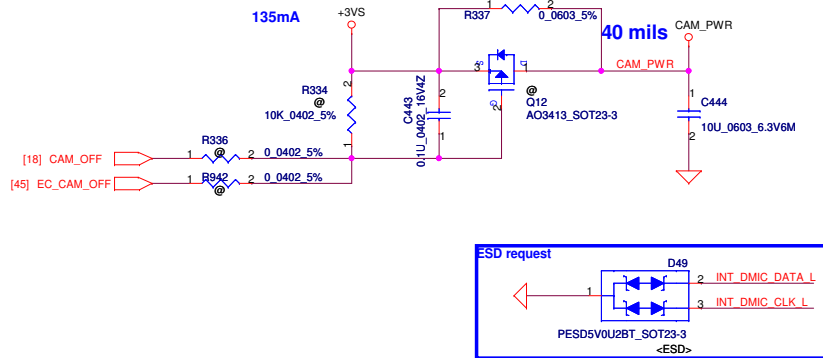
Screw Hole



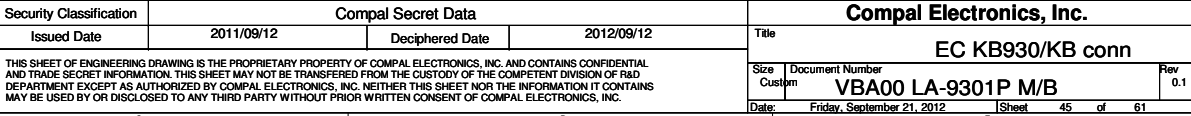
PCH heat sink



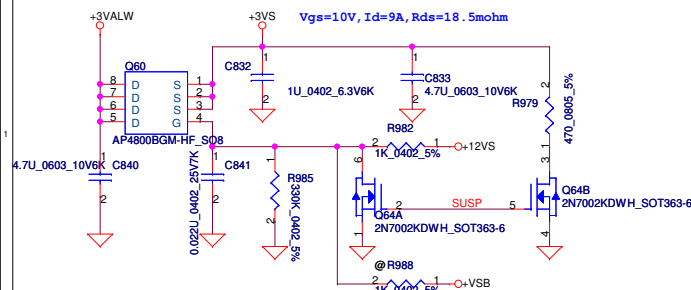
WebCam+Digital Mic



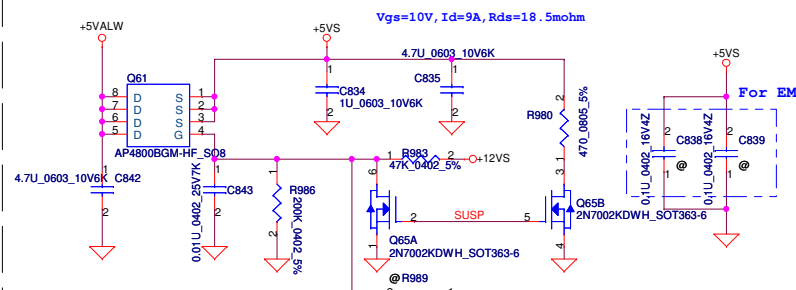
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Issued Date	2010/10/1	Deciphered Date	2011/11/01	Size	Document Number
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				VBA00 LA-9301P M/B	
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				Rev	1.0



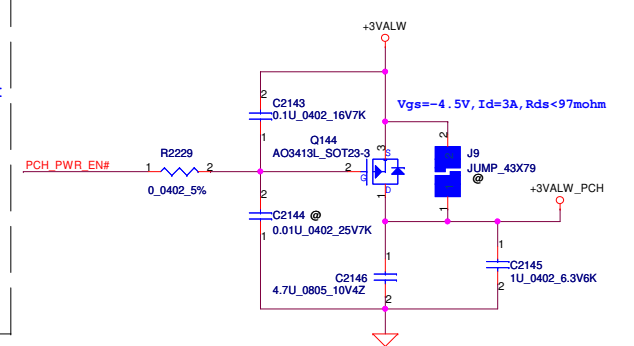
+3VALW TO +3VS



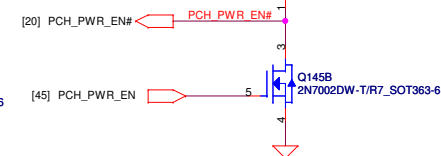
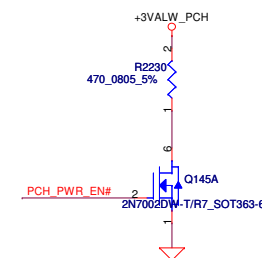
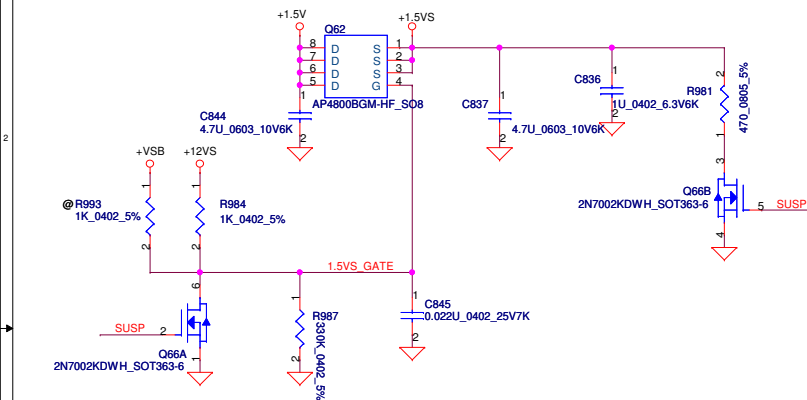
+5VALW TO +5VS



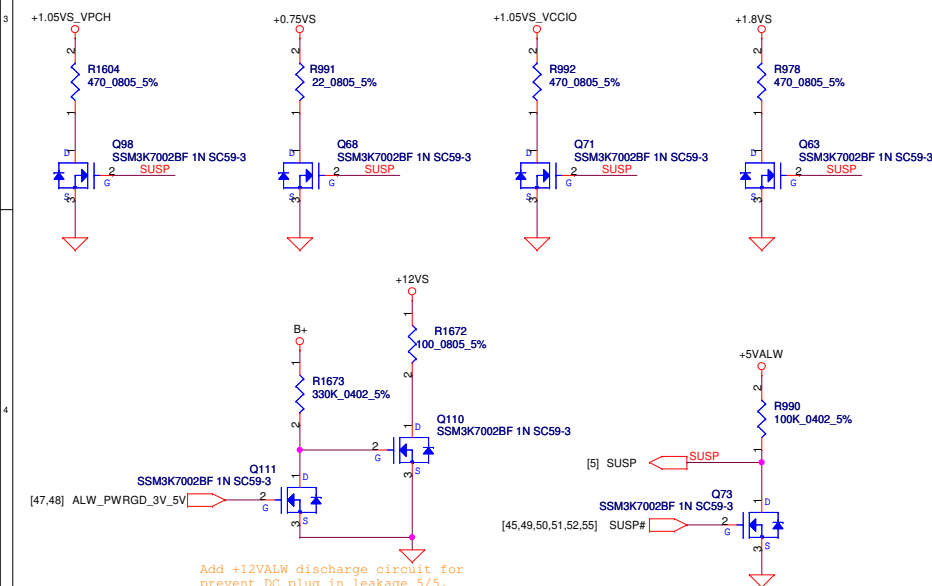
+3VALW TO +3VALW_PCH



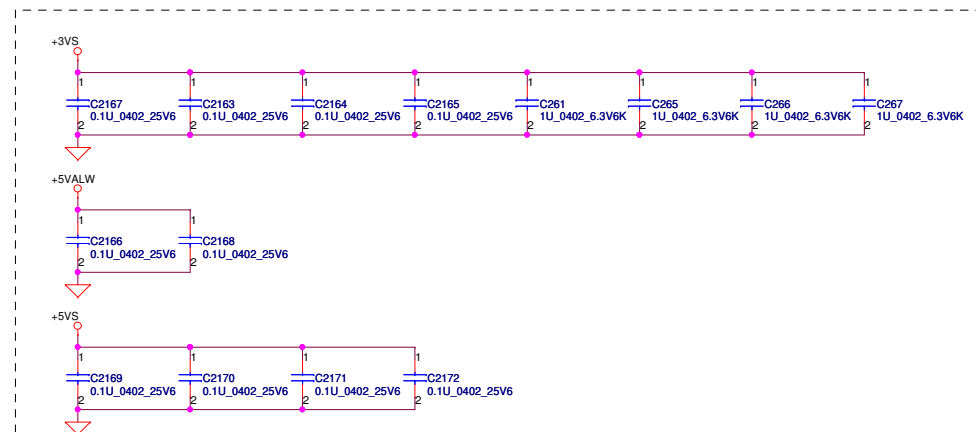
+1.5V to +1.5VS



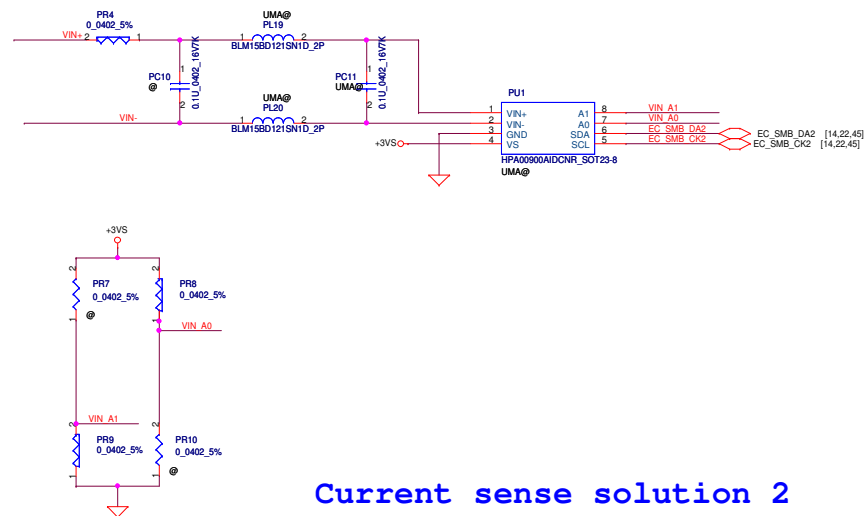
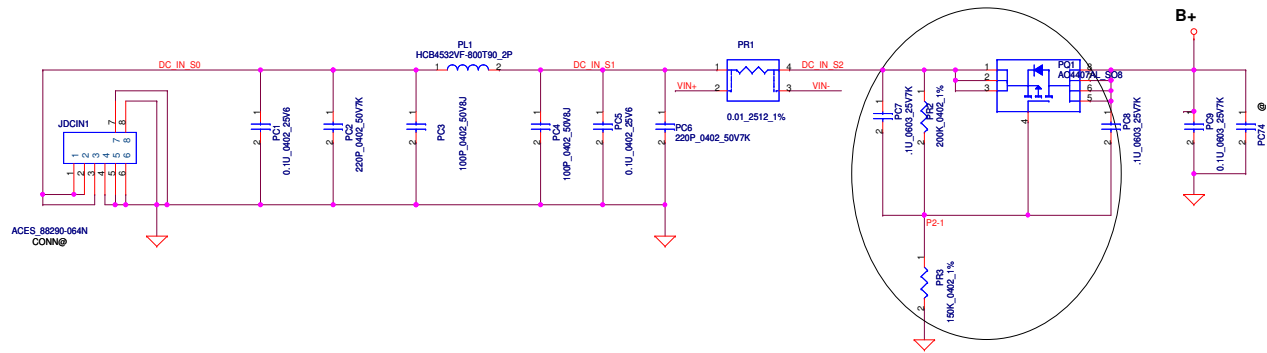
Discharge circuit



For EMI-0629

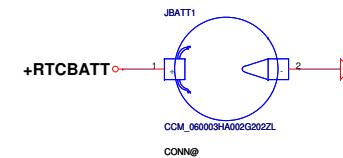
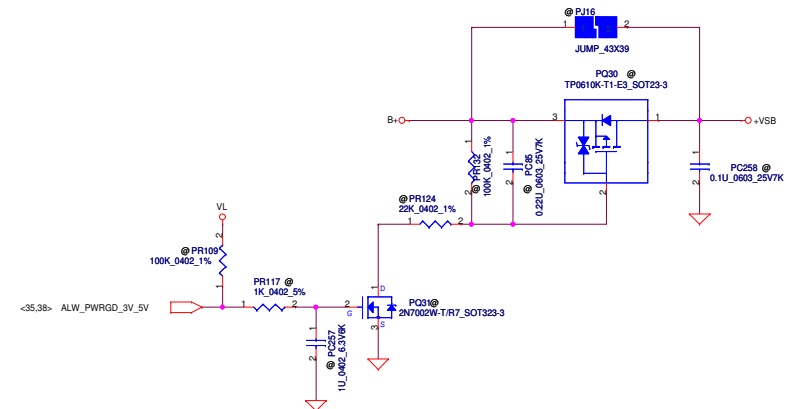


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				Size	Document Number	Rev
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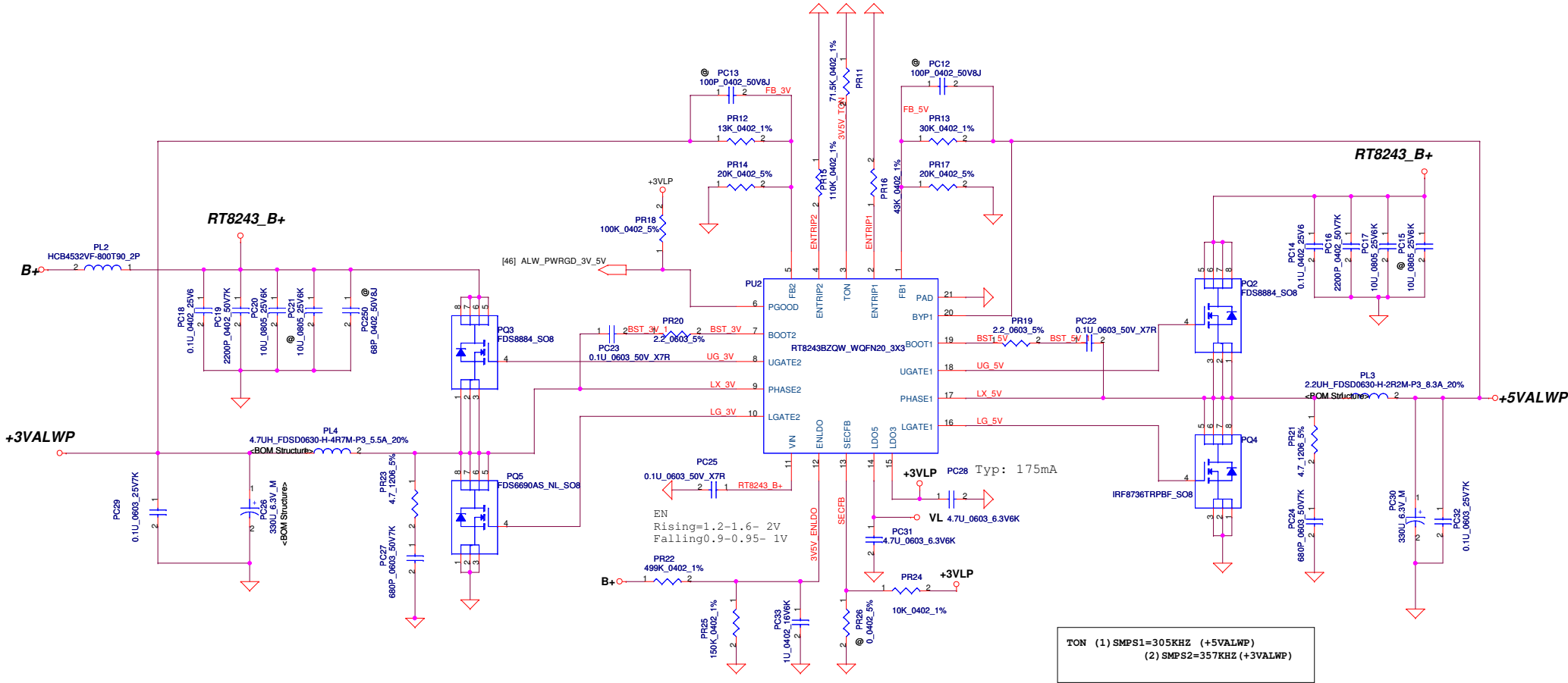


Current sense solution 2

Ventura for CPU side
slave address : 1000001
please placemnet near R-sense

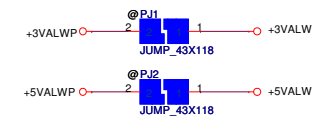


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				DCIN			
				Size		Document Number	
				VBA00 LA-9301P M/B		0.4	
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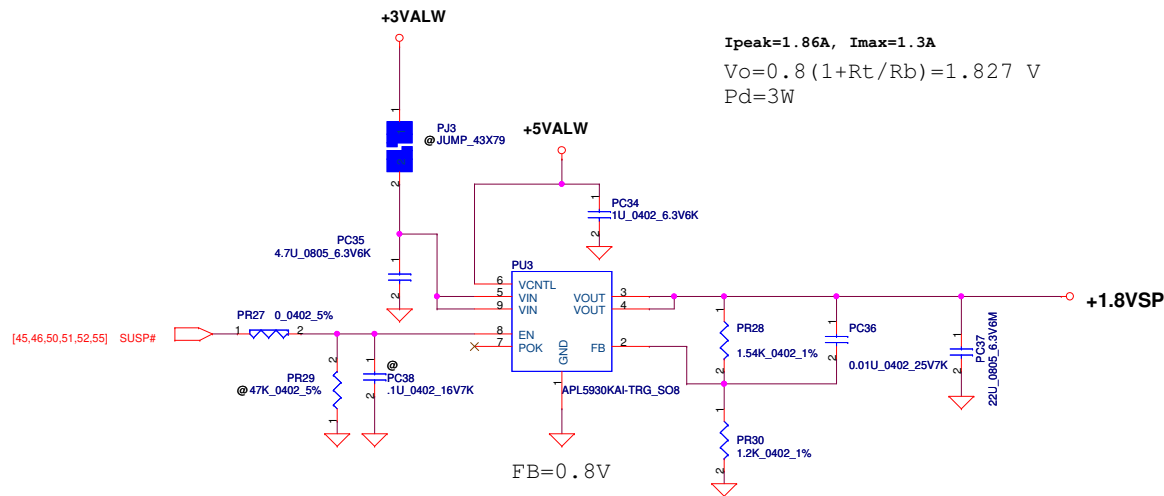


+3.3VALWP
 $I_{peak}=6.68A$; $1.2I_{peak}=8.025A$; $I_{max}=4.68A$
 $f=375KHz$, $L=4.7UH$
 $R_{dson}=12m\sim 15m\ ohm$
 $1/2\Delta I = 1/2 * (19.5-3.3) * (3.3/19) / (375KHz * 4.7UH) = 1.48/2 = 0.816A$
 $I_{ocp}=8.01\sim 10.1A$ ($4.26A > 3.895A \rightarrow ok$)

+5VALWP
 $I_{peak}=8.563A$; $1.2I_{peak}=10.25A$; $I_{max}=6A$
 $f=300KHz$, $L=2.2UH$, $R_{entrip}=64.9k\ ohm$
 $R_{dson}=5.5\sim 6.8m\ ohm$
 $1/2\Delta I = 1/2 * (19.5) * (5/19) / (305KHz * 1UH) = 2.77A$
 $I_{ocp}=10.6\sim 12.8A$ ($10.6A > 10.25A \rightarrow OK$)



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				Deciphered Date				PWR- 3VALWP/5VALWP			
				2014/12/31				Size			
								Document Number			
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								Wednesday, September 26, 2012			
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I_{max}=6.2A

I_{peak}=8.8A

ESR=14 mohm

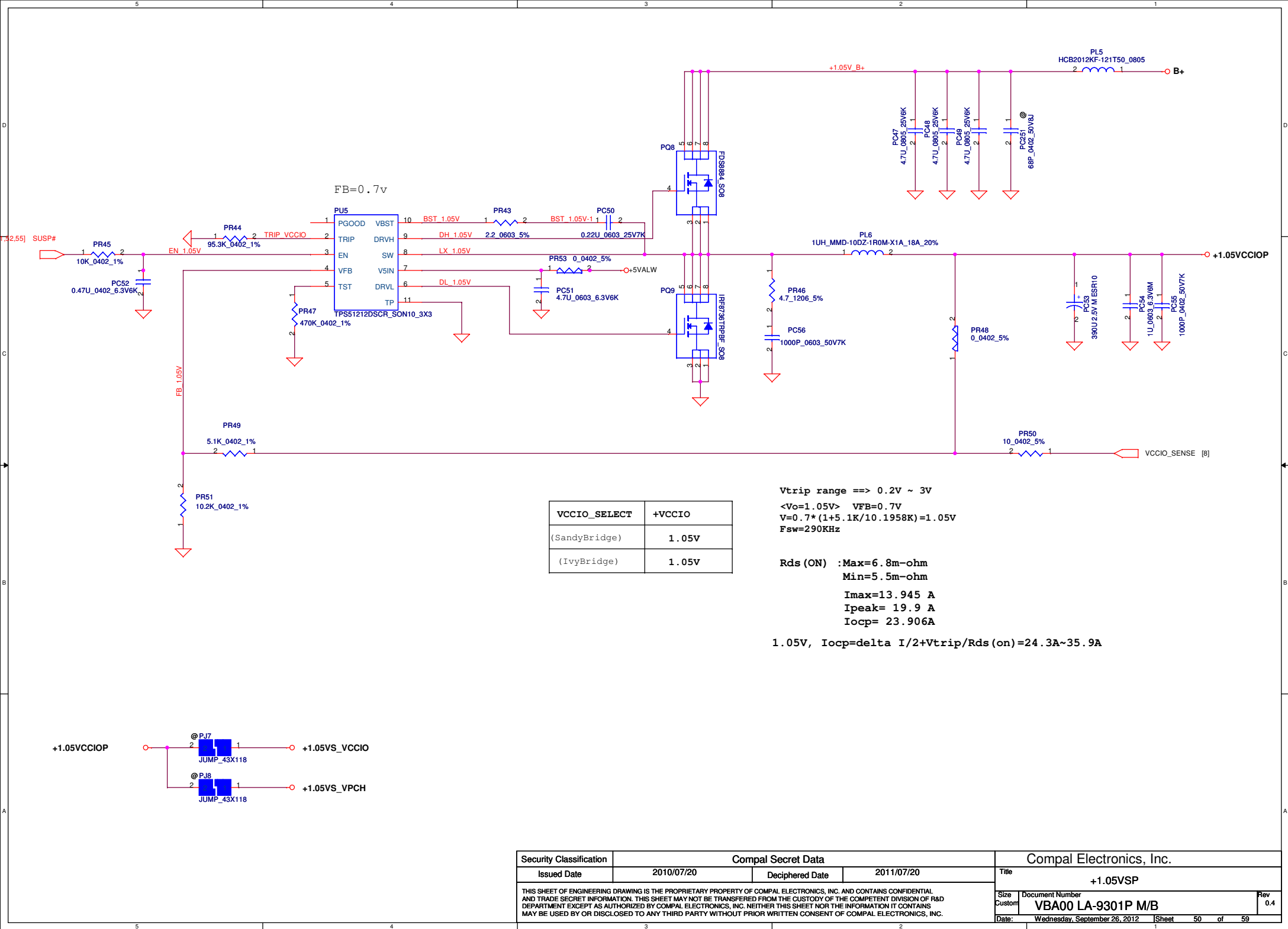
V_o=0.8(1+R_t/R_b)=0.928 V

P_d=2.5W

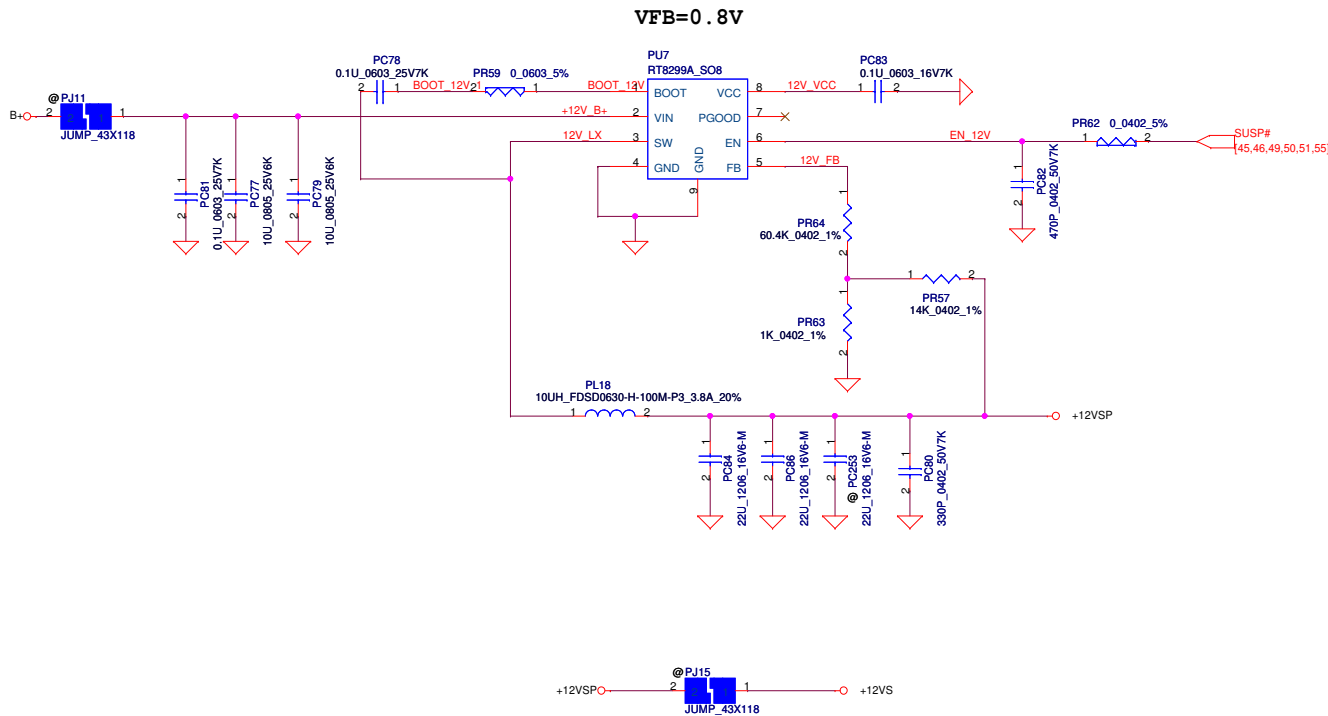
VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)

Default

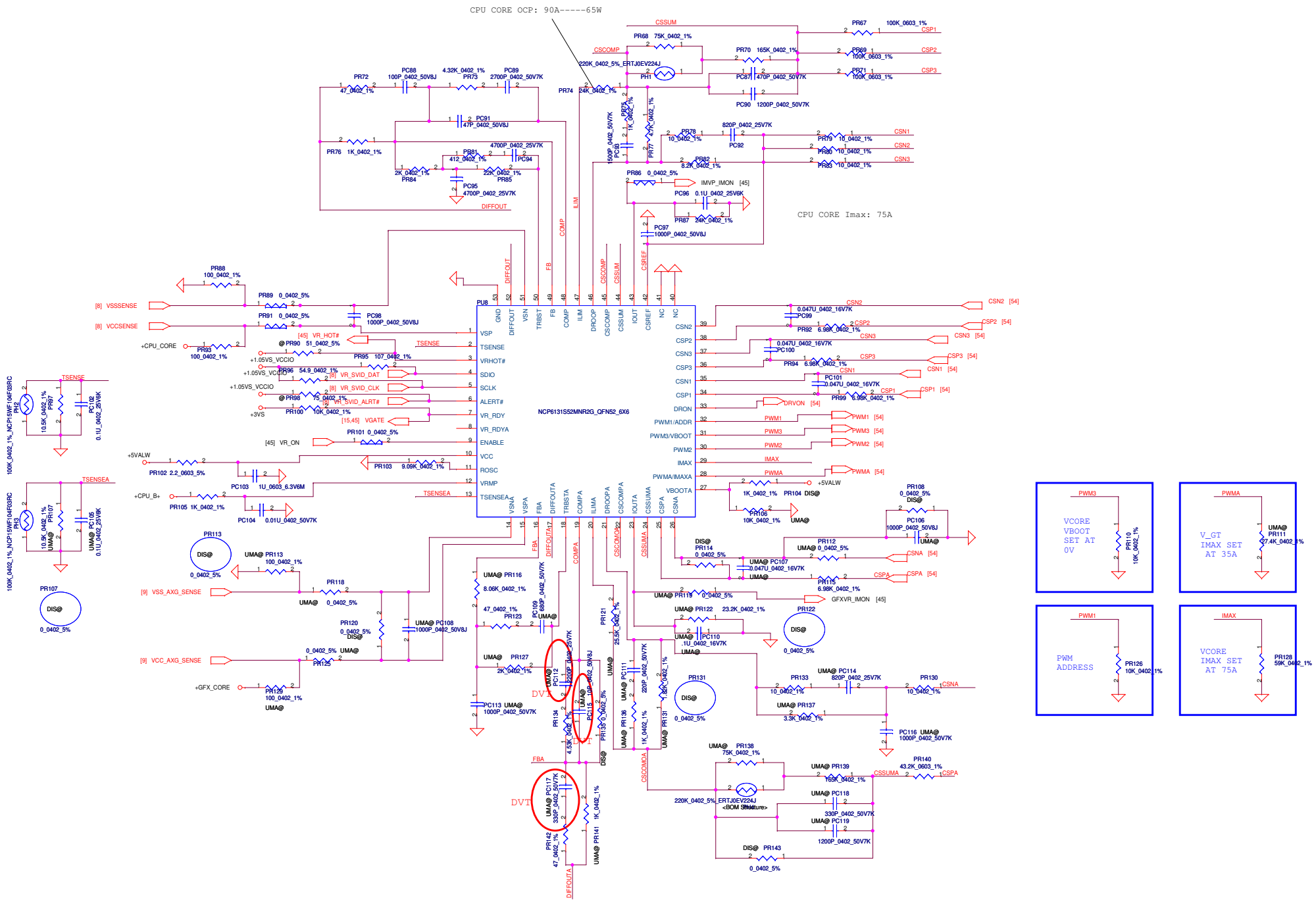
Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2010/07/20		Deciphered Date		2011/07/20		Title							
								+VCCSA/+1.8VSP							
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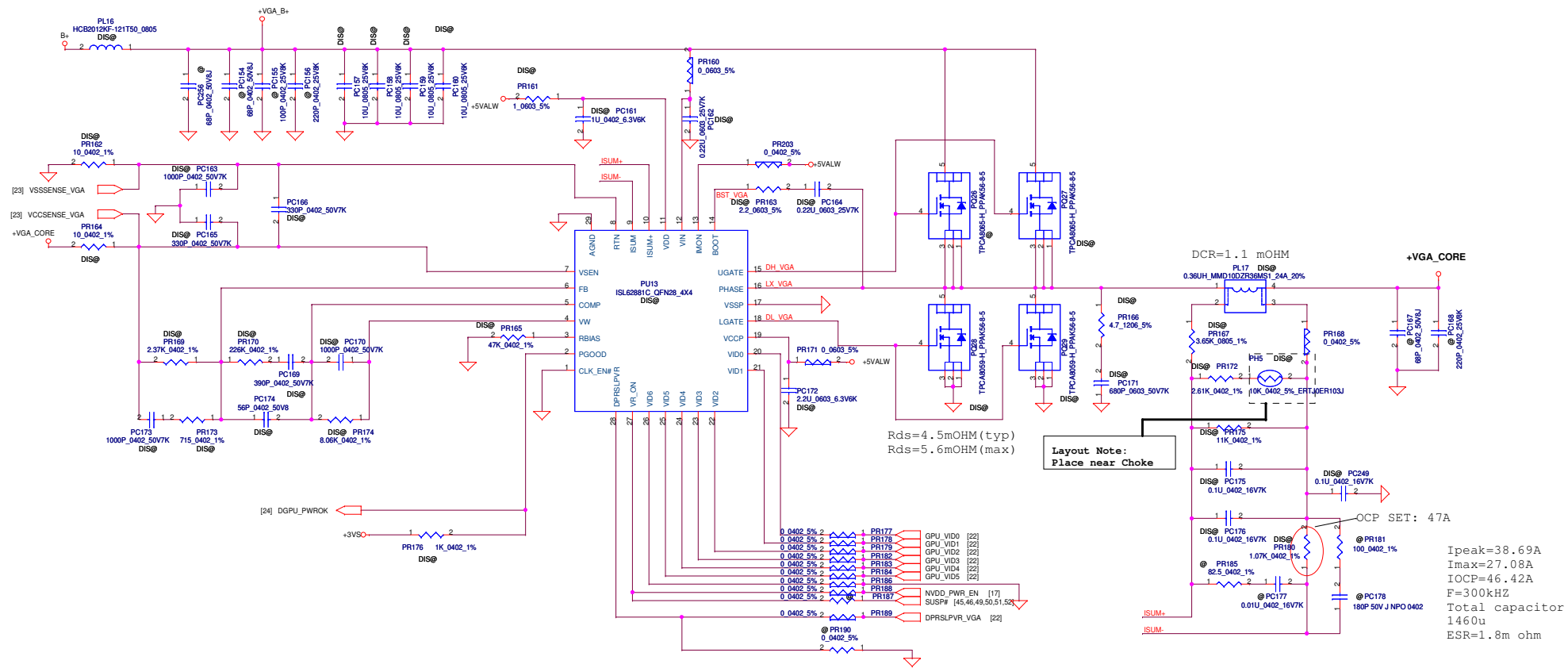
+1.2VS
 $I_{peak}=2.7A$; $I_{ocp}=3.5A\sim 5.8A$; $I_{max}=1.89A$; $L=10\mu H$
 $V_{out}=V_{fb}*[1+(R1/R2)]=0.8*[1+(30k/2.1k)]=12V$



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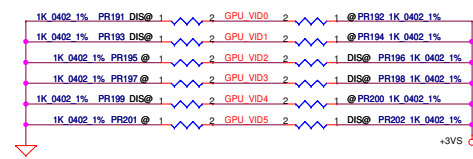
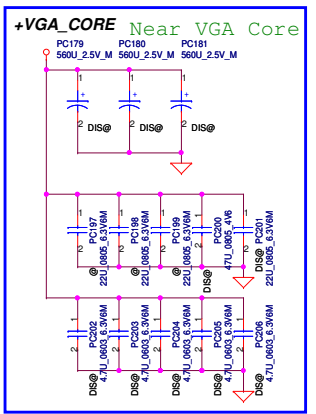
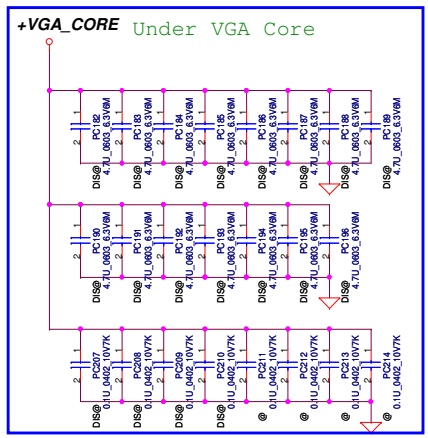


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Deciphered Date		2011/07/20		CPU CORE 1	
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Layout Note:
Place near Choke

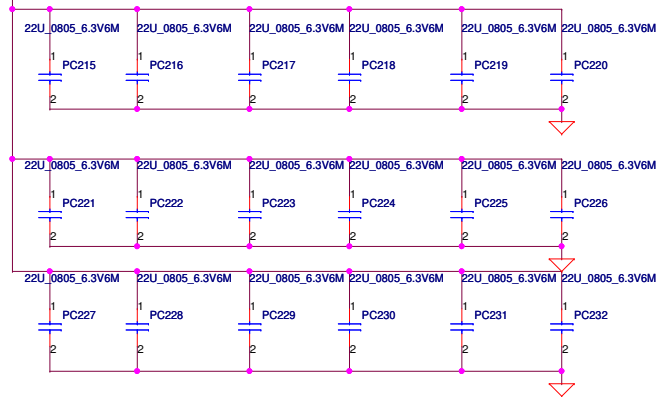
Ipeak=38.69A
Imax=27.08A
IOCP=46.42A
F=300kHz
Total capacitor
1460u
ESR=1.8m ohm



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+CPU_CORE

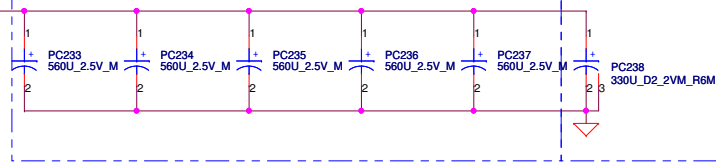
14 pcs in TOP and 4pcs in BOT Socket Cavity



+CPU_CORE

TOP Socket Edge

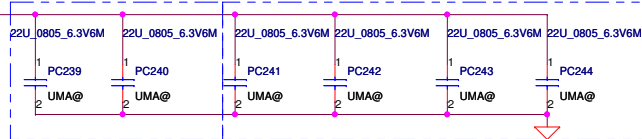
Bottom Socket Edge



+GFX_CORE

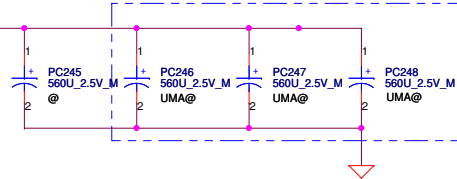
Bottom Socket Edge

Top Socket Cavity



+GFX_CORE

Top Socket Edge



NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	20120521	P55	ADD PC249	Let the Feedback loop more stable
2	20120523	P51	PC64, PC65, PC66 Change to SE093106M80	more cheaper than used to be
3	20120524	P50 P54	PR53, PR204, PR205, PR206, PR207	Add VCC resister for Lenovo design rule
4	20120528	P55	Add PC201, Remove PC199	Modify capacitor position for VGA Core
5	20120528	P55	PU2 Change to SA00005VH00	Change IC type from B to A
6	20120615	P48	Add PC31; Change PR15 to 110K ; Change PR16 to 54.9K	Modify 3.3V and 5V OCP setting
7	20120615	P51	Change PR54 to 6.81K	Modify 1.5V OCP setting
8	20120626	P50	Change PR45 to 4.7K; Change PC52 to 0.22uF	Modify 1.05V Startup timing
9	20120626	P52	Change PU7 to RT8299A Groop	Change more benifit control IC
10	20120716	P47	Change PC7 to 0.47uF ; Change PC8 to 0.068uF	Modify the inrush function
11	20120716	P52	Change PR63 to 44.2Kohm ; Change PR57 to 620Kohm	Modify the feed back resistor
12	20120726	P48;P50;P51	Change PR16 to 43Kohm ; Change PR44 to 95.3Kohm Change PR54 to 5.1Kohm	Modify the Current limit function
13	20120803	P52	ADD PR64	Modify the 12V groop of FB loop
14	20120807	P50	PR45 Change to 10K Ohm ; PC52 Change to 0.47uF	Modify the sequence of Power
15	20120825	P47	Replace PR5 PR6 by PL19 PL20 and remove PC10	Modify the part of the current monitor.

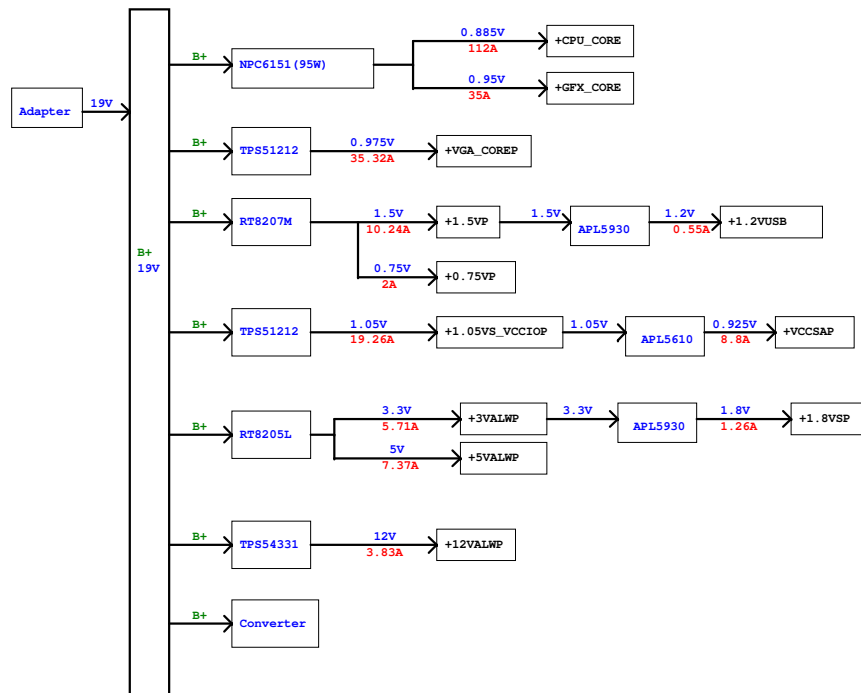
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HW PIR (Product Improve Record)

VBA00 LA-9301P SCHEMATIC CHANGE LIST

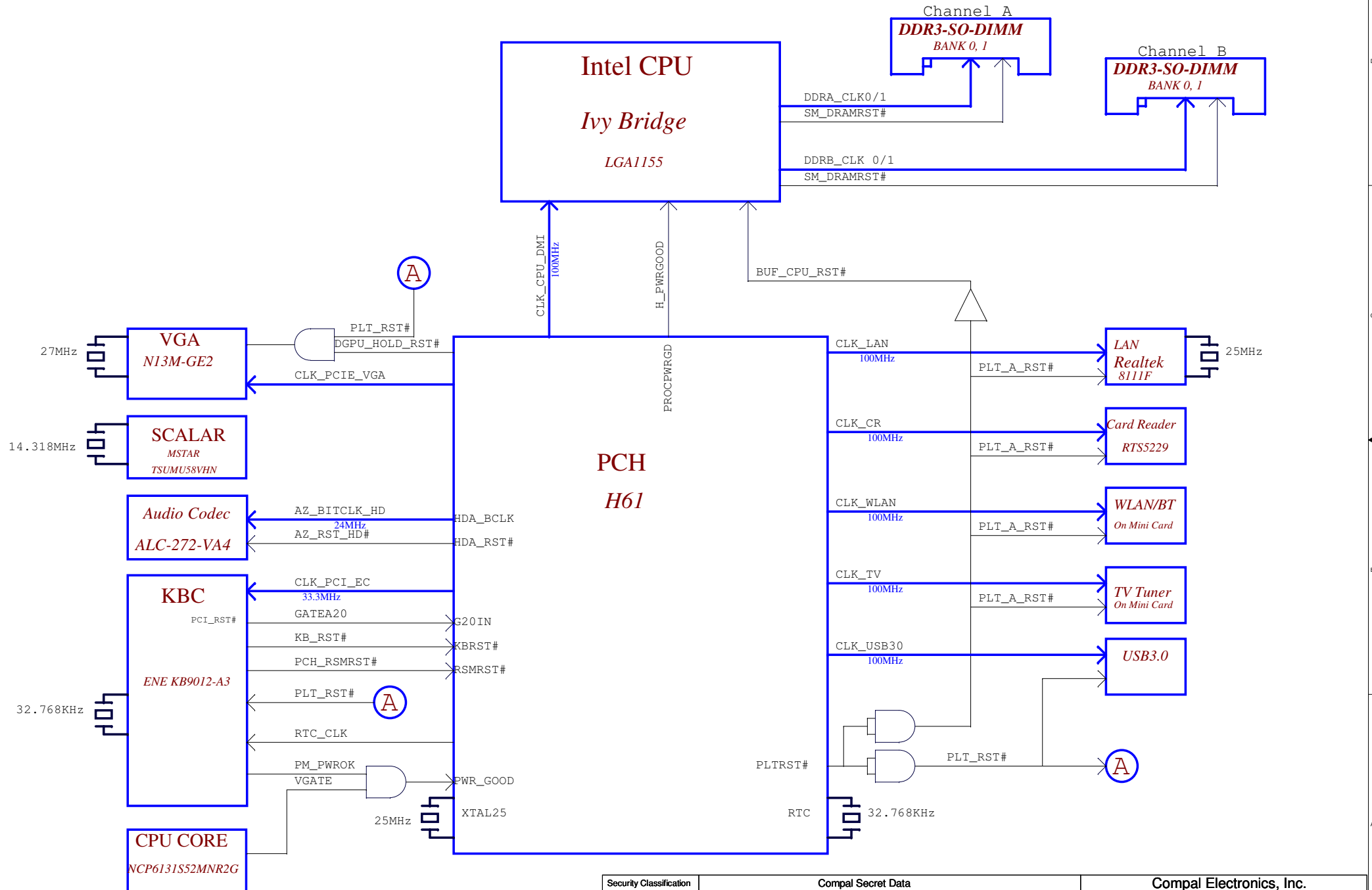
NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	20120618	P39	modify same pin define for JHP1 & JHP1	Prevent insert wrong cable.
2	20120618	P44	Add JP1/JP2 for PCH heat sink	PCH heat sink
3	20120619	P44	Change H2-H7 from 3F5 to 4P2.	ME request
4	20120621	P44	Change JCAM1 to right angle type	ME request
5	20120621	P44	Change K75 to 0ohm C2131 unmount.	USB 30 yellow mark issue
6	20120626	P13	Change JCMOS2 to 3 pin	
7	20120626	P46	Change R982 to 1K	remove CPU_RST# glitch
8	20120626	P46	Reserve +VSB power	Reserve for timing control
9	20120626	P23	Change GPU HDMI OUT data pin	For HDMI OUT issue.
10	20120626	P22	Connect GPU reset to PLT_RST# directly.	No OPTIMUS needs.
11	20120626	P18/11	Reserve PCH QP10 57/60 (sus power).	For scaler FW update
12	20120627	P38	Add 6 0.1uF CAP on +USB3_VCCA	For EMC request
13	20120627	P45	Connect JCMOS2 pin1/2 to EC_CRISIS and EC_CRISIS_KSO0	For Crisis and clear CMOS use.
14	20120628	P14	CLKREQ_LAN# pull high to +3V_LAN	prevent leakage.
15	20120630	P35	Remove C714 @	Add 10uF CAP for LAN power.
16	20120630	P05	Remove R23 @	Follow Intel CRB
17	20120630	P13	Change U66 BIOS ROM to 1MB	
18	20120630	P13	Change C202 & C204 to 18p for 32.768 K*TAL	Follow vendor suggestion.
19	20120630	P22	Change C1910 & C1911 to 12p for 27M K*TAL	Follow vendor suggestion.
20	20120630	P24	Add GPU power discharge circuit	For sequence.
21	20120630	P16	Change C229 & C230 to 14p and 25M K*TAL to CL=12P	Follow vendor suggestion.
22	20120630	P37	Change K713 to 10K and C2100 to 1Hf	For sequence.
23	20120630	P37	Remove U7 ROM and PD SPI signal.	Combine U3 FW to BIOS
24	20120704	P45	Change R1989 to 33K	For BID (BOM memo)
25	20120704	P45	Remove R2059	S_ENVID no need input to EC (BOM memo)
26	20120705	P36	Change C349 from 1000p to 0.022uF.	Panel timing finetune (BOM memo)
27	20120711	P05	Delete XDP test point T258, T259.	For ESD
28	20120711	P10	Delete CFG test point T236, T15-T27.	For ESD
29	20120711	P46	Add C2167-C2172	For EMI(BOM memo)
30	20120713	P42	Change AMP PU/PD resistor to 0ohm.	For AMP Gain control(BOM memo)
31	20120713	P45	Remove R1999/R2000	For AMP Gain control(BOM memo)
32	20120712	P10	Remove R1576-1577, R1664,	For ESD
33	20120712	P08	Remove R56 100 Ohm	For ESD
34	20120713	P42	Remove Q26 and add R620/R630	For AMP Gain control
35	20120713	P42	Swap U80.15 and U80.16	For AMP Gain control
36	20120724	P46	Change 1.5VS switch from P-MOS to N-MOS	For 1.5VS drop
37	20120724	P16, 37, 38	Add 0ohm for USB30 Rx P/N	For separate PCH and Reneses USB30 Rx signal
38	20120724	P37	Change K715 from 1.6K to 1.5K	For enhance high speed eye
39	20120724	P35, 38	Change USB PWR SW to MSOP package, add 10u for input power	Follow Compal standard
40	20120725	P36	Change JCON1 to vertical type	ME request
41	20120725	P44	Change screw hole size	ME request
42	20120726	P09	Add 3 pcs 22uF cap on +GFX_CORE	For ESD
43	20120807	P05	Add 4 pcs 47nF cap on XDP_DBRESET#	For ESD
44	20120807	P05, 18	Add 3 pcs 47nF cap on HLPWRGOOD	For ESD
44	20120726	P05	Add 1 pcs 47nF cap on HLCATERR#	For ESD
45	20120726	P05	Reserve 1 pcs 47nF cap on HLPBC1	For ESD
46	20120726	P45	Change R1989 to 56K	For Board ID
47	20120727	P44	Change Screw hole	For ME request
48	20120727	P13	Change BIOS ROM footprint	For correct footprint
49	20120727	P34	Add HDMI repeater	For EMI
50	20120730	P05	Reserve 2 pcs 47nF cap on HLPBC1	For ESD
51	20120730	P05	Reserve 1 pcs 47nF cap on Xdp_Dbreset#	For ESD
52	20120730	P01-P45	Change 0ohm to short pad.	For Cost reduce
53	20120802	P37	Un-mount R727.	For USB3.0 device show exclamatory point issue.
54	20120803	P47-57	Update power sch.	For USB3.0 device show exclamatory point issue.
55	20120807	P13	Change V1 to 2nd source	For KTC test issue
56	20120807	P04	Add HDMI0# in note list.	For load BOM
57	20120807	P46	Mount +3VALW TO +3VALW_PCH switch	For power Erp lot6
58	20120807	P41	Change CODEC LDO to APL5320-475B1-TRG	For LDO issue
59	20120810	P34	Change Q25 PN to common PN	For PUR request (BOM memo control)
60	20120810	P34	Change Q25 PN to common PN	For PUR request (BOM memo control)
61	20120810	P05	Unmount R1/R2/R3/R4/R6/R23	For ESD request (BOM memo control)
62	20120810	P05	Change C77/79/80/81 to 5P	For ESD request (BOM memo control)
63	20120810	P46	Unmount C2144 and change R2229 to 0 ohm	For Erp lot 6 (BOM memo control)
64	20120824	P09/13/24/37/41/42	R65, 140, 143, 144, 145, 146, 2130, 2131, 710, 721, 579, 609, 612	For 0 ohm short pad
65	20120824	P32	Mount R445 10K ohm	For Converter team request
66	20120824	P45	Change R1999-R2003 PU to +3VS	For power Erp lot 6
67	20120824	P46	Change C2144 to GND	Reserve
68	20120824	P33/45	Reserve EDID flash control by EC and PD resistor	Reserve EDID WP control by EC
69	20120827		Update power 0 ohm resistor	For 0 ohm short pad
70	20120827	P35	Remove SW3	For MP
71	20120827	P13	C202/C204 change to 16P	For KTC timing fine tune
72	20120827	P05	Remove XDP PU/PD resistor	For ESD request
73	20120827		Update power part	For ESD request
74	20120827	P05	Add test pad on XDP	For 测试
75	20120907	P05	Remove C72, C77, C78, C82 and put R22 close to U4.	For ESD
76	20120907	P46	Add C261/C265/C266/C267 on +3VS	For ESD
77	20120907	P13/45	U6 and U66 change to X76# and change BID	Combine same BIOS ROM vendor to prevent timing issue.
78	20120919	P34	Mount R643 and R642	For EMC
78	20120921	P18	Remove Q96	For PUR

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Clock and Reset Diagram



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