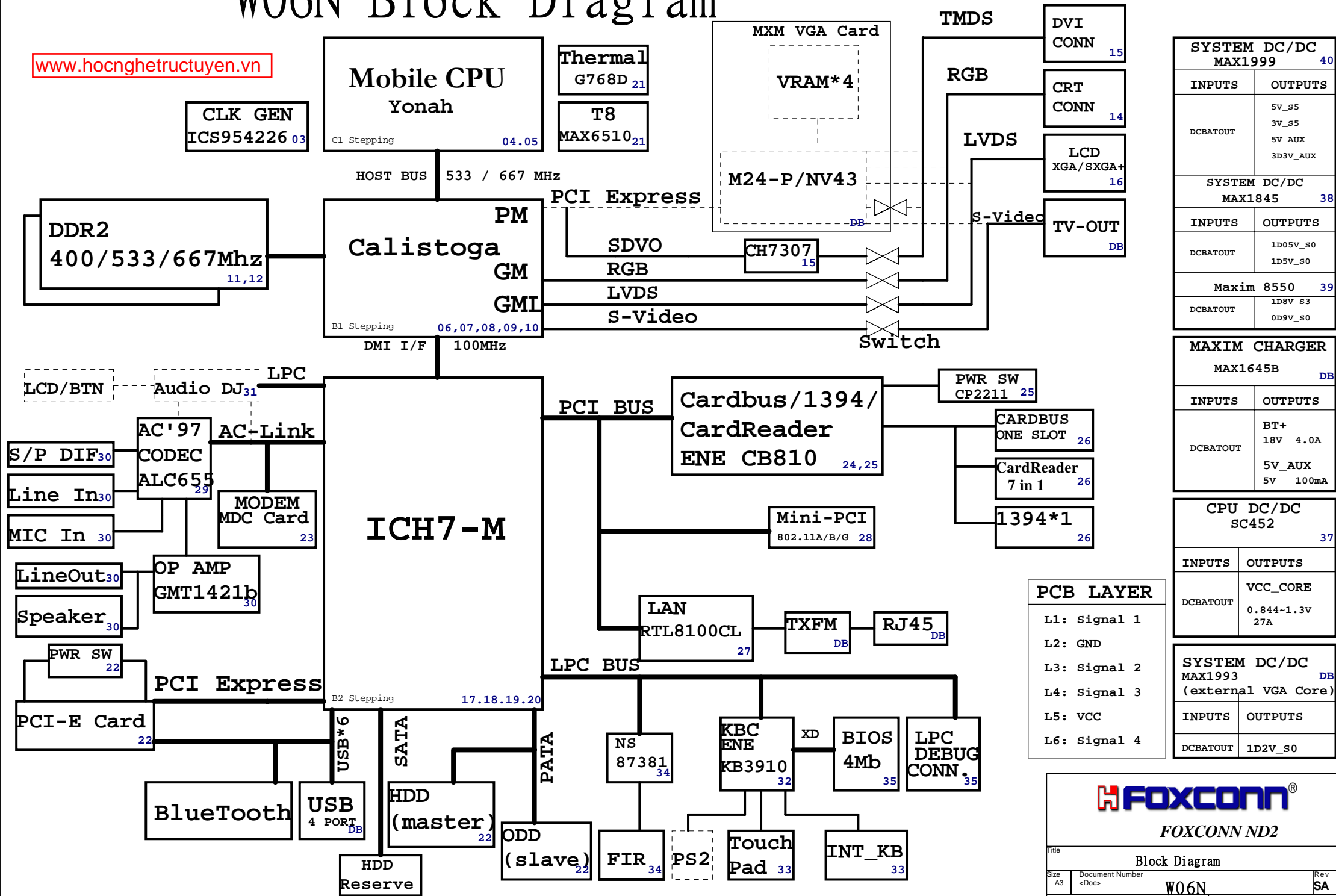


# W06N Block Diagram

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| SYSTEM DC/DC MAX1999 40 |                                      |
|-------------------------|--------------------------------------|
| INPUTS                  | OUTPUTS                              |
| DCBATOUT                | 5V_S5<br>3V_S5<br>5V_AUX<br>3D3V_AUX |

| SYSTEM DC/DC MAX1845 38 |                     |
|-------------------------|---------------------|
| INPUTS                  | OUTPUTS             |
| DCBATOUT                | 1D05V_S0<br>1D5V_S0 |

| Maxim 8550 39 |                    |
|---------------|--------------------|
| DCBATOUT      | OUTPUTS            |
| DCBATOUT      | 1D8V_S3<br>0D9V_S0 |

| MAXIM CHARGER MAX1645B DB |                                       |
|---------------------------|---------------------------------------|
| INPUTS                    | OUTPUTS                               |
| DCBATOUT                  | BT+<br>18V 4.0A<br>5V_AUX<br>5V 100mA |

| CPU DC/DC SC452 37 |                               |
|--------------------|-------------------------------|
| INPUTS             | OUTPUTS                       |
| DCBATOUT           | VCC_CORE<br>0.844~1.3V<br>27A |

| PCB LAYER |          |
|-----------|----------|
| L1:       | Signal 1 |
| L2:       | GND      |
| L3:       | Signal 2 |
| L4:       | Signal 3 |
| L5:       | VCC      |
| L6:       | Signal 4 |

| SYSTEM DC/DC MAX1993 DB (external VGA Core) |         |
|---|---------|
| INPUTS                                      | OUTPUTS |
| DCBATOUT                                    | 1D2V_S0 |

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Title: Block Diagram

|          |                        |         |
|----------|------------------------|---------|
| Size: A3 | Document Number: <Doc> | Rev: SA |
|----------|------------------------|---------|

Date: Saturday, February 19, 2005 Sheet 1 of 44

# Calistoga Strapping Signals and Configuration

| Pin Name       | Strap Description   | Configuration  |
|----------------|---|--|
| CFG[2:0]       | FSB Frequency Select  | 001 = FSB533<br>011 = FSB667<br>Others = Reversed  |
| CFG[3:4]       | Reversed  |  |
| CFG5           | DMI x2 Select   | 0 = DMI x2<br>1 = DMI x4 (Default)   |
| CFG6           | NB strap  | 0 = Moby Dick<br>1 = Calistoga (Default)   |
| CFG7           | CPU Strap   | 0= Reserved<br>1=Mobility (Default)  |
| CFG8           | Reversed  |  |
| CFG9           | PCI Express Graphics Lane reverse option for layout convenience | 0=Reverse Lanes<br>1=Normal Operation (Default)  |
| CFG10          | Reversed  |  |
| CFG11          | Reversed  |  |
| CFG[13:12]     | Reversed  |  |
| CFG[14:15]     | Reversed  |  |
| CFG16          | FSB Dynamic ODT   | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)  |
| CFG17          | Reversed  |  |
| CFG18          | GMCH core VCC Select  | 0 = 1.05V (Default)<br>1 = 1.5V  |
| CFG19          | DMI Lane Reversal   | 0 = Normal(Default)<br>1 = Lanes Reversal  |
| CFG20          |   | 0= Only SDVO or PCIe x1 is operational ( default)<br>1= SDVO and PCIE x1 are operating simultaneously via the PEG port |
| SDVO CRTL_DATA | SDVO Present  | 0 = No SDVO device present<br>1= SDVO device present (Default)   |

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

## KBC Hardware Strap

| PinNumber | PinName | Function   |
|-----------|---------|--|
| 125       | A1      | High:Enable the internal pull-up resistors on XIOCS [F:0] pins<br>Low:Disable the internal pull-up resistors on XIOCS [F:0]                      |
| 128       | A4      | High: Diasble DMPP(Recommended)<br>Low : Enable DMPP   |
| 131       | A5      | High:Enable EMWB(Recommended for application using shared BIOS)<br>Low:Disable EMWB  |
| 11        | GPIO05  | High:Test Mode<br>Low:32KHz clock in normal running(Recommend)   |
| 12        | GPIO06  | High:Test Mode(KSOUT0~15 become DPLL internal data outputs, KS016 becomes internal power-on reset output<br>Low:Normal operation(Recommended)    |
| 105       | GPIO20  | High:Normal operation(Recommended)<br>Low:Enable ISP mode during which the RD#,WR#,MEMSEL#,A[20:0] andD[7:0]will be controlled by ISP Contriller |

# ICS954226 Spread Spectrum Select

| Byte 6b7 | Byte 6b6 | byte 6b5 | Byte 6b4 | Spread Mode | Spread Amount% | Pin17/18 Mhz |
|----------|----------|----------|----------|-------------|----------------|--------------|
| 1        | 0        | 0        | 0        | Down        | 0.8            | 100          |
| 1        | 0        | 0        | 1        | Down        | 1.25           | 100          |
| 1        | 0        | 1        | 0        | Down        | 1.75           | 100          |
| 1        | 0        | 1        | 1        | Down        | 2.5            | 100          |
| 1        | 1        | 0        | 0        | Center      | +0.3           | 100          |
| 1        | 1        | 0        | 1        | Center      | +0.5           | 100          |
| 1        | 1        | 1        | 0        | Center      | +0.8           | 100          |
| 1        | 1        | 1        | 1        | Center      | +1.25          | 100          |

## PCI Routing

|         | IDSEL | IRQ | REQ/GNT |
|---------|-------|-----|---------|
| CB810   | 25    | E   | 0       |
| MiniPCI | 21    | G   | 1       |
| LAN     | 23    | F   | 2       |
| 1394    | 19    | E   | 3       |

## ICH7-M IDE Integrated Series Termination Resistors

|  |                      |
|--|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ | approximately 33 ohm |
|--|----------------------|

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# ICH7-M Integrated Pull-up and Pull-down Resistors

|   |                                |
|---|--------------------------------|
| EE_DIN, EE_DOUT, GNT[3:0]<br>GNT[4]#/GPO[48], GNT[5]#/GPO[17], GNT[6]#/GPO[16], GPIO[25]<br>LAD[3:0]#/FB[3:0]#, LAN_RXD[2:0], LDRQ[0], LDRQ[1]/GPI[41],PME#, PWRBTN#, TP[3] | ICH7 internal 20K pull-ups     |
| SATALED#  | ICH7 internal 15K pull-ups     |
| ACZ_BITCLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSTP#   | ICH7 internal 20K pull-downs   |
| DPRSLPVR, EE_CS,SPKR#SPI_ARB, SPI_CLK, USB[7:0][P,N]  | ICH7 internal 15K pull-downs   |
| DD[7], DDREQ  | ICH7 internal 11.5K pull-downs |
| LAN_CLK   | ICH7 internal 100K pull-downs  |

## ICH7-M Strapping Options

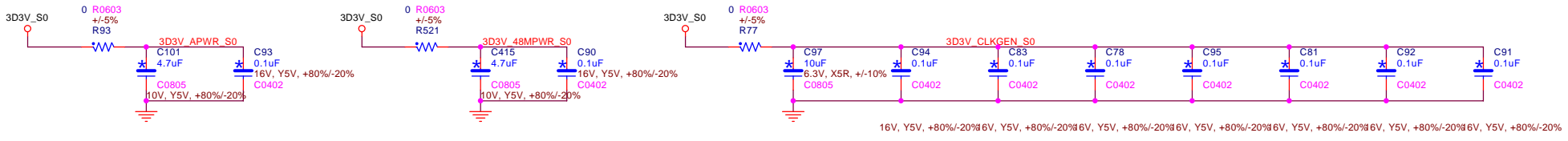
|           |   |
|-----------|---|
| INVTVRMEN | This signal enables the internal VccSus1_5V suspend regulator when connected to VccRTC. When connected to GND, the internal regulator is disabled. To enable interna VccSus1_5V VRM pull signal to VccRTC via 330Kohm   |
| SPKR      | The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH7M will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit. NOTE: Please refer to ICH7M EDS Rev0.5 (or latest) for all ICH7M Strap details. |

| Pin Name                          | Strap Description               | Configuration  |
|-----------------------------------|---------------------------------|--|
| GNT3#                             | Top-Block Swap Override         | Internal Pull-up for top-block swap mode.                                |
| LINKALERT#                        | Reversed                        |  |
| SPKR                              | No Reboot                       | Internal pull-down to indicate system is strapped to the no reboot more. |
| INTVRMEN                          | VccSus1_05 VRM Enable/Disable.  | 0 = Disable (Default)<br>1 = Enable                                      |
| GPIO25                            | Reserved                        |  |
| EE_CS                             | Reversed                        |  |
| GNT5# /GPIO17#.<br>GNT4# /GPIO48. | Boot BIOS Destination Selection | 01 = SPI<br>10 = PCI<br>11 = LPC (Default)                               |
| EE_DOUT                           | Reversed                        |  |
| ACZ_SDOUT                         | XOR Chain Entrance              | 0 = Allow XOR Testing (Default)<br>1 = Not Allow                         |
| ACZ_SYNC                          | PCI-E Port CFG Bit 0            | Reversed   |
| GPIO16/<br>DPRSLPVR               | Reversed                        |  |
| SATALED#                          | Reversed                        |  |
| REQ[4:1]#                         | XOR Chain Selection             | Not available in Datasheet Yet   |
| TP3                               | XOR Chain Entrance              | Not available in Datasheet Yet   |

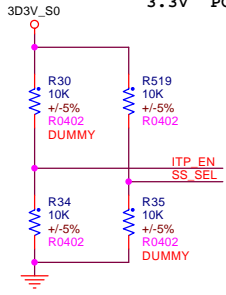
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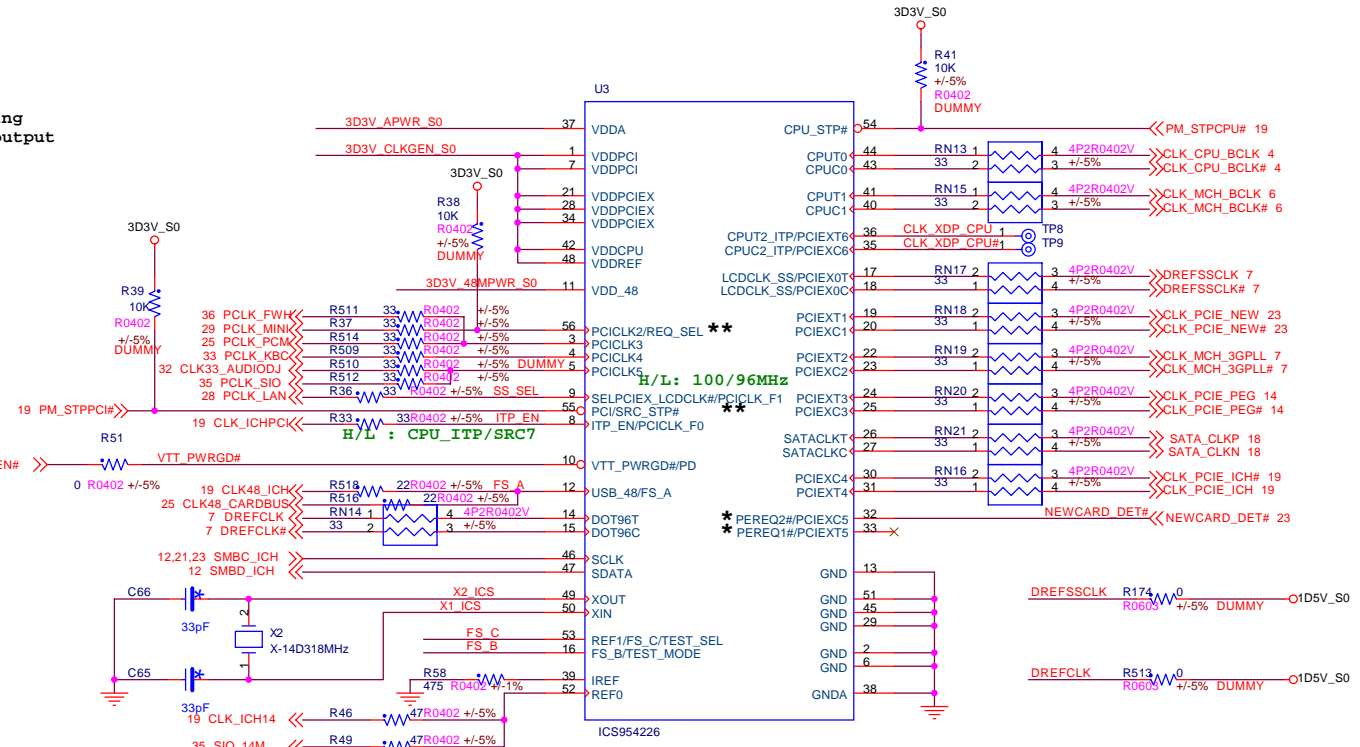
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| Size  | Document Number             | W06N  |                  | Rev | SA |
| A3    | <Doc>                       |       |                  |     |    |
| Date: | Saturday, February 19, 2005 | Sheet | 2                | of  | 44 |



ITP\_EN 0=PCIEX\_6 1=CPU\_2\_ITP  
 SS\_SEL 0=LCDCLK 1=PCIEX/free running  
 3.3V PCI clock output



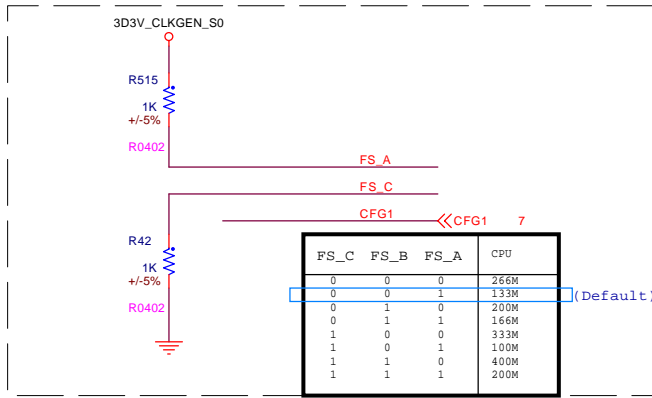
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\*internal Pull-Up resistors  
 \*\*internal Pull-Down resistor

EMI capacitor

|               |      |      |       |                 |       |
|---------------|------|------|-------|-----------------|-------|
| CLK_ICH14     | C80  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| CLK33_AUDIODJ | C405 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_PCM      | C413 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_MINI     | C77  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_KBC      | C404 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| CLK_ICHPCI    | C64  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| CLK48_ICH     | C414 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| PCLK_SIO      | C411 | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |
| SIO_14M       | C82  | 10pF | C0402 | 50V, NPO, +/-5% | DUMMY |



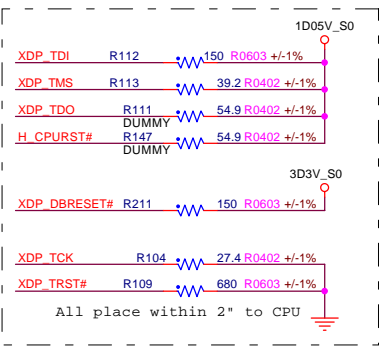
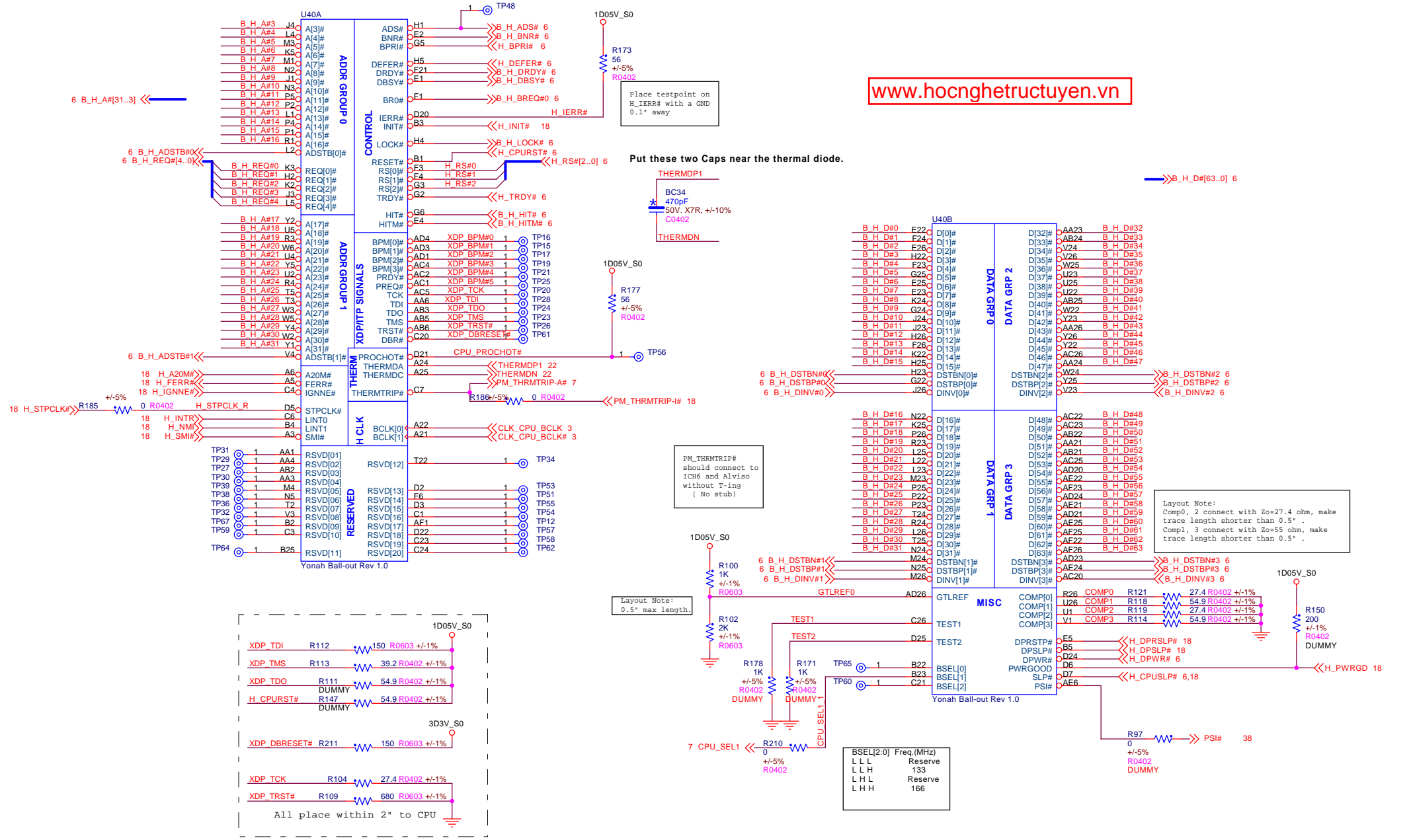
|                |     |                  |
|----------------|-----|------------------|
| CLK_PCIE_ICH   | R59 | 49.9 R0402 +/-1% |
| CLK_PCIE_ICH#  | R60 | 49.9 R0402 +/-1% |
| DREFSSCLK#     | R62 | 49.9 R0402 +/-1% |
| DREFSSCLK      | R61 | 49.9 R0402 +/-1% |
| CLK_PCIE_NEW   | R63 | 49.9 R0402 +/-1% |
| CLK_PCIE_NEW#  | R64 | 49.9 R0402 +/-1% |
| DREFCLK        | R53 | 49.9 R0402 +/-1% |
| DREFCLK#       | R55 | 49.9 R0402 +/-1% |
| SATA_CLKP      | R69 | 49.9 R0402 +/-1% |
| SATA_CLKN      | R70 | 49.9 R0402 +/-1% |
| CLK_CPU_BCLK   | R52 | 49.9 R0402 +/-1% |
| CLK_CPU_BCLK#  | R54 | 49.9 R0402 +/-1% |
| CLK_MCH_BCLK   | R56 | 49.9 R0402 +/-1% |
| CLK_MCH_BCLK#  | R57 | 49.9 R0402 +/-1% |
| CLK_PCIE_PEG   | R67 | 49.9 R0402 +/-1% |
| CLK_PCIE_PEG#  | R68 | 49.9 R0402 +/-1% |
| CLK_MCH_3GPLL  | R66 | 49.9 R0402 +/-1% |
| CLK_MCH_3GPLL# | R65 | 49.9 R0402 +/-1% |

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Title  
**Clock Generator**

Size A3 Document Number **W06N** Rev SA  
 <Doc>

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Layout Note:  
0.5" max length.

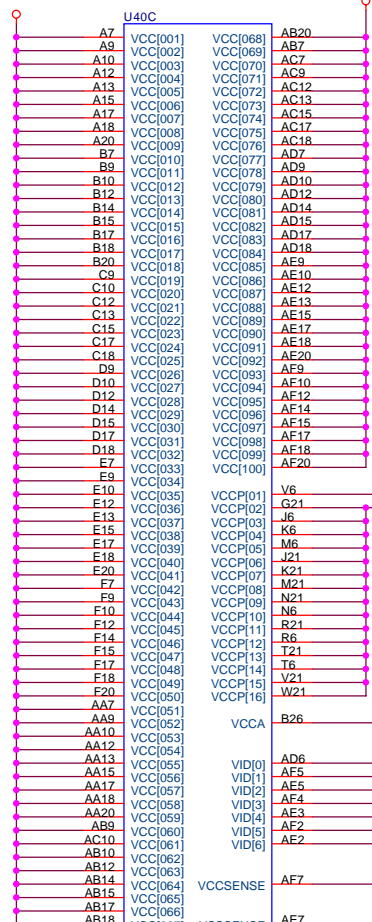
Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

|                      |         |
|----------------------|---------|
| BSEL[2:0] Freq.(MHz) |         |
| L L L                | Reserve |
| L L H                | 133     |
| L H L                | Reserve |
| L H H                | 166     |

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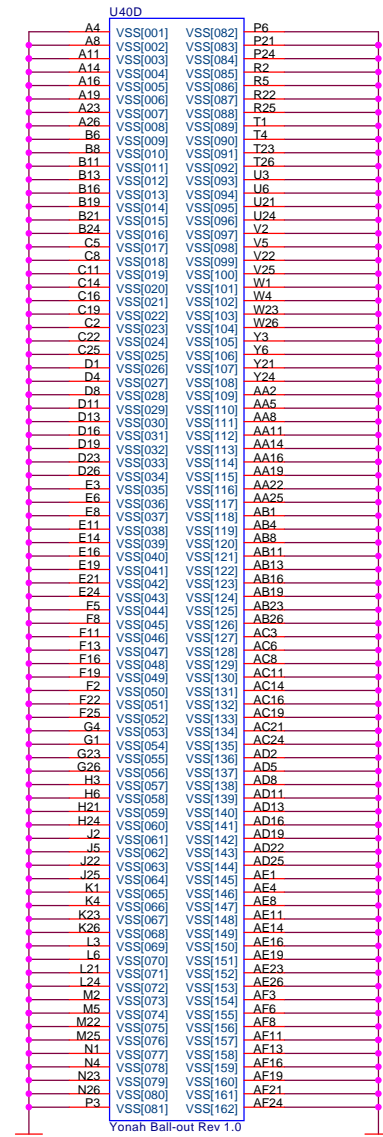
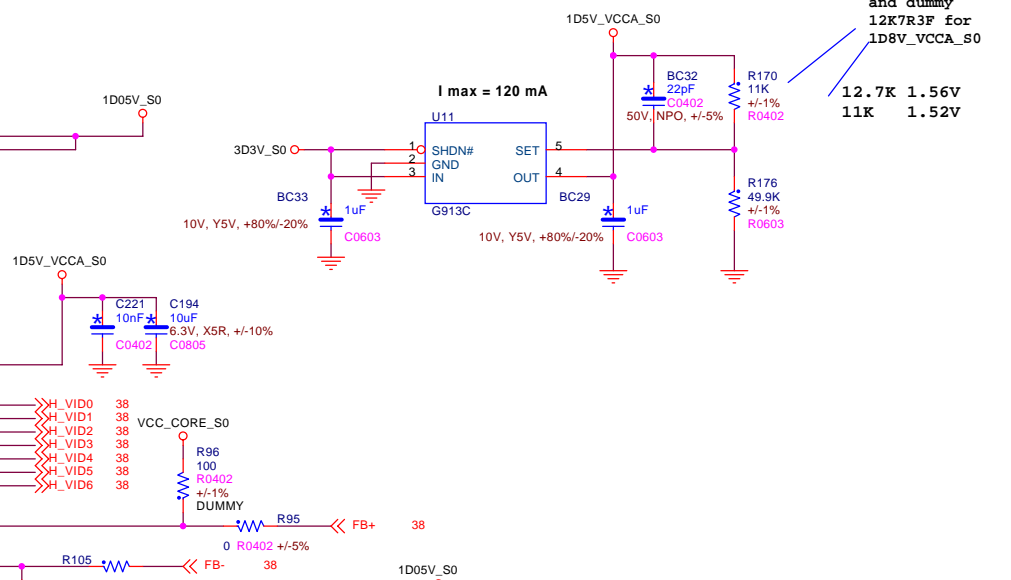
Title: CPU(1/2)

|                                 |                       |         |
|---------------------------------|-----------------------|---------|
| Size: A3                        | Document Number: W06N | Rev: SA |
| Date: Monday, February 21, 2005 | Sheet: 4 of 44        |         |



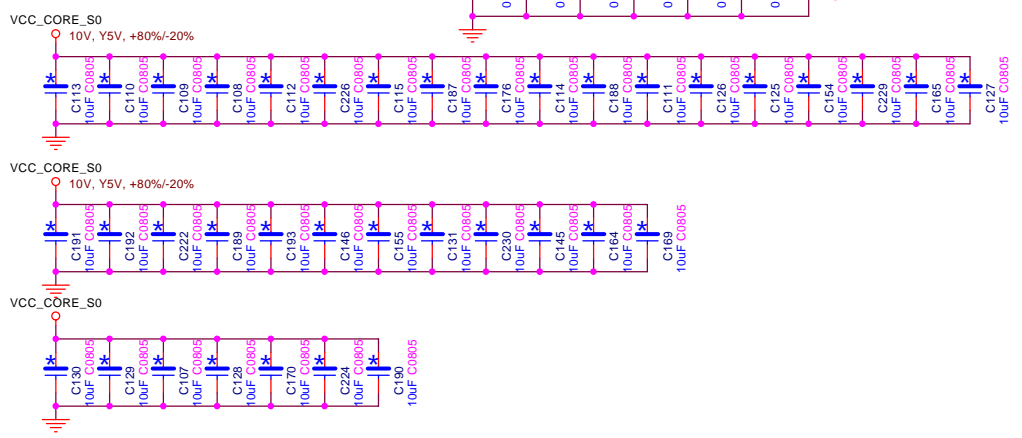
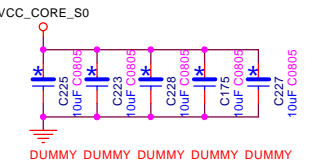
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Place these and dummy 12K7R3F for 1D8V\_VCCA\_S0  
12.7K 1.56V  
11K 1.52V

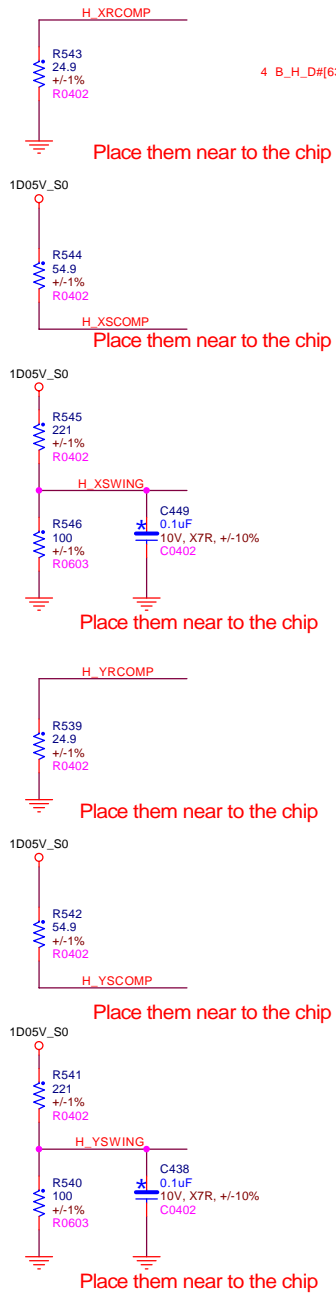


Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.



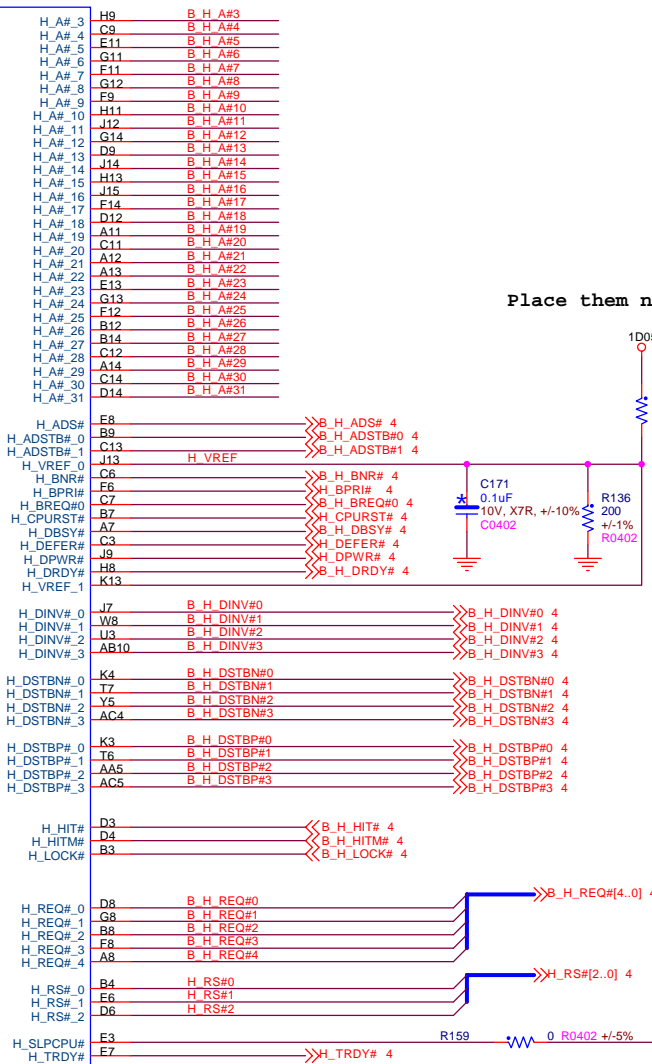
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FOXCONN ND2  
CPU(2/2)  
W06N  
Rev SA  
Date: Saturday, February 19, 2005 Sheet 5 of 44



4 B\_H\_D#[63..0]

| U39A     |      | CALISTOGA_1p0 |     |
|----------|------|---------------|-----|
| B_H_D#0  | F1   | H_XRCOMP      | E1  |
| B_H_D#1  | J1   | H_XSCOMP      | E2  |
| B_H_D#2  | H1   | H_XSWING      | E4  |
| B_H_D#3  | J6   | H_YRCOMP      | Y1  |
| B_H_D#4  | H3   | H_YSCOMP      | U1  |
| B_H_D#5  | K2   | H_YSWING      | W1  |
| B_H_D#6  | G1   | H_CLKIN       | AG2 |
| B_H_D#7  | G2   | H_CLKIN#      | AG1 |
| B_H_D#8  | K9   |               |     |
| B_H_D#9  | K1   |               |     |
| B_H_D#10 | K7   |               |     |
| B_H_D#11 | J8   |               |     |
| B_H_D#12 | H4   |               |     |
| B_H_D#13 | J3   |               |     |
| B_H_D#14 | K11  |               |     |
| B_H_D#15 | G4   |               |     |
| B_H_D#16 | T10  |               |     |
| B_H_D#17 | W11  |               |     |
| B_H_D#18 | T3   |               |     |
| B_H_D#19 | U7   |               |     |
| B_H_D#20 | U9   |               |     |
| B_H_D#21 | U11  |               |     |
| B_H_D#22 | T11  |               |     |
| B_H_D#23 | W9   |               |     |
| B_H_D#24 | T1   |               |     |
| B_H_D#25 | T8   |               |     |
| B_H_D#26 | T4   |               |     |
| B_H_D#27 | W7   |               |     |
| B_H_D#28 | U5   |               |     |
| B_H_D#29 | T9   |               |     |
| B_H_D#30 | W6   |               |     |
| B_H_D#31 | T5   |               |     |
| B_H_D#32 | AB7  |               |     |
| B_H_D#33 | AA9  |               |     |
| B_H_D#34 | W4   |               |     |
| B_H_D#35 | W3   |               |     |
| B_H_D#36 | Y3   |               |     |
| B_H_D#37 | Y7   |               |     |
| B_H_D#38 | W5   |               |     |
| B_H_D#39 | Y10  |               |     |
| B_H_D#40 | AB8  |               |     |
| B_H_D#41 | W2   |               |     |
| B_H_D#42 | AA4  |               |     |
| B_H_D#43 | AA7  |               |     |
| B_H_D#44 | AA2  |               |     |
| B_H_D#45 | AA6  |               |     |
| B_H_D#46 | AA10 |               |     |
| B_H_D#47 | Y8   |               |     |
| B_H_D#48 | AA1  |               |     |
| B_H_D#49 | AB4  |               |     |
| B_H_D#50 | AC9  |               |     |
| B_H_D#51 | AB11 |               |     |
| B_H_D#52 | AC11 |               |     |
| B_H_D#53 | AB3  |               |     |
| B_H_D#54 | AC2  |               |     |
| B_H_D#55 | AD1  |               |     |
| B_H_D#56 | AD9  |               |     |
| B_H_D#57 | AC1  |               |     |
| B_H_D#58 | AD7  |               |     |
| B_H_D#59 | AC6  |               |     |
| B_H_D#60 | AB5  |               |     |
| B_H_D#61 | AD10 |               |     |
| B_H_D#62 | AD4  |               |     |
| B_H_D#63 | AC8  |               |     |
| H_D#_0   |      |               |     |
| H_D#_1   |      |               |     |
| H_D#_2   |      |               |     |
| H_D#_3   |      |               |     |
| H_D#_4   |      |               |     |
| H_D#_5   |      |               |     |
| H_D#_6   |      |               |     |
| H_D#_7   |      |               |     |
| H_D#_8   |      |               |     |
| H_D#_9   |      |               |     |
| H_D#_10  |      |               |     |
| H_D#_11  |      |               |     |
| H_D#_12  |      |               |     |
| H_D#_13  |      |               |     |
| H_D#_14  |      |               |     |
| H_D#_15  |      |               |     |
| H_D#_16  |      |               |     |
| H_D#_17  |      |               |     |
| H_D#_18  |      |               |     |
| H_D#_19  |      |               |     |
| H_D#_20  |      |               |     |
| H_D#_21  |      |               |     |
| H_D#_22  |      |               |     |
| H_D#_23  |      |               |     |
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| H_D#_25  |      |               |     |
| H_D#_26  |      |               |     |
| H_D#_27  |      |               |     |
| H_D#_28  |      |               |     |
| H_D#_29  |      |               |     |
| H_D#_30  |      |               |     |
| H_D#_31  |      |               |     |
| H_D#_32  |      |               |     |
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| H_D#_41  |      |               |     |
| H_D#_42  |      |               |     |
| H_D#_43  |      |               |     |
| H_D#_44  |      |               |     |
| H_D#_45  |      |               |     |
| H_D#_46  |      |               |     |
| H_D#_47  |      |               |     |
| H_D#_48  |      |               |     |
| H_D#_49  |      |               |     |
| H_D#_50  |      |               |     |
| H_D#_51  |      |               |     |
| H_D#_52  |      |               |     |
| H_D#_53  |      |               |     |
| H_D#_54  |      |               |     |
| H_D#_55  |      |               |     |
| H_D#_56  |      |               |     |
| H_D#_57  |      |               |     |
| H_D#_58  |      |               |     |
| H_D#_59  |      |               |     |
| H_D#_60  |      |               |     |
| H_D#_61  |      |               |     |
| H_D#_62  |      |               |     |
| H_D#_63  |      |               |     |

HOST



Place them near to the chip

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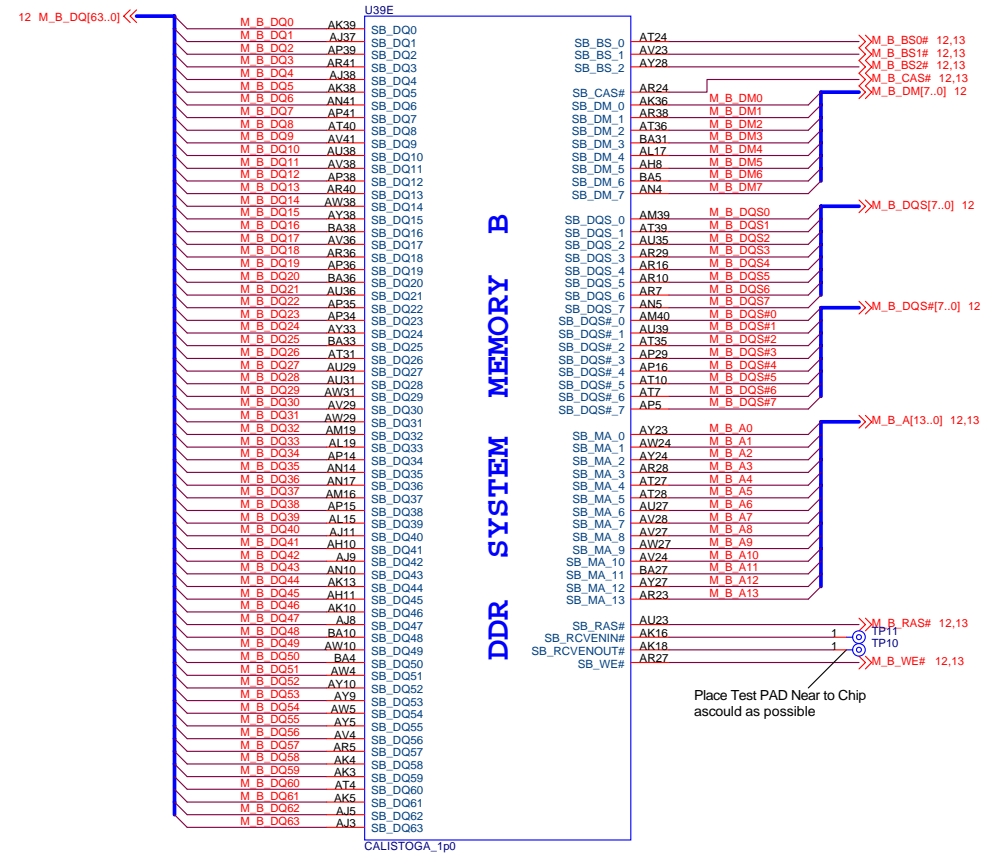
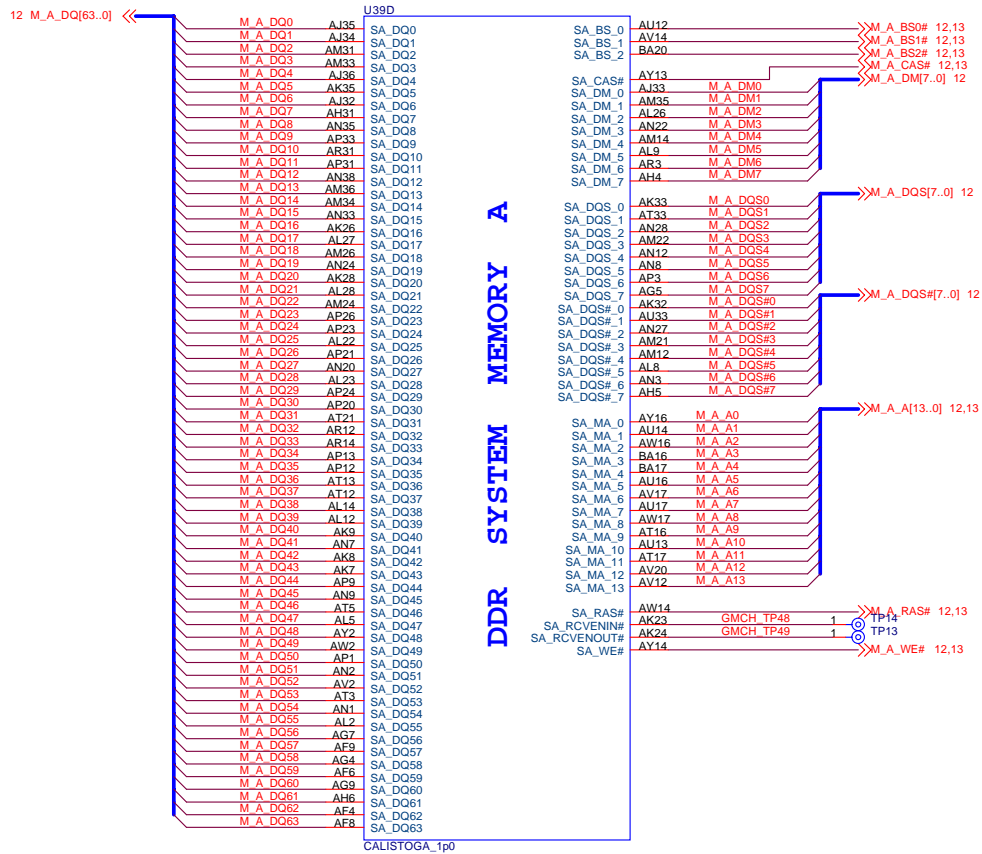
FOXCONN ND2

Title  
Calistoga (1 of 6)

|            |                          |      |           |
|------------|--------------------------|------|-----------|
| Size<br>A3 | Document Number<br><Doc> | W06N | Rev<br>SA |
|------------|--------------------------|------|-----------|

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**FOXCONN**  
 FOXCONN ND2

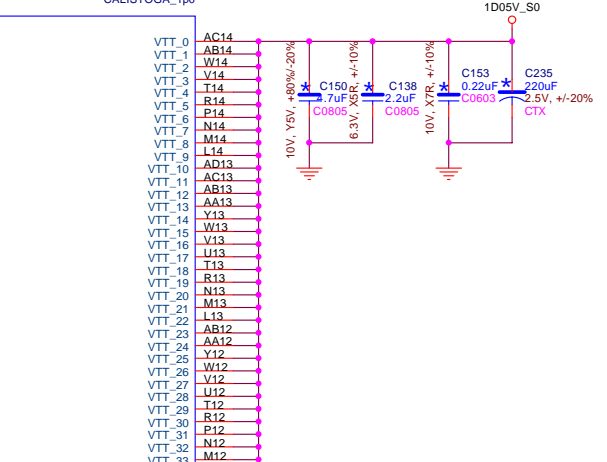
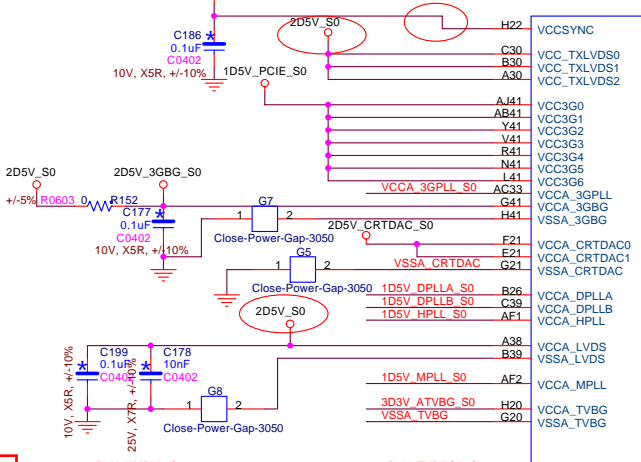
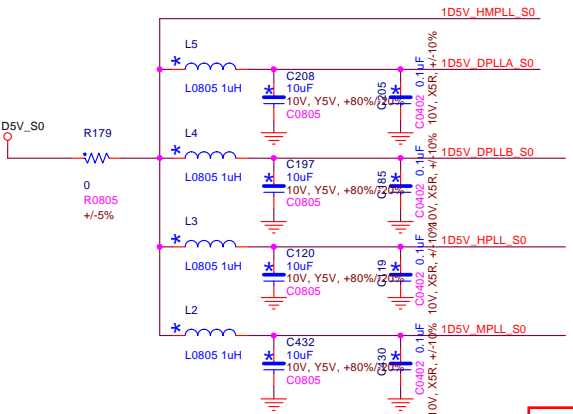
Title: Calistoga (3 of 6)

Size: W06N  
 Document Number: W06N  
 Customer Doc#

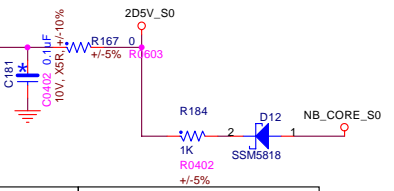
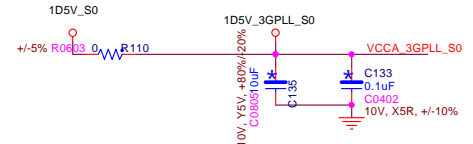
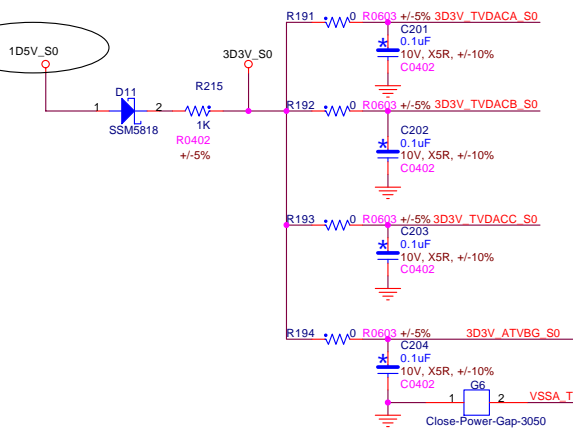
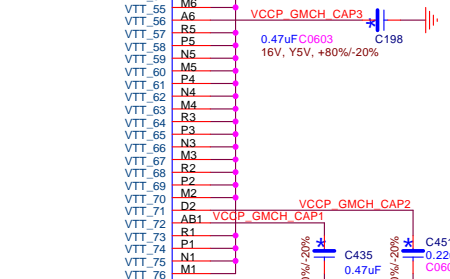
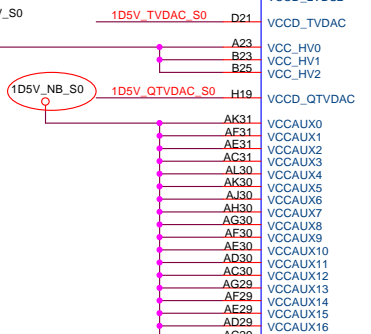
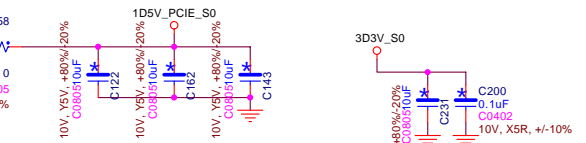
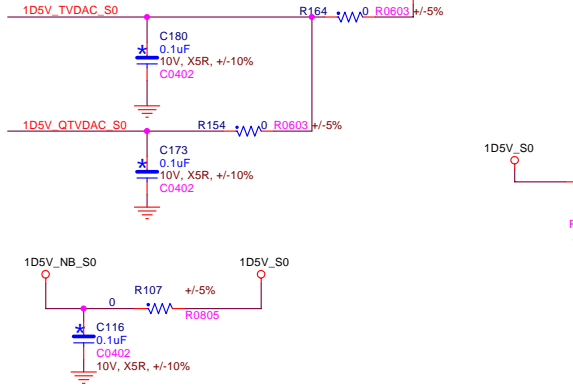
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Rev SA





**POWER**



|      |              |
|------|--------------|
| AH1  | VCCD_HMPLL0  |
| AH2  | VCCD_HMPLL1  |
| A28  | VCCD_LVDS0   |
| B28  | VCCD_LVDS1   |
| C28  | VCCD_LVDS2   |
| D21  | VCCD_TV_DAC  |
| A23  | VCC_HV0      |
| B23  | VCC_HV1      |
| B25  | VCC_HV2      |
| H19  | VCCD_QTV_DAC |
| AK31 | VCCAUX0      |
| AE31 | VCCAUX1      |
| AC31 | VCCAUX2      |
| AL30 | VCCAUX3      |
| AK30 | VCCAUX4      |
| AJ30 | VCCAUX5      |
| AH30 | VCCAUX6      |
| AG30 | VCCAUX7      |
| AF30 | VCCAUX8      |
| AE30 | VCCAUX9      |
| AD30 | VCCAUX10     |
| AC30 | VCCAUX11     |
| AG29 | VCCAUX12     |
| AE29 | VCCAUX13     |
| AD29 | VCCAUX14     |
| AC29 | VCCAUX15     |
| AG28 | VCCAUX16     |
| AE28 | VCCAUX17     |
| AD28 | VCCAUX18     |
| AC28 | VCCAUX19     |
| AH22 | VCCAUX20     |
| AJ21 | VCCAUX21     |
| AH21 | VCCAUX22     |
| AJ20 | VCCAUX23     |
| AH20 | VCCAUX24     |
| AH19 | VCCAUX25     |
| PI9  | VCCAUX26     |
| PI6  | VCCAUX27     |
| AH15 | VCCAUX28     |
| PI5  | VCCAUX29     |
| AH14 | VCCAUX30     |
| AE14 | VCCAUX31     |
| AE14 | VCCAUX32     |
| AE14 | VCCAUX33     |
| AE14 | VCCAUX34     |
| Y14  | VCCAUX35     |
| AE13 | VCCAUX36     |
| AE12 | VCCAUX37     |
| AE12 | VCCAUX38     |
| AD12 | VCCAUX39     |
| AD12 | VCCAUX40     |

Route AGSATVBG gnd from GMCH1 to decoupling cap ground lead and then connect to the gnd plane

Layout Notes: VSSA\_CRTDAC Route caps within 250mml of Alvigo. Route RB within 3" of Alvigo. Route VSSA\_CRTDAC gnd from GMCH1 to decoupling cap ground lead and then connect to the gnd plane.

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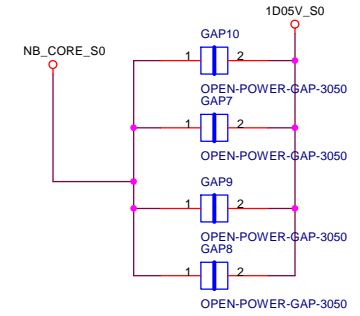
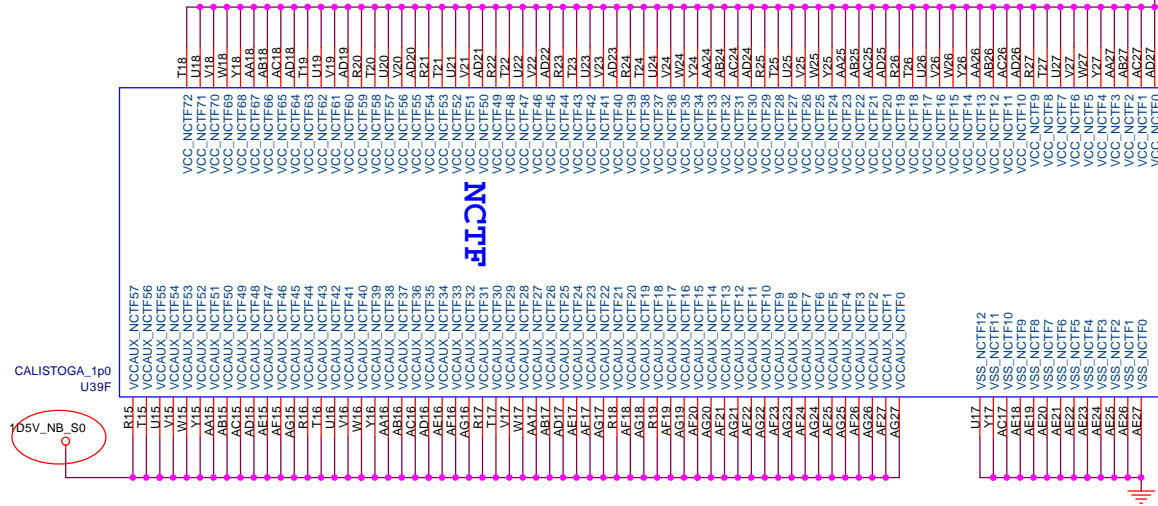
FOXCONN ND2

|               |                           |       |                    |    |    |
|---------------|---------------------------|-------|--------------------|----|----|
| Title         |                           |       | Calistoga (4 of 6) |    |    |
| Size          | Document Number           | Rev   |                    |    |    |
| Customer Doc# | W06N                      | SA    |                    |    |    |
| Date:         | Monday, February 21, 2005 | Sheet | 9                  | of | 44 |

NB\_CORE\_S0

Follow Demo Circuit.

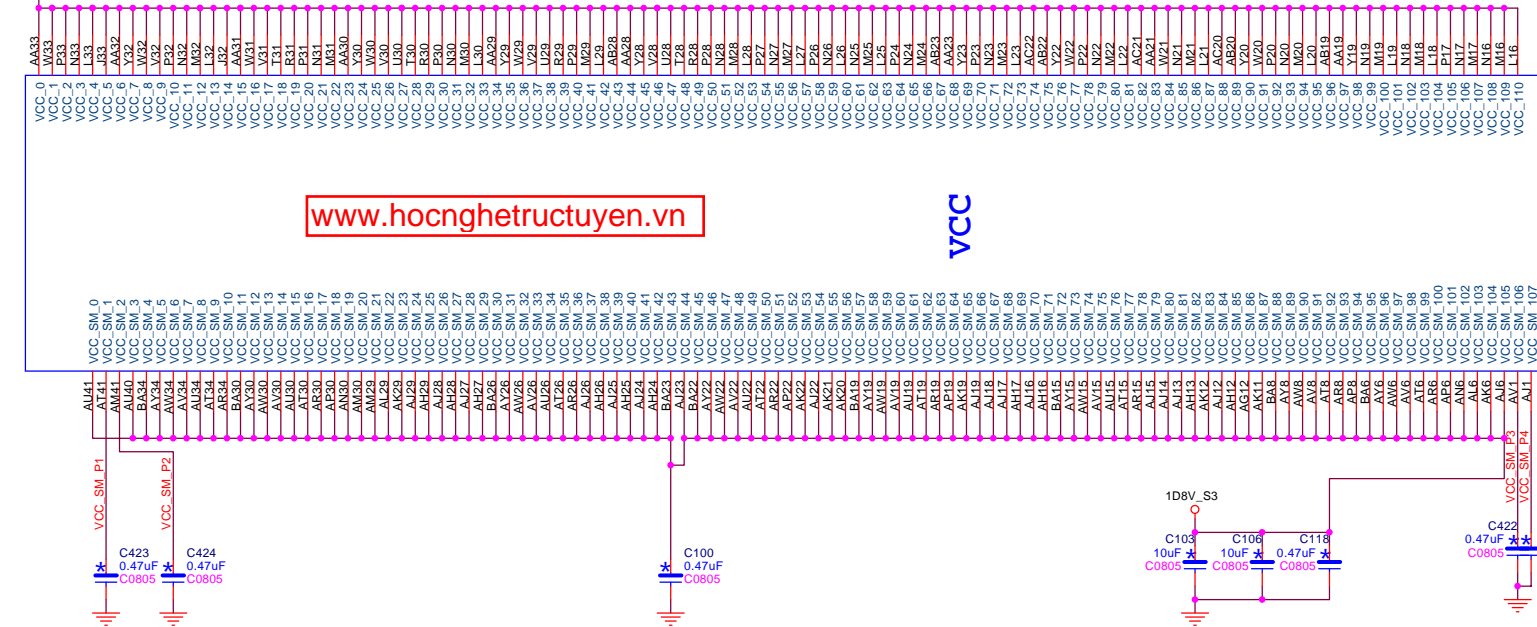
www.hocnghetructuyen.vn



NB\_CORE\_S0

www.hocnghetructuyen.vn

VCC

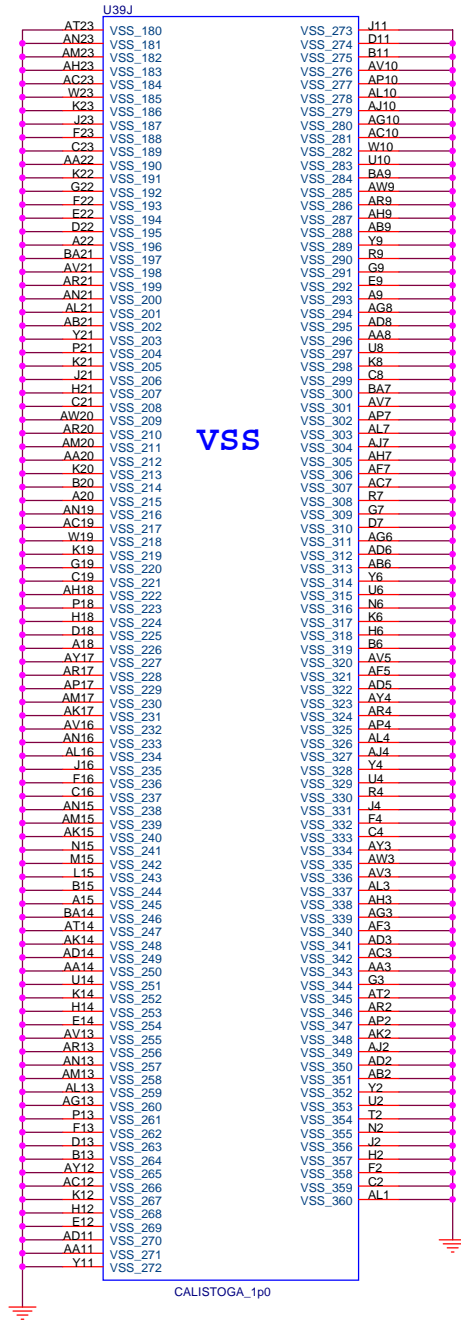
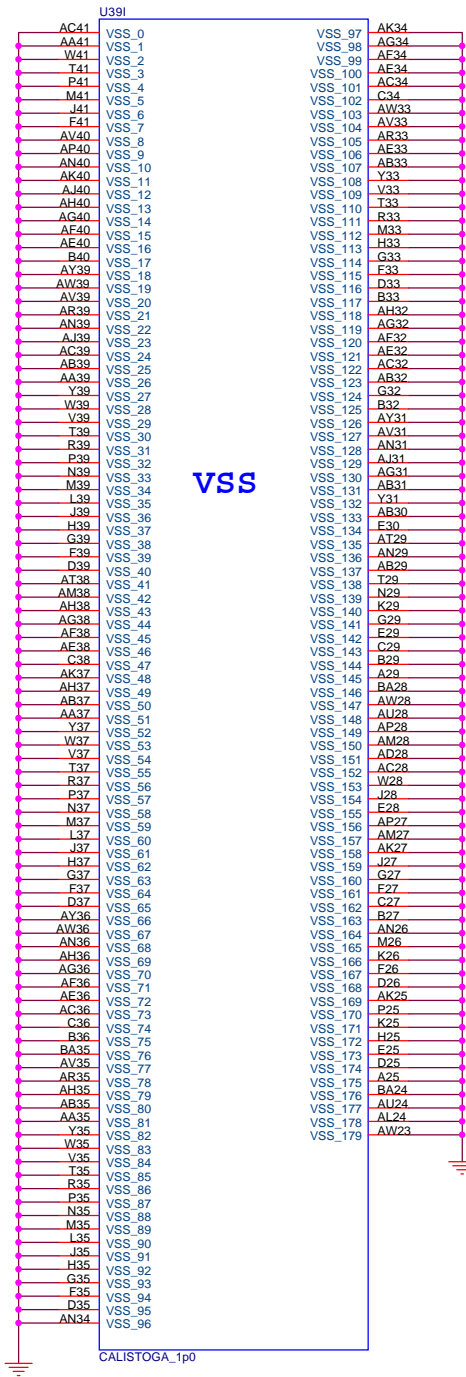


CALISTOGA\_1p0 U39F



FOXCONN ND2

|                    |                             |       |          |
|--------------------|-----------------------------|-------|----------|
| Title              |                             |       |          |
| Calistoga (5 of 6) |                             |       |          |
| Size               | Document Number             | Rev   |          |
| A3                 | <Doc>                       | W06N  | SA       |
| Date:              | Saturday, February 19, 2005 | Sheet | 10 of 44 |



VSS

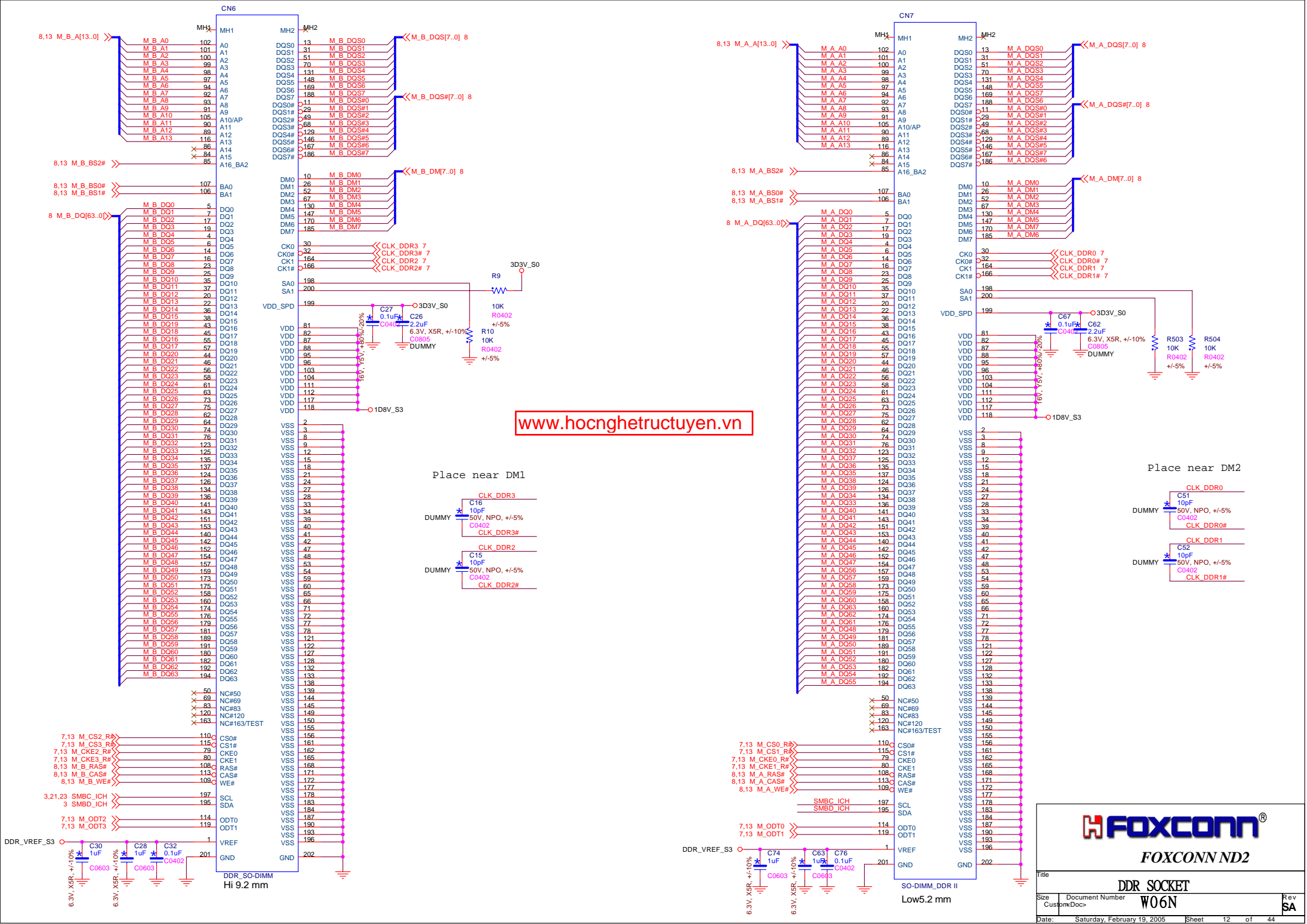
VSS

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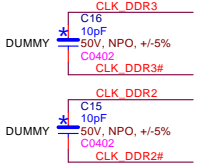
FOXCONN ND2

|                             |                 |          |
|-----------------------------|-----------------|----------|
| Title                       |                 |          |
| Calistoga (6 of 6)          |                 |          |
| Size                        | Document Number | Rev      |
| A3                          | <Doc>           | SA       |
| Date:                       |                 | W06N     |
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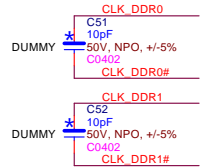


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Place near DM1



Place near DM2



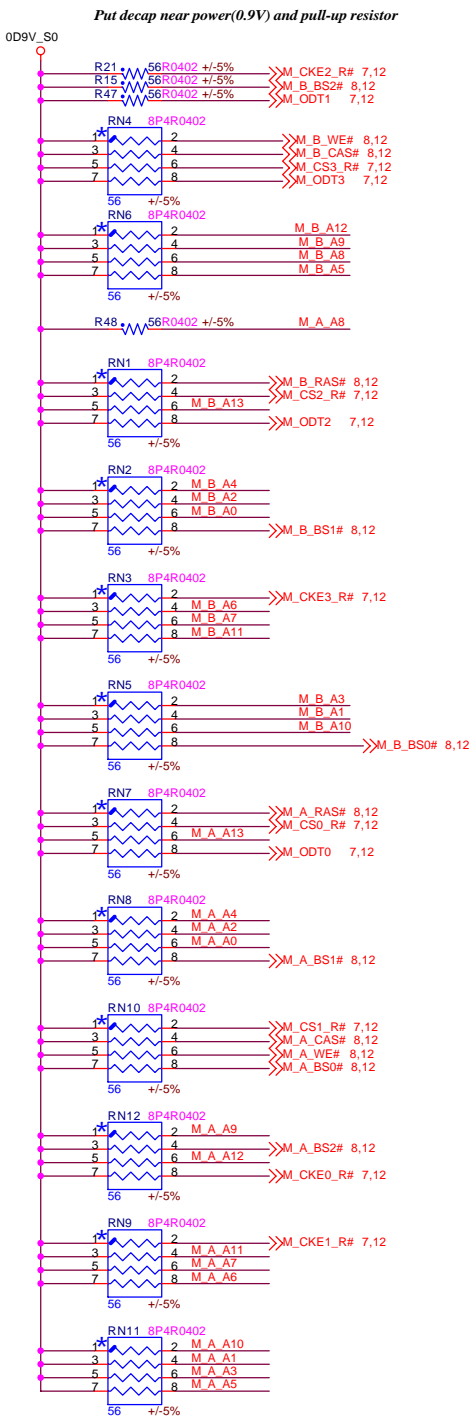
**FOXCONN ND2**

DDR SOCKET

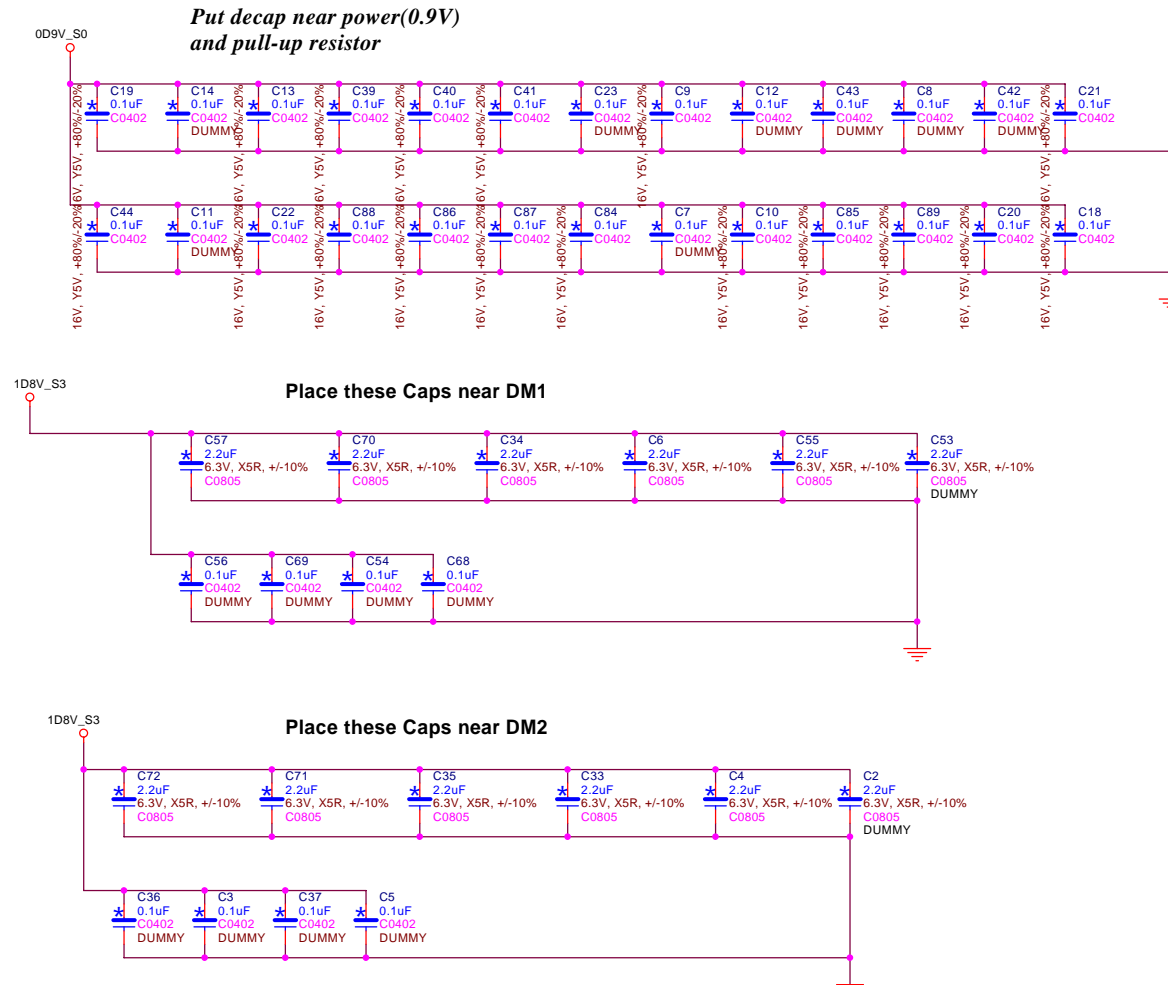
W06N

|                                   |                 |        |          |
|-----------------------------------|-----------------|--------|----------|
| Title                             |                 | Rev SA |          |
| Size                              | Document Number | W06N   |          |
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# PARALLEL TERMINATION



# Decoupling Capacitor



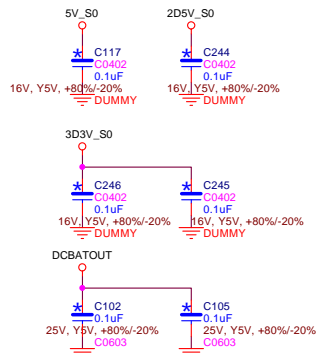
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**FOXCONN ND2**

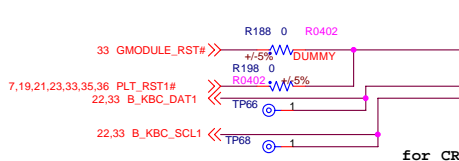
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|                                   |                        |                 |
|-----------------------------------|------------------------|-----------------|
| Size: A3                          | Document Number: <Doc> | Rev: SA         |
| Date: Saturday, February 19, 2005 |                        | Sheet: 13 of 44 |

change to 1.8V\_S0 from 2.5V\_S0



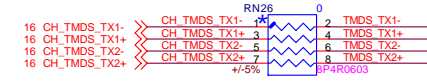
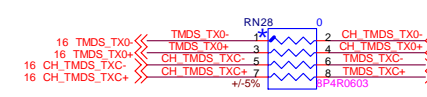
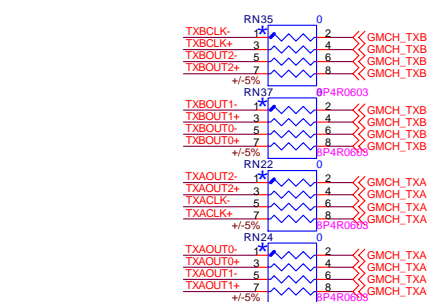
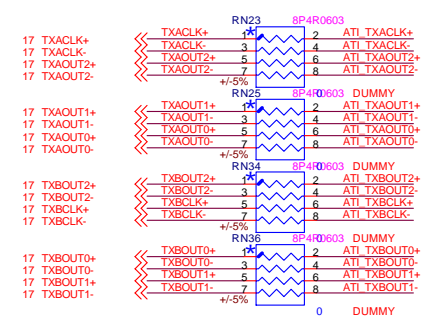
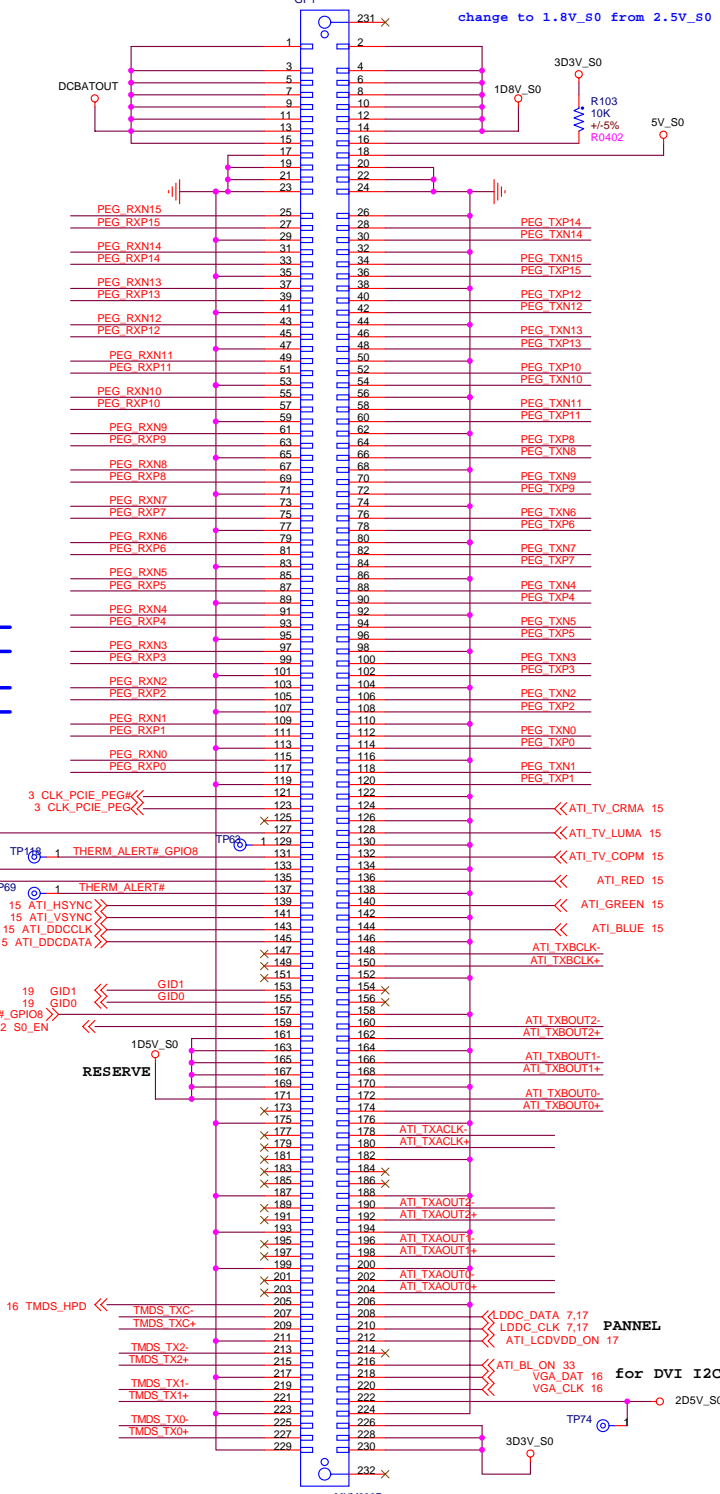
7 PEG\_RXP[15..0] >>  
 7 PEG\_RXN[15..0] >>  
 7 PEG\_TXP[15..0] <<  
 7 PEG\_TXN[15..0] <<



for CRT DDC

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|       | GID1 | GID0 |
|-------|------|------|
| X     | LOW  | HI   |
| X     | LOW  | LOW  |
| NV43M | HI   | LOW  |



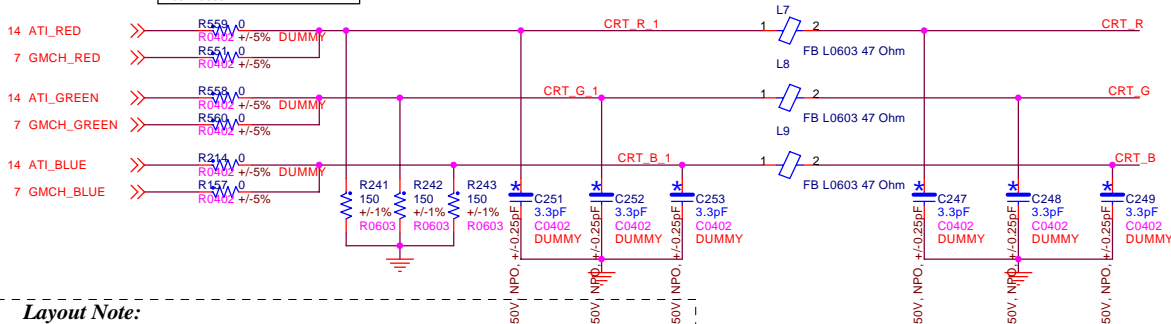
**FOXCONN®**  
**FOXCONN ND2**

file External VGA Conn.  
 Size Document Number W06N  
 Customer Doc: Rev SA  
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# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 47ohm@100MHz

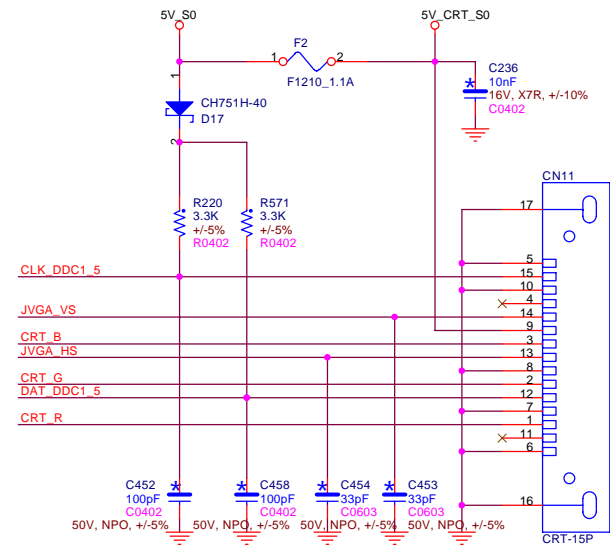
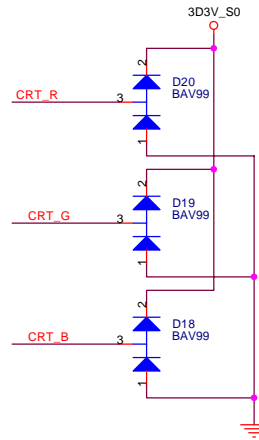
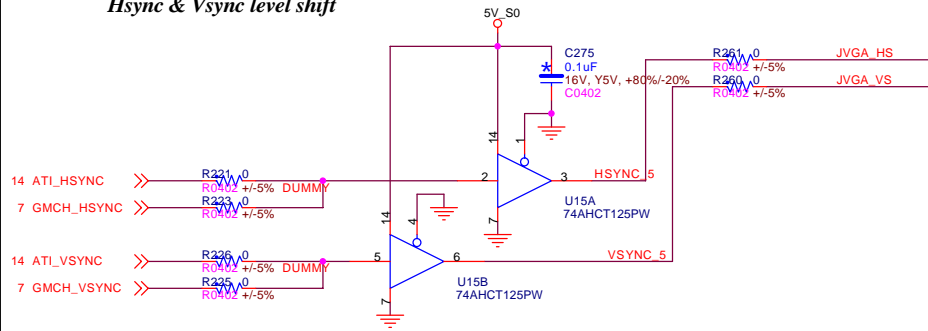


Layout Note:

\* Must be a ground return path between this ground and the ground on the VGA connector.

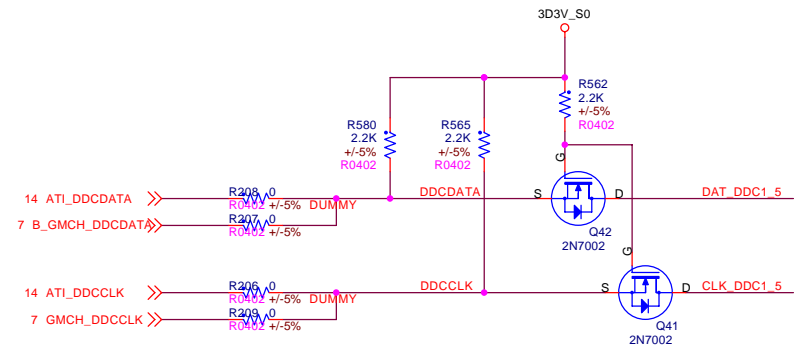
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift

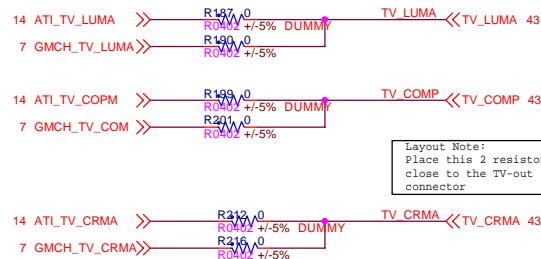
Change VCC from 3.3V to 2.5V 10/27 03'



5V @ ext. CRT side

## TV OUT CONN

Place this 2 resistors close to the TV-out connector



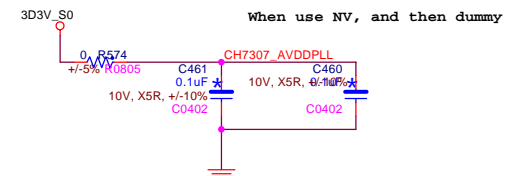
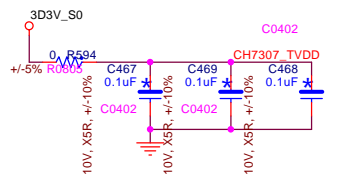
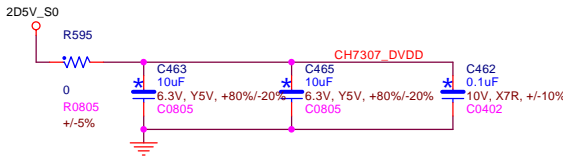
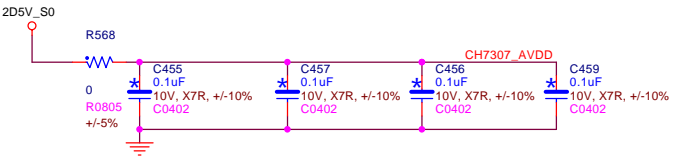
Layout Note:  
Place this 2 resistors close to the TV-out connector

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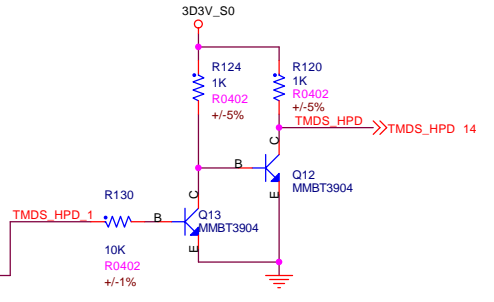
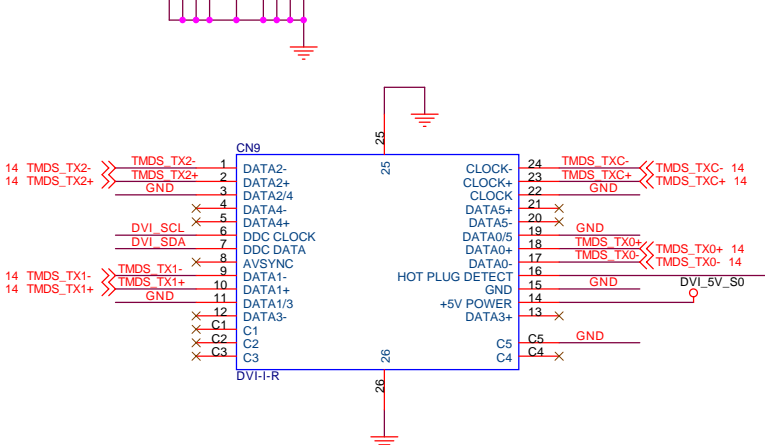
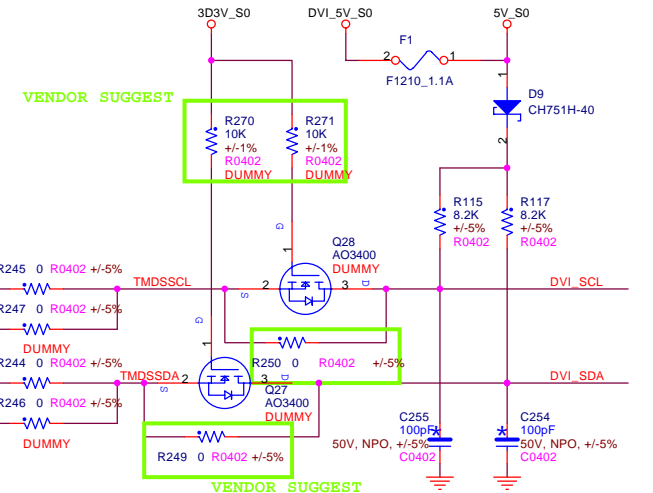
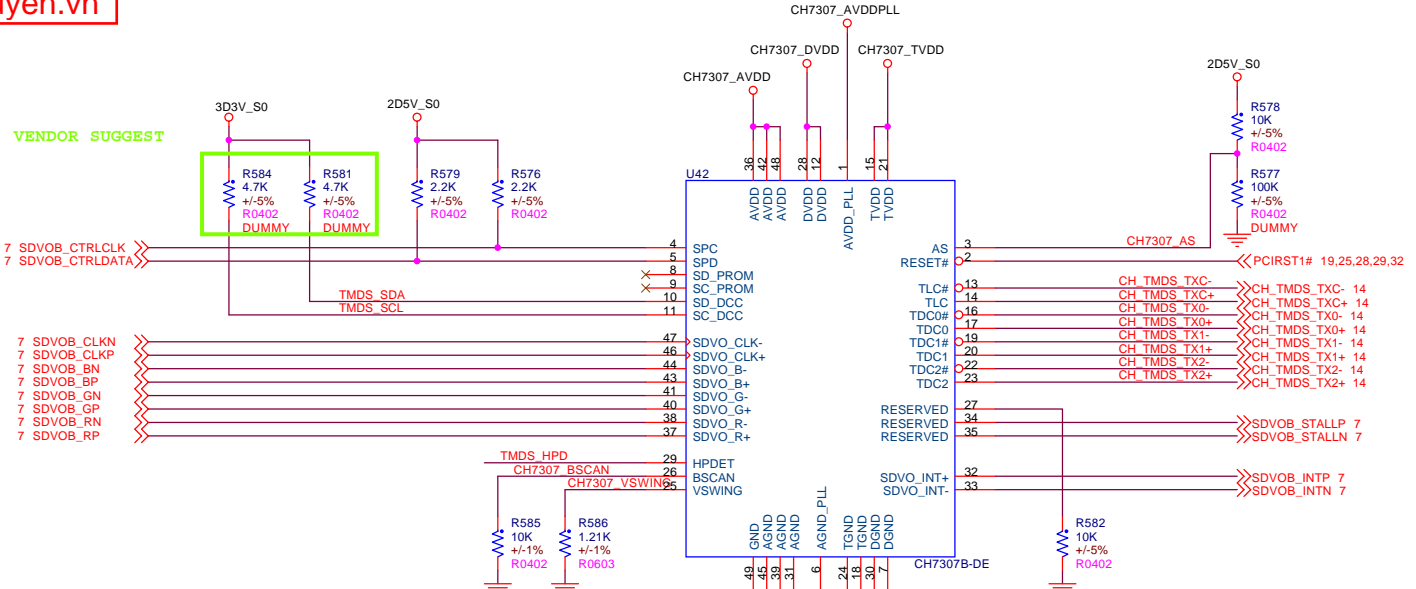
**FOXCONN**

FOXCONN ND2

|                                      |                          |           |
|--------------------------------------|--------------------------|-----------|
| Title<br>CRT/TV                      |                          |           |
| Size<br>A3                           | Document Number<br><Doc> | Rev<br>SA |
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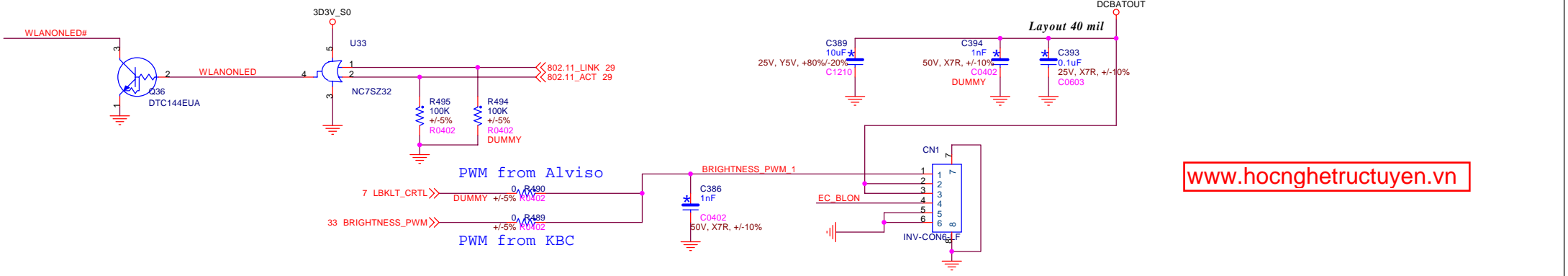


**FOXCONN**  
FOXCONN ND2

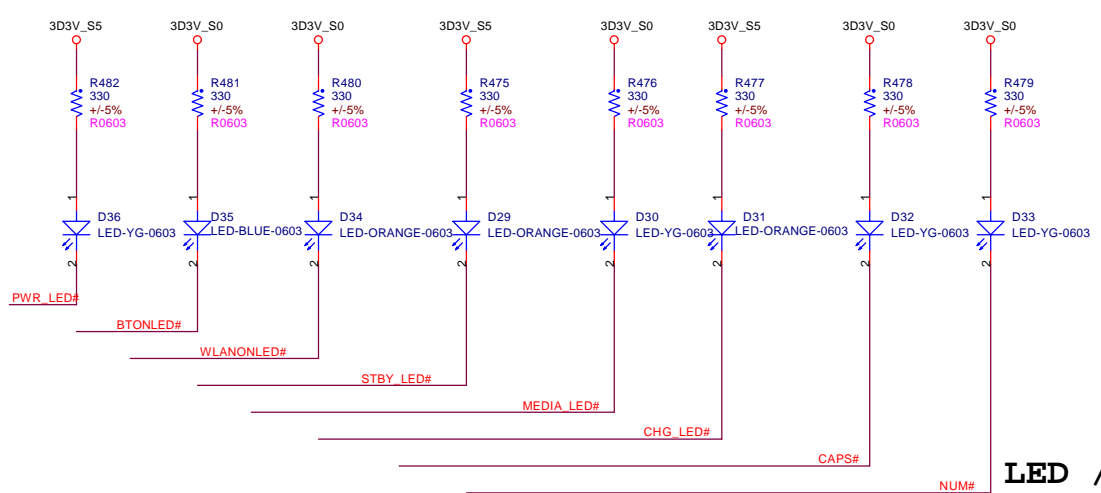
Title: DVI TRANSMITTER

|  |                       |         |
|--|-----------------------|---------|
| Size: A3   | Document Number: W06N | Rev: SA |
| Date: Saturday, February 19, 2005 Sheet 16 of 44 |                       |         |

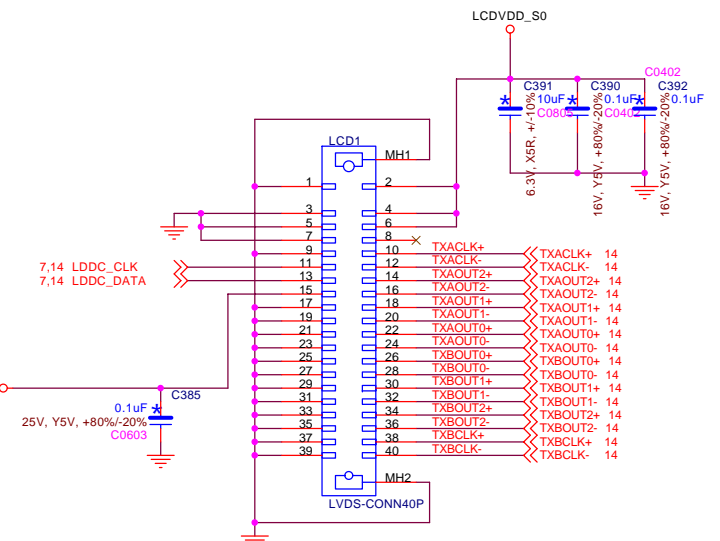
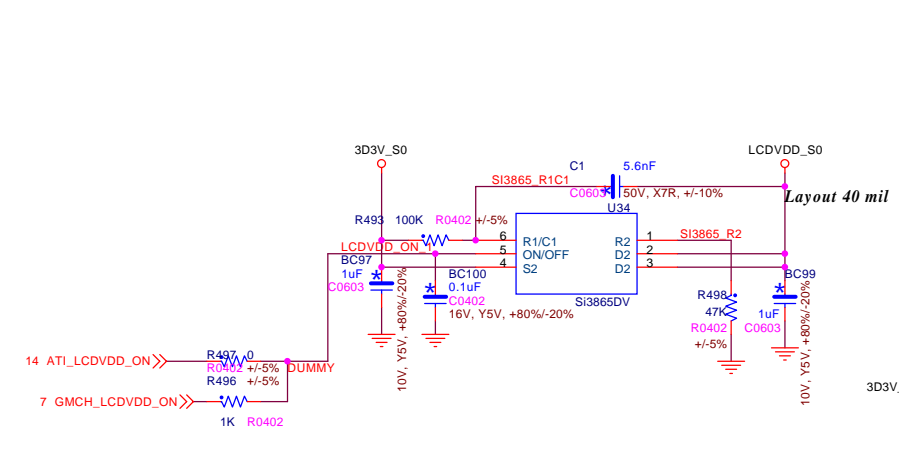
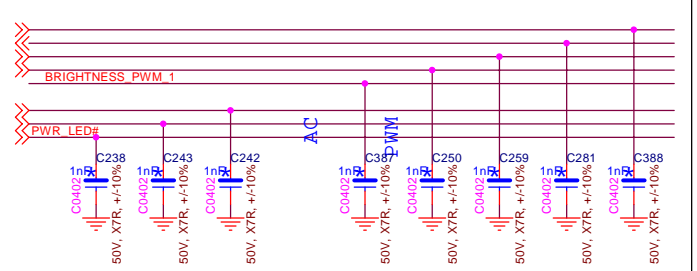




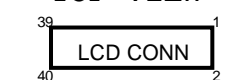
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**LED / INVERTER**



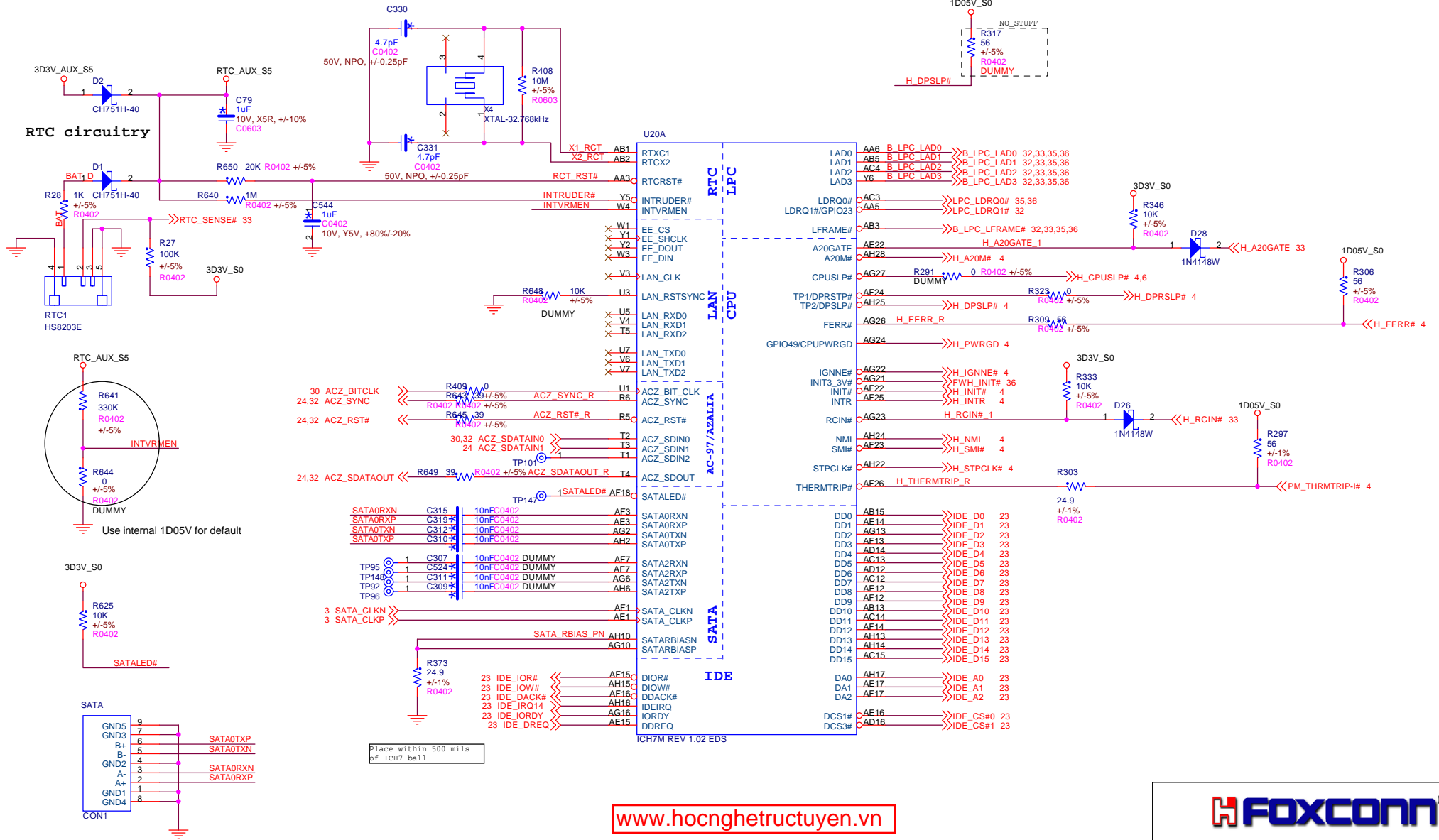
**LCD CONN  
TOP VIEW**





**FOXCONN ND2**

|                                   |                          |                  |
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| Title                             |                          |                  |
| <b>LVDS / Inverter</b>            |                          |                  |
| Size<br>A3                        | Document Number<br><Doc> | Rev<br><b>SA</b> |
| <b>W06N</b>                       |                          |                  |
| Date: Saturday, February 19, 2005 |                          |                  |
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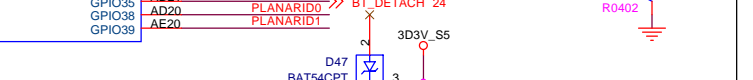
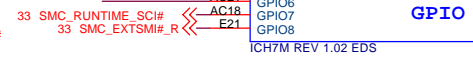
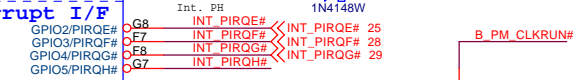
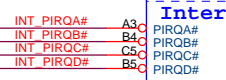
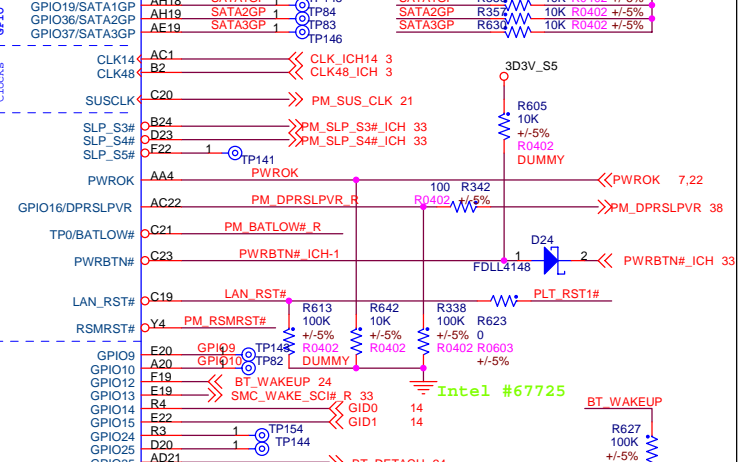
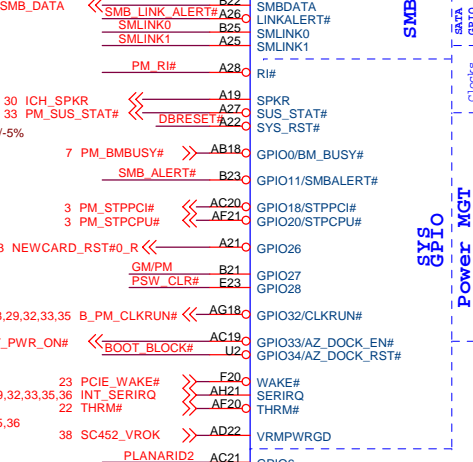
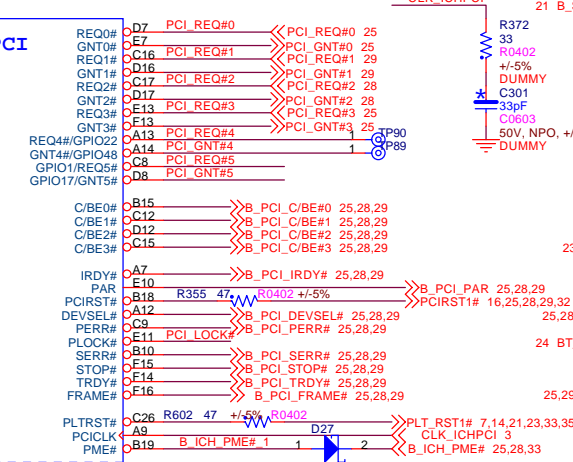
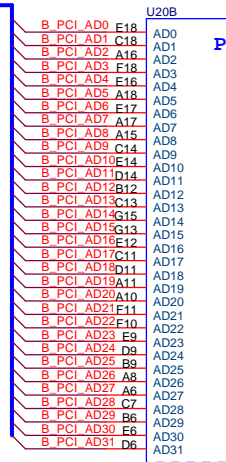
**FOXCONN**<sup>®</sup>

**FOXCONN ND2**

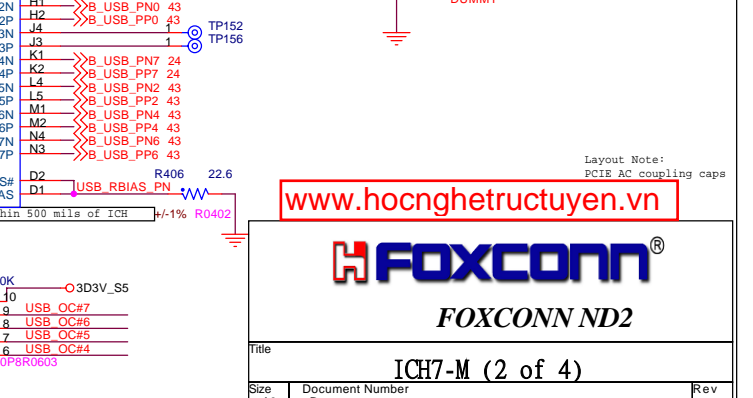
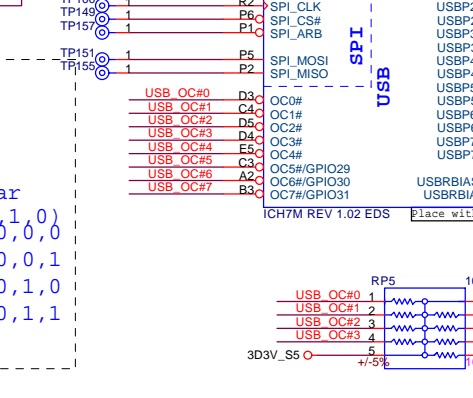
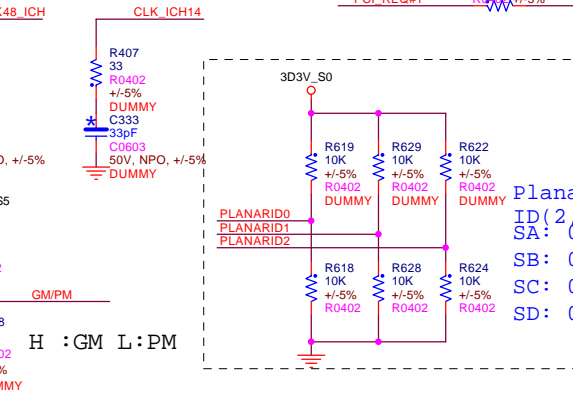
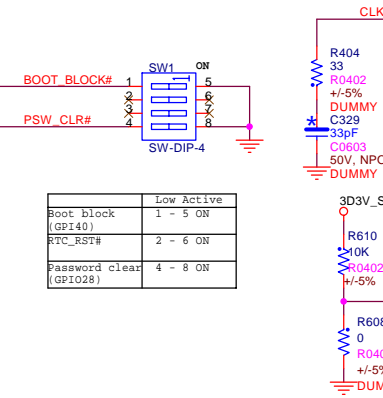
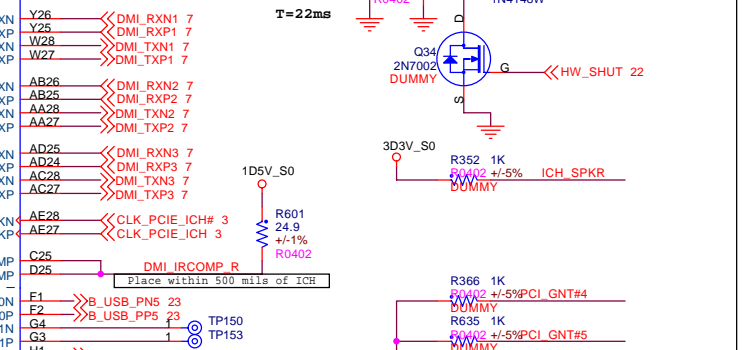
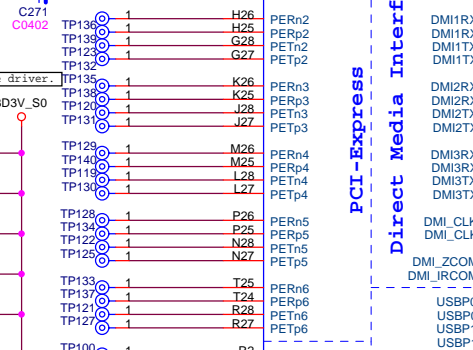
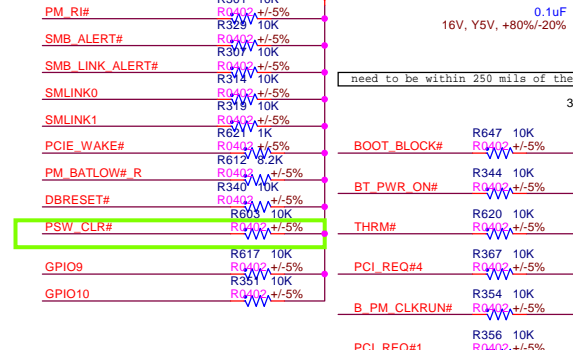
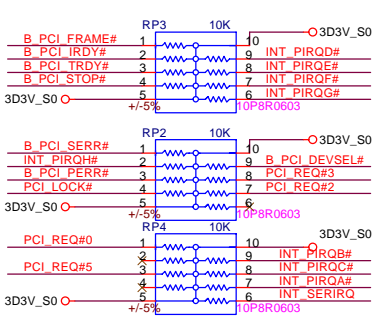
Title: ICH7-M (1 of 4)

|  |                       |             |        |
|--|-----------------------|-------------|--------|
| Size A3  | Document Number <Doc> | <b>W06N</b> | Rev SA |
| Date: Saturday, February 19, 2005 Sheet 18 of 44 |                       |             |        |

25,28,29 B\_PCI\_AD[31..0]



### ICH7 Pullups



|                         |          |
|-------------------------|----------|
| Boot block (GP140)      | 1 - 5 ON |
| RTC_RST#                | 2 - 6 ON |
| Password clear (GPIO28) | 4 - 8 ON |

Planar ID(2,1,0)  
 SA: 0,0,0  
 SB: 0,0,1  
 SC: 0,1,0  
 SD: 0,1,1

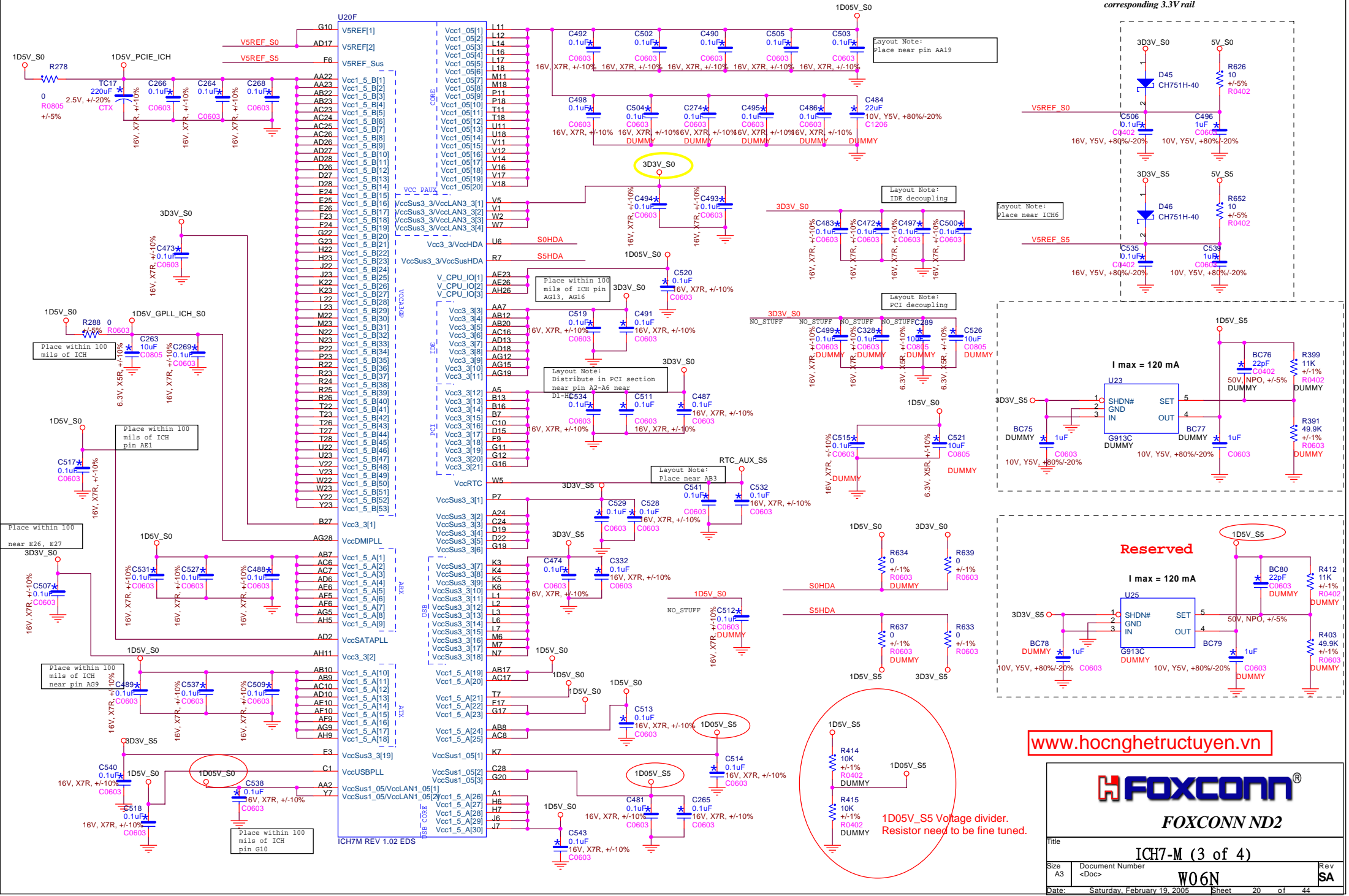
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ICH7-M (2 of 4)  
 W06N  
 Date: Saturday, February 19, 2005 Sheet 19 of 44

Layout Note:  
Place above caps within  
100 mils of ICH near F27, P27, AB27

\*Within a given well, 5VREF needs to be up before the  
corresponding 3.3V rail



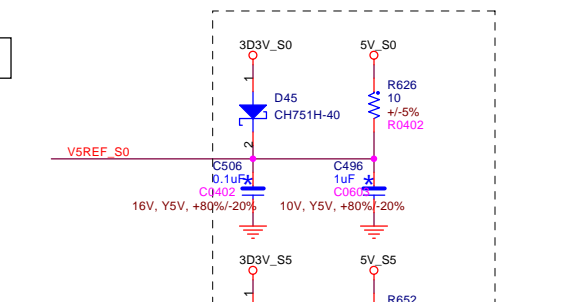
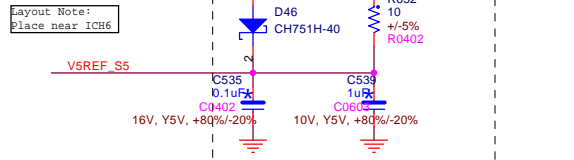
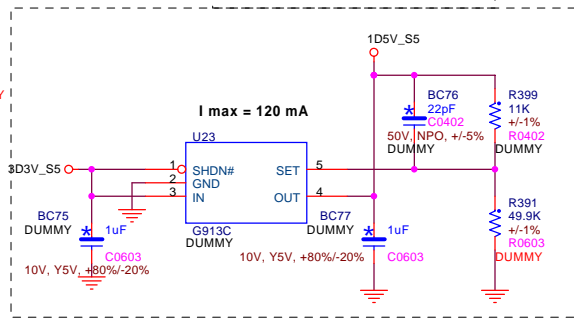
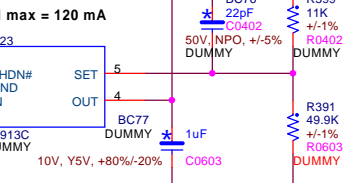
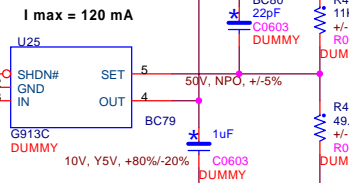
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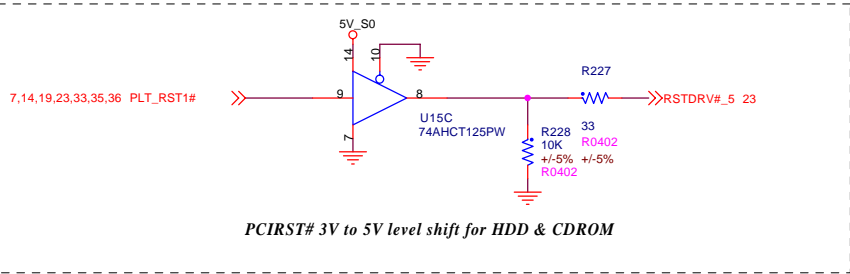
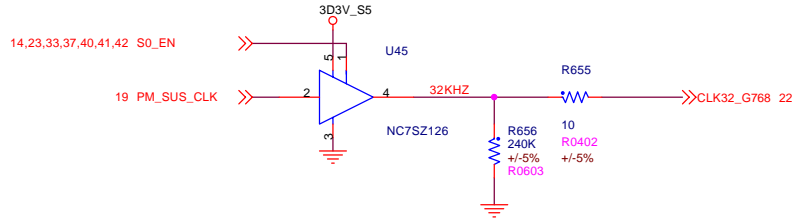
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|-------|-----------------------------|-----------------|----------|
| Title |                             | ICH7-M (3 of 4) |          |
| Size  | A3                          | Document Number | W06N     |
| Date: | Saturday, February 19, 2005 | Sheet           | 20 of 44 |

1D05V\_S5 Voltage divider.  
Resistor need to be fine tuned.

Reserved

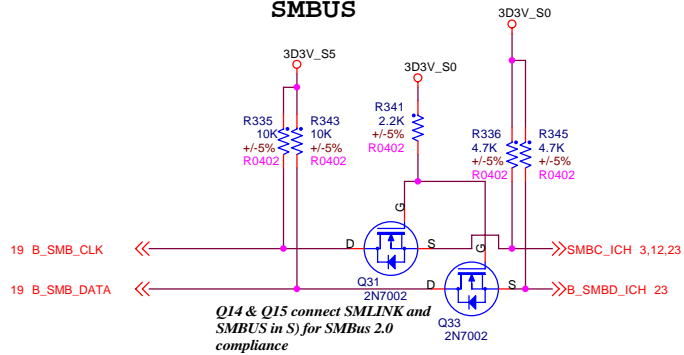


**32K suspend clock output**



*PCIRST# 3V to 5V level shift for HDD & CDROM*


**SMBUS**



*Q14 & Q15 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance*

| U20E |         |          |
|------|---------|----------|
| A4   | VSS[1]  | VSS[98]  |
| A23  | VSS[2]  | VSS[99]  |
| B1   | VSS[3]  | VSS[100] |
| B8   | VSS[4]  | VSS[101] |
| B11  | VSS[5]  | VSS[102] |
| B14  | VSS[6]  | VSS[103] |
| B17  | VSS[7]  | VSS[104] |
| B20  | VSS[8]  | VSS[105] |
| B26  | VSS[9]  | VSS[106] |
| B28  | VSS[10] | VSS[107] |
| C2   | VSS[11] | VSS[108] |
| C6   | VSS[12] | VSS[109] |
| C27  | VSS[13] | VSS[110] |
| D10  | VSS[14] | VSS[111] |
| D13  | VSS[15] | VSS[112] |
| D18  | VSS[16] | VSS[113] |
| D21  | VSS[17] | VSS[114] |
| D24  | VSS[18] | VSS[115] |
| E1   | VSS[19] | VSS[116] |
| E2   | VSS[20] | VSS[117] |
| E4   | VSS[21] | VSS[118] |
| E8   | VSS[22] | VSS[119] |
| E15  | VSS[23] | VSS[120] |
| F3   | VSS[24] | VSS[121] |
| F4   | VSS[25] | VSS[122] |
| F5   | VSS[26] | VSS[123] |
| F12  | VSS[27] | VSS[124] |
| F27  | VSS[28] | VSS[125] |
| F28  | VSS[29] | VSS[126] |
| G1   | VSS[30] | VSS[127] |
| G2   | VSS[31] | VSS[128] |
| G6   | VSS[32] | VSS[129] |
| G6   | VSS[33] | VSS[130] |
| G9   | VSS[34] | VSS[131] |
| G14  | VSS[35] | VSS[132] |
| G18  | VSS[36] | VSS[133] |
| G21  | VSS[37] | VSS[134] |
| G24  | VSS[38] | VSS[135] |
| G25  | VSS[39] | VSS[136] |
| G26  | VSS[40] | VSS[137] |
| H3   | VSS[41] | VSS[138] |
| H4   | VSS[42] | VSS[139] |
| H5   | VSS[43] | VSS[140] |
| H24  | VSS[44] | VSS[141] |
| H27  | VSS[45] | VSS[142] |
| H28  | VSS[46] | VSS[143] |
| J1   | VSS[47] | VSS[144] |
| J2   | VSS[48] | VSS[145] |
| J5   | VSS[49] | VSS[146] |
| J24  | VSS[50] | VSS[147] |
| J25  | VSS[51] | VSS[148] |
| J26  | VSS[52] | VSS[149] |
| K24  | VSS[53] | VSS[150] |
| K27  | VSS[54] | VSS[151] |
| K28  | VSS[55] | VSS[152] |
| L13  | VSS[56] | VSS[153] |
| L15  | VSS[57] | VSS[154] |
| L25  | VSS[58] | VSS[155] |
| L26  | VSS[59] | VSS[156] |
| M3   | VSS[60] | VSS[157] |
| M4   | VSS[61] | VSS[158] |
| M5   | VSS[62] | VSS[159] |
| M12  | VSS[63] | VSS[160] |
| M13  | VSS[64] | VSS[161] |
| M14  | VSS[65] | VSS[162] |
| M15  | VSS[66] | VSS[163] |
| M16  | VSS[67] | VSS[164] |
| M17  | VSS[68] | VSS[165] |
| M24  | VSS[69] | VSS[166] |
| M27  | VSS[70] | VSS[167] |
| M28  | VSS[71] | VSS[168] |
| N1   | VSS[72] | VSS[169] |
| N2   | VSS[73] | VSS[170] |
| N5   | VSS[74] | VSS[171] |
| N6   | VSS[75] | VSS[172] |
| N11  | VSS[76] | VSS[173] |
| N12  | VSS[77] | VSS[174] |
| N13  | VSS[78] | VSS[175] |
| N14  | VSS[79] | VSS[176] |
| N15  | VSS[80] | VSS[177] |
| N16  | VSS[81] | VSS[178] |
| N17  | VSS[82] | VSS[179] |
| N18  | VSS[83] | VSS[180] |
| N24  | VSS[84] | VSS[181] |
| N25  | VSS[85] | VSS[182] |
| N26  | VSS[86] | VSS[183] |
| P3   | VSS[87] | VSS[184] |
| P4   | VSS[88] | VSS[185] |
| P12  | VSS[89] | VSS[186] |
| P13  | VSS[90] | VSS[187] |
| P14  | VSS[91] | VSS[188] |
| P15  | VSS[92] | VSS[189] |
| P16  | VSS[93] | VSS[190] |
| P17  | VSS[94] | VSS[191] |
| P24  | VSS[95] | VSS[192] |
| P27  | VSS[96] | VSS[193] |
|      | VSS[97] | VSS[194] |

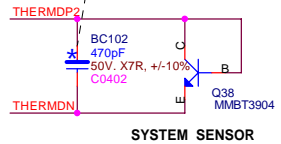
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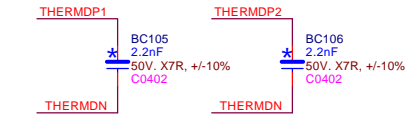
**FOXCONN ND2**

|                 |                             |                |
|-----------------|-----------------------------|----------------|
| Title           |                             |                |
| ICH7-M (4 of 4) |                             |                |
| Size            | Document Number             | Rev            |
| A3              | <Doc>                       | SA             |
| W06N            |                             |                |
| Date:           | Saturday, February 19, 2005 | Sheet 21 of 44 |

Put these two Caps near the thermal diode.



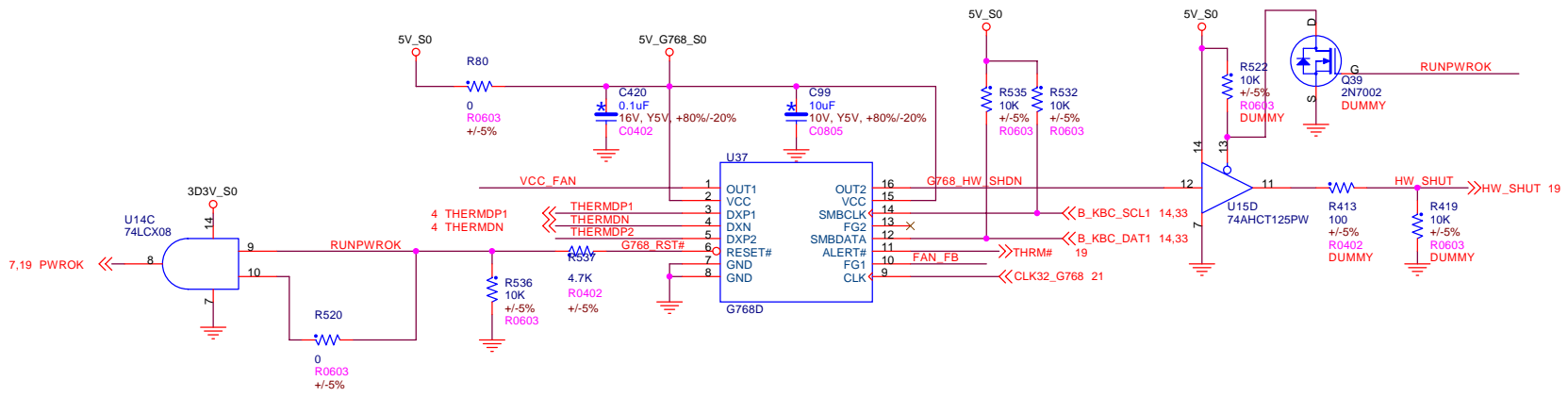
SYSTEM SENSOR



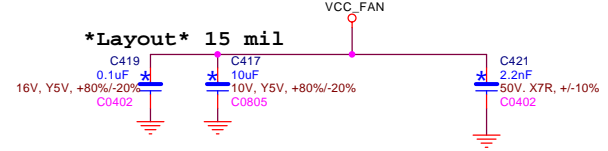
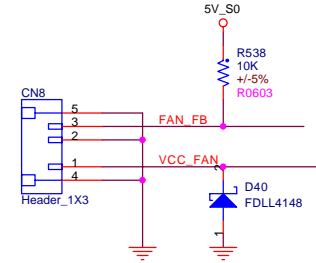
THERMDP1/DP2/THERMDN ON THE SAME LAYER  
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS  
CAPS CLOSE TO G768B

HW thermal shut down temperature  
setting 95 degree . Put Near CPU .

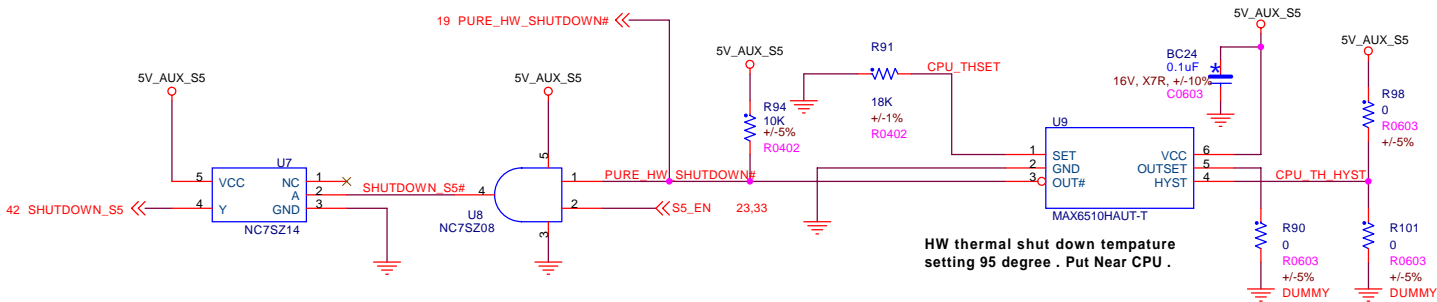
Reserve for G768B  
works at High  
Speed



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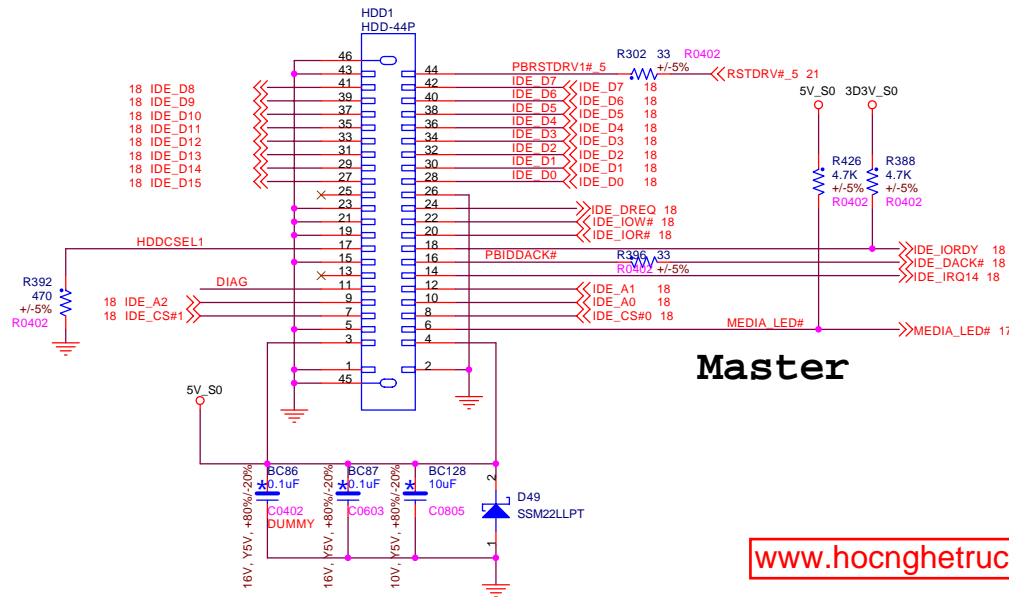
\*Layout\* 15 mil



HW thermal shut down temperature  
setting 95 degree . Put Near CPU .

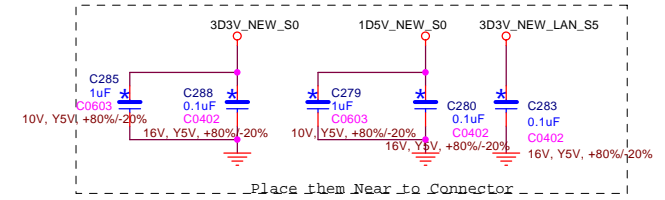
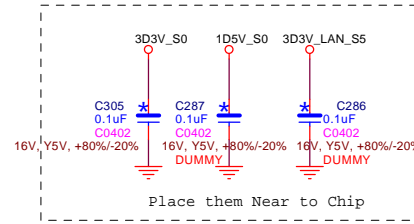
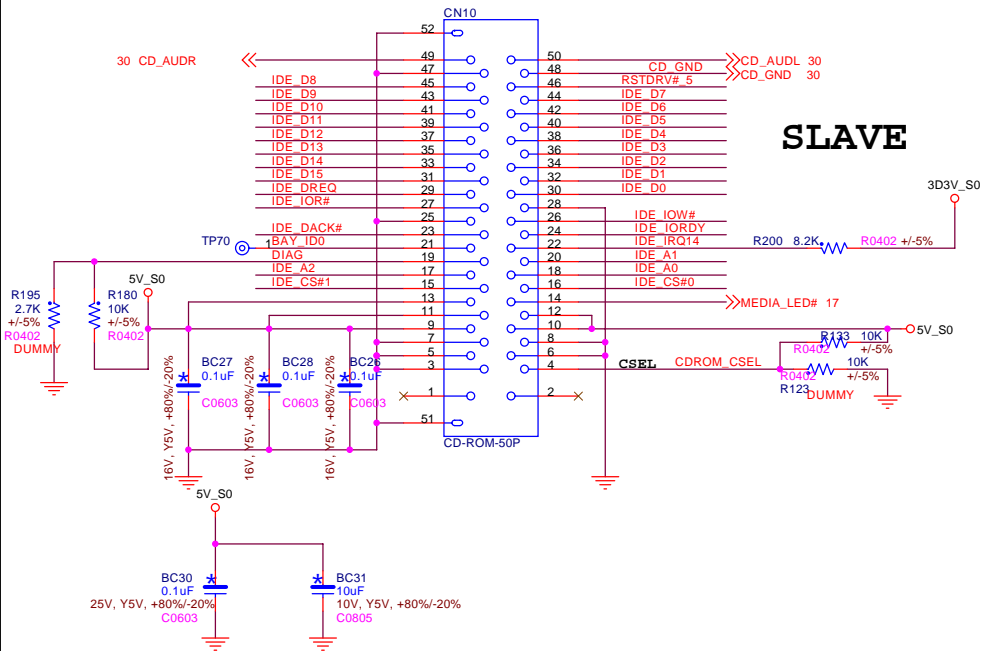


# HDD Connector

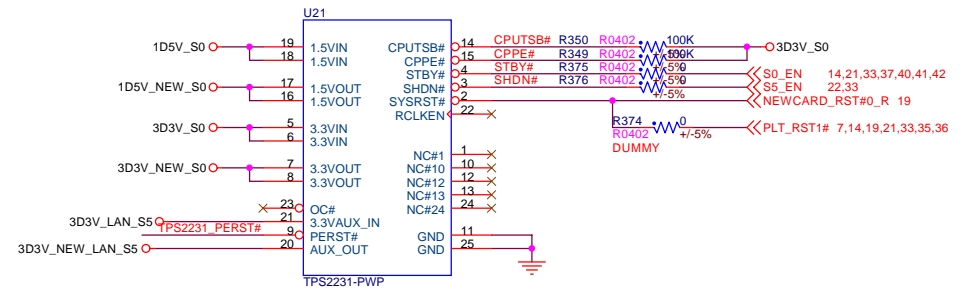
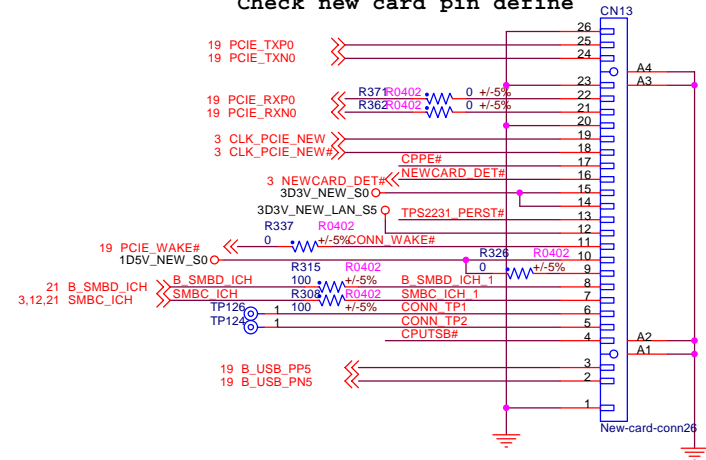


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# CDROM



## Check new card pin define

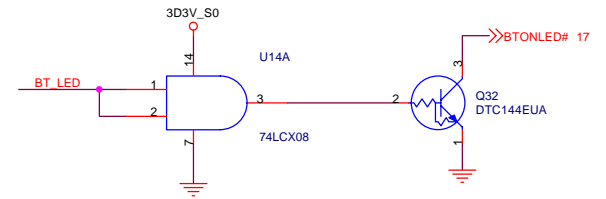
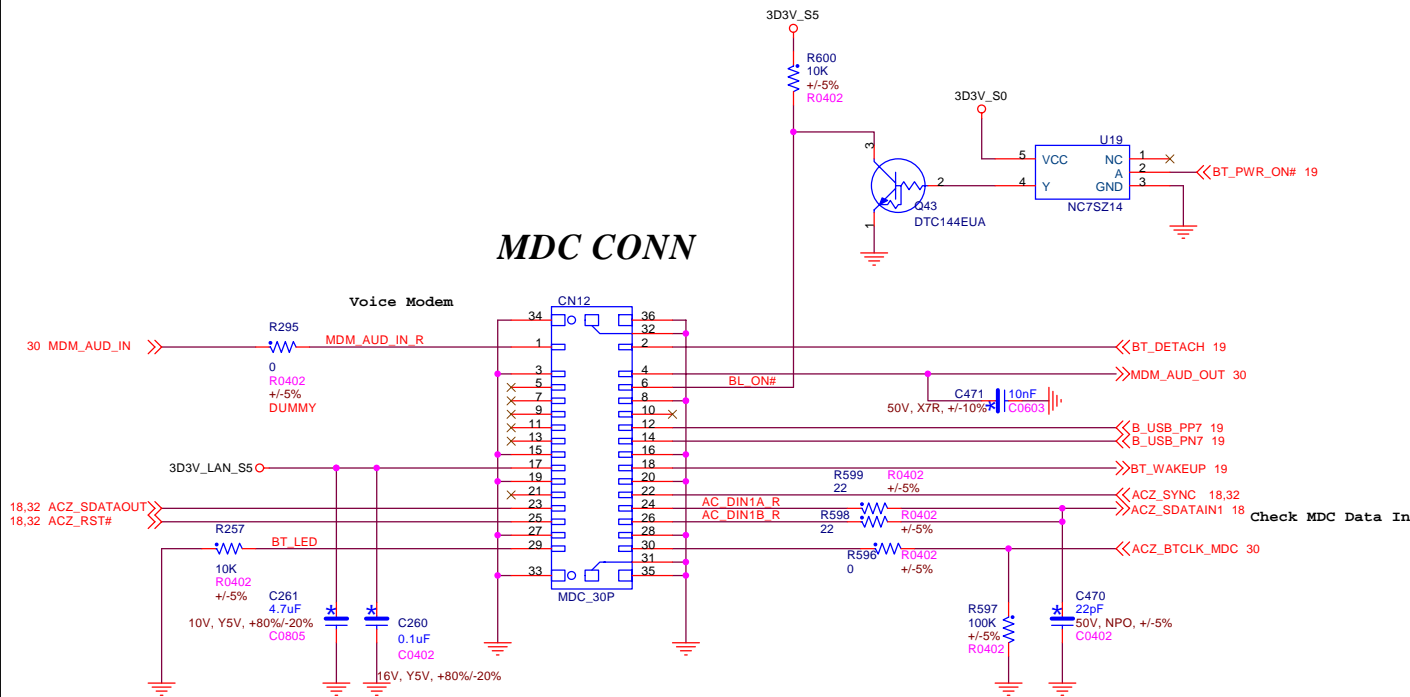


**FOXCONN**

FOXCONN ND2

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|-------|-----------------------------|-------|--------------------|----|----|
| Title |                             |       | SATA/CDROM/NEWCARD |    |    |
| Size  | Document Number             |       | Rev                |    |    |
| A3    | <Doc>                       |       | SA                 |    |    |
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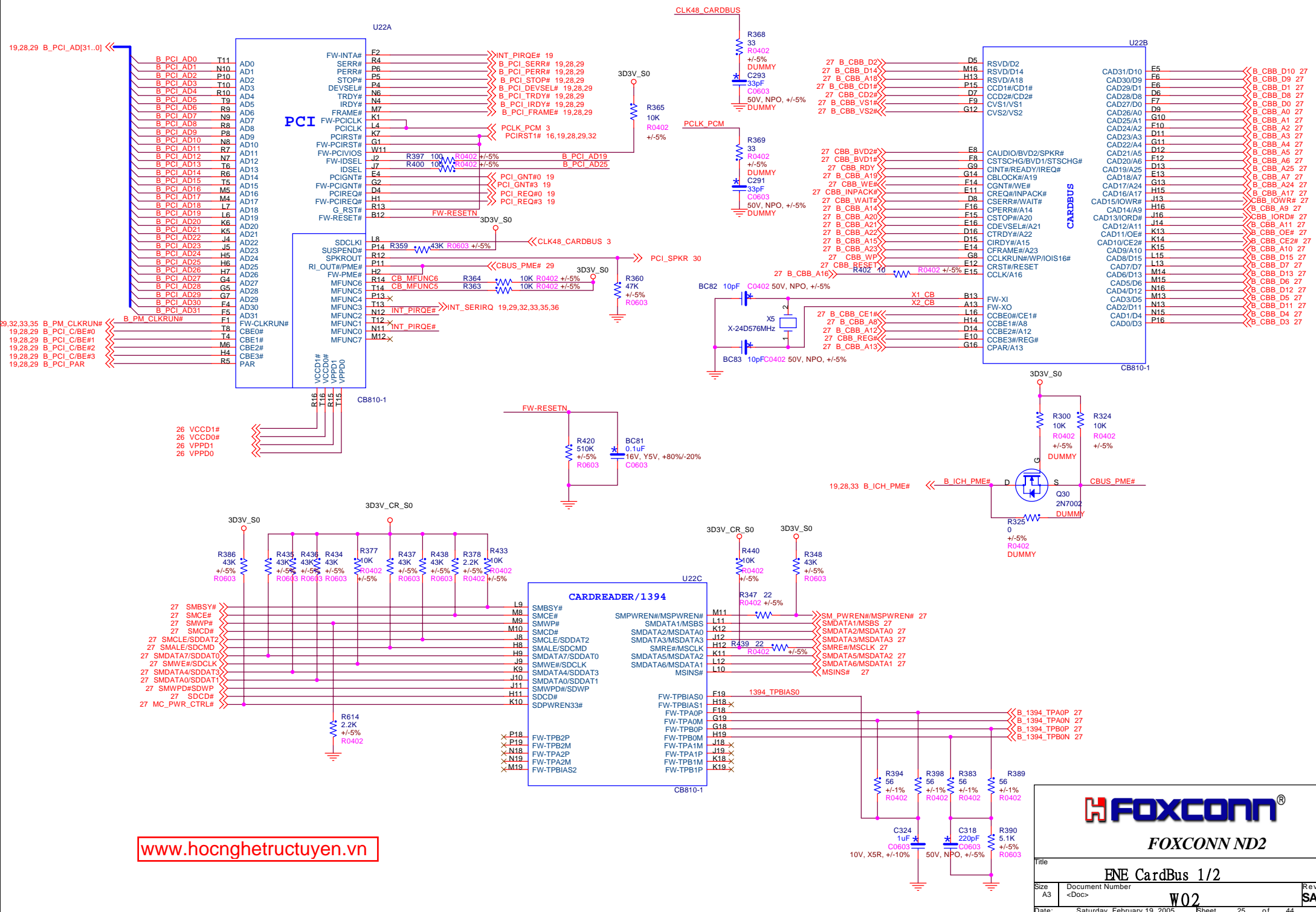
### MDC CONN



FOXCONN ND2

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|-------|-----------------------------|-------|----------|
| Title |                             | MDC   |          |
| Size  | Document Number             | Rev   |          |
| A3    | <Doc>                       | SA    |          |
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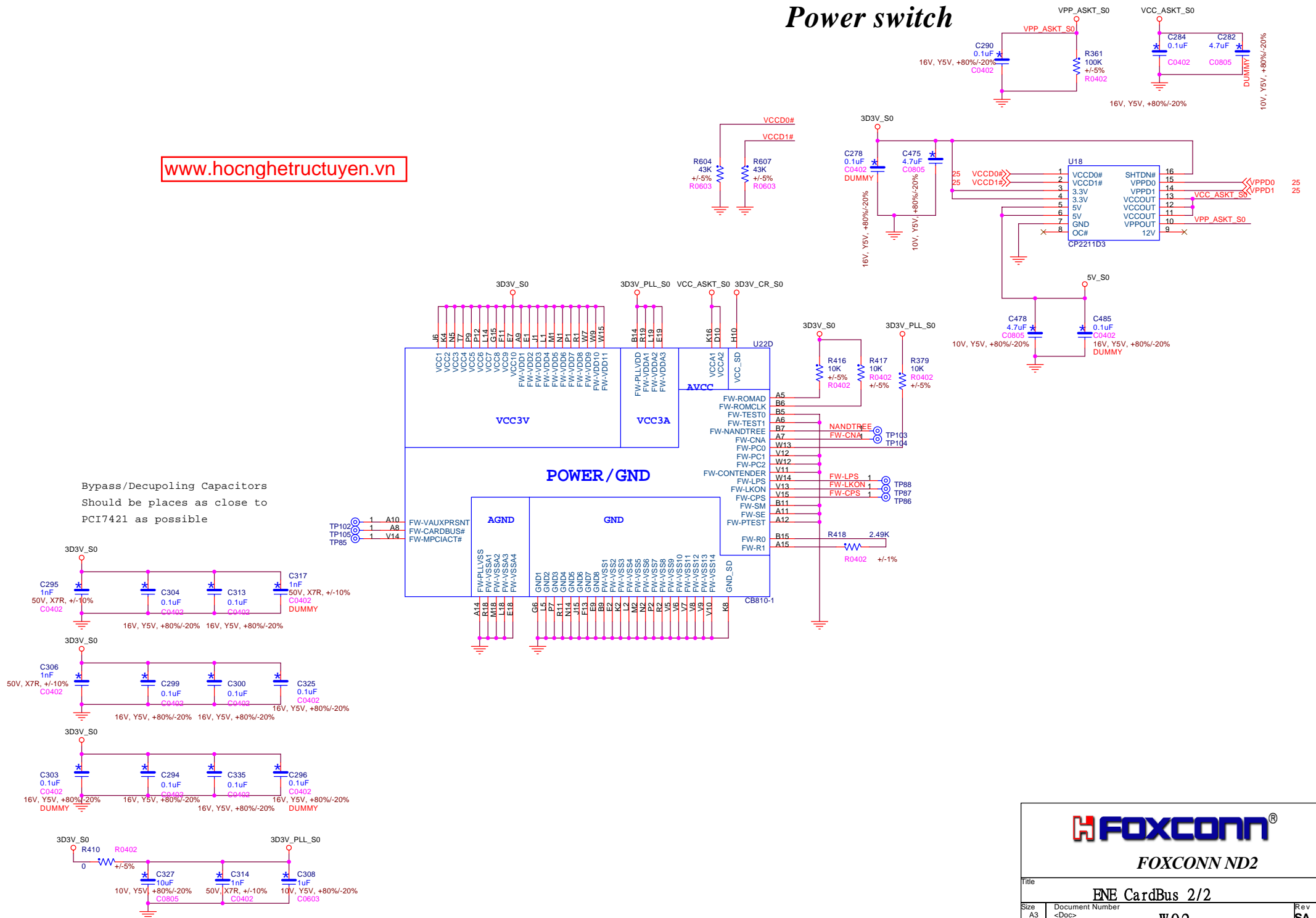
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|       |                             |                 |          |
|-------|-----------------------------|-----------------|----------|
| Title |                             | ENE CardBus 1/2 |          |
| Size  | A3                          | Document Number | W02      |
| Date: | Saturday, February 19, 2005 | Sheet           | 25 of 44 |
| Rev   | SA                          |                 |          |

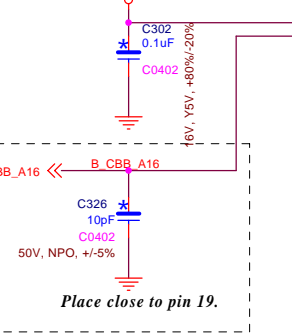
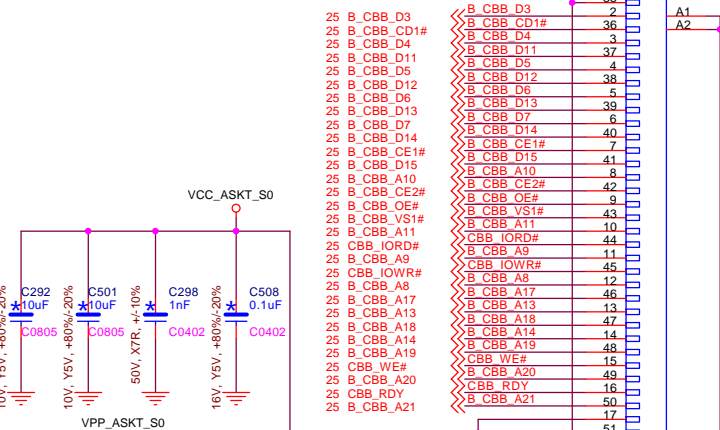
# Power switch

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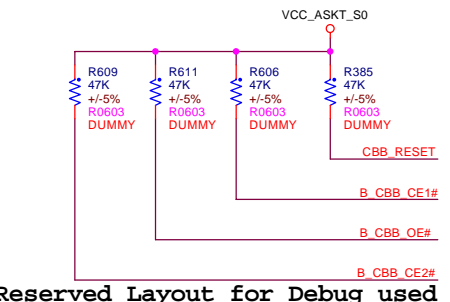


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| ENE CardBus 2/2 |                             |       |          |
| Size            | Document Number             | Rev   |          |
| A3              | <Doc>                       | W02   | SA       |
| Date:           | Saturday, February 19, 2005 | Sheet | 26 of 44 |

# PCMCIA Socket



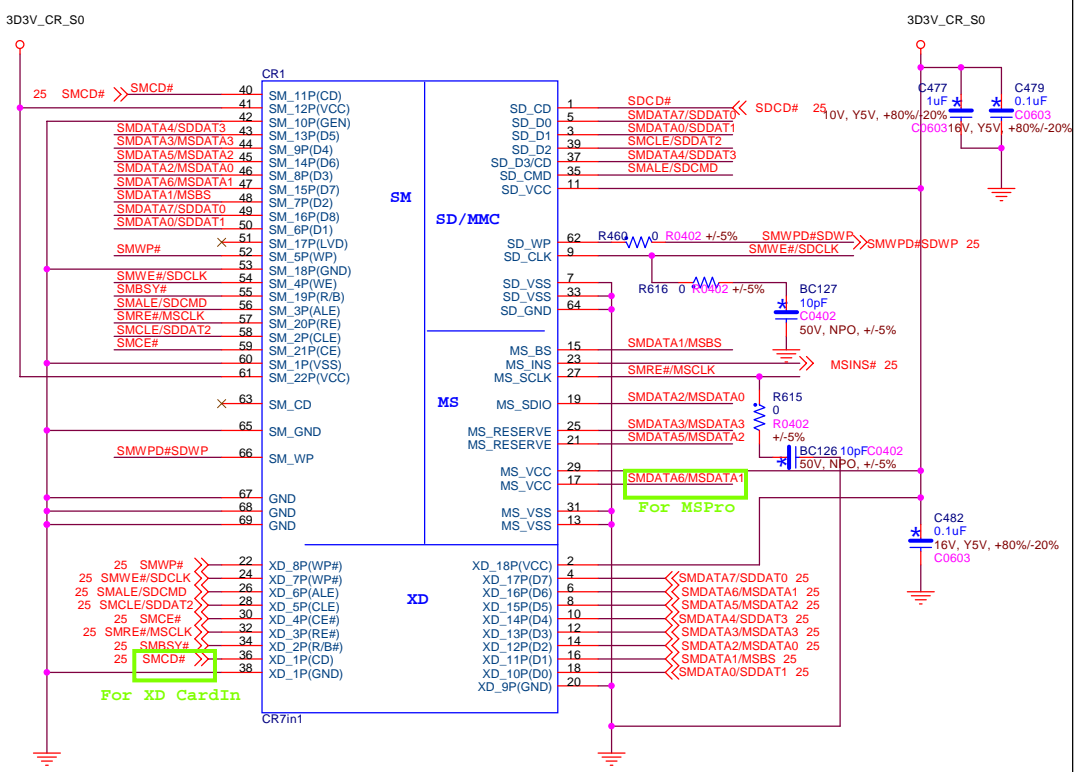
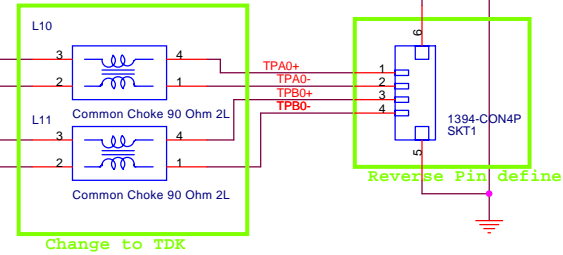
Clock AC termination  
33MHz clock for 32-bit  
Cardbus card I/F



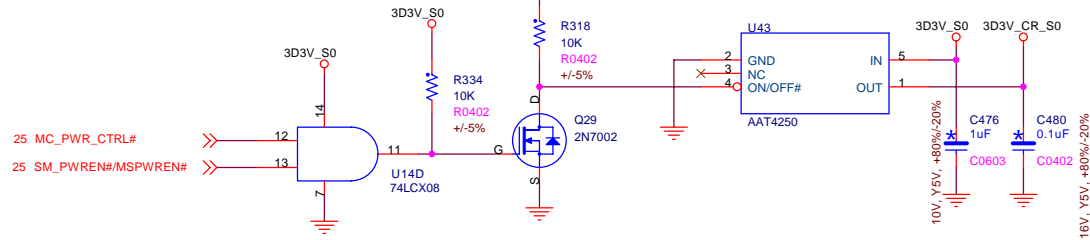
Reserved Layout for Debug used

# 1394 Connector

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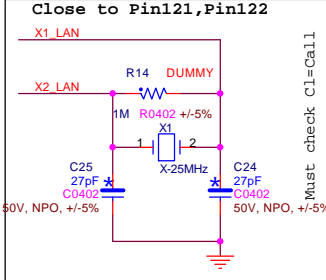


## Card Reader POWER SWITCH

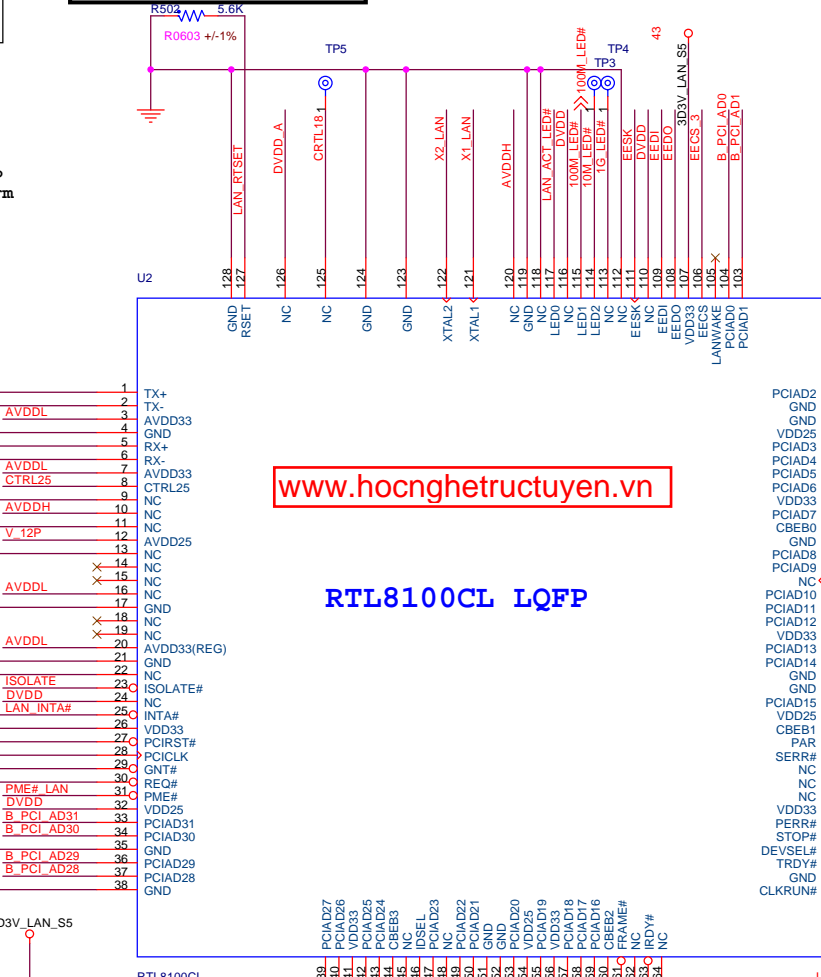
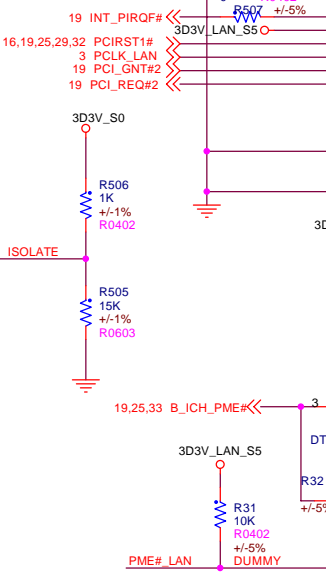
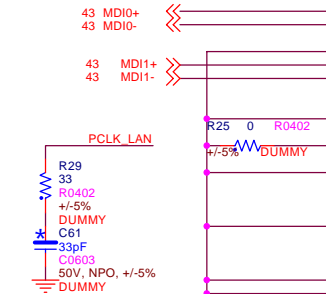
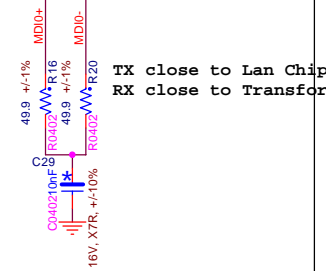
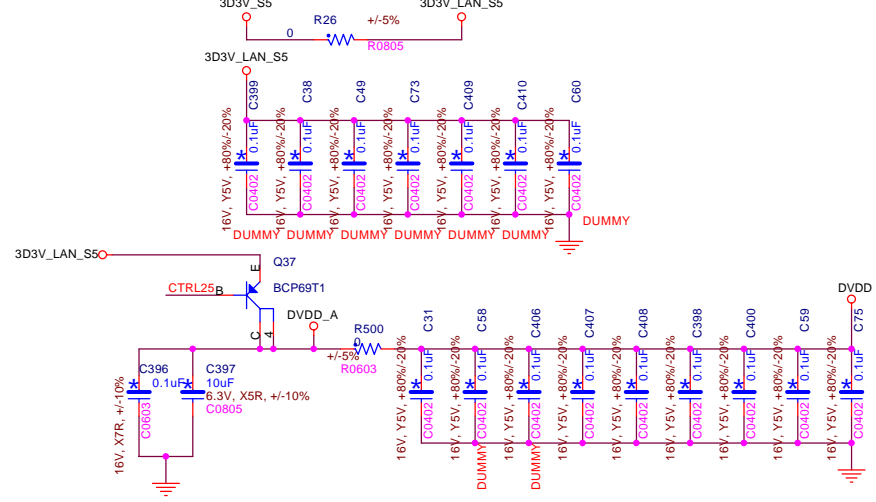
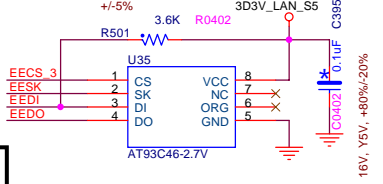


**FOXCONN**  
FOXCONN ND2

File: PCMCIA SLOT / 1394 CONN.  
Size: A3 Document Number: <Doc> Rev: SA  
Date: Saturday, February 19, 2005 Sheet: 27 of 44



R827 value should be 5.6K at RTL8100CL application, and 2.49K at RTL8110SBL application.



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>>>B\_PCI\_AD[31..0] 19,25,29

<<<B\_PCI\_C/BE#0 19,25,29

<<<B\_PCI\_C/BE#1 19,25,29

<<<B\_PCI\_PAR 19,25,29

<<<B\_PCI\_SERR# 19,25,29

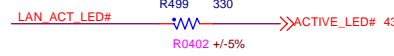
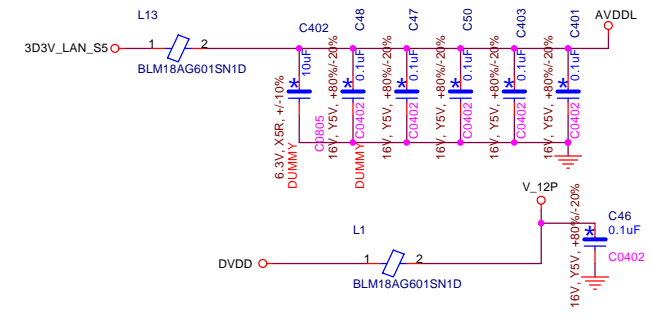
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<<<B\_PCI\_STOP# 19,25,29

<<<B\_PCI\_DEVSEL# 19,25,29

<<<B\_PCI\_TRDY# 19,25,29

<<<B\_PM\_CLKRUN# 19,25,29,32,33,35



**FOXCONN**<sup>®</sup>

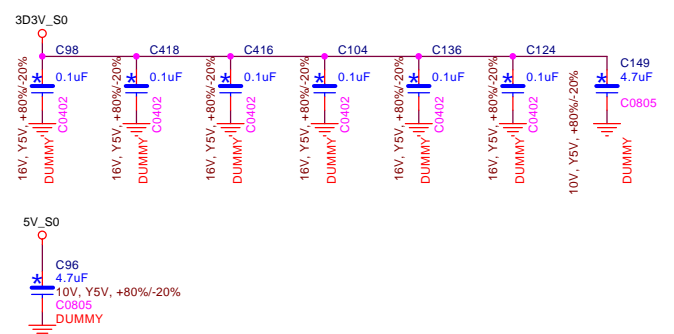
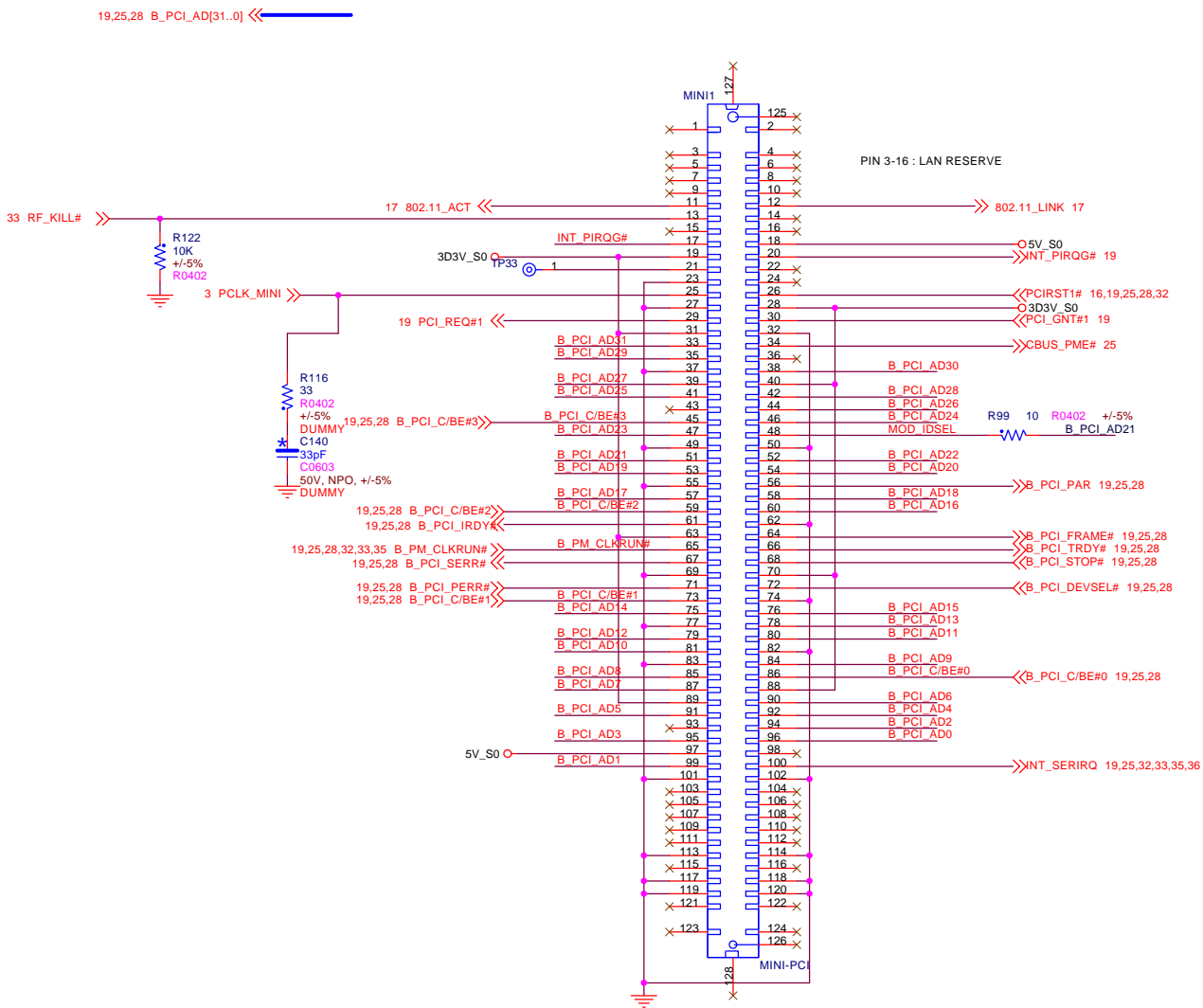
FOXCONN ND2

Title  
**LAN RTL8100CL**

Size A3 Document Number <Doc> Rev SA

W02

Date: Saturday, February 19, 2005 Sheet 28 of 44



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**FOXCONN**<sup>®</sup>

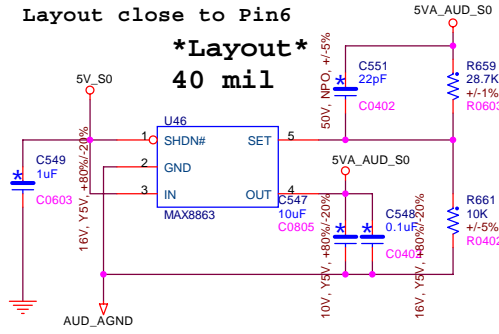
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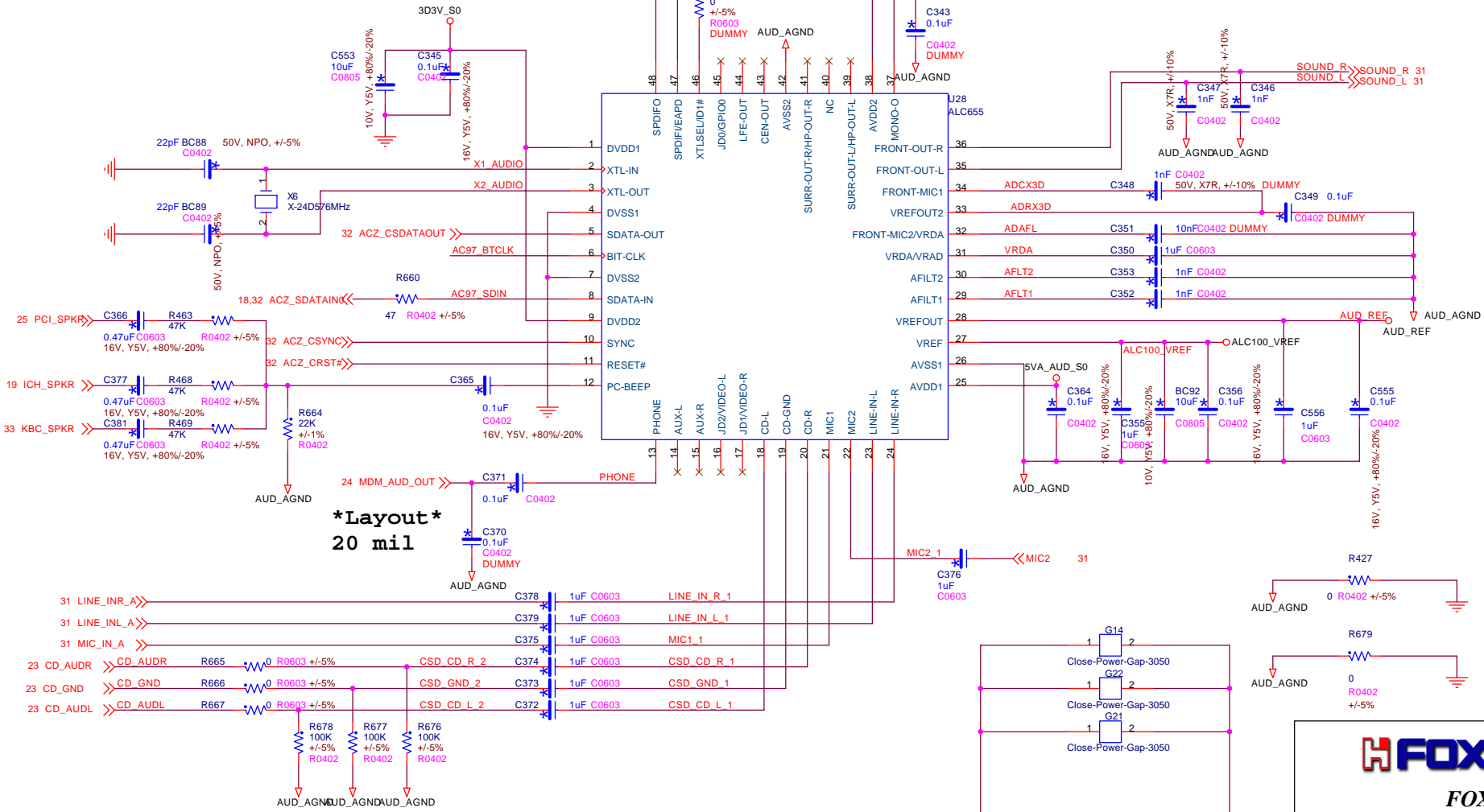
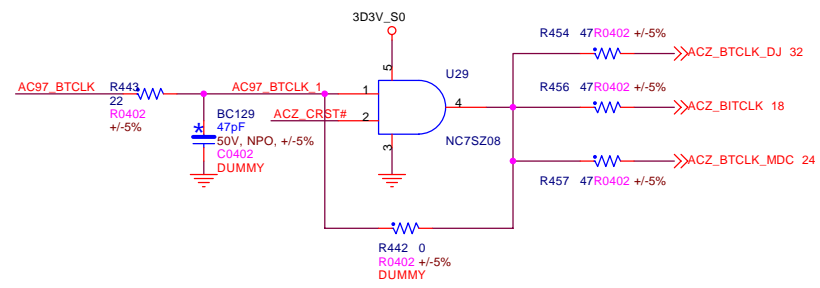
|                                   |                        |         |
|-----------------------------------|------------------------|---------|
| Size: A3                          | Document Number: <Doc> | Rev: SA |
| Date: Saturday, February 19, 2005 | Sheet: 29 of 44        |         |

F&E suggest  
Layout close to Pin6

**\*Layout\*  
40 mil**



Low for internal CLK  
NC for external CLK



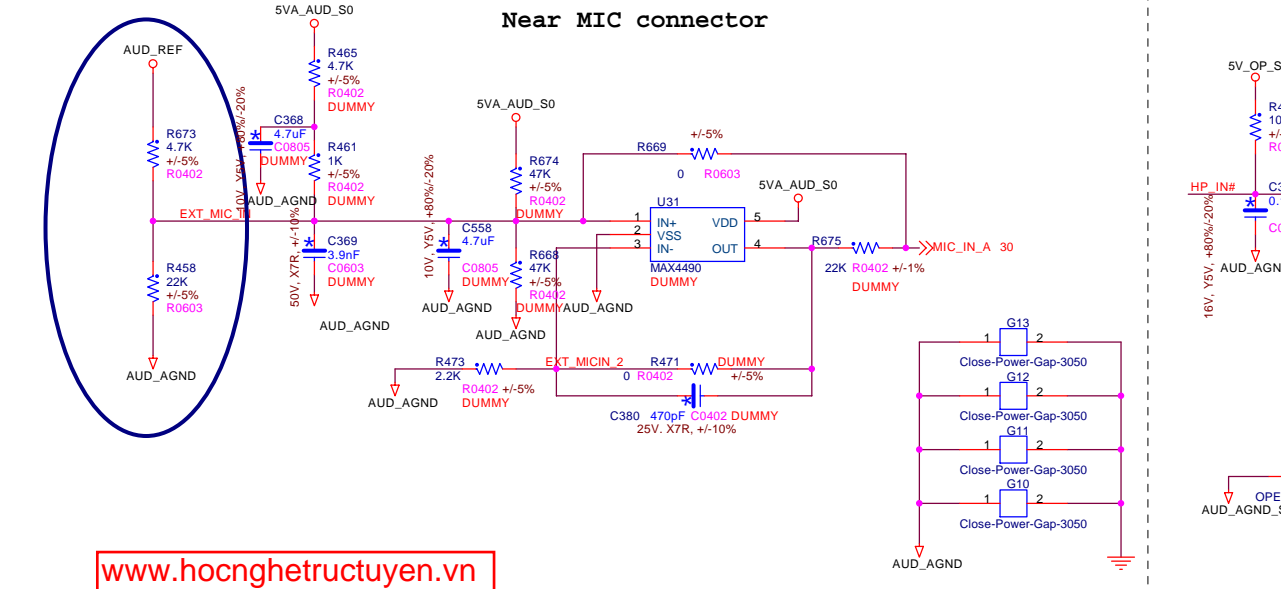
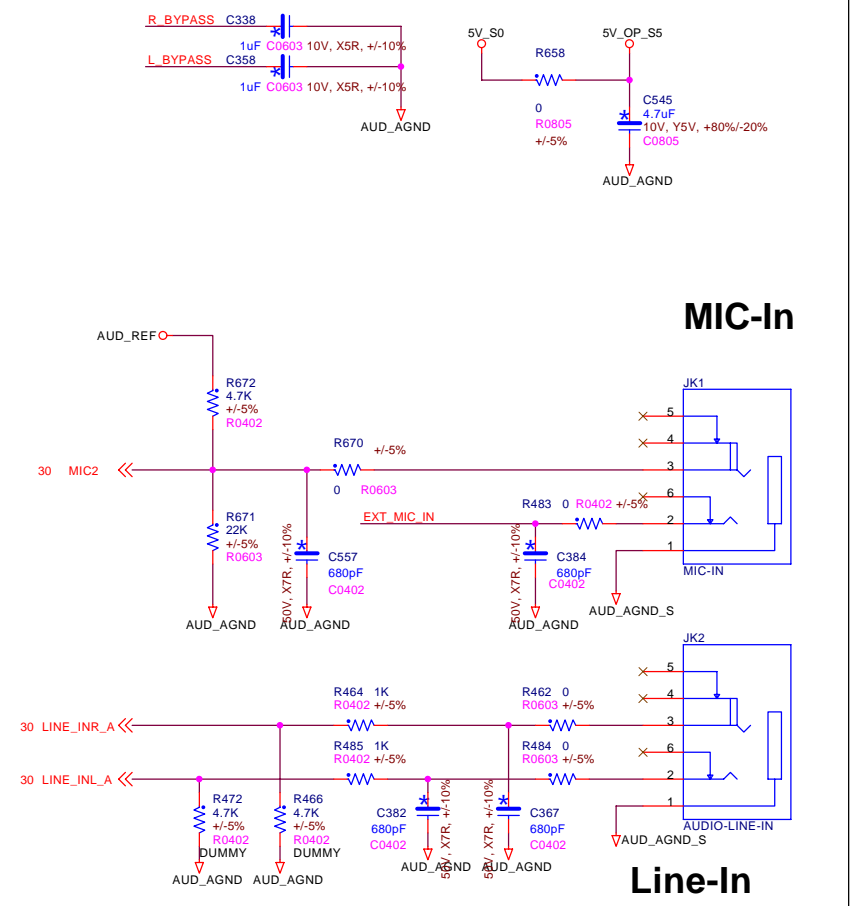
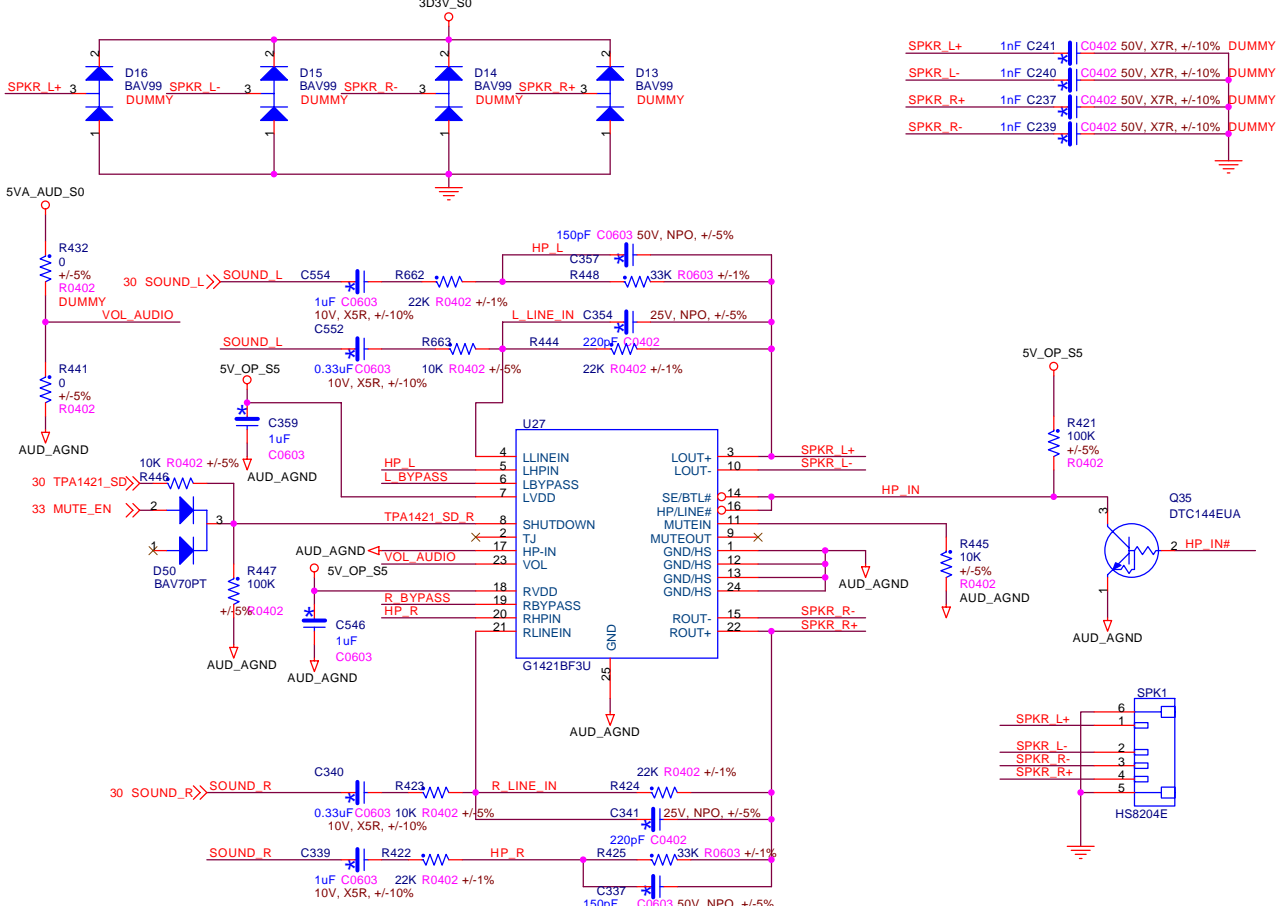
**\*Layout\*  
20 mil**

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**FOXCONN**  
FOXCONN ND2

Title: AC97 code

|                                   |                        |                 |
|-----------------------------------|------------------------|-----------------|
| Size: A3                          | Document Number: <Doc> | Rev: SA         |
| Date: Saturday, February 19, 2005 |                        | Sheet: 30 of 44 |



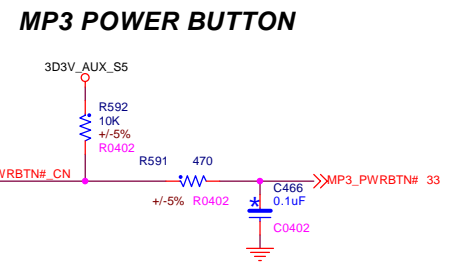
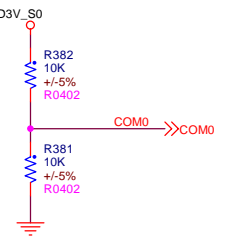
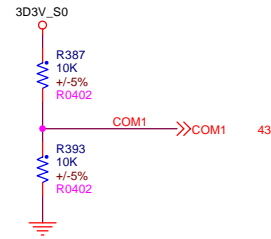
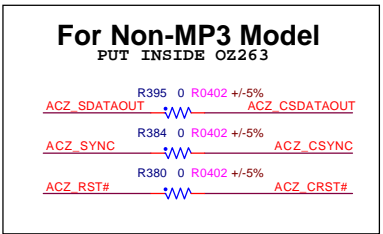
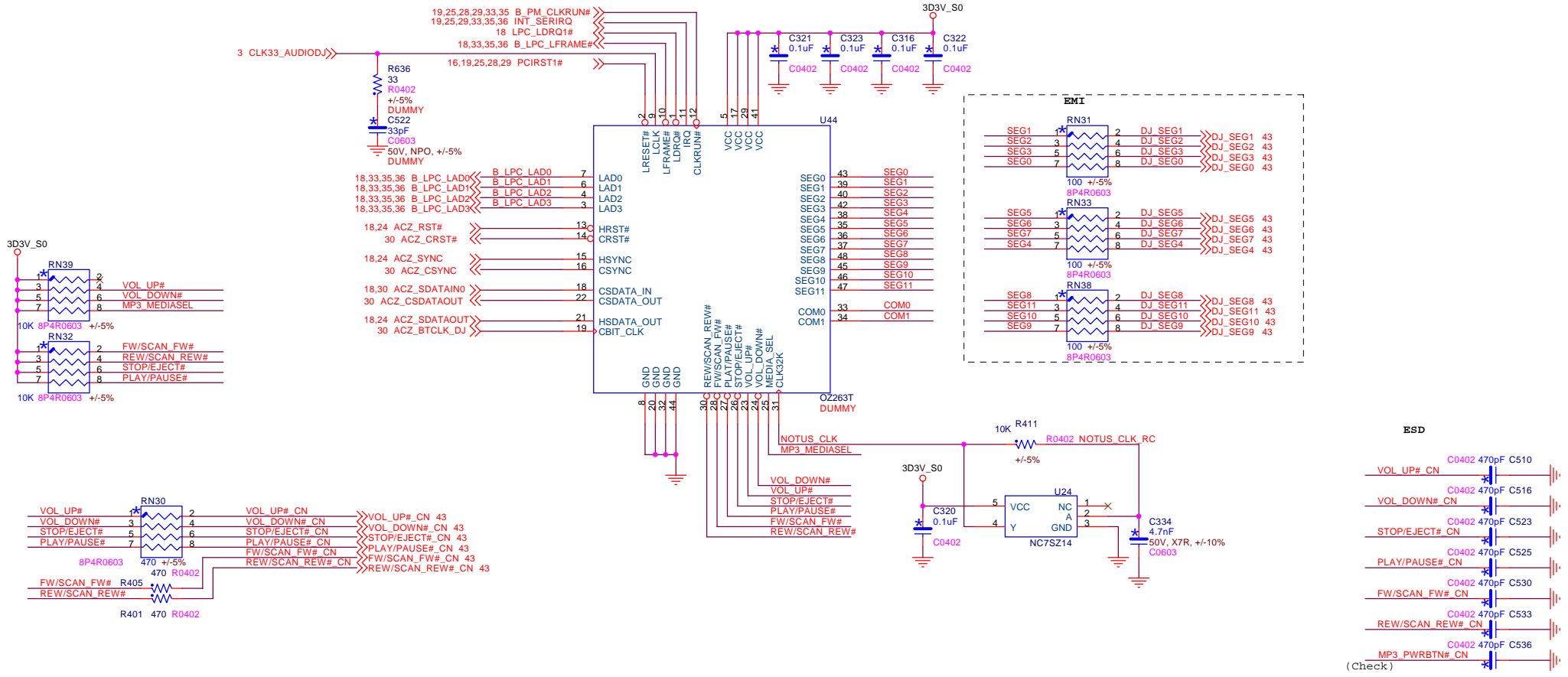
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**FOXCONN ND2**

Title: **Audio AMP and Jack**

Size: A3 | Document Number: <Doc> | Rev: SA

Date: Saturday, February 19, 2005 | Sheet: 31 of 44



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**FOXCONN ND2**

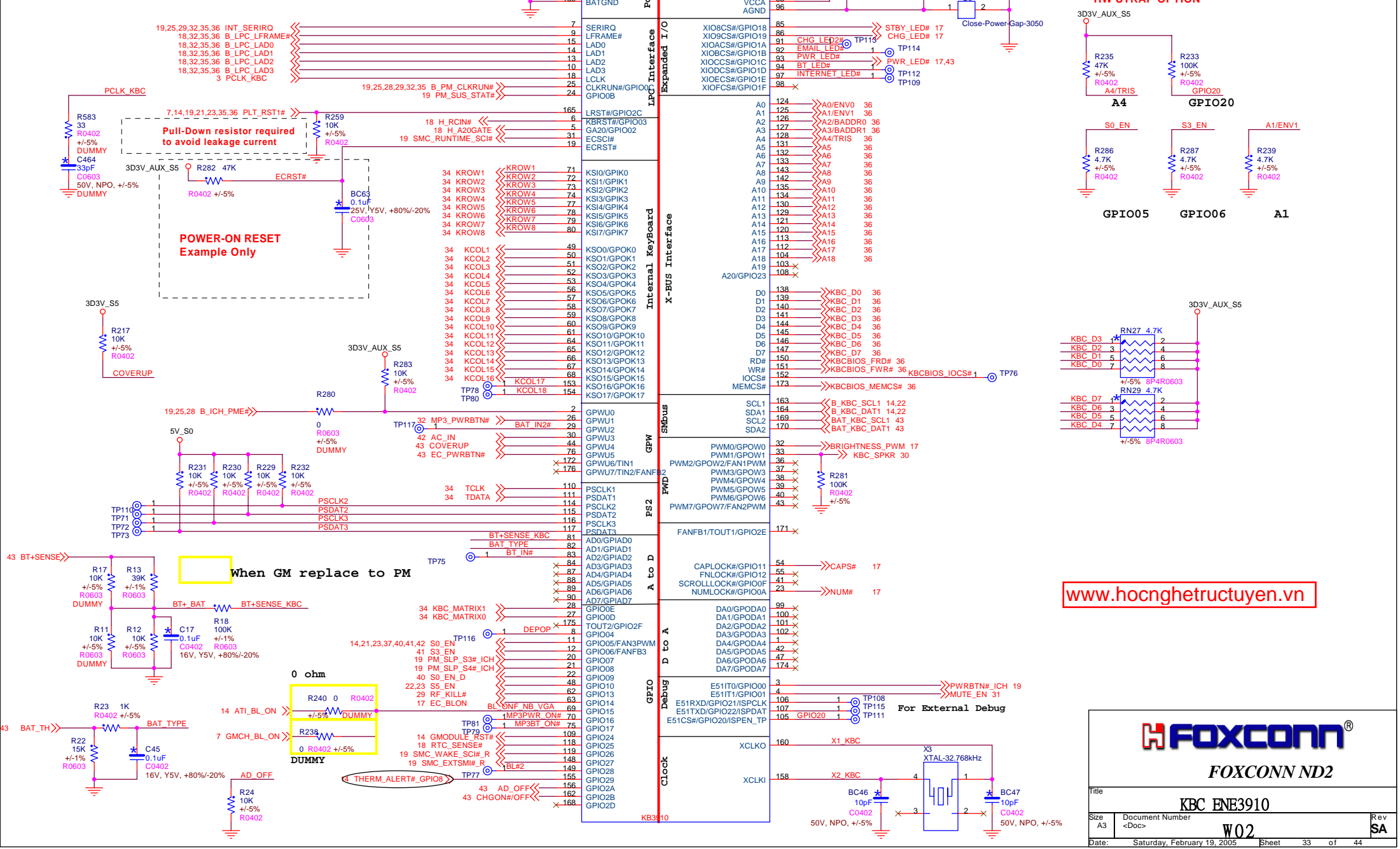
Title: OZ263

Size: A3 Document Number: W02 Rev: SA

Date: Saturday, February 19, 2005 Sheet: 32 of 44



- Rev 1.1:  
 1. Change RS232 NTXD/NRXD connection  
 2. Change PS/2 interface pull-up to VCC5  
 3. Change Flash ROM Power to VCC3\_ALWAYS  
 4. Change HW strap pull-up to VCC3\_ALWAYS
- Rev 1.2  
 1. Change SRAM to 128Kx8
- Rev 1.3  
 1. Fix FAN1PWM and FAN2PWM Pin#
- Rev 1.4  
 1. Correct HW Strap pin 124 to pin 125



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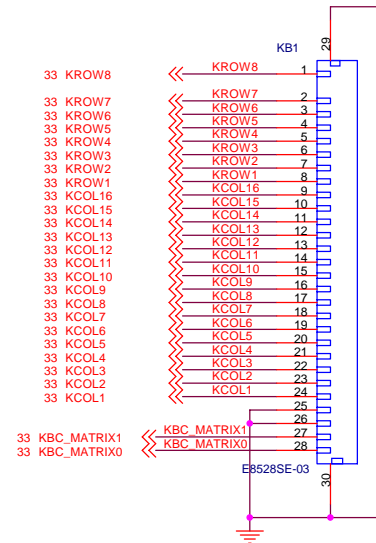
Title: KBC ENE3910

Size: A3 | Document Number: W.02 | Rev: SA

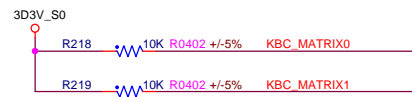
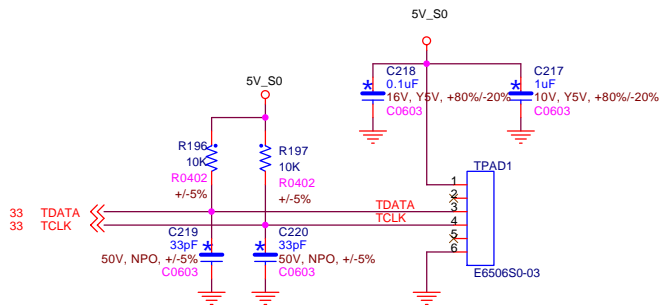
Date: Saturday, February 19, 2005 | Sheet: 33 of 44

## Internal KeyBoard Connector

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## TouchPad Connector



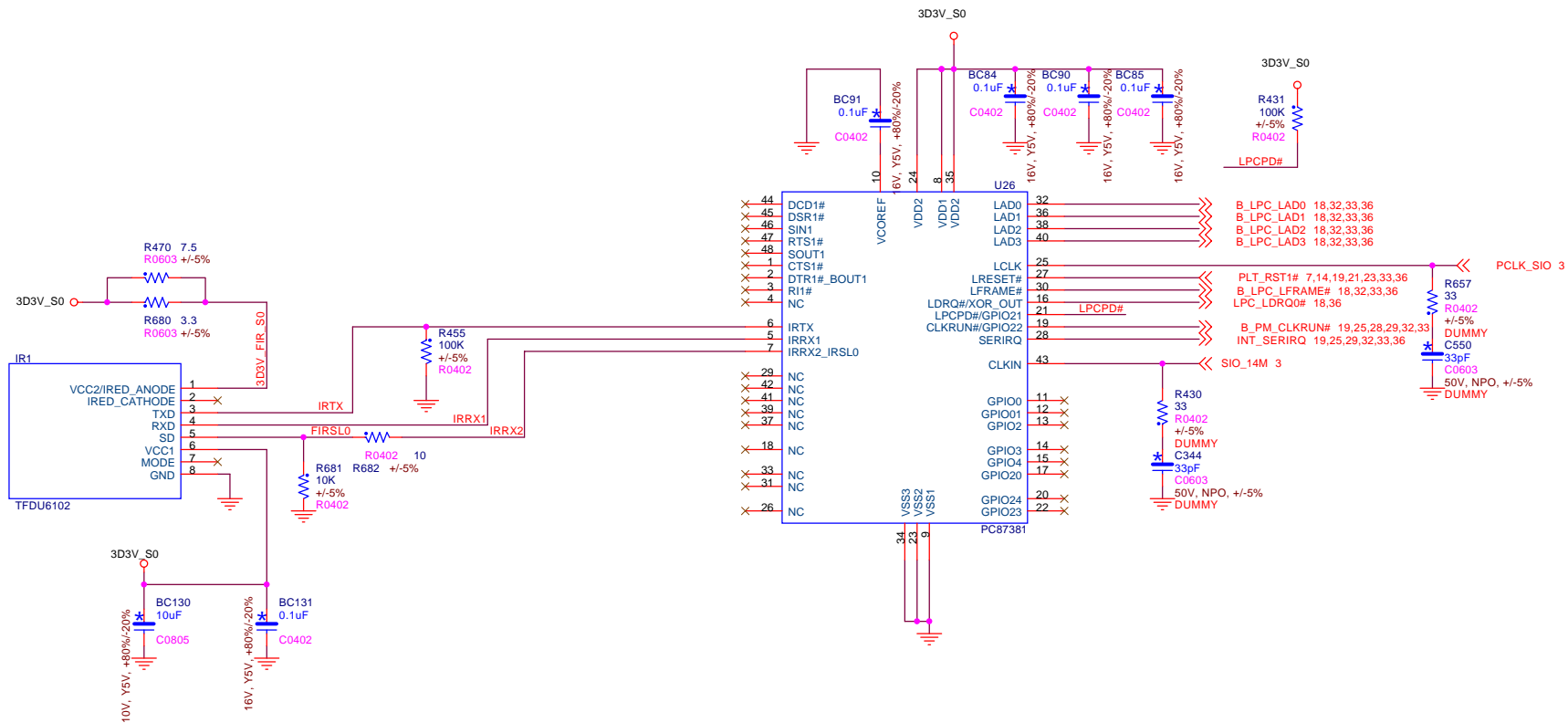
Keyboard matrix ( from vendor )

|            | US | Eur | Jap | Ohter |
|------------|----|-----|-----|-------|
| MATRIXID1# | 1  | 0   | 1   | 0     |
| MATRIXID2# | 1  | 1   | 0   | 0     |



**FOXCONN ND2**

|       |                             |                 |           |
|-------|-----------------------------|-----------------|-----------|
| Title |                             | <b>KB Conn.</b> |           |
| Size  | Document Number             | Rev             |           |
| A3    | <Doc>                       | <b>W02</b>      | <b>SA</b> |
| Date: | Saturday, February 19, 2005 | Sheet           | 34 of 44  |

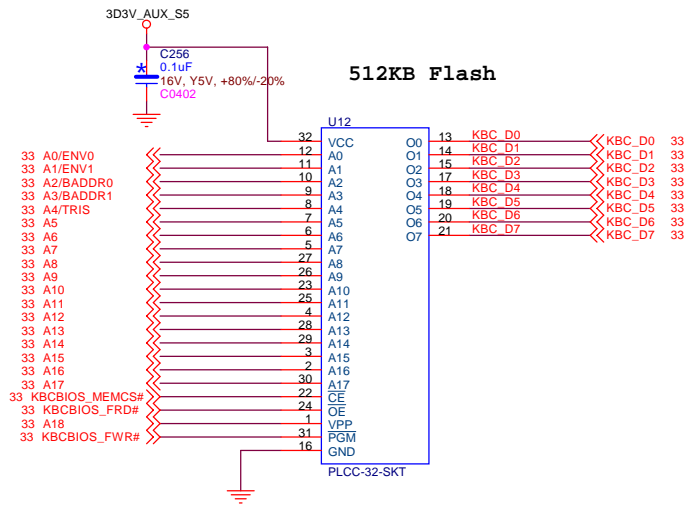


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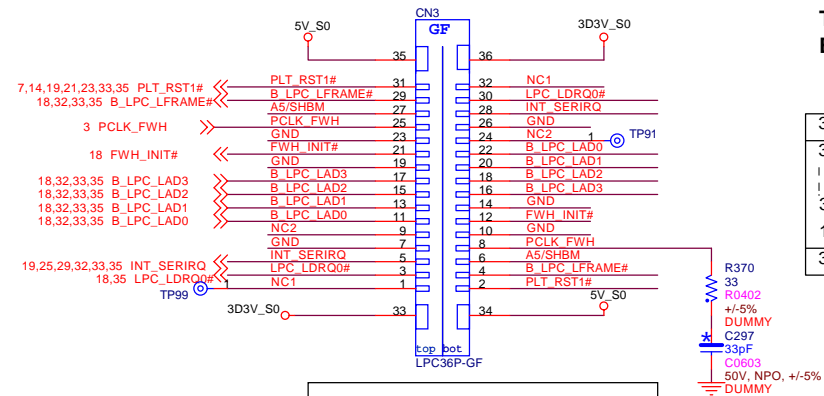


FOXCONN ND2

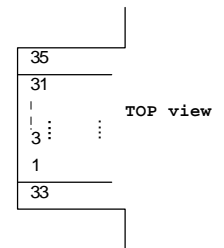
|       |                             |             |          |
|-------|-----------------------------|-------------|----------|
| Title |                             | SIO NS87381 |          |
| Size  | Document Number             | W06N        |          |
| A3    | <Doc>                       | SA          |          |
| Date: | Saturday, February 19, 2005 | Sheet       | 35 of 44 |



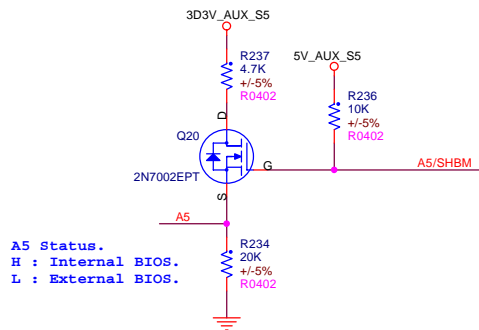
## DEBUG GOLDEN FINGER GOLDEN FINGER FOR DEBUG BOARD



TOP VIEW(1.3...35)  
BOTTOM VIEW(2.4..36)



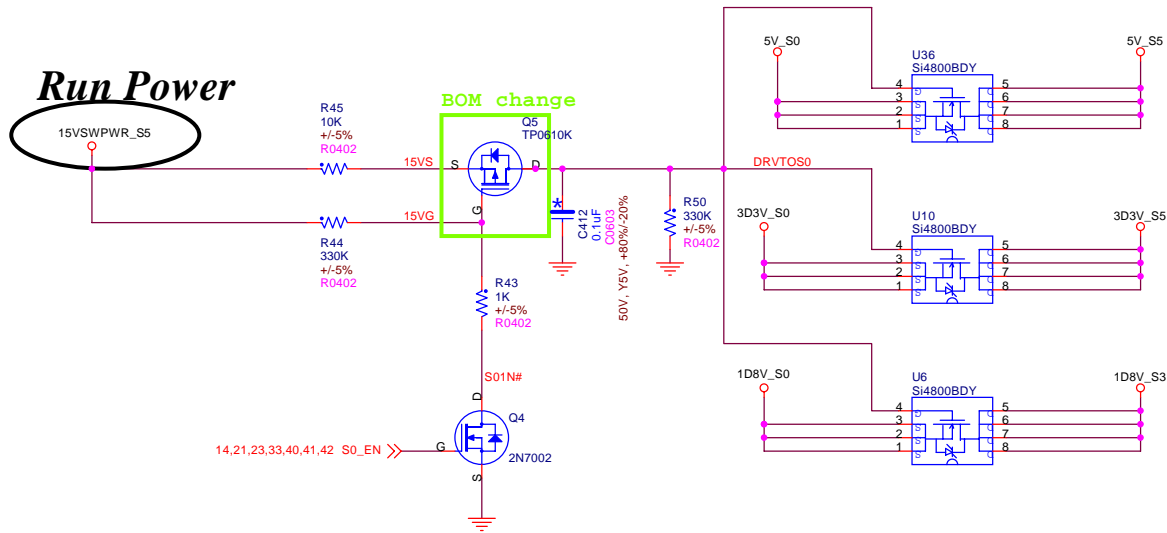
Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46



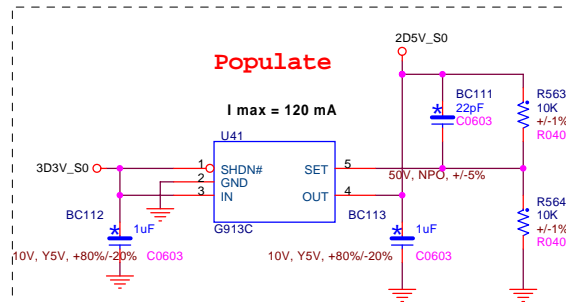
A5 Status.  
H : Internal BIOS.  
L : External BIOS.

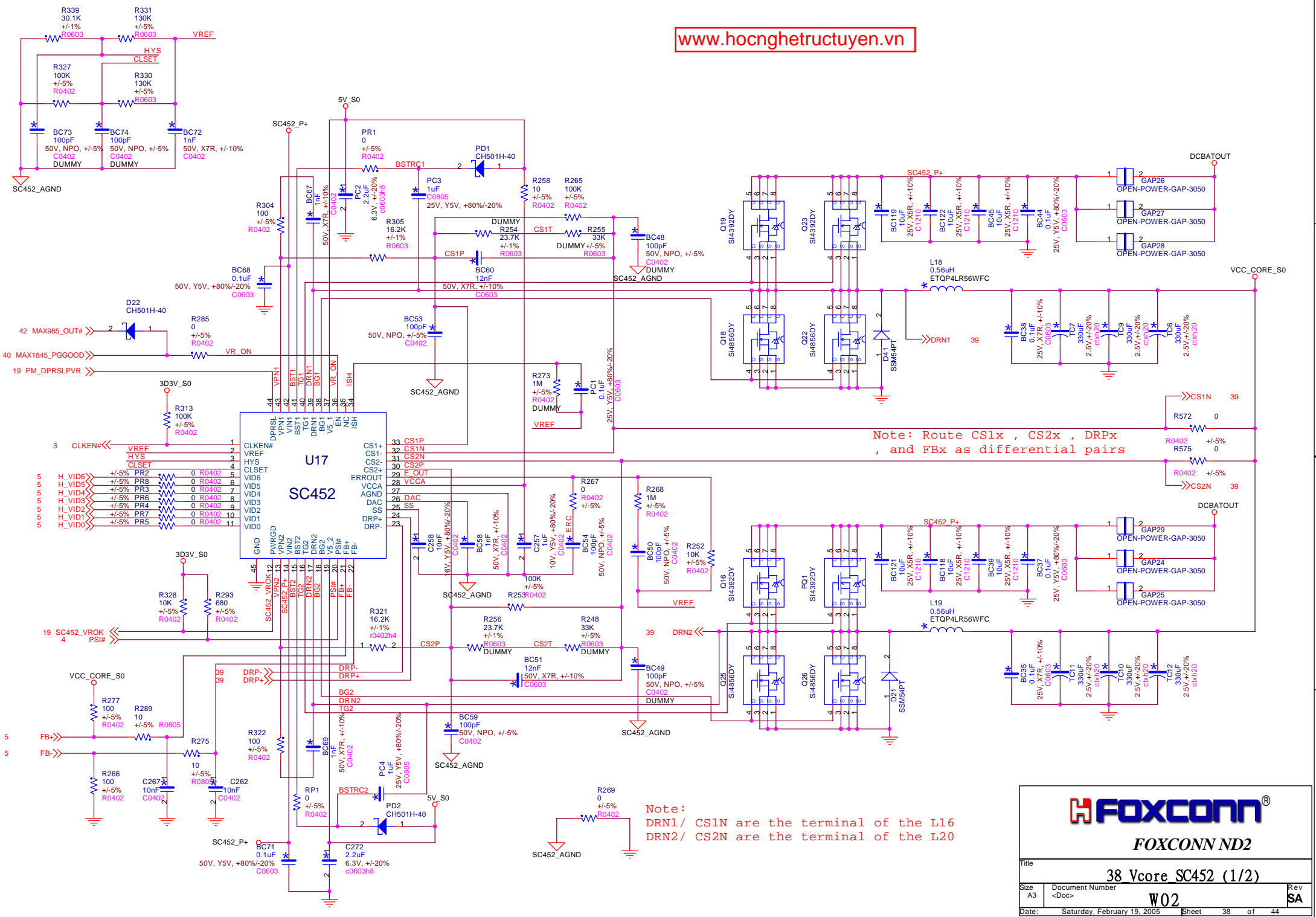
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|                                   |                        |        |  |
|-----------------------------------|------------------------|--------|--|
| <b>FOXCONN®</b>                   |                        |        |  |
| FOXCONN ND2                       |                        |        |  |
| Title: BIOS /Debug                |                        |        |  |
| Size: A3                          | Document Number: <Doc> | Rev SA |  |
| W02                               |                        |        |  |
| Date: Saturday, February 19, 2005 | Sheet: 36              | of: 44 |  |




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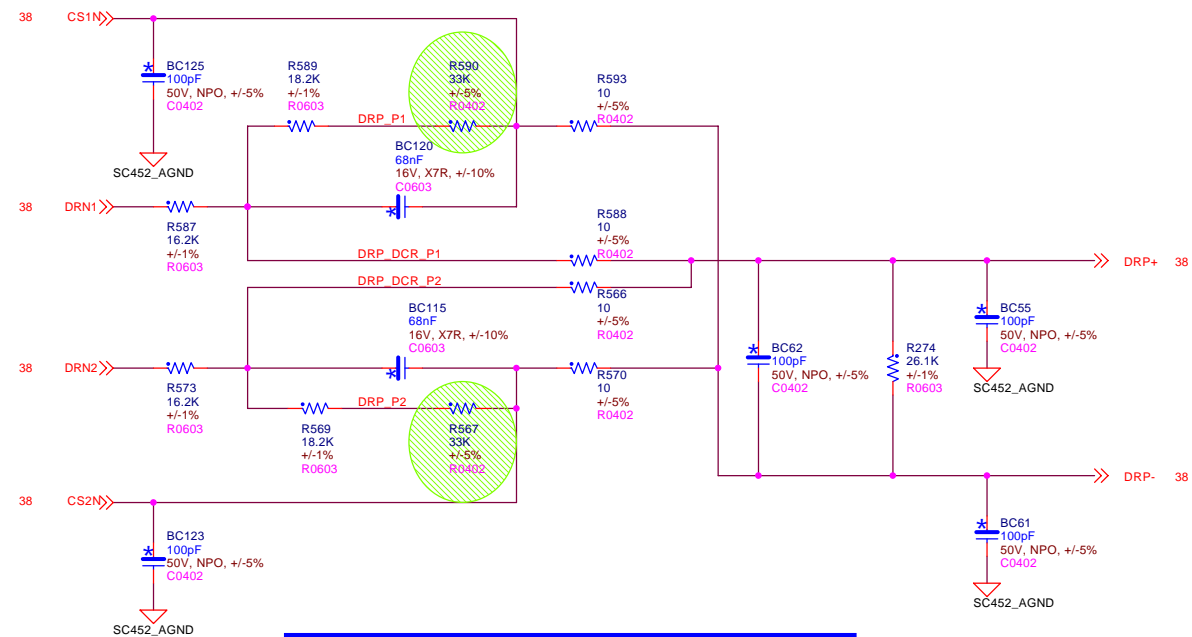
Note: Route CS1x , CS2x , DRPx , and FBx as differential pairs

Note: DRN1/ CS1N are the terminal of the L16  
DRN2/ CS2N are the terminal of the L20



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|       |                             |                             |            |       |
|-------|-----------------------------|-----------------------------|------------|-------|
| Title |                             | <b>38 Vcore SC452 (1/2)</b> |            | Rev   |
| Size  | A3                          | Document Number             | <b>W02</b> |       |
| Date: | Saturday, February 19, 2005 | Sheet                       | 38         | of 44 |



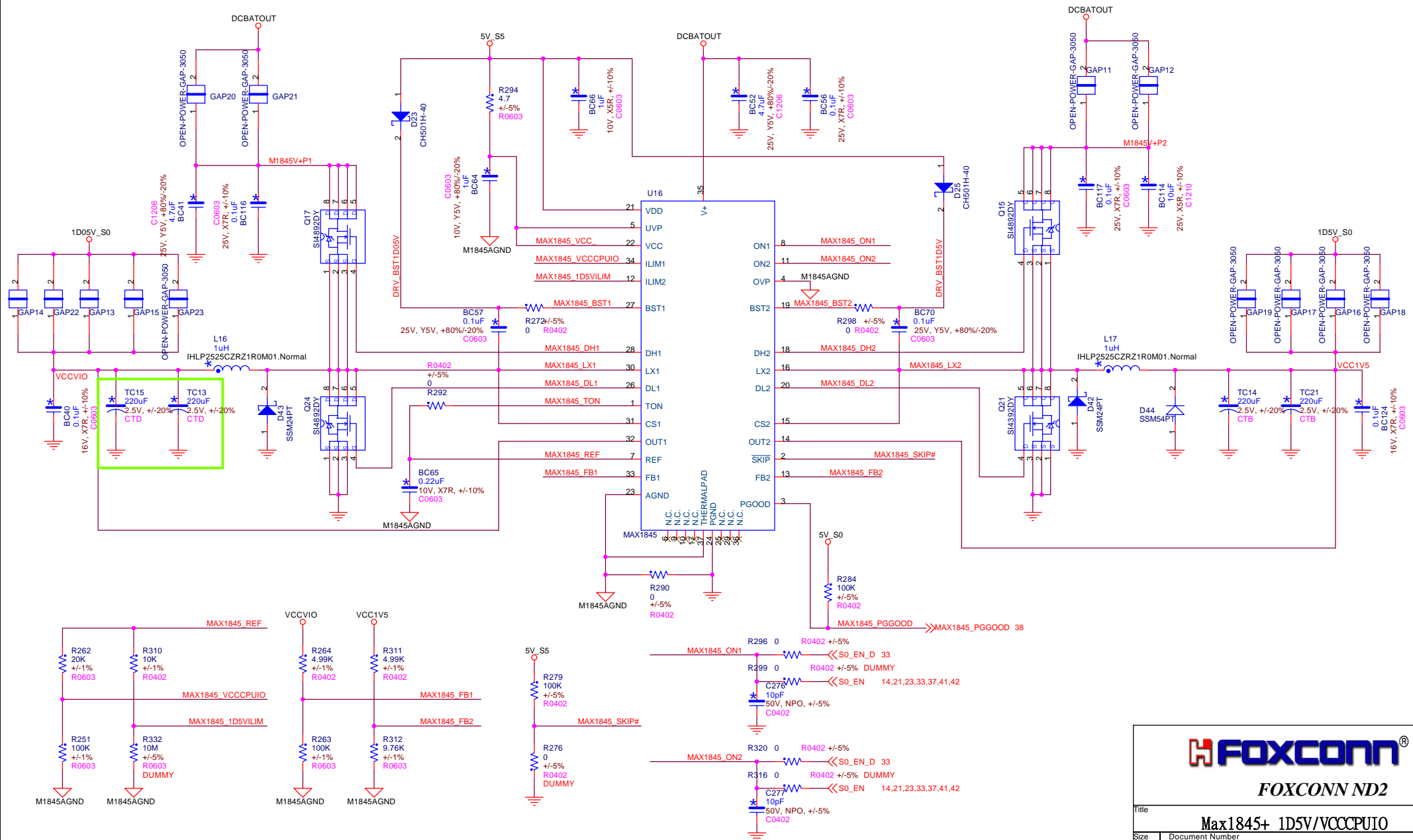
Note:  
 DRN1/ CS1N are the terminal of the L16  
 DRN2/ CS2N are the terminal of the L20

INDUCTOR DROOP

DRNx is the "+" end of the inductor . CSxN is the "-" end .

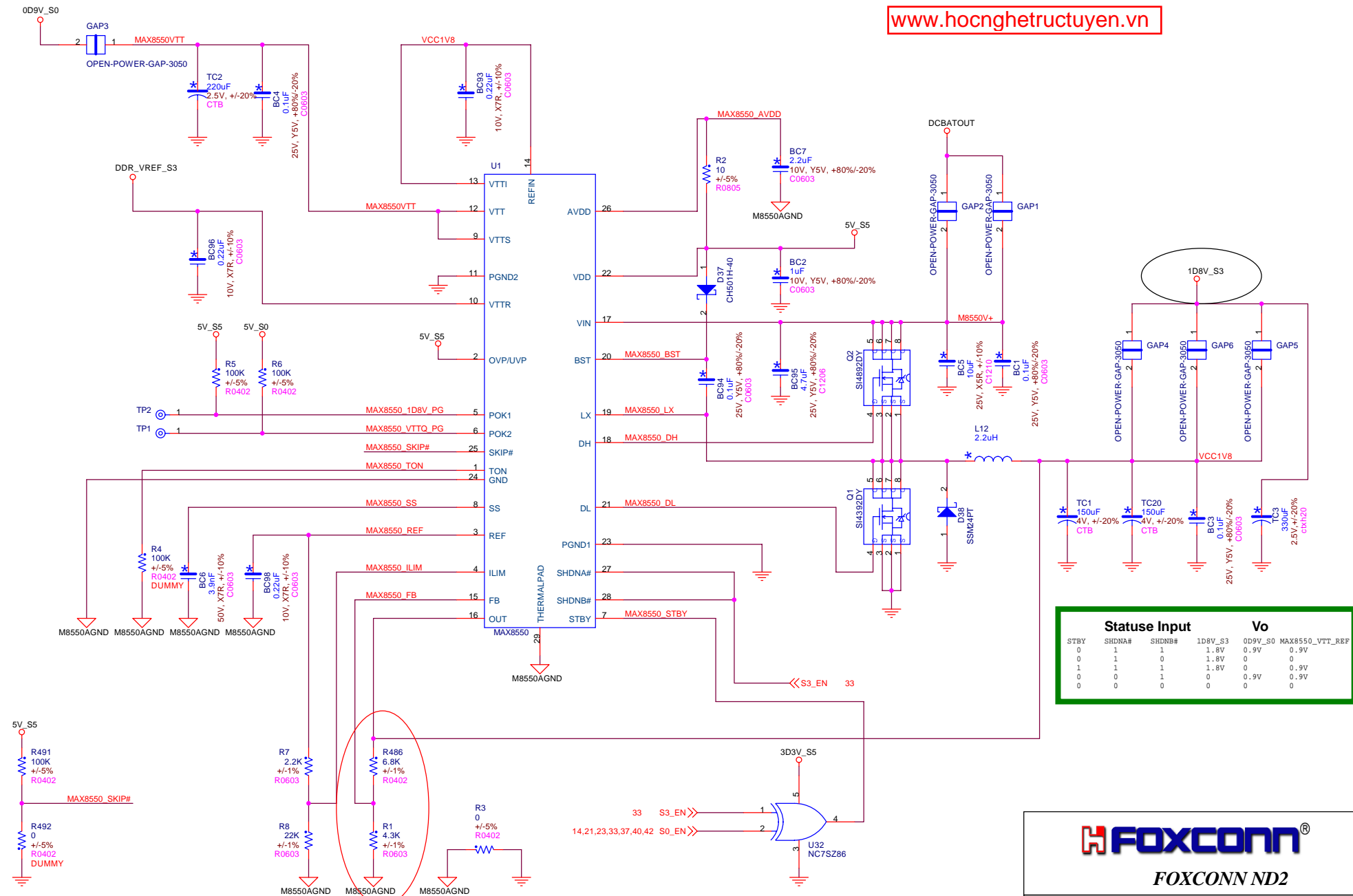
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 FOXCONN ND2

|                      |                             |                |
|----------------------|-----------------------------|----------------|
| Title                |                             |                |
| 39_Vcore_SC452 (2/2) |                             |                |
| Size                 | Document Number             | Rev            |
| A3                   | <Doc>                       | SA             |
| Date:                | Saturday, February 19, 2005 | Sheet 39 of 44 |



|       |                             |                        |          |
|-------|-----------------------------|------------------------|----------|
| Title |                             | Max1845+ 1D5V/VCCCPUIO |          |
| Size  | A3                          | Document Number        | <Doc>    |
| Date: | Saturday, February 19, 2005 | Sheet                  | 40 of 44 |
| Rev   | SA                          | W02                    |          |



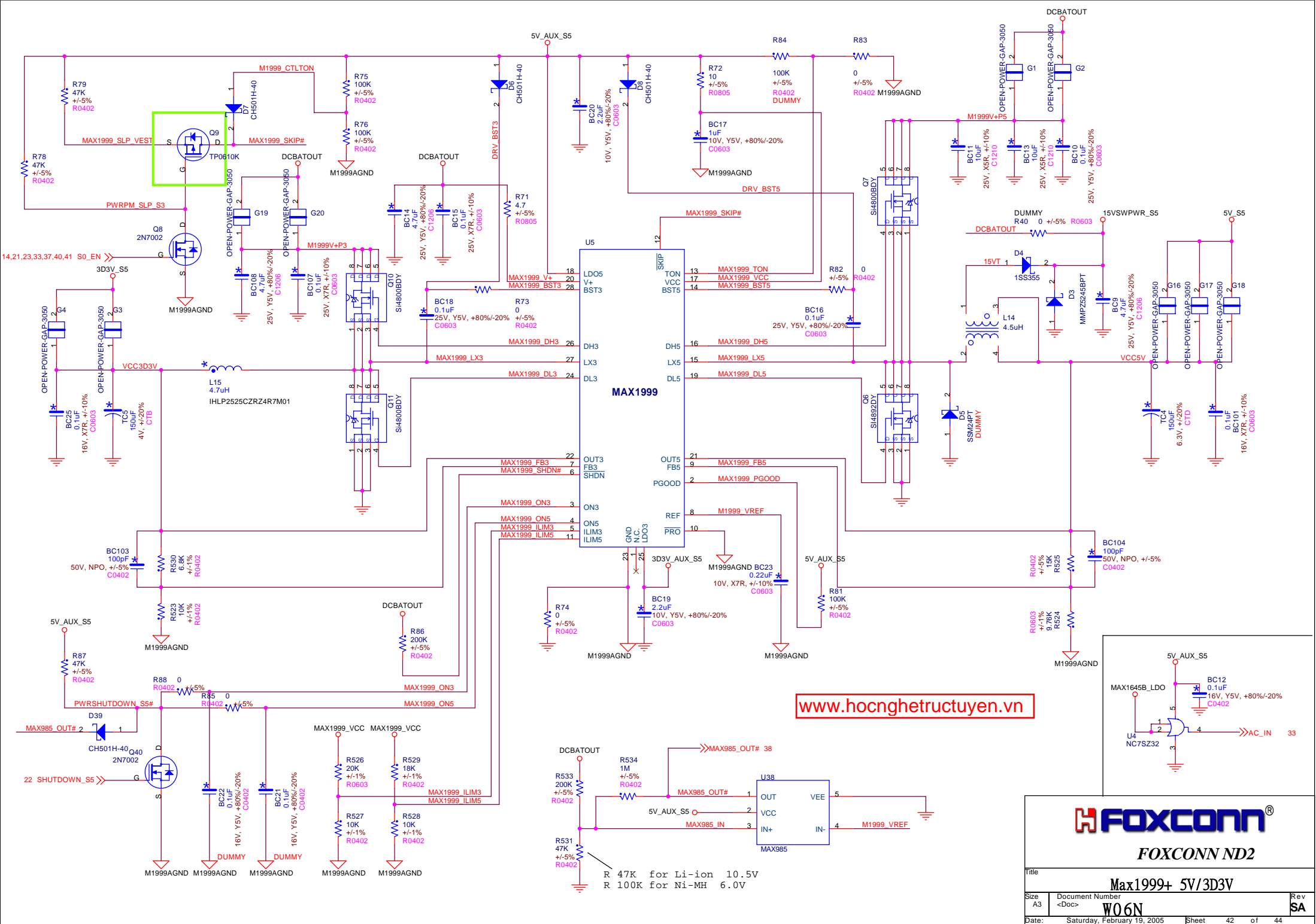



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**FOXCONN ND2**

Title: **Max8550+ 1D8V/VTIQ**

|                                   |                        |         |
|-----------------------------------|------------------------|---------|
| Size: A3                          | Document Number: <Doc> | Rev: SA |
| <b>W06N</b>                       |                        |         |
| Date: Saturday, February 19, 2005 | Sheet: 41              | of: 44  |

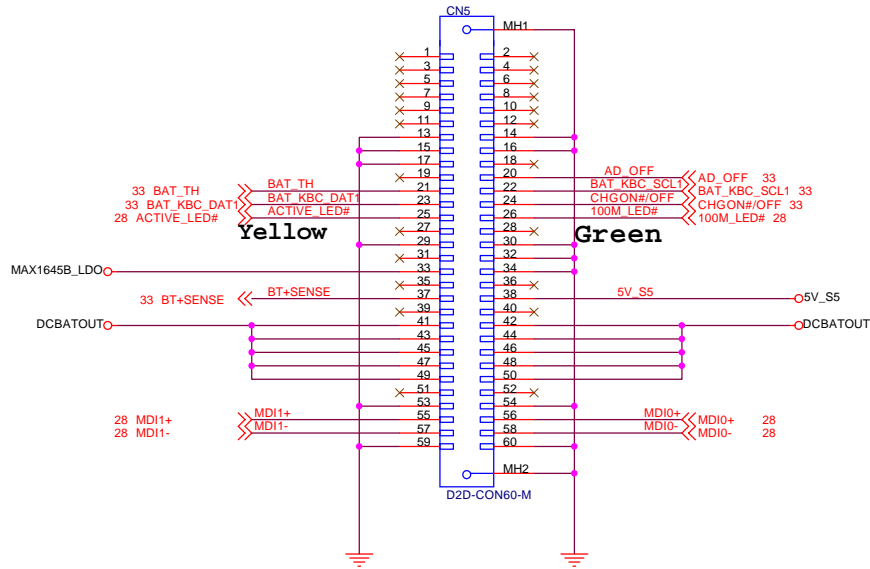




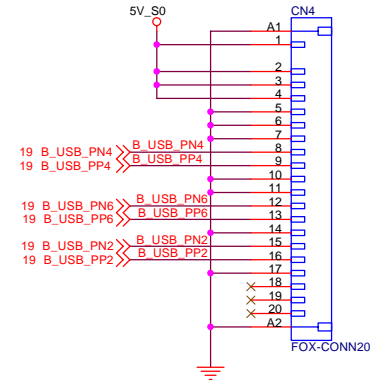
**FOXCONN ND2**

Title  
**Max1999+ 5V/3D3V**

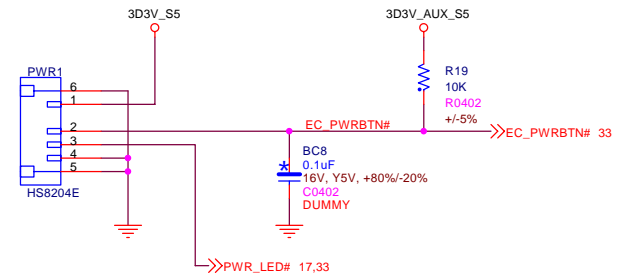
|  |   |                  |
|--|---|------------------|
| Size<br>A3                                       | Document Number<br><Doc><br><b>W06N</b> | Rev<br><b>SA</b> |
| Date: Saturday, February 19, 2005 Sheet 42 of 44 |   |                  |



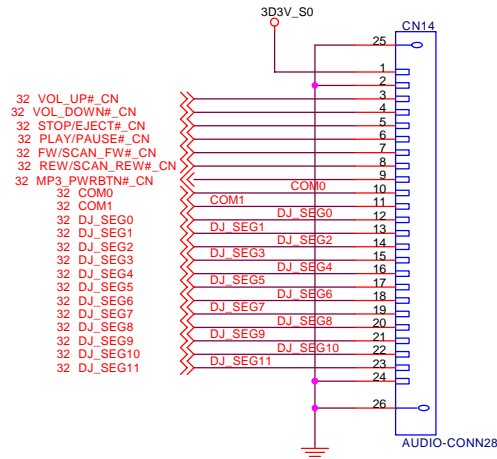
Power / LAN Connector



3 PORT USB Connector

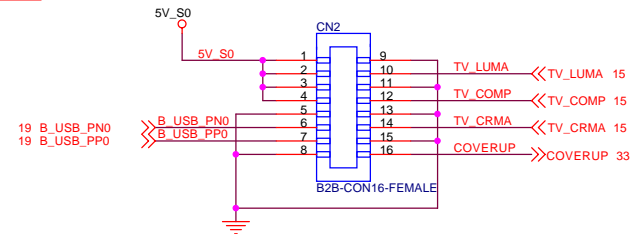


Power Switch Connector

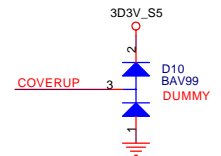


AudioDJ Connector

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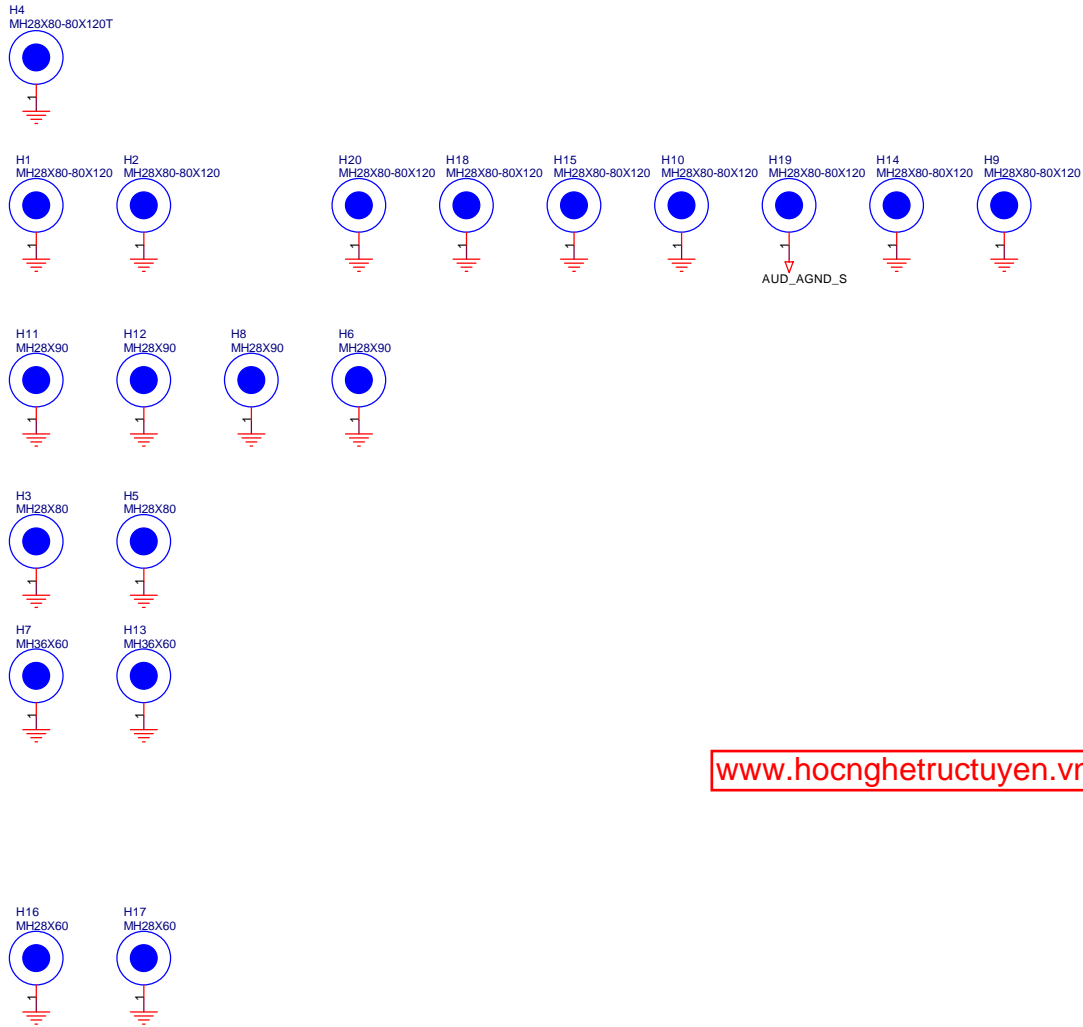
USB / TV Connector



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FOXCONN ND2

|                           |                             |                |
|---------------------------|-----------------------------|----------------|
| Title                     |                             |                |
| Daughter Board Connectors |                             |                |
| Size                      | Document Number             | Rev            |
| A3                        | <Doc>                       | SA             |
| Date:                     | Saturday, February 19, 2005 | Sheet 43 of 44 |



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