


# HuaQin Confidential

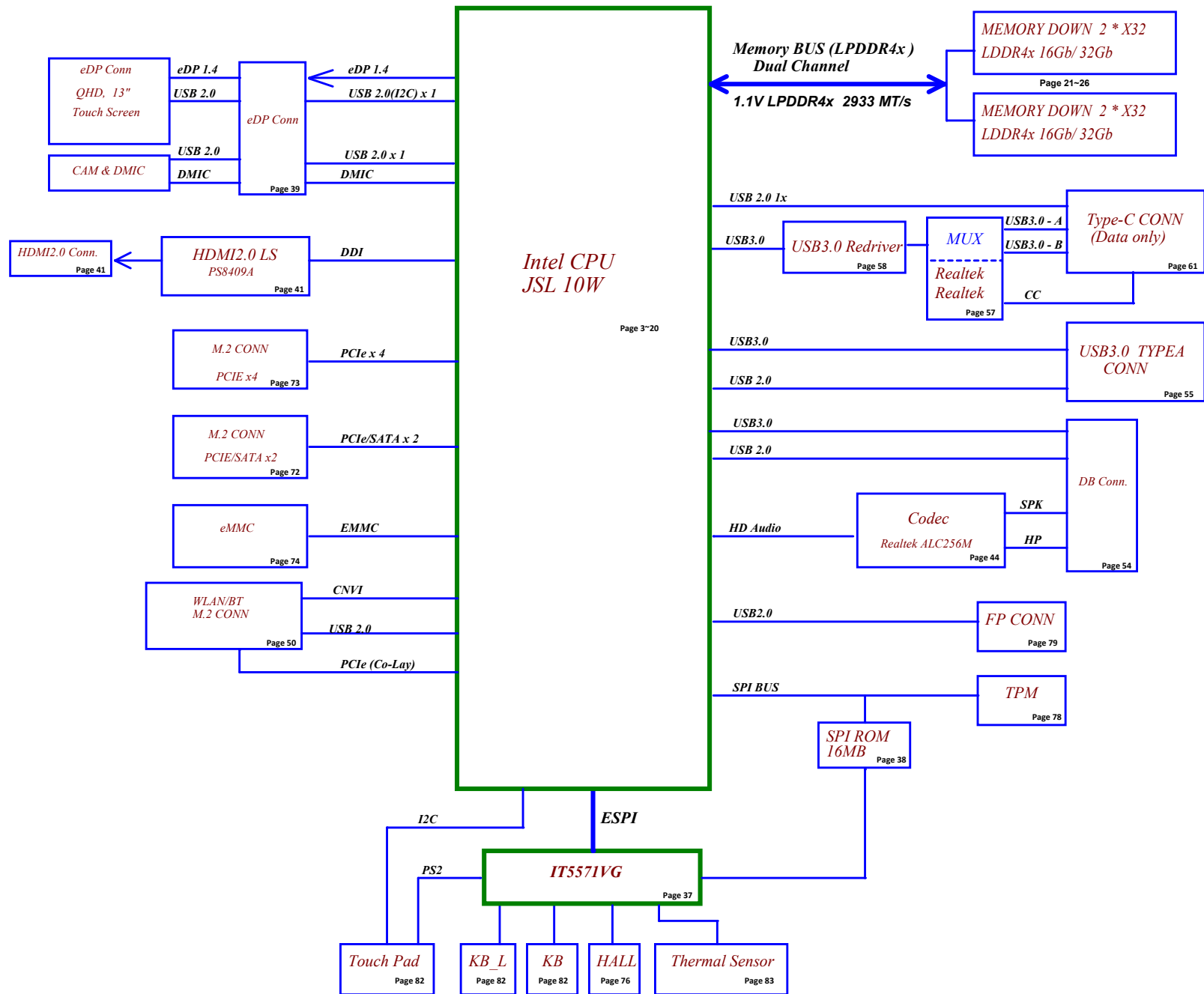
## NB2950\_MB&DB Schematics Document

### Intel JSL Lake-Processor with LPDDR4x MD

### REV1.0

### 2020-0622

Author		<div><div>HUAQIN 华勤通信</div><div>Huaqin Telecom Technology Com.,Ltd.</div></div>			
Reviewer		Page name: <b>Cover page</b>			
Approver		Size: A4	Project Name: NB2950-JSL	REV: V1.0	
		Date: Monday, September 28, 2020 Sheet: 1 of 110			

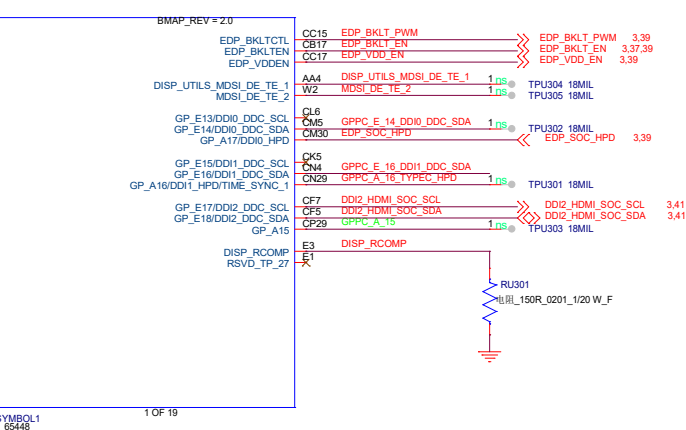


## EDP



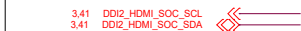
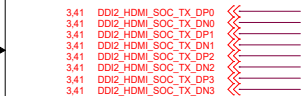
eDP

## DP/TYPEC

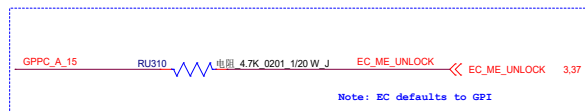


## DP/TYPEC

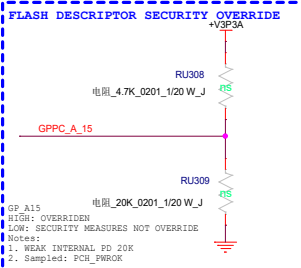
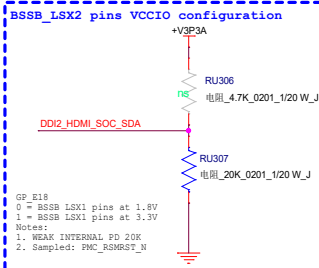
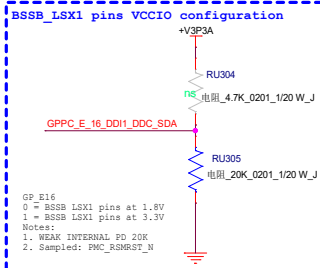
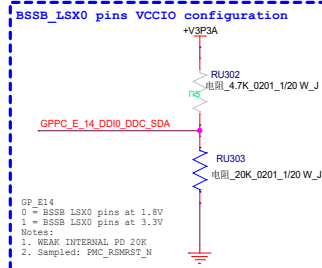
## HDMI



## Other

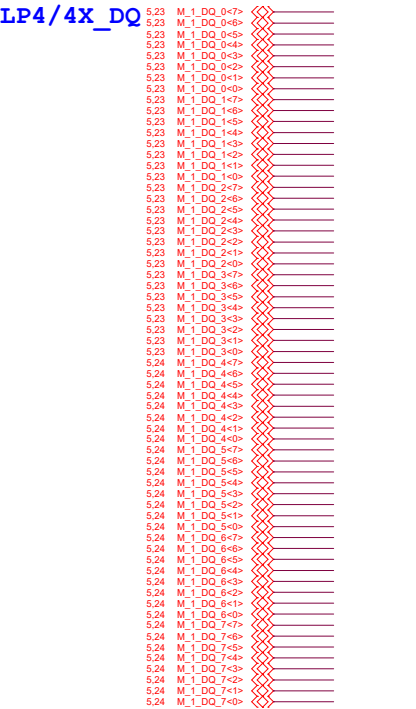


## Strap pin





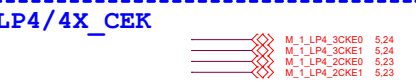
LP4/4X\_DQ



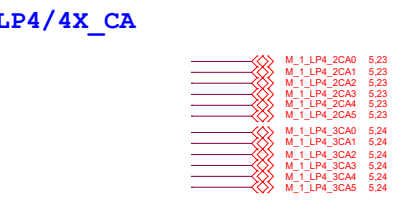
LP4/4X\_CLK



LP4/4X\_CEK



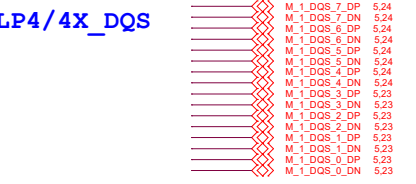
LP4/4X\_CA



LP4/4X\_CS

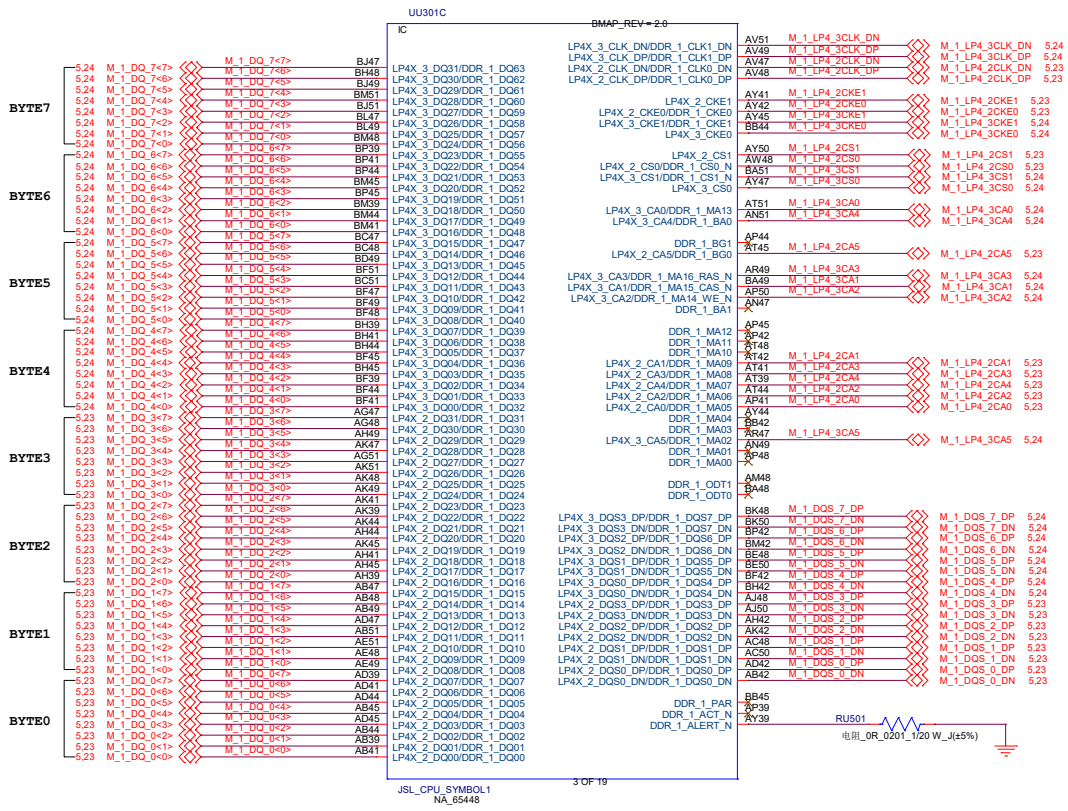


LP4/4X\_DQS



SOC\_LP4\_CHB

DDR = LPDDR4/4X





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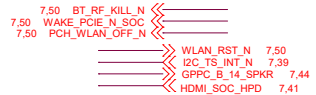
SPI



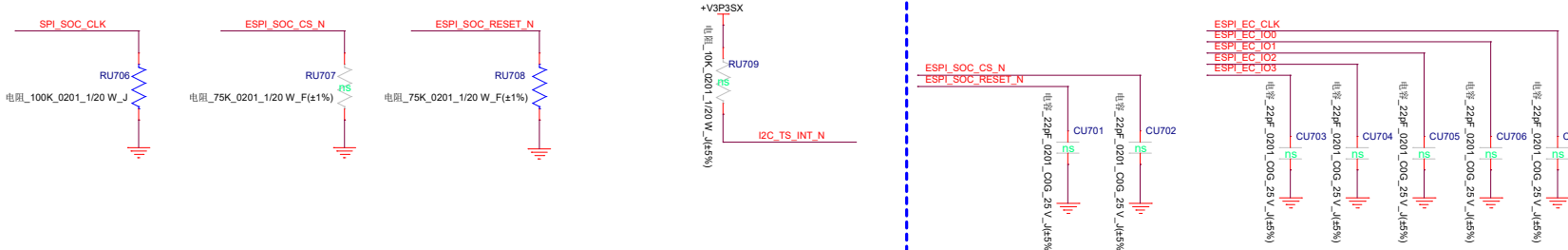
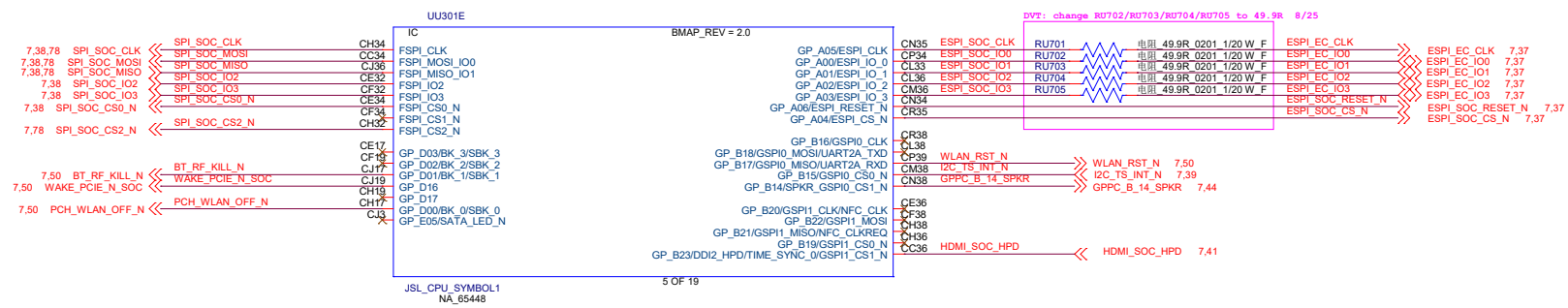
ESPI

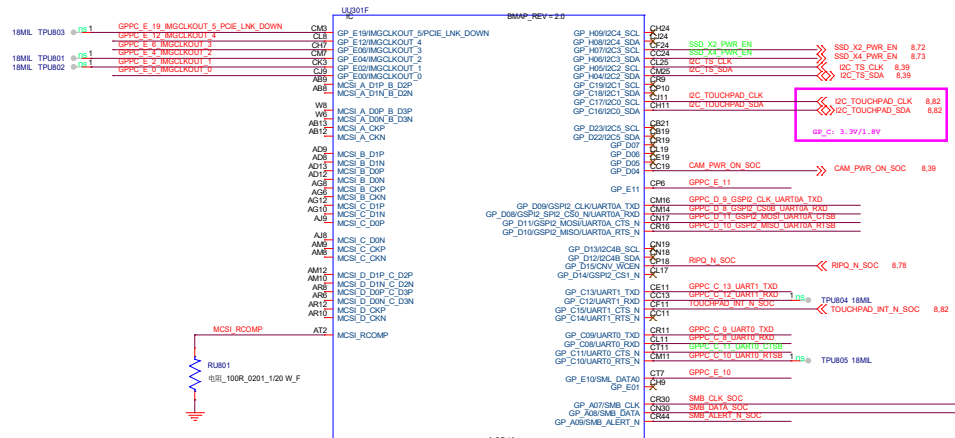
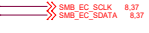


Other

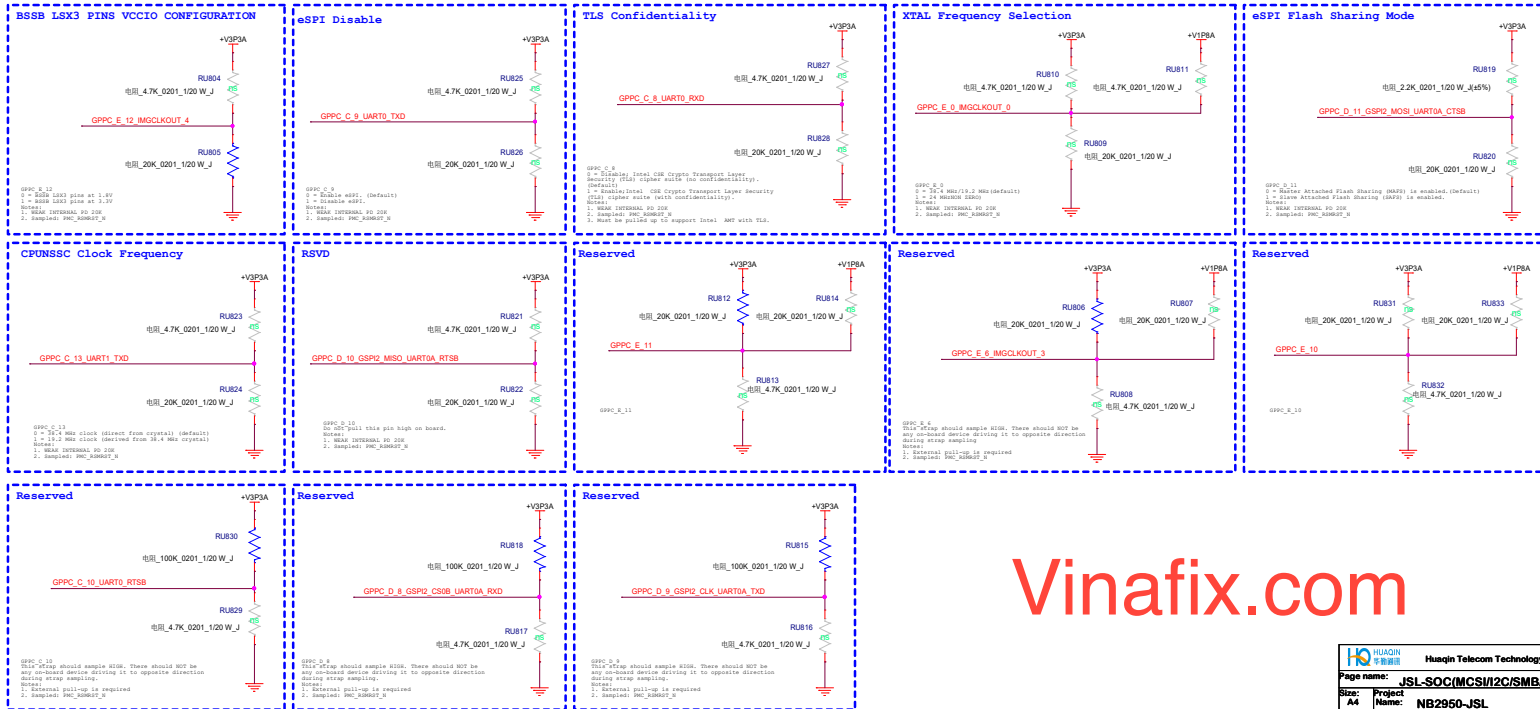
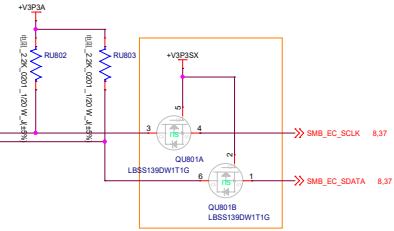


SOC





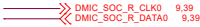
Touch Panel (Reserver)  
Touch Pad



Vinafix.com

Off-Page

DMIC\_0



DMIC\_1

HDA

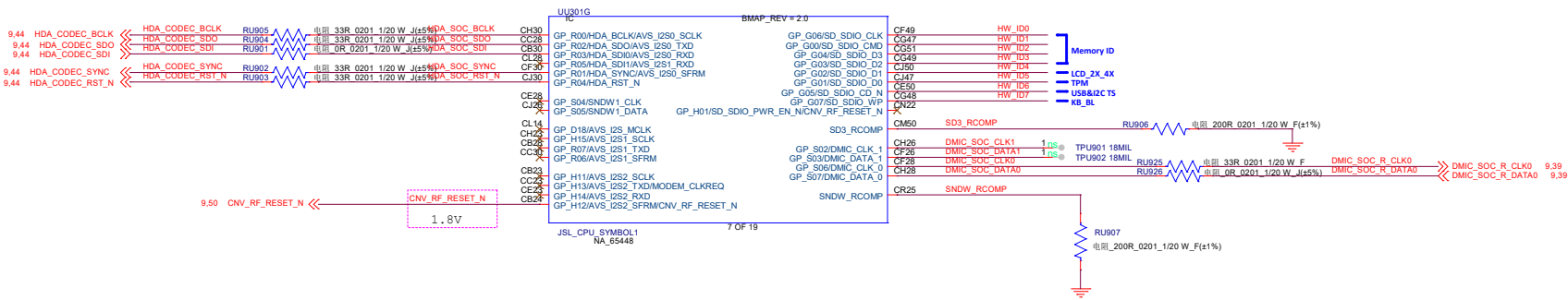


CNVI

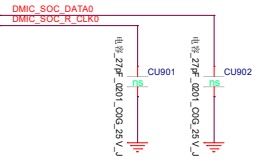
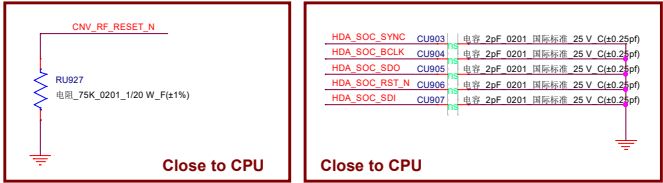
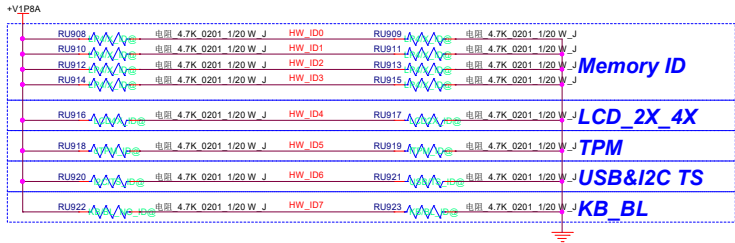


Other

SOC

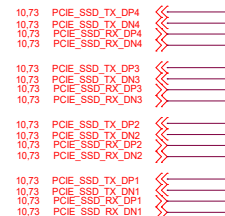


HWID

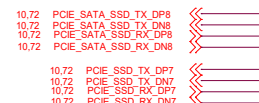


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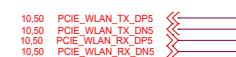
PCIE\_SSD x 4



PCIE\_SSD x 2

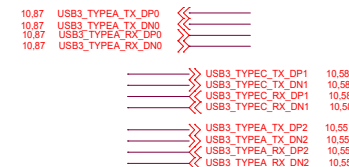


PCIE\_WLAN

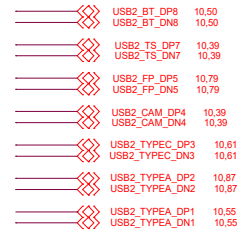


PCIE\_LAN

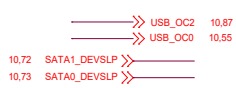
USB3.2



USB2.0



Other



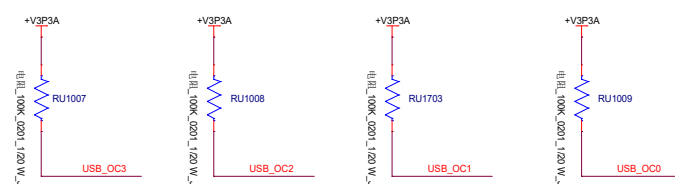
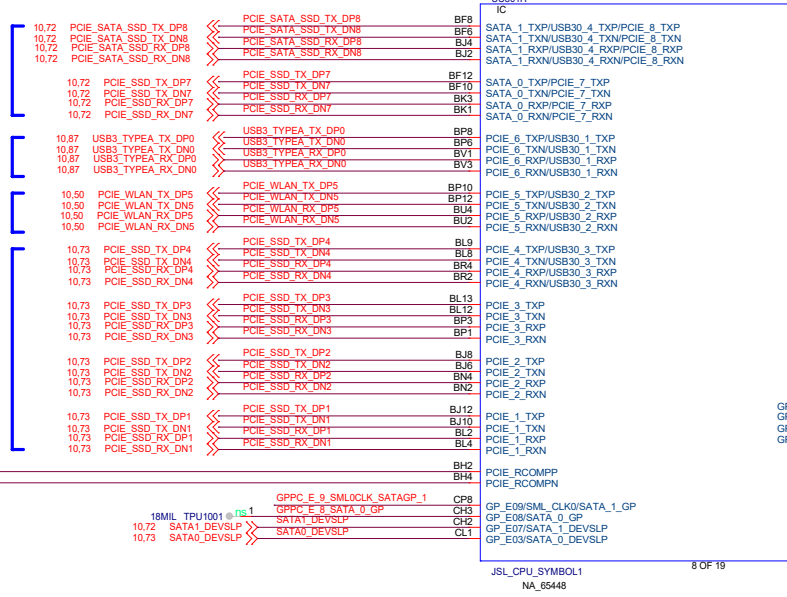
SOC

SSD x2

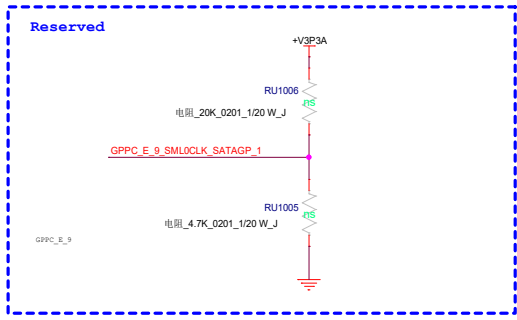
DB\_TypeA@USB3.1

WLAN

SSD x4



STRAP



BMAP\_REV = 2.0

UJ301H

IC

SATA\_1\_TXN/USB30\_4\_TX/PCIE\_8\_TXP  
SATA\_1\_TXN/USB30\_4\_TXN/PCIE\_8\_TXN  
SATA\_1\_RXP/USB30\_4\_RXP/PCIE\_8\_RXP  
SATA\_1\_RXN/USB30\_4\_RXN/PCIE\_8\_RXN

SATA\_0\_TXP/PCIE\_7\_TXP  
SATA\_0\_TXN/PCIE\_7\_TXN  
SATA\_0\_RXP/PCIE\_7\_RXP  
SATA\_0\_RXN/PCIE\_7\_RXN

PCIE\_6\_TXP/USB30\_1\_TXP  
PCIE\_6\_TXN/USB30\_1\_TXN  
PCIE\_6\_RXP/USB30\_1\_RXP  
PCIE\_6\_RXN/USB30\_1\_RXN

PCIE\_5\_TXP/USB30\_2\_TXP  
PCIE\_5\_TXN/USB30\_2\_TXN  
PCIE\_5\_RXP/USB30\_2\_RXP  
PCIE\_5\_RXN/USB30\_2\_RXN

PCIE\_4\_TXP/USB30\_3\_TXP  
PCIE\_4\_TXN/USB30\_3\_TXN  
PCIE\_4\_RXP/USB30\_3\_RXP  
PCIE\_4\_RXN/USB30\_3\_RXN

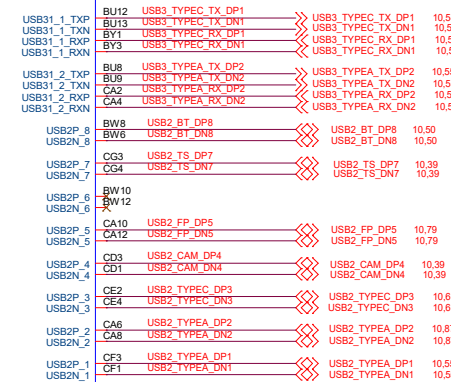
PCIE\_3\_TXP  
PCIE\_3\_TXN  
PCIE\_3\_RXP  
PCIE\_3\_RXN

PCIE\_2\_TXP  
PCIE\_2\_TXN  
PCIE\_2\_RXP  
PCIE\_2\_RXN

PCIE\_1\_TXP  
PCIE\_1\_TXN  
PCIE\_1\_RXP  
PCIE\_1\_RXN

PCIE\_RCOMP  
PCIE\_RCOMP\_N

GP\_E09/SML\_CLK0/SATA\_1\_GP  
GP\_E08/SATA\_0\_GP  
GP\_E07/SATA\_1\_DEVSLP  
GP\_E03/SATA\_0\_DEVSLP



Type-C@USB3.1

MB\_TypeA@USB3.1

BT

Touch Panel

Finger Print

Camera

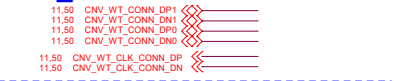
TYPE-C@USB2.0

DB\_TypeA@USB2.0

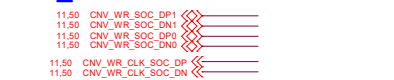
MB\_TypeA@USB2.0

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CNVI\_WT



CNVI\_WR



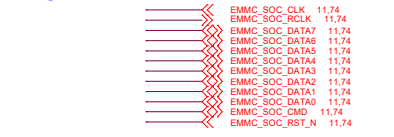
CNVI\_RGI



CNVI\_BRI



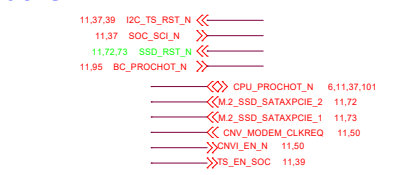
EMMC



Debug\_UART

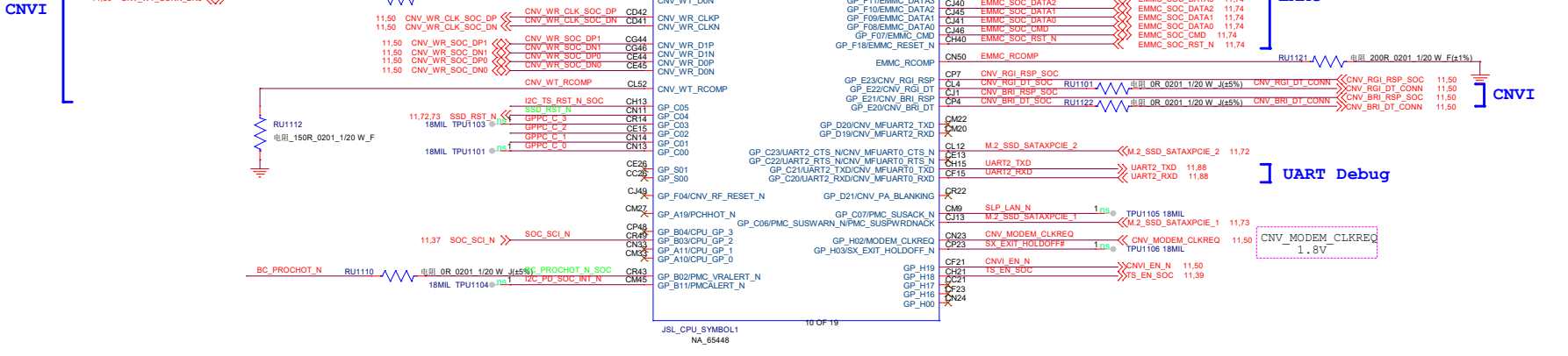


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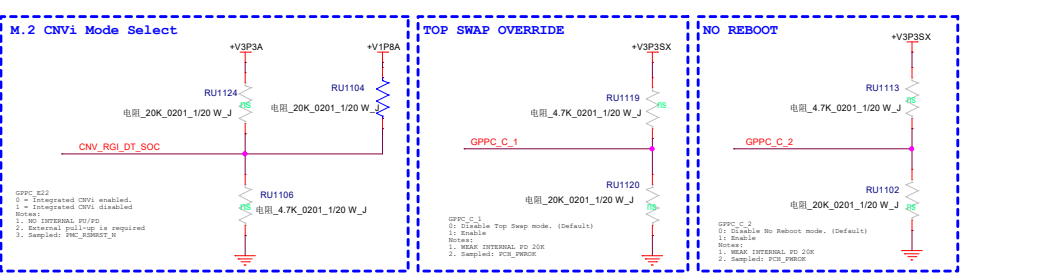


SOC

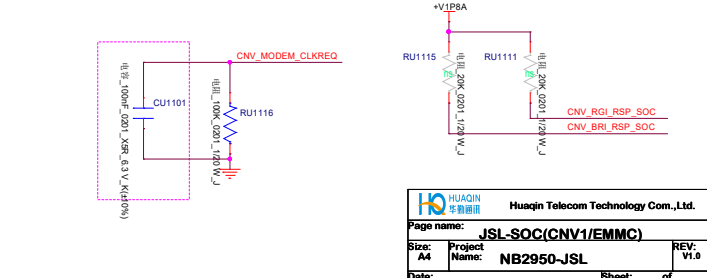
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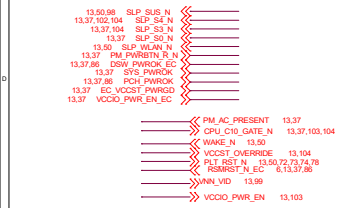
STRAP



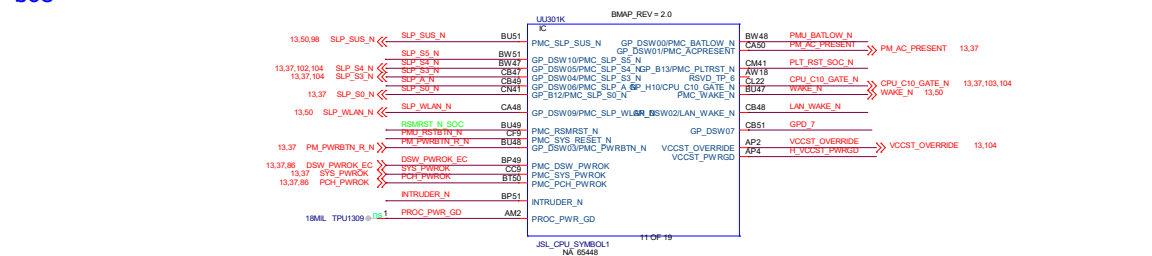
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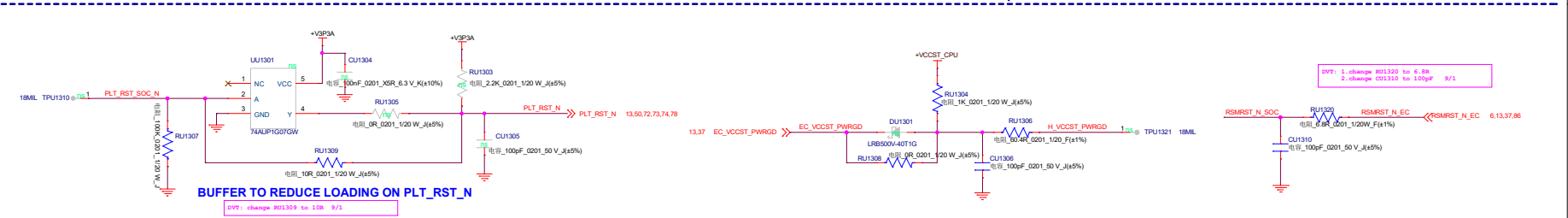
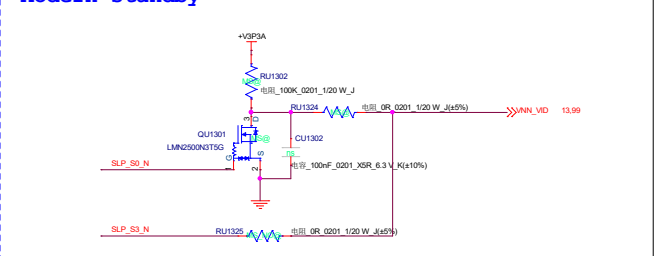




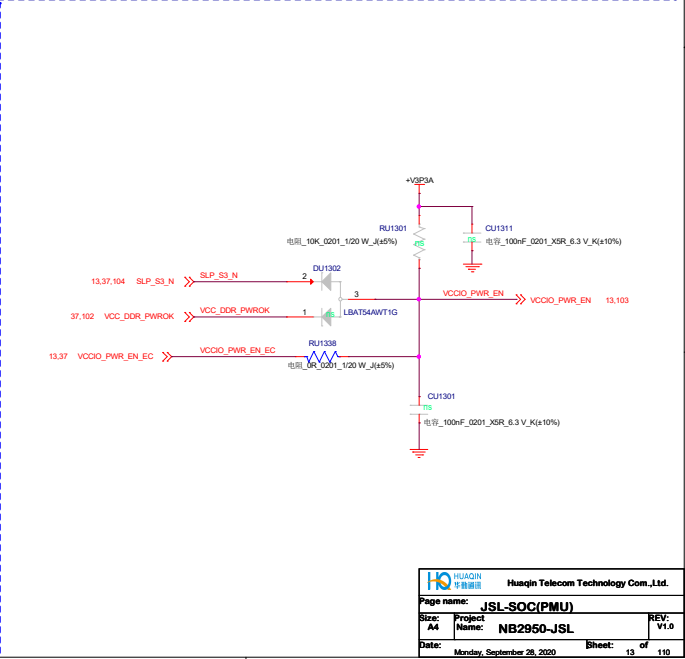
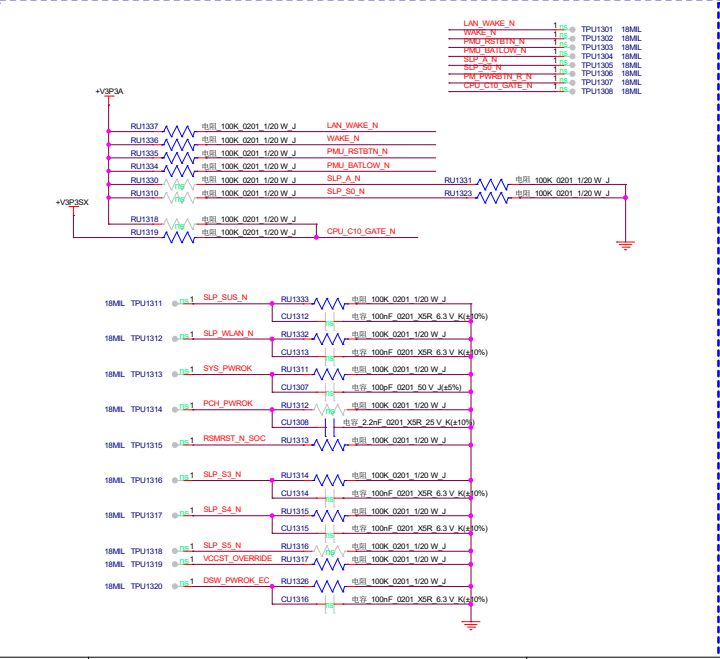
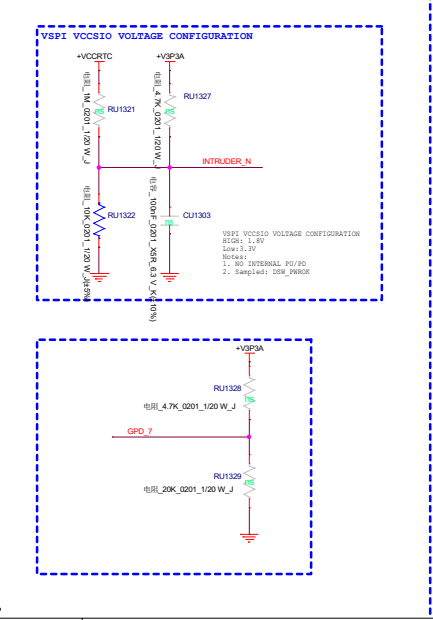
## SOC



## Modern standby



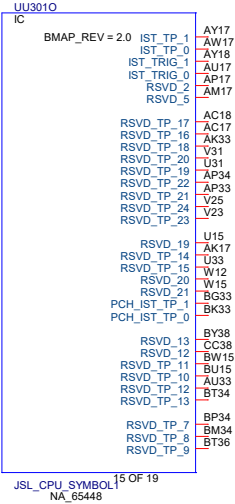
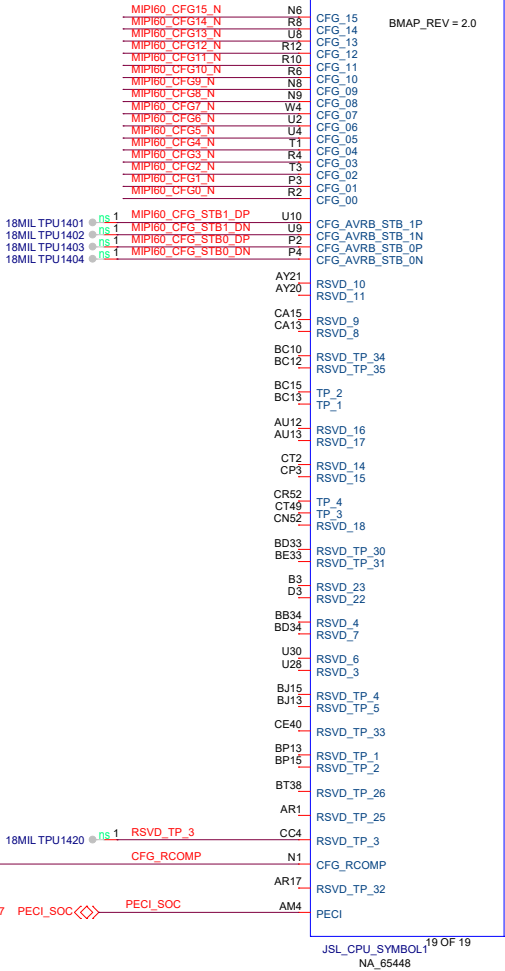
## Strap



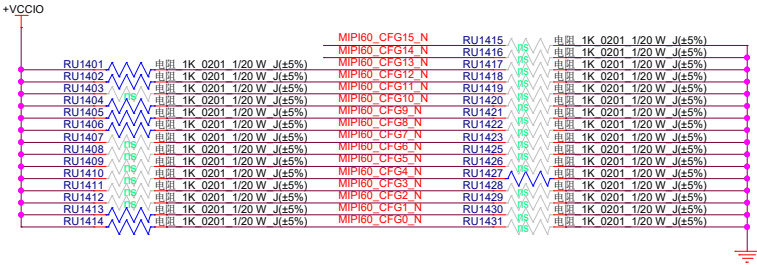
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RESERVED SIGNALS

14.37 PECL\_SOC



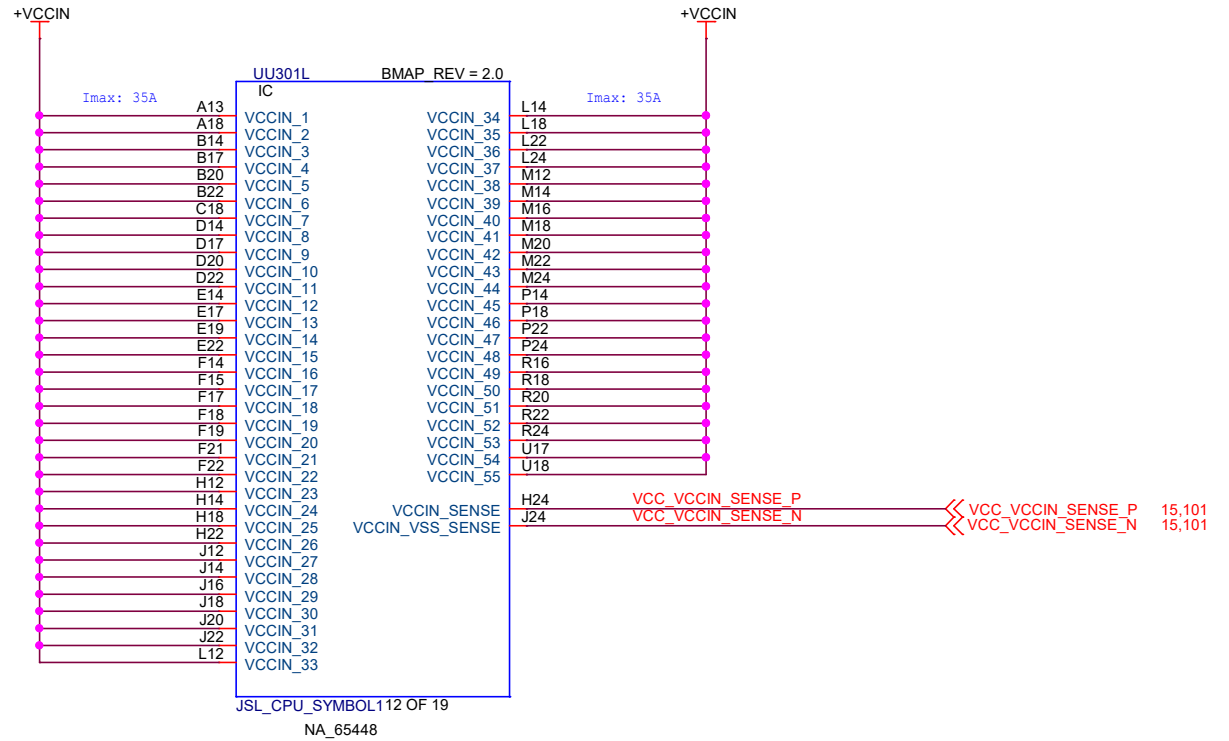
CFG Signals Functionality and Termination

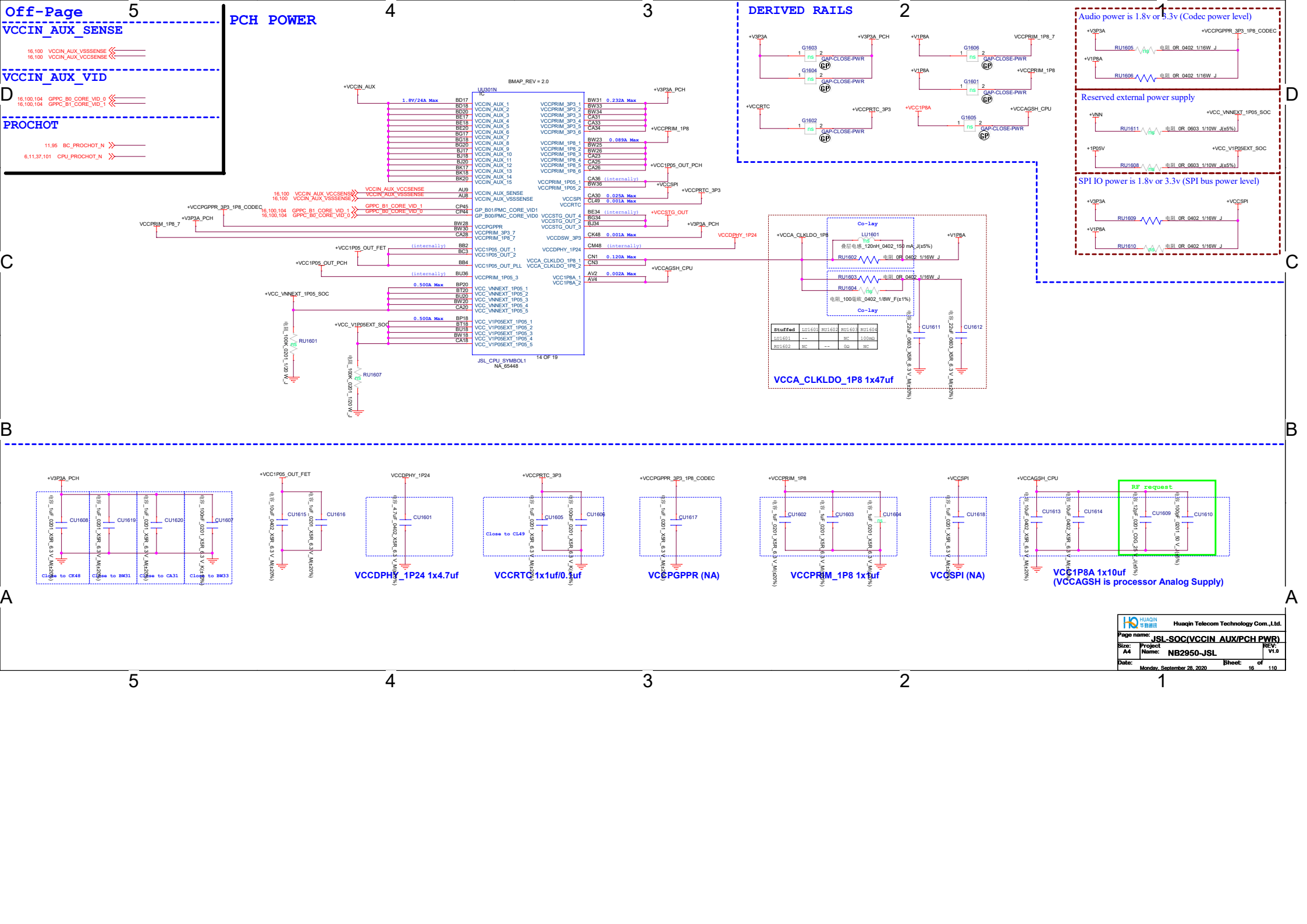


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VCCIN\_SENSE

VCC\_VCCIN\_SENSE\_P 15,101  
VCC\_VCCIN\_SENSE\_N 15,101

CPU POWER

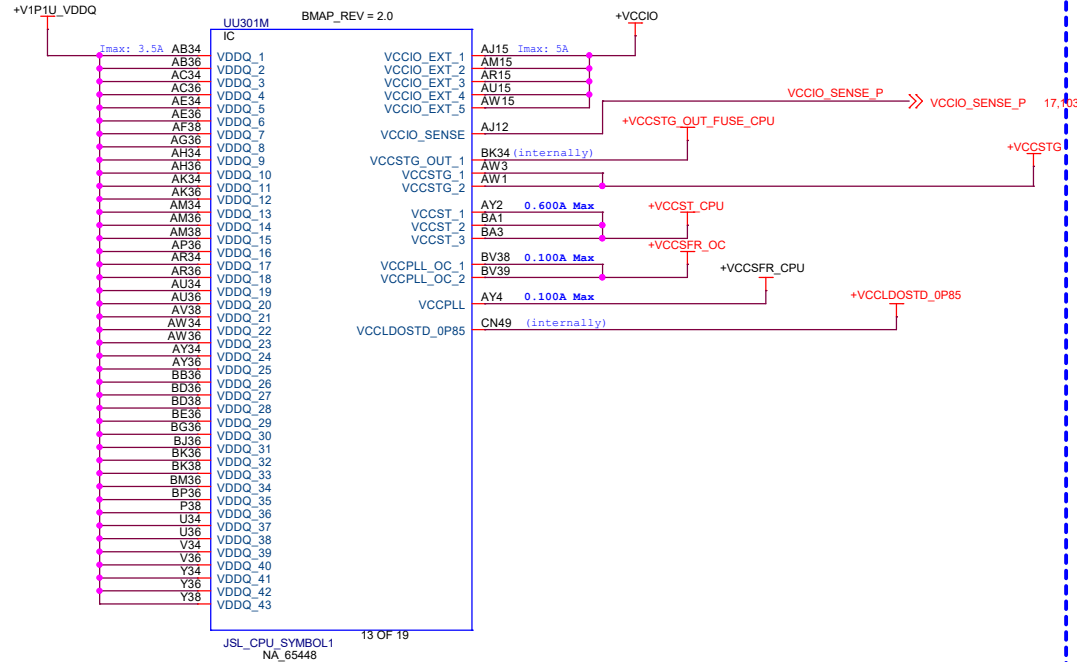




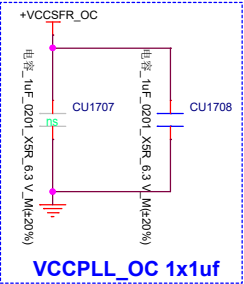
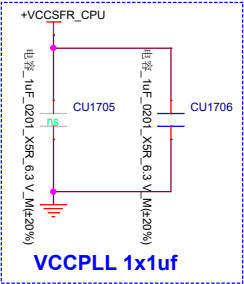
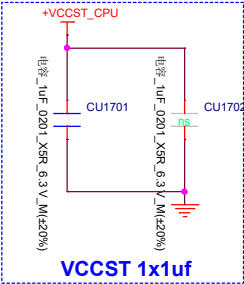
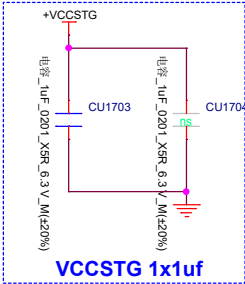
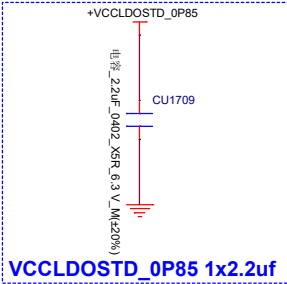
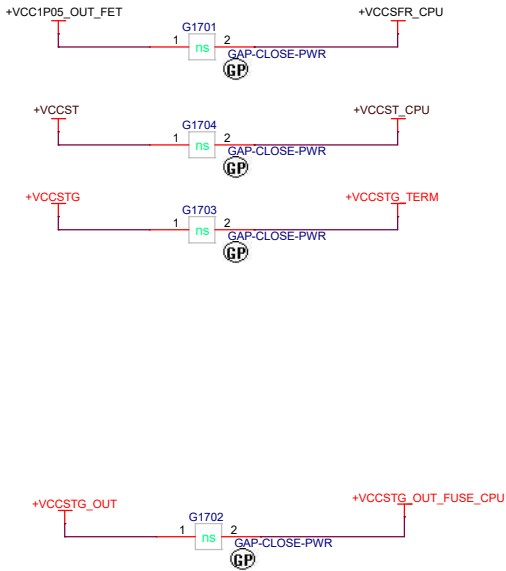
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VCCIO\_SENSE


VCCIO\_SENSE\_P 17.103

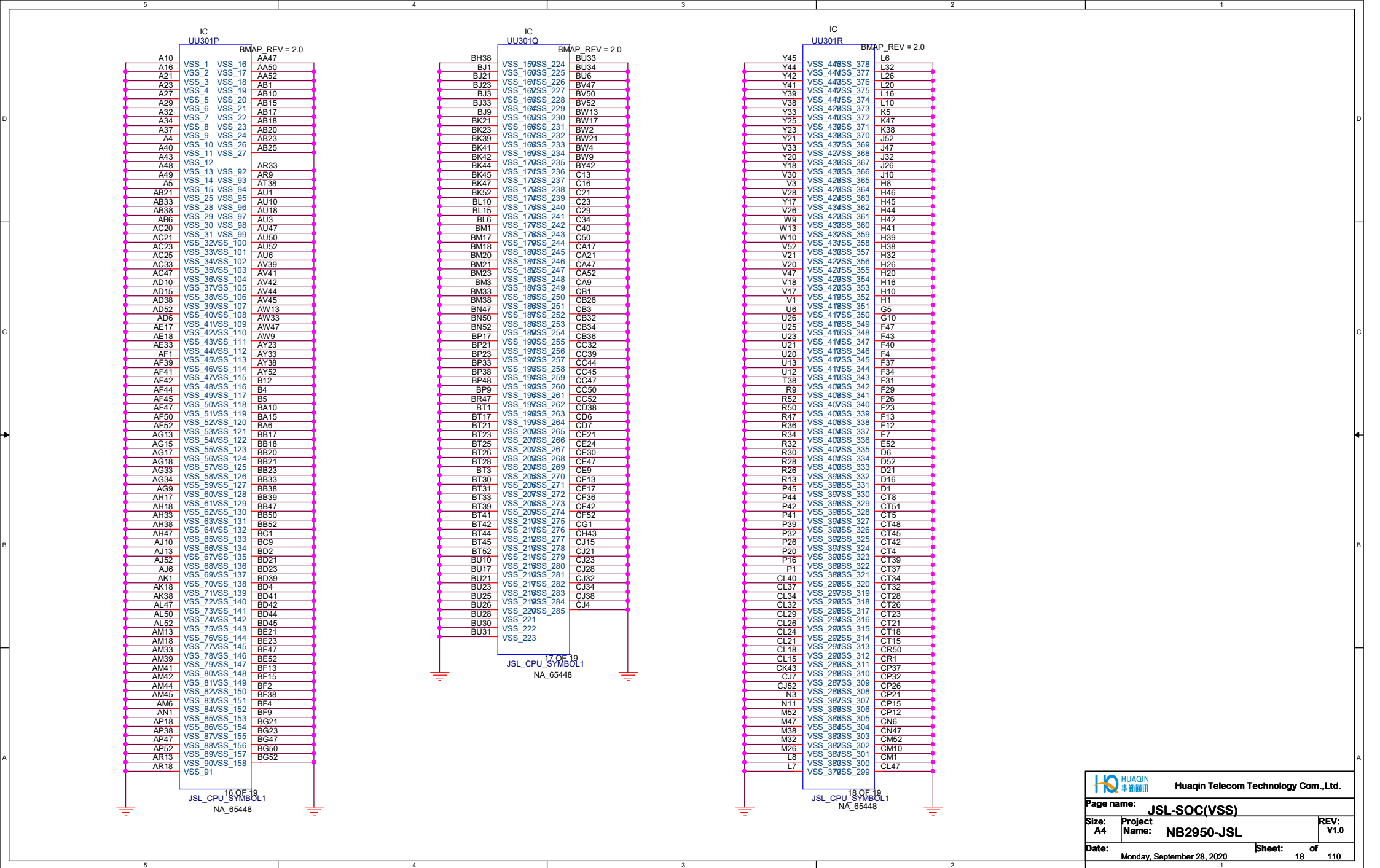
CPU POWER



DERIVED RAILS

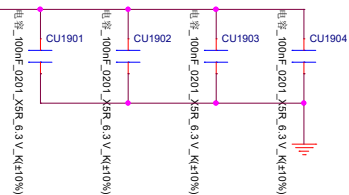


 HUAQIN 华勤通讯		Huaqin Telecom Technology Com.,Ltd.	
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Size: A4	Project Name: NB2950-JSL	REV: V1.0	
Date: Monday, September 28, 2020	Sheet: 17		of 110

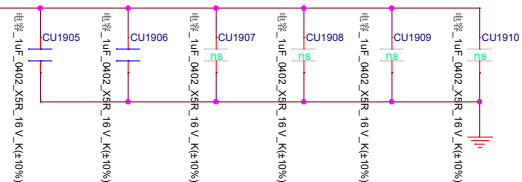


+VCCIN

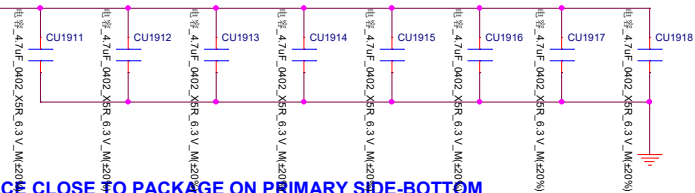
PLACE THESE CAPS UNDERNEATH BGA AREA---Top



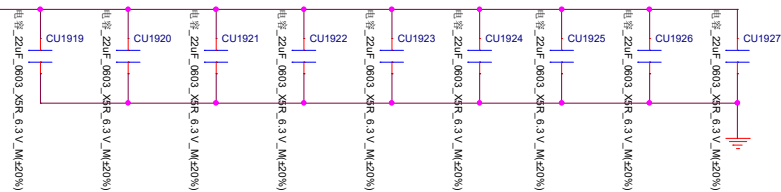
PLACE THESE CAPS UNDERNEATH BGA AREA-Top



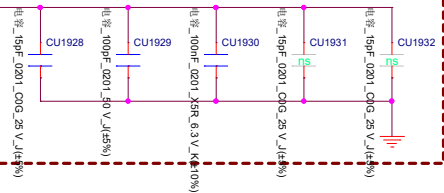
PLACE THESE CAPS UNDERNEATH BGA AREA--Top



PLACE CLOSE TO PACKAGE ON PRIMARY SIDE-BOTTOM



RF

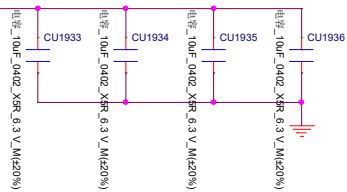


+VCCIN

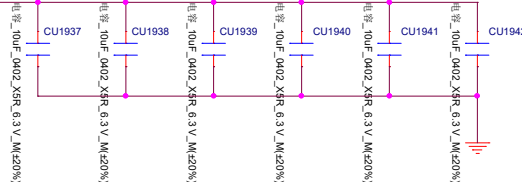
	PDG	S1
0.1uF	4	4
1uF	2	2
22uF	7+2(NC)	7+2(NC)
4.7uF	4+4(NC)	4+4(NC)
330uF	1	1

+VCCIO

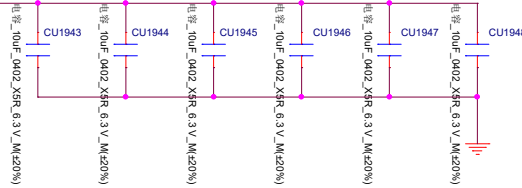
PLACE THESE CAPS UNDERNEATH BGA AREA---Top



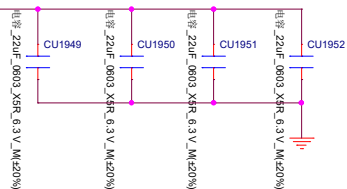
PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



+VCCIO

	PDG	S1
10uF	12+4	16
22uF	4	4

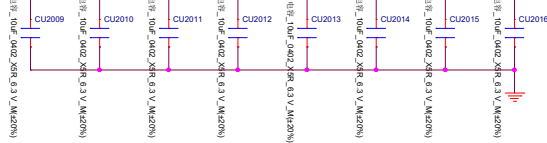
## +VCCIN\_AUX

	PDG	S1
2.2uF	4+4(NC)	4+4(NC)
10uF	4+4(NC)	4+4(NC)
22uF	4(NC)	22+4(NC)
47uF	8	0

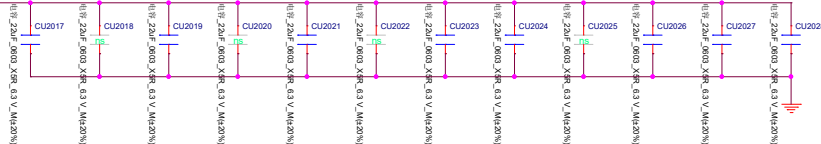
### PLACE THESE CAPS UNDERNEATH BGA AREA



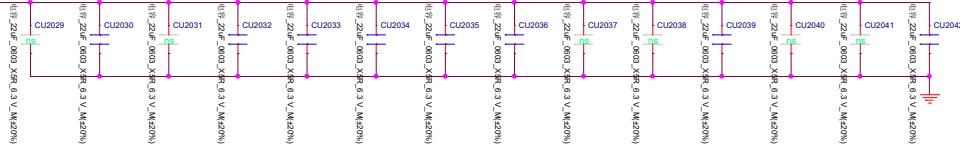
### PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



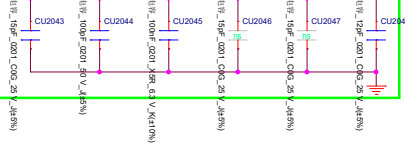
### PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



### PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



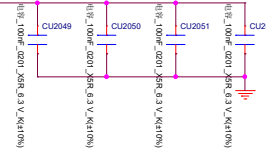
## RF



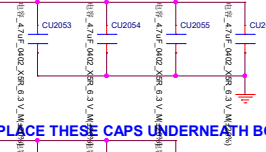
## +VDDQ\_CPU

	PDG	S1
1uF	14	14
10uF	6+1 (NC)	7
22uF	3	3
4.7uF	2+2 (NC)	4
0.1uF	2+2 (NC)	4

### PLACE THESE CAPS UNDERNEATH BGA AREA



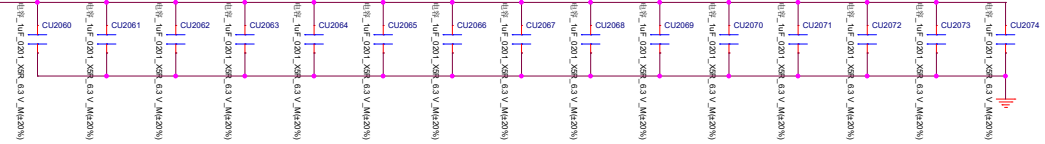
### PLACE THESE CAPS UNDERNEATH BGA AREA



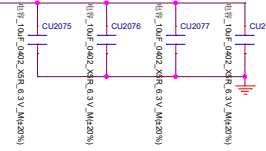
### PLACE THESE CAPS UNDERNEATH BGA AREA



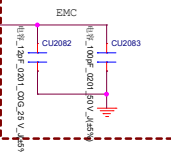
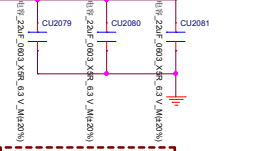
### PLACE CLOSE TO PACKAGE ON PRIMARY SIDE

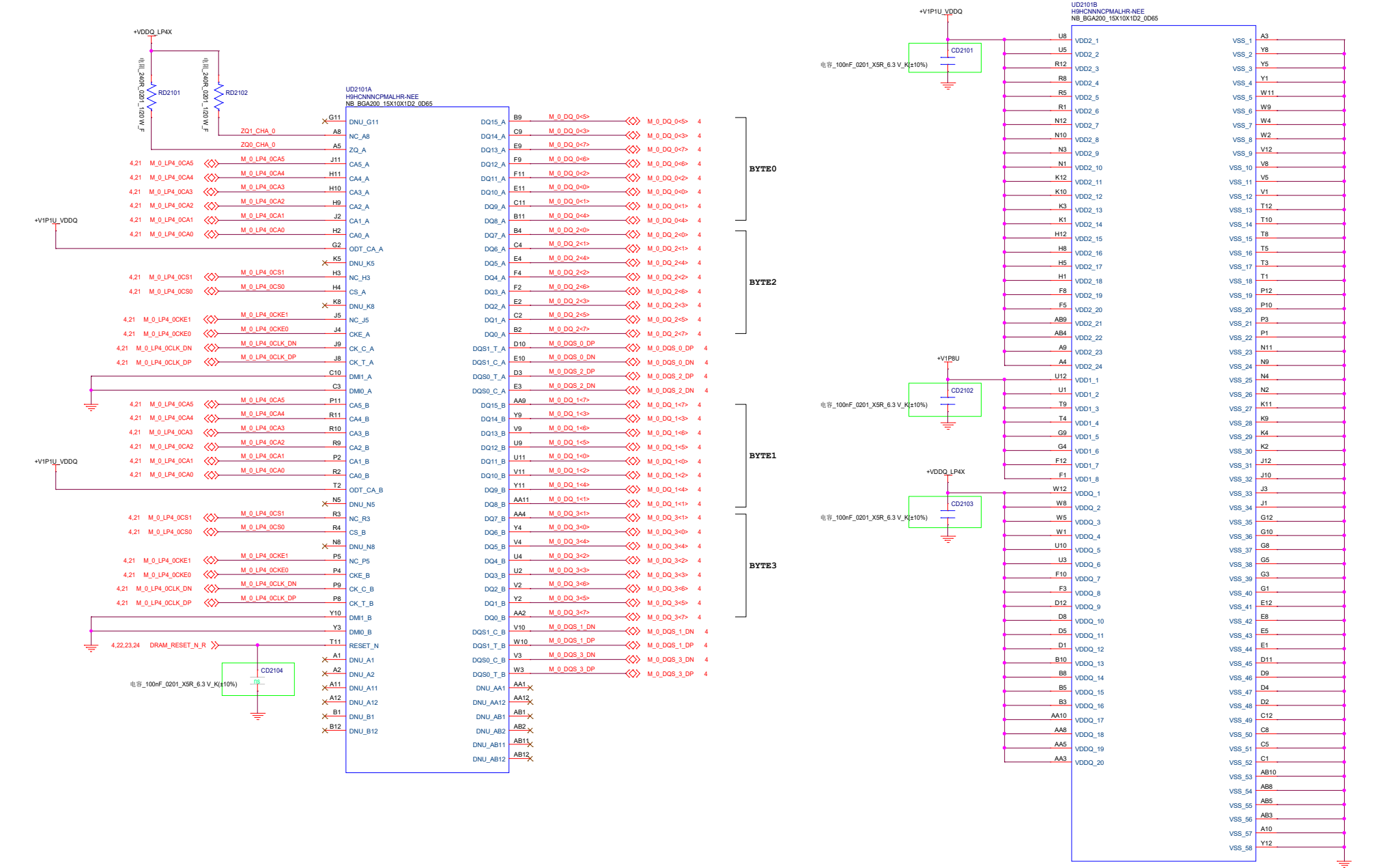


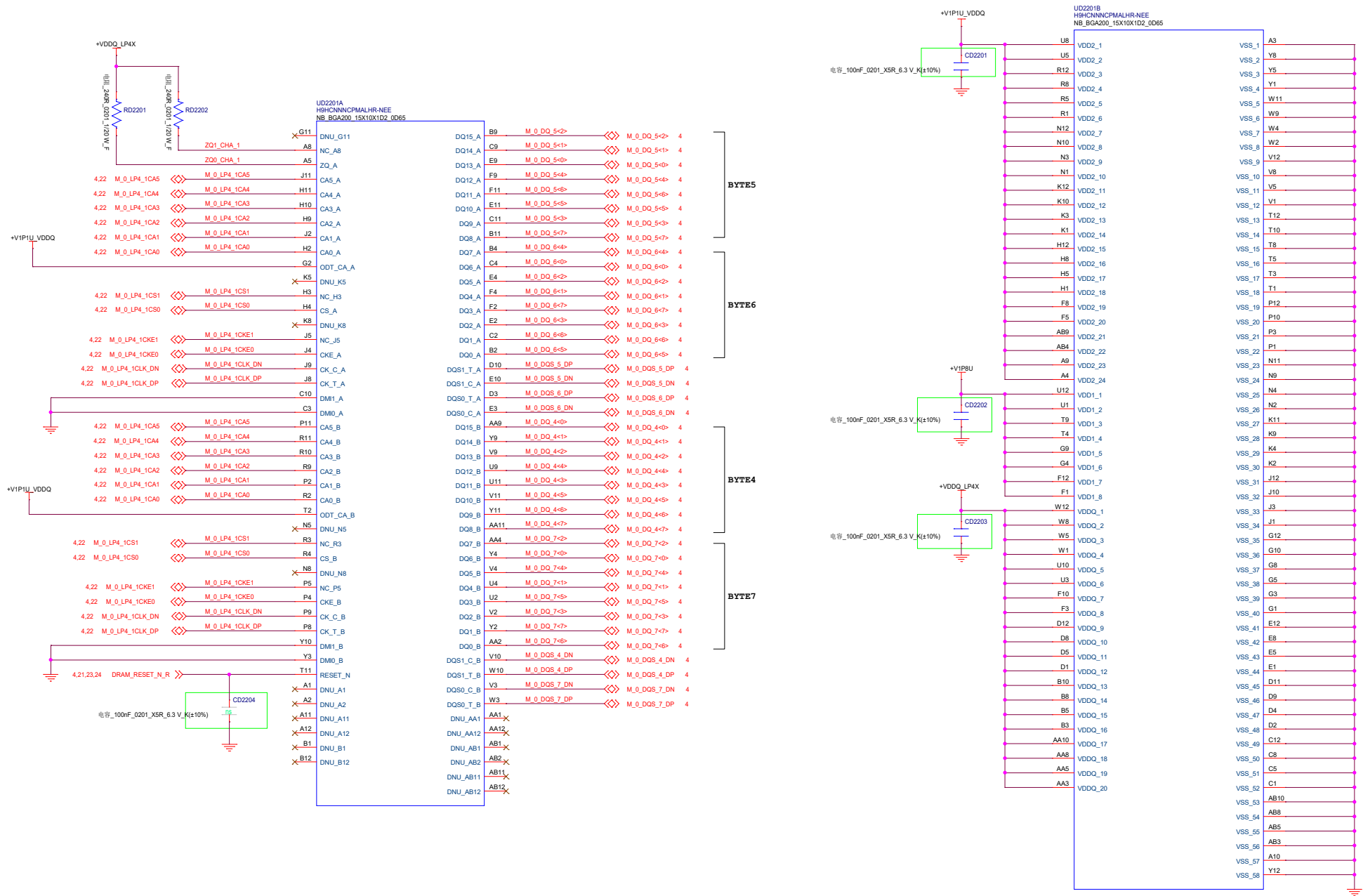
### PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



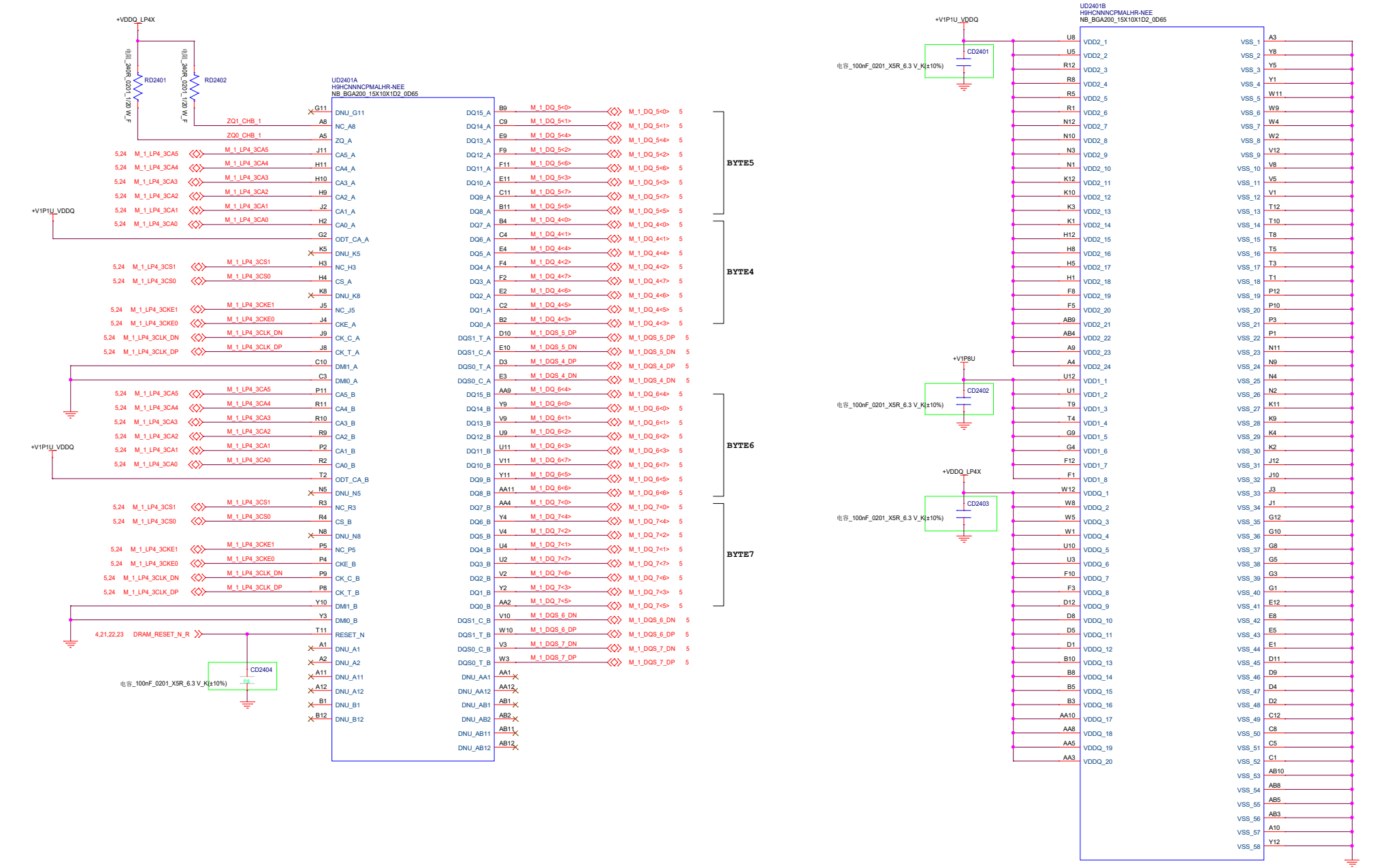
### PLACE CLOSE TO PACKAGE ON PRIMARY SIDE









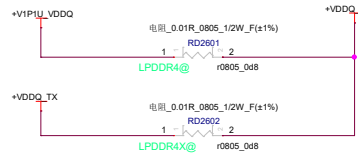
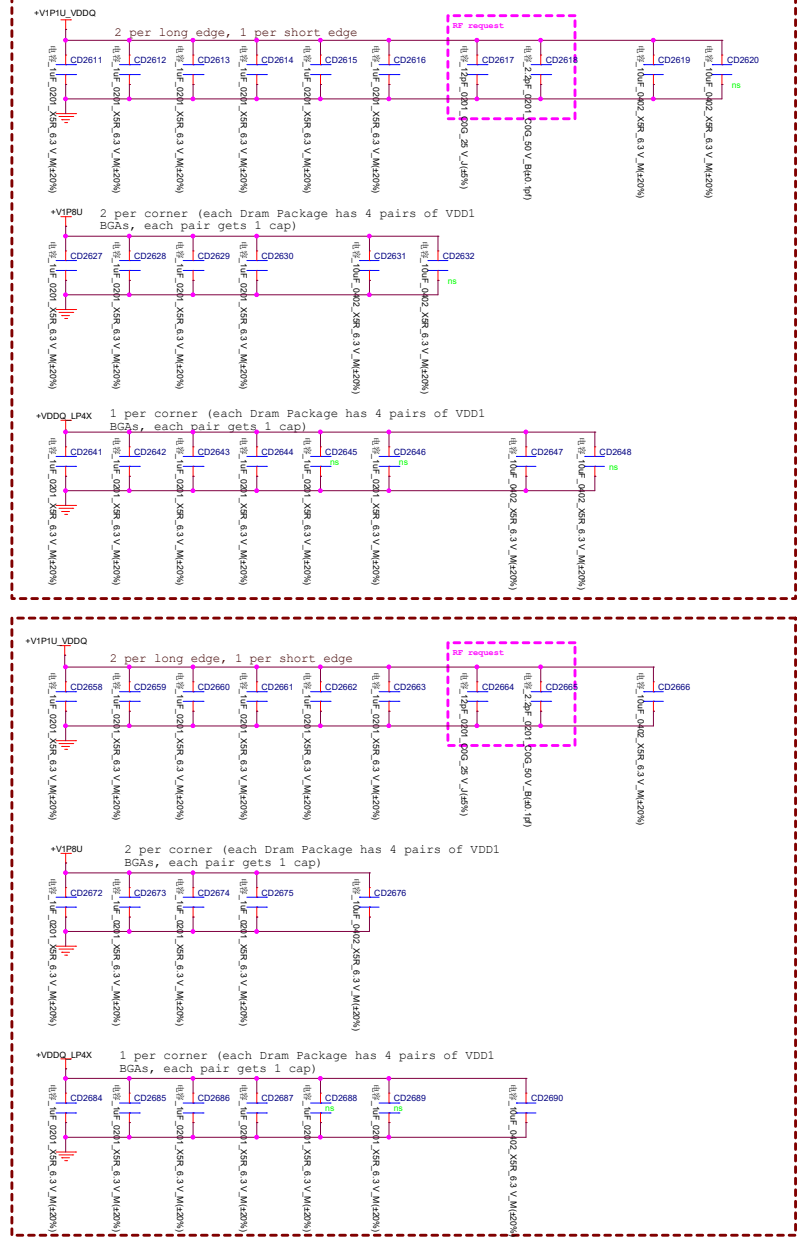




## DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL A



## DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL B



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



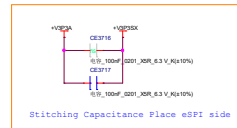
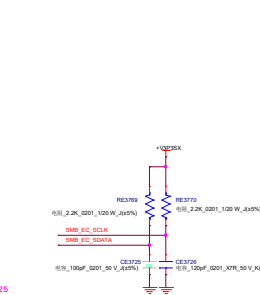
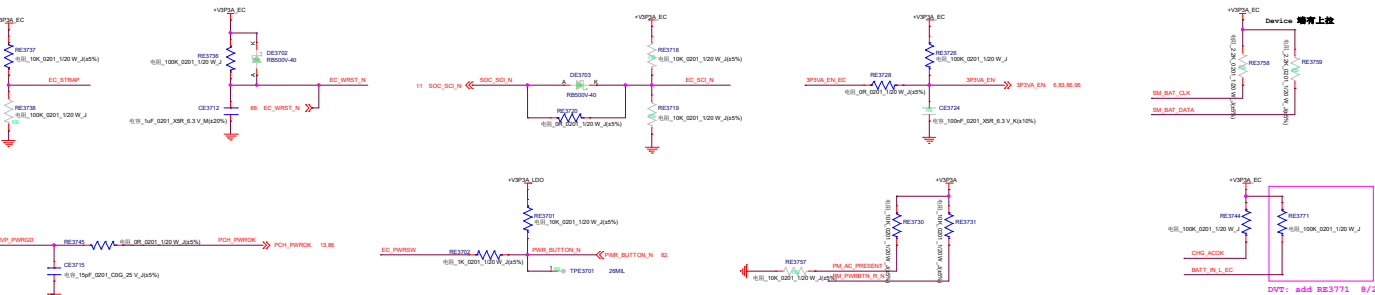
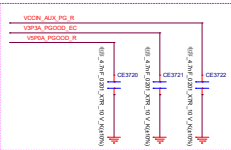
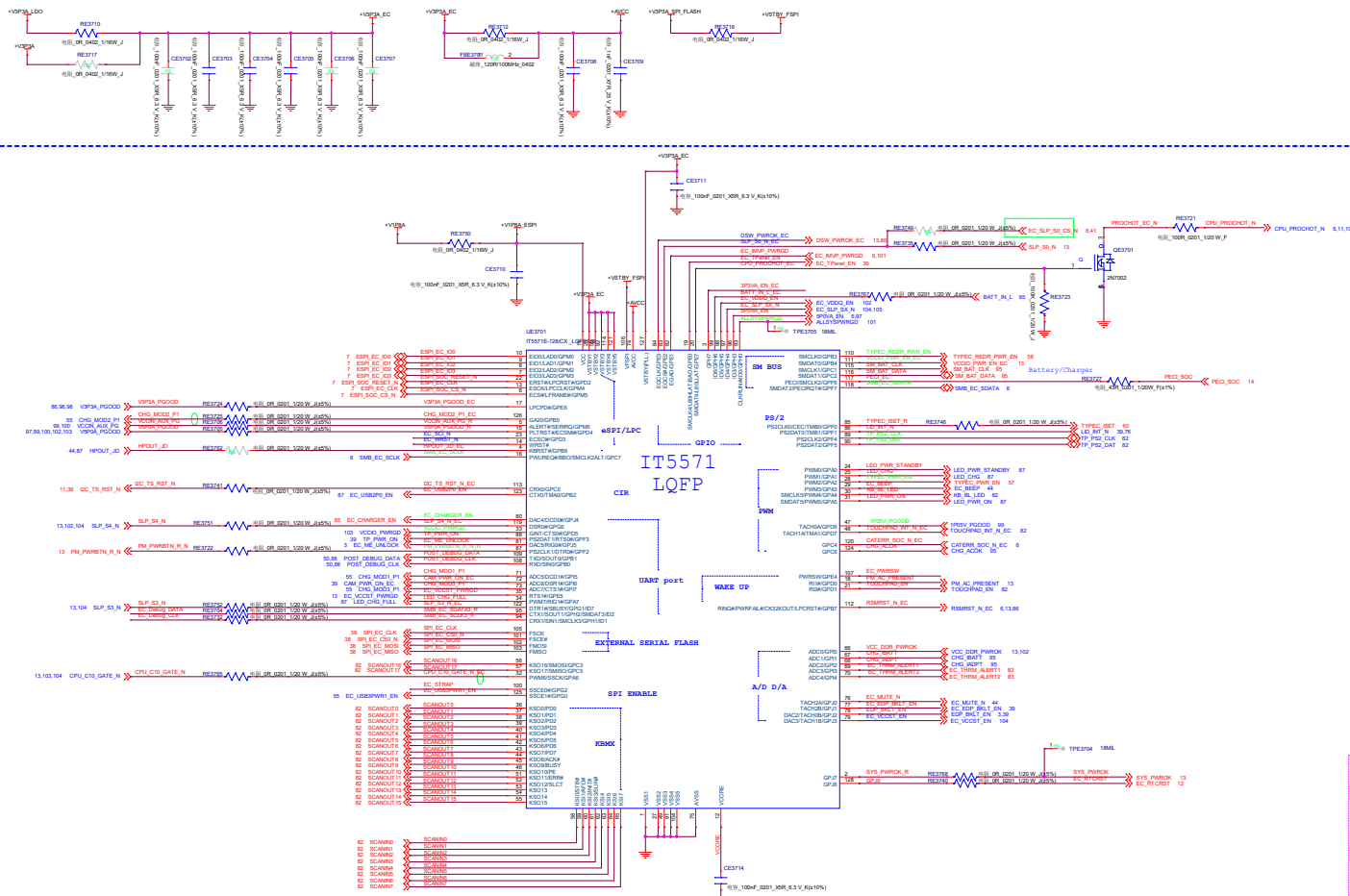


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

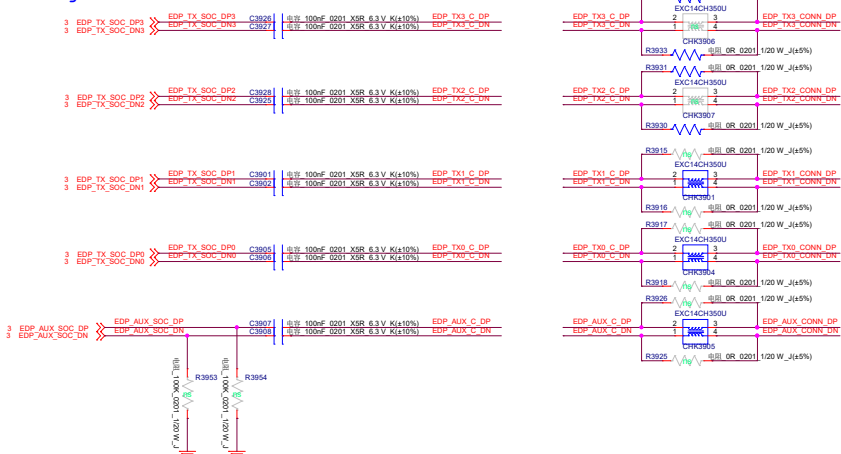
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



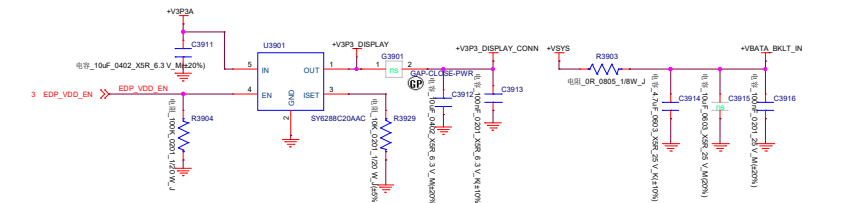




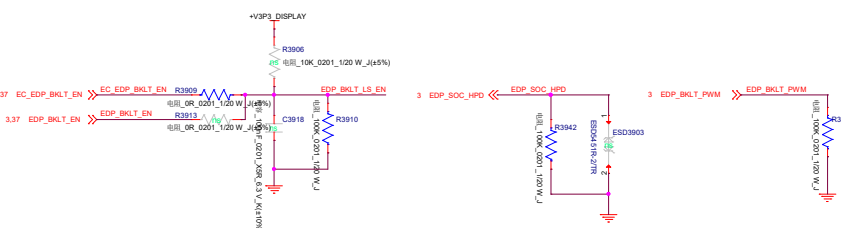
eDP Signal



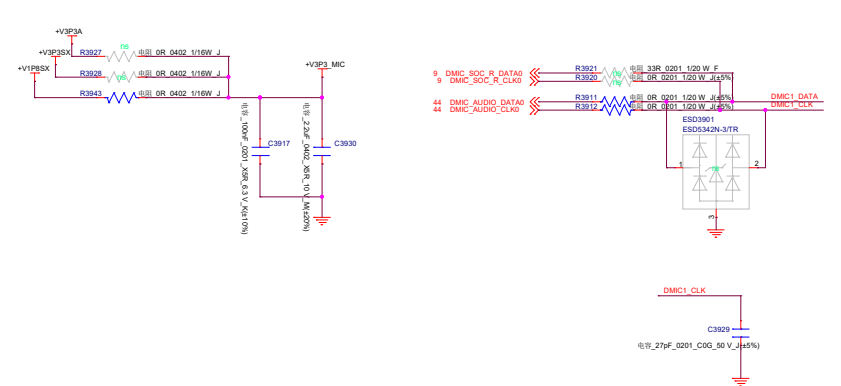
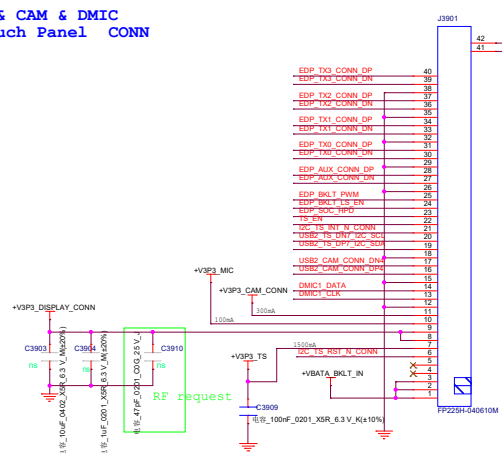
-----  
eDP VCC & BL Power



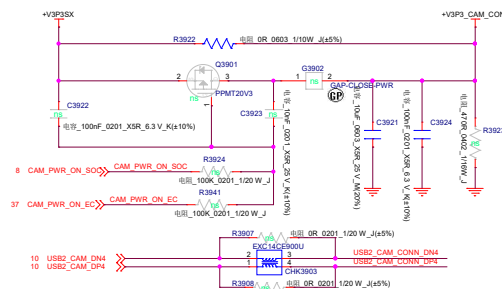
## eDP Control



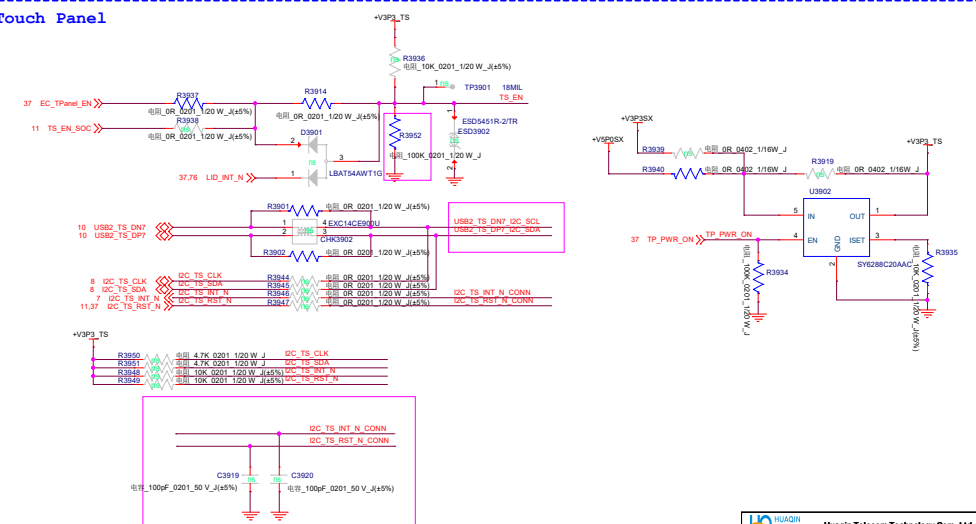
## MIC

eDP & CAM & DMIC  
& Touch Panel CONN

## CAM Power



Touch Panel

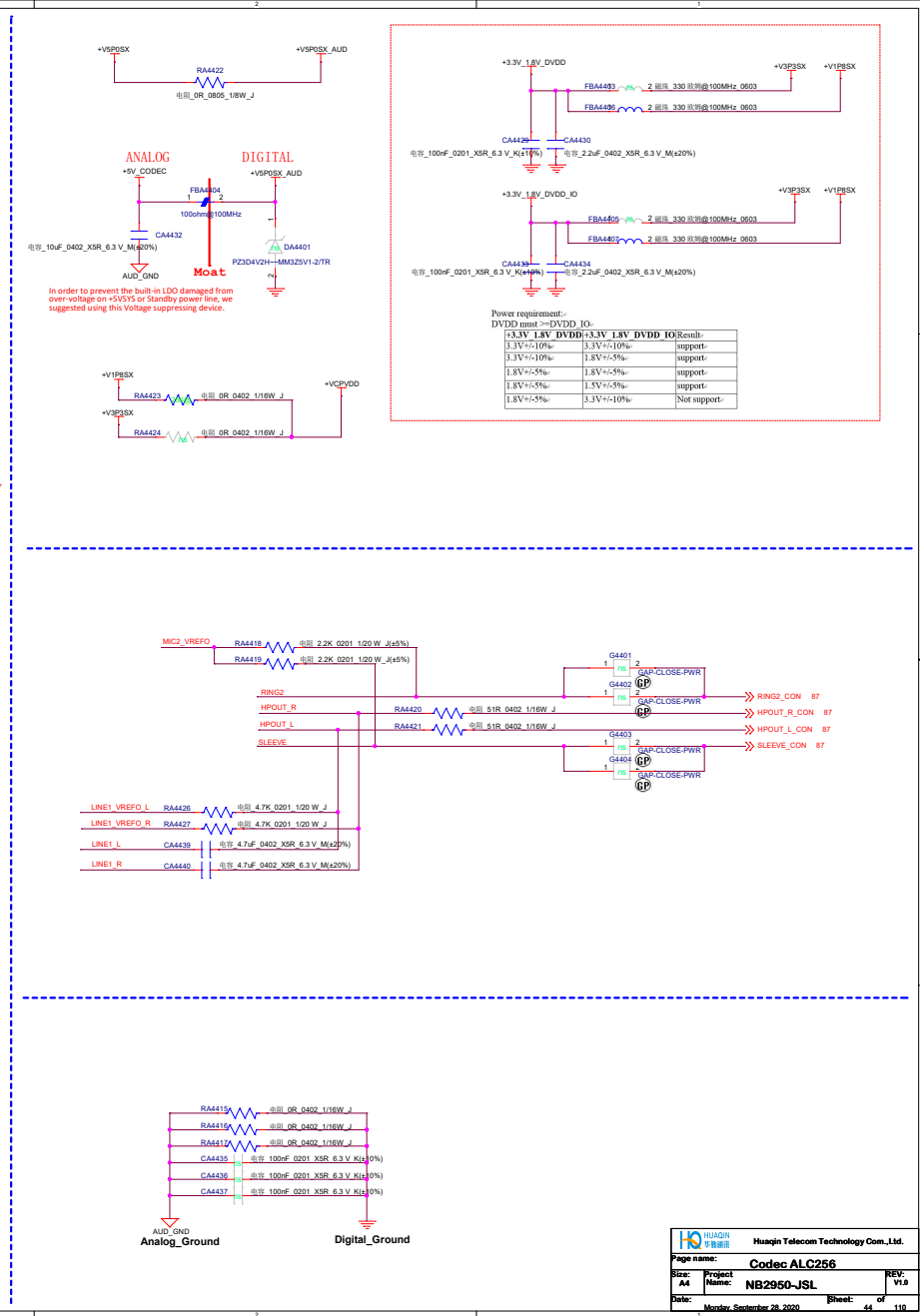
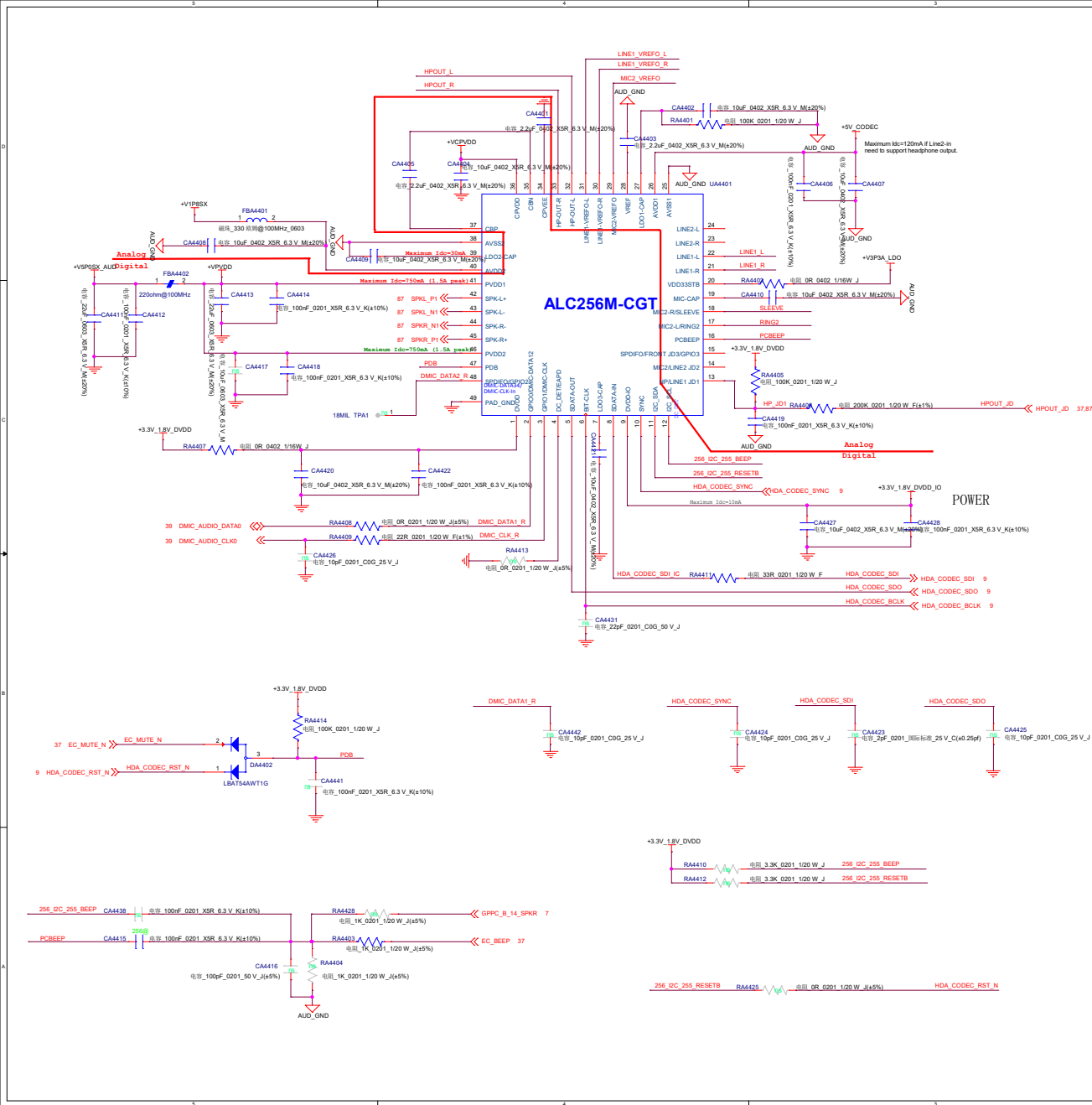















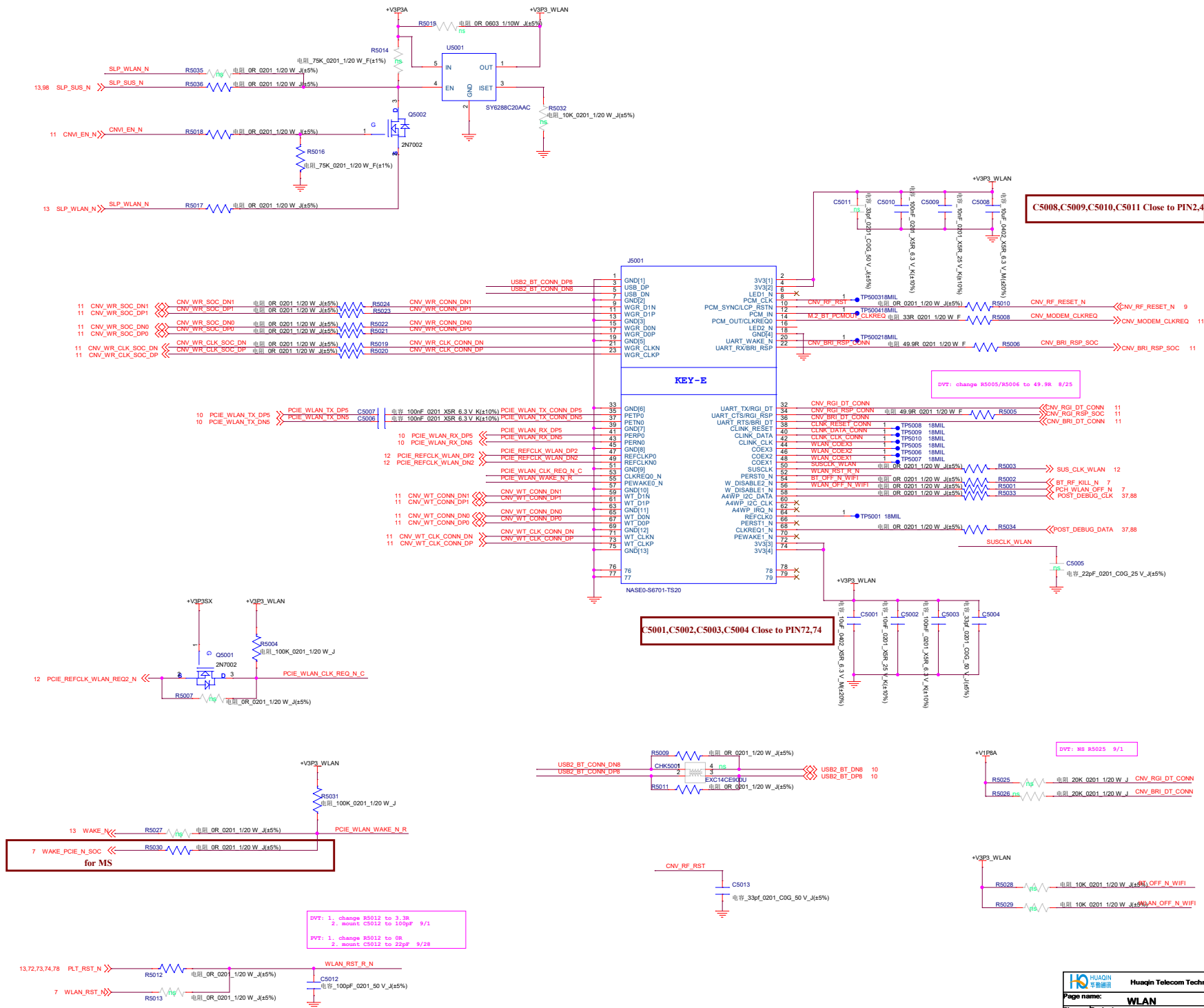
		Huaqin Telecom Technology Com.,Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB2950-JSL	REV: V1.0	
Date: Monday, September 28, 2020	Sheet: 45	of 110	



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

	5	4	3	2	1
D					
C					
B					
A					





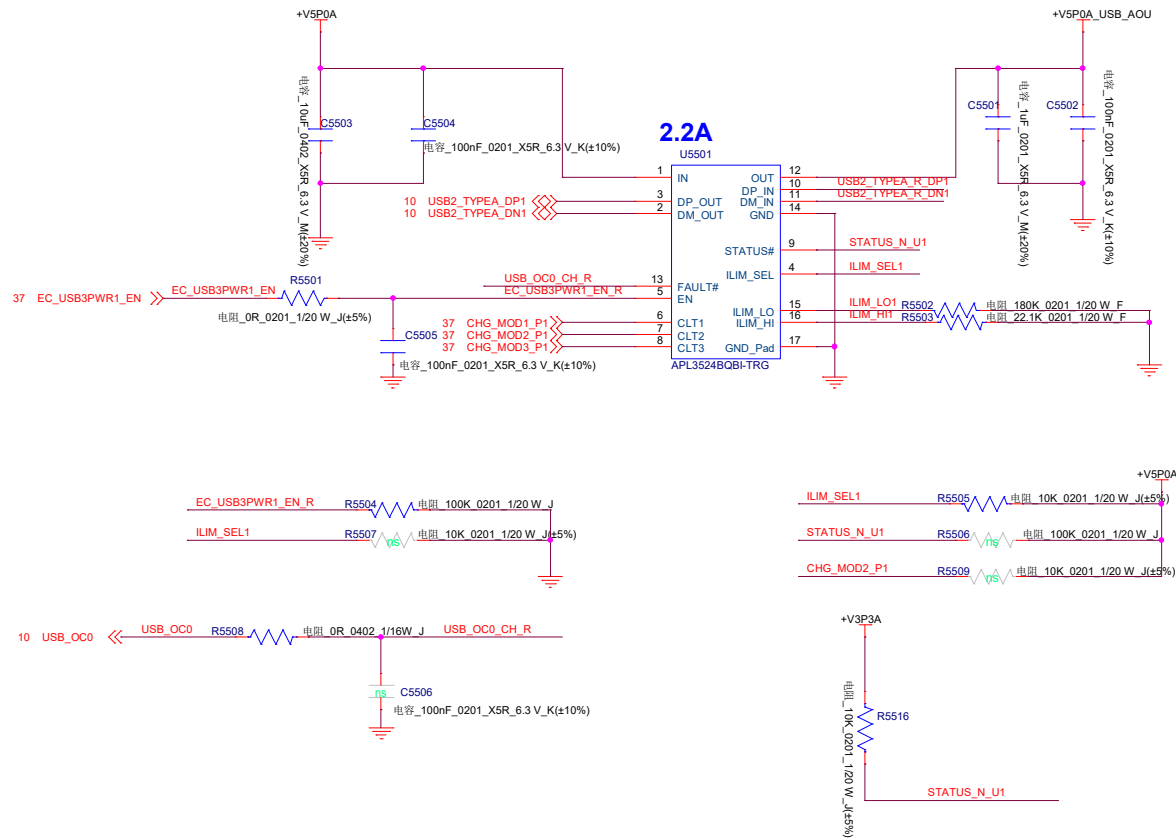


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

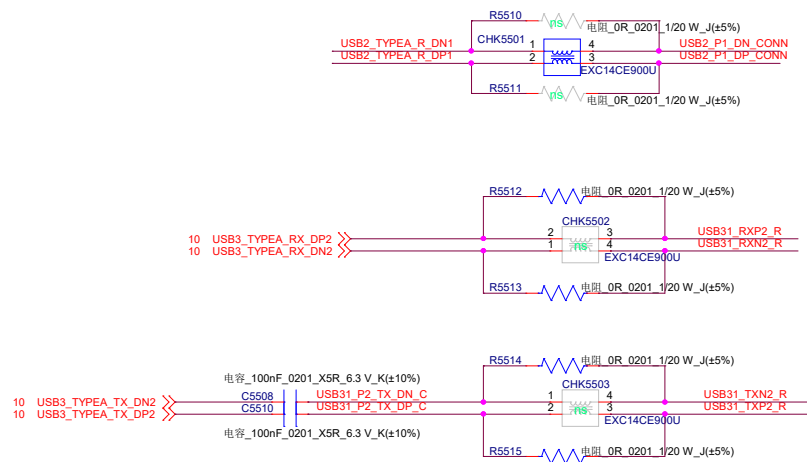
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



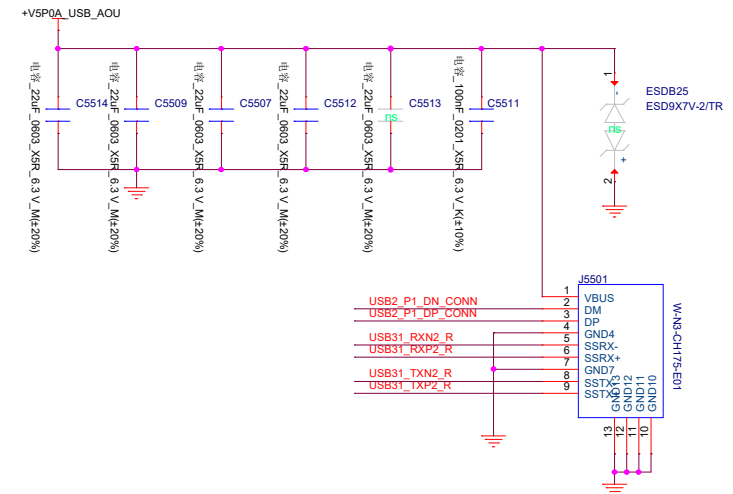
## USB3.1 POWER Port



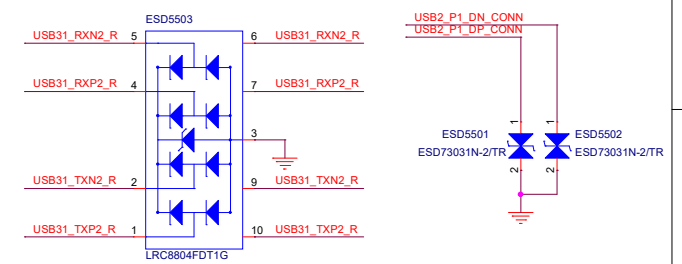
## USB3.1 Signal



## USB3.1 Connector

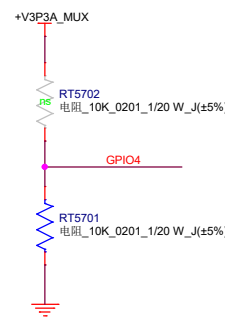
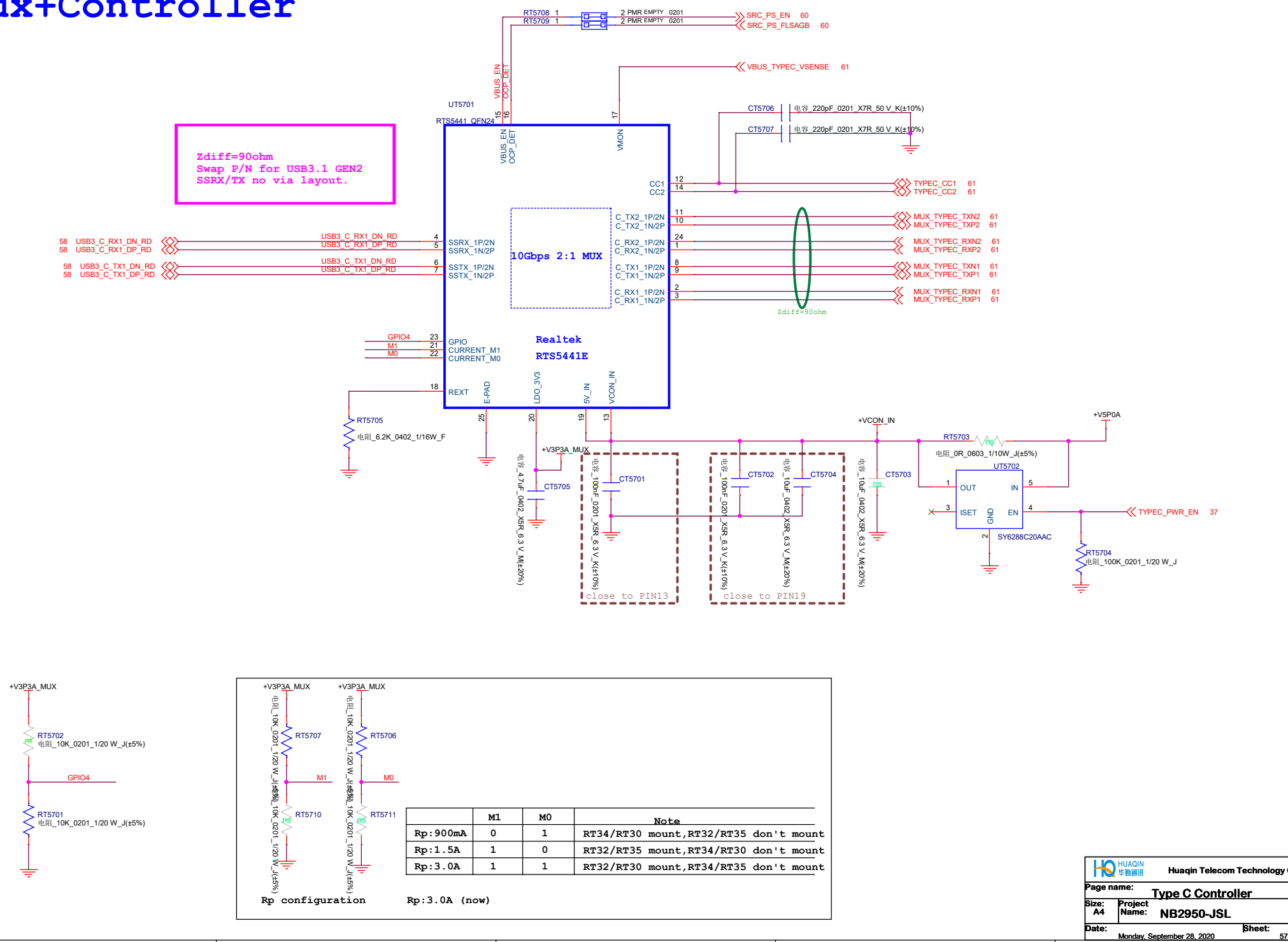


## USB3.1 ESD





Mux+Controller

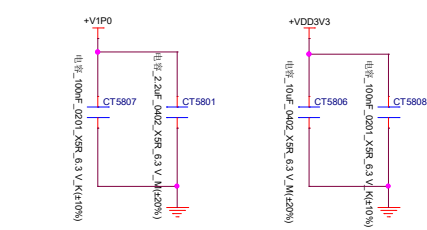
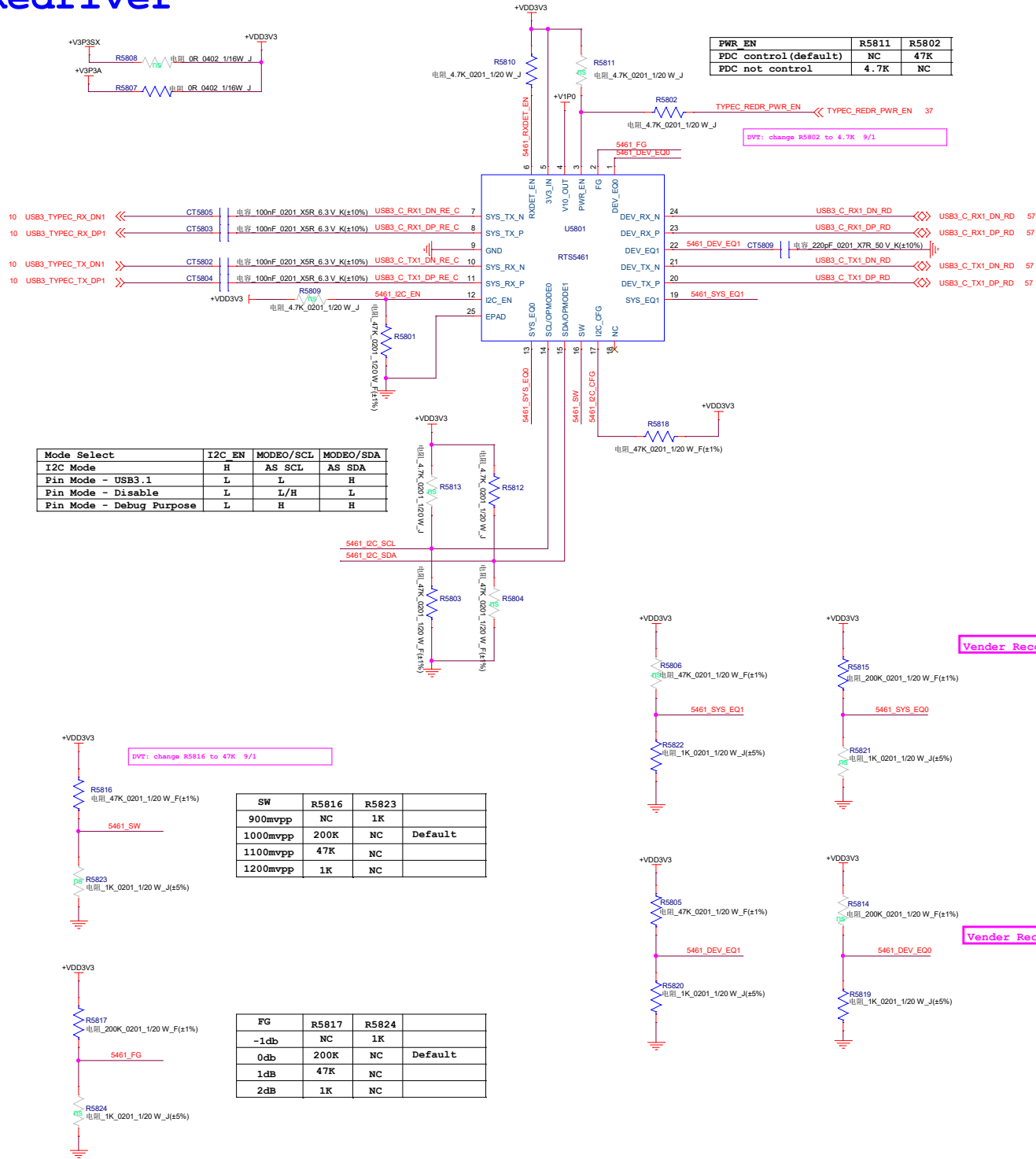


	M1	M0	Note
Rp: 900mA	0	1	RT34/RT30 mount, RT32/RT35 don't mount
Rp: 1.5A	1	0	RT32/RT35 mount, RT34/RT30 don't mount
Rp: 3.0A	1	1	RT32/RT30 mount, RT34/RT35 don't mount

Rp configuration

Rp: 3.0A (now)

Redriver



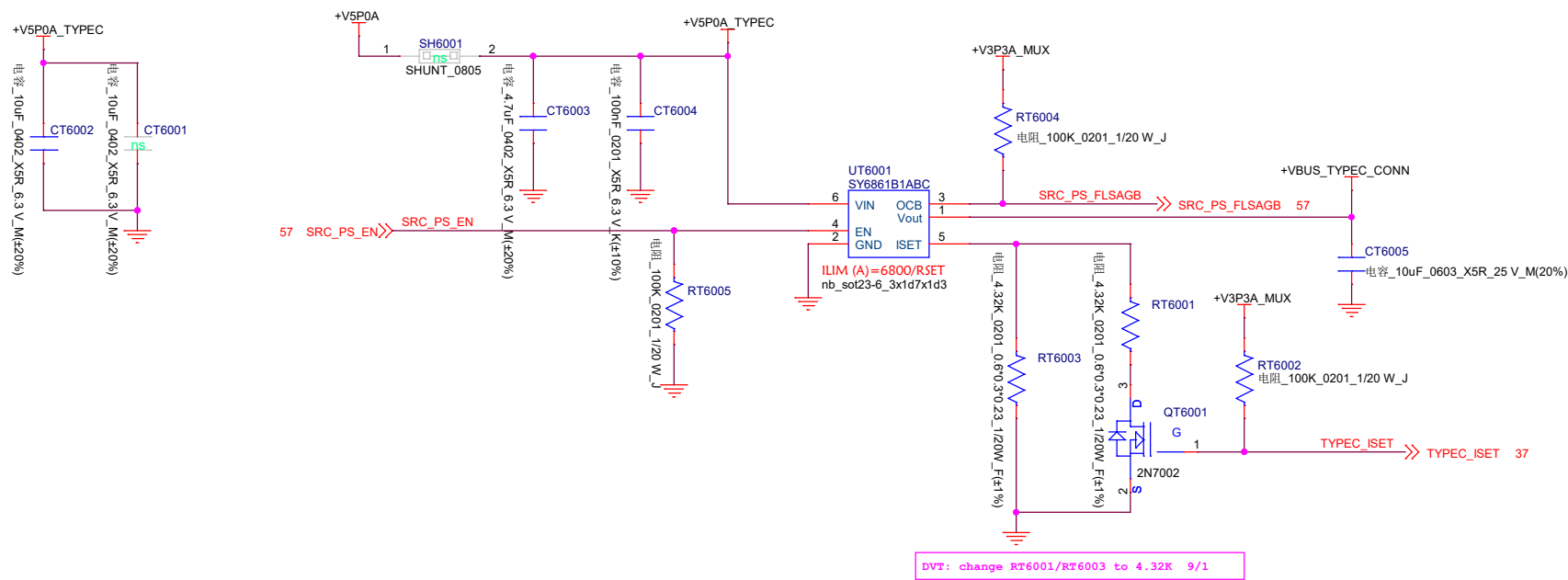
5461_EQX	Rpu	Rpd
L	NC	1K
ML	200K	NC
MH	47K	NC
H	1K	NC

Table 5-3 Host SSTX Channel Equalization Configuration Table				
Host SSTX channel EQ Setting	SYS_EQ1 pin	SYS_EQ0 pin	EQ@2.5GHz (dB)	EQ@5GHz (dB)
0	L	L	-0.3	-0.2
1	L	ML	0.5	1.8
2	L	MH	1.3	3.6
3	L	H	2.2	5.2
4	ML	L	3.2	6.6
5	ML	ML	4.1	7.8
6	ML	MH	5.0	8.9
7	ML	H	5.9	9.8
8	MH	L	6.8	10.3
9	MH	ML	7.6	11.0
10	MH	MH	8.3	11.5
11	MH	H	9.0	12.1
12	H	L	9.7	12.4
13	H	ML	10.3	12.9
14	H	MH	10.9	13.2
15	H	H	11.4	13.6

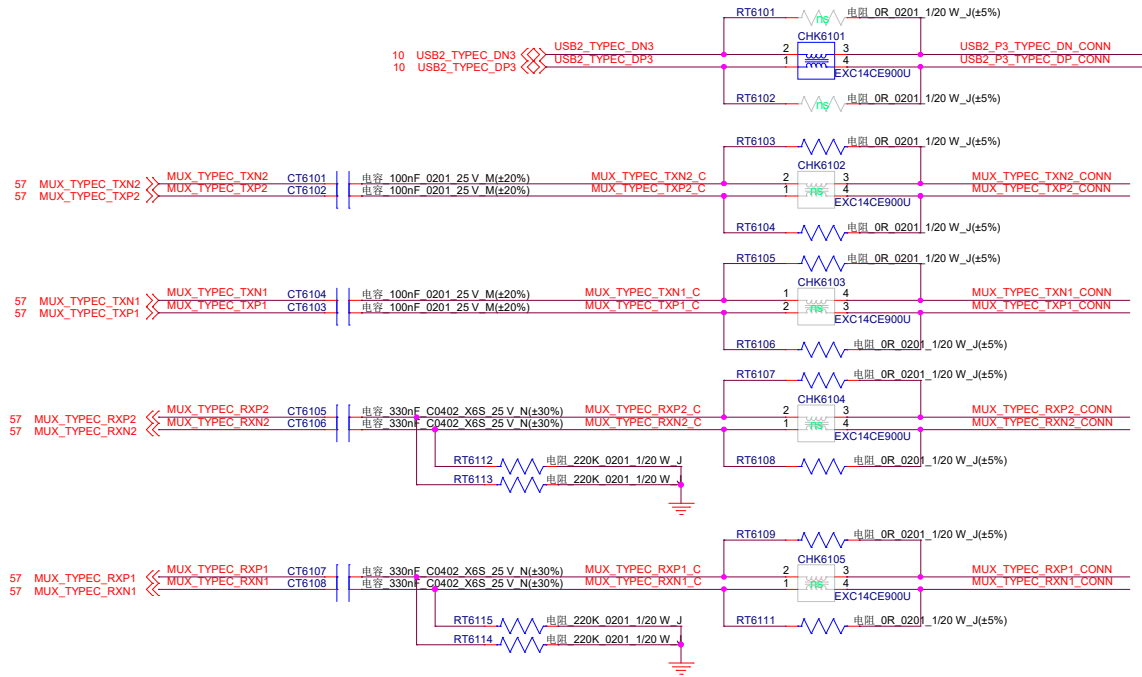
Table 5-4 Host SSRX Channel Equalization Configuration Table				
Host SSRX channel EQ Setting	DEV_EQ1 pin	DEV_EQ0 pin	EQ@2.5GHz (dB)	EQ@5GHz (dB)
0	L	L	-0.3	-0.2
1	L	ML	0.5	1.8
2	L	MH	1.3	3.6
3	L	H	2.2	5.2
4	ML	L	3.2	6.6
5	ML	ML	4.1	7.8
6	ML	MH	5.0	8.9
7	ML	H	5.9	9.8
8	MH	L	6.8	10.3
9	MH	ML	7.6	11.0
10	MH	MH	8.3	11.5
11	MH	H	9.0	12.1
12	H	L	9.7	12.4
13	H	ML	10.3	12.9
14	H	MH	10.9	13.2
15	H	H	11.4	13.6

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

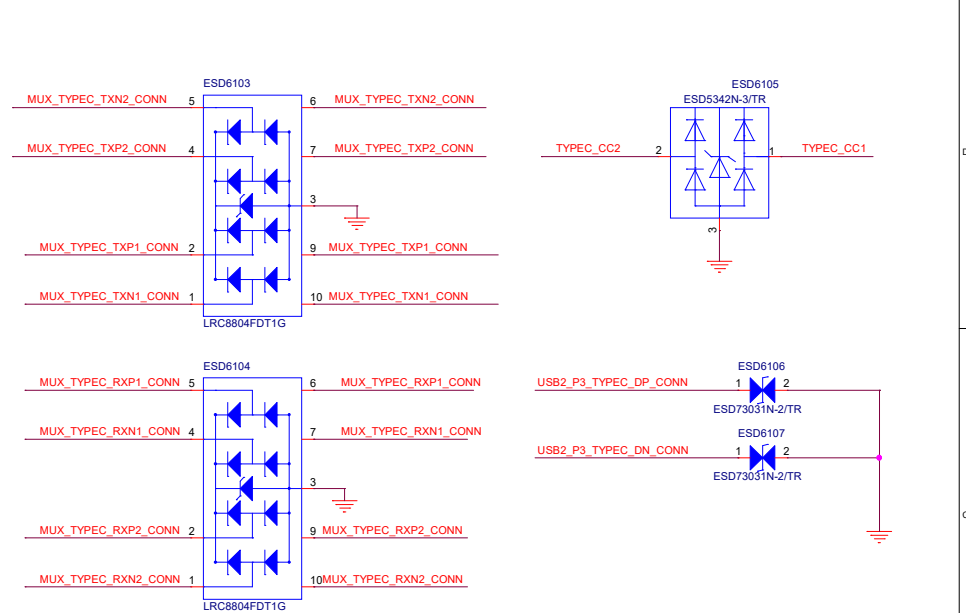
# TYPEC Output



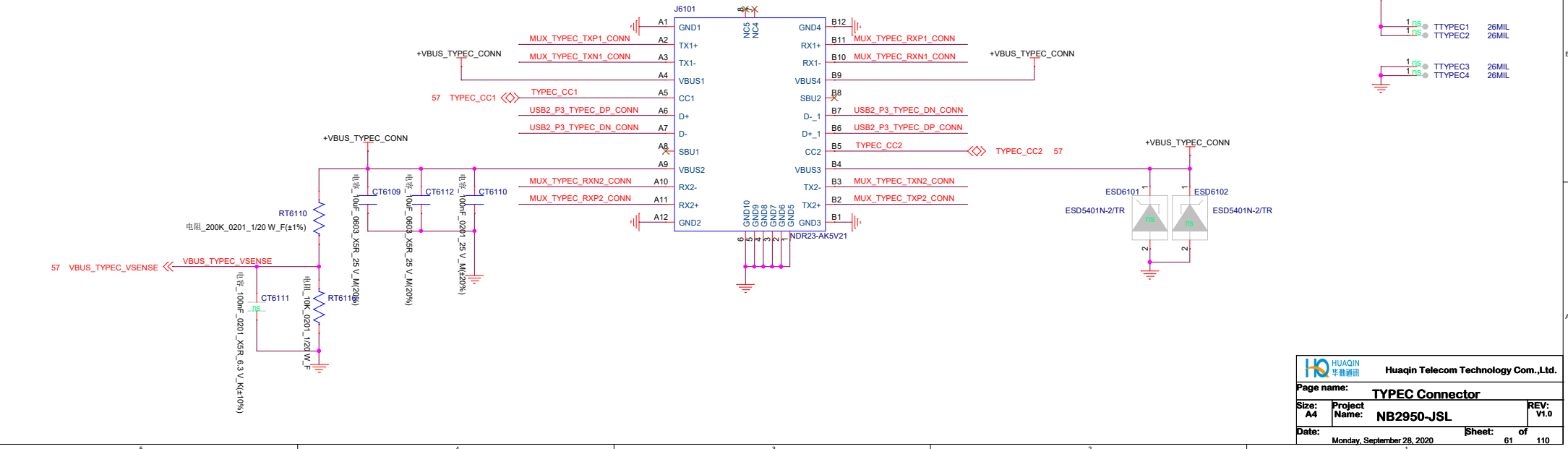
TYPE-C Signal



TYPE-C ESD



TYPE-C Connector



	5	4	3	2	1
D					
C					
B					
A					

	5	4	3	2	1
D					
C					
B					
A					






5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1





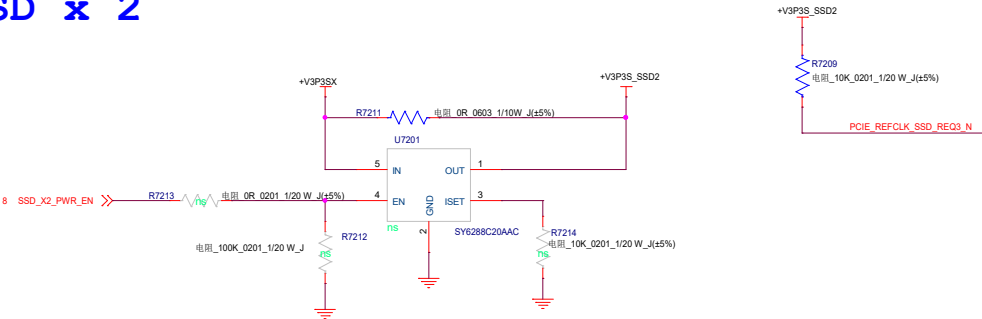
		Huaqin Telecom Technology Com.,Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB2950-JSL	REV: V1.0	
Date: Monday, September 28, 2020	Sheet: 68	of 110	

	5	4	3	2	1
D					
C					
B					
A					

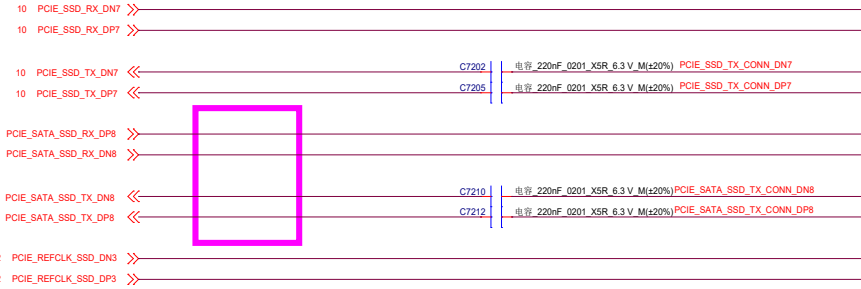




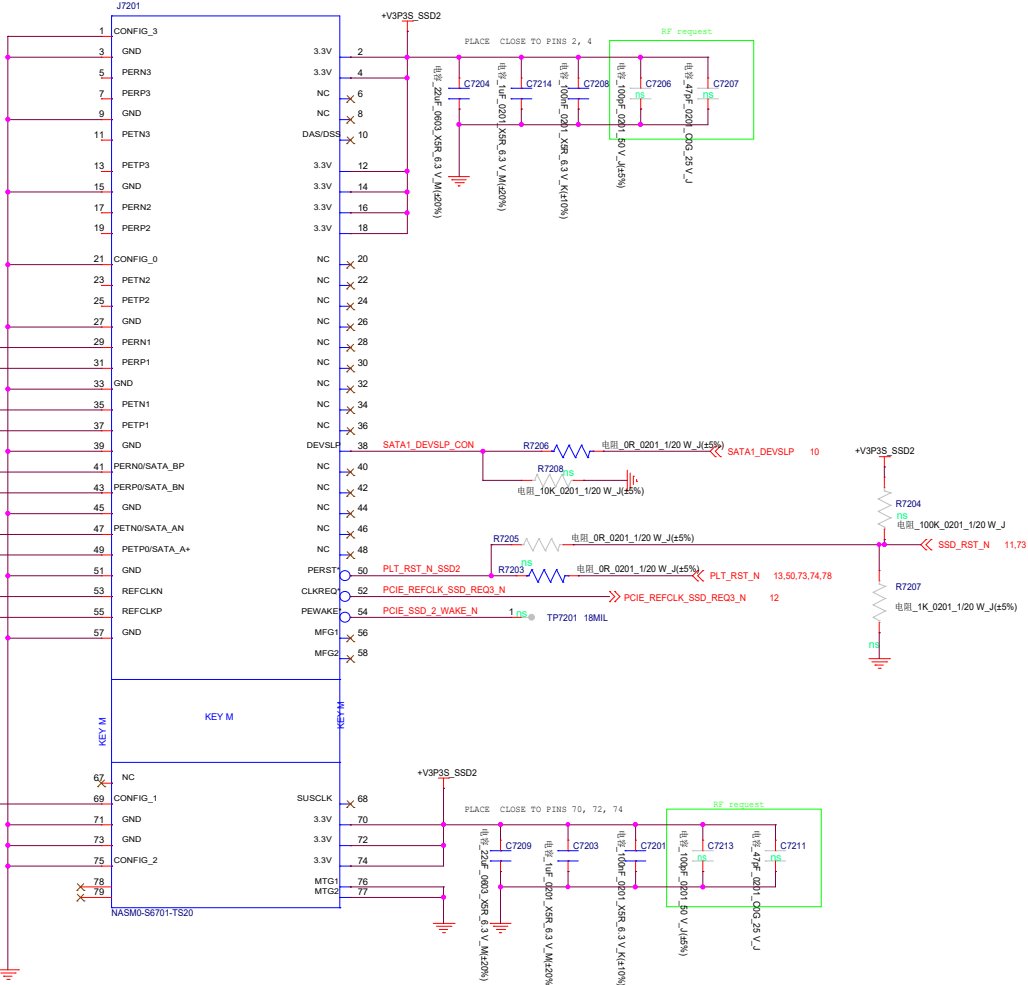
SSD x 2



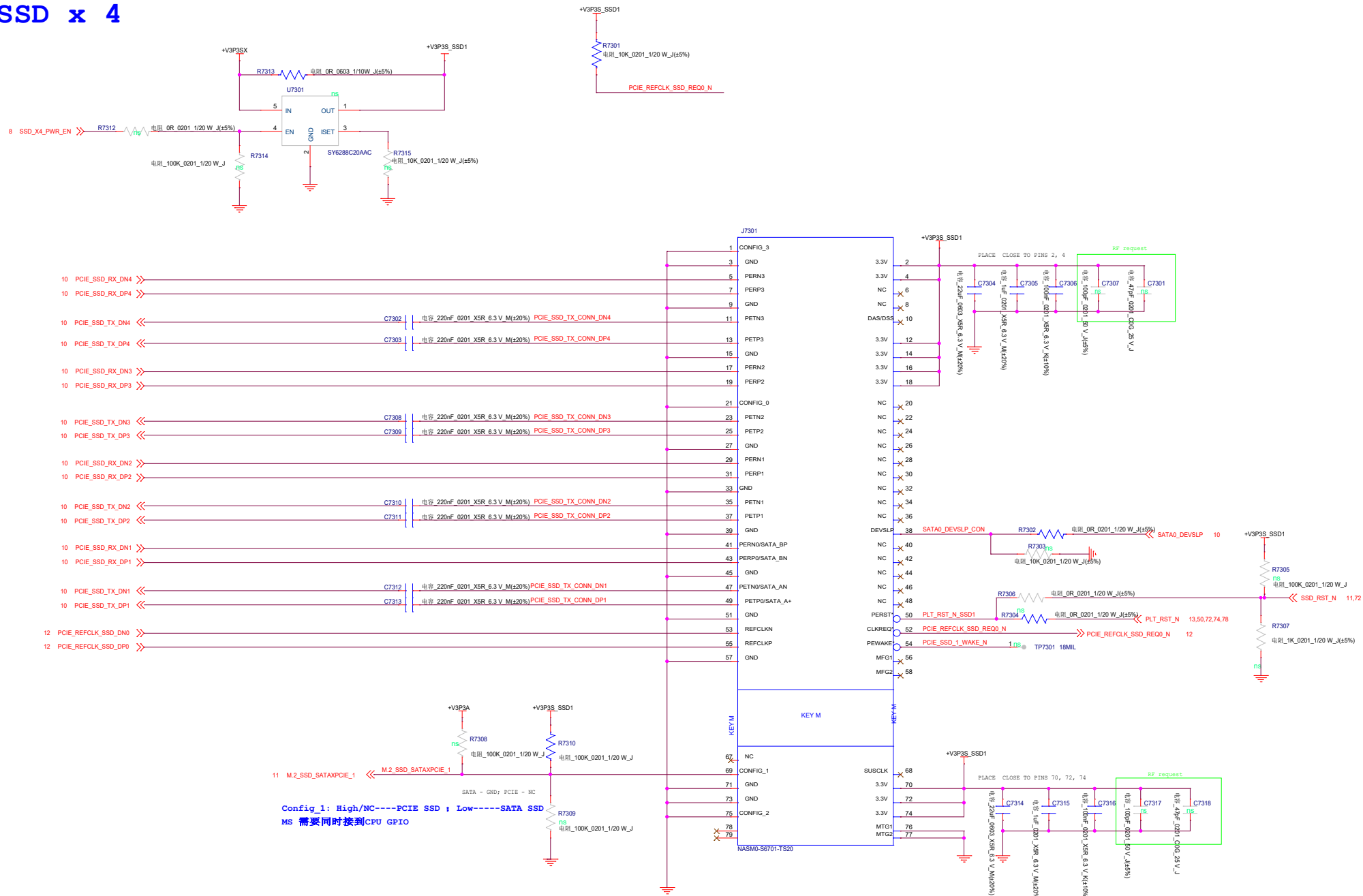
PCIE3.0 X2 & SATA3.0 X1

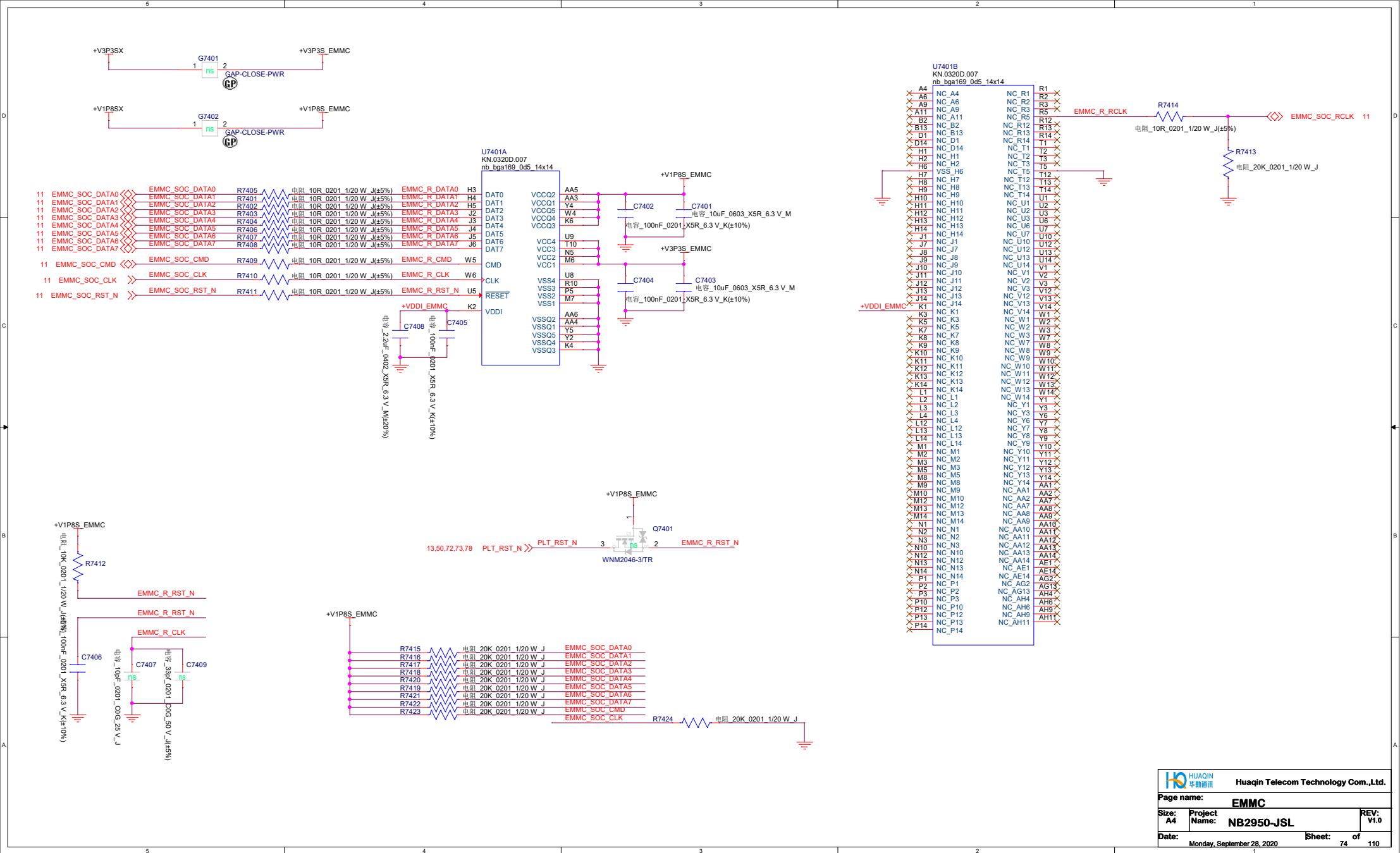


Config 1: High/NC---PCIE SSD only  
MS 需要同时接到CPU GPIO



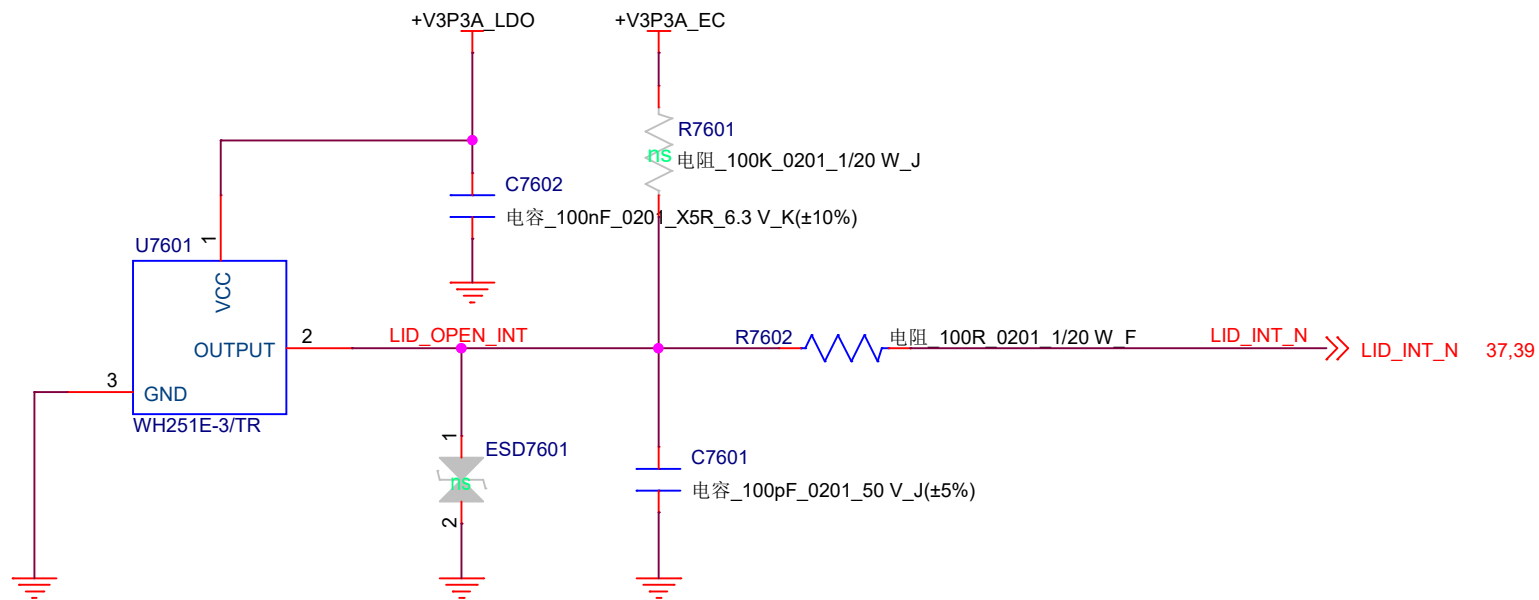
# SSD x 4



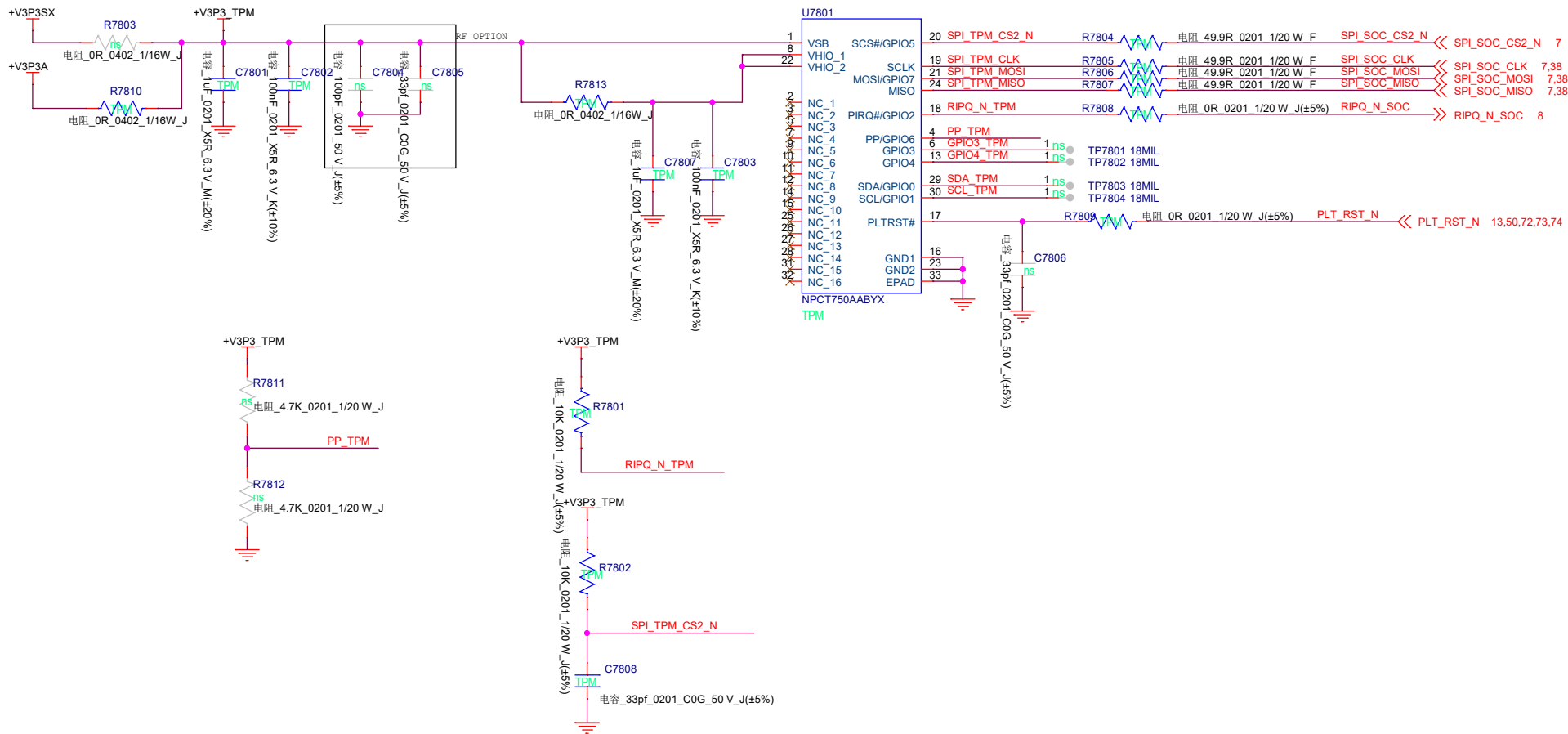


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

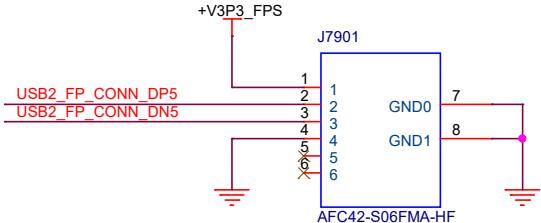
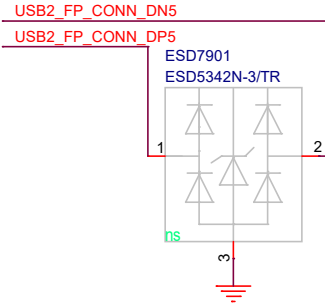
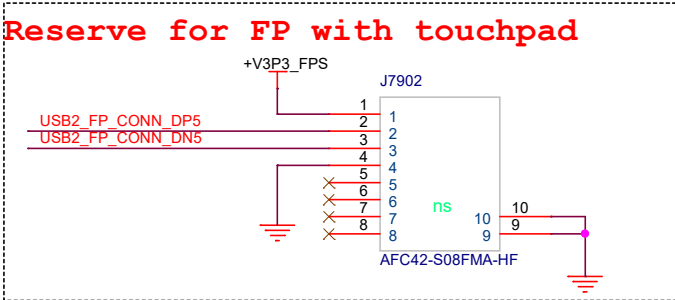
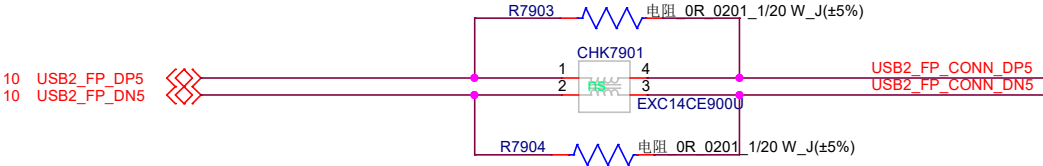
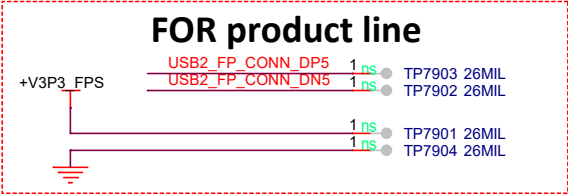
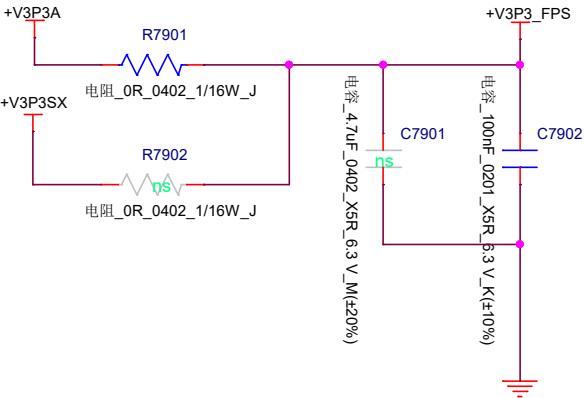
# HALL



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



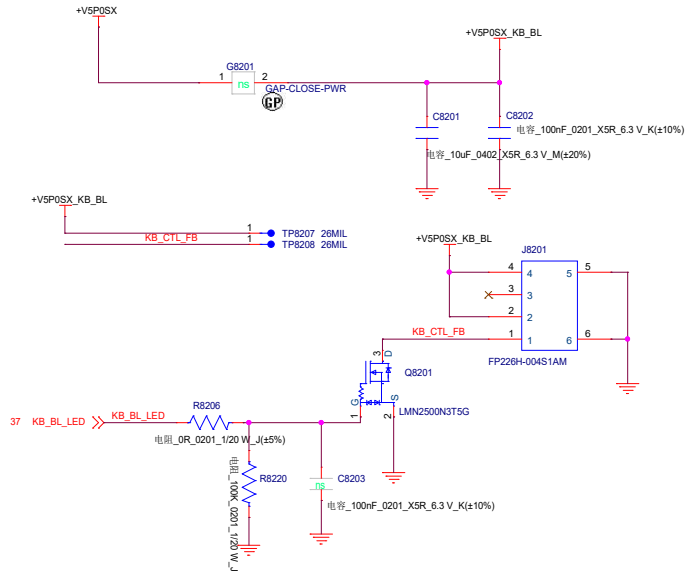
# Finger Print





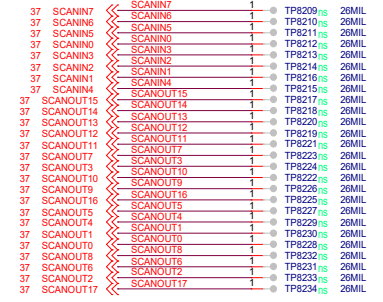
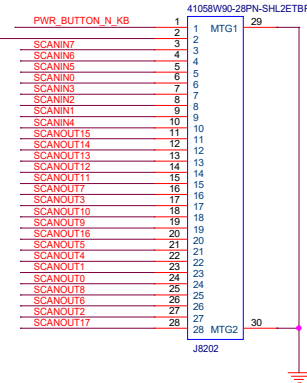
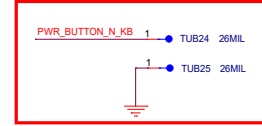
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

## KB Backlight

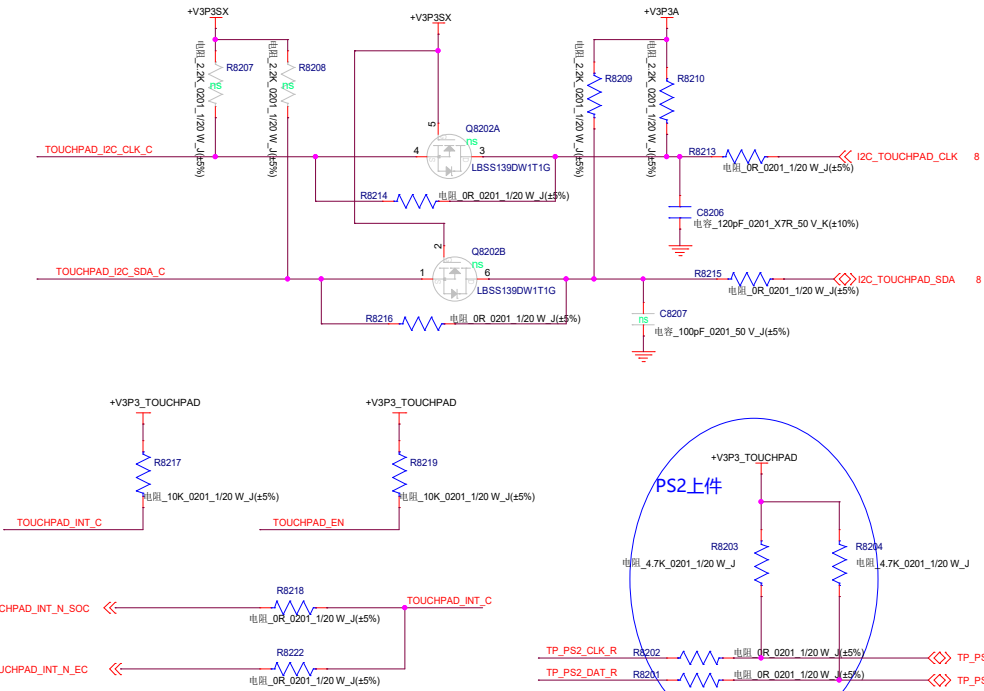


## KB CONN

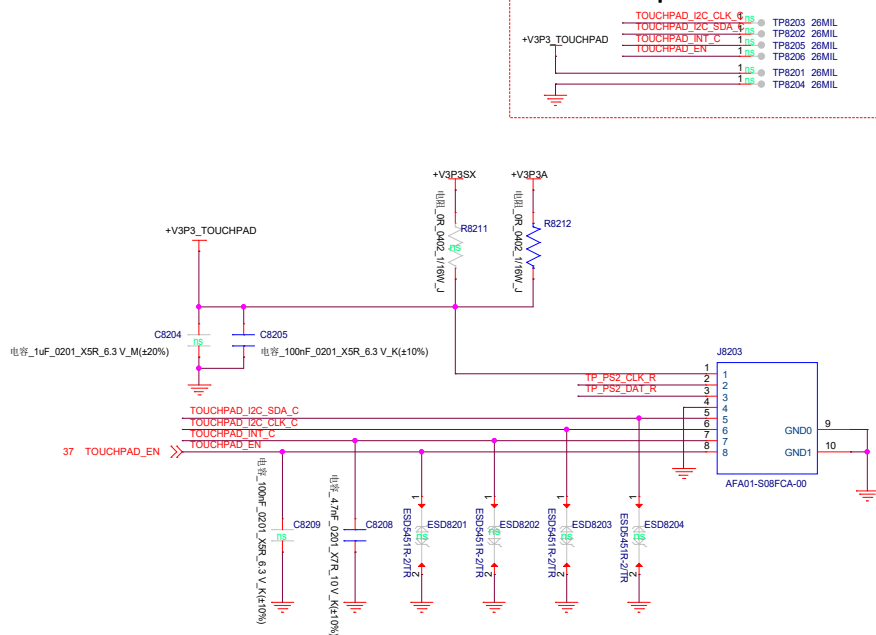
2 Test Point place on Bottom Lay and have a 2mm Air Gap



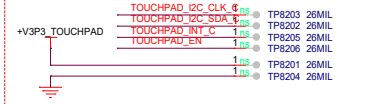
## Touch Pad



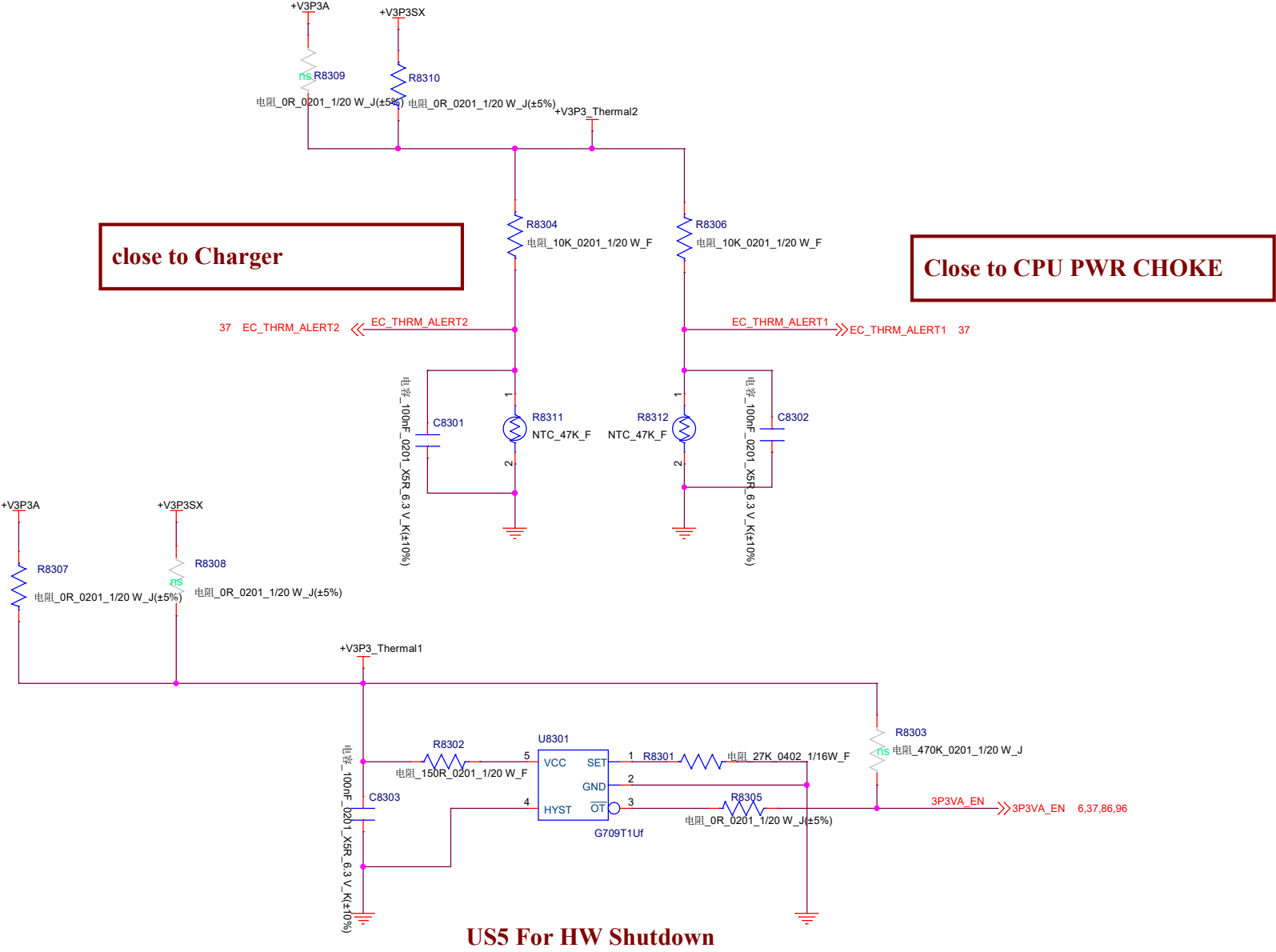
## Touch Pad CONN




FOR product line



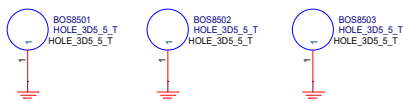
REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"  
Connect guard traces to GND on either side of the  
DXP-DXN traces



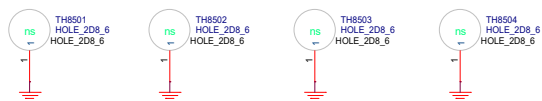
		Huaqin Telecom Technology Com.,Ltd.	
Page name: Thermal sensor			
Size: A4	Project Name: NB2950-JSL	REV: V1.0	
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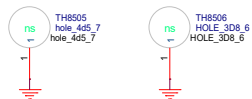
## Thermal Pad BOSS \*3



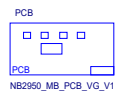
## HOLE \*4



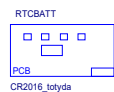
## HOLE \*2



## PCB



## RTC

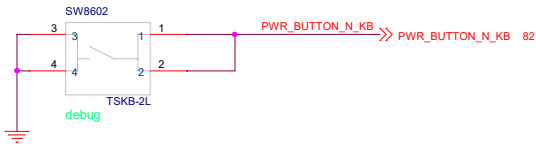


Reset BUTTON

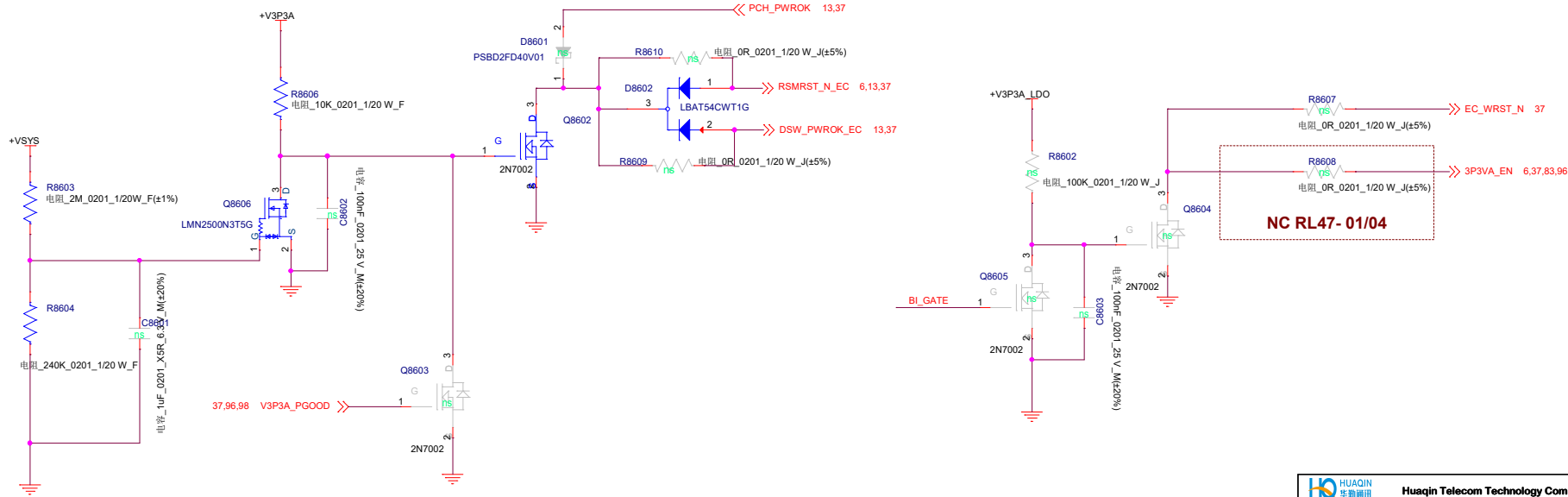


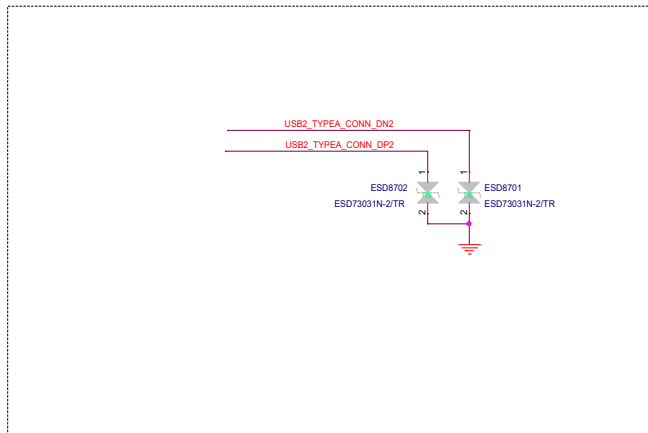
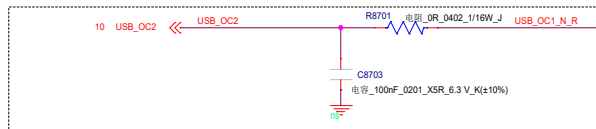
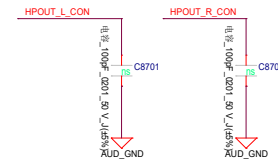
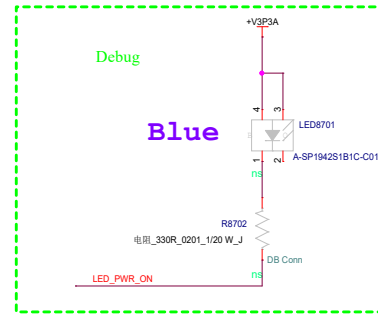
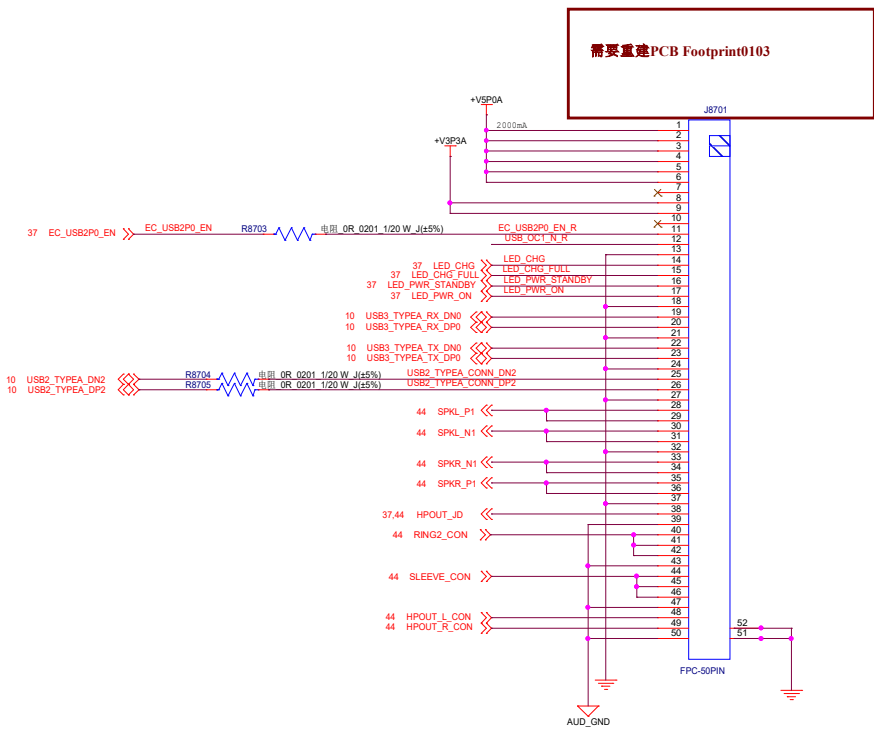
Open door BUTTON

Debug BUTTON

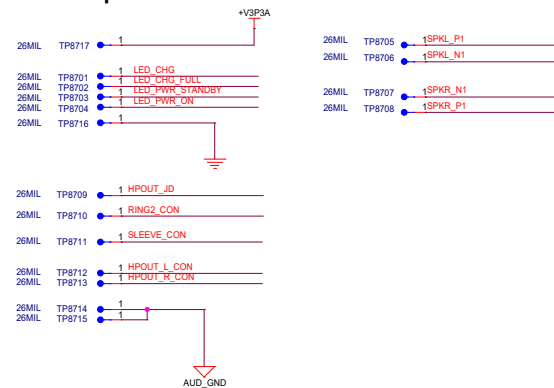


Abnormal PD logic





## FOR product line





5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



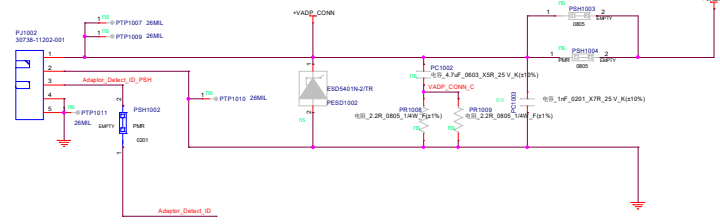


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

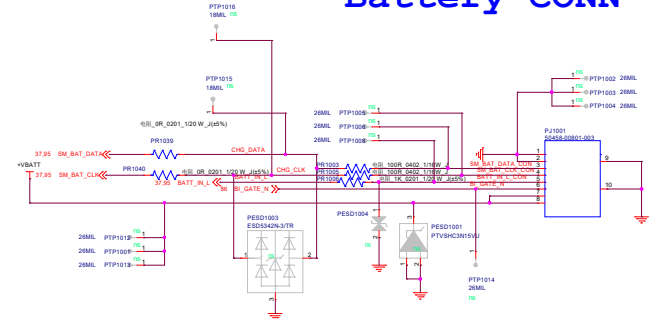
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

CHG\_ACLK 37.95  
SM\_BAT\_DATA 37.95  
SM\_BAT\_CLA 37.95  
BATT\_PL 37.95  
CHG\_BATT 37.95  
CHG\_BATT 37.95

## DC IN

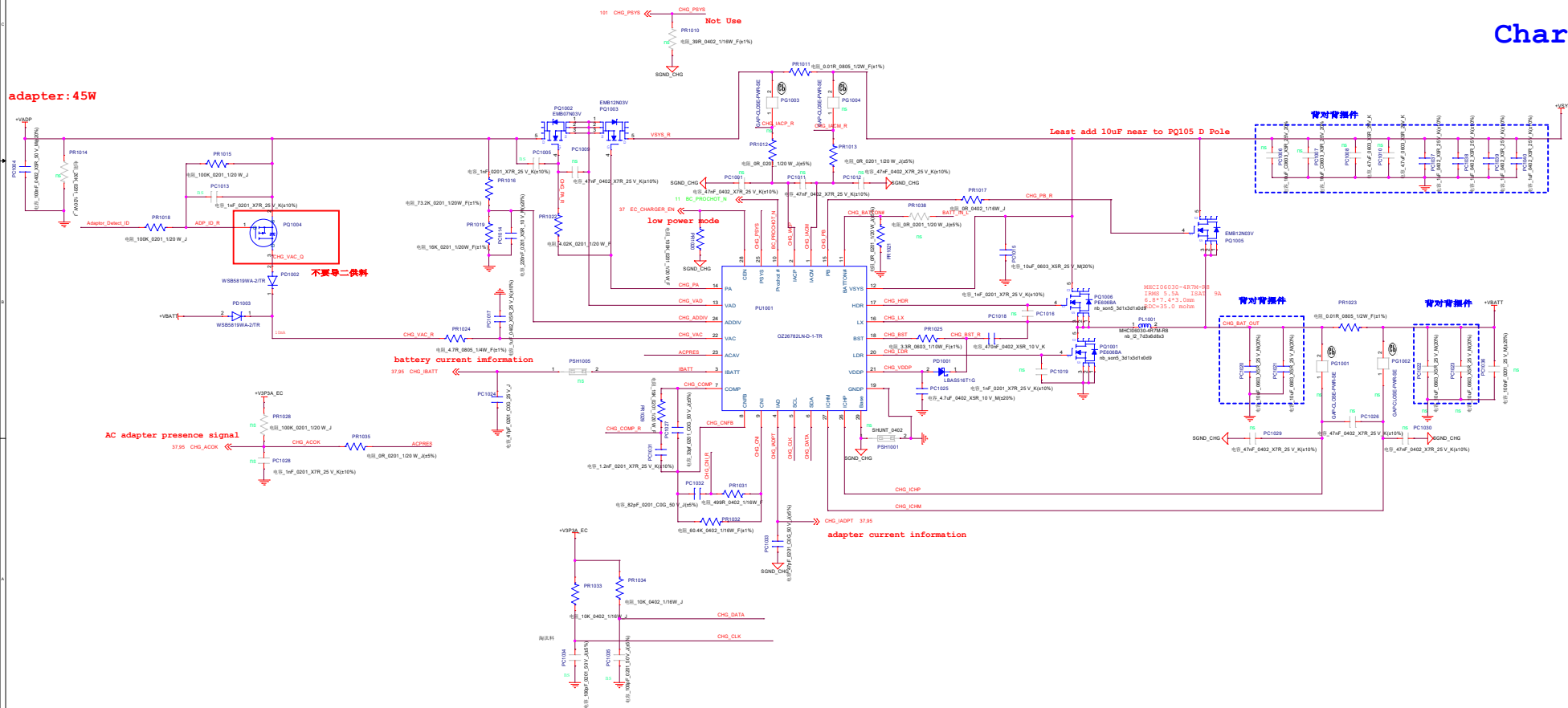


## Battery CONN



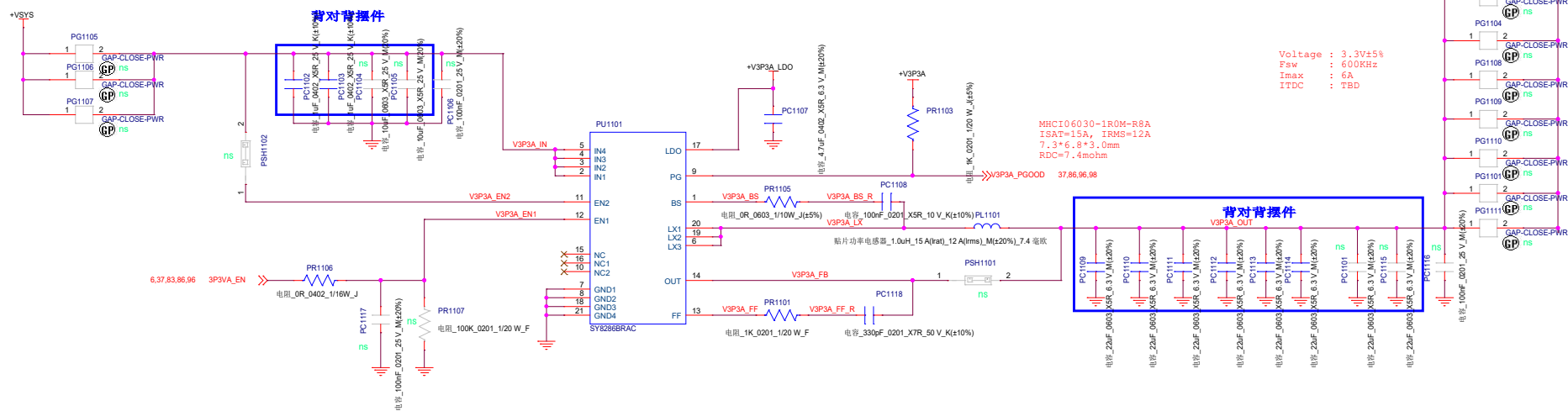
## Charger

adaptee: 45W



3P3VA\_EN 6.37,83,96,96  
V3P3A\_PG00D 37,86,96,98

+V3P3A

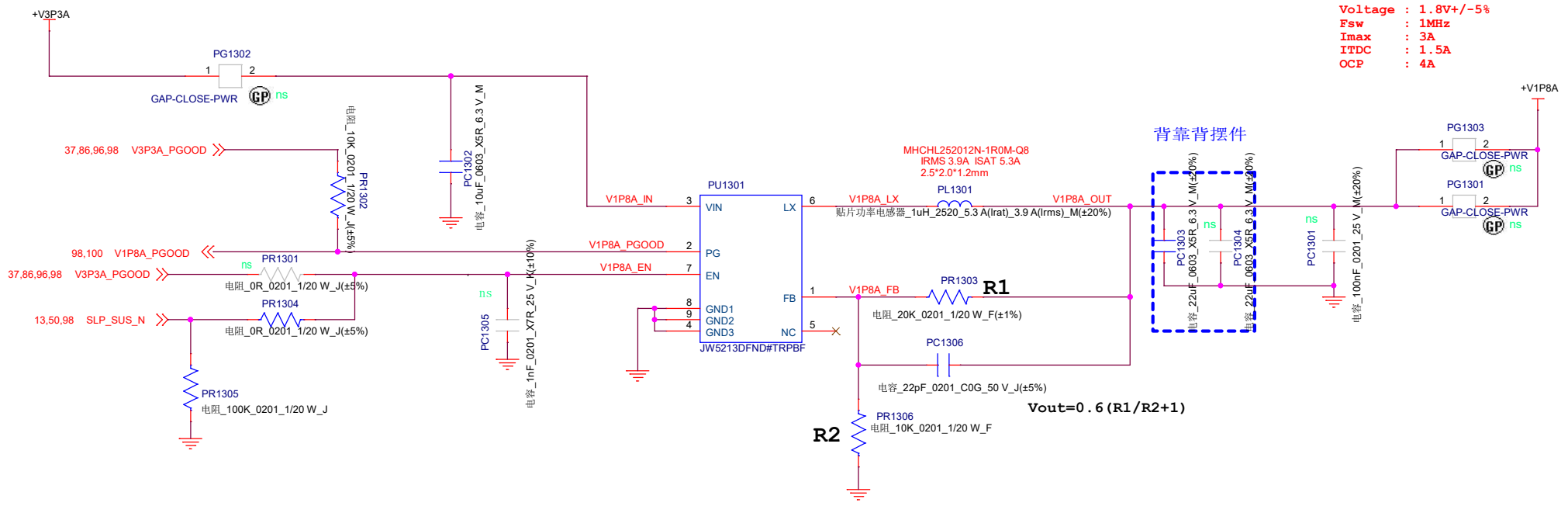


Voltage : 3.3V±5%  
Fsw : 600KHz  
Imax : 6A  
ITDC : TBD

MHCI06030-1R0M-R8A  
ISAT=15A, IRMS=12A  
7.3\*6.8\*3.0mm  
RDC=7.4mohm




V3P3A\_PGOOD 37,86,96,98  
V1P8A\_PGOOD 98,100  
V3P3A\_PGOOD 37,86,96,98  
SLP\_SUS\_N 13,50,98

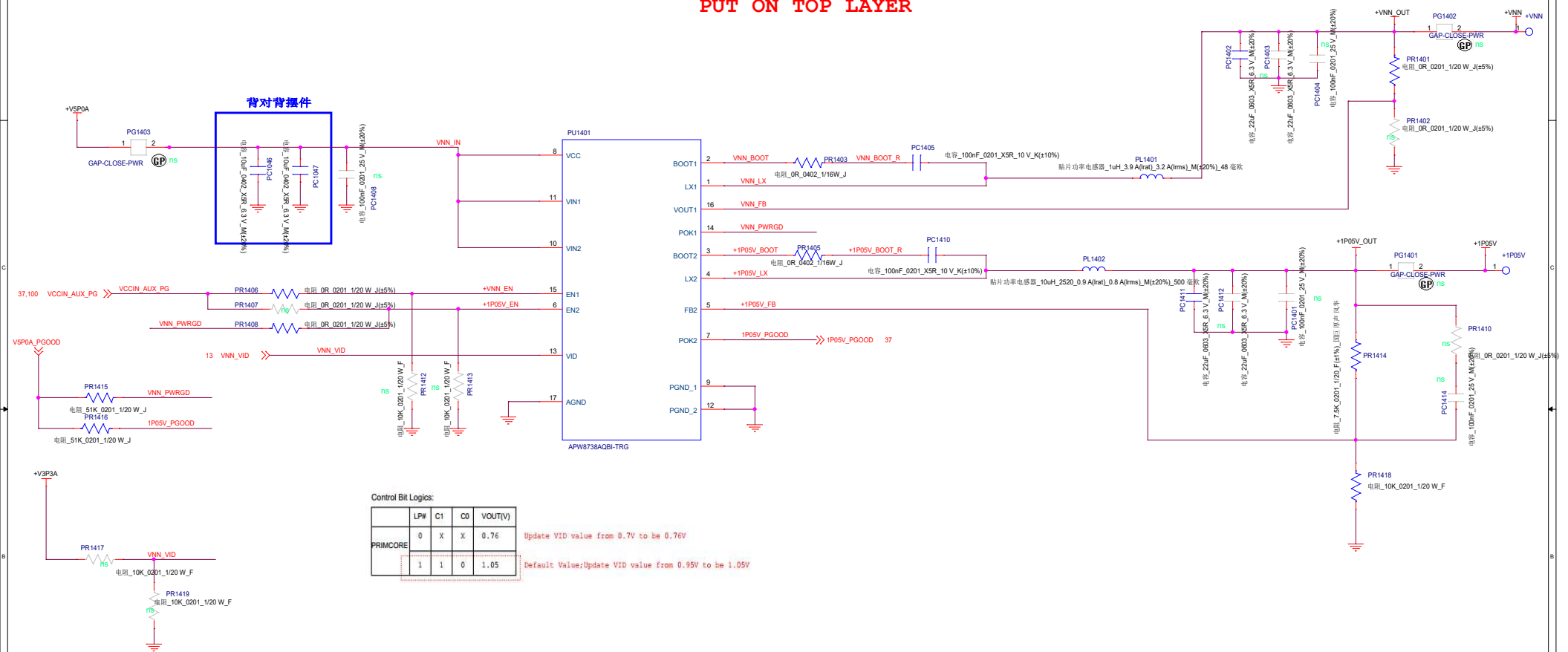


Voltage : 1.8V+/-5%  
Fsw : 1MHz  
Imax : 3A  
ITDC : 1.5A  
OCP : 4A

$V_{out}=0.6(R1/R2+1)$

 HUAQIN 华勤通讯		Huaqin Telecom Technology Com.,Ltd.	
Page name: <b>POWER DELIVERY V1P8A</b>			
Size: A4	Project Name: NB2950-JSL	REV: V1.0	
Date: Monday, September 28, 2020	Sheet: 98 of 110		

PUT ON TOP LAYER

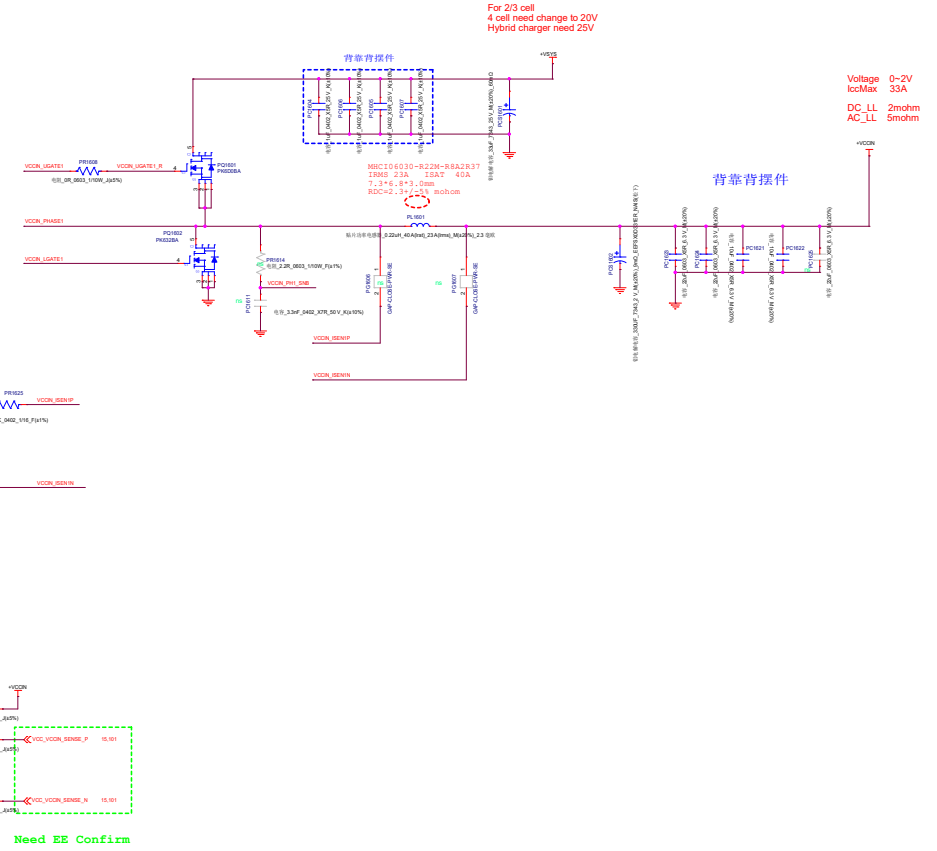
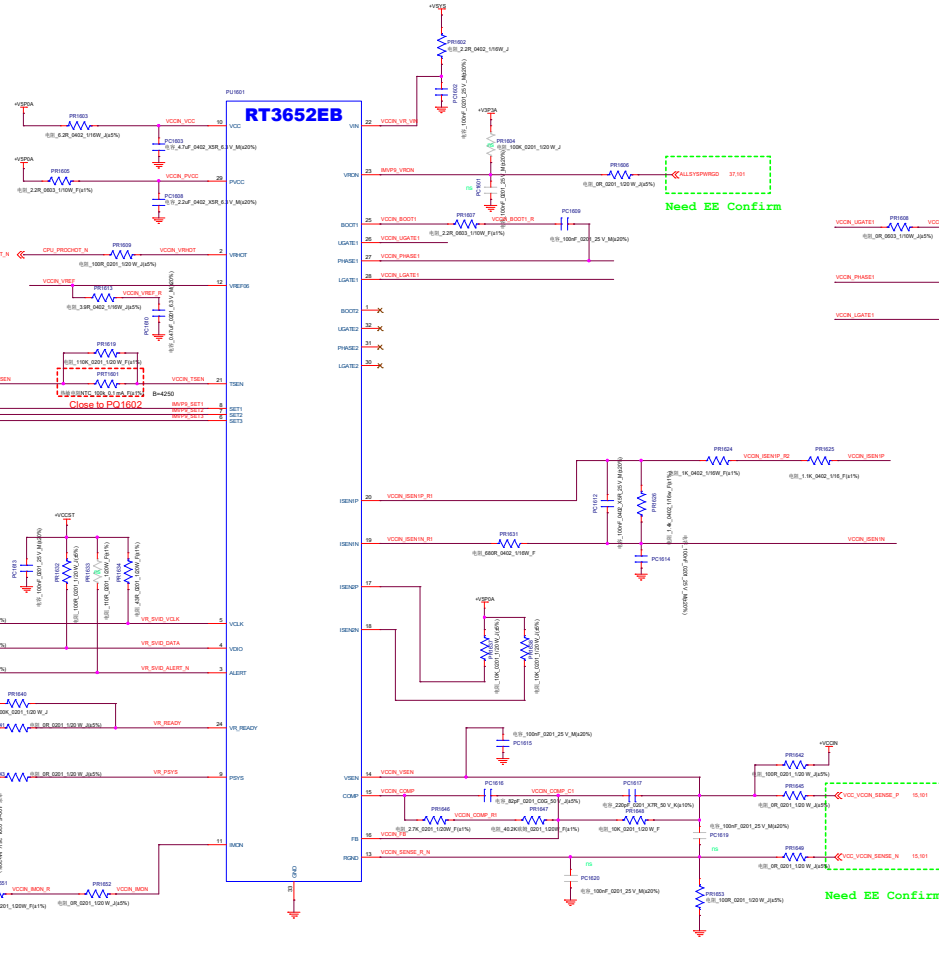




ALLSYSWROD 37.01  
 CPU\_PWDEN1\_N 0.1137.001  
 VCON\_VCONN 0.101  
 VCON\_VCONP 0.101  
 VCON\_VCONN\_N 0.101  
 VCON\_VCONN\_P 0.101  
 VCON\_VCONN\_N 0.101  
 VCON\_VCONN\_P 0.101  
 VCON\_VCONN\_N 0.101  
 VCON\_VCONN\_P 0.101

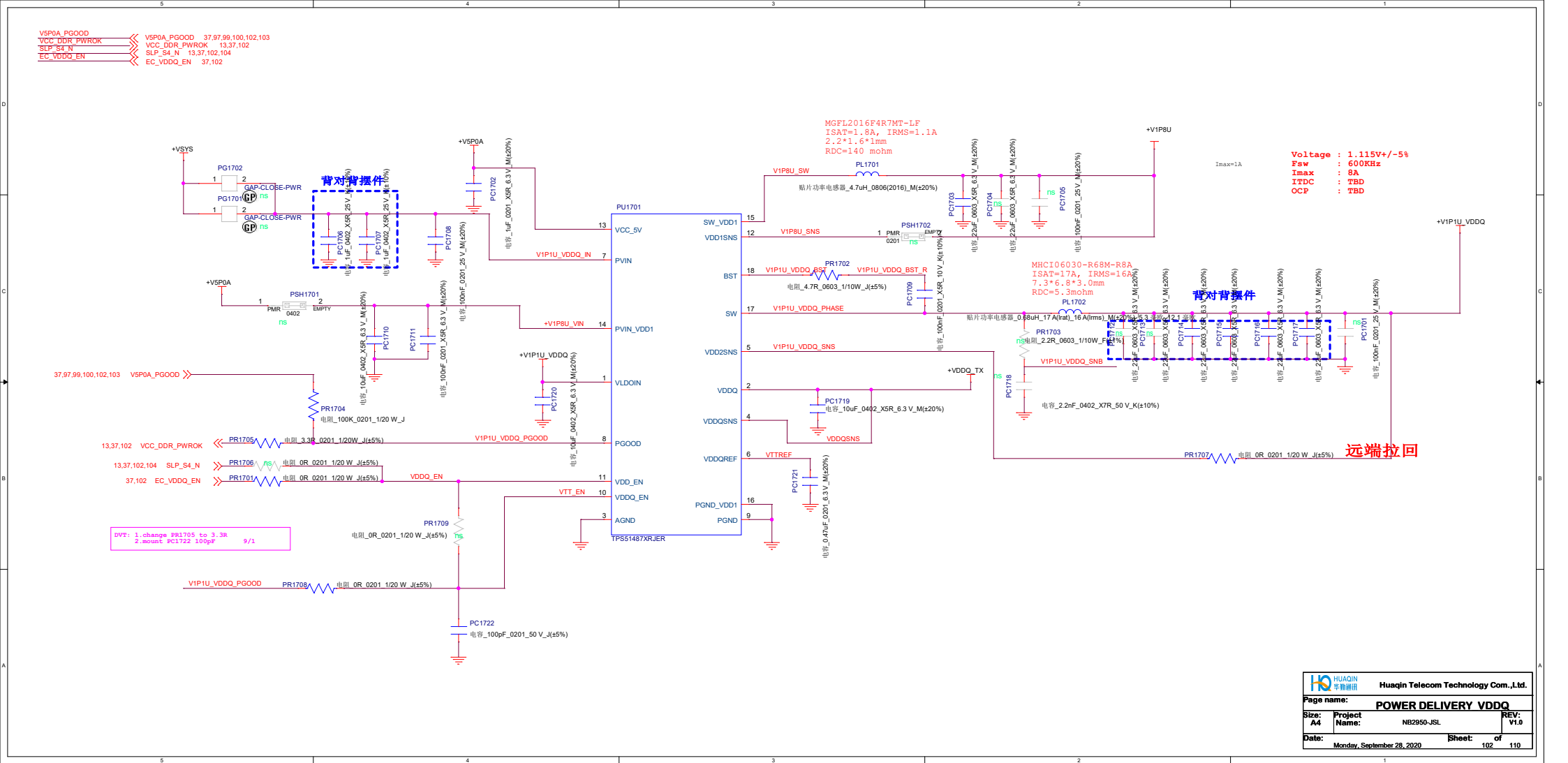
Number of Gaps Depend on Battery cells and placement

PIN SETTING	FUNCTION1	FUNCTION2	FUNCTION3
SET1	EN_LV_HIGH	VBOOT	ICCMAX
SET2	1.6-2.2V	1.8V	80A
SET3	AKTIVOS_TH	AI_GAIN	NA
SET4	0.5V	0.25	NA
SET5	OR_TN_DISABLE	NA	NA
SET6	0.1V	NA	NA
SET7	DISABLE	NA	NA
SET8	DISABLE	NA	NA
SET9	DISABLE	NA	NA
SET10	DISABLE	NA	NA
SET11	DISABLE	NA	NA
SET12	DISABLE	NA	NA
SET13	DISABLE	NA	NA
SET14	DISABLE	NA	NA
SET15	DISABLE	NA	NA
SET16	DISABLE	NA	NA
SET17	DISABLE	NA	NA
SET18	DISABLE	NA	NA
SET19	DISABLE	NA	NA
SET20	DISABLE	NA	NA
SET21	DISABLE	NA	NA
SET22	DISABLE	NA	NA
SET23	DISABLE	NA	NA
SET24	DISABLE	NA	NA
SET25	DISABLE	NA	NA
SET26	DISABLE	NA	NA
SET27	DISABLE	NA	NA
SET28	DISABLE	NA	NA
SET29	DISABLE	NA	NA
SET30	DISABLE	NA	NA
SET31	DISABLE	NA	NA
SET32	DISABLE	NA	NA
SET33	DISABLE	NA	NA
SET34	DISABLE	NA	NA
SET35	DISABLE	NA	NA
SET36	DISABLE	NA	NA
SET37	DISABLE	NA	NA
SET38	DISABLE	NA	NA
SET39	DISABLE	NA	NA
SET40	DISABLE	NA	NA
SET41	DISABLE	NA	NA
SET42	DISABLE	NA	NA
SET43	DISABLE	NA	NA
SET44	DISABLE	NA	NA
SET45	DISABLE	NA	NA
SET46	DISABLE	NA	NA
SET47	DISABLE	NA	NA
SET48	DISABLE	NA	NA
SET49	DISABLE	NA	NA
SET50	DISABLE	NA	NA
SET51	DISABLE	NA	NA
SET52	DISABLE	NA	NA
SET53	DISABLE	NA	NA
SET54	DISABLE	NA	NA
SET55	DISABLE	NA	NA
SET56	DISABLE	NA	NA
SET57	DISABLE	NA	NA
SET58	DISABLE	NA	NA
SET59	DISABLE	NA	NA
SET60	DISABLE	NA	NA
SET61	DISABLE	NA	NA
SET62	DISABLE	NA	NA
SET63	DISABLE	NA	NA
SET64	DISABLE	NA	NA
SET65	DISABLE	NA	NA
SET66	DISABLE	NA	NA
SET67	DISABLE	NA	NA
SET68	DISABLE	NA	NA
SET69	DISABLE	NA	NA
SET70	DISABLE	NA	NA
SET71	DISABLE	NA	NA
SET72	DISABLE	NA	NA
SET73	DISABLE	NA	NA
SET74	DISABLE	NA	NA
SET75	DISABLE	NA	NA
SET76	DISABLE	NA	NA
SET77	DISABLE	NA	NA
SET78	DISABLE	NA	NA
SET79	DISABLE	NA	NA
SET80	DISABLE	NA	NA
SET81	DISABLE	NA	NA
SET82	DISABLE	NA	NA
SET83	DISABLE	NA	NA
SET84	DISABLE	NA	NA
SET85	DISABLE	NA	NA
SET86	DISABLE	NA	NA
SET87	DISABLE	NA	NA
SET88	DISABLE	NA	NA
SET89	DISABLE	NA	NA
SET90	DISABLE	NA	NA
SET91	DISABLE	NA	NA
SET92	DISABLE	NA	NA
SET93	DISABLE	NA	NA
SET94	DISABLE	NA	NA
SET95	DISABLE	NA	NA
SET96	DISABLE	NA	NA
SET97	DISABLE	NA	NA
SET98	DISABLE	NA	NA
SET99	DISABLE	NA	NA
SET100	DISABLE	NA	NA

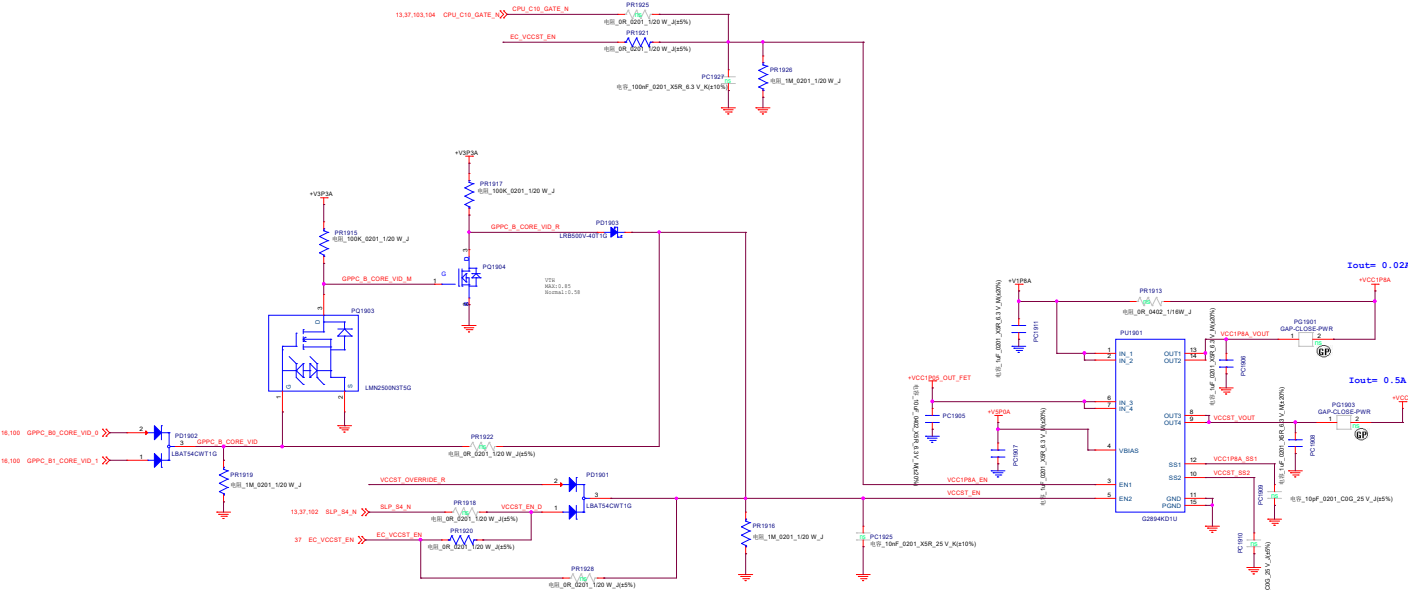
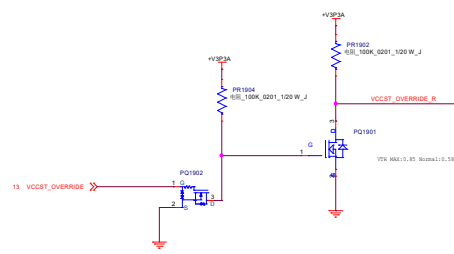
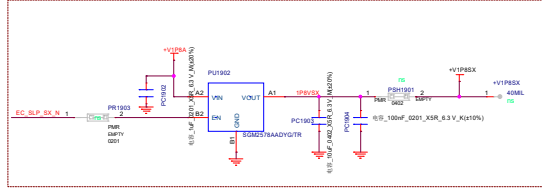


For 2/3 cell  
4 cell need change to 20V  
Hybrid charger need 25V

Voltage 0~2V  
I<sub>OL</sub>Max 33A  
DC\_LL 2mohm  
AC\_LL 5mohm





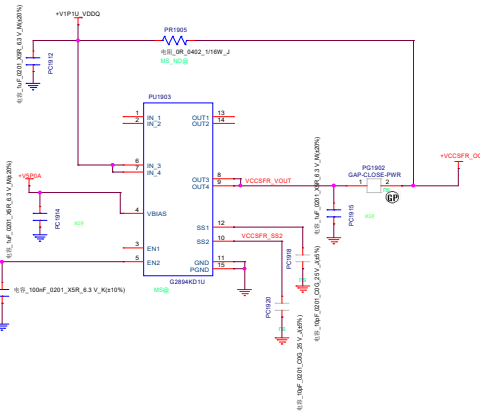
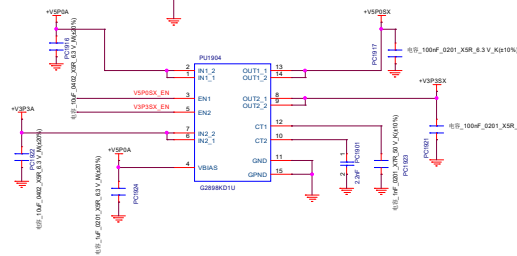


**+VCC1P8A**

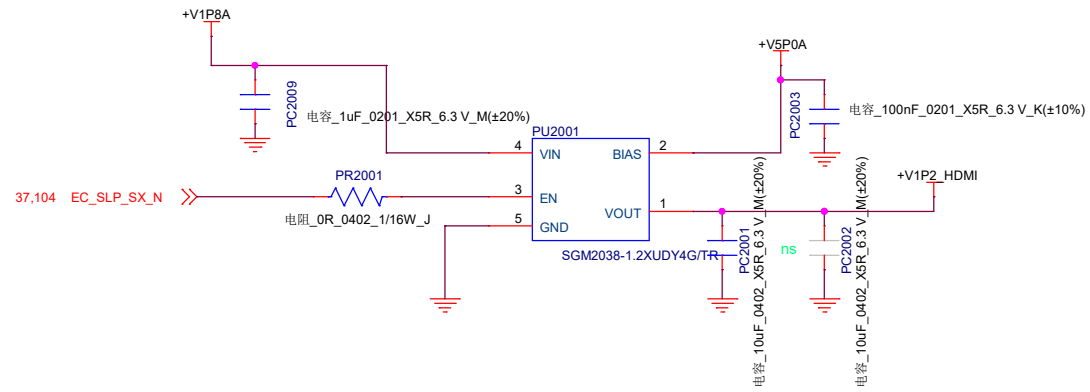
**+VCCST**



**+V3P3SX, +V5P0SX G2898**



**+VCCSFR\_OC**











5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1