

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

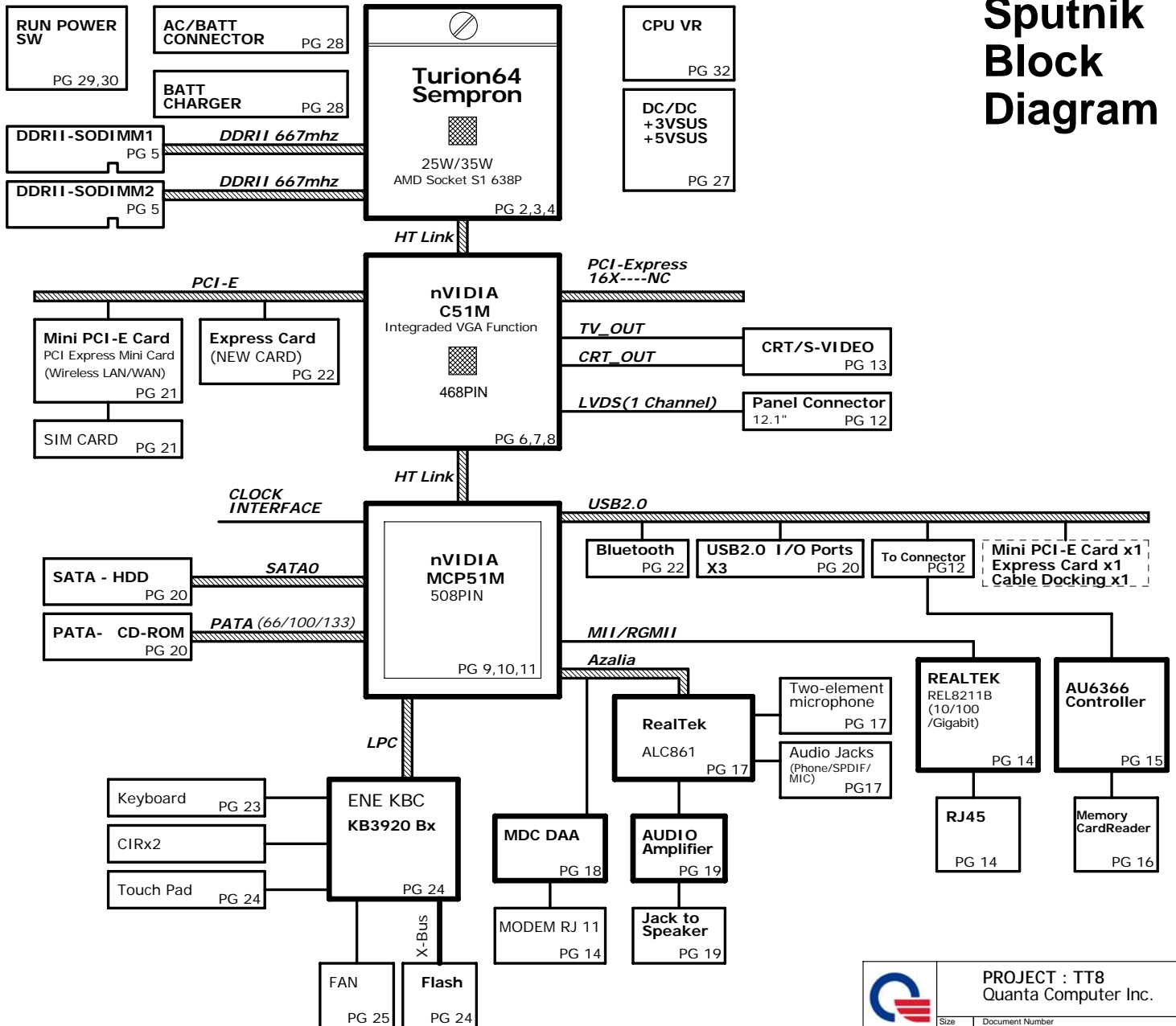
PG 25

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)



Sputnik Block Diagram



Size
Custom

PROJECT : TT8
Quanta Computer Inc.

Document Number
Block Diagram
Date: Friday, November 24, 2006
Sheet 1 of 36
Rev 1A

U21B

M A DQ63 AA12	MA_DATA[63]	MA_DM[7]
M A DQ62 AB12	MA_DATA[62]	MA_DM[6]
M A DQ61 AA14	MA_DATA[61]	MA_DM[5]
M A DQ60 AB14	MA_DATA[60]	MA_DM[4]
M A DQ59 W11	MA_DATA[59]	MA_DM[3]
M A DQ58 Y12	MA_DATA[58]	MA_DM[2]
M A DQ57 AD13	MA_DATA[57]	MA_DM[1]
M A DQ56 AB13	MA_DATA[56]	MA_DM[0]
M A DQ55 AD15	MA_DATA[55]	
M A DQ54 AB15	MA_DATA[54]	
M A DQ53 Y17	MA_DATA[53]	
M A DQ52 Y14	MA_DATA[52]	
M A DQ51 W14	MA_DATA[51]	
M A DQ50 W16	MA_DATA[50]	
M A DQ49 W16	MA_DATA[49]	
M A DQ48 AD17	MA_DATA[48]	
M A DQ47 Y18	MA_DATA[47]	
M A DQ46 AD19	MA_DATA[46]	
M A DQ45 AD21	MA_DATA[45]	
M A DQ44 AB21	MA_DATA[44]	
M A DQ43 AB18	MA_DATA[43]	
M A DQ42 AA18	MA_DATA[42]	
M A DQ41 AA20	MA_DATA[41]	
M A DQ40 Y20	MA_DATA[40]	
M A DQ38 Y22	MA_DATA[39]	
M A DQ37 W21	MA_DATA[38]	
M A DQ36 W22	MA_DATA[37]	
M A DQ35 AA21	MA_DATA[36]	
M A DQ34 AB22	MA_DATA[35]	
M A DQ33 AB24	MA_DATA[34]	
M A DQ32 Y24	MA_DATA[33]	
M A DQ31 H22	MA_DATA[32]	
M A DQ30 H20	MA_DATA[31]	
M A DQ29 E22	MA_DATA[30]	
M A DQ28 E21	MA_DATA[29]	
M A DQ27 H19	MA_DATA[28]	
M A DQ26 H24	MA_DATA[27]	
M A DQ25 F22	MA_DATA[26]	
M A DQ24 F20	MA_DATA[25]	
M A DQ23 C23	MA_DATA[24]	
M A DQ22 B22	MA_DATA[23]	
M A DQ21 E18	MA_DATA[22]	
M A DQ20 E18	MA_DATA[21]	
M A DQ19 E20	MA_DATA[20]	
M A DQ18 D22	MA_DATA[19]	
M A DQ17 C19	MA_DATA[18]	
M A DQ16 G18	MA_DATA[17]	
M A DQ15 G17	MA_DATA[16]	
M A DQ14 F14	MA_DATA[15]	
M A DQ13 F14	MA_DATA[14]	
M A DQ12 E14	MA_DATA[13]	
M A DQ11 H17	MA_DATA[12]	
M A DQ10 H17	MA_DATA[11]	
M A DQ9 E15	MA_DATA[10]	
M A DQ8 H15	MA_DATA[9]	
M A DQ7 E13	MA_DATA[8]	
M A DQ6 C13	MA_DATA[7]	
M A DQ5 H12	MA_DATA[6]	
M A DQ4 H11	MA_DATA[5]	
M A DQ3 G14	MA_DATA[4]	
M A DQ2 H14	MA_DATA[3]	
M A DQ1 F12	MA_DATA[2]	
M A DQ0 G12	MA_DATA[1]	
M A ADD15	MA_ADD[15]	
M A ADD14	MA_ADD[14]	
M A ADD13	MA_ADD[13]	
M A ADD12	MA_ADD[12]	
M A ADD11	MA_ADD[11]	
M A ADD10	MA_ADD[10]	
M A ADD9	MA_ADD[9]	
M A ADD8	MA_ADD[8]	
M A ADD7	MA_ADD[7]	
M A ADD6	MA_ADD[6]	
M A ADD5	MA_ADD[5]	
M A ADD4	MA_ADD[4]	
M A ADD3	MA_ADD[3]	
M A ADD2	MA_ADD[2]	
M A ADD1	MA_ADD[1]	
M A ADD0	MA_ADD[0]	

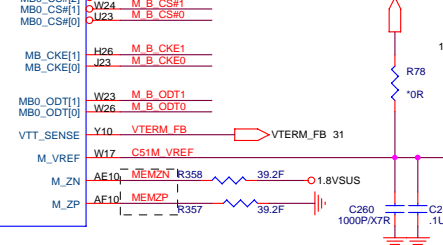
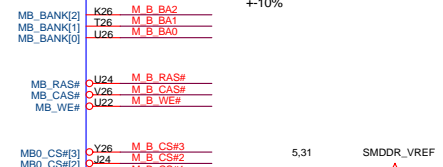
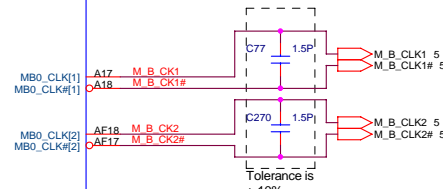
AMD S1 SOCKET

U21C

M B DQ63 AD11	MB_DATA[63]	MB_DM[7]
M B DQ62 AF11	MB_DATA[62]	MB_DM[6]
M B DQ61 AF14	MB_DATA[61]	MB_DM[5]
M B DQ60 AE14	MB_DATA[60]	MB_DM[4]
M B DQ59 Y11	MB_DATA[59]	MB_DM[3]
M B DQ58 AB11	MB_DATA[58]	MB_DM[2]
M B DQ57 AC12	MB_DATA[57]	MB_DM[1]
M B DQ56 AE13	MB_DATA[56]	MB_DM[0]
M B DQ55 AF16	MB_DATA[55]	
M B DQ54 AF16	MB_DATA[54]	
M B DQ53 AC18	MB_DATA[53]	
M B DQ52 AF19	MB_DATA[52]	
M B DQ51 AD14	MB_DATA[51]	
M B DQ50 AC14	MB_DATA[50]	
M B DQ49 AE18	MB_DATA[49]	
M B DQ48 AD18	MB_DATA[48]	
M B DQ47 AD20	MB_DATA[47]	
M B DQ46 AC20	MB_DATA[46]	
M B DQ45 AF23	MB_DATA[45]	
M B DQ44 AF24	MB_DATA[44]	
M B DQ43 AF20	MB_DATA[43]	
M B DQ42 AE20	MB_DATA[42]	
M B DQ41 AD22	MB_DATA[41]	
M B DQ40 AC22	MB_DATA[40]	
M B DQ39 AE25	MB_DATA[39]	
M B DQ38 AD26	MB_DATA[38]	
M B DQ37 AA25	MB_DATA[37]	
M B DQ36 AA26	MB_DATA[36]	
M B DQ35 AE24	MB_DATA[35]	
M B DQ34 AD24	MB_DATA[34]	
M B DQ33 AA23	MB_DATA[33]	
M B DQ32 AA24	MB_DATA[32]	
M B DQ31 G23	MB_DATA[31]	
M B DQ30 G23	MB_DATA[30]	
M B DQ29 D26	MB_DATA[29]	
M B DQ28 C26	MB_DATA[28]	
M B DQ27 G26	MB_DATA[27]	
M B DQ26 G25	MB_DATA[26]	
M B DQ25 E24	MB_DATA[25]	
M B DQ24 E23	MB_DATA[24]	
M B DQ23 C24	MB_DATA[23]	
M B DQ22 B24	MB_DATA[22]	
M B DQ21 C20	MB_DATA[21]	
M B DQ20 B00	MB_DATA[20]	
M B DQ19 C25	MB_DATA[19]	
M B DQ18 D24	MB_DATA[18]	
M B DQ17 A21	MB_DATA[17]	
M B DQ16 D20	MB_DATA[16]	
M B DQ15 D18	MB_DATA[15]	
M B DQ14 C18	MB_DATA[14]	
M B DQ13 D14	MB_DATA[13]	
M B DQ12 C14	MB_DATA[12]	
M B DQ11 A20	MB_DATA[11]	
M B DQ10 A16	MB_DATA[10]	
M B DQ9 A16	MB_DATA[9]	
M B DQ8 A15	MB_DATA[8]	
M B DQ7 A13	MB_DATA[7]	
M B DQ6 D12	MB_DATA[6]	
M B DQ5 E11	MB_DATA[5]	
M B DQ4 G11	MB_DATA[4]	
M B DQ3 B14	MB_DATA[3]	
M B DQ2 A14	MB_DATA[2]	
M B DQ1 A11	MB_DATA[1]	
M B DQ0 C11	MB_DATA[0]	
M B ADD15	MB_ADD[15]	
M B ADD14	MB_ADD[14]	
M B ADD13	MB_ADD[13]	
M B ADD12	MB_ADD[12]	
M B ADD11	MB_ADD[11]	
M B ADD10	MB_ADD[10]	
M B ADD9	MB_ADD[9]	
M B ADD8	MB_ADD[8]	
M B ADD7	MB_ADD[7]	
M B ADD6	MB_ADD[6]	
M B ADD5	MB_ADD[5]	
M B ADD4	MB_ADD[4]	
M B ADD3	MB_ADD[3]	
M B ADD2	MB_ADD[2]	
M B ADD1	MB_ADD[1]	
M B ADD0	MB_ADD[0]	

AMD S1 SOCKET

TRACE FROM CAP TO CPU MUST BE LESS
THAN 1200MILS MAX NECKDOWN TO &
FROM CAPS IS 500MILS



C51MVREF : W = 20MIL AND SPACE = 20MIL

5 M_A_DQ[63..0]	M A DQ[63..0]	M A DQ[63..0]
4.5 M_A_A[15..0]	M A A[15..0]	M A A[15..0]
M A DQ[63..0]	M A DQ[63..0]	M A DQ[63..0]
M A DQ[62..0]	M A DQ[62..0]	M A DQ[62..0]
M A DQ[61..0]	M A DQ[61..0]	M A DQ[61..0]
M A DQ[60..0]	M A DQ[60..0]	M A DQ[60..0]
M A DQ[59..0]	M A DQ[59..0]	M A DQ[59..0]
M A DQ[58..0]	M A DQ[58..0]	M A DQ[58..0]
M A DQ[57..0]	M A DQ[57..0]	M A DQ[57..0]
M A DQ[56..0]	M A DQ[56..0]	M A DQ[56..0]
M A DQ[55..0]	M A DQ[55..0]	M A DQ[55..0]
M A DQ[54..0]	M A DQ[54..0]	M A DQ[54..0]
M A DQ[53..0]	M A DQ[53..0]	M A DQ[53..0]
M A DQ[52..0]	M A DQ[52..0]	M A DQ[52..0]
M A DQ[51..0]	M A DQ[51..0]	M A DQ[51..0]
M A DQ[50..0]	M A DQ[50..0]	M A DQ[50..0]
M A DQ[49..0]	M A DQ[49..0]	M A DQ[49..0]
M A DQ[48..0]	M A DQ[48..0]	M A DQ[48..0]
M A DQ[47..0]	M A DQ[47..0]	M A DQ[47..0]
M A DQ[46..0]	M A DQ[46..0]	M A DQ[46..0]
M A DQ[45..0]	M A DQ[45..0]	M A DQ[45..0]
M A DQ[44..0]	M A DQ[44..0]	M A DQ[44..0]
M A DQ[43..0]	M A DQ[43..0]	M A DQ[43..0]
M A DQ[42..0]	M A DQ[42..0]	M A DQ[42..0]
M A DQ[41..0]	M A DQ[41..0]	M A DQ[41..0]
M A DQ[40..0]	M A DQ[40..0]	M A DQ[40..0]
M A DQ[39..0]	M A DQ[39..0]	M A DQ[39..0]
M A DQ[38..0]	M A DQ[38..0]	M A DQ[38..0]
M A DQ[37..0]	M A DQ[37..0]	M A DQ[37..0]
M A DQ[36..0]	M A DQ[36..0]	M A DQ[36..0]
M A DQ[35..0]	M A DQ[35..0]	M A DQ[35..0]
M A DQ[34..0]	M A DQ[34..0]	M A DQ[34..0]
M A DQ[33..0]	M A DQ[33..0]	M A DQ[33..0]
M A DQ[32..0]	M A DQ[32..0]	M A DQ[32..0]
M A DQ[31..0]	M A DQ[31..0]	M A DQ[31..0]
M A DQ[30..0]	M A DQ[30..0]	M A DQ[30..0]
M A DQ[29..0]	M A DQ[29..0]	M A DQ[29..0]
M A DQ[28..0]	M A DQ[28..0]	M A DQ[28..0]
M A DQ[27..0]	M A DQ[27..0]	M A DQ[27..0]
M A DQ[26..0]	M A DQ[26..0]	M A DQ[26..0]
M A DQ[25..0]	M A DQ[25..0]	M A DQ[25..0]
M A DQ[24..0]	M A DQ[24..0]	M A DQ[24..0]
M A DQ[23..0]	M A DQ[23..0]	M A DQ[23..0]
M A DQ[22..0]	M A DQ[22..0]	M A DQ[22..0]
M A DQ[21..0]	M A DQ[21..0]	M A DQ[21..0]
M A DQ[20..0]	M A DQ[20..0]	M A DQ[20..0]
M A DQ[19..0]	M A DQ[19..0]	M A DQ[19..0]
M A DQ[18..0]	M A DQ[18..0]	M A DQ[18..0]
M A DQ[17..0]	M A DQ[17..0]	M A DQ[17..0]
M A DQ[16..0]	M A DQ[16..0]	M A DQ[16..0]
M A DQ[15..0]	M A DQ[15..0]	M A DQ[15..0]
M A DQ[14..0]	M A DQ[14..0]	M A DQ[14..0]
M A DQ[13..0]	M A DQ[13..0]	M A DQ[13..0]
M A DQ[12..0]	M A DQ[12..0]	M A DQ[12..0]
M A DQ[11..0]	M A DQ[11..0]	M A DQ[11..0]
M A DQ[10..0]	M A DQ[10..0]	M A DQ[10..0]
M A DQ[9..0]	M A DQ[9..0]	M A DQ[9..0]
M A DQ[8..0]	M A DQ[8..0]	M A DQ[8..0]
M A DQ[7..0]	M A DQ[7..0]	M A DQ[7..0]
M A DQ[6..0]	M A DQ[6..0]	M A DQ[6..0]
M A DQ[5..0]	M A DQ[5..0]	M A DQ[5..0]
M A DQ[4..0]	M A DQ[4..0]	M A DQ[4..0]
M A DQ[3..0]	M A DQ[3..0]	M A DQ[3..0]
M A DQ[2..0]	M A DQ[2..0]	M A DQ[2..0]
M A DQ[1..0]	M A DQ[1..0]	M A DQ[1..0]
M A DQ[0..0]	M A DQ[0..0]	M A DQ[0..0]

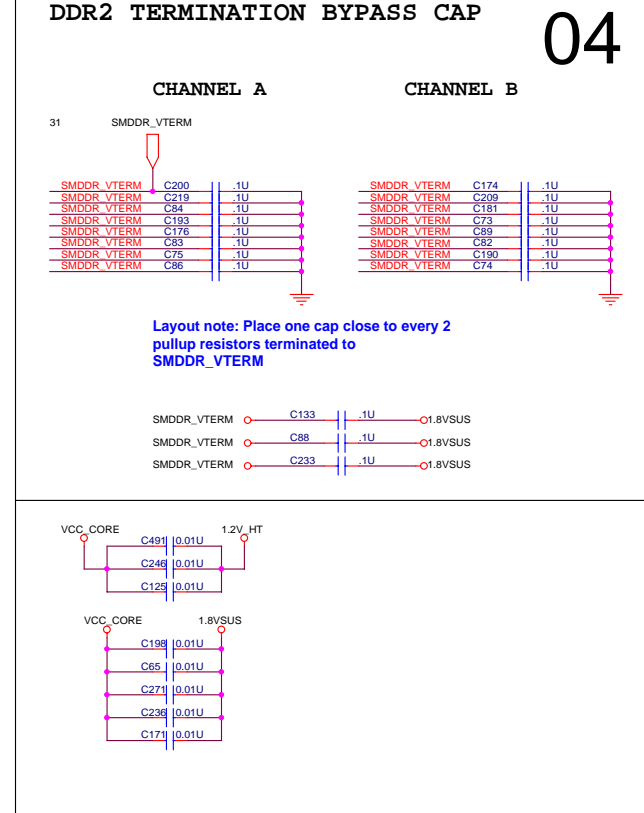
M B DQ[63..0]	M B DQ[63..0]	M B DQ[63..0]
M B DQ[62..0]	M B DQ[62..0]	M B DQ[62..0]
M B DQ[61..0]	M B DQ[61..0]	M B DQ[61..0]
M B DQ[60..0]	M B DQ[60..0]	M B DQ[60..0]
M B DQ[59..0]	M B DQ[59..0]	M B DQ[59..0]
M B DQ[58..0]	M B DQ[58..0]	M B DQ[58..0]
M B DQ[57..0]	M B DQ[57..0]	M B DQ[57..0]
M B DQ[56..0]	M B DQ[56..0]	M B DQ[56..0]
M B DQ[55..0]	M B DQ[55..0]	M B DQ[55..0]
M B DQ[54..0]	M B DQ[54..0]	M B DQ[54..0]
M B DQ[53..0]	M B DQ[53..0]	M B DQ[53..0]
M B DQ[52..0]	M B DQ[52..0]	M B DQ[52..0]
M B DQ[51..0]	M B DQ[51..0]	M B DQ[51..0]
M B DQ[50..0]	M B DQ[50..0]	M B DQ[50..0]
M B DQ[49..0]	M B DQ[49..0]	M B DQ[49..0]
M B DQ[48..0]	M B DQ[48..0]	M B DQ[48..0]
M B DQ[47..0]	M B DQ[47..0]	M B DQ[47..0]
M B DQ[46..0]	M B DQ[46..0]	M B DQ[46..0]
M B DQ[45..0]	M B DQ[45..0]	M B DQ[45..0]
M B DQ[44..0]	M B DQ[44..0]	M B DQ[44..0]
M B DQ[43..0]	M B DQ[43..0]	M B DQ[43..0]
M B DQ[42..0]	M B DQ[42..0]	M B DQ[42..0]
M B DQ[41..0]	M B DQ[41..0]	M B DQ[41..0]
M B DQ[40..0]	M B DQ[40..0]	M B DQ[40..0]
M B DQ[39..0]	M B DQ[39..0]	M B DQ[39..0]
M B DQ[38..0]	M B DQ[38..0]	M B DQ[38..0]
M B DQ[37..0]	M B DQ[37..0]	M B DQ[37..0]
M B DQ[36..0]	M B DQ[36..0]	M B DQ[36..0]
M B DQ[35..0]	M B DQ[35..0]	M B DQ[35..0]
M B DQ[34..0]	M B DQ[34..0]	M B DQ[34..0]
M B DQ[33..0]	M B DQ[33..0]	M B DQ[33..0]
M B DQ[32..0]	M B DQ[32..0]	M B DQ[32..0]
M B DQ[31..0]	M B DQ[31..0]	M B DQ[31..0]
M B DQ[30..0]	M B DQ[30..0]	M B DQ[30..0]
M B DQ[29..0]	M B DQ[29..0]	M B DQ[29..0]
M B DQ[28..0]	M B DQ[28..0]	M B DQ[28..0]
M B DQ[27..0]	M B DQ[27..0]	M B DQ[27..0]
M B DQ[26..0]	M B DQ[26..0]	M B DQ[26..0]
M B DQ[25..0]	M B DQ[25..0]	M B DQ[25..0]
M B DQ[24..0]	M B DQ[24..0]	M B DQ[24..0]
M B DQ[23..0]	M B DQ[23..0]	M B DQ[23..0]
M B DQ[22..0]	M B DQ[22..0]	M B DQ[22..0]
M B DQ[21..0]	M B DQ[21..0]	M B DQ[21..0]
M B DQ[20..0]	M B DQ[20..0]	M B DQ[20..0]
M B DQ[19..0]	M B DQ[19..0]	M B DQ[19..0]
M B DQ[18..0]	M B DQ[18..0]	M B DQ[18..0]
M B DQ[17..0]	M B DQ[17..0]	M B DQ[17..0]
M B DQ[16..0]	M B DQ[16..0]	M B DQ[16..0]
M B DQ[15..0]	M B DQ[15..0]	M B DQ[15..0]
M B DQ[14..0]	M B DQ[14..0]	M B DQ[14..0]
M B DQ[13..0]	M B DQ[13..0]	M B DQ[13..0]
M B DQ[12..0]	M B DQ[12..0]	M B DQ[12..0]
M B DQ[11..0]	M B DQ[11..0]	M B DQ[11..0]
M B DQ[10..0]	M B DQ[10..0]	M B DQ[10..0]
M B DQ[9..0]	M B DQ[9..0]	M B DQ[9..0]
M B DQ[8..0]	M B DQ[8..0]	M B DQ[8..0]
M B DQ[7..0]	M B DQ[7..0]	M B DQ[7..0]
M B DQ[6..0]	M B DQ[6..0]	M B DQ[6..0]
M B DQ[5..0]	M B DQ[5..0]	M B DQ[5..0]
M B DQ[4..0]	M B DQ[4..0]	M B DQ[4..0]
M B DQ[3..0]	M B DQ[3..0]	M B DQ[3..0]
M B DQ[2..0]	M B DQ[2..0]	M B DQ[2..0]
M B DQ[1..0]	M B DQ[1..0]	M B DQ[1..0]
M B DQ[0..0]	M B DQ[0..0]	M B DQ[0..0]



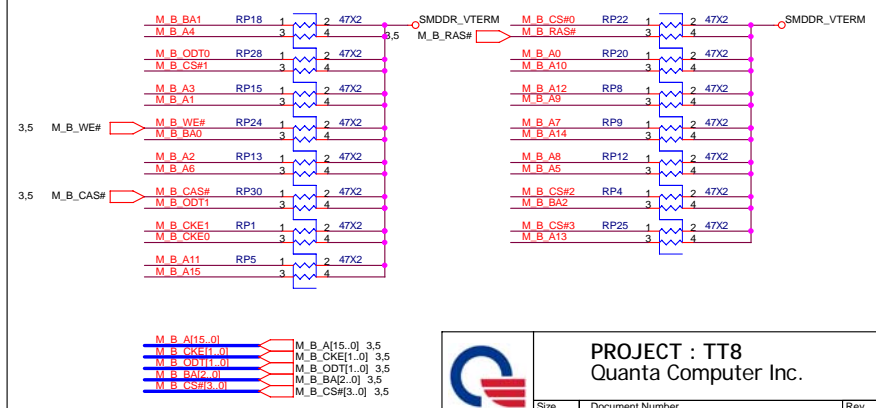
NBS/RD2/HW1

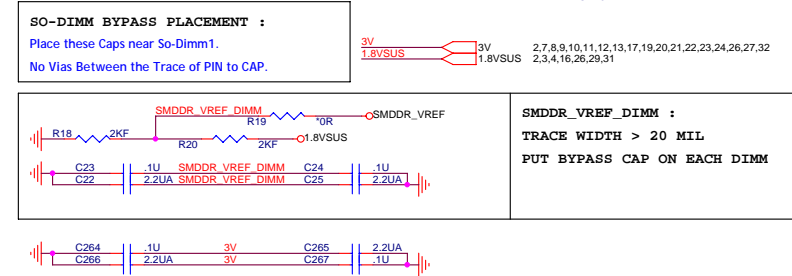
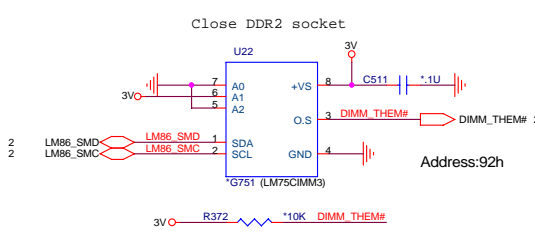
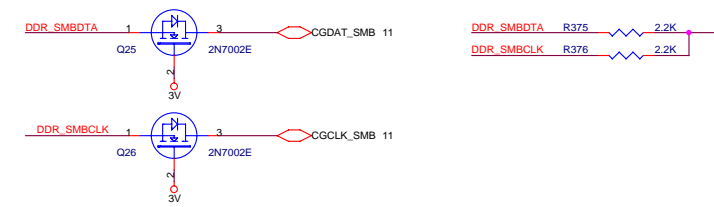
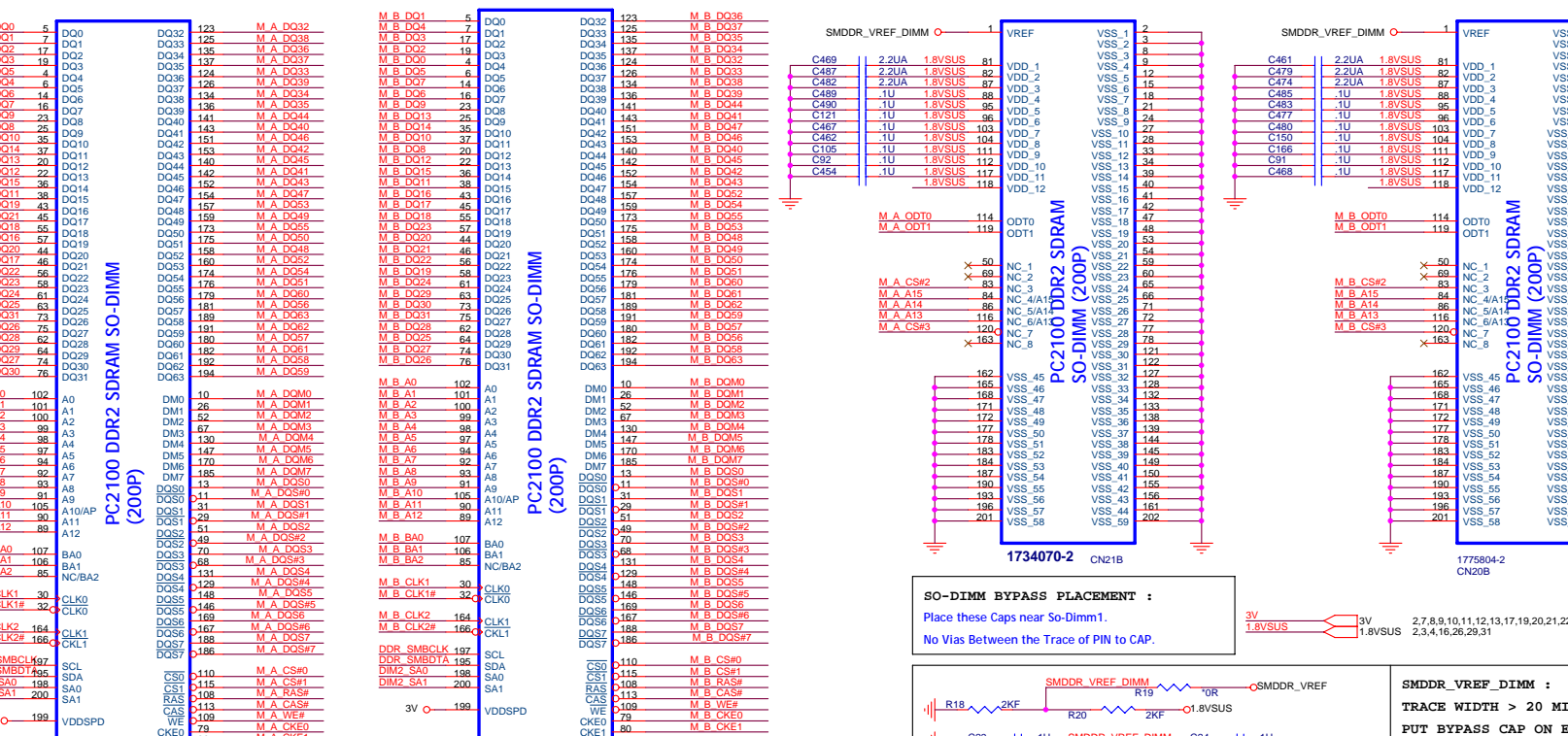
PROJECT : TT8
Quanta Computer Inc.

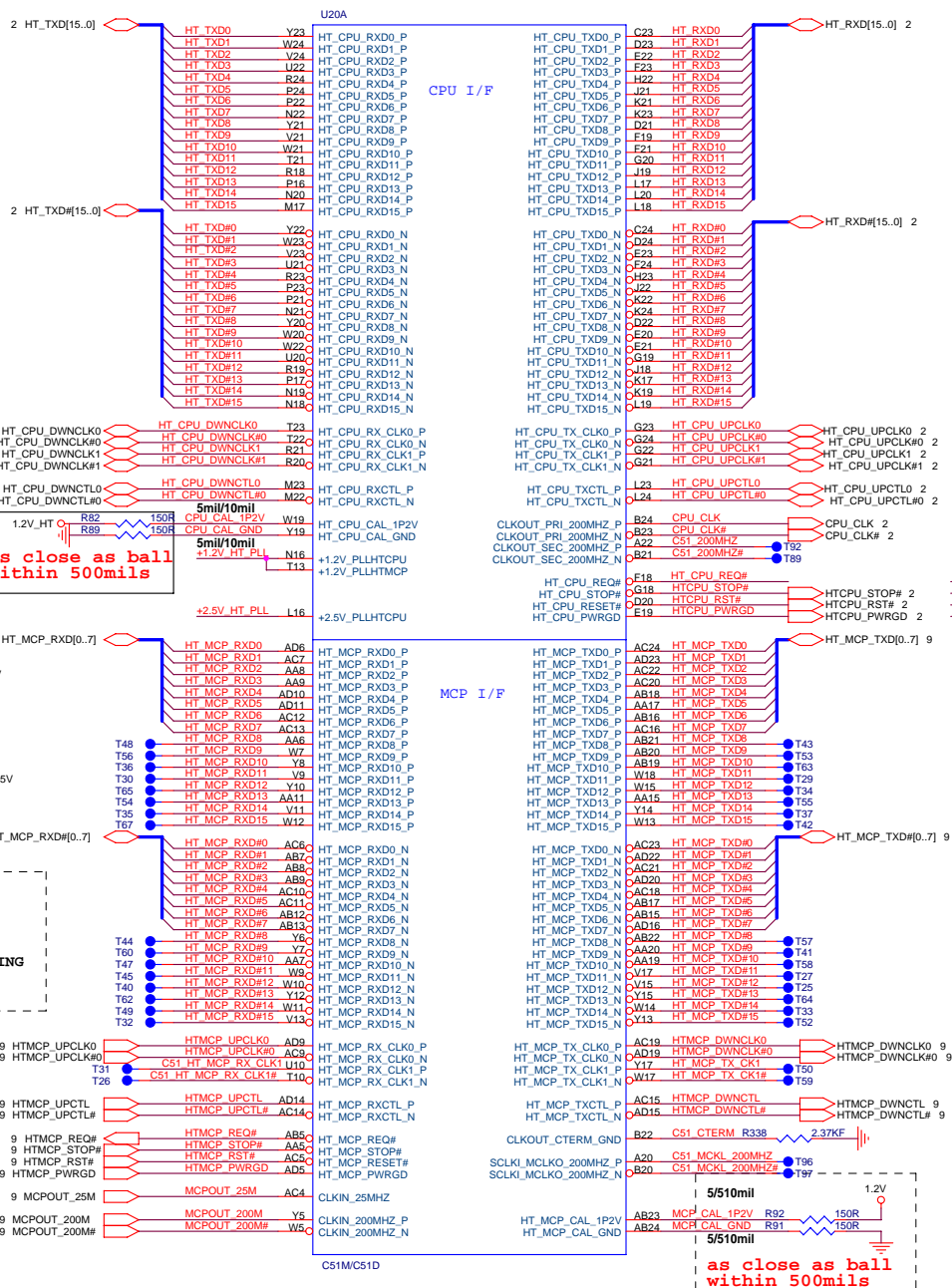
04

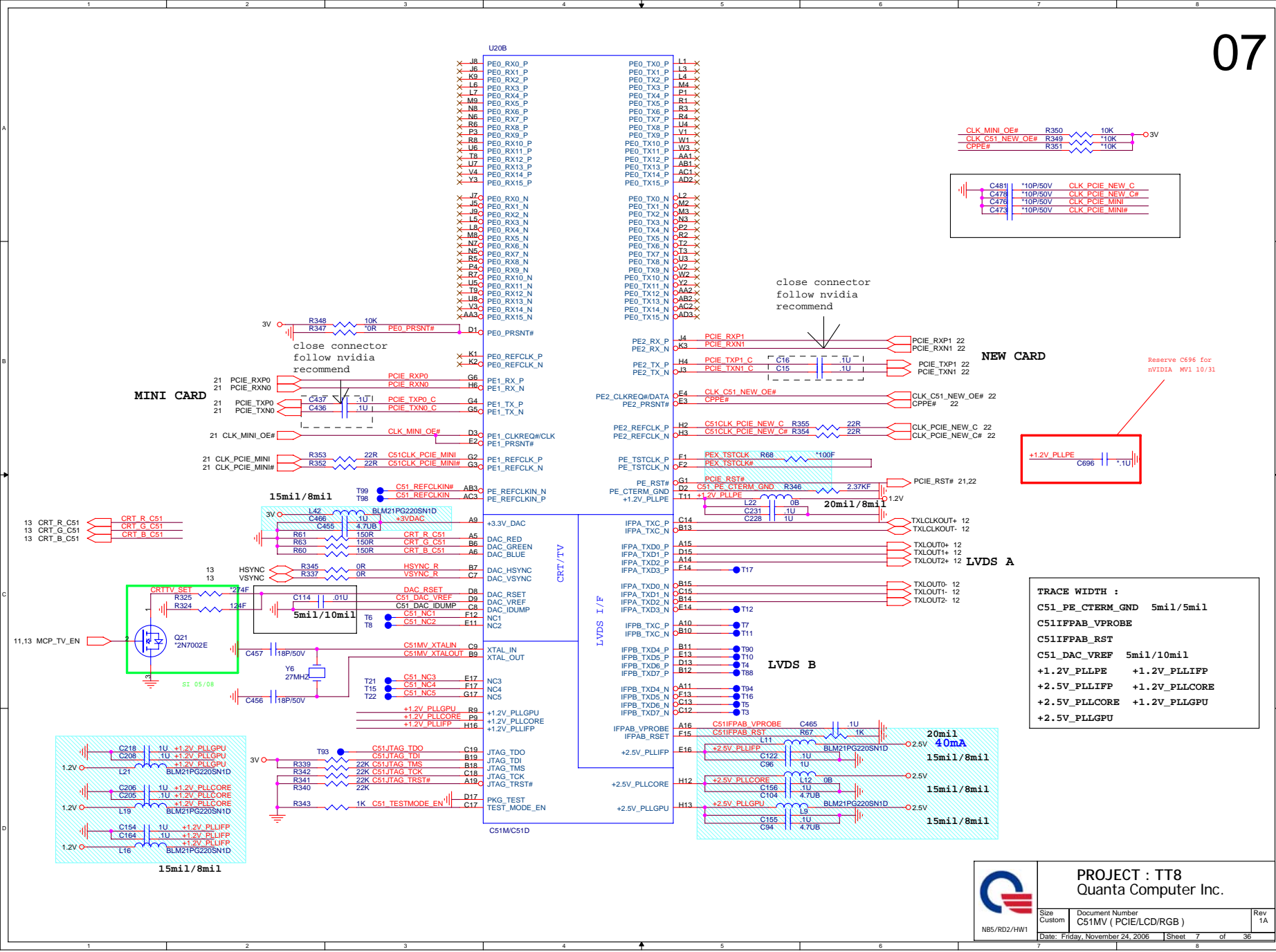


DDRII CHANNEL B TERMINATION

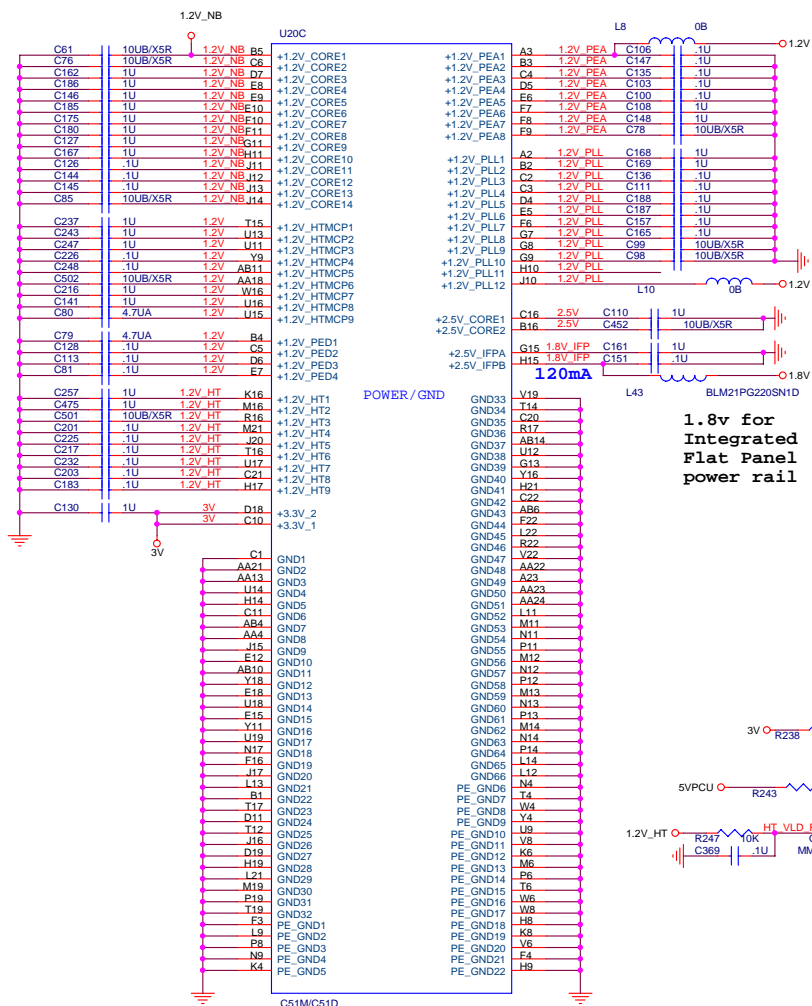
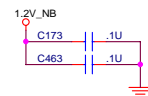


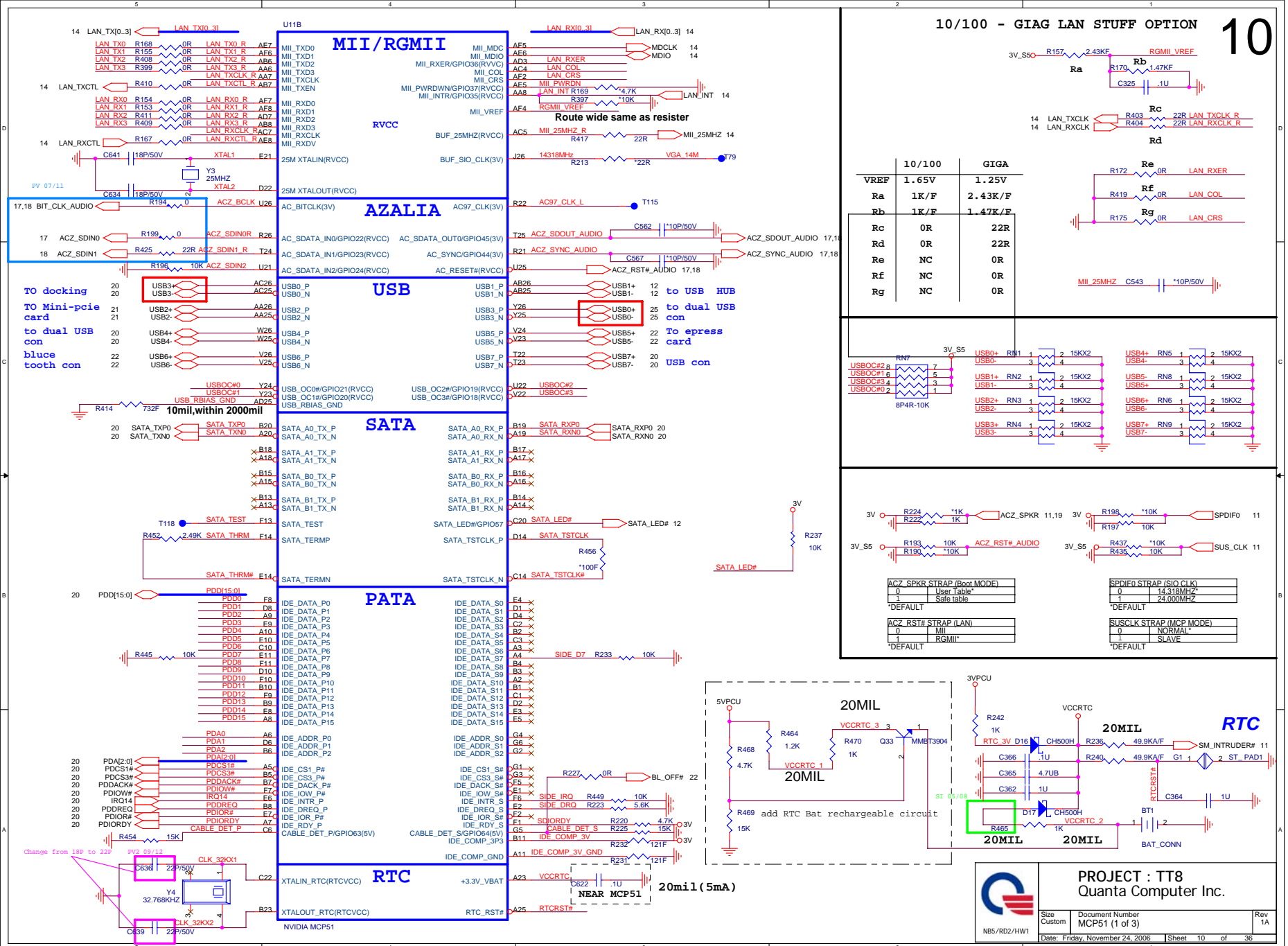


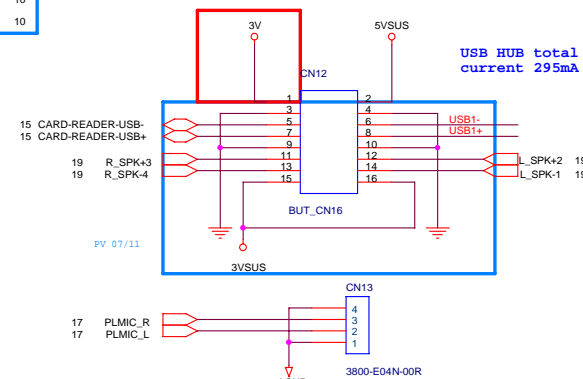
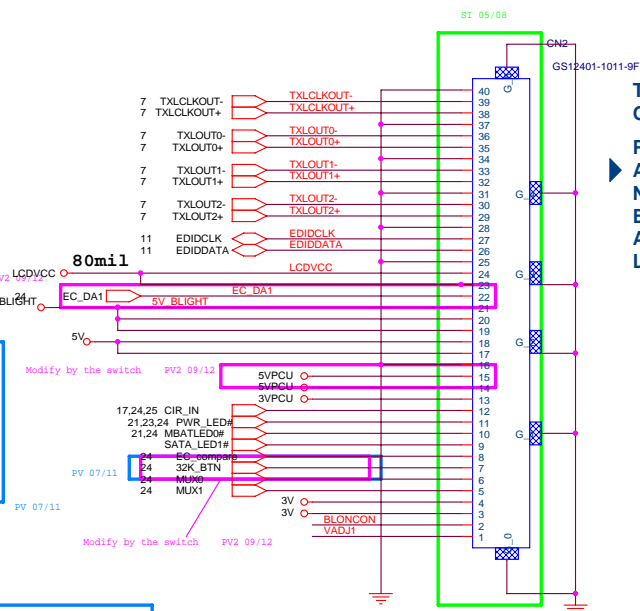
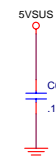
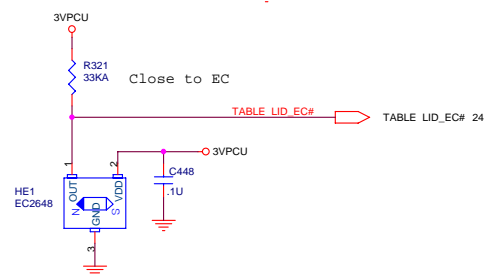
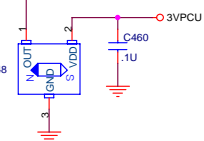
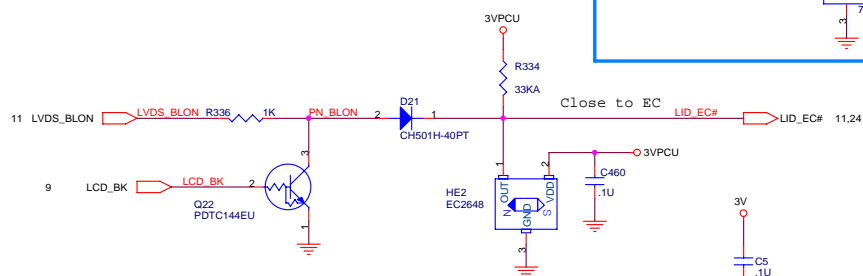
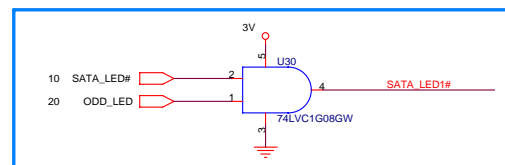
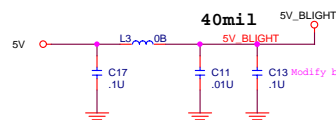
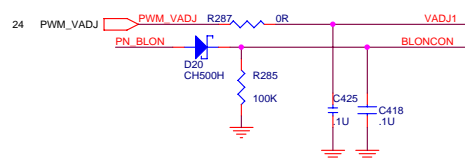
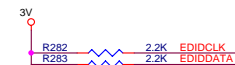
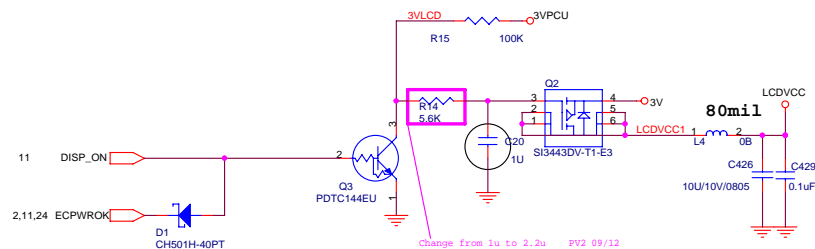




C51M POWER PLANE/GND & BYPASS





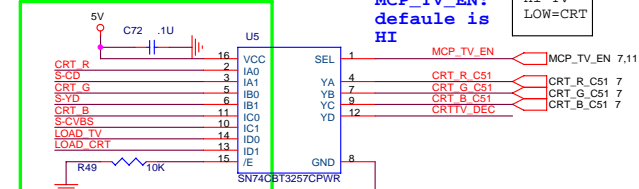


► **FRAMEWORK**

CRT/TV SWITCH

MCP_TV_EN:
default is
HI

HI=TV
LOW=CRT

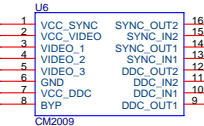


LOAD_CRT -- TV WORK
LOAD_TV -- CRT WORK

SI 05/08

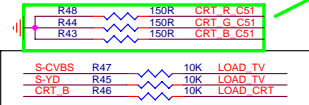
Change from nVIDIA for B-test

ESD PROTECTION



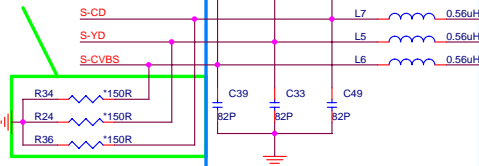
close within 600mils (
close data switch)

Change from nVIDIA for B-test



That is for CRT and TV choose..
used impedance and driver to
choose

Change from nVIDIA for B-test

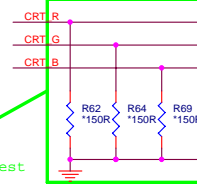


150-R as possible as
closed to Tv connector (close with
in 600 mil)

PV 07/11

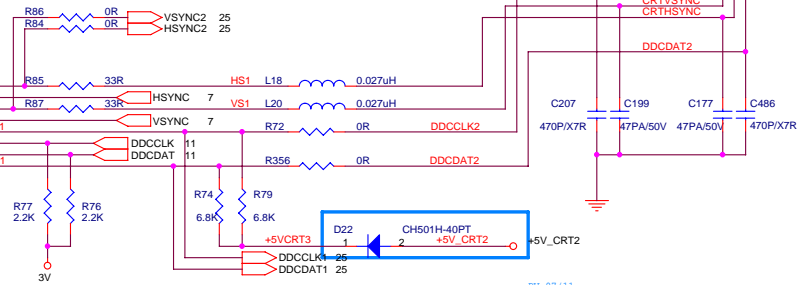
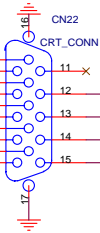


150-R as possible as
closed to CRT connector (
close with in 600 mil
)



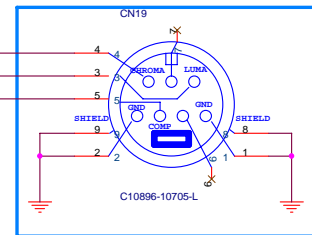
close conn within
600mils

CRT PORT



PV 07/11

TV_OUT



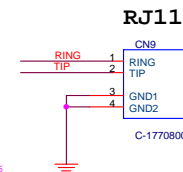
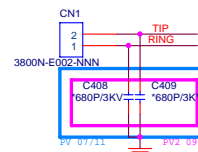
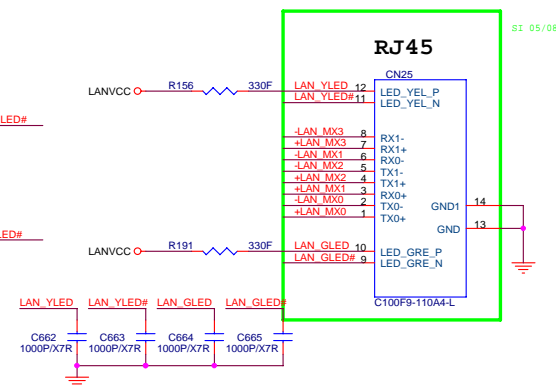
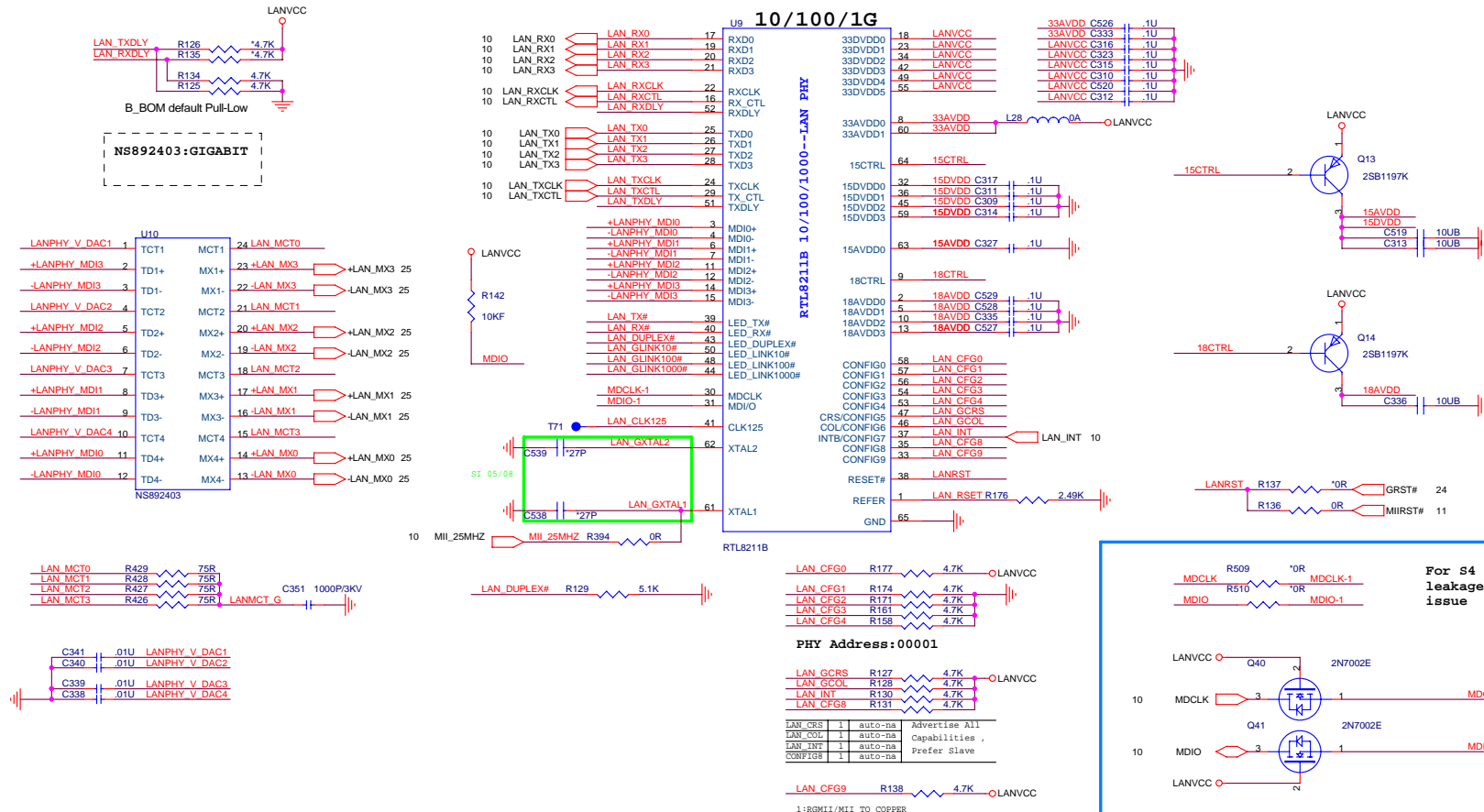
PV 07/11

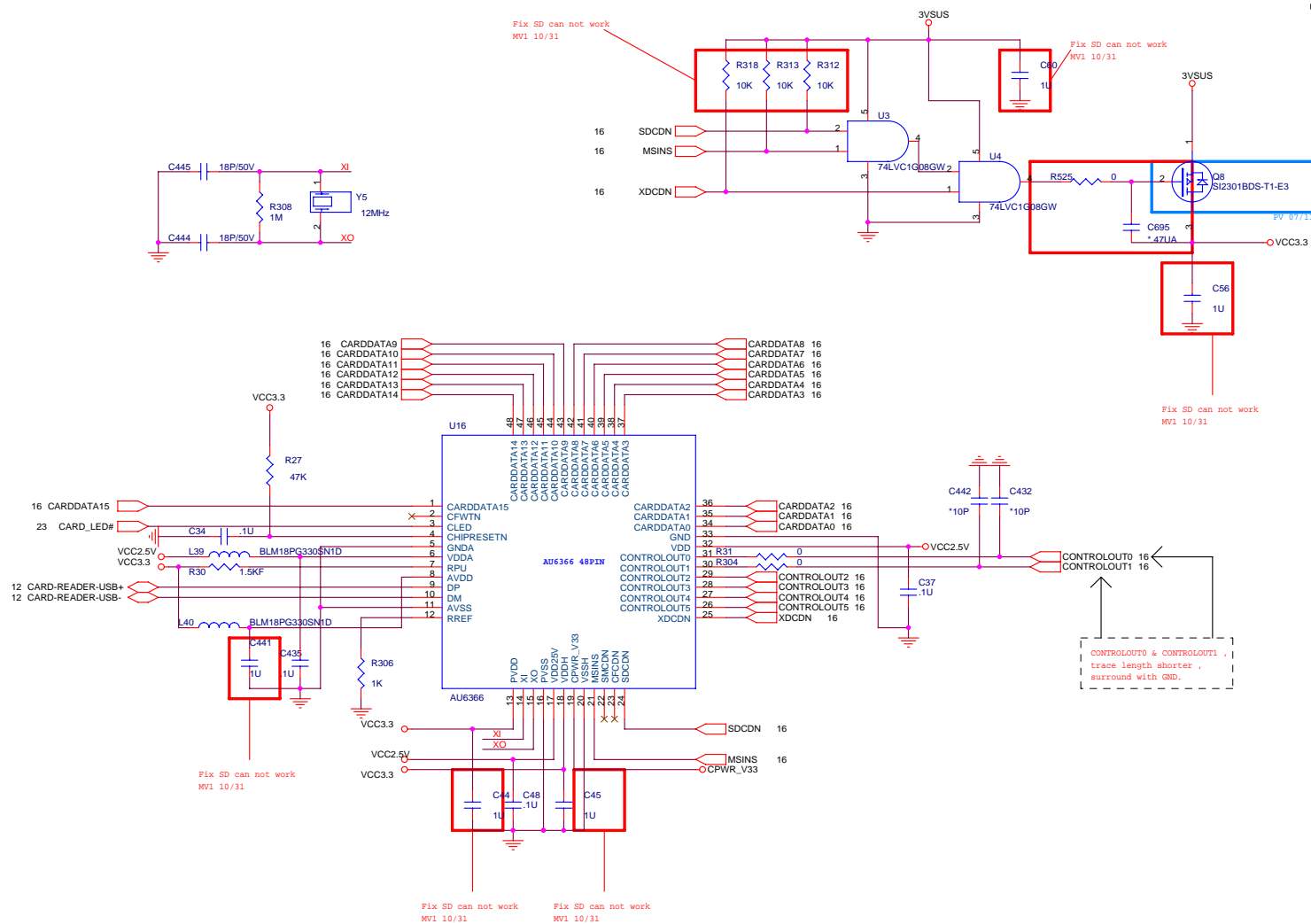


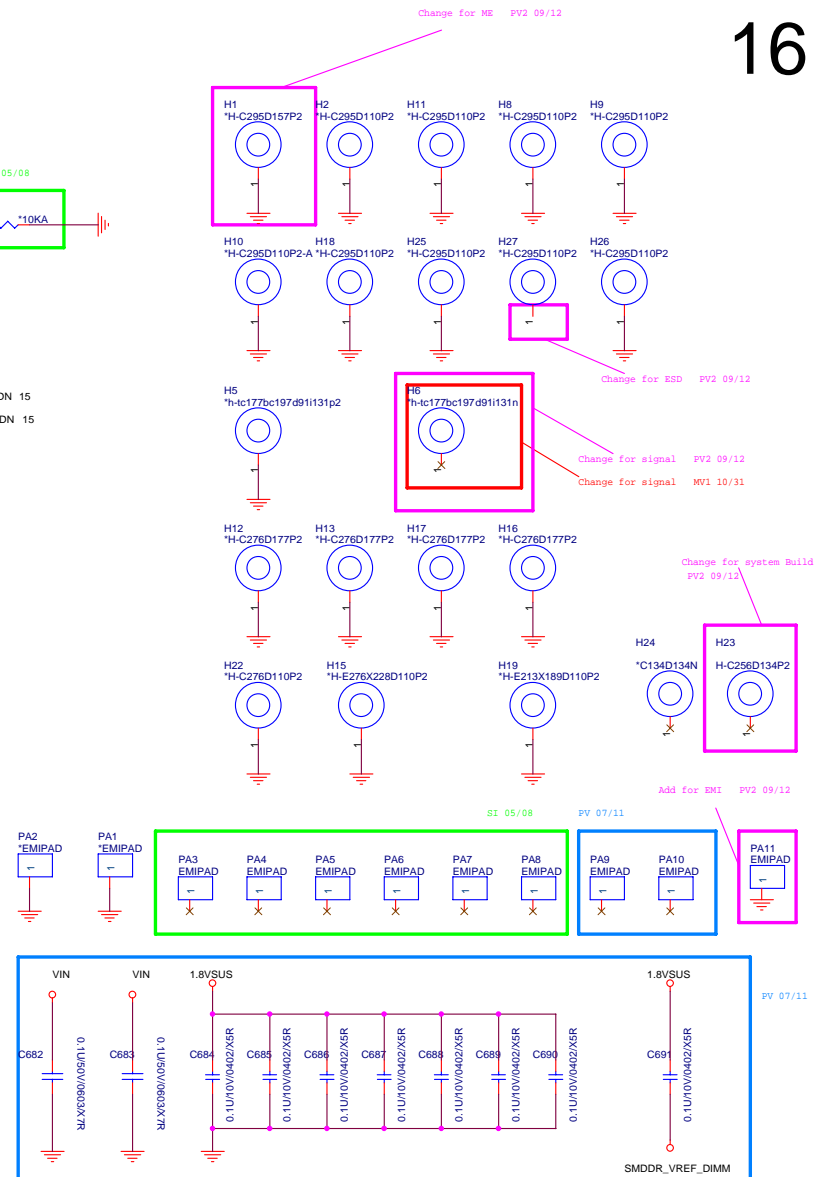
NBS/RD2/HW1

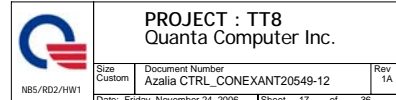
PROJECT : TT8
Quanta Computer Inc.

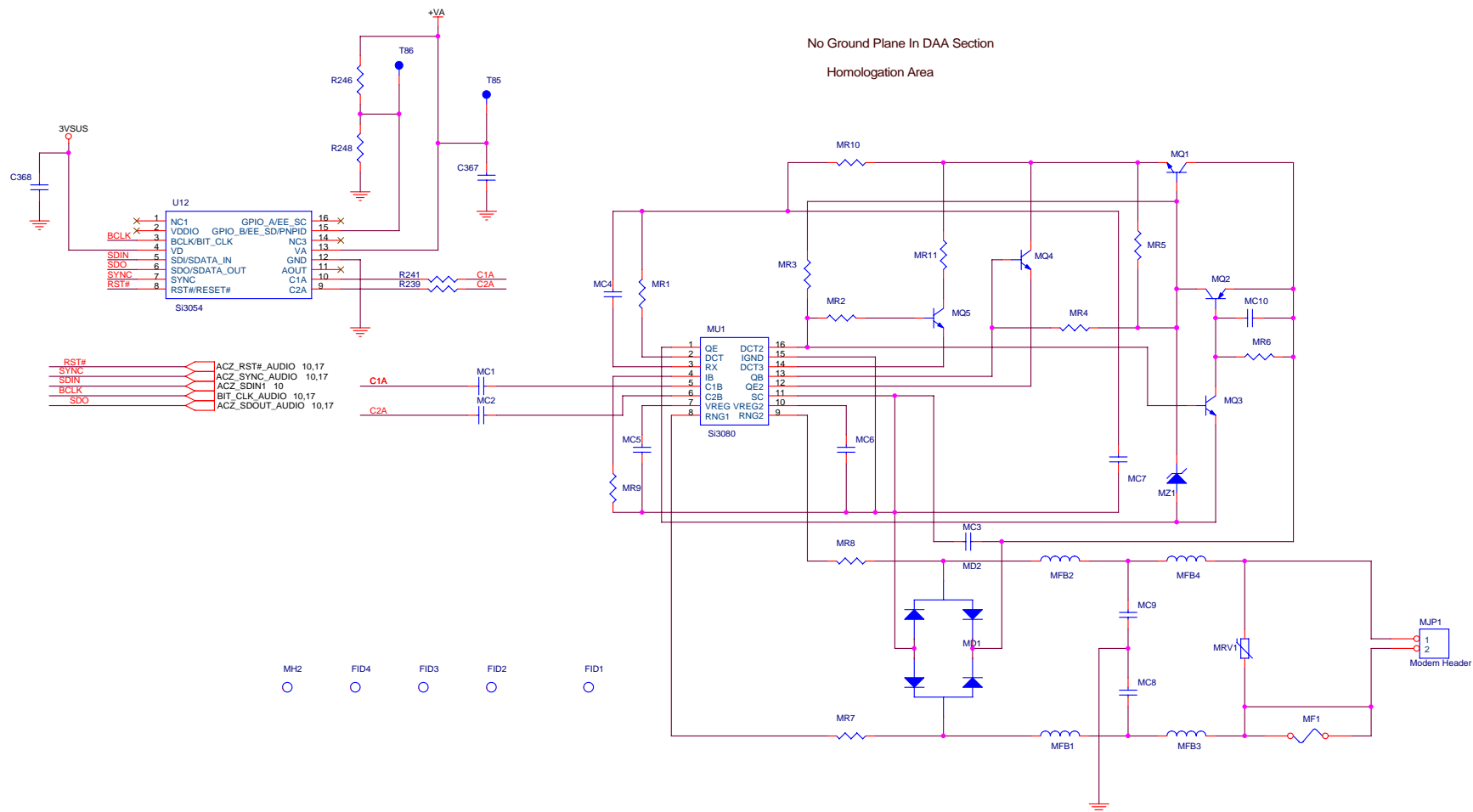
Size Custom Document Number CRT_TV_OUT Rev 1A
Date: Friday, November 24, 2006 Sheet 13 of 36











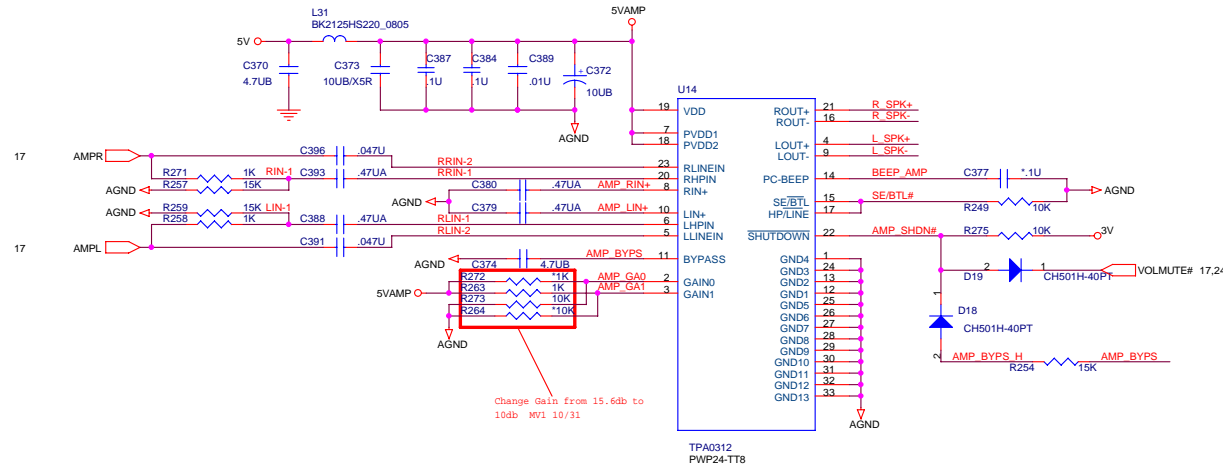
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL



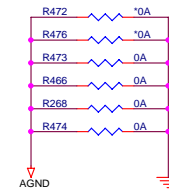
PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number MODEM (DAA)	Rev 1A
Date: Friday, November 24, 2006	Sheet 18 of 36	



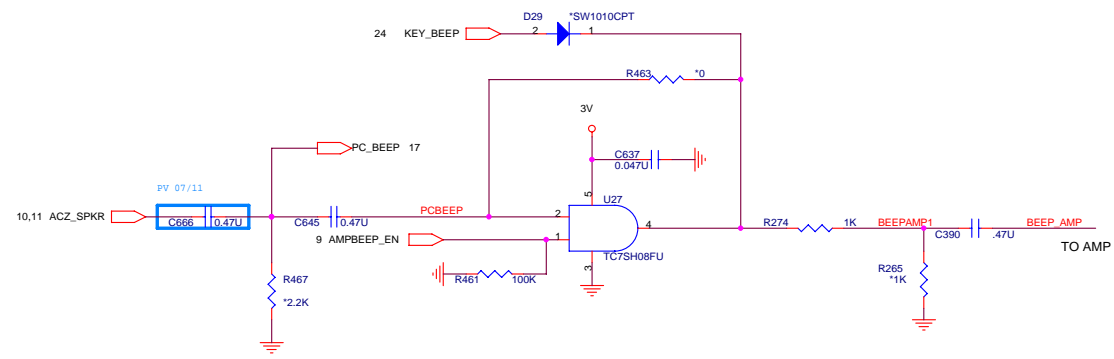
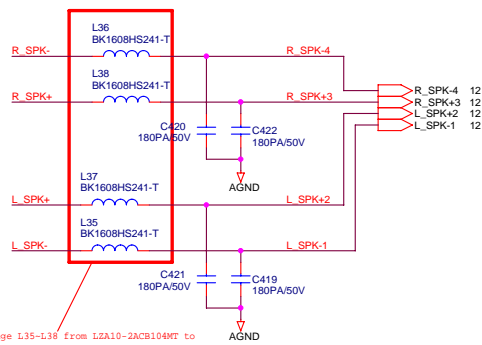
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

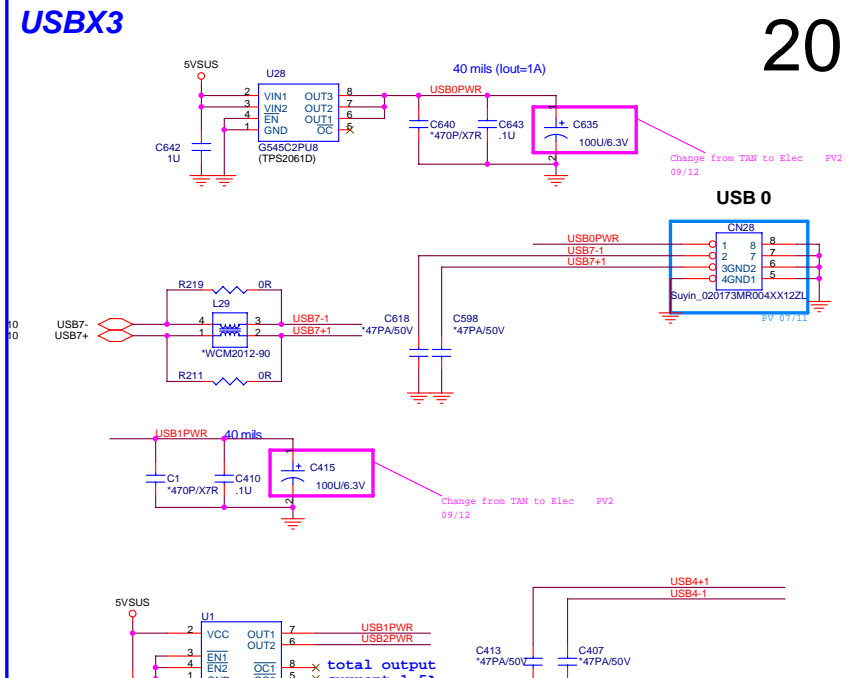


INT. SPEAKER

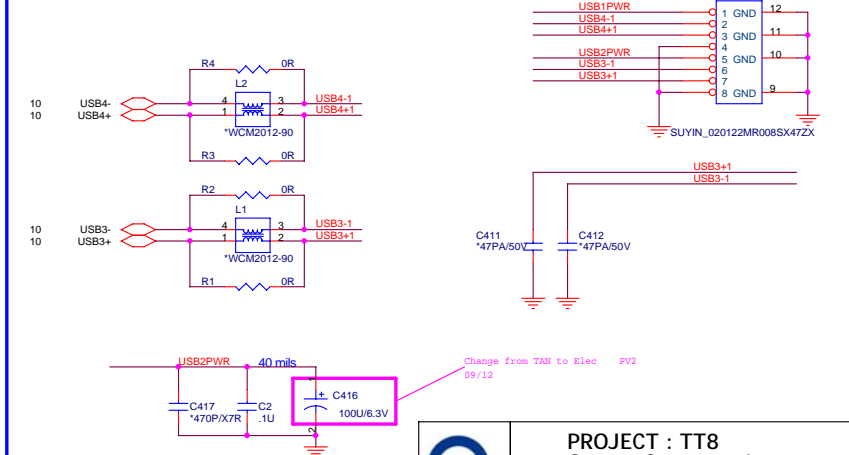
PCSPK BEEP



PROJECT : TT8
Quanta Computer Inc.

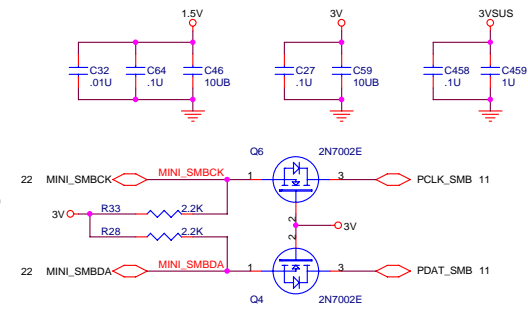
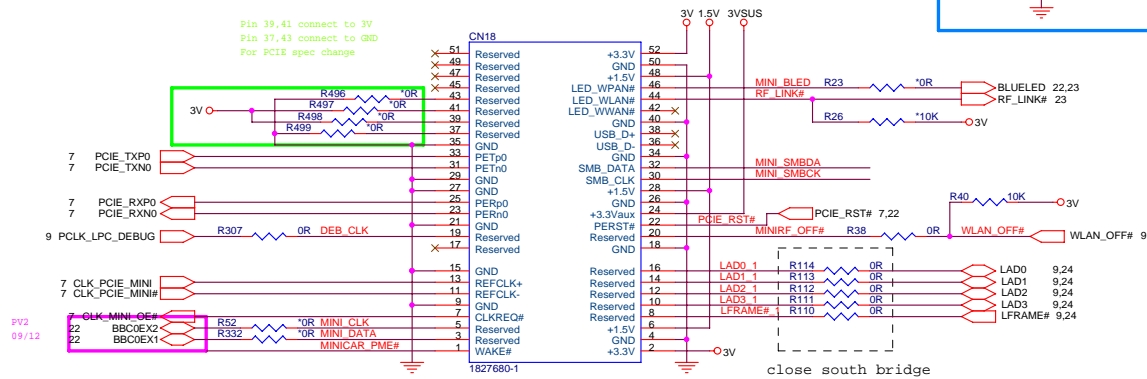


USB 1& 2

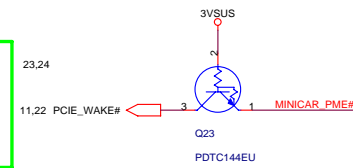
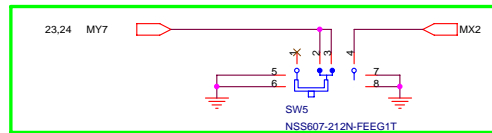


Mini PCI-E Card 1 WLAN

Pin 39,41 connect to 3V
Pin 37,43 connect to GND
For PCIe spec change

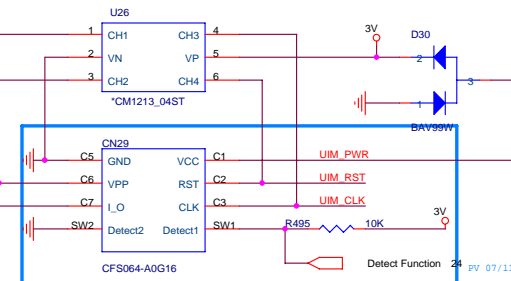
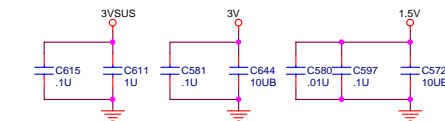
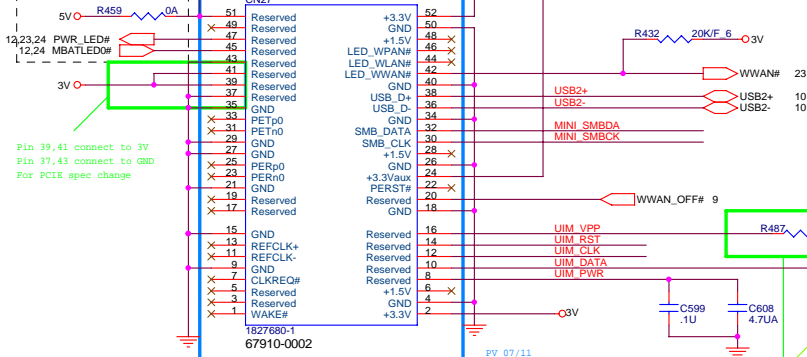


SI 05/08



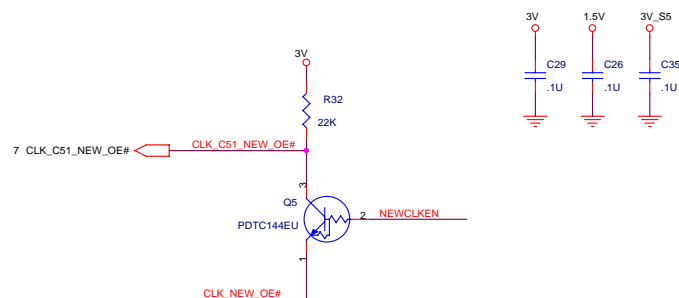
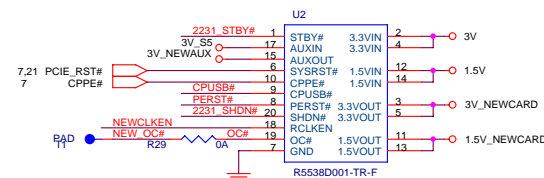
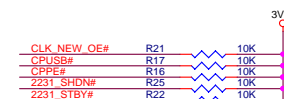
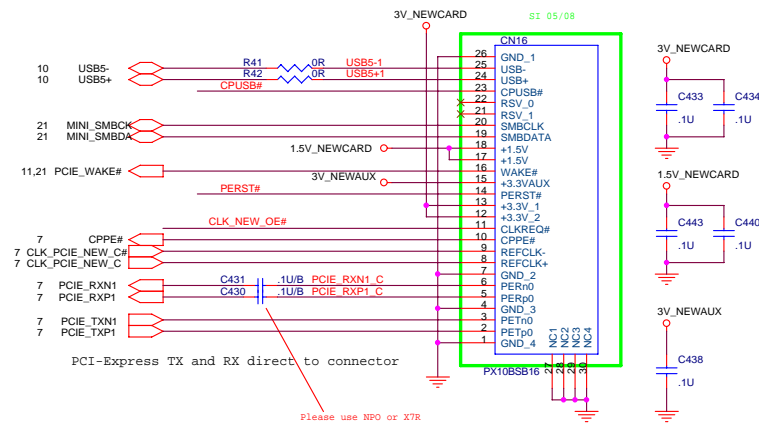
Mini PCI-E Card 2 WWAN(W/SIM)

FOR KBC DEBUG

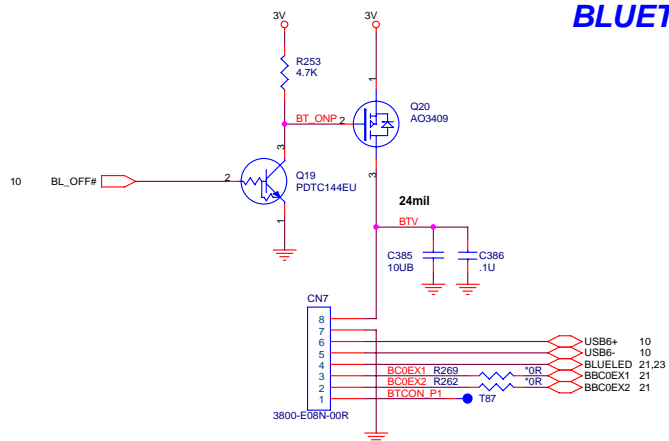


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NEWCARD



BLUETOOTH



PROJECT : TT8
Quanta Computer Inc.

Size
Custom

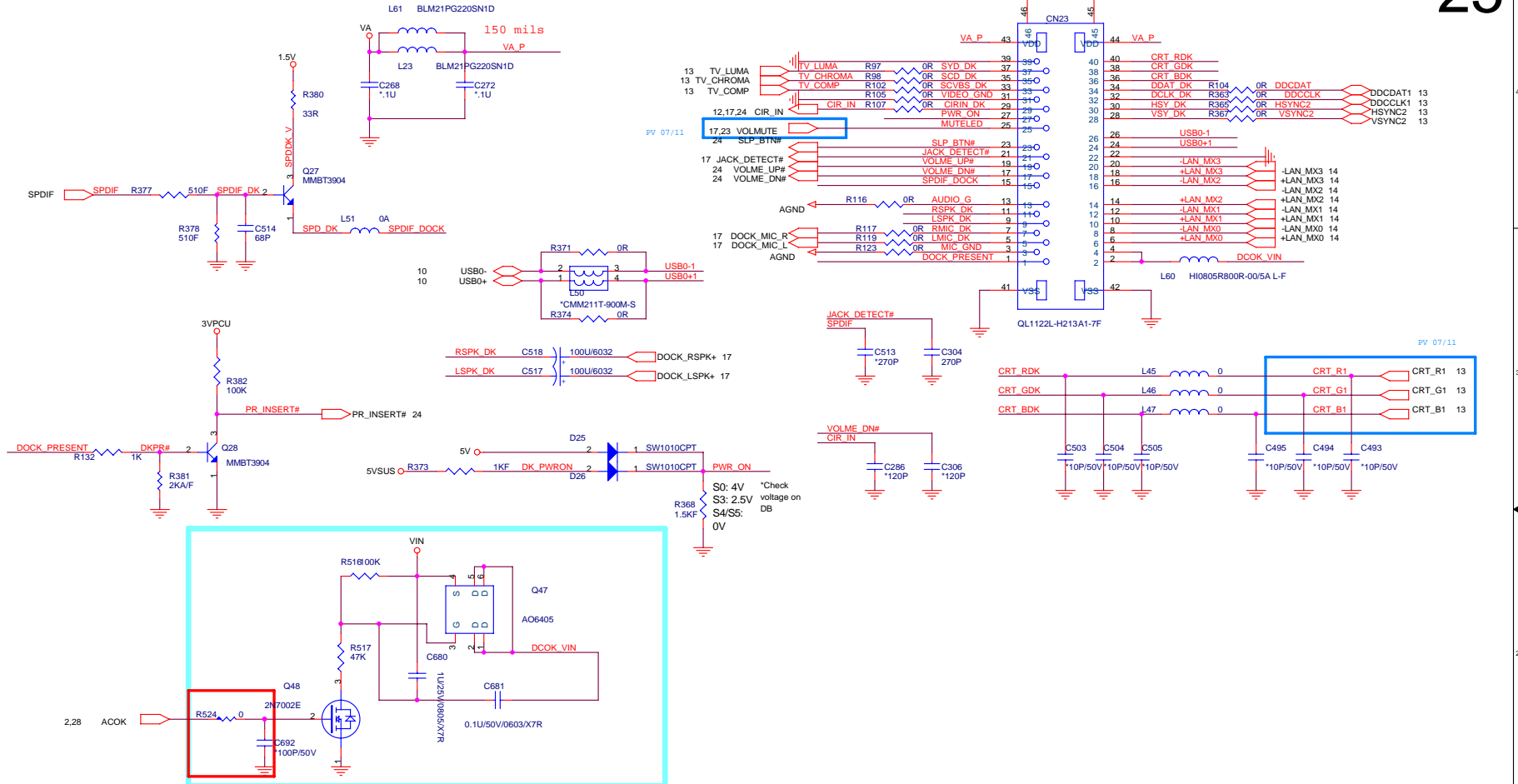
Document Number
NEW CARD/BT

Rev
1A

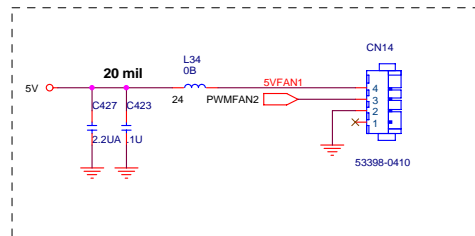
Date: Friday, November 24, 2006 Sheet 22 of 36

CABLE DOCK

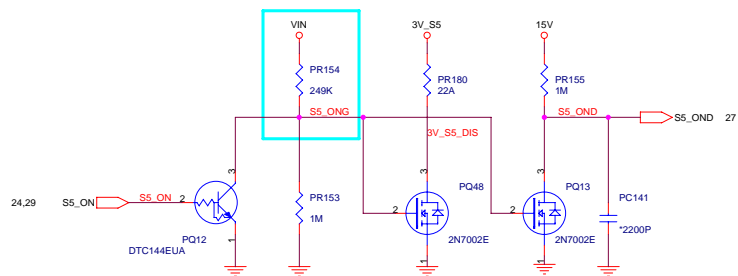
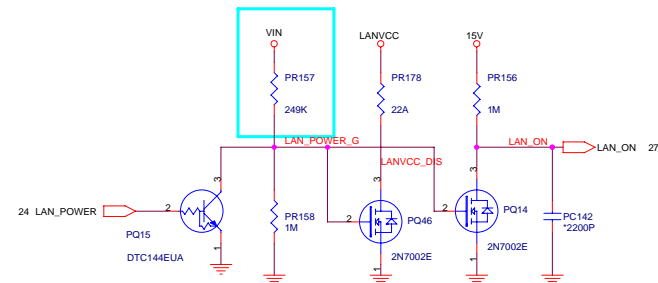
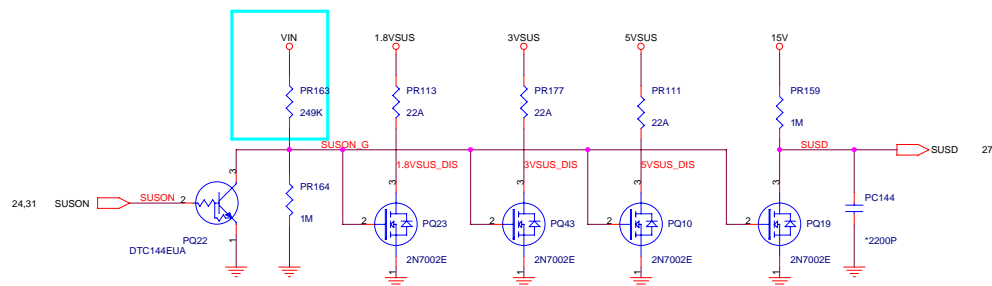
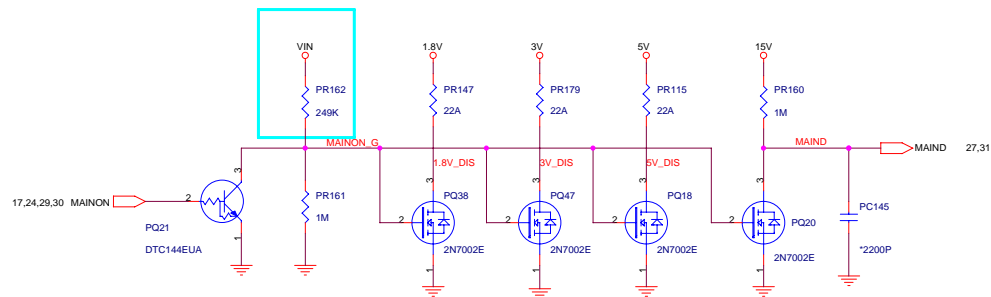
25



FAN

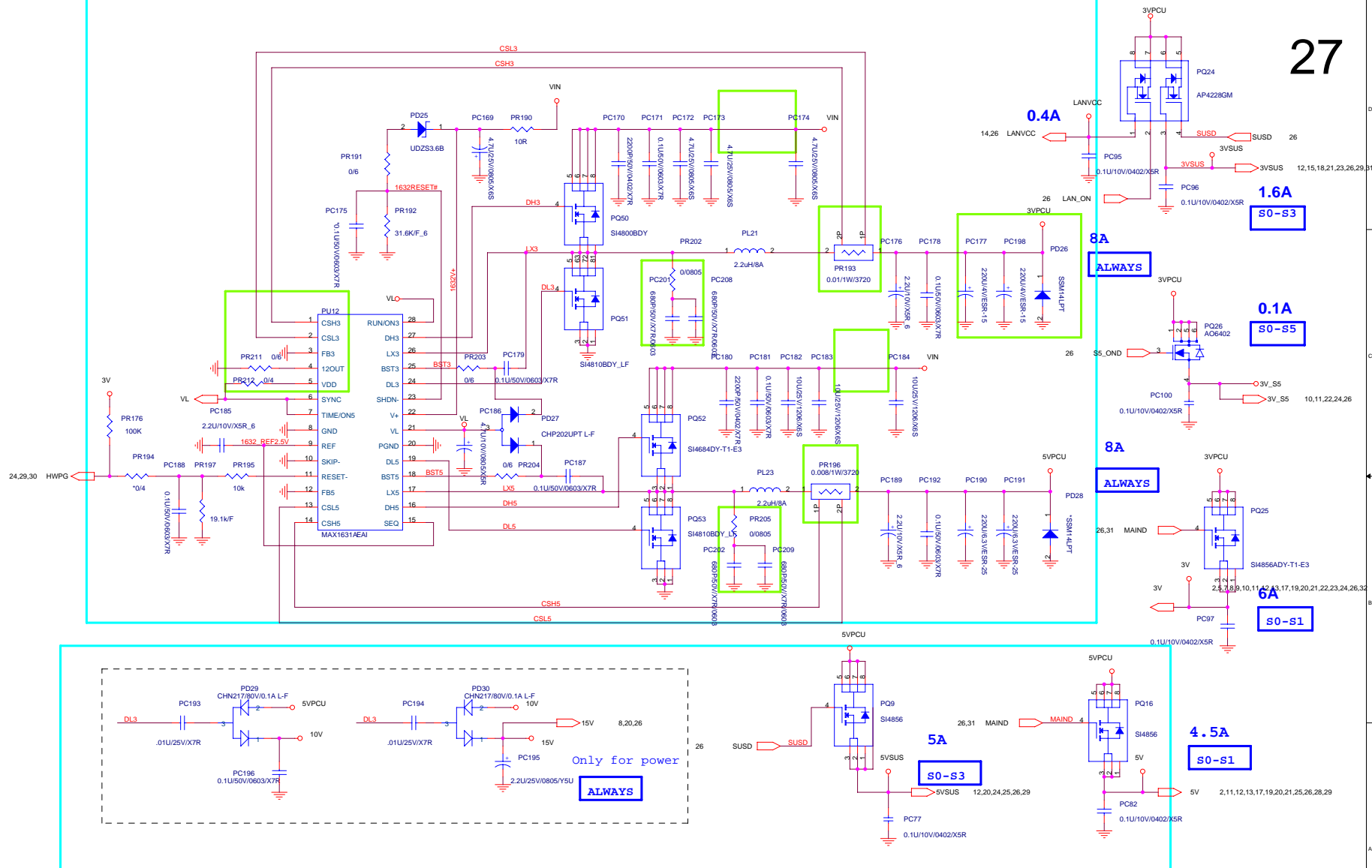


FAN1 PWM CONNECTOR



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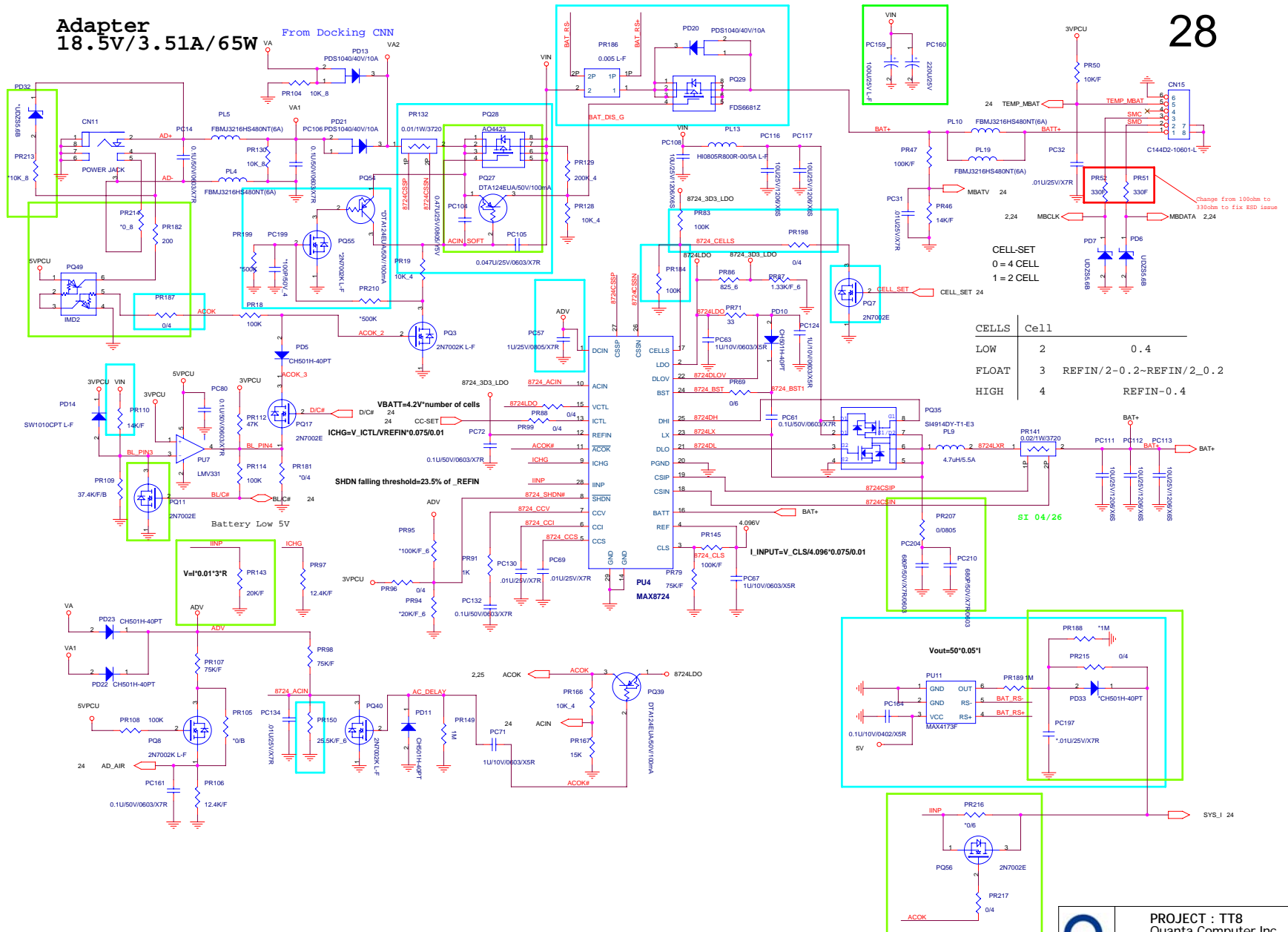
Size Custom	Document Number DISCHARGE	Rev 1A
Date: Friday, November 24, 2006	Sheet 26 of 36	



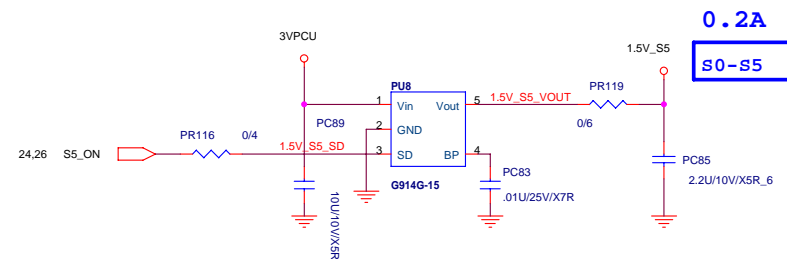
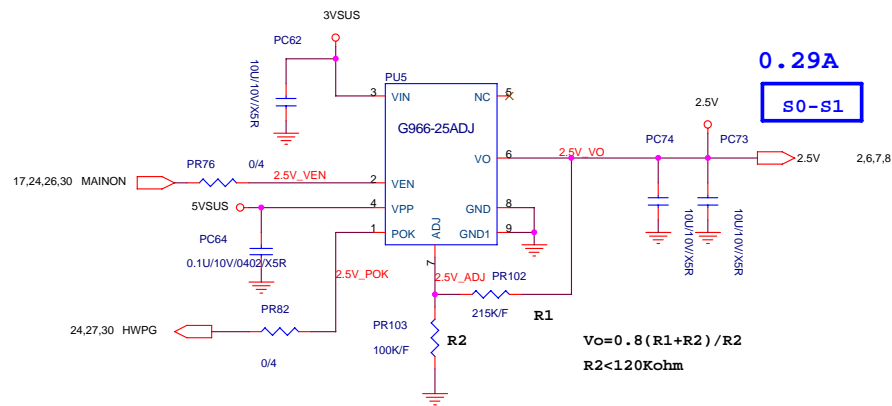
Adapter
18.5V/3.51A/65W

From Docking CNN

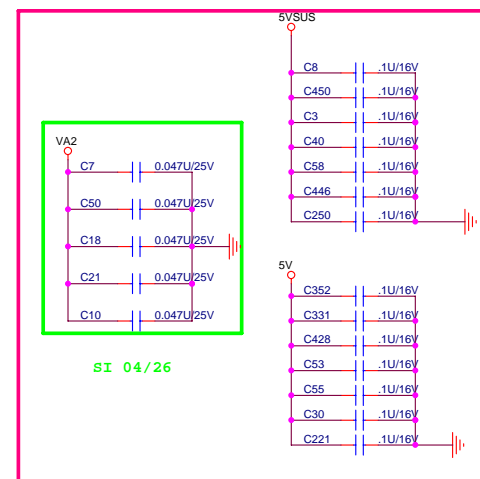
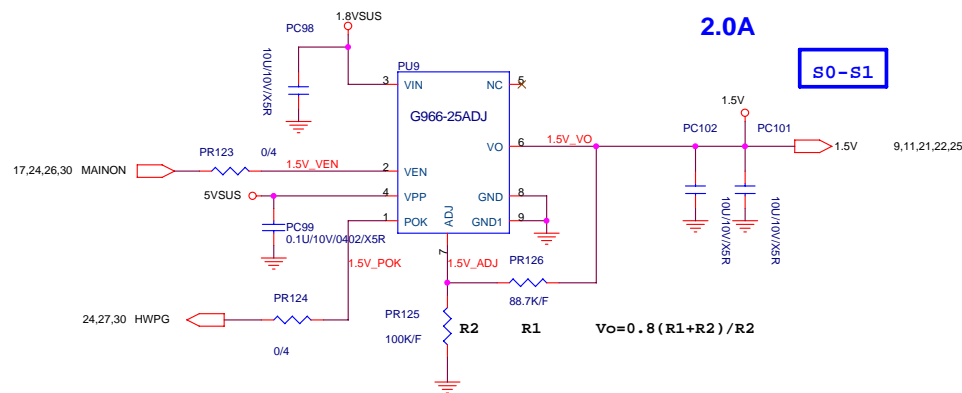
28



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EMI



NB5/RD2/HW1

PROJECT : TT8
Quanta Computer Inc.

Size
CustomDocument Number
2.5V/1.5V_S5/1.5VRev
1A

Date: Friday, November 24, 2006

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MAX1549

S0-S1

3A

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$

DCR 28m OHM

$$V_{out} = 0.5V(1 + R1/R2)$$

SI-2 modified

S0-S1

3.7A

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$

DCR 28m OHM

$$V_{out1} = 2.0V(REQ / (R_b + REQ))$$

INPUTS		OUTPUTS			REQ	VOUT1
G1	G0	OD1	OD2	OD3		
0	0	High-Z	High-Z	Hight-Z	Ra=150K	1.2V
1	0	0	High-Z	Hight-Z	Ra//ROD1=100.1K	1.0V
0	1	High-Z	0	Hight-Z	Ra//ROD2=122.4K	1.1V
1	1	High-Z	High-Z	0	Ra//ROD3=82.02K	

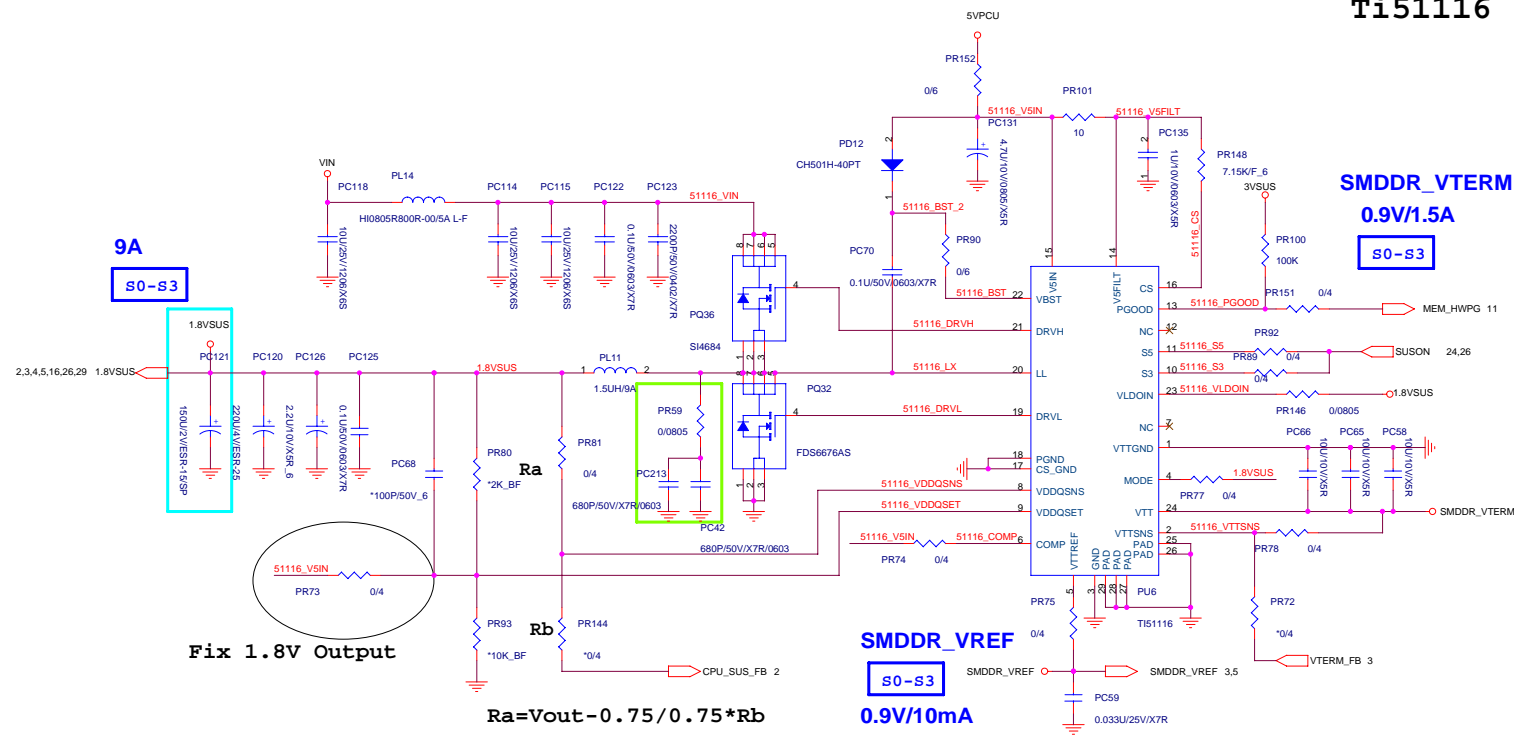
FBLANK			
VCC	OPEN	REF	GND
150us	100us	50us	blanking disabled
150us	100us	50us	100us

MAX1549Etl+



PROJECT : TT8
Quanta Computer Inc.

Size Custom Document Number
MAX1549 1.2V/1.2V_NB
Date: Friday, November 24, 2006 Sheet 30 of 36
Rev 1A




Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_TRIP(mV) = R_TRIP(Kohm) * 10(uA)$

$I_OCP = V_trip / Rds_on + I_Ripple / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_vddqns / 2$	DDR
V5IN	1.8	$V_vddqns / 2$	DDR2
FB	adjustable	$V_VDDQNS / 2$	$1.5V < VDDQ < 3V$

MODEL		CHANGE LIST	Model	OT1 MB BOARD	
DB1 --->SI1	4/17-4/20		Page	FROM	TO
			1	1A	
TT8 MB 31TT8MB0006		1.Change Audio port and senser pin resistor. Internal MIC change from Pin14,15 to Pin16,17 Docking Mic Change from Pin16,17 to Pin14,15 Docking spk change from Pin23,24 to Pin 43,44 Swap Pin30 and Pin31 Change R486 from Pin 13 to Pin 34 and change from 5.1KK to 10K Change R251 10K to R485 5.1K 2.Change WWAN and WLAN Pin define Add R487 and R488 3.Change TEMP Control chip for leakage, Change Q9 and Q10 to BAM70020074 4.Change HDD connector type, RJ45/CRT connector footprint 5.Swap LCD connector singnal from machine require 6.Swap US CRT/TV signal from nVIDIA require 7.Change battery and D30 footprint 8.Change C251,C242,C138,C66,C71,C276,C277 footprint from 0603 to 0402 9.Add Q36,Q37,R489,C661,R490 for Docking MIC detect 10.Change SW5 and CN8 footprint for machinecal request 11.Change L41 to PBY201209T-300Y-N (Footprint : 0805) 12.Delect H3 and H4 for machinecal change 13.Change C20 from 0.1U to 1U (Fix LCD rise time) 14.Move Net "SLP_BTN# from pin99 to pin87 15.Modify Docking mute LED circuit 16.Modify U25 SCI# signal from BIOS request, AddR491,R492 17.Modify Buletooth switch and ODD BAYINS# to EC 18.Change caps lock connector footprint from machencal request 19.Add U30,R495,R494,R493,Q38 for reserve SIM card 20.Change 4-in-1 card footprint 21.Add R44,R43,R48 Remove R62,R64,R69,R34,R24,R36 22.Change L45,L46,L47 to 0 ohm Del C503,C504,C505,C493,C494,C495 for D-SUB function	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	



NBS/RD2/1W/1

PROJECT : TT8
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Size Custom

Document Number
--> SI** Change history


Date: Friday, November 24, 2006

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Rev 1A

MODEL		CHANGE LIST	Model	OT1 MB BOARD	
	SI1 --->PV1		Page	FROM	TO
TT8 MB 31TT8MB0006	5/17~7/11	1.Exchange Audio port External MIC Exchange Pin22 and Pin21 CD Line Exchange Pin18 and Pin20 Internal MIC Exchange Pin16 and Pin17 Docking Mic Exchange Pin14 and Pin15 3.Change R478 from 22ohm to 0ohm 4.Change R462 0ohm to C666 0.47u for Audio chip distortion 5.Exchange R272 and R263, R273 and R264 for amplifier gain change 6.Change Q8 from BAM51030Z15 to BAM23010Z30 for Rdson issue 7.Remove C439 for MS pro card can not detect 8.Add C667,C668,C669,C670,C671,C672,C673,C674,C675,C676 for WLAN con not detect issue 9.Add reverse circuit for LED issue 10.Delect Q7 for Cap lock LED 11.Add EMI Cap C93,C118,C496,C497,C499,C566,C589,C555,C334,C337 12.Change CN19,CN27,CN28,CN29 footprint 14.Change Sim connector (Add detect pin) 15.Move Docking CRT signal after PI circuit 16.Add R500, R501 for Audio chip function 17.Add D37 and R502 for nVIDIA soluction 18.Move D22 from +5VCRT to +5VCRT3 19.Change Docking detect circuit 20.Delet H20 H21 21.Exchange MINI_DATA and MINI_CLK 22.Add Diode for SATA and ODD LED control 23.Add power controller for 5V shutdown 24.Change WLAN LED circuit 25.Add Res for ACZ signal 26.Delete H7 and H14 for ME change 27.Modify SB to Audio and Modem signal	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	
<div><div><div>NBS/RD2/1W1</div></div><div>PROJECT : TT8 Quanta Computer Inc.</div><div><div>Size Custom</div><div>Document Number --> SI** Change history</div><div>Date: Friday, November 24, 2006</div><div>Sheet 34 of 36</div><div>Rev 1A</div></div></div>					

[illegible]

MODEL		CHANGE LIST		OT1 MB BOARD	
		Model	Page	FROM	TO
TT8 MB 31TT8MB0006	PV2 --->MV1 10/17-11/15	1.Page10 Exchange USB0+/- with USB3+/- signal 2.Page12 Change CN12 Pin1 from 5VSUS to 3V 3.Page17 Change C648 and C656 from 4.7U to 22U to fix Vista issue 4.Page19 Change L35-L38 from LZA10-2ACB104MT to BK1608HS241-T 5.Page19 Change Gain from 15.6db to 10db 6.Page17 Del R260,R267,D312,D322 for Docking MIC 7.Page17 ADD R520,R521,R522,R523 for Docking MIC 8.Page21 Change PR51 PR52 from 100ohm to 330ohm to fix ESD issue 9.Page20 unstuff R188 to fix ODD problem 10.Page11 Change the board ID1 from low to high 11.Page15 Change Cap (C60,C56,C441,C44,C45)from 0.1u to 1u 12.Page15 Change Res (R318,R313,R312)from 39K to 10K 13.Page17 Add 0.01u(C693, C694) to fix high frequency problem 14.Page14 remove the cap(C408,C409) from MV build 15.Page7 Reserve C696 for nVIDIA 16.Page15 Reserve R525 and C695 for 3VSUS drop 17.Page23 Change LED4 for ME requests	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
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			31	1A	
			32	1A	
			33	1A	
<div><div><div>NBS/RD2/1HW1</div></div><div>PROJECT : TT8 Quanta Computer Inc.</div><div><div>Size Custom</div><div>Document Number --> SI** Change history</div><div>Date: Friday, November 24, 2006</div><div>Sheet 35 of 36</div><div>Rev 1A</div></div></div>					