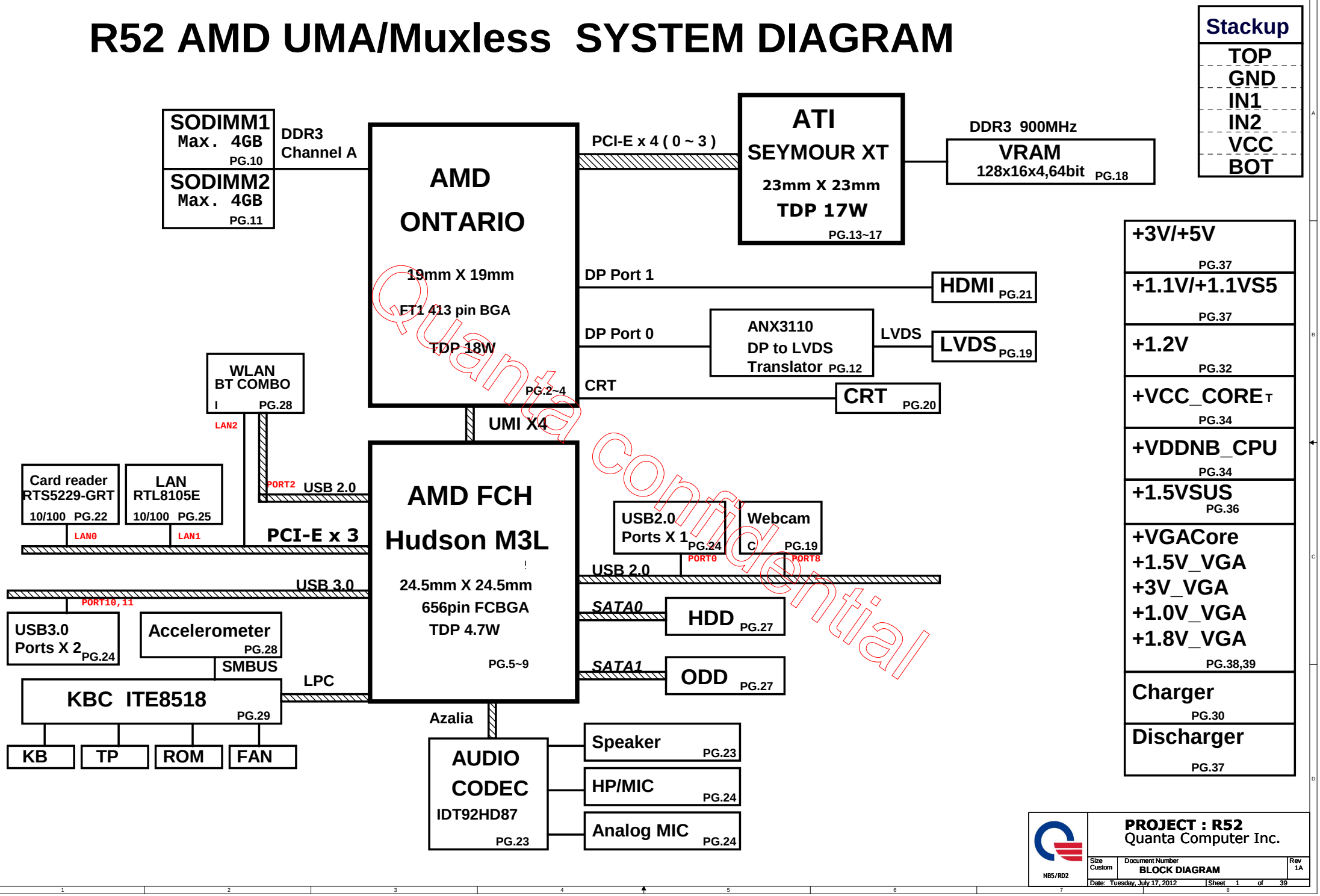
R52 AMD UMA/Muxless SYSTEM DIAGRAM



Stackup
TOP
GND
IN1
IN2
VCC
BOT

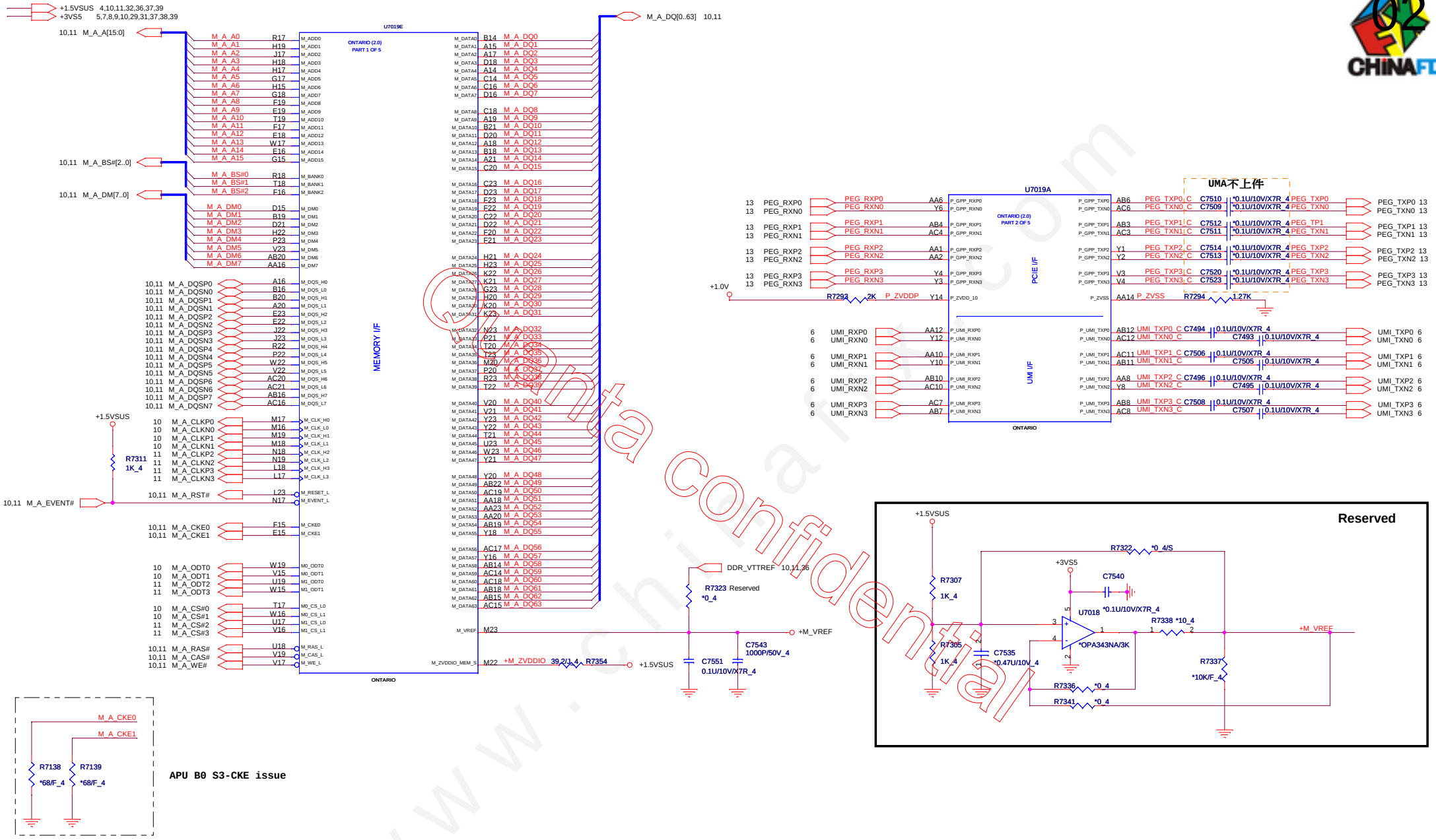
+3V/+5V	PG.37
+1.1V/+1.1VS5	PG.37
+1.2V	PG.32
+VCC_CORE T	PG.34
+VDDNB_CPU	PG.34
+1.5VSUS	PG.36
+VGACore +1.5V_VGA +3V_VGA +1.0V_VGA +1.8V_VGA	PG.38,39
Charger	PG.30
Discharger	PG.37

PROJECT : R52
Quanta Computer Inc.

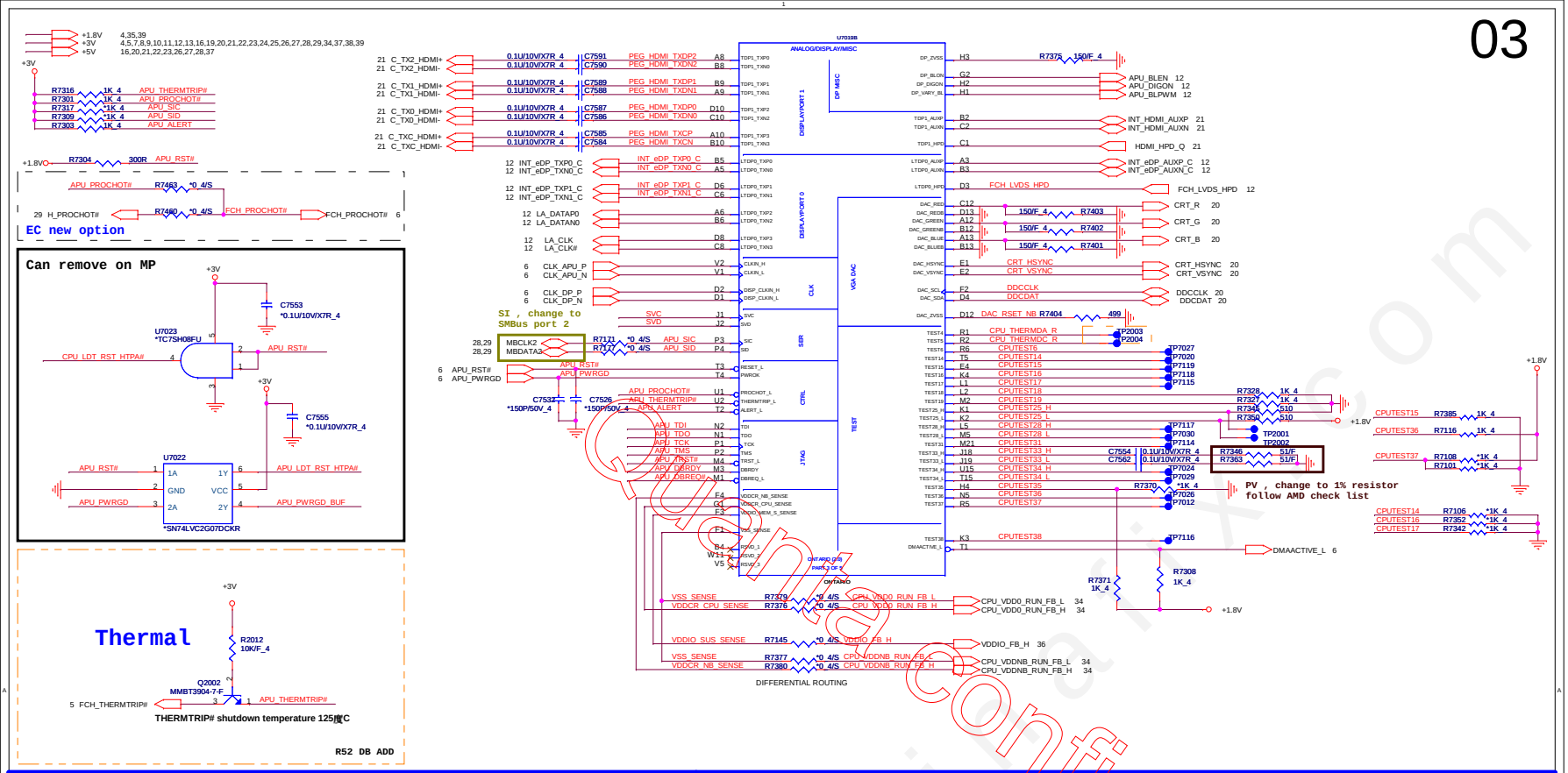
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

NB5/RD2

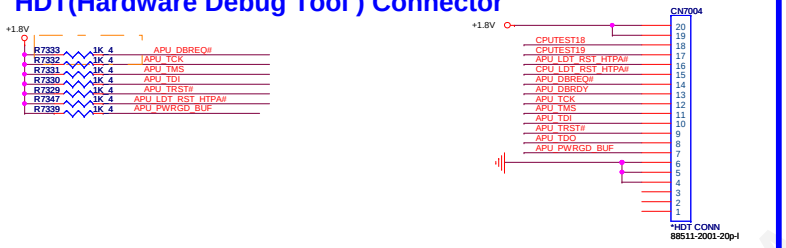
Date: Tuesday, July 17, 2012 Sheet 1 of 39



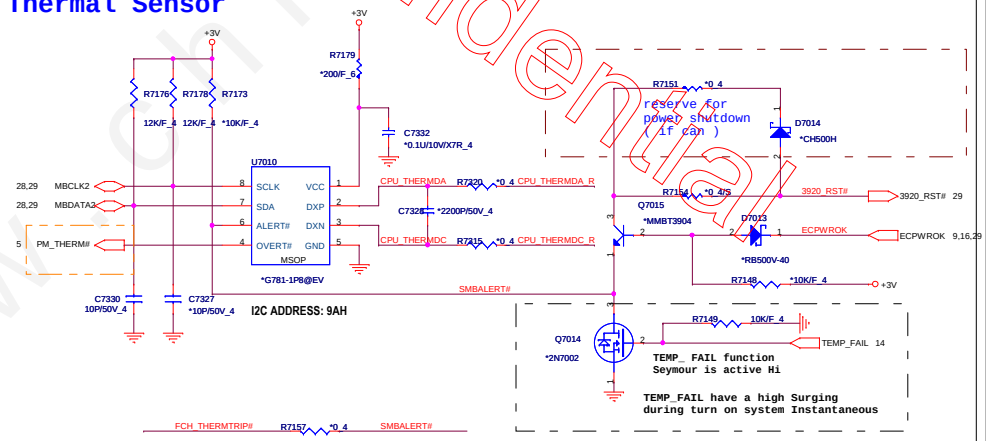
N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size	Document Number ONTARIO MEM & PCIE I/F(1/3)	Rev 1A
Date: Tuesday, July 17, 2012	Sheet 2 of 39	



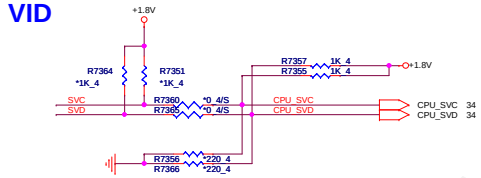
HDT(Hardware Debug Tool) Connector



Thermal Sensor

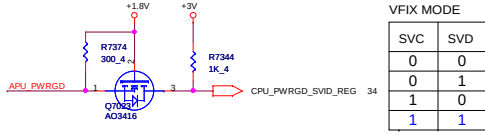


Serial VID



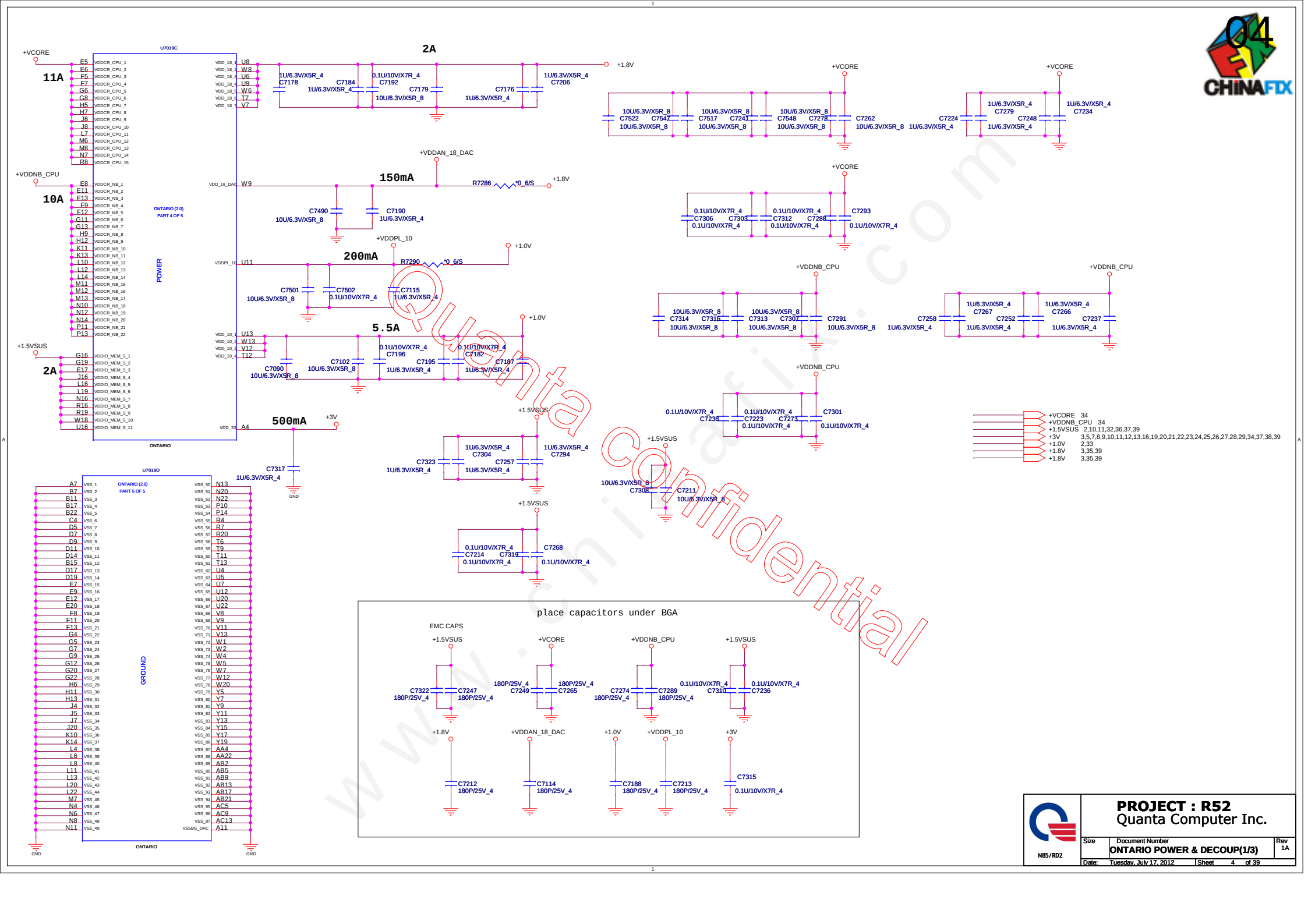
VFIX MODE — VID Override table (VDD)

SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



PROJECT :	R52
Quanta Computer Inc.	
Size	Document Number: ONTATIO DISPLAY/CLK/MI(2/3) Rev 1A
Date:	Tuesday, July 17, 2012 Sheet 3 of 39

NB5/RD2


04
CHINAFDX
U7019C
ONTARIO (2.0)
PART 4 OF 5
POWER
ONTARIO
+VCORE
11A
+VDDNB_CPU
10A
+1.5VSUS
2A
2A
150mA
200mA
5.5A
500mA
+3V
+1.8V
+1.0V
+VDDAN_18_DAC
+VDDPL_10
R7286 *0_6/S
R7290 *0_6/S
U7019D
GROUND
ONTARIO
GND
place capacitors under BGA
EMC CAPS
+1.5VSUS
+VCORE
+VDDNB_CPU
+1.5VSUS
+1.8V
+VDDAN_18_DAC
+1.0V
+VDDPL_10
+3V
+VCORE 34
+VDDNB_CPU 34
+1.5VSUS 2,10,11,32,36,37,39
+3V 3,5,7,8,9,10,11,12,13,16,19,20,21,22,23,24,25,26,27,28,29,34,37,38,39
+1.0V 2,33
+1.8V 3,35,39
+1.8V 3,35,39
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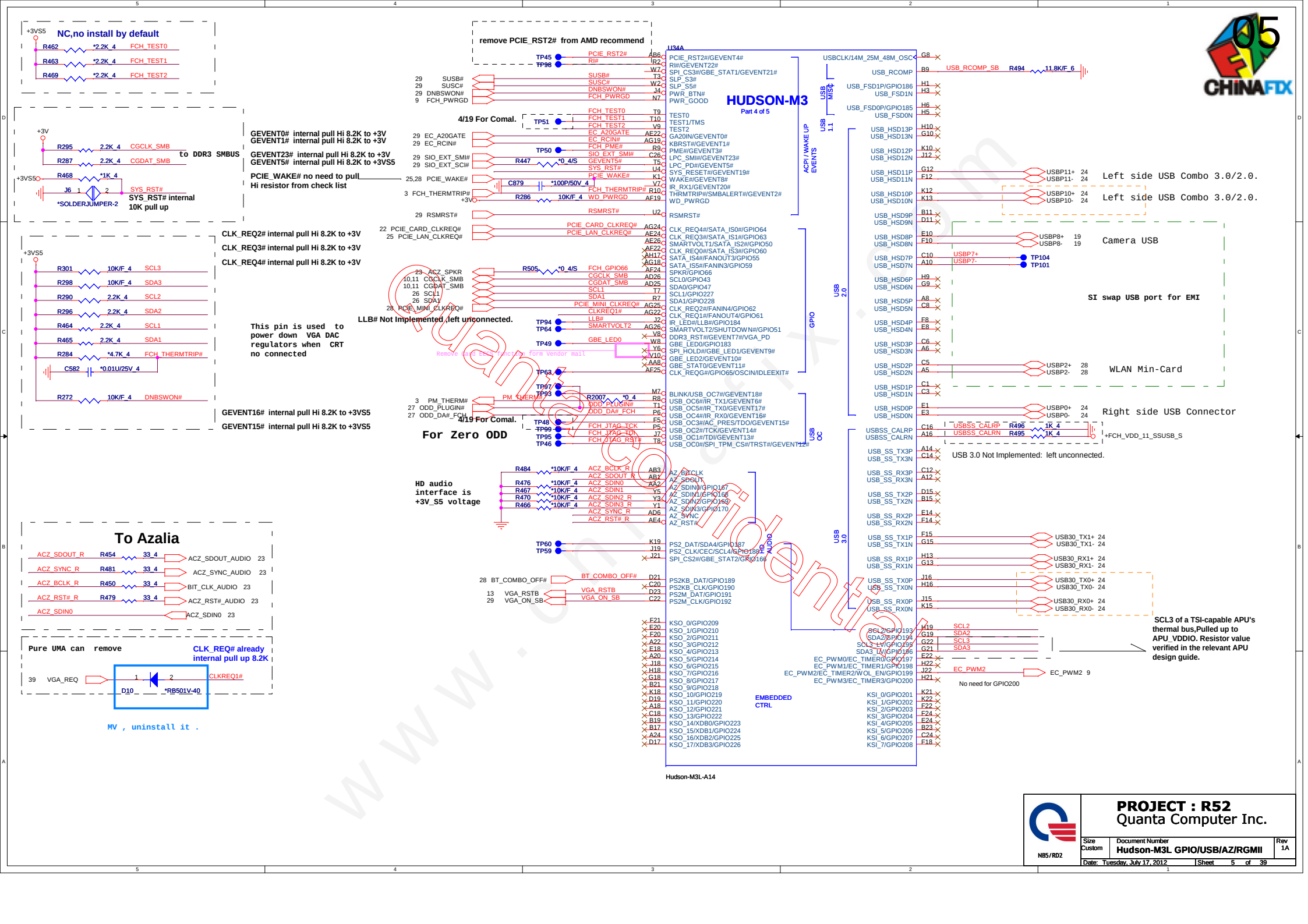
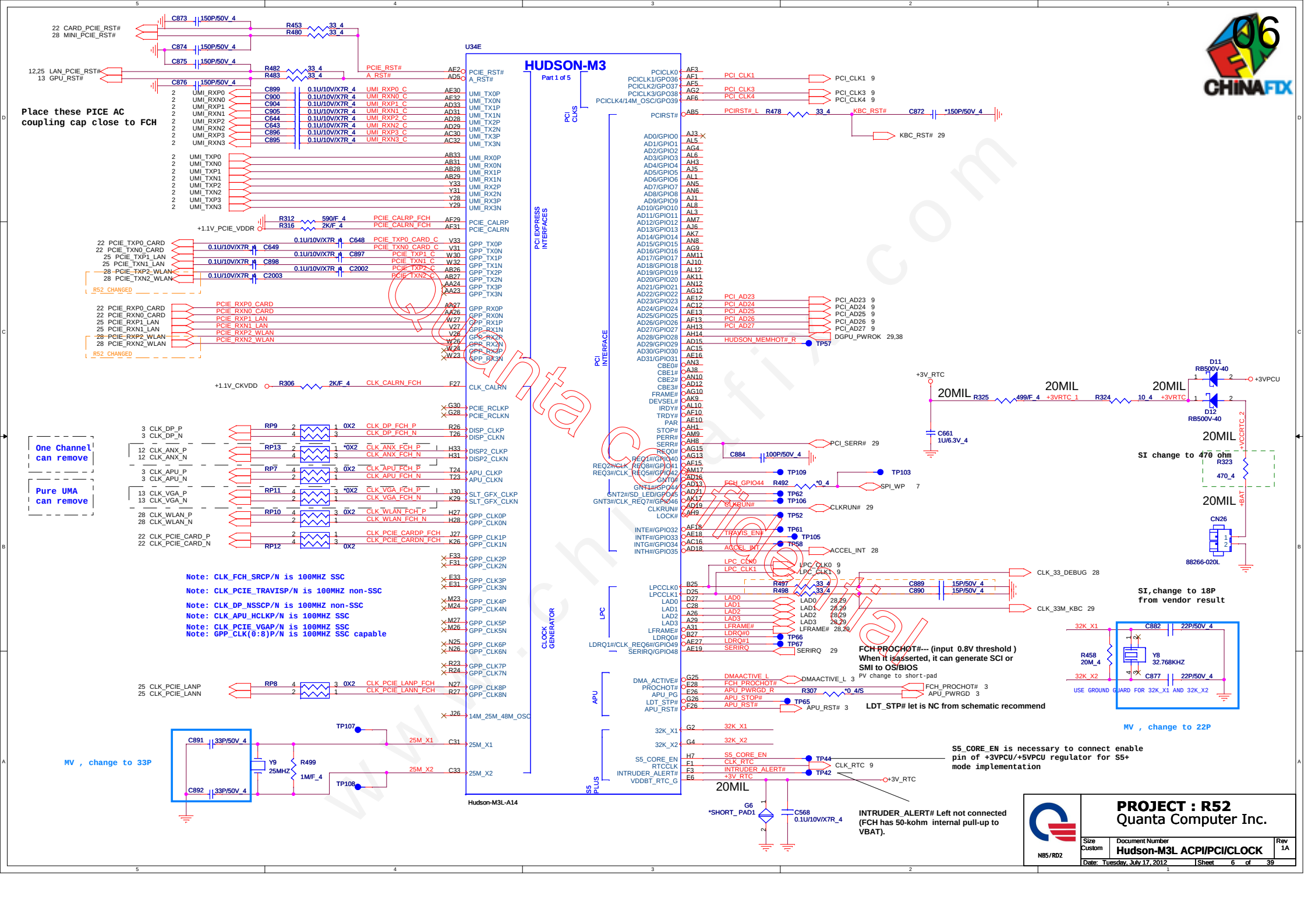
PROJECT : R52
Quanta Computer Inc.
N85/RD2
Size
Document Number
ONTARIO POWER & DECOUP(1/3)
Rev
1A
Date: Tuesday, July 17, 2012
Sheet 4 of 39


NC,no install by default
+3VS5
R462 *2.2K_4 FCH_TEST0
R463 *2.2K_4 FCH_TEST1
R469 *2.2K_4 FCH_TEST2
remove PCIE_RST2# from AMD recommend
TP45 PCIE_RST2#
TP98 RI#
29 SUSB#
29 SUSC#
29 DNBSWON#
9 FCH_PWRGD
SUSB#
SUSC#
DNBSWON#
FCH_PWRGD
4/19 For Comal.
TP51
FCH_TEST0
FCH_TEST1
FCH_TEST2
HUDSON-M3
Part 4 of 5
+3V
R295 2.2K_4 CGCLK_SMB
R287 2.2K_4 CGDAT_SMB
to DDR3 SMBUS
+3VS5
R468 *1K_4
J6
*SOLDERJUMPER-2
SYS_RST#
SYS_RST# internal 10K pull up
GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull
Hi resistor from check list
29 EC_A20GATE
29 EC_RCIN#
EC_A20GATE
EC_RCIN#
TP50
29 SIO_EXT_SMI#
29 SIO_EXT_SCI#
SIO_EXT_SMI#
SIO_EXT_SCI#
R447 *0_4/S
GEVENT5#
SYS_RST#
25,28 PCIE_WAKE#
PCIE_WAKE#
C879 *100P/50V_4
3 FCH_THERMTRIP#
FCH_THERMTRIP#
R286 10K/F_4 WD_PWRGD
RSMRST#
29 RSMRST#
CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V
22 PCIE_CARD_CLKREQ#
25 PCIE_LAN_CLKREQ#
PCIE_CARD_CLKREQ#
PCIE_LAN_CLKREQ#
+3VS5
R301 10K/F_4 SCL3
R298 10K/F_4 SDA3
R290 2.2K_4 SCL2
R296 2.2K_4 SDA2
R464 2.2K_4 SCL1
R465 2.2K_4 SDA1
R284 *4.7K_4 FCH_THERMTRIP#
C582 *0.01U/25V_4
R272 10K/F_4 DNBSWON#
23 ACZ_SPKR
10,11 CGCLK_SMB
10,11 CGDAT_SMB
26 SCL1
26 SDA1
28 PCIE_MINI_CLKREQ#
R505 *0_4/S
FCH_GPIO66
CGCLK_SMB
CGDAT_SMB
SCL1
SDA1
PCIE_MINI_CLKREQ#
CLKREQ1#
LLB# Not Implemented ,left unconnected.
This pin is used to power down VGA DAC regulators when CRT no connected
TP94 LLB#
TP64 SMARTVOLT2
TP49 GBE_LED0
TP63
TP97
TP93
3 PM_THERM#
27 ODD_PLUGIN#
27 ODD_DA#_FCH
PM_THERM#
R2007 *0_4
ODD_PLUGIN#
ODD_DA#_FCH
4/19 For Comal.
TP48
TP99
TP95
TP46
FCH_JTAG_TCK
FCH_JTAG_TDI
FCH_JTAG_RST#
For Zero ODD
GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5
R484 *10K/F_4 ACZ_BCLK_R
R476 *10K/F_4 ACZ_SDOUT_R
R467 *10K/F_4 ACZ_SDIN0
R470 *10K/F_4 ACZ_SDIN1
R466 *10K/F_4 ACZ_SDIN2_R
ACZ_SDIN3_R
ACZ_SYNC_R
ACZ_RST#_R
HD audio interface is +3V_S5 voltage
TP60
TP59
28 BT_COMBO_OFF#
BT_COMBO_OFF#
13 VGA_RSTB
29 VGA_ON_SB
VGA_RSTB
VGA_ON_SB
U34A
PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
ACPI / WAKE UP EVENTS
GPIO
USB 2.0
USB OC
HD AUDIO
EMBEDDED CTRL
USB 3.0
USB 1.1
USB MISC
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_RCOMP_SB R494 11.8K/F_6
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBP11+ 24
USBP11- 24
Left side USB Combo 3.0/2.0.
USBP10+ 24
USBP10- 24
Left side USB Combo 3.0/2.0.
USBP8+ 19
USBP8- 19
Camera USB
USBP7+
USBP7-
TP104
TP101
SI swap USB port for EMI
USBP2+ 28
USBP2- 28
WLAN Min-Card
USBP0+ 24
USBP0- 24
Right side USB Connector
USBSS_CALRP R496 1K_4
USBSS_CALRN R495 1K_4
+FCH_VDD_11_SSUSB_S
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
USB30_TX1+ 24
USB30_TX1- 24
USB30_RX1+ 24
USB30_RX1- 24
USB30_TX0+ 24
USB30_TX0- 24
USB30_RX0+ 24
USB30_RX0- 24
USB 3.0 Not Implemented: left unconnected.
SCL2
SDA2
SCL3
SDA3
SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.
EC_PWM2
EC_PWM2 9
No need for GPIO200
To Azalia
ACZ_SDOUT_R R454 33_4 ACZ_SDOUT_AUDIO 23
ACZ_SYNC_R R481 33_4 ACZ_SYNC_AUDIO 23
ACZ_BCLK_R R450 33_4 BIT_CLK_AUDIO 23
ACZ_RST#_R R479 33_4 ACZ_RST#_AUDIO 23
ACZ_SDIN0 ACZ_SDIN0 23
Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
39 VGA_REQ
D10 *RB501V-40
CLKREQ1#
MV , uninstall it .
Hudson-M3L-A14
PROJECT : R52
Quanta Computer Inc.
Size Custom
Document Number Hudson-M3L GPIO/USB/AZ/RGMII
Rev 1A
Date: Tuesday, July 17, 2012
Sheet 5 of 39
N85/RD2


HUDSON-M3
Part 1 of 5
U34E
Hudson-M3L-A14
Place these PICE AC coupling cap close to FCH
One Channel can remove
Pure UMA can remove
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable
MV , change to 33P
SI change to 470 ohm
SI,change to 18P from vendor result
MV , change to 22P
FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS
LDT_STP# let is NC from schematic recommend
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
LPC
CLOCK GENERATOR
APU
S5 PLUS
PROJECT : R52
Quanta Computer Inc.
Hudson-M3L ACPI/PCI/CLOCK
N85/RD2
Size Custom
Rev 1A
Date: Tuesday, July 17, 2012
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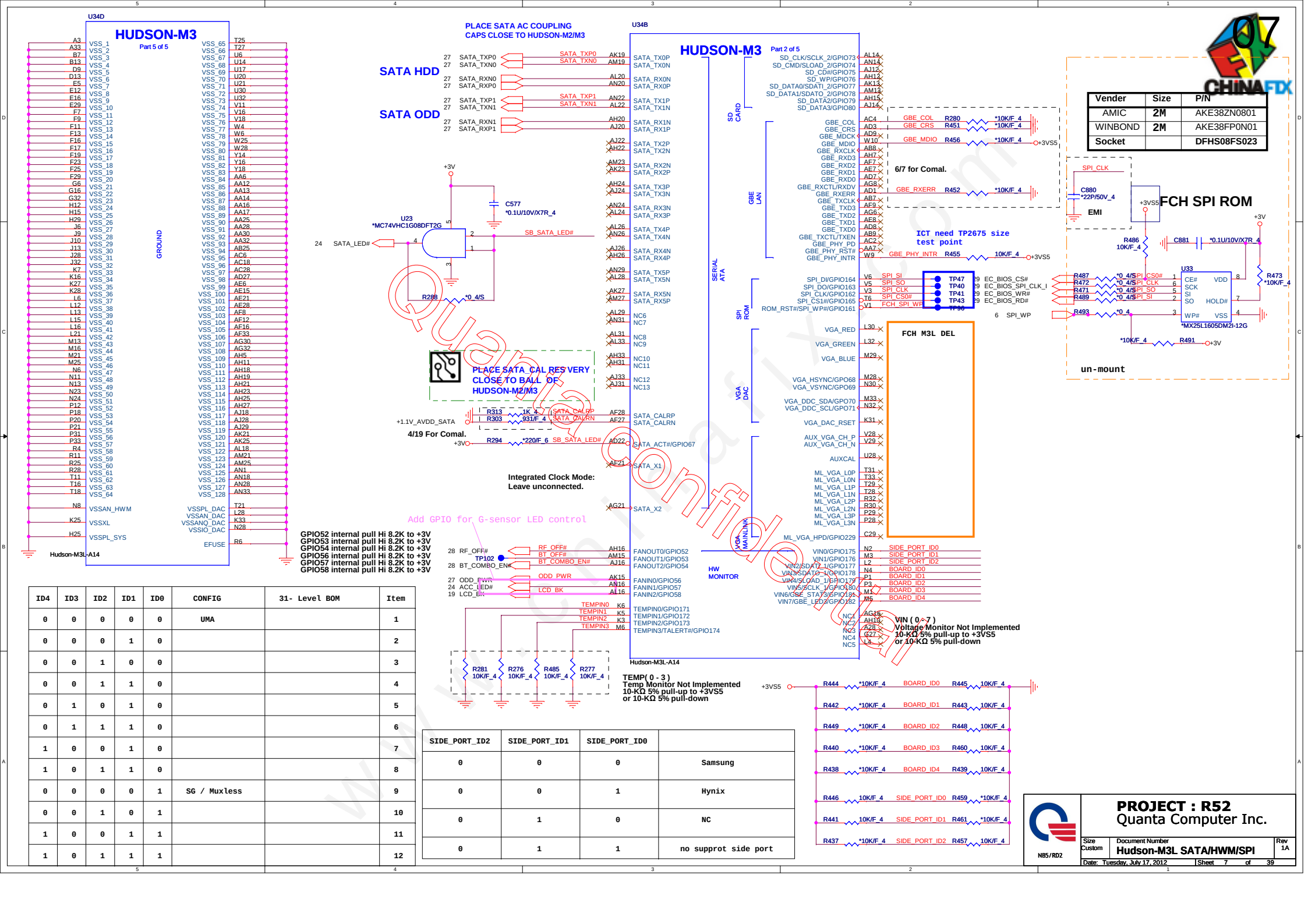
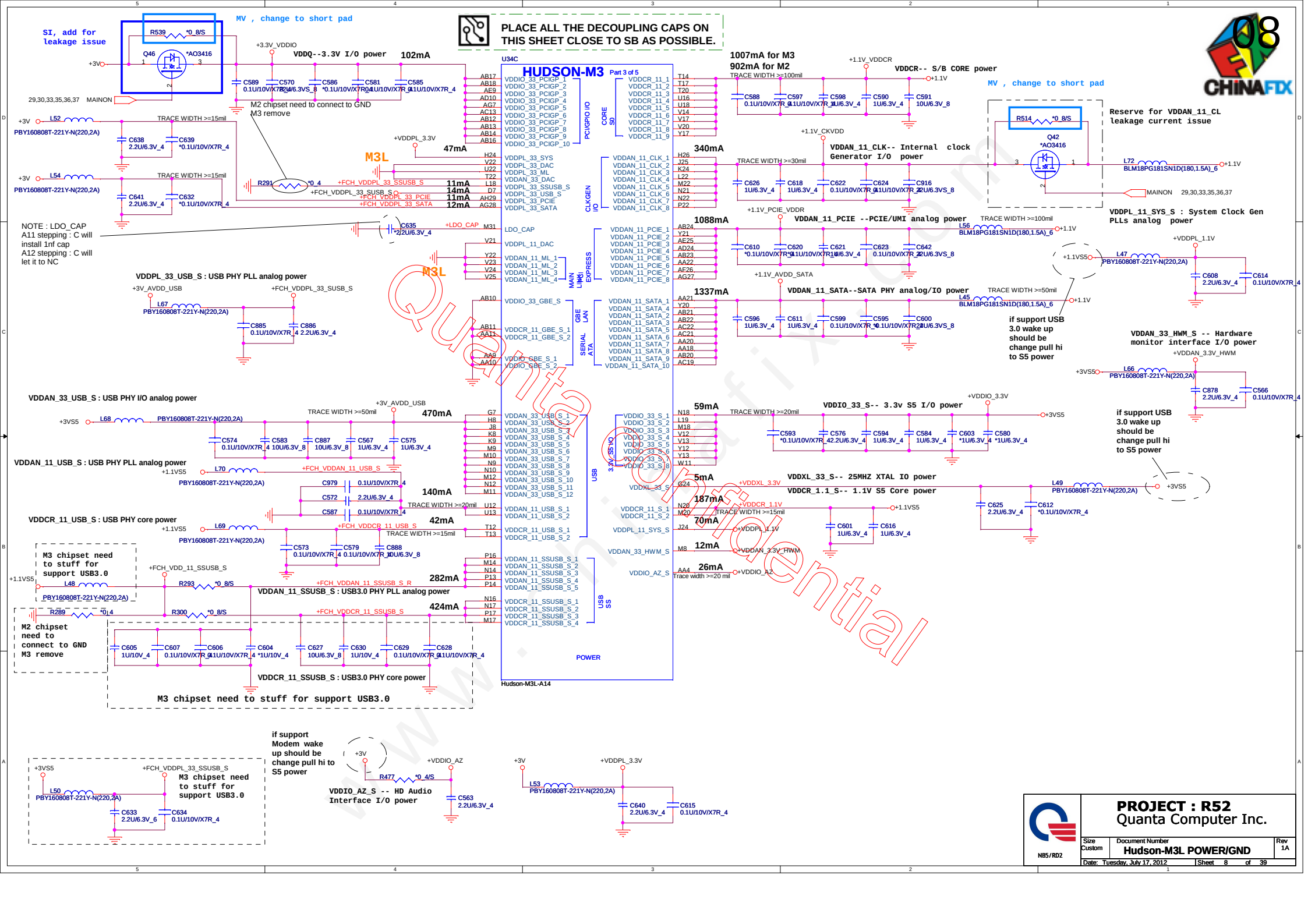


Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

PROJECT : R52			
Quanta Computer Inc.			
Size: Custom	Document Number: Hudson-M3L SATA/HWM/SPI		Rev: 1A
N85/RD2	Date: Tuesday, July 17, 2012	Sheet 7 of 39	


SI, add for leakage issue
MV , change to short pad
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
HUDSON-M3
Part 3 of 5
U34C
M3L
VDDQ--3.3V I/O power
102mA
M2 chipset need to connect to GND
M3 remove
47mA
340mA
VDDAN_11_CLK-- Internal clock Generator I/O power
1088mA
VDDAN_11_PCIE --PCIE/UMI analog power
1337mA
VDDAN_11_SATA--SATA PHY analog/IO power
VDDPL_33_USB_S : USB PHY PLL analog power
VDDAN_33_USB_S : USB PHY I/O analog power
470mA
VDDAN_11_USB_S : USB PHY PLL analog power
140mA
VDDCR_11_USB_S : USB PHY core power
42mA
M3 chipset need to stuff for support USB3.0
282mA
VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power
424mA
VDDCR_11_SSUSB_S : USB3.0 PHY core power
M3 chipset need to stuff for support USB3.0
if support Modem wake up should be change pull hi to S5 power
VDDIO_AZ_S -- HD Audio Interface I/O power
1007mA for M3
902mA for M2
VDDCR-- S/B CORE power
Reserve for VDDAN_11_CL leakage current issue
VDDPL_11_SYS_S : System Clock Gen PLLs analog power
VDDAN_33_HWM_S -- Hardware monitor interface I/O power
if support USB 3.0 wake up should be change pull hi to S5 power
VDDIO_33_S-- 3.3v S5 I/O power
59mA
VDDXL_33_S-- 25MHZ XTAL IO power
5mA
VDDCR_1.1_S-- 1.1V S5 Core power
187mA
70mA
12mA
26mA
NOTE : LDO_CAP
A11 stepping : C will install 1nf cap
A12 stepping : C will let it to NC
Hudson-M3L-A14
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PROJECT : R52
Quanta Computer Inc.
Hudson-M3L POWER/GND
N85/RD2
Size Custom
Rev 1A
Date: Tuesday, July 17, 2012
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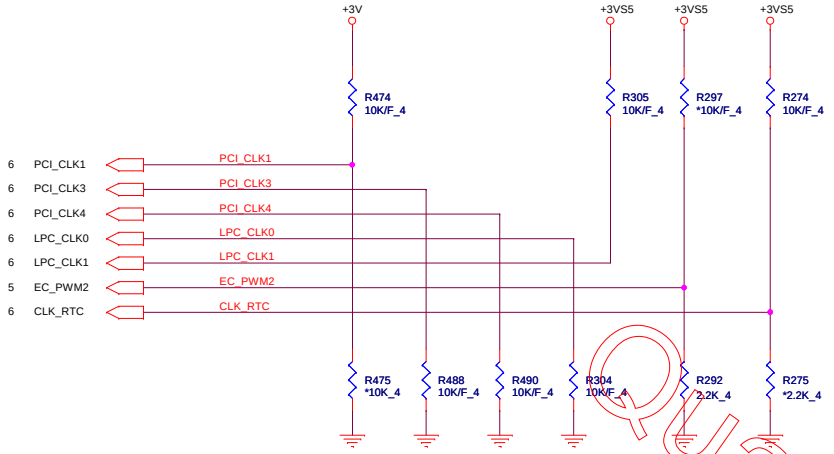
STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

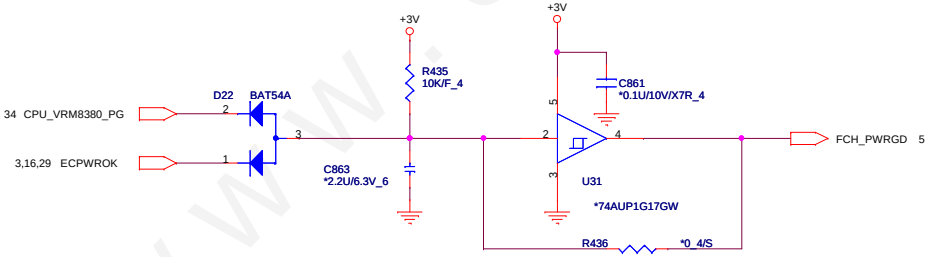
	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: Hudson-M3L STRAP/PWRGD	Rev: 1A
Date: Tuesday, July 17, 2012	Sheet 9 of 39	

DDR_STD(9.2mm)

+1.5VSUS 2,4,11,32,36,37,39
+3V 3,4,5,7,8,9,11,12,13,16,19,20,21,22,23,24,25,26,27,28,29,34,37,38,39
+0.75V_DDR_VTT 11,36

CN7018A — PC2100 DDR3 SDRAM SO-DIMM (204P)

2,11 M_A_A[15:0]	M_A_A0	98	A0	DQ0 5	M_A_DQ0
	M_A_A1	97	A1	DQ1 7	M_A_DQ1
	M_A_A2	96	A2	DQ2 15	M_A_DQ2
	M_A_A3	95	A3	DQ3 17	M_A_DQ3
	M_A_A4	92	A4	DQ4 4	M_A_DQ4
	M_A_A5	91	A5	DQ5 6	M_A_DQ5
	M_A_A6	90	A6	DQ6 16	M_A_DQ6
	M_A_A7	86	A7	DQ7 18	M_A_DQ7
	M_A_A8	89	A8	DQ8 21	M_A_DQ8
	M_A_A9	85	A9	DQ9 23	M_A_DQ9
	M_A_A10	107	A10/AP	DQ10 33	M_A_DQ10
	M_A_A11	84	A11	DQ11 35	M_A_DQ11
	M_A_A12	83	A12/BC#	DQ12 22	M_A_DQ12
	M_A_A13	119	A13	DQ13 24	M_A_DQ13
	M_A_A14	80	A14	DQ14 34	M_A_DQ14
	M_A_A15	78	A15	DQ15 36	M_A_DQ15
				DQ16 39	M_A_DQ16
2,11 M_A_BS#0		109	BA0	DQ17 41	M_A_DQ17
2,11 M_A_BS#1		108	BA1	DQ18 51	M_A_DQ18
2,11 M_A_BS#2		79	BA2	DQ19 53	M_A_DQ19
2 M_A_CS#0		114	S0#	DQ20 40	M_A_DQ20
2 M_A_CS#1		121	S1#	DQ21 42	M_A_DQ21
2 M_A_CLKP0		101	CK0	DQ22 50	M_A_DQ22
2 M_A_CLKN0		103	CK0#	DQ23 52	M_A_DQ23
2 M_A_CLKP1		102	CK1	DQ24 57	M_A_DQ24
2 M_A_CLKN1		104	CK1#	DQ25 59	M_A_DQ25
2,11 M_A_CKE0		73	CKE0	DQ26 67	M_A_DQ26
2,11 M_A_CKE1		74	CKE1	DQ27 69	M_A_DQ27
2,11 M_A_CAS#		115	CAS#	DQ28 56	M_A_DQ28
2,11 M_A_RAS#		110	RAS#	DQ29 58	M_A_DQ29
2,11 M_A_WE#		113	WE#	DQ30 68	M_A_DQ30
	DIMM1_SA0	197	SA0	DQ31 70	M_A_DQ31
	DIMM1_SA1	201	SA1	DQ32 129	M_A_DQ32
5,11 CGCLK_SMB	PCLK_SMB	202	SCL	DQ33 131	M_A_DQ33
5,11 CGDAT_SMB	PDAT_SMB	200	SDA	DQ34 141	M_A_DQ34
				DQ35 143	M_A_DQ35
2 M_A_ODT0		116	ODT0	DQ36 130	M_A_DQ36
2 M_A_ODT1		120	ODT1	DQ37 132	M_A_DQ37
				DQ38 140	M_A_DQ38
2,11 M_A_DM0		11	DM0	DQ39 142	M_A_DQ39
2,11 M_A_DM1		28	DM1	DQ40 147	M_A_DQ40
2,11 M_A_DM2		46	DM2	DQ41 149	M_A_DQ41
2,11 M_A_DM3		63	DM3	DQ42 157	M_A_DQ42
2,11 M_A_DM4		136	DM4	DQ43 159	M_A_DQ43
2,11 M_A_DM5		153	DM5	DQ44 146	M_A_DQ44
2,11 M_A_DM6		170	DM6	DQ45 148	M_A_DQ45
2,11 M_A_DM7		187	DM7	DQ46 158	M_A_DQ46
2,11 M_A_DQSP[7:0]	M_A_DQSP0	12	DQS0	DQ47 160	M_A_DQ47
	M_A_DQSP1	29	DQS1	DQ48 163	M_A_DQ48
	M_A_DQSP2	47	DQS2	DQ49 165	M_A_DQ49
	M_A_DQSP3	64	DQS3	DQ50 175	M_A_DQ50
	M_A_DQSP4	137	DQS4	DQ51 177	M_A_DQ51
	M_A_DQSP5	154	DQS5	DQ52 164	M_A_DQ52
	M_A_DQSP6	171	DQS6	DQ53 166	M_A_DQ53
	M_A_DQSP7	188	DQS7	DQ54 174	M_A_DQ54
2,11 M_A_DQSN[7:0]	M_A_DQSN0	10	DQS#0	DQ55 176	M_A_DQ55
	M_A_DQSN1	27	DQS#1	DQ56 181	M_A_DQ56
	M_A_DQSN2	45	DQS#2	DQ57 183	M_A_DQ57
	M_A_DQSN3	62	DQS#3	DQ58 191	M_A_DQ58
	M_A_DQSN4	135	DQS#4	DQ59 193	M_A_DQ59
	M_A_DQSN5	152	DQS#5	DQ60 180	M_A_DQ60
	M_A_DQSN6	169	DQS#6	DQ61 182	M_A_DQ61
	M_A_DQSN7	186	DQS#7	DQ62 192	M_A_DQ62
				DQ63 194	M_A_DQ63

DDR3-DIMM1

M_A_DQ[0..63] 2,11

Footprint check ok

Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

+1.5VSUS

C7191 0.1U/10V/X7R_4, C7167 0.1U/10V/X7R_4, C7218 0.1U/10V/X7R_4, C7171 0.1U/10V/X7R_4, C7339 0.1U/10V/X7R_4, C7321 0.1U/10V/X7R_4, C7235 0.1U/10V/X7R_4, C7130 0.1U/10V/X7R_4, C7320 0.1U/10V/X7R_4

Placement between +1.5vsus & GND(SVCC SHAPE)

+1.5VSUS

C2014 0.1U/10V/X7R_4, C2015 0.1U/10V/X7R_4, C2016 0.1U/10V/X7R_4, C2017 0.1U/10V/X7R_4

+1.5VSUS

C7202 10U/6.3V_8, C7227 10U/6.3V_8, C7200 10U/6.3V_8

DE-COUPLING FOR DIMM1

+3V

C7047 1U/6.3V_4, C7048 560P/50V_4

+0.75V_DDR_VTT

C7044 4.7U/6.3V_6

+0.75V_DDR_VTT

C7039 *0.1U/10V/X7R_4, C7040 0.1U/10V/X7R_4 — +1.5VSUS

CN7018B — PC2100 DDR3 SDRAM SO-DIMM (204P)

+1.5VSUS

2.48A

			VDD1	VSS16	44
			VDD2	VSS17	48
			VDD3	VSS18	49
			VDD4	VSS19	54
			VDD5	VSS20	55
			VDD6	VSS21	60
			VDD7	VSS22	61
			VDD8	VSS23	65
			VDD9	VSS24	66
			VDD10	VSS25	71
			VDD11	VSS26	72
			VDD12	VSS27	127
			VDD13	VSS28	128
			VDD14	VSS29	133
			VDD15	VSS30	134
			VDD16	VSS31	138
			VDD17	VSS32	139
			VDD18	VSS33	144
				VSS34	145
+3V		199	VDDSPD	VSS35	150
		77	NC1	VSS36	151
		122	NC2	VSS37	155
		125	NCTEST	VSS38	156
				VSS39	161
2,11 M_A_EVENT#		198	EVENT#	VSS40	162
2,11 M_A_RST#		30	RESET#	VSS41	167
				VSS42	168
11 +VREF_DQ		1	VREF_DQ	VSS43	172
+VREF_CA_A		126	VREF_CA	VSS44	173
				VSS45	178
		2	VSS1	VSS46	179
		3	VSS2	VSS47	184
		8	VSS3	VSS48	185
		9	VSS4	VSS49	189
		13	VSS5	VSS50	190
		14	VSS6	VSS51	195
		19	VSS7	VSS52	196
		20	VSS8		
		25	VSS9		
		26	VSS10	VTT1	203
		31	VSS11	VTT2	204
		32	VSS12		
		37	VSS13	VSS53	205
		38	VSS14	VSS54	206
		43	VSS15		

DDR3-DIMM1

+0.75V_DDR_VTT

SI , add for EMI debug

C2010 0.1U/10V/X7R_4, C7140 1000P/50V_4, C2011 0.1U/10V/X7R_4, C7370 1000P/50V_4

Place close to DIMMs

+1.5VSUS

R7210 *0_4/S

R7216 1K/F_4

+3VS5

C7354

U7014 *0.1U/10V/X7R_4

*OPA343NA/3K

R7209 *10_4

+VREF_DQ

C7380 *0.1U/10V/X7R_4

R7215 1K/F_4

C7368 *1000P/50V_4

R7206 *0_4

R7204 *0_4

R7192 *10K/F_4

C7356 0.01U/25V_4

+VREF_CA_A

R7083 *0_4/S — DDR_VTTREF 2,11,36

R7084 *1K_4

R7085 *1K_4 — +1.5VSUS

N85/RD2	PROJECT : R52 Quanta Computer Inc.	
	Size	Document Number: DDRIII SODIMM1 — Rev 1A
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+1.5VSUS 2,4,10,32,36,37,39
+3V 3,4,5,7,8,9,10,12,13,16,19,20,21,22,23,24,25,26,27,28,29,34,37,38,39
+0.75V_DDR_VTT 10,36

DDR_STD(5.2mm)

CHINAFDX

CN7019A

2,10 M_A_A[15:0]

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

2,10 M_A_BS#0 109 BA0
2,10 M_A_BS#1 108 BA1
2,10 M_A_BS#2 79 BA2
2 M_A_CS#2 114 S0#
2 M_A_CS#3 121 S1#
2 M_A_CLKP2 101 CK0
2 M_A_CLKN2 103 CK0#
2 M_A_CLKP3 102 CK1
2 M_A_CLKN3 104 CK1#
2,10 M_A_CKE0 73 CKE0
2,10 M_A_CKE1 74 CKE1
2,10 M_A_CAS# 115 CAS#
2,10 M_A_RAS# 110 RAS#
2,10 M_A_WE# 113 WE#

+3V R7051 4.7K_4 DIMM2_SA0 197 SA0
DIMM2_SA1 201 SA1
5,10 CGCLK_SMB PCLK_SMB 202 SCL
5,10 CGDAT_SMB PDAT_SMB 200 SDA

2 M_A_ODT2 116 ODT0
2 M_A_ODT3 120 ODT1

2,10 M_A_DM0 11 DM0
2,10 M_A_DM1 28 DM1
2,10 M_A_DM2 46 DM2
2,10 M_A_DM3 63 DM3
2,10 M_A_DM4 136 DM4
2,10 M_A_DM5 153 DM5
2,10 M_A_DM6 170 DM6
2,10 M_A_DM7 187 DM7

2,10 M_A_DQSP[7:0]
M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

2,10 M_A_DQSN[7:0]
M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

M_A_DQ[0..63] 2,10

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

DDR3-DIMM2

Footprint check ok

+1.5VSUS

2.48A

CN7019B

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V VDDSPD 199

NC1 77
NC2 122
NCTEST 125

2,10 M_A_EVENT# EVENT# 198
2,10 M_A_RST# RESET# 30

10 +VREF_DQ +VREF_DQ VREF_DQ 1
+VREF_CA_B VREF_CA 126

C7141 1000P/50V_4
C2012 0.1U/10V/X7R_4
C2013 0.1U/10V/X7R_4
C7344 1000P/50V_4

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203
VTT2 204
+0.75V_DDR_VTT

VSS53 205
VSS54 206

SI , add for EMI debug

DDR3-DIMM2

+VREF_CA_B

R7086 *0_4/S DDR_VTTREF 2,10,36
R7087 *1K_4
R7088 *1K_4 +1.5VSUS

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)

+1.5VSUS

C7128 0.1U/10V/X7R_4
C7169 0.1U/10V/X7R_4
C7170 0.1U/10V/X7R_4
C7168 0.1U/10V/X7R_4
C7158 0.1U/10V/X7R_4
C7131 0.1U/10V/X7R_4
C7172 0.1U/10V/X7R_4
C7129 0.1U/10V/X7R_4
C7132 0.1U/10V/X7R_4

EMI Reserve

+1.5VSUS

C2020 *0.1U/10V/X7R_4
C2021 0.1U/10V/X7R_4

DE-COUPLING FOR DIMM2

+3V

C7053 1U/6.3V_4
C7054 560P/50V_4

+0.75V_DDR_VTT

C7043 4.7U/6.3V_6

+0.75V_DDR_VTT

C7037 *0.1U/10V/X7R_4
C7038 0.1U/10V/X7R_4
+1.5VSUS

+1.5VSUS

C7201 10U/6.3V_8
C7228 10U/6.3V_8
C7226 10U/6.3V_8

N85/RD2

PROJECT : R52
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SODIMM2	1A
Date: Tuesday, July 17, 2012	Sheet 11 of 39	

Single CHANNEL drive (Stuff)

EDIDCLK 19
EDIDDATA 19

TXLOUT2+ 19
TXLOUT2- 19
TXLOUT1+ 19
TXLOUT1- 19
TXLOUT0+ 19
TXLOUT0- 19
TXLCLKOUT+ 19
TXLCLKOUT- 19

LVDS_BLON 19
DISP_ON 19
DPST_PWM 19

PV , change to 1K

Place close to LCD Conn

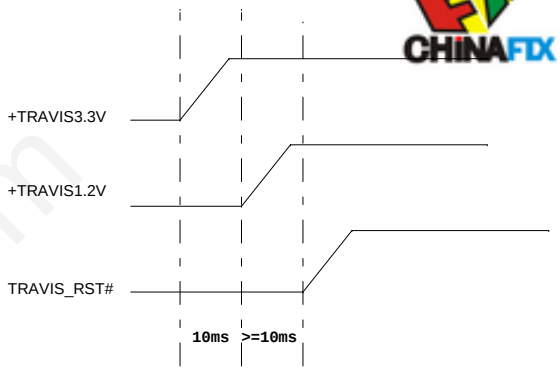
R52 DB ADD
Place close to APU

Dual CHANNEL drive

EDOM recommend R2003/R2004 NO Stuff
AMD recommend R2005/R2006 Stuff

R2005 & R2006 UMA不上件

ANX3110 Power Up Sequence



GPIO_0 : Define VAR_BL & BL_EN & DIGON H/W or S/W control power up timming
Pull Hi for H/W mode
---chip have defined power up timing
Pull Low for S/W mode --
APU through DPRX port to program it

GPIO_1 & GPIO_2 can let it to NC from vendor review

CLK_SEL:
Pull Hi for 100MHZ clk source input
Pull Low for 27MHZ crystal input

DPRX_HPD :
It will transfer to Hi when power enable

That is for debug only, can let it to NC

remove level shift

Place close to Travis

ANALOGIX ANX3110

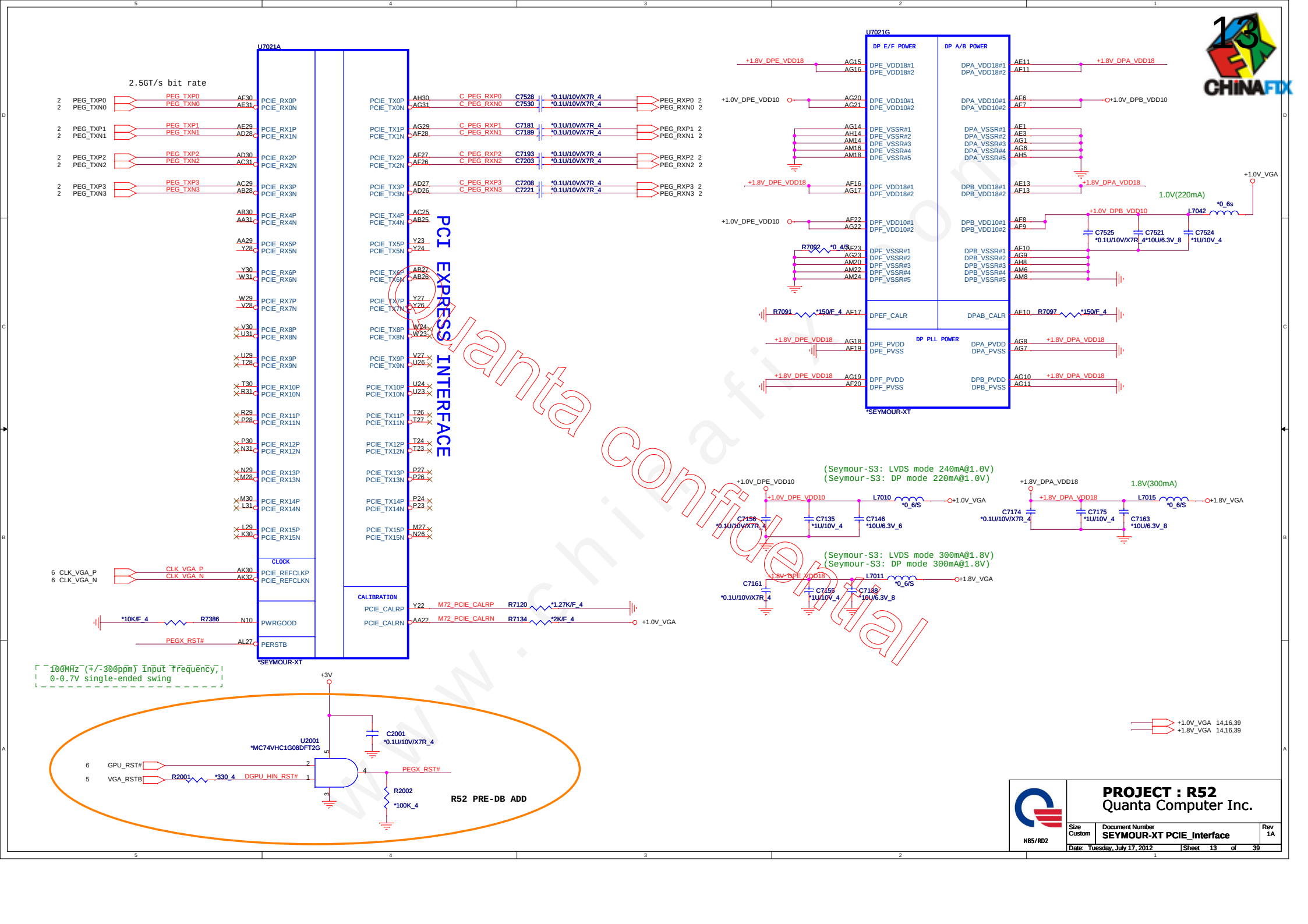
*ANX3110

50mA 120mA 100mA 120mA

150mA

250mA

PROJECT : R52 Quanta Computer Inc.			
Size: Custom	Document Number: ANX3110		Rev: 1A
Date: Tuesday, July 17, 2012	Sheet 12 of 39		
NB5/RD2			


U7021A
2.5GT/s bit rate
PCI EXPRESS INTERFACE
CLOCK
CALIBRATION
*SEYMOUR-XT
U7021G
DP E/F POWER
DP A/B POWER
DP PLL POWER
DPEF_CALR
DPAB_CALR
(Seymour-S3: LVDS mode 240mA@1.0V)
(Seymour-S3: DP mode 220mA@1.0V)
(Seymour-S3: LVDS mode 300mA@1.8V)
(Seymour-S3: DP mode 300mA@1.8V)
1.0V(220mA)
1.8V(300mA)
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing
U2001
*MC74VHC1G08DFT2G
R52 PRE-DB ADD
PROJECT : R52
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number
SEYMOUR-XT PCIE_Interface
Rev 1A
Date: Tuesday, July 17, 2012
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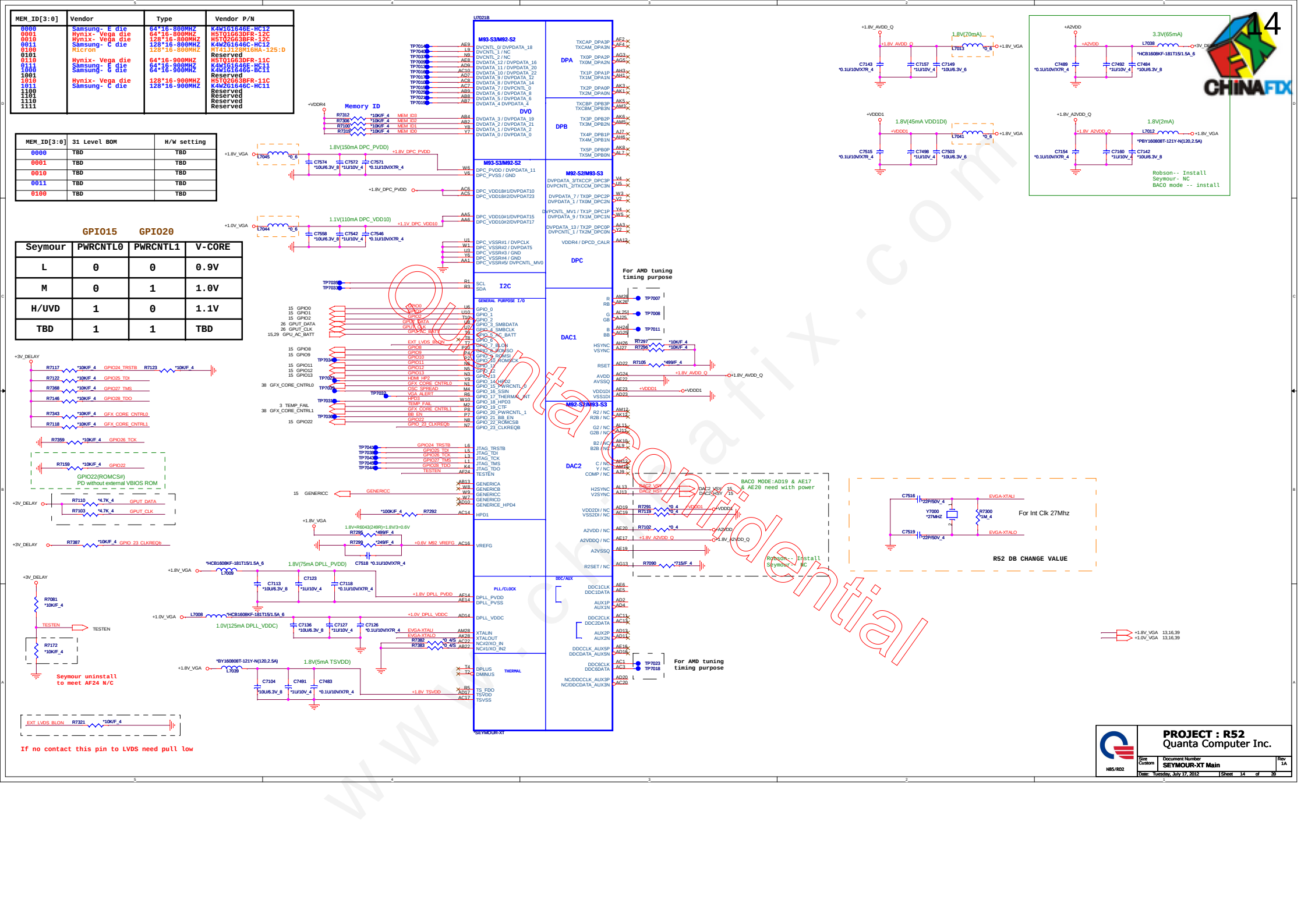
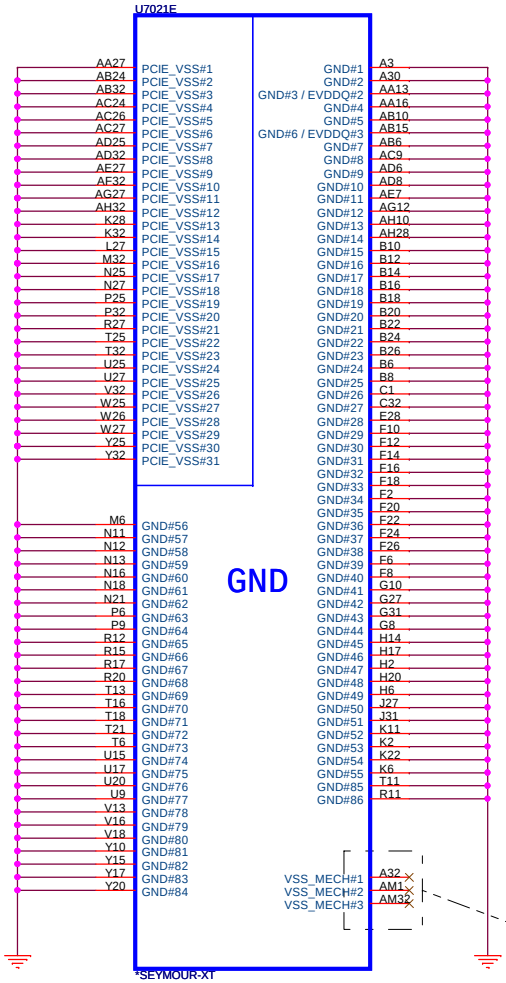
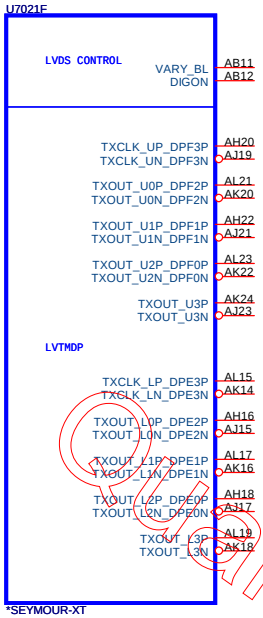
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63DFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101	Reserved		
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- E die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- E die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

MEM_ID[3:0]	31 Level BOM	H/W setting
0000	TBD	TBD
0001	TBD	TBD
0010	TBD	TBD
0011	TBD	TBD
0100	TBD	TBD

	GPIO15	GPIO20	
Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1.0V
H/UVD	1	0	1.1V
TBD	1	1	TBD







CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

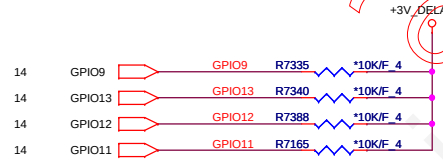
RECOMMENDED SETTINGS:
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
			X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

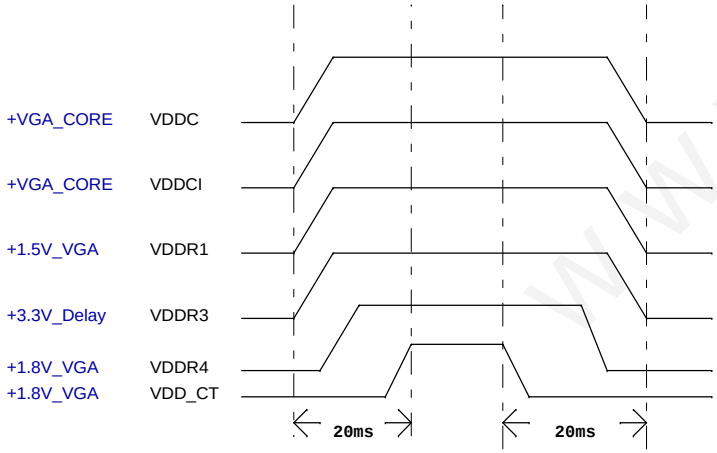
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2



For Robson & Seymour should be NC

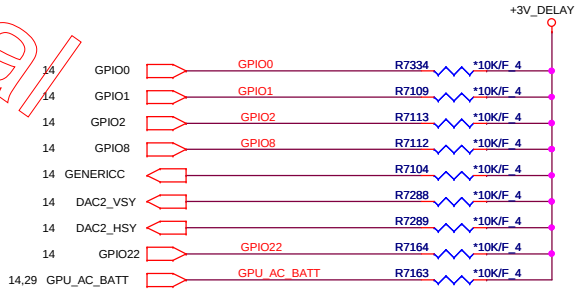
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



+3V_DELAY 14,16,38

PROJECT : R52
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SEYMOUR-XT GND / LVDS/ Straps	1A
NB5/RD2	Date: Tuesday, July 17, 2012	Sheet 15 of 39

+1.5V_VGA 17,18,39
+1.8V_VGA 13,14,39
+1.0V_VGA 13,14,39
+VGA_CORE 38
+3V 3,4,5,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,34,37,38,39
+5V 20,21,22,23,26,27,28,37

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

+1.5V_VGA
1.5V (DDR3, MVDDQ = 1.5V@1.2A)
C7357 *2.2U/6.3V_4 C7283 *2.2U/6.3V_4 C7302 *2.2U/6.3V_4 C7297 *2.2U/6.3V_4 C7290 *2.2U/6.3V_4 C7282 *2.2U/6.3V_4
C7623 *10U/6.3V_6S C7619 *10U/6.3V_6S C7364 *10U/6.3V_6S C7369 *10U/6.3V_6S C7375 *10U/6.3V_6S C7298 *0.1U/10V/X7R_4 C7296 *0.1U/10V/X7R_4 C7300 *0.1U/10V/X7R_4 C7352 *0.1U/10V/X7R_4

U7021D
MEM I/O
VDDR1#1 H13
VDDR1#2 H16
VDDR1#3 H19
VDDR1#4 J10
VDDR1#5 J23
VDDR1#6 J24
VDDR1#7 J9
VDDR1#8 K10
VDDR1#9 K23
VDDR1#10 K24
VDDR1#11 K9
VDDR1#12 L11
VDDR1#13 L12
VDDR1#14 L13
VDDR1#15 L20
VDDR1#16 L21
VDDR1#17 L22

LEVEL TRANSLATION
VDD_CT#1 AA20
VDD_CT#2 AA21
VDD_CT#3 AB20
VDD_CT#4 AB21

M93-S3/M92-S2 I/O
VDDR3#1 AA17
VDDR3#2 AA18
VDDR3#3 AB17
VDDR3#4 AB18

VDDR4#1 / VDDR5 V12
VDDR4#2 Y12
VDDR4#3 / VDDR5 U12
NC#1 / VDDR4 AA11
DVCLK / VDDR4 Y11
NC#3 / VDDR5 V11
NC / VDDR5 U11

MEM CLK
VDDRHA L17
VSSRHA L16

PLL
PCIE_PVDD AM30

MPV18 L8
SPV18 H7
SPV10 H8
SPVSS J7

BACK BIAS
BBP#1 M11
BBP#2 M12

*SEYMOUR-XT

PCIE
PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AF25
PCIE_VDDR#8 AG26

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 M22
PCIE_VDDC#6 N22
PCIE_VDDC#7 N23
PCIE_VDDC#8 N24
PCIE_VDDC#9 R22
PCIE_VDDC#10 T22
PCIE_VDDC#11 U22
PCIE_VDDC#12 V22

CORE POWER
VDDC#1 AA15
VDDC#2 N15
VDDC#3 N17
VDDC#4 R13
VDDC#5 R16
VDDC#6 R18
VDDC#7 Y21
VDDC#8 T12
VDDC#9 T15
VDDC#10 T17
VDDC#11 T20
VDDC#12 U13
VDDC#13 U16
VDDC#14 U18
VDDC#15 V21
VDDC#16 V15
VDDC#17 V17
VDDC#18 V20
VDDC#19 Y13
VDDC#20 Y16
VDDC#21 Y18
VDDC#22 R21
VDDC#23 /BIF_VDDC U21
VDDC#19/BIF_VDDC

ISOLATED CORE I/O
VDDCI#1 M13
VDDCI#2 M15
VDDCI#3 M16
VDDCI#4 M17
VDDCI#5 M18
VDDCI#6 M20
VDDCI#7 M21
VDDCI#8 N20

1.8V(219mA VDD_CT)
+1.8V_VGA L7040 *PBY160808T-121Y-N(120,2.5A) +1.8V_VDD_CT
C7500 *10U/6.3V_6 C7499 *1U/10V_4 C7225 *1U/10V_4 C7497 *1U/10V_4 C7219 *0.1U/10V/X7R_4
Gated 3.3V 60mA by VDDC

+3V_VGA L7043 *0_6/S +3V_DELAY
C7207 *1U/10V_4 C7216 *1U/10V_4 C7210 *1U/10V_4 C7538 *10U/6.3V_6
VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

+VDDR4
+1.8V_VGA L7016 *0_6 +VDDR4
C7185 *10U/6.3V_6 C7194 *1U/10V_4 C7229 *0.1U/10V/X7R_4 TP7028
1.8V(170mA VDDR4)

For Seymour,PCIE_PVDD is PCIE_VDDR

1.8V(75mA MPV18)
+1.8V_VGA L7046 *HCB1608KF-181T15/1.5A_6 MPV18
C7578 *1U/10V_4 C7577 *0.1U/10V/X7R_4

1.8V(50mA SPV18)
+1.8V_VGA L7020 *PBY160808T-121Y-N(120,2.5A) SPV18
C7269 *1U/10V_4 C7255 *0.1U/10V/X7R_4

1.0V_VGA(100mA SPV10)
+1.0V_VGA L7017 *PBY160808T-121Y-N(120,2.5A) +1.0V_VGA_SPV10
C7275 *10U/6.3V_6 C7299 *0.1U/10V/X7R_4 C7272 *1U/10V_4

+1.8V_PCIE_VDDR
1.8V(440mA)
*PBY160808T-221Y-N(220,2A) L7014
C7217 *0.1U/10V/X7R_4 C7220 *0.1U/10V/X7R_4 C7162 *1U/10V_4 C7151 *1U/10V_4 C7150 *1U/10V_4 C7205 *1U/10V_4 C7139 *1U/10V_4 C7165 *10U/6.3V_6

+1.0V_PCIE_VDDC
1.0V(2.0A)
L7019 *0_8/S
C7271 *1U/10V_4 C7253 *1U/10V_4 C7239 *1U/10V_4 C7261 *1U/10V_4 C7251 *1U/10V_4 C7270 *1U/10V_4 C7280 *1U/10V_4 C7263 *10U/6.3V_6

VDDC+VDDCI
0.85~1.1V(14.2A peak)(Ripple < 87.2mV)
+VGA_CORE
C7080 *1U/10V_4 C7081 *1U/10V_4 C7276 *1U/10V_4 C7245 *1U/10V_4 C7084 *1U/10V_4 C7244 *1U/10V_4 C7246 *1U/10V_4 C7094 *10U/6.3V_6
C7264 *1U/10V_4 C7243 *2.2U/6.3V_4 C7077 *1U/10V_4 C7295 *10U/6.3V_6 C7079 *1U/10V_4 C7230 *1U/10V_4 C7232 *1U/10V_4 C7256 *330U_2.5V_3528
C7233 *1U/10V_4 C7242 *2.2U/6.3V_4 C7231 *1U/10V_4 C7083 *1U/10V_4 C7082 *1U/10V_4 C7215 *1U/10V_4
C7096 *10U/6.3V_6 C7101 *10U/6.3V_6 C7092 *10U/6.3V_6 C7093 *10U/6.3V_6 C7098 *10U/6.3V_6 C7095 *10U/6.3V_6

Note1.
BIF_VDDC Ra R7136 *0_4 +VGA_CORE
SI , add R117 for disable BACO

0.95V~1.1V(2A VDDCI)
+VDDCI L7018 *0_8/S +VGA_CORE
C7285 *1U/10V_4 C7287 *1U/10V_4 C7286 *1U/10V_4 C7284 *10U/6.3V_6 C7292 *10U/6.3V_6 C7281 *10U/6.3V_6

BACO

PX_MODE R7378 *0_4 PX_MODE1
39 PX_MODE1 Q7013B PX_EN *2N7002DW-7-F
+3V R7166 *10K_4 PX_MODE 38
3,9,29 ECPWROK
Q7013A PX_EN 17 R7160 *2N7002DW-7-F *5.1K

SI , BACO circuit change to reserve only

+3V R7381 *100K/F_4 Q7026B *2N7002DW-7-F
Q7026A *2N7002DW-7-F
39 VGA_PWROK PX_MODE
+3V C7326 *0.1U/10V/X7R_4 BACO_EN U7008 *TC7SH08FU

+5V R7141 *1K_4 Q7010A *2N7002DW-7-F
R7142 *1K_4 PX_EN## PX_EN# Q7010B *2N7002DW-7-F

Note1.
1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

+1.0V_VGA Q7012 *AO3416 Q7022 *AO3416 PX_EN#
+VGA_CORE Q7008 *AO3416 Q7009 *AO3416 PX_EN##
BIF_VDDC C7550 *10U/6.3VS_6 C7557 *2.2U/6.3V_4 C7570 *10U/6.3VS_6 C7566 *2.2U/6.3V_4
C7563 *22U/6.3VS_8

NB5/RD2

PROJECT : R52
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SEYMOUR-XT_Power_and_NC	1A

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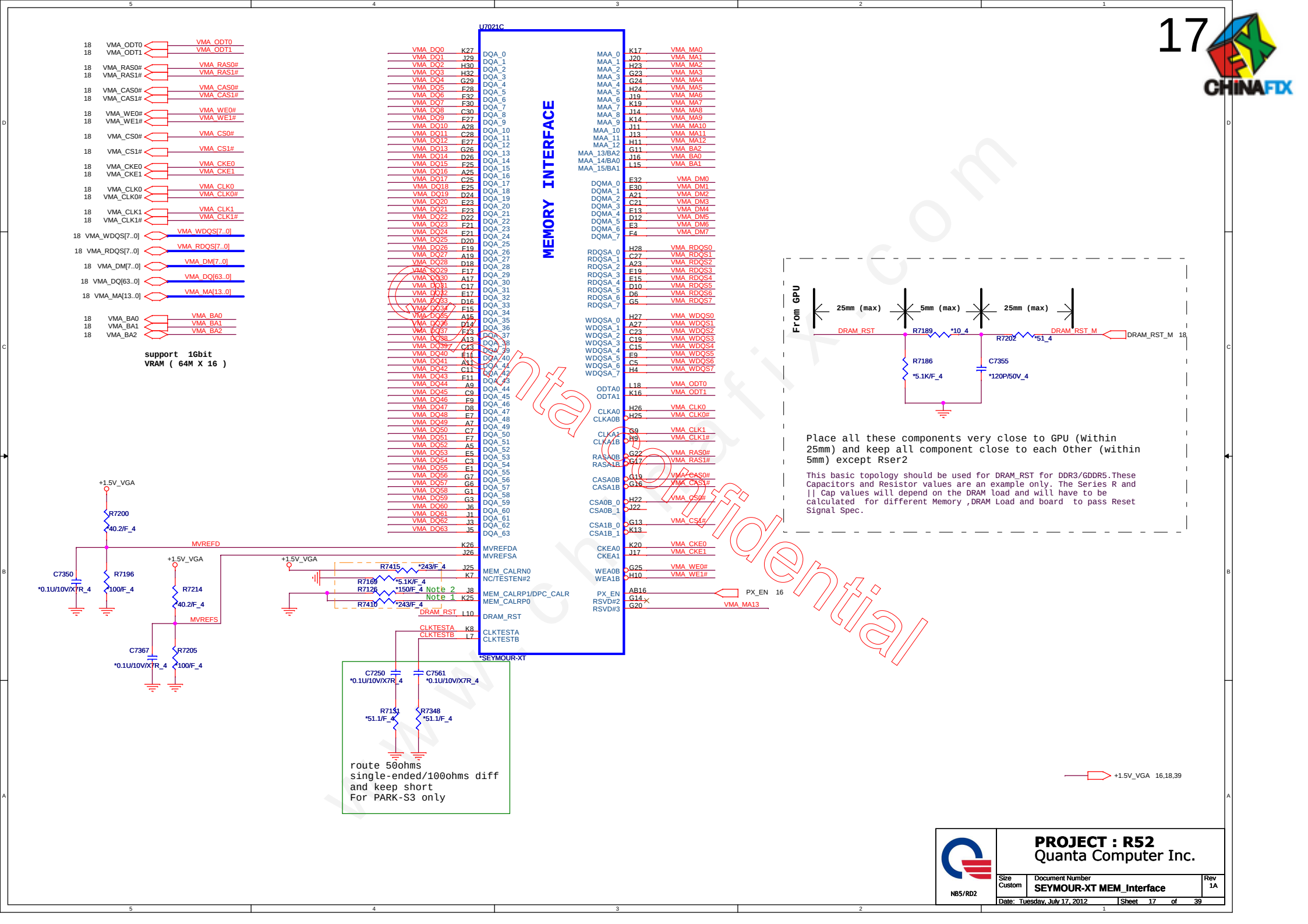
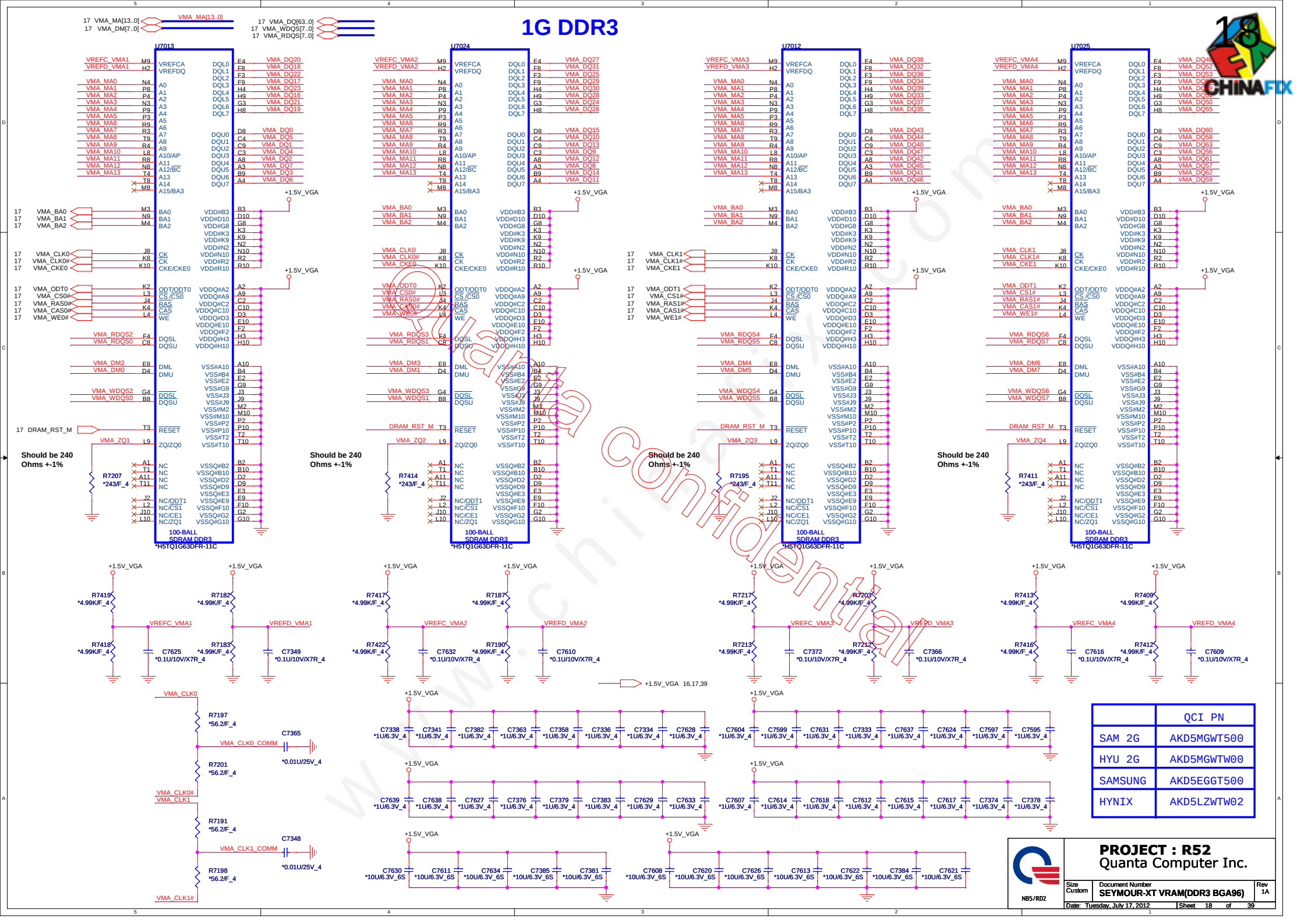


NB5/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: SEYMOUR-XT MEM_Interface	Rev: 1A
Date: Tuesday, July 17, 2012	Sheet 17 of 39	

1G DDR3



	QCI PN
SAM 2G	AKD5MGWT500
HYU 2G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZWTW02

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	SEYMOUR-XT VRAM(DDR3 BGA96)	1A

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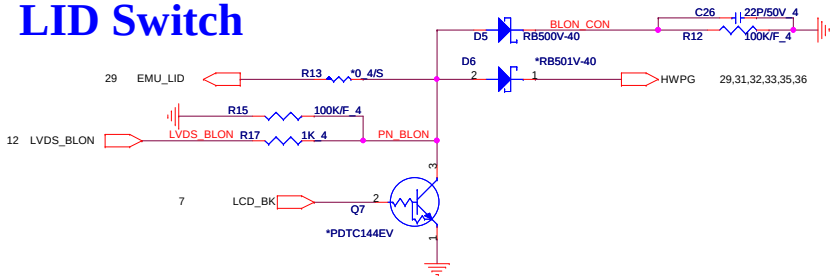
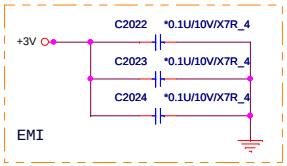
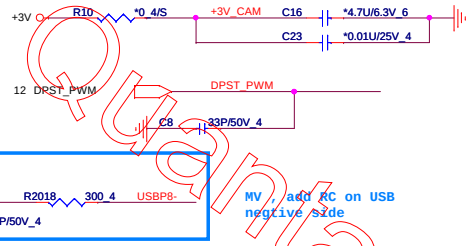
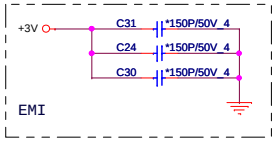
NB5/RD2

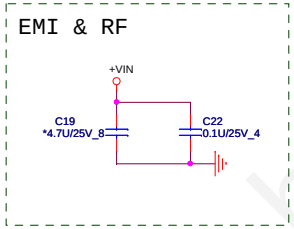
LID Switch

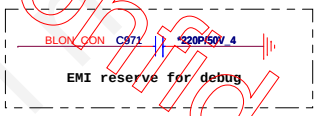


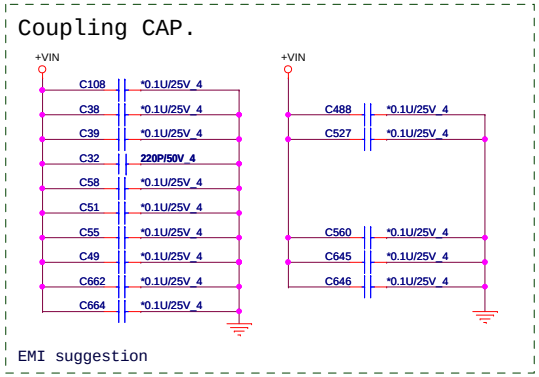


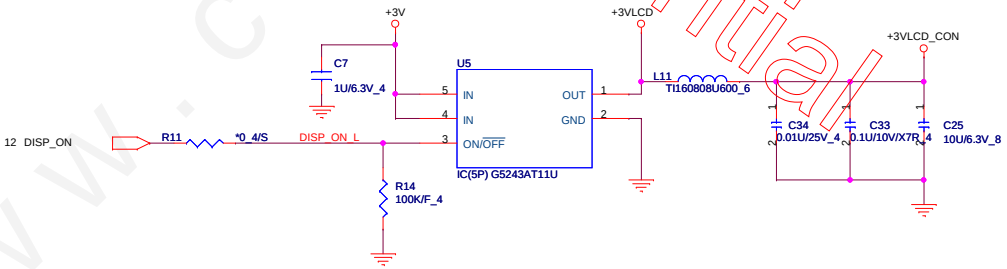


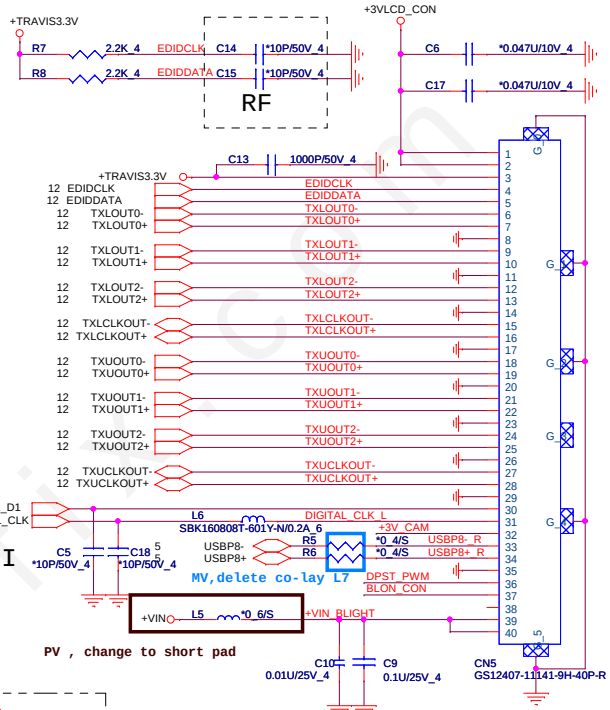












6,26,29,30,31 +3VPCU
3,4,5,7,8,9,10,11,12,13,16,20,21,22,23,24,25,26,27,28,29,34,37,38,39 +3V
30,37,39 +12VALW
30,31,32,33,34,36,37,38,39 +VIN

N85/RD2

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Quanta Computer Inc.

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Custom	LCD CONN/LID/CAM	1A
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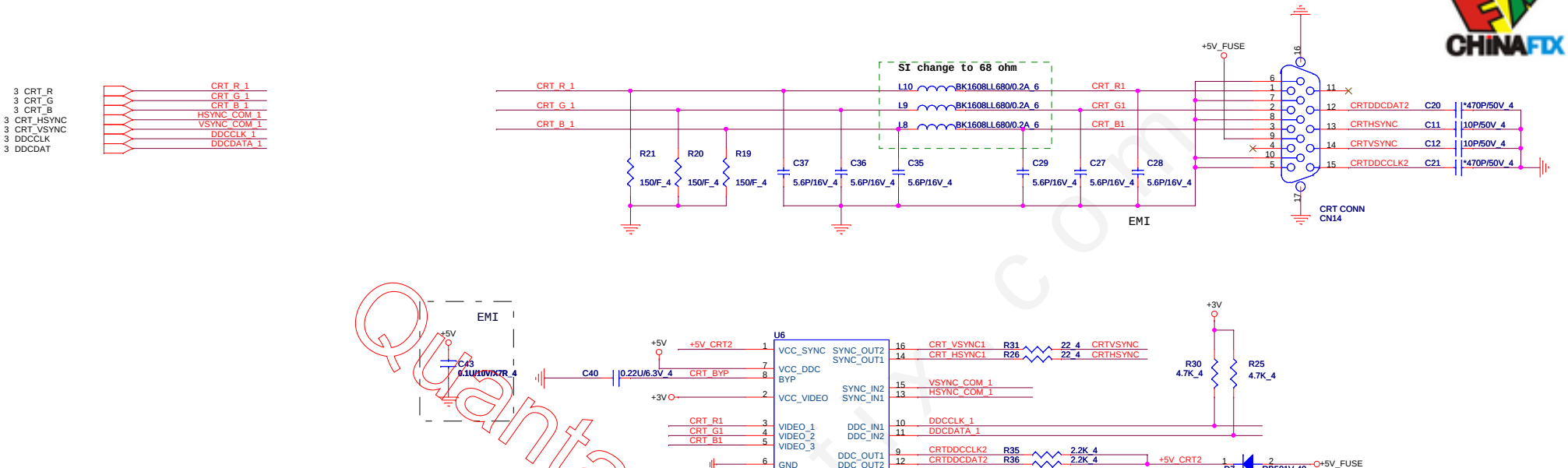
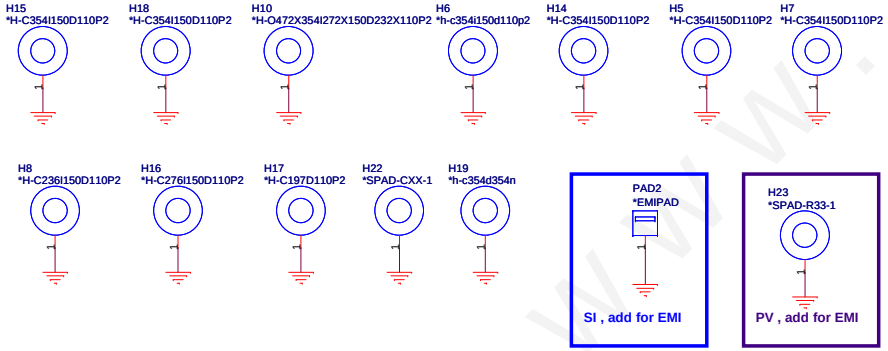
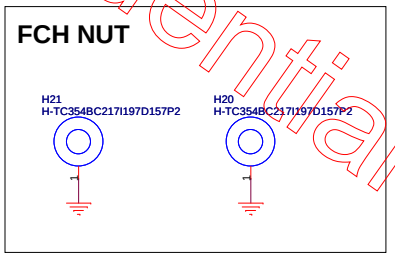
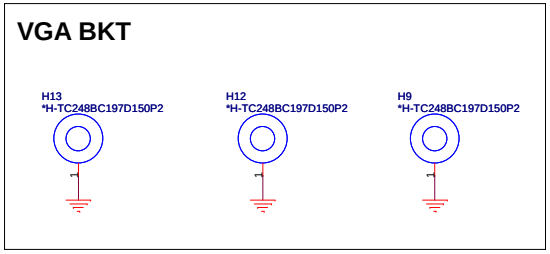
CRT PORT

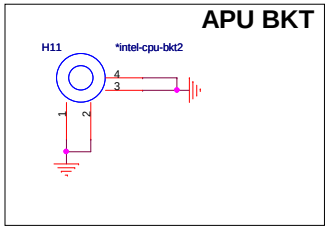


HOLE









N85/RD2	**PROJECT : R52** Quanta Computer Inc.	
Size: Custom	Document Number: **CRT,Hole**	Rev: 1A
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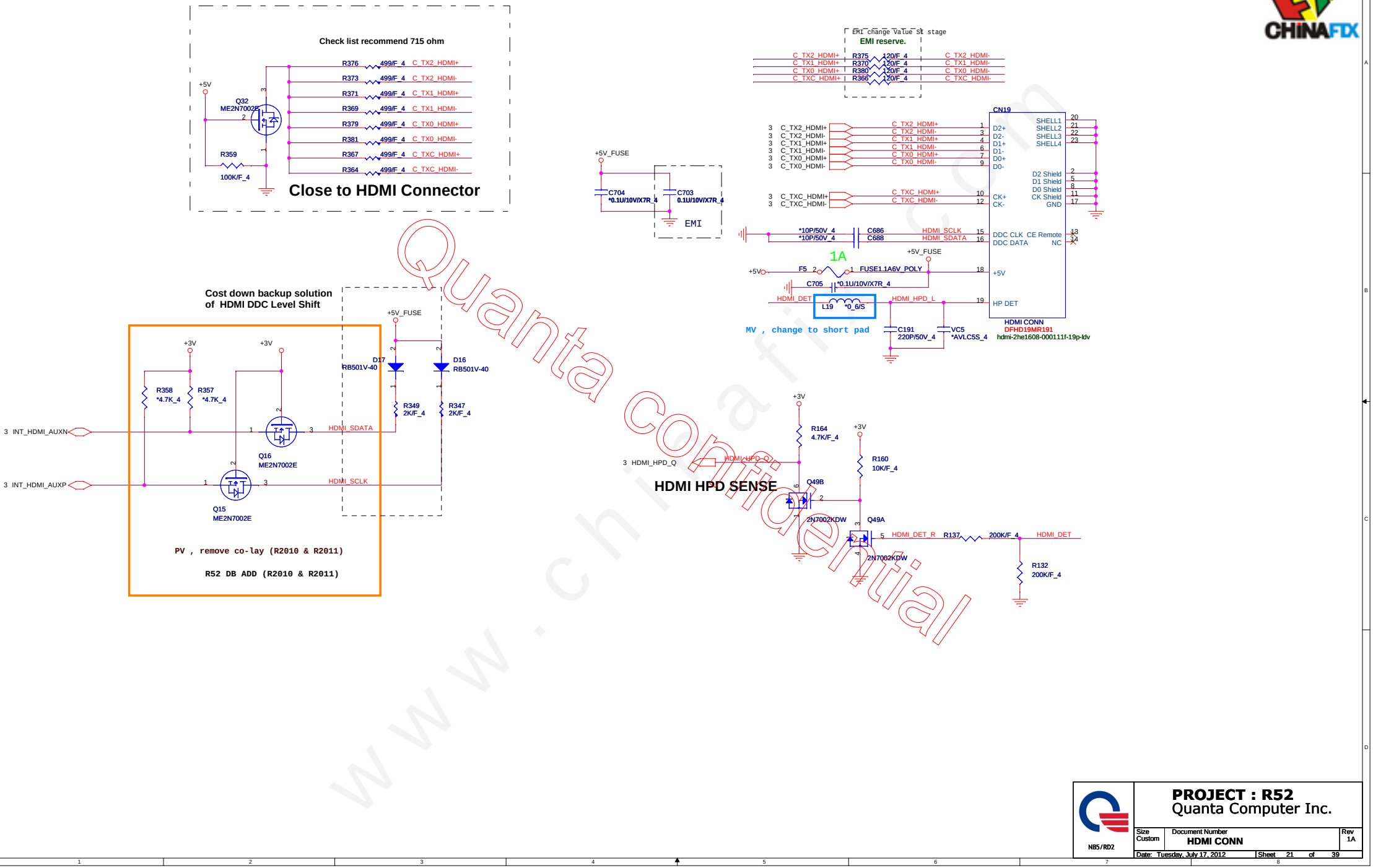
HDMI PORT



N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: HDMI CONN	Rev: 1A
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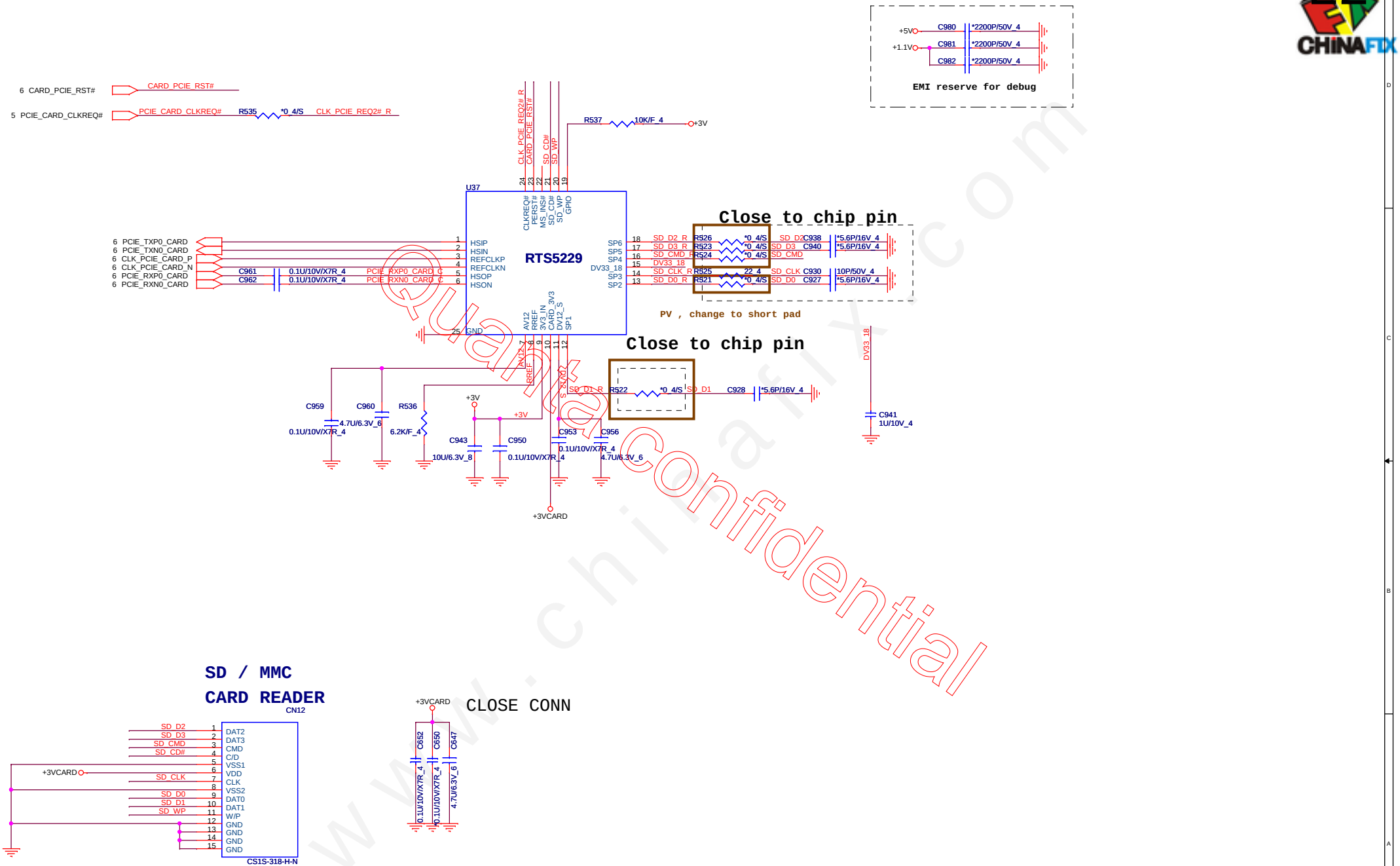

NB5/RD2	PROJECT : R52 Quanta Computer Inc.	
	Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE — Rev: 1A
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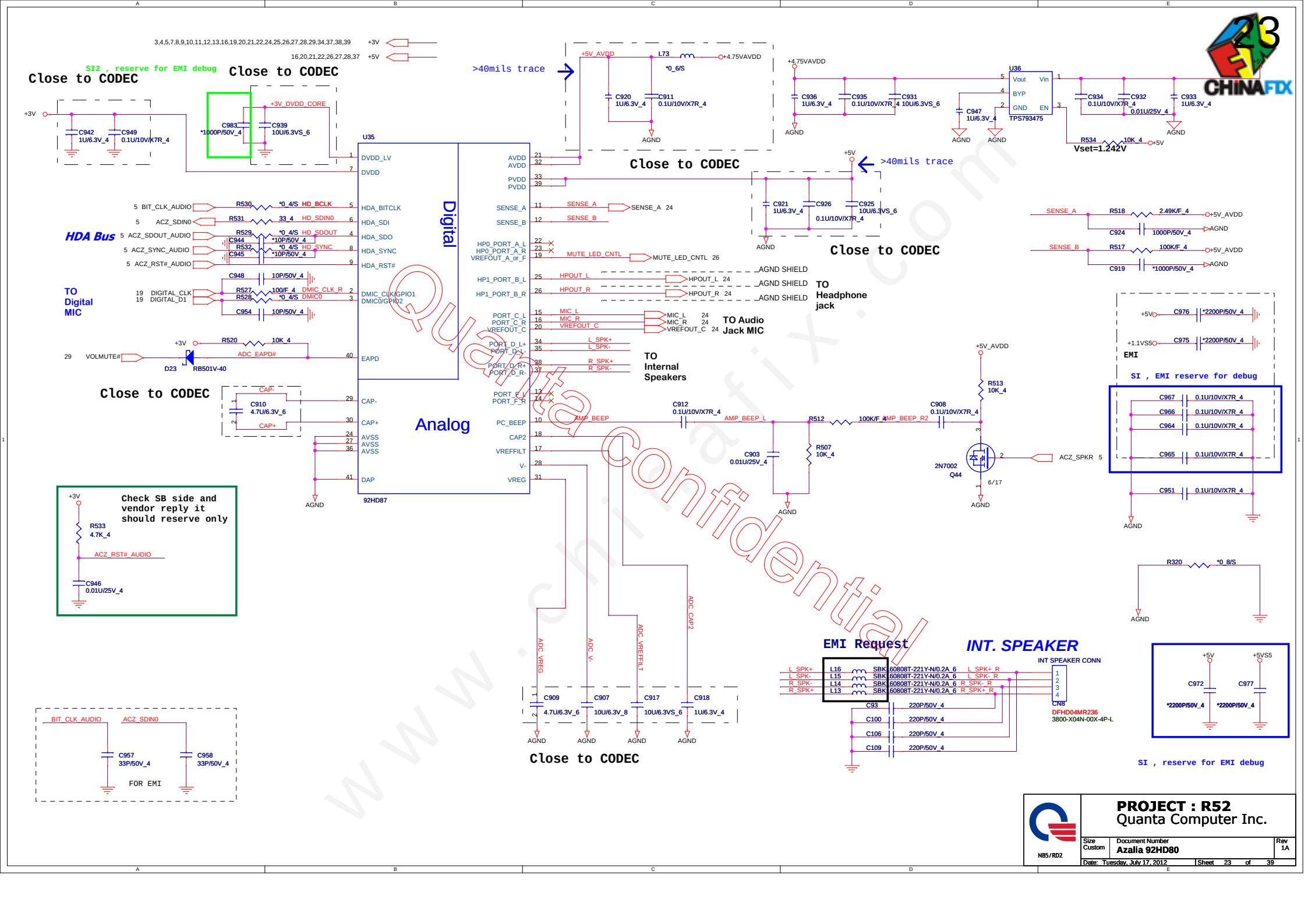
Close to CODEC
SI2 , reserve for EMI debug
>40mils trace
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Digital
Analog
U35
92HD87
Check SB side and vendor reply it should reserve only
EMI Request
INT. SPEAKER
INT SPEAKER CONN
FOR EMI
SI , EMI reserve for debug
SI , reserve for EMI debug
Vset=1.242V
PROJECT : R52
Quanta Computer Inc.
Azalia 92HD80
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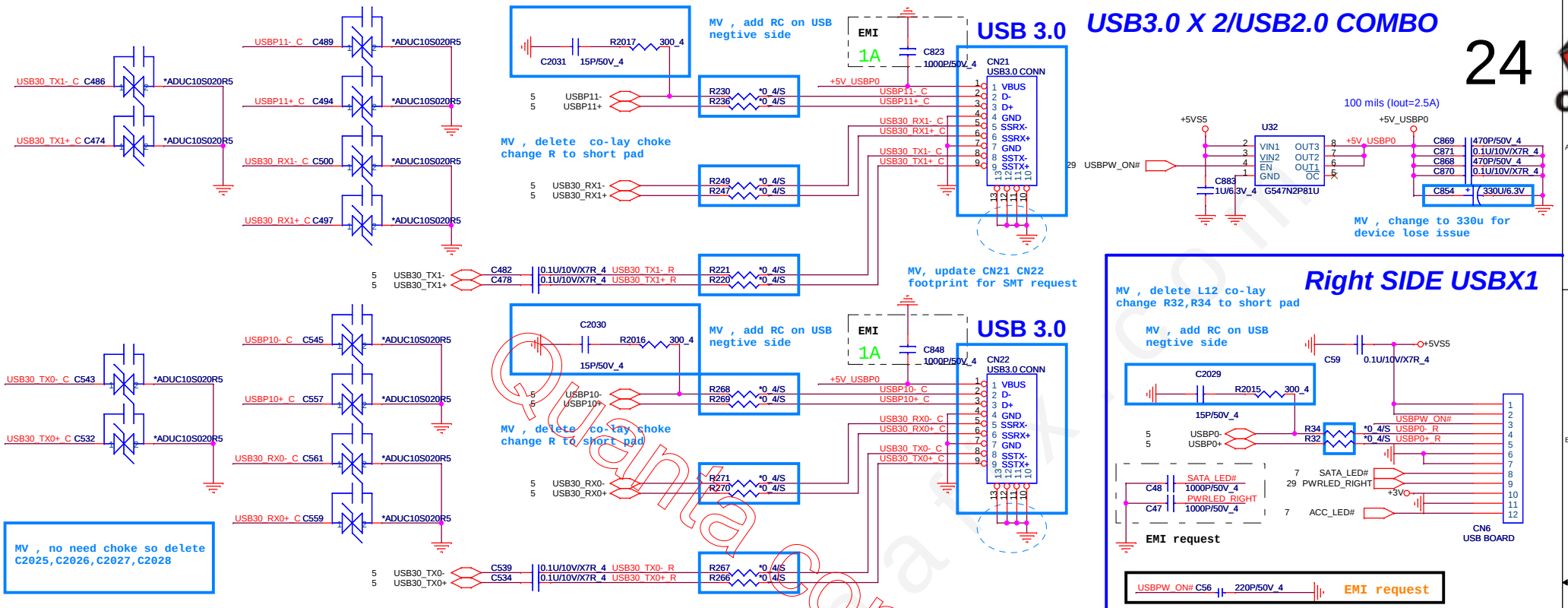
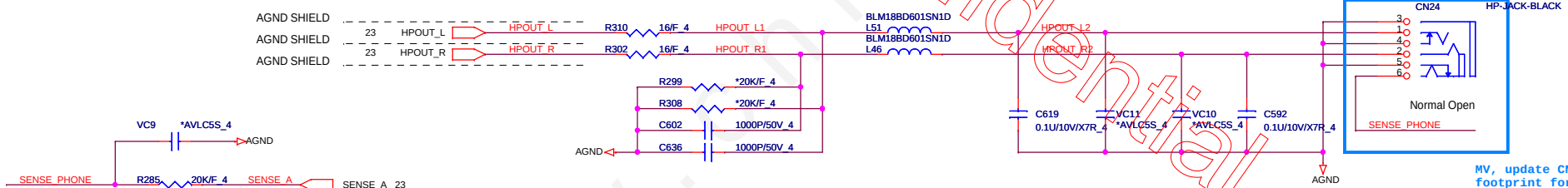
USB3.0 X 2/USB2.0 COMBO

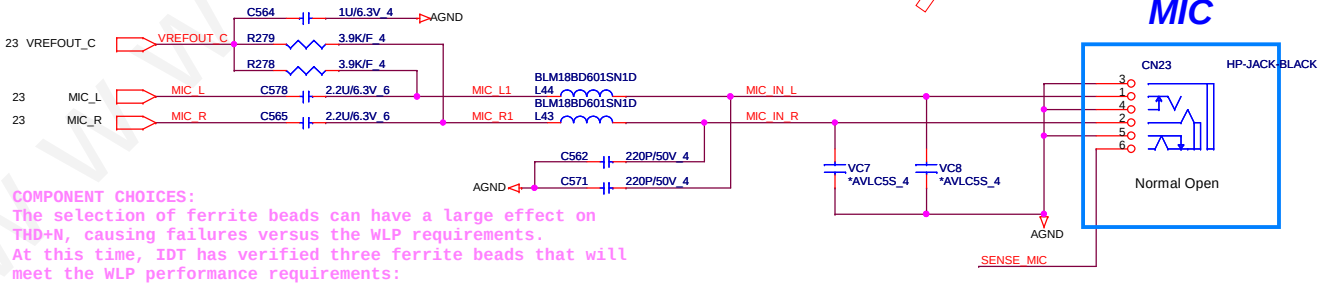


Right SIDE USBX1

Line out



MIC



COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

NB5/RD2	PROJECT : R52 Quanta Computer Inc.	
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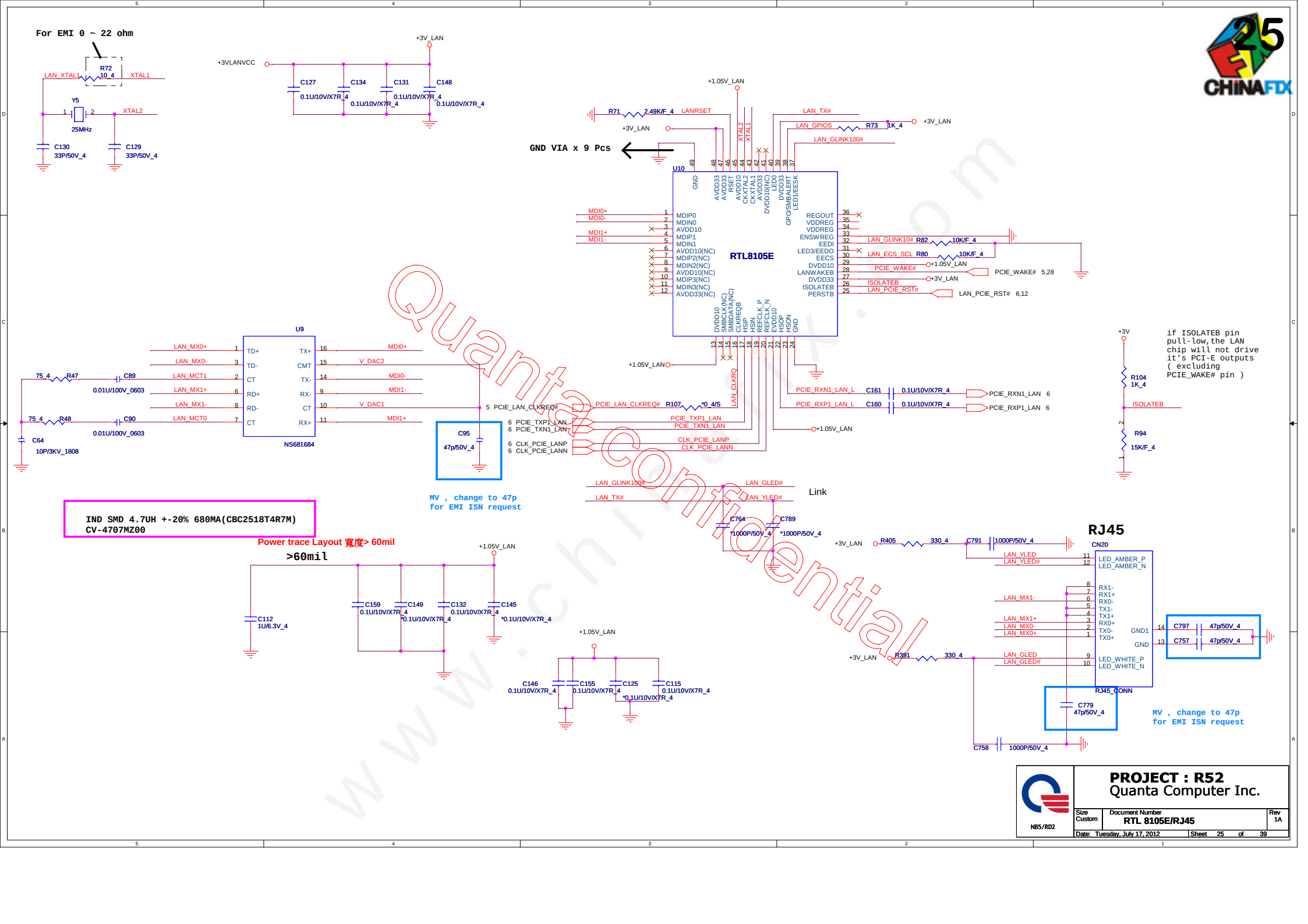
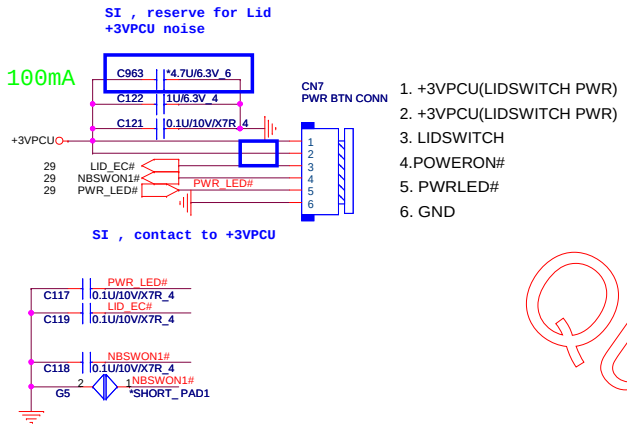
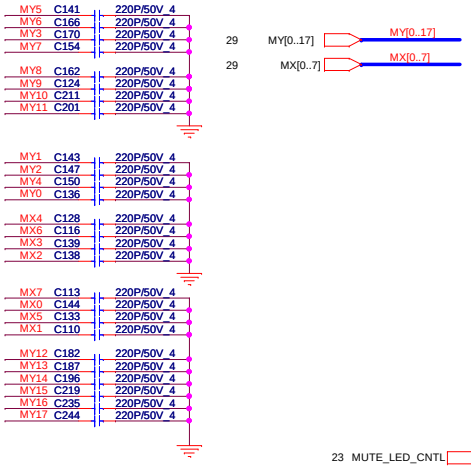


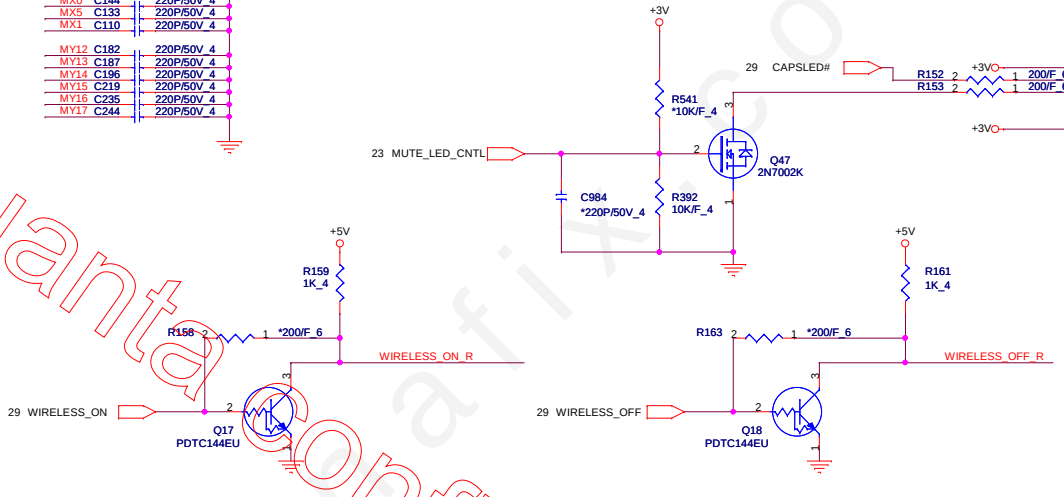
POWER BOTTON CONNECT



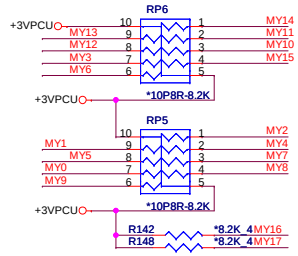
1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



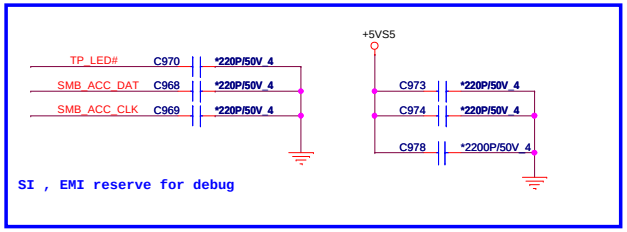
KEYBOARD Con.



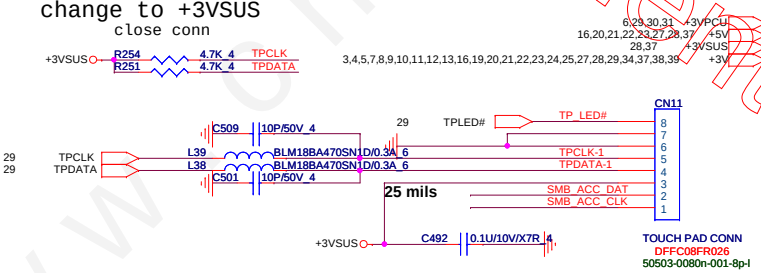
KEYBOARD PULL-UP

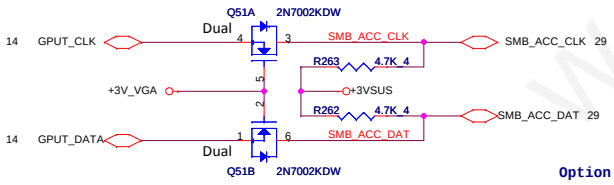


TOUCH PAD Con.

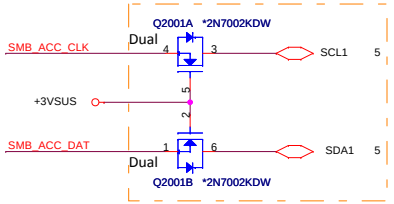


change to +3VSUS
close conn





Option Q51 or Q2001



N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size Custom	Document Number KB/SW/TP	Rev 1A
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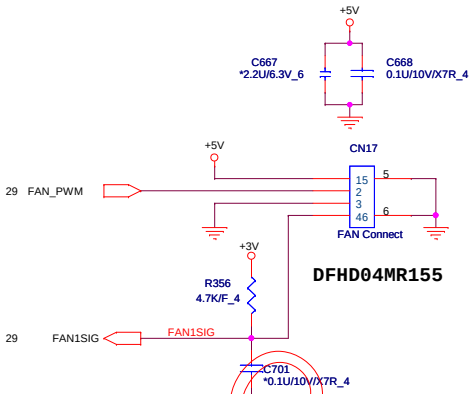
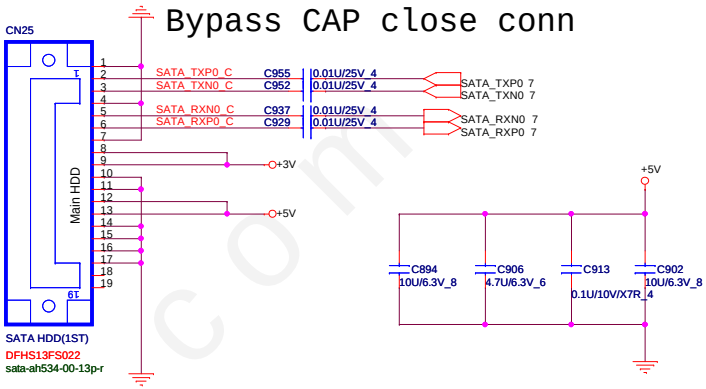
CPU FAN

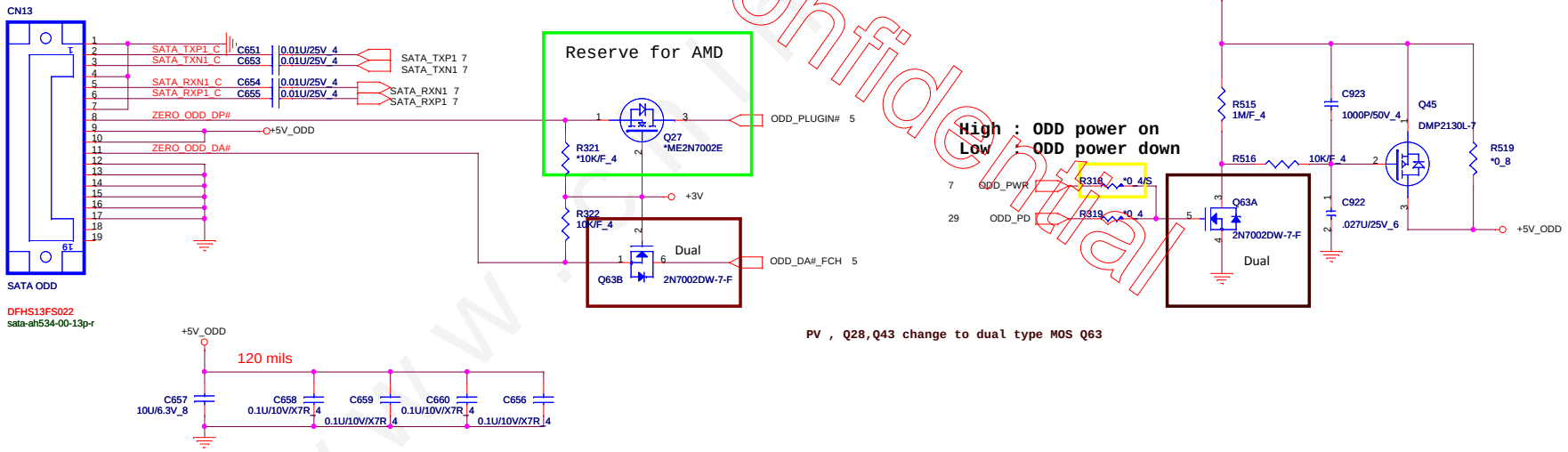


SATA HDD CONNECTOR



SATA ODD CONNECTOR

SATA ODD



PV , Q28,Q43 change to dual type MOS Q63

N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
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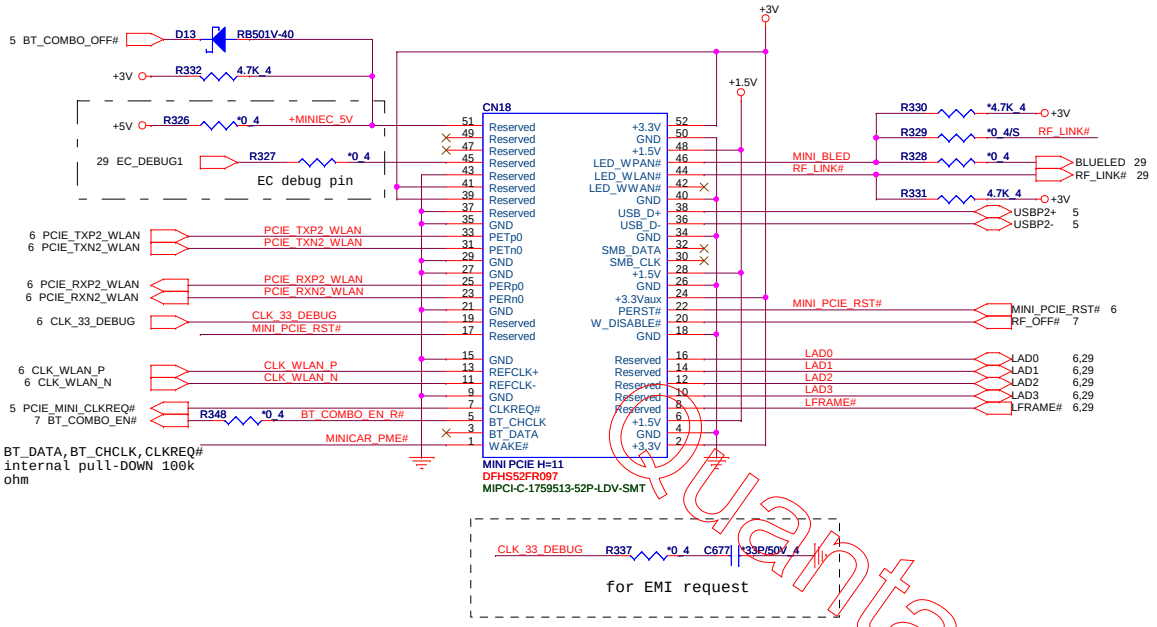
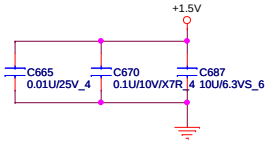
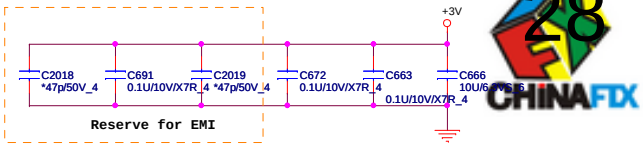
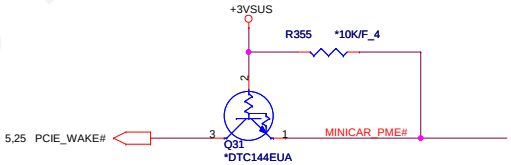
Mini PCI-E Card 1 WLAN







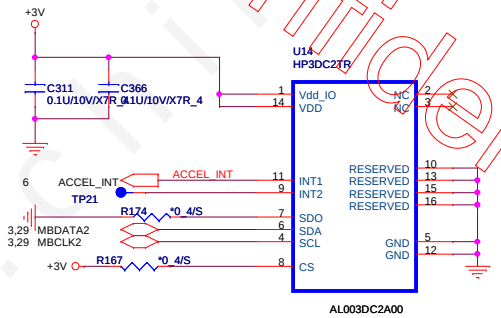
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm



CLK_33_DEBUG R337 *0_4 C677 *33P/50V_4
for EMI request

37 +1.5V
3,4,5,7,8,9,10,11,12,13,16,19,20,21,22,23,24,25,26,27,29,34,37,38,39 +3V
6,26,29,30,31 +3VPCU
16,20,21,22,23,26,27,37 +5V

Accelerometer Sensor



N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE & G-sensor	Rev: 1A
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ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

Smart adapter Type check

Change to 1SS355 as Current loss

D18 1SS355

Change to RB500 as Current loss

SI , del QB button PU resistor R392

For +VIN noise

Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

4M SPI EC ROM

U20 EN25Q32B-104HIP AKE39ZN0Q02 SOIC8-8-1_27

128K byte SPI EC ROM

U19 *DFHS08FS023 SOIC8-6-1_27

ICT need TP2675 size test point

TP place on top lay for ICT request

Adapter select

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

IT8518E/HX

AJ085180F04

IT8518_AGND

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Quanta Computer Inc.

N85/RD2

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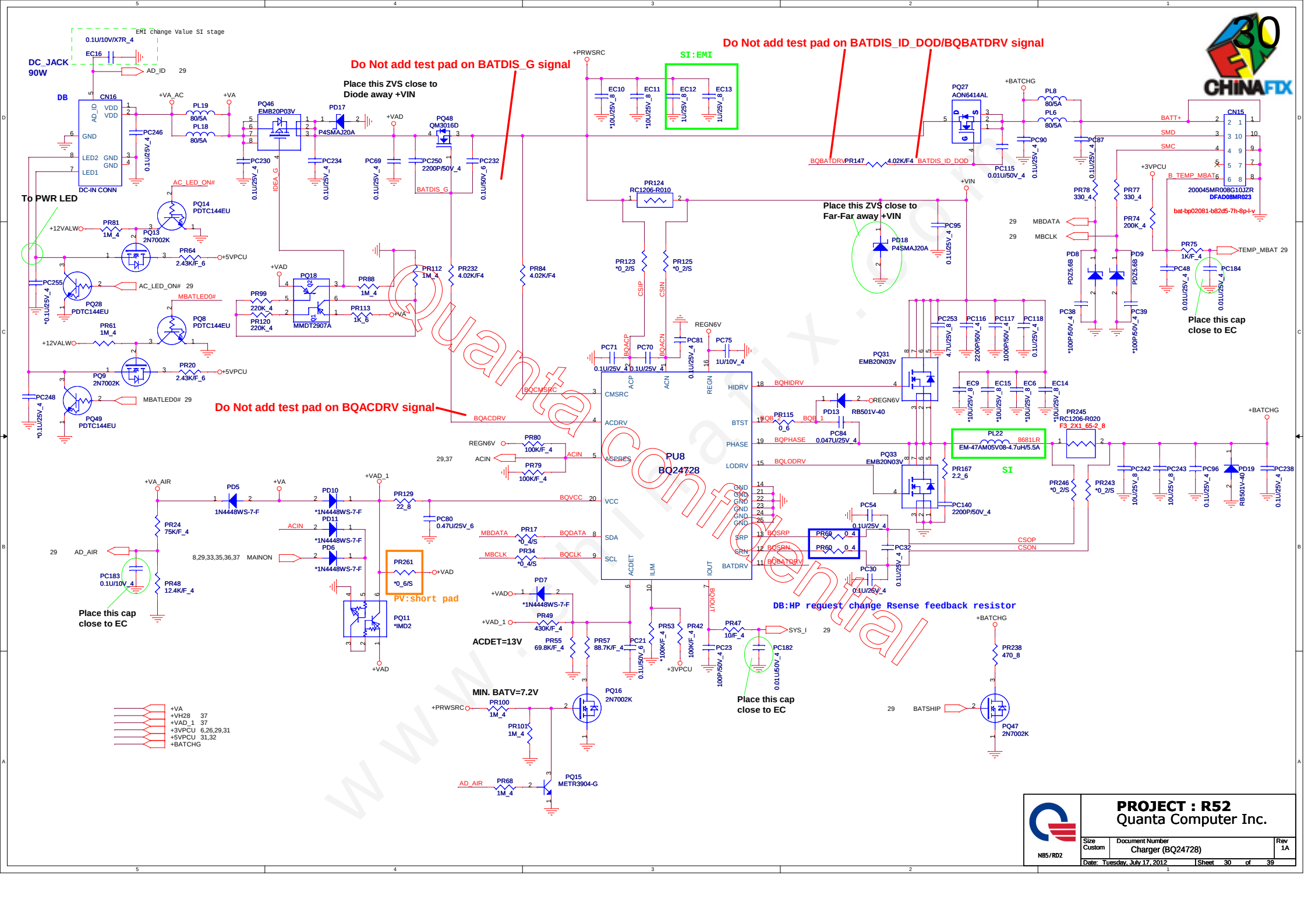
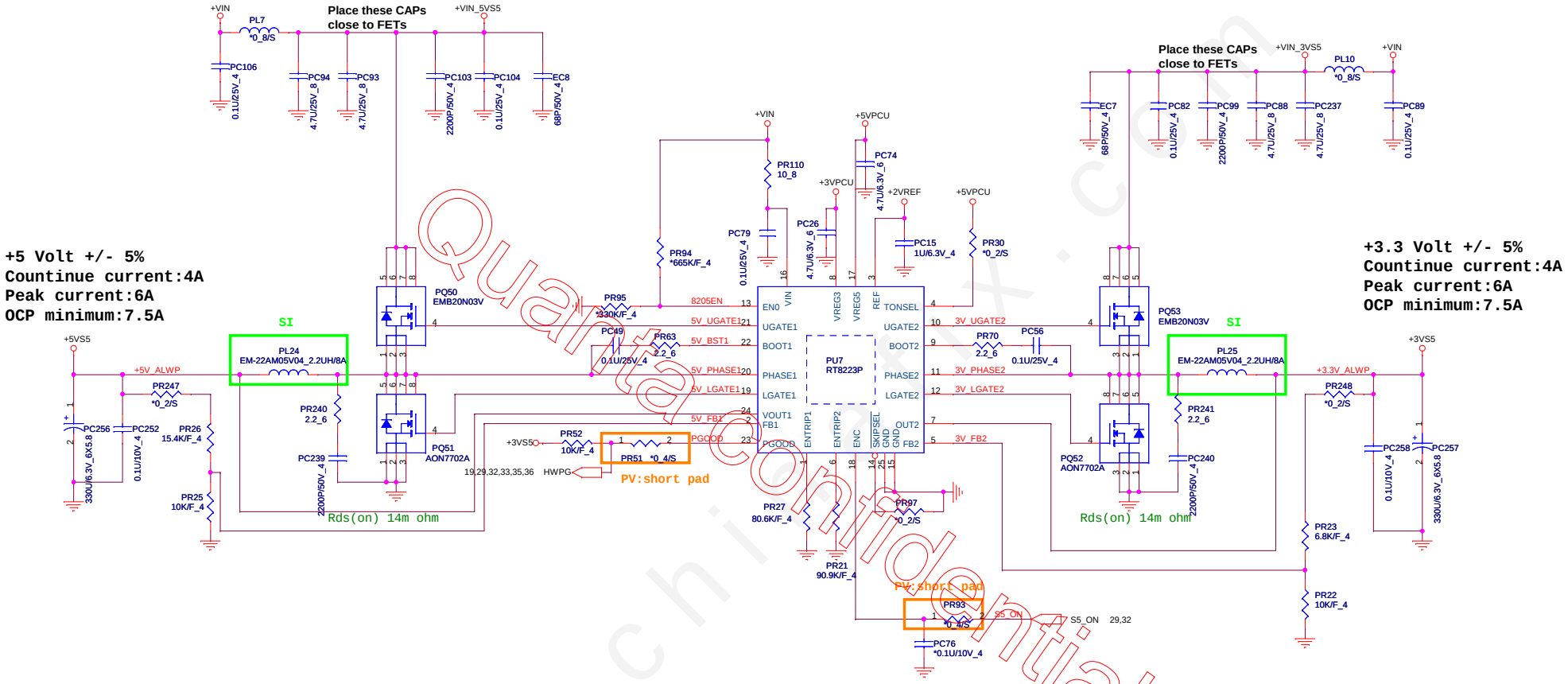

DC_JACK 90W
DB
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Do Not add test pad on BATDIS_ID_DOD/BQBATDRV signal
Do Not add test pad on BQACDRV signal
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
SI:EMI
SI
PU8
BQ24728
PV:short pad
DB:HP request change Rsense feedback resistor
ACDET=13V
MIN. BATV=7.2V
Quanta Confidential
www.chinafix.com
PROJECT : R52
Quanta Computer Inc.
N85/RD2
Charger (BQ24728)
Tuesday, July 17, 2012

DC/DC +3VS5/+5VS5



N85/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(TPS51123A)	Rev: 1A
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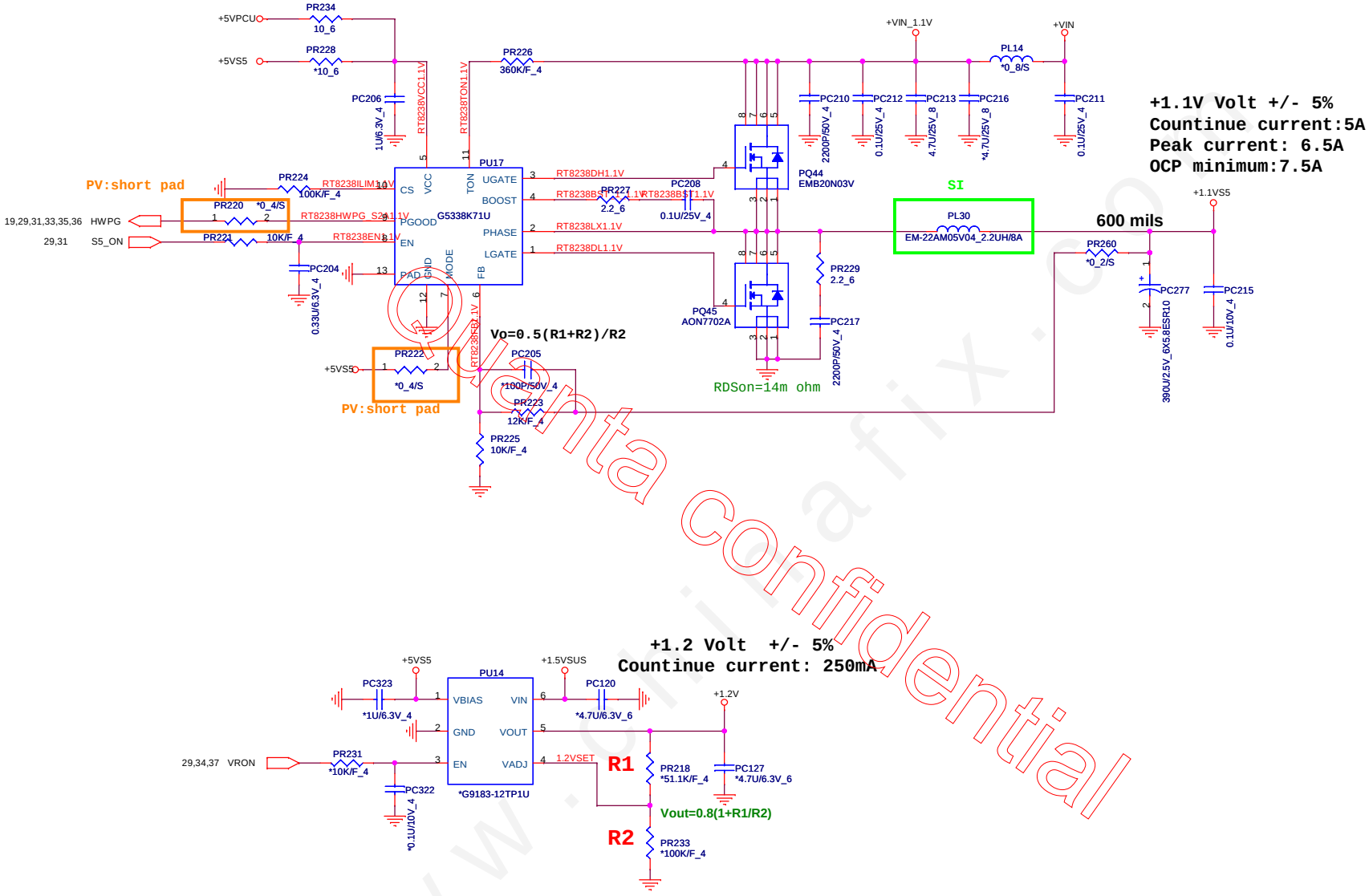
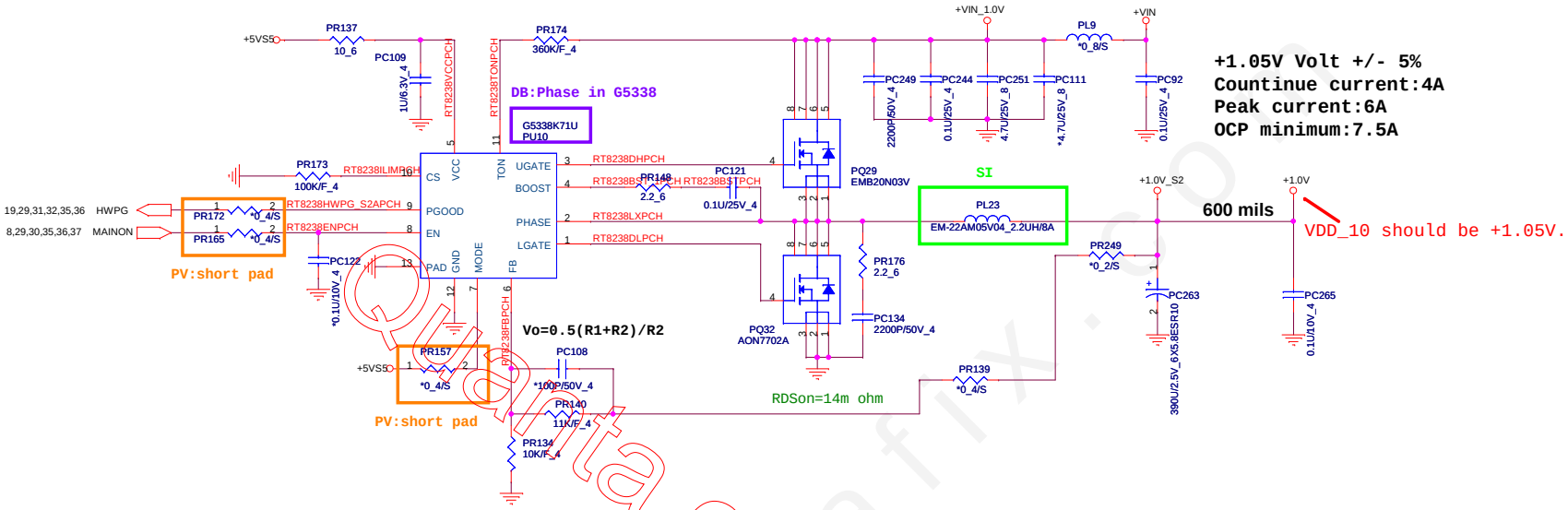
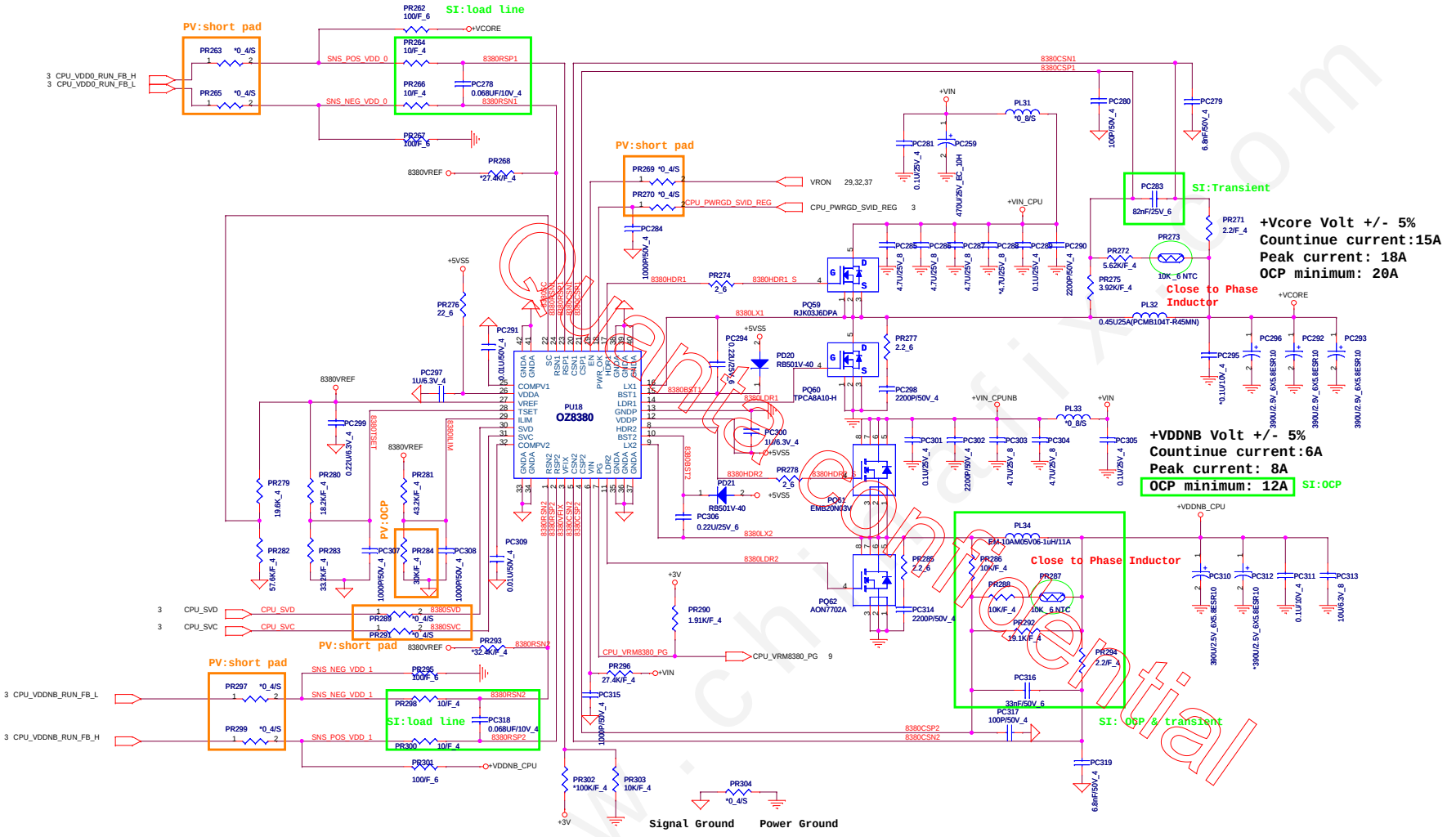


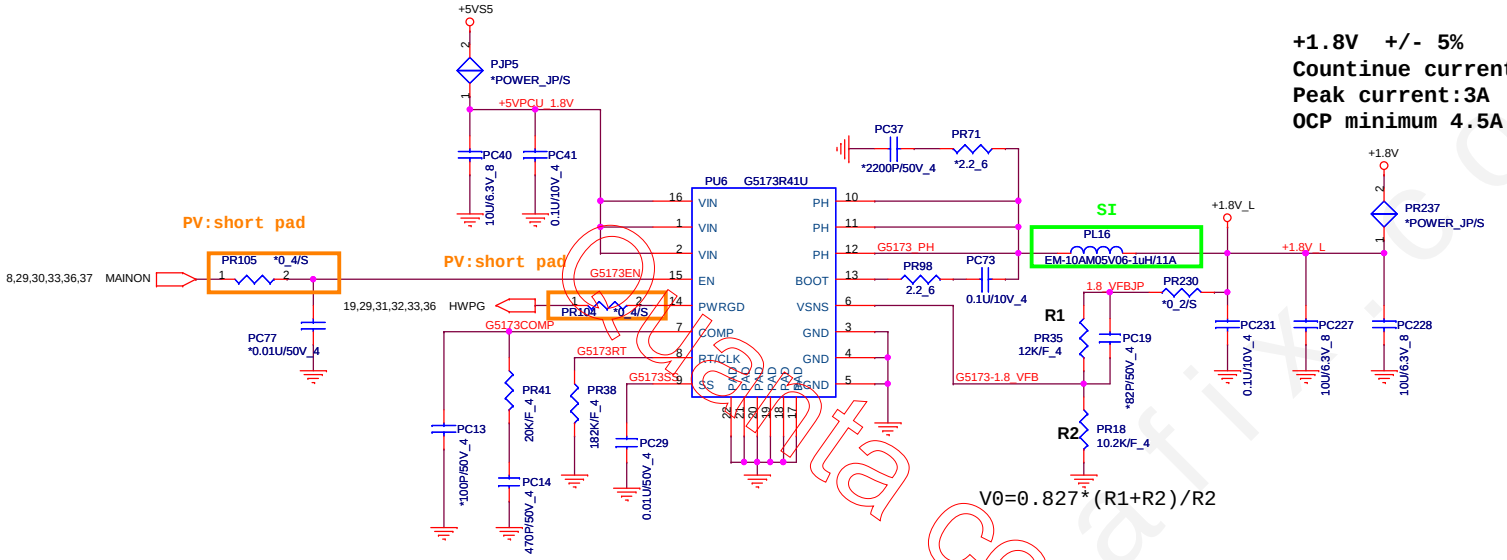
NB5/RD2	PROJECT : R52 Quanta Computer Inc.	
Size: Custom	Document Number: +1.1VS5 (RT8228)	Rev: 1A
Date: Tuesday, July 17, 2012	Sheet 32 of 39	



NB5/RD2	**PROJECT : R52** Quanta Computer Inc.	
Size: Custom	Document Number: +1.0V (RT8228)	Rev: 1A
Date: Tuesday, July 17, 2012	Sheet 33 of 39	



NB5/RD2	PROJECT : R52 Quanta Computer Inc.	
Size C	Document Number +VCORE (OZ8380)	Rev 1A
Date: Tuesday, July 17, 2012	Sheet 34 of 39	



+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

V0=0.827*(R1+R2)/R2

NB5/RD2	**PROJECT : R52** Quanta Computer Inc.	
Size: Custom	Document Number: +1.8V (G5173)	Rev: 1A
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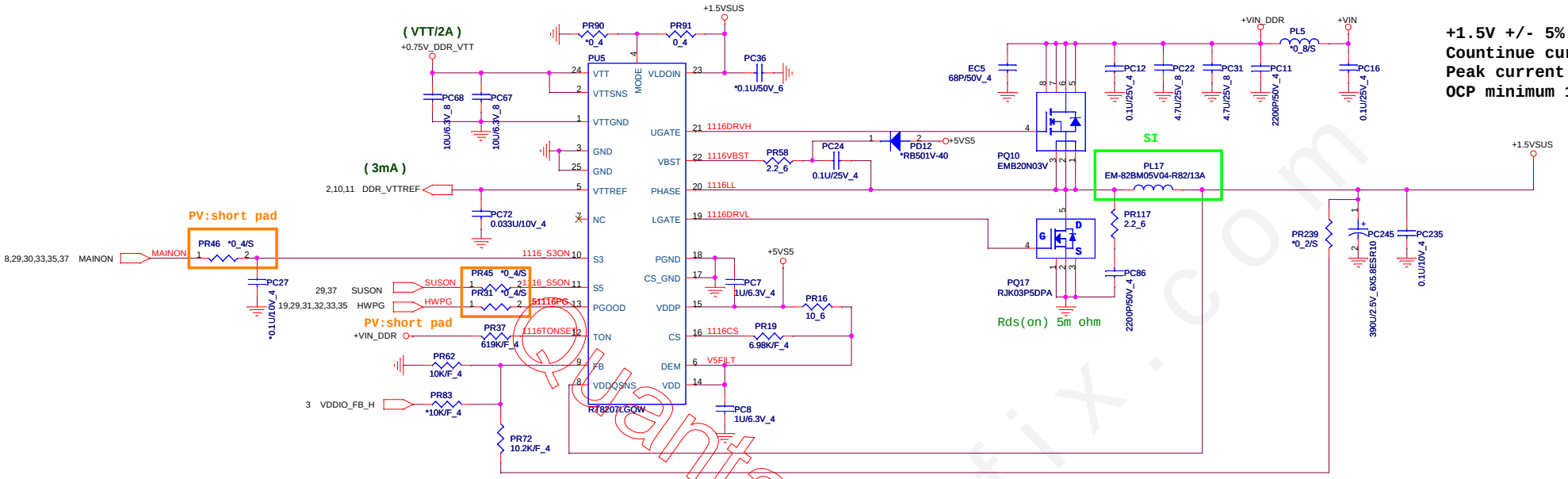

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

PROJECT : R52 Quanta Computer Inc.		
Size: Custom	Document Number: DDRIII(G5616)	Rev: 1A
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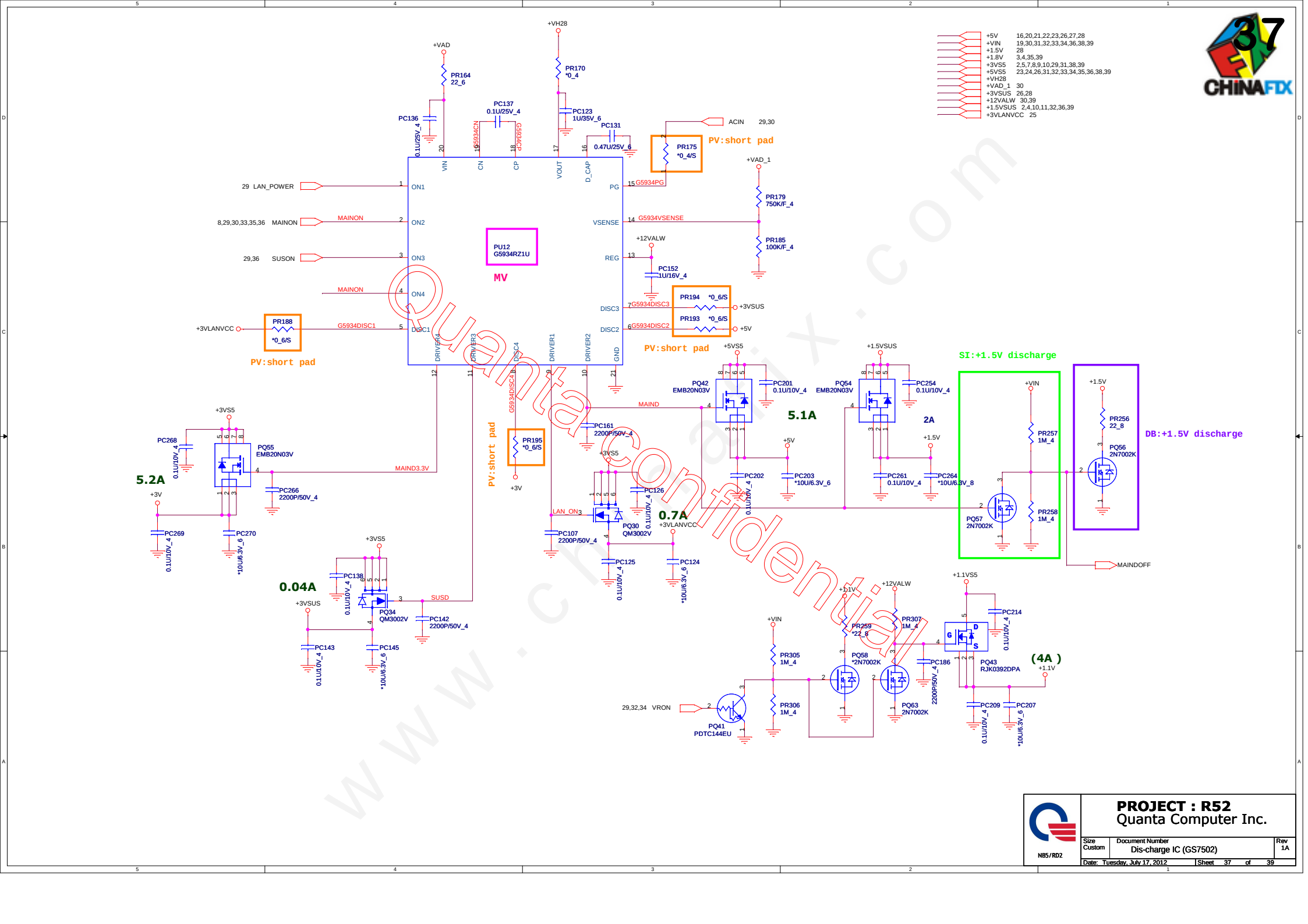
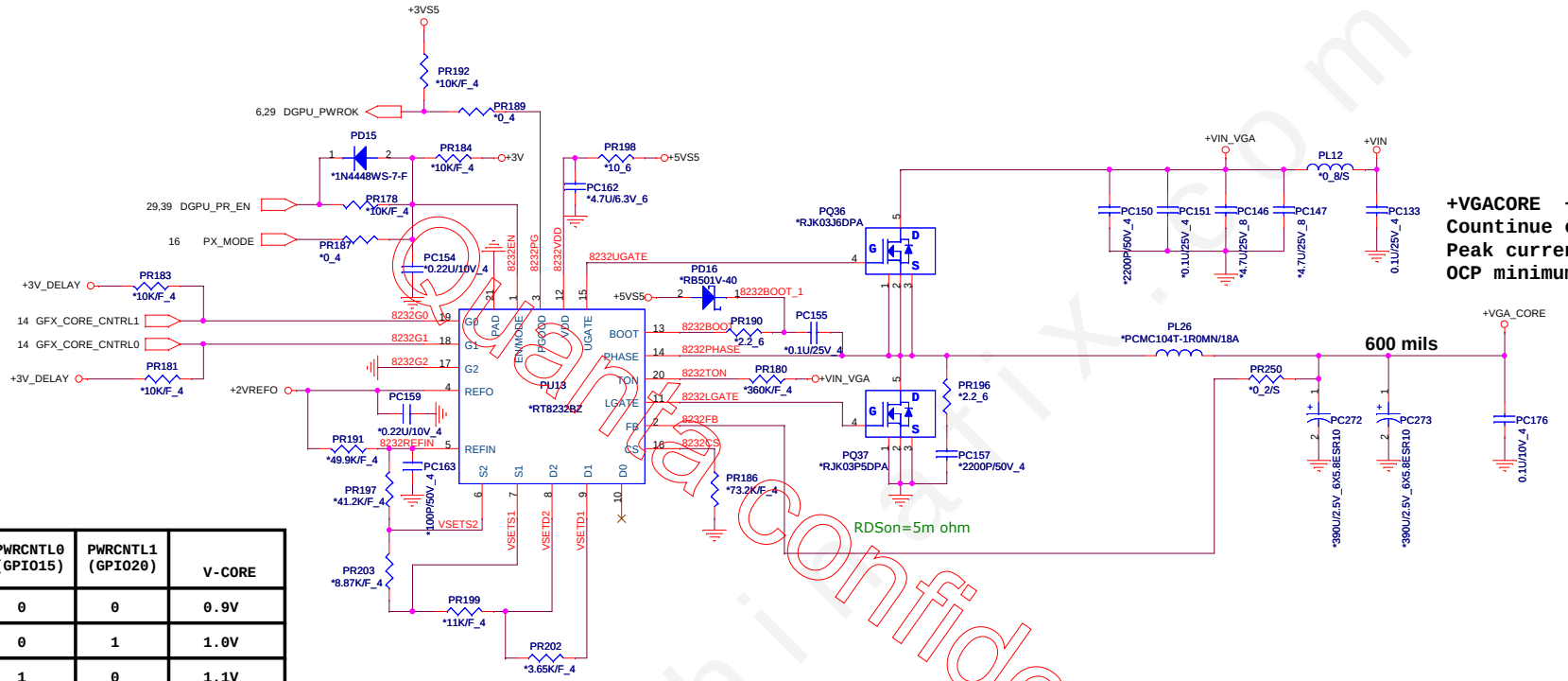
NB5/RD2



VGA Core



+VGACORE +/- 5%
Countinue current:10.5A
Peak current:11.5A
OCP minimum 16A

Symour-LP	PWRCNTL0 (GPIO15)	PWRCNTL1 (GPIO20)	V-CORE
L	0	0	0.9V
M	0	1	1.0V
H	1	0	1.1V
TBD	1	1	NA

PROJECT : R52
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8232AZ)	1A

N85/RD2

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