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IH61W-MHS

REV 8.0

CPU:

Intel Sandy/Ivy Bridge processors in LGA1155 Package 95W

System Chipset:

Cugar Point H61

Main Memory:

Dual Channel/DDR- III* 2(Max 16GB) 1066/1333

DDR3- 1600 /1333 /1066 /800

Onboard Device:

Super I/O:IT8772E

LAN:Atheros AR8152

HD Codec:VIA VT1708S 3 jacks

Power solution:

CPU Voltage Regulators:2phase by ISL6363

AXG voltage Regulators:1phase by ISL6363

VTT voltage Regulators:1Phase by FP6326

DDR voltage Regulators:1Phase by FP6326

Expansion Slots:

PCI EXPRESS 16X SLOT* 1

PCI EXPRESS 1X SLOT* 1

REAR IO:

PS/2 KB/MS

VGA

2 layer USB2.0 Ports

2 layer USB2.0 + RJ- 45 Ports

Audio Jackets

Front I/O:

SATA2 * 4

USB Header * 2

CPU /System1

Front Audio Header

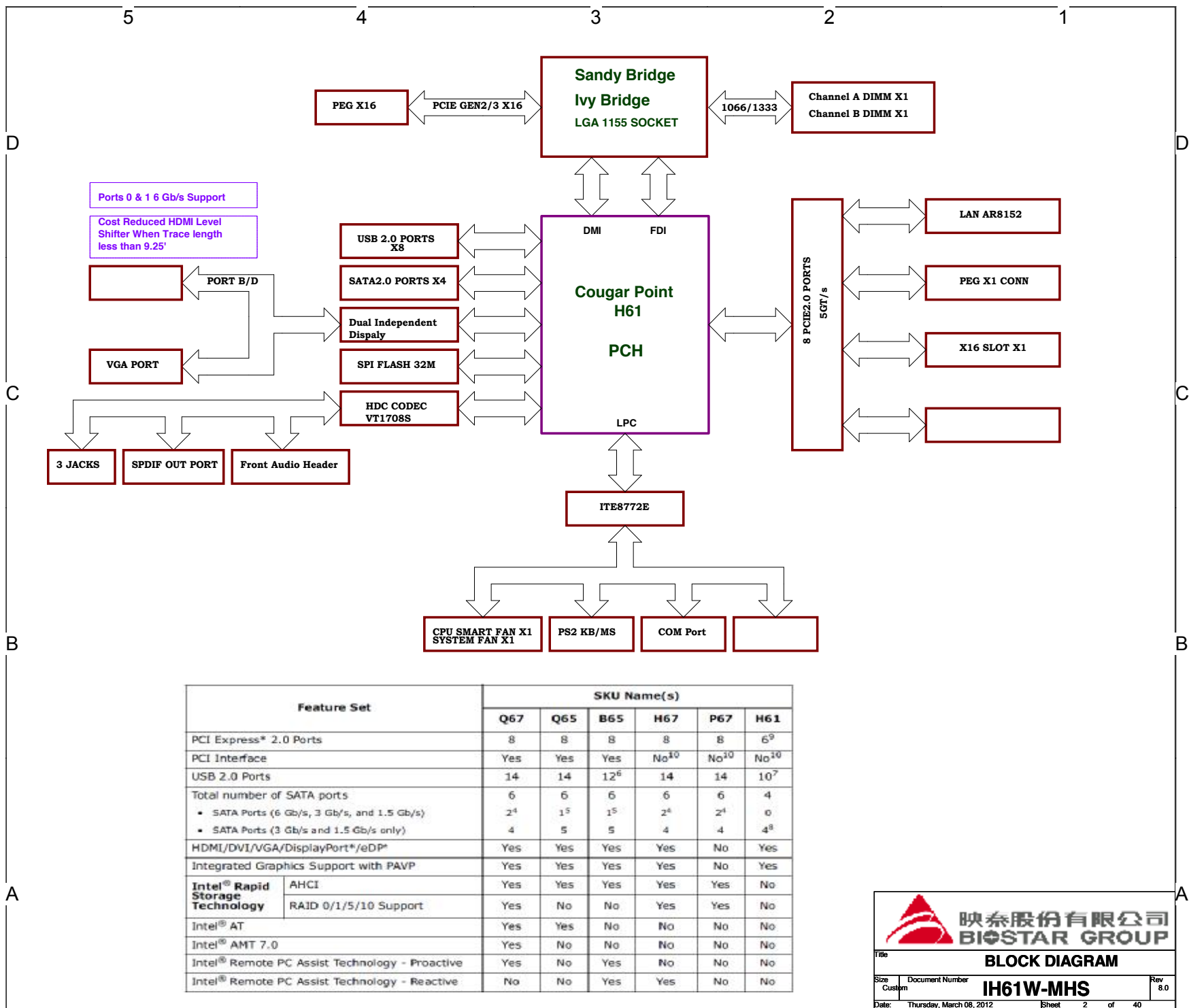
COM1



HW Engineer	ELI	Date	2011/ 03/ 08
HW Leader1	Cobra	Date	
HW Leader2	Belle	Date	

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BLOCK DIAGRAM

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Date: Thursday, March 08, 2012

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5

4

3

2

1

D

C

B

A

D

C

B

A

Change from IH61N-MHS 6.1:

- 1. Remove S3
- 2. Remove DVI
- 3. Remove PCI-E Slot
- 4 .Remove V_SA
- 5 .Remove Audio 12v to 5v
- 6 .Change PWM to UP1625Q
- 7 .Change LAN to RTL8105T

Change from 0.7


- 1.DDR3=1.525V
- 2.Change LAN to AR8152
- 3.Change Audio VCC to +5V_STBY
- 4.Change Logic VCC to +3v3_DUAL
- 5.Change 2N7002 to 3904 for Q27

Change from 0.71

- 1.Add Model Name
- 2.Fine tune Eup
- 3.Fine tune RTC
- 4.Change low noise CHOKE
- 5.Add CPU PWM NTC
- 6.Change DDR voltage to 1.52v
- 7.Change PCIE16X AC Coupling Capacitor to 0.1uF

Change from 7.0

- 1.Change ALC662 to VIA1708S
- 2.Change IT8728 to IT8772
- 3.Remove CPU PWM Input Choke
- 4.Remove CPU PWM Low Side Mosfet
- 5.Remove LPT Header
- 6.Change UP0105 to az1117 For 3VSB
- 7.Change PCH Voltage to 1.06V
- 8.Change +3V3_STBY to 3.26V

		
Title		
CHANGE LIST		
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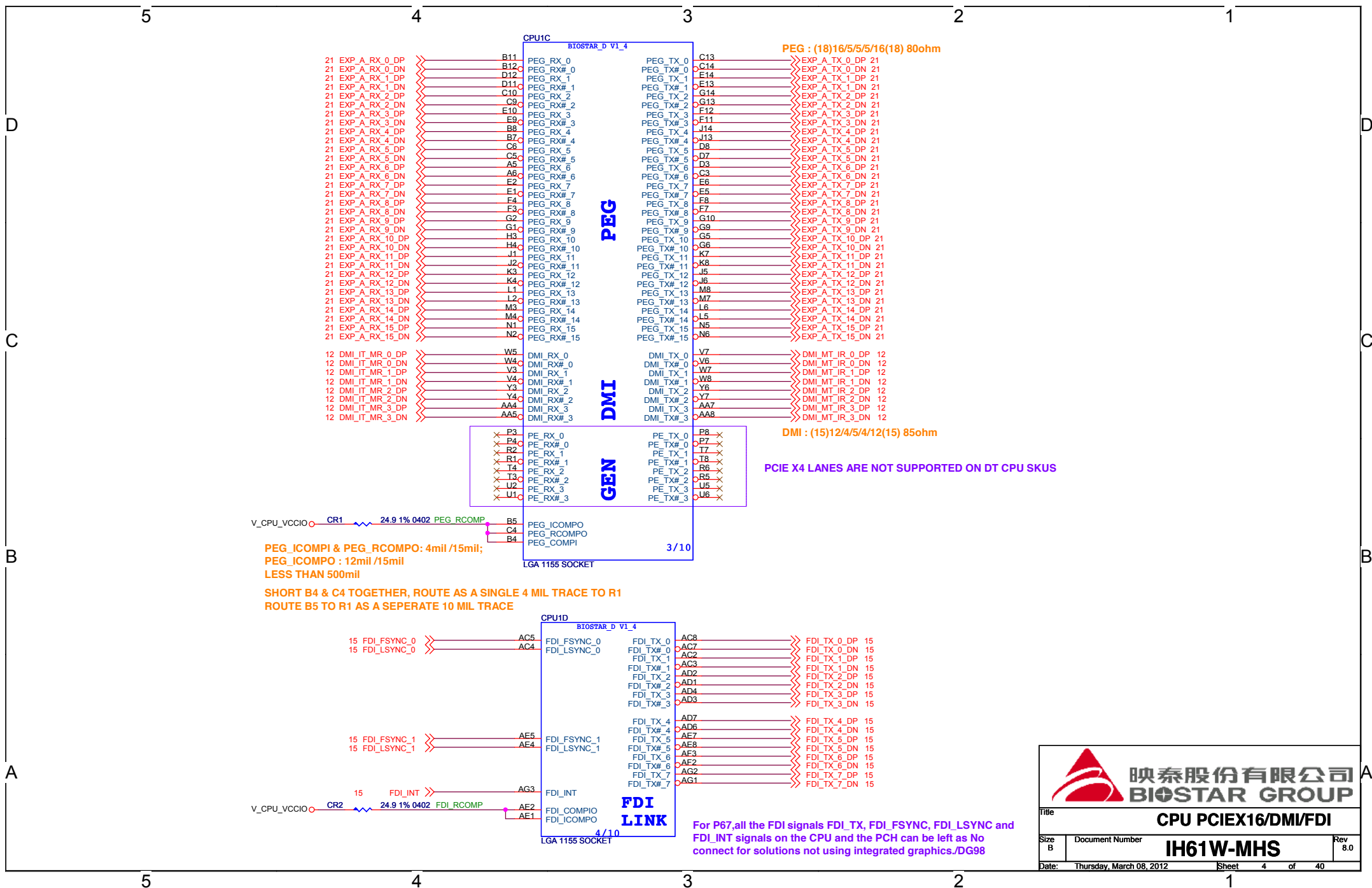
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4

3

2

1

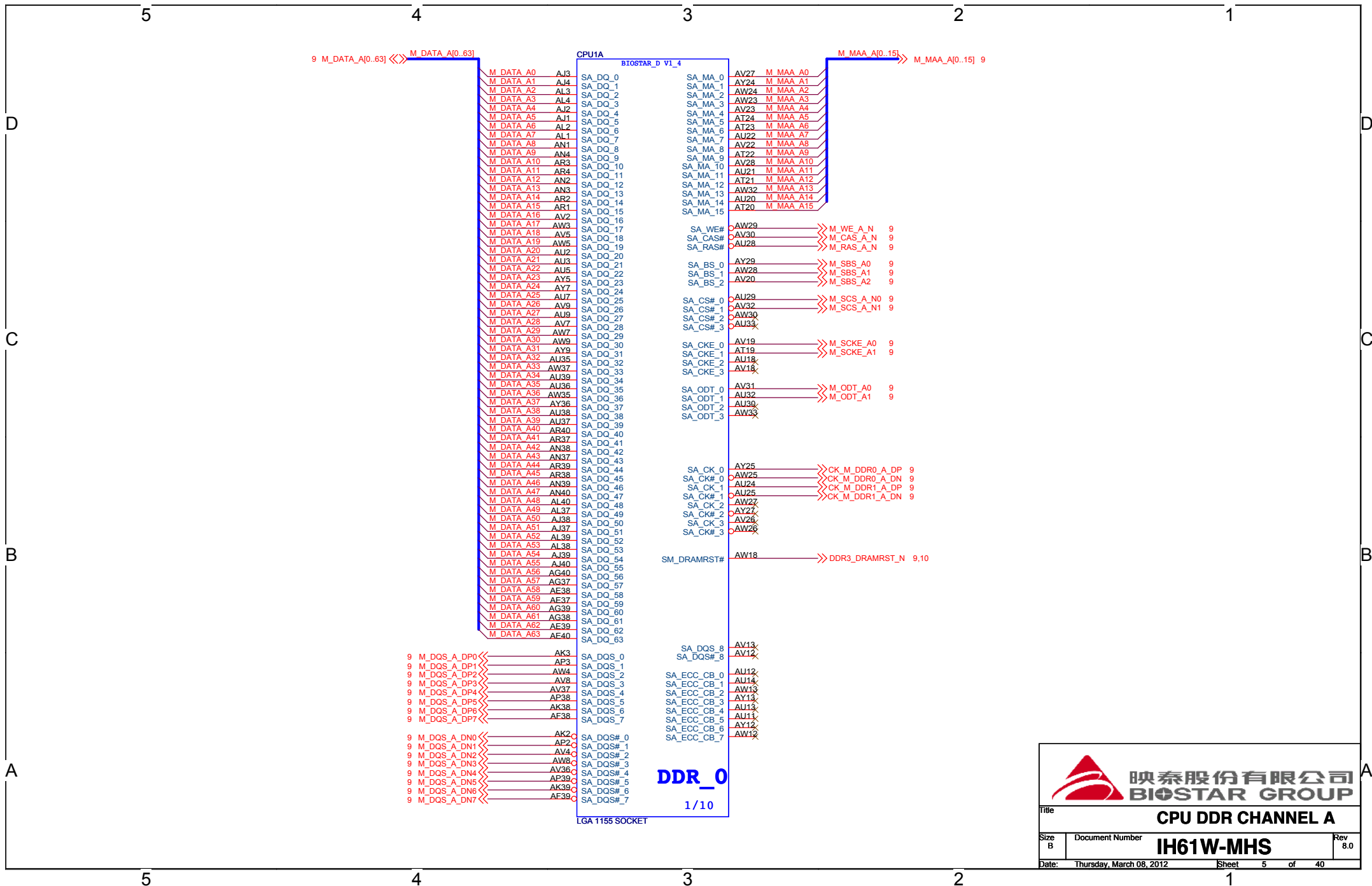


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Title: **CPU PCIEX16/DMI/FDI**

Size B: **IH61W-MHS**

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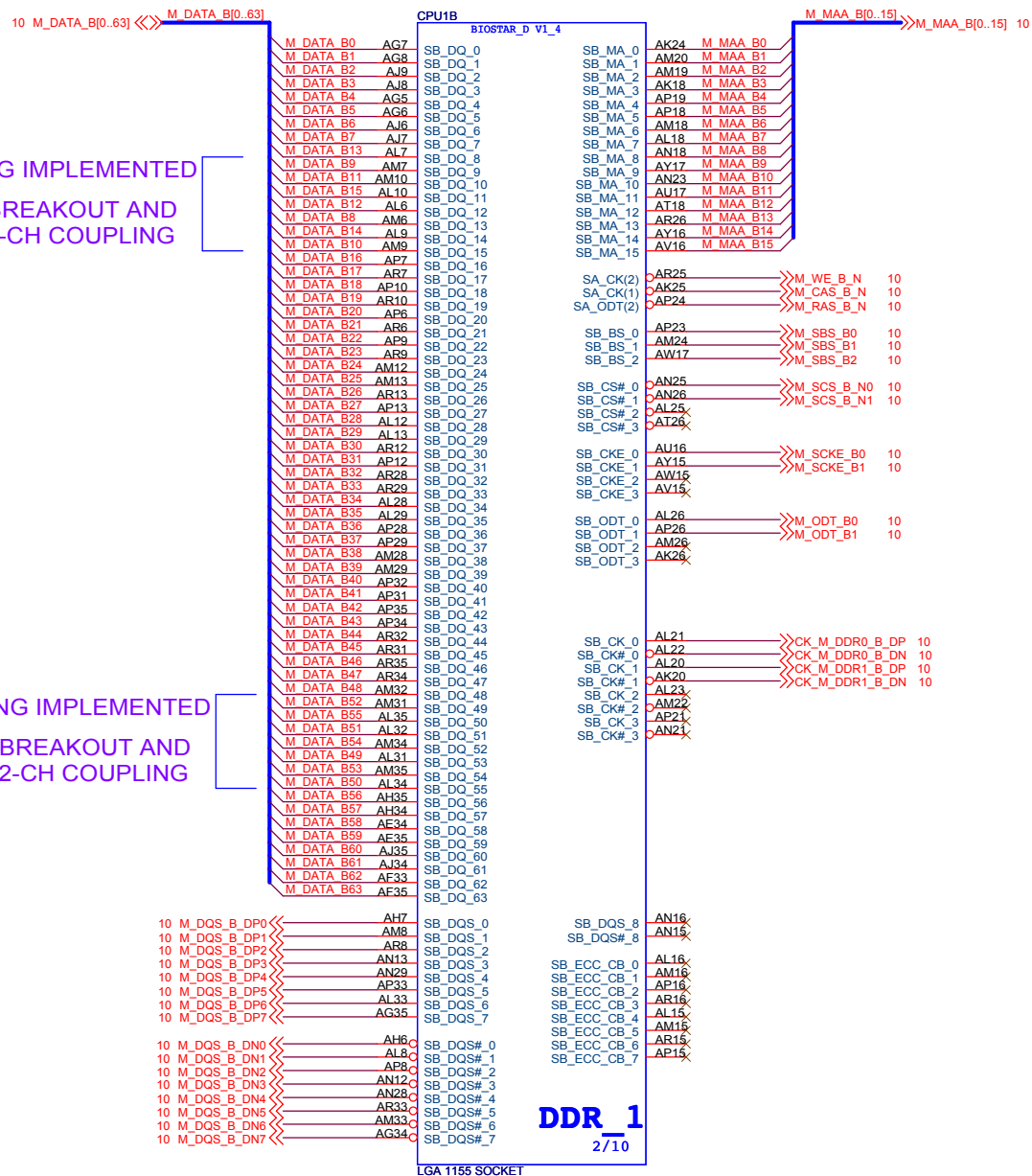
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Title: CPU DDR CHANNEL A

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DQ REMAPPING IMPLEMENTED
TO IMPROVE BREAKOUT AND
MINIMIZE CH-2-CH COUPLING

DQ REMAPPING IMPLEMENTED
TO IMPROVE BREAKOUT AND
MINIMIZE CH-2-CH COUPLING



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Title: **CPU DDR CHANNEL A**

Size B: **IH61W-MHS**

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Rev 8.0

FROM CLK GEN.

FROM PCH

NEAR CPU

for Ivy bridge processor support

VRD12 INTERFACE

37 H_VIDSCK
37 H_VIDSOUT_C
37 H_VIDALERT_N

TBD NEAR PCH

15 NV_CLE >> CR15 4.7K 0402
update for Ivy bridge
DMI/FDI Termination Select
V_1P8_SFR
CR14 2.2K 0402
H_SNB_N
CC2 0.1UF 16V Y5V 0402

PUT INSIDE THE CPU SOCKET

V_SM
CR18 1K 1% 0402
SNB_DDR_VREF
CR24 1K 1% 0402
CC3 0.1UF 16V Y5V 0402

NEAR CPU

H_PWRGD CR32 1K 0402
CC55 0.1UF 16V Y5V 0402/NI

PCH NO PECI SUPPORTED

CFG6	CFG5	PCIE CONFIG
1	1	1 X 16
1	0	2 X 8
0	1	RESERVED
0	0	X8,X4,X4

CFG	H	L	DESCRIPTION
2	NORM	RESERVED	PEGLANE REVERSAL[0],X16
5	*	*	SEL0
6	*	*	SEL1

MTP1 1 CK_PE_100M_MCP_DP
MTP2 1 CK_PE_100M_MCP_DN
MTP3 1 H_PWRGD
MTP4 1 H_DRAMPWRGD
MTP5 1 PLTRST_CPU_N

CPU1E
BIOSTAR_D_V1_4
BCLK_0 BCLK#_0
VIDSCLK C37
VIDSOUT B37
VIDALERT# A37
VCCP_SELECT P33 VCCP_SEL 1 MTP6
VCCSA_VID P34 VCCSA_VID 1 MTP13
VCCSA_SENSE
VCC_SENSE A36 VCCIO_SENSE VCC_SENSE 37
VSS_SENSE B36 VSSIO_SENSE VSS_SENSE 37
VCCIO_SENSE
VSSIO_SENSE
VCCAXG_SENSE L32 VCCAXG_SENSE 37
VSSAXG_SENSE M32 VSSAXG_SENSE 37
TDO L39 H_TDO
TDI L40 H_TDI
TCK M40 H_TCK
TMS L38 H_TMS
H_TRST_N J39 H_TRST_N
K38
K40
C40
C40
D40
RSVD_001
RSVD_002
CFG_0 H40
CFG_1 H38
CFG_2 G38
CFG_3 G40
CFG_4 G39
CFG_5 F38
CFG_6 F38
CFG_7 E40
CFG_8 BPM#_7
CFG_9 BPM#_6
CFG_10 BPM#_5
CFG_11 BPM#_4
CFG_12 BPM#_3
CFG_13 BPM#_2
CFG_14 BPM#_1
CFG_15 H40
CFG_16 H38
CFG_17 G38
RSVD_016 AT14
RSVD_020 AY3
RSVD_023 H7
RSVD_028 H8
RSVD_029

MISC

VCCSA_VID
1kΩ Pull-Down On VID Lines

CPU1J
BIOSTAR_D_V1_4
RSVD_04 FC_AH1
RSVD_05 FC_AH2
RSVD_08
RSVD_10 AT11
RSVD_11 AP20
RSVD_12 AN20
RSVD_13 AU10
RSVD_17 AY10
RSVD_21
RSVD_22
RSVD_43
RSVD_44
RSVD_45
RSVD_46
RSVD_47
RSVD_48
RSVD_49
RSVD_07 AF4
RSVD_09 AB6
RSVD_06 AEG
RSVD_09 AJ11
NCTF_01 D38
NCTF_02 C38
NCTF_03 J34
NCTF_04 N34
NCTF_05
SPARES 10/10
LGA 1155 SOCKET

V_CPU_VCCIO
H_THERMTRIP_N CR17 51 0402 /NI
H_PROCHOT_N CR19 51 0402
H_CATERR_N CR20 1K 0402 /NI
H_PECI CR22 1K 0402 /NI
H_PWRGD CR23 51 0402 /NI
CRN1 51 8P4R 0402
H_TDI 2
H_TDO 4
H_TMS 6
H_TRST_N CR31 51 0402
H_TCK CR25 51 0402
H_DRAMPWRGD CR34 1K 0402
V_SM

CPU RESET LOGIC

14,27 PLTRST_N >> PLTRST_N CR30 200 1% 0402
CR28 110 1% 0402
CC4 0.1UF 16V Y5V 0402

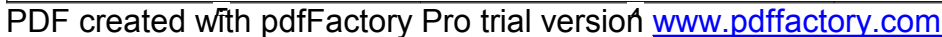
www.vinafix.vn

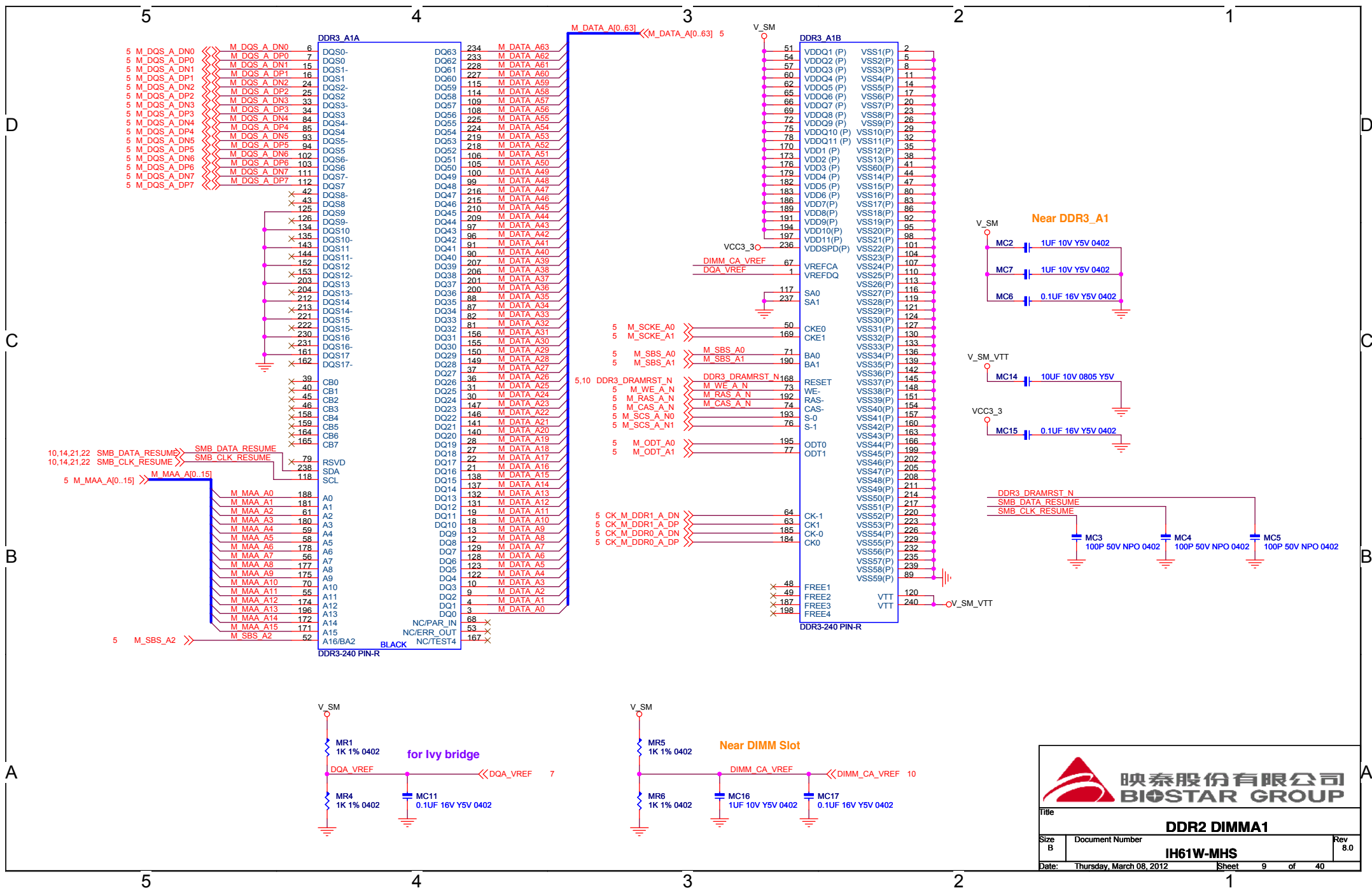
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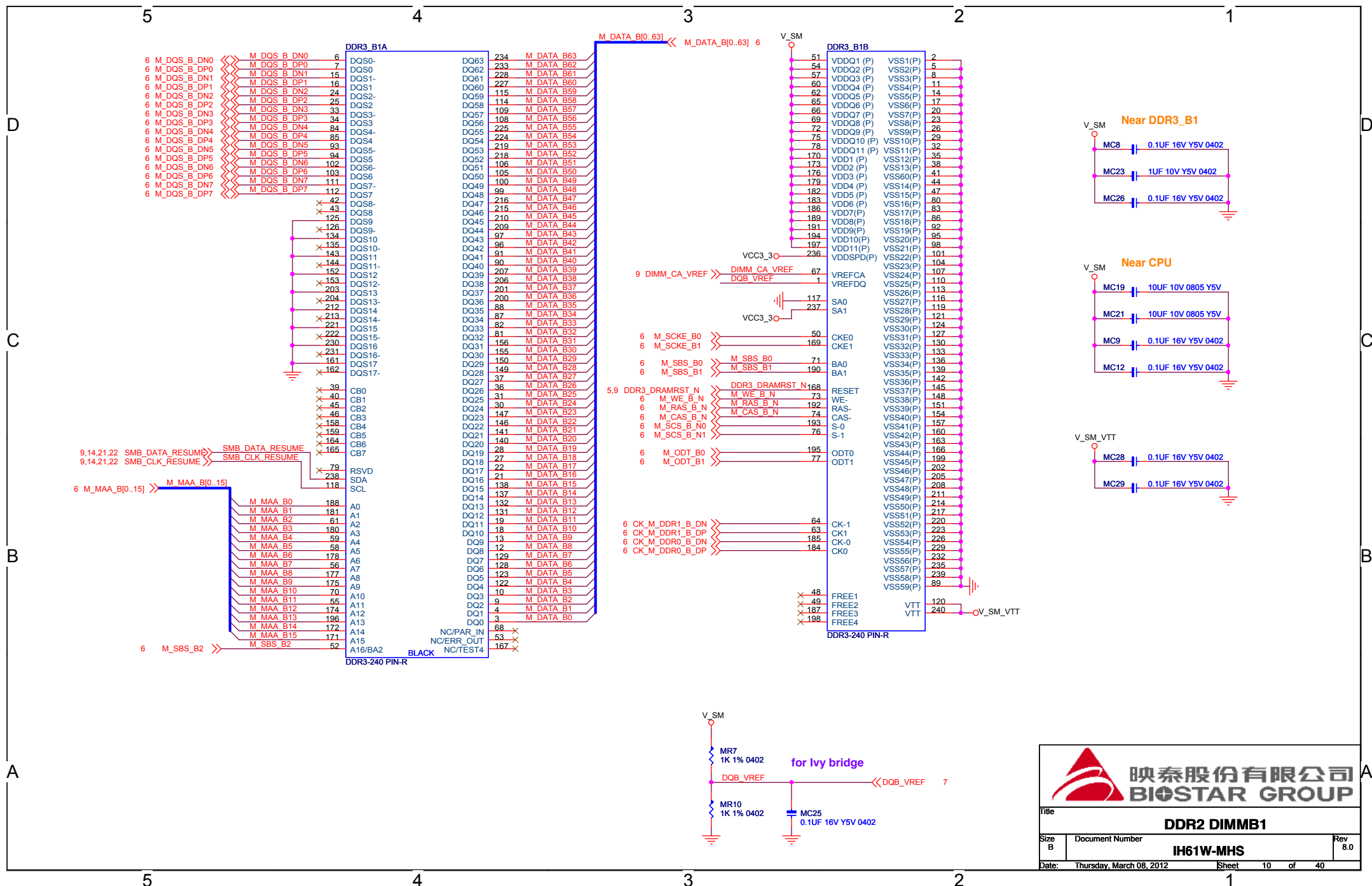
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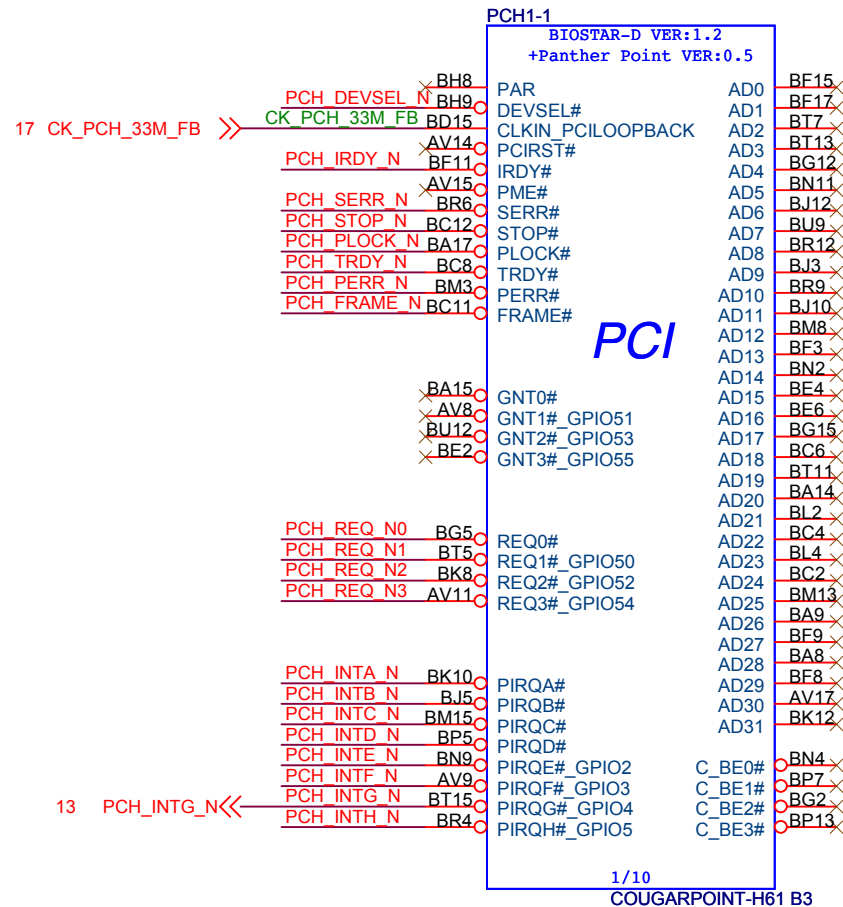
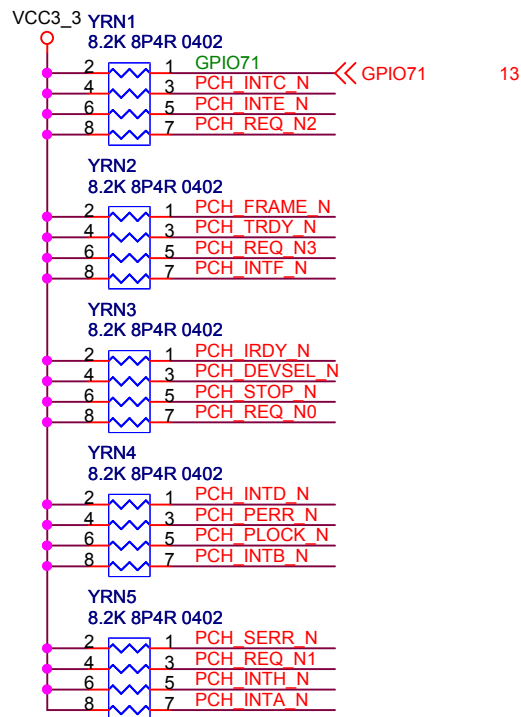
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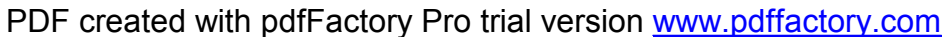


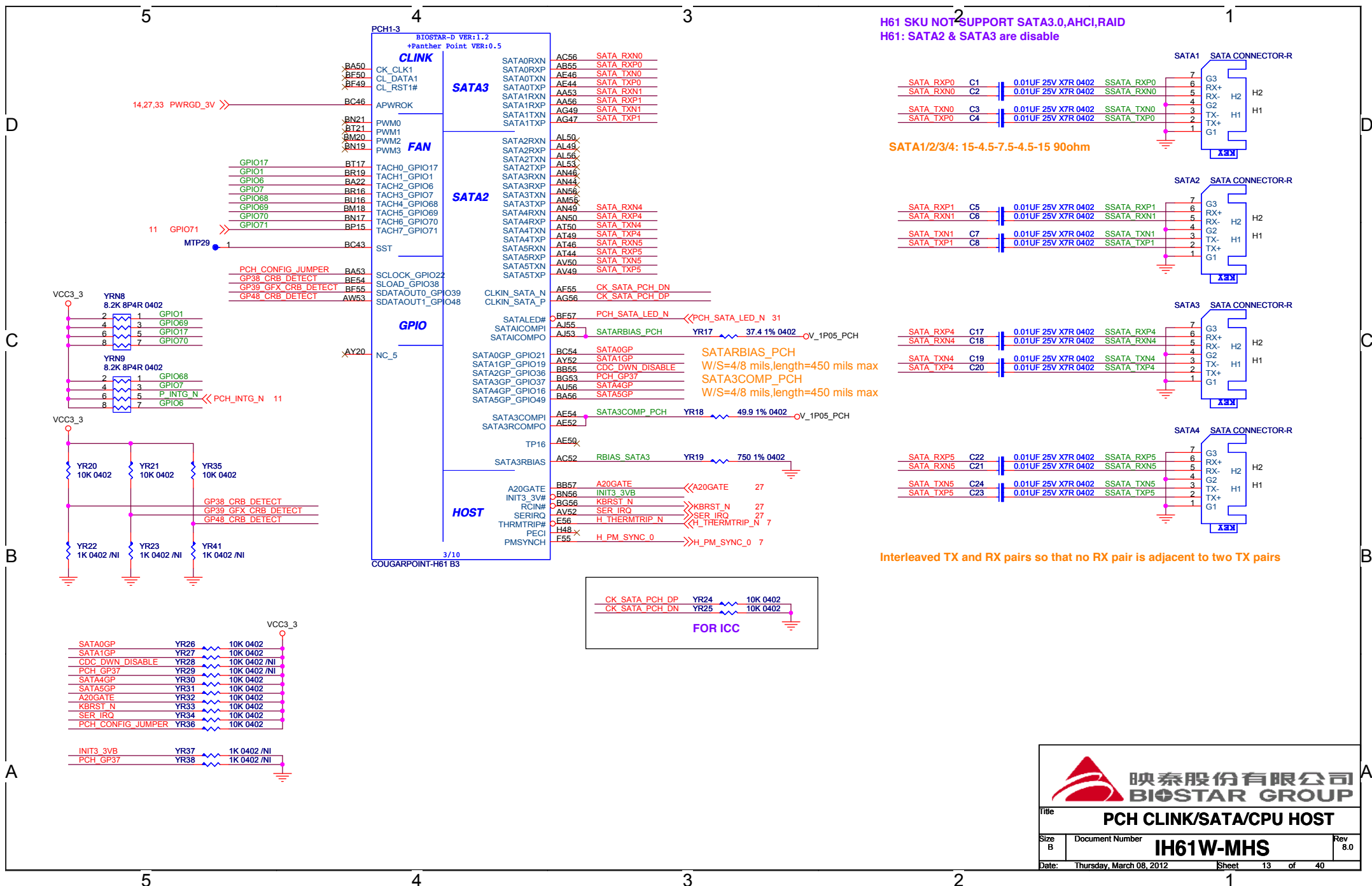


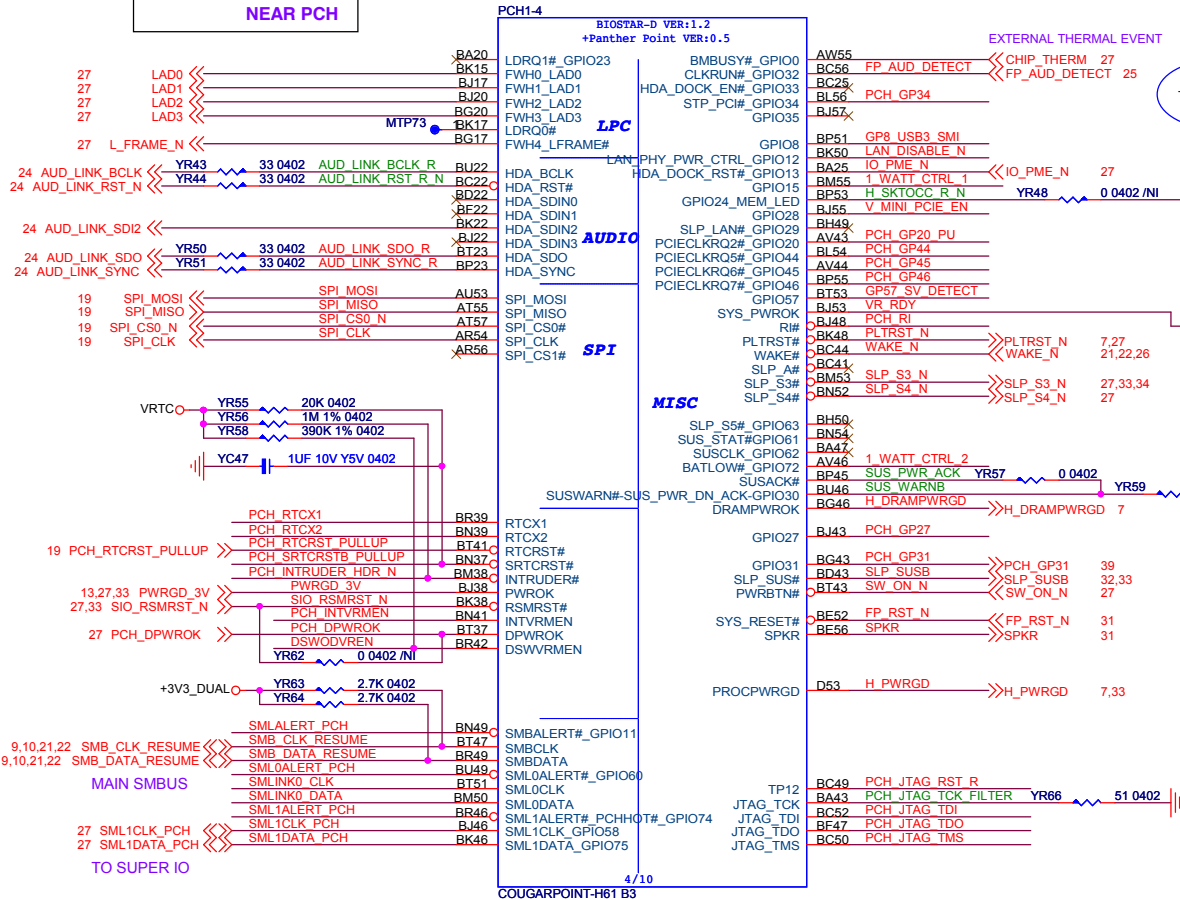
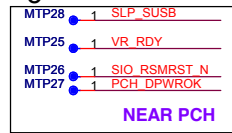
WEAK INTERNAL PULLUPS ON GNT*.DEFAULT SPI BOOT DEVICE

GNT1	GNT0/SATA1GP	BOOT DEVICE
0	0	LPC
0	1	NANO
1	0	PCI
1	1	SPI

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Title PCH PCI		
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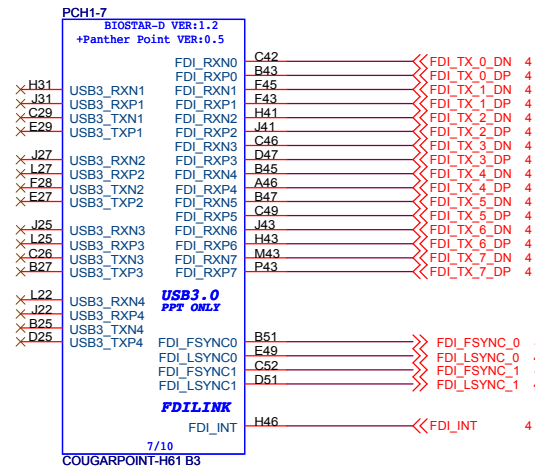
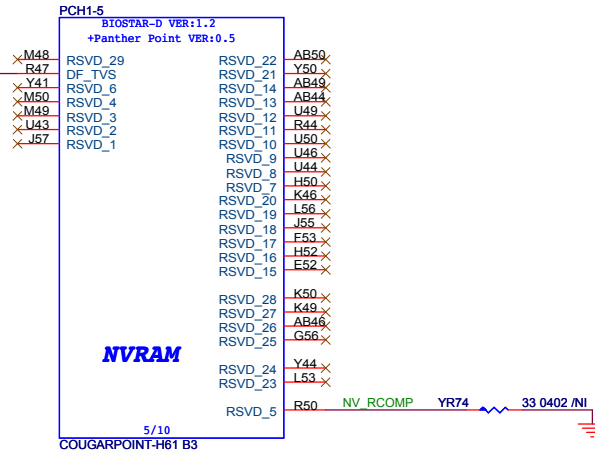




DMI/FDI Termination Select

H:For Sandy Bridge

L:For Ivy Bridge

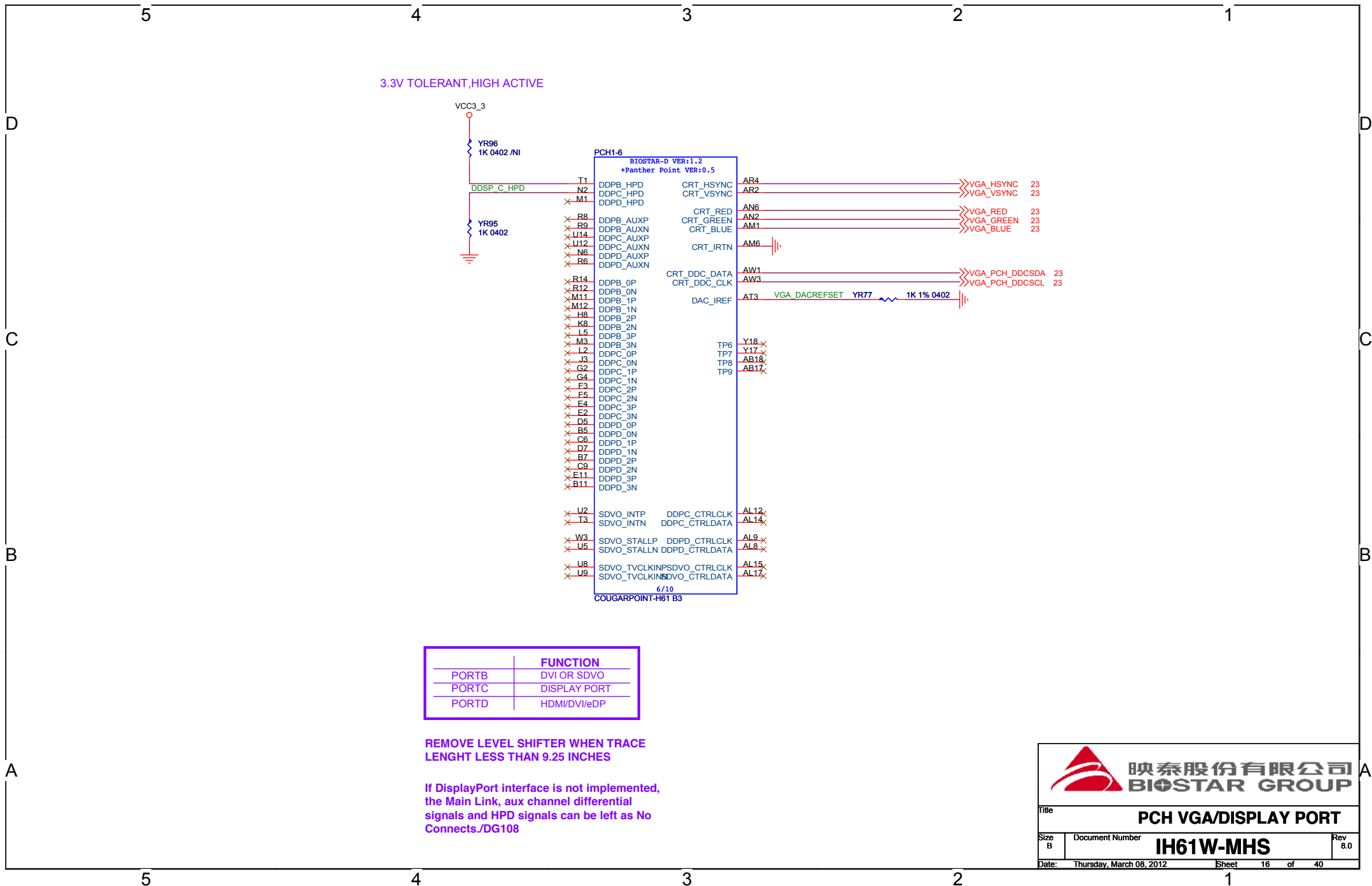


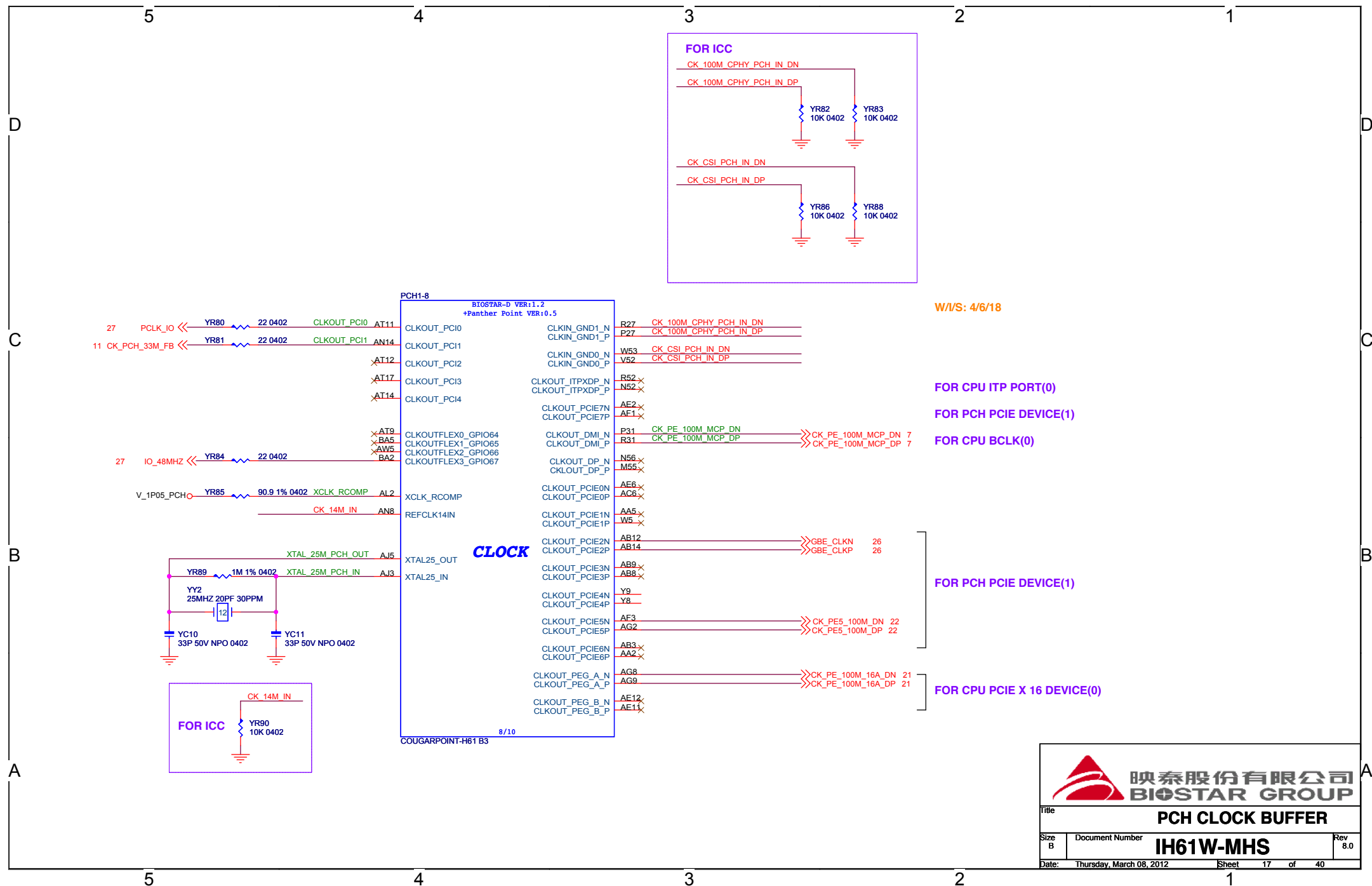
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Title PCH NVRAM & FDI LINK

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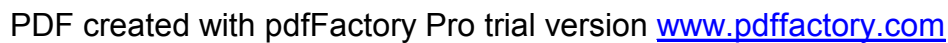
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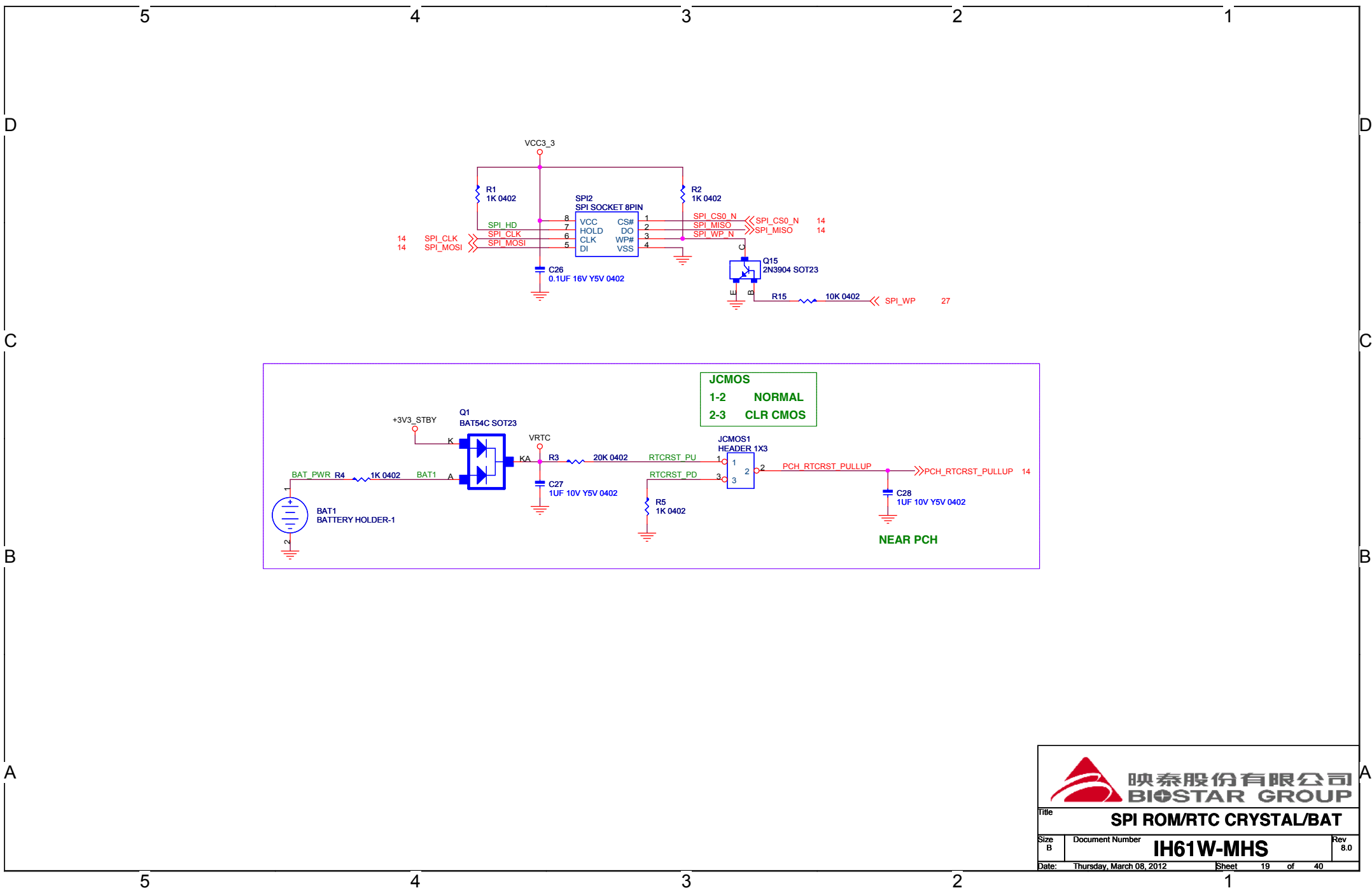
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Size B: **IH61W-MHS**

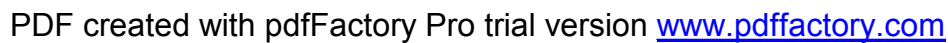
Date: Thursday, March 08, 2012 Sheet 17 of 40

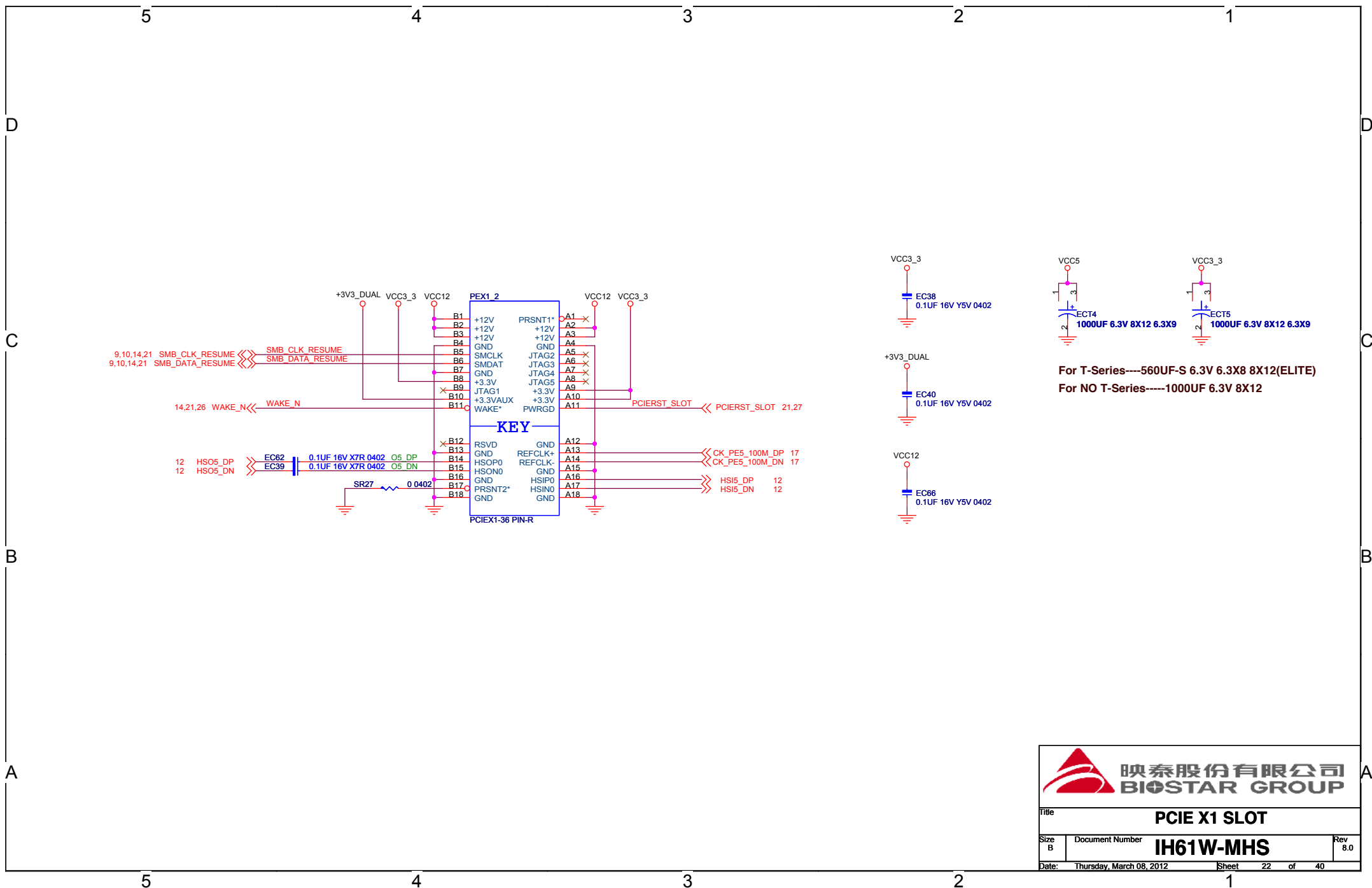
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SPI ROM/RTC CRYSTAL/BAT		
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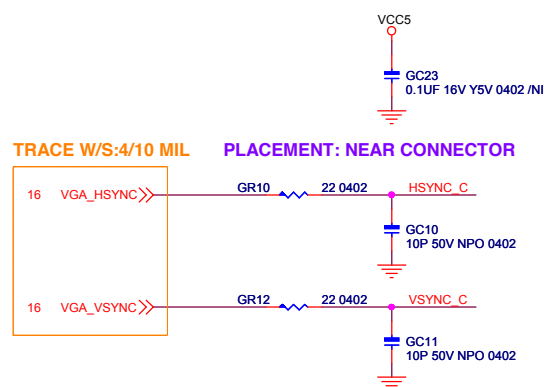
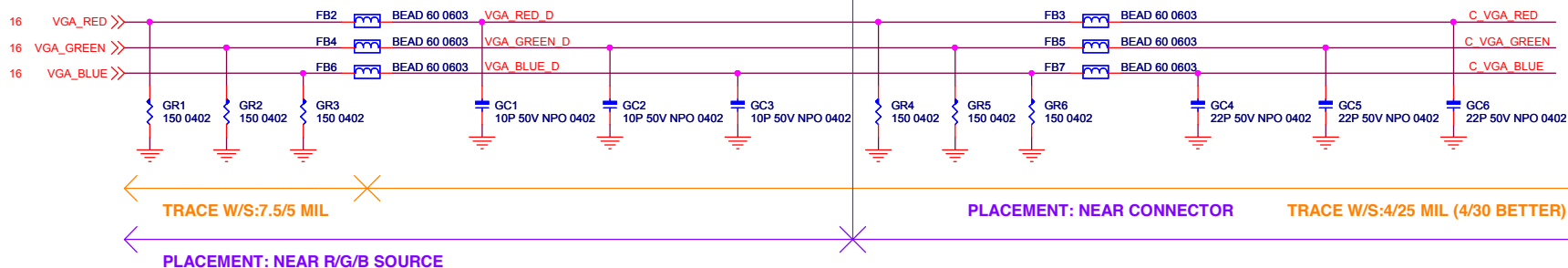




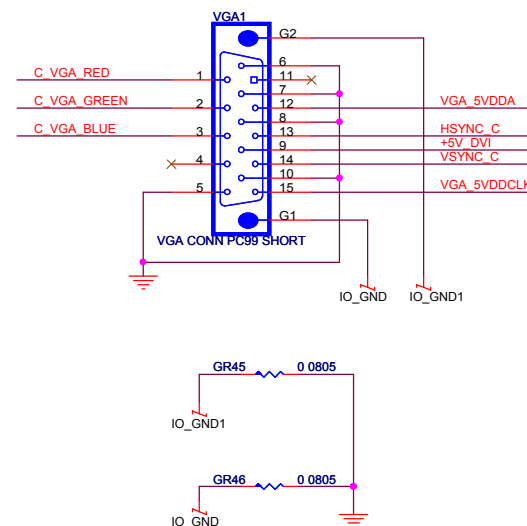
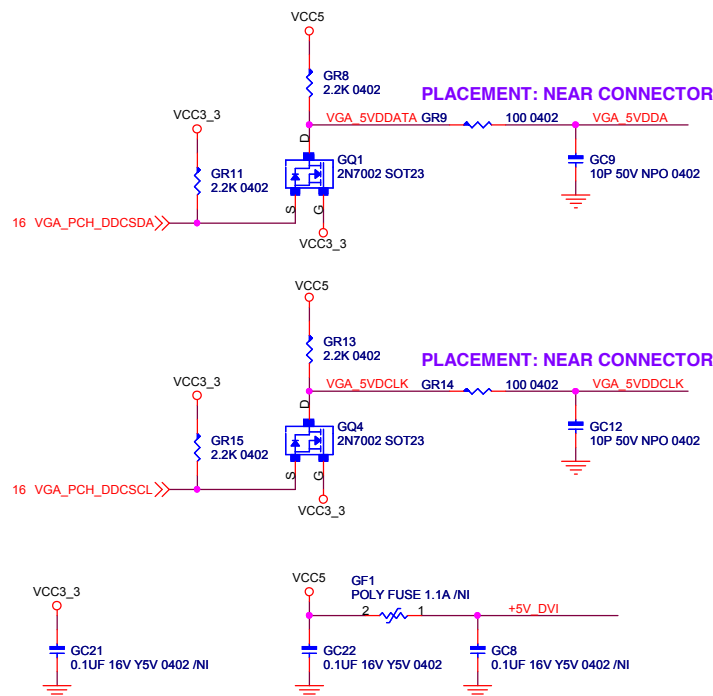


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Title PCIE X1 SLOT		
Size B	Document Number IH61W-MHS	Rev 8.0
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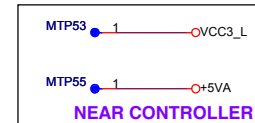
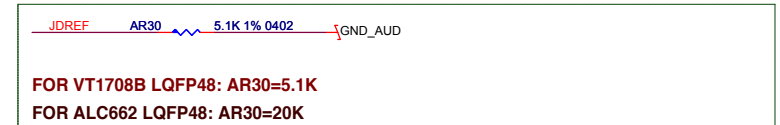
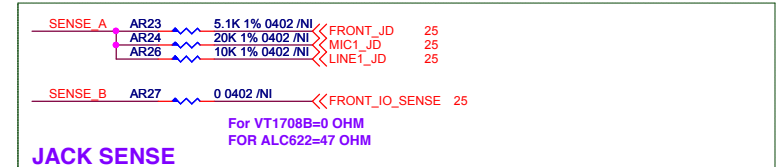
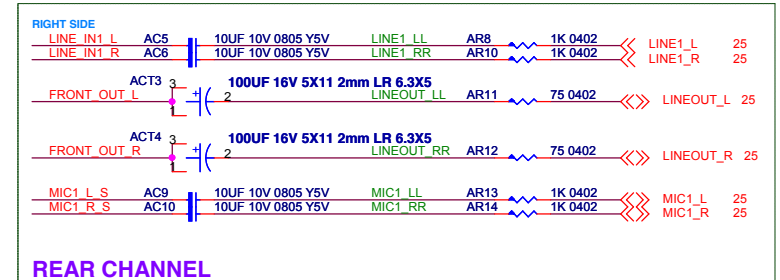
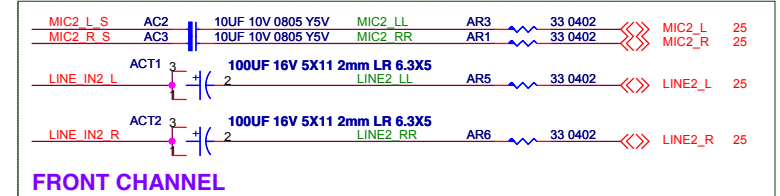
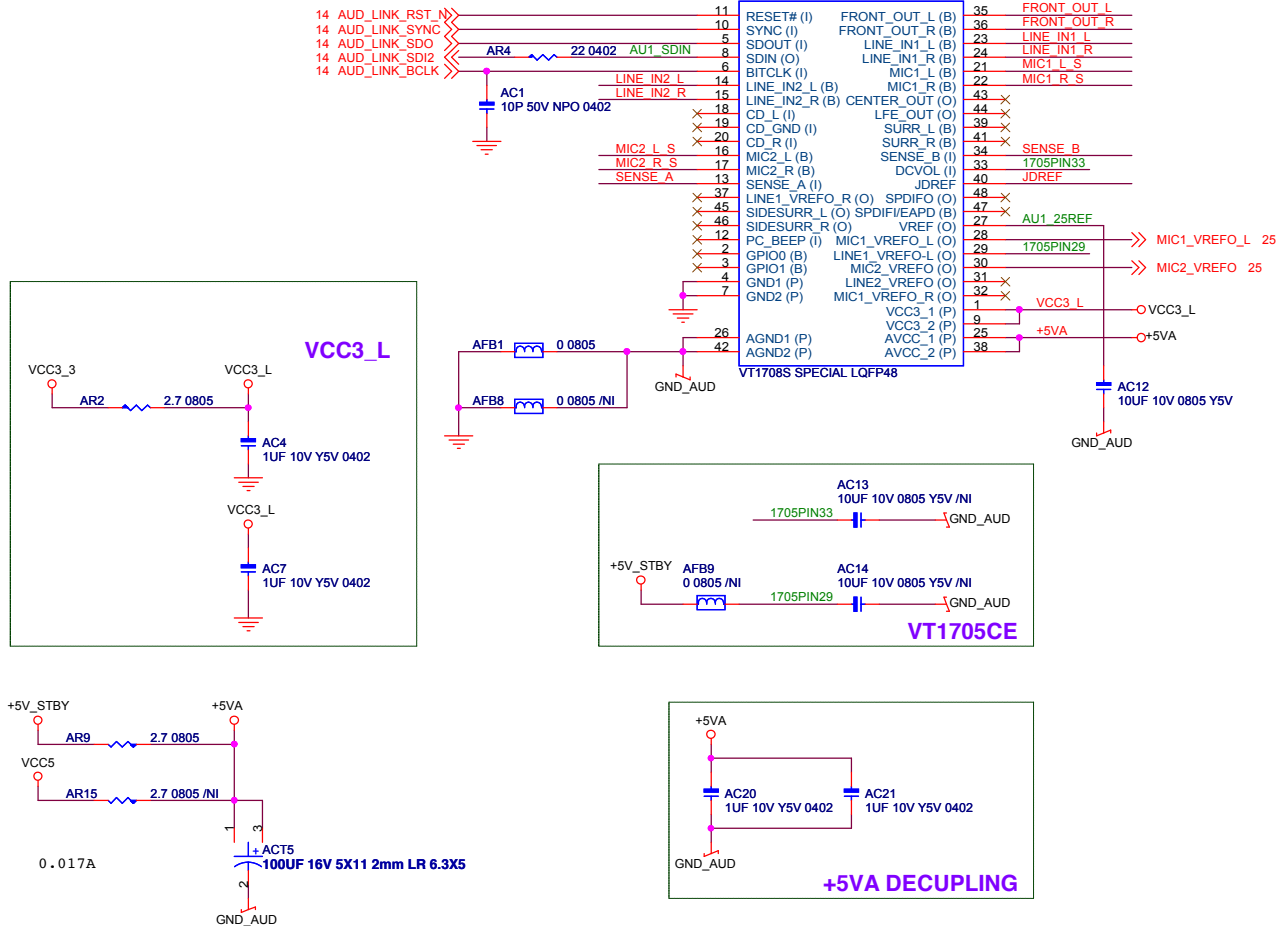


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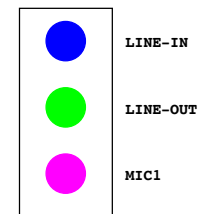
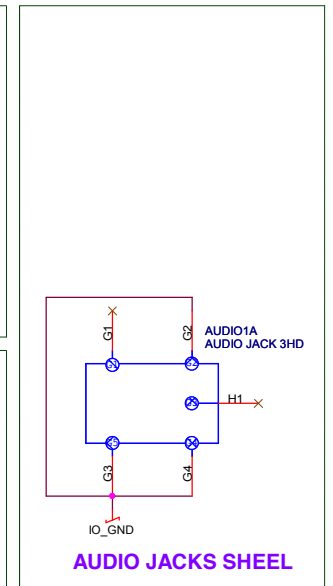
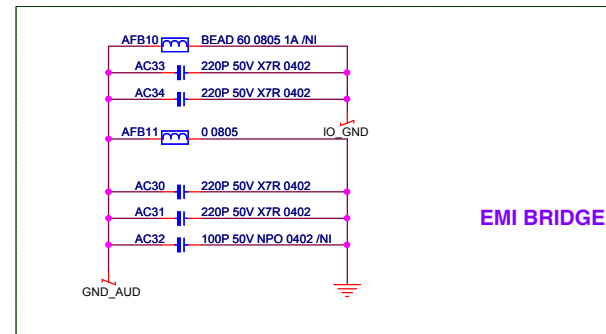
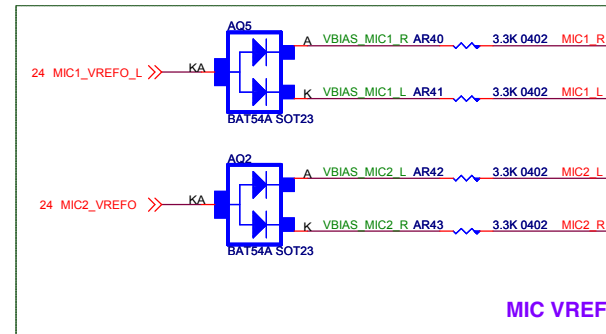
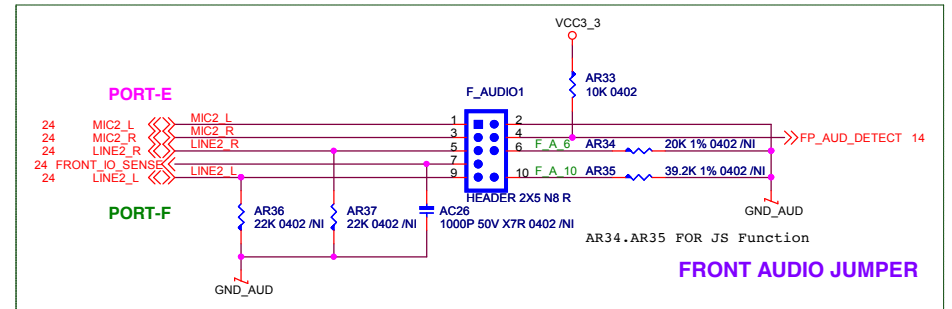
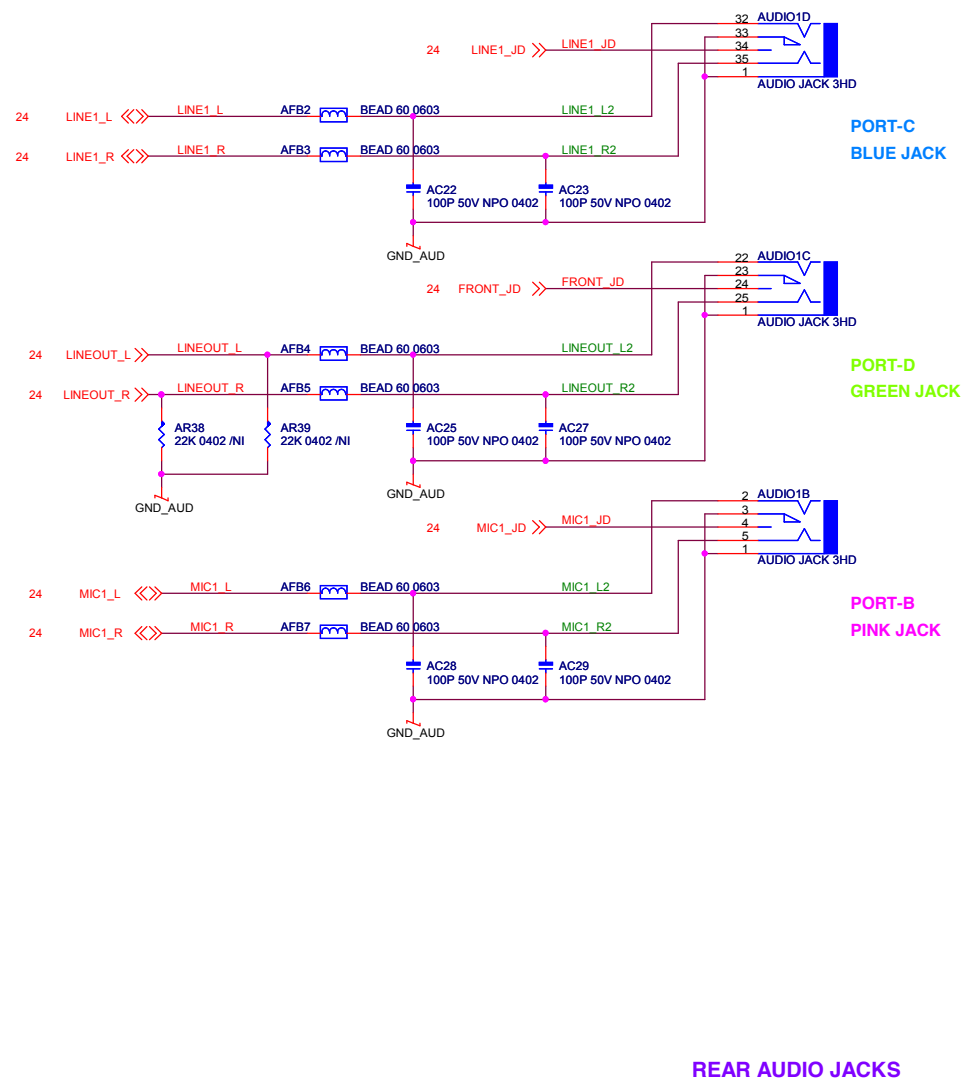


Title: VGA CONNECTOR		
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AUDIO PART: A+Reference



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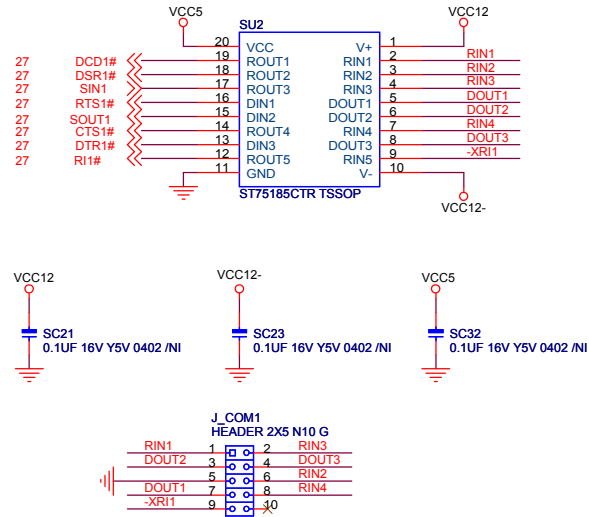
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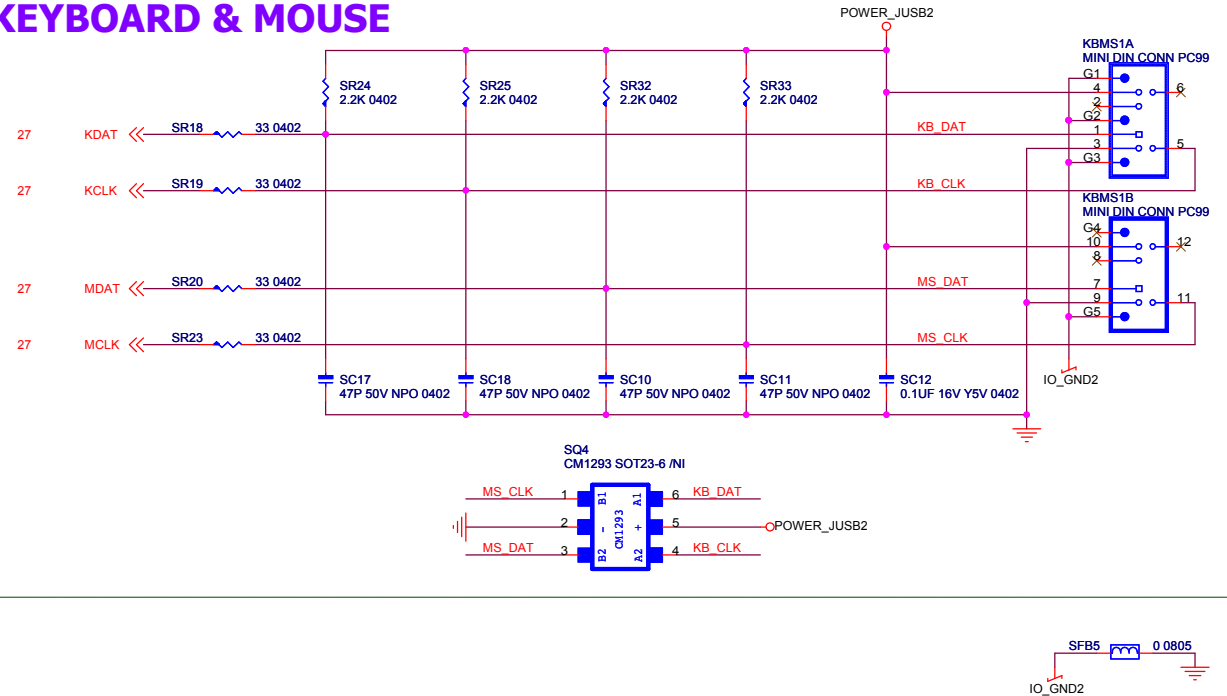
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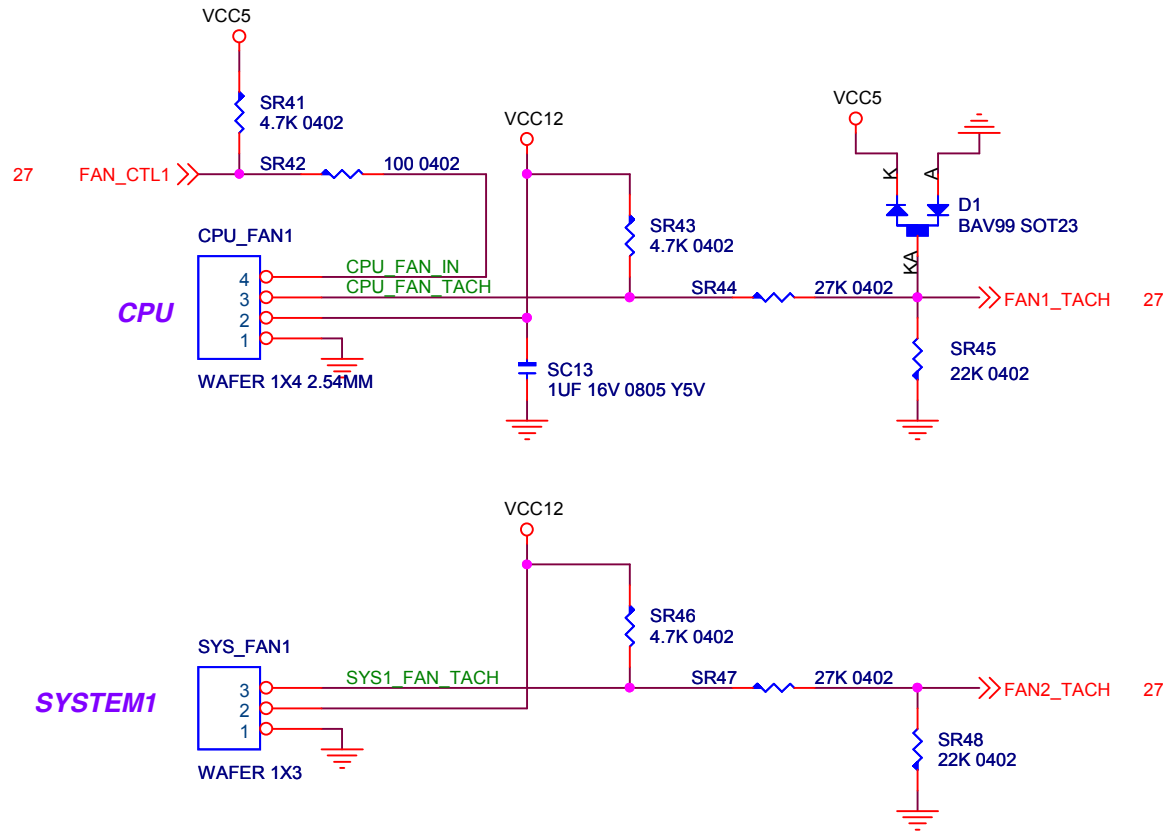
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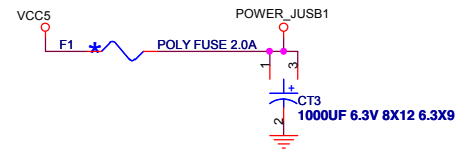
KEYBOARD & MOUSE



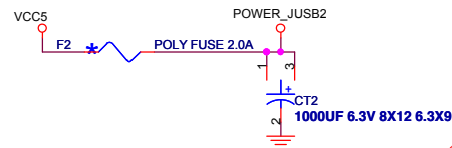
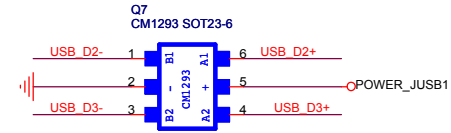
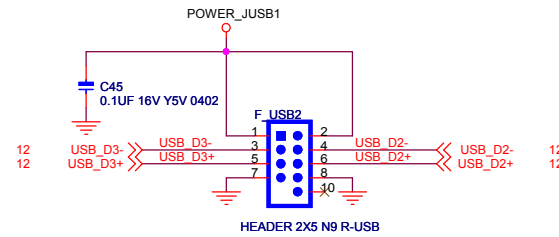
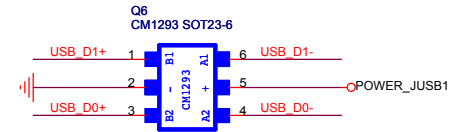
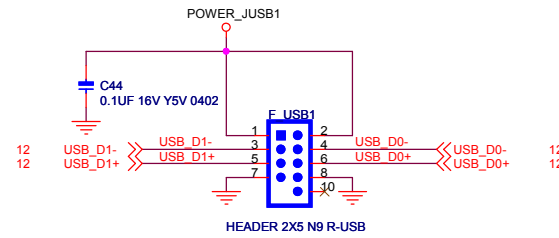
CPU FAN/SYSTEM FAN1



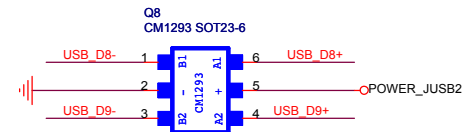
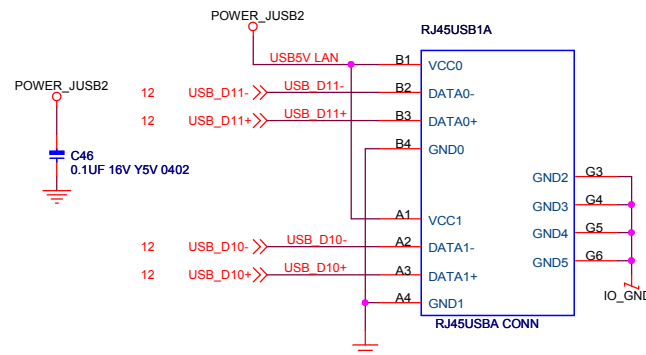
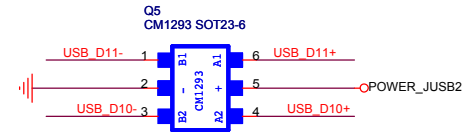
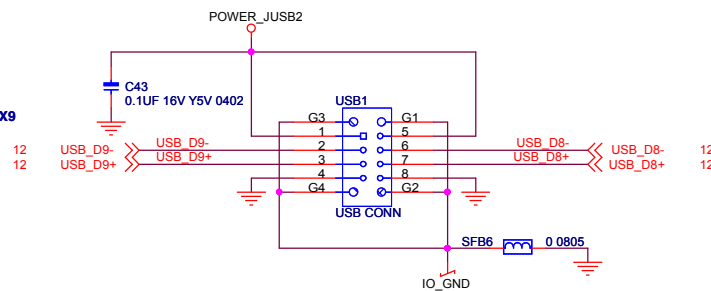
		
Title HW MONITOR/FAN CONTROL		
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For T-Series-----560UF-S 6.3V 6.3X8 8X12(ELITE)
For NO T-Series-----1000UF 6.3V 8X12



BACK PANEL USB
PLACE NEAR CONN



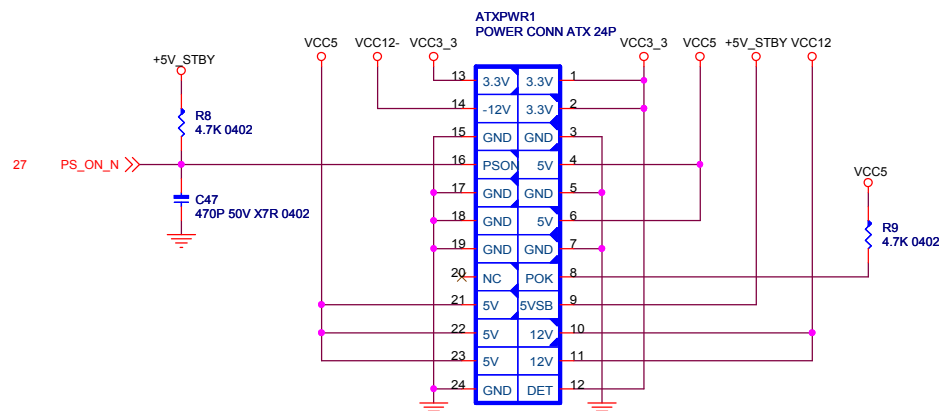


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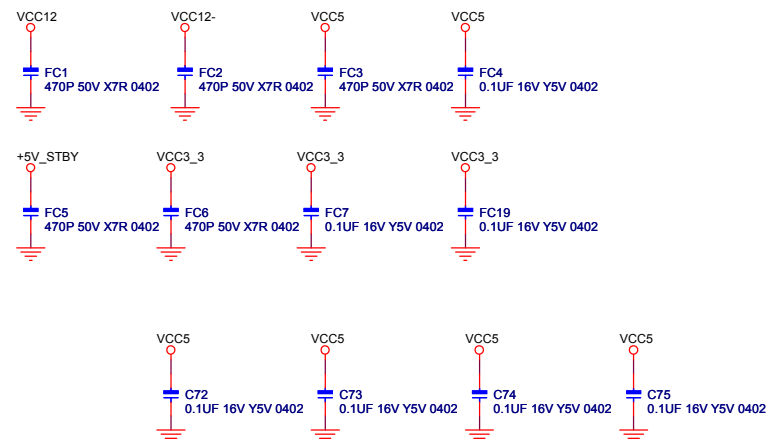
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USB CONN		
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24 PIN POWER CONNECTOR

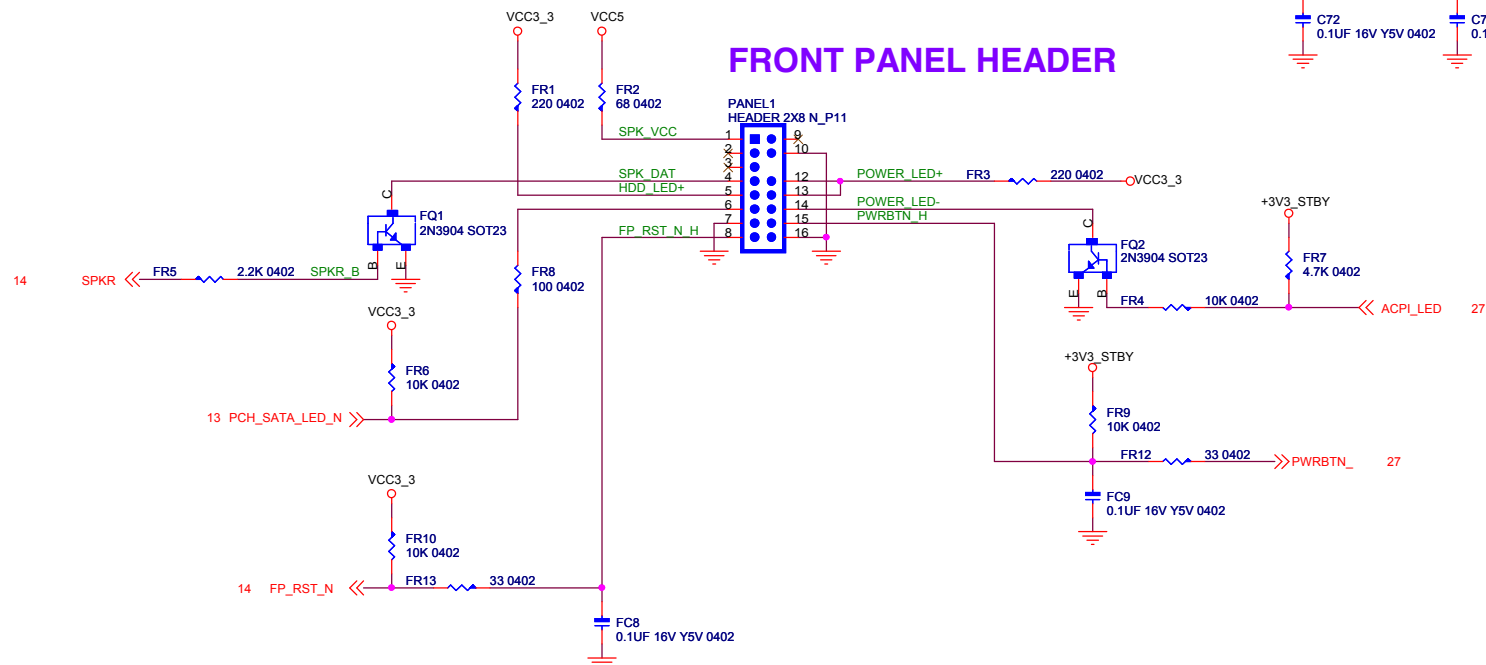
JATXPWR



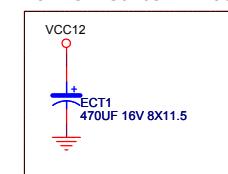
FOR EMI



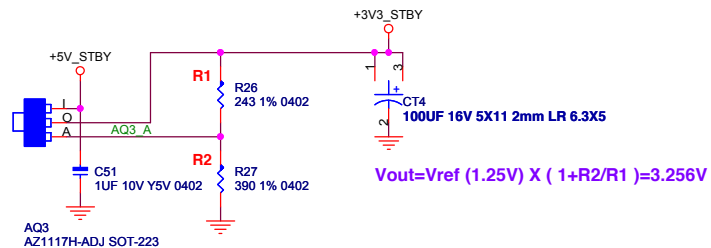
FRONT PANEL HEADER



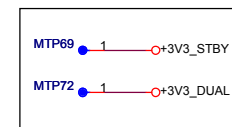
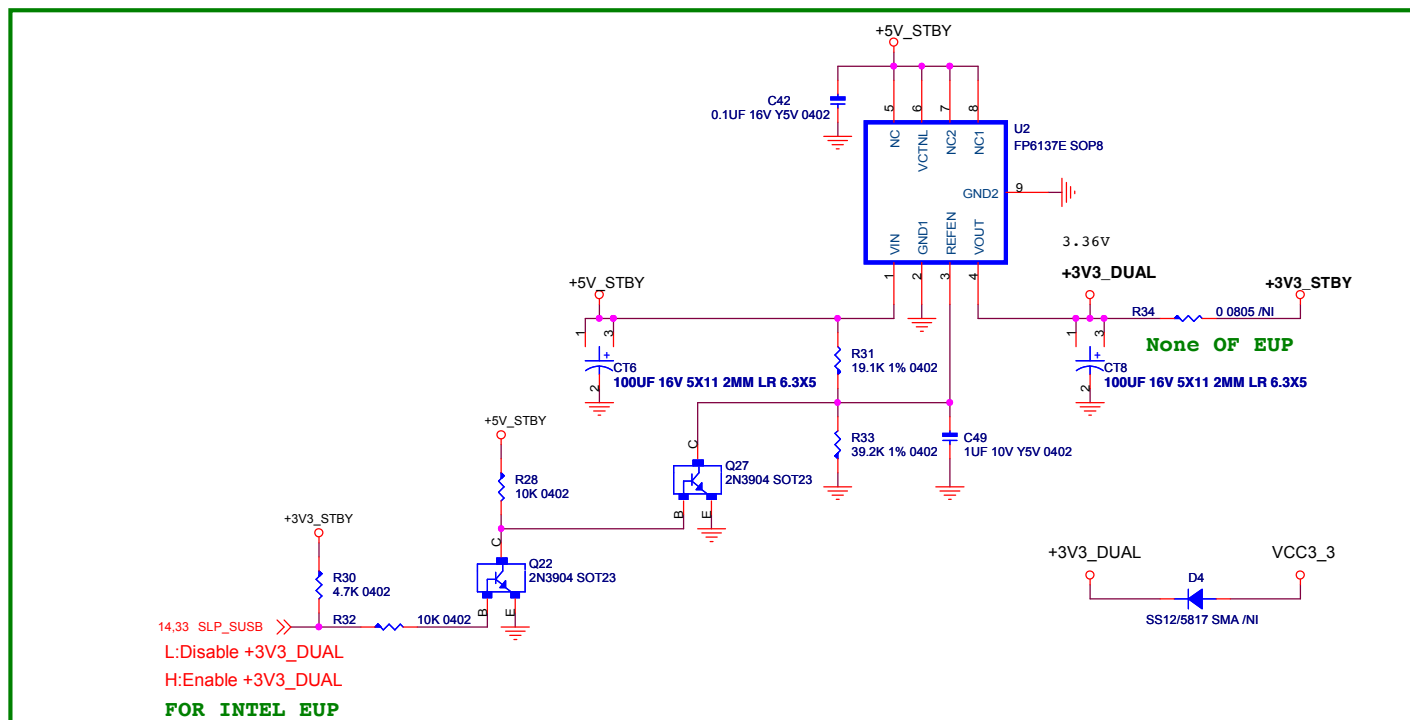
For NO T-Series-----470UF 16V 8X11.5



Title 24PIN POWER CONN&FP			
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CT4,CT5,CT13:
 NETIN: 100UF 16V 5X11 2MM LR 6.3X5
 BOM: 100UF 16V 5X11 2mm LR
 100UF-S 16V 6.3X8 ELITE

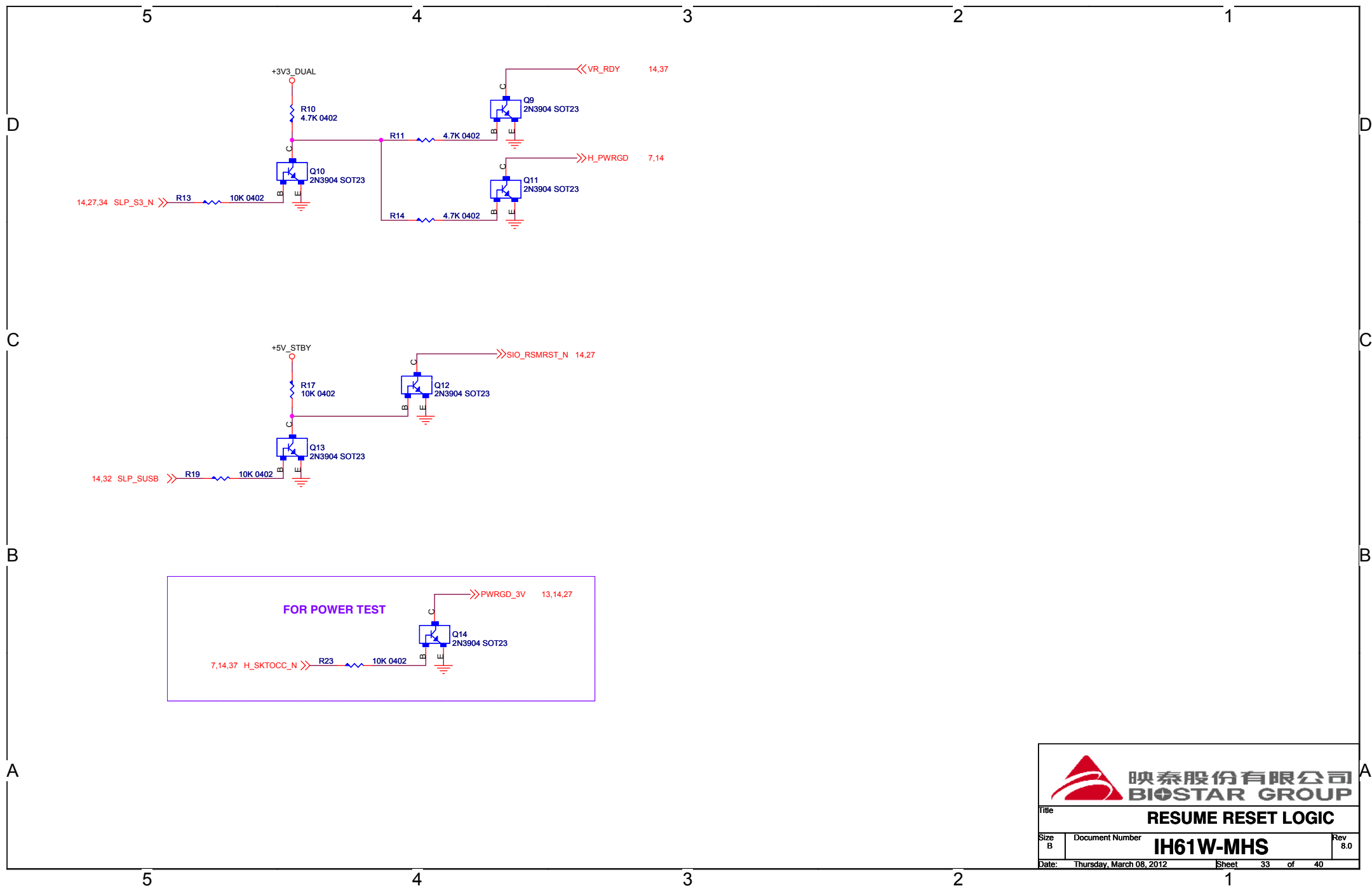


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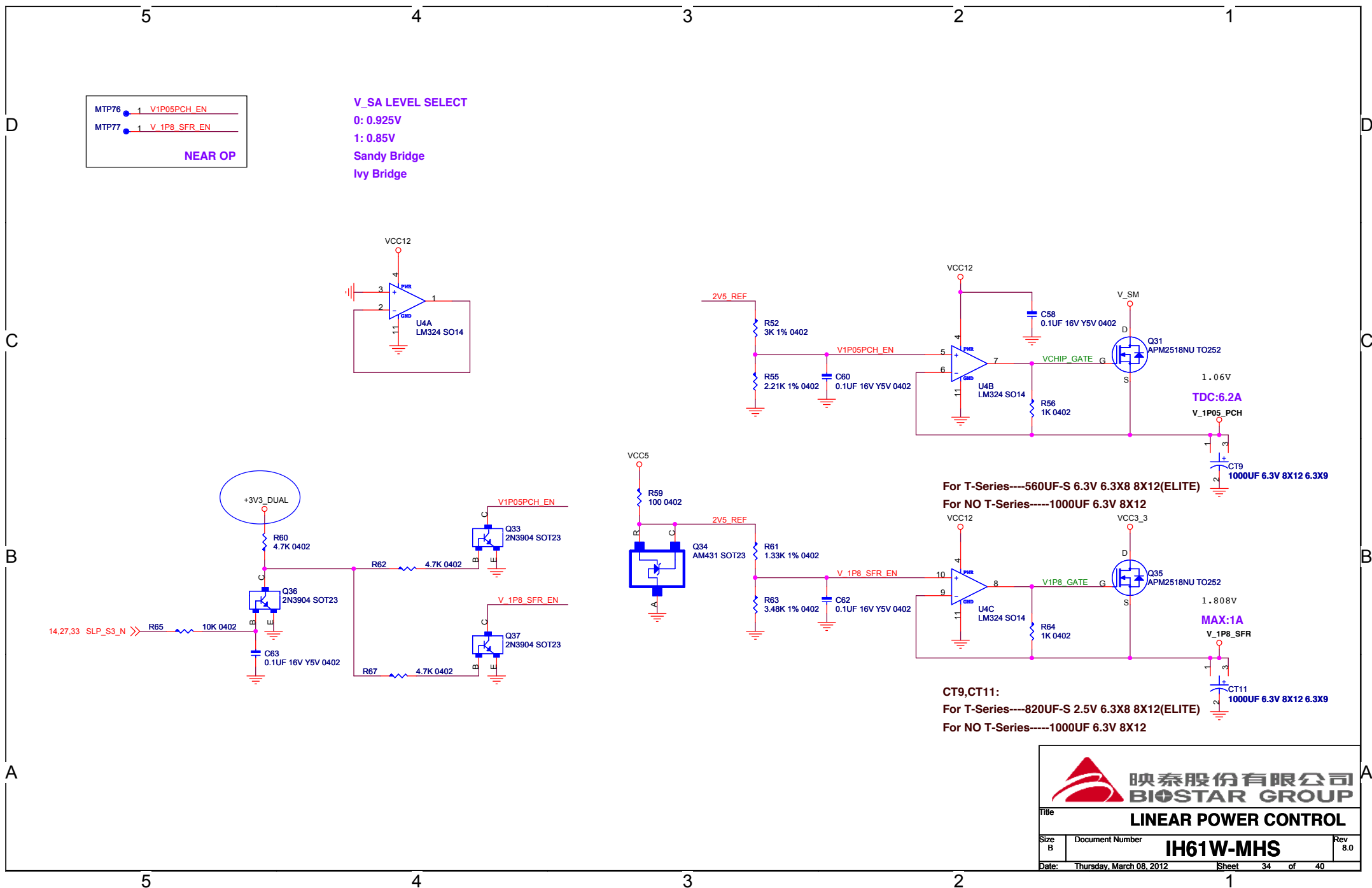
Title **ACPI POWER CONTROL**

Size B Document Number **IH61W-MHS** Rev 8.0

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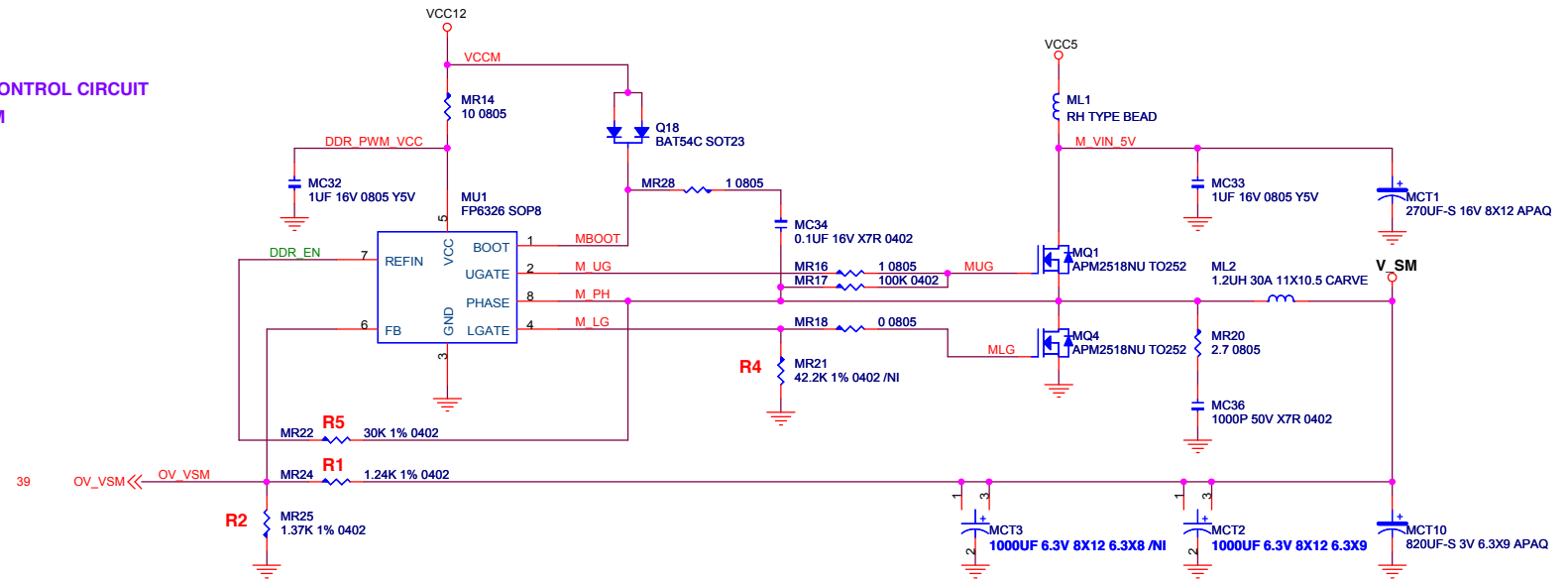
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Title
LINEAR POWER CONTROL

Size B Document Number
IH61W-MHS

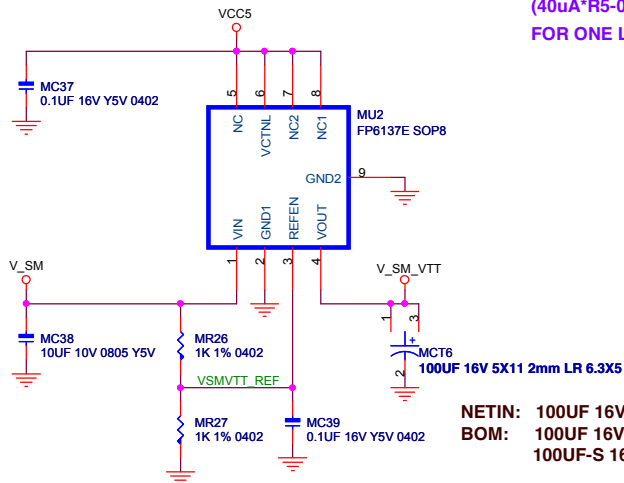
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MEMORY VLOTAGE CONTROL CIRCUIT FOR INTEL PLATFORM



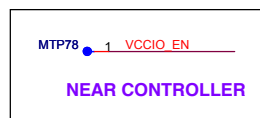
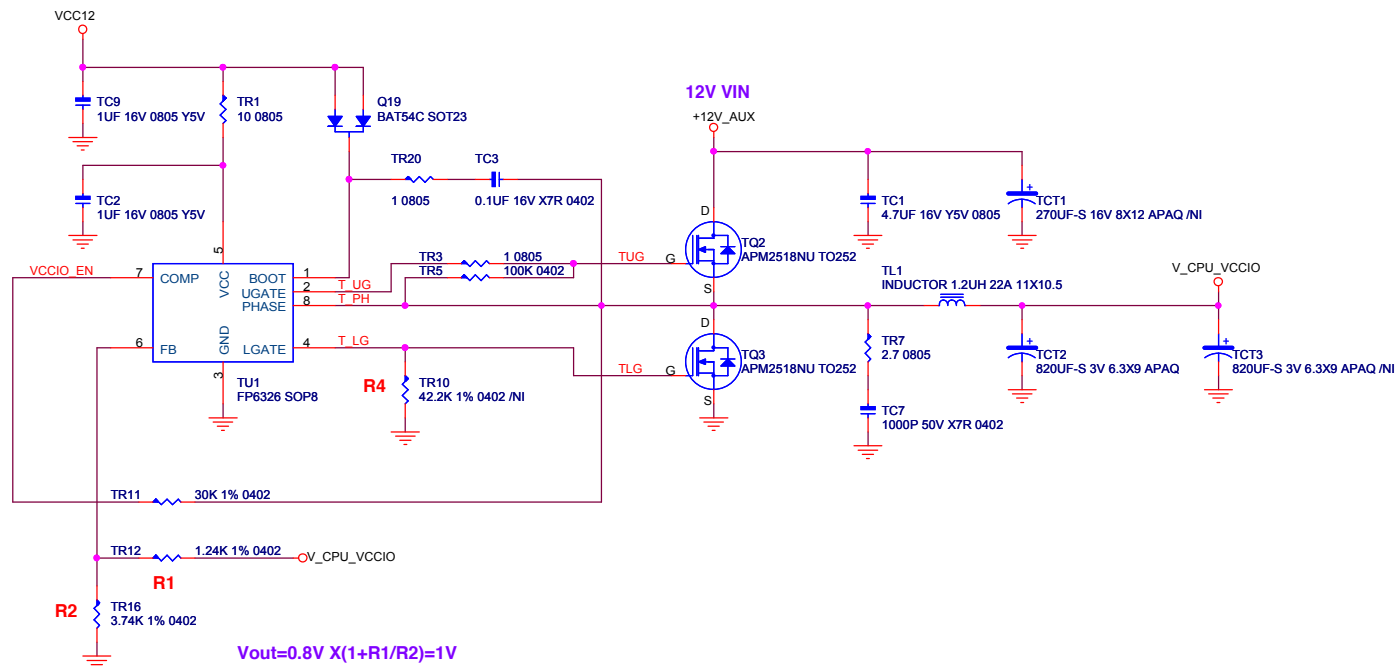
$V_{SM} = 0.8(1 + R1/R2) = 1.524V$ ($R1 = 1.24K$ $R2 = 1.37K$)
R5 Only For FP6326 **R4 Only For UP6109**
 $(40\mu A \cdot R5 - 0.4V) / R_{ds} = I_{oc}$ **OCF Set : 31A**
FOR ONE LS MOSFET, R5=14.7K 1% **FOR ONE LS MOSFET, P0603BDL : R4=42.2K 1%**

For T-Series-----820UF-S 2.5V 6.3X8 8X12(ELITE)
For NO T-Series-----1000UF 6.3V 8X12



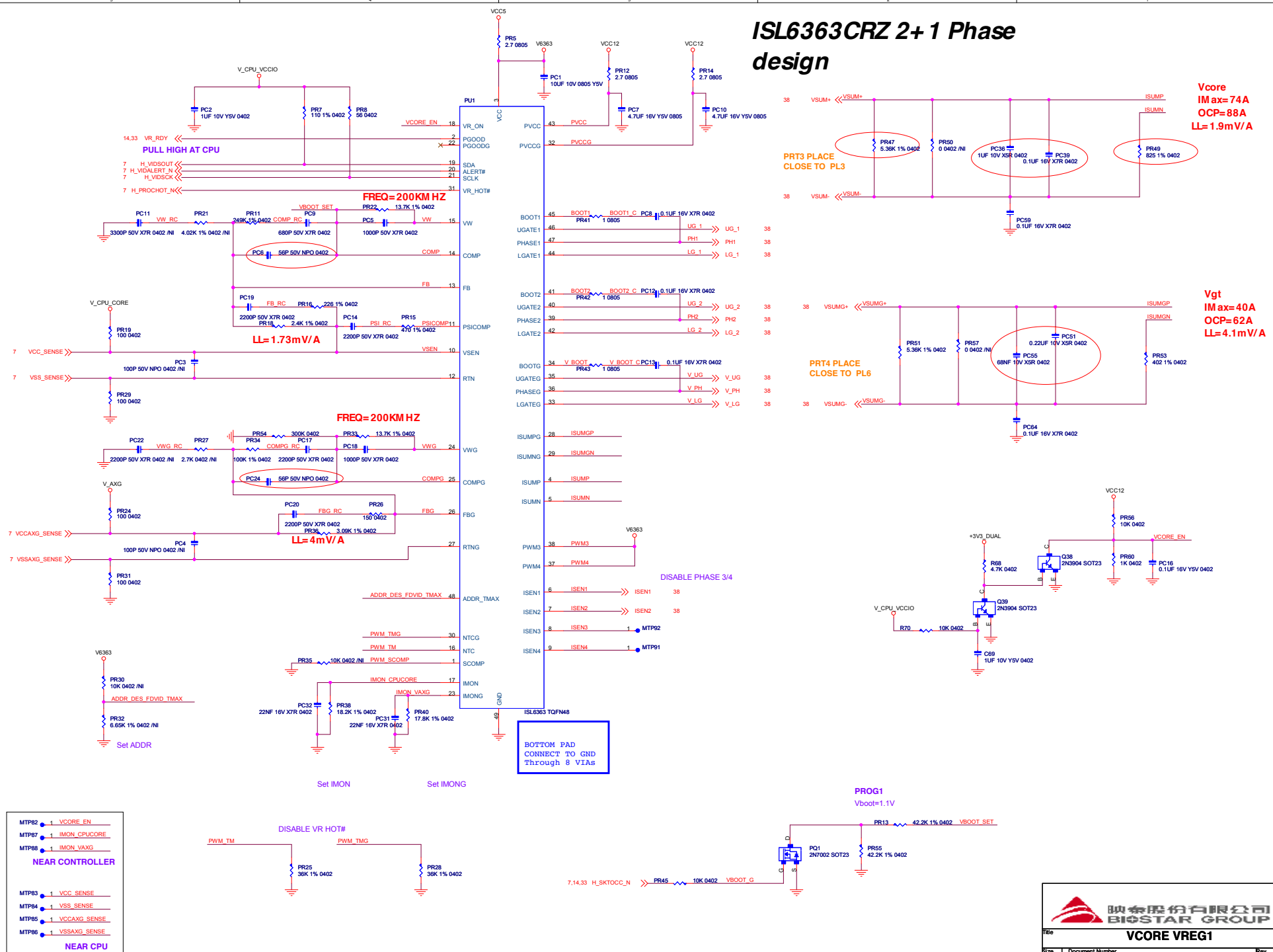
NETIN: 100UF 16V 5X11 2MM LR 6.3X5
BOM: 100UF 16V 5X11 2mm LR
100UF-S 16V 6.3X8 ELITE

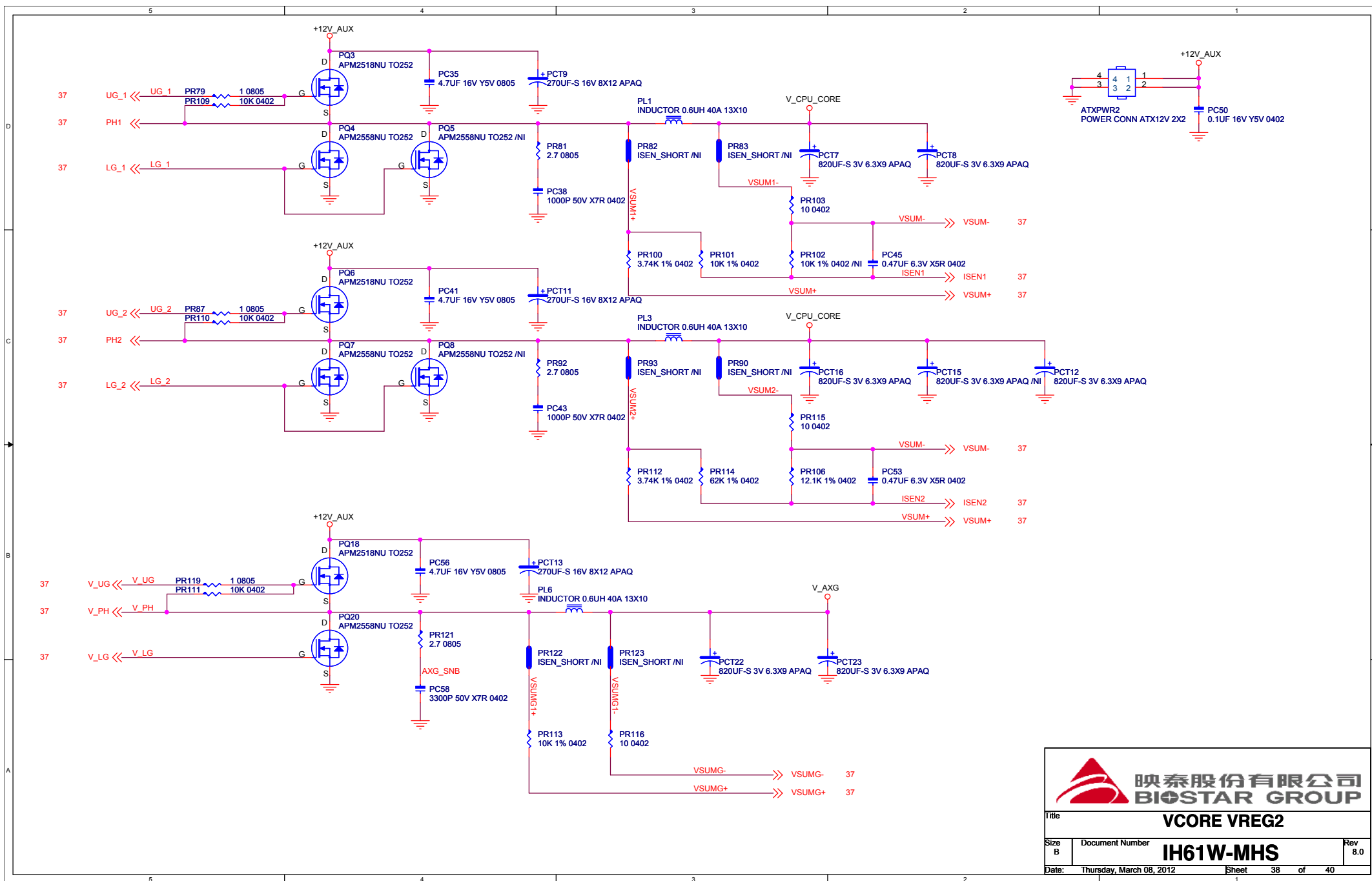
Title			
VSM DC-DC Conver			
Size	Document Number	Rev	
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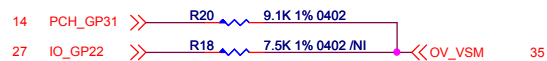


Title			
VTT DC-DC Conver			
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ISL6363CRZ 2+1 Phase design







V_CPU_CORE	OV_CPU0	OV_CPU1
DEFAULT	1	1
+5%	0	1
+10%	1	0
+15%	0	0

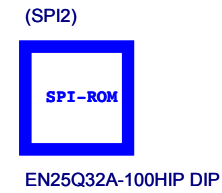
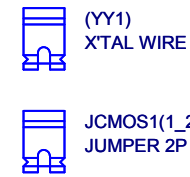
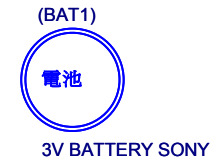
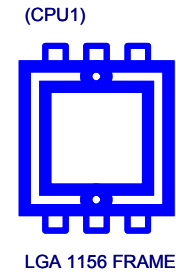
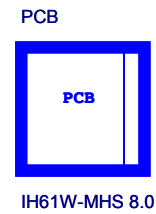
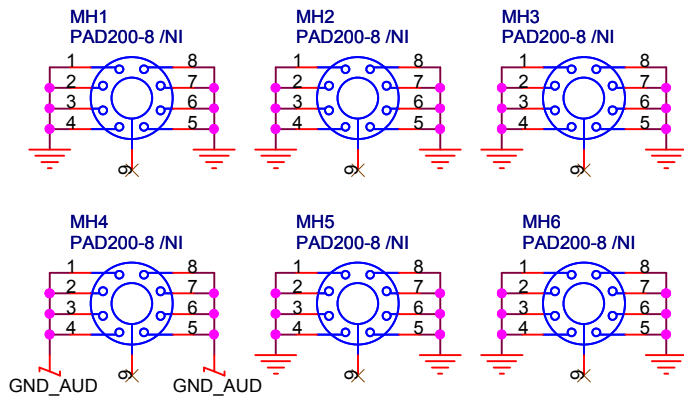
V_AXG	OV_AXG	OV_AXG1
DEFAULT	1	1
+5%	0	1

V_CPU_VCCIO	OV_VCCIO0	OV_VCCIO1
1.05V(DEFAULT)	1	1
1.1V	0	1
1.15V	1	0
1.2V	0	0

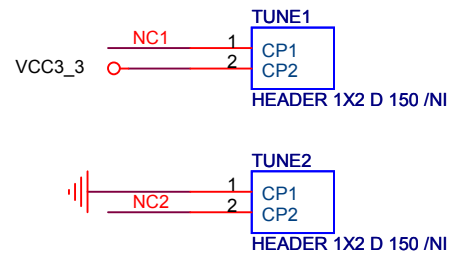
V_SM	OV_VSM0
1.5V(DEFAULT)	1
1.6V	0


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Impedance Testing Coupon



New PANEL1
PANEL1 2*8

YELLOW COLOR



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