

P2002

2GB GDDR5, 256b, 64Mx32

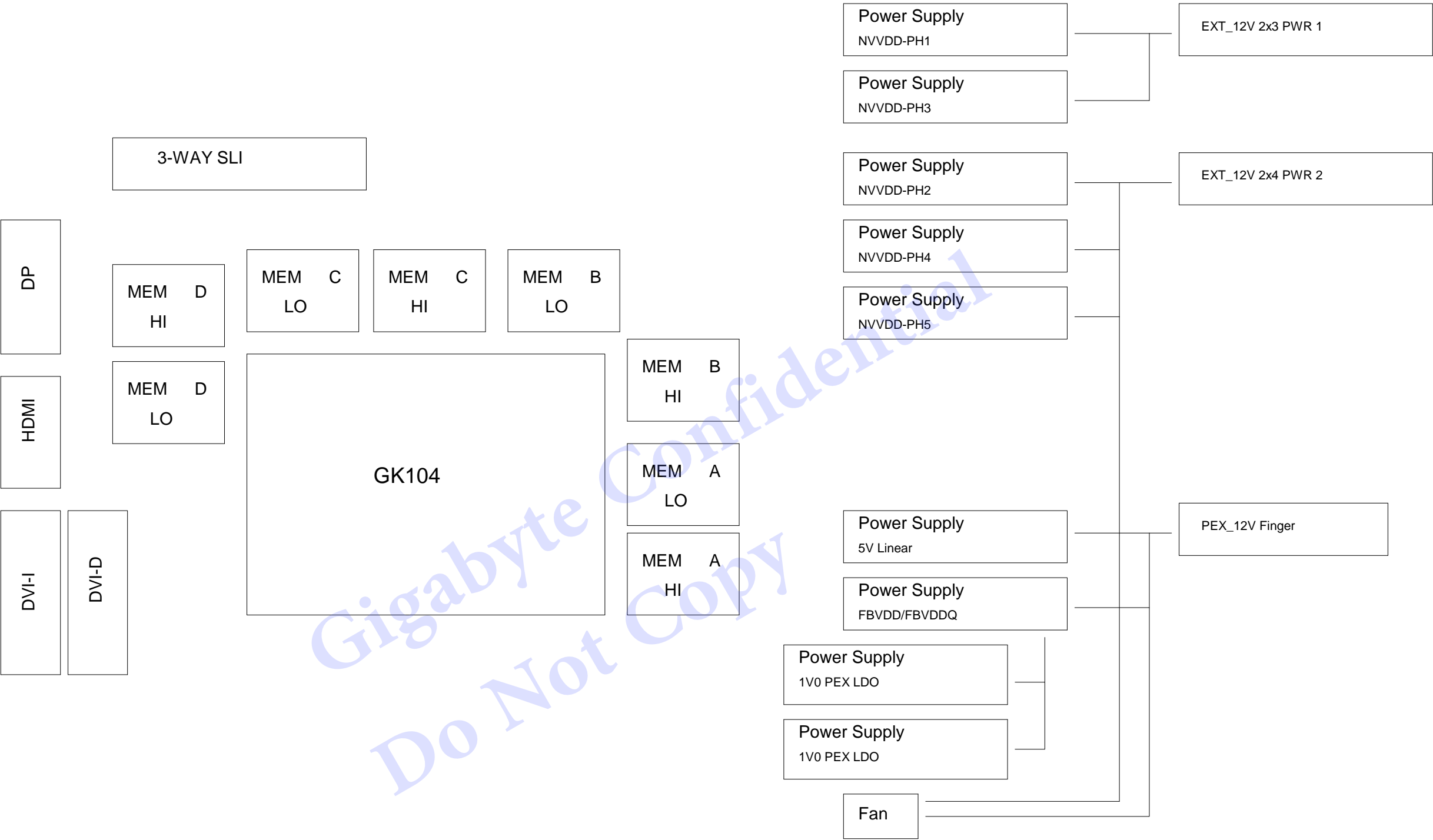
Stacked DVI-I/DVI-D + HDMI + DP

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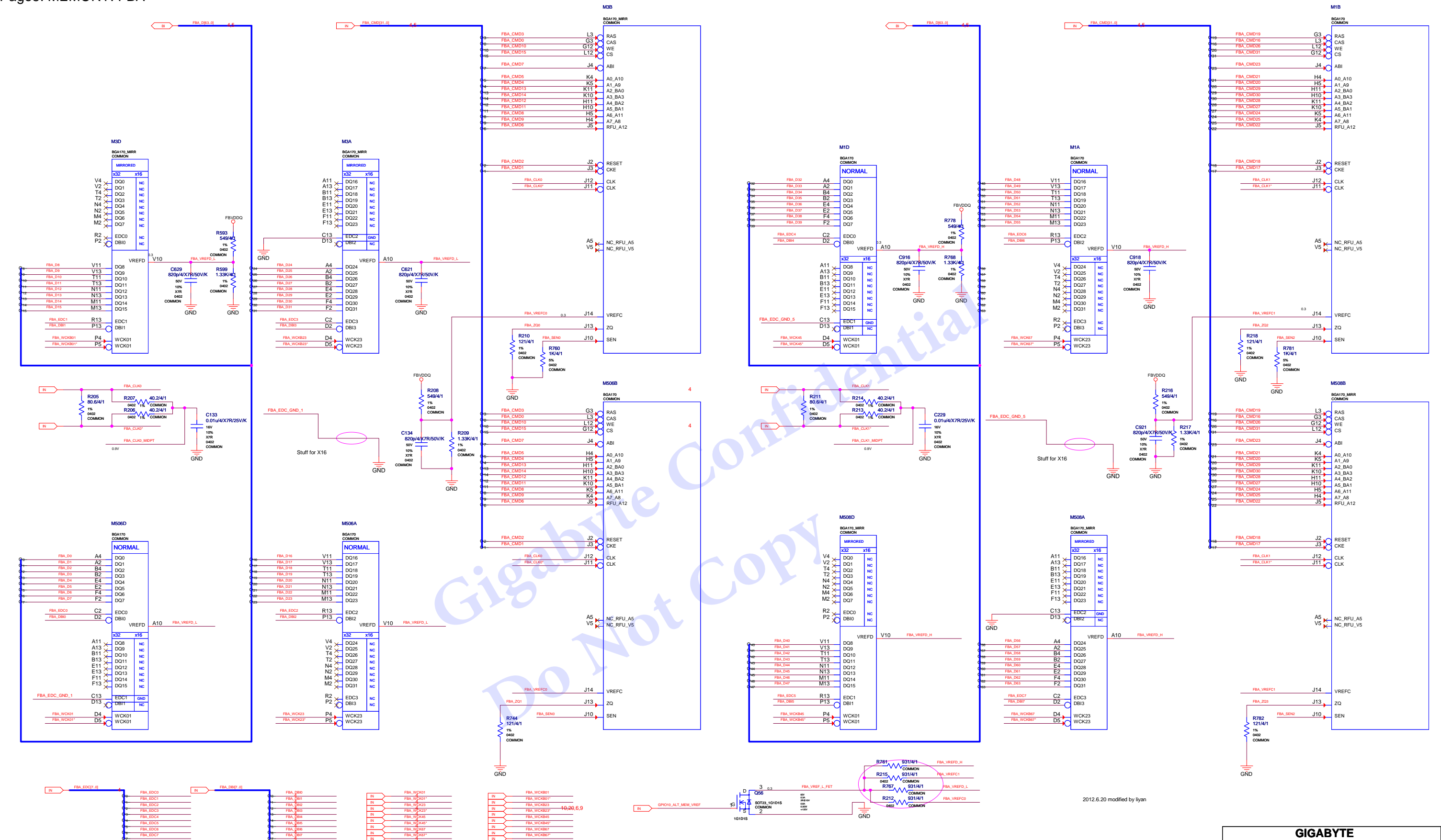
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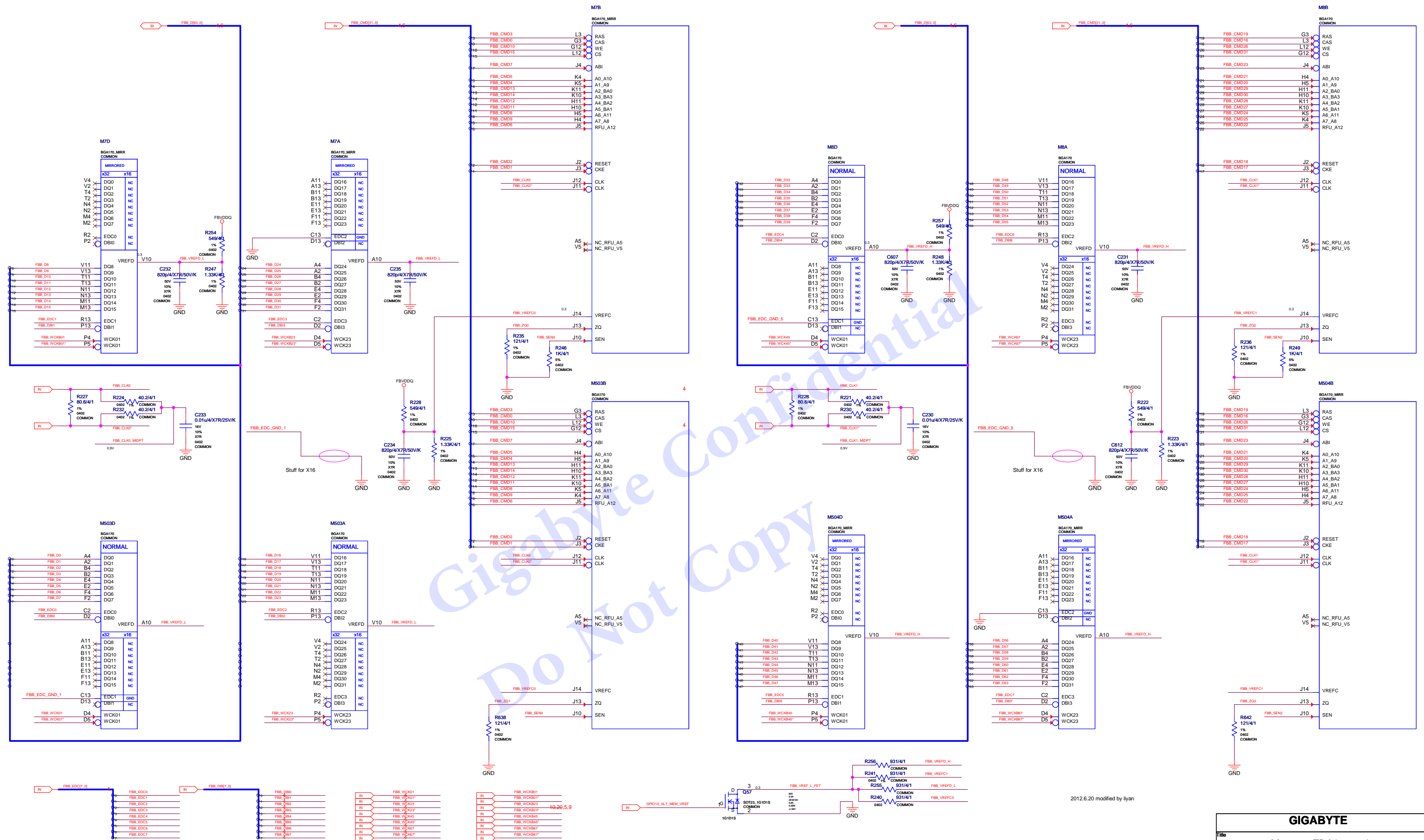




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Title			
PCIe Express			
Size Custom	Document Number GV-N770OC-4GD		Rev 2.0
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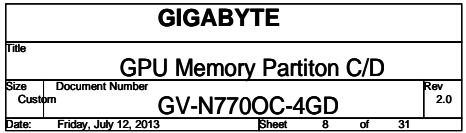


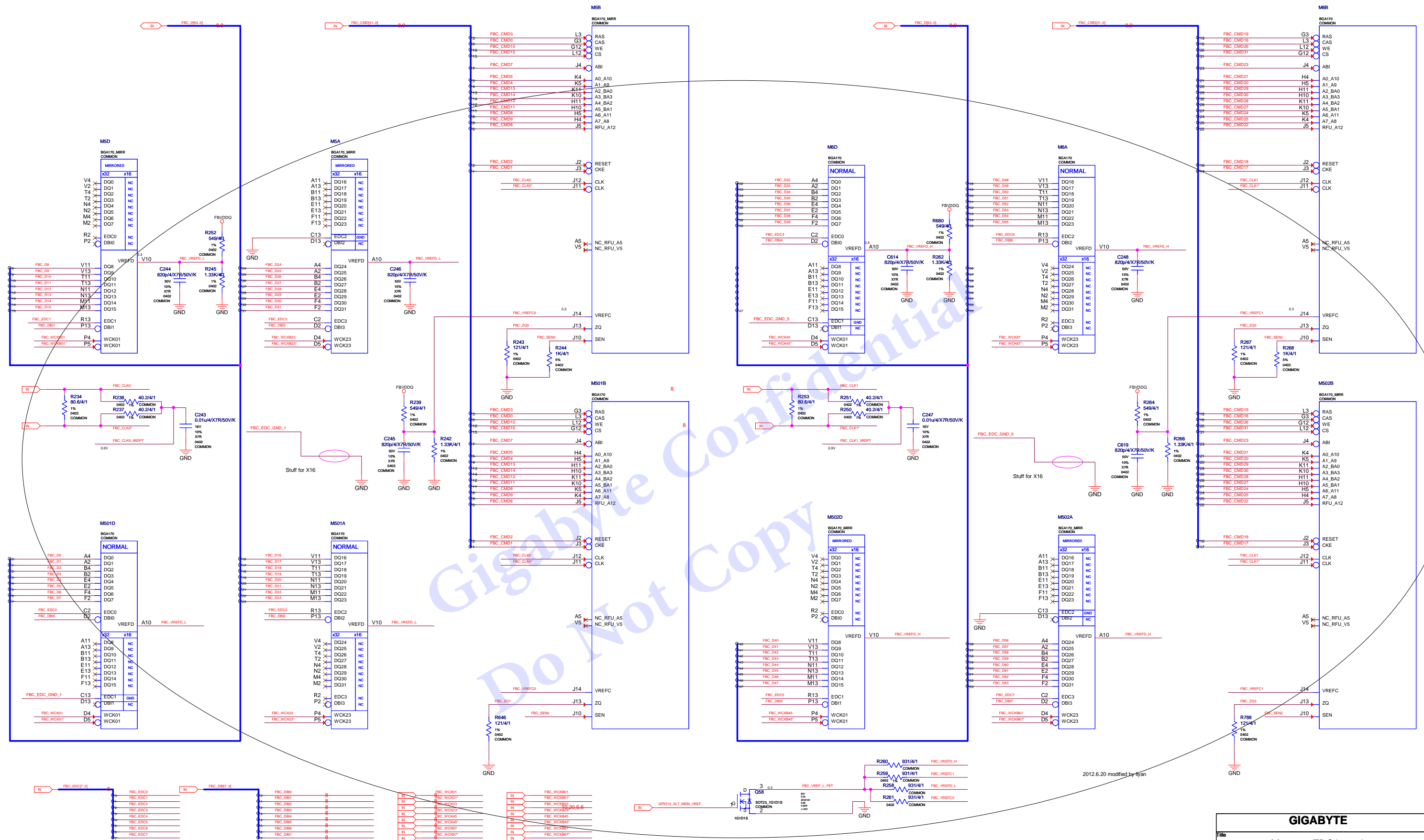
GIGABYTE			
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Memory FBA{0..31}			
Size	Document Number	Rev	
Custom	GV-N770OC-4GD	2.0	
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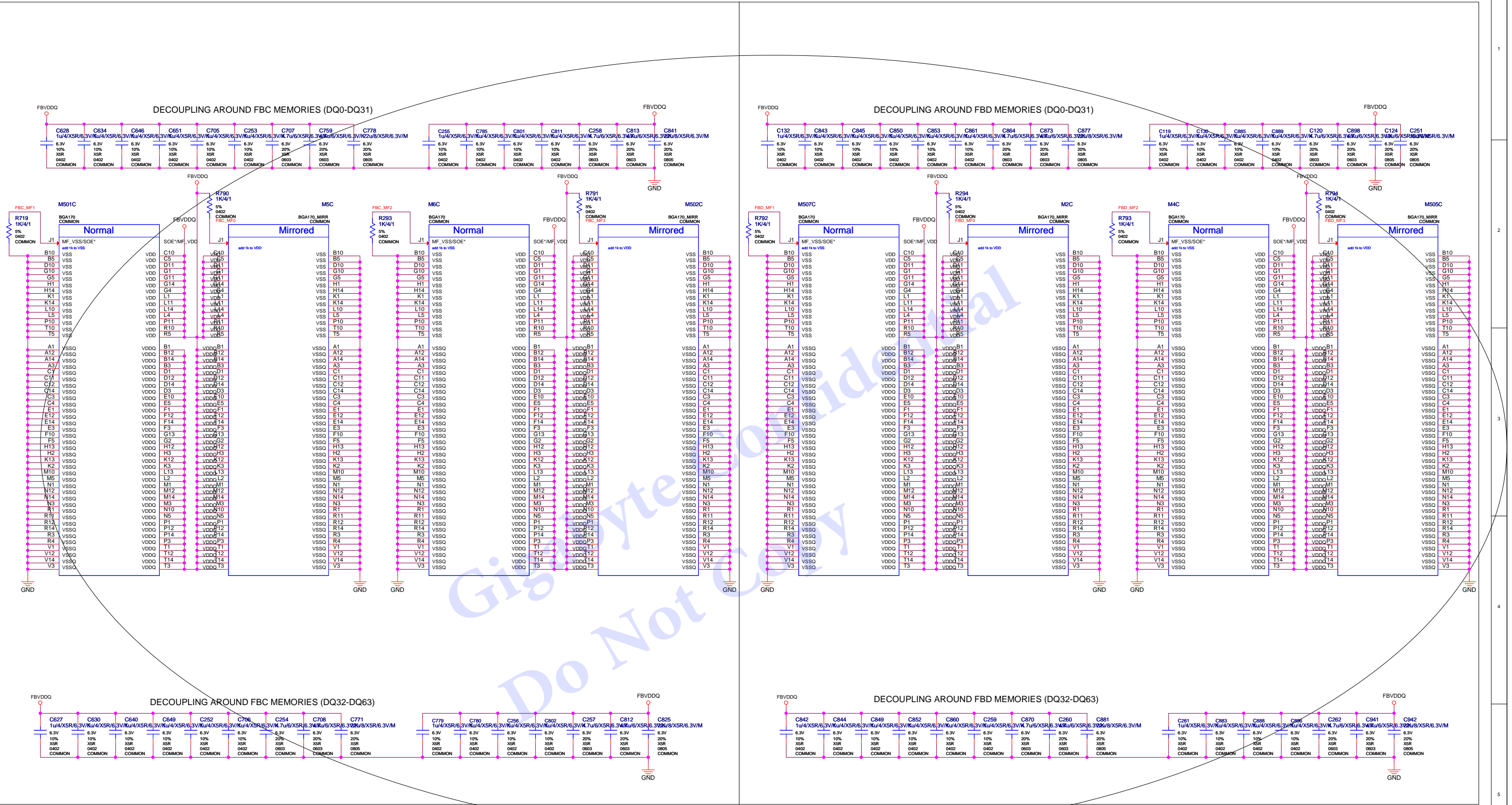




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Title			
Memory FBB{0..31}			
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Custom	GV-N7700C-4GD	2.0	
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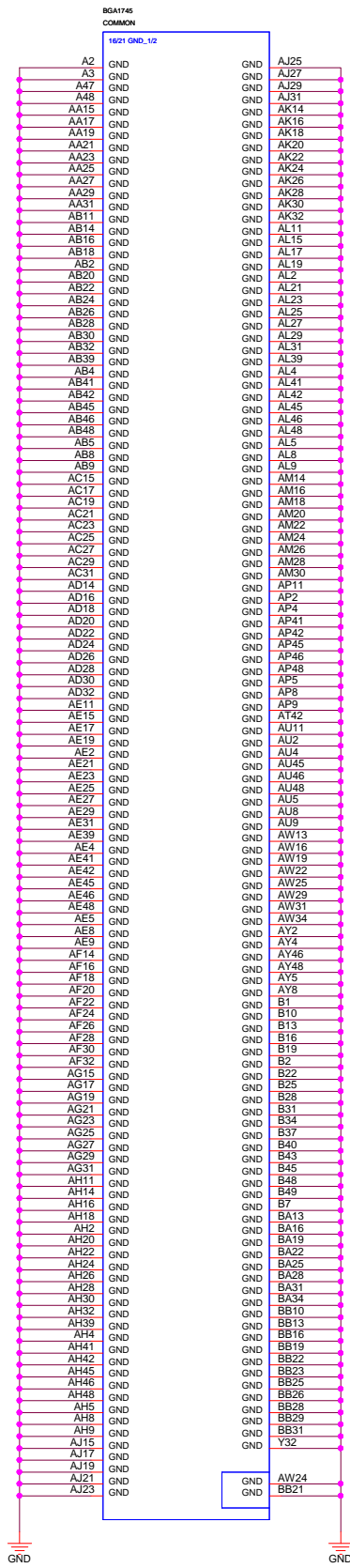




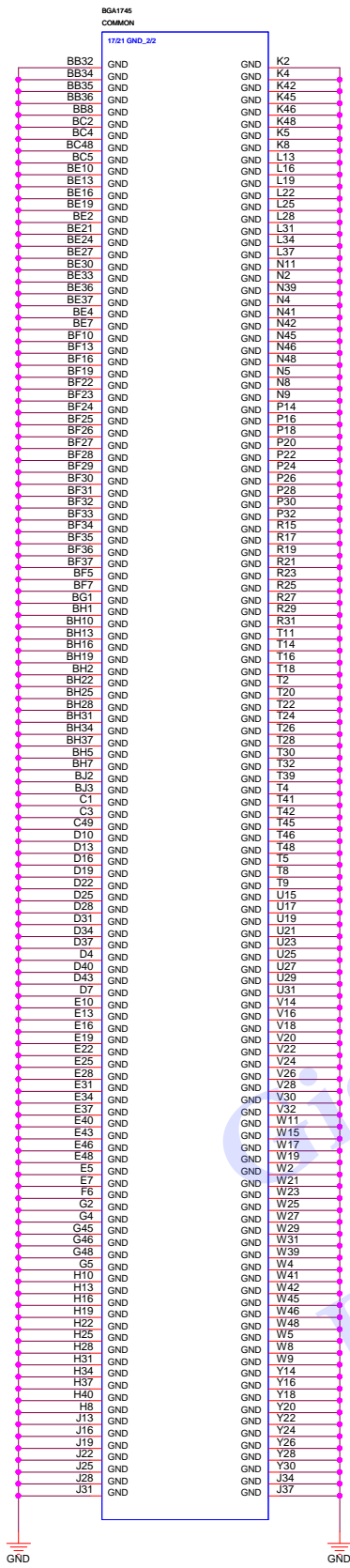
2012.6.20 modified by liyan

GIGABYTE			
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Memory FBD{0.31}			
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Custom	GV-N7700C-4GD	2.0	
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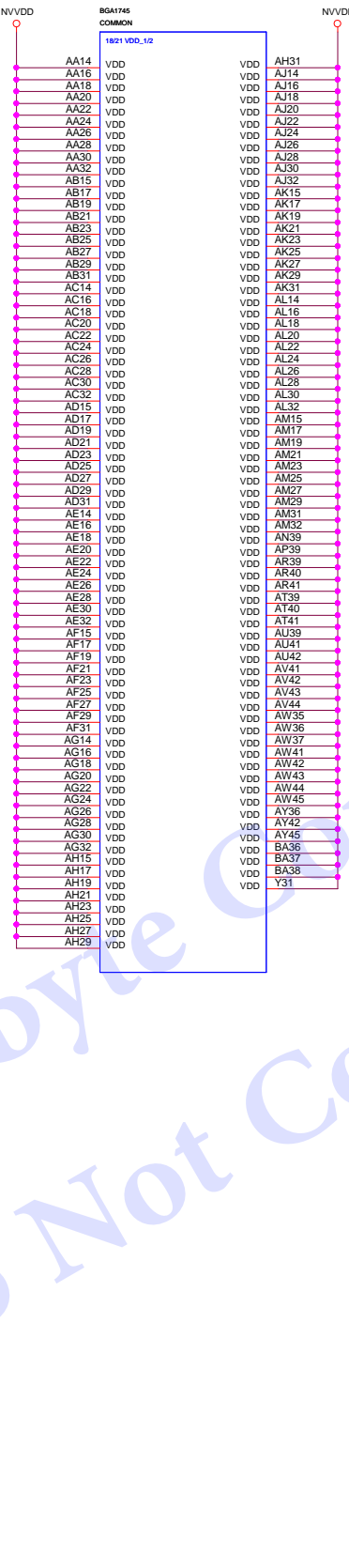
G1F



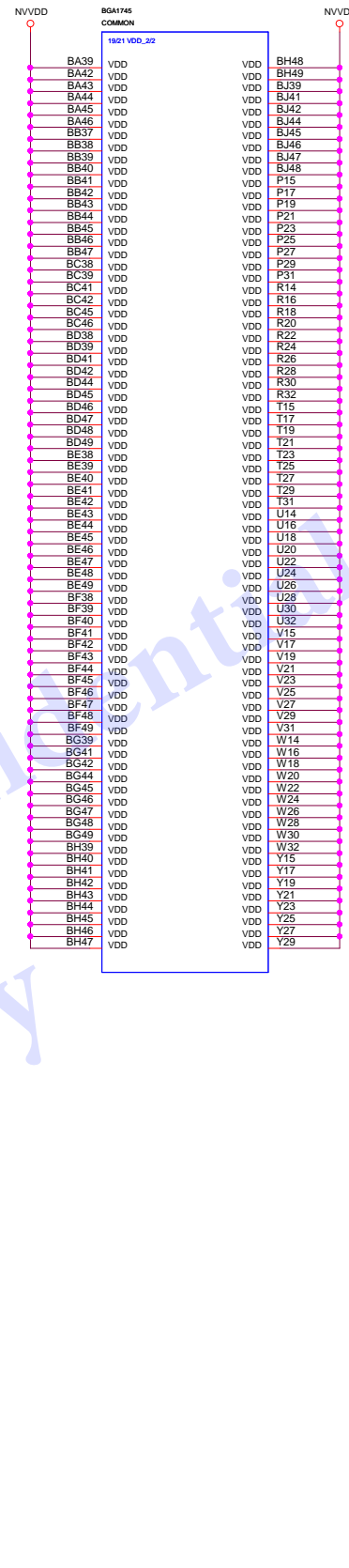
G1G



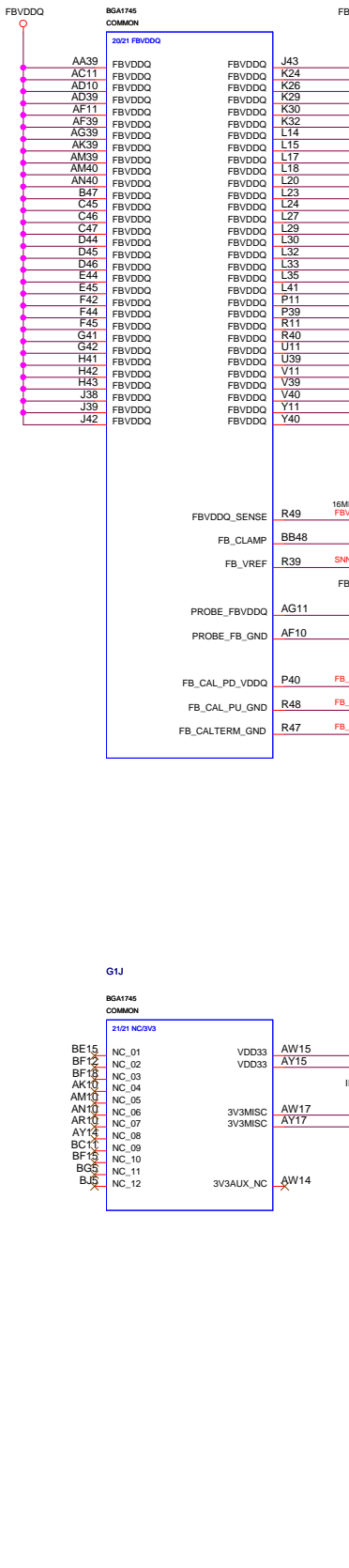
G1H



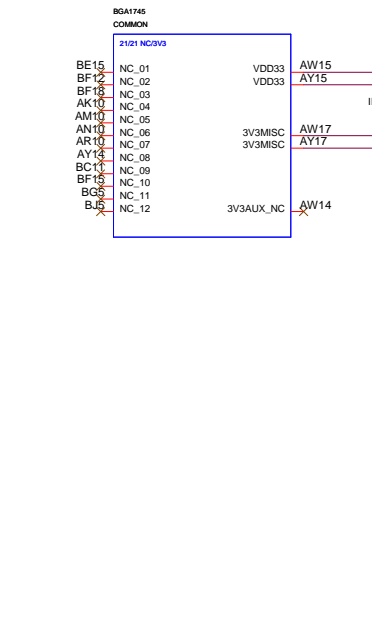
G1I



G1K



G1J



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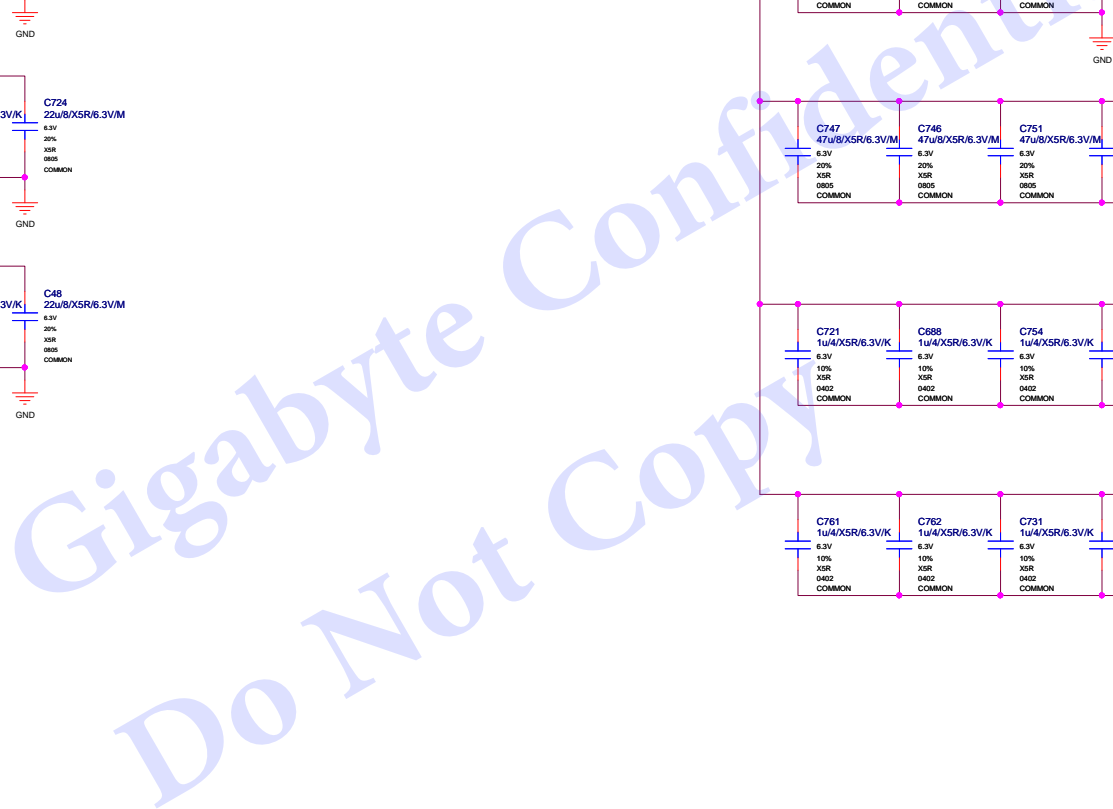
ASSEMBLY
PAGE DETAIL

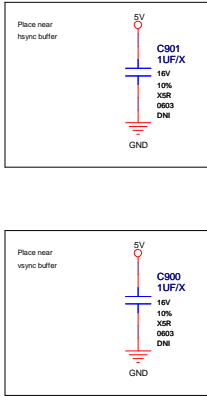
BASE LEVEL GENERIC SCHEMATIC ONLY
GPU PWR and GND

GIGABYTE

GPU PWR & GND			
Size	Document Number	Rev	
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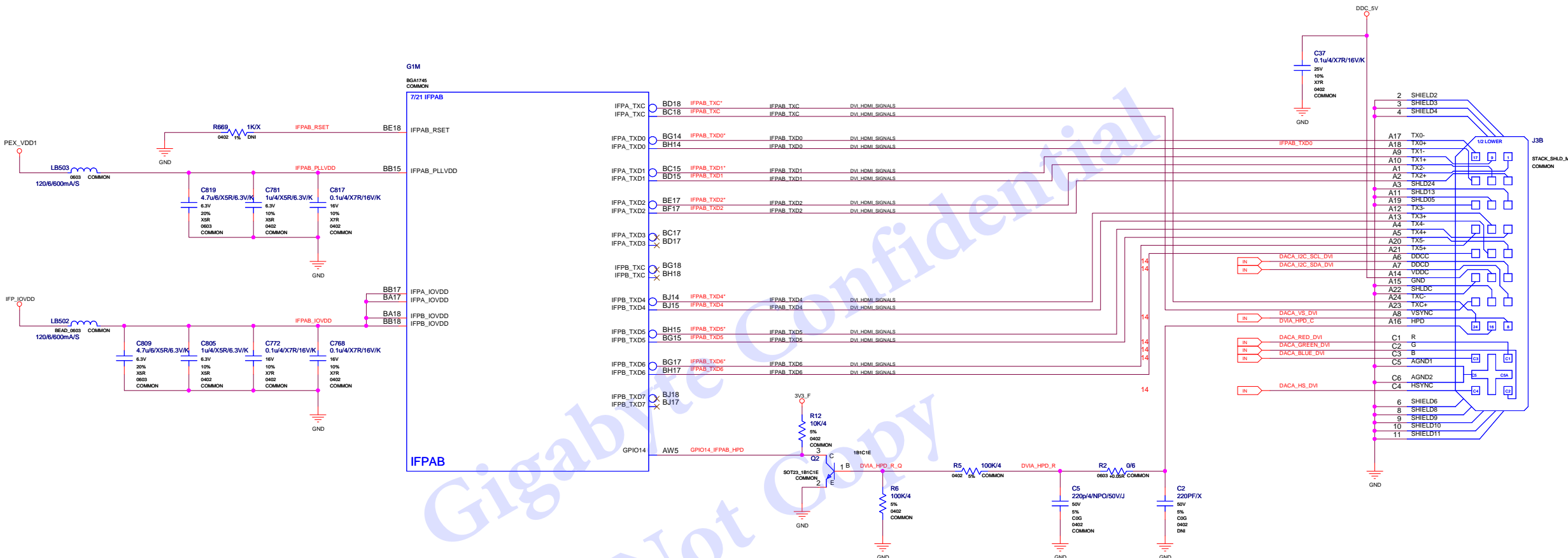
1 Based on GB2-X GDDR5 FBVDDQ Decap Guideline 1





GIGABYTE			
Title			
DACA Interface			
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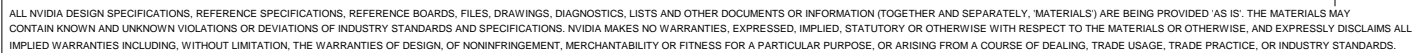


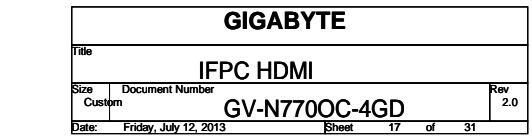
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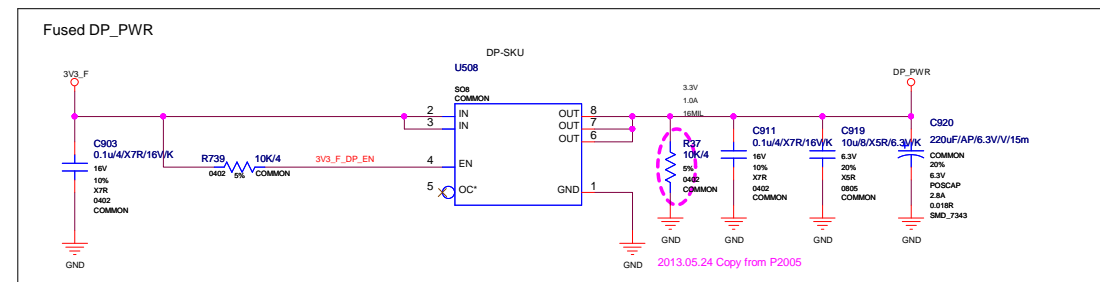
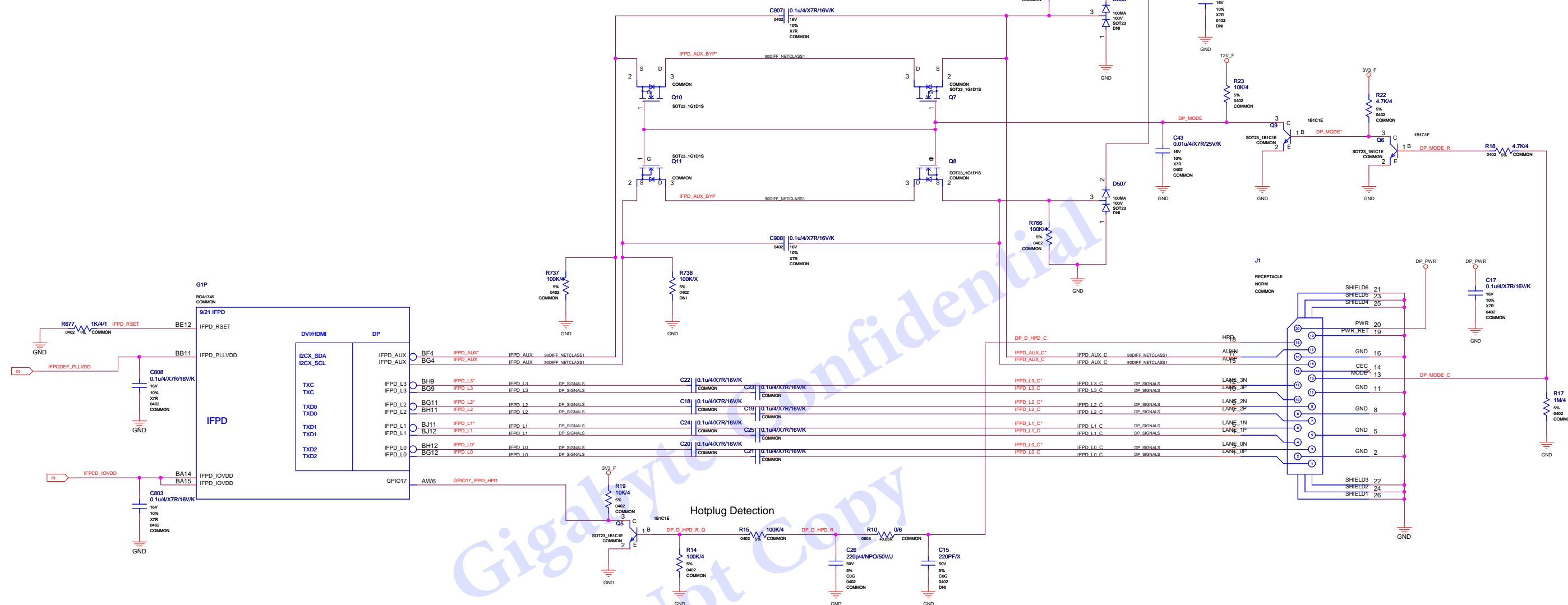
BASE LEVEL GENERIC SCHEMATIC ONLY
IFPAB DVI-I-DL

GIGABYTE			
Title		IFPAB DVI-DL	
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Custom	GV-N770OC-4GD	2.0	
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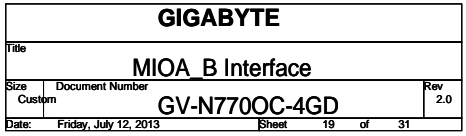


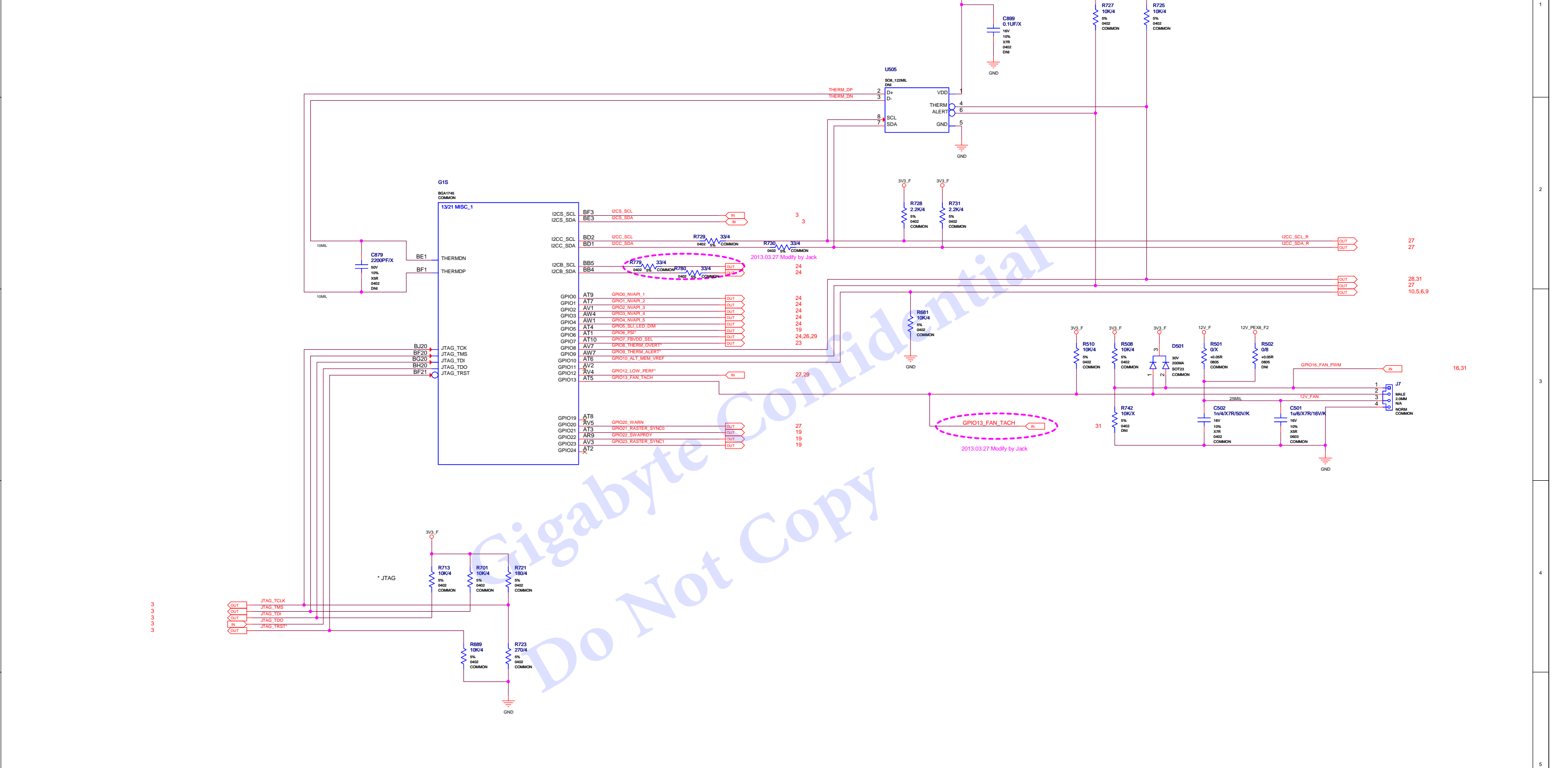
The schematic diagram illustrates a DP-to-LAN interface circuit. It includes two DP connectors (J1 and J2) and a LAN connector (J3). The circuit features two 181C1E transistors (Q9 and Q6) for signal conversion, various resistors (R23, R22, R18, R17), capacitors (C43, C909, C17), and diodes (D506, D507). The circuit is powered by DP_PWR and GND. Signal lines for DP_MODE, DP_MODE_R, DP_MODE_C, and DP_MODE_N are shown. The LAN connector J3 has pins for SHIELD6, SHIELD5, SHIELD4, PWR_RET, GND, CEC, MODEX, and LANE signals.



GIGABYTE			
Title			
IFPD DP			
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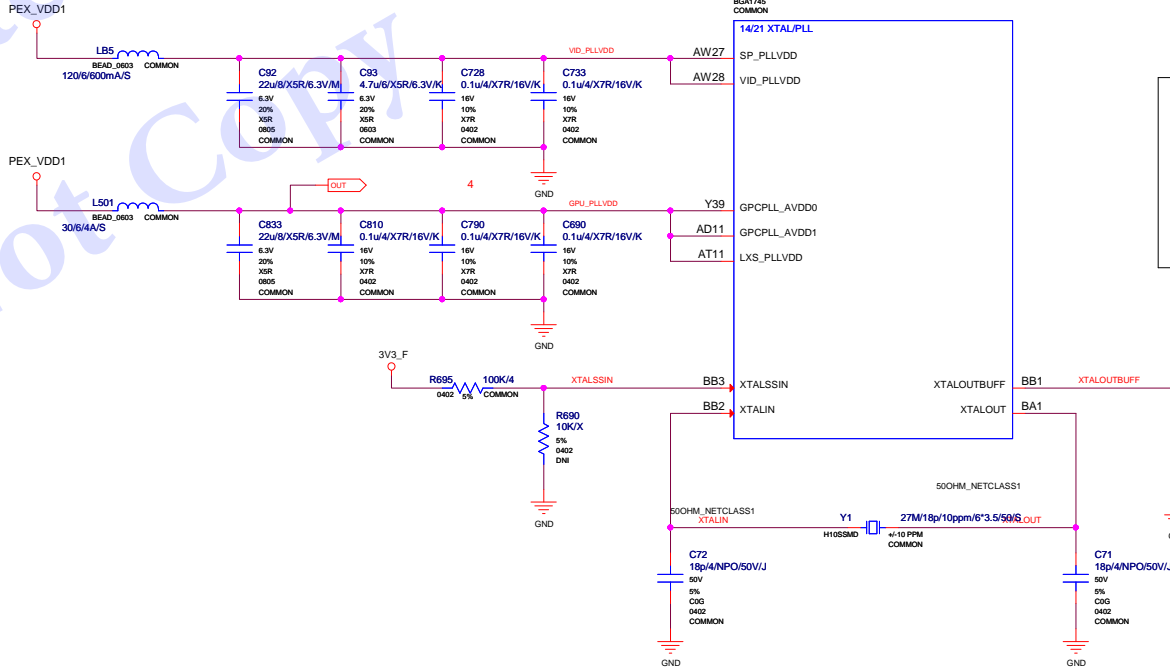
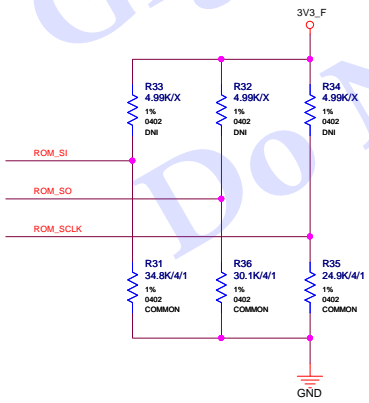
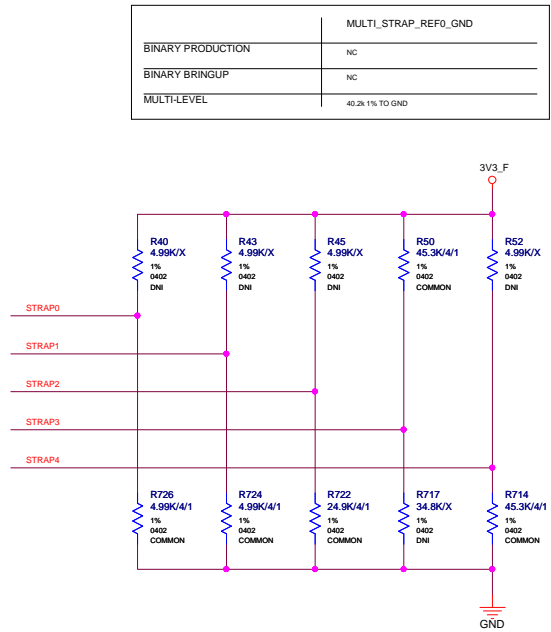
BASE LEVEL GENERIC SCHEMATIC ONLY
MISC1: Fan, Thermal, JTAG, GPIO

GIGABYTE			
Title			
FAN Thermal JTAG			
Size	Document Number	Rev	
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STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*	5K PD -400 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	0110 for 64Mx32 256 bit Hynix for SKU 0 primary memory
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	
	FB[0]_APERTURE_SIZE*	0* For 256MB*	10k PU*
	FB[1]_APERTURE_SIZE*	1* For 256MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLED*	
	PCI_DEVID_EXT[5]*	0* For 0x1180*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1180*	

GND			3V3
5k	0000	1000	
10k	0001	1001	
15k	0010	1010	
20k	0011	1011	
25k	0100	1100	
30k	0101	1101	
35k	0110	1110	
45k	0111	1111	

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Elpida
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Elpida
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Elpida
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Elpida
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung



Smart Fan		
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

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ASSEMBLY
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BASE LEVEL GENERIC SCHEMATIC ONLY
MISC2: ROM, XTAL, Straps

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Title			
ROM Xtal Straps			
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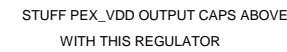
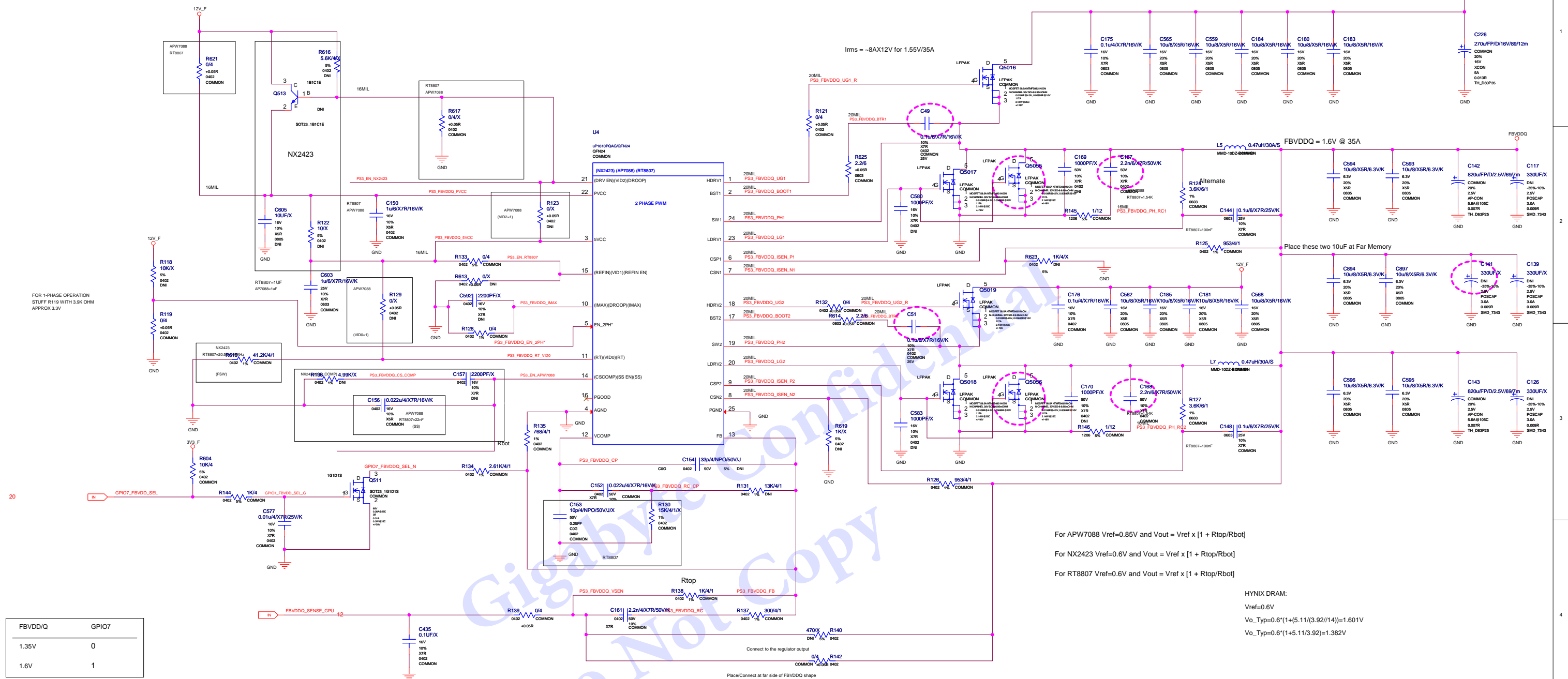
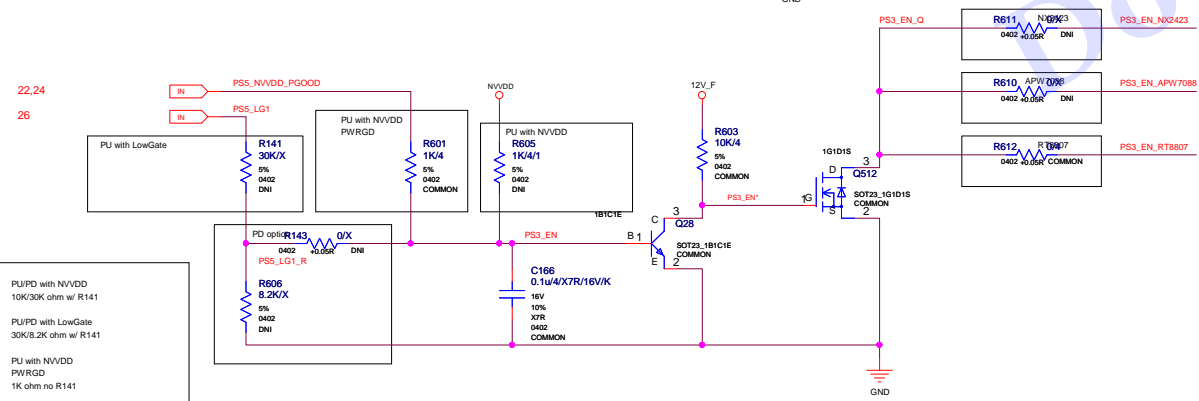


Diagram illustrating a horizontal line with four points marked by red circles. The labels above the line are: FBVDDQ, FBVDDQ, 30A, 20ML, and 1.6V. The labels below the line are: NETNAME, MAX_CURRENT, MIN_LINE_WIDTH, and VOLTAGE.



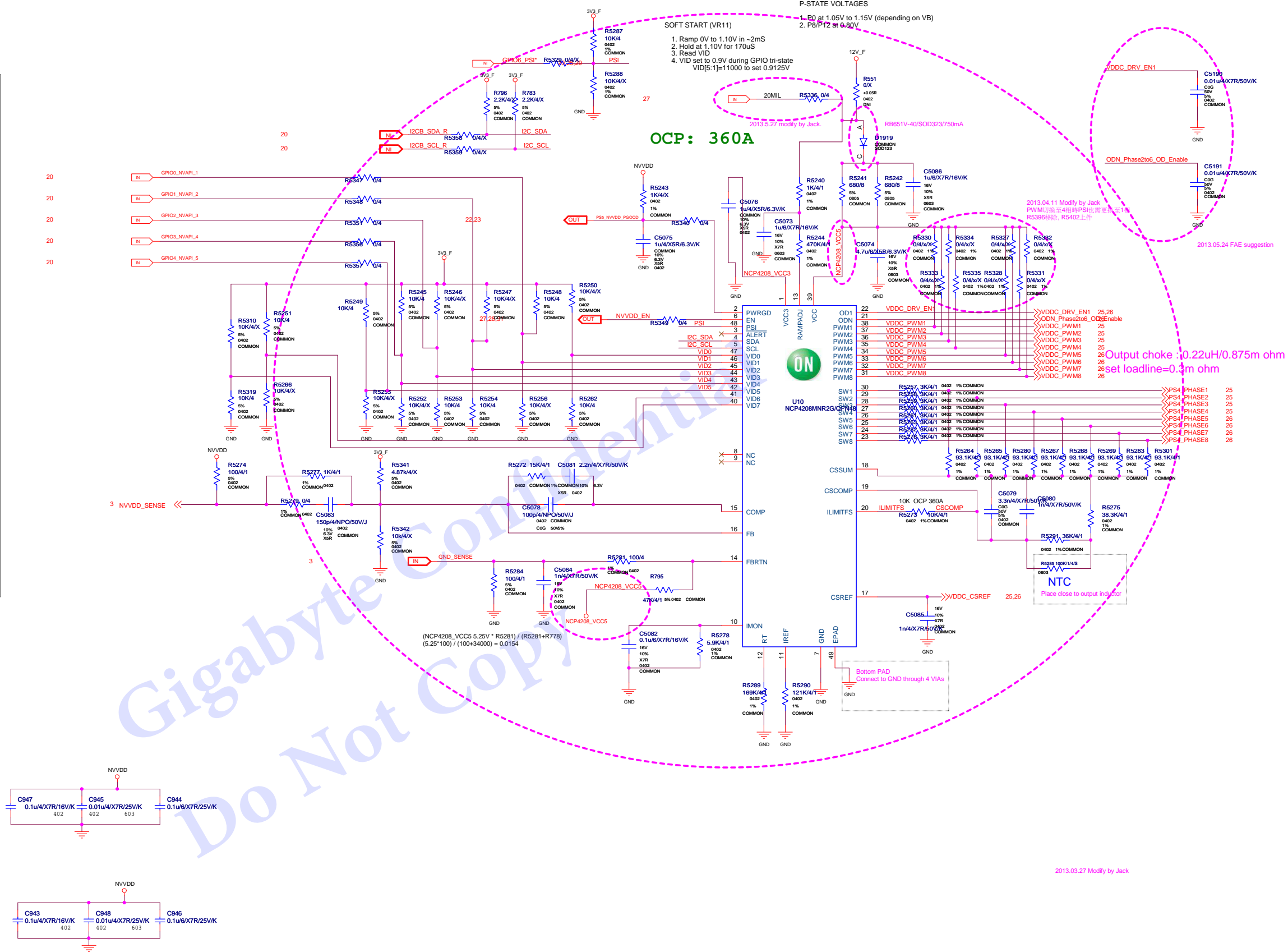
FBVDD/Q	GPIO7
1.35V	0
1.6V	1



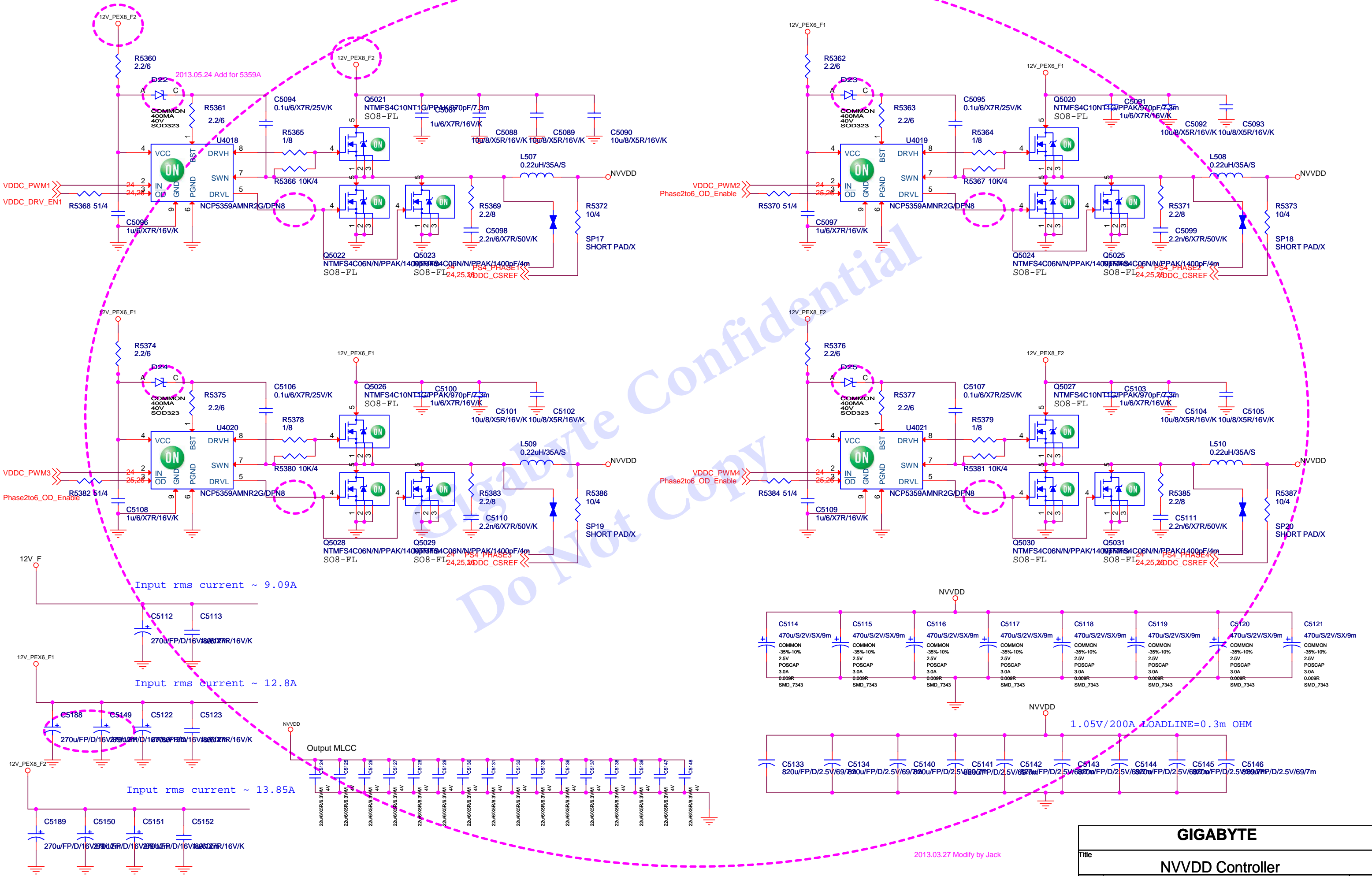
GIGABYTE			
Title			
FBVDDQ			
Size Custom	Document Number GV-N770OC-4GD		Rev 2.0
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VID Table

GPI07	GPI06	GPI05	GPI02	GPI017	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

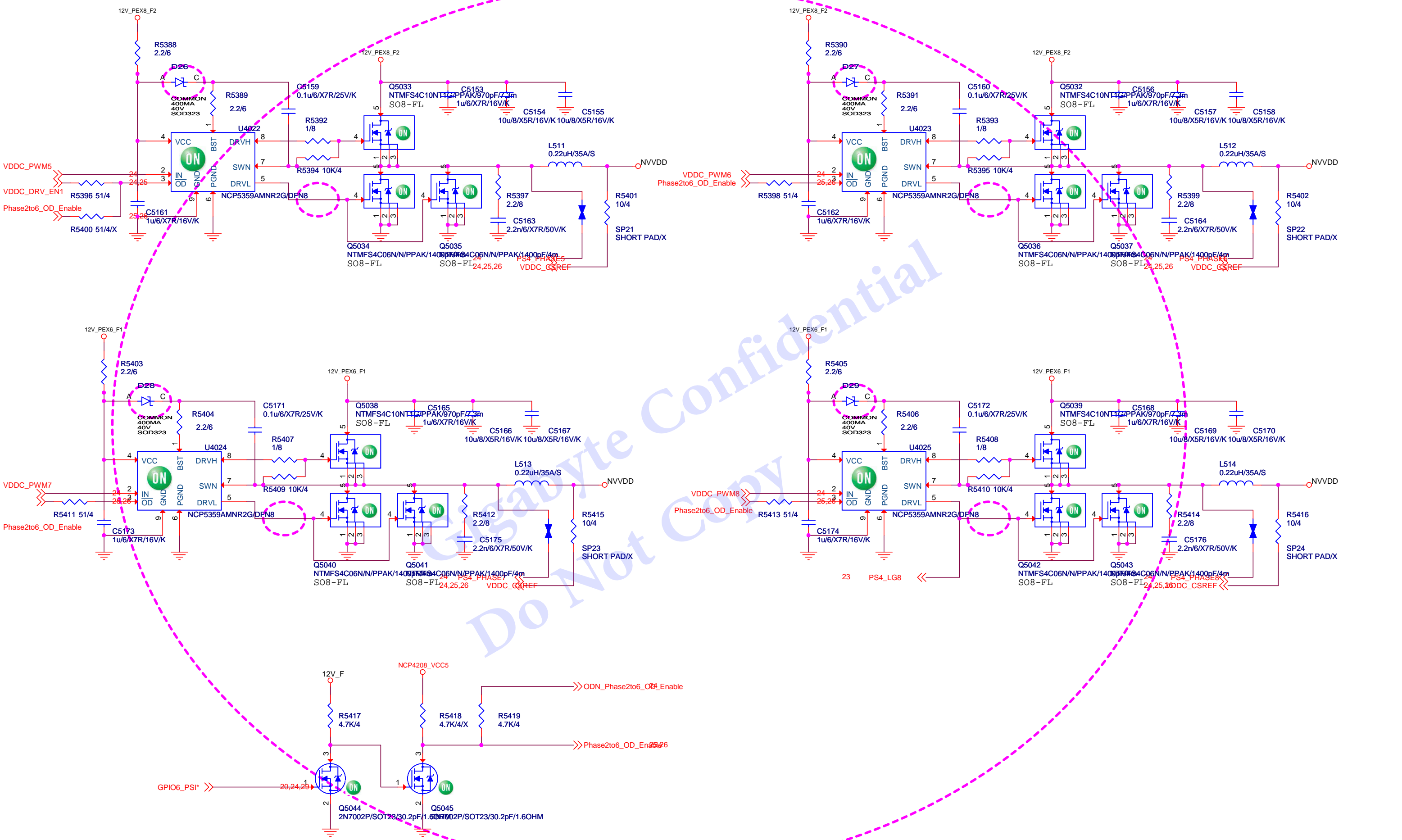


25_PS_ NVVDD Phase 1,2,3,4

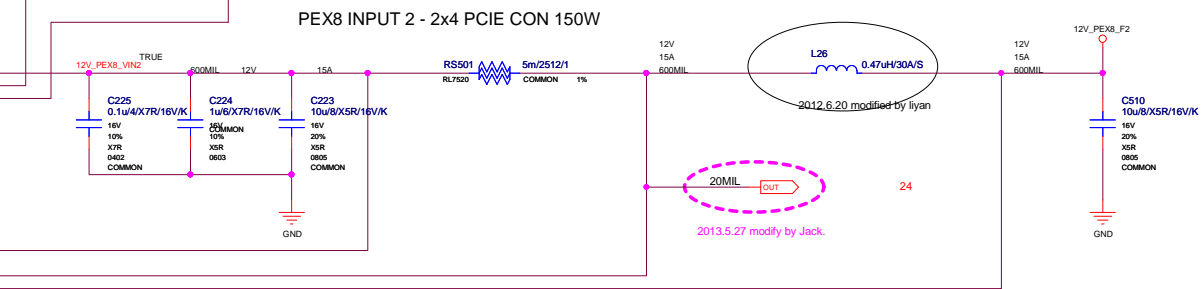
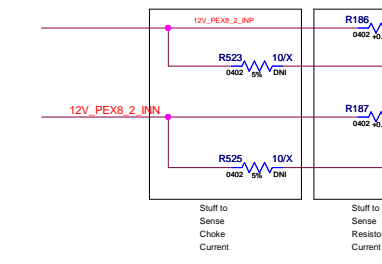


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Title			
NVVDD Controller			
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26_PS_ NVVDD Phase 5,6,7,8



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Title			
NVVDD Controller			
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GIGABYTE			
Title			
Input Filtering Monitoring			
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Custom			
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THERM OVERT SHUTDOWN LATCH

IFP_IOVDD (backdrive prevention)

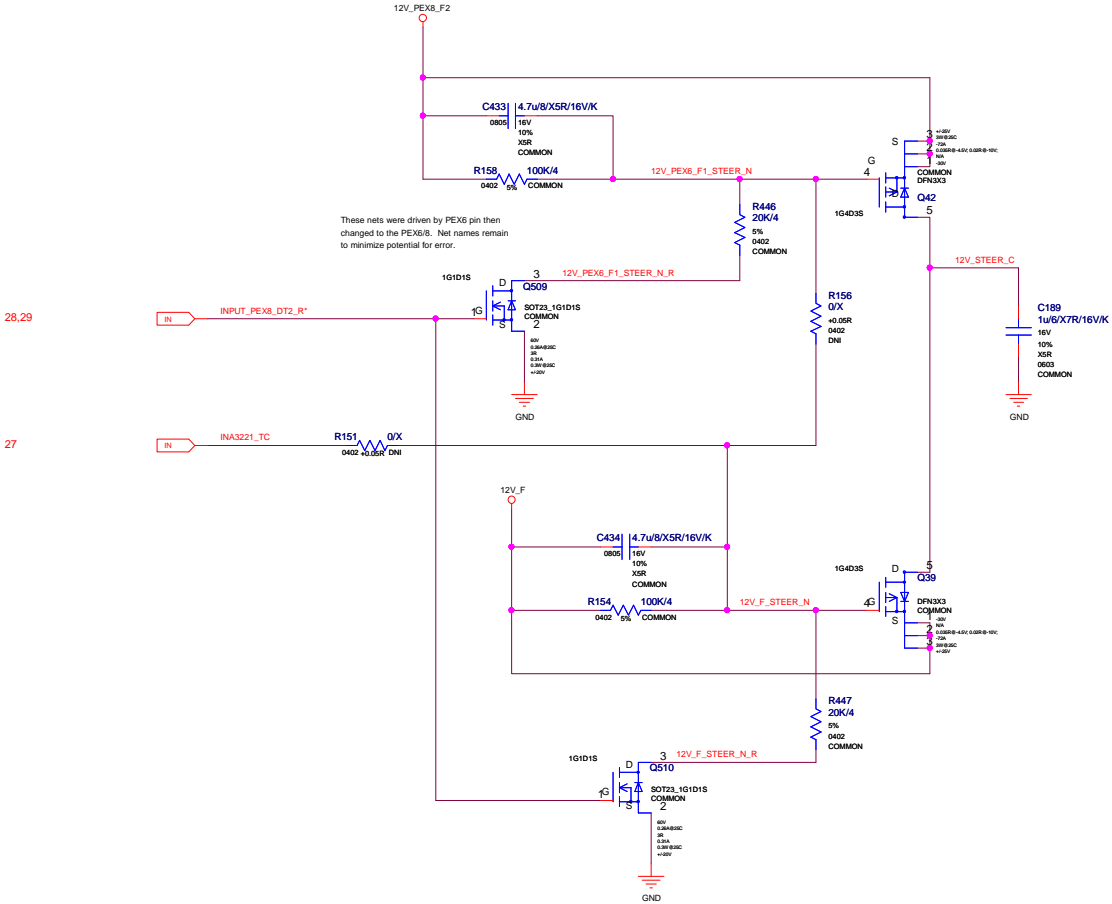
PEX Input - NVVDD Power Sequence

POWER CONNECTOR HPD

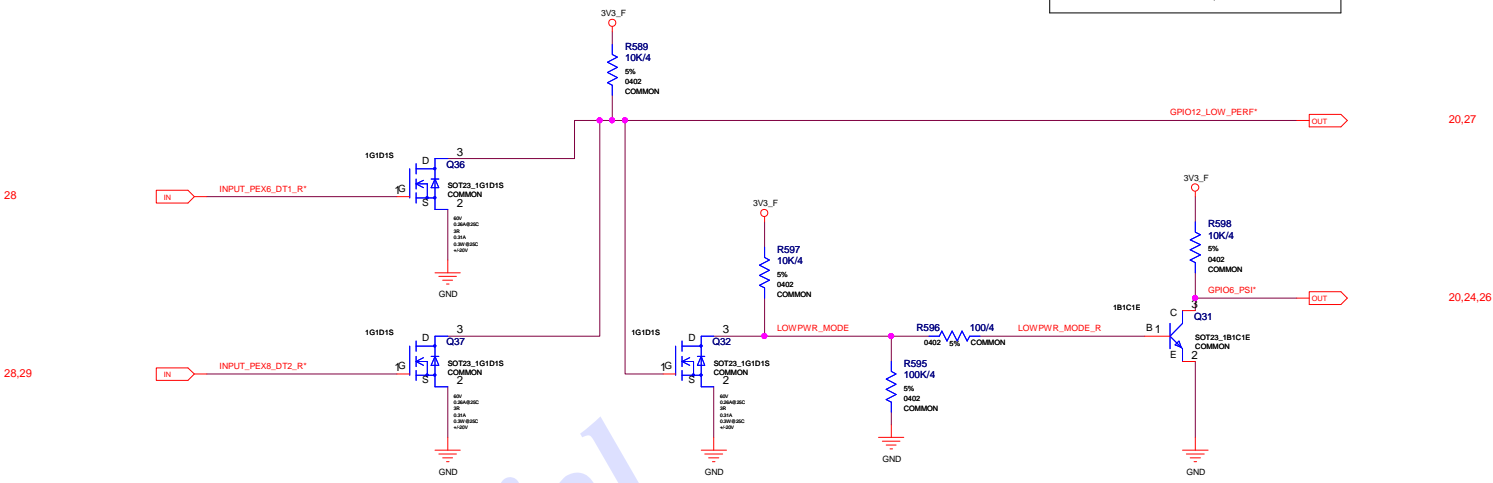
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GIGABYTE			
Title	Shutdown		
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PEX Input - 12V Current Steering FETs



PEX Input - Power Level/PSI* Control

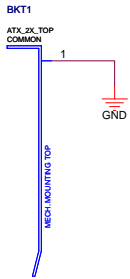


GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

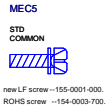
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GIGABYTE			
Title			
12V Current Steering, PSI Control, and LED			
Size	Document Number	Rev	
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Brackets:



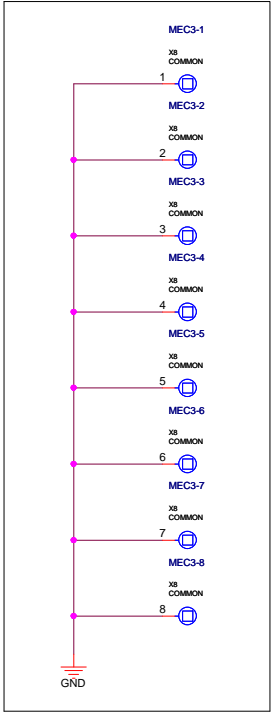
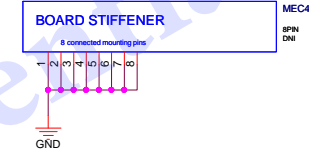
Bracket Screw



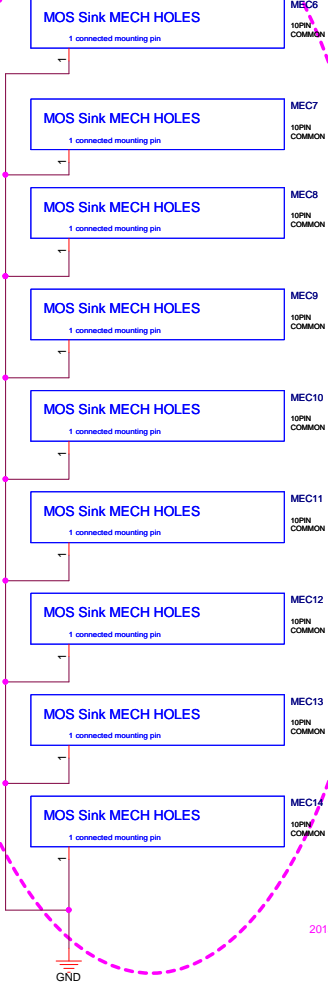
Hockey Stick



GPU Stiffner



Mechanical Holes Symbol



2013.04.02 Add new MOSFET Sink, Modify by Jack

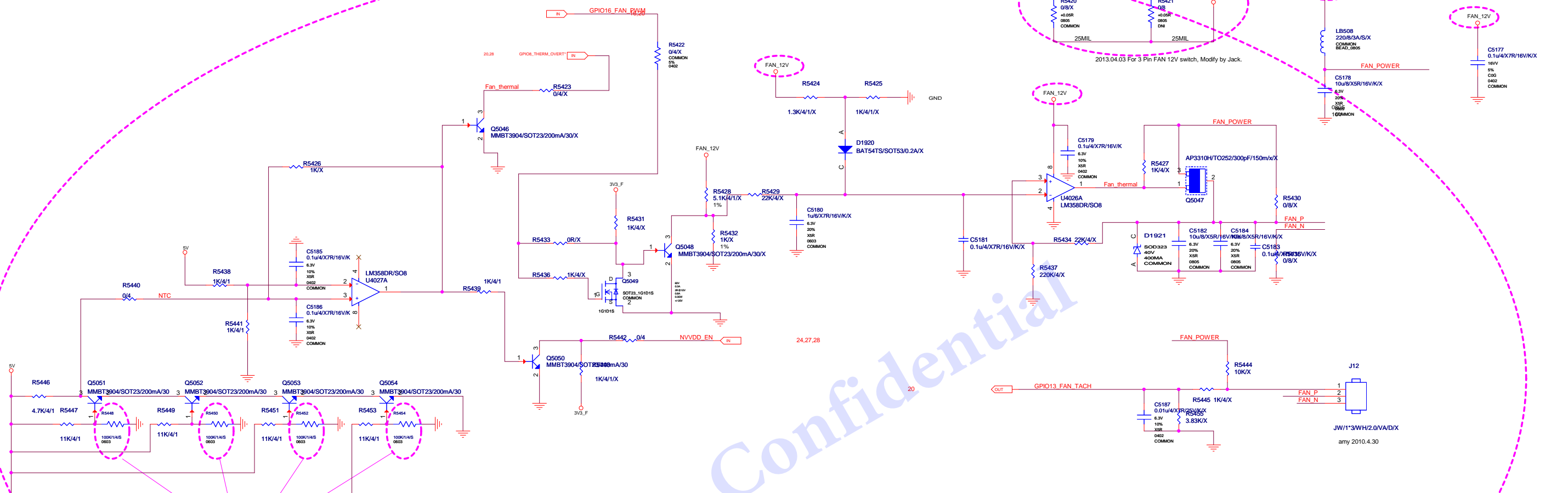
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31_ Thermal_3 Pin Fan



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ASSEMBLY PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY
Straps, Thermal, Mechanical

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