## Schematics Page Index (Title / Revision / Change Date)

| Page | Title of Schematics Page | Rev. | Date | Page | Title of Schematics Page | Rev. | Date |
|---|---|---|---|---|---|---|---|
| 01 | Schematics Page Index | 1.00 | 060311 | 36 | Flash ROM/XBUS | 1.00 | 060311 |
| 02 | Block Diagram | 1.00 | 060311 | 37 | Mini-PCIE Card | 1.00 | 060311 |
| 03 | Yonah(HOST BUS) 1/2 | 1.00 | 060311 | 38 | FAN/HW THERMAL PROTECT | 1.00 | 060311 |
| 04 | Yonah(HOST BUS) 2/3 | 1.00 | 060311 | 39 | EXPRESS/CAM/OIDE | 1.00 | 060311 |
| 05 | Yonah(Power/Gnd) 3/3 | 1.00 | 060311 | 40 | AUDIO(CODEC & POWER) | 1.00 | 060311 |
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| 07 | CALISTOG (DMI) 2/7 | 1.00 | 060311 | 42 | AUDIO( EXTMIC&LINE IN) | 1.00 | 060311 |
| 08 | CALIST (GRAPHIC) 3/7 | 1.00 | 060311 | 43 | AUDIO (MUTE & INTMIC) | 1.00 | 060311 |
| 09 | CALISTOGA (DDRII) 4/7 | 1.00 | 060311 | 44 | AUDIO( EQ ) | 1.00 | 060311 |
| 10 | CALIST (POWER,VCC) 5/7 | 1.00 | 060311 | 45 | AEC | 1.00 | 060311 |
| 11 | CALIST (VCC CORE) 6/7 | 1.00 | 060311 | 46 | PCI (PCI BUS) / TV-Tuner | 1.00 | 060311 |
| 12 | CALIST (VSS) 7/7 | 1.00 | 060311 | 47 | PCI ( 1LINK) | 1.00 | 060311 |
| 13 | DDRII(SO-DIMM 0) 1/3 | 1.00 | 060311 | 48 | PCI (MS-DUO/MDC) | 1.00 | 060311 |
| 14 | DDRII(SO-DIMM 1) 2/3 | 1.00 | 060311 | 49 | PCI ( PCMCIA) | 1.00 | 060311 |
| 15 | DDRII(Termination) 3/3 | 1.00 | 060311 | 50 | USB2.0 | 1.00 | 060311 |
| 16 | VGA(PCI-E/STRAP) 1/8 | 1.00 | 060311 | 51 | LAN (1/2) | 1.00 | 060311 |
| 17 | VGA(PCI-E/STRAP) 2/8 | 1.00 | 060311 | 52 | LAN (2/2) | 1.00 | 060311 |
| 18 | VGA(GDDR) 3/8 | 1.00 | 060311 | 53 | Power Design Diagram | 1.00 | 060311 |
| 19 | VGA(POWER) 4/8 | 1.00 | 060311 | 54 | Charger (MAX1909) | 1.00 | 060311 |
| 20 | VGA(POWER) 5/8 | 1.00 | 060311 | 55 | DCIN&BATTIN | 1.00 | 060311 |
| 21 | VGA(POWER) 6/8 | 1.00 | 060311 | 56 | SYSPWR(+3VALW/+5VALW) | 1.00 | 060311 |
| 22 | VGA(MULTIUSE) 7/8 | 1.00 | 060311 | 57 | SYSPWR(+1.5VRUN/+1.05VRUN) | 1.00 | 060311 |
| 23 | VGA(LVDS/VDAC ) 8/8 | 1.00 | 060311 | 58 | DDR2PWR(+1.8V BUS/+0.9VRUN | 1.00 | 060311 |
| 24 | VRAM(GDDR) 1/4 | 1.00 | 060311 | 59 | VHCORE(MAX8771) | 1.00 | 060311 |
| 25 | VRAM(GDDR) 2/4 | 1.00 | 060311 | 60 | Others power plan | 1.00 | 060311 |
| 26 | VRAM(POWERBYPASS) 3/4 | 1.00 | 060311 | 61 | OVP protection | 1.00 | 060311 |
| 27 | VRAM(POWERBYPASS) 4/4 | 1.00 | 060311 | 62 | VGA POWER(VGACORE&IO) | 1.00 | 060311 |
| 28 | LVDS | 1.00 | 060311 | 63 | CLOCK GEN | 1.00 | 060311 |
| 29 | ICH7-M( PCI/USB ) 1/5 | 1.00 | 060311 | 64 | HOLE/DB CONNS | 1.00 | 060311 |
| 30 | ICH7-M( LPC,IDE,SATA )2/5 | 1.00 | 060311 | 65 | CRT | 1.00 | 060311 |
| 31 | ICH7-M( GPIO) 3/5 | 1.00 | 060311 | 66 | History (EVT) | 1.00 | 060311 |
| 32 | ICH7-M( POWER) 4/5 | 1.00 | 060311 | 67 | History (DVT/PVT/MP) | 1.00 | 060311 |
| 33 | ICH7-M( GND) 5/5 | 1.00 | 060311 | | | | |
| 34 | SATA HDD/CD-ROM | 1.00 | 060311 | | | | |
| 35 | EC+KBC | 1.00 | 060311 | | | | |

| Value | MS50/GM | MS50/PM | MS30/GM | MS30/PM |
|---|---|---|---|---|
| MS30_ | | | V | V |
| MS50_ | V | V | | |
| GA_ | V | | V | |
| NV_ | | V | | V |
| NC_ | V | V | V | V |





| P. Leader | Check by | Design by |
|---|---|---|
| 4/6 | 4/6 | 4/6 |

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Title: Index Page

Size: Custom | Document Number: MS30-1-01 | Rev: 1.00

Date: Monday, April 03, 2006 | Sheet 1 of 67

**Project Code & Schematics Subject: MS30 Main Board** **PCB P/N: 1P-0063100-6011**

# Schematics Page Index (Title / Revision / Change Date)

| Page | Title of Schematics Page | Rev. | Date | Page | Title of Schematics Page | Rev. | Date |
|---|---|---|---|---|---|---|---|
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| 34 | SATA HDD/CD-ROM | 1.00 | 060311 | | | | |
| 35 | EC+KBC | 1.00 | 060311 | | | | |

| Value | MS50/GM | MS50/PM | MS30/GM | MS30/PM |
|---|---|---|---|---|
| MS30_ | | | V | V |
| MS50_ | V | V | | |
| CA_ | V | | V | |
| NV_ | | V | | V |
| NC_ | V | V | V | V |





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|---|---|---|
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**Project Code & Schematics Subject: MS30 Main Board** | **PCB P/N: 1P-0063100-6011**

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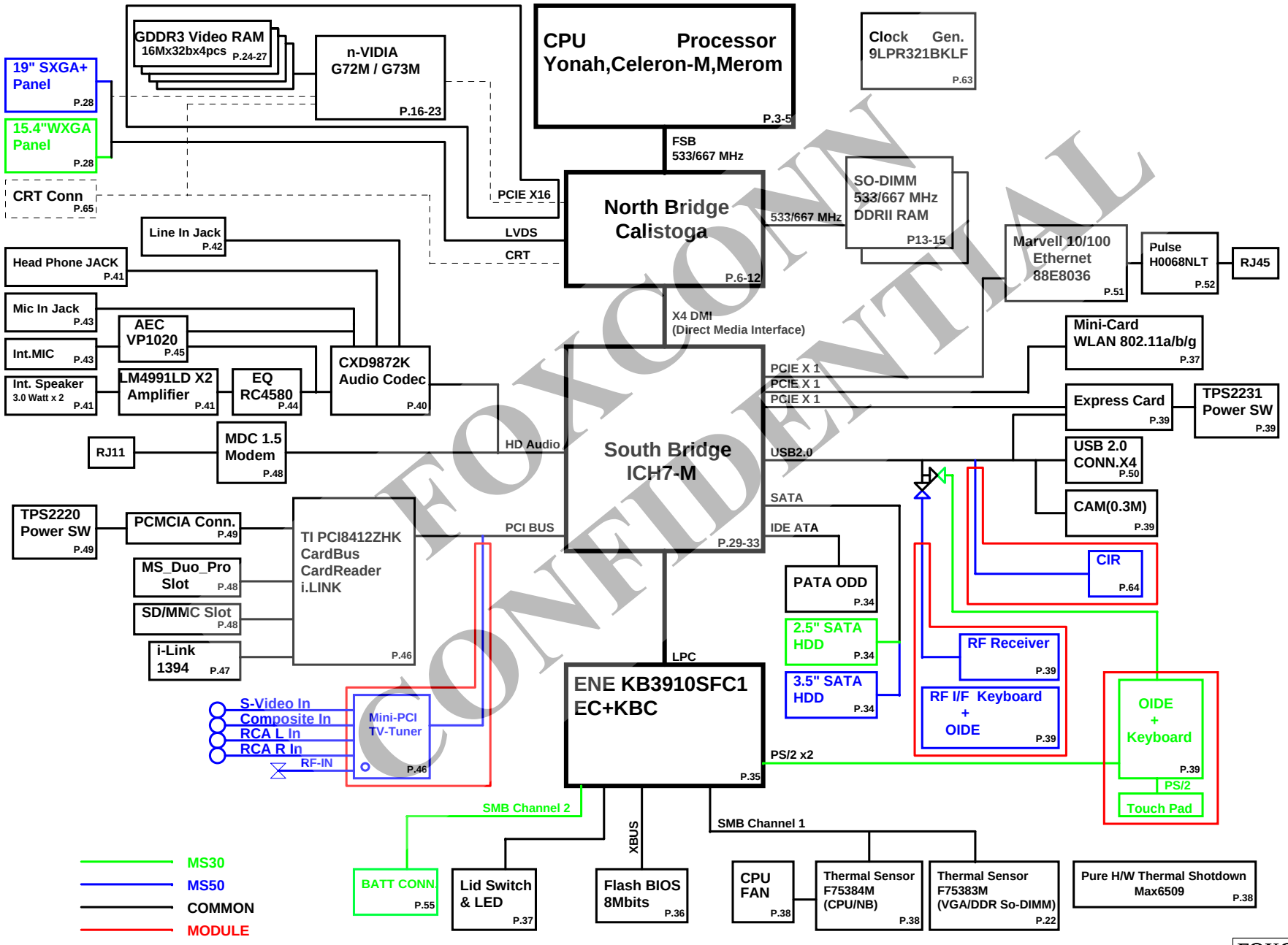
CPBG - R&D Division

Title: ***Index Page***

Size: Custom | Document Number: **MS30-1-01** | Rev: 1.00

Date: Monday, April 03, 2006 | Sheet 1 of 67

# MBX-152(CALISTOGA PM/GM+Gfx Block Diagram




| SYSTEM DC/DC MAX8734A P.56 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | +5VALW<br>+5VALW_LDO<br>+3VALW<br>+ECVCC |

| SYSTEM DC/DC MAX8743 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | +1_5VRUN<br>+1_05VRUN |
| SC486 | |
| DCBATOUT | +1_8VSUS<br>+0_9VRUN |

| CPU DC/DC MAX8771 P.59 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | VHCORE |

| AMP DC/DC MAX668 P.60 | |
|---|---|
| INPUTS | OUTPUTS |
| +5VALW | +12VRUN |

| SYSTEM DC/DC SC1470/GMT966 (external VGA Core) P.63 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT<br>+1_5VRUN | PEX_VDD<br>NV_VDD |

| MAXIM CHARGER MAX1909 P.54 | |
|---|---|
| INPUTS | OUTPUTS |
| AD+ | BT+<br>DCBATOUT |



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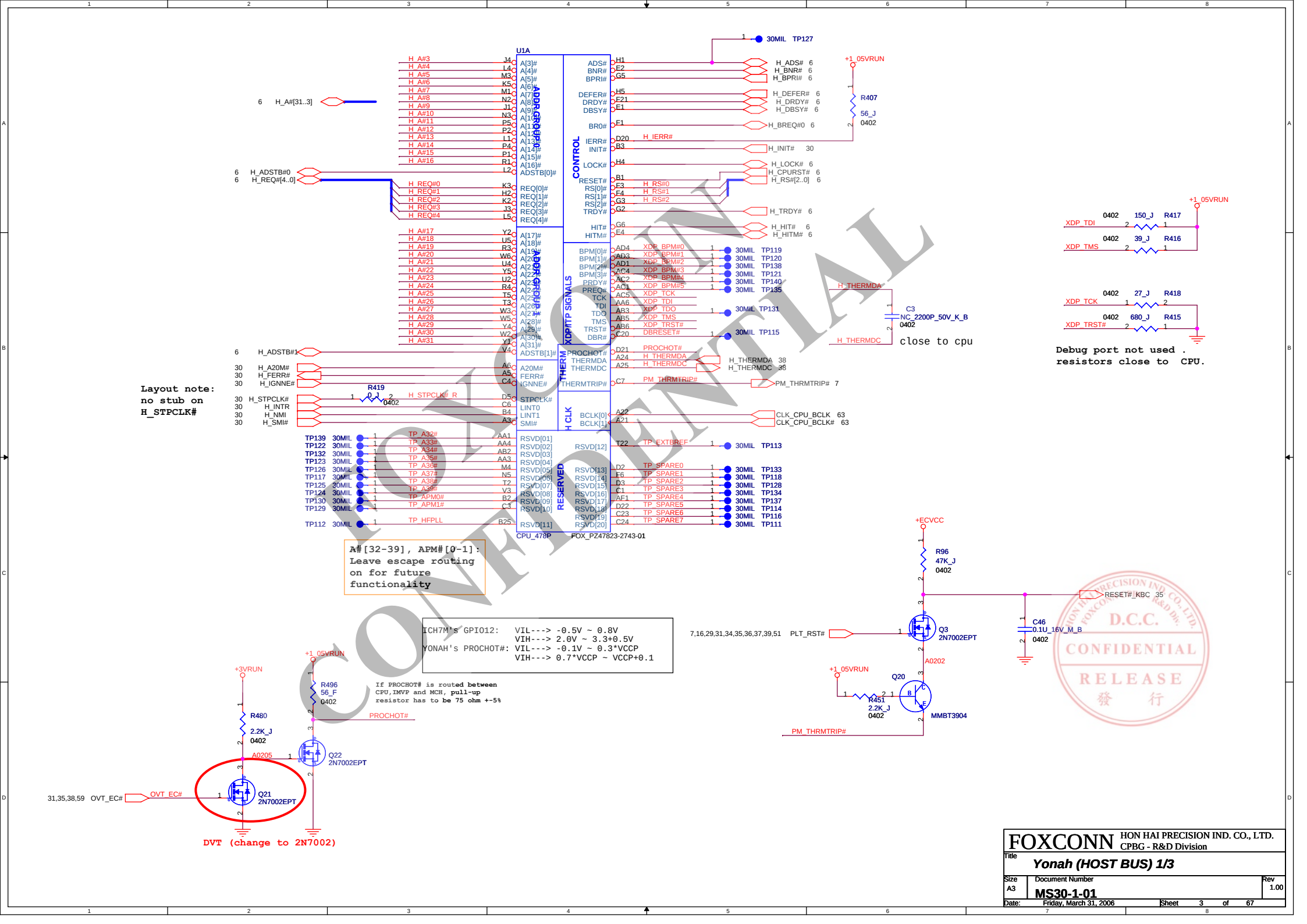
Title: Block Diagram (All)

Size: C | Document Number: MS30-1-01 | Rev: 1.00

Date: Friday, March 31, 2006 | Sheet 2 of 67


U1A
CPU_478P
FOX_PZ47823-2743-01
Layout note:
no stub on
H_STPCLK#
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality
ICH7M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1
If PROCHOT# is routed between CPU,IMVP and MCH, pull-up resistor has to be 75 ohm +-5%
close to cpu
Debug port not used .
resistors close to CPU.
DVT (change to 2N7002)
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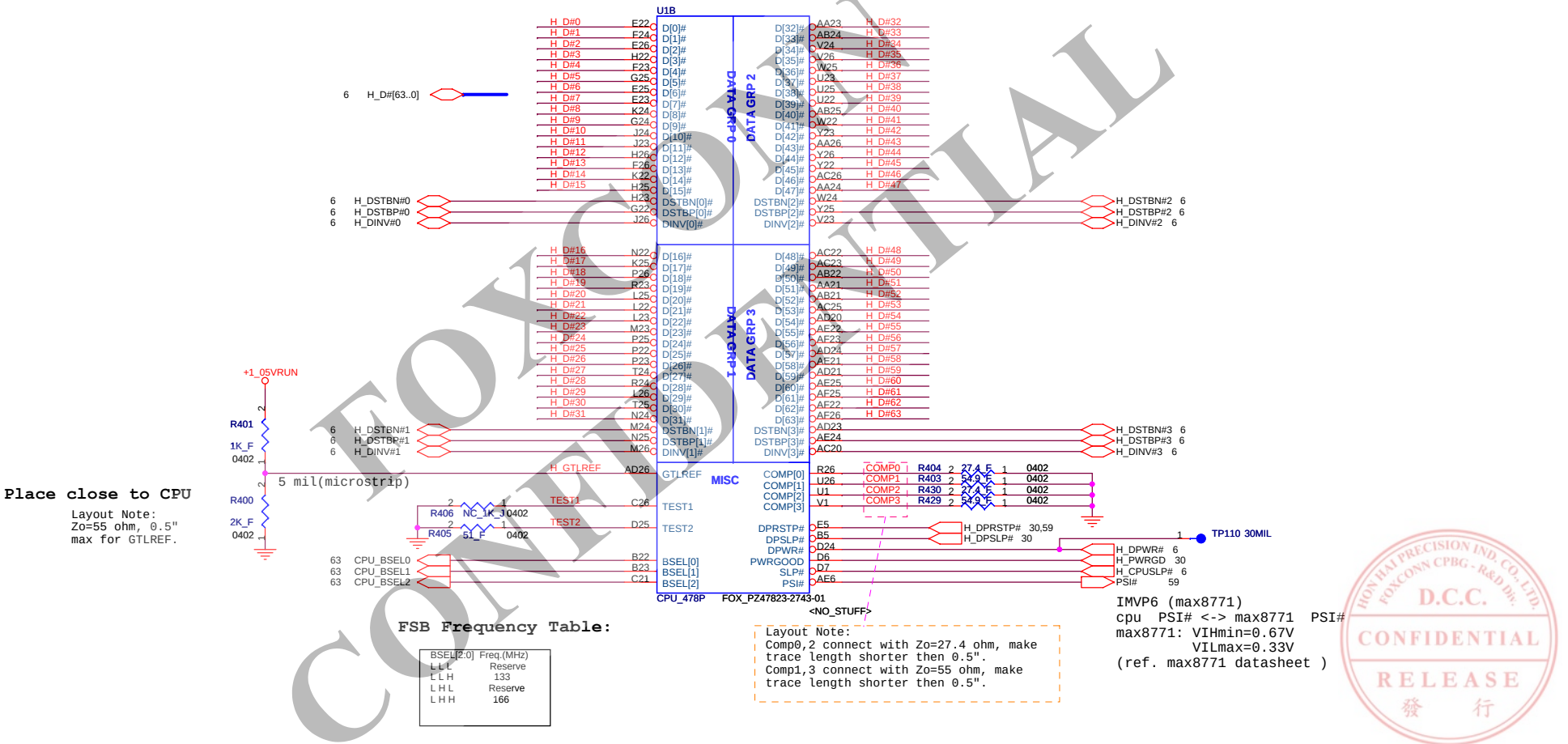
Yonah (HOST BUS) 1/3
MS30-1-01
Friday, March 31, 2006
Sheet 3 of 67




**Place close to CPU**

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

**FSB Frequency Table:**

| BSEL[2:0] | Freq.(MHz) |
|---|---|
| L L L | Reserve |
| L L H | 133 |
| L H L | Reserve |
| L H H | 166 |

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

IMVP6 (max8771)
cpu PSI# <-> max8771 PSI#
max8771: VIHmin=0.67V
VILmax=0.33V
(ref. max8771 datasheet )



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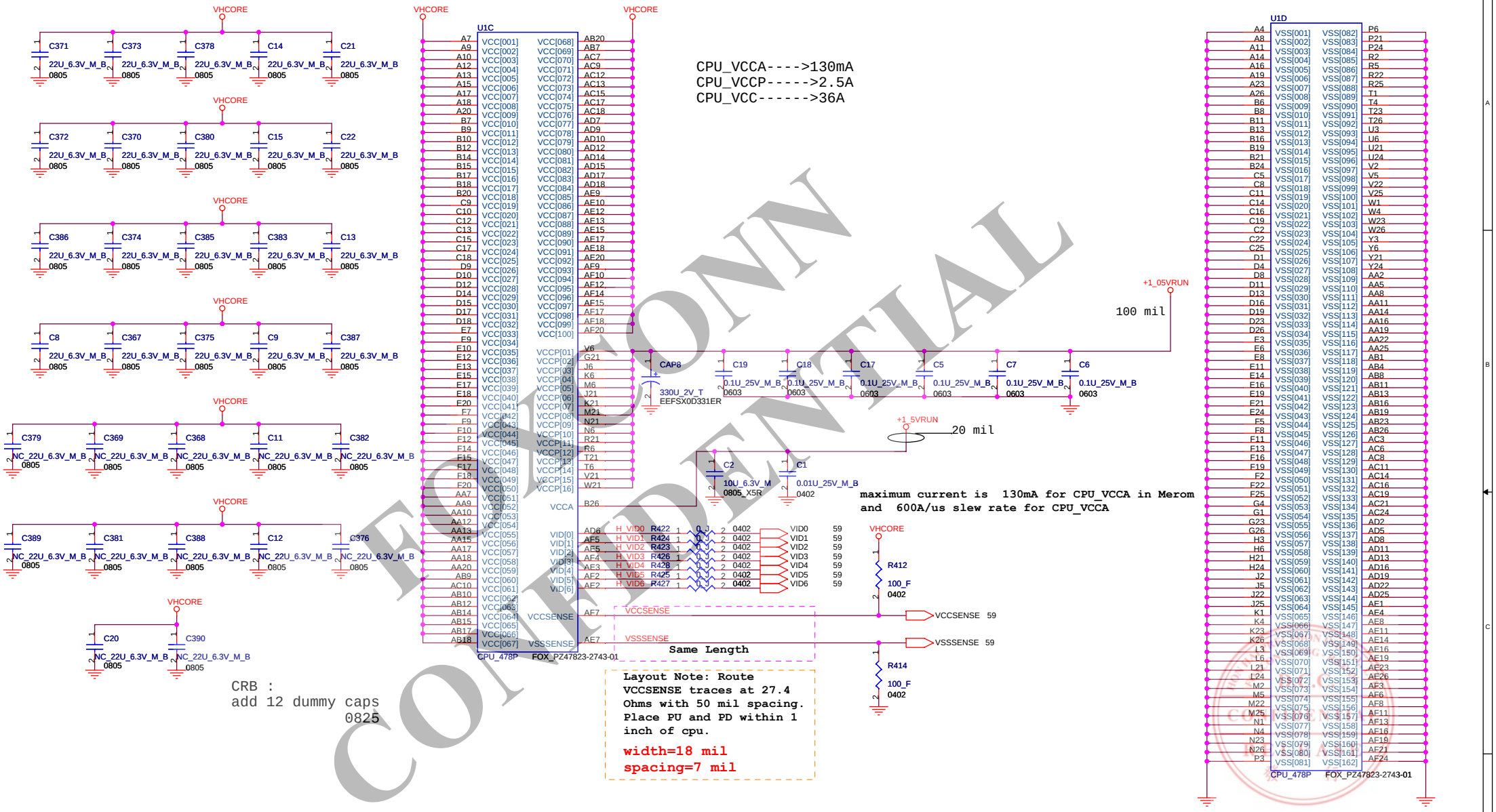
Title: *Yonah (HOST BUS) 2/3*

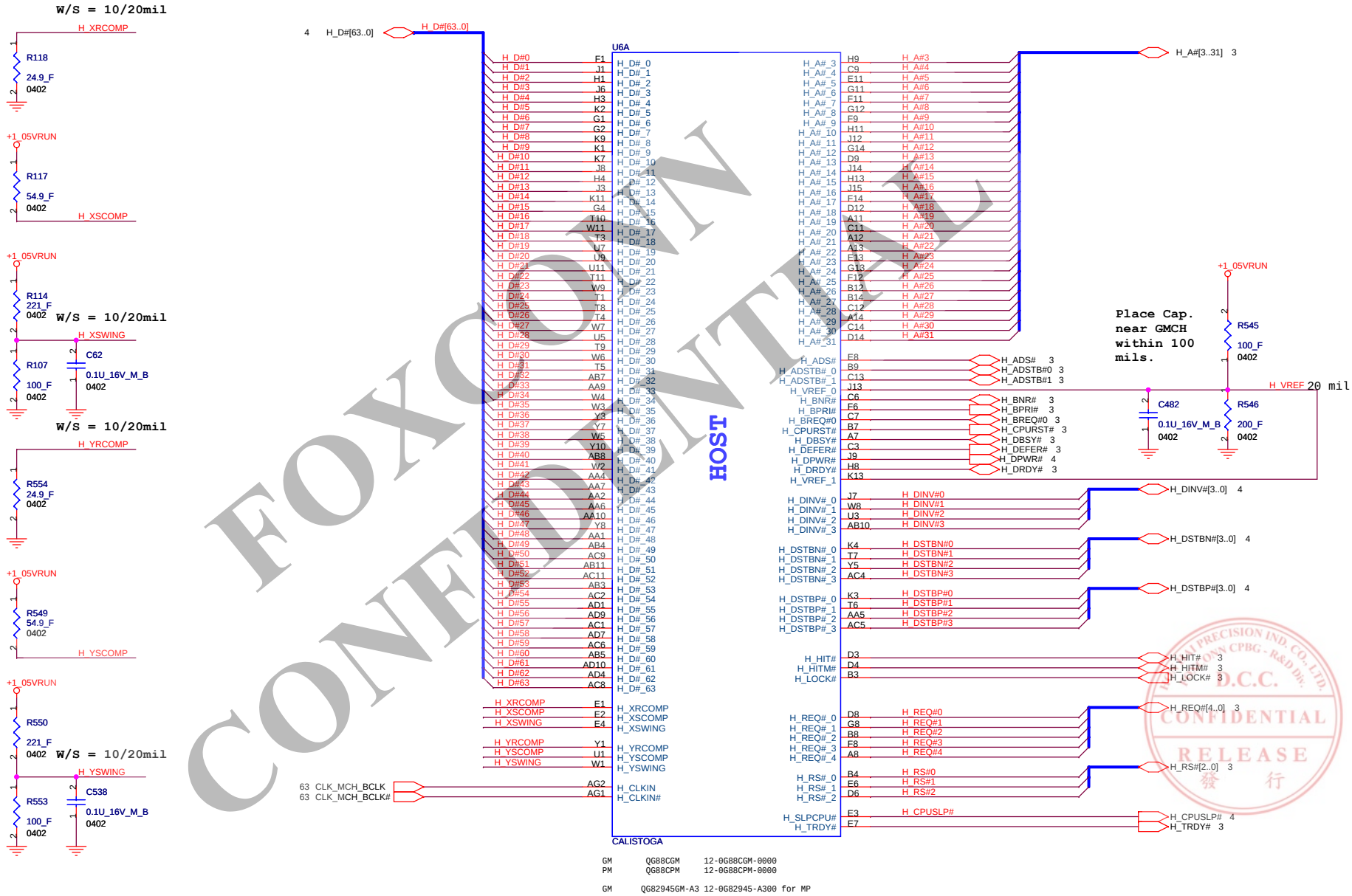
Size: A3 | Document Number: MS30-1-01 | Rev: 1.00

Date: Friday, March 31, 2006 | Sheet 4 of 67






| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division |
| Title | Yonah (POWER/GROUND) 3/3 |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 5 of 67 |






| | | |
|---|---|---|
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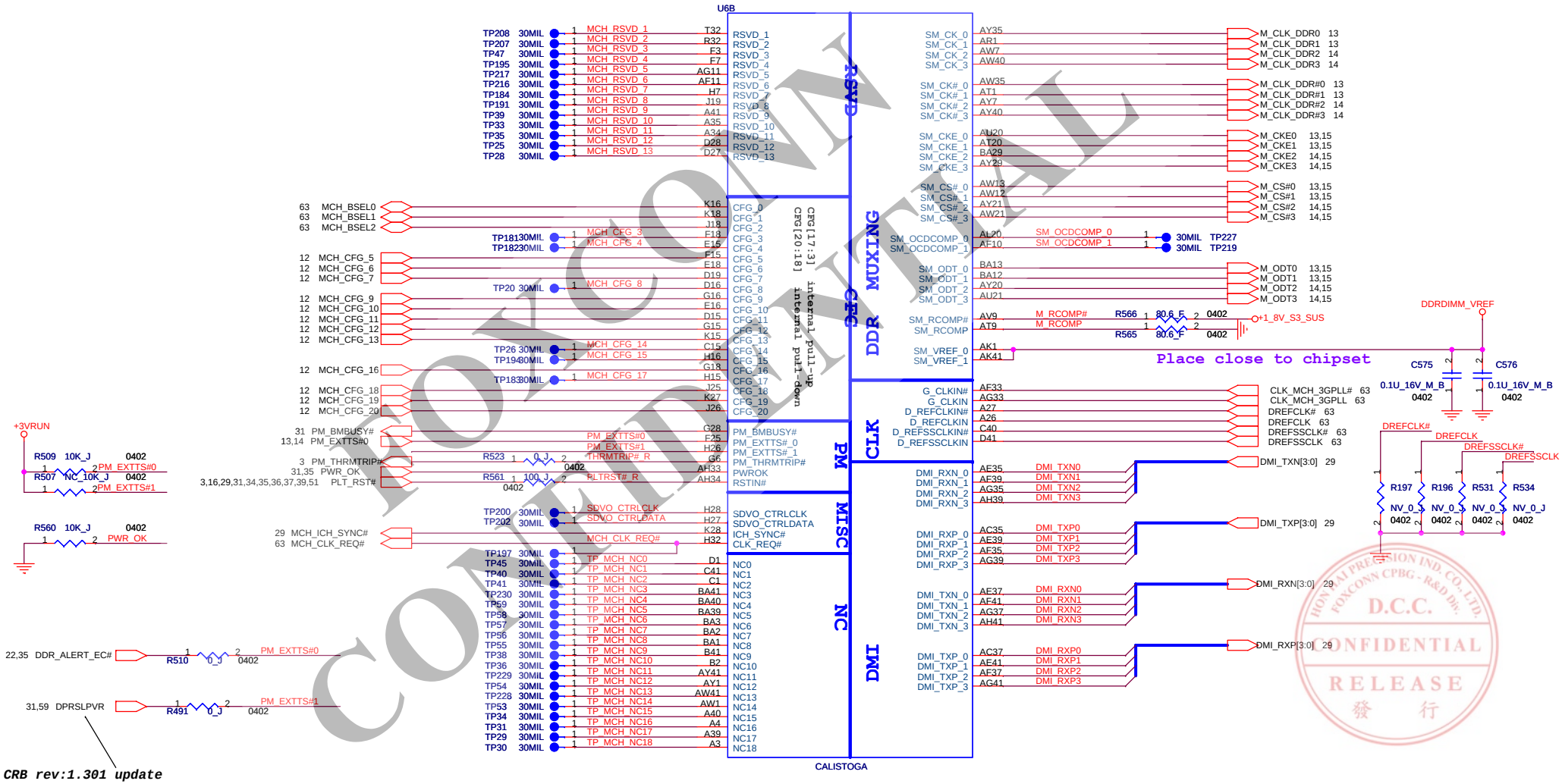
| Title | CALISTOHA (HOST) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 6 of 67 | |






| | | | |
|---|---|---|---|
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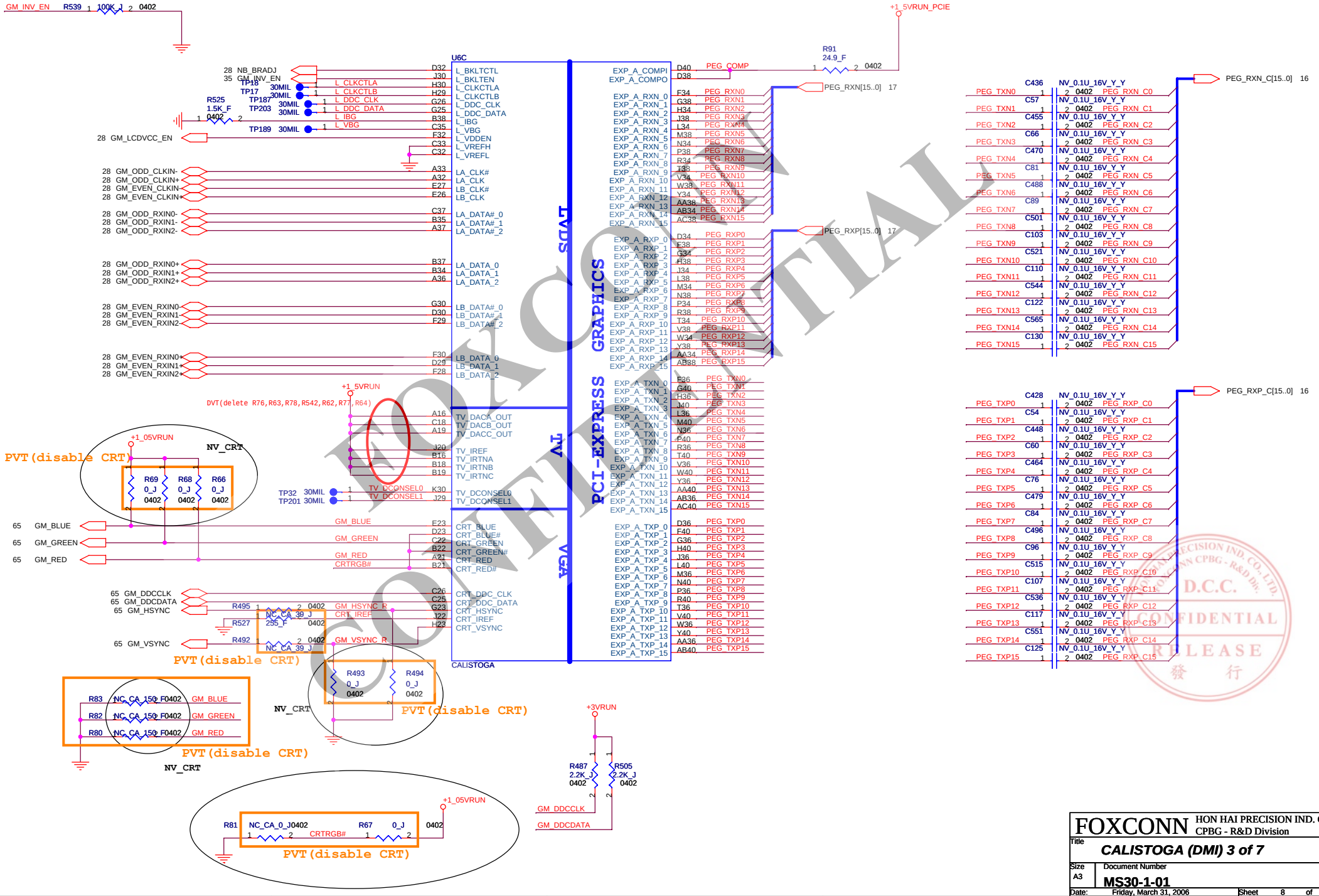
| Title | CALISTOGA (DMI) 2 of 7 | | |
| Size A3 | Document Number MS30-1-01 | | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 7 of 67 | | |


GM_INV_EN
R539 100K_J 0402
+1_5VRUN_PCIE
R91 24.9_F 0402
U6C
CALISTOGA
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CLKCTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATA_0
LA_DATA_1
LA_DATA_2
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LB_DATA_0
LB_DATA_1
LB_DATA_2
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
TV_DCONSEL0
TV_DCONSEL1
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
EXP_A_COMPI
EXP_A_COMPO
PEG_COMP
PEG_RXN[15..0] 17
PEG_RXP[15..0] 17
PEG_RXN_C[15..0] 16
PEG_RXP_C[15..0] 16
NB_BRADJ
GM_LCDVCC_EN
GM_ODD_CLKIN-
GM_ODD_CLKIN+
GM_EVEN_CLKIN-
GM_EVEN_CLKIN+
GM_ODD_RXIN0-
GM_ODD_RXIN1-
GM_ODD_RXIN2-
GM_ODD_RXIN0+
GM_ODD_RXIN1+
GM_ODD_RXIN2+
GM_EVEN_RXIN0
GM_EVEN_RXIN1
GM_EVEN_RXIN2
GM_EVEN_RXIN0+
GM_EVEN_RXIN1+
GM_EVEN_RXIN2+
+1_5VRUN
DVT(delete R76,R63,R78,R542,R62,R77,R64)
+1_05VRUN
NV_CRT
PVT(disable CRT)
R69 0_J 0402
R68 0_J 0402
R66 0_J 0402
TP32 30MIL
TP201 30MIL
GM_BLUE
GM_GREEN
GM_RED
CRTRGB#
GM_DDCCLK
GM_DDCDATA
GM_HSYNC
GM_VSYNC
R495 NC_CA_39_J 295_F 0402
R527
R492 NC_CA_39_J 0402
GM_HSYNC_R
GM_VSYNC_R
R493 0_J 0402
R494 0_J 0402
R83 NC_CA_150_F0402
R82 NC_CA_150_F0402
R80 NC_CA_150_F0402
R81 NC_CA_0_J0402
R67 0_J 0402
+3VRUN
R487 2.2K_J 0402
R505 2.2K_J 0402
C436 NV_0.1U_16V_Y_Y 0402
C57 NV_0.1U_16V_Y_Y 0402
C455 NV_0.1U_16V_Y_Y 0402
C66 NV_0.1U_16V_Y_Y 0402
C470 NV_0.1U_16V_Y_Y 0402
C81 NV_0.1U_16V_Y_Y 0402
C488 NV_0.1U_16V_Y_Y 0402
C89 NV_0.1U_16V_Y_Y 0402
C501 NV_0.1U_16V_Y_Y 0402
C103 NV_0.1U_16V_Y_Y 0402
C521 NV_0.1U_16V_Y_Y 0402
C110 NV_0.1U_16V_Y_Y 0402
C544 NV_0.1U_16V_Y_Y 0402
C122 NV_0.1U_16V_Y_Y 0402
C565 NV_0.1U_16V_Y_Y 0402
C130 NV_0.1U_16V_Y_Y 0402
C428 NV_0.1U_16V_Y_Y 0402
C54 NV_0.1U_16V_Y_Y 0402
C448 NV_0.1U_16V_Y_Y 0402
C60 NV_0.1U_16V_Y_Y 0402
C464 NV_0.1U_16V_Y_Y 0402
C76 NV_0.1U_16V_Y_Y 0402
C479 NV_0.1U_16V_Y_Y 0402
C84 NV_0.1U_16V_Y_Y 0402
C496 NV_0.1U_16V_Y_Y 0402
C96 NV_0.1U_16V_Y_Y 0402
C515 NV_0.1U_16V_Y_Y 0402
C107 NV_0.1U_16V_Y_Y 0402
C536 NV_0.1U_16V_Y_Y 0402
C117 NV_0.1U_16V_Y_Y 0402
C551 NV_0.1U_16V_Y_Y 0402
C125 NV_0.1U_16V_Y_Y 0402
PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
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PEG_TXN9
PEG_TXN10
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PEG_TXP3
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PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15
FOXCONN
HON HAI PRECISION IND. CO., LTD.
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CALISTOGA (DMI) 3 of 7
MS30-1-01
Rev 1.00
Friday, March 31, 2006
Sheet 8 of 67
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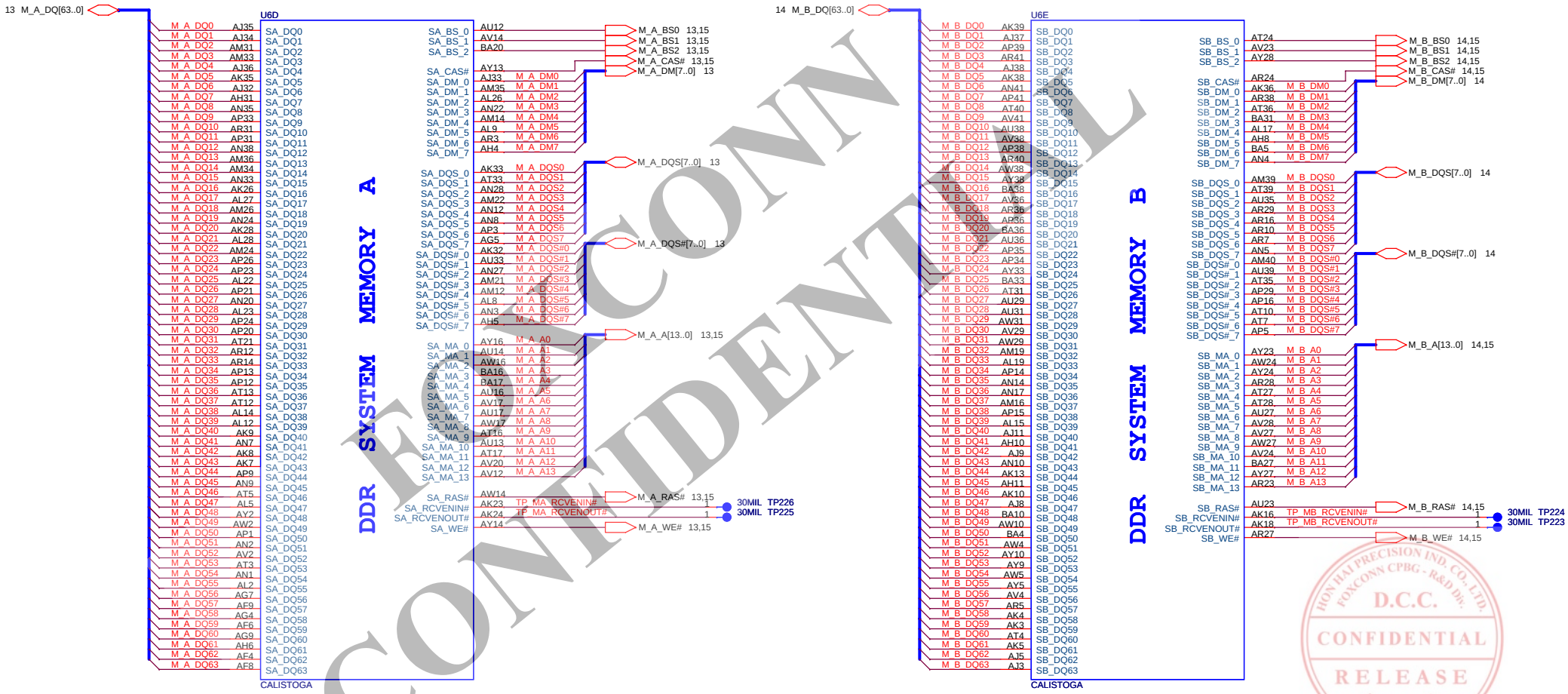






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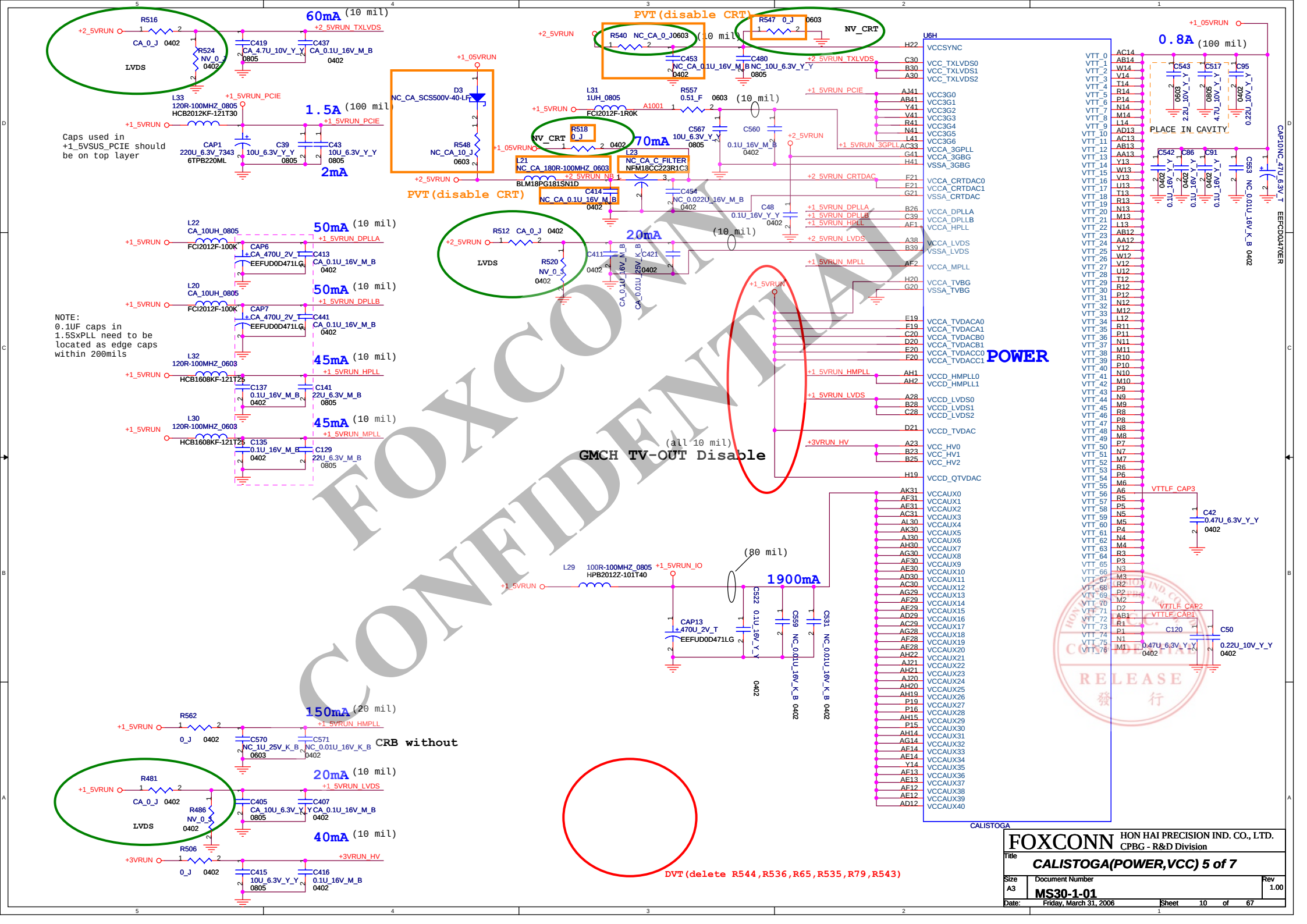
Title: CALISTOGA (DDRII) 4 of 7

Size: A3 | Document Number: MS30-1-01 | Rev: 1.00

Date: Friday, March 31, 2006 | Sheet 9 of 67


60mA (10 mil)
1.5A (100 mil)
2mA
70mA
PVT(disable CRT)
50mA (10 mil)
50mA (10 mil)
45mA (10 mil)
45mA (10 mil)
20mA
(10 mil)
0.8A (100 mil)
PLACE IN CAVITY
Caps used in +1_5VSUS_PCIE should be on top layer
NOTE: 0.1UF caps in 1.5SxPLL need to be located as edge caps within 200mils
(all 10 mil)
GMCH TV-OUT Disable
POWER
(80 mil)
1900mA
150mA (20 mil)
CRB without
20mA (10 mil)
40mA (10 mil)
DVT(delete R544,R536,R65,R535,R79,R543)
CALISTOGA
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
CALISTOGA(POWER,VCC) 5 of 7
MS30-1-01
Friday, March 31, 2006
Sheet 10 of 67
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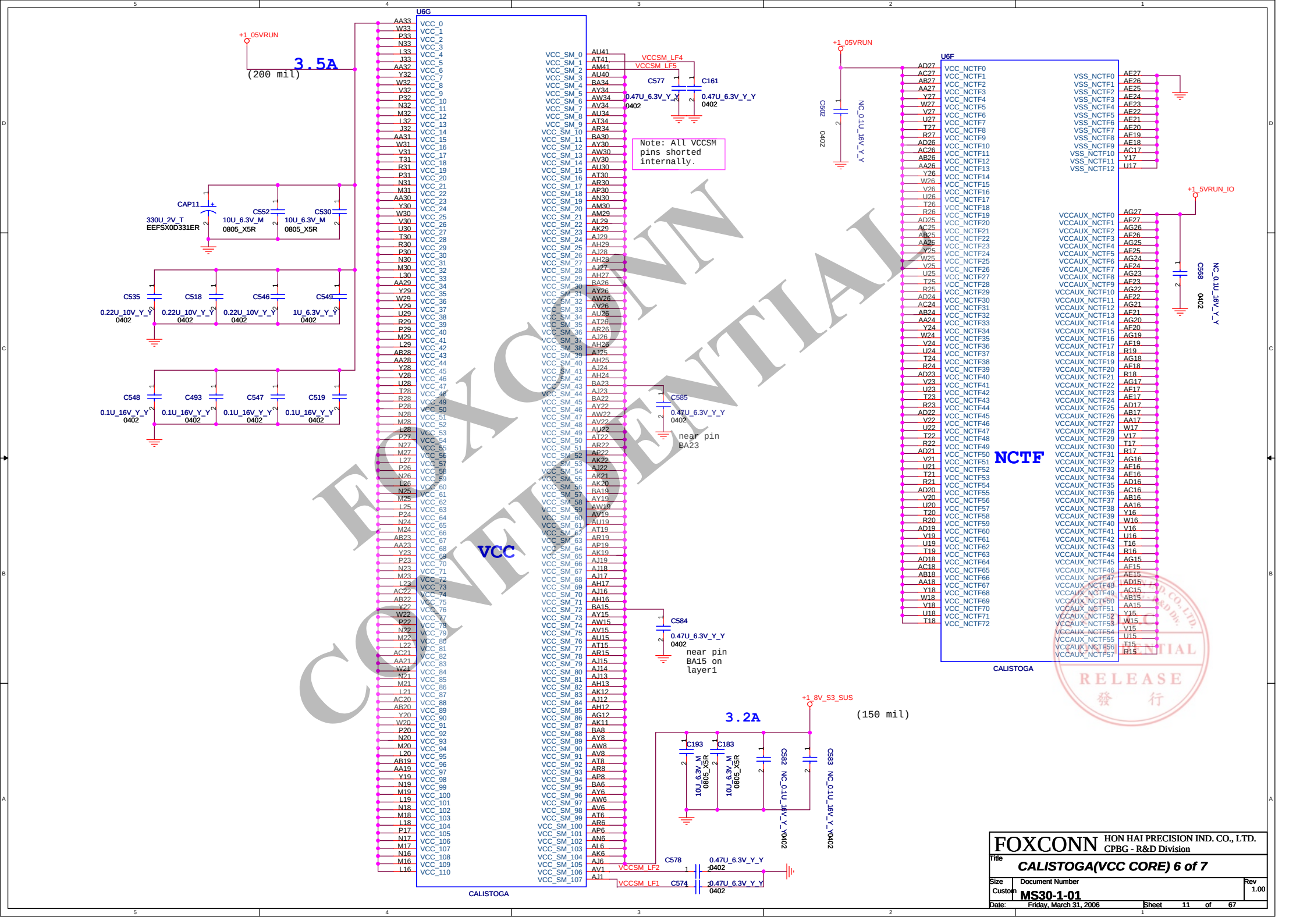




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|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | CALISTOGA(VCC CORE) 6 of 7 | |
| Size: Custom | Document Number: MS30-1-01 | Rev: 1.00 |
| Date: Friday, March 31, 2006 | Sheet 11 of 67 | |

7 MCH_CFG_5 — 30MIL TP193

| MCH_CFG_5 | Low = DMIx2<br>High = DMIx4 |
|---|---|

7 MCH_CFG_6 — 30MIL TP180

| MCH_CFG_6 | Low = Moby Dick<br>High = Calistoga |
|---|---|

DDR2 select (default high)

7 MCH_CFG_7 — 30MIL TP15

| MCH_CFG_7<br>(CPU Strap) | Low = RSVD<br>High = Mobile Yonah processor |
|---|---|

7 MCH_CFG_9 — 30MIL TP250

DVT (delete R514,add TP)

| MCH_CFG_9<br>(PCIE Graphics Lane) | Low = Reverse Lane<br>High = Normal operation |
|---|---|

**For layout convenience**

7 MCH_CFG_10 — 30MIL TP192

| MCH_CFG_10<br>(HOST PLL VCC SELECT) | Low = RESERVED<br>High = MOBILITY |
|---|---|

7 MCH_CFG_11

| MCH_CFG_11<br>(PSB 4x CLK ENABLE) | Low = Reserved<br>High= Calistoga |
|---|---|

R85 NC_2.2K_J 0402

7 MCH_CFG_12 — 30MIL TP185
7 MCH_CFG_13 — 30MIL TP205

| MCH_CFG_[13:12]<br>(XOR/ALLZ) | 00=Partial Clock Gating Disable<br>01=XOR Mode Enable<br>10=All-Z Mode Enable<br>11=Normal Operation(Default) |
|---|---|

7 MCH_CFG_16 — 30MIL TP178

| MCH_CFG_16<br>(FSB Dynamic ODT) | Low = Dynamic ODT Disabled<br>High = Dynamic ODT Enable |
|---|---|

| MCH_CFG_18<br>(VCC_CORE Select) | Low = 1.05V(default)<br>High = 1.5V |
|---|---|

7 MCH_CFG_18 — 30MIL TP248

DVT (delete R508,add TP)

| MCH_CFG_19<br>(DMI LANE REVERSAL) | Low = Normal(default)<br>High = LANES REVERSED |
|---|---|

7 MCH_CFG_19 — 30MIL TP249

DVT (delete R541,add TP)

| MCH_CFG_20<br>(PCIe Backward Interpoerability mode) | Low = Only SDVO or PCIE x1 is operational (defaults))<br>High = SDVO and PCIE x1 are operating simultaneously via the PEG port |
|---|---|

7 MCH_CFG_20 — 30MIL TP204

**Layout Noe:**
**Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub**

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U6I

VSS

CALISTOGA

U6J

VSS

CALISTOGA



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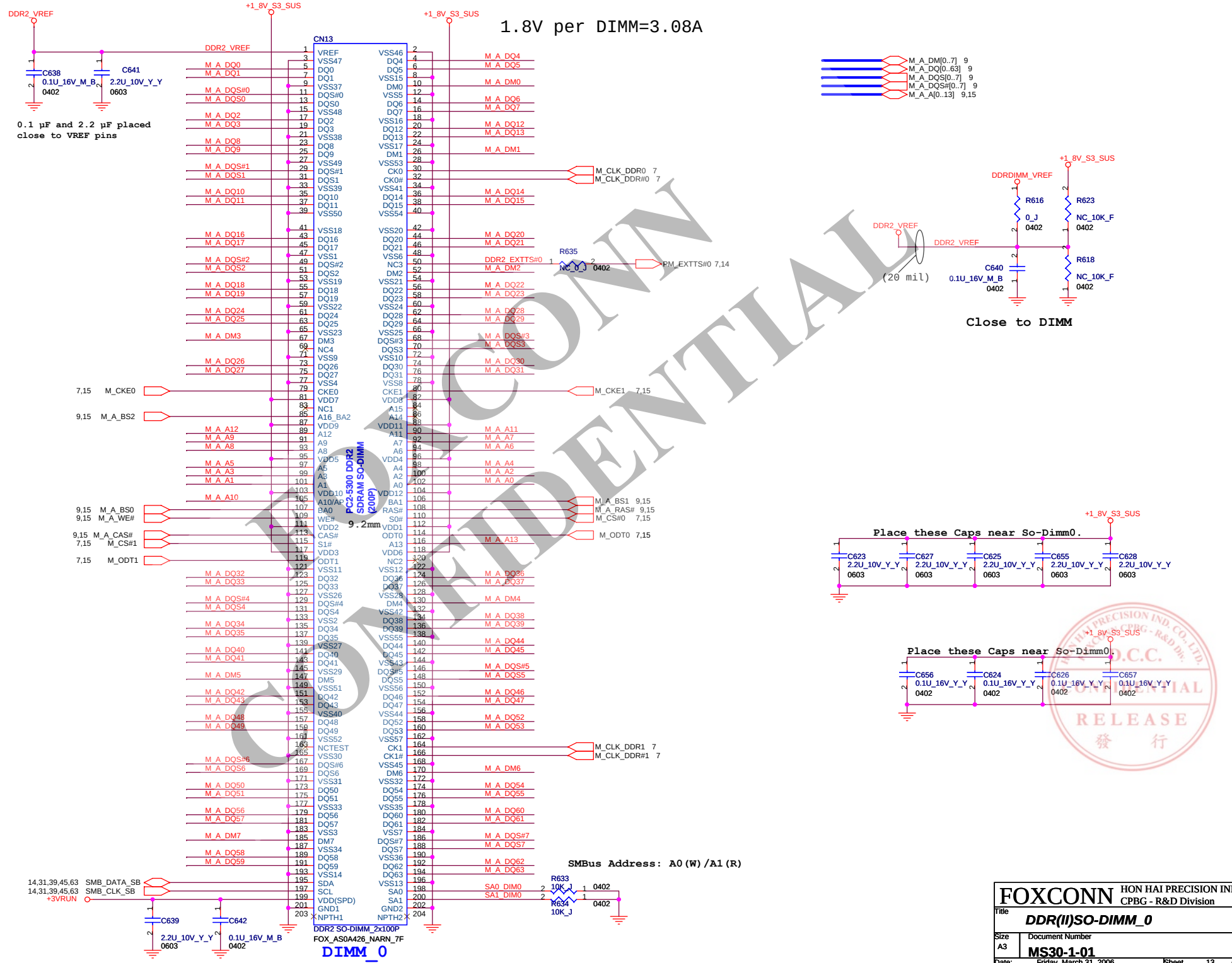
Title: CALISTOGA(VSS) 7 of 7

| Size | Document Number | Rev |
|---|---|---|
| A3 | MS30-1-01 | 1.00 |

Date: Friday, March 31, 2006 Sheet 12 of 67


1.8V per DIMM=3.08A
DDR2_VREF
+1_8V_S3_SUS
C638 0.1U_16V_M_B 0402
C641 2.2U_10V_Y_Y 0603
0.1 µF and 2.2 µF placed close to VREF pins
CN13
DDR2 SO-DIMM_2x100P
FOX_AS0A426_NARN_7F
DIMM_0
PC2-5300 DDR2 SDRAM SO-DIMM (200P)
9.2mm
M_A_DM[0..7] 9
M_A_DQ[0..63] 9
M_A_DQS[0..7] 9
M_A_DQS#[0..7] 9
M_A_A[0..13] 9,15
M_CLK_DDR0 7
M_CLK_DDR#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
M_CKE0 7,15
M_CKE1 7,15
M_A_BS2 9,15
M_A_BS1 9,15
M_A_BS0 9,15
M_A_RAS# 9,15
M_A_WE# 9,15
M_A_CAS# 9,15
M_CS#0 7,15
M_CS#1 7,15
M_ODT0 7,15
M_ODT1 7,15
DDR2_EXTTS#0
PM_EXTTS#0 7,14
R635 NC_0_J 0402
SMB_DATA_SB 14,31,39,45,63
SMB_CLK_SB 14,31,39,45,63
+3VRUN
C639 2.2U_10V_Y_Y 0603
C642 0.1U_16V_M_B 0402
SMBus Address: A0(W)/A1(R)
R633 10K_J 0402
R634 10K_J 0402
DDRDIMM_VREF
R616 0_J 0402
R623 NC_10K_F 0402
R618 NC_10K_F 0402
C640 0.1U_16V_M_B 0402
(20 mil)
Close to DIMM
Place these Caps near So-Dimm0.
C623 2.2U_10V_Y_Y 0603
C627 2.2U_10V_Y_Y 0603
C625 2.2U_10V_Y_Y 0603
C655 2.2U_10V_Y_Y 0603
C628 2.2U_10V_Y_Y 0603
Place these Caps near So-Dimm0.
C656 0.1U_16V_Y_Y 0402
C624 0.1U_16V_Y_Y 0402
C626 0.1U_16V_Y_Y 0402
C657 0.1U_16V_Y_Y 0402
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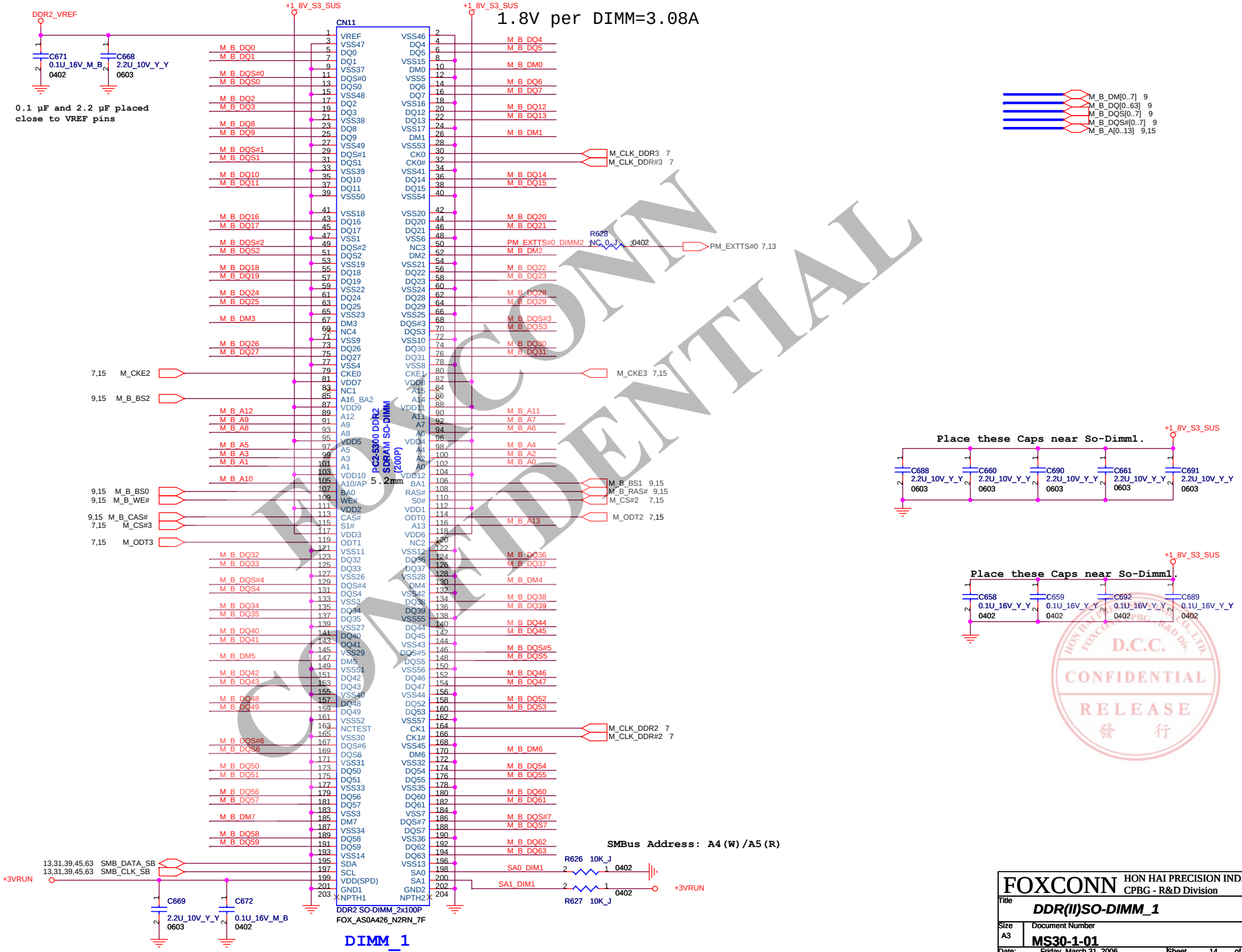
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title: DDR(II)SO-DIMM_0
Size: A3
Document Number: MS30-1-01
Rev: 1.00
Date: Friday, March 31, 2006
Sheet 13 of 67






| | |
|---|---|
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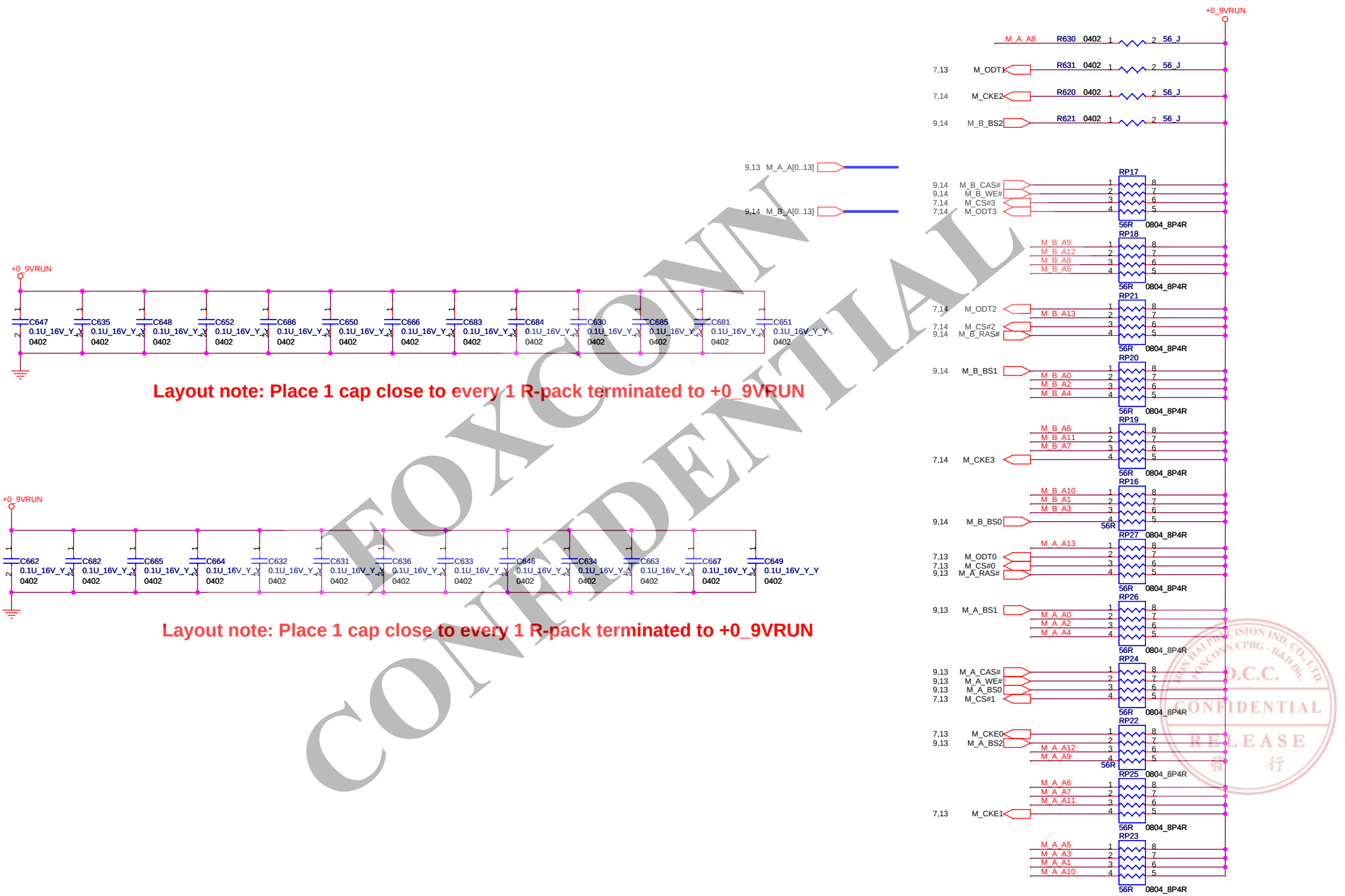
| Title | DDR(II)SO-DIMM_1 |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 14 of 67 |





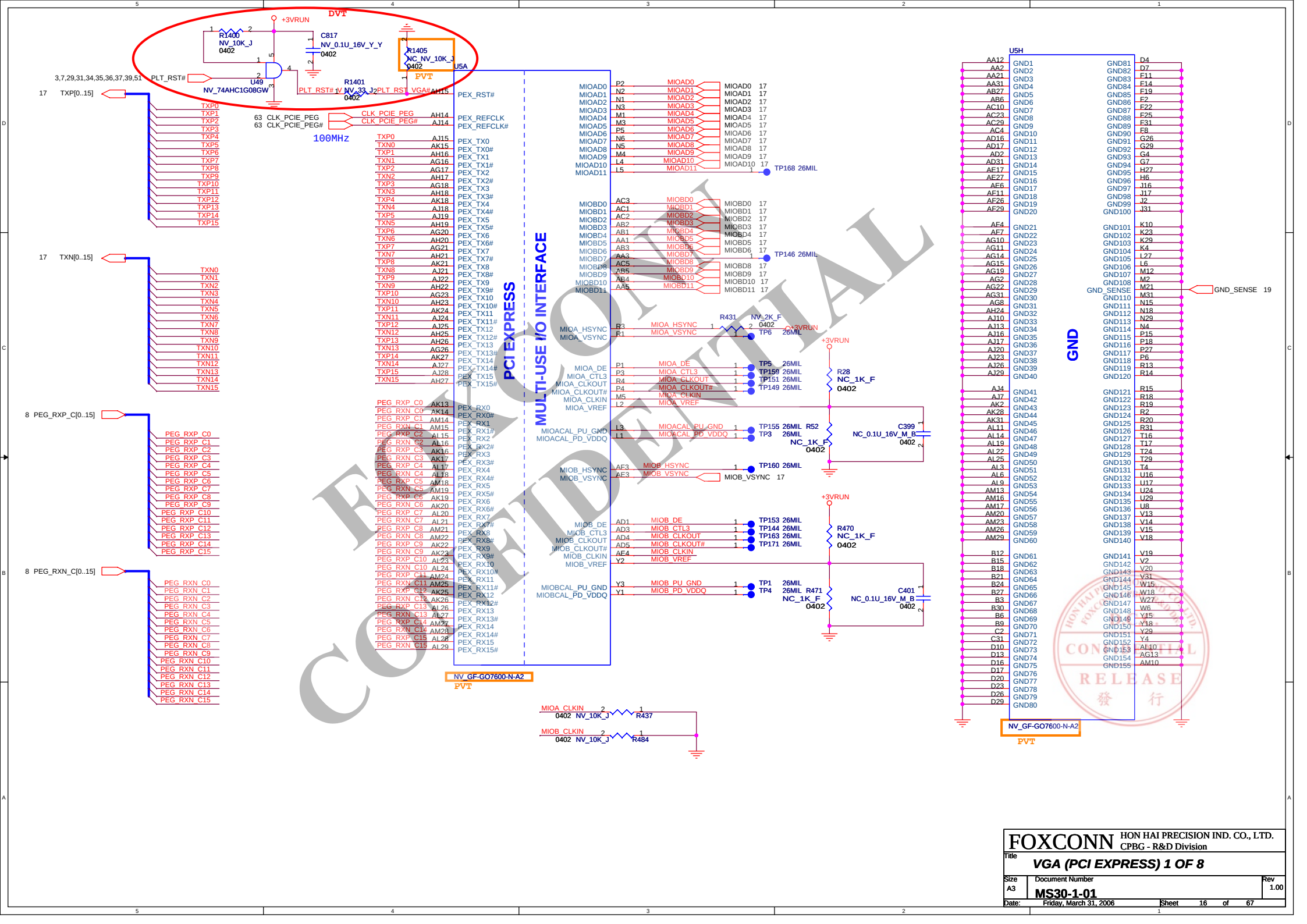



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: DDR(II)Termination

| Size | Document Number | Rev |
|---|---|---|
| A3 | MS30-1-01 | 1.00 |

Date: Friday, March 31, 2006 Sheet 15 of 67






| | |
|---|---|
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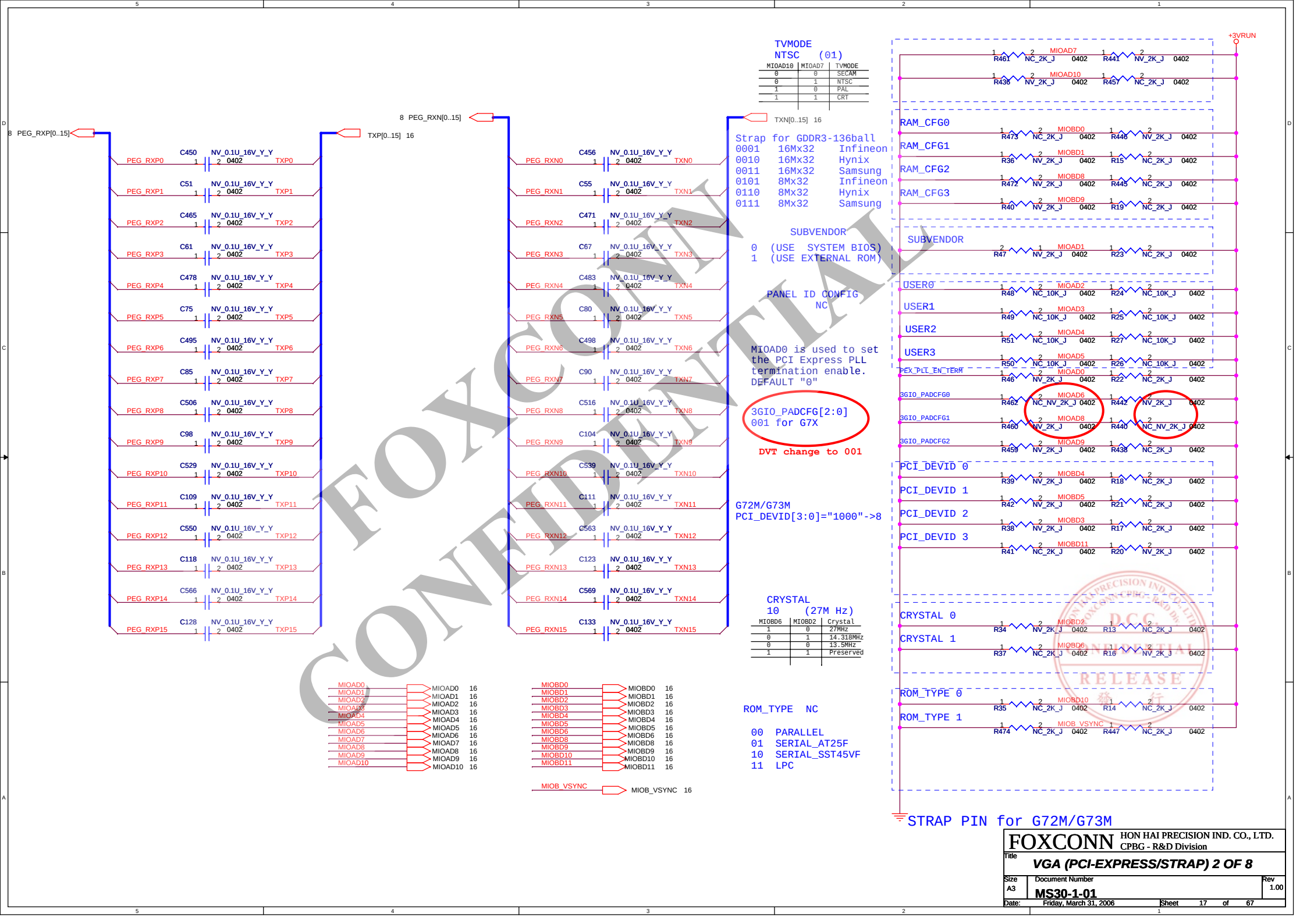
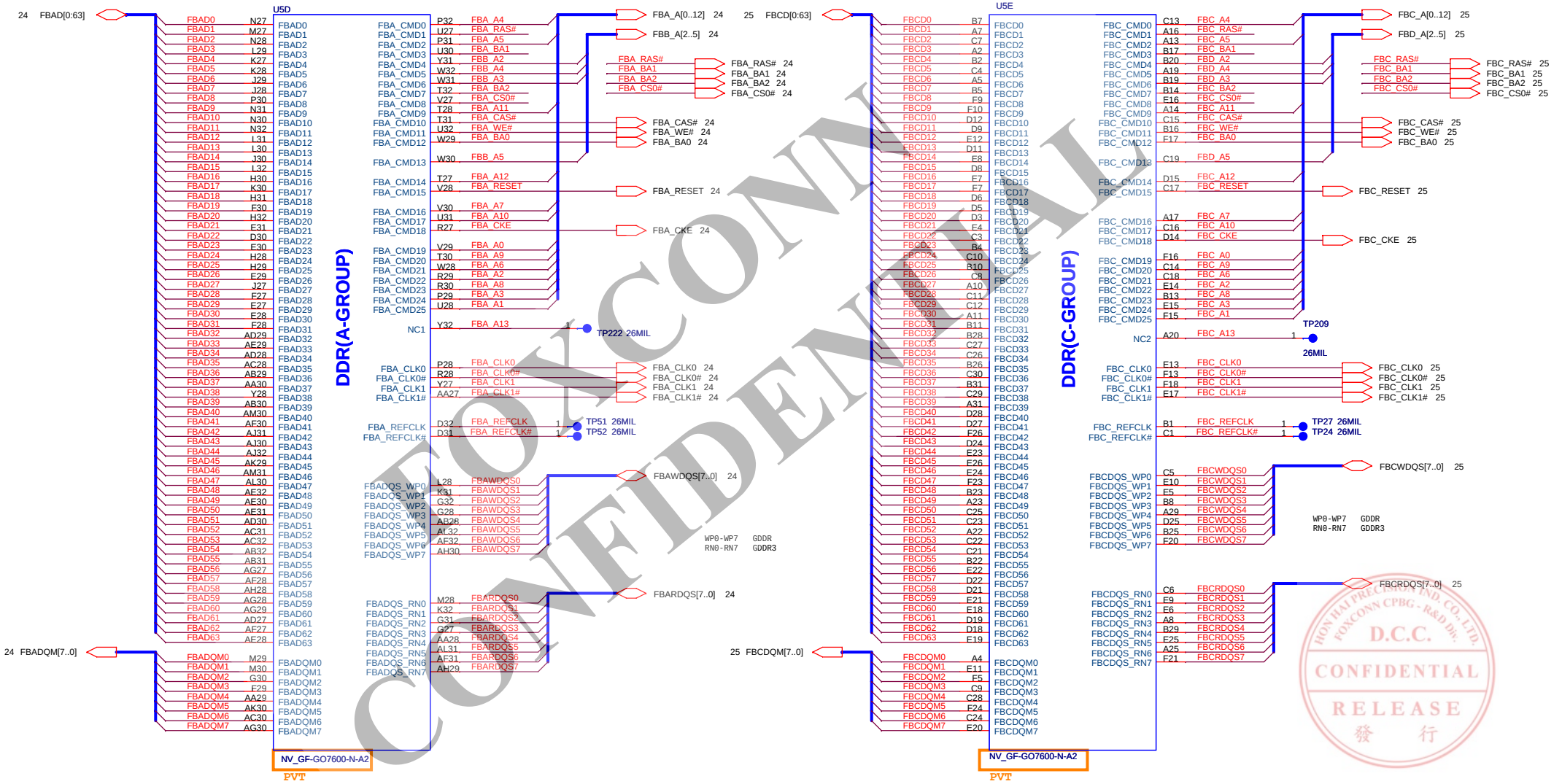
| Title | VGA (PCI EXPRESS) 1 OF 8 |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 16 of 67 |










| | |
|---|---|
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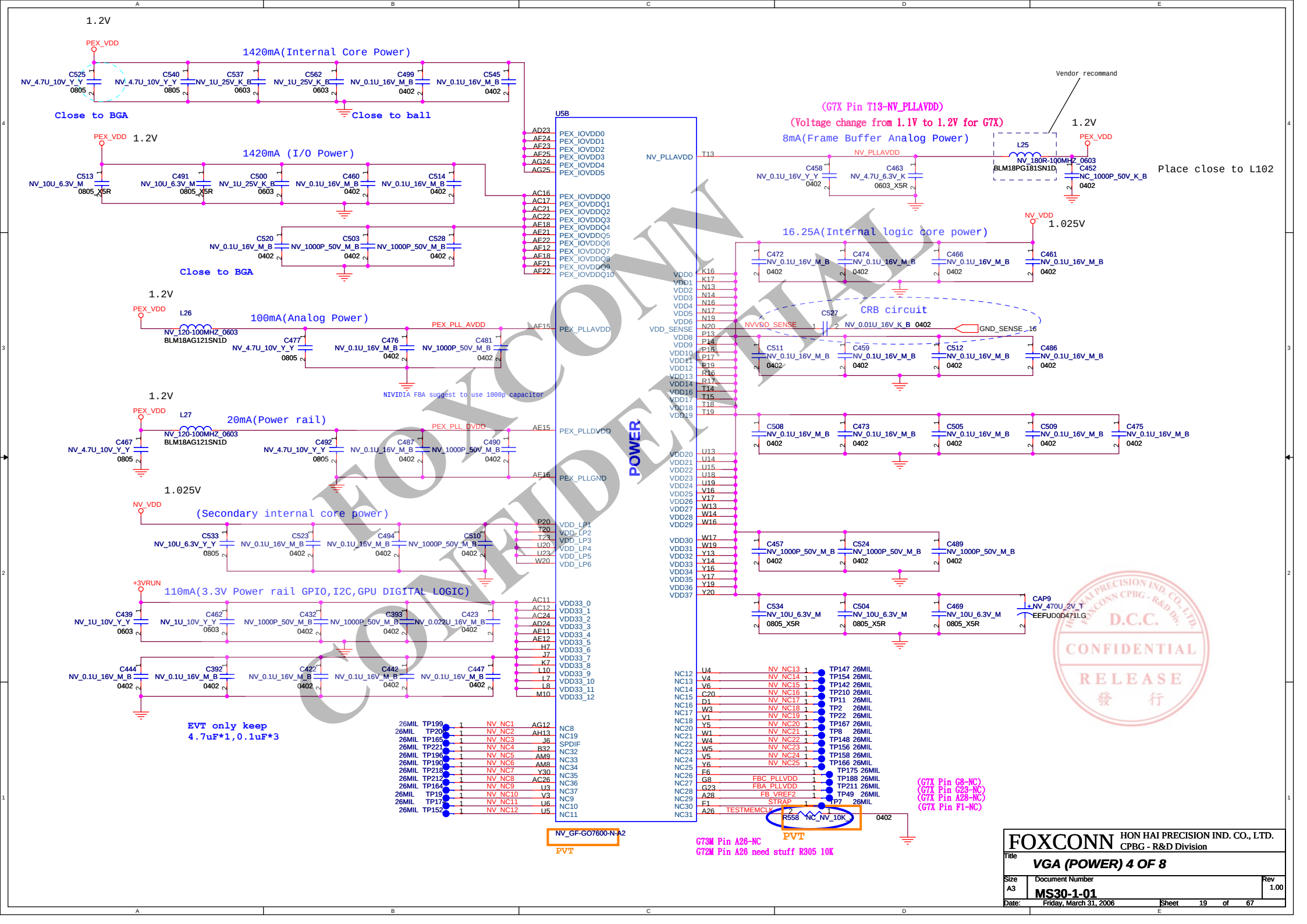
| Title | VGA (GDDR) 3 OF 8 |
| Size A3 | Document Number MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 18 of 67 |


1.2V
PEX_VDD
1420mA(Internal Core Power)
C525 NV_4.7U_10V_Y_Y 0805
C540 NV_4.7U_10V_Y_Y 0805
C537 NV_1U_25V_K_B 0603
C562 NV_1U_25V_K_B 0603
C499 NV_0.1U_16V_M_B 0402
C545 NV_0.1U_16V_M_B 0402
Close to BGA
Close to ball
1420mA (I/O Power)
C513 NV_10U_6.3V_M 0805_X5R
C491 NV_10U_6.3V_M 0805_X5R
C500 NV_1U_25V_K_B 0603
C460 NV_0.1U_16V_M_B 0402
C514 NV_0.1U_16V_M_B 0402
C520 NV_0.1U_16V_M_B 0402
C503 NV_1000P_50V_M_B 0402
C528 NV_1000P_50V_M_B 0402
Close to BGA
U5B
POWER
PEX_IOVDD0
PEX_IOVDD1
PEX_IOVDD2
PEX_IOVDD3
PEX_IOVDD4
PEX_IOVDD5
PEX_IOVDDQ0
PEX_IOVDDQ1
PEX_IOVDDQ2
PEX_IOVDDQ3
PEX_IOVDDQ4
PEX_IOVDDQ5
PEX_IOVDDQ6
PEX_IOVDDQ7
PEX_IOVDDQ8
PEX_IOVDDQ9
PEX_IOVDDQ10
NV_PLLAVDD
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
VDD_LP1
VDD_LP2
VDD_LP3
VDD_LP4
VDD_LP5
VDD_LP6
VDD33_0
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
VDD33_7
VDD33_8
VDD33_9
VDD33_10
VDD33_11
VDD33_12
NC8
NC19
SPDIF
NC32
NC33
NC34
NC35
NC36
NC37
NC9
NC10
NC11
VDD0
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD_SENSE
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD16
VDD17
VDD18
VDD19
VDD20
VDD21
VDD22
VDD23
VDD24
VDD25
VDD26
VDD27
VDD28
VDD29
VDD30
VDD31
VDD32
VDD33
VDD34
VDD35
VDD36
VDD37
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC20
NC21
NC22
NC23
NC24
NC25
NC26
NC27
NC28
NC29
NC30
NC31
1.2V
PEX_VDD
L26
NV_120-100MHZ_0603
BLM18AG121SN1D
100mA(Analog Power)
PEX_PLL_AVDD
C477 NV_4.7U_10V_Y_Y 0805
C476 NV_0.1U_16V_M_B 0402
C481 NV_1000P_50V_M_B 0402
NIVIDIA FBA suggest to use 1000p capacitor
1.2V
PEX_VDD
L27
NV_120-100MHZ_0603
BLM18AG121SN1D
20mA(Power rail)
PEX_PLL_DVDD
C467 NV_4.7U_10V_Y_Y 0805
C492 NV_4.7U_10V_Y_Y 0805
C487 NV_0.1U_16V_M_B 0402
C490 NV_1000P_50V_M_B 0402
1.025V
NV_VDD
(Secondary internal core power)
C533 NV_10U_6.3V_Y_Y 0805
C523 NV_0.1U_16V_M_B 0402
C494 NV_0.1U_16V_M_B 0402
C510 NV_1000P_50V_M_B 0402
+3VRUN
110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)
C439 NV_1U_10V_Y_Y 0603
C462 NV_1U_10V_Y_Y 0603
C432 NV_1000P_50V_M_B 0402
C393 NV_1000P_50V_M_B 0402
C423 NV_0.022U_16V_M_B 0402
C444 NV_0.1U_16V_M_B 0402
C392 NV_0.1U_16V_M_B 0402
C422 NV_0.1U_16V_M_B 0402
C442 NV_0.1U_16V_M_B 0402
C447 NV_0.1U_16V_M_B 0402
EVT only keep
4.7uF*1,0.1uF*3
26MIL TP199 NV_NC1 AG12
26MIL TP200 NV_NC2 AH13
26MIL TP165 NV_NC3 J6
26MIL TP221 NV_NC4 B32
26MIL TP196 NV_NC5 AM9
26MIL TP190 NV_NC6 AM8
26MIL TP218 NV_NC7 Y30
26MIL TP212 NV_NC8 AC26
26MIL TP164 NV_NC9 U3
26MIL TP19 NV_NC10 V3
26MIL TP17 NV_NC11 U6
26MIL TP152 NV_NC12 U5
NV_GF-GO7600-N-A2
PVT
(G7X Pin T13-NV_PLLAVDD)
(Voltage change from 1.1V to 1.2V for G7X)
8mA(Frame Buffer Analog Power)
Vendor recommand
1.2V
PEX_VDD
L25
NV_180R-100MHZ_0603
BLM18PG181SN1D
C458 NV_0.1U_16V_Y_Y 0402
C463 NV_4.7U_6.3V_K 0603_X5R
C452 NC_1000P_50V_K_B 0402
Place close to L102
NV_VDD
1.025V
16.25A(Internal logic core power)
C472 NV_0.1U_16V_M_B 0402
C474 NV_0.1U_16V_M_B 0402
C466 NV_0.1U_16V_M_B 0402
C461 NV_0.1U_16V_M_B 0402
CRB circuit
C527
NVVSD_SENSE
NV_0.01U_16V_K_B 0402
GND_SENSE_16
C511 NV_0.1U_16V_M_B 0402
C459 NV_0.1U_16V_M_B 0402
C512 NV_0.1U_16V_M_B 0402
C486 NV_0.1U_16V_M_B 0402
C508 NV_0.1U_16V_M_B 0402
C473 NV_0.1U_16V_M_B 0402
C505 NV_0.1U_16V_M_B 0402
C509 NV_0.1U_16V_M_B 0402
C475 NV_0.1U_16V_M_B 0402
C457 NV_1000P_50V_M_B 0402
C524 NV_1000P_50V_M_B 0402
C489 NV_1000P_50V_M_B 0402
C534 NV_10U_6.3V_M 0805_X5R
C504 NV_10U_6.3V_M 0805_X5R
C469 NV_10U_6.3V_M 0805_X5R
CAP9 NV_470U_2V_T EEFUD0D471LG
NV_NC13 TP147 26MIL
NV_NC14 TP154 26MIL
NV_NC15 TP142 26MIL
NV_NC16 TP210 26MIL
NV_NC17 TP11 26MIL
NV_NC18 TP2 26MIL
NV_NC19 TP22 26MIL
NV_NC20 TP167 26MIL
NV_NC21 TP8 26MIL
NV_NC22 TP148 26MIL
NV_NC23 TP156 26MIL
NV_NC24 TP158 26MIL
NV_NC25 TP166 26MIL
TP175 26MIL
FBC_PLLVDD TP188 26MIL
FBA_PLLVDD TP211 26MIL
FB_VREF2 TP49 26MIL
STRAP TP7 26MIL
TESTMEMCLK
R558 NC_NV_10K_J 0402
PVT
(G7X Pin G8-NC)
(G7X Pin G23-NC)
(G7X Pin A28-NC)
(G7X Pin F1-NC)
G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K
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Title
VGA (POWER) 4 OF 8
Size A3
Document Number MS30-1-01
Rev 1.00
Date: Friday, March 31, 2006
Sheet 19 of 67
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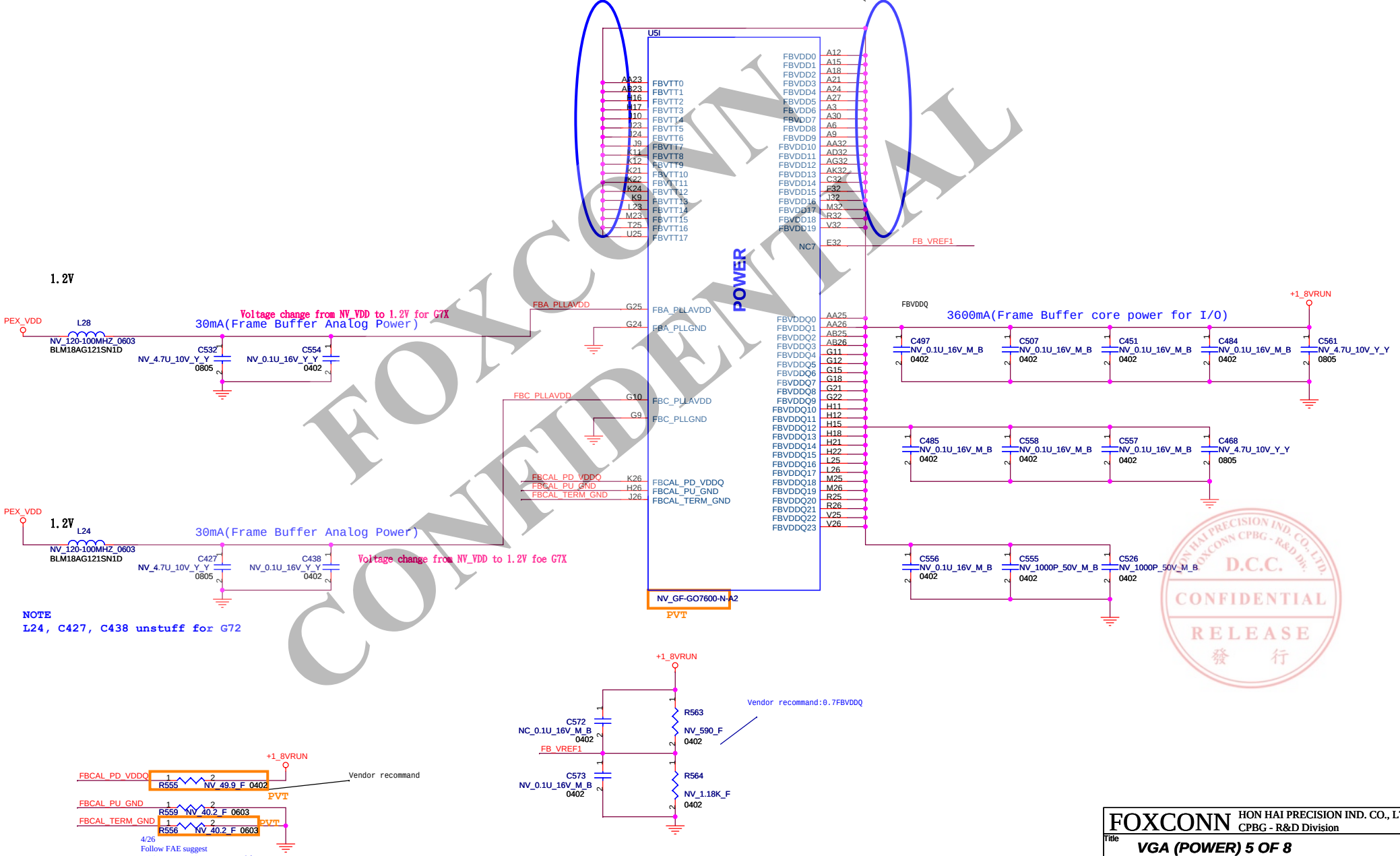
Follow FAE suggest the design guide table 4-4 and 4-5.
DDR1 underminated solution,so FBVTT/FBVDDQ/FBVDD can connect together.
for the power rails decoupling,FBVTT/FBVDD do not require caps decoupling.
only FVDDQ power rail required.



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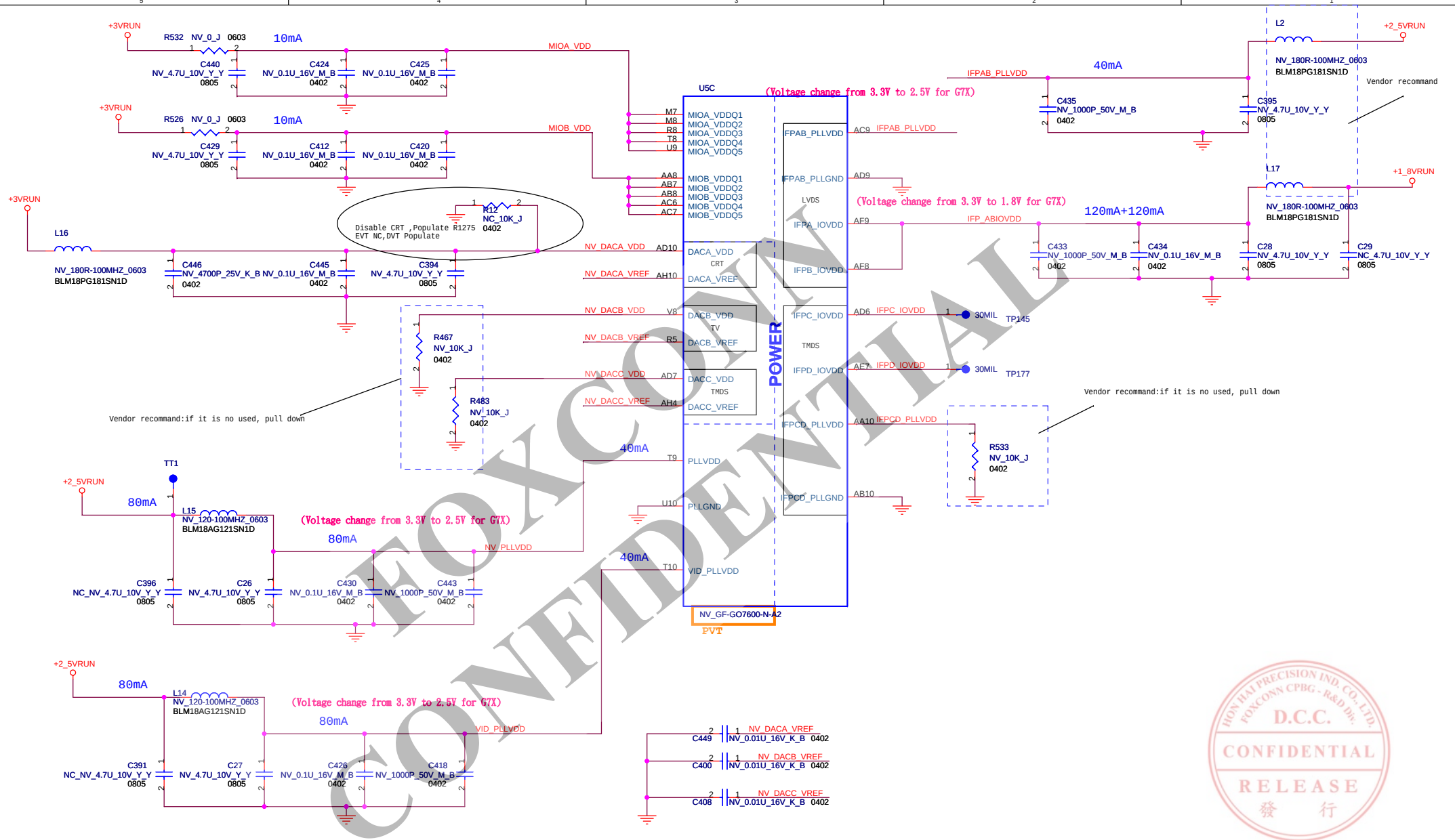
| Title | VGA (POWER) 5 OF 8 | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 20 of 67 | |








| | | |
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| Title | VGA (POWER) 6 OF 8 | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 21 of 67 | |

SM bus Address :
1001100(EC)
For F75383M

U8 close to DDR SO-DIMM

Disable DVI

ROM interface can be NC if not use.
FAE Suggest

C409,C402 unstuffed for G7X

TSTCLK_OUT and TSTCLK_OUT# can be NC for G7X,FAE suggest

close to VGA

close to thermal IC

DVT

Update New version

Check Spec.

4/26
Follow FAE suggest

PVT

Vendor recommand

PVT (DUMMY)

Shortest stub.
Place near GPU

Place near SSCK IC (U9)

| GPIO TABLE | | | |
|---|---|---|---|
| | I/O | Inter pull low | |
| GPIO0 | I | Yes | DVI Hot Plug Detect 0 (HPD0) |
| GPIO1 | I | Yes | Hot Plug Detect 1 (HPD1) |
| GPIO2 | O | Yes | Panel Brightness (PWM) **Active High** |
| GPIO3 | O | No | Panel Power **Active Low** |
| GPIO4 | O | Yes | Panel Backlight On/Off **Active High** |
| GPIO5 | O | Yes | GPU Voltage CTL0 H: NVDD=1.1V |
| GPIO6 | O | Yes | GPU Voltage CTL1 H: NVDD=1.0V |
| GPIO7 | O | Yes | MEM VID |
| GPIO8 | I | No | Thermal Alert **Active Low** |
| GPIO9 | O | No(Low) | Fan control. Support either PWM or on/off |
| GPIO10 | I/O | No | Available for general use. |
| GPIO11 | O | No(Low) | Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7) |
| GPIO12 | O | No | Available for general use. |

ENS : H->SS ON
L->SS OFF
XPD : H->Normal
L->Power Down



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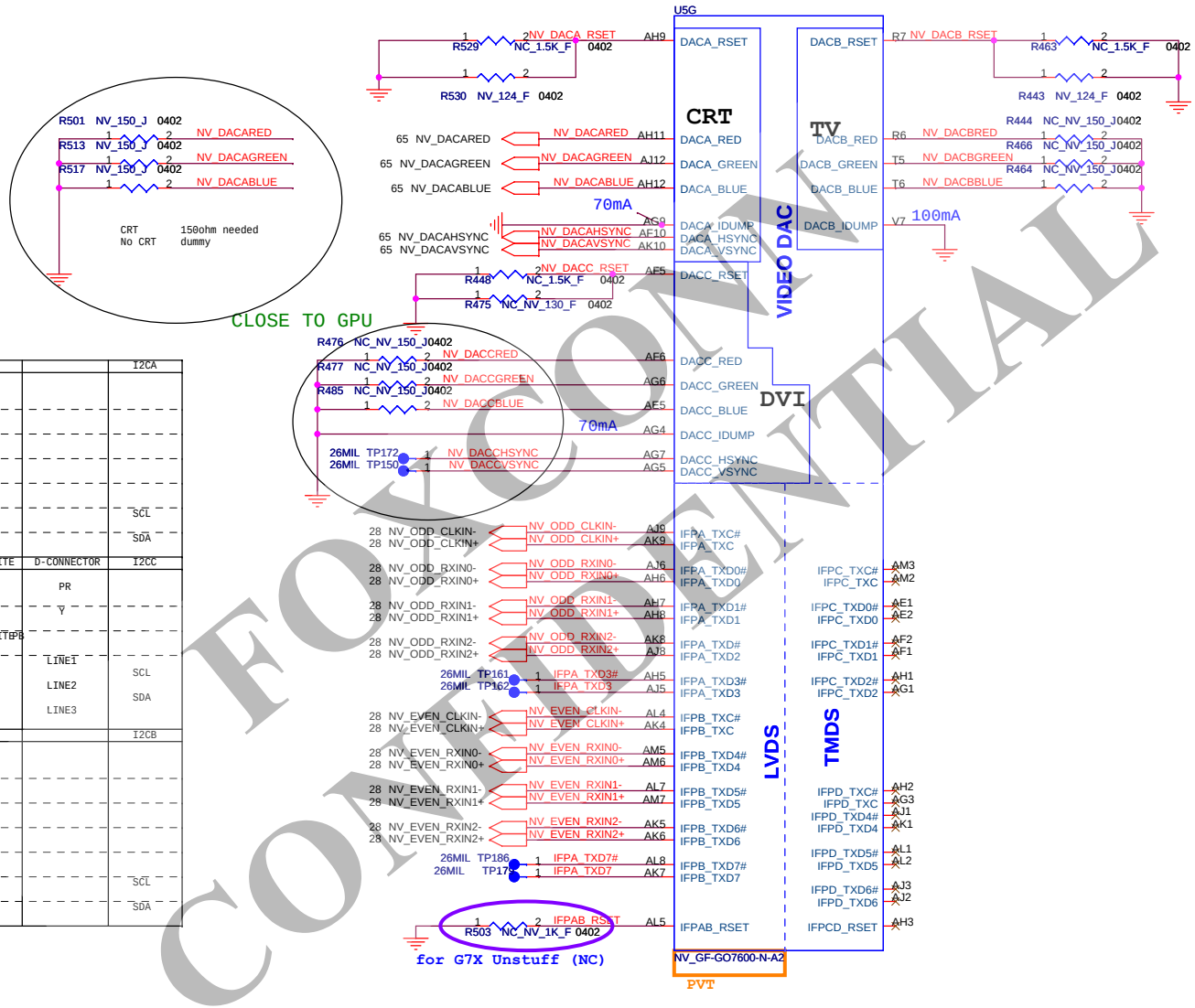
Title: VGA (POWER) 7 OF 8

Size: A3 | Document Number: MS30-1-01 | Rev: 1.00

Date: Friday, March 31, 2006 | Sheet 22 of 67




| DACA | VGA-CRT | | | I2CA |
|---|---|---|---|---|
| DACA-RED | R | | | |
| DACA-GREEN | G | | | |
| DACA-BLUE | B | | | |
| DACA-HSYNC | HSYNC | | | |
| DACA-VSYNC | VSYNC | | | |
| | VGA-DDCCLK | | | SCL |
| | VGA-DDCDATA | | | SDA |
| **DACB** | **S-VIDEO** | **COMPOSITE** | **D-CONNECTOR** | **I2CC** |
| DACB-RED | C | | PR | |
| DACB-GREEN | Y | | Y | |
| DACB-BLUE | | COMPOSITE | | |
| | | | LINE1 | SCL |
| | | | LINE2 | SDA |
| | | | LINE3 | |
| **DACC** | **DVI-I** | | | **I2CB** |
| DACC-RED | R | | | |
| DACC-GREEN | G | | | |
| DACC-BLUE | B | | | |
| DACC-HSYNC | HSYNC | | | |
| DACC-VSYNC | VSYNC | | | |
| | DVI-DDCCLK | | | SCL |
| | DVI-DDCDATA | | | SDA |





| | | |
|---|---|---|
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| Title | VGA (POWER) 8 OF 8 | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 23 of 67 | |

**Address / Command on Die termination is set to 120 ohm.**

U30 — NV_HYB18H512321AFL20

U31 — NV_HYB18H512321AFL20

**DLL POWER --- Add decoupling C and L ?**

Minimum 200us delay required prior to applying any executable command after stable power and clock.

**For 16Mx32 Bit stuff**
**8Mx32 Bit no stuff**

**For 8Mx32 Bit Stuff**
**16Mx32 Bit no stuff**

FAE suggestion on 8/16==>120 ohm
For garbage display ===>80.6 ohm
Demo circuit ===>40.2 ohm
FAE suggestion in DVT ===>240 ohm

**VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V**

**VRAM_VREF is 70%FBVDDQ for GDDR3**



| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division |
| Title | VRAM (GDDR3) 1 OF 4 |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 24 of 67 |

**Address / Command on Die termination is set to 120 ohm.**

U28

U29

Minimum 200us delay required prior to applying any executable command after stable power and clock.

For 16Mx32 Bit stuff
8Mx32 Bit no stuff

For 8Mx32 Bit Stuff
16Mx32 Bit no stuff

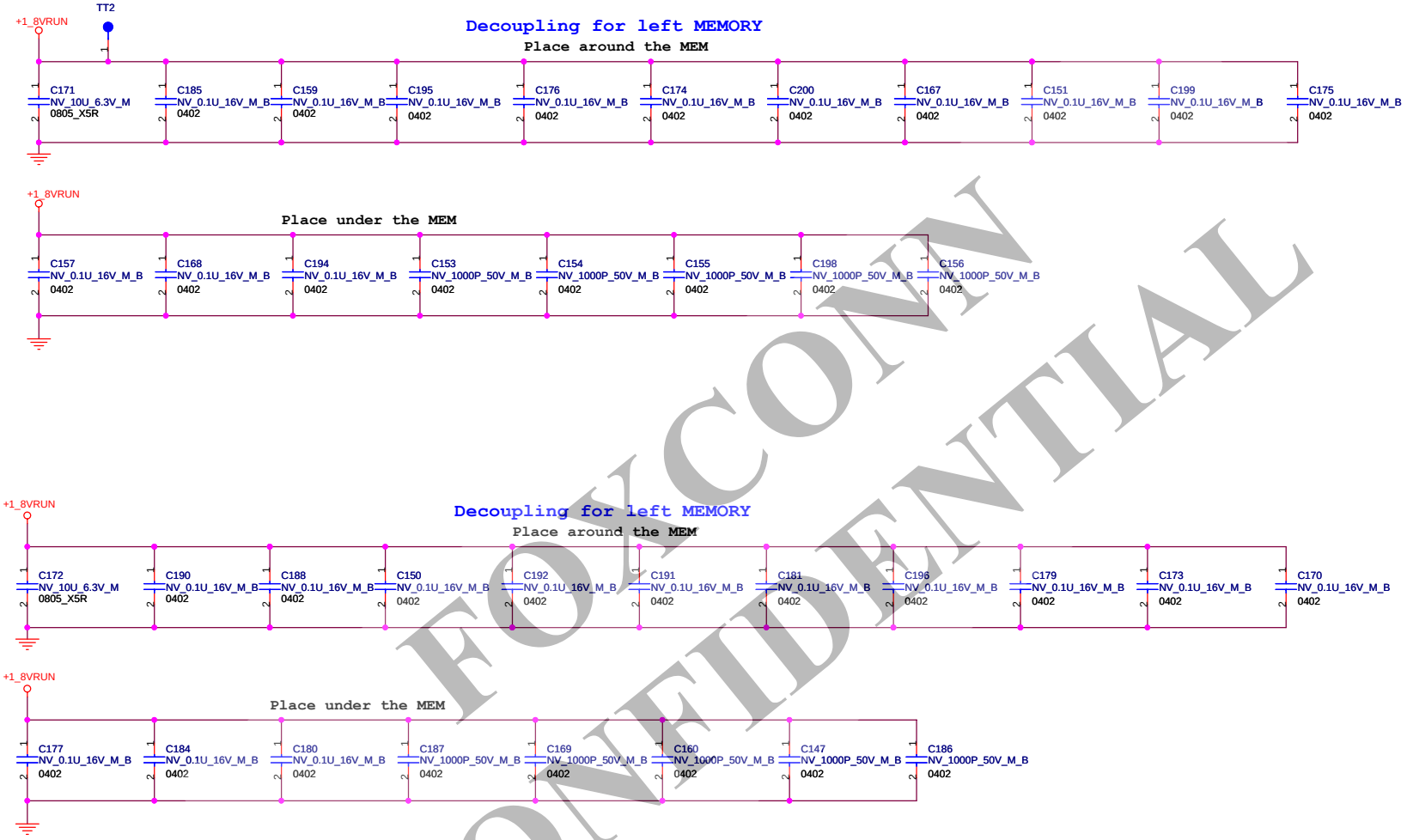
VRAM_VREF is 70% FBVDDQ for GDDR3 1.26V

VRAM_VREF is 70% FBVDDQ for GDDR3

FAE suggestion on 8/16==>120 ohm
For garbage display ===>80.6 ohm
nvidia demo circuit for G72 ==>40.2_F
FAE suggestion in DVT ==>240 ohm



| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division |
| Title | VRAM (GDDR3) 2 OF 4 |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 25 of 67 |

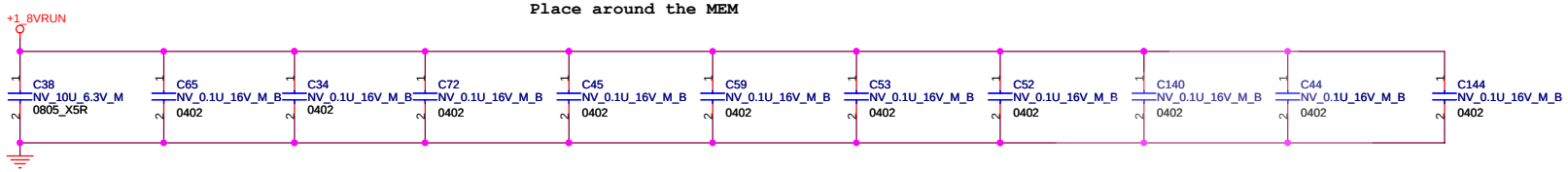





| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title: VRAM (GDDR) 3 OF 4 | | |
| Size: A3 | Document Number: MS30-1-01 | Rev: 1.00 |
| Date: Friday, March 31, 2006 | Sheet 26 of 67 | |

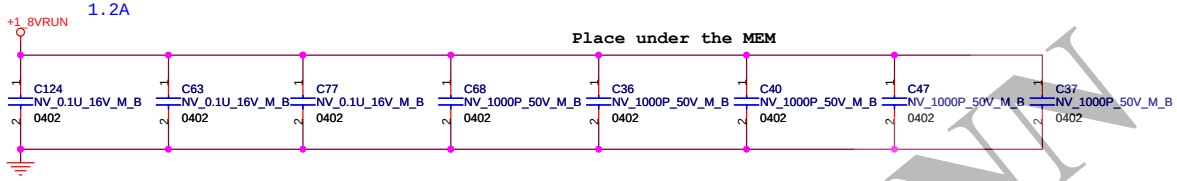
## Decoupling for right MEMORY

Place around the MEM




1.2A

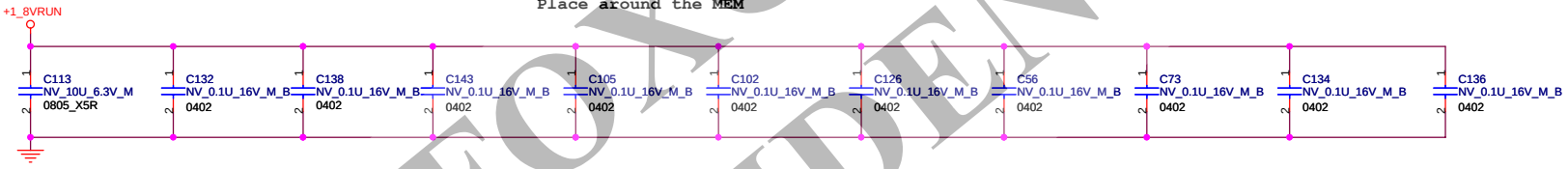
Place under the MEM




NO USE

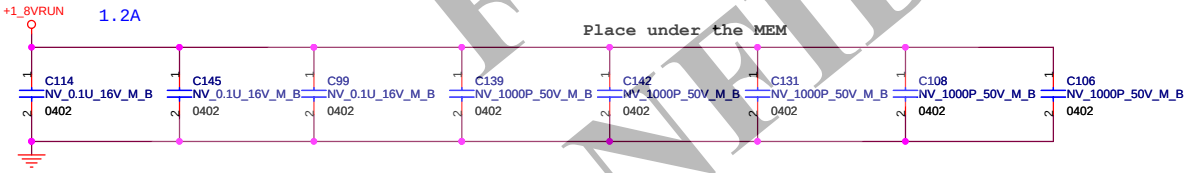
## Decoupling for right MEMORY

Place around the MEM



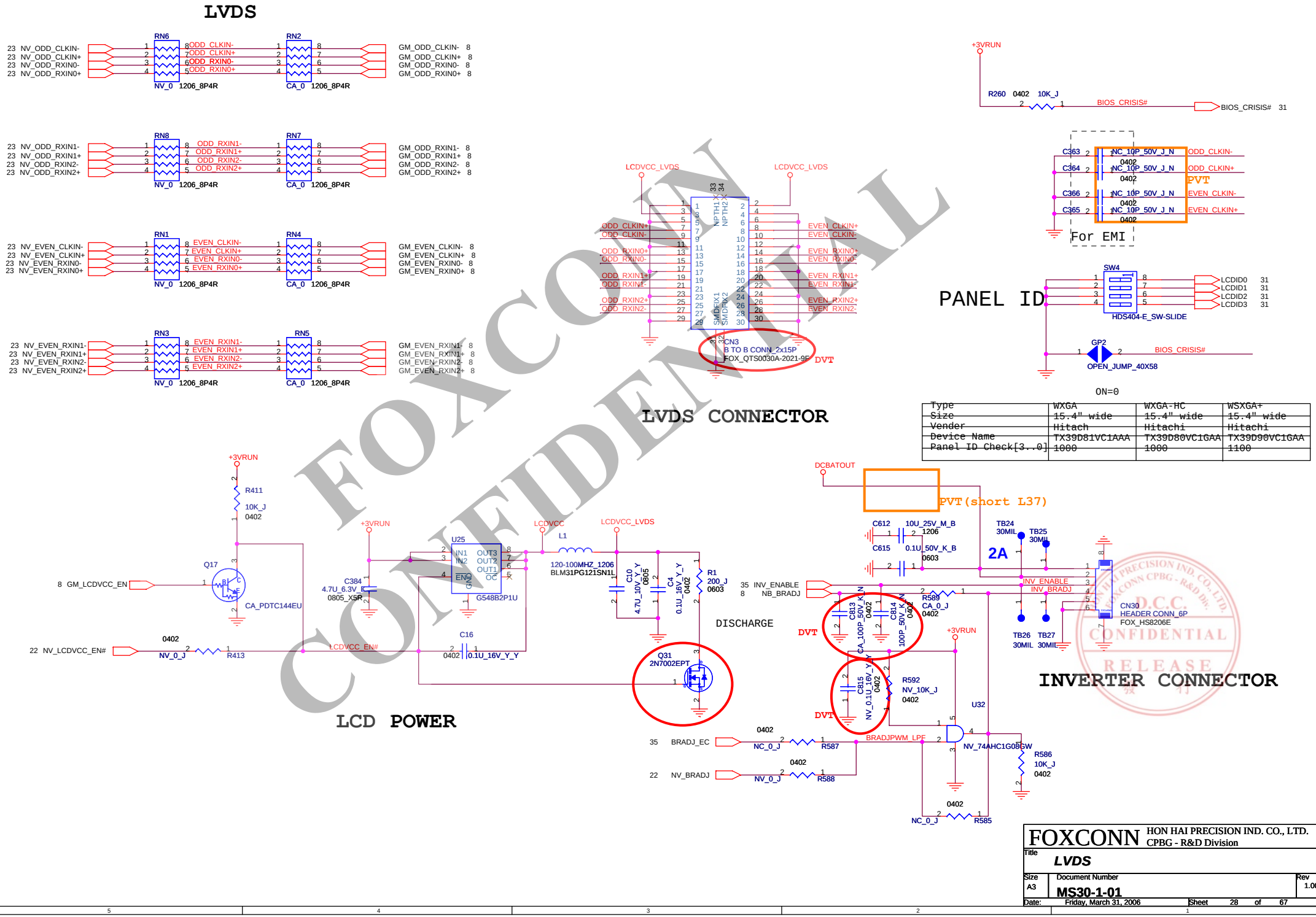

1.2A

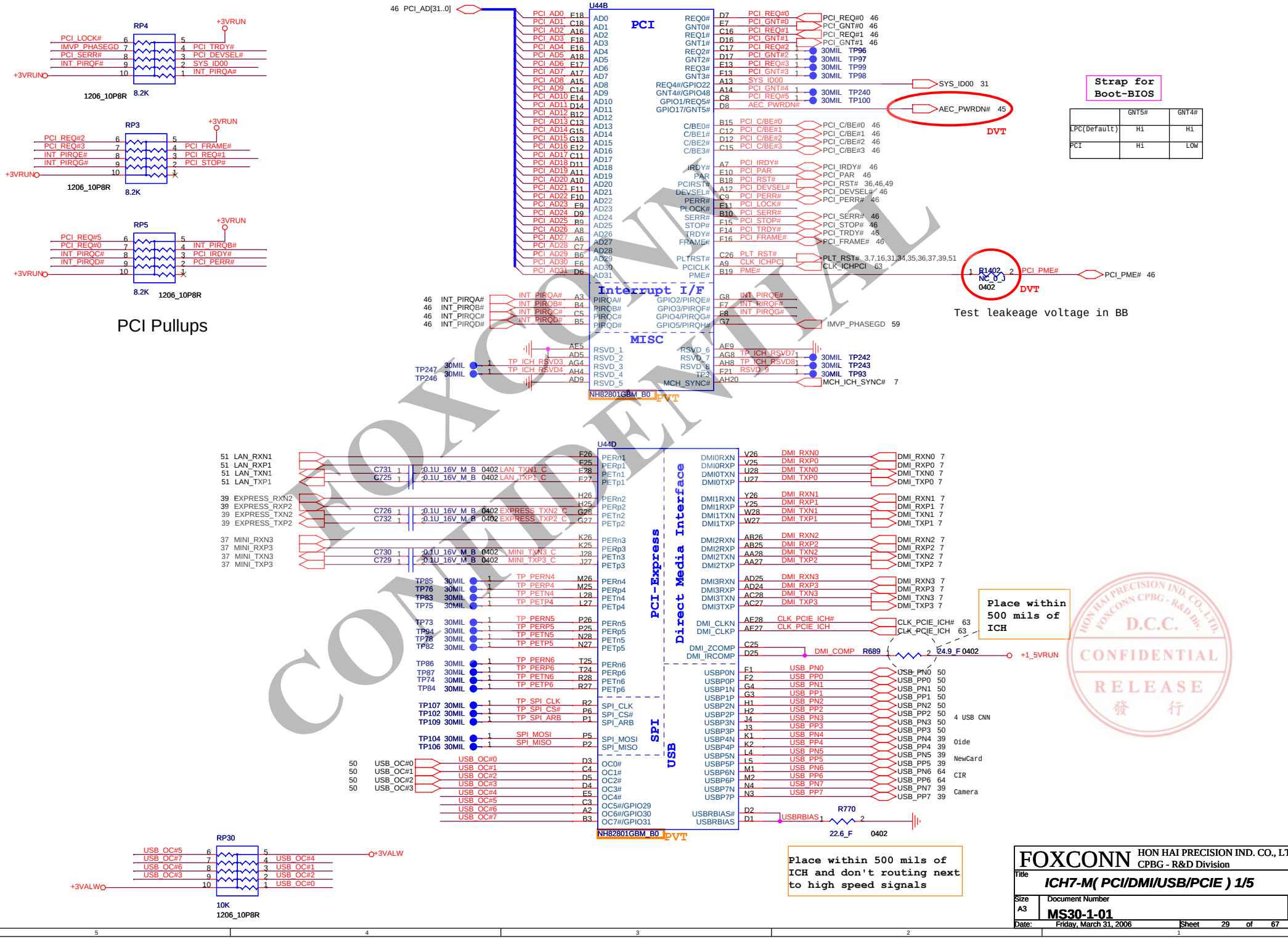
Place under the MEM






| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | VRAM (POWERBYPASS) 4 OF 4 | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 27 of 67 | |




RP4
PCI_LOCK#
IMVP_PHASEGD
PCI_SERR#
INT_PIRQF#
+3VRUN
PCI_TRDY#
PCI_DEVSEL#
SYS_ID00
INT_PIRQA#
1206_10P8R
8.2K
RP3
PCI_REQ#2
PCI_REQ#3
INT_PIRQE#
INT_PIRQG#
PCI_FRAME#
PCI_REQ#1
PCI_STOP#
RP5
PCI_REQ#5
PCI_REQ#0
INT_PIRQC#
INT_PIRQD#
INT_PIRQB#
PCI_IRDY#
PCI_PERR#
PCI Pullups
46 PCI_AD[31..0]
U44B
PCI
Interrupt I/F
MISC
NH82801GBM_B0
PVT
Strap for Boot-BIOS
GNT5#
GNT4#
LPC(Default)
PCI
DVT
Test leakeage voltage in BB
U44D
PCI-Express
Direct Media Interface
USB
SPI
Place within 500 mils of ICH
Place within 500 mils of ICH and don't routing next to high speed signals
RP30
10K
1206_10P8R
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH7-M( PCI/DMI/USB/PCIE ) 1/5
MS30-1-01
Rev 1.00
Friday, March 31, 2006
Sheet 29 of 67
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RTCRST#

VccRTC

Min : 5ms

The traces inside this block should be wider.

No digital signals routed under XTAL

+ECVCC

VCCRTC

D14 SCS500V-40-LF

C805 1U_6.3V_M_B 0402

32.768KHZ_12.5P_10PPM Q13MC3061001800

Y7

C799 0402 15P_50V_K_N CLK_32KX1

C802 0402 15P_50V_K_N CLK_32KX2

6 mils

R765 10M_J 0402

R378 20K_J 0402

C353 1U_25V_K_B 0603

R784 510_F 0402

R379 1M_J 0402

R785 510_F 0402

OPEN_JUMP_OPEN2 PJ31

PVT

A3504

CN23 HEADER_2P FOX_HS8102E

U44A

RTCX1 RTCX2 RTCRST# INTRUDER# INTVRMEN

SM_INTRUDER# INTVRMEN

EE_CS EE_SHCLK EE_DOUT EE_DIN

LAN_CLK LAN_RSTSYNC LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2

ACZ_BIT_CLK ACZ_SYNC ACZ_RST# ACZ_SDIN0 ACZ_SDIN1 ACZ_SDIN2 ACZ_SDOUT

SATALED# SATA0RXN SATA0RXP SATA0TXN SATA0TXP SATA2RXN SATA2RXP SATA2TXN SATA2TXP SATA_CLKN SATA_CLKP SATARBIASN SATARBIASP

DIOR# DIOW# DDACK# IDEIRQ IORDY DDREQ

NH82801GBM_B0

PVT

RTC LPC LAN CPU AC-97/AZALIA SATA IDE

LAD0 LAD1 LAD2 LAD3 LDRQ0# LDRQ1#/GPIO23 LFRAME# A20GATE A20M# CPUSLP# TP1/DPRSTP# TP2/DPSLP# FERR# GPIO49/CPUPWRGD IGNNE# INIT3_3V# INIT# INTR RCIN# NMI SMI# STPCLK# THERMTRIP#

DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15

DA0 DA1 DA2 DCS1# DCS3#

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_DRQ#0 SYS_ID01 LPC_FRAME# H_A20GATE H_A20M# TP_CPUSLP# H_DPRSTP# H_DPSLP# H_FERR# H_PWRGD H_IGNNE# FWH_INIT# H_INIT# H_INTR H_RCIN# H_NMI H_SMI# H_STPCLK# PM_THRMTRIP#

IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15

IDE_PDA0 IDE_PDA1 IDE_PDA2 IDE_PDCS1# IDE_PDCS3#

+3VRUN

R370 10K_J 0402

R706 10K_J 0402 H_RCIN#

R294 8.2K_J 0402 H_A20GATE

DVT (delete R702,R697 and short)

30MIL TP80

R690 56_J 0402 +1_05VRUN

R692 56_J 0402 +1_05VRUN

R715 NC_10K_J 0402

ACZ_SDATAIN0 ACZ_MDC_SDATAIN1 IAC_BITCLK IAC_SYNC IAC_RESET# IAC_SDATAO

TP108 30MIL

SATA_LED#

SATA_RXN0 SATA_RXP0 SATA_TXN0 SATA_TXP0

C787 C788 C792 C790 3900P_25V_K_B 0603

SATA_RXN0_C SATA_RXP0_C SATA_TXN0_C SATA_TXP0_C

SATA_TXN2 SATA_TXP2

TP245 30MIL TP244 30MIL

CLK_PCIE_SATA# CLK_PCIE_SATA

DVT for MS50 sata cable

R745 24.9_F 0402 R1175 NC_MS50_20_F 0402

A3502

IDE_PDIOR# IDE_PDIOW# IDE_PDDACK# INT_IRQ14 IDE_PDIORDY IDE_PDDREQ

R380 332K_F 0402 INTVRMEN

Pull-up to enable internal VccSus1_05 regular

Pull-Low to disable

Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

R763 39_J 0402 ACZ_BITCLK

R383 39_J 0402 IAC_BITCLK_AUDIO

EC1 10P_50V_J_N 0402

DVT for EMI

R762 39_J 0402 ACZ_SDATAOUT

R385 39_J 0402 IAC_SDATAO_AUDIO

DVT

R389 47_J 0402 ACZ_RST#

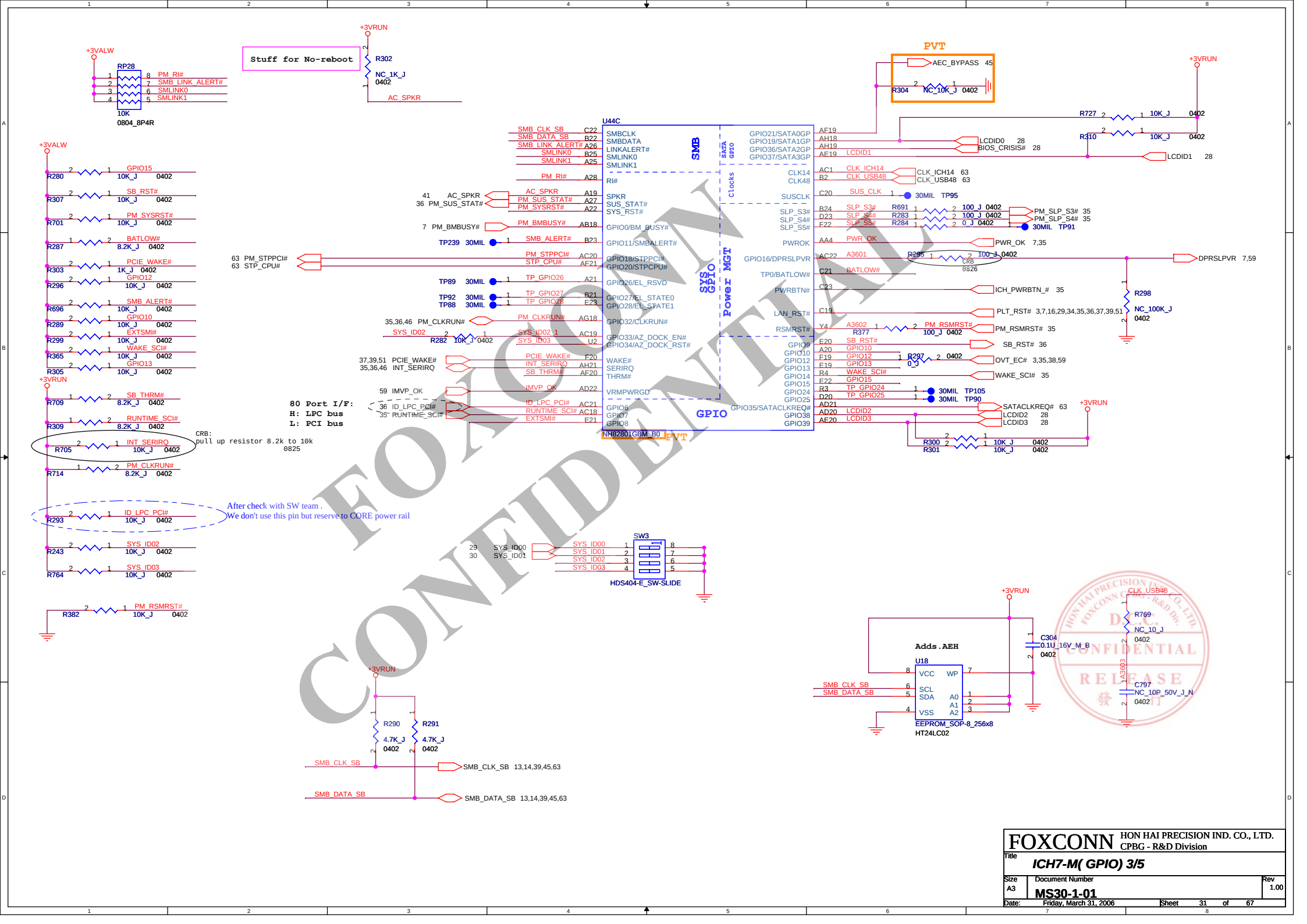
R776 47_J 0402 IAC_RESET#_AUDIO

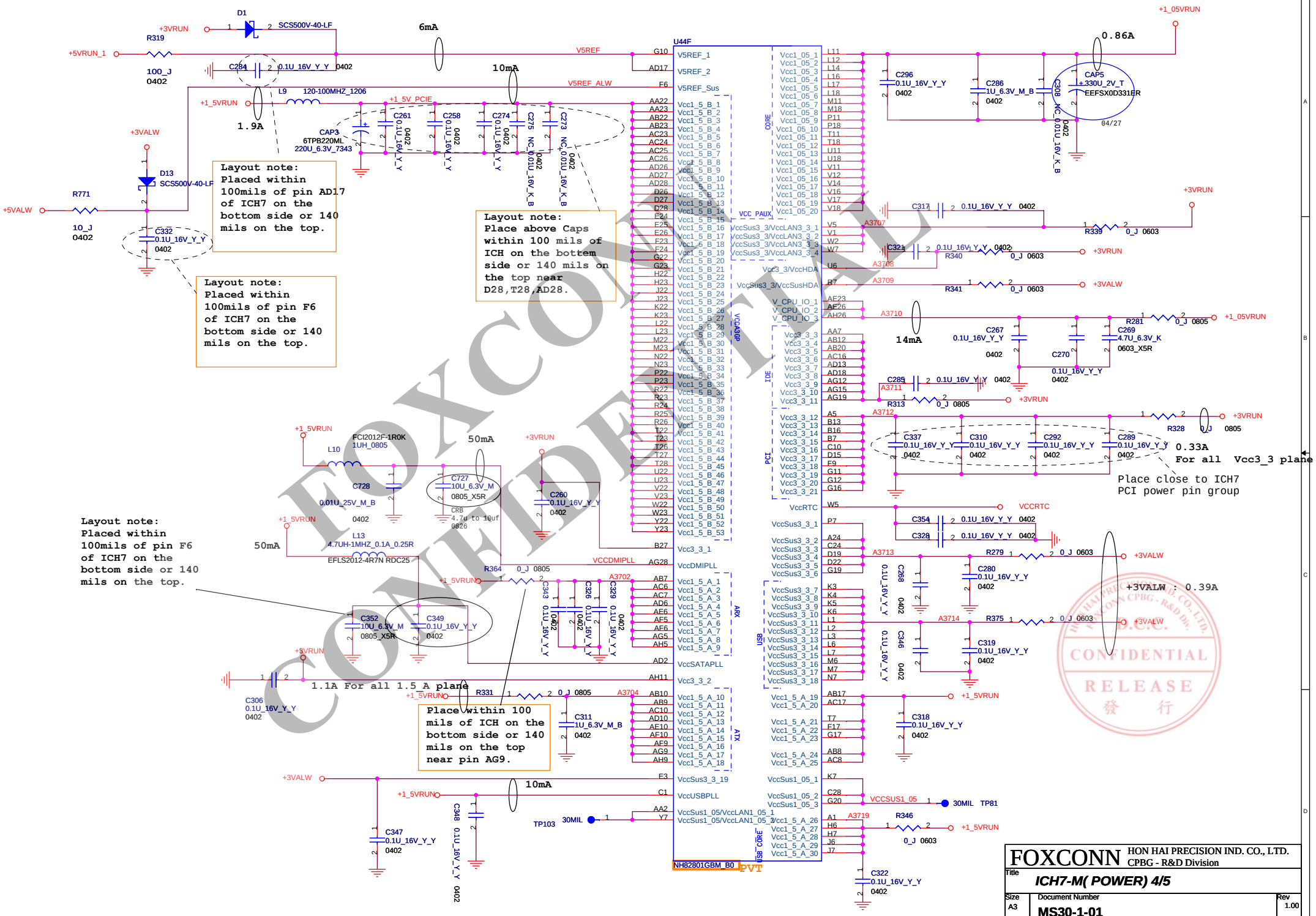
R761 39_J 0402 IAC_SYNC

R384 39_J 0402



| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | ICH7-M( LPC,IDE,SATA ) 2/5 | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 30 of 67 | |


+3VALW
RP28
PM_RI#
SMB_LINK_ALERT#
SMLINK0
SMLINK1
10K
0804_8P4R
Stuff for No-reboot
+3VRUN
R302
NC_1K_J
0402
AC_SPKR
PVT
AEC_BYPASS 45
R304 NC_10K_J 0402
U44C
SMB
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
Clocks
CLK14
CLK48
SUSCLK
SYS GPIO
Power MGT
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35/SATACLKREQ#
GPIO38
GPIO39
GPIO
SMB_CLK_SB
SMB_DATA_SB
SMB_LINK_ALERT#
SMLINK0
SMLINK1
PM_RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26/EL_RSVD
GPIO27/EL_STATE0
GPIO28/EL_STATE1
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
NH82801GBM_B0
PVT
AC_SPKR
PM_SUS_STAT#
PM_SYSRST#
PM_BMBUSY#
SMB_ALERT#
PM_STPPCI#
STP_CPU#
TP_GPIO26
TP_GPIO27
TP_GPIO28
PM_CLKRUN#
SYS_ID02
SYS_ID03
PCIE_WAKE#
INT_SERIRQ
SB_THRM#
IMVP_OK
ID_LPC_PCI#
RUNTIME_SCI#
EXTSMI#
80 Port I/F:
H: LPC bus
L: PCI bus
CLK_ICH14
CLK_USB48
SUS_CLK
SLP_S3#
SLP_S4#
SLP_S5#
PWR_OK
A3601
DPRSLPVR
ICH_PWRBTN_# 35
PLT_RST# 3,7,16,29,34,35,36,37,39,51
PM_RSMRST#
SB_RST# 36
GPIO10
GPIO12
GPIO13
WAKE_SCI#
TP_GPIO24
TP_GPIO25
SATACLKREQ# 63
LCDID2
LCDID3
LCDID0
BIOS_CRISIS#
LCDID1
R298
NC_100K_J
0402
R727
R310
10K_J
0402
R295
CRB
0826
R297
0_J
R691
R283
R284
100_J 0402
0_J 0402
30MIL TP91
30MIL TP95
30MIL TP105
30MIL TP90
R300
R301
10K_J 0402
GPIO15
SB_RST#
PM_SYSRST#
BATLOW#
PCIE_WAKE#
GPIO12
SMB_ALERT#
GPIO10
EXTSMI#
WAKE_SCI#
GPIO13
SB_THRM#
RUNTIME_SCI#
INT_SERIRQ
PM_CLKRUN#
ID_LPC_PCI#
SYS_ID02
SYS_ID03
PM_RSMRST#
CRB:
pull up resistor 8.2k to 10k
0825
After check with SW team .
We don't use this pin but reserve to CORE power rail
SW3
HDS404-E_SW-SLIDE
R290
R291
4.7K_J
0402
Adds.AEH
U18
VCC
WP
SCL
SDA
A0
A1
A2
VSS
EEPROM_SOP-8_256x8
HT24LC02
C304
0.1U_16V_M_B
0402
C797
NC_10P_50V_J_N
R769
NC_10_J
CLK_USB48
FOXCONN
CONFIDENTIAL
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
ICH7-M( GPIO) 3/5
Size
A3
Document Number
MS30-1-01
Rev
1.00
Date:
Friday, March 31, 2006
Sheet
31
of
67


Layout note: Placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top.
Layout note: Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.
Layout note: Place above Caps within 100 mils of ICH on the bottem side or 140 mils on the top near D28,T28,AD28.
Layout note: Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.
Place close to ICH7 PCI power pin group
0.33A For all Vcc3_3 plane
1.1A For all 1.5_A plane
+3VALW : 0.39A
0.86A
14mA
6mA
10mA
50mA
1.9A
U44F
NH82801GBM_B0
PVT
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH7-M( POWER) 4/5
MS30-1-01
Rev 1.00
Friday, March 31, 2006
Sheet 32 of 67
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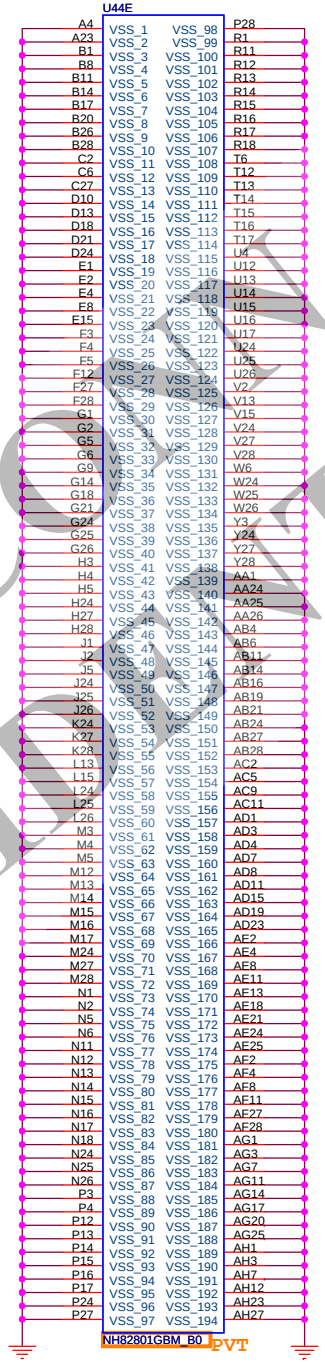
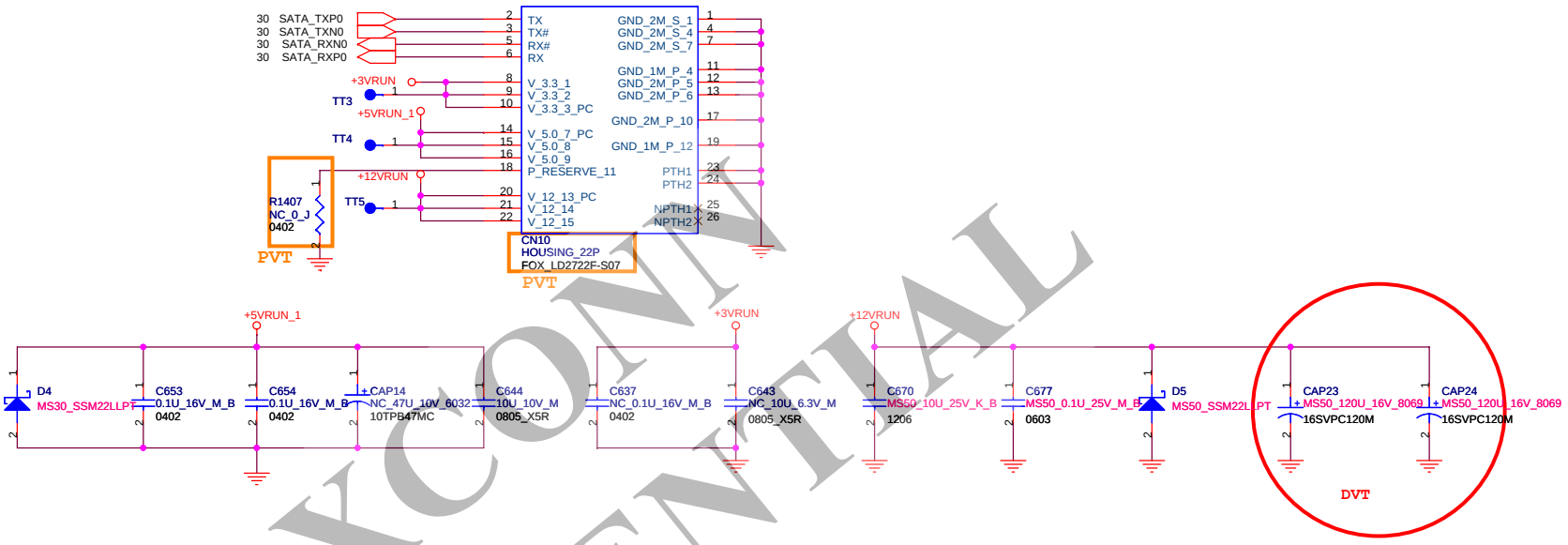


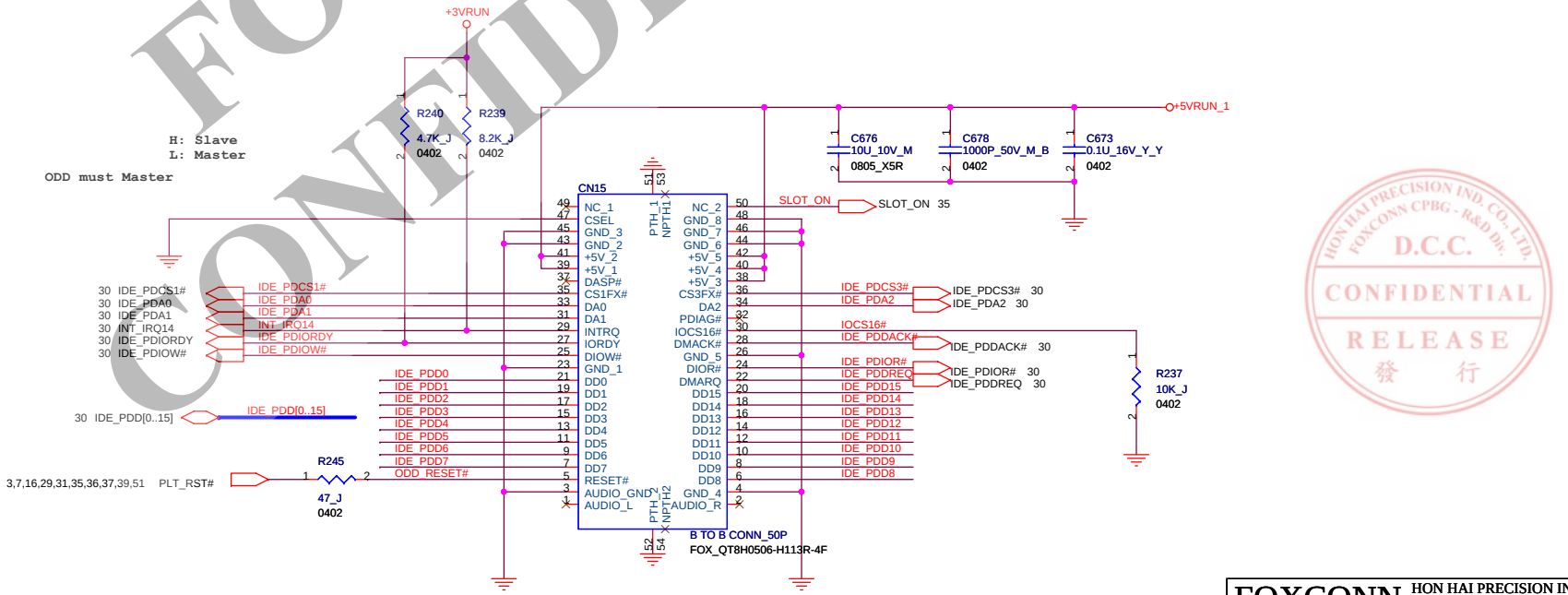





| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | *ICH7-M( GND) 5/5* | |
| Size A3 | Document Number **MS30-1-01** | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 33 of 67 | |

# SATA HDD CONN



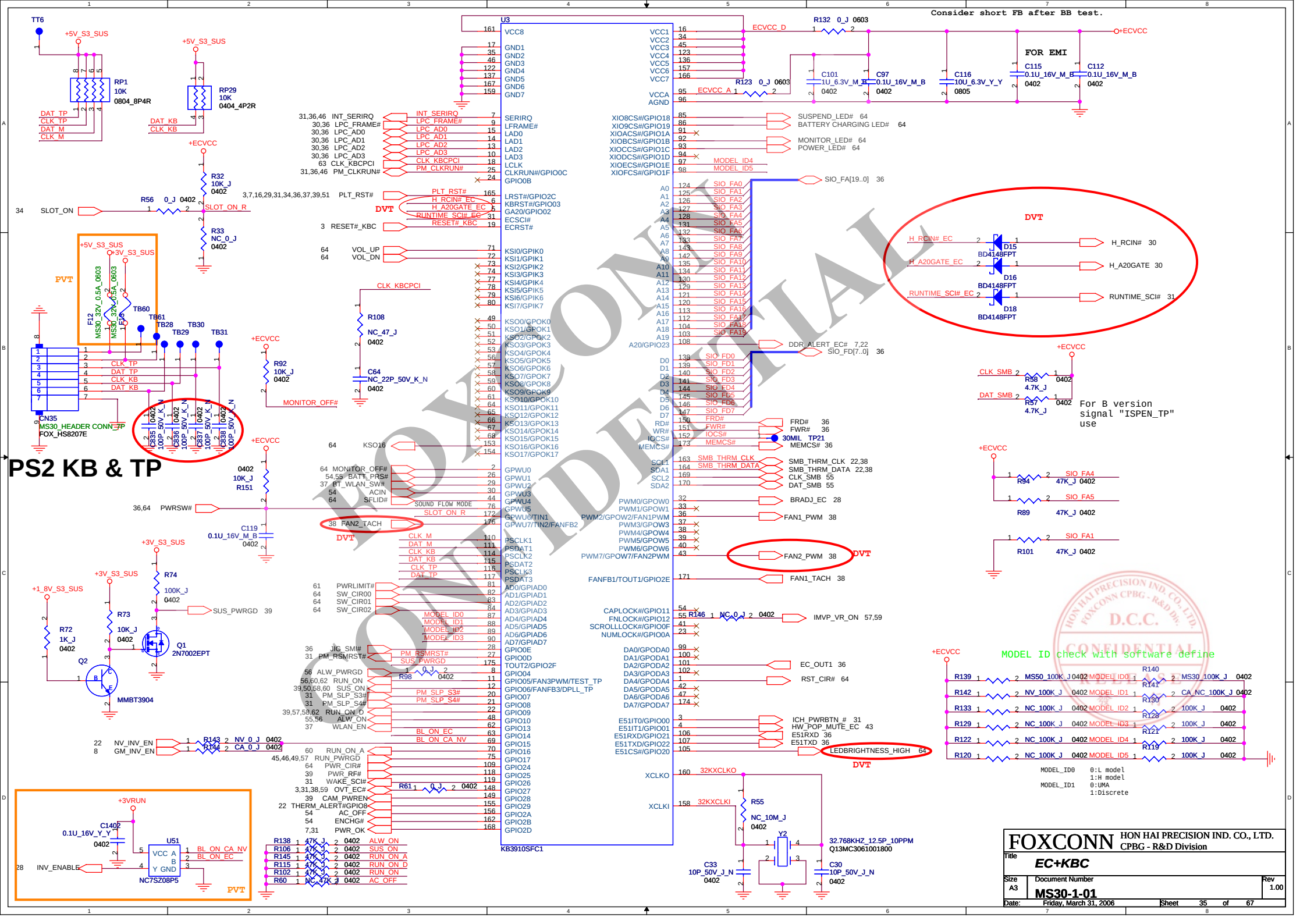

# CD-ROM CONN



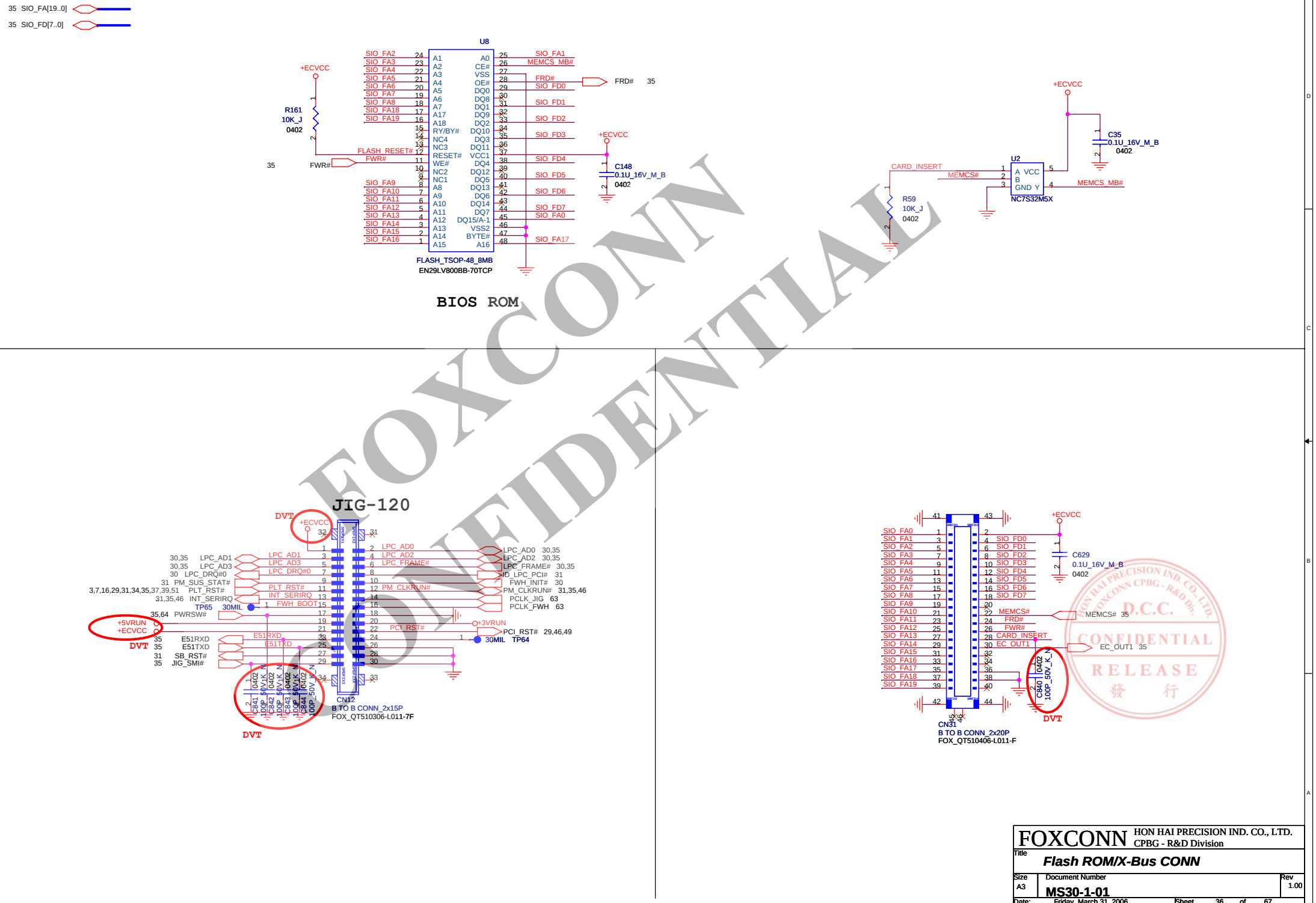
| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | SATA HDD/CD-ROM | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 34 of 67 | |

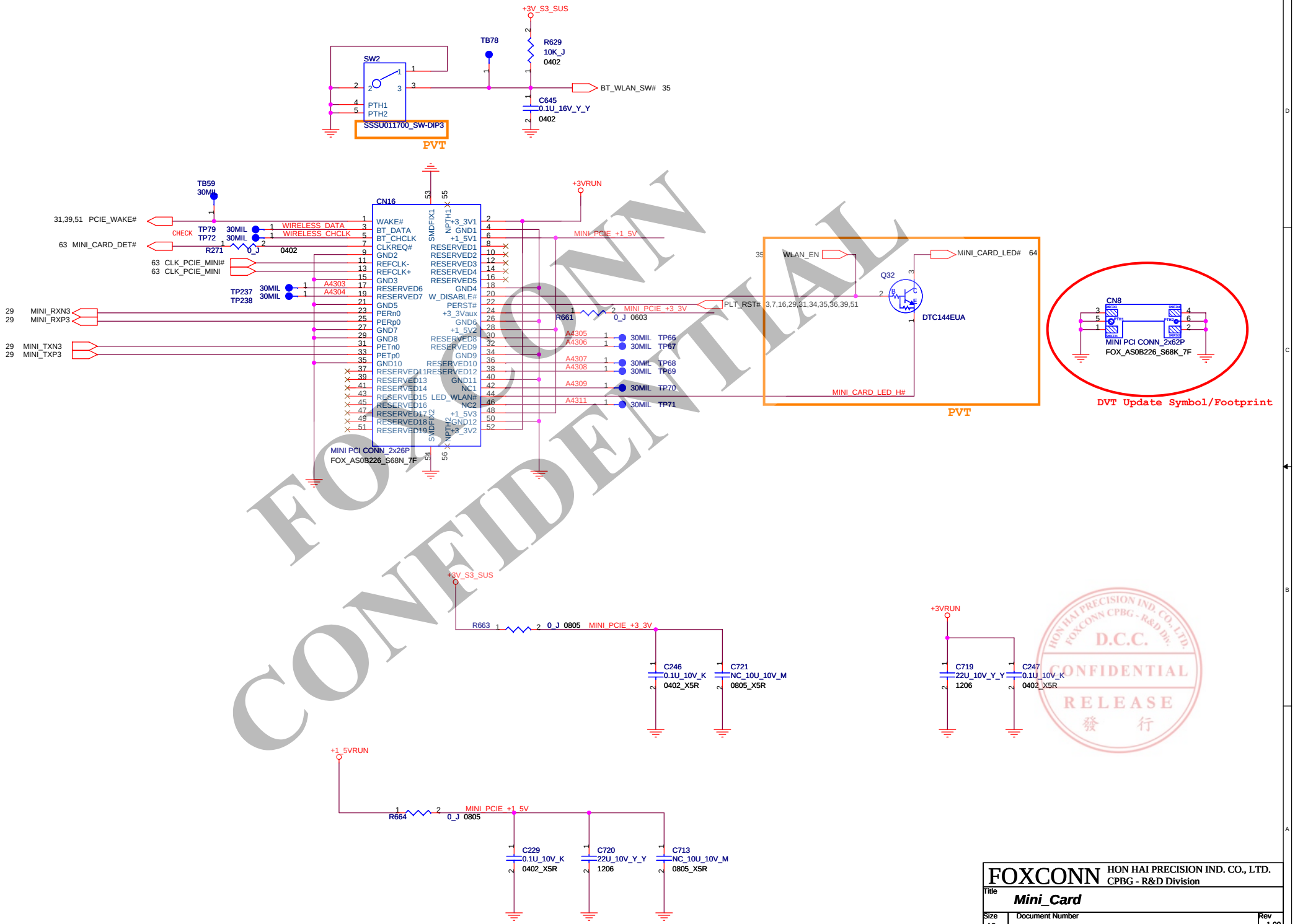
# PS2 KB & TP

Consider short FB after BB test.




| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division |
| Title | EC+KBC |
| Size A3 | Document Number MS30-1-01 Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 35 of 67 |

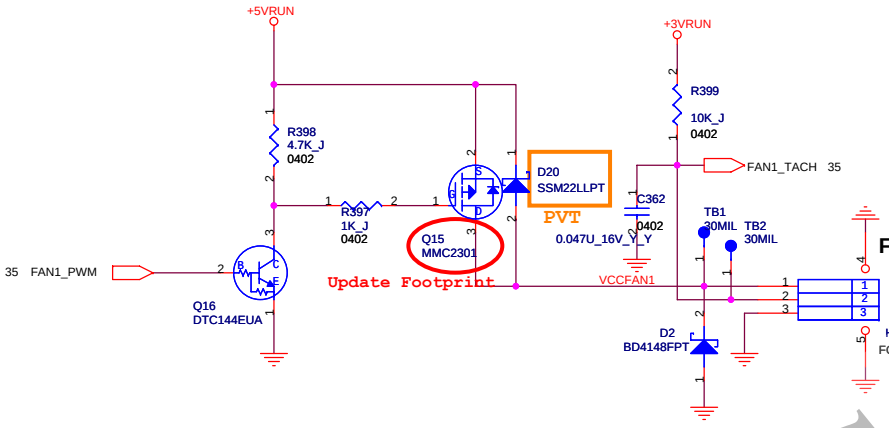




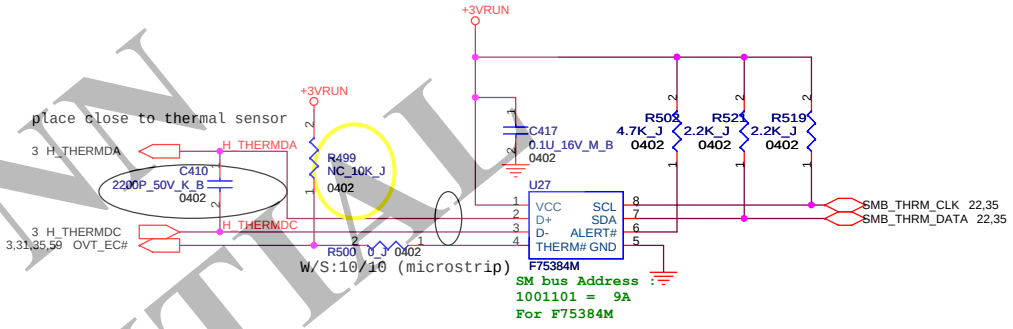



| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | *Mini_Card* | |
| Size A3 | Document Number **MS30-1-01** | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 37 of 67 | |

# FAN

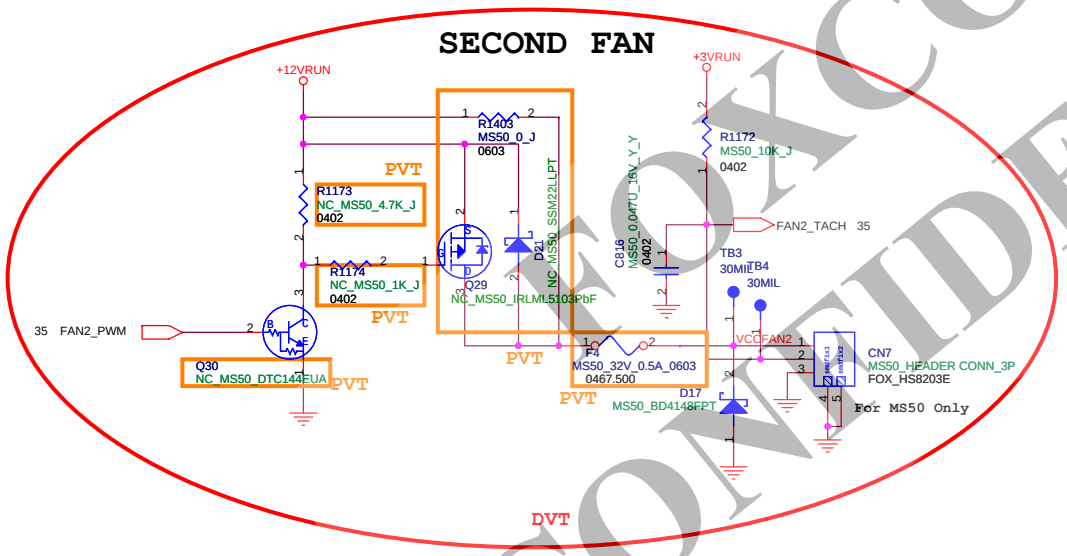



# CPU SENSOR

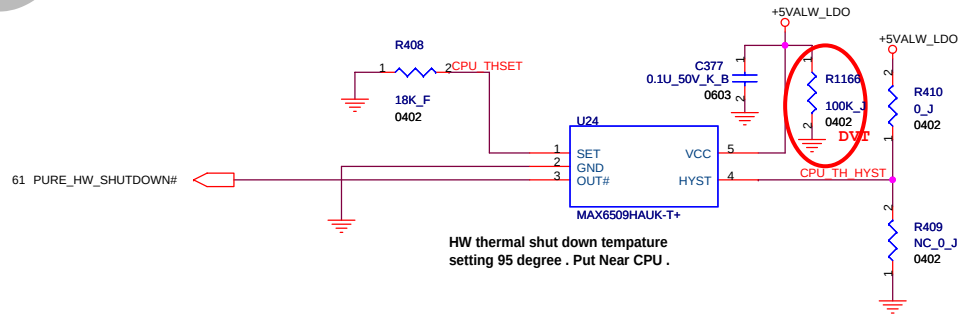



Place Thermal-Sensor near
CPU & GMCH.

# SECOND FAN




# HW THERMAL PROTECTION

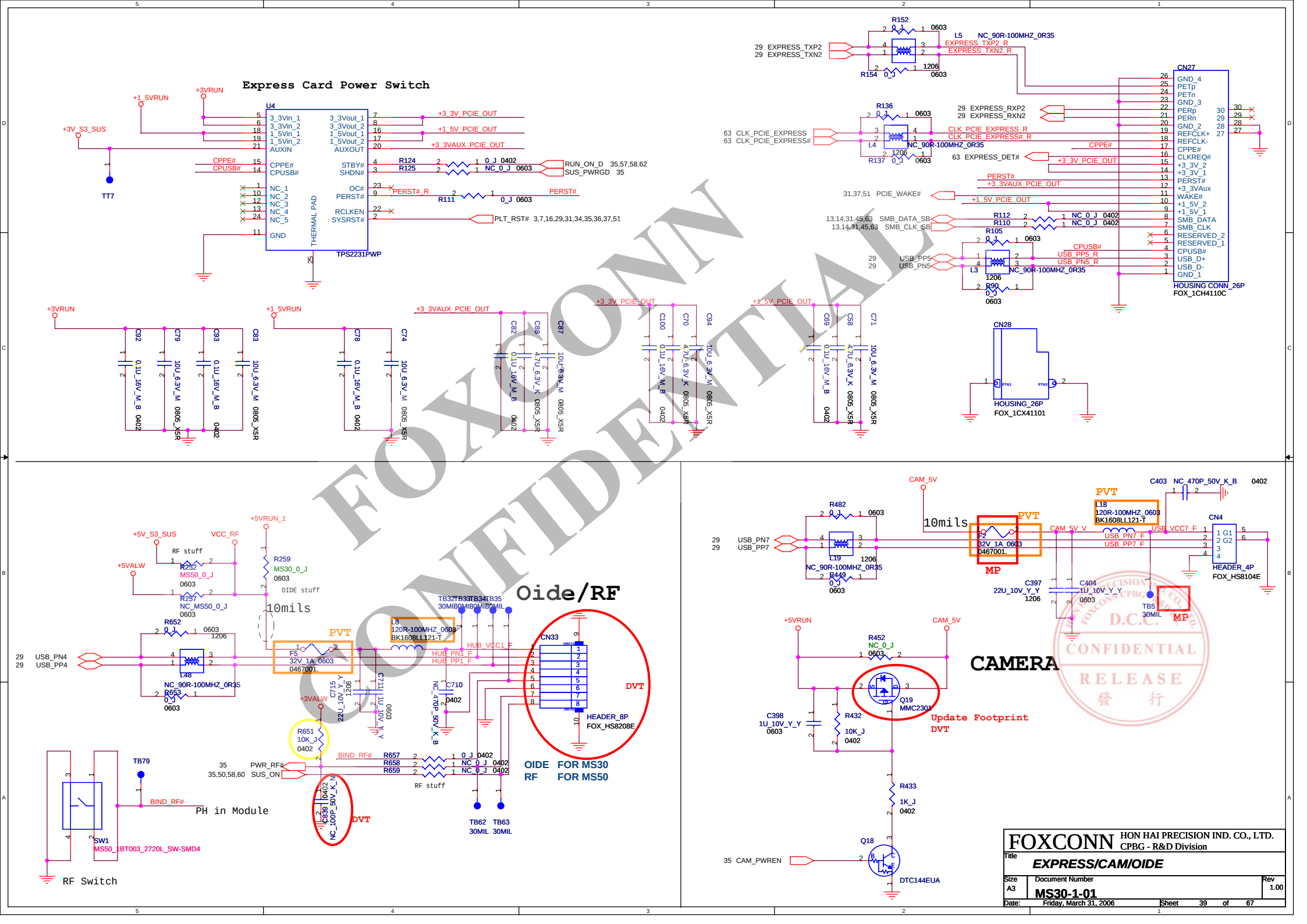


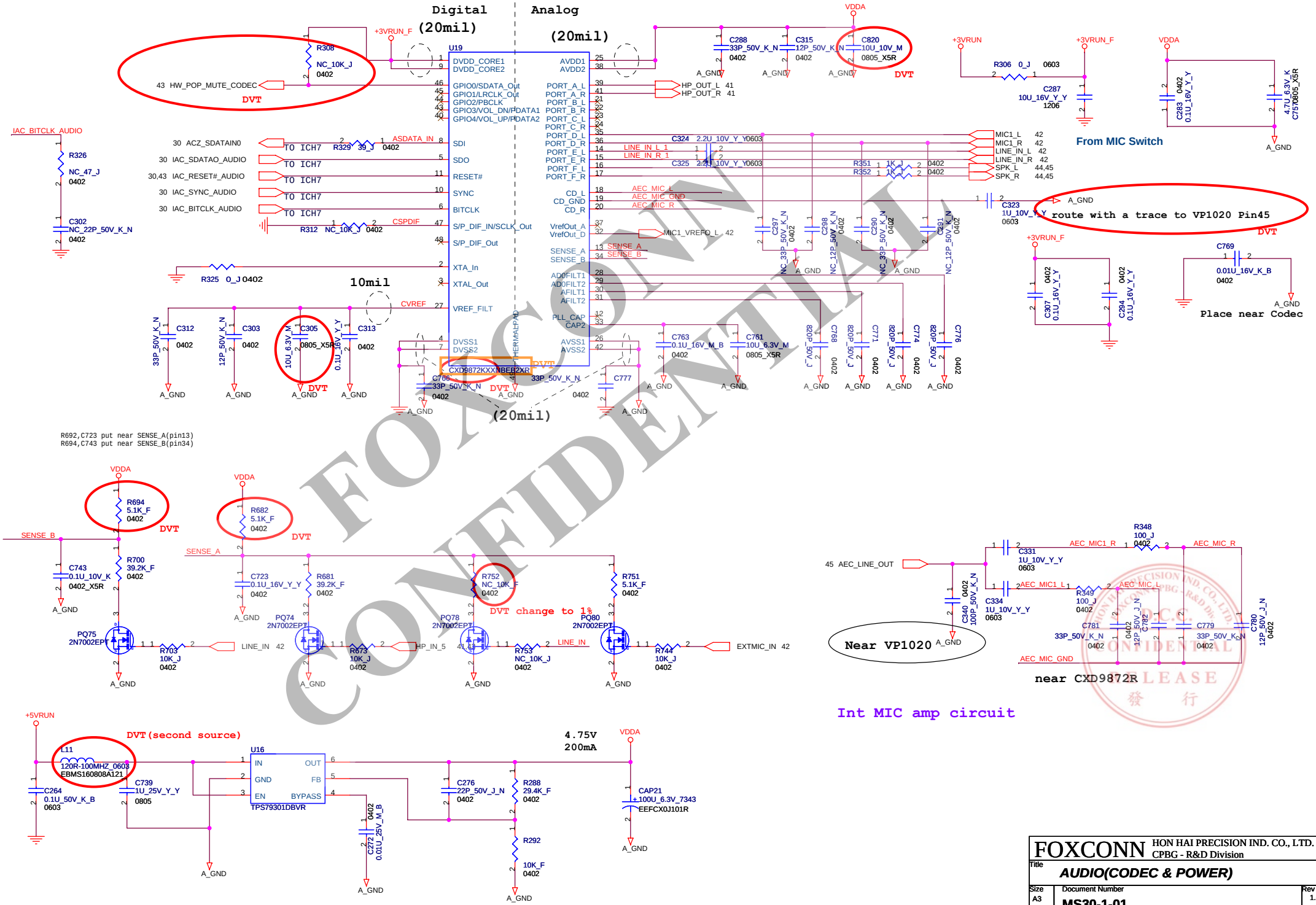

HW thermal shut down tempature
setting 95 degree . Put Near CPU .



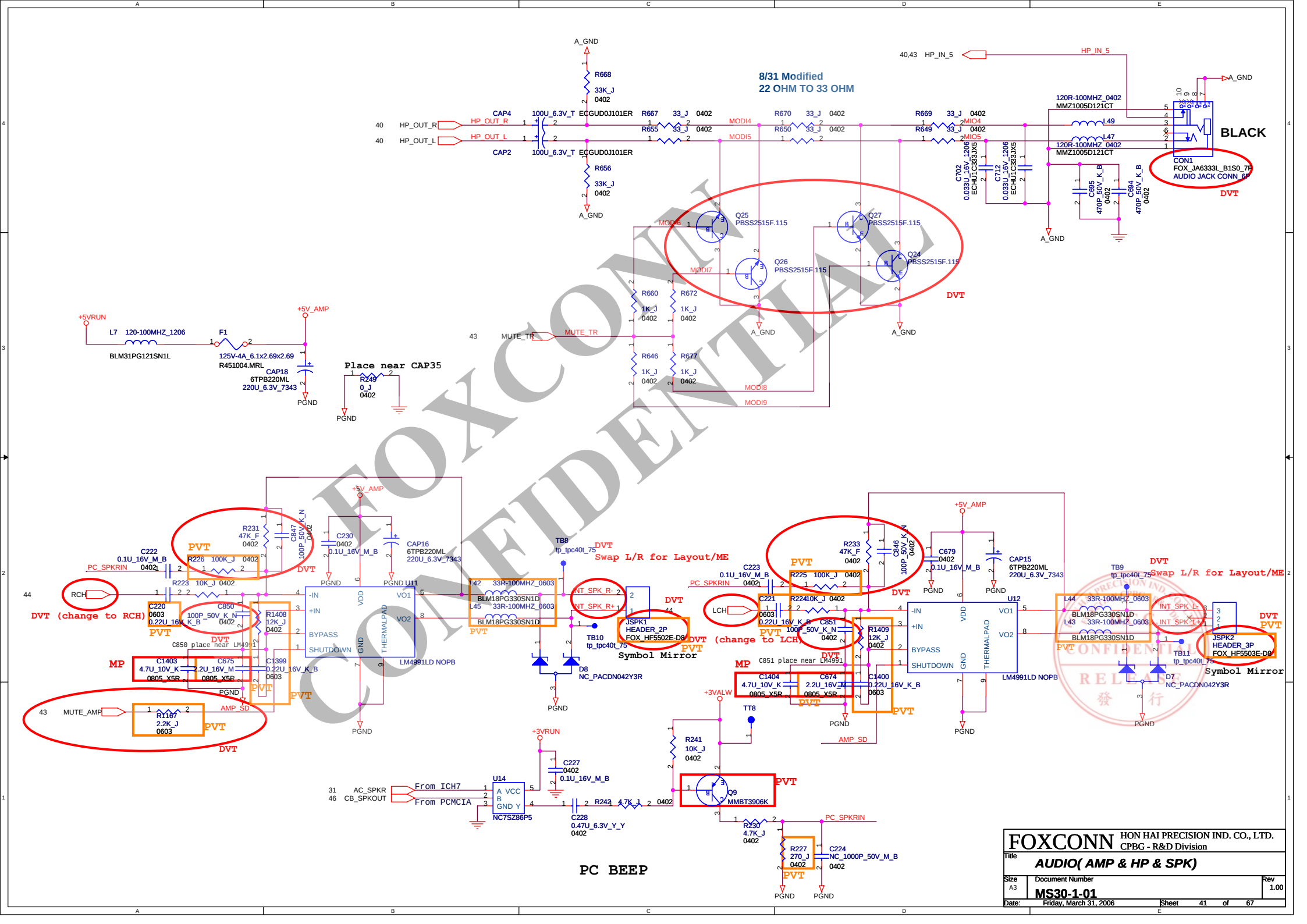


| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | FAN/HW THERMAL PROTECT | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 38 of 67 | |






| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. |
| | CPBG - R&D Division |
| Title | AUDIO(CODEC & POWER) |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 40 of 67 |


8/31 Modified
22 OHM TO 33 OHM
BLACK
Place near CAP35
PC BEEP
DVT (change to RCH)
DVT (change to LCH)
Swap L/R for Layout/ME
Symbol Mirror
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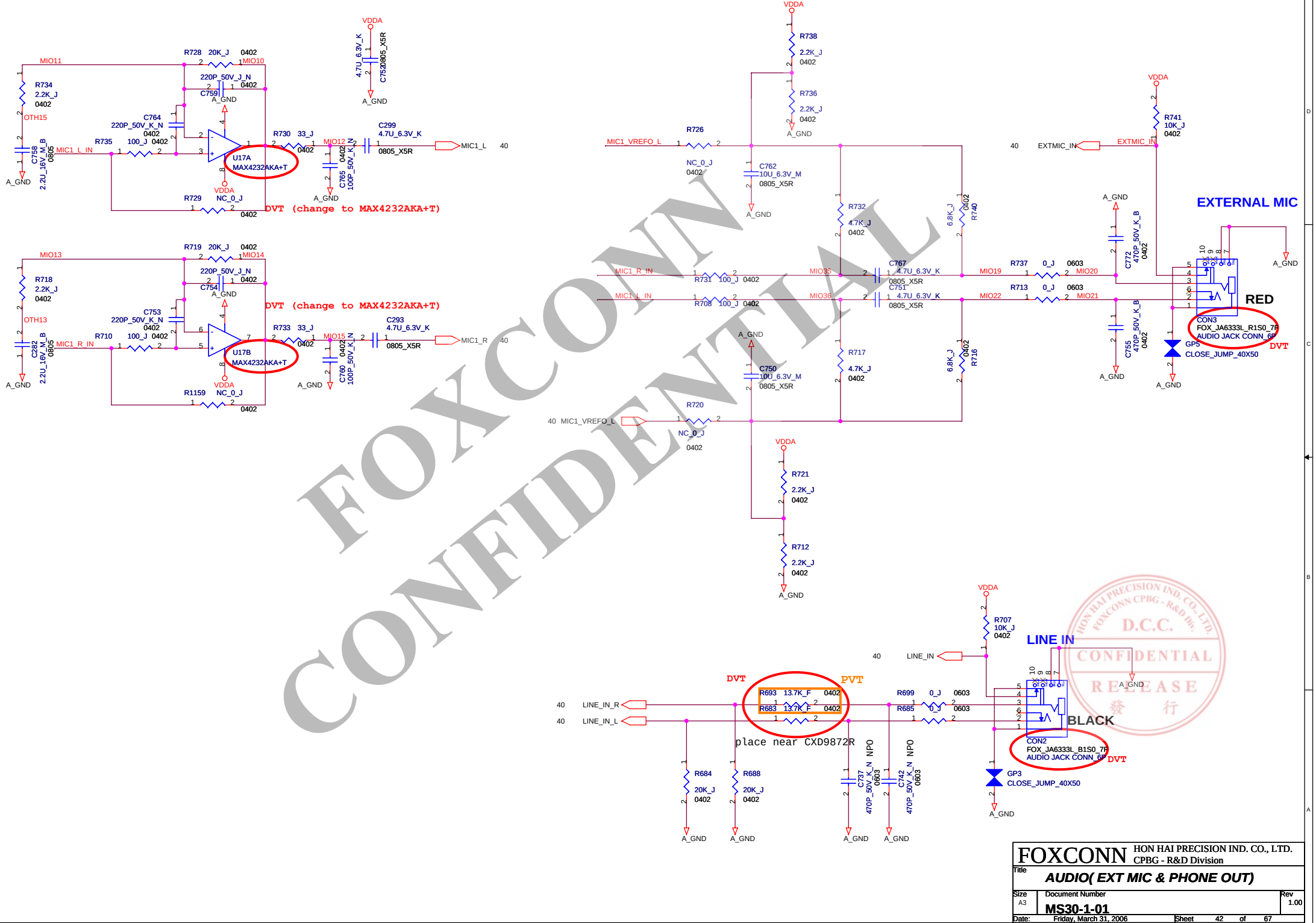
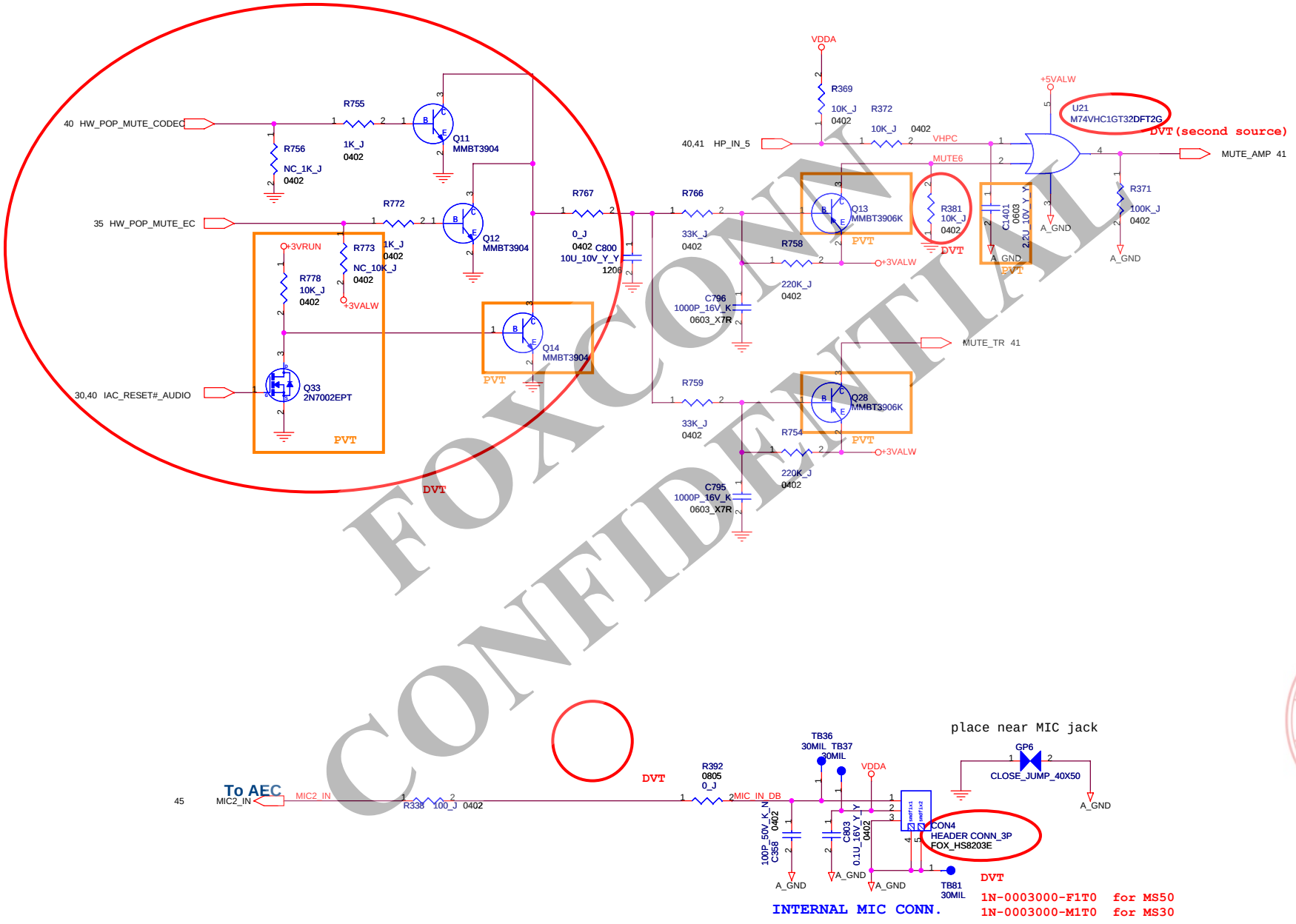
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
AUDIO( AMP & HP & SPK)
Size A3
Document Number MS30-1-01
Rev 1.00
Date: Friday, March 31, 2006
Sheet 41 of 67







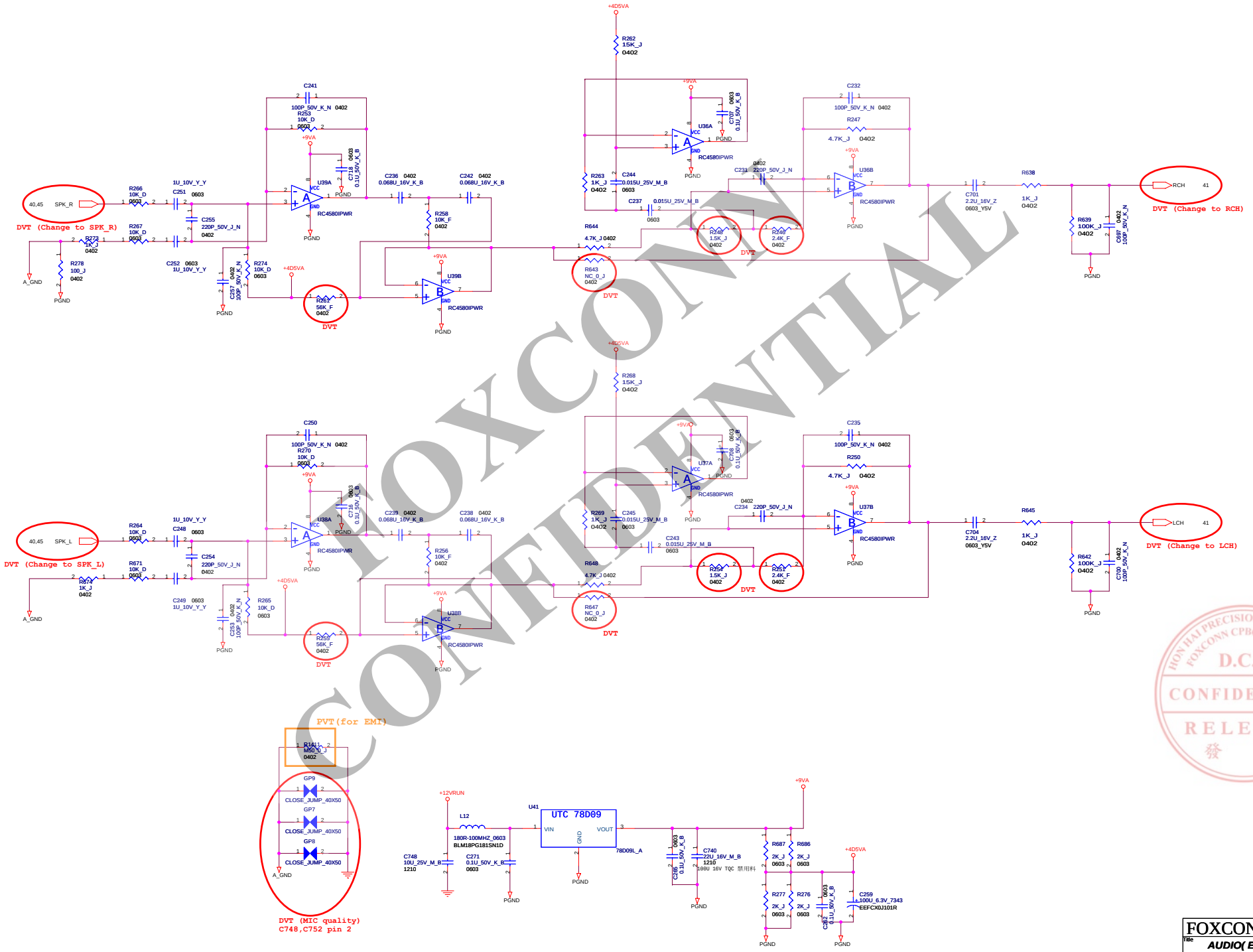

| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division |
| Title | AUDIO( EXT MIC & PHONE OUT) |
| Size | A3 |
| Document Number | MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 42 of 67 |







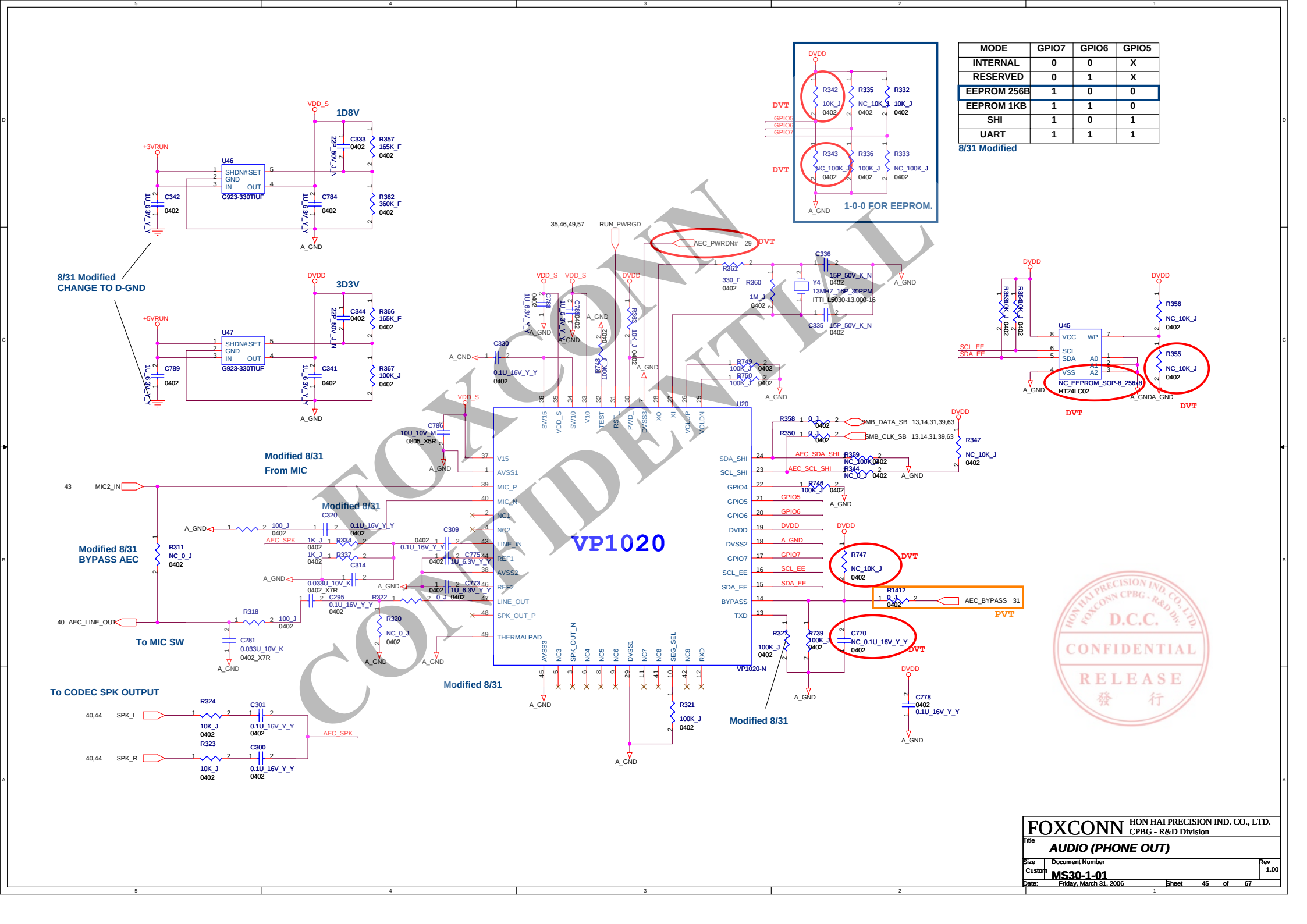

| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | AUDIO (MUTE & INTMIC) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 43 of 67 | |








| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | AUDIO( EQ ) | |
| Size A2 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 44 of 67 | |




| MODE | GPIO7 | GPIO6 | GPIO5 |
|---|---|---|---|
| INTERNAL | 0 | 0 | X |
| RESERVED | 0 | 1 | X |
| EEPROM 256B | 1 | 0 | 0 |
| EEPROM 1KB | 1 | 1 | 0 |
| SHI | 1 | 0 | 1 |
| UART | 1 | 1 | 1 |

8/31 Modified

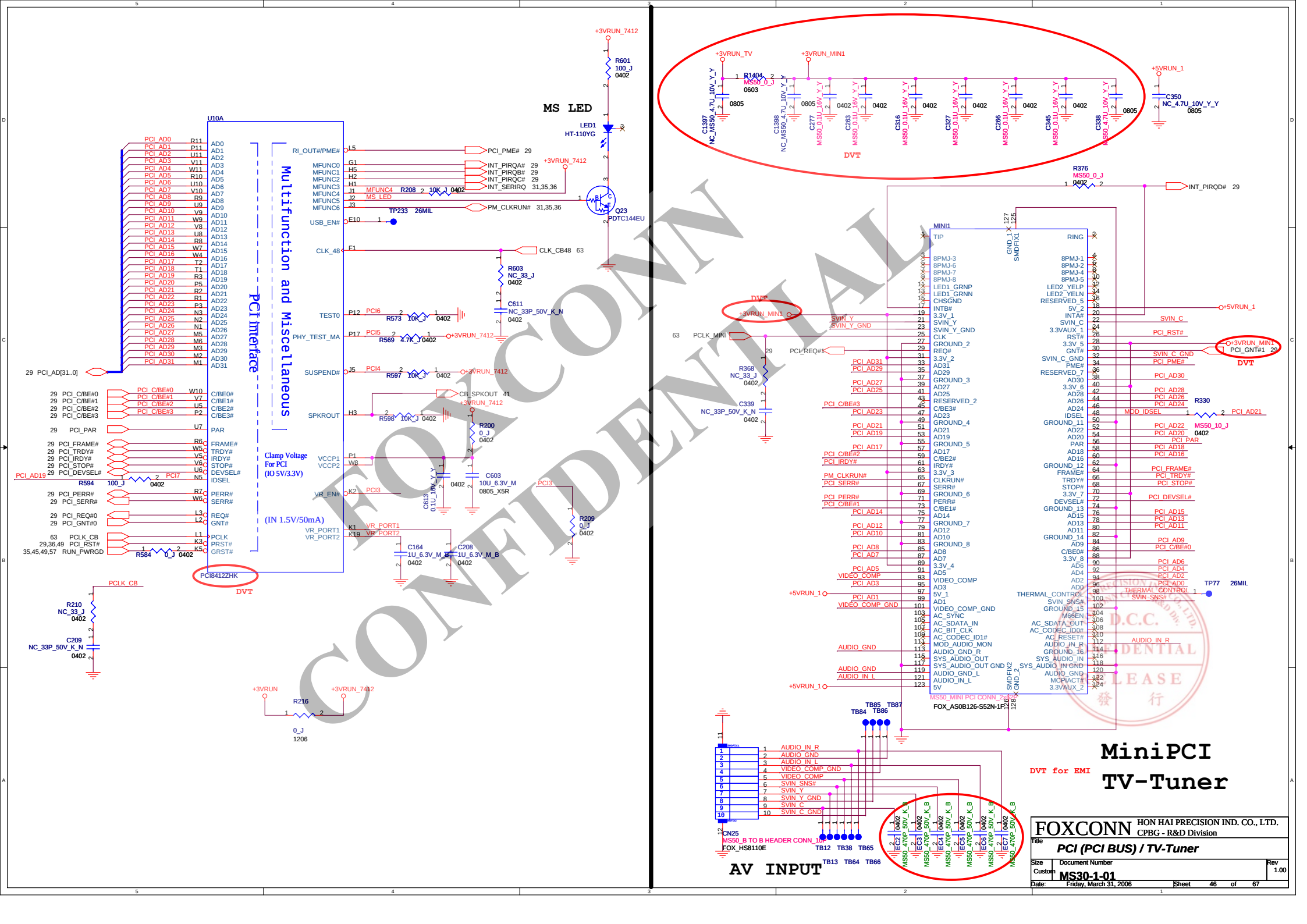


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **AUDIO (PHONE OUT)**

| Size | Document Number | Rev |
|---|---|---|
| Custom | MS30-1-01 | 1.00 |

Date: Friday, March 31, 2006 Sheet 45 of 67


MS LED
LED1
HT-110YG
Q23
PDTC144EU
U10A
PCI interface
Multifunction and Miscellaneous
PCI8412ZHK
DVT
Clamp Voltage
For PCI
(IO 5V/3.3V)
(IN 1.5V/50mA)
MINI1
MS50_MINI PCI CONN_2
FOX_AS0B126-S52N-1F
CN25
MS50_B TO B HEADER CONN_10P
FOX_HS8110E
AV INPUT
DVT for EMI
MiniPCI
TV-Tuner
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
PCI (PCI BUS) / TV-Tuner
MS30-1-01
Friday, March 31, 2006
Sheet 46 of 67
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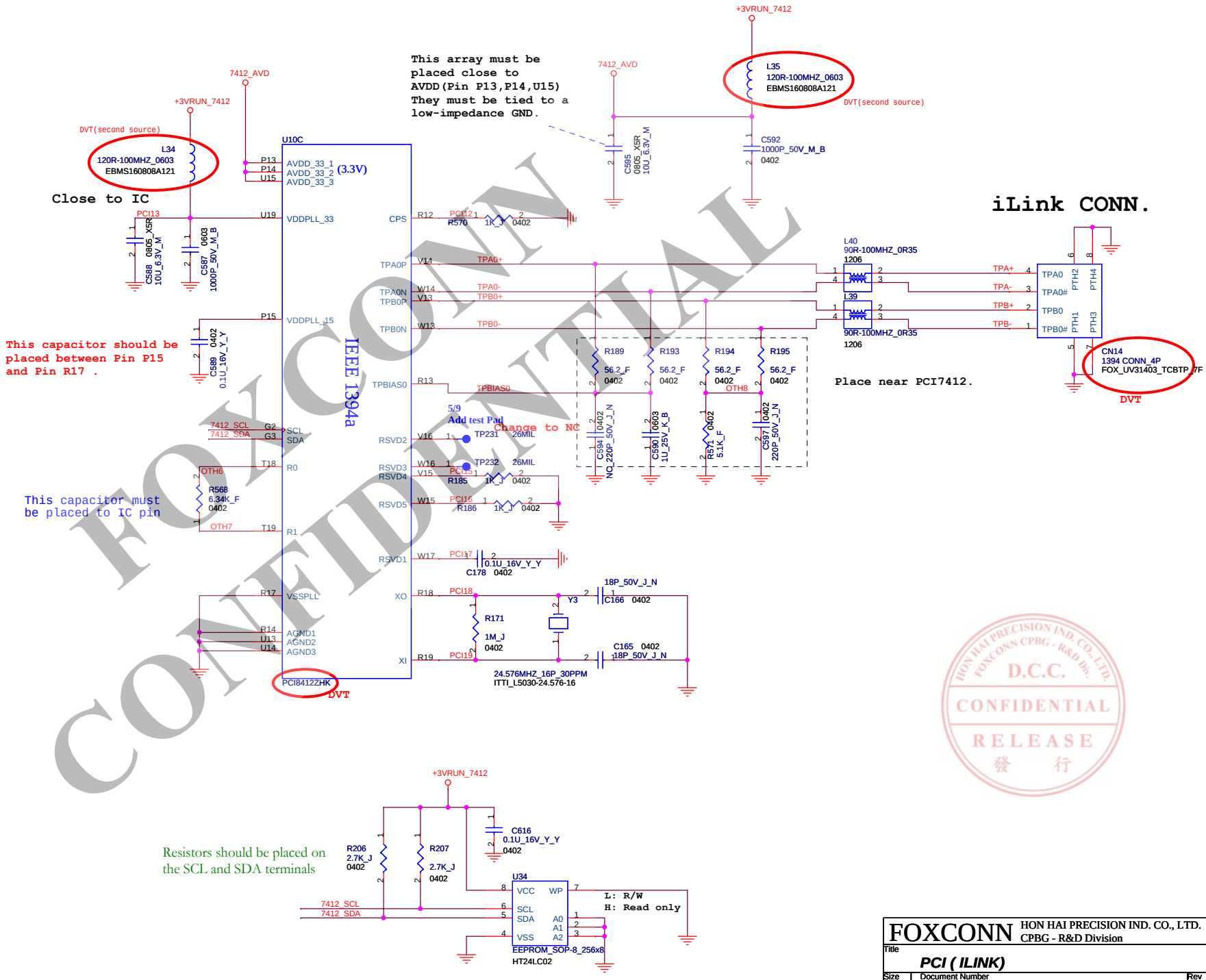
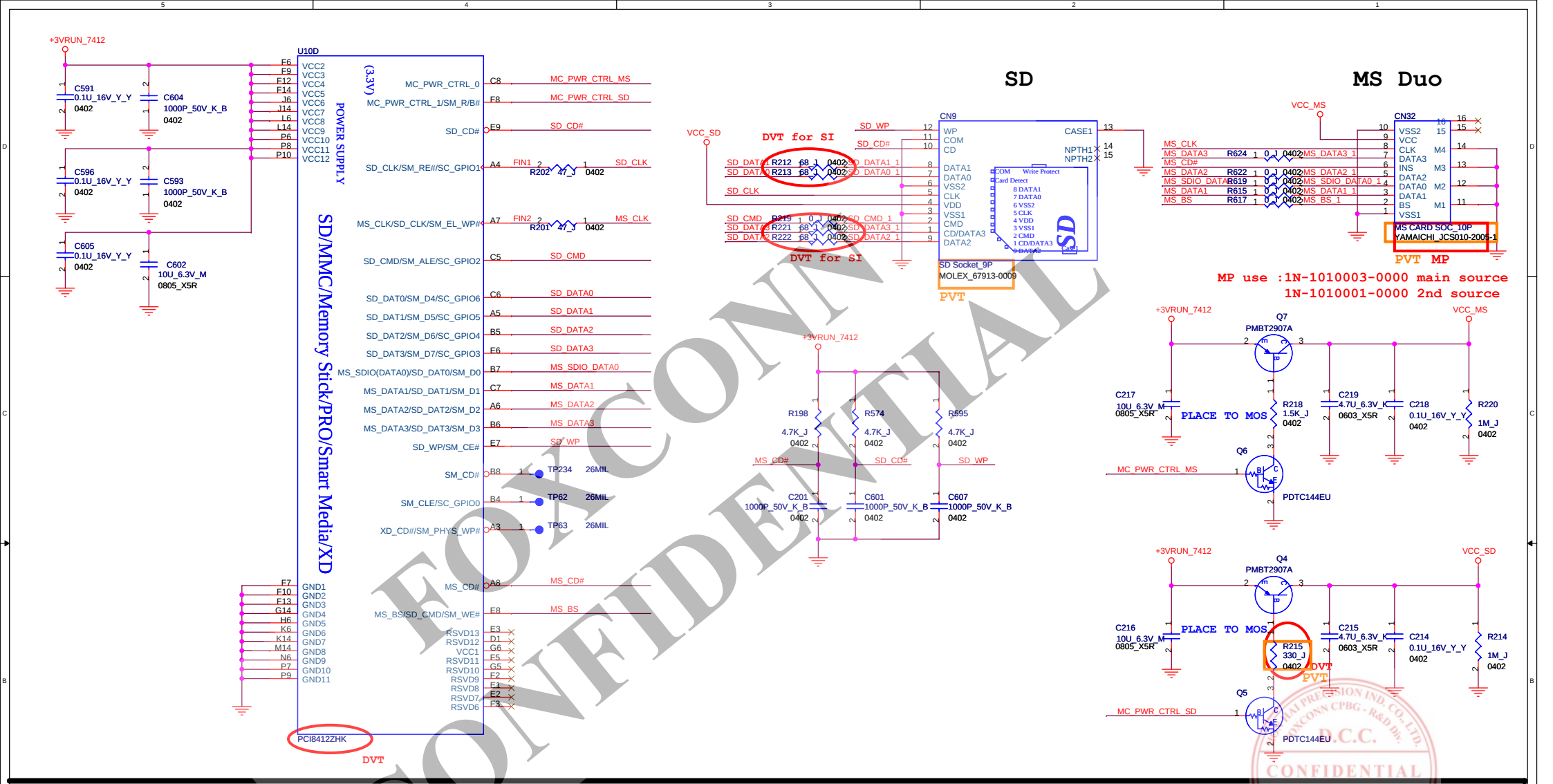
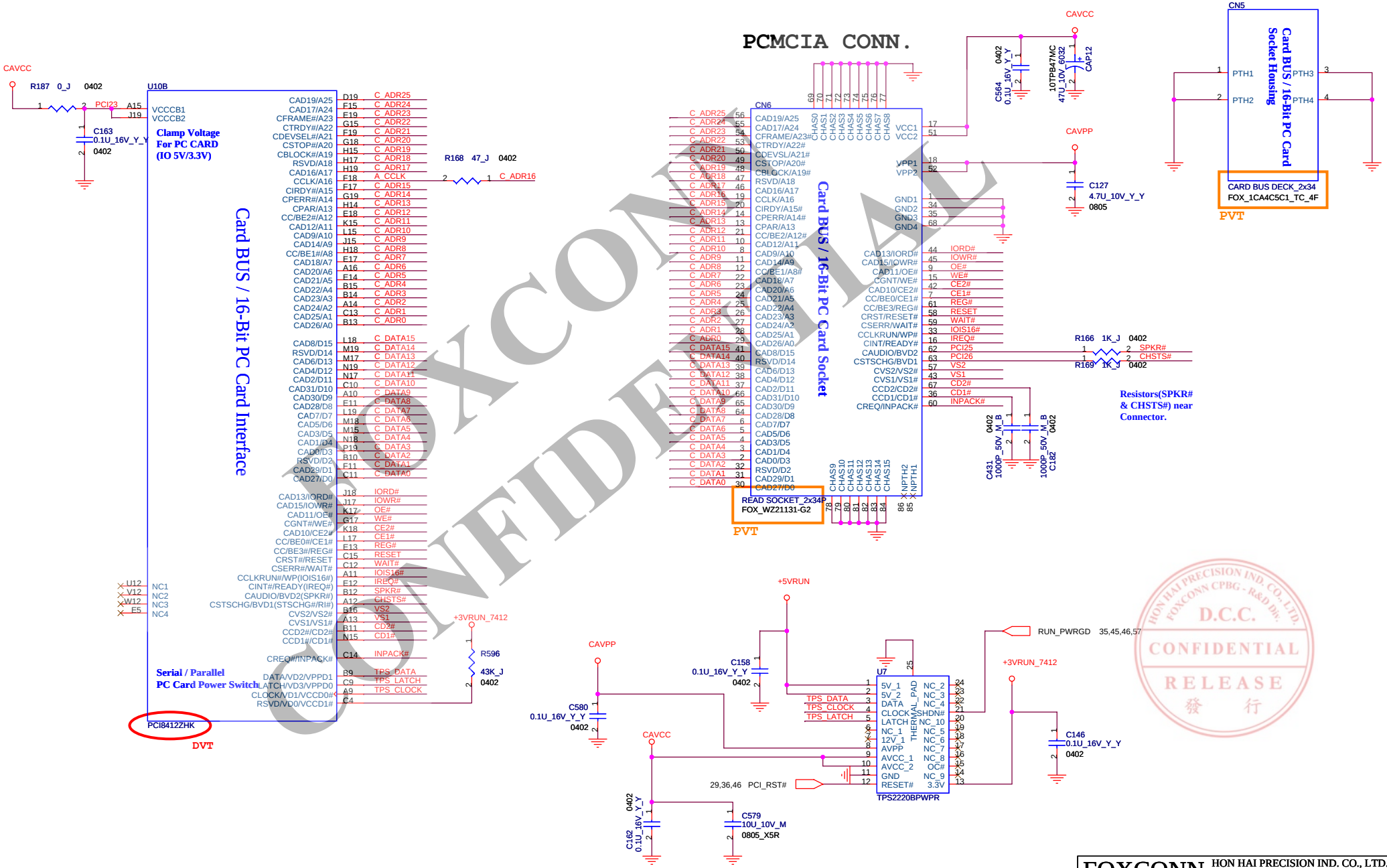





| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | PCI ( ILINK) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 47 of 67 | |







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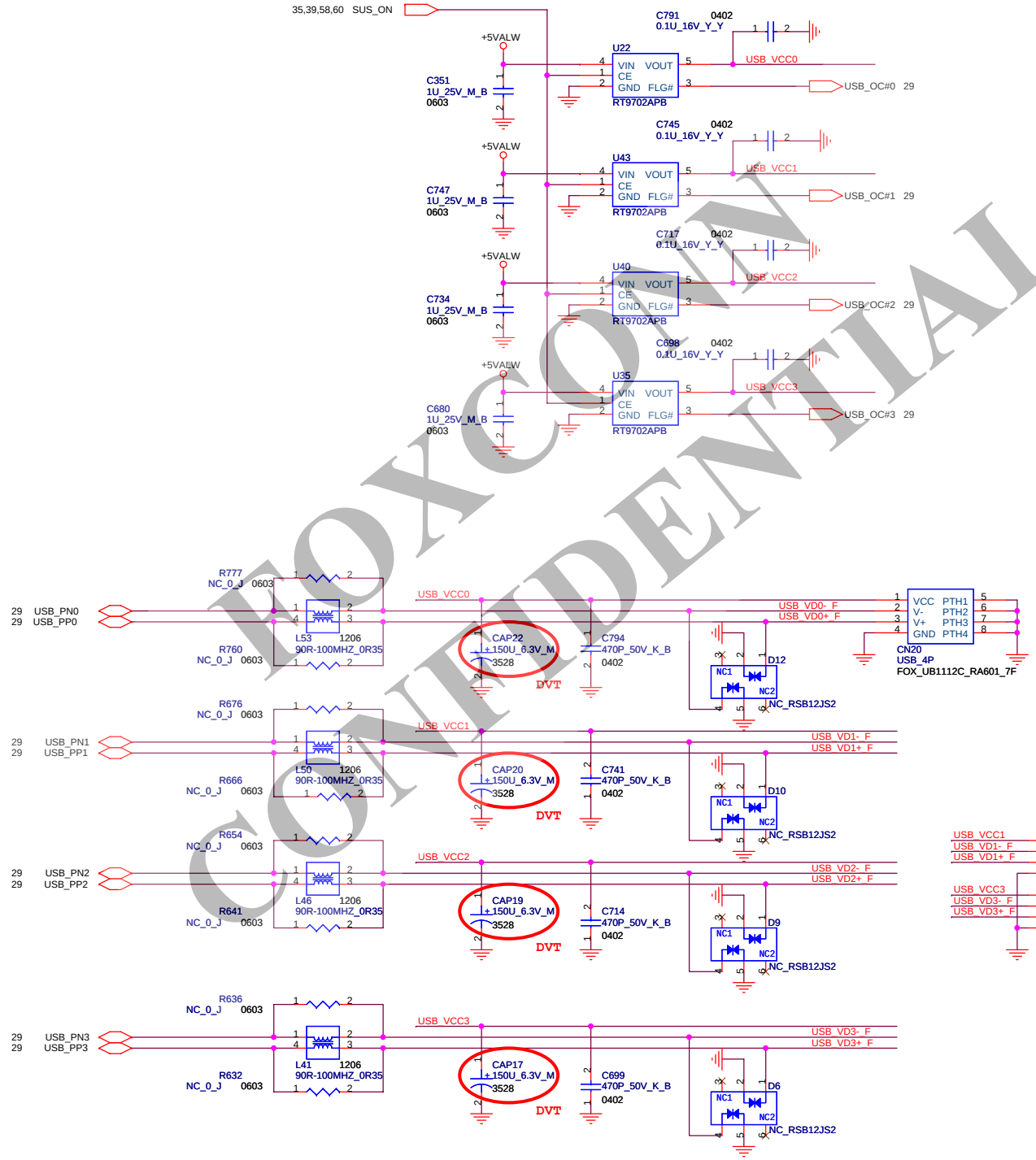
Title: PCI ( PCMCIA)

Size: A3 | Document Number: MS30-1-01 | Rev: 1.00

Date: Monday, April 03, 2006 | Sheet 49 of 67

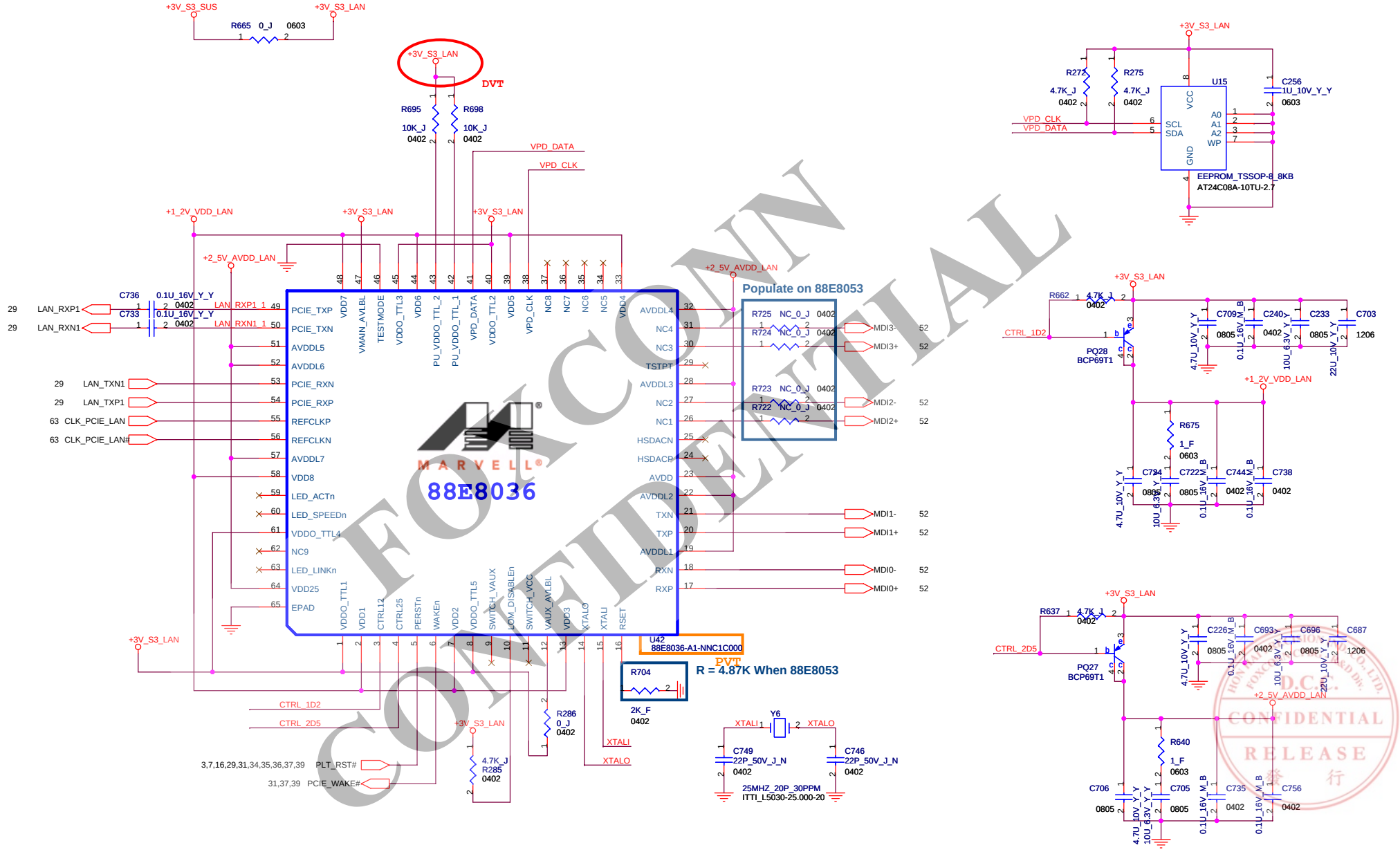



Use Power Switch

USB CONN X 4

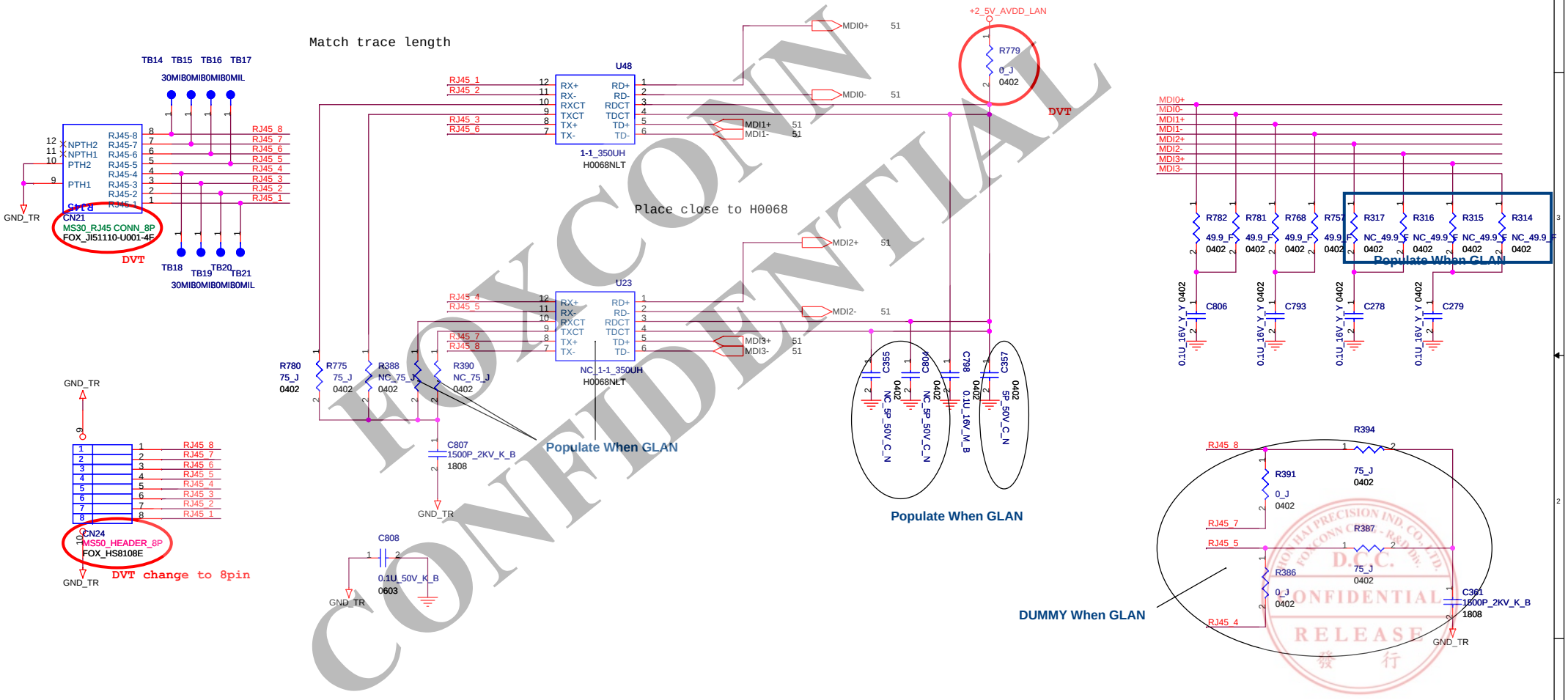


| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | USB2.0/DOCKING CONN. | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 50 of 67 | |



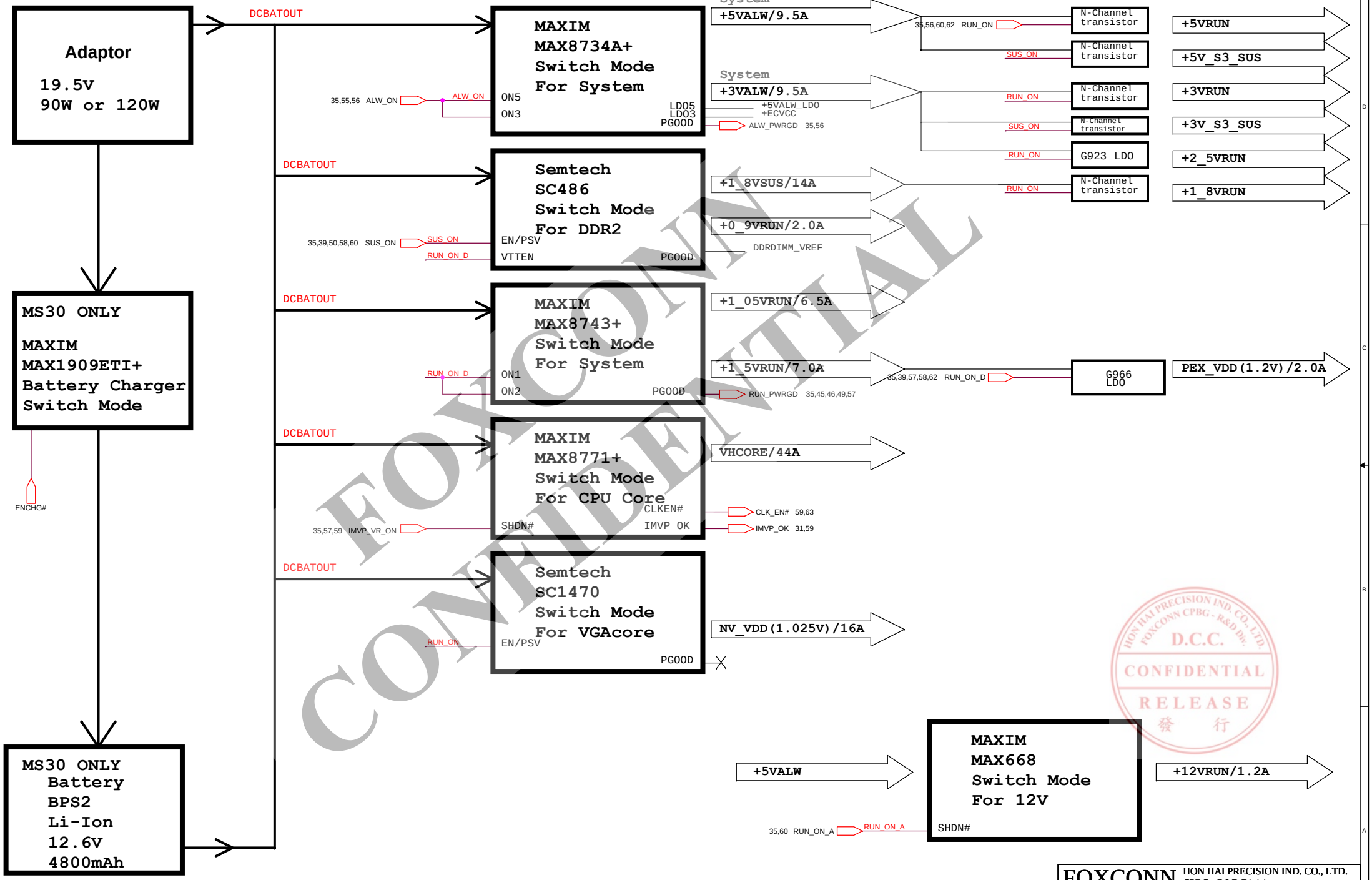



| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | Marvell_LAN (1/2) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 51 of 67 | |





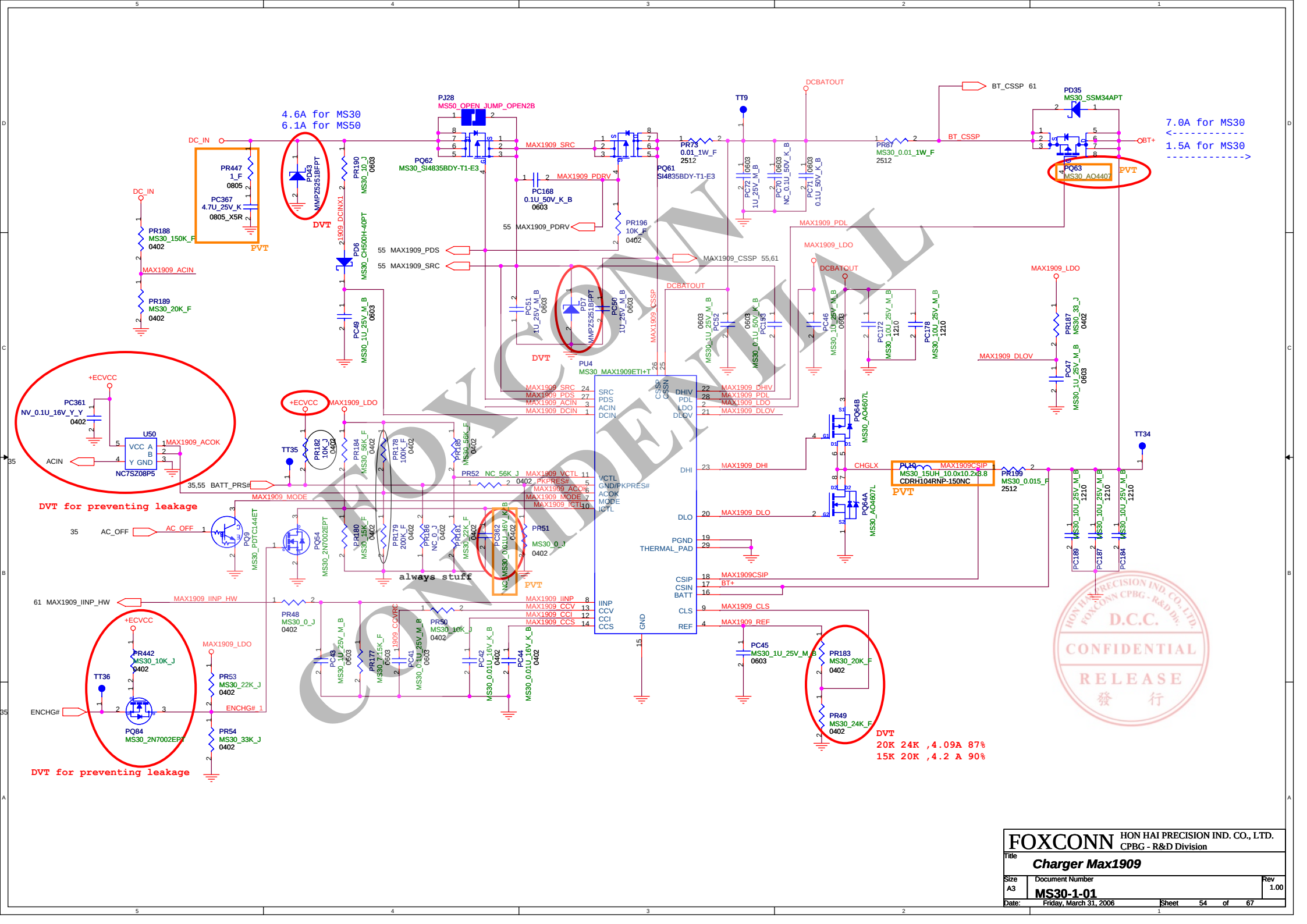

| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | Marvell_LAN (2/2) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 52 of 67 | |

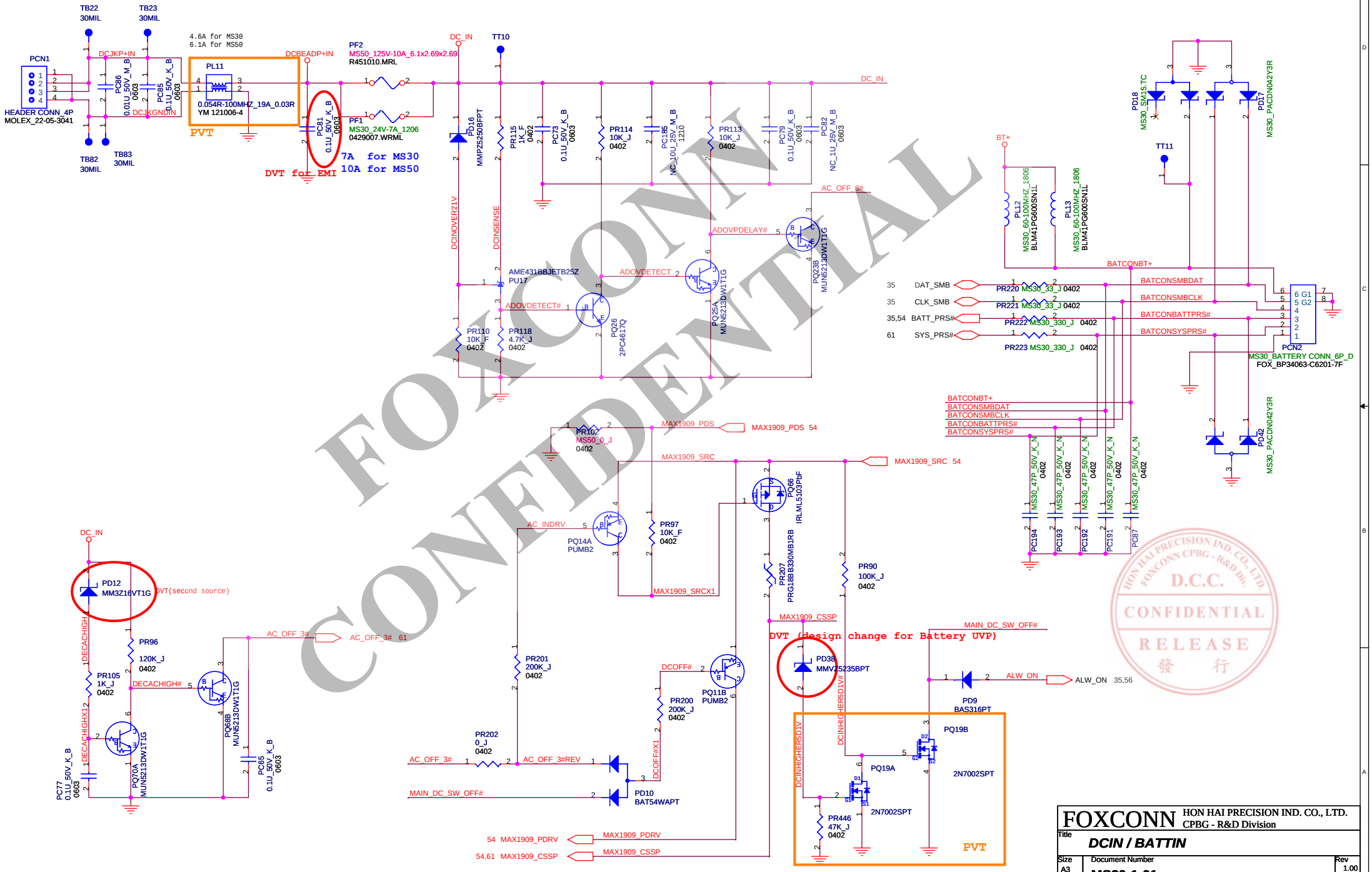







| | |
|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division |
| Title | Power Design Diagram-ZG |
| Size A3 | Document Number MS30-1-01 |
| Rev | 1.00 |
| Date: | Friday, March 31, 2006 |
| Sheet | 53 of 67 |

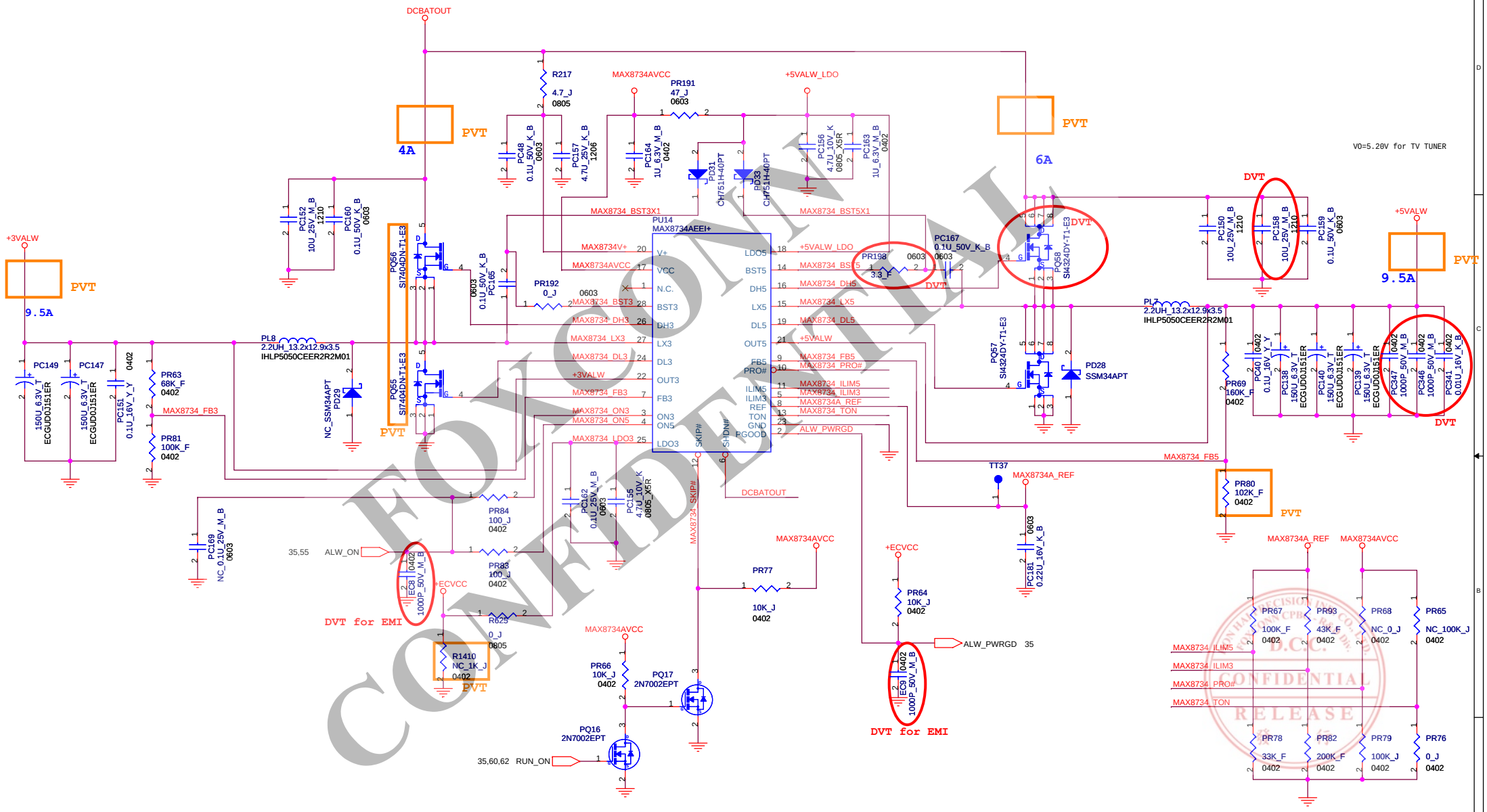


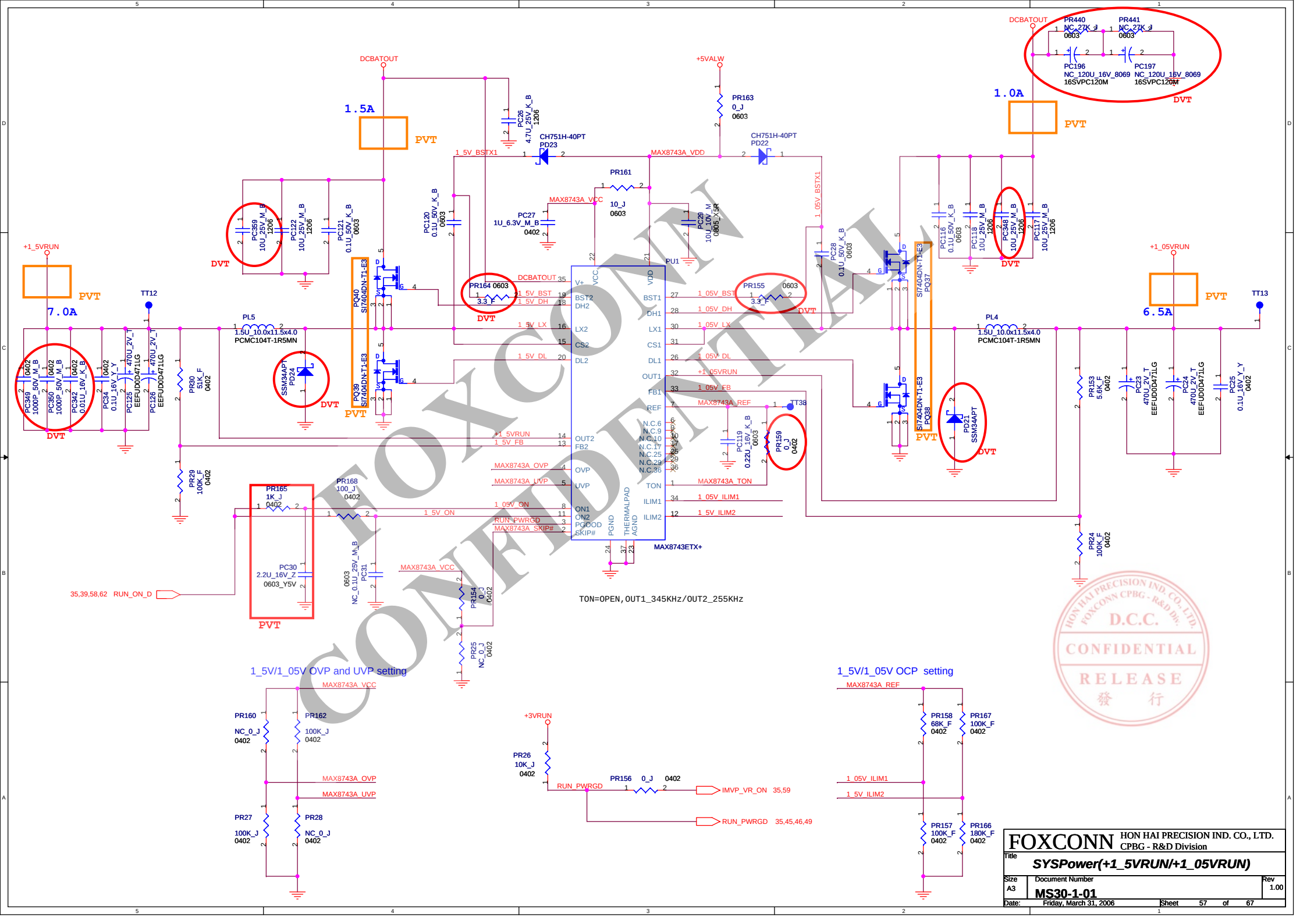







| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | DCIN / BATTIN | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 55 of 67 | |




DCBATOUT
+5VALW
+1_5VRUN
+1_05VRUN
1.5A
1.0A
7.0A
6.5A
PVT
DVT
MAX8743ETX+
TON=OPEN,OUT1_345KHz/OUT2_255KHz
1_5V/1_05V OVP and UVP setting
1_5V/1_05V OCP setting
35,39,58,62 RUN_ON_D
IMVP_VR_ON 35,59
RUN_PWRGD 35,45,46,49
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
SYSPower(+1_5VRUN/+1_05VRUN)
MS30-1-01
Friday, March 31, 2006
Sheet 57 of 67
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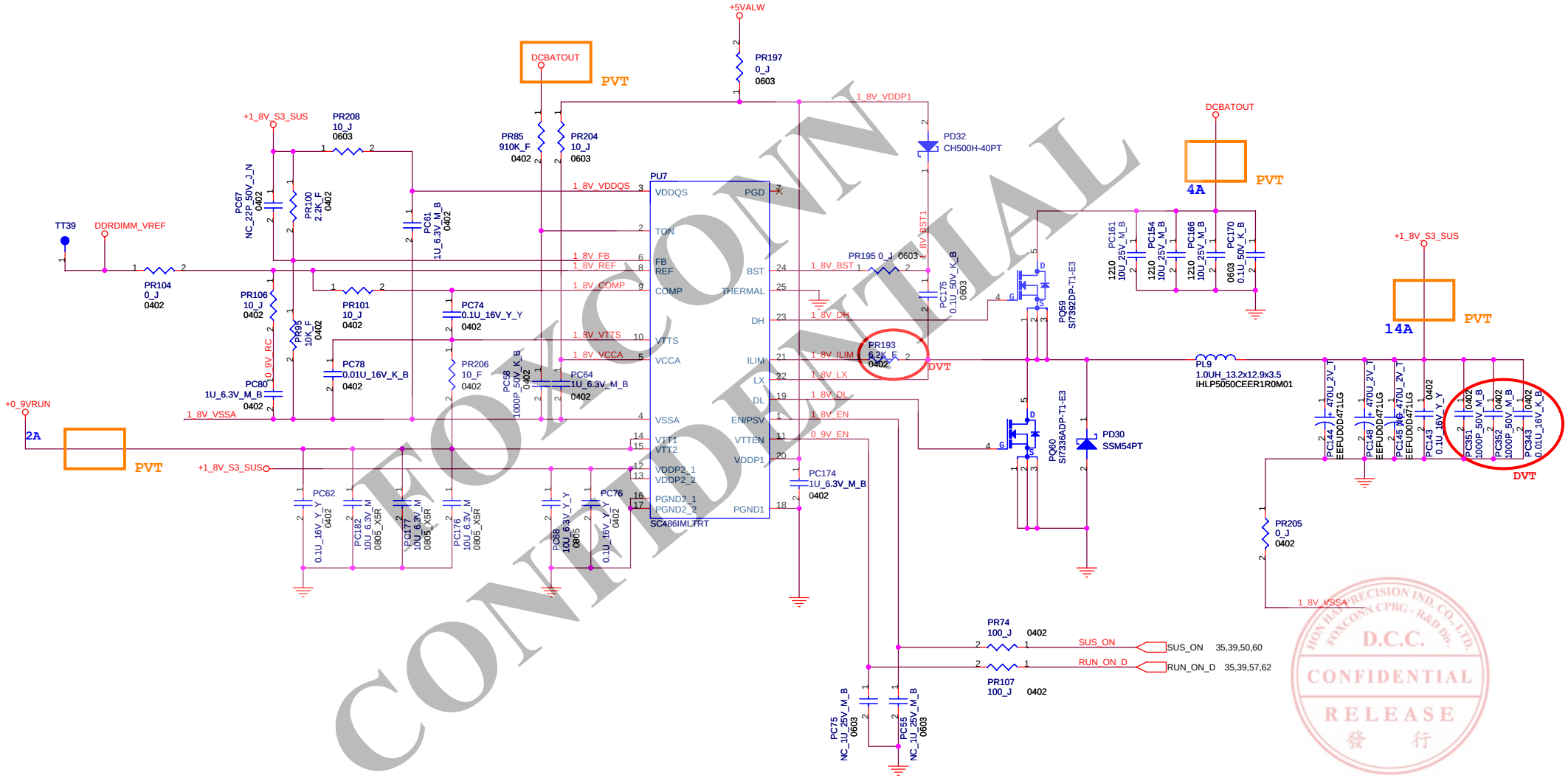
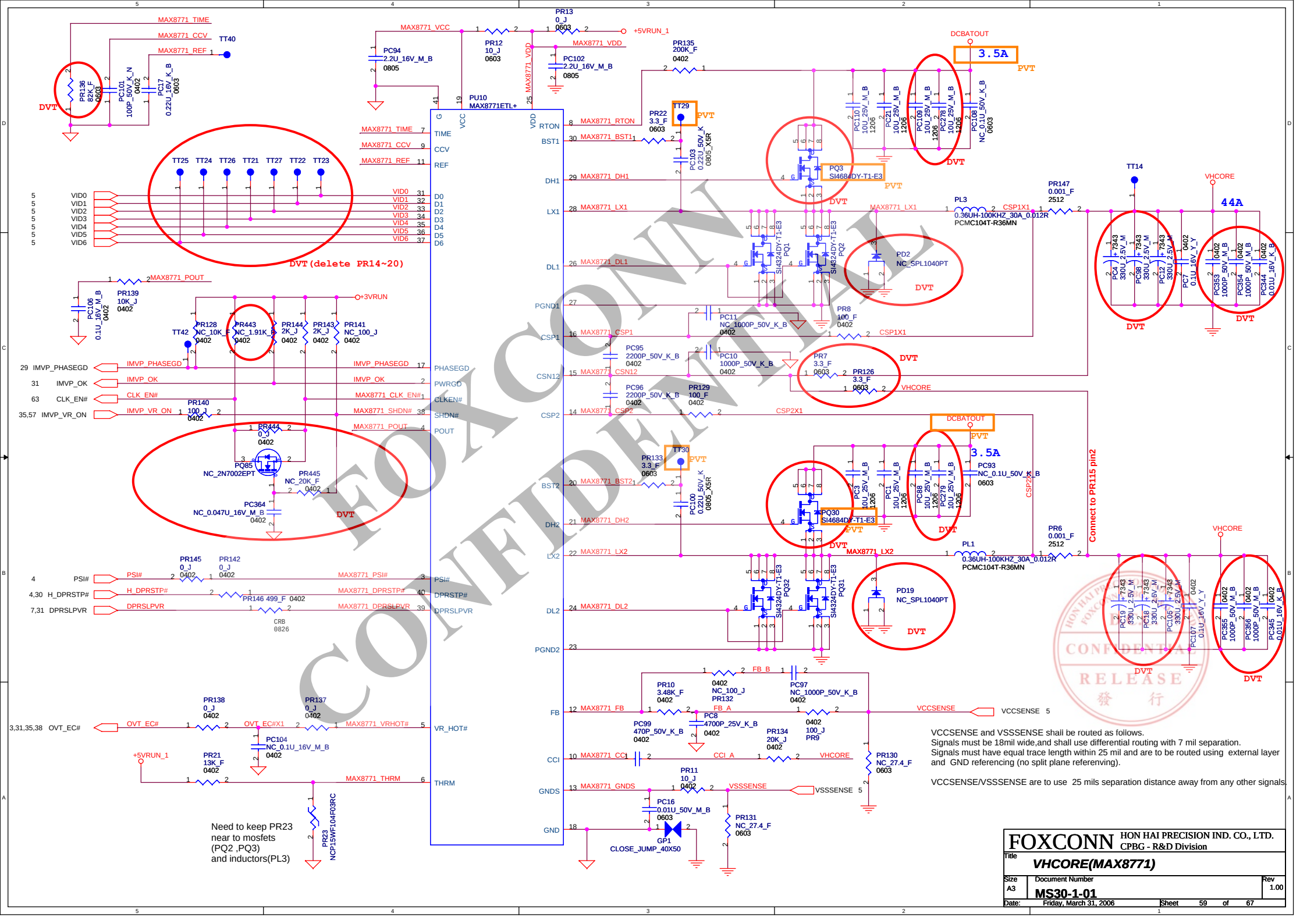
D.C.C.
CONFIDENTIAL
RELEASE

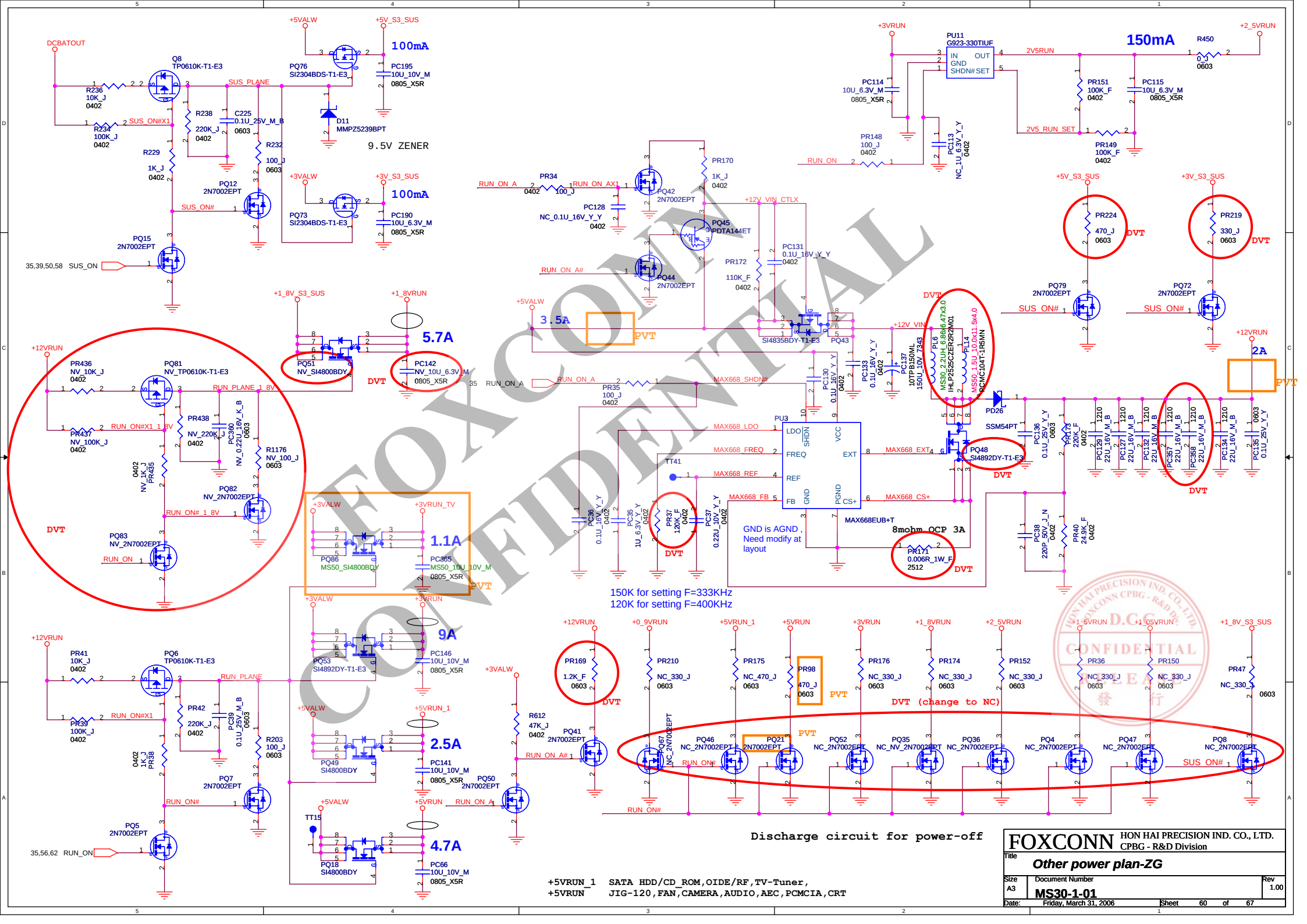


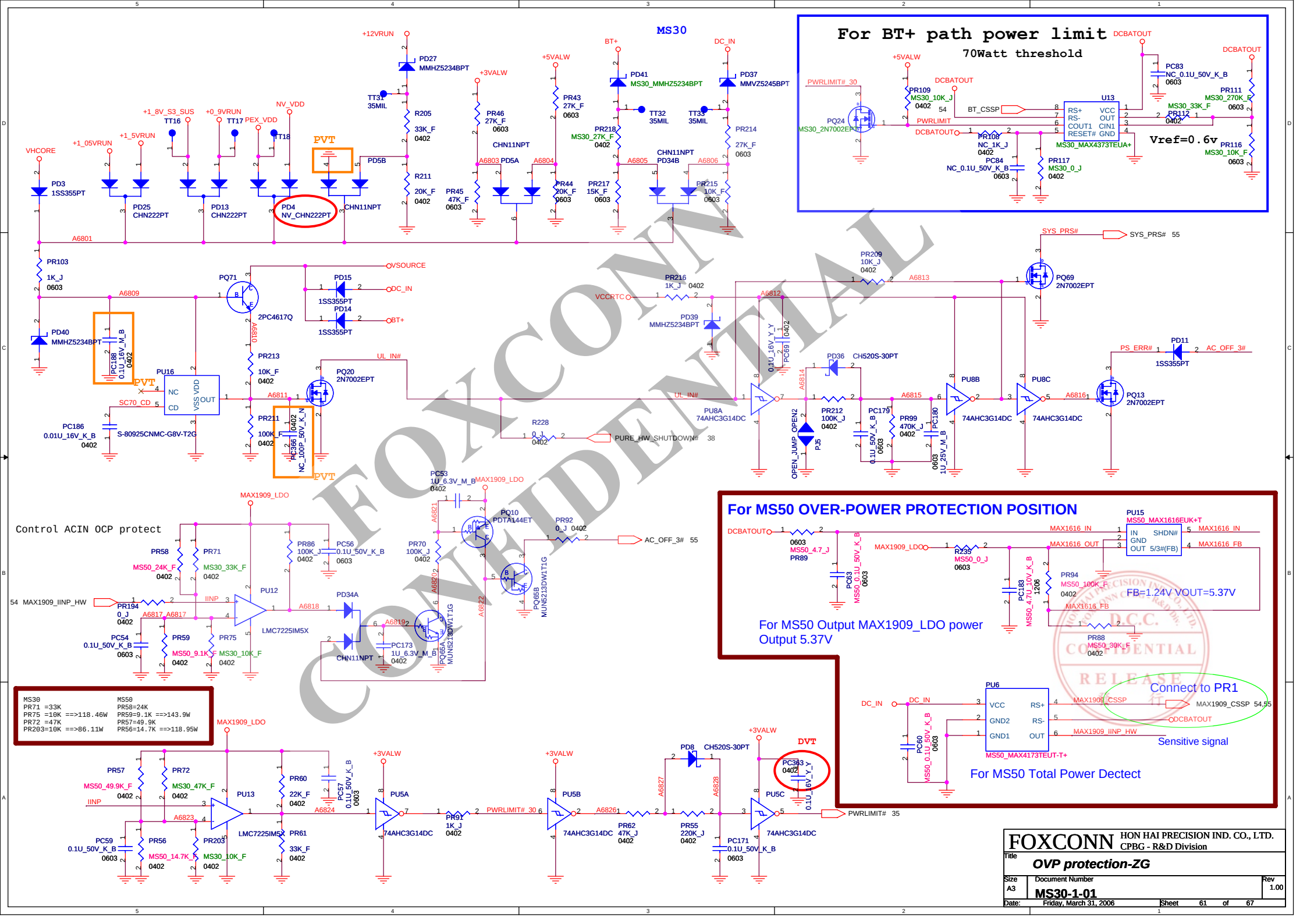





| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | DDR2Power(+1_8V_S3_SUS/+0_9VRUN) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 58 of 67 | |






MS30
For BT+ path power limit
70Watt threshold
Vref=0.6v
For MS50 OVER-POWER PROTECTION POSITION
For MS50 Output MAX1909_LDO power Output 5.37V
FB=1.24V VOUT=5.37V
Connect to PR1
Sensitive signal
For MS50 Total Power Dectect
Control ACIN OCP protect
MS30
PR71 =33K
PR75 =10K ==>118.46W
PR72 =47K
PR203=10K ==>86.11W
MS50
PR58=24K
PR59=9.1K ==>143.9W
PR57=49.9K
PR56=14.7K ==>118.95W
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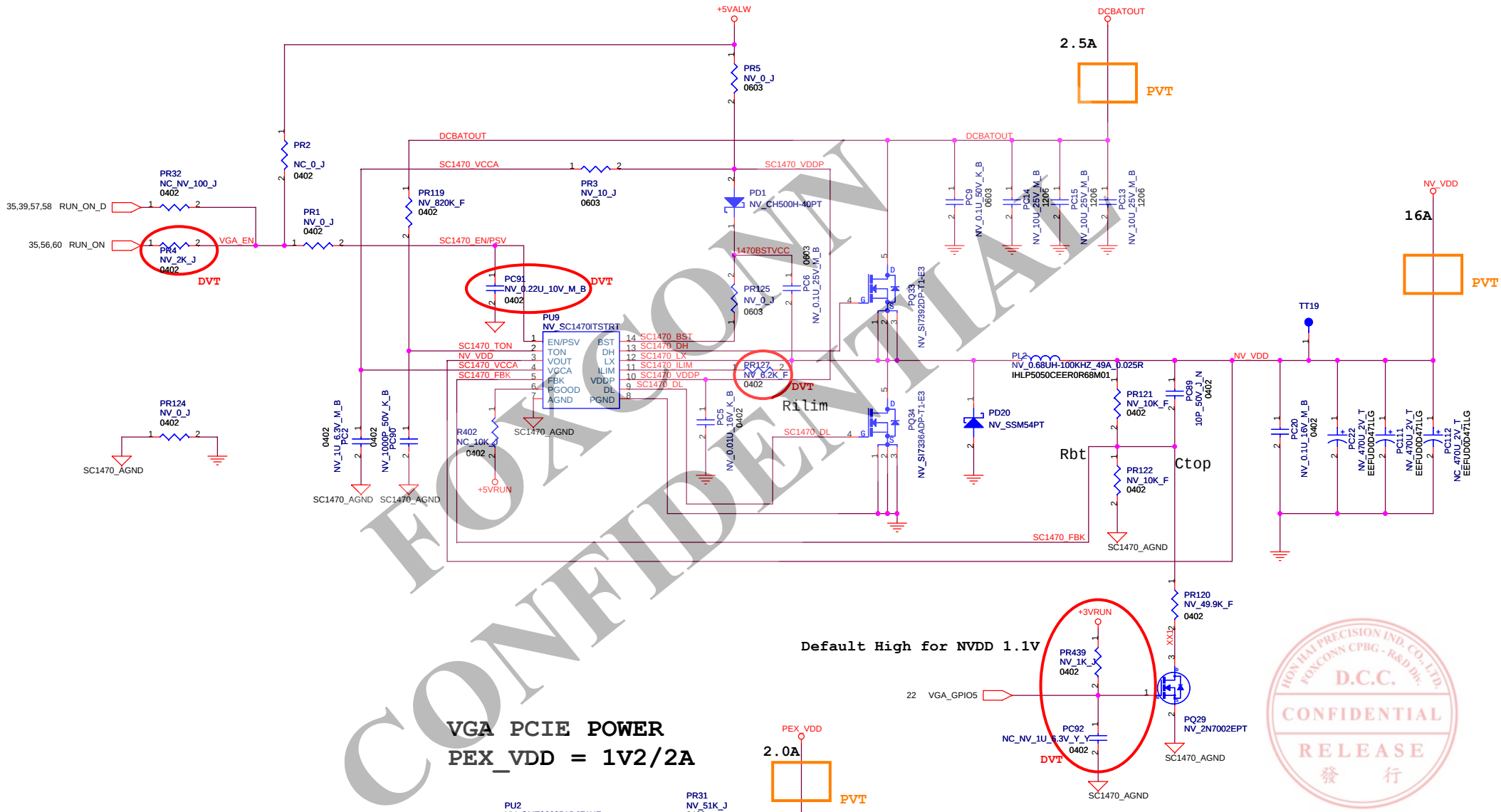
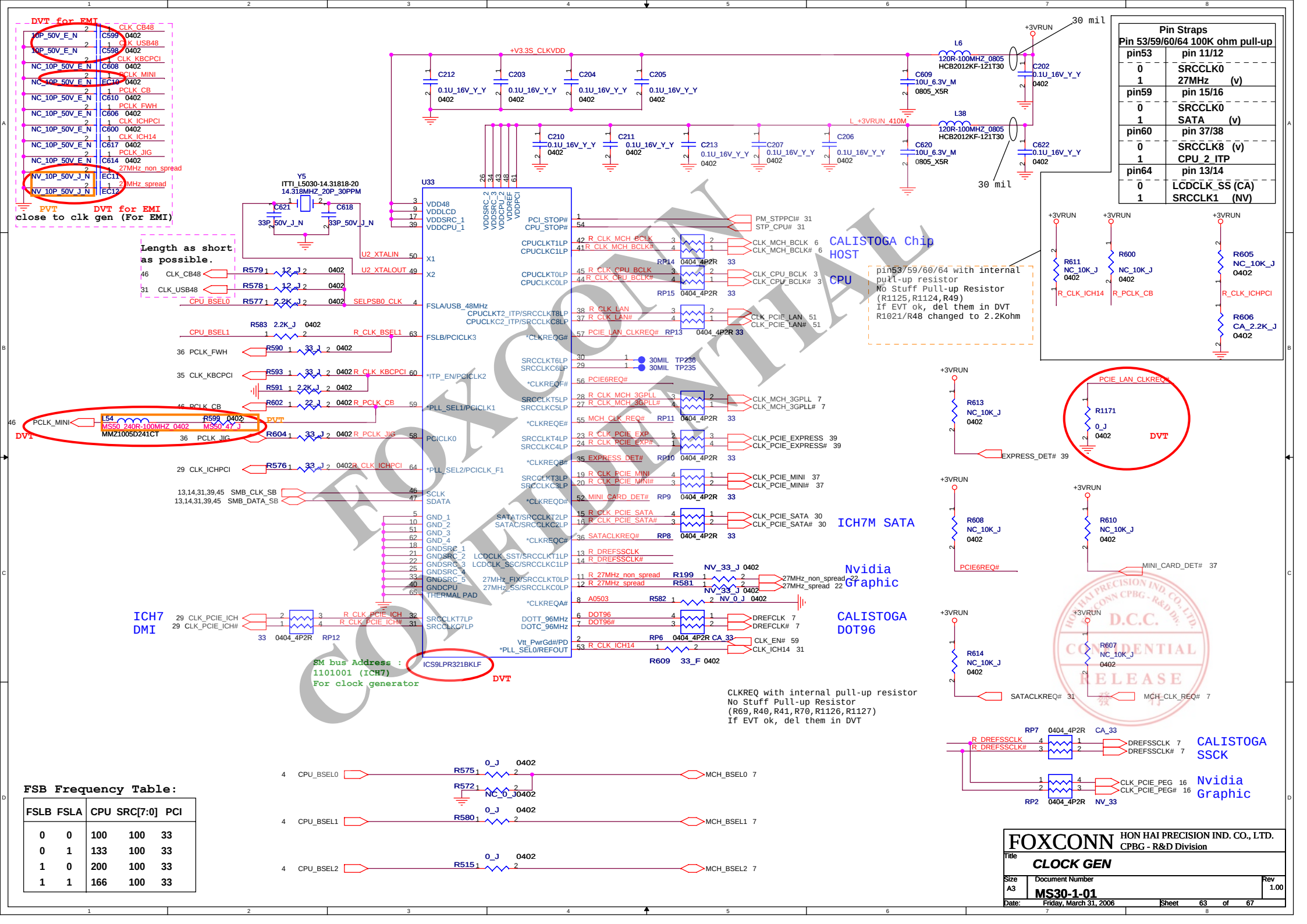
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
OVP protection-ZG
MS30-1-01
Friday, March 31, 2006




| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title | VGA POWER(VGACORE&IO) | |
| Size A3 | Document Number MS30-1-01 | Rev 1.00 |
| Date: Friday, March 31, 2006 | Sheet 62 of 67 | |




**FSB Frequency Table:**

| FSLB | FSLA | CPU | SRC[7:0] | PCI |
|---|---|---|---|---|
| 0 | 0 | 100 | 100 | 33 |
| 0 | 1 | 133 | 100 | 33 |
| 1 | 0 | 200 | 100 | 33 |
| 1 | 1 | 166 | 100 | 33 |



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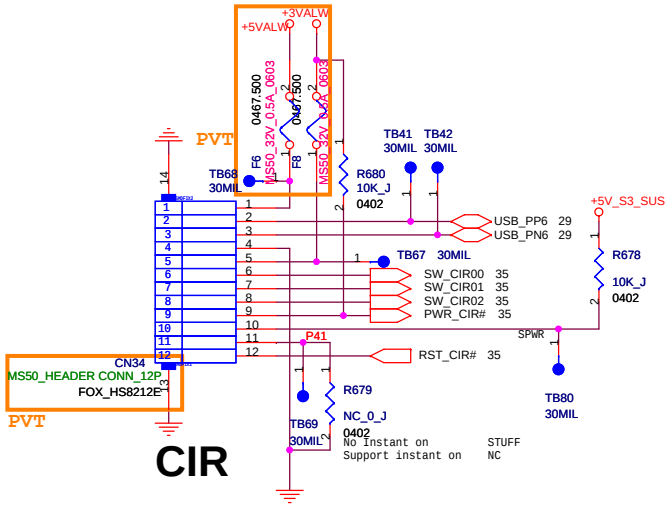
CPBG - R&D Division

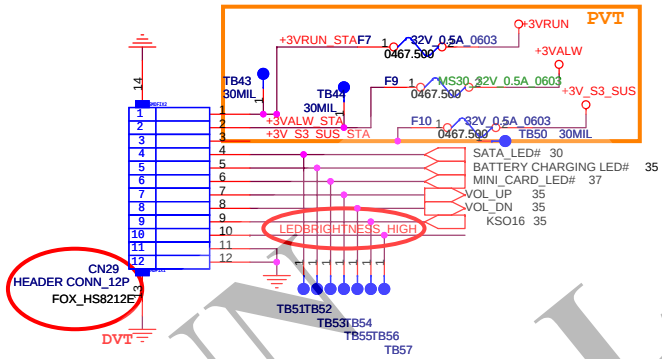
Title: CLOCK GEN

Size: A3 | Document Number: MS30-1-01 | Rev: 1.00

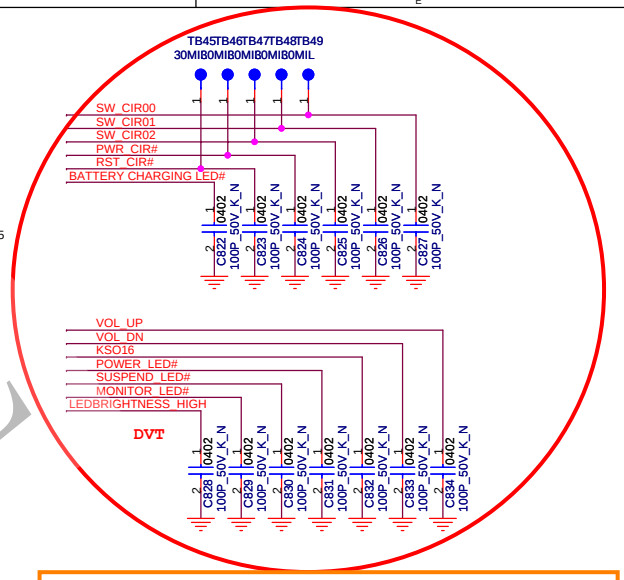
Date: Friday, March 31, 2006 | Sheet 63 of 67

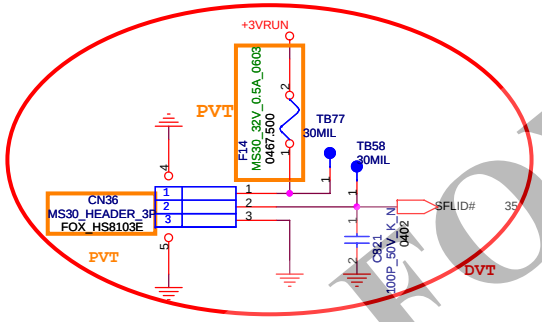



# CIR

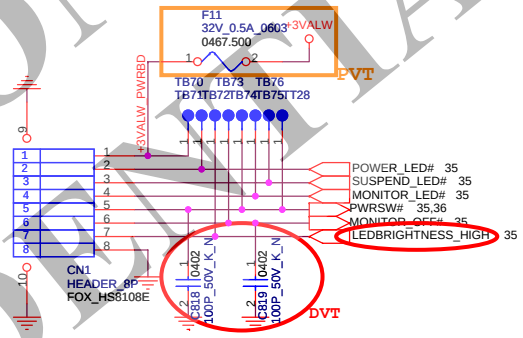



# STATUS LED CONN

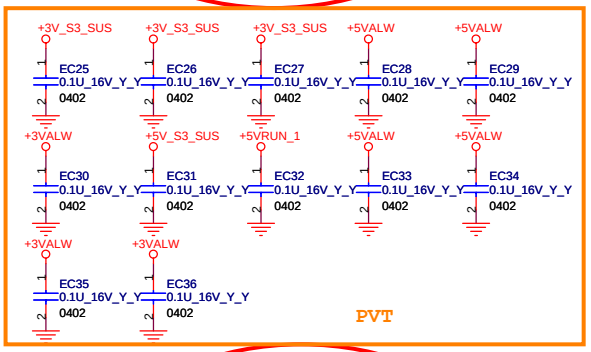


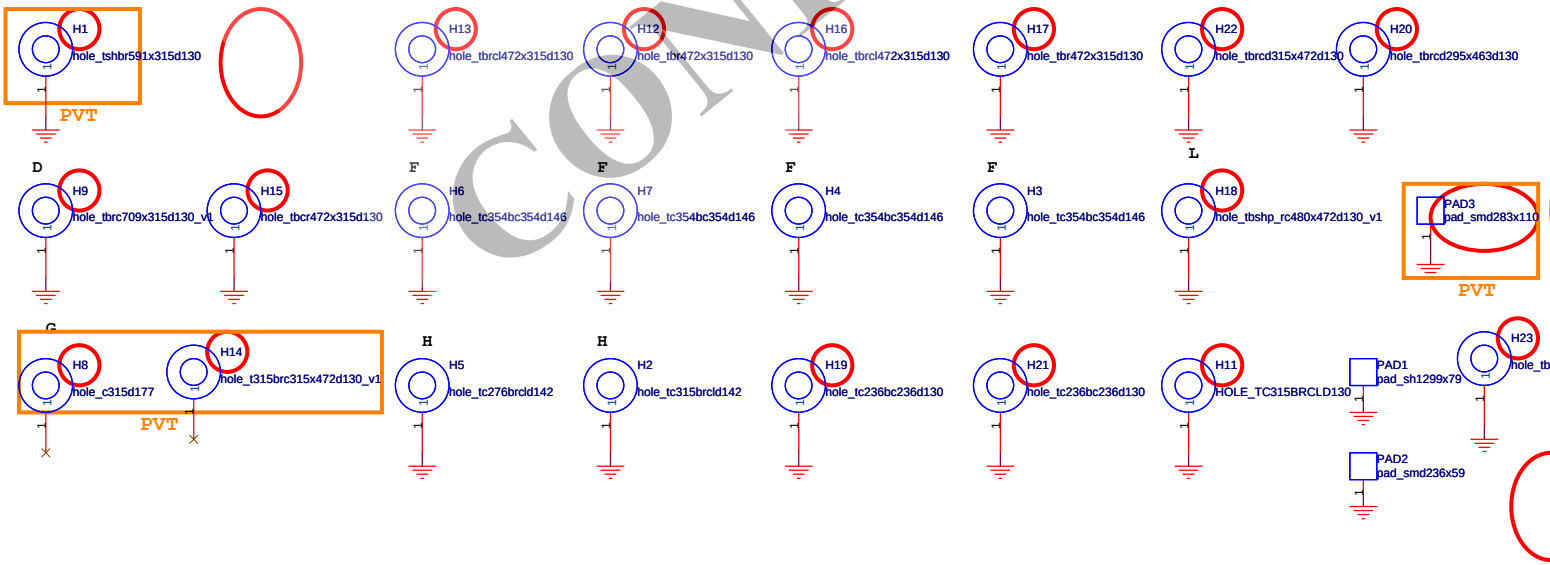



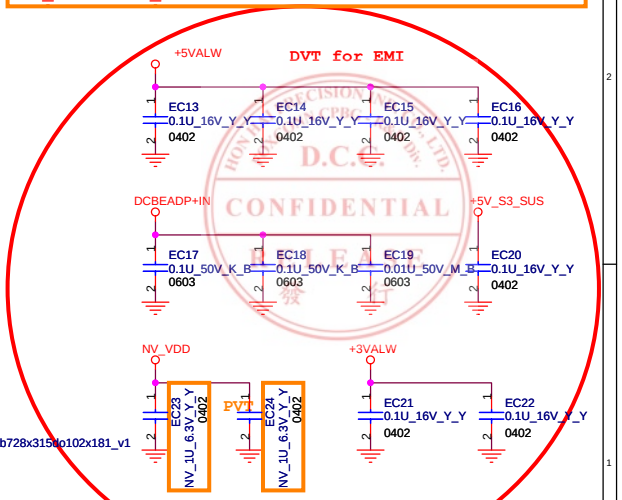

# Cover SW CONN




# Power LED/Power BTN



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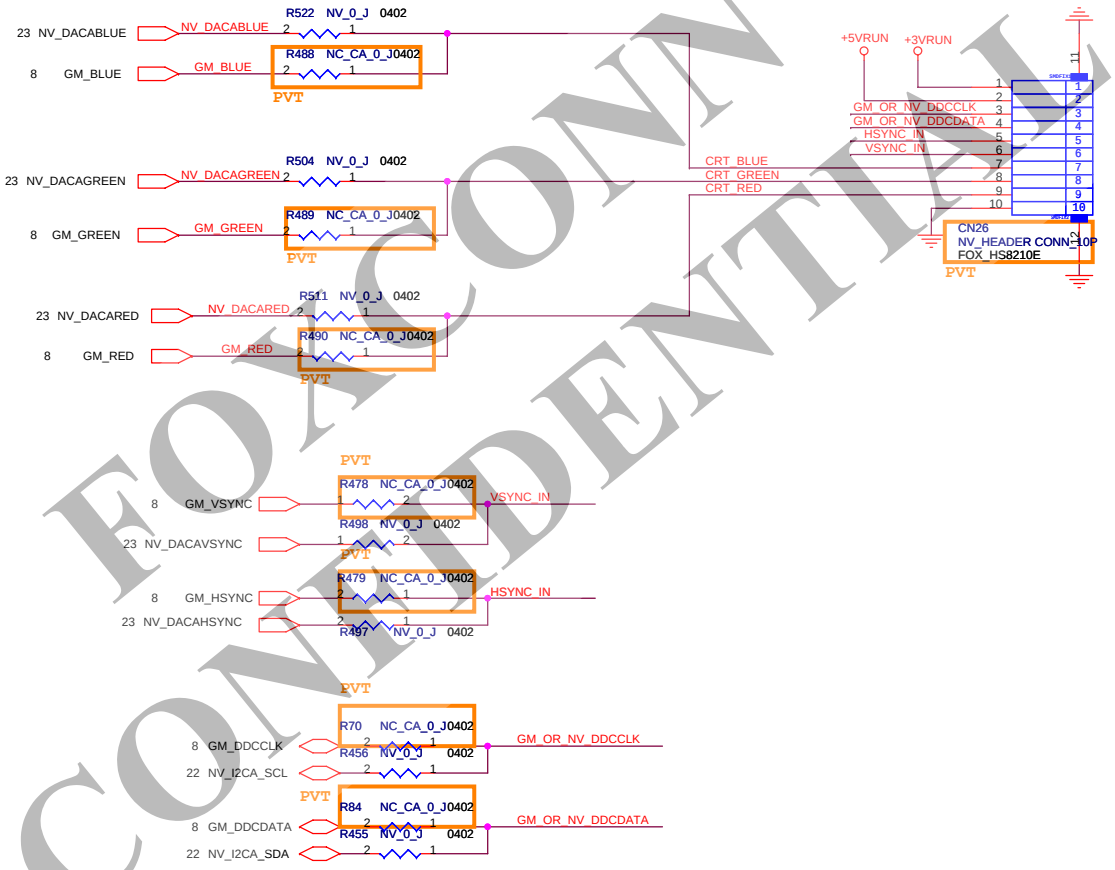
Title: **HOLE**

| Size | Document Number | Rev |
|---|---|---|
| A3 | MS30-1-01 | 1.00 |

Date: Friday, March 31, 2006 Sheet 64 of 67








| | | |
|---|---|---|
| FOXCONN | HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division | |
| Title: CRT | | |
| Size: A3 | Document Number: MS30-1-01 | Rev: 1.00 |
| Date: Friday, March 31, 2006 | Sheet 65 of 67 | |

# History

## REV 0.20 (2005/09/02)

P37 (1)move Q1,R32,LED4 to Page PCI (PCI BUS) / TV-Tuner
(2)move CN62 to Page EC+KBC
(3)move U35,C807,R753 to Page Flash ROM/XBUS
(4)remove R23,LED16,R24,LED17,R25,LED18,R30,LED7,R31,LED8
(5)delete Page37 for page saving
P44 add AUDIO (EQ)page as P44
9/2
P24,25 Change U11,U12,U13,U14
from K4J5532QG-BC20 to K4J52324QC-BC20
P35 Add R1785 for EC IMVP_VR_ON path
P36 Change CN15 pin 1,21 power rail from +ECVCC to +3VALW
P39 Change R1093 pin1 from RUN_ON to RUN_ON_D
P44 Add R1783,R1784 for reserve AEC SMBus(pin23,24) to SB SMBus
P51 Add R1788,R1789 for CTRL_1D2,CTRL_2D5 pull up +3V_S3_LAN

9/2 power schematic
P55 Add PF1 for MS30/MS50 different adapter power Input
P56 (1)Delete PC364,PC365 for noise issue
(2)JP29 change to resistor R1790 for space saving
(3)Add PR1791,PR1792 for boost drive issue,EMI improve
P57 (1)PR331=0 ohm ,PR370=NC for skip mode disable
(2)Add PR1794,PR1793 for boost driver issue ,EMI improve
P58 (1)PR93 change from 0402 to 0603 parts.Power issue
(2)delete PR97,PR98
P59 (1)PC118 change to 110pf,maxim suggest
(2)Delete PR111,PC117,PR342,PC321
(3)change PR130 to 100 ohm,PC125 to 10nF for maxim suggest
P60 (1)MAX668_SHDN# connect to PR103 pin 1 for delay adjustable
(2)Add PQ135,PQ134,PR1795,PR1796,PC396,PR1796 for leakage issue

9/3
P48 Add R1787 100k Ohm Pull-Low on trace SDATA_IN1
P46 Connect singal SVIN_SNS# SB GPIO21,MINI1 pin100
P60 Add +3V_S3_SUS and +5V_S3_SUS power rail for
wired lan , wireless lan , KBC I/F(MS-30)
P51 Change LAN chip(U129) power orignal:+3VALW new:+3V_S3_SUS,
orignal:+3VALW_LAN new:+3V_S3_LAN
P35 Connect RP99 pin1,2 to +5V_S3_SUS
P37 (1)Change R760 pin1 power rail as +3VALW
(2)Change CN18 pin2 power rail as +3VRUN
(3)Connect CN18 pin 22 from RST_SUS# to PLT_RST#
P50 Connect U67,U63,U64,U114 pin 1 from RST_SUS# to SUS_ON
P39 Add CN21 signals for both OIDE (MS_30) and RF(MS_50)
P64 Add CN36 for CIR I/F

9/6
P30 remove R584 ,short CLK_32KX2 and CLK_32KX2_R
P63 remove R1055,short U2_XTALOUT and A0501
P39 remove Q79,R1266,C1222,R1267,Q80 ,connecto L66 to +5VRUN
P46 change CN59 to 10p and pin define
P47 add U59,C969 for reserved 1394 EEPROM
P64 (1)remove CN44,CN45,CN46,
(2)R756 pin 1 connect to +3VRUN
(3)change CN61 pin define
P46 Add US8A pin J2 as MS_LED
P34 CN32 pin 37 change to test pad

9/6 Power
P54 (1)remove PR314,PR315,PR316,PR317,PQ92A,PQ92B,PQ93A,
PQ93B,PC2,PR318,PR319,PQ21,PC336,PR24,PQ8
rename MAX1909_BATT to BT+ for delete BATT_EN function
(2)remove PR319
P62 (1)add PC1640,PR1802,PR1804,PQ76, for VGA power dynamic switch
(2)add PC197 for VGA power input caps
P65 remove C1152,move R1225,R1228 to Page8
P61 remove PD36 for delete net BATT_EN function

9/7
P52 remove R1305 and R1309 for duplicate with R1750 and R1754
P29 change GPIO IMVP_PHASEGD to SB GPIO5,
P31 (1)SB GPIO 10,12,13,15 PH 10K to +3VALW(R649,R650,R671,R672)
(2)SB GPIO 21 PH 10K(R1168) to +3VRUN
P37 BT_WLAN_SW# PH 10K(R1317) from +3VRUN to +3V_S3_SUS and add C1637 for ESD
P35 (1)Remove D26,R1108
(2)ALW_ON,SUS_ON,RUN_ON,RUN_ON_A,RUN_ON_D,SIO_FA1 PL 47K(R1805,R1806, R1807,R1808,R1809,R705)to GND
(3)U32 pin106(ES1RXD)connect to CN15 pin23, U32 pin107(ES1TXD) connect to CN15 pin25
(4)change U32 Pin176 to NC for reserved fan2
(5)change U32 Pin23 to NC
(6)change U32 Pin24 to NC
(7)change U32 Pin28 to JIG_SMI#
(8)change U32 Pin41 to NC
(9)change U32 Pin54 to NC
(10)change U32 Pin91 to NC
(11)change U32 Pin105 to FWH_BOOT
(12)change U32 Pin109 to PWR_CIR#
(13)change U32 Pin118 to PWR_RF#
(14)change U32 Pin168 to PWR_OK
(15)change U32 Pin171 to FAN1_TACH
(16)change U32 Pin175 to NC
(17)change U32 Pin71 to VOL_UP
(18)change U32 Pin72 to VOL_DN
(19)change U32 Pin73 to NC
(20)change U32 Pin74 to NC
(21)change U32 Pin99 to NC
(22)change U32 Pin100 to NC
(23)change U32 Pin1 to SW_CIR#
(24)change U32 Pin82 to SW_CIR00
(25)change U32 Pin83 to SW_CIR01
(26)change U32 Pin84 to SW_CIR02
(27)change U32 Pin36 to FAN1_PWM

P56 ALW_PWRGD PH 10K(PR328) from 3D3V_OUT to +ECVCC
P64 CN36 pin9 PWR_CIR# PH 10K(R1786) to +3VALW
P39 RN31 pin2 PWR_RF# PH 10K(R1791) to +3VALW
P35 (1)Add U32 pin97 as SYSTEM_ID4,pin 98 as SYSTEM_ID5,
(2)change U32 pin175 to NC
P16 (1)remove R262 short L_NV_VDD and NV_VDD to NV_VDD
(2)remove R259 short L_PEX_VDD and PEX_VDD to PEX_VDD
P21 Add L107,C483,C484,C486,C482 for VGA VID_PLLVDD power rail
P44 Add C1088 for filter
P24 (1)U12, Group4->Group5,Group6->Group4,Group5->Group7,Group7->Group6
(2)U11,Group3->Group5,Group2->Group2,Group1->Group1,Group0->Group0
P25 (1)U13,Group1->Group1,Group0->Group3,Group3->Group0,Group2->Group2
(2)U14,Group5->Group7,Group6->Group5,Group4->Group6,Group7->Group4

9/7 Power
P53 Add +5V_S3_SUS and +3V_S3_SUS in power block diagram
P55 Add PR342 for MS50
P56 (1)change PR65 from 270K to 200K 1% 0402
(2)change PL9 from 2.2UH_6.86x6.47x3.0 to 2.2UH_13.2x12.9x3.5
(3)change PQ27,PQ109 from SI4800BDY to SI7404DY-T1-E3
P45 change U122,U123 from G913 to G923-330TIUF
P41 (1)change C876 from 10U_6.3V_M to 10U_25V_M_B
(2)change CAP13 from 47U_6.3V_3528 to 10U_25V_M_B
P59 (1)change PQ118,PQ120 from SI7392DP-T1-E3 to SI4684DY-T1-E3
(2)change PQ117,PQ119,PQ121,PQ122 from SI7336ADP-T1-E3 to SI4324DY-T1-E3
P60 change PQ52 from SI4800BDY to SI4892DY-T1-E3
P61 Add U132 for BT+ path power limit

9/8
P3 add C3 close to chip for sensor
P22 add C487 close to chip for sensor
P35 U32 pin24 change to NC
P7 Add C1396 for DDRDIMM_VREF
P52 remove C1602,C1614,C1616,C1618 for duplicate parts

9/13
P48 add Q57 for SD power
P5 short R1415
p31 add R673 for reserved OVT_EC# to SB GPIO12
P3 R1404 change to 56ohm
P3 remove R1400 ,add TP(TP596) for DBRESET#
P7 add RN32 for external vga use
P3 add text note for VCCA_CPU
P8 remove R1633,R1634 adn add test pad for L_CLKCTLA,L_CLKCTLB
remove R1632
P08 add R1810,R1811 for CRT disable
P12 remove R1774 and add test pad for MCH_CFG_20
P19 add vale NV_ for C322,C323,CAP10
P21 add vale NV_ for L136,C1633
P22 R321,R317,C495,C494,Y2 to NC,
Mount R1132,R1131
C496 value remove NV_
P25.26 change C605,C575 value to NV
P28 C1151 value remove NV
P29 SPI_CS#/SPI_MOSI/SPI_MISO add test and remove pH resistors
P30 remove R590, R591, R607, and R1205
P30 C1530-1533 remove
P31 add R675,R1762,R1761,PQ78,PQ79 for lan SMbus S3_SUS power
change U31 power source to +3VRUN and SMbus connect to SMB_CLK_SB,SMB_DATA_SB
P32 change R1384 to 0603 size
P34 R987 short to GND
CN32 pin 3 connect to GND
pin 32 NC , reverse R1510
P35 R698,R699 pull up to +ECVCC
P61 add PURE_HW_SHUTDOWN# to OVP
P39 U36 pin21 connect to +3V_S3_SUS
P48 remove R1778
P49 add R1812 ph 10K to +3VRUN for U58B pinC4
P51 add C311,C349 for PCIE AC couple caps
P56 remove U130 connect ON3_ON5 to ALW_ON
P22 add R1819,R1818 for 27MHz_non_spread 3.3V level to 1.2V
P40 (1)change U39 pin25,38 power source to +5VRUN
(2)C1249,C1250 value add NC_ and connect to MIC_L
C1251,C1252 value add NC_ and connect to MIC_R
(3)change U39 pin37 to NC
(4)C1270,R799 connect to Digital GND
(5)remove GP3 and add C1638
(6)change U41 to 78D05
P41 (1)R847,R852 change to 33K
P42 (1)R1171,R1172 change to 4.7K
(2)R1635,R1637 change to 11K
R1639,R1640 change to 20K
(3)MIC1_VREFO_R change to MIC1_VREFO_L
(4)add GP16,GP17
P43 (1)move R1319,R1360,C1255,R1321,U127A,U127B,R1329,C1230, R1318 to IntMIC Board
(2)remove U102,U105,D67,C1188,Q87,Q42,U104,R1370,R1361, U50,R1376,Q86,R1156
add R1823,R1824,R1826,R1822,R1825,Q88,Q89,Q90,R1827, R1828,R1829,C1640,Q91,C1639
(3)MIC1_VREFO_R change to MIC1_VREFO_L
(4)change C1088 to 10u_10V_Y_Y,
change R1323 to 6.8K
add R1821
P45 (1)connect U122,U123 pin 2 to A_GND
P46 (1)connect U58 pinK5 to PWR_OK
(2)add R1830
(3)modify CN59 pin define
P51 (1)add R1831,R1832,remove U129 pin42.43(SMbus) interface to SB SMbus
(2)add R1833
P38 connect OVT_EC# to U131 pin4
P60 R1602,PR426 change to 470K
P61 PD34 change to MMHZ5234BPT, R1796= 33K 1% 0402, R1797 20K 1% 0402, PR185 = 15K 1% 0603
P31 add SW2 for SYSTEM_ID00~03 on SB GPIO 22,23,33,34
P35 RP110 PH +5V_S3_SUS
P62 PR1804 change to 10K
P61 change PR199 to 33K
change PR207 to 47K
add PR1834,PR1835,PR1836,PR1837 for MS50
P30 R1304 change to NC_
P35 Add R702 for Monitor_off# PH
P28 add L138,L139
P47 L73 change to 90R-100MHZ_0R35 and add L141

9/14
P24 change U12 to no mirror setting
P25 change U14 to no mirror setting
P44 change R1868 to 2K
change R1869 to 2K
add R1870,R1872 for power rating

9/15
P50 Swap L87 for layout
P38 add L140
P45 populate R1783,R1784
Dummy R1663,R1782,R1662
P40 change U41 to TPS79301DBVR
P45 change U58 pinK5 to RUN_PWRGD
P46 add R1873 for separate 7412 power
P63 change PR418 to 820K 1%
change PR421 to 10K 1%
change PC210 to 10pF
P58 change PR333 to 910K 1%
change PR305 to 9.1K 1%
change PC374 to NC_470uF
P10 change L117,CAP27,C1386,L120,CAP28,C1389 value to EA_*
P31 rename SMB_CLK_SUS to SMB_CLK_ALW,SMB_DATA_SUS to SMB_DATA_ALW
P29 RSVD1,2,5,6 connect to GND
P60 R1602,PR426 change to 220K
P41 change amp to LM4991LD

9/16
P22 U8 pin 4 connect to THERM_ALERT#GPIO8
U8 pin6 connect DDR_ALERT_EC#
P38 add R769 for OVT_EC# PH resistor
P50 change CN37 pin connection
P48 correct CN55 symbol
P52 change CN63 pin define
P55 change PCN4 pin define

9/20
P29 Swap net of RP92-RP95
P31 Del PQ62,PQ67,R635,R669 and R637
Change Net name SMB_CLK_SB , SMB_DATA_SB of U29C-Pin C22 and B22
P32 Change L119 to 4.7uH
P34 Add Net : SLOT_IN at CN32-Pin50
P35 Add Net : SLOT_IN and add R1884-1886 at U32-Pin172
Del Net : FWH_BOOT, Change to TP785 of U32-Pin105
P36 Del R735 and del Net : FWH_BOOT of CN15-Pin15 , Change to TP786 ,
Change symbol : CN15
P38 Change symbol : U20
P39 Del RN31,Add R1881(ON),R1882(Dummy),R1883(Dummy)
Change R784 power from +5VALW to +5V_S3_SUS
Change R1800 power from +5VALW to +5V_S3_SUS
P40 Change Net name : MIC1_L ,MIC1_R of U39-Pin35 and Pin36
Del C861,C1248 and del NET: PC_SPKRIN
Del C1574,C1575,R797,R799 and C865
Change Net name PCBEEPPL to AEC_MIC_L
Change Net name PCBEEPPR to AEC_MIC_R
Add R1887-R1890 , D80 , Q103,Q104 and CN66
P41 Change symbol & value : C910,C911 to 0.033uF
Change symbol : U141,U112
P43 Change Q89 and Q90 to Dummy
Del U100,R1322 and C894
P44 Change symbol : U133,U134,U135 and U137
P46 Change symbol : LED4
P48 Change symbol : CN26
P50 Del R969,R972,R1044 and R1525
Change Package CAP17,CAP18 and CAP34
P53 Change +12VRUN/1.5A to +12VRUN/1.2A
Change +3VALW/7.0A to +3VALW/9.5A
Change +1_8VSUS/16A to +1_8VSUS/14A
P54 Add R1838,R1839 at PU1-Pin5
Add R1840,R1841 at PQ11-Pin1
P57 Change PL104&PL11 to 1.5uH
P58 PD16 Change to CH500H-40PT
P59 Change PL13&PL21 to 0.36uH
P60 D79 change from NC to mount
Change +5VALW from 4.2A to 3.5A
Change +12VRUN from 1.4A to 1.2A
Del PC380,PC381(22uF POS CAP)
Add PC380,PC381,PC401 and PC402 to 22uF MLCC type cap
Change PR174,PR182 and PR187 to Dummy
P61 Del PD2A/B,PD27A/B and PD30A/B
Add CHN222PT for PD2,PD27 and PD30
P62 Change PD53 to CH500H-40PT
P65 Vertically RP10&RP109

9/21
P48 add R1892,R1893 for discharge path
P03 change Q100 to MMBT3904 and add R1891
P04 Connect CN36 pin5 to +3VALW
P34 Change D77,D78 to SSM22LLPT
P56 change PR40 to 160K_F,PR52 to 100K_F for TV-TUNER
P39 add R785,R784 for reserved +5VALW for RF
P58 change PC89 to 0.1uF,PR335 to 10 ohm ,PC90 to 10nF
P17 change R205 value to NV_,R206 to NC_ for Infineon
P24,25 change U11,U12,U13,U14 to Infineon HYB18H512321AFL28
P36 change BIOS ROM(U34) to EN29LV800BB-70TCP(EON)
P29 change D79 to 9.5V Zener MMPZ5239BPT
P28 change U17 to GS48B2P1U
P40 (1)remove L112, connect U39 AVDD1,AVDD2 to VDDA
(2)C1576,C1577 change to 2.2UF
(3)serial R1896,R1897 for SPK_L,SPK_R
(4)change C1238,C1239,C1270 to 1UF
(5)add C1687,C1688,C1689,C1690 for AEC_MIC_L,AEC_MIC_R
(6)replace C869 with CAP38(100U_6.3V_7343)
(7)add R1898,R1899,C1691,PQ128,R1901,R1900,C1692,R1902,PQ129,R1905,R1903, PQ131,R1906,
R1904,PC136,R1907
P41 (1)change amp gnd to PGND,
(2)add L142,L143,L144,L145
P60 change PR427,R1603 to 100K
add PQ126,PQ115,R1911,R1912
P48 CN26 pin2 connect to +3VRUN
P45 U124 pin 31 connect to RUN_PWRGD
P22 C487 change to NC_
P31 add R785 for protect GPIO33
P34 C791,C792 change value to NC_
P35 rename SLOT_IN to SLOT_ON
P46 change R32 to 100 ohm
P61 add R361 for merge Power Limit
P21 add R1275 for reserve disable CRT

9921 Audio
P40 (1)add sense_A,SENSE_B related schematic
(2)remove Buzzer schematic
(3)add C1687,C1688,C1689,C1690 for ACE_MIC_L,AEC_MIC_R
(4)serial R1896 on SPK_L,serial R1897 on SPK_R
(5)bypass L112, and connect to VDDA
(6)add L76 for U41 power
(7)add CAP38 for VDDA Output caps
(8)change R801 to 29.4K_F for adjust VDDA voltage to 4.75V
P41 (1)add R1908 for GND and PGND
(2)change AMP GND to PGND
(3)mix LCH and PC_SPKRIN,mix RCH and PC_SPKRIN
(4)add L142,L143,L144,L145 for speaker EMI
(5)NC D70 and D71
P42 add Line_in signal on CON4 pin4
P43 (1)reverse the polarity of HW_POP_MUTE_EC to HW_POP_MUTE_EC#
(2)separate MUTE signal (MUTE_AMP and MUTE_TR)
P44 (1)change EQ GND sourse to PGND
(2)change R1840,R1846,R1849,R1836 to 10K_D
(3)change R1857,R1863,R1853,R1865 to 10K_D
(4)change R1851,R1867 to 33K
(5)change R1858,R1841 to 10K_F 1%
(6)correct C1649,C1655,C1665,C1670,C1666,C1651 symbol
(7)replace C1678 with 22U_16V_M_B(100U/16V TQC 禁用料)
(8)replace C1680 with 100U_6.3V_7343
P45 connect U124 pin 31 to RUN_PWRGD

0922
P10 (1)bypass R1475,R1470
(2)change L115 to HCB2012KF-121T30
P19 (1)change C1192 to 0603 size
P22 remove R1133
P28 (1)change R461 to 200_J 0603
(2)add INV_BRADJ PL resistor R773
(3)connect NB_BRADJ to Cn49 pin4
P32 bypass R655
P39 (1)remove R774,R772,Q35,R1096
(2)connect CN19 to EXPRESS_DET#
(3)U36 pin23 change to NC
P46 separate C954,C955
P47 change R934,R940,R942 to 1K
P22 add R307 for NV_JTAG_TMS PH +3VRUN
add R309 for NV_JTAG_TDI PH +3VRUN
add R306 for NV_JTAG_TCK PL GND
P48 modify SD/MS card power
P64 change CN36 pin10 to CN+5V_S3_SUS
P10 change C1381,C1382 to 10U_6.3V_Y_Y
P52 connect CN40,CN63 GND to GND_TR
P55 (1)change PR373,PR374 to 10K
(2)change PR408 to 4.7K_J
(2)change PR15,PR16 to 33_J
(3)PC9,PC10,PC11,PC12,PC13 change to 47P

0923
P43 add C1695 for EMI
P59 change PR272 to 2K_J
P07 add R1444

0924
P41 change F1 to 125V-4A_6.1x2.69x2.69
P40 add R1913,R1914
P41 connect C865 to P_GND
P43 add R1871,C1641,R1917,Q92 for MUTE_TR
P43 change Q89 to NC_MMBT3904,change HW_POP_MUTE_EC# to HW_POP_MUTE_EC
P35 change HW_POP_MUTE_EC# to HW_POP_MUTE_EC
P23 change R1592,R1593,R1594,R1580,R1582,R1584 to NC
P05 bypass R1416
P07 mount R1443,NC R1441
P28 change U106,R1330 to NV_
P29 remove R577, add test pad for RSVD_9
P30 change R589 to 510_F,add R1916
P35 connect R707,R706 to +3V_S3_SUS
P35 remove U121,R1629,R1628,R1630
P61 remove PR368
P39 remove R1800
P39 change SW17 value to MS50_*
P39 add Q79,R1267,R1266,C1222,Q80,R788 for camera power
P35 add CAM_PWREN for camera power
P46 Mini1 Pin11,13 change to NC
P60 add PC399
P38 remove C827,add D80,C1696 for fan speed

0926
P63 R48 pin 1 connect to R_CLK_ICHPCI because swap R_CLK_ICHPCI and R_PCLK_JIG
P35 remove R723
P43 remove R943
P60 (1)add +5VRUN_1 for layout,
(2)+5VRUN in P32,P34,P42,P59 change to +5VRUN_1,
(3)add PQ90,R191 for +5VRUN_1 discharge path

0926
P63 R48 pin 1 connect to R_CLK_ICHPCI because swap R_CLK_ICHPCI and R_PCLK_JIG
P35 remove R723
P43 remove R943
P60 (1)add +5VRUN_1 for layout,
(2)+5VRUN in P32,P34,P42,P59 change to +5VRUN_1,
(3)add PQ90,R191 for +5VRUN_1 discharge path

0927
P60 add PC403,PR1797 for PQ135 soft start
P39 pin 3 connect to SUS_PWRGD
P48 add R1920-R1924,R1926-R1930 for MS DUo and SD signals
add R967,C1005 for SD_WP
P49 R965,R966 change to 1K
U62 pin 21 connect to RUN_PWRGD
P50 change USB power switch enable pin to SUS_ON
P41 add U142,R798,Q93,R1918,C1697 ,remove C1575
P42 (1)R848,R857 change to 20K
(2)mount R1639,R1640,and change C1578,C1579 to 470P
(3)move GP14 close to INT MIC jack
P43 connect R1825 pin2 to +3VALW
P44 connect C1676 pin2 to PGND,conenct C1675 pin2 to GND,put L139 between C1676 pin1 and C1675 pin1
P40 connect C873 pin2 to A_GND,connect C1154 pin2 to GND,put L176 between C873 pin1 and C1154 pin1
P46 change Q1 to PDTC144EU
P62 reserve R1931 PH +5VRUN for VGA power good
P60 change PR406 to 0.008_1W_F
P36 correct U34 pin45 to SIO_FA0

0928
P60 change PR361 to 1K 0402
P46 change R1141 to 0 ohm
P60 (1)add PQ137,PQ67,
(2)change PR1797 to 1K,PR1795 to 110K
P51 connect LAN_TXP1 to U129 pin54
connect LAN_TXN1 to U129 pin53
connect C311 pin2 to U129 pin50
connect C349 pin2 to U129 pin49
P42 add R816,R814 for jack detect
P60 mount R1445

0929
P62 (1)add PR228 for vga power,
(2)PR415 pin1,PR416 pin1 connect to +5VALW
P47 mount U59,C969

0930(after rename)
P40 connect U19 pin49 to A_GND
P35 change CN35 value to MS30_HEADER CONN_7P

1001(after rename)
P34 cn10 pin 25,26 change to NC
P46 mini1 pin128,127 change to NC
P48 cn32 pin15,16 change to NC
P39 cn27 pin29,30 change to NC
P49 cn6 pin85,86 change to NC

1005R
P39 change R651 value to 10K_J
P38 change R499 value to NC_10K_J





FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title: History(EVT)
Size: Custom | Document Number: MS30-1-01 | Rev: 1.00
Date: Friday, March 31, 2006 | Sheet 66 of 67

## History
## REV 0.30 (2005/12/01)

DVT
P64 CN1 pin1 change to +3VALW for leakage
P52 mount R779 for lan get ip fail
P40 net name HW_POP_MUTE_CODEC# change to HW_POP_MUTE_CODEC
P43 (1)net name HW_POP_MUTE_CODEC# change to HW_POP_MUTE_CODEC
(2)change Q11 from MMBT3906 to MMBT3904
P60 mount PR224 for +5V_S3_SUS discharge too slow
P57 (1)change PR155,PR164 from 0ohm to 3.3 ohm for decrease 1.5V/1.05 noise
(2)mount PD21,PD24 for decrease 1.5V/1.05 noise
P59 mount PC278,PC279; mount PC88,PC109 for decrease Vcore noise
P62 mount PC92 for decrease VGA power noise
P40 (1)mount R682,R694 for sense_B,sense_A detect
(2)NC R308
P44 NC R643,R647
P43 mount R381 for amp abnormal be mute
P41 change JSPK1,JSPK2 from 2N-0002000-M0N0 to 2N-0002001-M1T0
P39 change CN33 from 1N-0008000-M1T0 to 1N-0008001-M1T0
P64 change CN36 from 1N-0002001-M1T0 to 1N-0002000-M1T0
P46~49 change U10 to PCI8412ZHK
P59 change PQ3,PQ30 to 17-S14324D-YT00
P40 U19 change to CXD9872AR
P29~P33 for EVT2 U6 is 12-CALIST0-A300(GML)
P41,P42 CON1,2,3 change to 2N-0006002-FKX0
P22 R567 change to 16-CH520S3-0P00
P59 PQ58 change to 17-S14324D-YT00
P58 PR193 change to 6.2K_F,PR136 change to 82K_F
P62 PR127 change to 6.2K_F
P60 PR37 change to 120K_F,PR171 change to 6mohm, PL6 change to 2.2uH
P24,P25 Change R99,R148,R165,R167 from 120 Ohm to 80.6Ohm 1%
P60 change PQ51,PC142,PQ35 value to NV_
P43 add Q12,R772,R773 for adding EC to control mute function
P45 (1)add R342,NC R343 for Change VP1020 initialization to SHI mode
(2)NC U45,R355
P59 NC PD2,PD19
P60 add PR219,PR169
P24 change R165 to 40.2_F and add R1160,C809, R1163,C810 for nvidia latest demo board for G72
P25 change R148,R99 to 40.2_F and add R1164,R1165, C811,C812 for nividia latest demo board for G72
P43 change U21 to M74VHC1GT32DFT2G for shortage of toshiba parts
P41 change Q24,Q25,Q26,Q27 to PBSS2515F.115 for toshiba parts shortage
P16 add U49 for PLT_RST# to VGA
P28 add C815,C813,C814
P29,45 connect GPIO17 to AEC pin30 powerdown
P35 (1)add D15,D16,D17 for preventing leakage from EC before power on
(2)reserved U3 pin 176 for second fan FB,pin43 for second fan PWM
(3)add U3 P105 as EC_LED to control LED brightness
P36 change CN12 pin1,pin21 to +ECVCC
P38 (1)add R1166 for discharge path of +5VALW_LDO
P39 update Q19 footprint
P43 change Q11 to MMT3904
P34 add CAP23,CAP24
P62 add PR439,delete PR123,NC PC92 for preventing VGA_GPIO5 floating
P63 delete R204,add R1171 for PCIE_LAN_CLKREQ# pull low
P45 delete PQ77
P48 change CN18 to smaller size
P47 change CN14 to 1394 normal type
P42 change CON3 to Red color
P41 JSKP1 change to 3 pin for manufacture
P43 delete R396,R393,C359,R395,C360
P54 add PC340
P55 change PD38 to MMVZ5235BPT for battery in UVP fail
P38 change second fan to adjustable
P56 add PC347,PC346,PC341,PC158 for +5VALW
P57 add PC349,PC350,PC342 for +1_5VRUN
P58 add PC351,PC352,PC343 for +1_8V_S3_SUS
P59 add PC353,PC354,PC344,PC355,PC356,PC345,PC278, PC279 for VGCORE
P57 add PC348,PC196,PC197,PC359
P59 change PD2,PD19 to NC_SPL1040PT (10A)
P60 (1)change PQ48 to SI4892DY-T1-E3
(2)add PL14 for MS50,PL6 for MS30
(3)add PC357,PC358 for +12VRUN
P34 add CAP23,CAP24 for MS50 HDD
P30 add R1175 for MS50 SATA Cable
P64 (1) delete R783
(2) CN1 add EC_LED to control LED brightness
(3)CN1 pin 1 change to +5VALW
P60 add Pr436,PR437,PQ81,PR435,PQ83,PR438, PC360,PQ82,R1176 for +1_8VRUN timing
P54 (1)add PR442,PQ84,U50 and connect PR182 pin2 to +ECVCC for preventing leakage of charger LDO
P56,57,58,59,60 Update PL6,PL9,PL7,PL8,PL2,PL4 PL5,PL14,PL1,PL3 footprint for shaking test

1202
P40 Follow FAE suggestions
(1)add C820(10U_10V_M) for AVDD
(2)change C305 to 10U_6.3V for VREFFILT
(3)change R752 to 1% tolerence

1205
P29 change GP4 to R1402
P51 add R1403,NC R665 for LAN S4 wake up
P54 add PC362
P57 add PR440,PR441 for balence 2 caps voltage
P22 U9 update new version

1206
P22 rename R567 to D19
P45 NC C770
P51 change R665 value to MS30_0_J,R1403 value to MS50_0_J
P60 NC PQ67,PQ46,PQ21,PQ52,PQ35,PQ36,PQ4,PQ47,PQ8
P62 change PC123 to 22U_10V_Y_Y,PC124 to 220U_2.5V_M for reduce PEX_VDD ripple
P64 add C821~C834 for protecting EC from ESD
P35 add C835~C838 for protecting EC from ESD
P39 add C839 for protecting EC from ESD
P36 add C840~C844 for protecting EC from ESD
P41 change R233,R231 to 47K_F,addC850,C847 C851,C846
P44 (1)R261,R255 change to 56K_F
(2)R248,R254 change to 2.4K_F
(3)R246,R251 change to 2.2K_J
Add TB1~TP77,TT1~20 for manufacture TE test
P44 add GP7.GP8.GP9 for MIC quality
P57 mount PR159

1206_1
P3 change Q21 to 2N7002
1206_2
P59 PC4,PC12,PC18,PC19,PC98,PC105 change to 330U_2.5V_M

1207
P28 change CN3 to 1N-0030000-FWG0
P42 change R693,R683 from 11K_F to 7.5K_F
P38 change second fan(CN7) source(R1173,Q29) to +12VRUN

1208
P52 CN24 chnage from 10pin to 8pin
P51 change R665 value to 0_J,delete R1403

1209
P59 add TT21~TT27 for manufacture
P61 add PC363 for PU5 power bypass
P38 add R1403 for reserve 12V path to second fan
P42 update U17 to MAX4232AKA+T
P59 delete PR14~PR20 ,and short
P08 delete R76,R63,R78,R542,R62,R77,R64,and short
P10 delete R544,R536,R65,R535,R79,R543 ,and short
P12 delete R514,R508,R541,add TP248,TP249,TP250
P30 delete R702,R697 and short
P41 (1)change R225,R226 from 22K_J to 47K_J
(2)change TB8~TB11 to 40mil
P46 (1)add R1404,C1397(NC),C1398(NC) for separate power for reduce noise of tv-tuner
P60 add R1415,C1400(NC),C1401(NC) for separate power for reduce noise of tv-tuner
P63 change R599 to 100_J,add L54 for PCLK_MIN1
P57 change PR440,PR441 from 2.2K_J to 100K_J
P54 (1)PQ63 change to SI4825
(2)mount PD7

1212
P63 mount C598,C599 for EMI
P55 mount PC81 for EMI
P30,P46,P56,P63,P64 Add EC1~EC24 for EMI solution
P59 reserve PR444,PQ85,PR445,PC364,PR443 for max8771 CLKEN# abnormal
P29 change R389,R776 from 39_J to 47_J for SI

1213
P28 add Q31 for LCD_VDD discharge path
P46 change EC2~EC7 value to MS50_*
P43 mount R778,Q14
P44 (1)change R248,R254 from 2.4K_F to 1.5K_J
(2)change R246,R251 from 2.2K_J to 2.4K_F
P48 (1)change R212,R213,R221,R222 from 0_J to 68_J for SI
(2)change R215 from 1.5K_J to 1K_J from customer suggestion
P54 (1)change PR183 from 15.4K_F to 20K_F
(2)change PR49 from 20K_F to 24K_F to set constant power to 4.09A(87%)
P57 (1)NC PC196,PC197
(2)change PR440,PR441 to NC_27K_J

1214
P50 change CAP17,CAP19,CAP20,CAP22 to 100U_6.3V_M for vendor shortage
P54 add PD43
P59 change PR7,PR126 to 3.3_J

1215
P61 change PD4 value to NV_*

## History
## REV 0.40 (2005/12/18)

1219
P54 change PD7,PD43 from 16-MMP2525-3B00 to 16-MMP2525-1B00
P63 change EC11,EC12 to 10P_50V_J_N
P51 change CN21 to MS30_*

1227
P42,P59 Update c282,C758,PC94,PC102

0110 for PVT BOM
P50 change CAP17,CAP19,CAP20,CAP22 to 150U_6.3V_M(NEC/TOKIN)
P54 (1)change PQ63 to AO4407
(2)NC PC362 for battery issue
P41 change L42,L43,L44,L45 to BLM18PG330SN1D
P20 (1)change R555 to 49.9 ohm 1%
(2)mount R556
P24 (1)change R165,R1160,R1163,R167 to 240_F
(2)change C809,C810 to 0.01U
P25 (1)change R148,R1164,R1165,R99 to 240_F
(2)change C811,C812 to 0.01u
P16~23 update U6 P/N to 12-G73NA20-A200
P43 NC R773 for +5VRUN leakage
P64 (1)change EC23,EC24 value to NV_*
(2)change CN36 value to MS30_*
P60 mount PR98,PQ21 for +5VRUN leakage
P56 change PR80 to 102K_F for meet TV-tuner power spec
P59 change PQ3,PQ30 for better VHcore design

0120
P37 add Q32 for wireless led always on
P38 add D20,D21 for fan reverse current to damage Q5
P49 update CN6,CN5 footprint
P55 add PR446,combine PQ22A/PQ19B to PQ19(2N7002DW) for abnormal ALW_ON
P60 add PQ86 for improve rf quality
P43 add Q33,and change Q14 to MMBT3904 for leakage
P37 change SW2 to SSSU011700_SW-DIP3
P48 change CN9 to MOLEX_67913-0009 for factory repair

0121
P64 change CIR connector value to MS50_* for ms50 only
P39 change L8,L18 to 120R-100MHZ_0603 for curren rating
P8 mount R69,R68,R66,R493,R494 ;NC R83,R82,R80 for disable CRT
P10 mount R547,R518,C454 ;NC R540,C453,D3,R548,L21,L25,C414 for disable CRT

0123
P8 change R67 value to 0_J,dummy R495,R492,R81 for CRT disable
P65 dummy R488,R489,R490,R478,R479,R70,R84 for CRT disable
P19 dummy R558 for G73M
P61 change PC188 to X5R type
P22 dummy R5,R2,R8,R7,R10,C23,C25,C24,U26,R11
P63 change R599 to 100ohm 0402 1%
P30 add PJ31 for RTCRST#
P61 add PC366 for reserve ;PD5B pin 4 connect to GND for preventing floating

0125
P64 change PAD3 to pad_smd283x110
P54 update PL10,PL11 footprint for cold solder issue
P63 update L54 vendor to TDK
P28 delete L37 and short for inverter fuse current rating
P60 change PQ86,PC365 value to MS50_*
P56~62 delete PJ1~PJ4,PJ6~PJ27,PJ29,PJ30 and shot
P54,P56~61 add TT29~41 for power test

0207
P48 change CN32 to 1N-1010003-0000
P34 change CN10 to 2N-0022000-MKG0(shorter pin length)
P41 (1)change JSPK1 to 2N-0002002-M1T0(shorter pin length)
(2)change JSPK2 to 2N-0003001-M1T0(shorter pin length)
P39 add F2 for protection
P16 reserve R1405 for new G73M
P22 reserve R1406 for new G73M

0208
P38 mount R1403,dummy Q30,R1173,R1174,Q29,D21 for fix mode by cusomer suggeston
P50 update U42 part number to 12-88E8036-A100 for manufacture
P64 change H1,H8,H14 footprint
P59 add TT42 for power test
P63 change R599 from 100ohm to 47ohm(1R-0000470-J200)
P39 change F2 to 1M-F24V0A2-0000(24V-0.2A_1206)
P34 reserve R1407 for Staggered spin-up disable by customer suggestion
P43 add C1401 by customer suggestion
P41 (1)change C220,C221 from 0.47u to 0.22u
(2)change C675,C674 from 1u to 6.8u
(3)change R1167 from 1K to 2.2K
(4)add R1408,C1399,R1409,C1400 by customer suggestion
P48 NC CN18 pin1,4 and remove R742,R743,L51,L52 by customer suggestion
P22 mount R1406
P40 change U19 to CXD9872K

0209
P56 reserve R1410 for discharge path

0210
P28 mount C363,C364,C365,C366 for EMI
P41 (1)change R225,R226 from 47K to 100K,
(2)change R227 from 2.2k t 270 ohm
P65 add EC25~EC36 for EMI
P44 add GP10 for EMI
P35 add U51,C1402 by customer suggestion
P55 change PQ19 to 17-2N7002S-PT00
P30 (1)change R745 value from MS30_24.9_F to 24.9_F
(2)dummy R1175
P48 change R215 from 1K_J to 330_J for SD card power drop

0213
P44 change GP10 to R1411(MS50_0_J) for EMI
P38 add F3,F4 for cable short protection
P39 add F5 for cable short protection
P64 add F6~F11 fo cable short protection
P31 (1)connect GPIO21 to U20 pin14 for bypass AEC
(2)dummy R304 for double pull low
P45 connect U20 pin14 to SB GPIO21 for bypass AEC
P54 add PR447,PC367(snubber circuit) for dc_in inrush voltage/current

0214
P38 delete F3,F4
P64 add F14 for cable short protection
P35 add F12,F13 for cable short protection
P45 add R1412 for hardware disable

0214_1
P38 add F4
P60 correct PQ6,PQ81,Q8 part number(TP610K-T1-E3) to TP0610K-T1-E3
P56 correct PQ55,PQ56 value to SI7404DN-T1-E3
P57 correct PQ37.PQ38,PQ39,PQ40 to SI7404DN-T1-E3

0215
P39,P38,P35,P64 change F2,F4~F14 size from 1206 to 0603
P60 correct PQ6,PQ81,Q8 vendor part number(TP610K-T1-E3) to TP0610K-T1-E3

0216
P39,P38,P35,P64 change F2,F4~F14 to 1M-F32VA75-F001 FUSE,Littelfuse,0467.750,32V, 0.75A

0223_SMT
P28 dummy C363,C364,C365,C366 for LVDS timing by customer
P42 change R693,R683 from 7.5K to 13.7K for Line in FSIV
P39 change F5 to 32V_1A_0603,F2 to 32V_0.5A_0603
P29~P33 update U44 part number to NH82801GBM_B0
P54 update PR447 to 1_F 0805,1R-0000010-F500
P39,P38,P35,P64 change F2,F4~F14 to 1M-F32V0A5-F000 FUSE Littelfuse,0467.500,32V, 0.5A

## History
## REV 1.00(2006/03/02)

MP

0302
P48 change CN32 to Yamaichi_JCS010_2005_1 for vendor shortage

0303
P41 (1)change C675,C674 to 1C-2B70225-M000 for 6.8U_6.3V_M shortage
(2)add C1403,C1404(1C-2B70475-K201) for 6.8U_6.3V_M shortage
P39 remove TB6,TB7 for manufacture test issue

0311
P39 change F2 to 32V_1A_0603 for cureent rating
P41,43 Change Q9,Q13,Q28 from 17-MMBT390-6000 to 17-MMBT390-6K00
P57 change PR165 to 1K_F,PC30 to 2.2uF,16V for adjusting 1D05V power on/off sequence



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