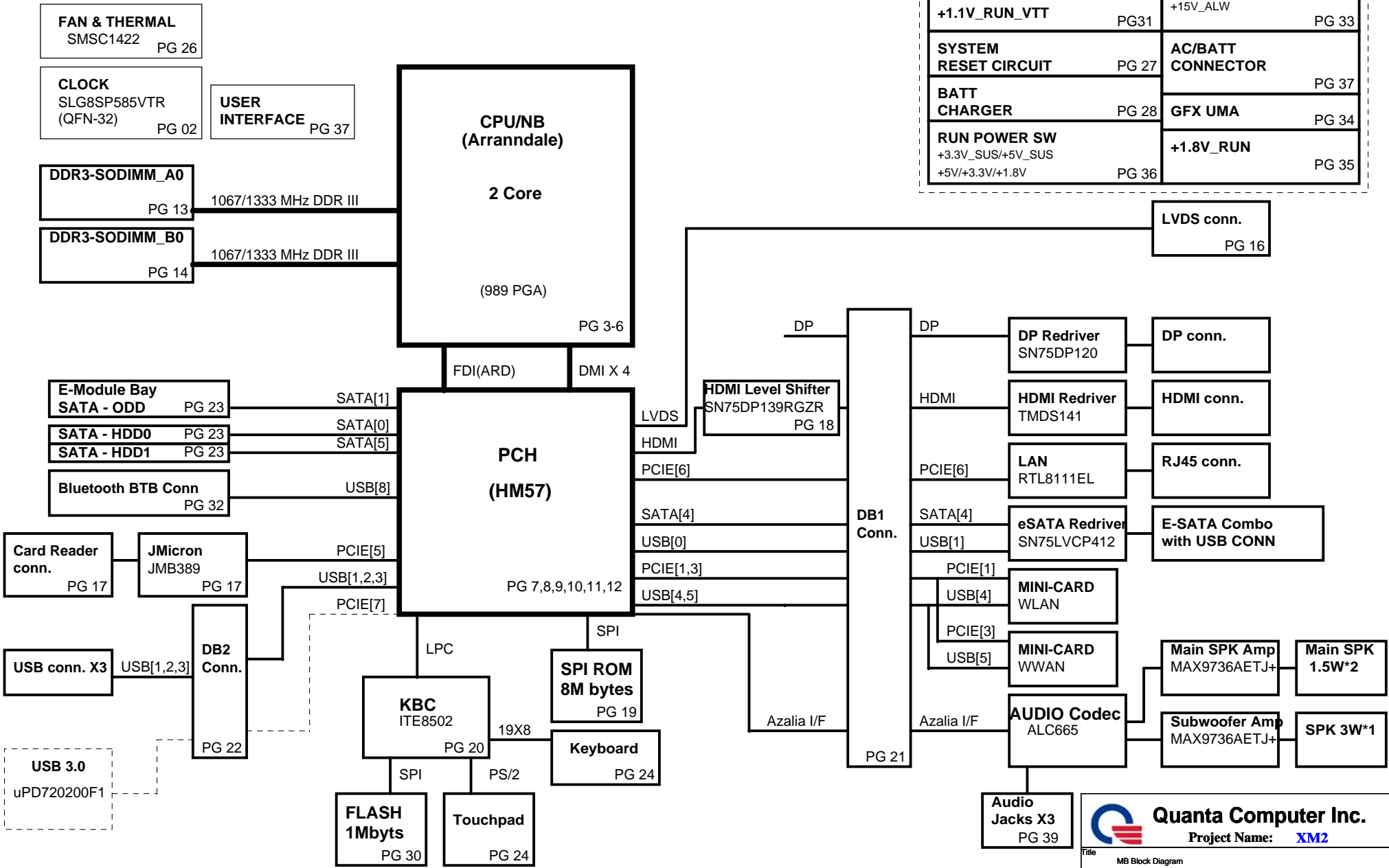


System Block Diagram of GM7



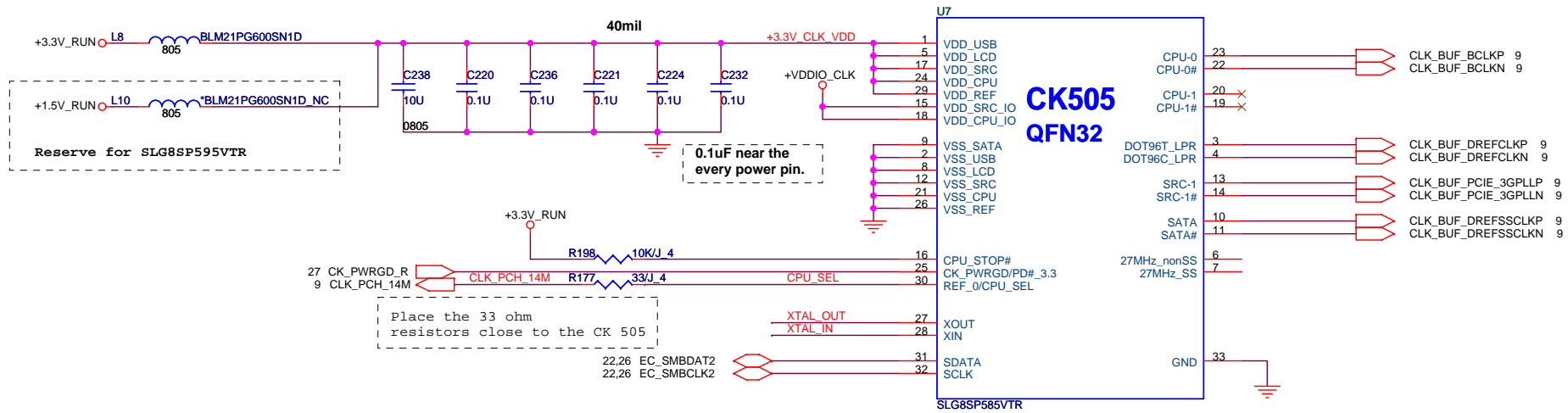
POWER	
REGULATOR +1.5V_SUS/+0.75V_DDR_VTT	PG 30
+1.05V_RUN	PG 32
+1.1V_RUN_VTT	PG31
SYSTEM RESET CIRCUIT	PG 27
BATT CHARGER	PG 28
RUN POWER SW +3.3V_SUS/+5V_SUS +5V/+3.3V/+1.8V	PG 36
CPU VCORE	PG 29
DC/DC +3.3V_ALW/+5V_ALW/ +15V_ALW	PG 33
AC/BATT CONNECTOR	PG 37
GFX UMA	PG 34
+1.8V_RUN	PG 35

Quanta Computer Inc.
Project Name: **XM2**

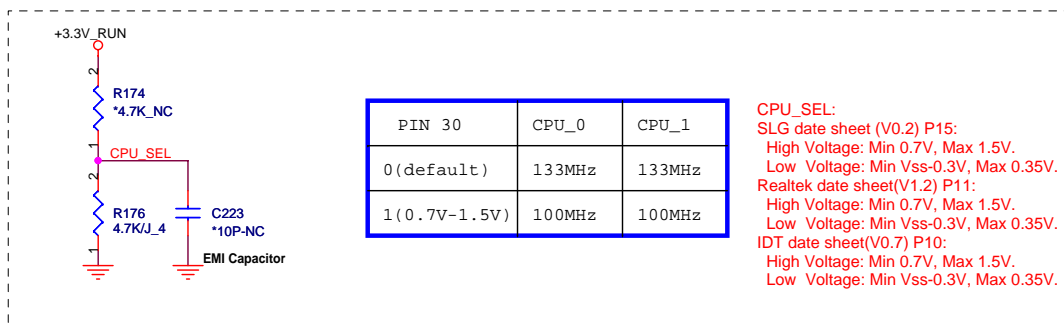
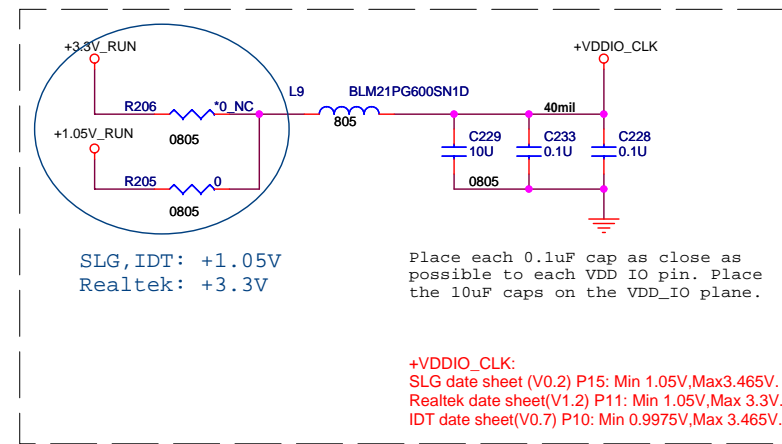
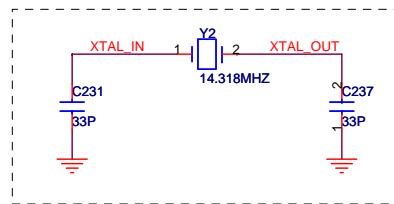
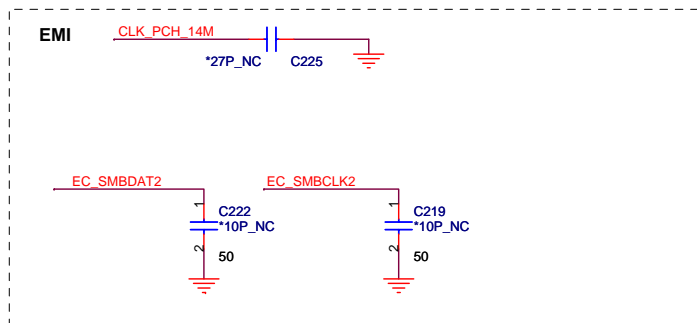
Title: MB Block Diagram

Size: Document Number: XM2_MB Rev D

Date: Friday, January 15, 2010 Sheet 1 of 40



Realtek: 0.1uFx3pcs, 22uFx1pcs
 IDT: 0.1uFx2pcs, 10uFx1pcs

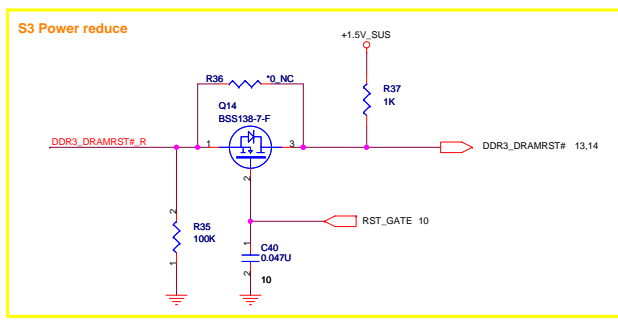
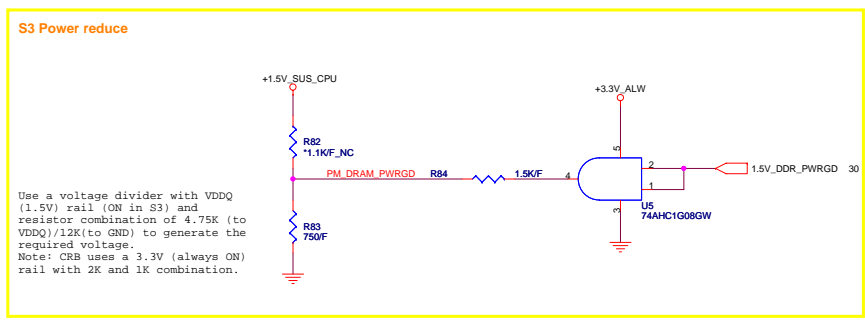
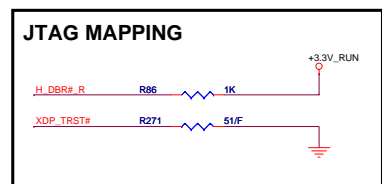
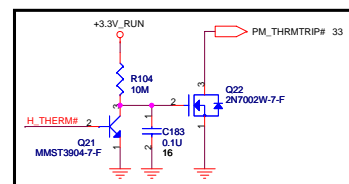
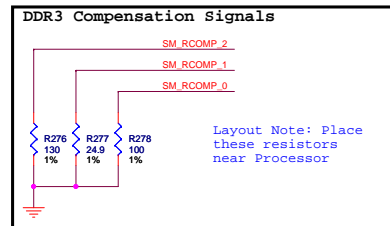
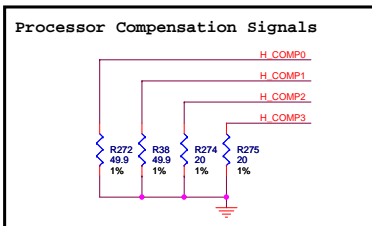
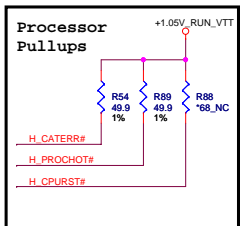
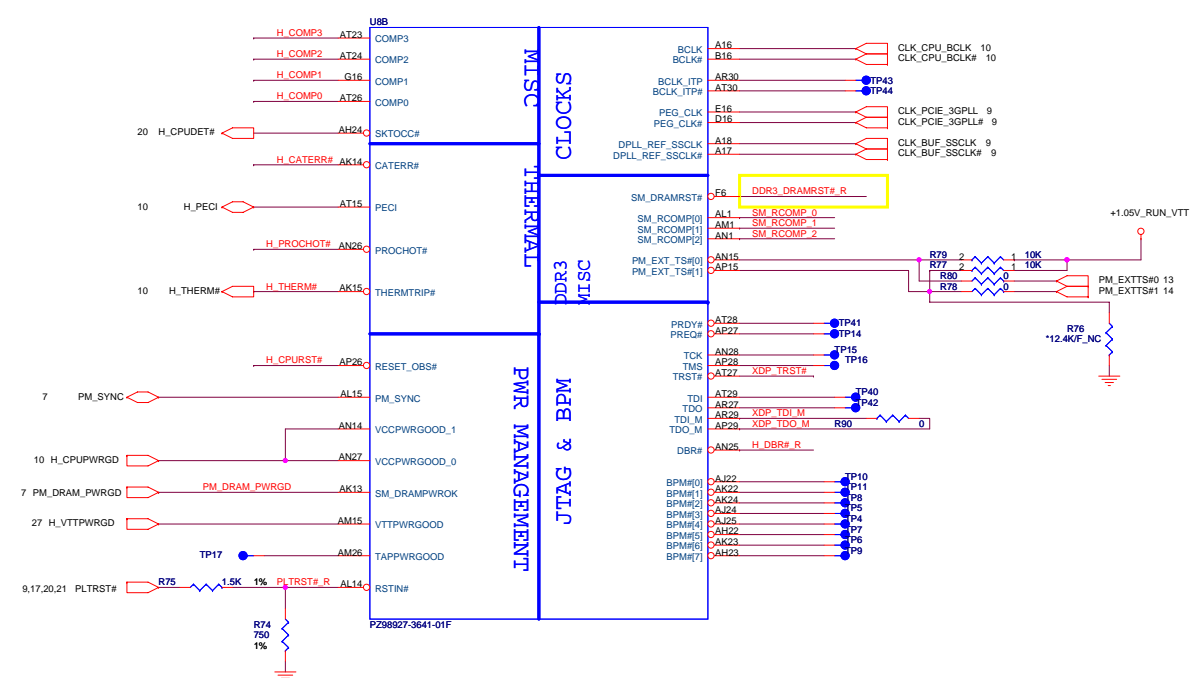
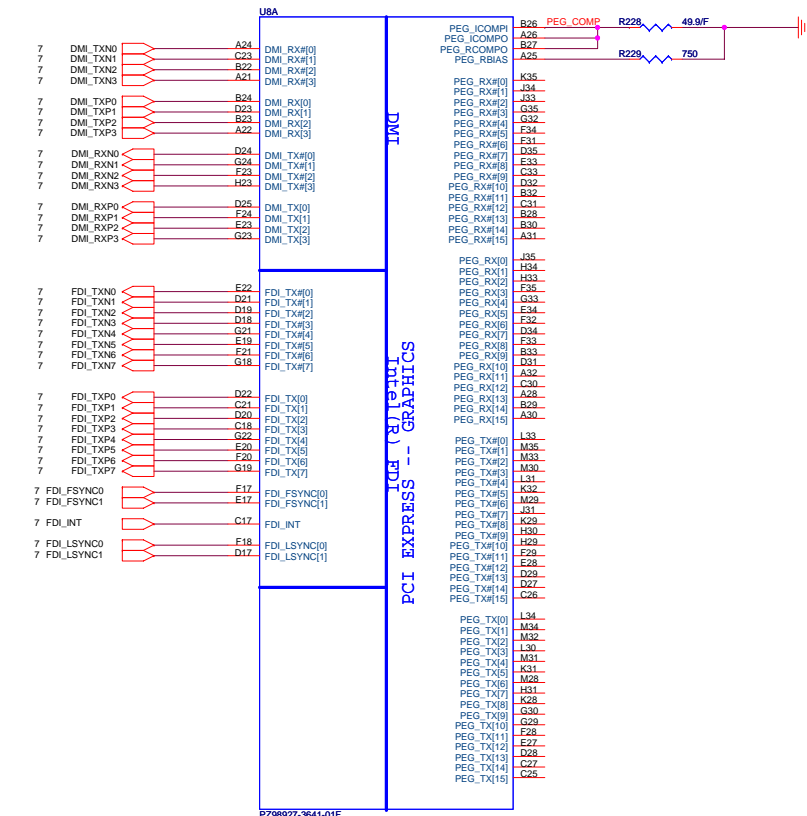


Quanta Computer Inc.
 Project Name: **GM7B**

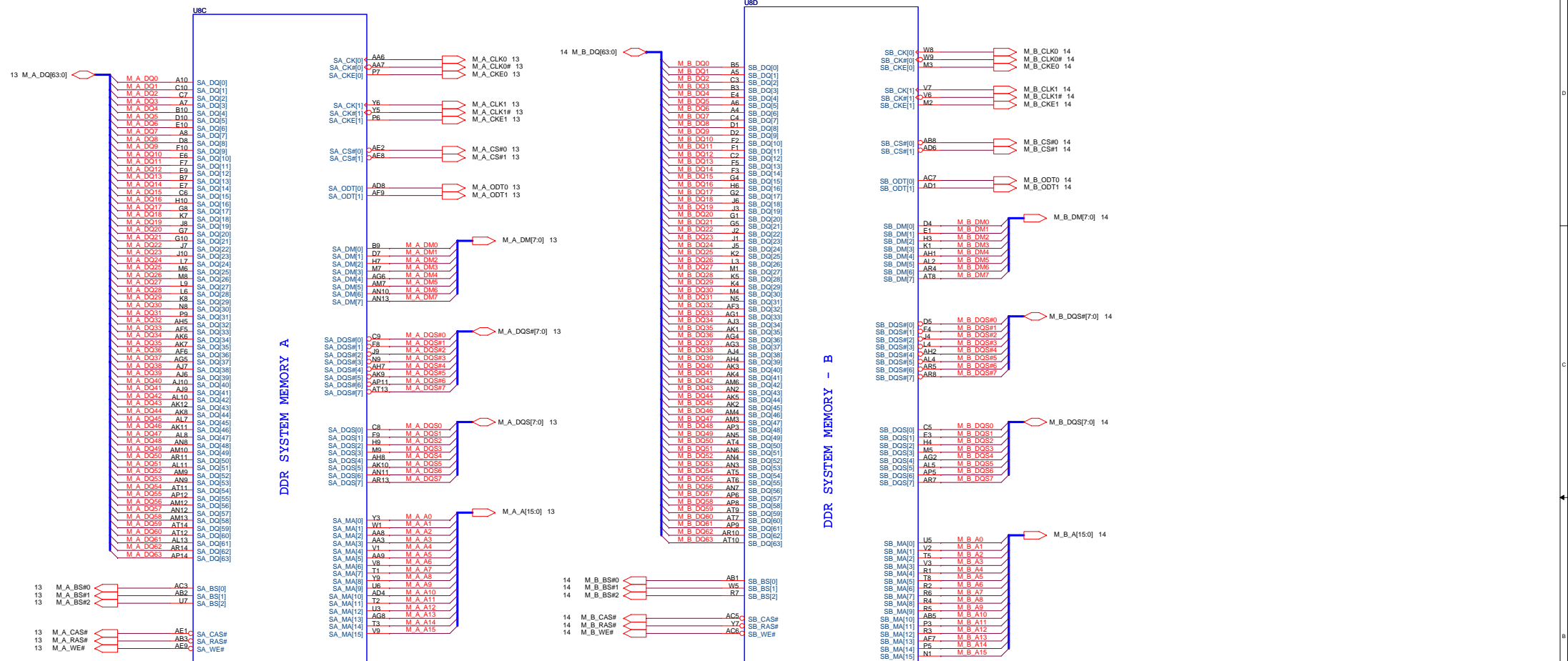
Title: Clock Gen

Size: Document Number GM7B Rev D

Date: Friday, January 15, 2010 Sheet 2 of 40



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

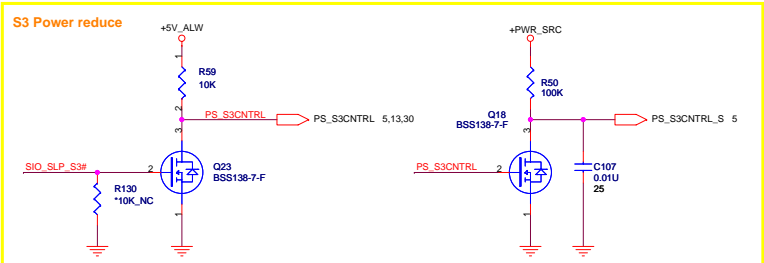
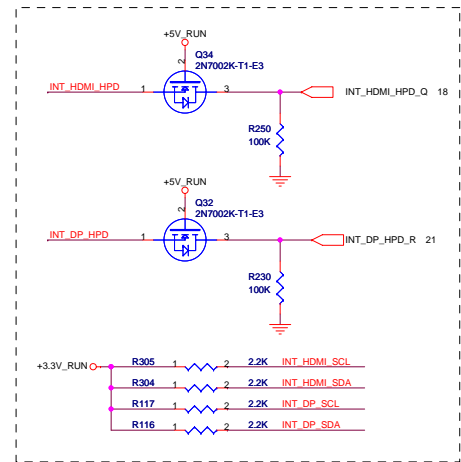
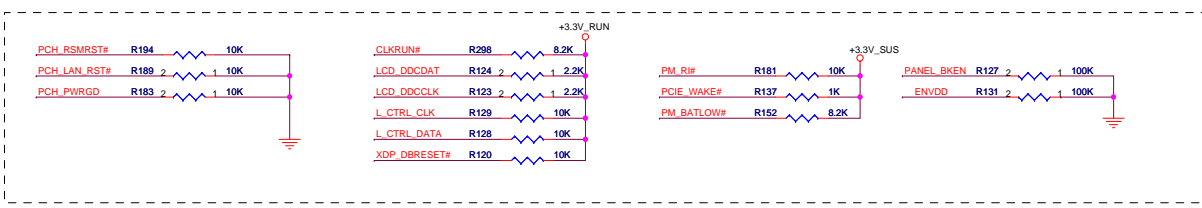
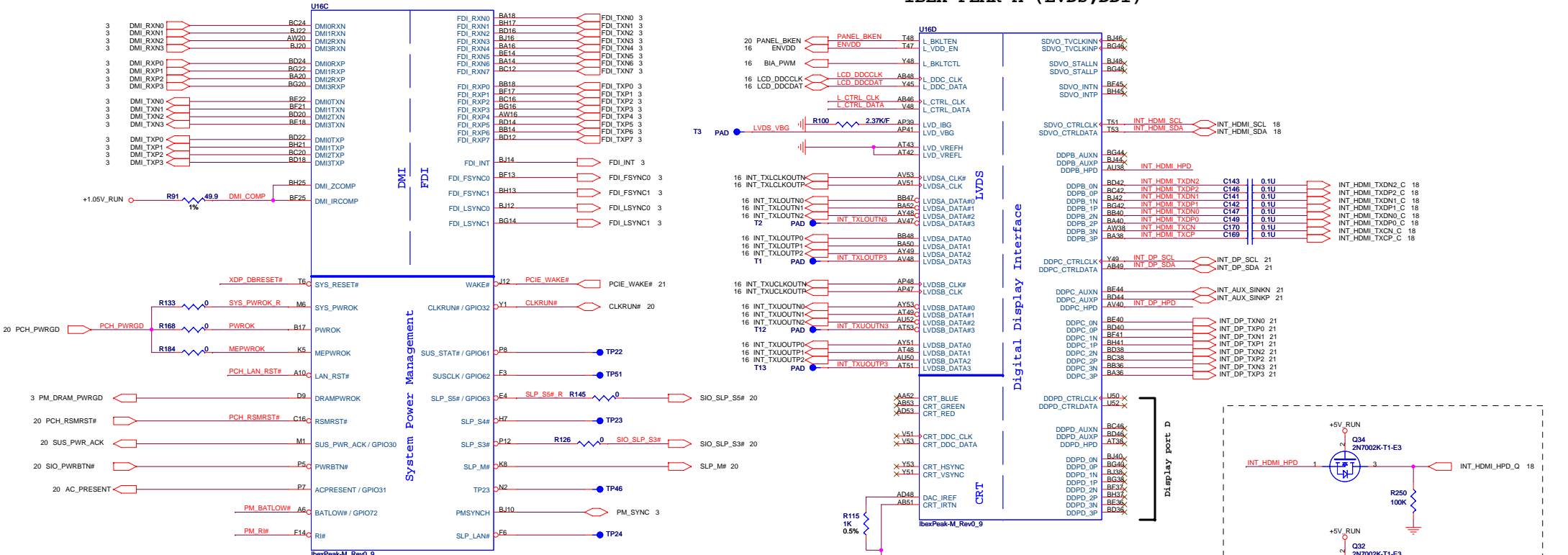


P298927-3641-01F

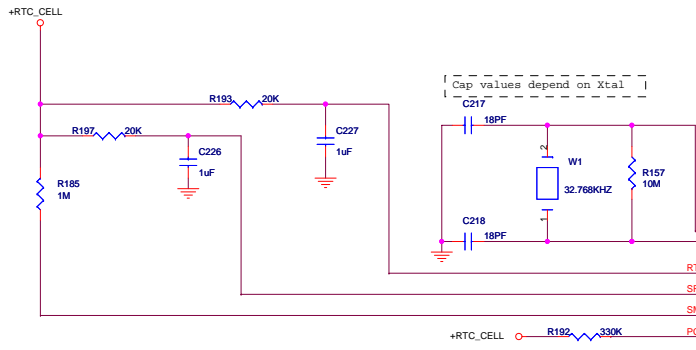
P298927-3641-01F

IBEX PEAK-M (DMI, FDI, GPIO)

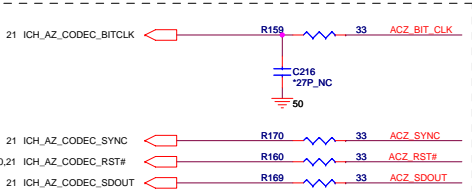
IBEX PEAK-M (LVDS, DDI)



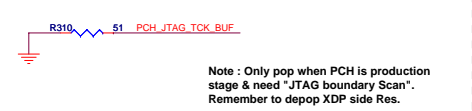
IBEX PEAK-M (HDA, JTAG, SATA)



No Reboot Strap	
SPKR	Low=Default
	High=No Reboot

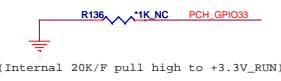


Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.



Note: Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

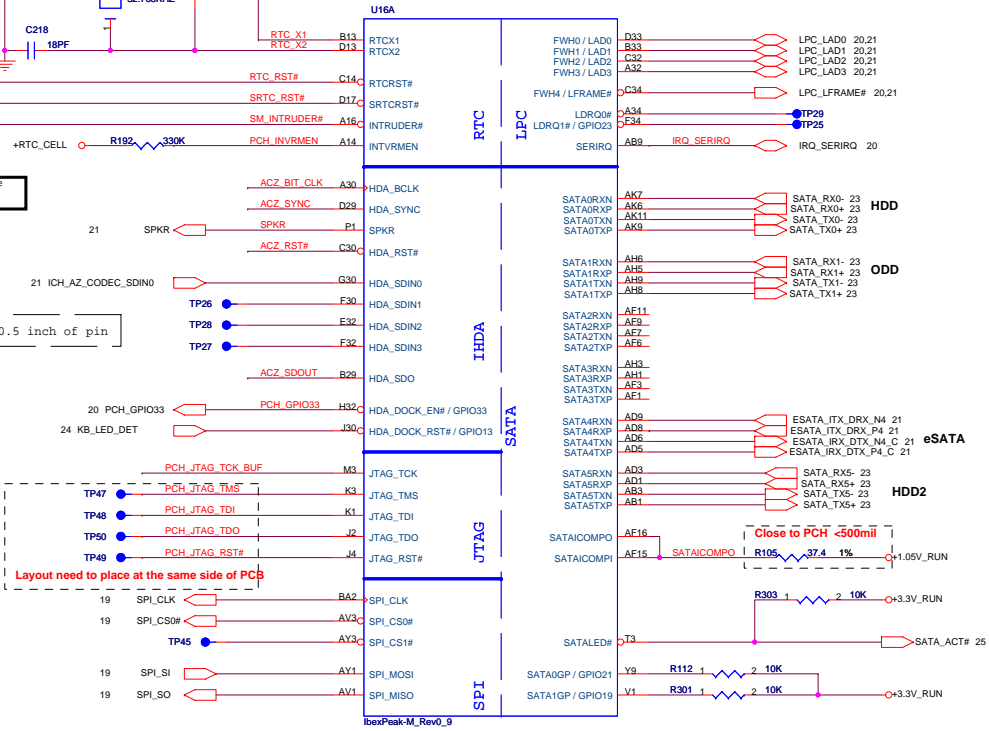
Flash Descriptor Security Override	
GPI033	Low = Enabled High = Disabled



Note: GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

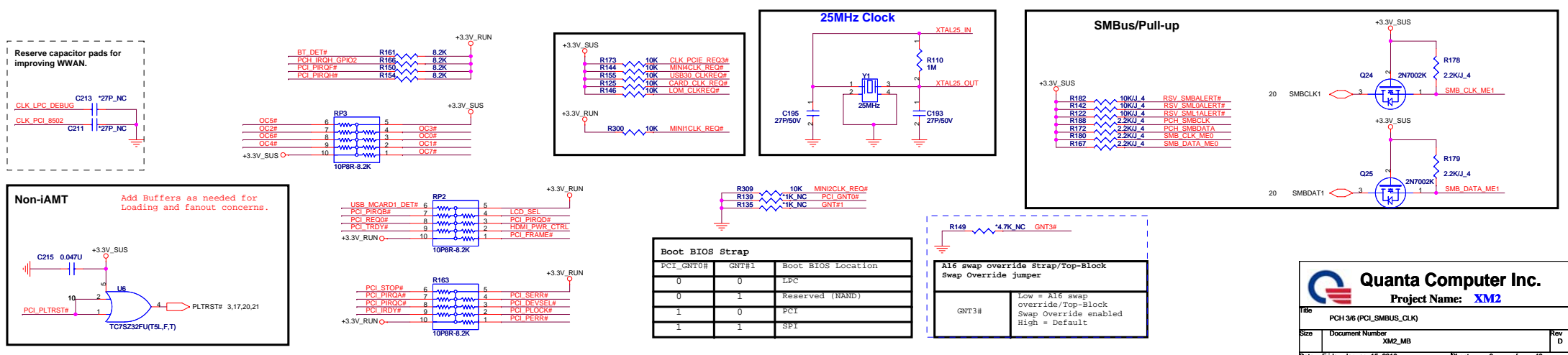
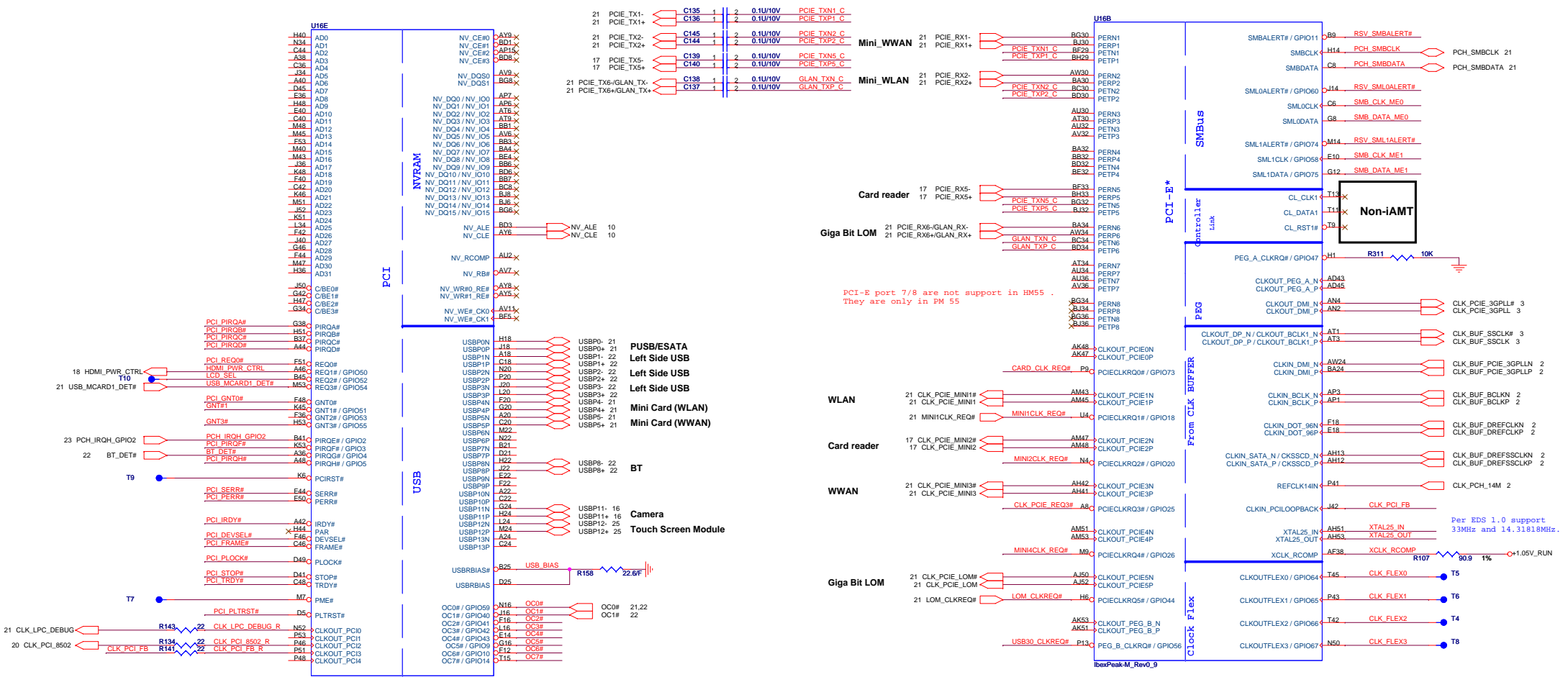
INVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

0 ohm resistor within 0.5 inch of pin



IBEX PEAK-M (PCI,USB,NVRAM)

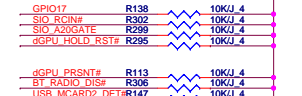
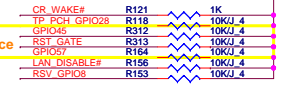
IBEX PEAK-M (PCI-E,SMBUS,CLK)



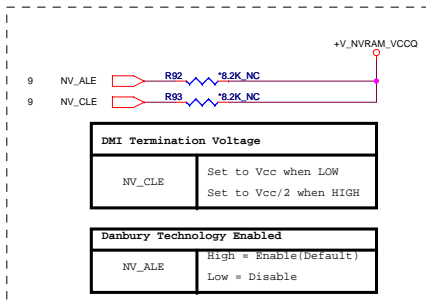
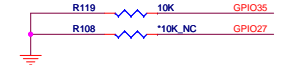
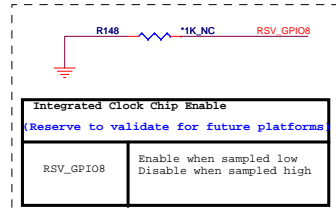
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

GPIO

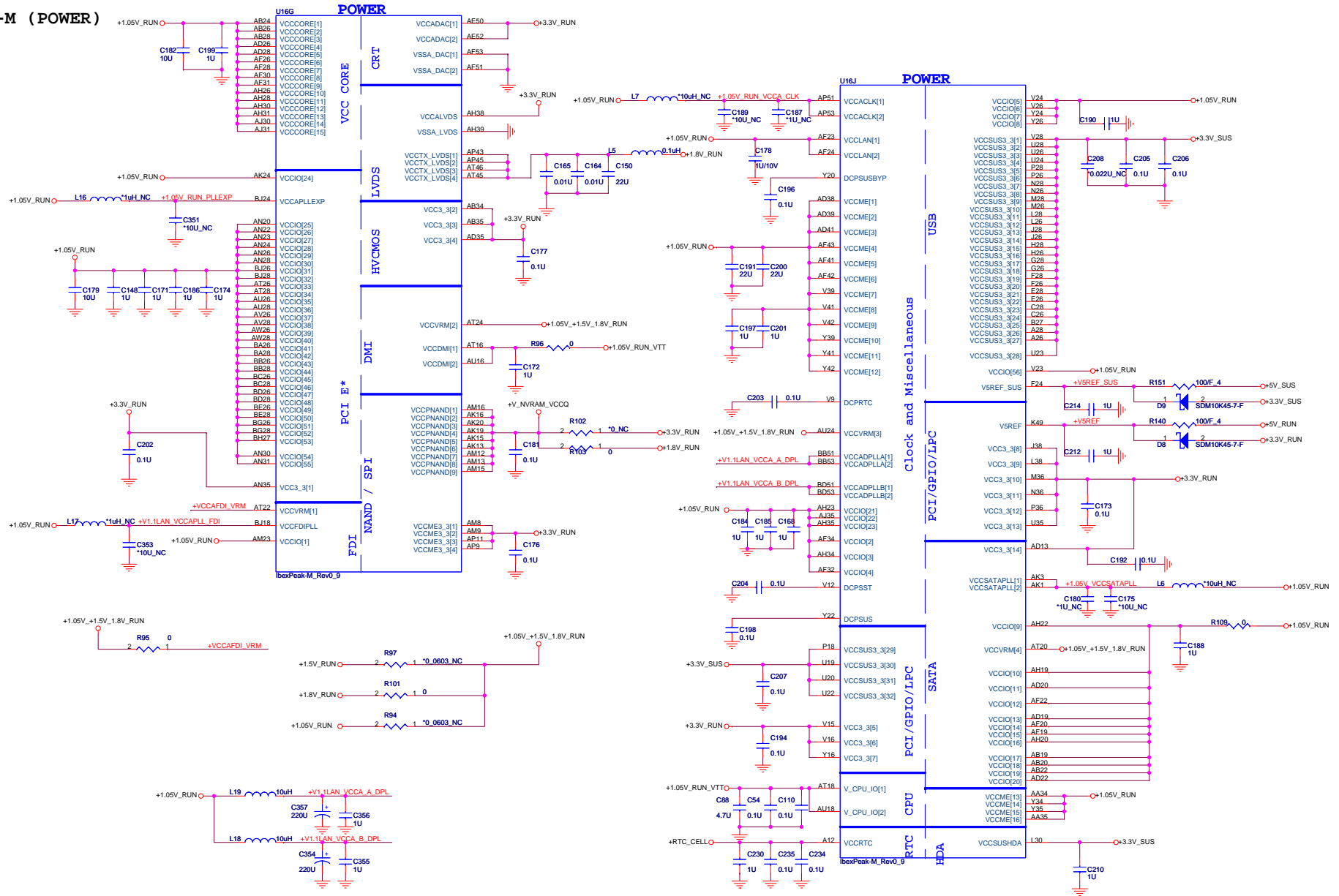
Pull-up/Pull-down



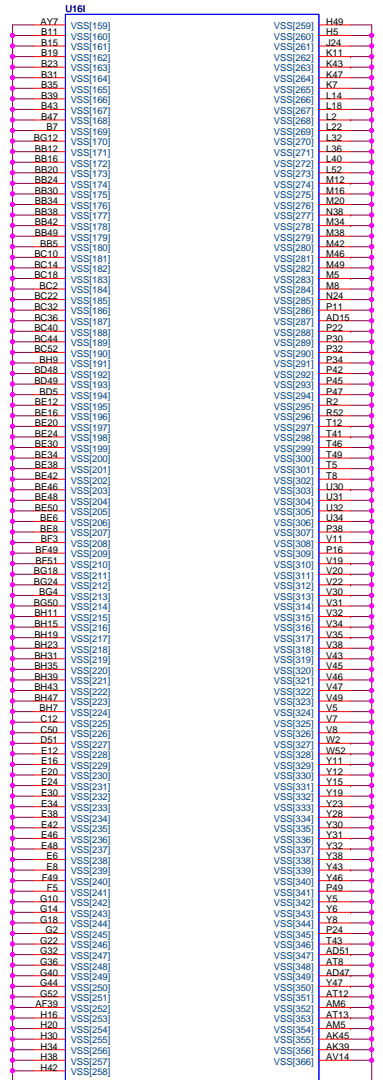
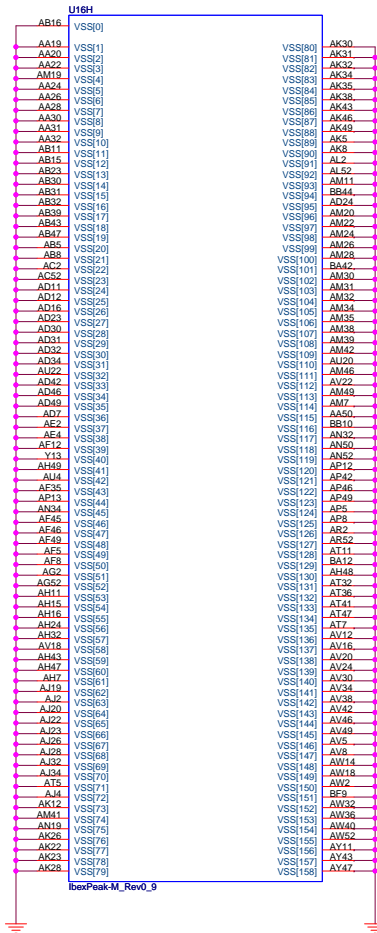
SV_SET_UP | 1-X High = Strong (Default)

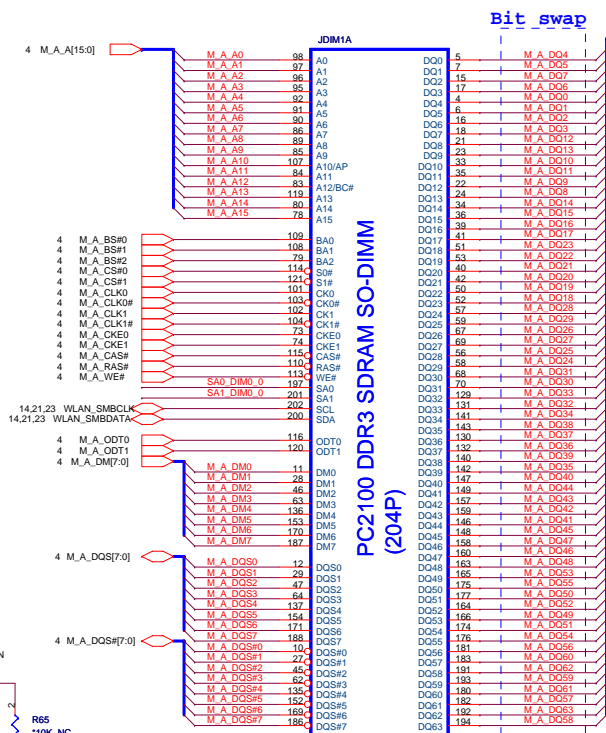


IBEX PEAK-M (POWER)

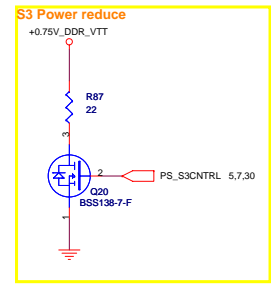
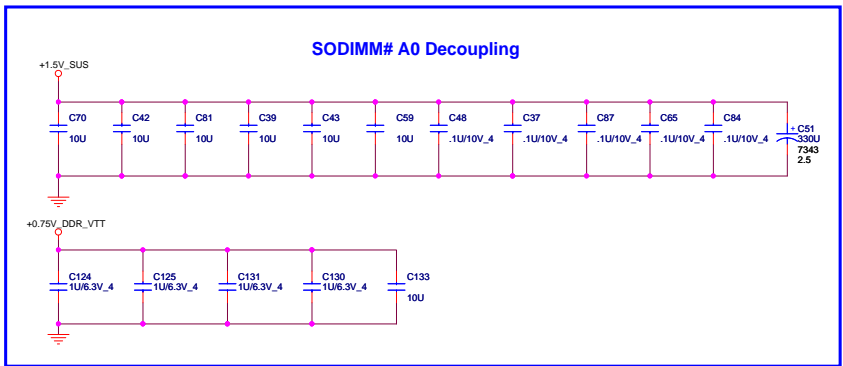
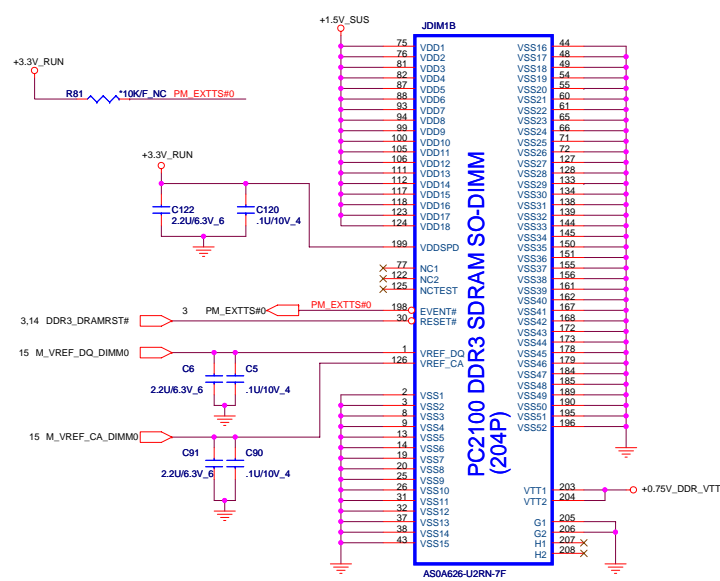


IBEX PEAK-M (GND)





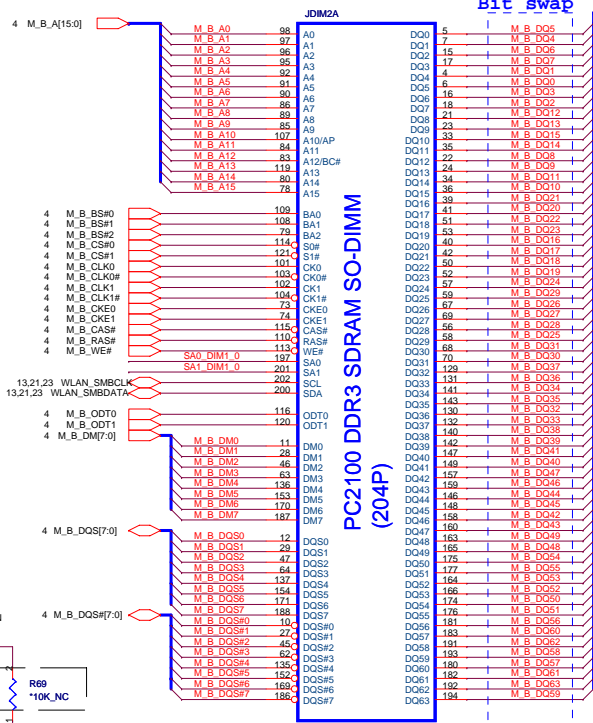
CHA_DIMM0_BOT_SIDE



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

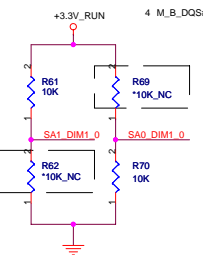
0105CT: Update JDIM4 footprint 5.2mm, STD type.



PC2100 DDR3 SDRAM SO-DIMM (204P)

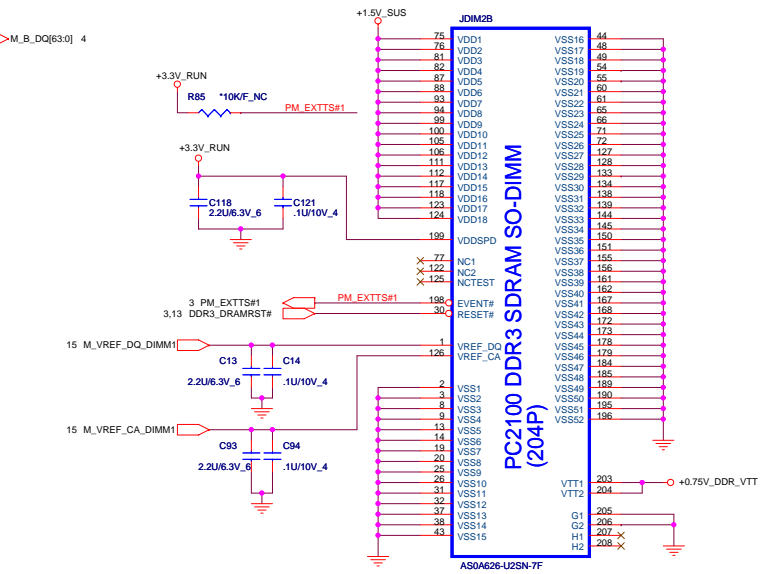
Bit swap

Bit swap

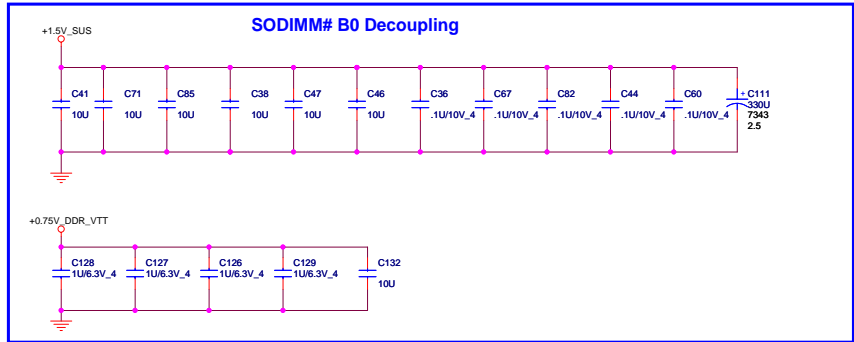


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

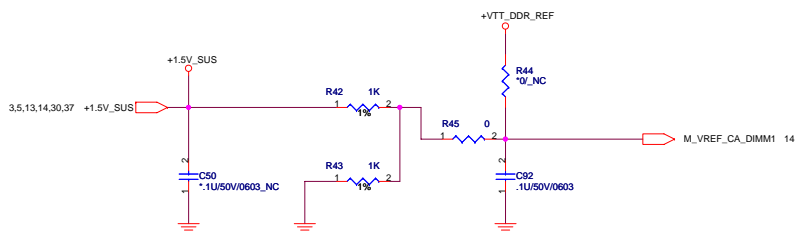
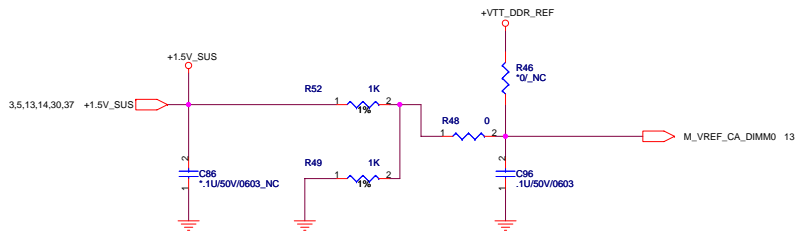
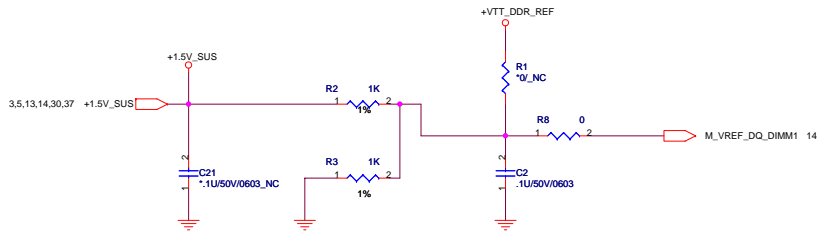
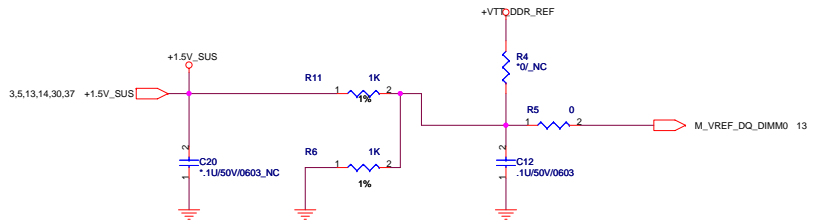
Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

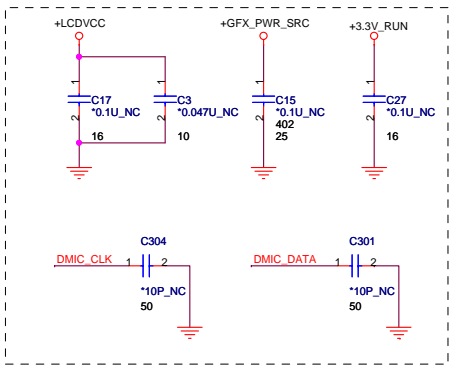
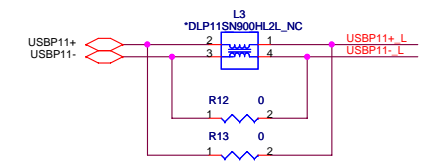
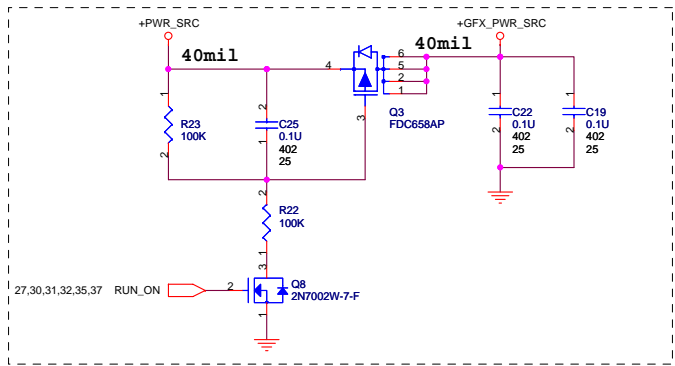
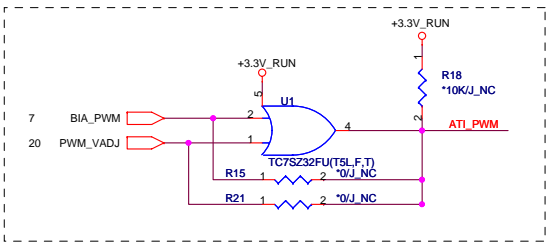
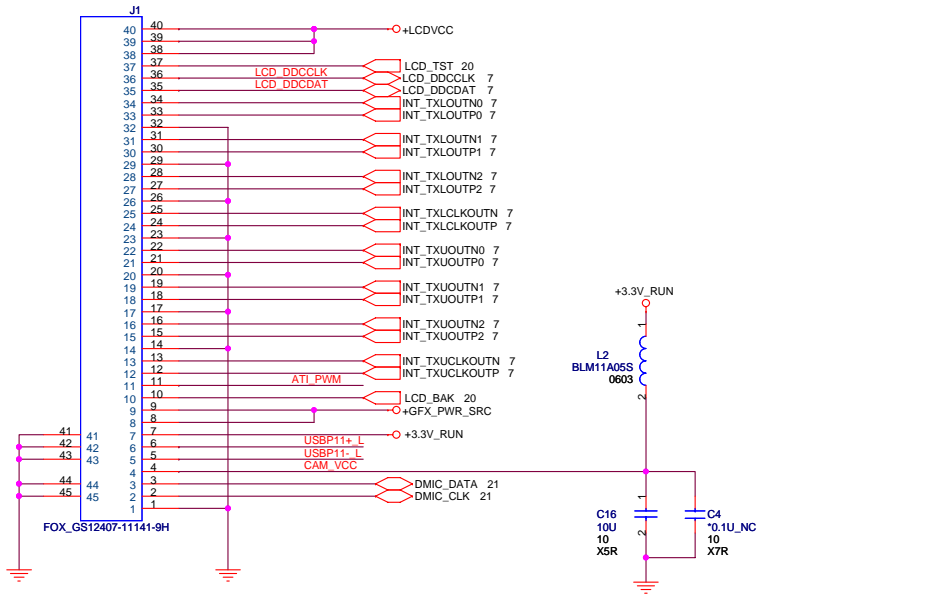
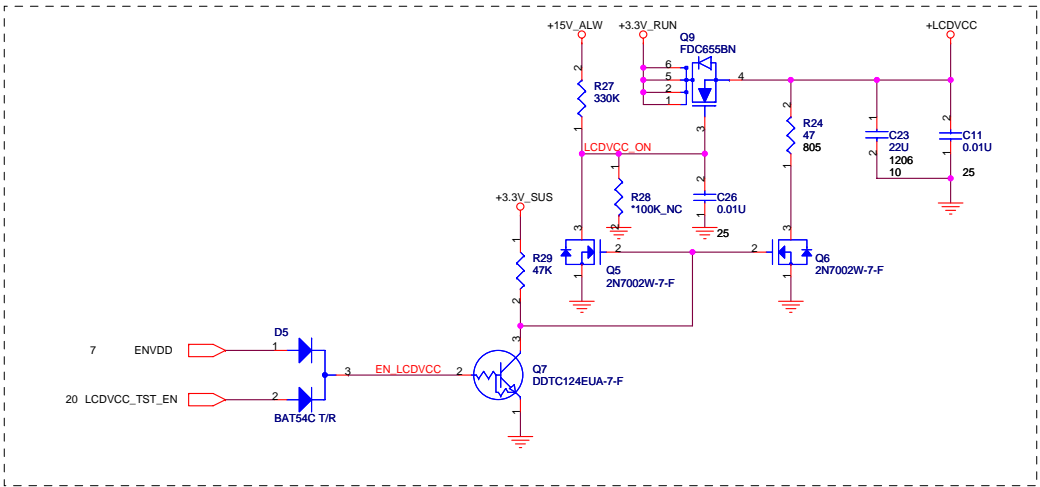


PC2100 DDR3 SDRAM SO-DIMM (204P)



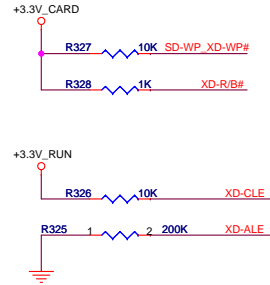
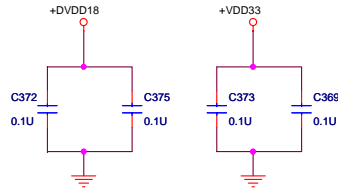
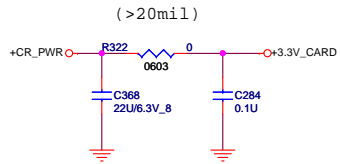
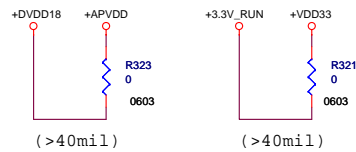
Fixed SO-DIMM VREF_DQ (M1): Default



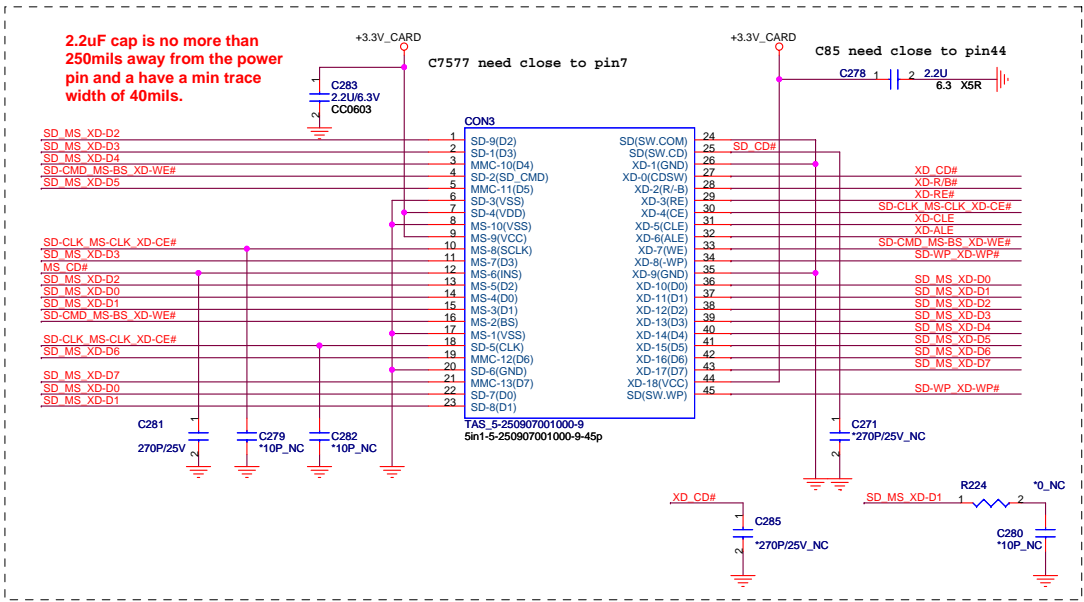
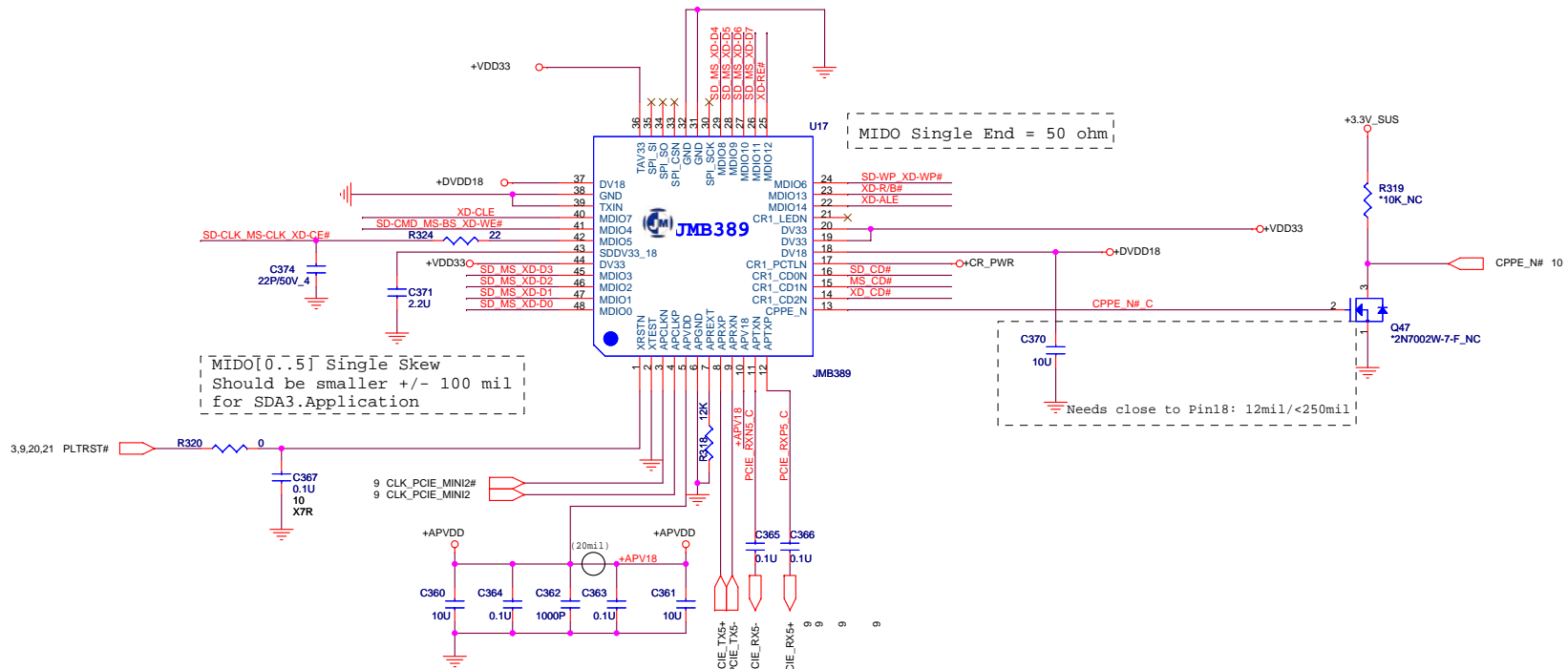


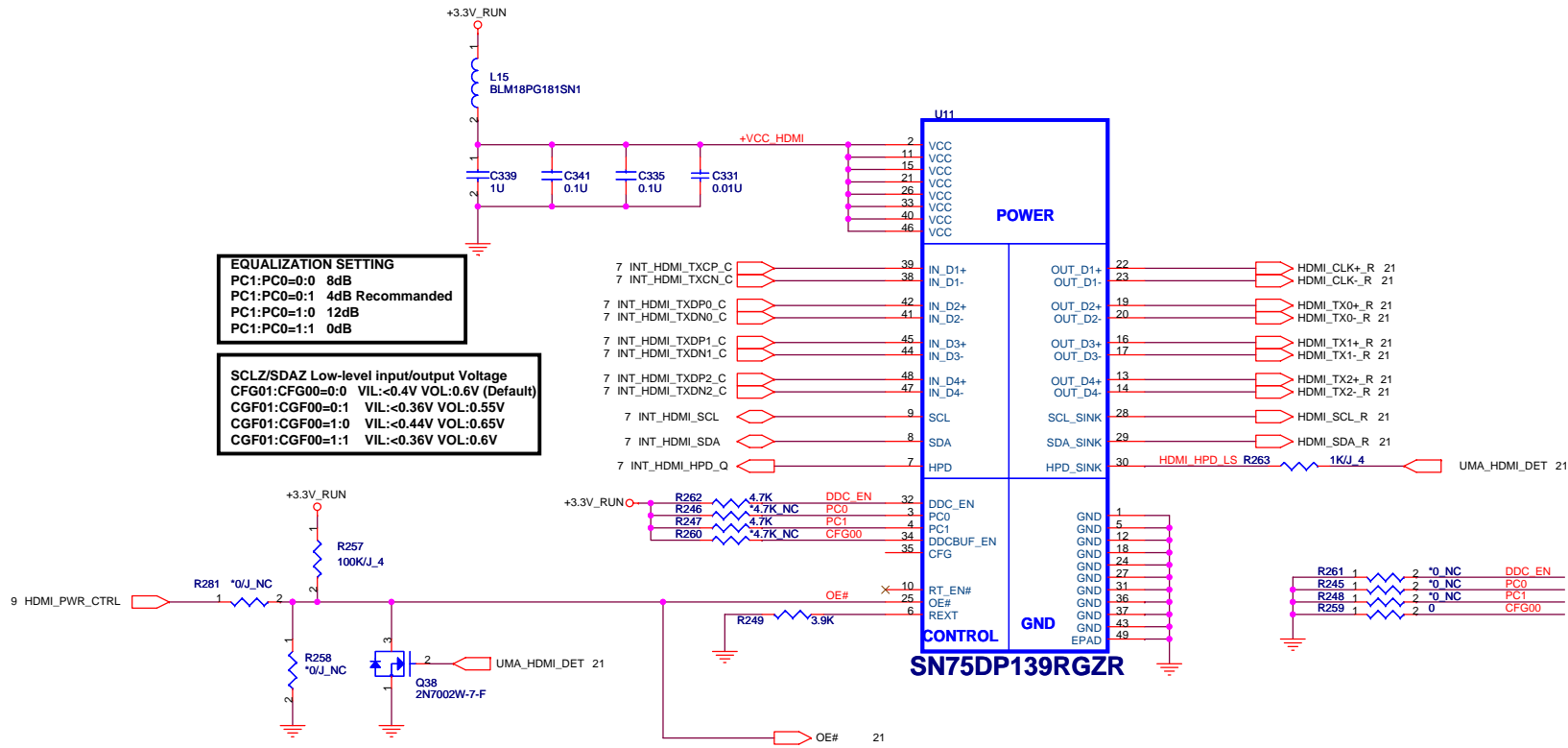
Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WE#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/#
MDIO14				XD_AL#
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#




MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3.Application





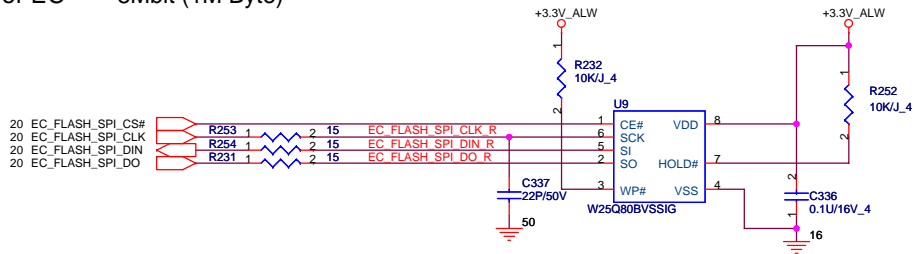
EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCL/SDA Low-level input/output Voltage
 CFG01:CFG00=0:0 VIL:<-0.4V VOL:0.6V (Default)
 CGF01:CGF00=0:1 VIL:<-0.36V VOL:0.55V
 CGF01:CGF00=1:0 VIL:<-0.44V VOL:0.65V
 CGF01:CGF00=1:1 VIL:<-0.36V VOL:0.6V

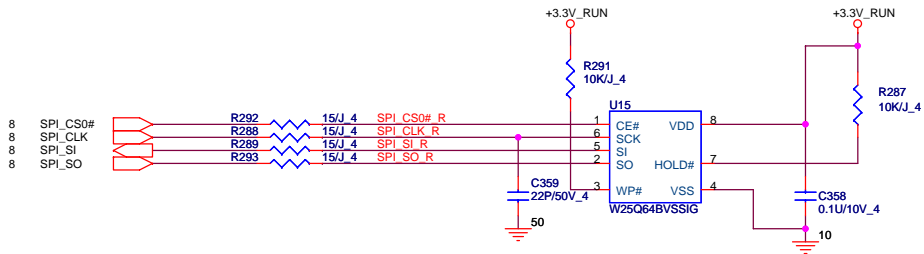

Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
	HDMI CONN	1A
Date:	Friday, January 15, 2010	Sheet 18 of 40

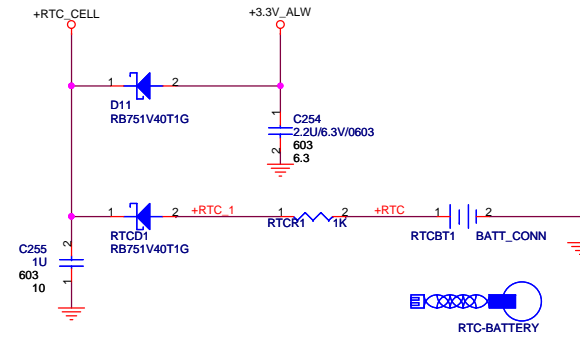
For EC 8Mbit (1M Byte)



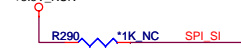
For PCH 64Mbit (8M Byte), SPI



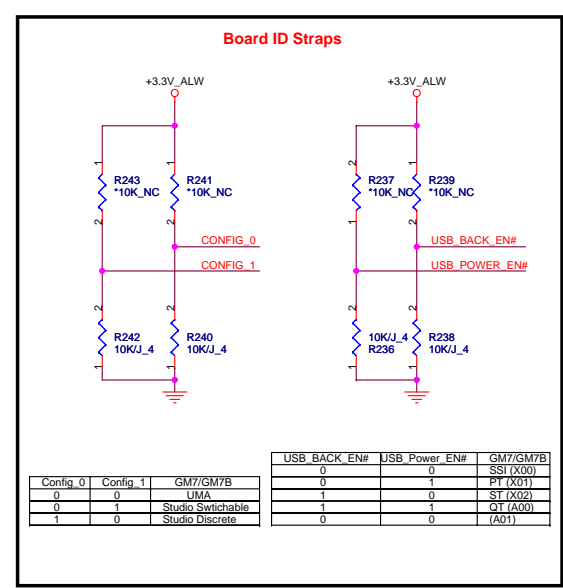
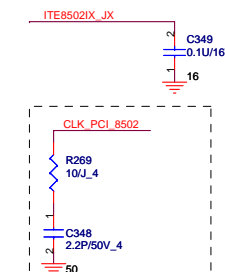
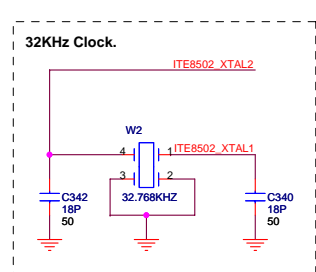
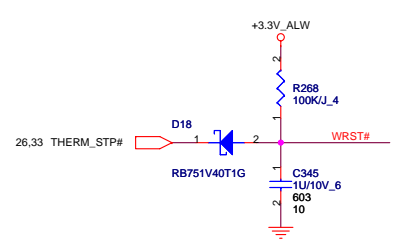
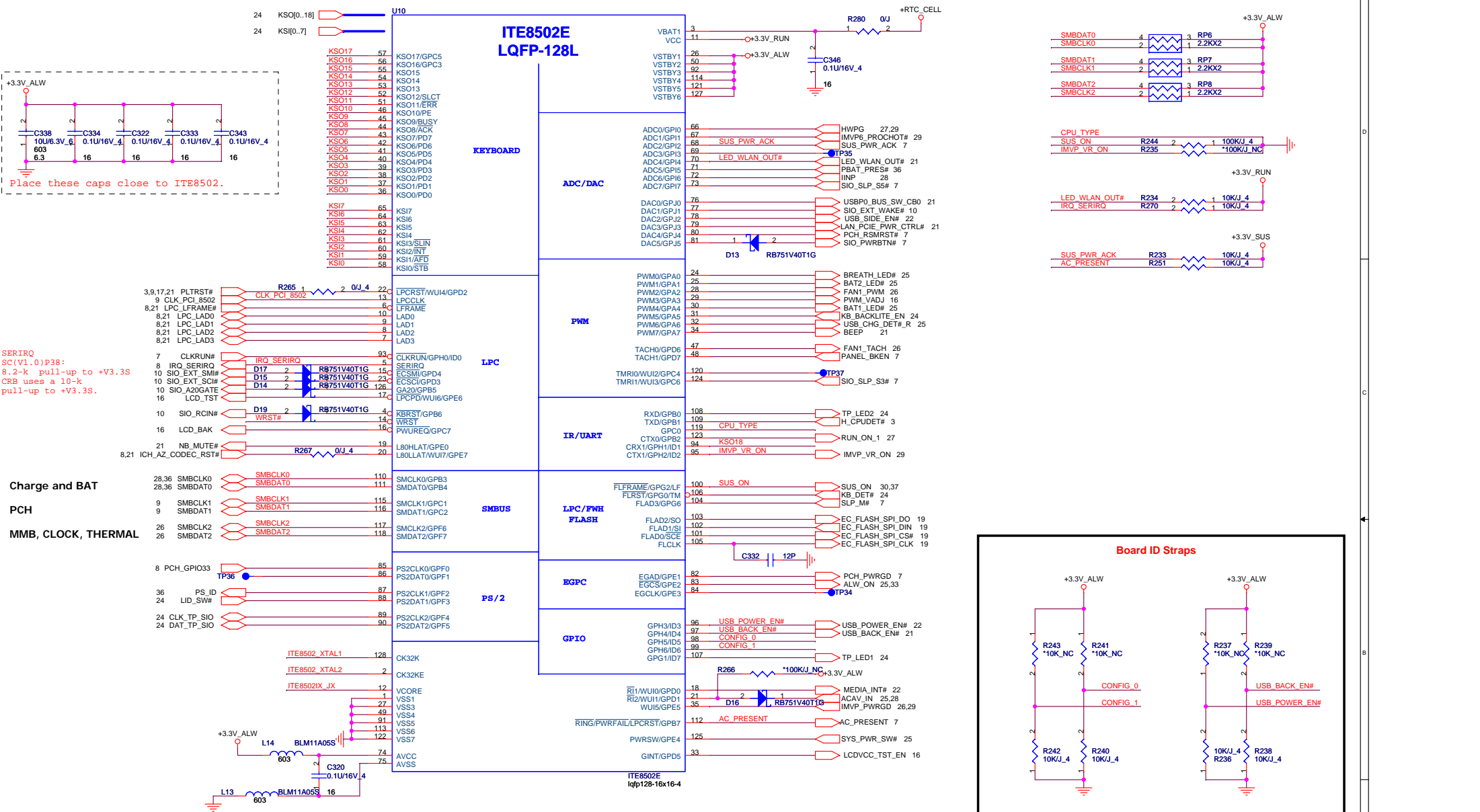
RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)



Config 0	Config 1	GM7/GM7B	USB_BACK_EN#	USB Power EN#	GM7/GM7B
0	0	UMA	0	0	SSI (X00)
0	1	Studio Switchable	1	1	PT (X01)
1	0	Studio Discrete	0	0	ST (X02)
			0	1	QT (X00)
			0	0	(A01)

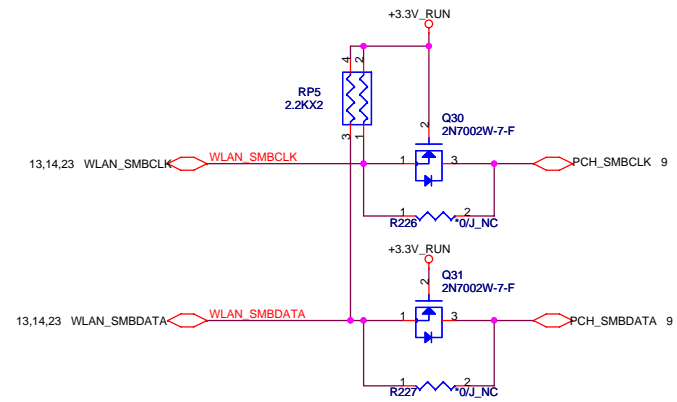
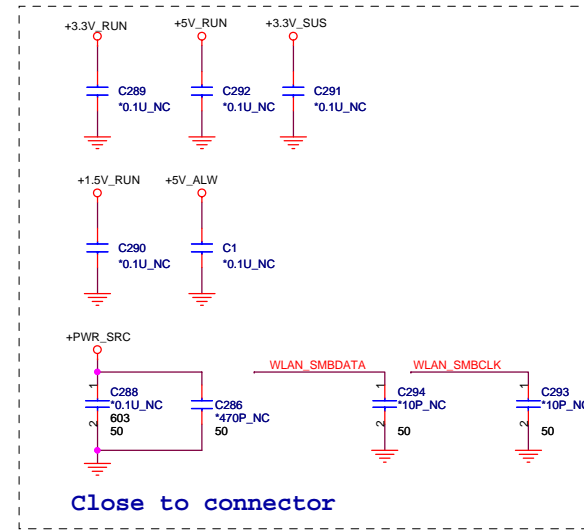
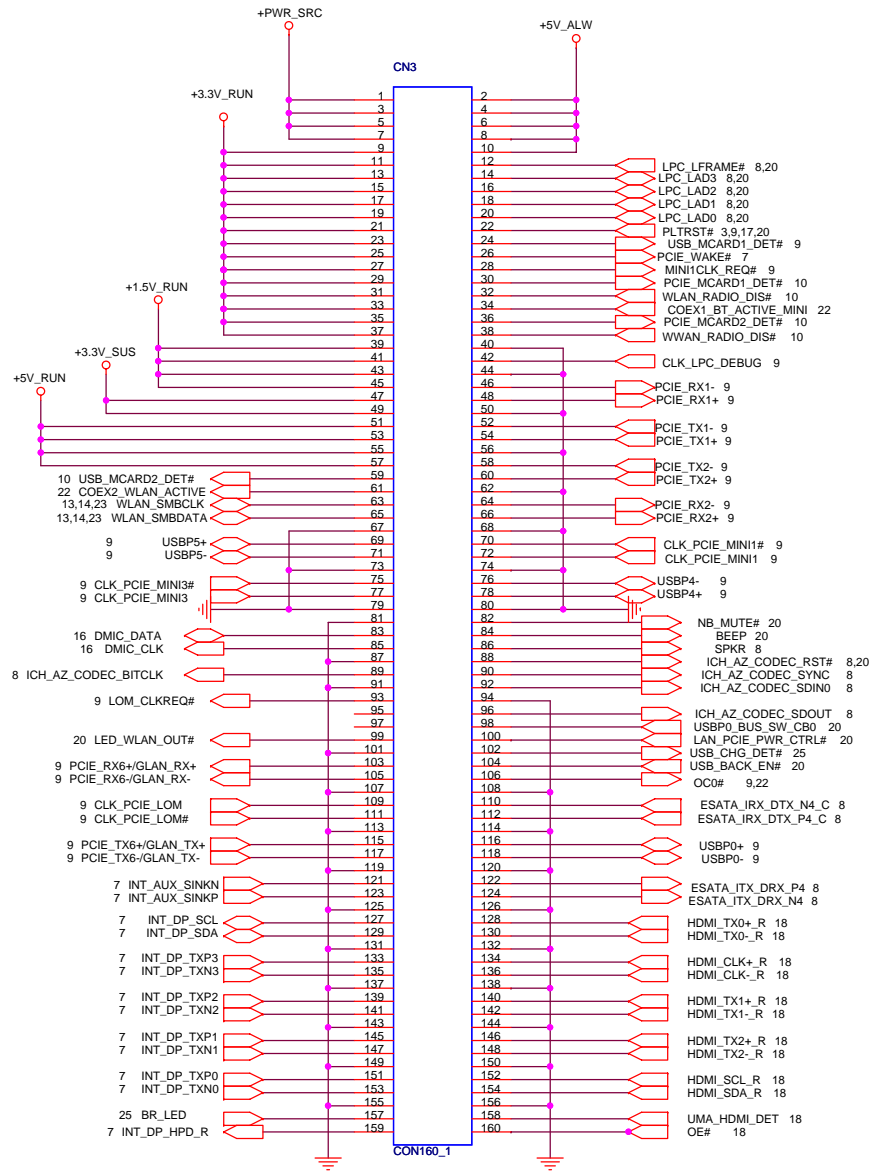
Quanta Computer Inc.

Project Name: **XM2**

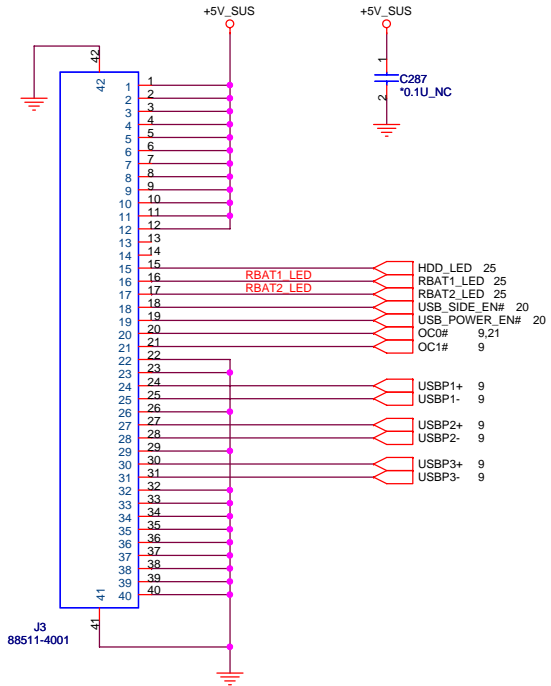
Title: CoverPage

Size: Document Number XM2_MB Rev D

Date: Friday, January 15, 2010 Sheet 20 of 40

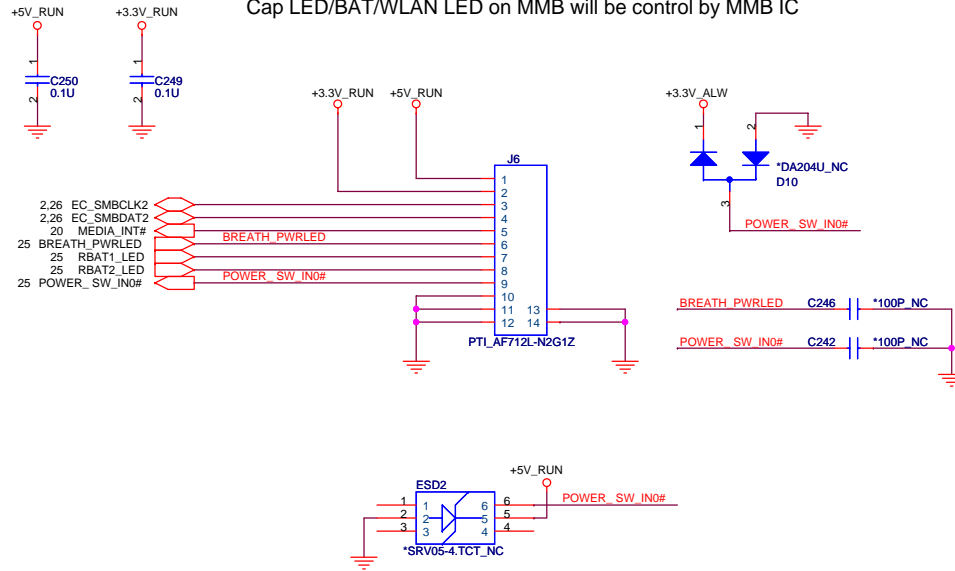


USB IO 40 pins

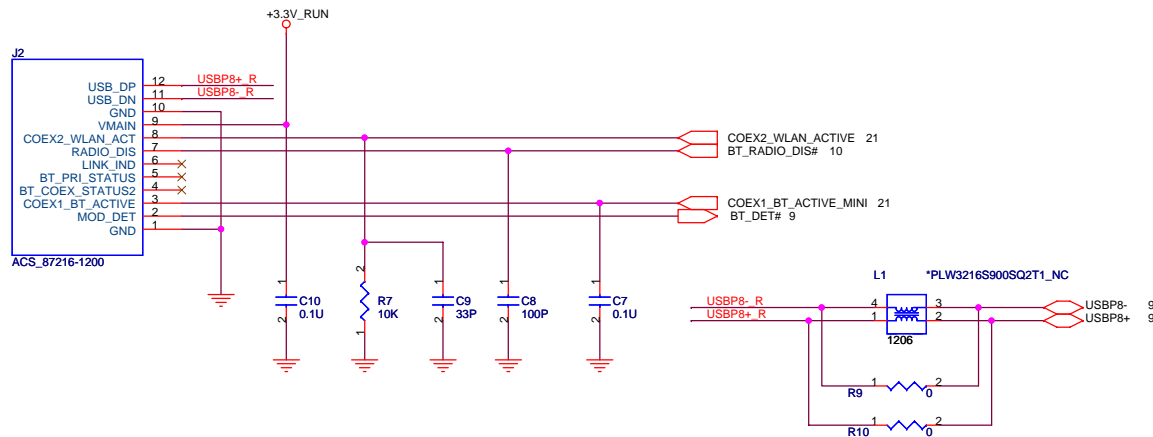


MMB & Power Board 12pins

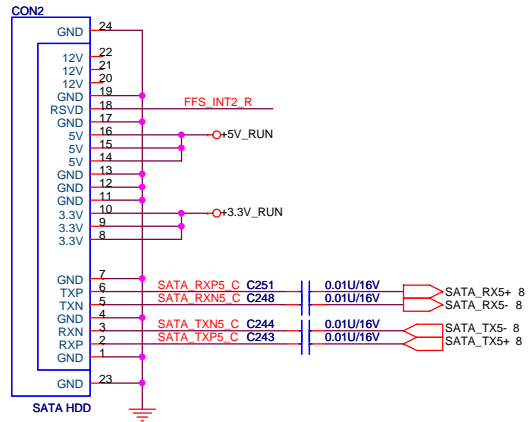
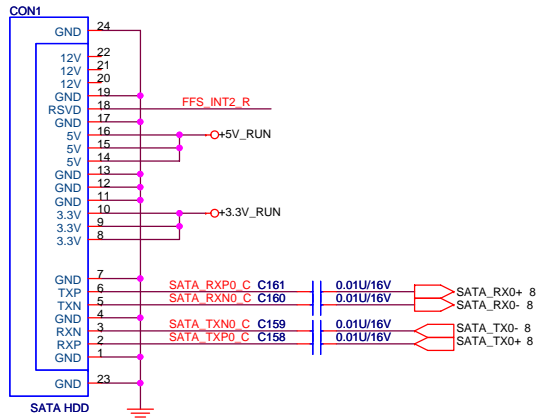
Cap LED/BAT/WLAN LED on MMB will be control by MMB IC



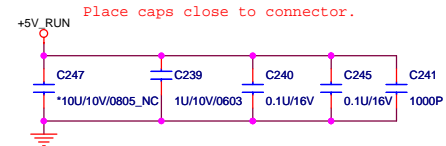
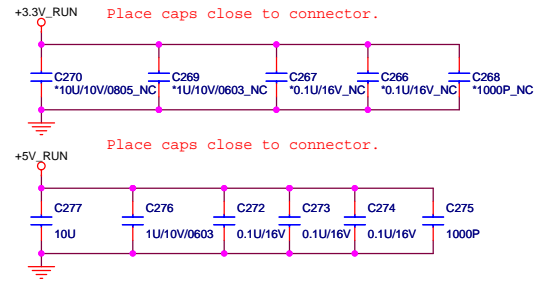
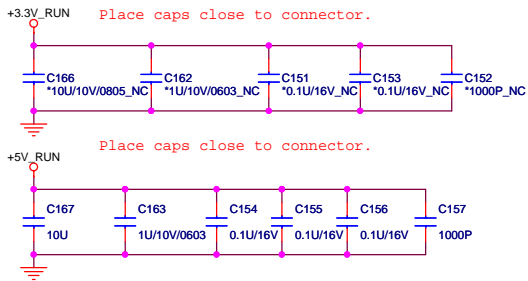
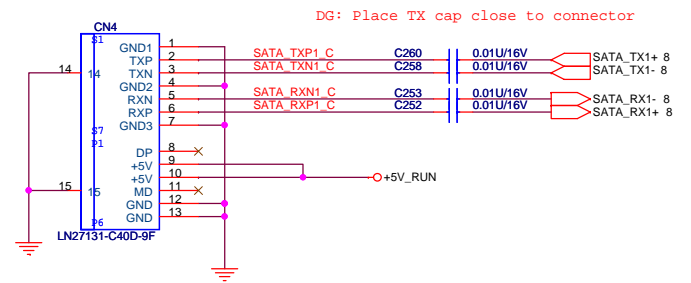
Support Dell BT3xx series module Bluetooth WTB Conn



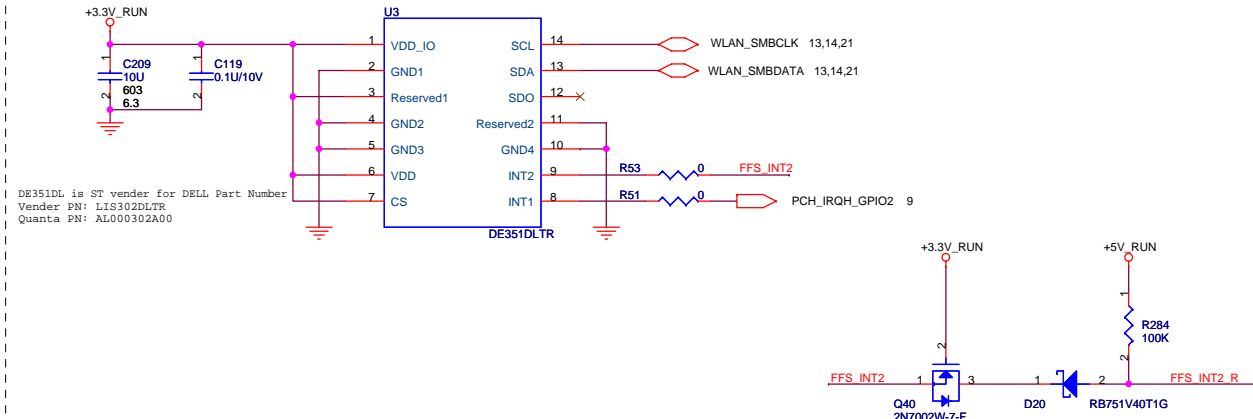
SATA Connector.



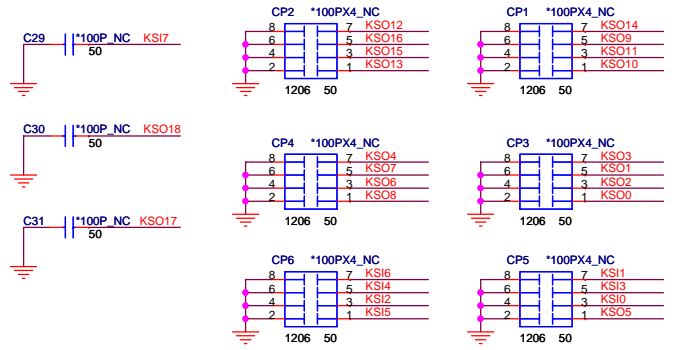
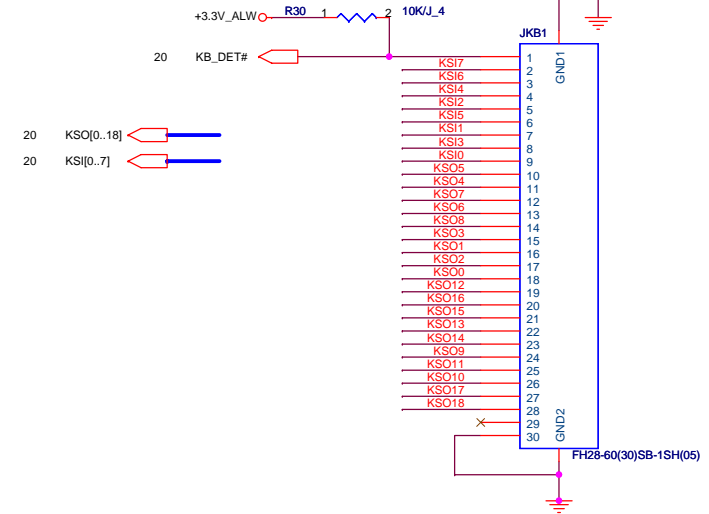
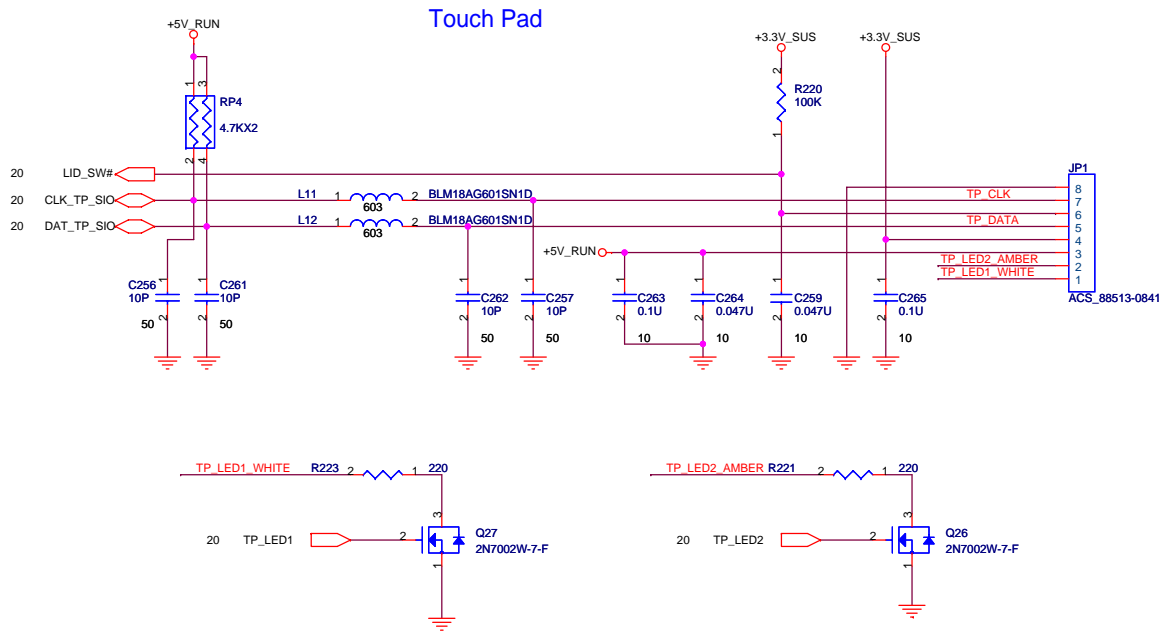
ODD Connector



3-axis Fall Sensor (HDD data protector)



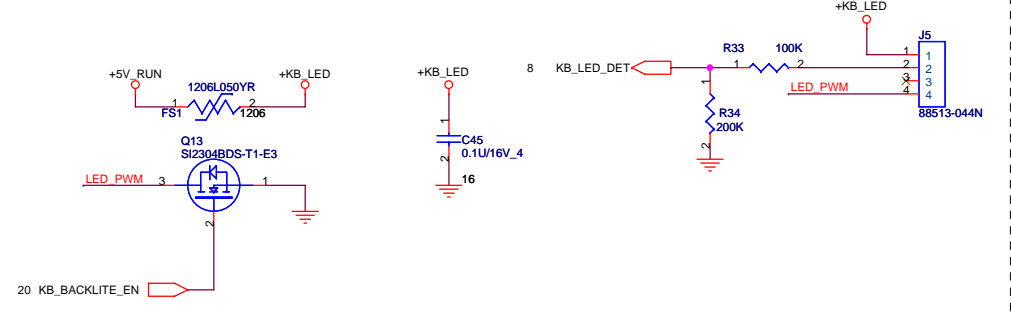
KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

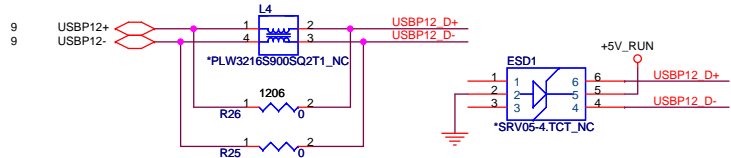
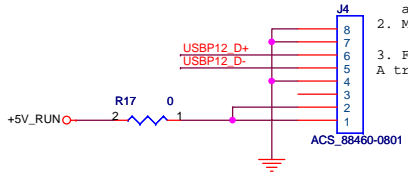
Key board illumination

+KB_LED power trace width >10 mil

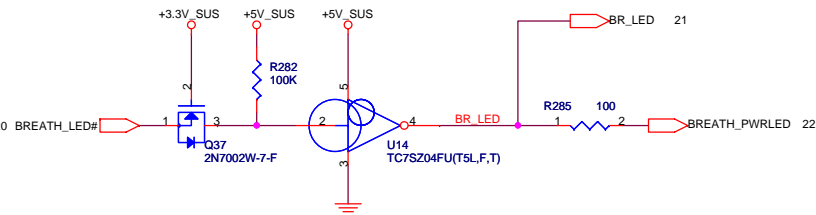
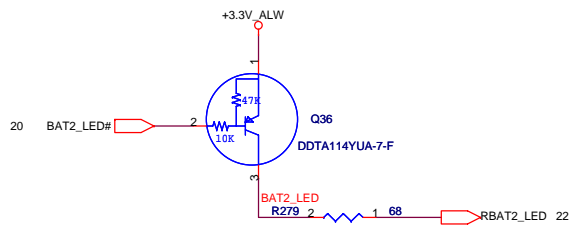
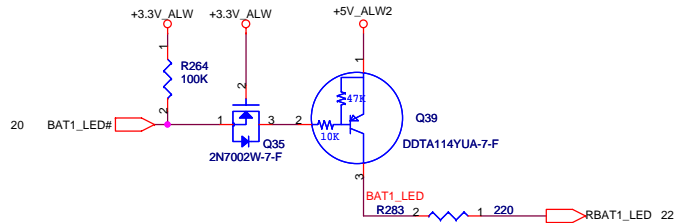


Touch Screen Module

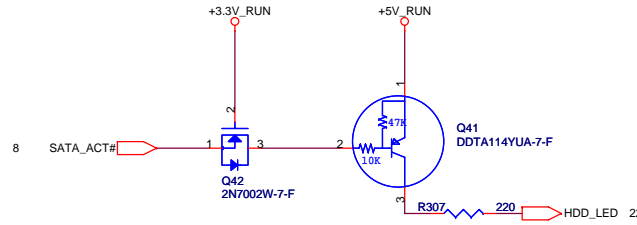
- Note:
- VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 - Maximum cable resistance on VCC, GND should be 150m ohm.
 - FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



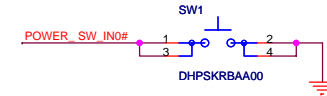
Battery status.



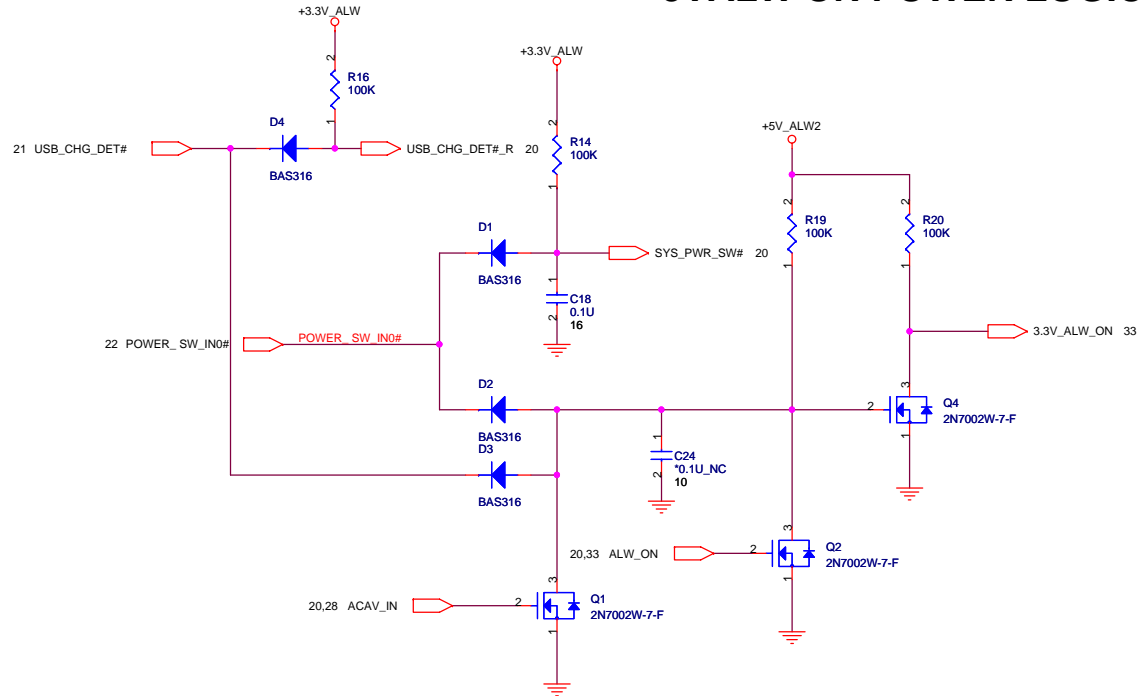
HDD activity LED.

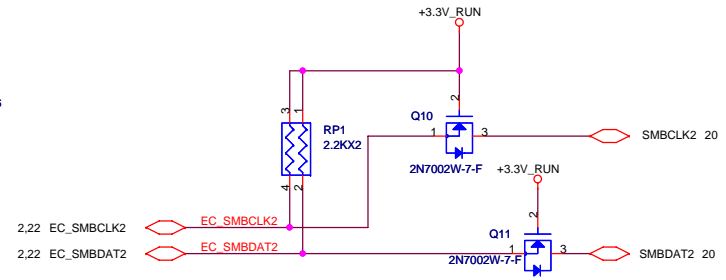
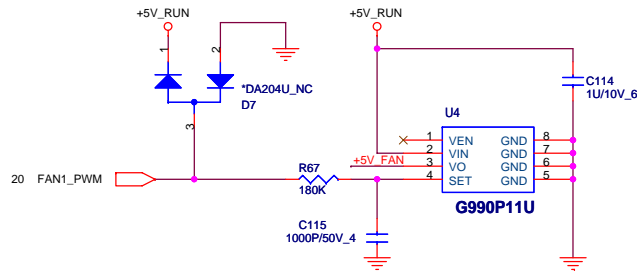
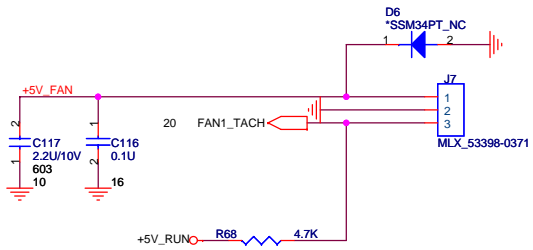


Power button for Engineer

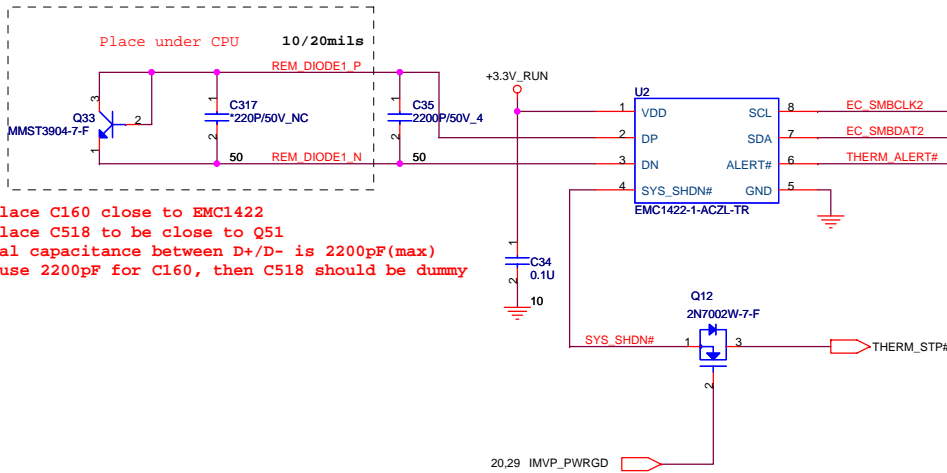


3VALW ON POWER LOGIC

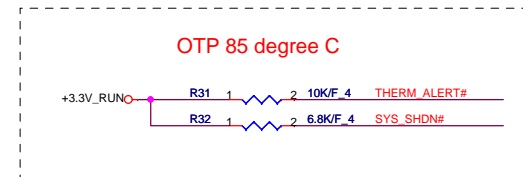


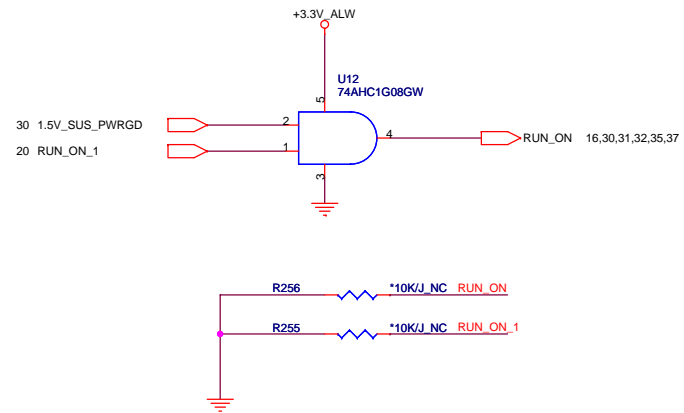
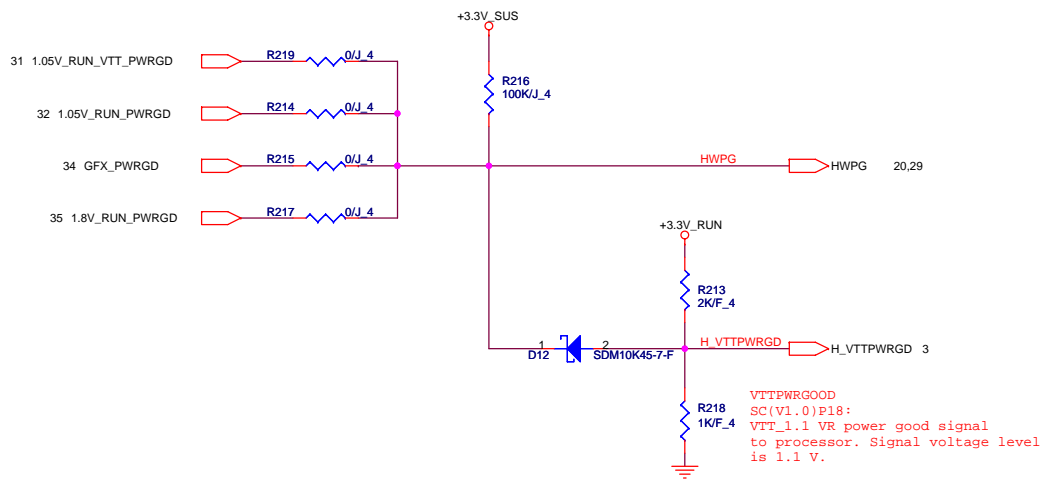
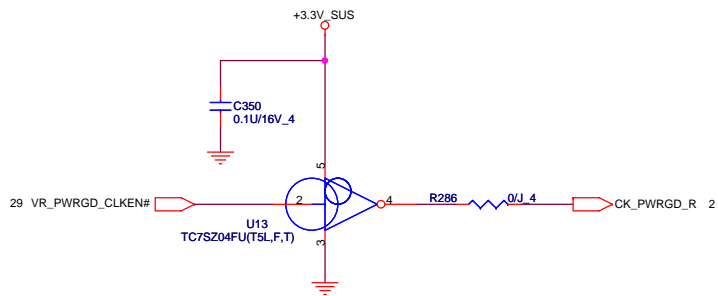


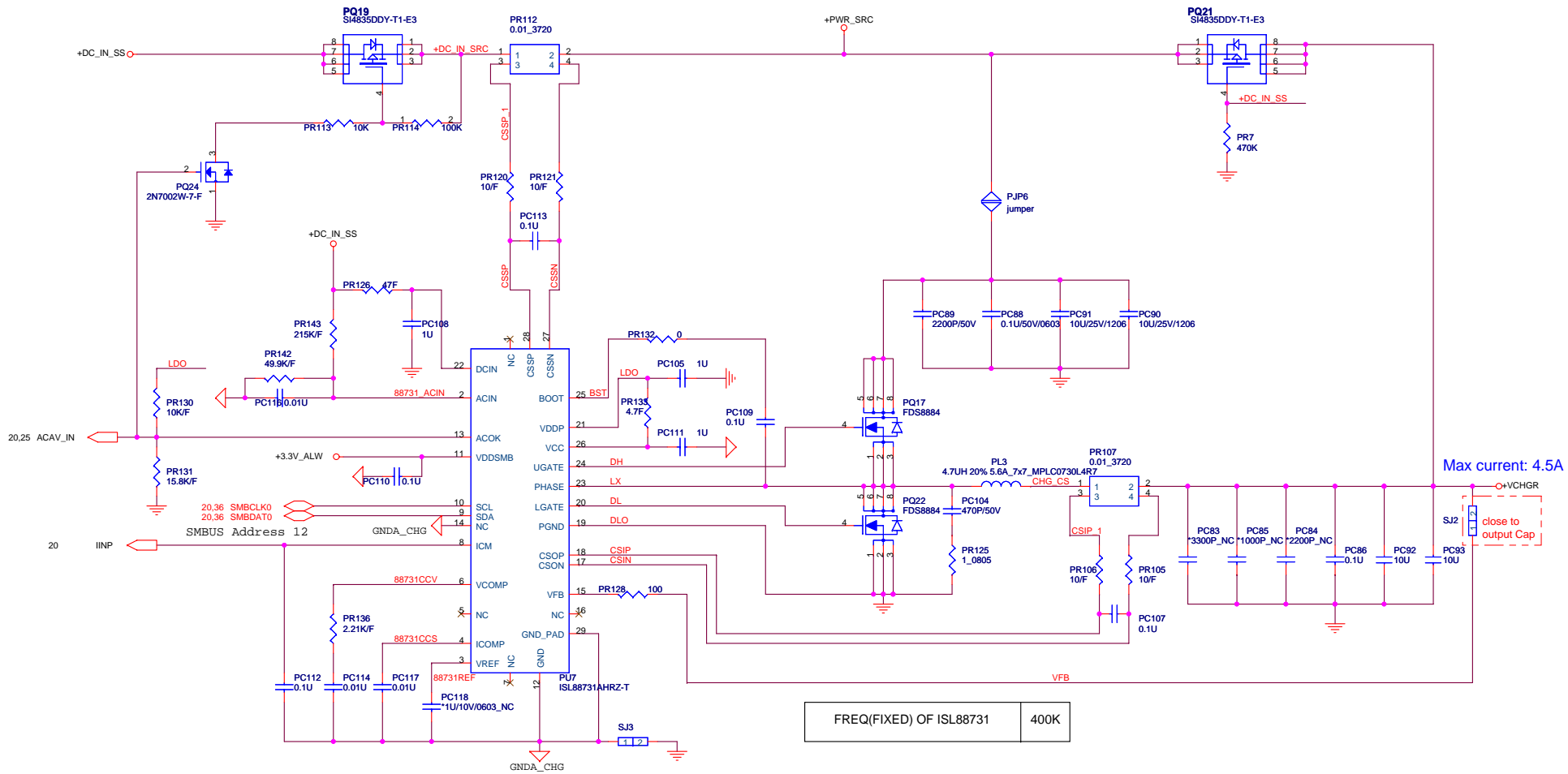
0907 Steg: Need to check C484 if needed

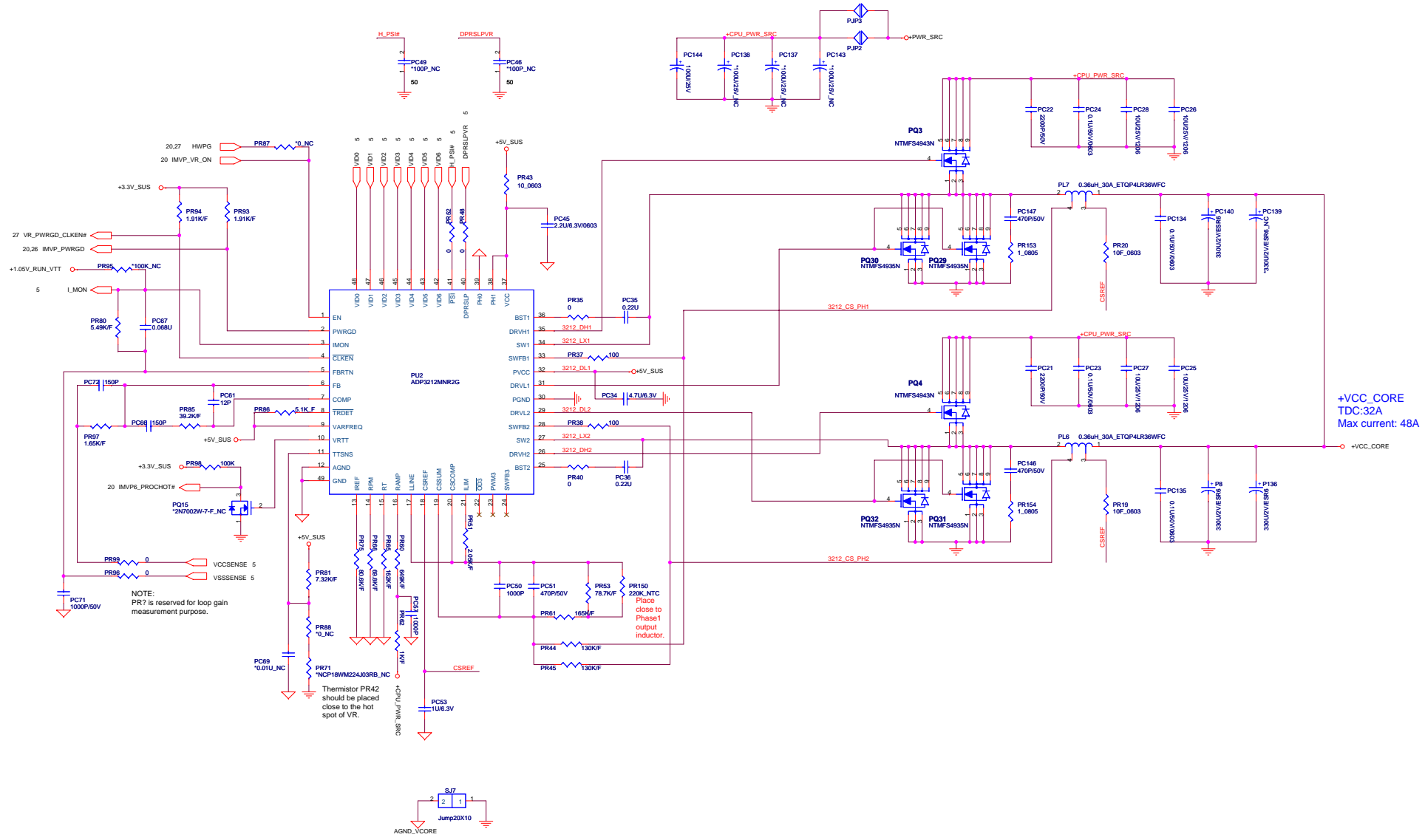


1. Place C160 close to EMC1422
 2. Place C518 to be close to Q51
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

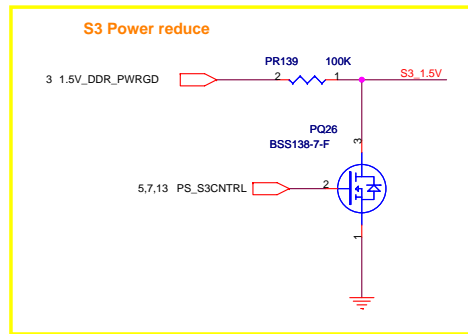








TON	PR67 = 620K
FREQ	400K



VDDQ and VTT discharge control

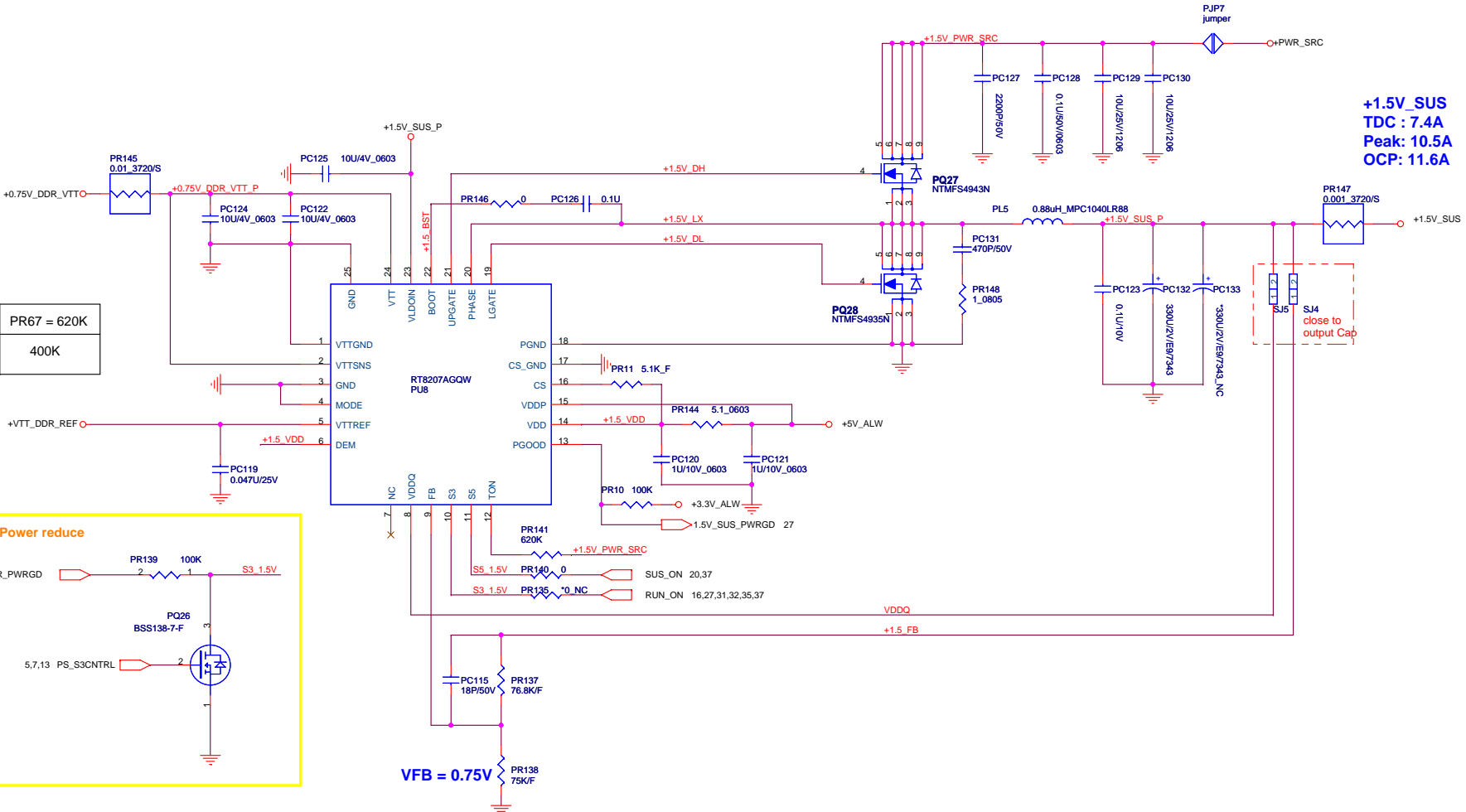
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

VDDQ output voltage selection

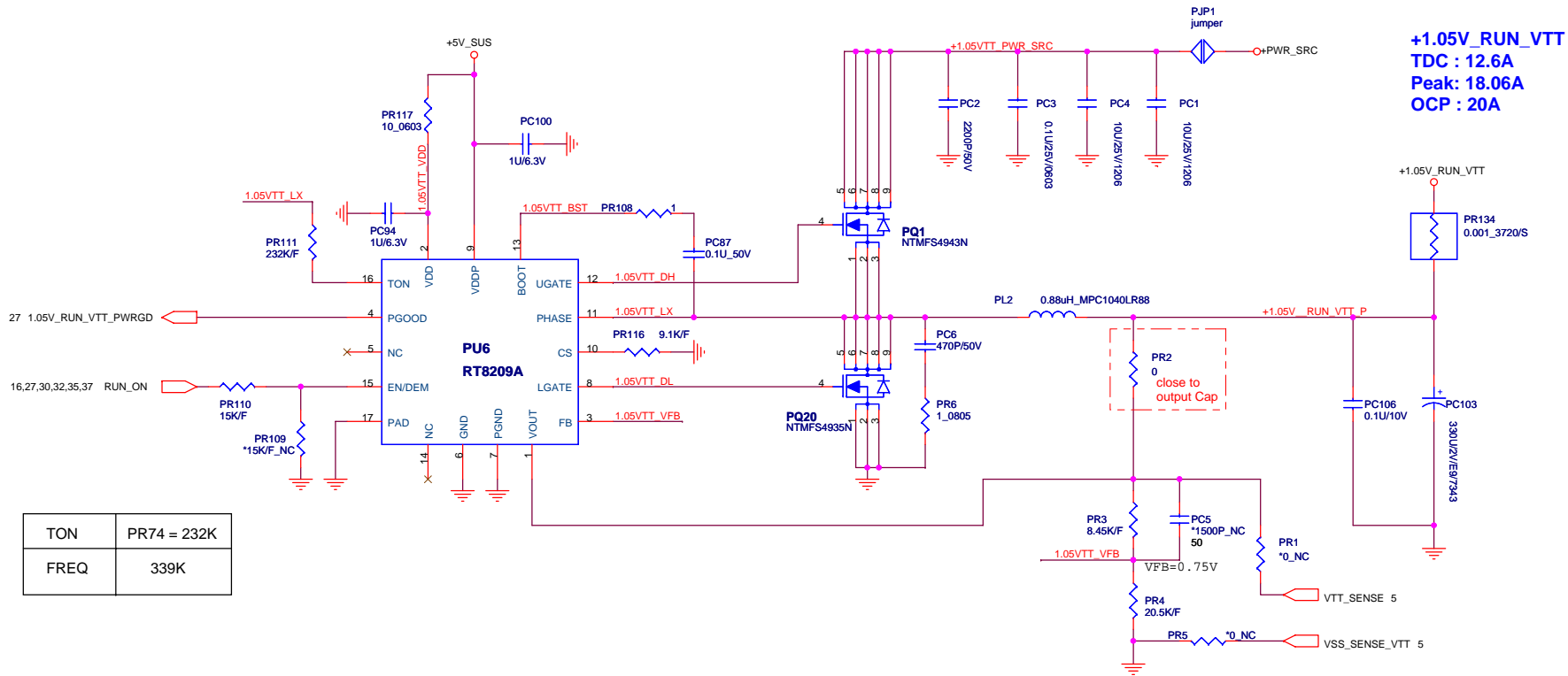
FB	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	0.75V < VDDQ < 3.3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

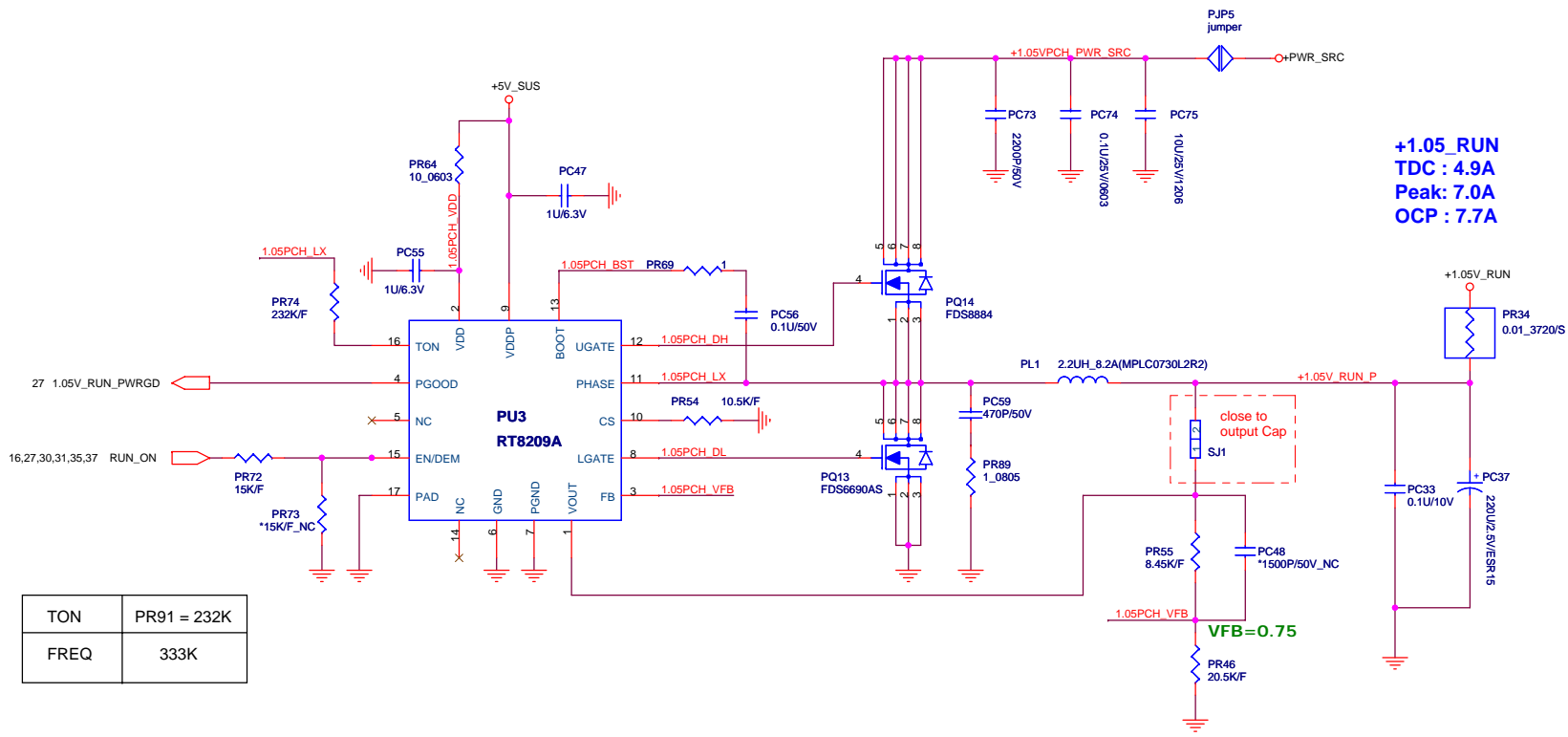


+1.5V_SUS
TDC : 7.4A
Peak: 10.5A
OCP: 11.6A



+1.05V_RUN_VTT
TDC : 12.6A
Peak: 18.06A
OCP : 20A

TON	PR74 = 232K
FREQ	339K



+1.05_RUN
TDC : 4.9A
Peak: 7.0A
OCP : 7.7A

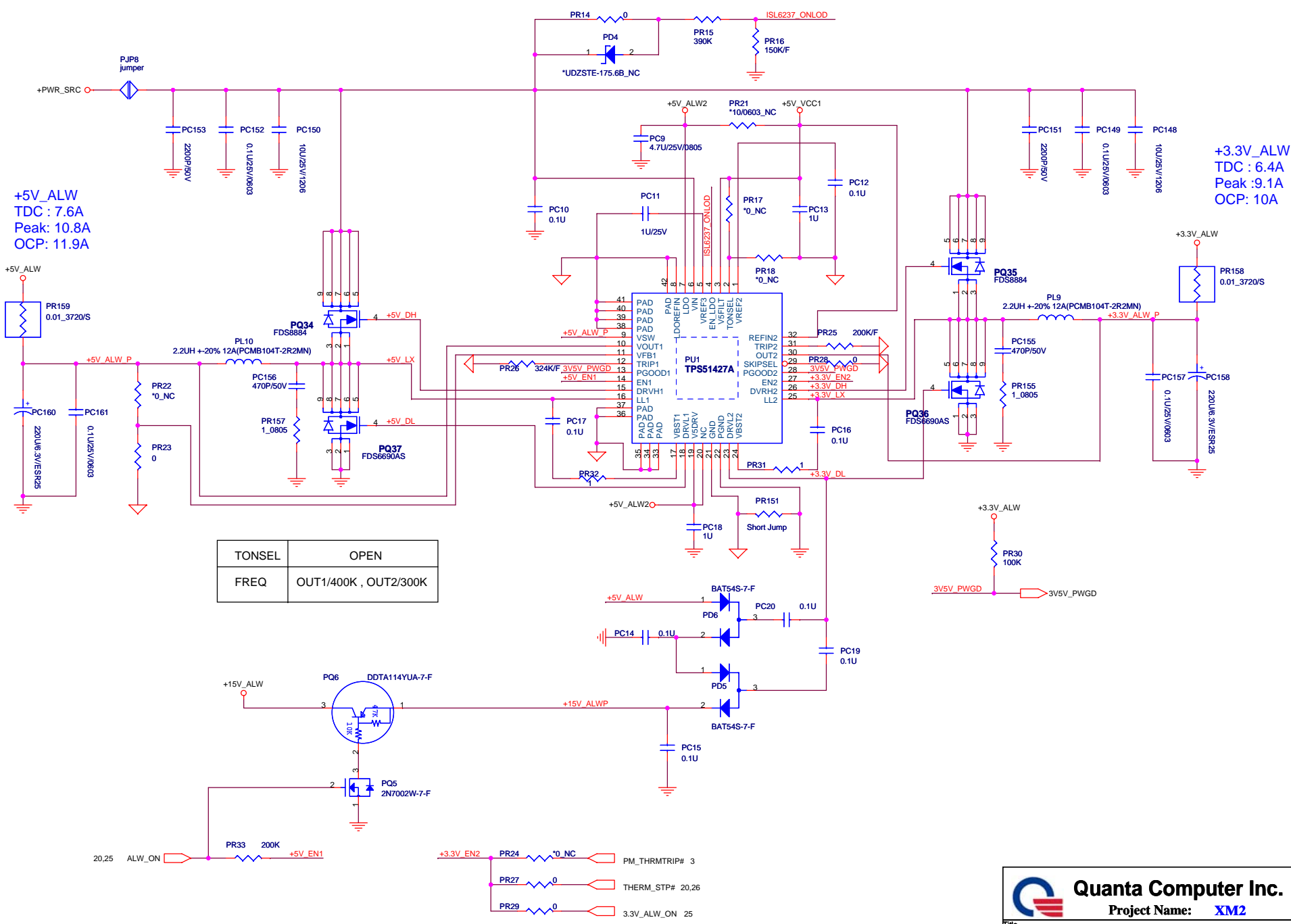
TON	PR91 = 232K
FREQ	333K

Quanta Computer Inc.
 Project Name: **XM2**

Title: CoverPage

Size: Document Number XM2_MB Rev D

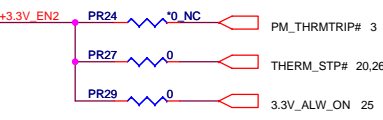
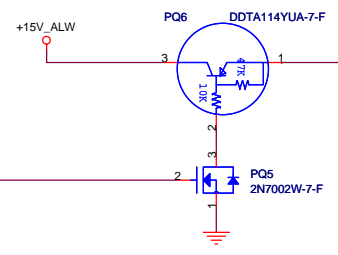
Date: Friday, January 15, 2010 Sheet 32 of 39



+5V_ALW
TDC : 7.6A
Peak: 10.8A
OCP: 11.9A

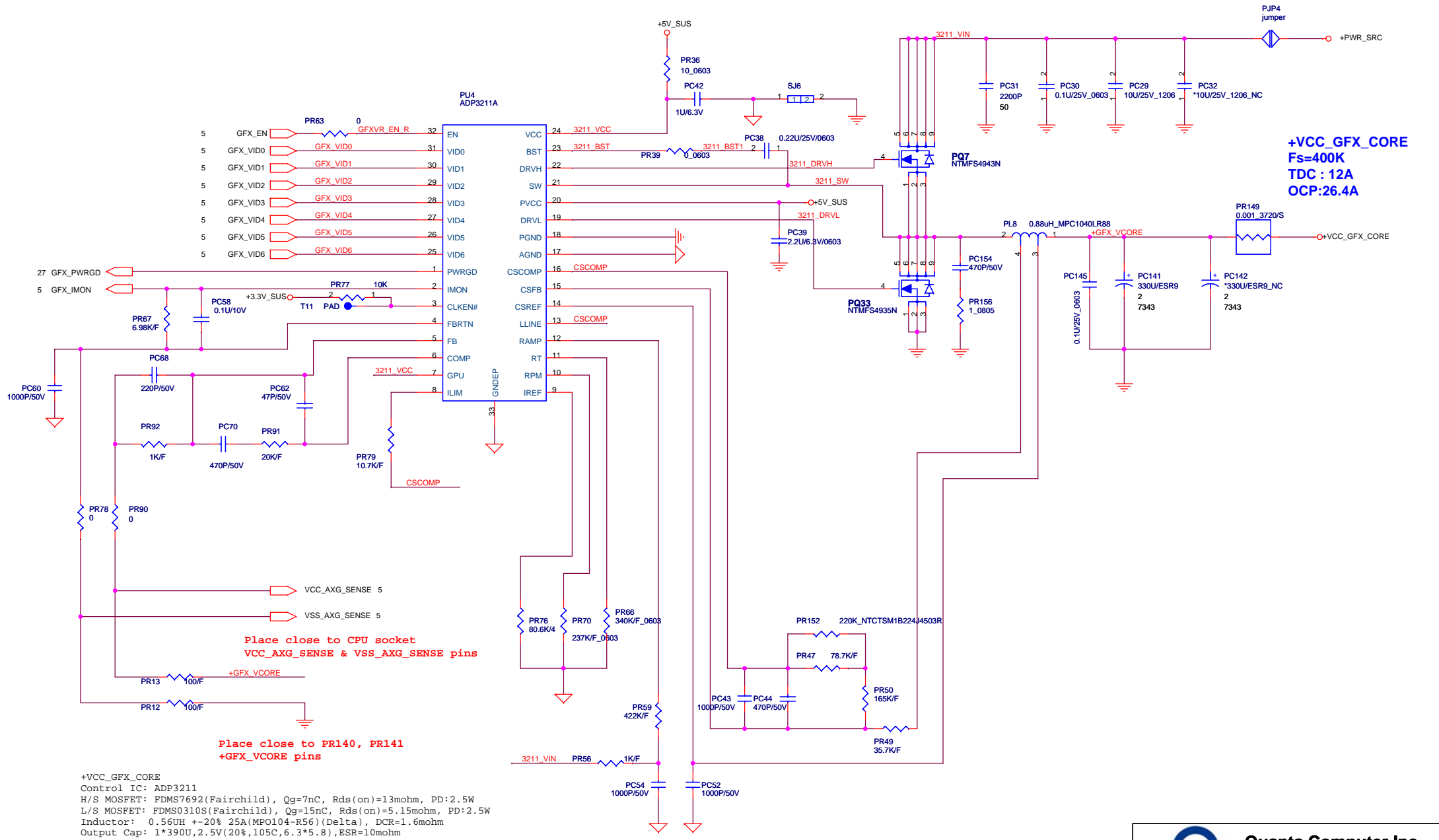
+3.3V_ALW
TDC : 6.4A
Peak :9.1A
OCP: 10A

TONSEL	OPEN
FREQ	OUT1/400K , OUT2/300K



Quanta Computer Inc.
Project Name: **XM2**

Title		
CoverPage		
Size	Document Number	Rev
	XM2_MB	D
Date:	Friday, January 15, 2010	Sheet
		33 of 39



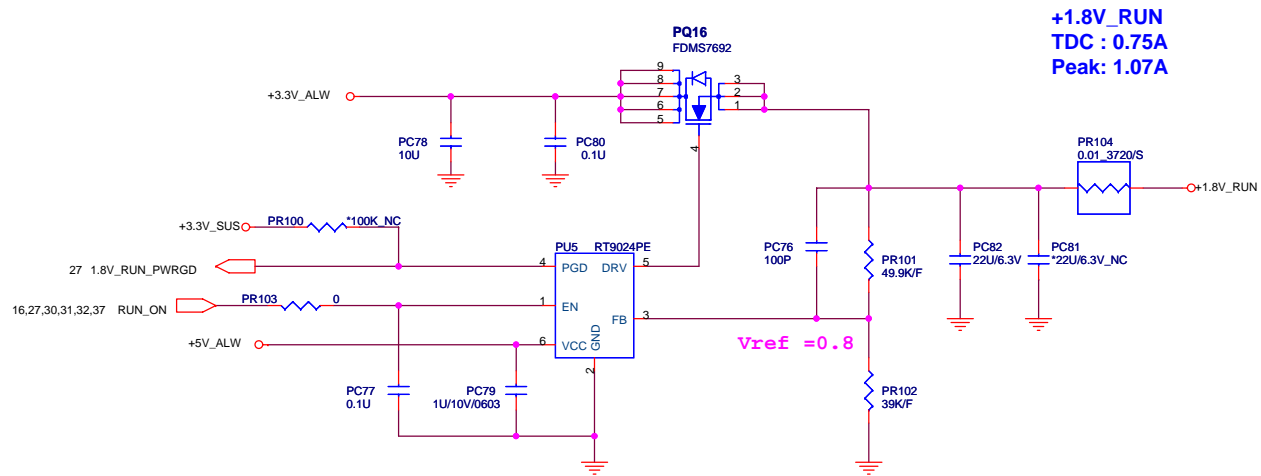
+VCC_GFX_CORE
Fs=400K
TDC : 12A
OCP:26.4A

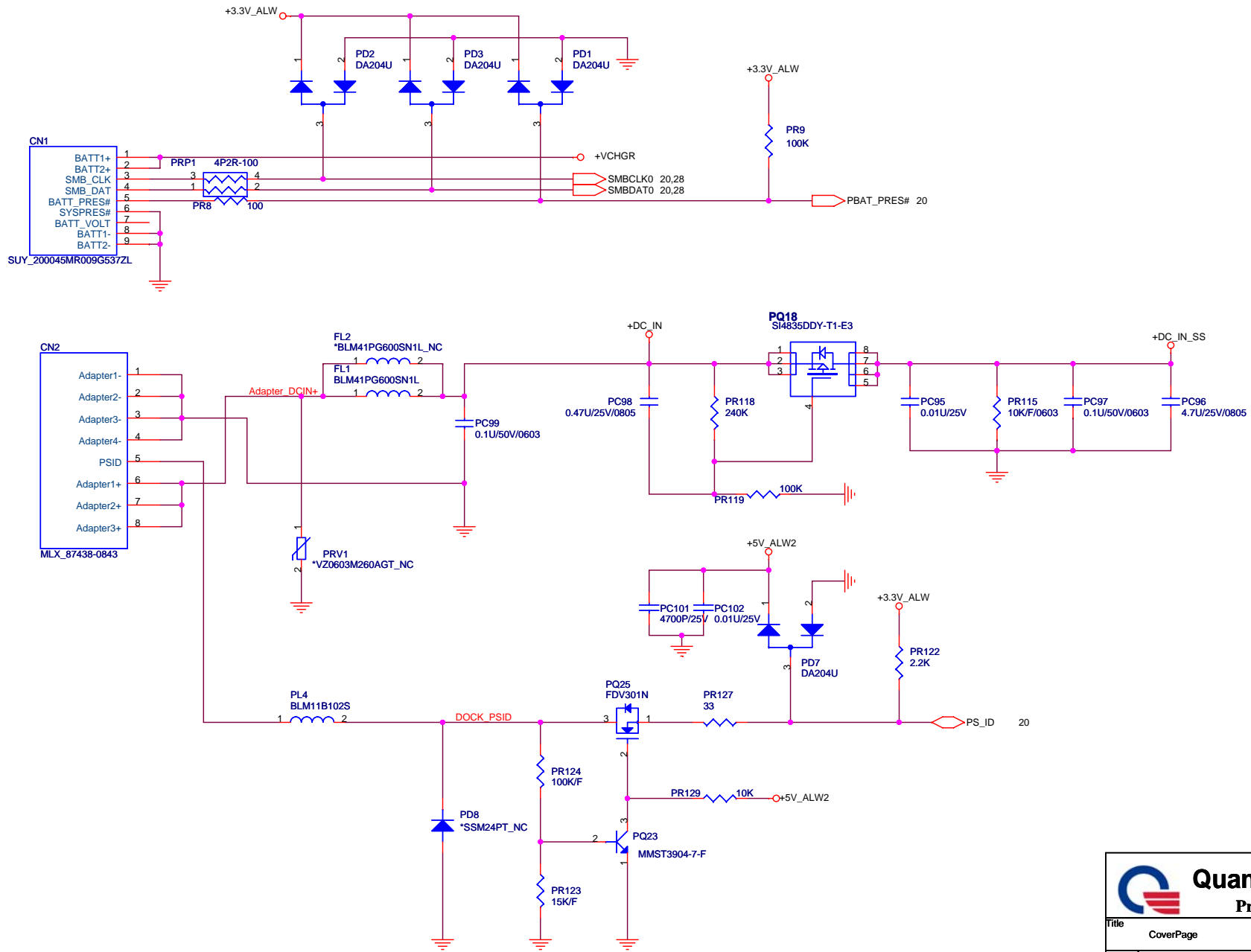
Place close to CPU socket
VCC_AXG_SENSE & VSS_AXG_SENSE pins

Place close to PR140, PR141
+GFX_VCORE pins

+VCC_GFX_CORE
 Control IC: ADP3211
 H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
 L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
 Inductor: 0.56UH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm
 Output Cap: 1*390U, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm

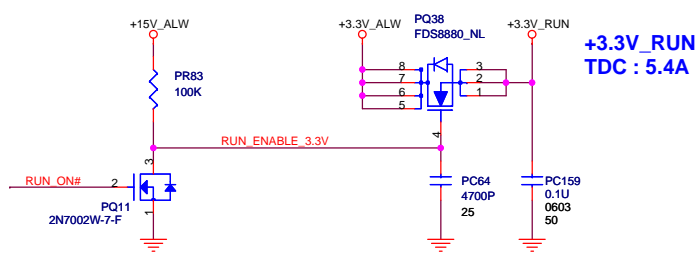
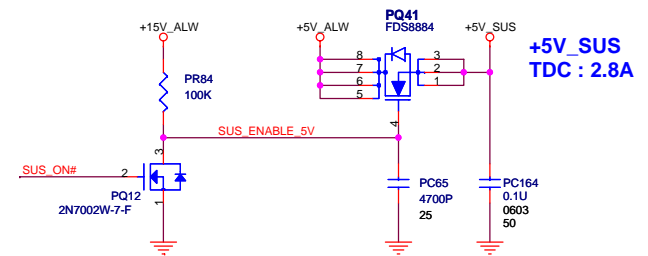
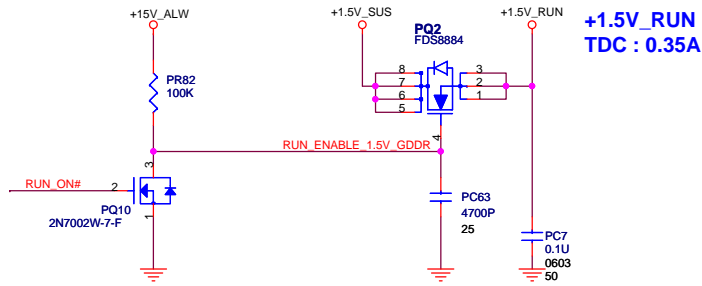
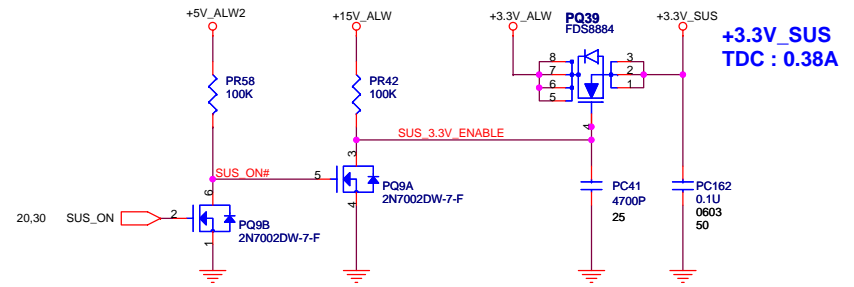
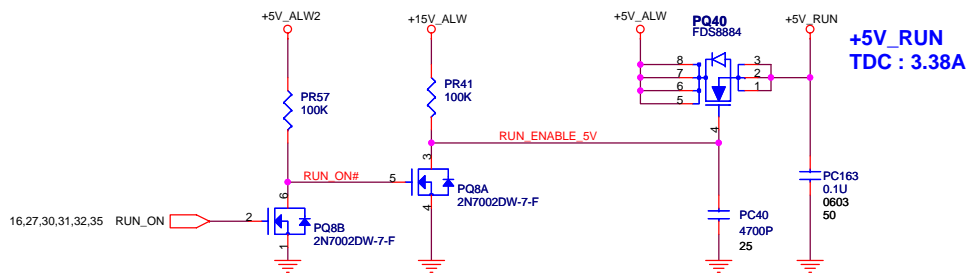
			Quanta Computer Inc. PROJECT : GM6 UMA MB
Date: Friday, January 15, 2010			Sheet 34 of 39



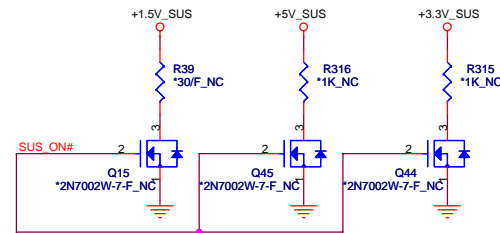
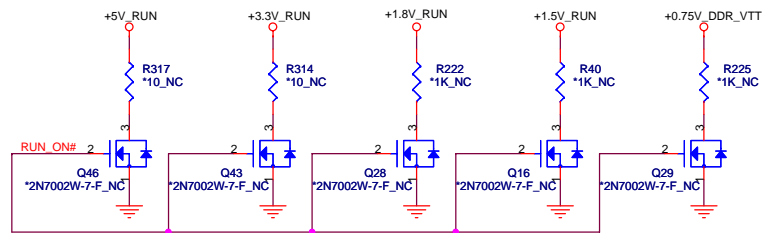


Quanta Computer Inc.
 Project Name: **XM2**

Title		Rev
CoverPage		D
Size	Document Number	
	XM2_MB	
Date: Friday, January 15, 2010		Sheet 36 of 39

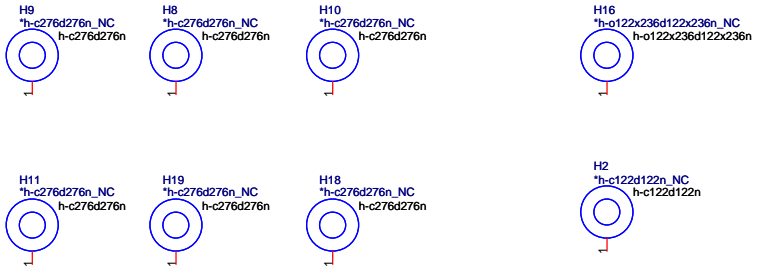
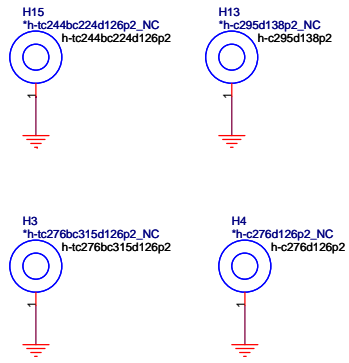
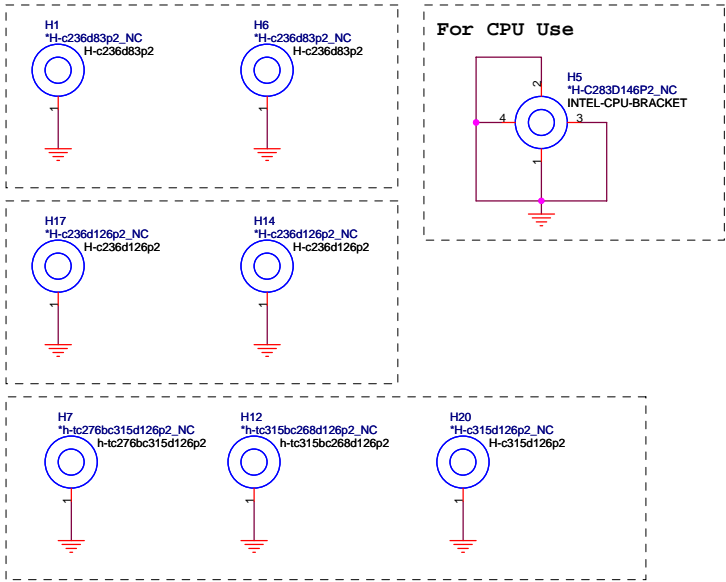



Reserve discharge path



Quanta Computer Inc.
Project Name: **XM2**

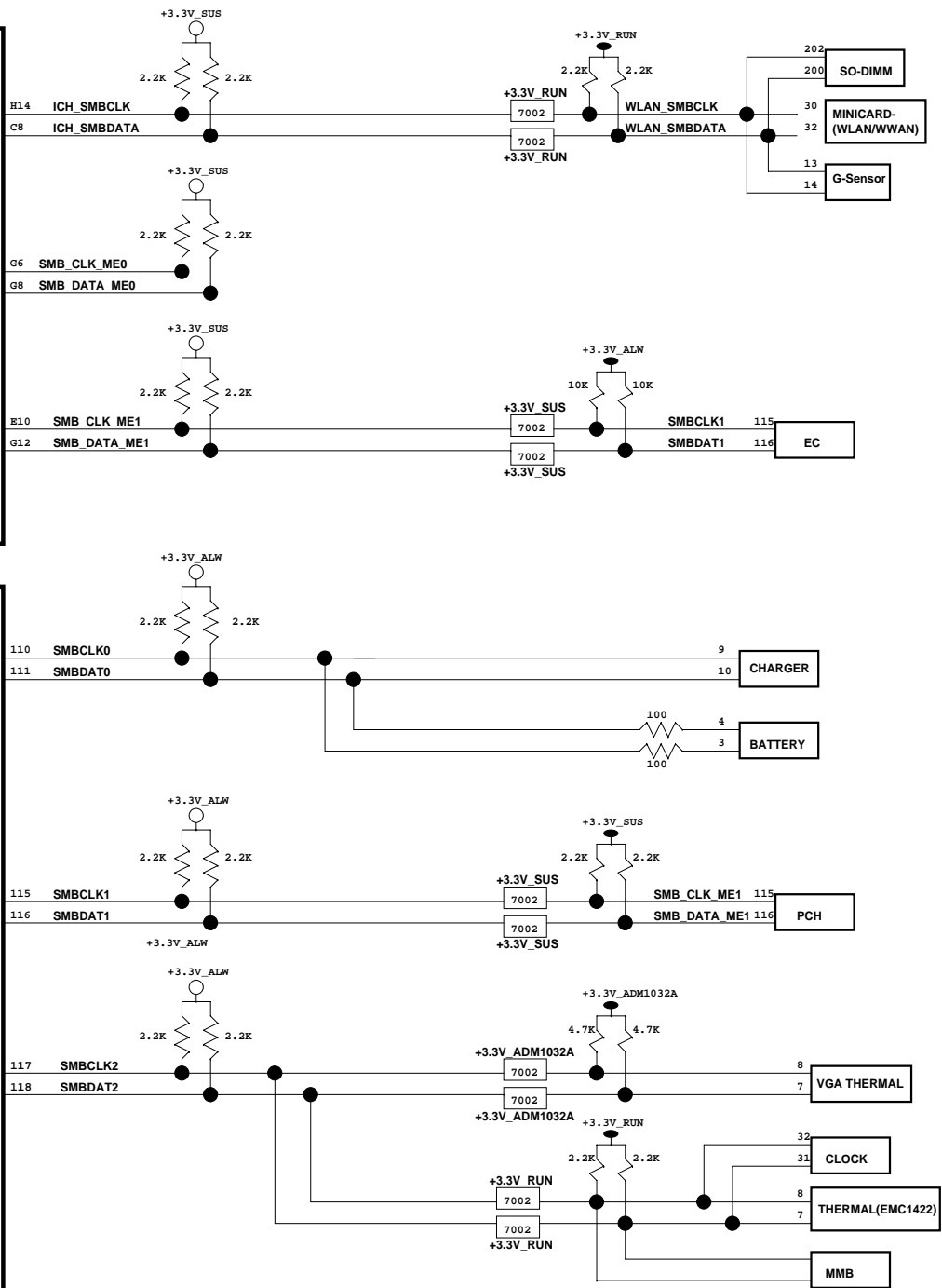
Title CoverPage		
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet	37 of 39



 Quanta Computer Inc. Project Name: GM7	
Title: PAD & SCREW	
Size: Document Number	Rev: D
Date: Friday, January 15, 2010	
Sheet 38 of 40	

PCH

SIO
ITE8502



www.s-manuals.com