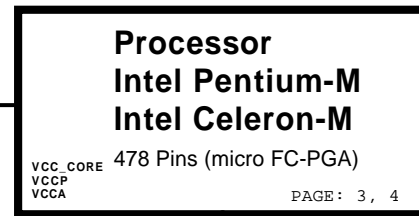


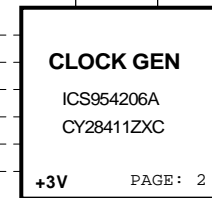
## PENTIUM-M / ALVISO / ICH6-M

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

**CPU THERMAL  
SENSOR**  
MAX6657 / GMT-781  
+3V PAGE: 3



```
HCLK_CPU
HCLK_CPU#
HCLK_MCH
HCLK_MCH#
SRC_MCH
SRC_MCH#
SRC_ICH
SRC_ICH#
DREFSSCLK
DREFSSCLK#
DOT96
DOT96#
```



14.318MHz

- > PCLK\_591
- > PCLK\_7411
- > PCLK\_ICH
- > PCLK\_MINI
- > PCLK\_LAN
- > CLK48\_USB
- > 14M\_ICH

SYSTEM POWER MAX1845  
2.5VSUS/1.5V\_S5 PAGE: 38

CPU CORE MAX1907  
POWER 1.356V

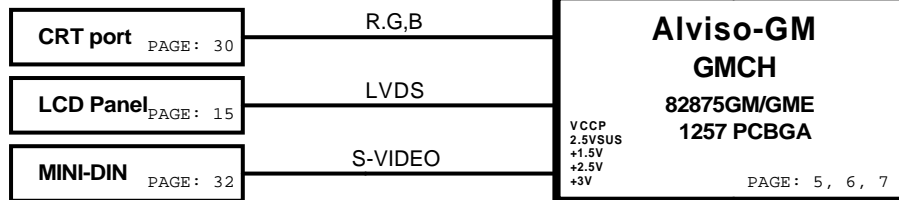
SYSTEM POWER MAX1999  
POWER(3V/5V/15V) PAGE: 36

SYSTEM POWER MAX1992  
VCCP PAGE: 37

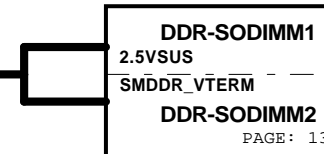
NS L2996  
VTT\_DDR  
PAGE: 39

**BATT CHARGER**  
**MAX1772**

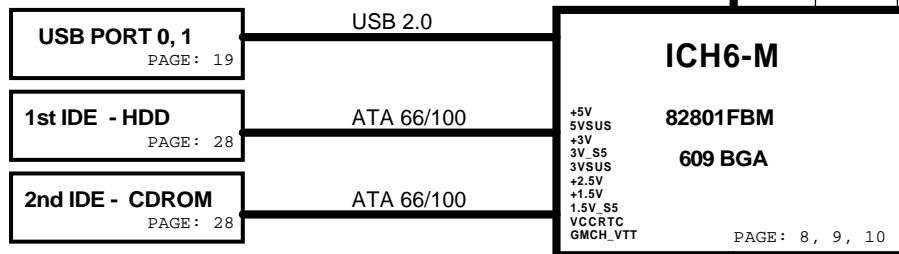
**DISCHARGE** PAGE: 35



DDR I/F 2.5V  
333MHz  
Single Channel

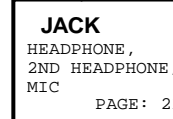
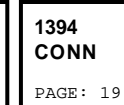
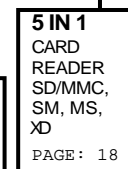
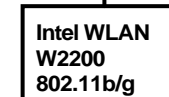
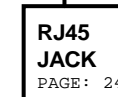
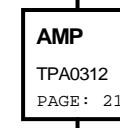
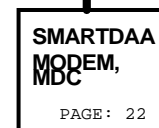
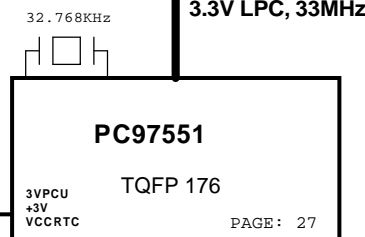
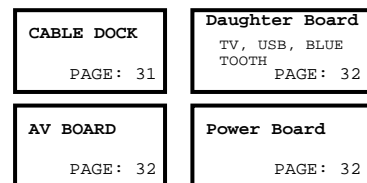
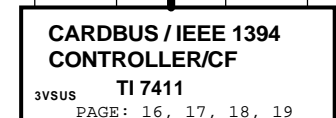
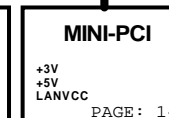
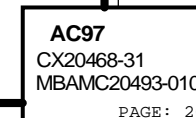
DMI interface  
100MHZ 4X

32.768KHz



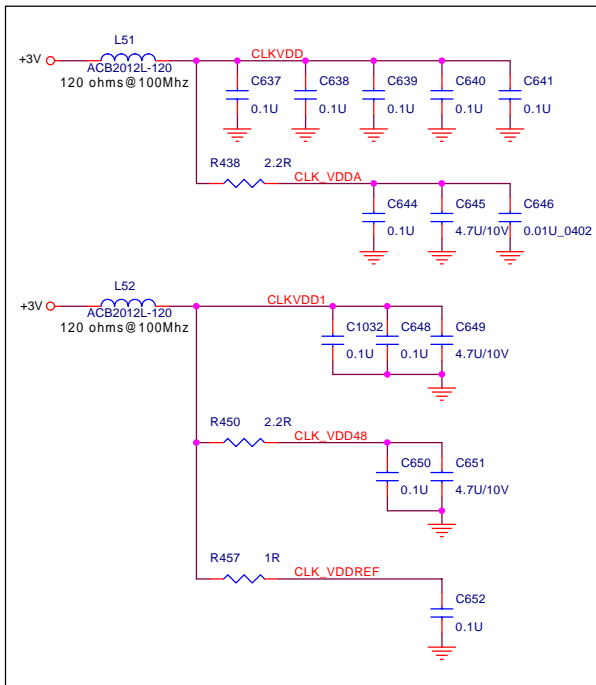
33MHZ, 3.3V PCI

AC97



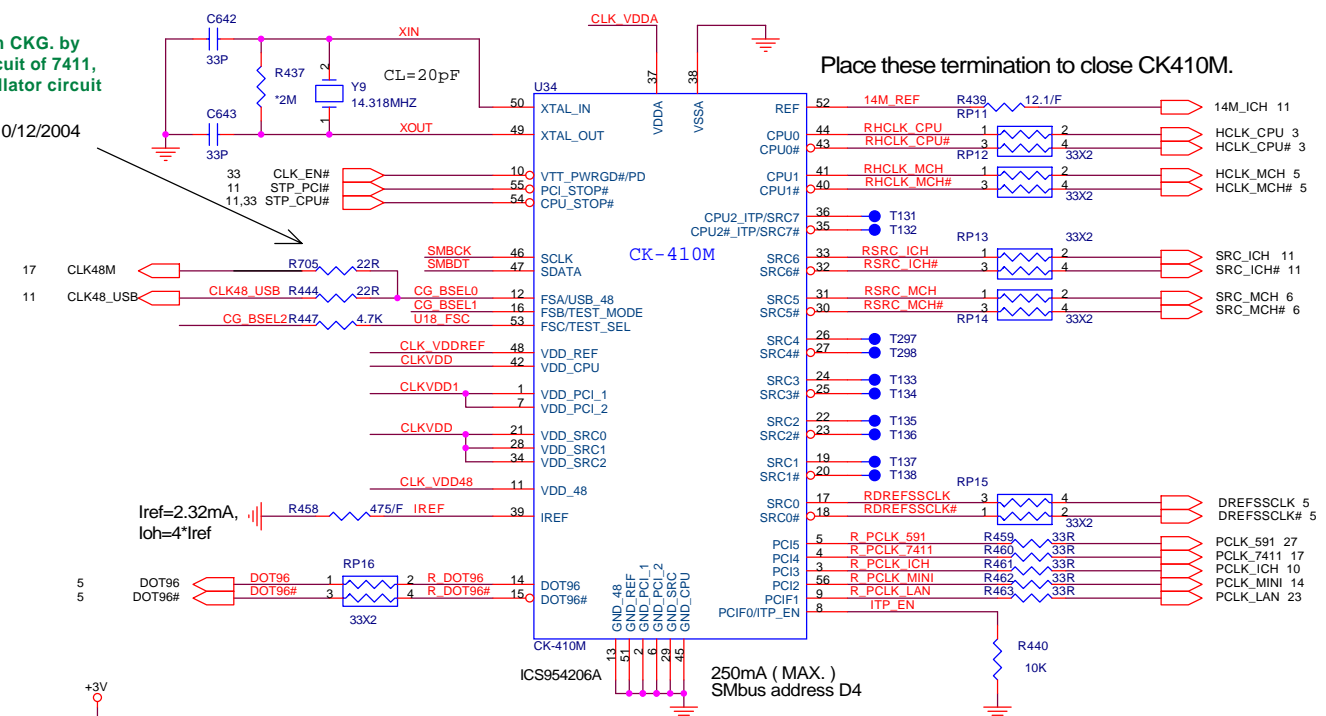
## PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET AD16		2	A
MINIPCI SLOT AD22		1	C,D
CardBus/1394 AD25		0	E,F,G



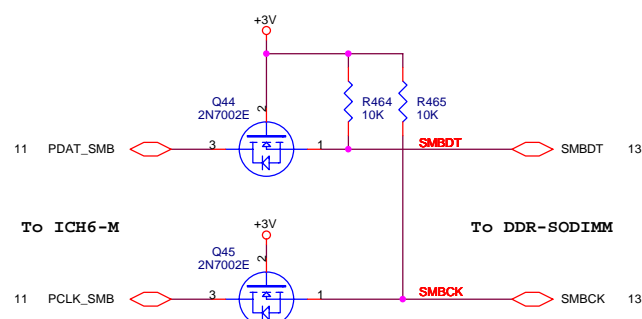
SI stage:  
Enable CLK48M from CKG. by  
R705 for the PLL circuit of 7411,  
and disable the oscillator circuit  
at PCI7411 side.

Sting 10/12/2004



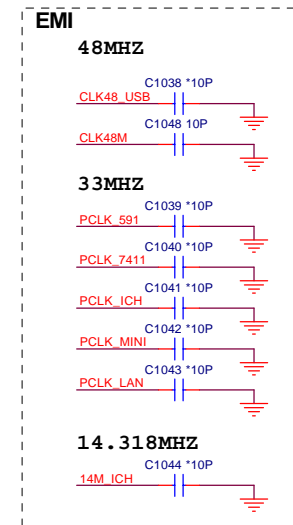
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33 DOTHAN FSB 400
0	0	1	133	100	33 DOTHAN FSB 533
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RESERVED		

\* Frequency select by CPU auto sense.

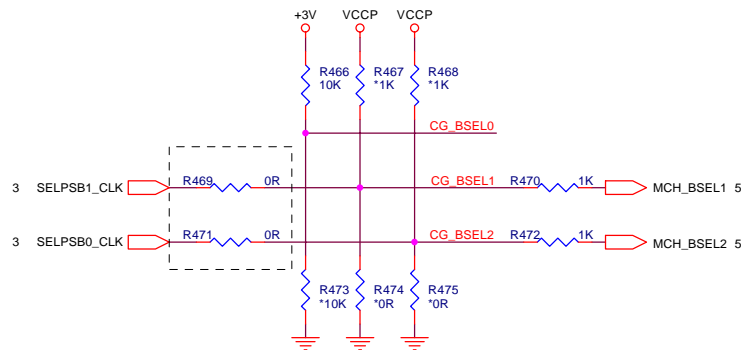
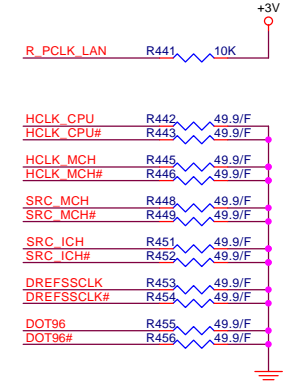


PV stage:  
Add C1048 for CLK48M to get better EMI  
performance.

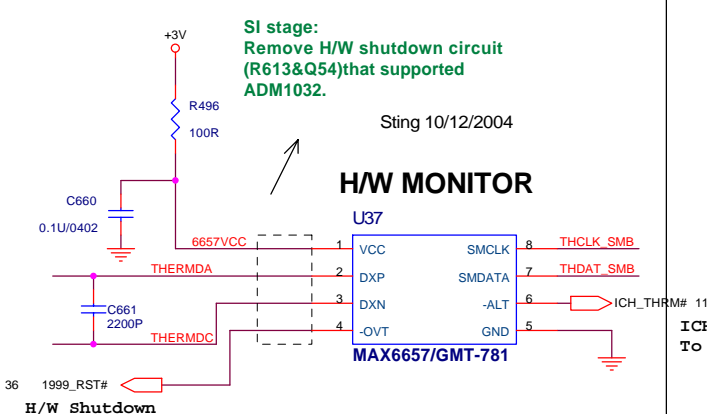
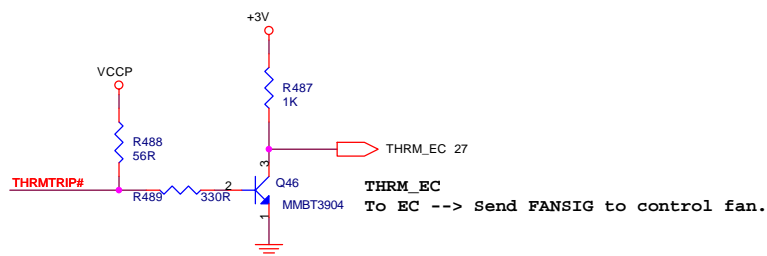
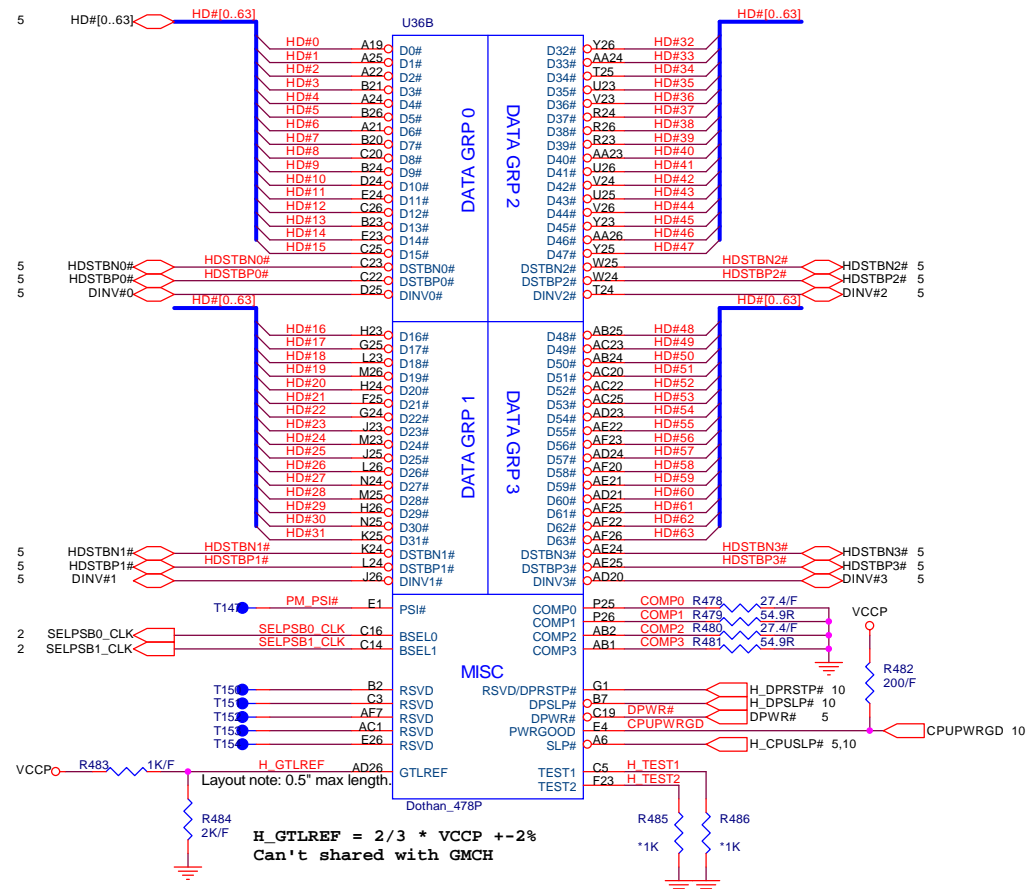
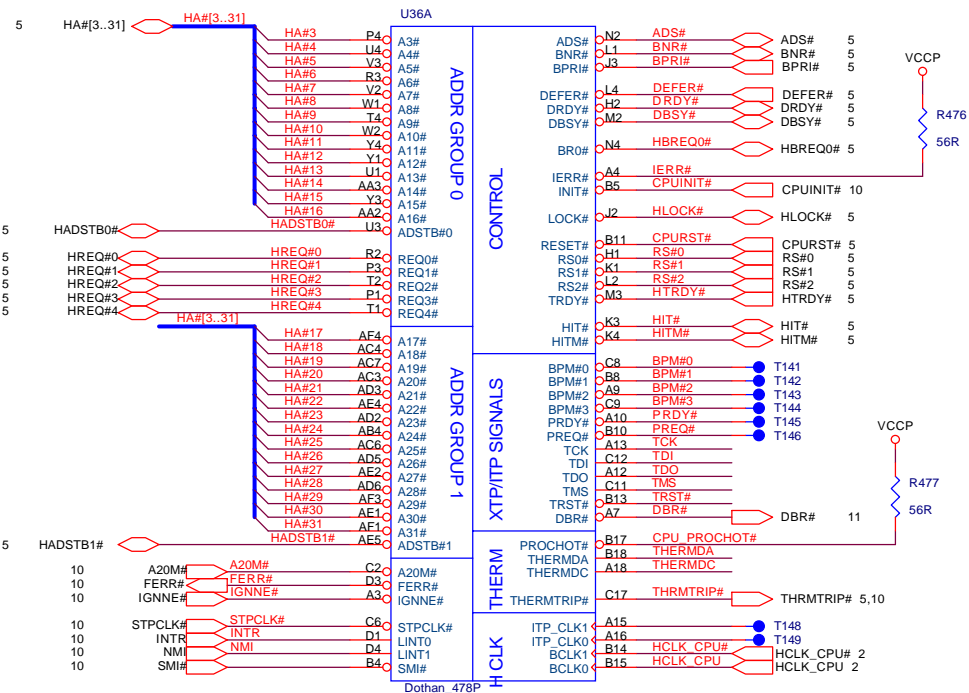
Sting 11/29/2004



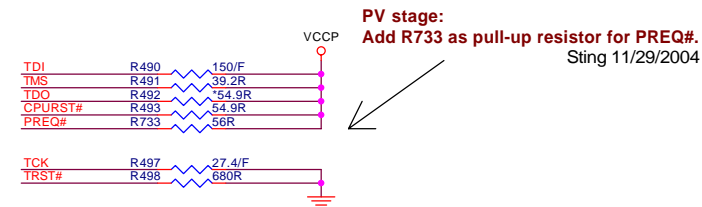
R\_PCLK\_LAN ITP\_EN  
0: SRCLK=96MHZ 0: SRC\_7 Pair  
1: SRCLK=100MHZ 1: CPU\_2 ITP Pair

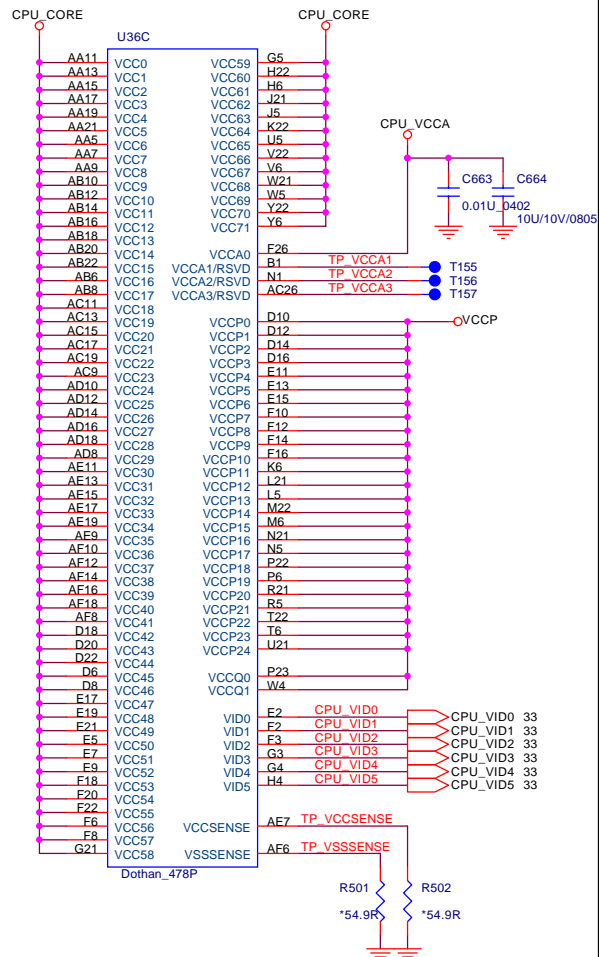


R469,R471  
Dothan-A can remove so that the FSB frequency will be selected by  
hardware setting(R474,R475,R467,R468).  
Dothan-B should be populated.

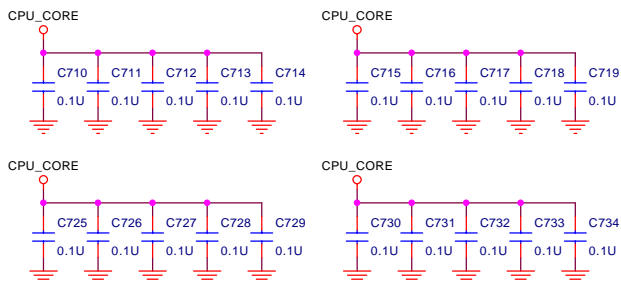
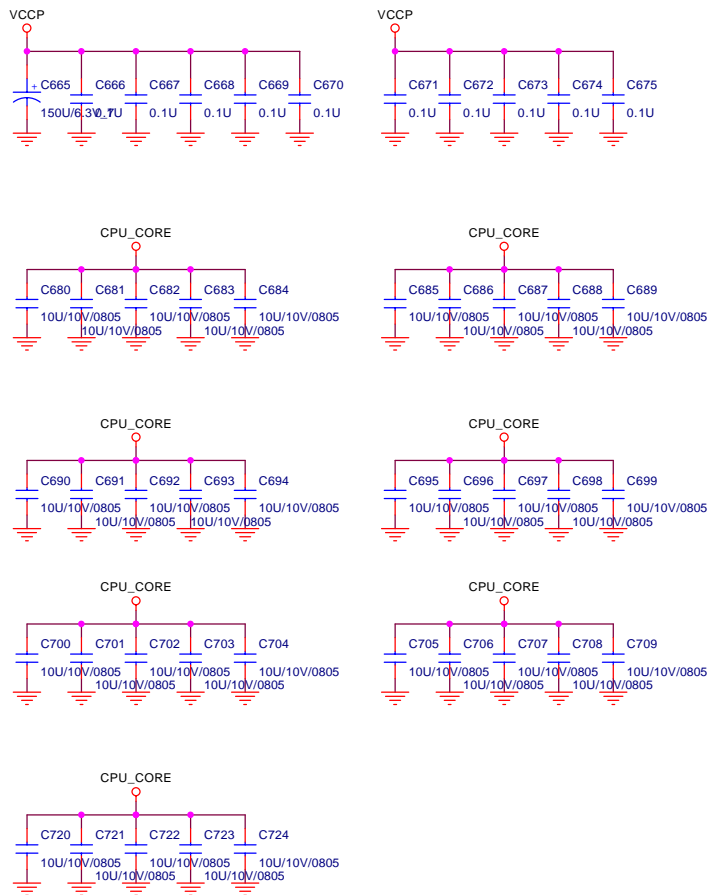


H\_GTLREF = 2/3 \* VCCP +-2%  
Can't shared with GMCH



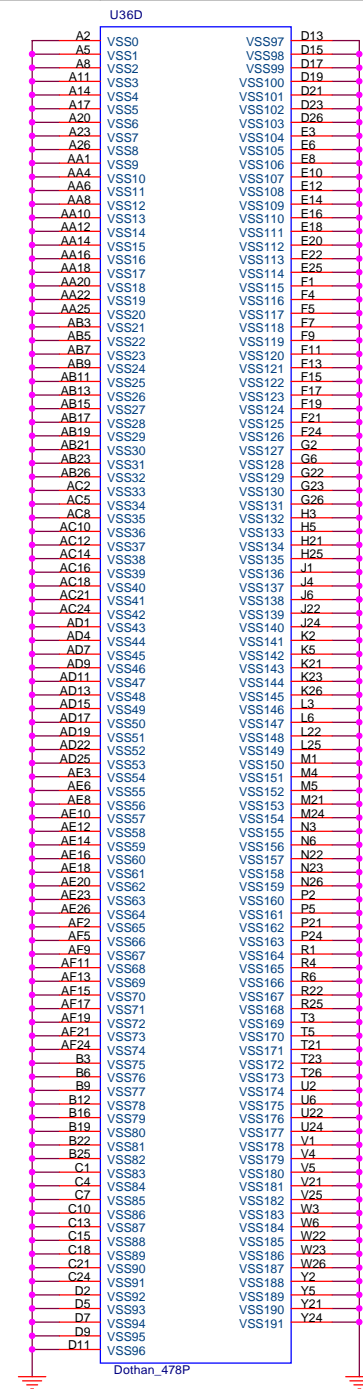
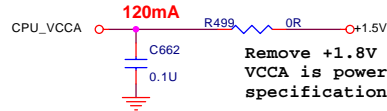


CPU de-coupling  
capacitor

CPU Bypass  
capacitor

Remove +1.8V optional cause of the  
VCCA is powered by +1.5V in Intel  
specification. Sting 08/05/2004

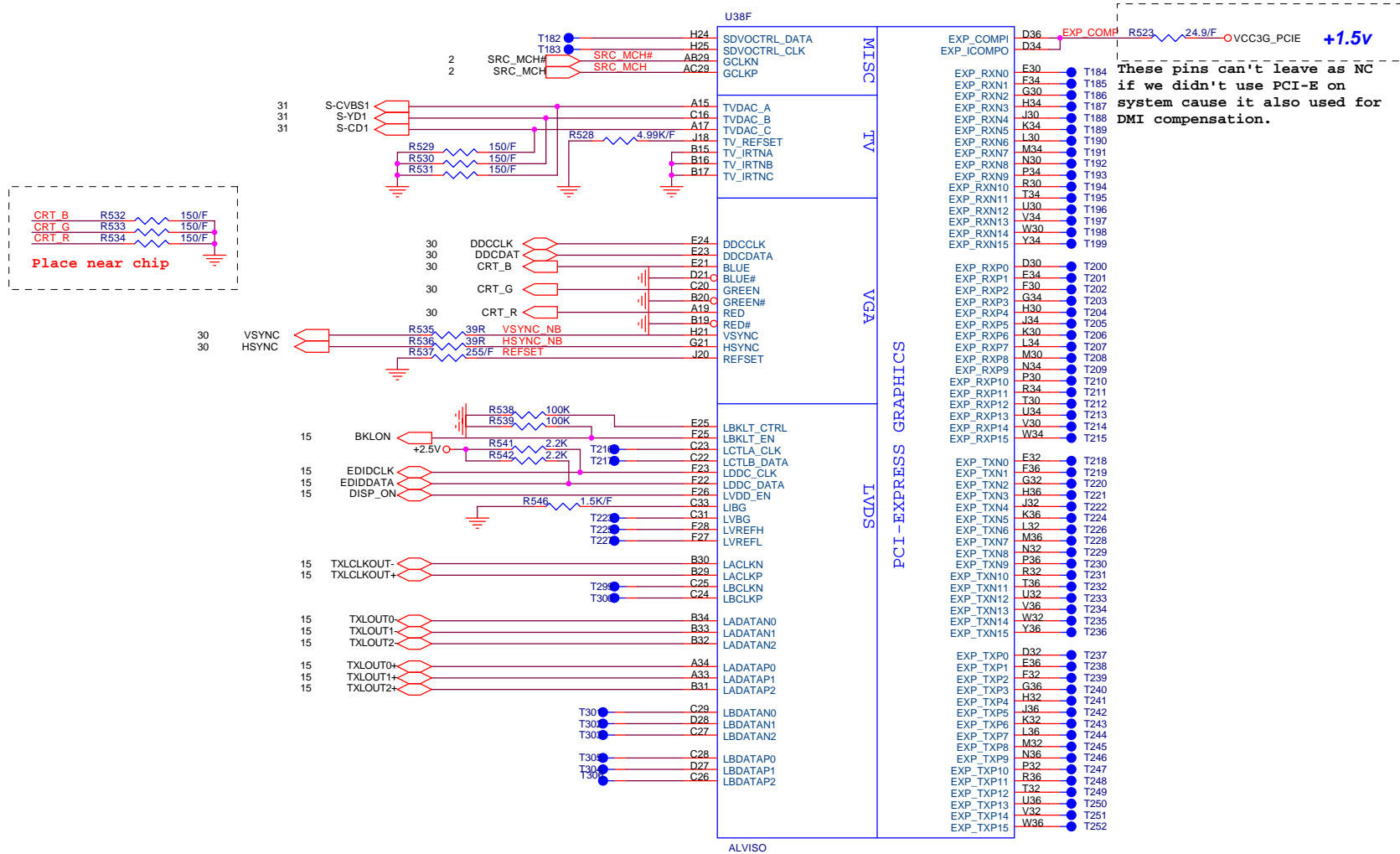
**SI stage:**  
Use X7R type to replace Y5V type  
for Decoupling/Bypass capacitor.



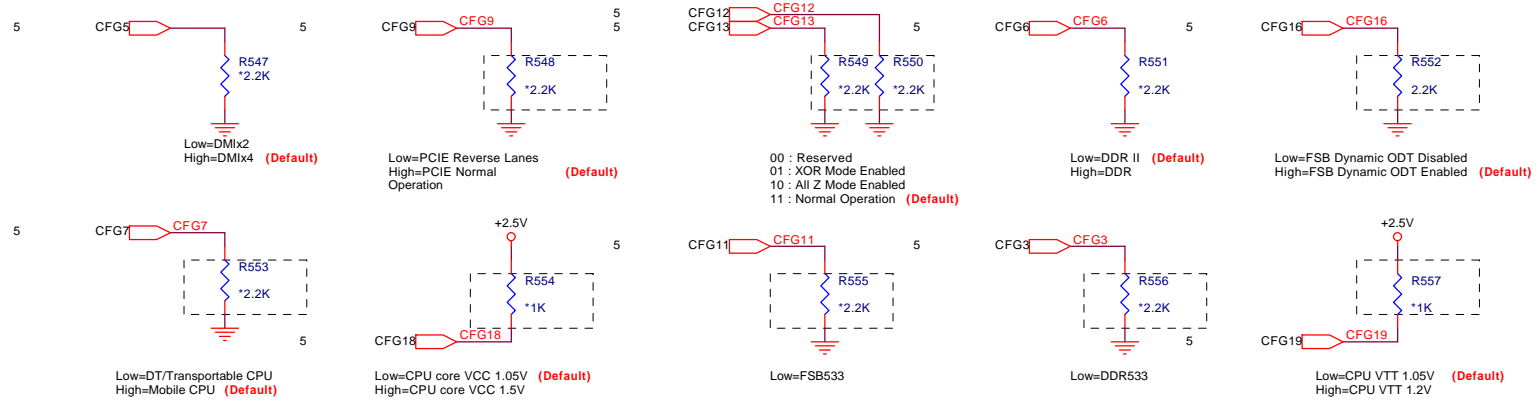
PROJECT : CT3  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<b>CPU POWER / GND</b>	2A
Date:	Friday, March 04, 2005	Sheet 4 of 42





# Strapping

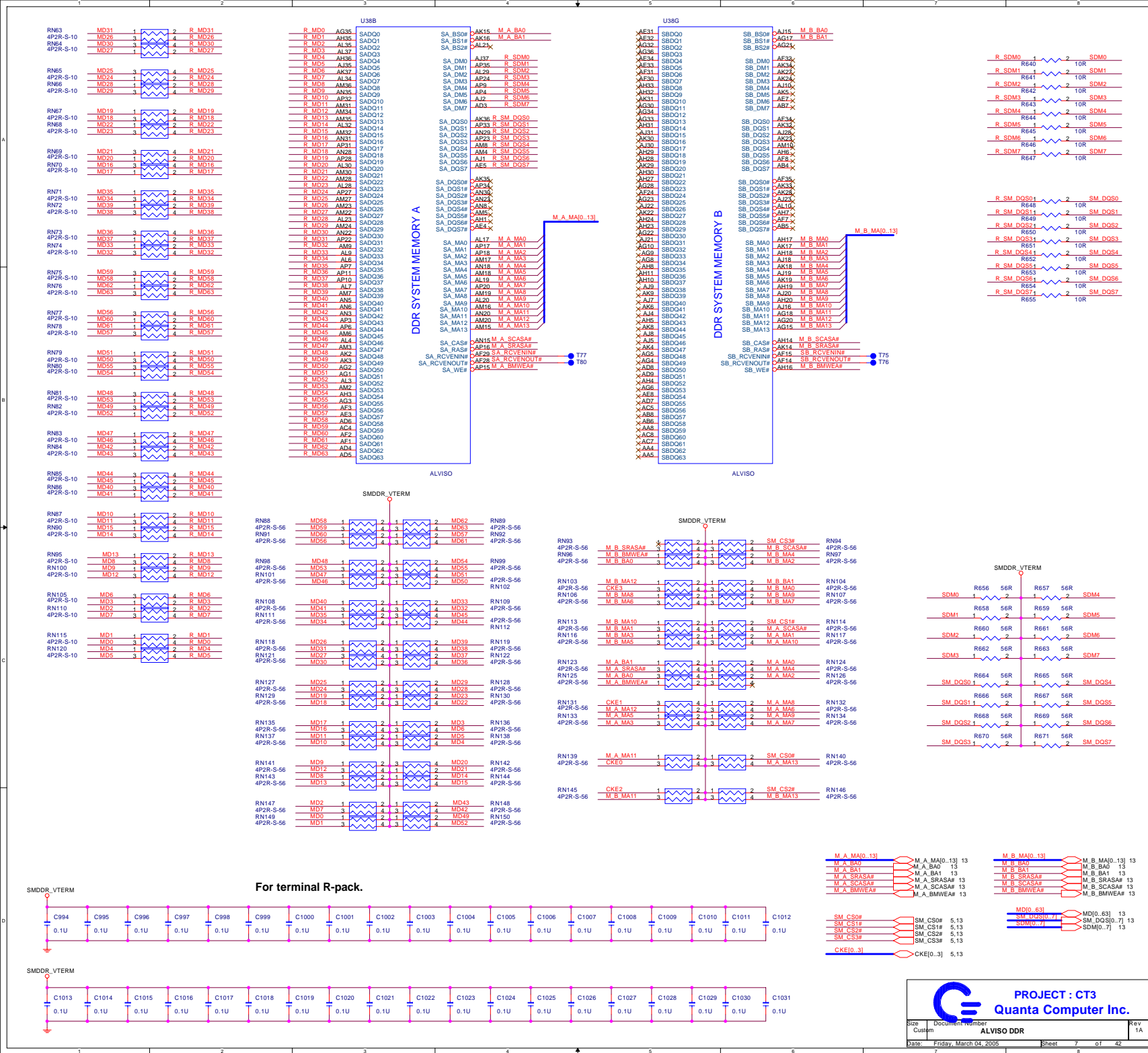


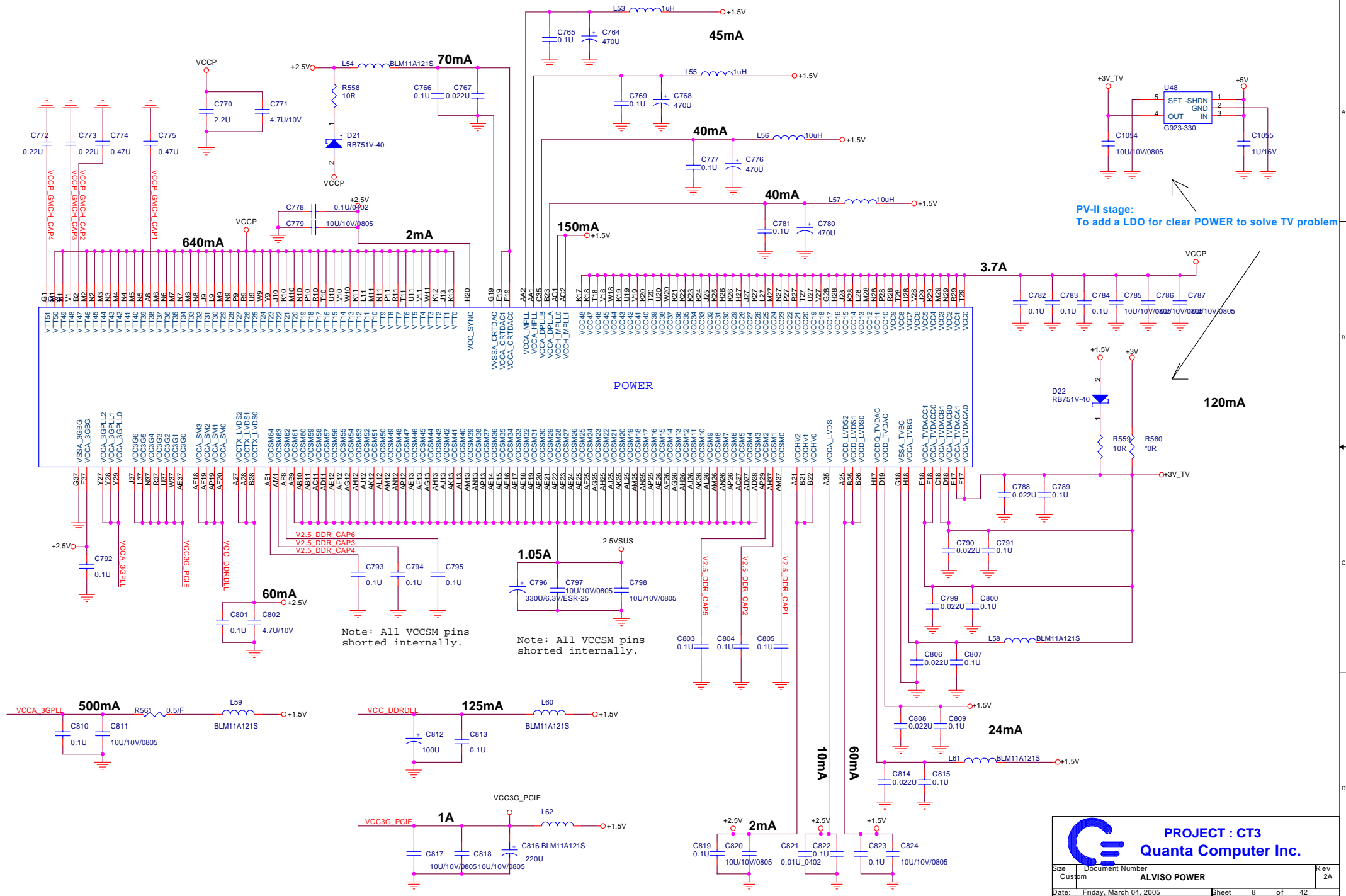
CFG[2:0]  
001=533MT/S FSB  
101=400MT/S FSB

CFG[3:17] have internal pullup.

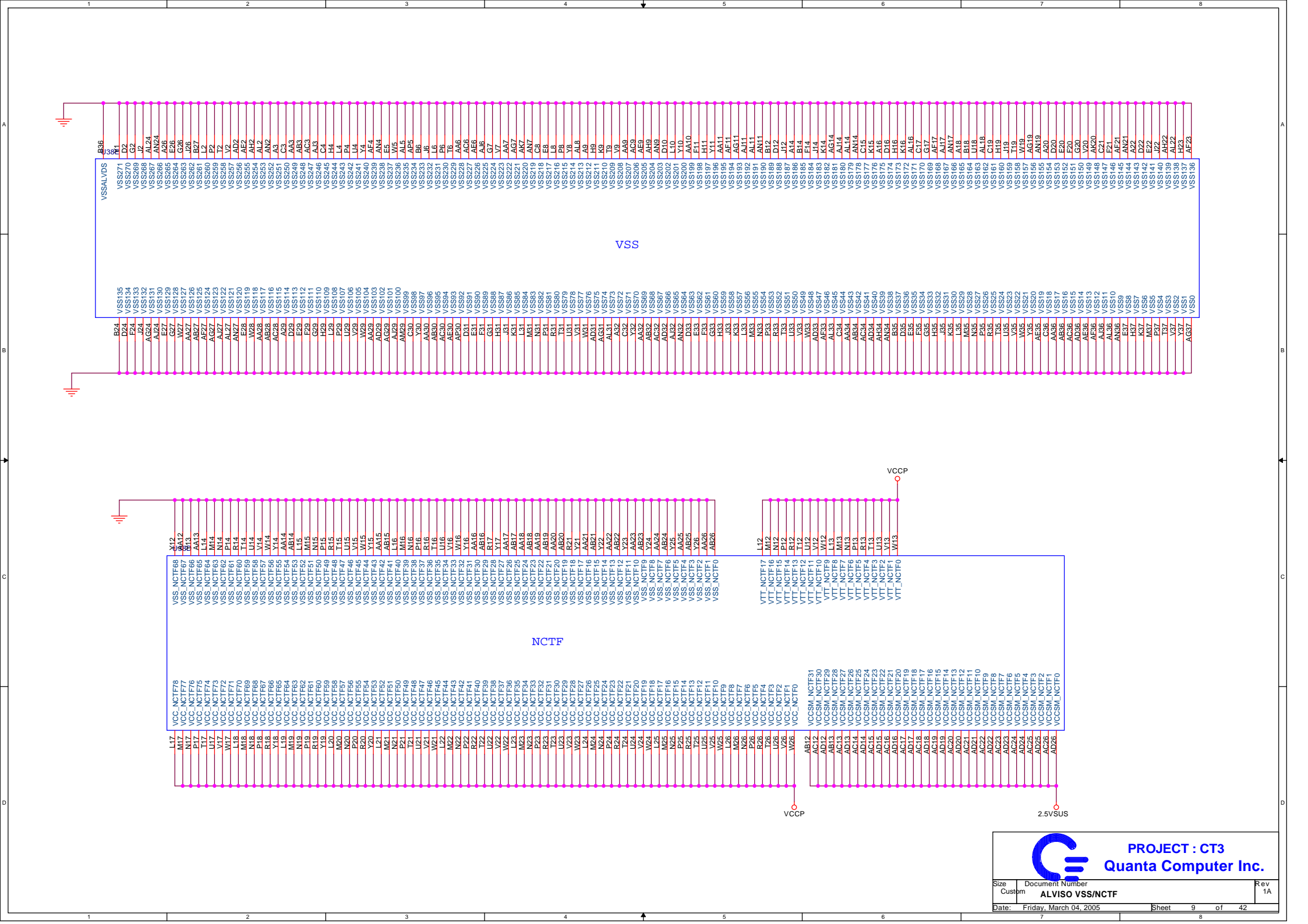
CFG[18:19] have internal pulldown.

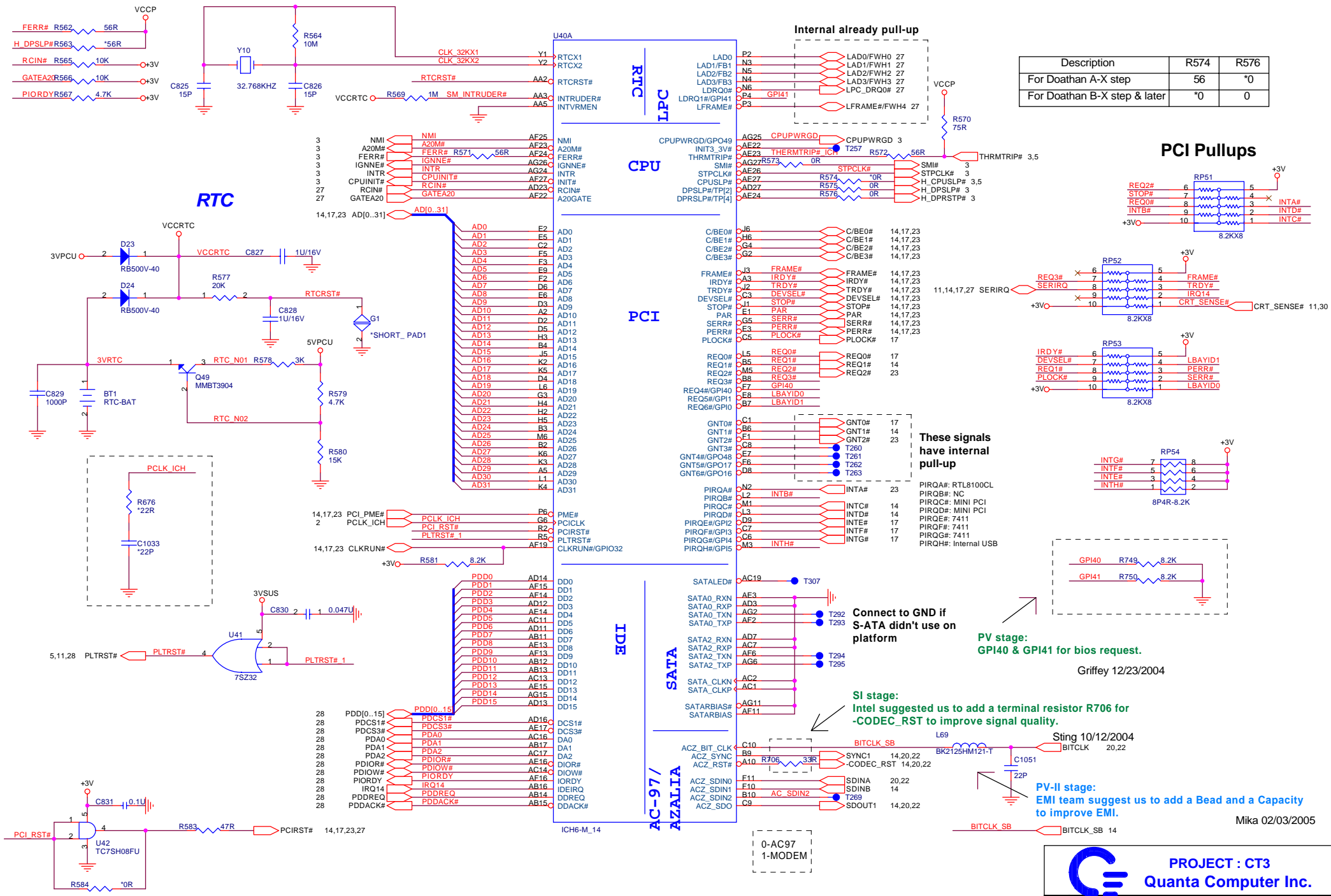






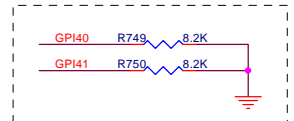
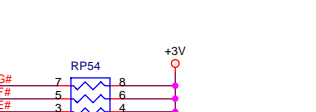
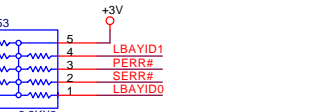
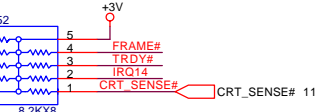
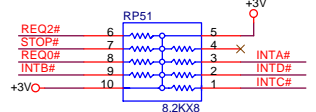






Description	R574	R576
For Doathan A-X step	56	*0
For Doathan B-X step & later	*0	0

PCI Pullups



These signals have internal pull-up

- PIRQA#: RTL8100CL
- PIRQB#: NC
- PIRQC#: MINI PCI
- PIRQD#: MINI PCI
- PIRQE#: 7411
- PIRQF#: 7411
- PIRQG#: 7411
- PIRQH#: Internal USB

Connect to GND if S-ATA didn't use on platform

SI stage: Intel suggested us to add a terminal resistor R706 for -CODEC\_RST to improve signal quality.

PV stage: GPI40 & GPI41 for bios request.

Griffey 12/23/2004

Sting 10/12/2004

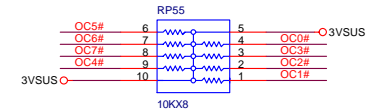
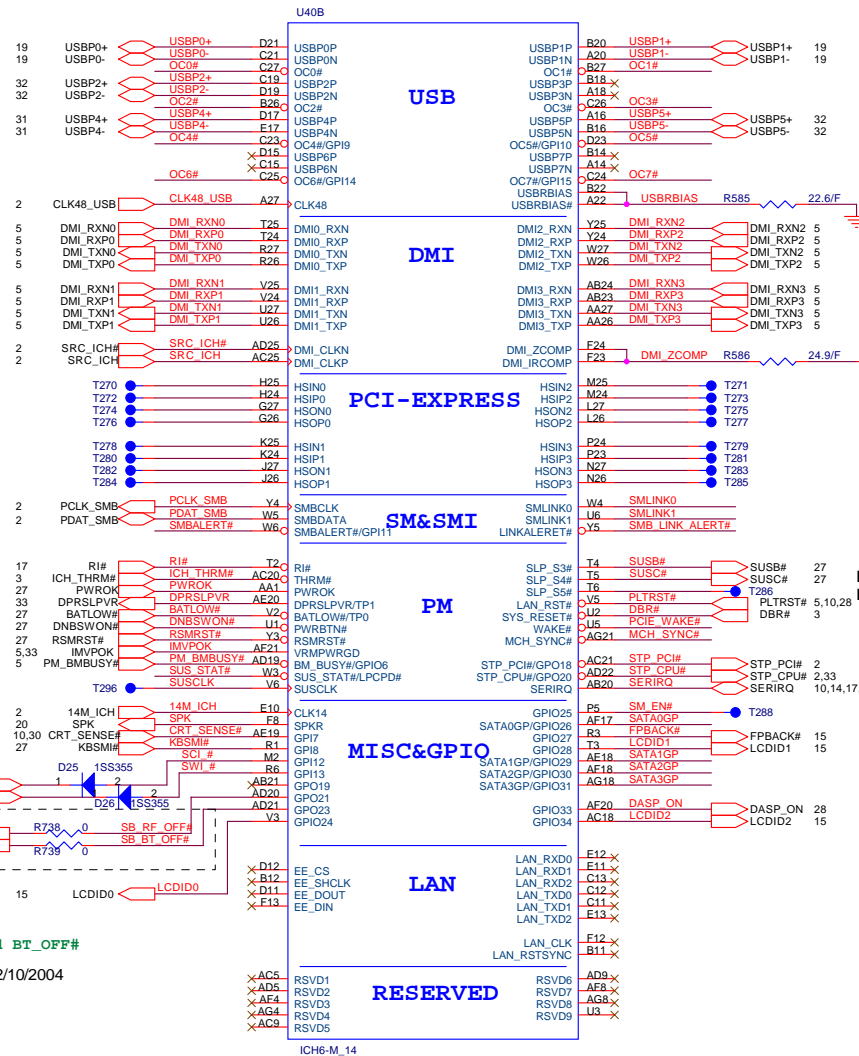
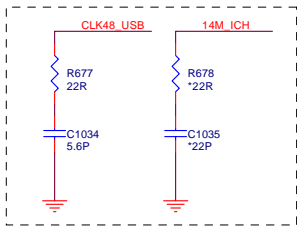
PV-II stage: EMI team suggest us to add a Bead and a Capacity to improve EMI.

Mika 02/03/2005

PROJECT : CT3

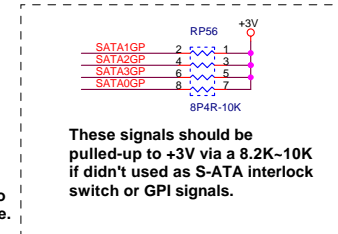
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH6-M (CPU/PCI/IDE)	3A
Date:	Friday, March 04, 2005	Sheet 10 of 42

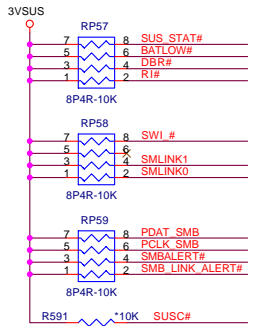
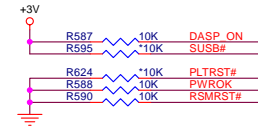


Place within 500mils of ICH-6

Place within 500mils of ICH-6

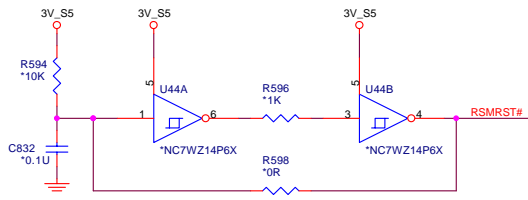


LAN\_RST# should be connected to PLTRST# if internal LAN didn't use.



PV stage:  
1. Add RF\_OFF# and BT\_OFF# circuit.

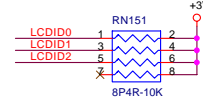
Griffey 12/10/2004



1. Change the power plane of PCIE\_WAKE# from 3VSUS to 3V\_S5 to solve system can't turn off issue.  
2. Change the power plane of ICH\_THRM# and SCI\_# from 3VSUS to +3V to solve leakage issue.

Sting 10/06/2004

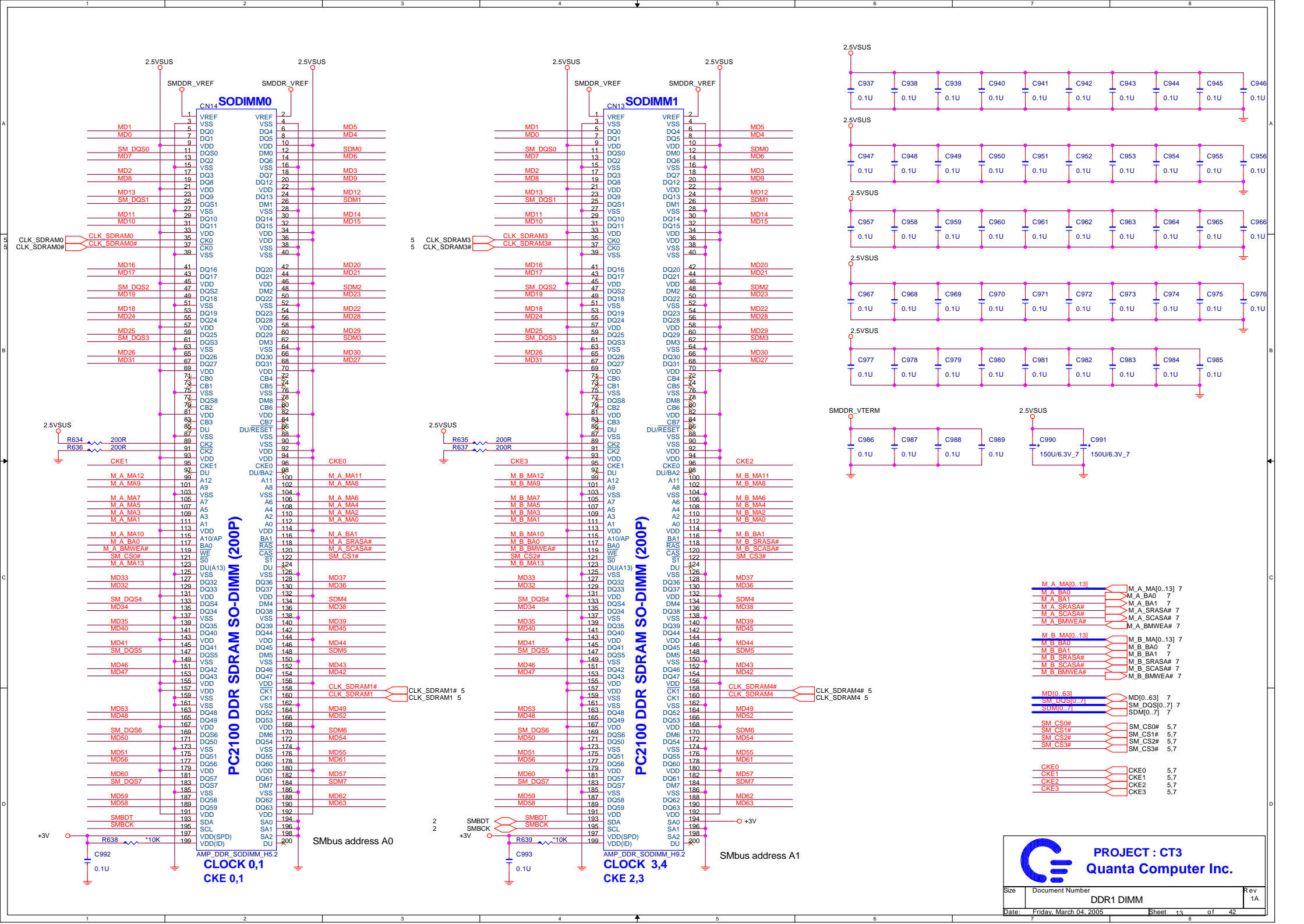
Enable Cable ID



SI stage:  
R589 should be populated, because MCH\_SYNC# is internally ANDed with PWROK. System will not booting without this pulled-up resistor.

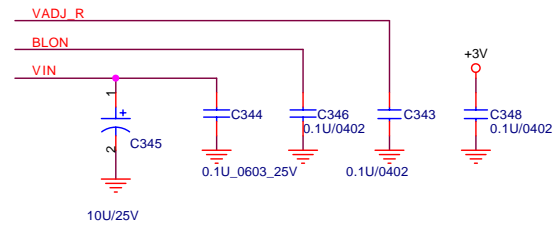
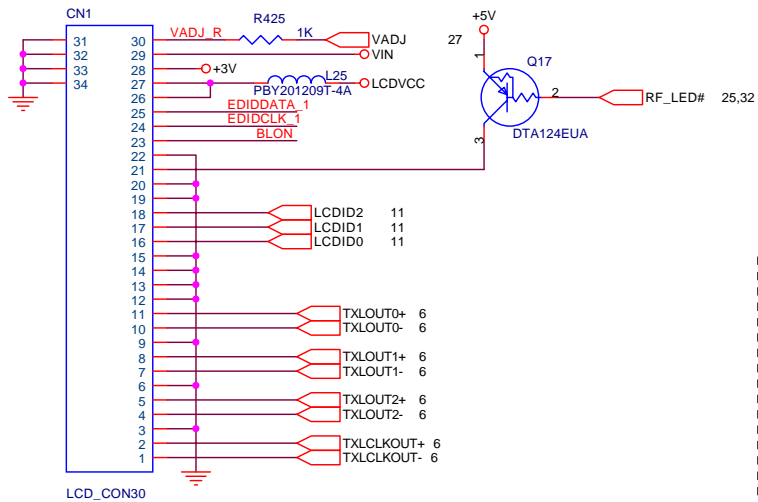
Sting 09/24/2004



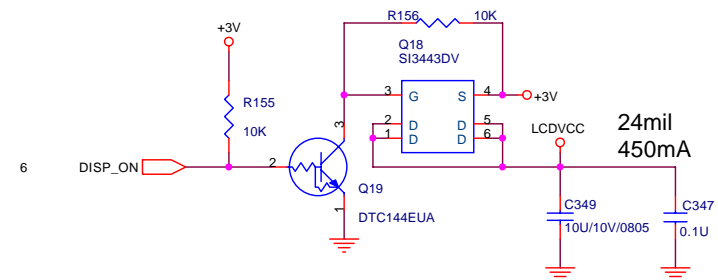
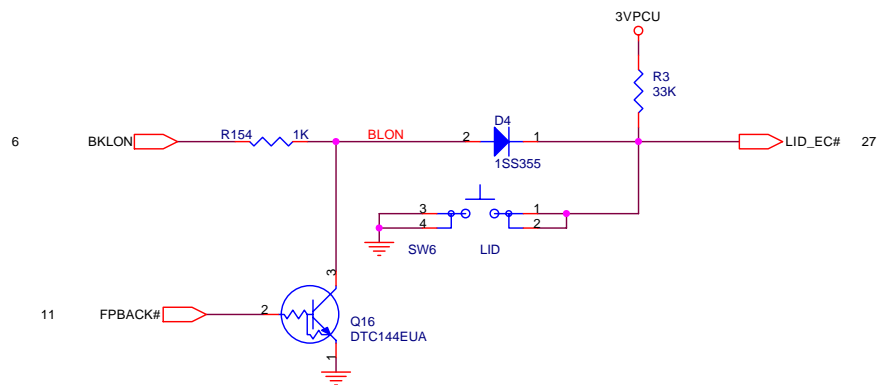
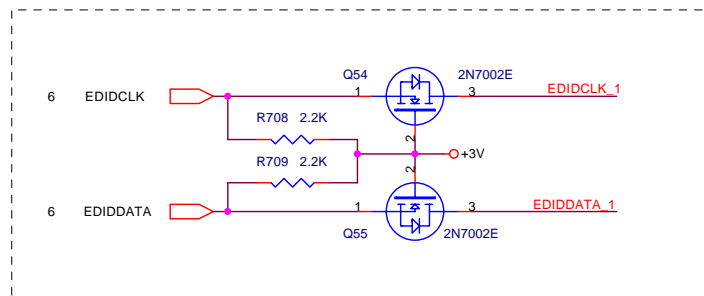




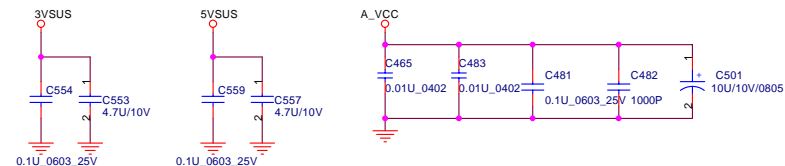




SI stage:  
Add a level-shift circuit for EDID interface.  
Sting 10/04/2004

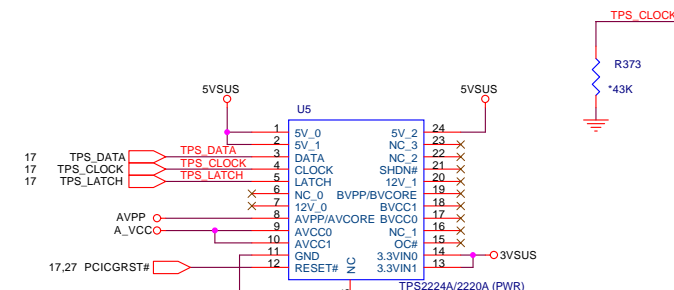


## CardBus Connector



## CARDBUS POWER SWITCH

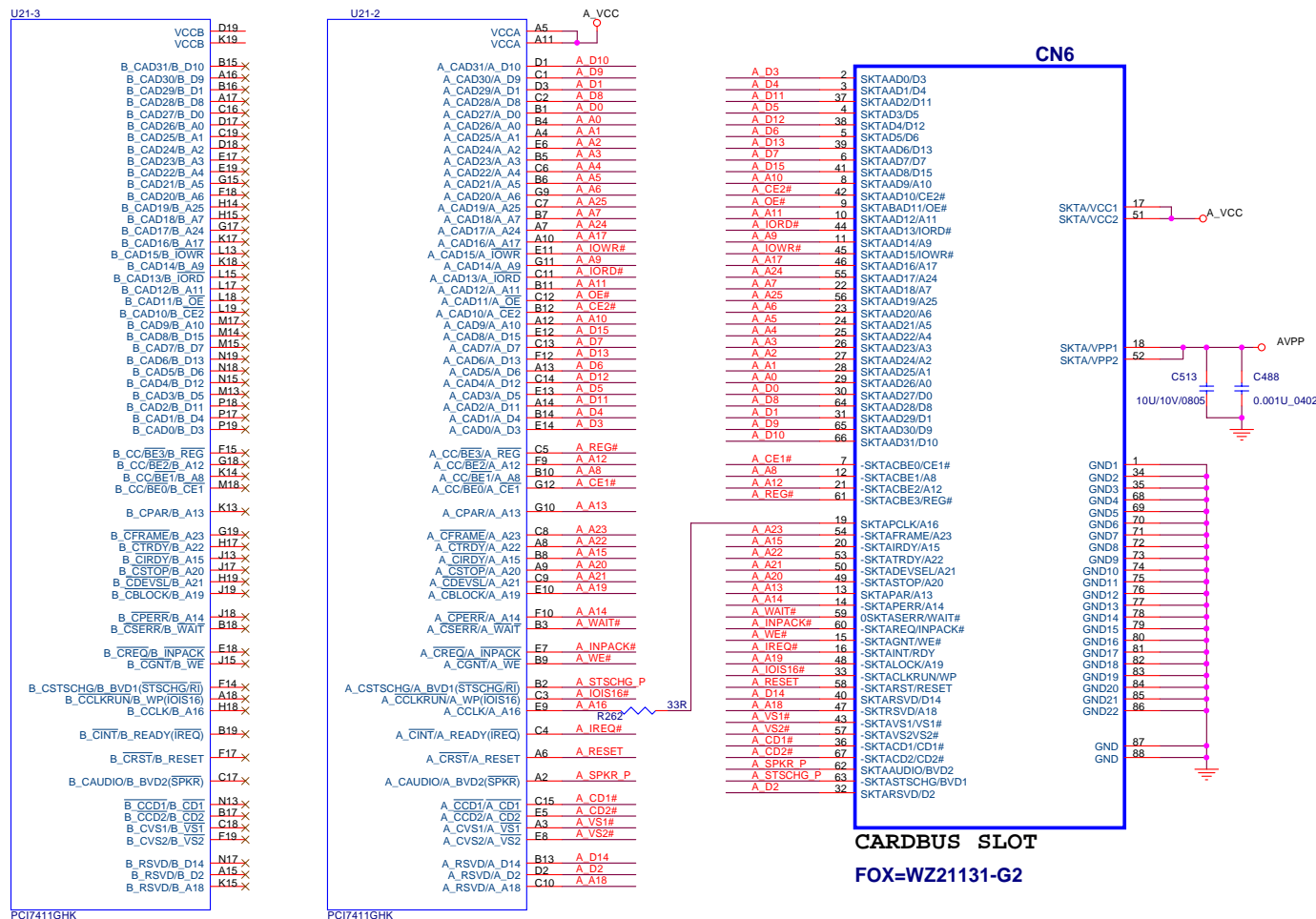
### For PCI7411



**For PCI1510**

**PV stage:**  
**Remove unused PCI1510RVGF circuit.**

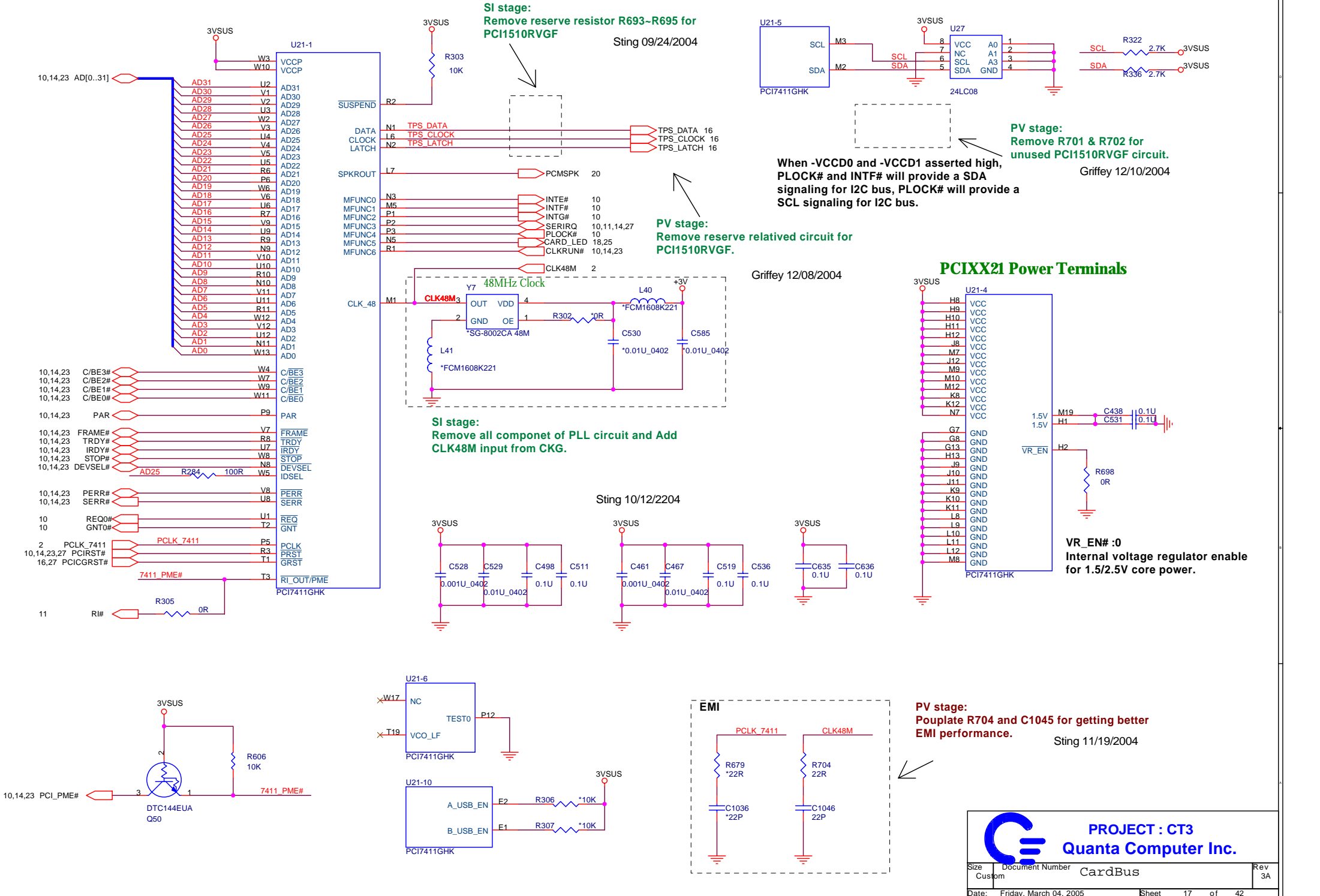
Griffey 12/08/2004



CARDBUS SLOT

FOX=WZ21131-G2

CardBus



## CARD POWER CONTROL

PV stage:  
Remove reserve relative circuit for  
PCI1510RVGF.  
Griffey 12/08/2004

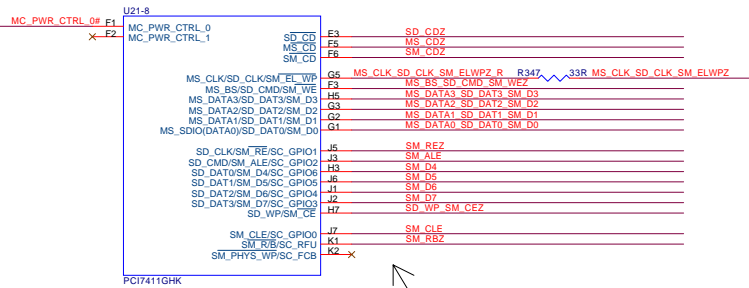
SI stage:  
Remove reserve resistor R696 fro  
PCI1510RVGF.  
Sting 10/12/2004

Reserve for smart card which is powered by 5V.

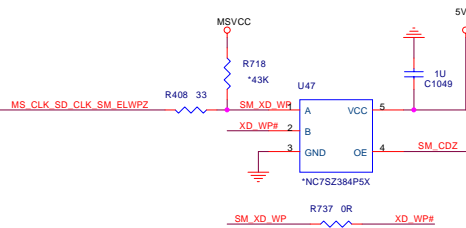
PV-II stage:  
Add a circuit for MS PRO DUO problem  
Mika 02/16/2005

PV stage:  
Add a discharge circuit for media  
card power.  
Sting 11/19/2004

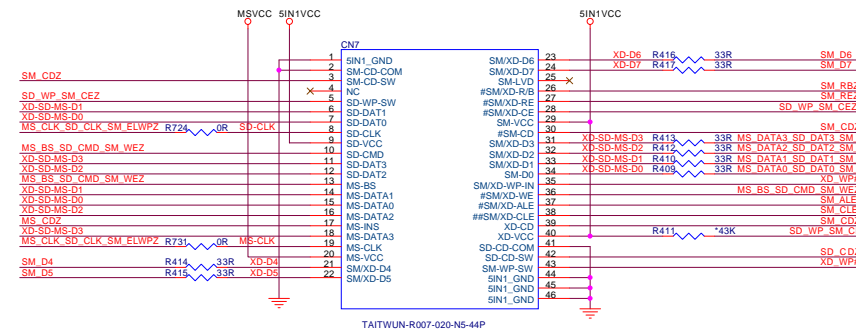
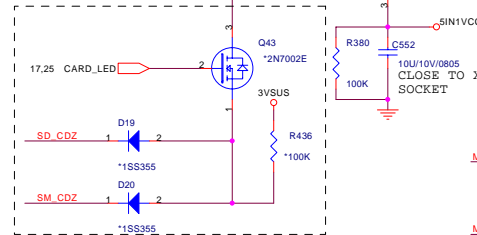
PV-II stage:  
Add a discharge circuit for media card power  
card power.  
Mika 02/16/2005



PV stage:  
1. Disconnect SM\_PHYS\_WP.  
2. Tie SM\_EL\_WP with SM\_PHYS\_WP of SM card to allow  
for normal operation of SD and SM.  
Sting 11/19/2004



PV stage:  
1. Add quick switch circuit.  
Griffey 12/10/2004



## 5 IN1 CARD READER

PV stage:  
1. Add pull-up circuit.  
Griffey 12/20/2004

PV stage:  
1. Add R717 to solve SM card can't write protect issue.  
2. Add R718 to solve cross-talk issue of MS-PRO card.  
3. Add R719-R736 as terminal on all multi-funtpin.  
Sting 11/19/2004

PV-II stage:change resistor value for card-reader  
R411 change to \*43K  
R409 change from 0R to 33R  
R410 change from 0R to 33R  
R412 change from 0R to 33R  
R413 change from 0R to 33R  
R414 change from 0R to 33R  
R415 change from 0R to 33R  
R416 change from 0R to 33R  
R417 change from 0R to 33R  
Mika 02/21/2005

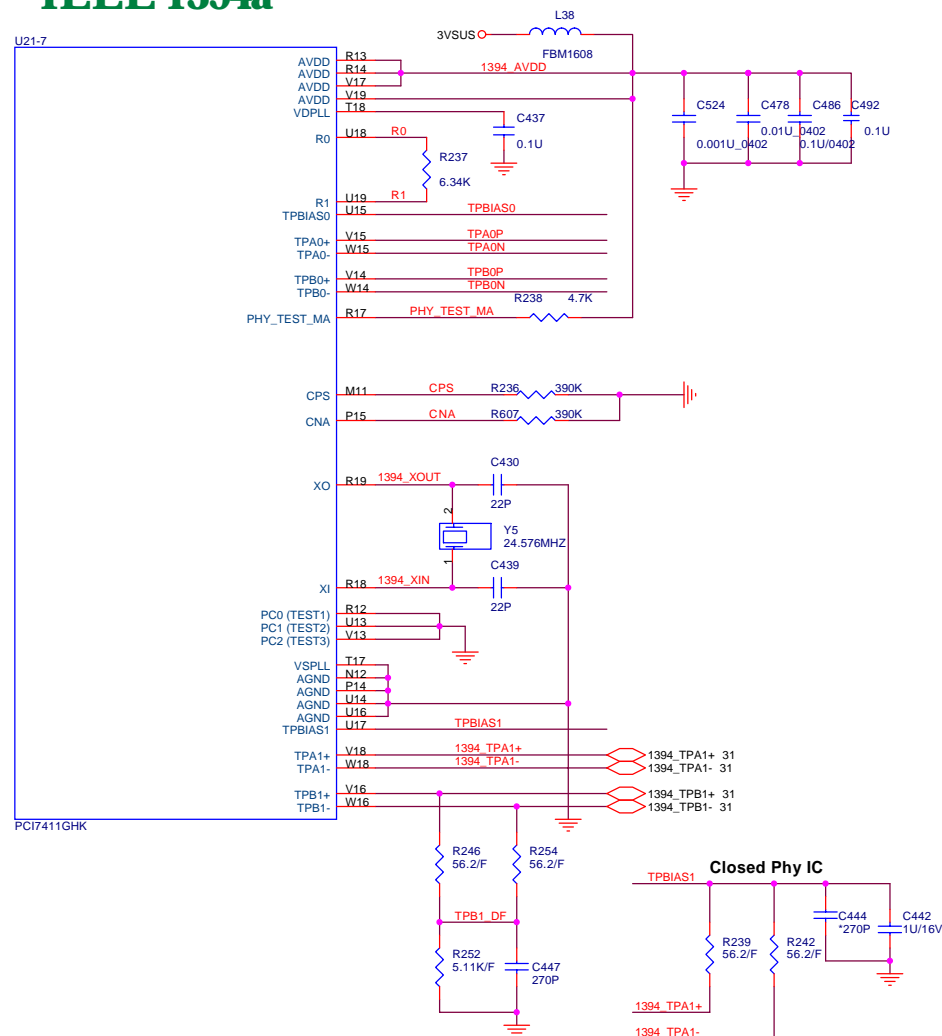
R742 change to \*10K  
R743 change to \*10K  
R744 change from 10k to 2.2K  
R745 change from 10k to 2.2K

R408 change from 3.3K to 33R  
R737 change to 0R  
R718 change to \*43K  
u47 change to \*NC7SZ384P5X

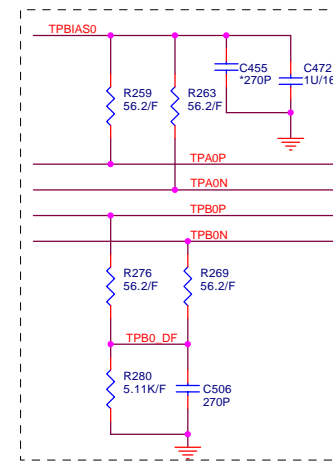


MV stage:  
1. reserve for 5VINVCC power  
Mika 03/04/2005

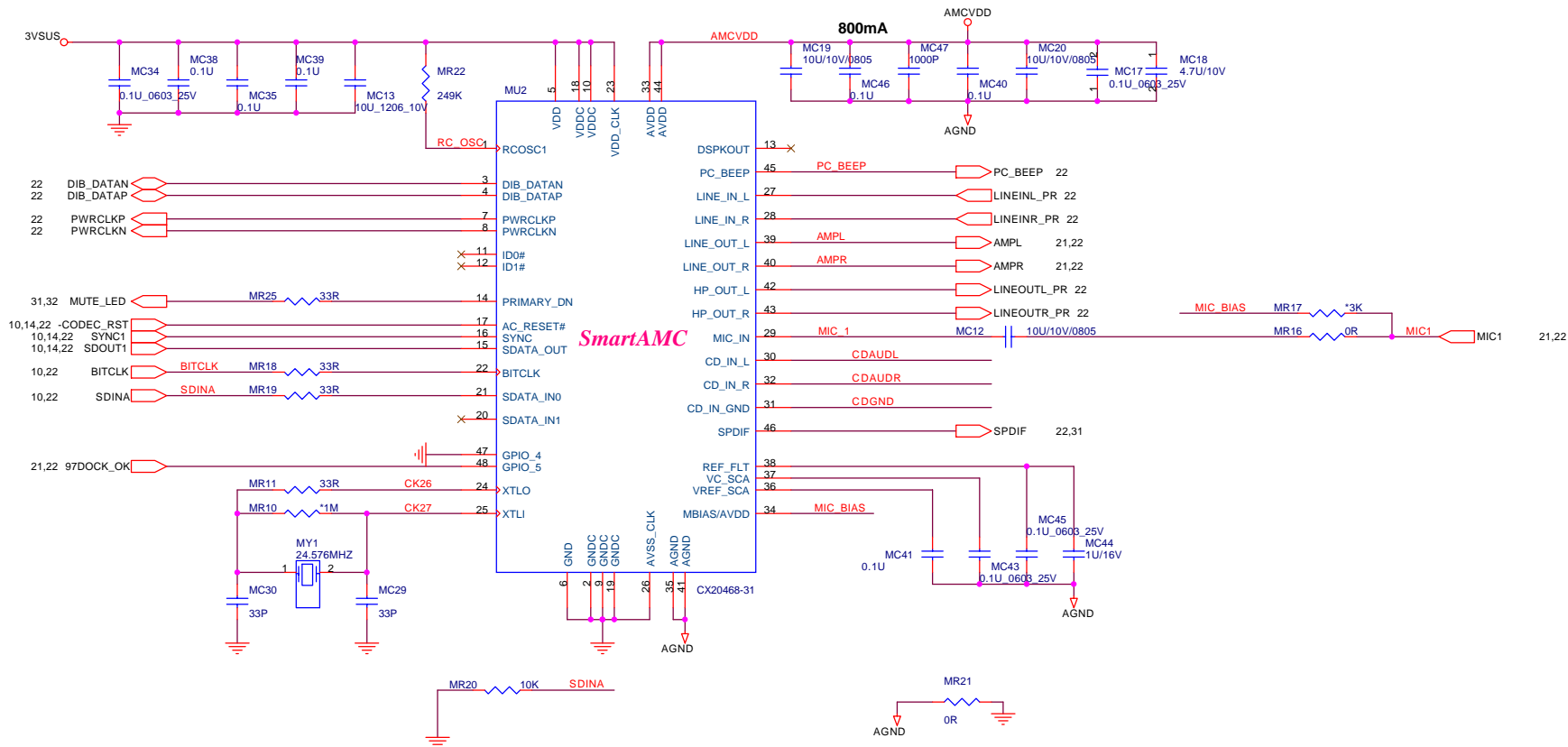
# IEEE 1394a



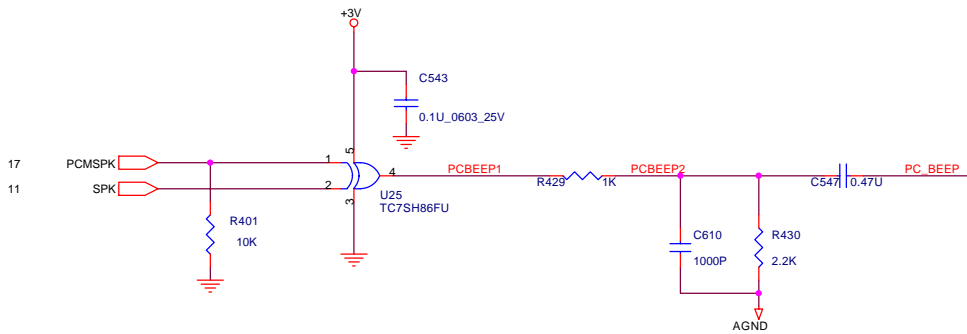
## IEEE 1394 CONNECTOR



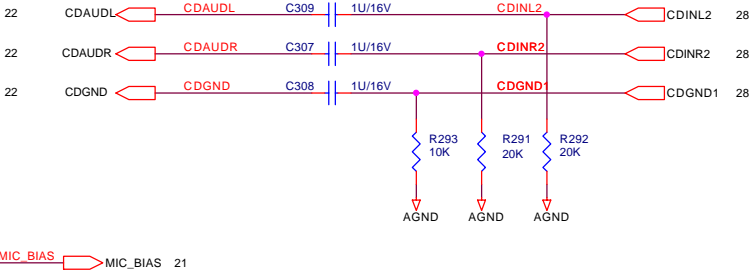
The AMC20493-001 modem is used for mother board family MBAMC20493-010.



PC SPEAKER

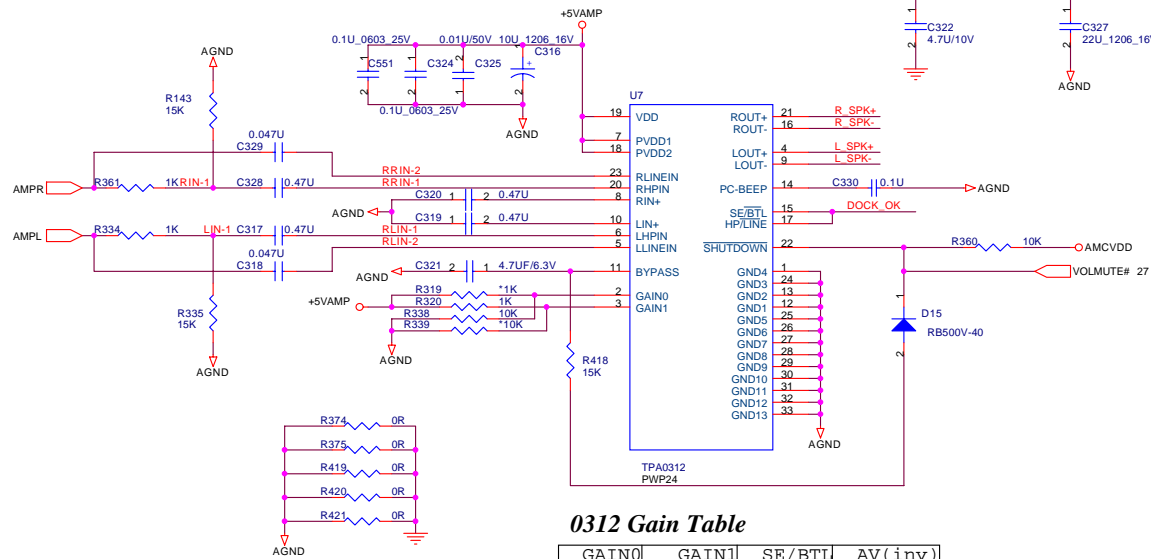


FROM CD-ROM





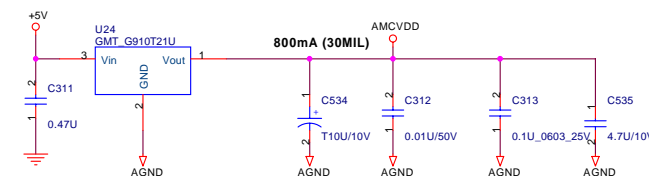
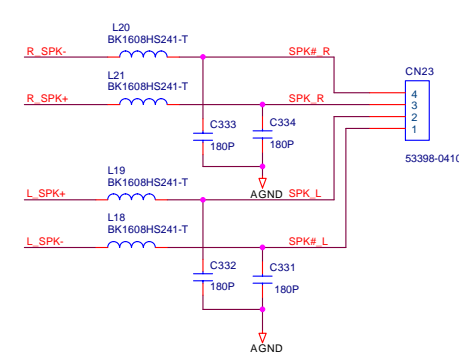
# AUDIO AMPLIFIER



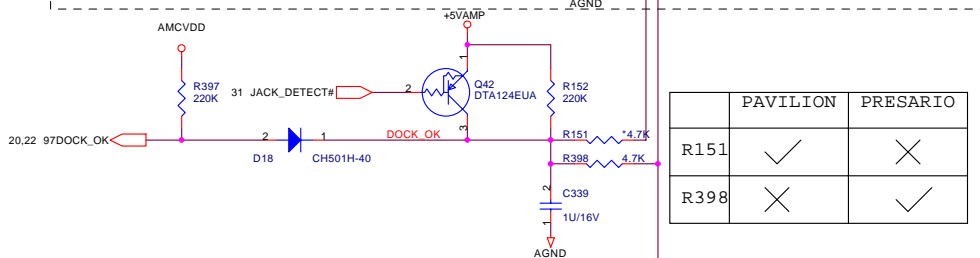
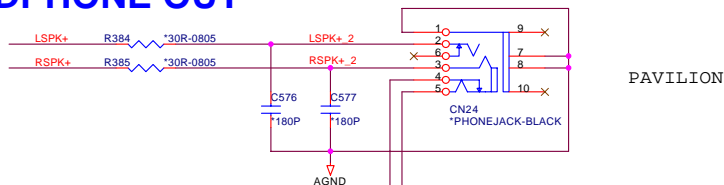
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

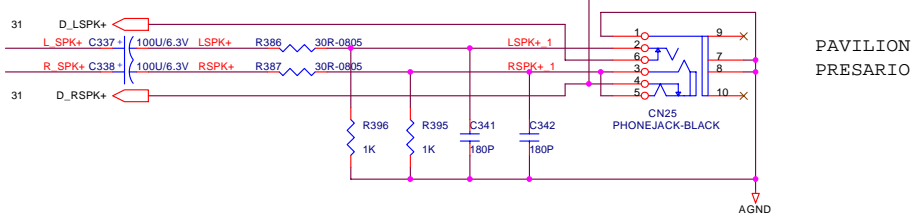
# SPEAKER OUT



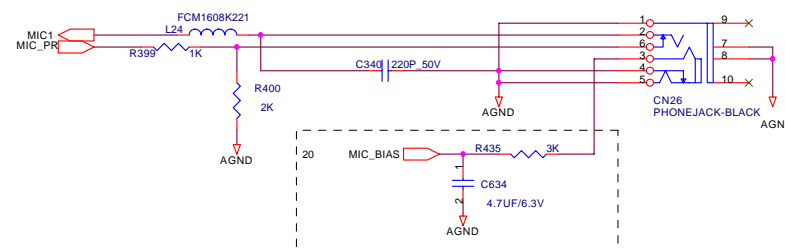
## 2ND HEADPHONE OUT

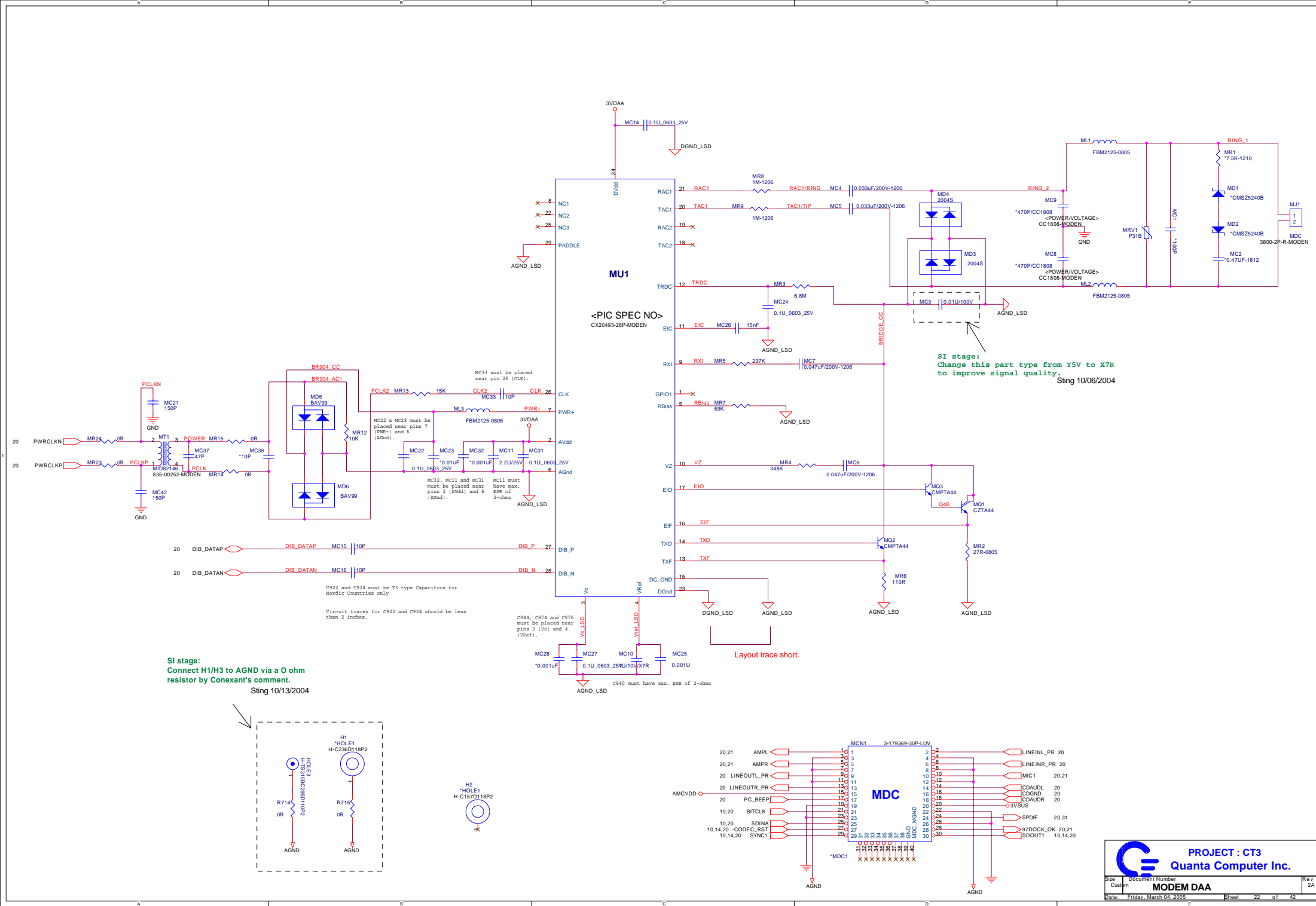


## HEADPHONE OUT



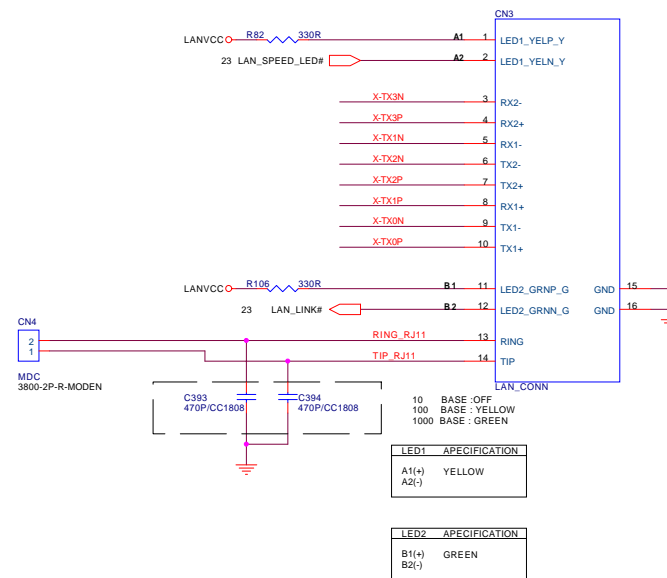
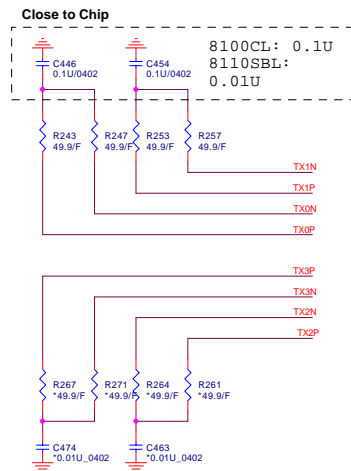
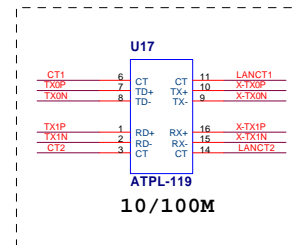
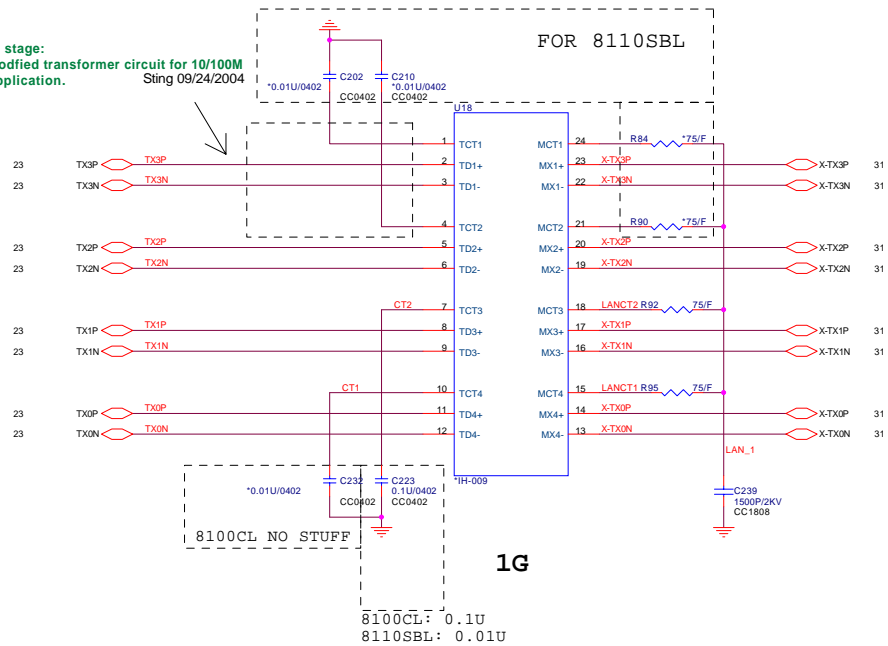
## MICROPHONE

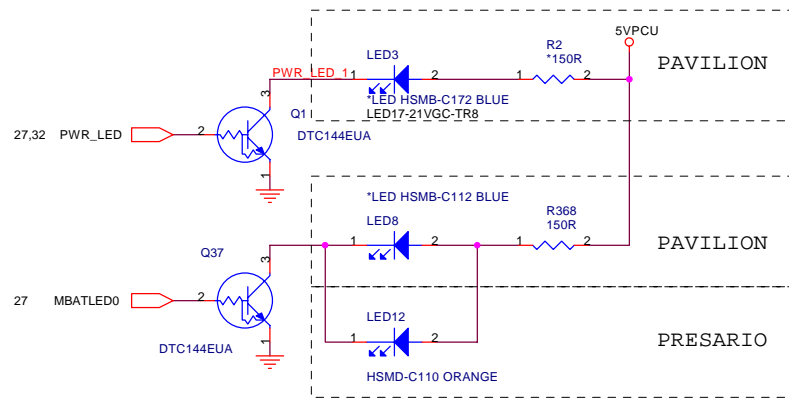




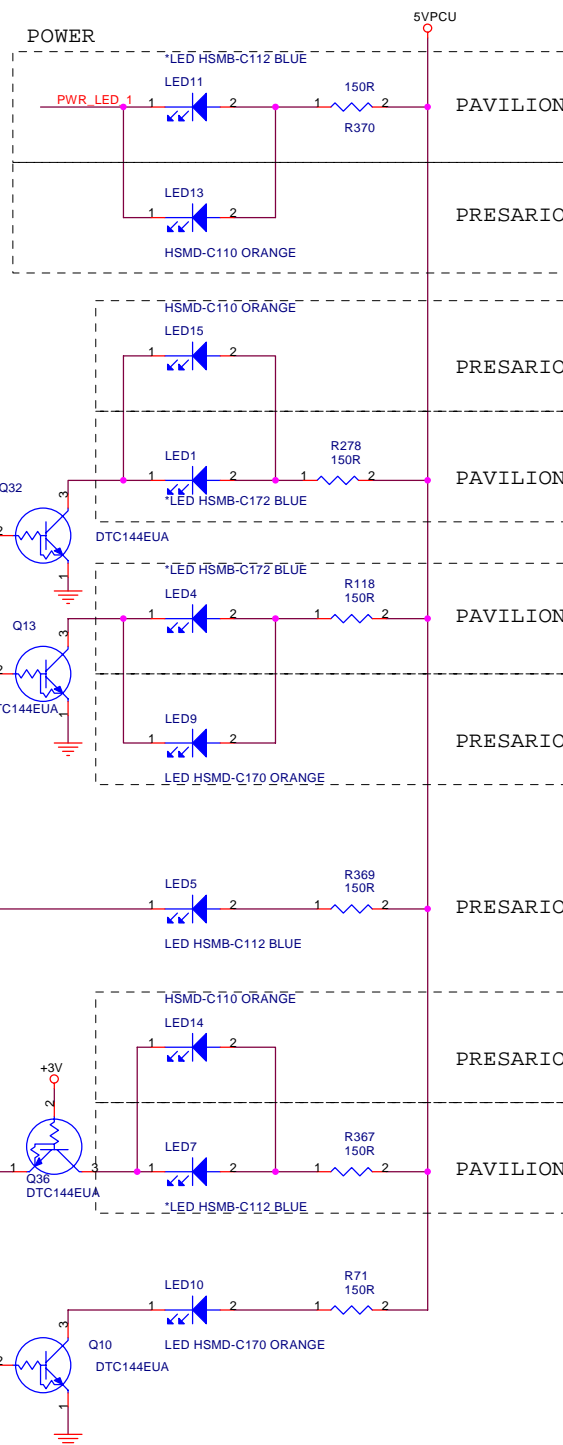
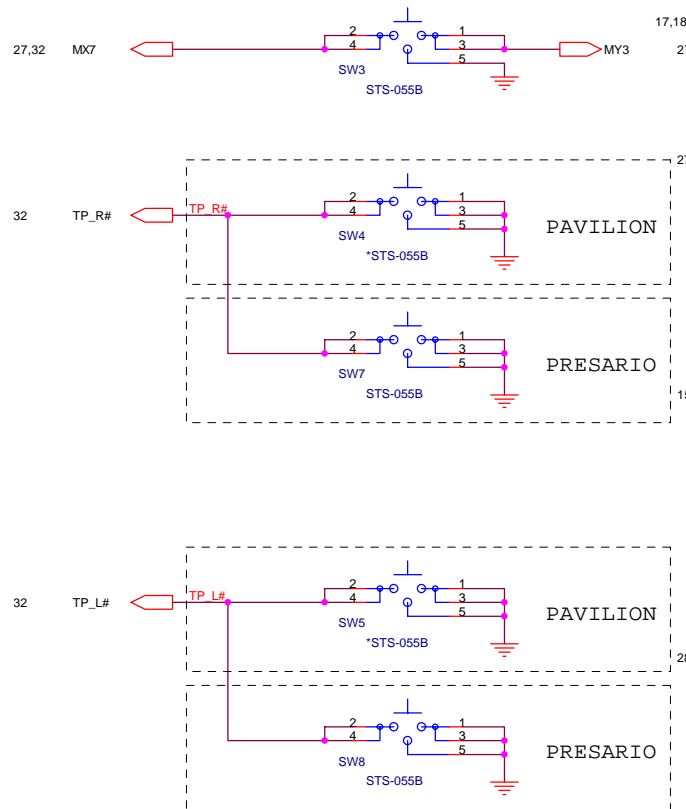


SI stage:  
Modified transformer circuit for 10/100M application.

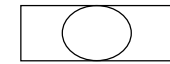




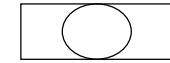
## Touchpad control



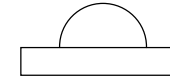
LED HSMD-C170 ORANGE



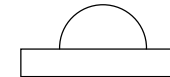
LED HSMB-C172 BLUE



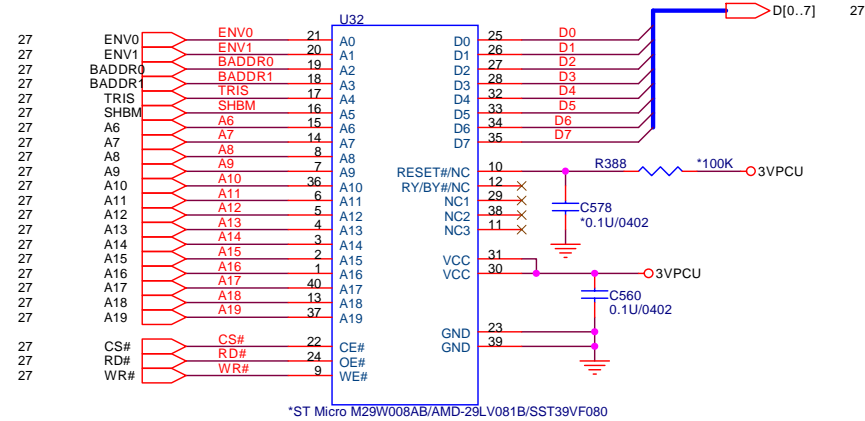
LED HSMD-C110 ORANGE



LED HSMD-C112 BLUE



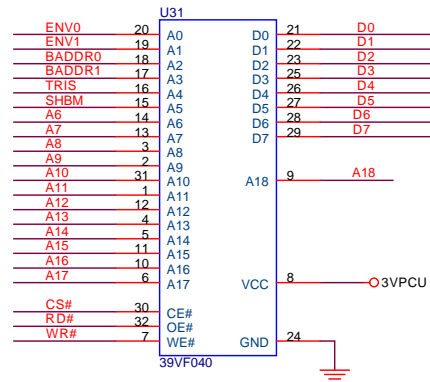
## 8Mbit (1M Byte), TSSOP40



- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326 \_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1\_PWROK

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#  
SST :Pin10,12 are NC

## 4Mbit (512k Byte), TSSOP32

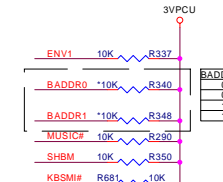
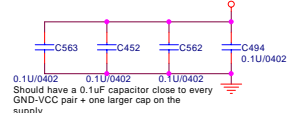
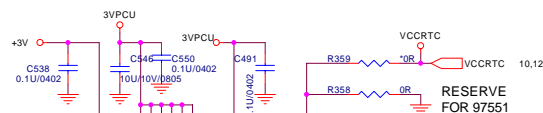
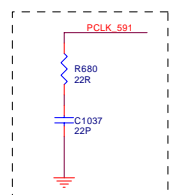


SI stage:  
Add PLCC32 cause of it is convenient for Bios debugging.  
Sting 10/01/2004

PV-II stage:  
Delete PLCC32 for SMT request  
Mika 02/03/2005

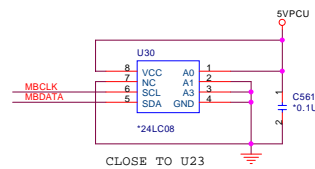


KBC-NS87551L



I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)	
1 1	Reserved	

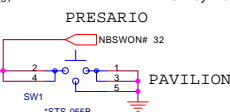
SHBM=1: Enable shared memory with host BIOS



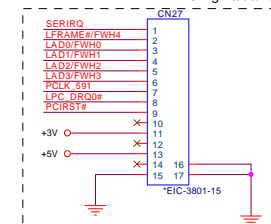
CLOSE TO U23 

PV stage:  
1. Reserve 0R for RF\_OFF#  
and BT\_OFF# circuit.

Griffey 12/11/2004



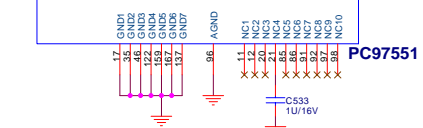
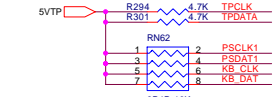
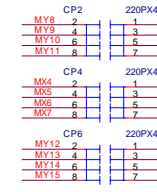
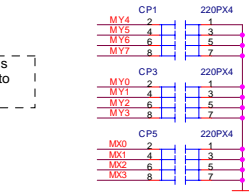
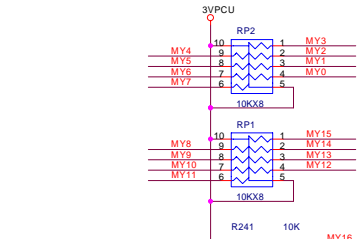
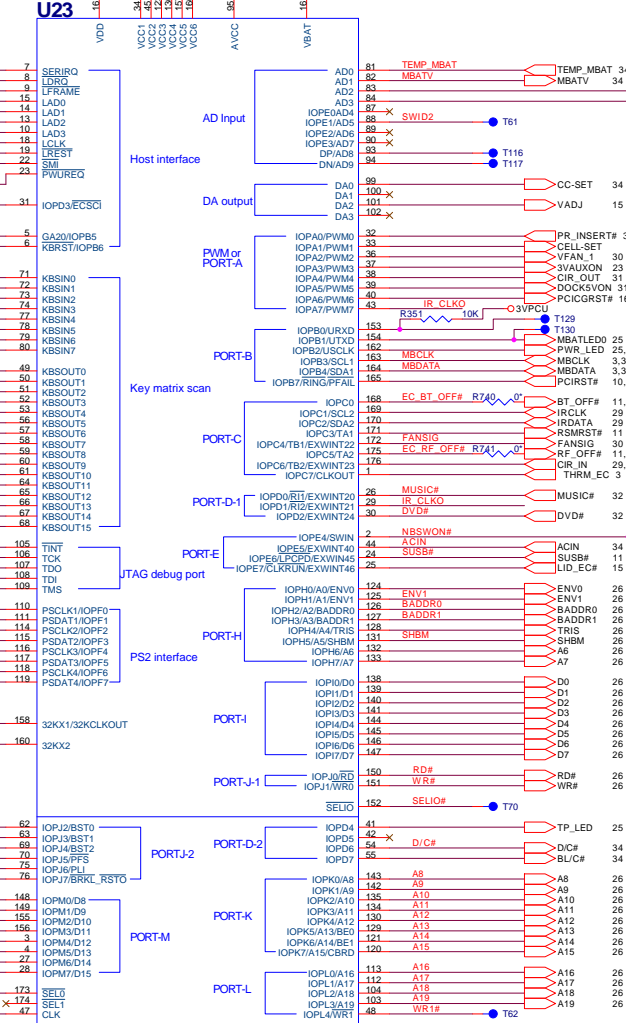
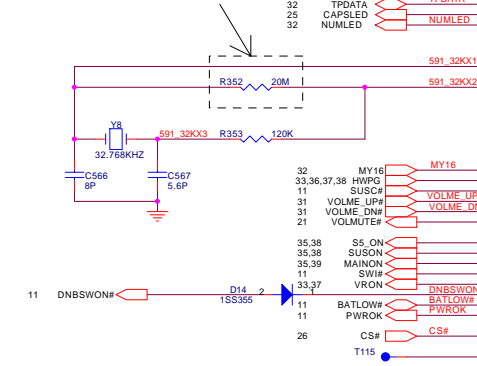
Pin 24 if no pull-  
will can't reboot.



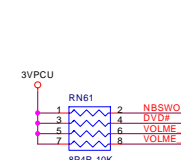
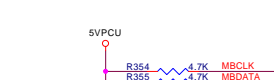
PV stage:  
Modify pin name. Griffey 12/10/200

SI stage:  
Change R352 value from 120K to 20M.  
Sting 09/24/2004

Sting 09/24/2004

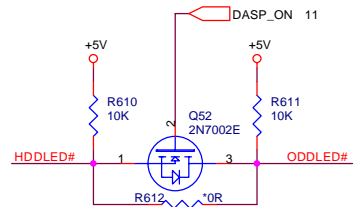


Pin 103 internal is "A19", Can't use to GPIO

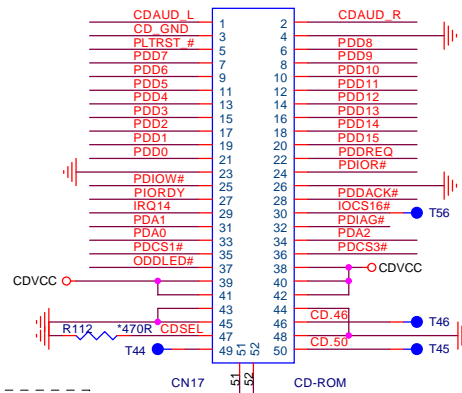


## HDD, CD-ROM

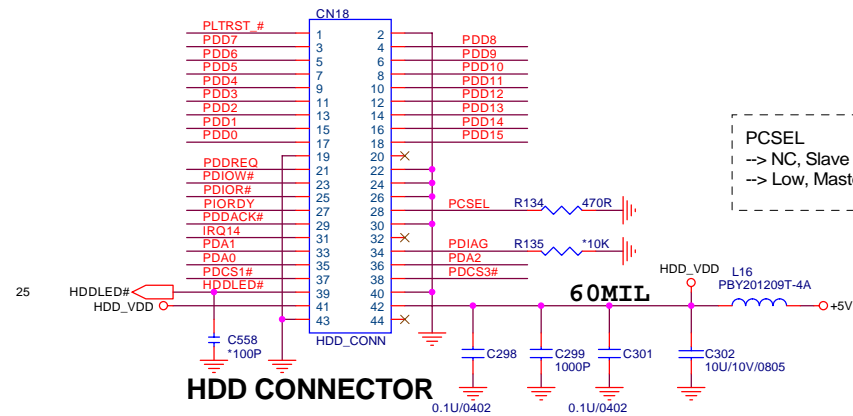
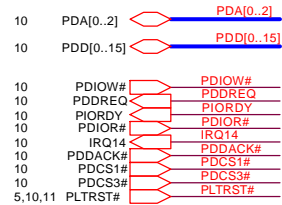
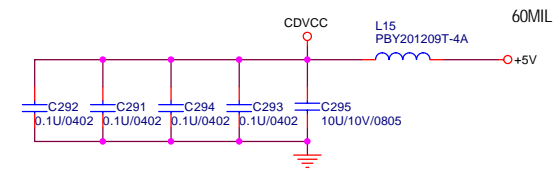
## CD-ROM



ADD DASP\_ON FOR IDE CABLE SELECT



- | CDSEL
- | --> NC, Slave device
- | --> Low, Master device



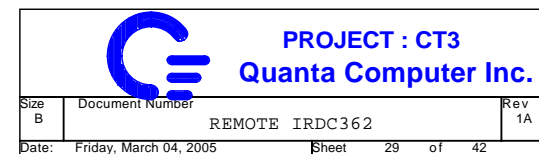
- | PCSEL
- | --> NC, Slave device
- | --> Low, Master device

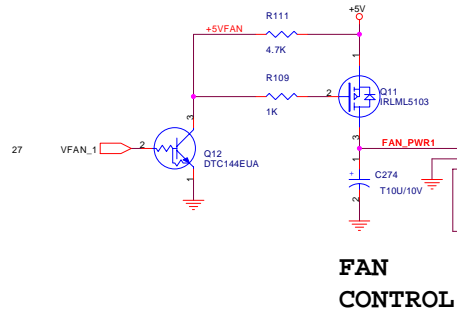
## HDD CONNECTOR



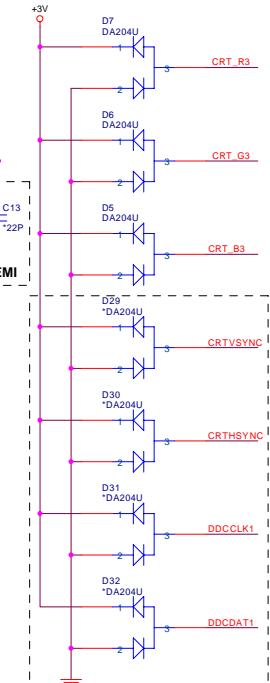
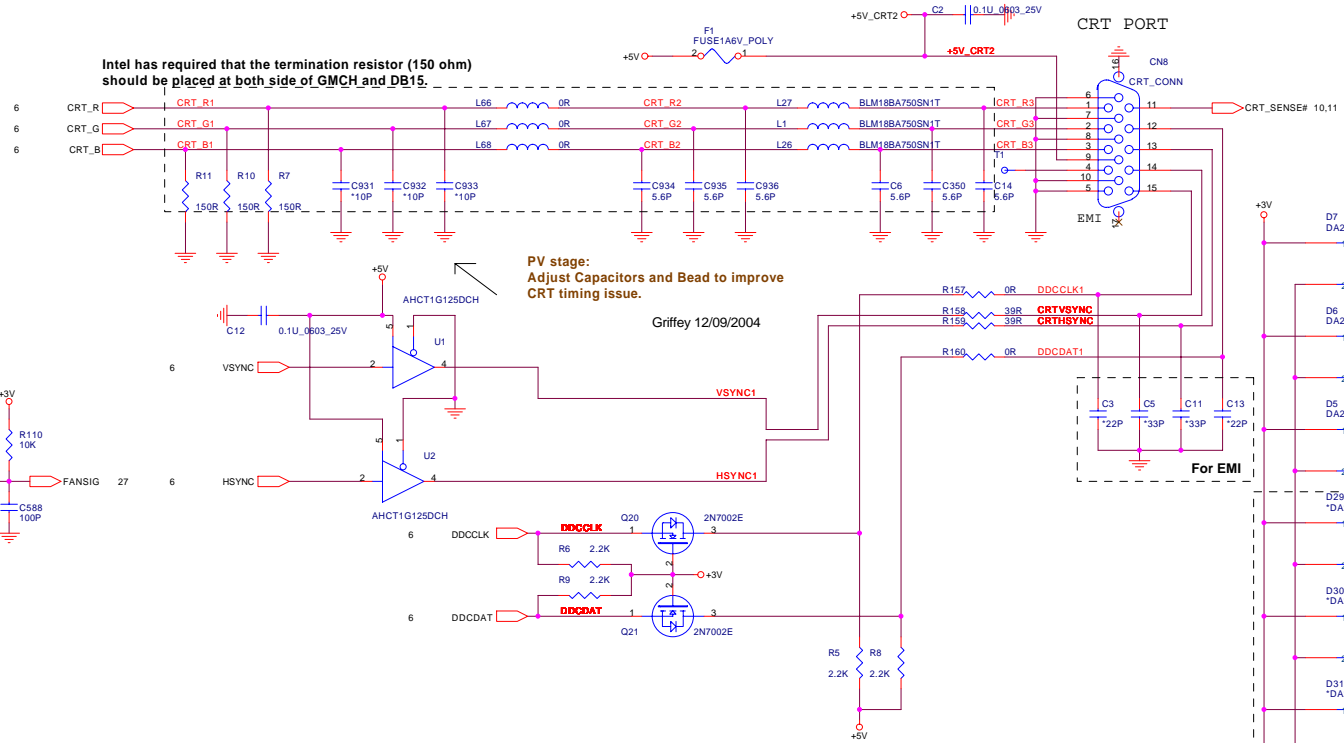
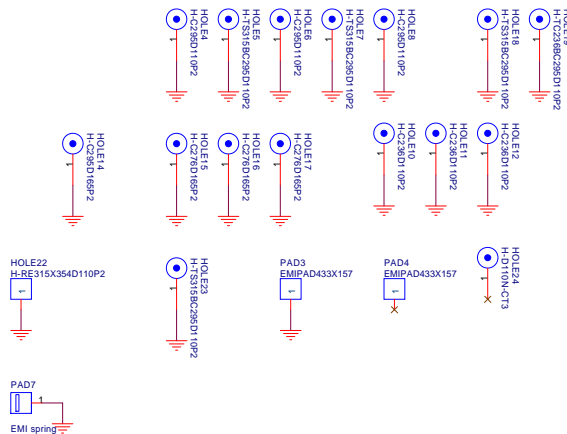
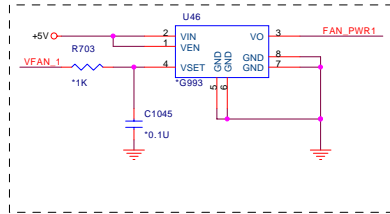
PROJECT : CT3  
Quanta Computer Inc.

Size Custom	Document Number <b>HDD&amp;ODD CONN.</b>	Rev 2A
Date: Friday, March 04, 2005	Sheet 28 of 42	

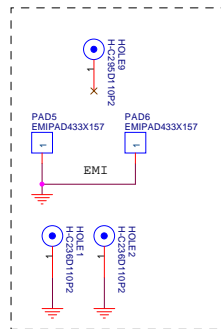


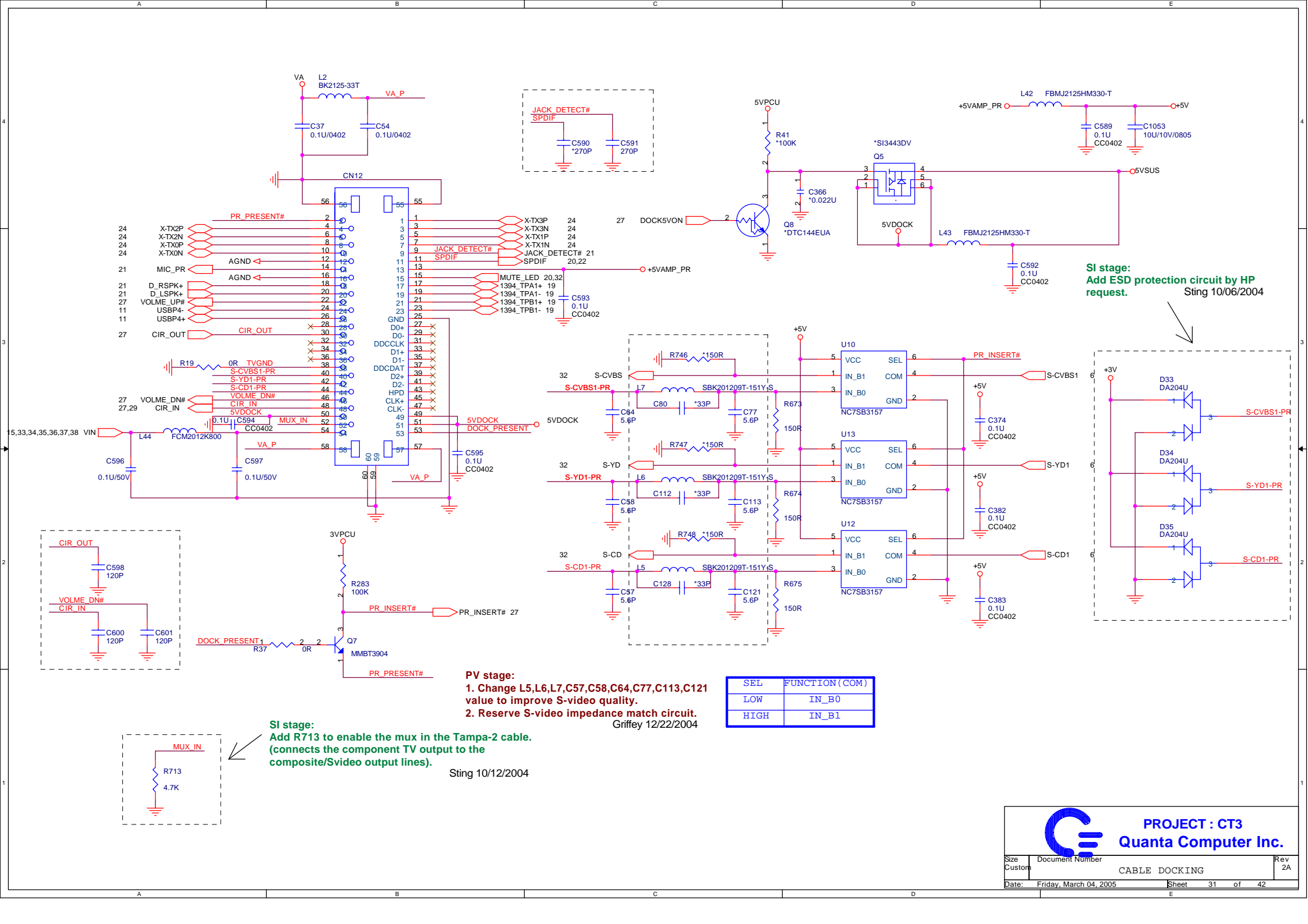


SI stage:  
Add GMT solution for B-test to costdown.  
Sting 09/24/2004



Add ESD protection by Sting 08/03/2004





**PV stage:**  
1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.  
2. Reserve S-video impedance match circuit.  
Griffey 12/22/2004

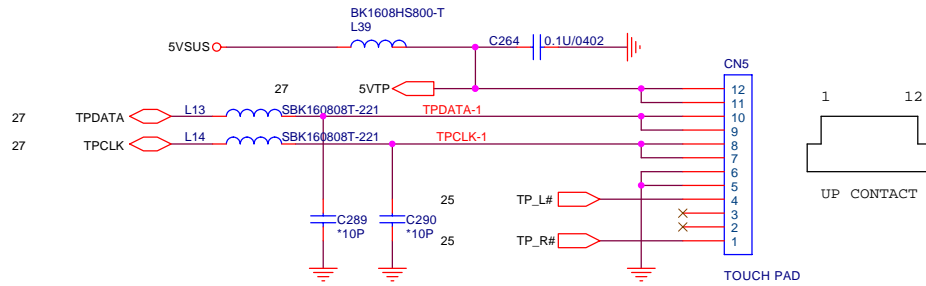
SEL	FUNCTION (COM)
LOW	IN_B0
HIGH	IN_B1

**SI stage:**  
Add R713 to enable the mux in the Tampa-2 cable.  
(connects the component TV output to the composite/Svideo output lines).

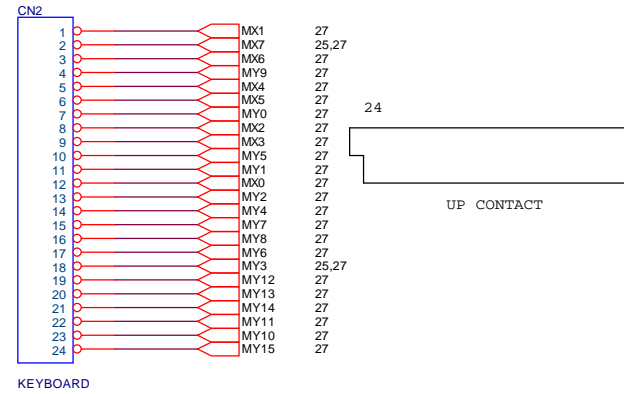
Sting 10/12/2004

**SI stage:**  
Add ESD protection circuit by HP request.  
Sting 10/06/2004

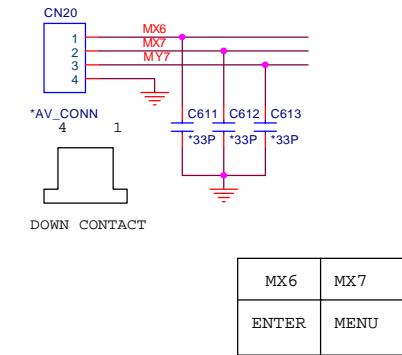
## TOUCH PAD CONNECTOR



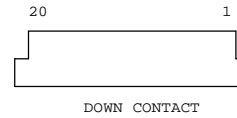
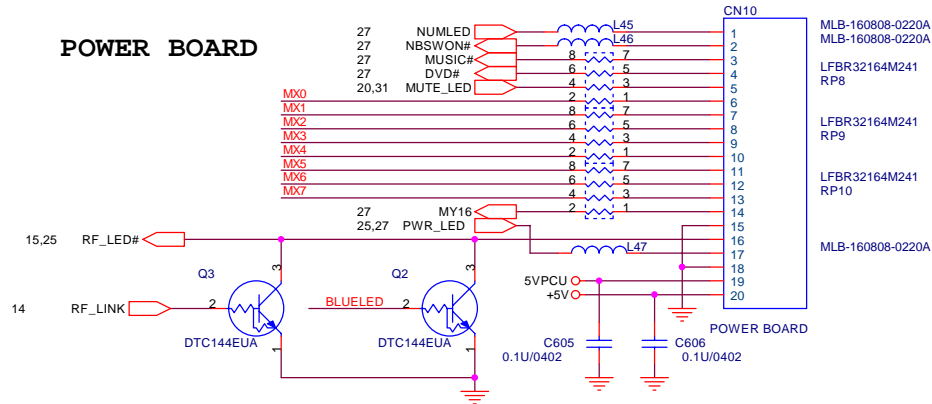
## KEYBOARD CONNECTOR



## AV BOARD

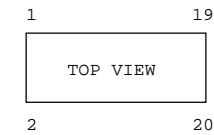
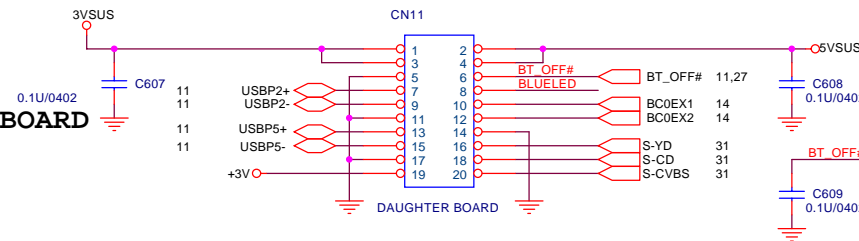


## POWER BOARD



MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

## DAUGHTER BOARD



PROJECT : CT3  
Quanta Computer Inc.

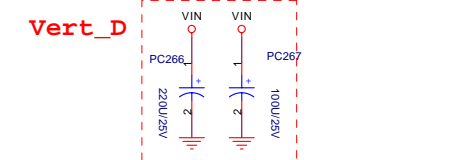
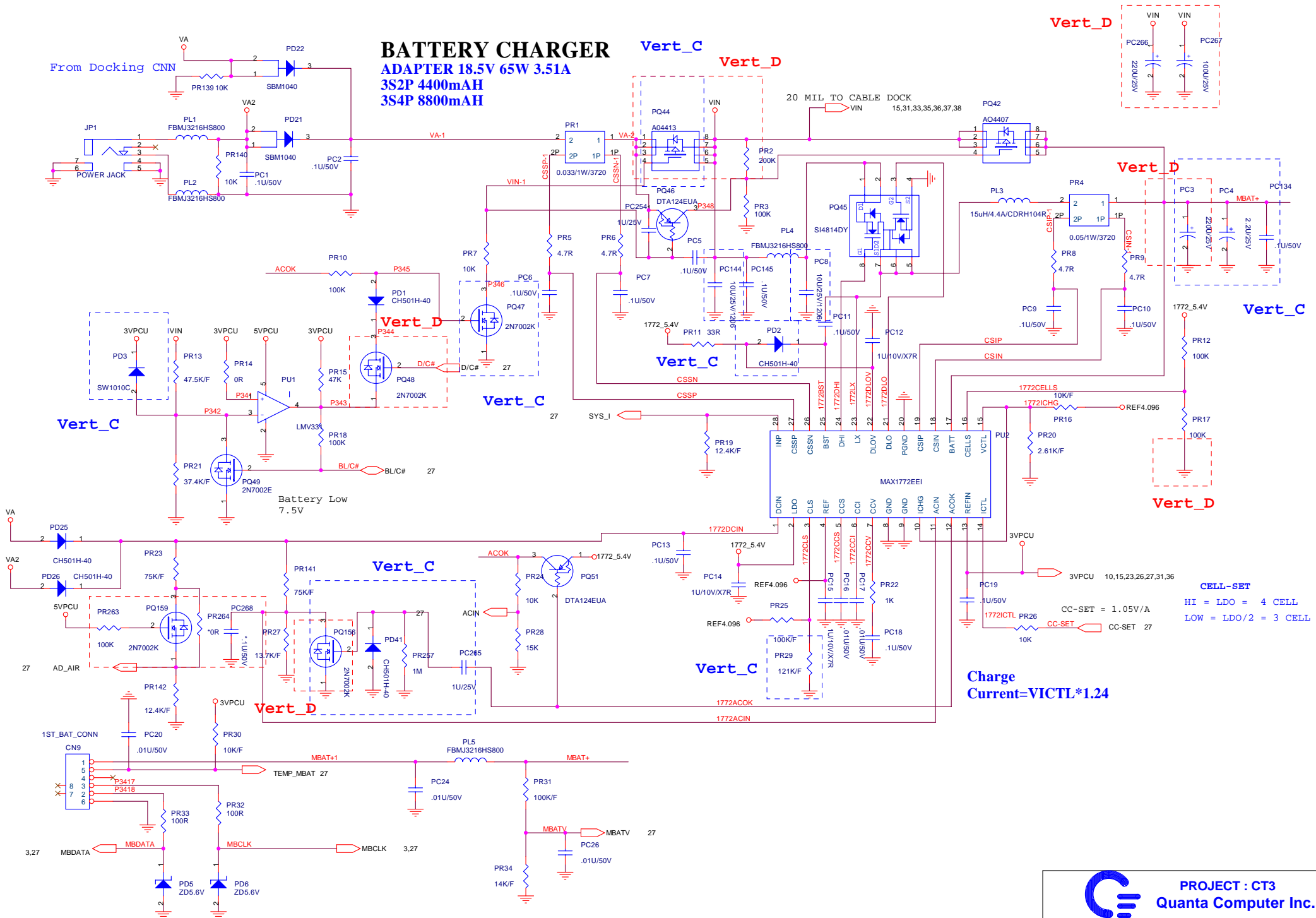
Size	Document Number	Rev
Custom	BLUETOOTH/TP/BTB	1A
Date:	Friday, March 04, 2005	Sheet 32 of 42





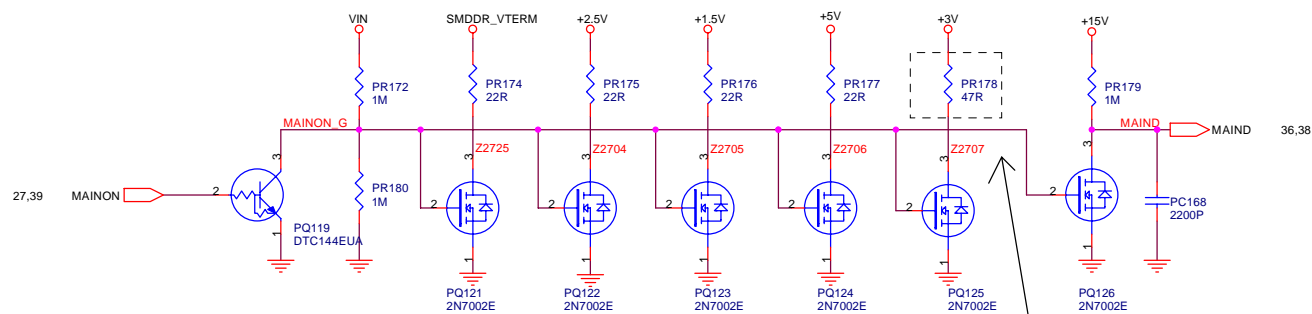
# BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A  
3S2P 4400mAh  
3S4P 8800mAh



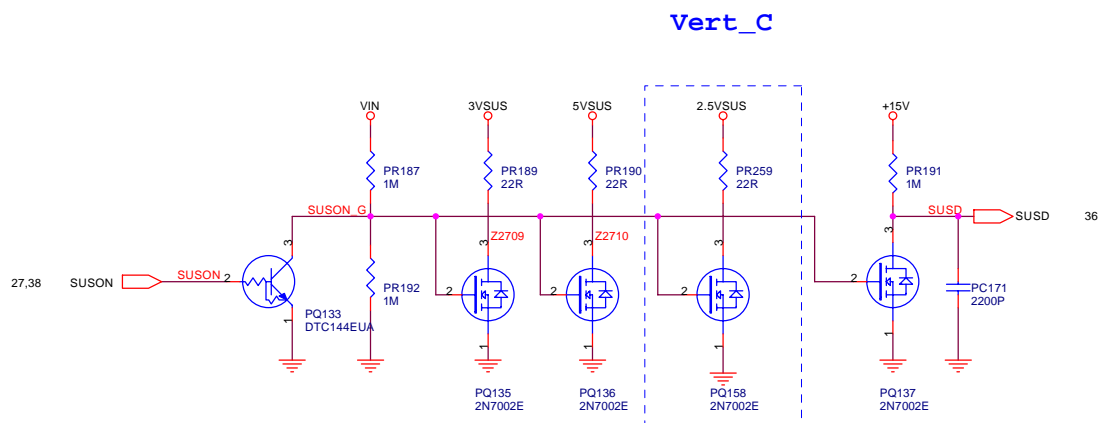
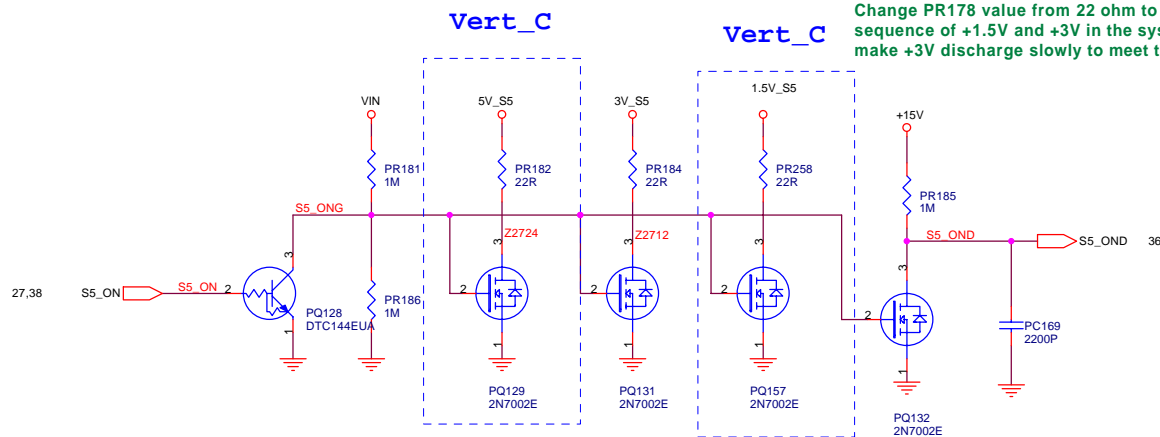
Charge  
Current=VICTL\*1.24

CELL-SET  
HI = LDO = 4 CELL  
LOW = LDO/2 = 3 CELL



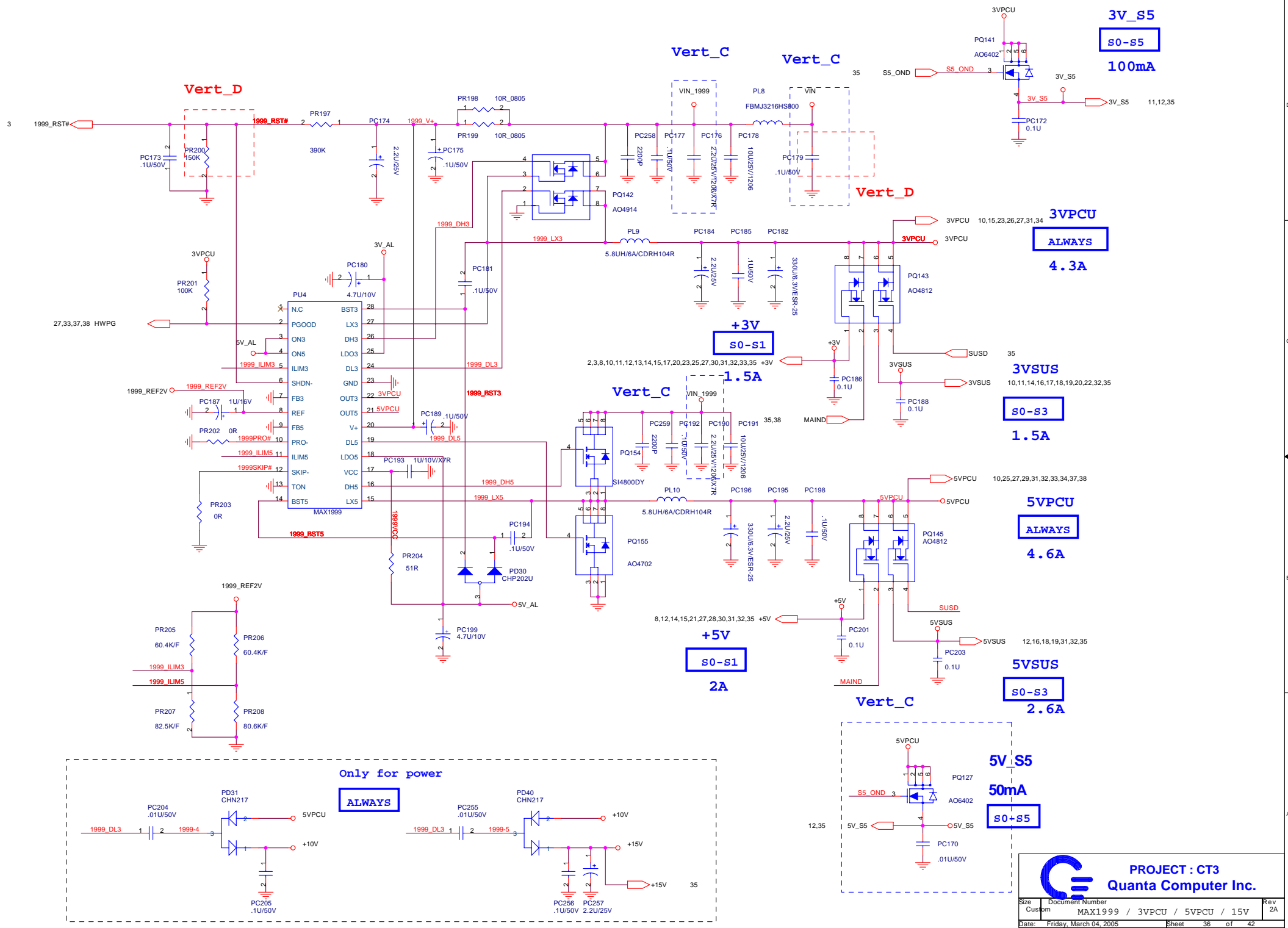
SI stage:  
Change PR178 value from 22 ohm to 47 ohm, Intel has required the timing sequence of +1.5V and +3V in the system, we'd like to increase the value to make +3V discharge slowly to meet the specification of falling time.

Sting 10/19/2004



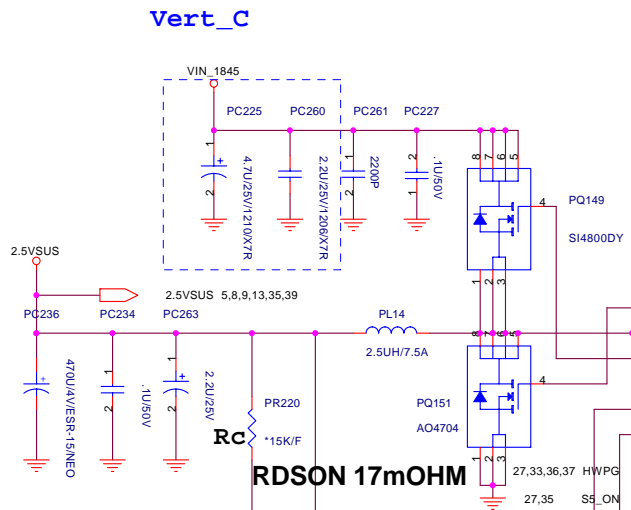
PROJECT : CT3  
Quanta Computer Inc.

Size	Document Number	Rev
Custom		2A
DISCHARGE		
Date	Friday, March 04, 2005	Sheet 35 of 42

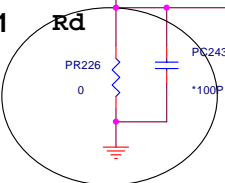




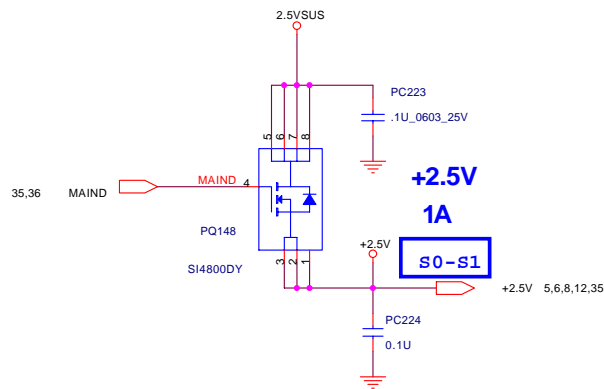
2.5VSUS  
6.5A  
S0-S3



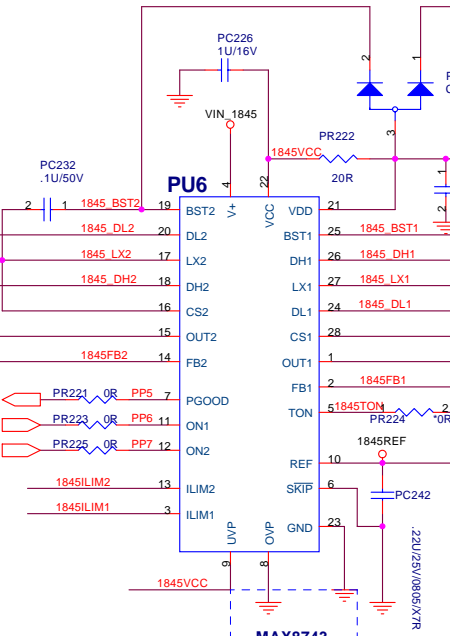
$$V_{out}=(1+R_c/R_d)*1$$



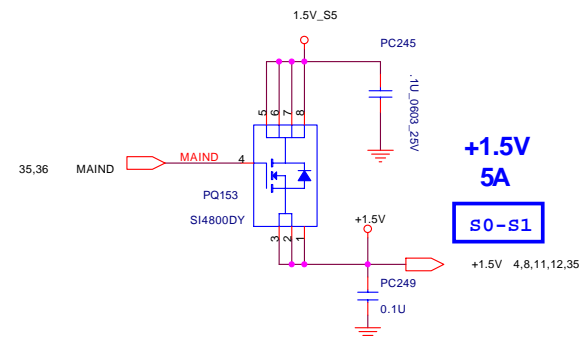
Fix 2.5V Output



+2.5V  
1A  
S0-S1



Fix 1.5V Output



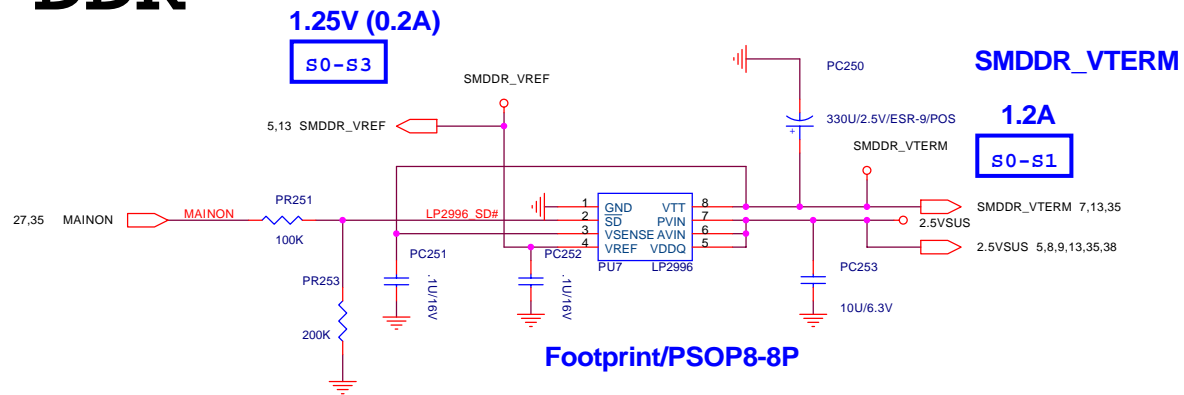
+1.5V  
5A  
S0-S1



PROJECT : CT3  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	2.5VSUS / 1.5V_S5	2A
Date:	Friday, March 04, 2005	Sheet 38 of 42


# DDR




PROJECT : CT3  
Quanta Computer Inc.


Size	Document Number	Rev
Custom	DDR_VTERM	2A
Date:	Friday, March 04, 2005	Sheet 39 of 42



MODEL	REV	CHANGE LIST	Model	CT3/5 MB BOARD	
			Page	FROM	TO
CT3/5 MB 31CT3MB0015 31CT3MB0031	1A	PAGE 2 --- Enable CLK48M from clock generator for the PLL circuit of 7411, and disable the ocsillator circuit of PCI7411 PLL. PAGE 3 --- Remove H/W shutdown circuit that supported ADM1032.  PAGE 4 --- Use X7R type to replace Y5V type for CPU Decoupling/Bypass capacitor.  PAGE 10 --- Add a terminal resistor R706 for -CODE_RST# to improve signal quality.  PAGE 11 --- 1. Add a 10K pull-up resistor on MCH_SYNC# for booting. 2. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue. 3. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to reduce leakage.  PAGE 12 --- We can also use 5VSUS to instead of 5V_S5 to save cost of MOSFET(A06402).  PAGE 15 --- Add a level-shift cicuit for EDID interface.  PAGE 17 --- 1. Add a off-page and a EMI solution for CLK48M. 2. Remove the reserve resistors (R693-R695) of parallel interface for PCI1510.  PAGE 18 --- Remove R696, connect controller and power switch directly .  PAGE 19 --- Change R682&R683 value from 56 ohms to 0 ohm cause of BOM error at A-test.  PAGE 22 --- 1. Change MC3 type from Y5V to X7R to improve singal quality. 2. Connect H1/H3 to AGND via a 0 ohm resistor by Conexant's comment.  PAGE 23 --- 1. Add a terminal resistor R707 for RTL8100/8110 id selection. 2. Add a 0.1uF to make Q40 turn on slowly to aviod 3VPCU drop issue.  PAGE 24 --- Modified transformer circuit cause of CT can't connect each other on 10/100M application.  PAGE 26 --- Add a flashrom as PLCC32 type for BIOS debugging.  PAGE 27 --- 1. Change R352 value from 120K ohms to 20M ohms. 2. Add a LPC debug port for software team to debug convenient.  PAGE 30 --- Add GMT fan controller for B-test to costdown. PAGE 31 --- 1. Add ESD protection circuit for S-VIDEO signal to Docking. 2. Add R713 to enable the mux in the Tampa-2 cable  PAGE 33 --- Change PR143 value from 100K to 10K to solve display abnormal issue.  PAGE 35 --- 1. Move 5V_S5 circuit to Page 36. 2. De-popuplate PQ129 and PR182. 3. Change PR178 value from 22 ohm to 47 ohm.  PAGE 36 --- Remove PC170 and PQ127 but reserve 5V_S5 power circuit.	1	1A	
			2	1A	2A
			3	1A	2A
			4	1A	2A
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	2A
			11	1A	2A
			12	1A	2A
			13	1A	
			14	1A	
			15	1A	2A
			16	1A	
			17	1A	2A
			18	1A	2A
			19	1A	2A
			20	1A	
			21	1A	
			22	1A	2A
			23	1A	2A
			24	1A	2A
			25	1A	
			26	1A	2A
			27	1A	2A
			28	1A	
			29	1A	
			30	1A	2A
			31	1A	2A
			32	1A	
			33	1A	2A
			34	1A	
			35	1A	2A
			36	1A	2A
			37	1A	
			38	1A	
			39	1A	
			<div><div></div><div><div>PROJECT : CT3</div><div>Quanta Computer Inc.</div></div></div> <div><div>Size Custom</div><div>Document Number DB history</div><div>Date: Friday, March 04, 2005</div><div>Sheet 40 of 42</div><div>Rev 1A</div></div>		

MODEL	REV	CHANGE LIST	Model	CT3/5 MB BOARD	
			Page	FROM	TO
CT3/5 MB 31CT3MB0015 31CT3MB0031	2A	PAGE 2 --- 1. Add C1048 for CLK48M to get better EMI performance.  PAGE 3 --- 1. Add R733 as pull-up resistor for PREQ#. PAGE 11 --- 1. Add RF_OFF# and BT_OFF# circuit. PAGE 17 --- 1. Populate R704 and C1046 to get better EMI performance.  2. Remove R701 & R702 for unused PCI1510RVGF circuit. PAGE 18 --- 1. Disconnect SM_PHYS_WP on controller side. 2. Tie SM_EL_WP with SM_PHYS_WP on conn side to allow for normal operation of SD and SM. 3. Add a discharge circuit for media card power. 4. Add R718 to solve cross-talk issue of MS-Pro card. 5. Add R717 to solve SM card can't write protect issue. 6. Add R719~R736 as terminal on all multi-function pins. 7. Add pull-up circuit.  PAGE 27 --- 1. Reserve 0R for RF_OFF# and BT_OFF# circuit. 2. Modify LPC pin name.  PAGE 28 --- 1. Change HDD and ODD select definition. PAGE 30 --- Adjust Capacitors and Bead to improve CRT timing issue. 1. Change L66, L67, L68 from BK1608HM470 to 0R. 2. Remove C931, C932, C933. 3. Change C934, C935, C936 from 22P to 5.6P. 4. Change C6, C14, C350 from 10P to 5.6P. 5. Change L1, L26, L27 from BK1608HM470 to BLM18BA750SN1T.  PAGE 31 --- 1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality. 2. Reserve S-video impedance match circuit.	1	1A	
			2	2A	3A
			3	2A	3A
			4	2A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	2A	
			11	2A	
			12	2A	
			13	1A	
			14	1A	
			15	2A	
			16	1A	
			17	2A	3A
			18	2A	3A
			19	2A	
			20	1A	
			21	1A	
			22	2A	
			23	2A	
			24	2A	
			25	1A	
			26	2A	2A
			27	2A	
			28	1A	2A
			29	1A	
			30	2A	
			31	2A	
			32	1A	
			33	2A	
			34	2A	
			35	2A	
			36	2A	
			37	2A	
			38	2A	
			39	2A	
			<div><div></div><div>PROJECT : CT3 Quanta Computer Inc.</div></div> <div><div>Size Custom</div><div>Document Number</div><div>SI history</div><div>Date: Friday, March 04, 2005</div><div>Sheet 41 of 42</div><div>Rev 1A</div></div>		

MODEL	REV	CHANGE LIST	Model	CT3/5 MB BOARD	
			Page	FROM	TO
CT3/5 MB 31CT3MB0015 31CT3MB0031	3A	PAGE 08 --- 1.To add a LDO for clear POWER to solve TV problem  PAGE 10 --- 1.EMI team suggest us to add a Bead and a Capacity to improve EMI  PAGE 14 --- 1.TO change net name from BITCLK to BITCLK_SB. 2.To add a 10U Capacity for better power.  PAGE 18 --- 1.To add a circuit for MS PRO DUO problem. 2.To add a discharge circuit for media card power. 3.To change resistor value to solve card-reader problem.  PAGE 19 --- 1.To delete CML1, CML2, L1 and L37 for SMT request. 2.To change USB and 1394 connector for strong ME.  PAGE 26 --- 1.To delete PLCC32 for SMT request	1	1A	
			2	3A	
			3	3A	
			4	2A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	2A
			9	1A	
			10	2A	3A
			11	2A	
			12	2A	
			13	1A	
			14	1A	2A
			15	2A	
			16	1A	
			17	3A	
			18	3A	4A
			19	2A	3A
			20	1A	
			21	1A	
			22	2A	
			23	2A	
			24	2A	
			25	1A	
			26	2A	3A
			27	2A	
			28	2A	
			29	1A	
			30	2A	
			31	2A	
			32	1A	
			33	2A	
			34	2A	
			35	2A	
			36	2A	
			37	2A	
			38	2A	
			39	2A	



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