

Compal Confidential

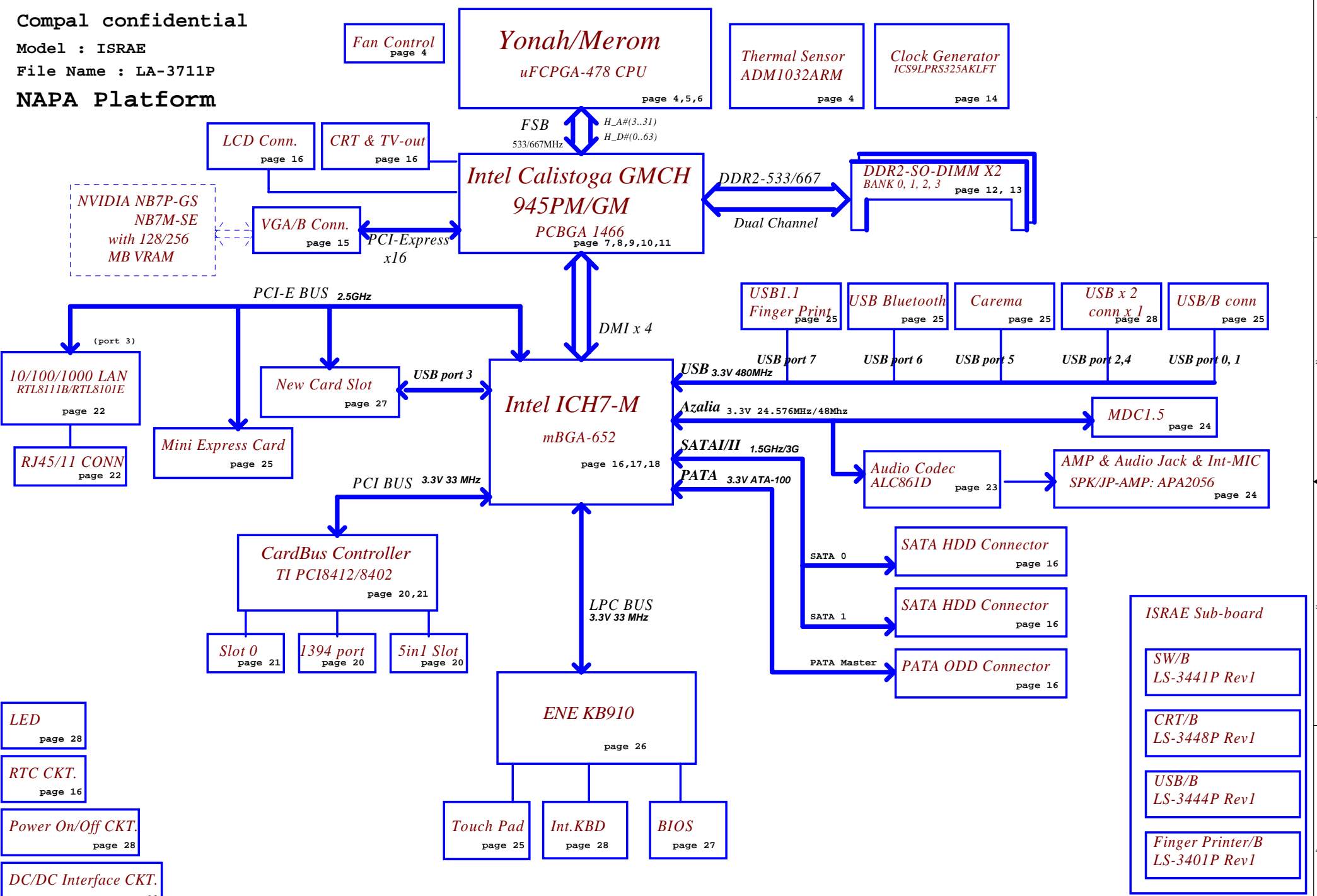
ISRAE LA-3711P Schematics Document

Intel Yonah/Merom with 945GM/943GML/940GML+ DDRII + ICH7M

2007-01-29

REV: 0.2

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Block Diagram		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	+VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C
CARD BUS	D4	AD20	2	A,B,C
5IN1	D4	AD20	2	A,B,C

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 1 0 1 1 X b
SM2 ADM0132	98H	1 0 1 1 0 0 X b
CPU THERMAL MONITOR		

ICH7-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	10 (10E)(10M)
1	10C
2	10G(10MG)
3	10GC
4	10J(10EJ) (10MJ)
5	10CJ
6	10G(10MG)J
7	10GC(10MGC)J

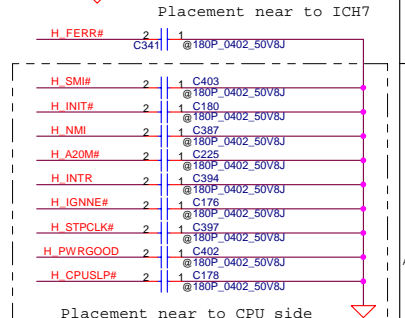
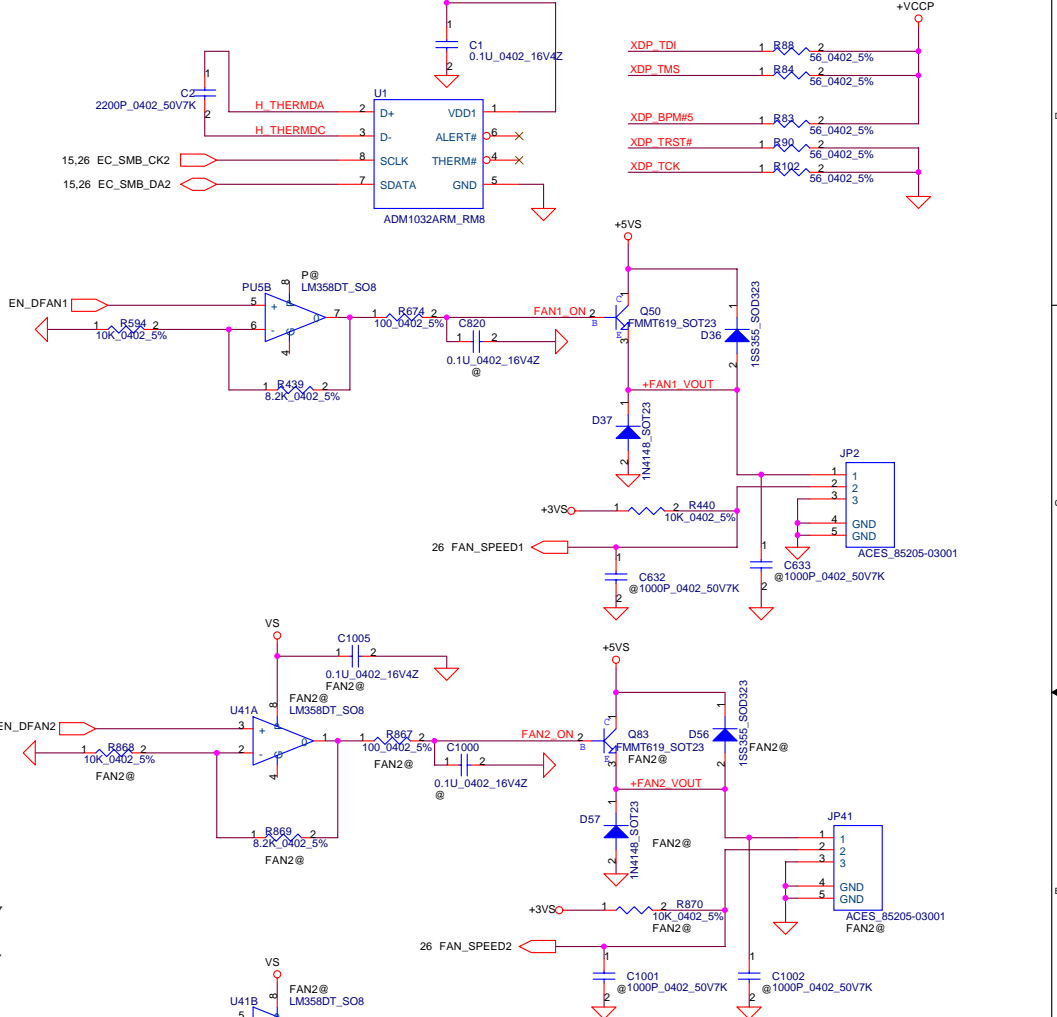
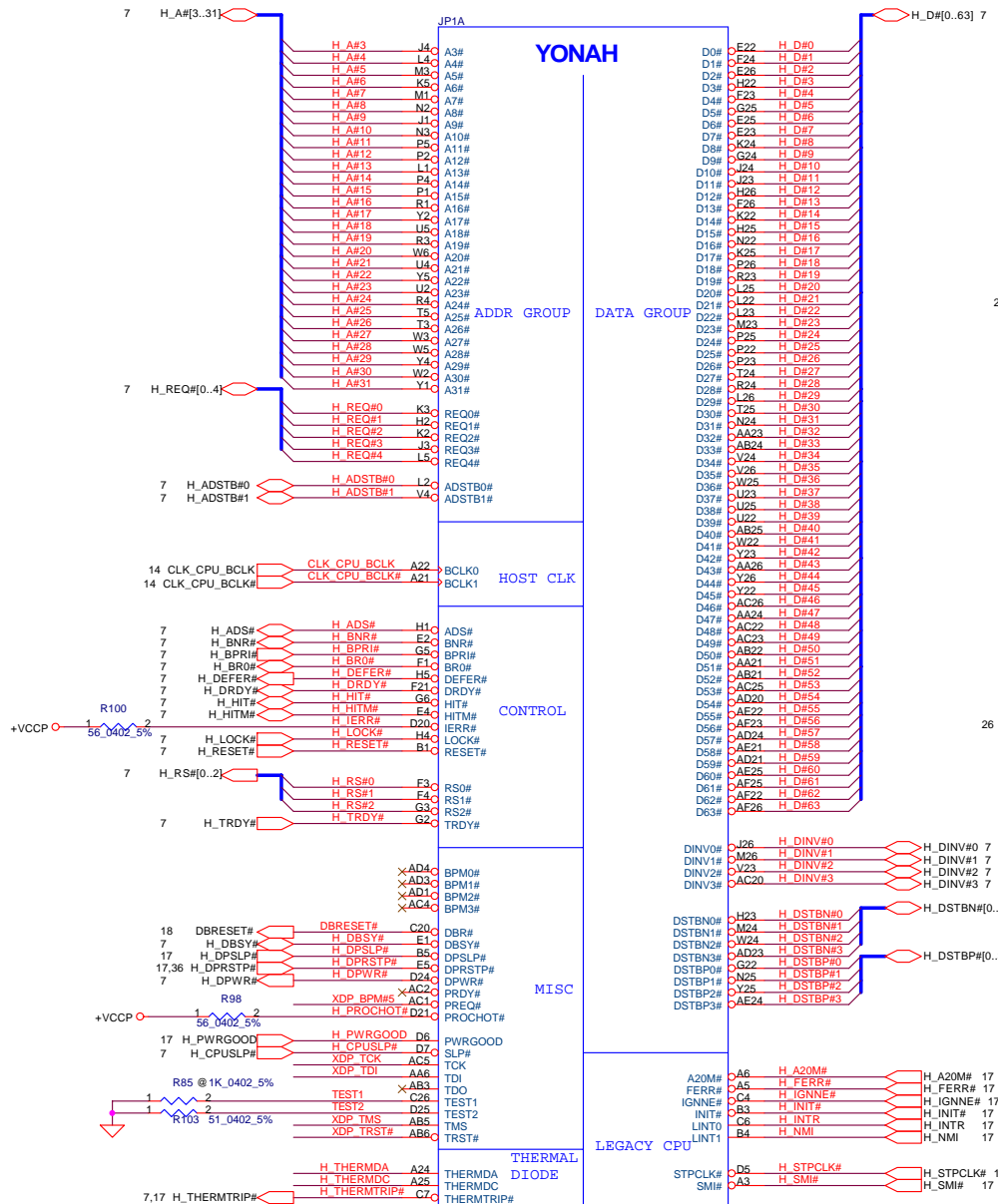
BTO Option Table

BTO Item	BOM Structure
45 level	45@
2ND HDD	2HDD@
LAN	100M@/1000M@
WLAN	KS@
MDC	MDC@
Blue tooth	BT@
Card ctrller	8412@/8402@/4512@
FINGER PRINT	FP@
5IN1	5IN1@, NON5IN1@
Express card	NEWCARD@
PCMCIA	PCMCIA@
Carema+MIC	CAREMA@
VGA FAN	FAN2@
CHIPSET (R3)	GMLR3@,GM@, ICH7R3@
change R3 to R1 for FRU	GMR3@,GM@, ICH7R3@
CIR	CIR@
Energy Star	ENG@

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Thermal Sensor ADM1032ARM

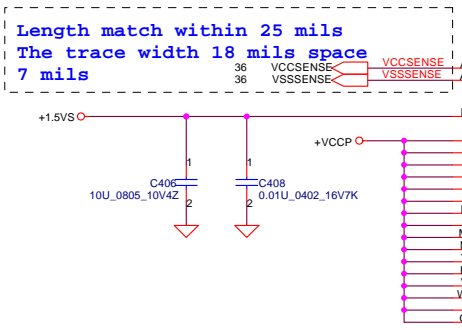
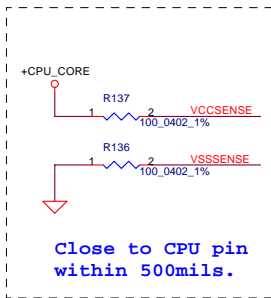
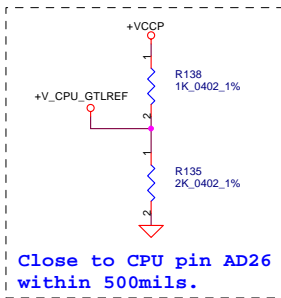
Place close to CPU within 500mil



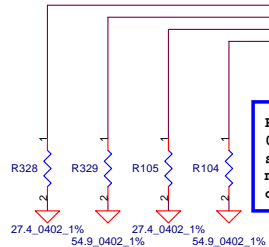
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

FOX_PZ47903-2741-42_YONAH

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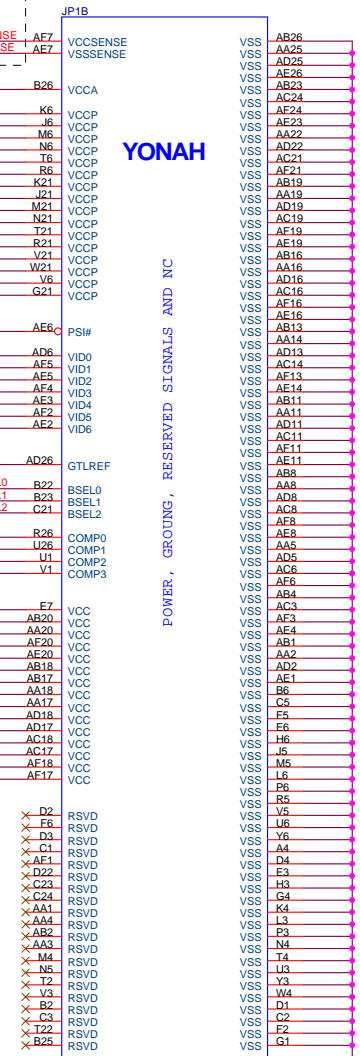
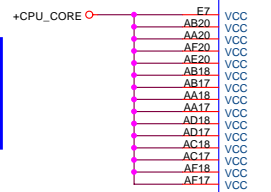
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



CPU_VID0	CPU_VID1	CPU_VID2	CPU_VID3	CPU_VID4	CPU_VID5	CPU_VID6
AD6	AE6	AE5	AE4	AE3	AE2	AE2

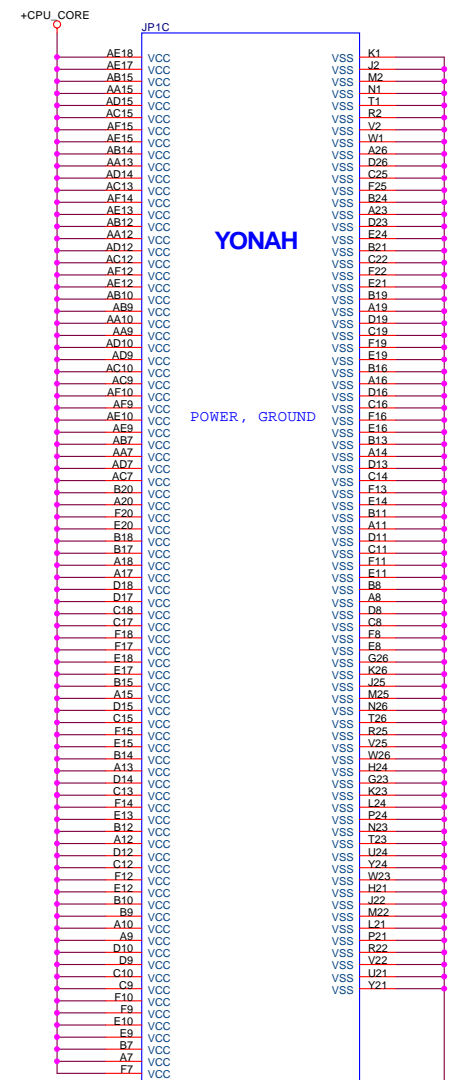
CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
B22	B23	C21

COMP0	COMP1	COMP2	COMP3
R26	U26	U1	V1



YONAH

POWER, GROUND, RESERVED SIGNALS AND INC



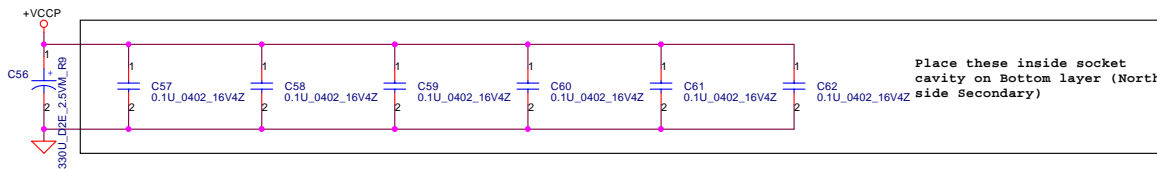
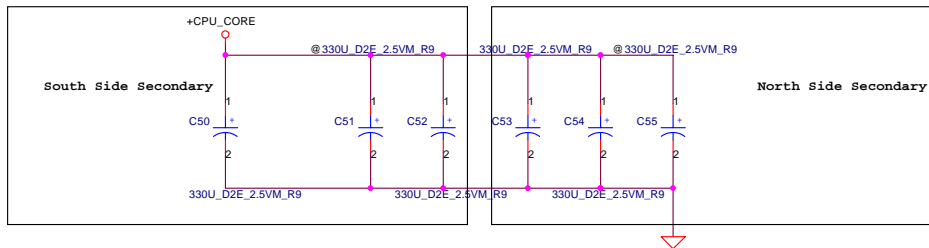
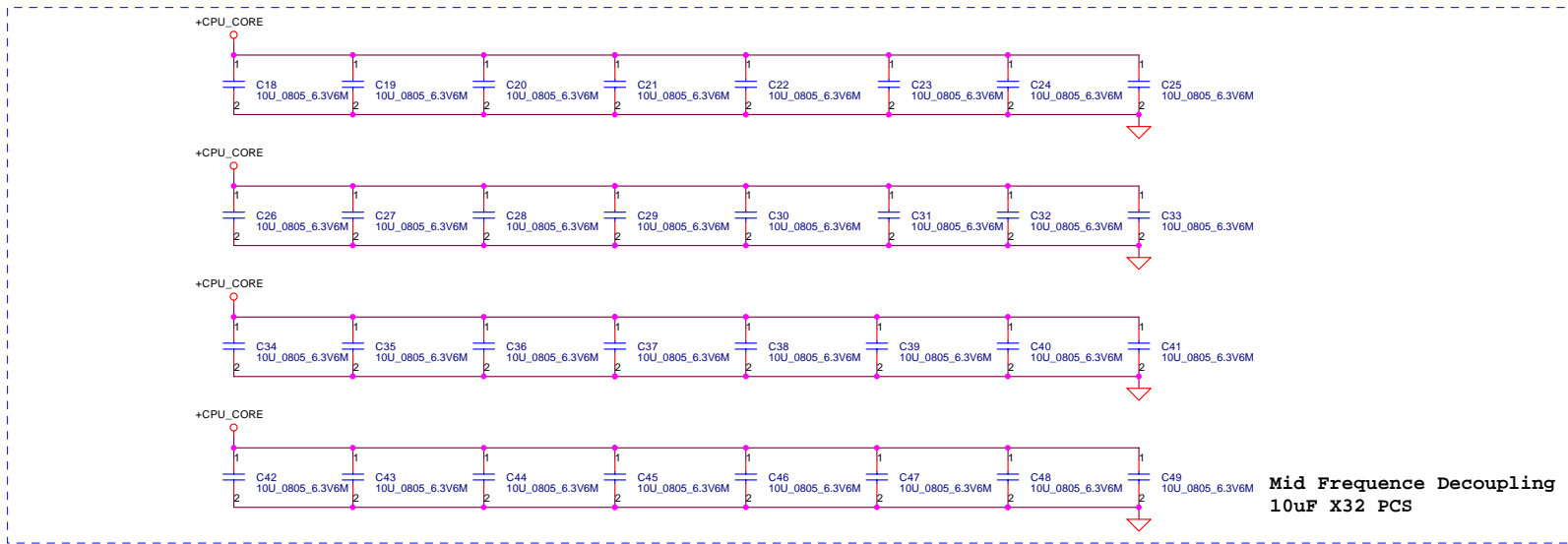
YONAH

POWER, GROUND

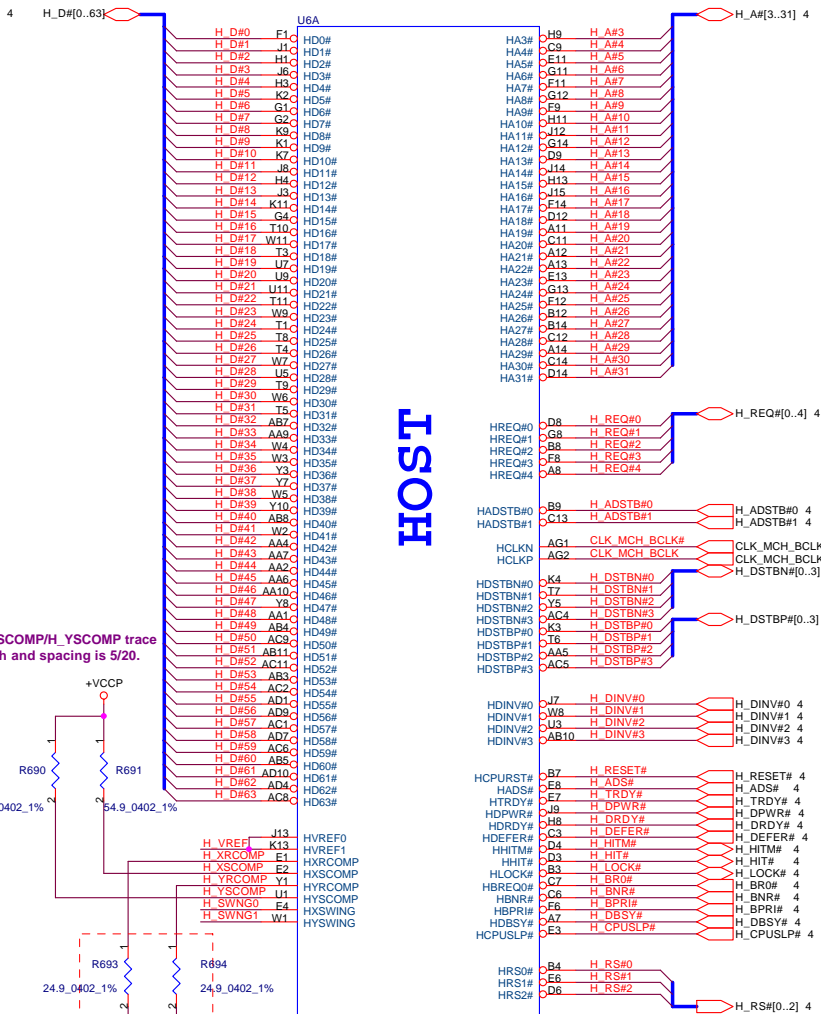
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Title		
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Yonah CPU in mFCPGA479		
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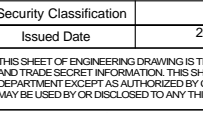
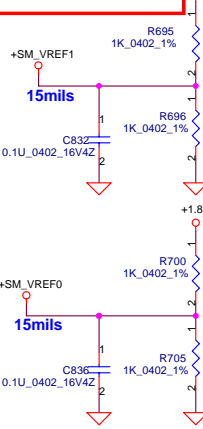


HOST

H_XSCOMP/H_YSCOMP trace width and spacing is 5/20.

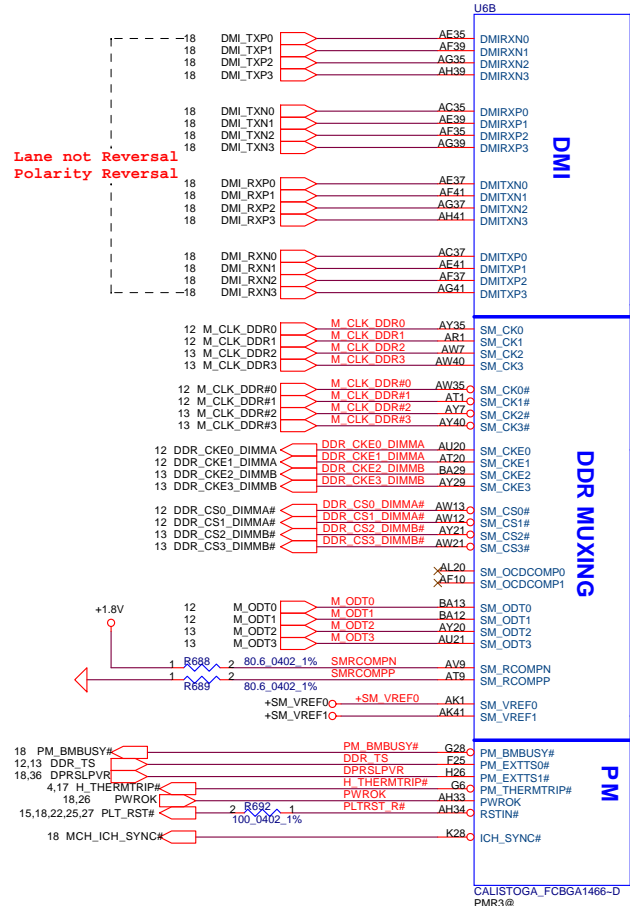
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 18/20.

Layout Note:
+SM_VREF0 & +SM_VREF1 trace width and spacing is 18/20.



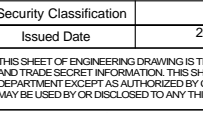
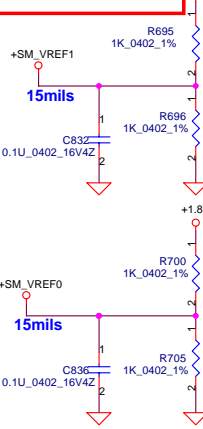
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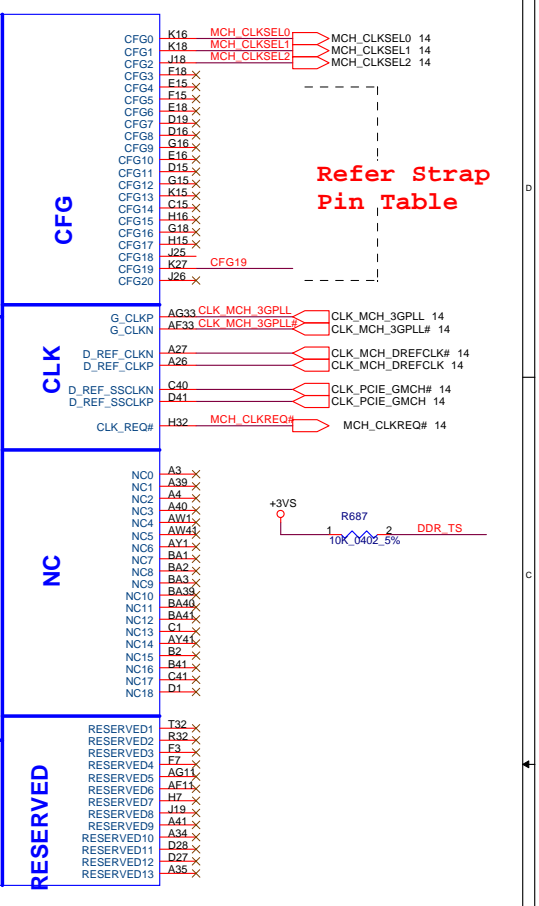
Lane not Reversal Polarity Reversal

Layout Note:
+SM_VREF0 & +SM_VREF1 trace width and spacing is 18/20.



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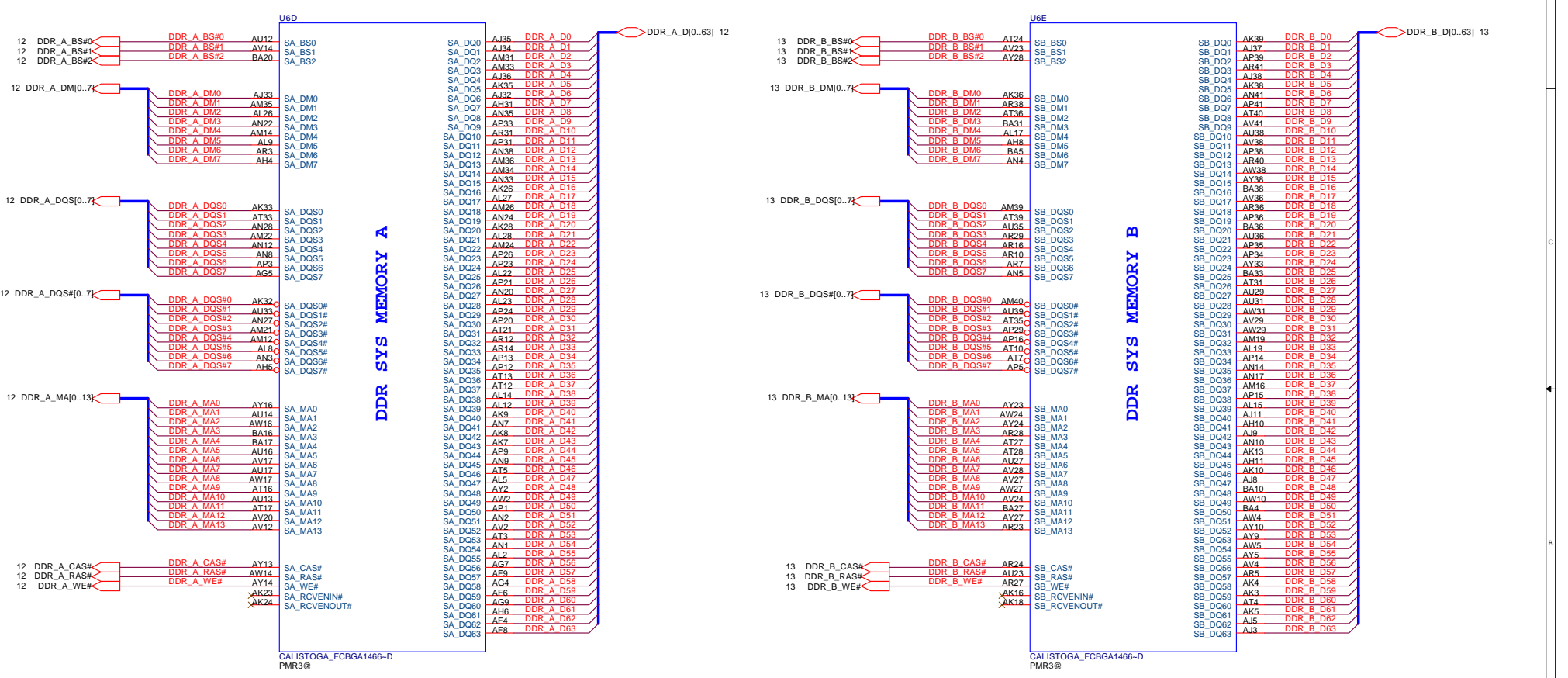
Refer Strap Pin Table

Strap Pin	CFG[3:17] have internal pull up	CFG[19:18] have internal pull down
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB	
CFG5	0 = DMI x 2 *1 = DMI x 4 (Default)	
CFG7	0 = Reserved *1 = Mobile Yonah CPU (Default)	
CFG9	0 = Lane Reversal Enable *1 = Normal Operation (Default)	
CFG11	0 = Reserved *1 = Calistoga (Default)	
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled *11 = Normal Operation (Default)	
CFG16	0 = Dynamic ODT Disabled *1 = Dynamic ODT Enabled (Default)	
CFG18	*0 = 1.05V (Default) 1 = 1.5V	
CFG19	*0 = Normal Operation (Default) *1 = DMI Lane Reversal Enable	
SDVO_CTRLDATA	*0 = No SDVO Device Present (Default) 1 = SDVO Device Present	
CFG20 (PCIE/SDVO select)	*0 = Only PCIE or SDVO is operational. (Default) 1 = PCIE/SDVO are operating simu.	

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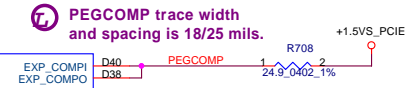
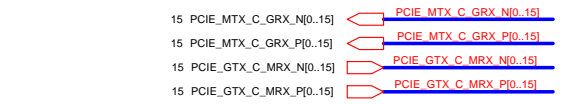
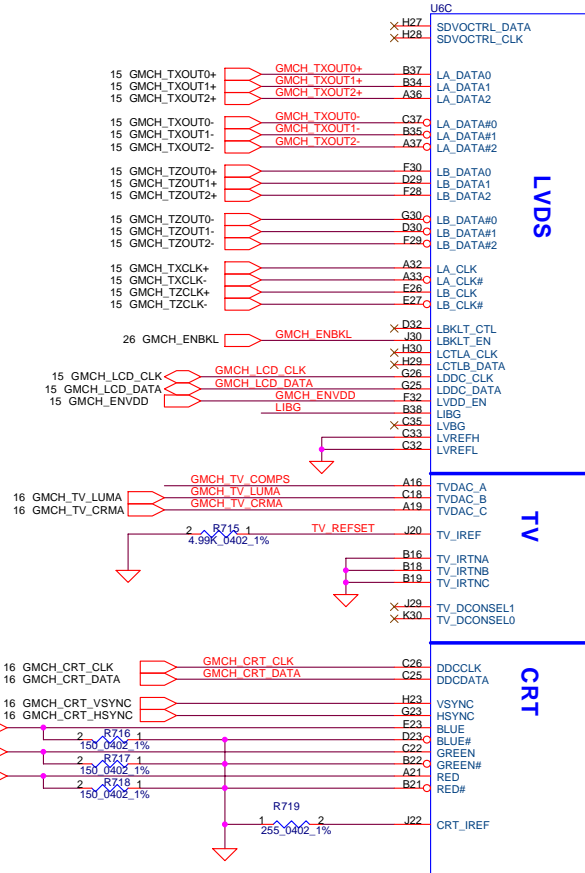
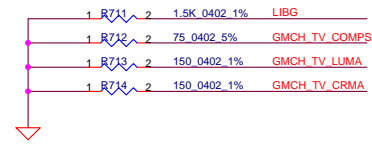
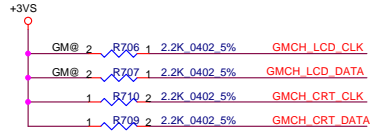
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 Calistoga (1/5)
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CALISTOGA_FCBGA1466-D
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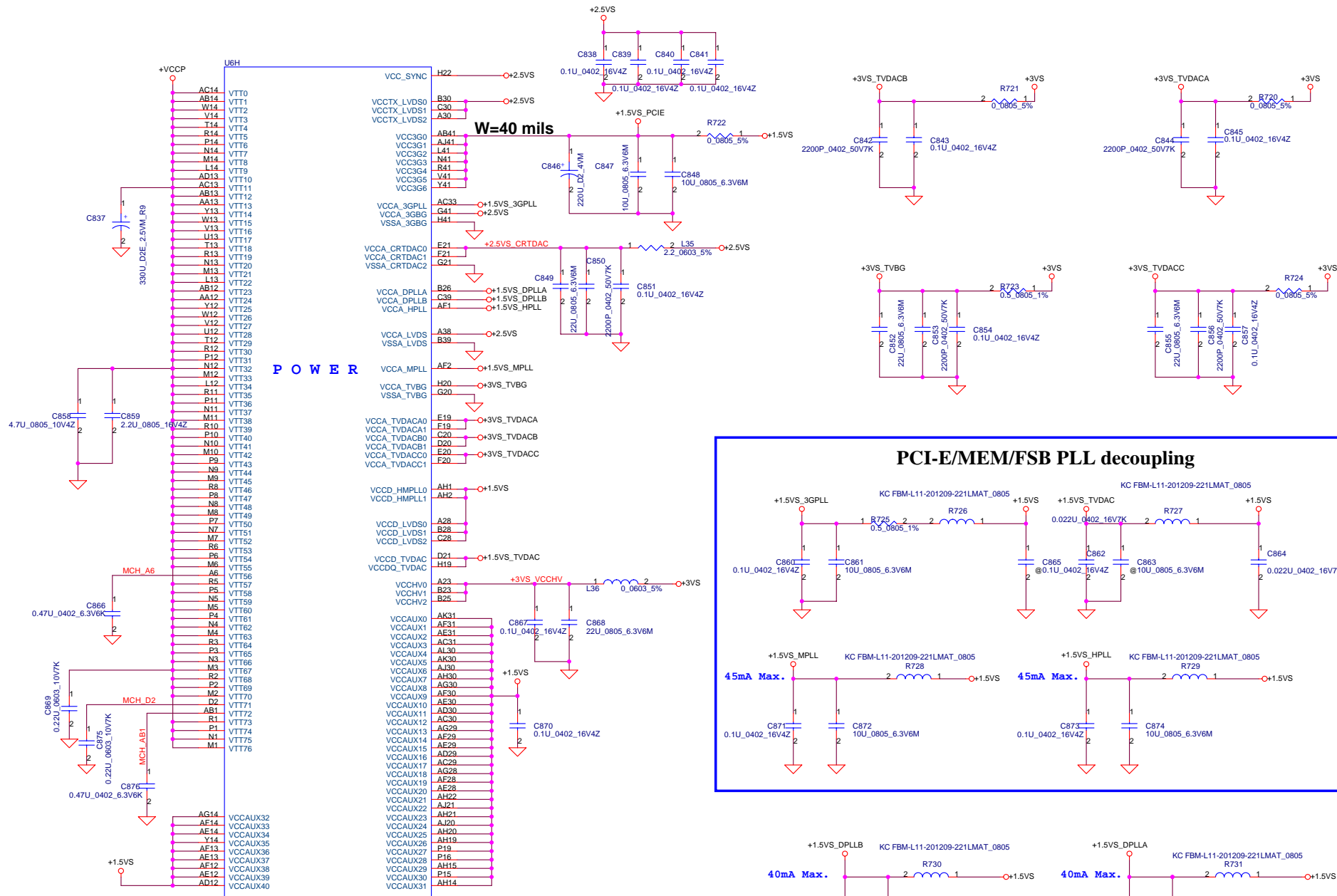
PCI-EXPRESS GRAPHICS

EXP_RXN0	F34	PCIE GTX C MRX P0	
EXP_RXN1	G38	PCIE GTX C MRX P1	
EXP_RXN2	H34	PCIE GTX C MRX P2	
EXP_RXN3	J38	PCIE GTX C MRX P3	
EXP_RXN4	L34	PCIE GTX C MRX P4	
EXP_RXN5	M38	PCIE GTX C MRX P5	
EXP_RXN6	N34	PCIE GTX C MRX P6	
EXP_RXN7	P38	PCIE GTX C MRX P7	
EXP_RXN8	R34	PCIE GTX C MRX P8	
EXP_RXN9	T38	PCIE GTX C MRX P9	
EXP_RXN10	V34	PCIE GTX C MRX P10	
EXP_RXN11	W38	PCIE GTX C MRX P11	
EXP_RXN12	Y34	PCIE GTX C MRX P12	
EXP_RXN13	AA38	PCIE GTX C MRX P13	
EXP_RXN14	AB34	PCIE GTX C MRX P14	
EXP_RXN15	AC38	PCIE GTX C MRX P15	
EXP_RXP0	D34	PCIE GTX C MRX N0	
EXP_RXP1	F38	PCIE GTX C MRX N1	
EXP_RXP2	G34	PCIE GTX C MRX N2	
EXP_RXP3	H38	PCIE GTX C MRX N3	
EXP_RXP4	J34	PCIE GTX C MRX N4	
EXP_RXP5	L38	PCIE GTX C MRX N5	
EXP_RXP6	M34	PCIE GTX C MRX N6	
EXP_RXP7	N38	PCIE GTX C MRX N7	
EXP_RXP8	P34	PCIE GTX C MRX N8	
EXP_RXP9	R38	PCIE GTX C MRX N9	
EXP_RXP10	T34	PCIE GTX C MRX N10	
EXP_RXP11	V38	PCIE GTX C MRX N11	
EXP_RXP12	W34	PCIE GTX C MRX N12	
EXP_RXP13	Y38	PCIE GTX C MRX N13	
EXP_RXP14	AA34	PCIE GTX C MRX N14	
EXP_RXP15	AB38	PCIE GTX C MRX N15	
EXP_TXN0	F36	PCIE MTX GRX N0	PM@ 0.1U 0402 16V7K
EXP_TXN1	G40	PCIE MTX GRX N1	PM@ 0.1U 0402 16V7K
EXP_TXN2	H36	PCIE MTX GRX N2	PM@ 0.1U 0402 16V7K
EXP_TXN3	J40	PCIE MTX GRX N3	PM@ 0.1U 0402 16V7K
EXP_TXN4	L36	PCIE MTX GRX N4	PM@ 0.1U 0402 16V7K
EXP_TXN5	M40	PCIE MTX GRX N5	PM@ 0.1U 0402 16V7K
EXP_TXN6	N36	PCIE MTX GRX N6	PM@ 0.1U 0402 16V7K
EXP_TXN7	P40	PCIE MTX GRX N7	PM@ 0.1U 0402 16V7K
EXP_TXN8	R36	PCIE MTX GRX N8	PM@ 0.1U 0402 16V7K
EXP_TXN9	T40	PCIE MTX GRX N9	PM@ 0.1U 0402 16V7K
EXP_TXN10	V36	PCIE MTX GRX N10	PM@ 0.1U 0402 16V7K
EXP_TXN11	W40	PCIE MTX GRX N11	PM@ 0.1U 0402 16V7K
EXP_TXN12	Y36	PCIE MTX GRX N12	PM@ 0.1U 0402 16V7K
EXP_TXN13	AA40	PCIE MTX GRX N13	PM@ 0.1U 0402 16V7K
EXP_TXN14	AB36	PCIE MTX GRX N14	PM@ 0.1U 0402 16V7K
EXP_TXN15	AC40	PCIE MTX GRX N15	PM@ 0.1U 0402 16V7K
EXP_TXP0	D36	PCIE MTX GRX P0	PM@ 0.1U 0402 16V7K
EXP_TXP1	F40	PCIE MTX GRX P1	PM@ 0.1U 0402 16V7K
EXP_TXP2	G36	PCIE MTX GRX P2	PM@ 0.1U 0402 16V7K
EXP_TXP3	H40	PCIE MTX GRX P3	PM@ 0.1U 0402 16V7K
EXP_TXP4	J36	PCIE MTX GRX P4	PM@ 0.1U 0402 16V7K
EXP_TXP5	L40	PCIE MTX GRX P5	PM@ 0.1U 0402 16V7K
EXP_TXP6	M36	PCIE MTX GRX P6	PM@ 0.1U 0402 16V7K
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EXP_TXP10	T36	PCIE MTX GRX P10	PM@ 0.1U 0402 16V7K
EXP_TXP11	V40	PCIE MTX GRX P11	PM@ 0.1U 0402 16V7K
EXP_TXP12	W36	PCIE MTX GRX P12	PM@ 0.1U 0402 16V7K
EXP_TXP13	Y40	PCIE MTX GRX P13	PM@ 0.1U 0402 16V7K
EXP_TXP14	AA36	PCIE MTX GRX P14	PM@ 0.1U 0402 16V7K
EXP_TXP15	AB40	PCIE MTX GRX P15	PM@ 0.1U 0402 16V7K

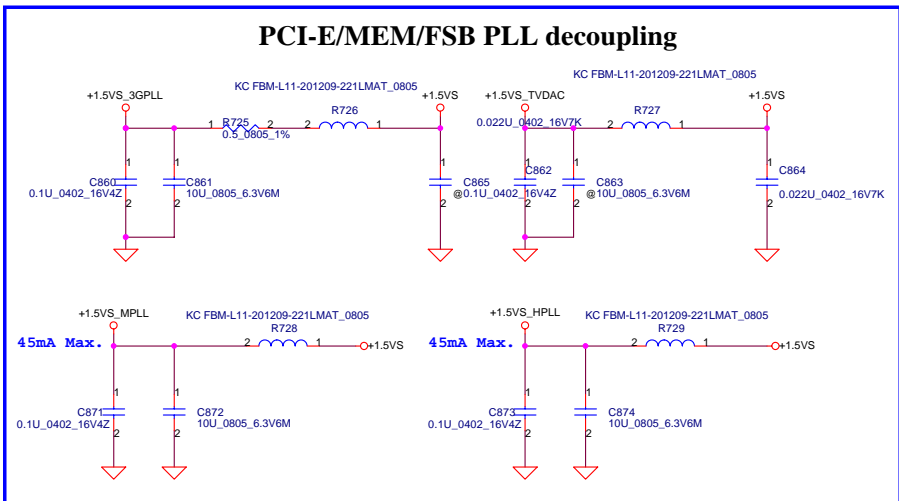
Lane not Reversal
Polarity not Reversal

Lane not Reversal
Polarity not Reversal

Security Classification	Compal Secret Data			Title	
Issued Date	2006/11/05	Deciphered Date	2009/11/05	Compal Electronics, Inc.	
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				ISRAEL M/B LA-3711P	
				Date:	Tuesday, February 06, 2007
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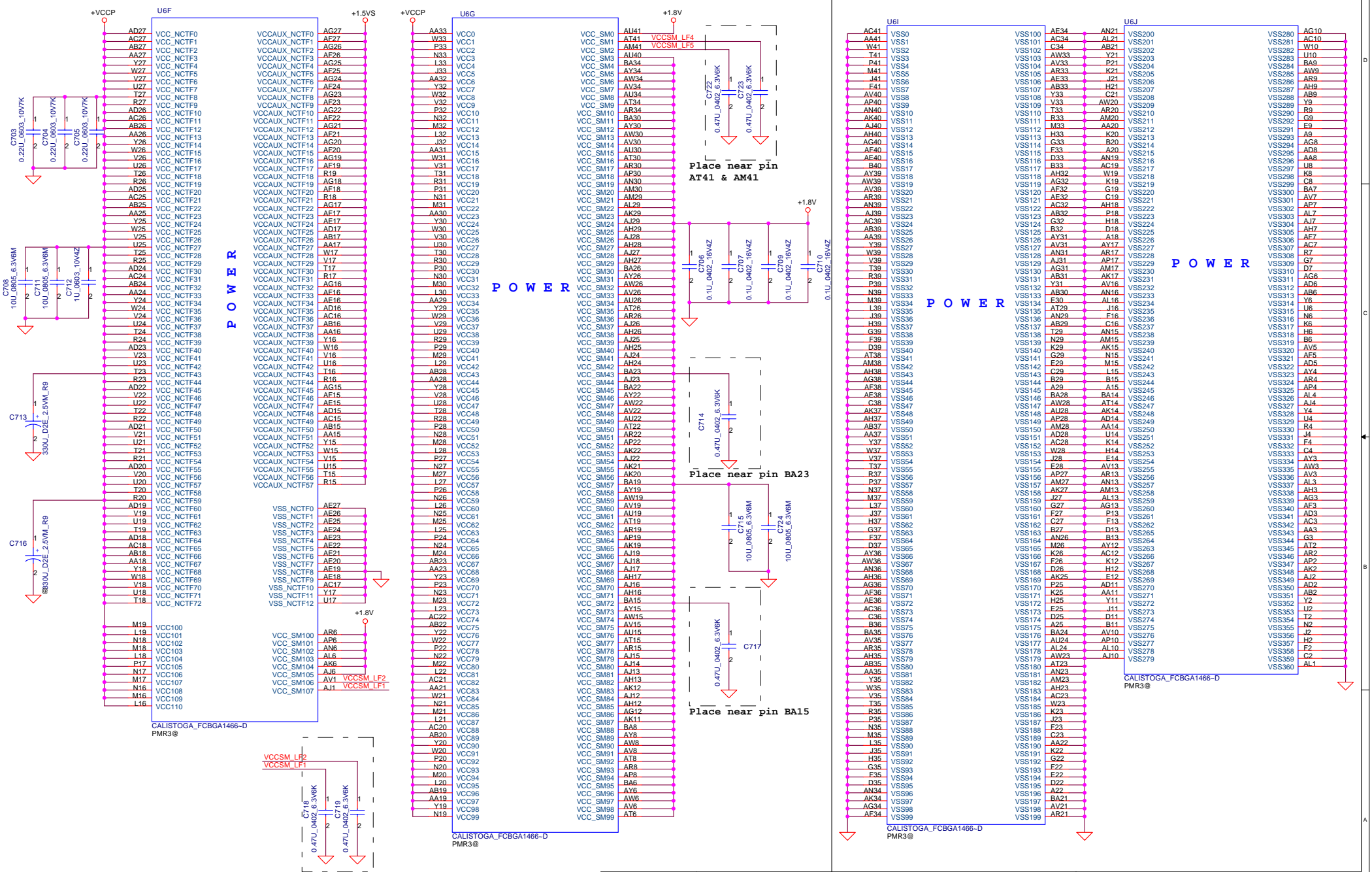
P O W E R



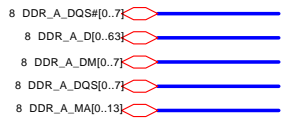
Security Classification	Compal Secret Data			Title		
Issued Date	2006/11/05	Deciphered Date	2009/11/05	Compal Electronics, Inc.		
				Calistoga (4/5)		
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				Date:	Tuesday, February 06, 2007	Sheet 10 of 39

POWER

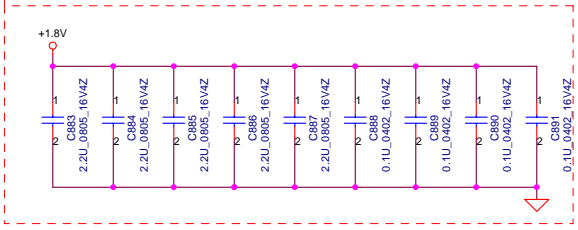
GND



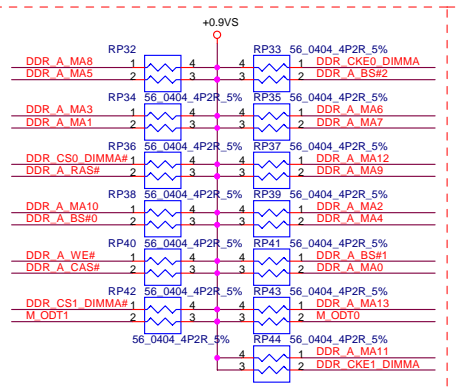
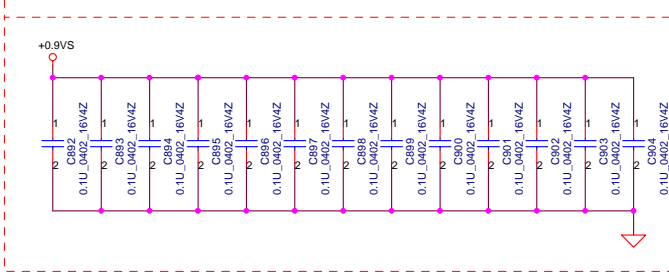
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Issued Date	2006/11/05	Deciphered Date	2009/11/05	Calistoga (5/5)	
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Date:	Tuesday, February 06, 2007	Sheet	11	of	39



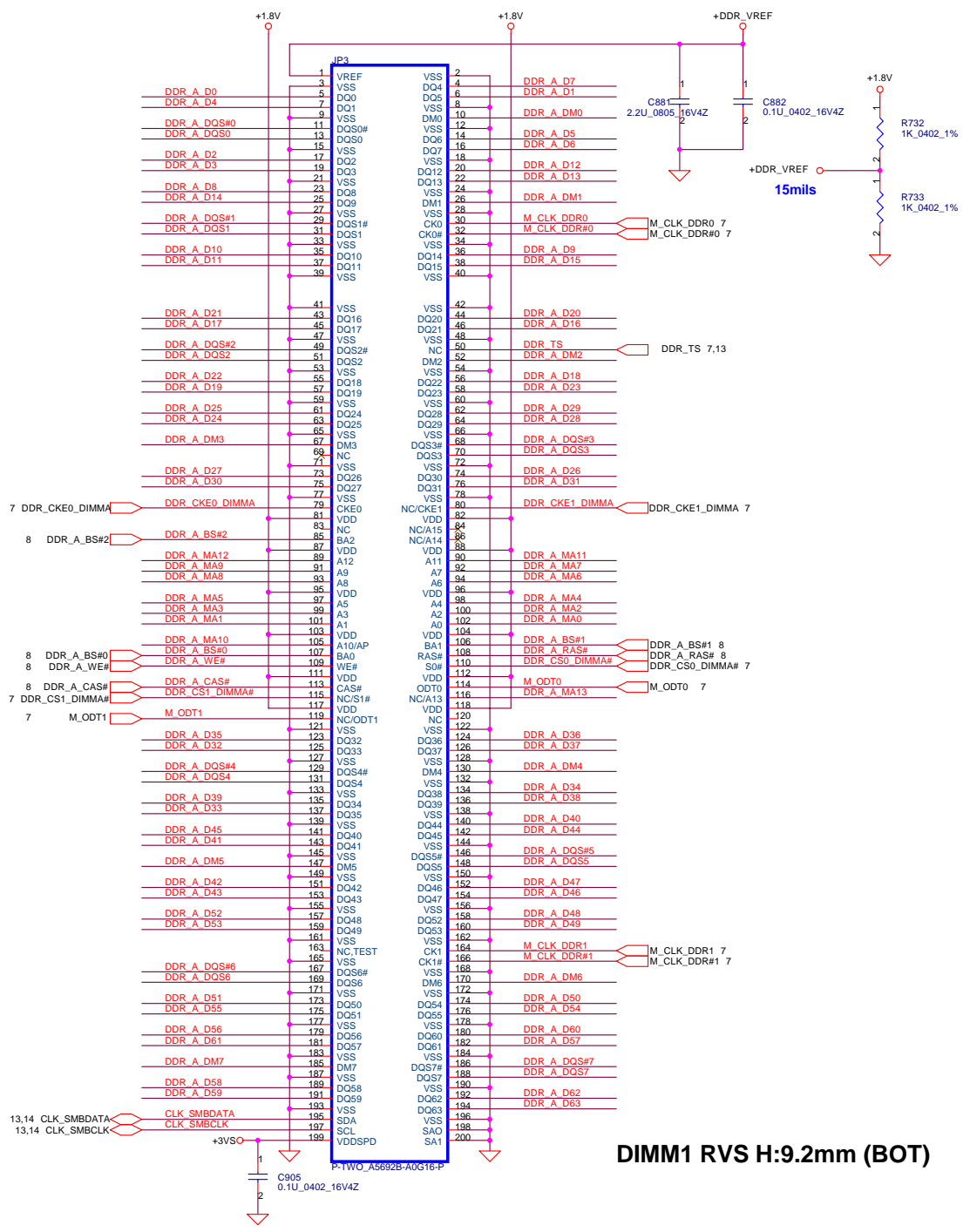
Layout Note:
Place near JP27



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP27, all trace length Max=1.5"

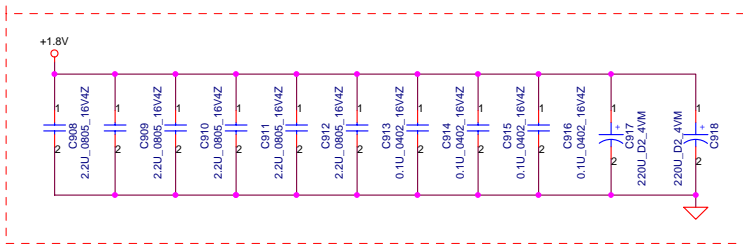


DIMM1 RVS H:9.2mm (BOT)

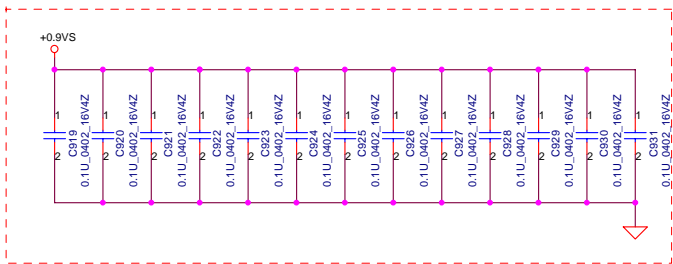
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2006/11/05	Deciphered Date	2009/11/05	DDRII-SODIMM SLOT1	
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- 8 DDR_B_DQS#(0..7)
- 8 DDR_B_D[0..63]
- 8 DDR_B_DM(0..7)
- 8 DDR_B_DQS(0..7)
- 8 DDR_B_MA(0..13)

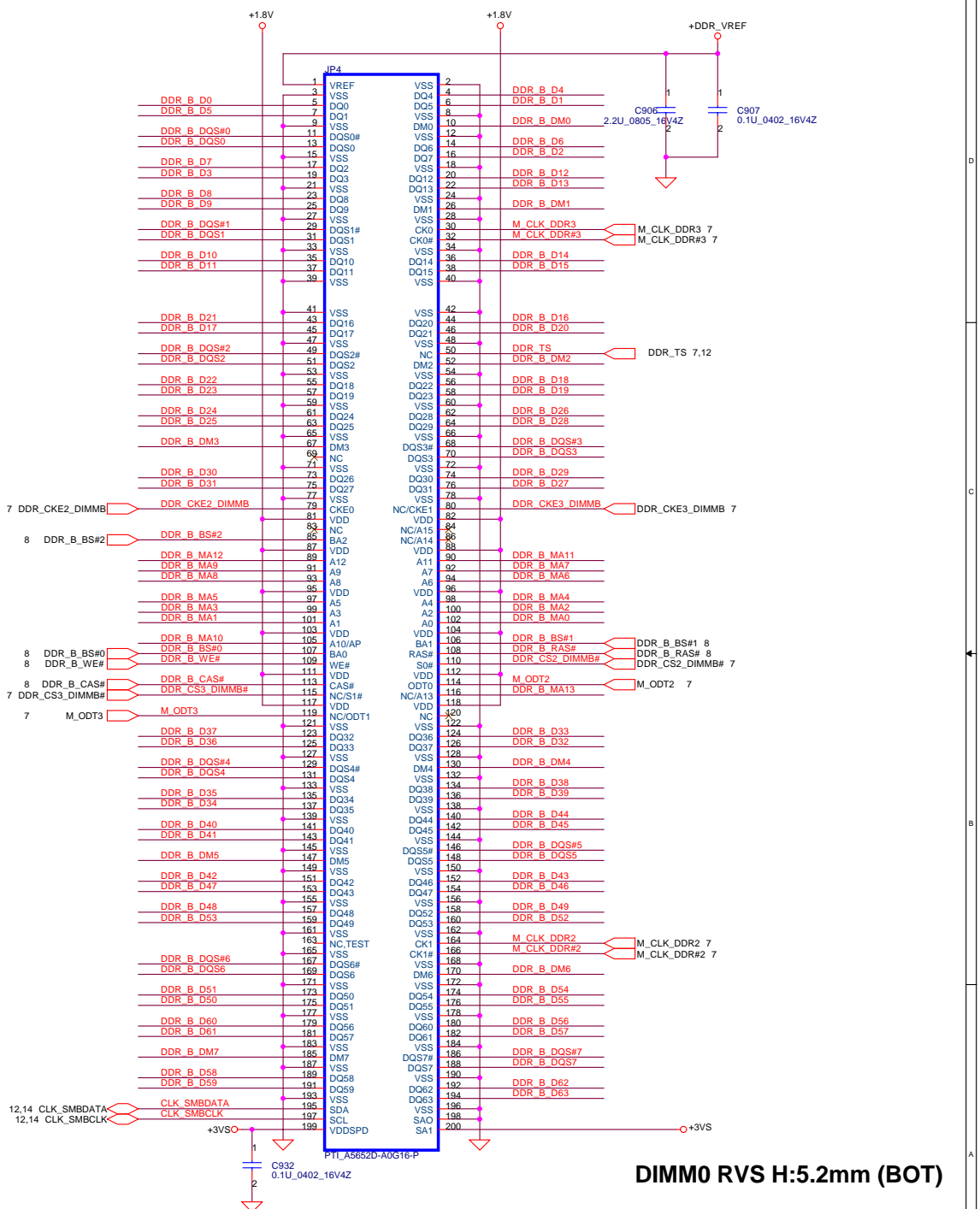
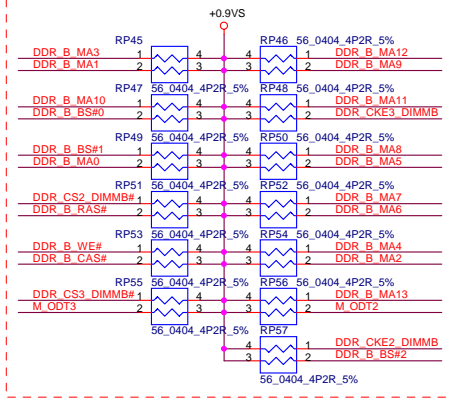
Layout Note:
Place near JP26



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

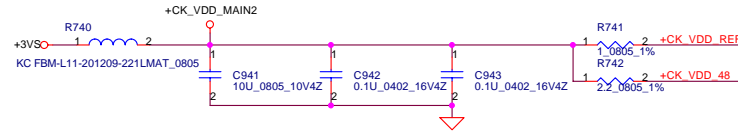
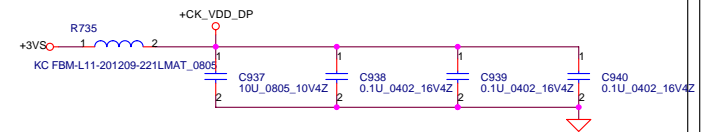
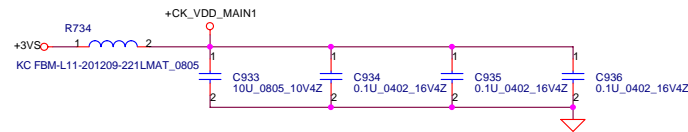
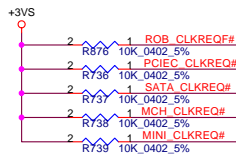


Layout Note:
Place these resistor closely JP26, all trace length Max=1.5"



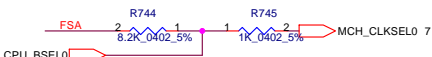
DIMM0 RVS H:5.2mm (BOT)

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				ISRAE MB LA-371IP		0.2	
Date:				Tuesday, February 06, 2007	Sheet	13	of 39

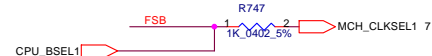


FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

FSA

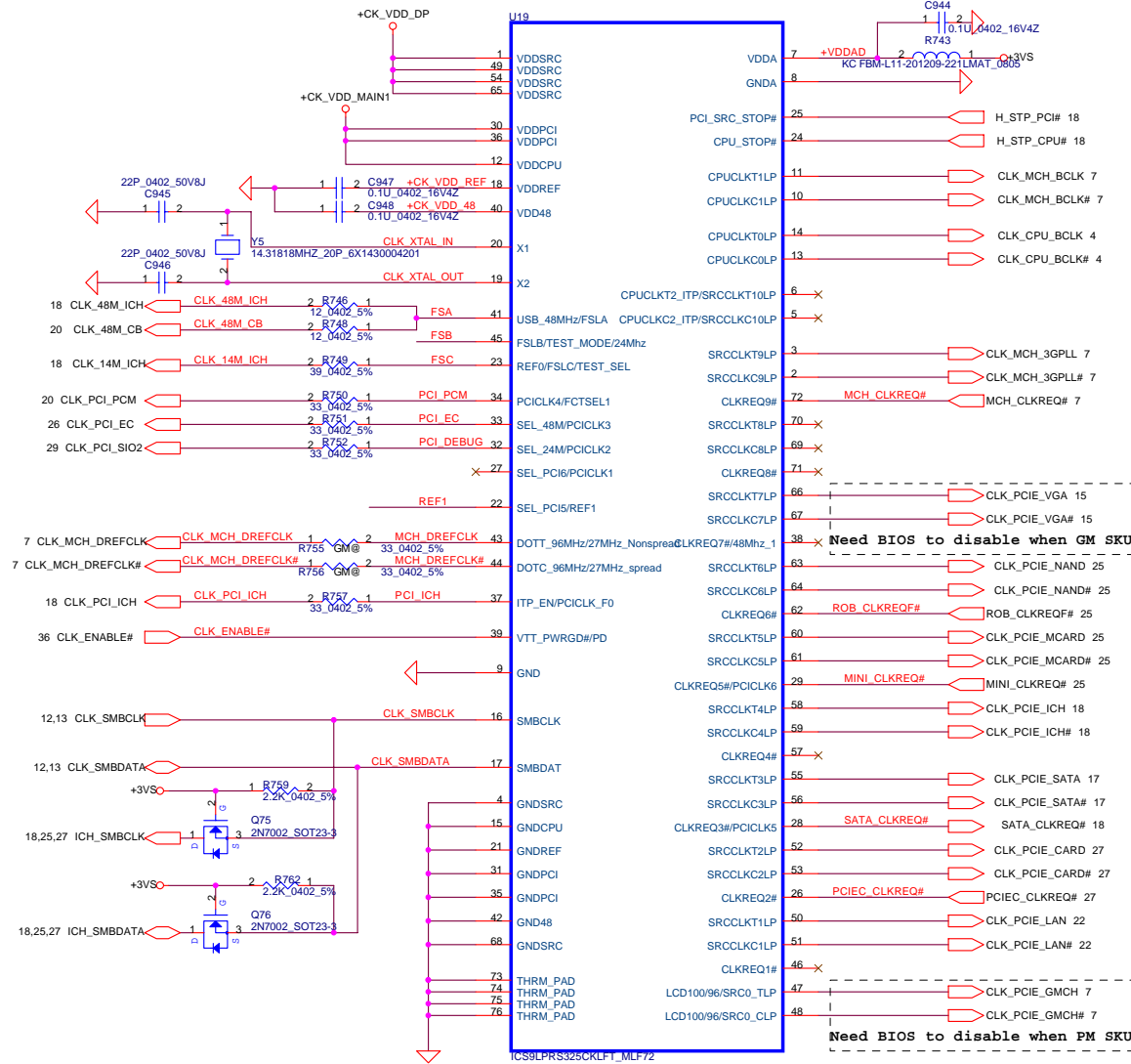
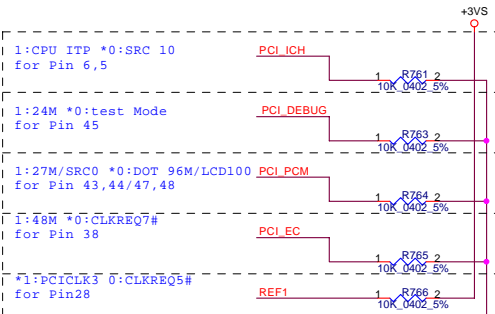
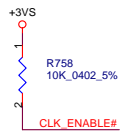
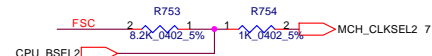


FSB



FSC

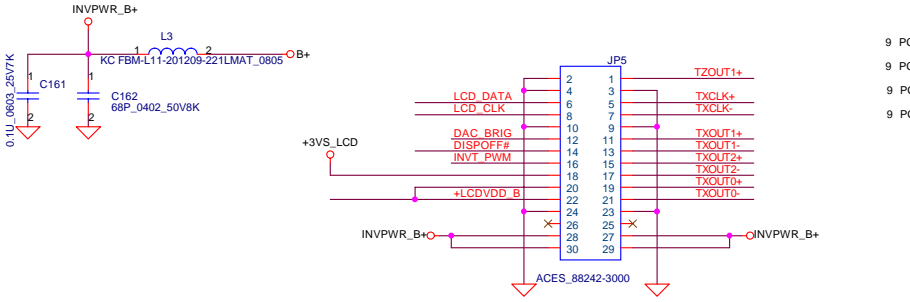
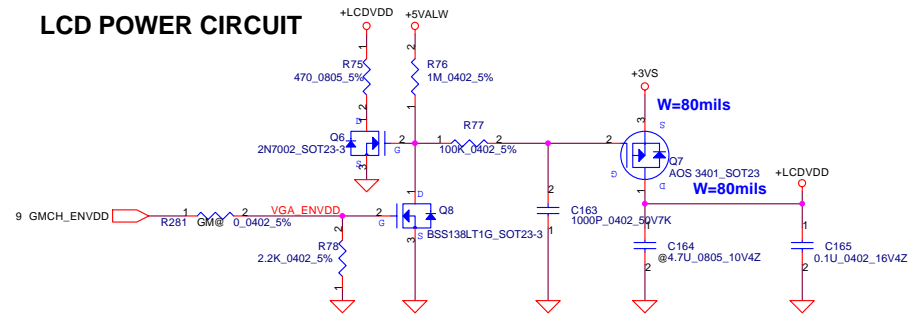
(Fixed at low)



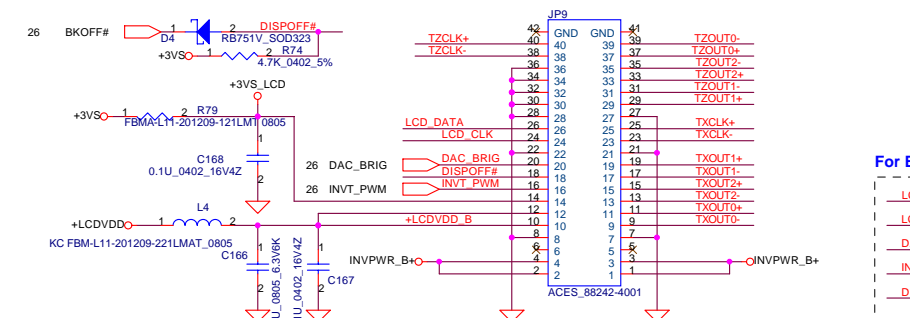
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Compal Electronics, Inc.			
Clock generator			
Size	Document Number	Rev	
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LCD POWER CIRCUIT



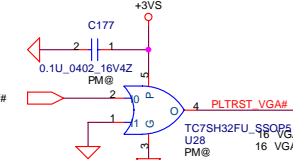
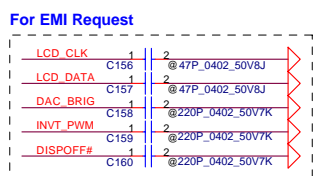
LCD PANEL BD. Conn.



ALL R CLOSE LVDS CONNECTOR

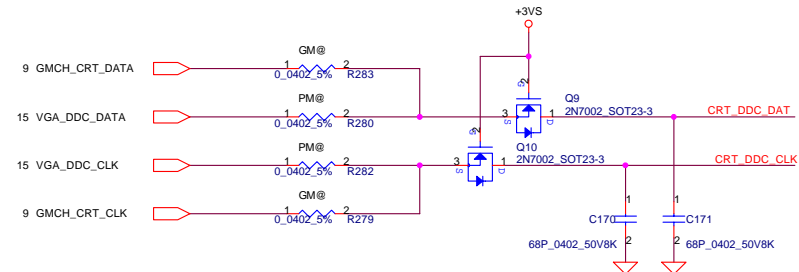
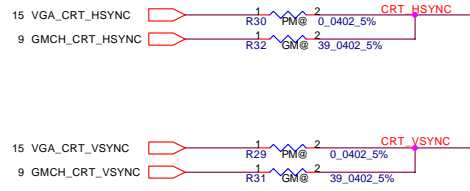
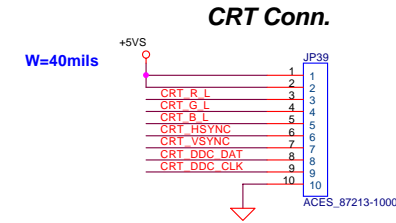
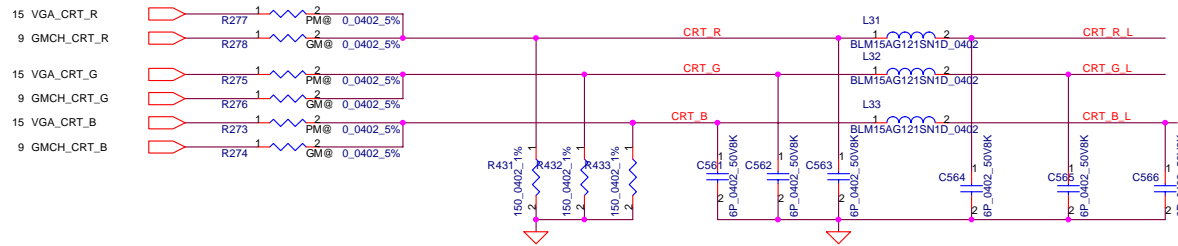


VGA BOARD Conn. VGA BOARD Conn.

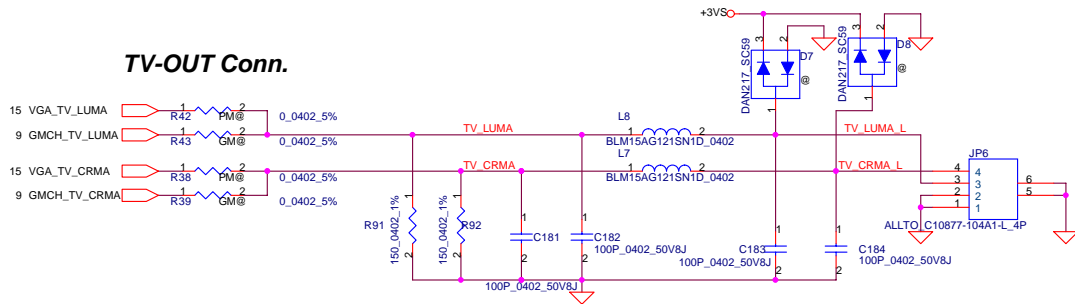


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Issued Date	2006/08/05	Deciphered Date	2007/08/05	VGA CONN	
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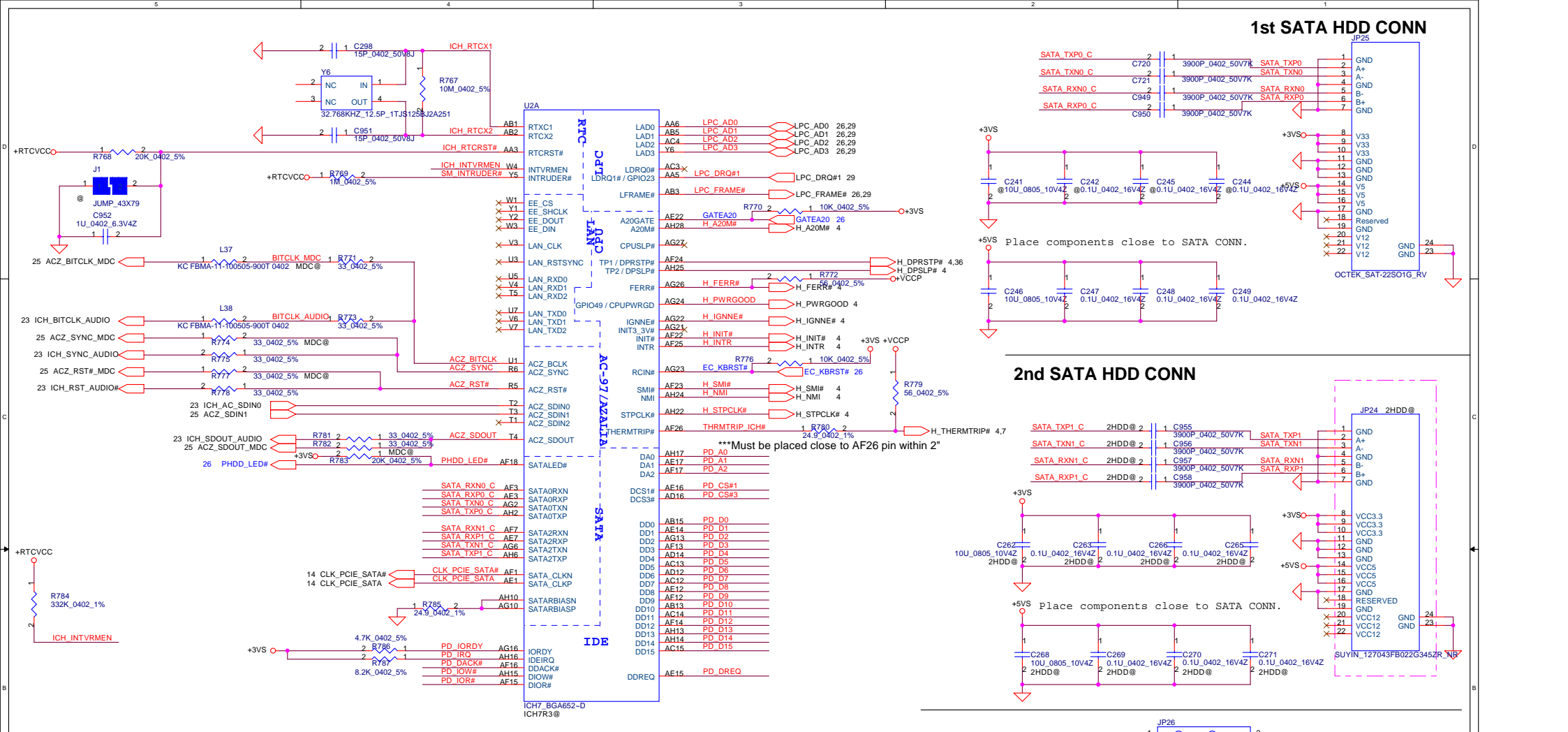
CRT CONNECTOR



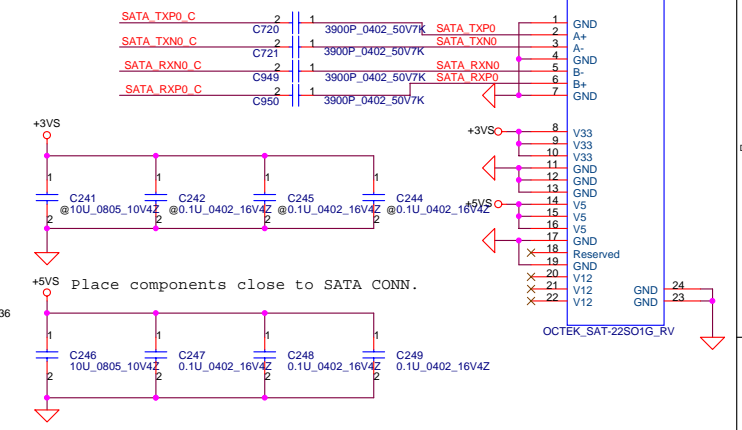
TV-OUT Conn.



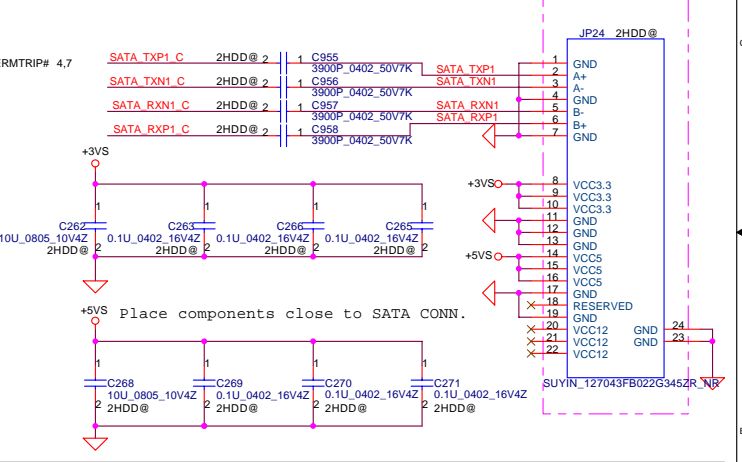
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Issued Date	2006/10/31	Deciphered Date	2009/11/13	Display Interface Connector	
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1st SATA HDD CONN



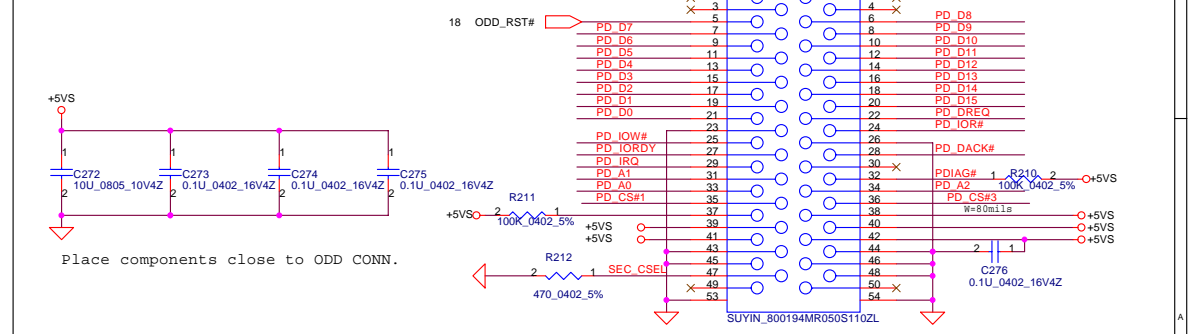
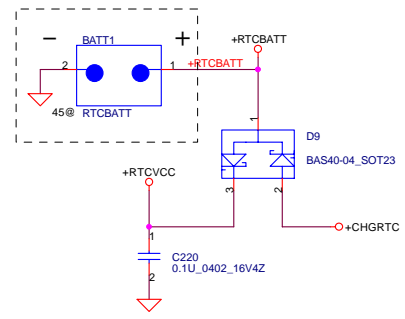
2nd SATA HDD CONN



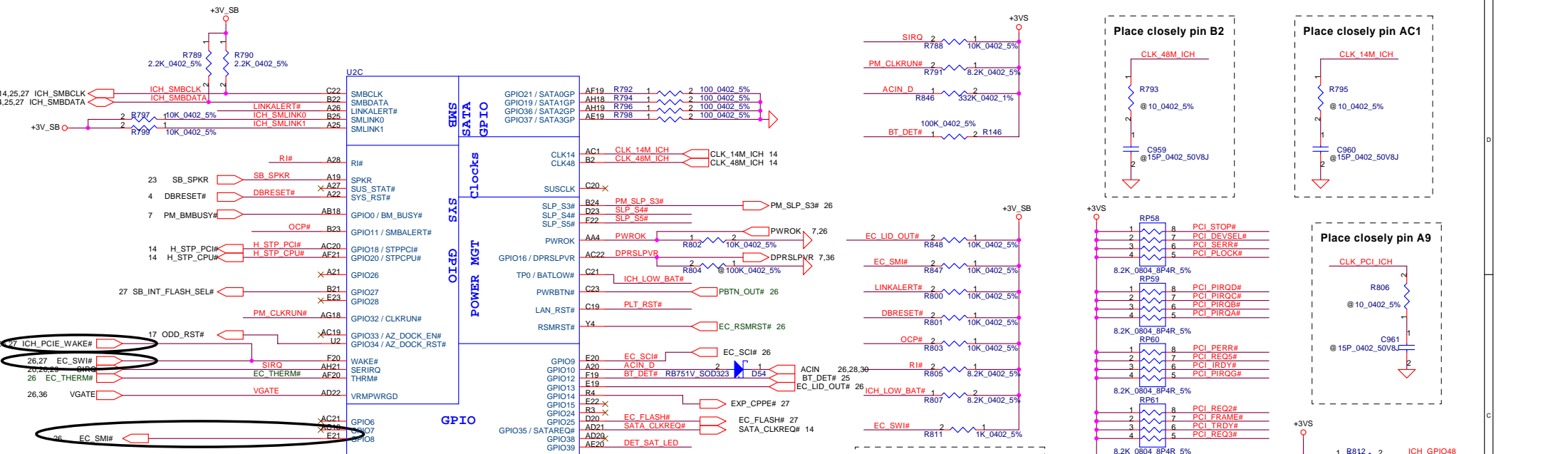
Layout Note:

RTC Battery

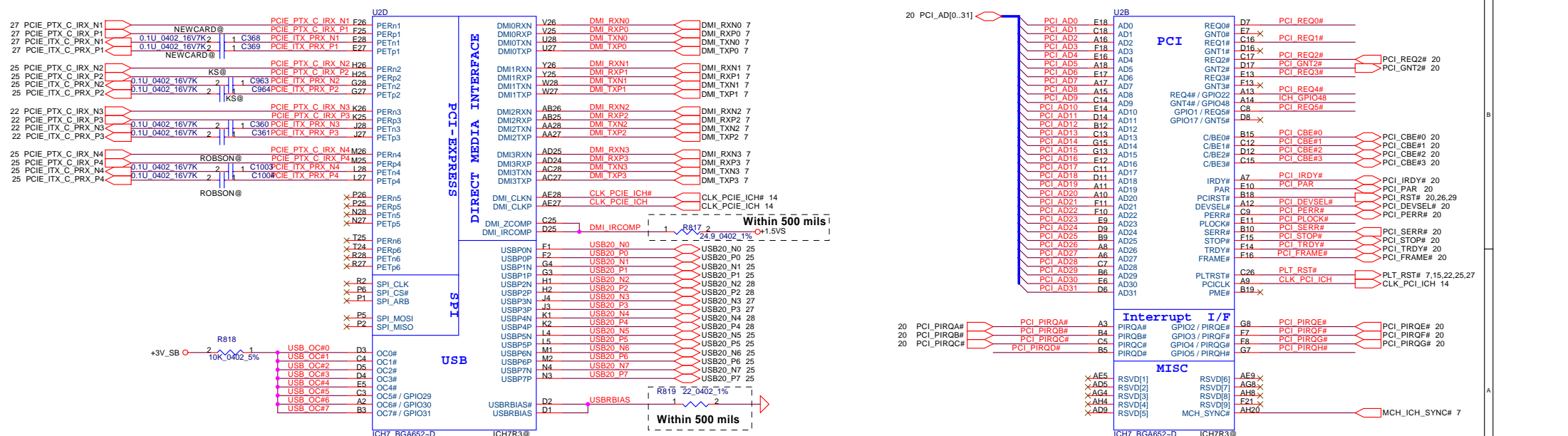
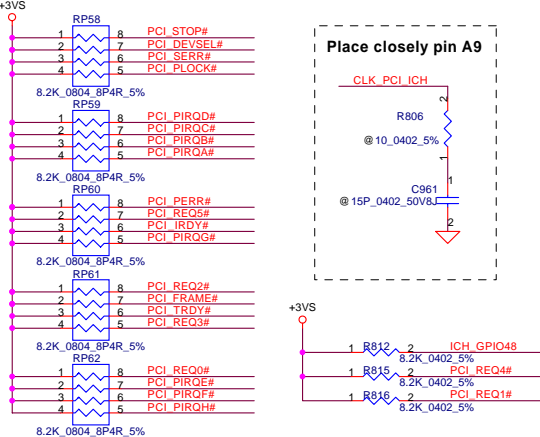
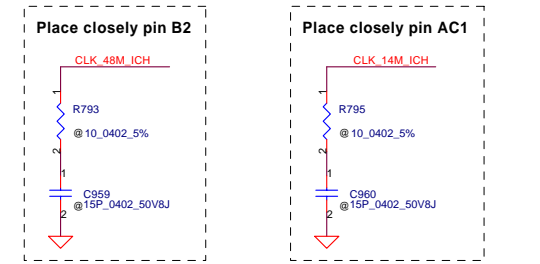
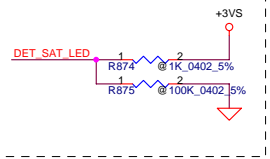
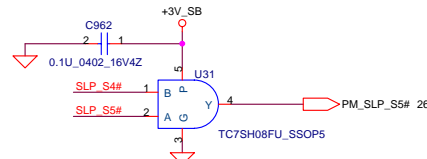
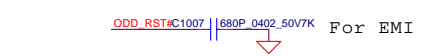
1. Under BATT1 battery Body, no Trace no Via
2. BATT1 +- PIN keep out 80mil from other component ,trace and via



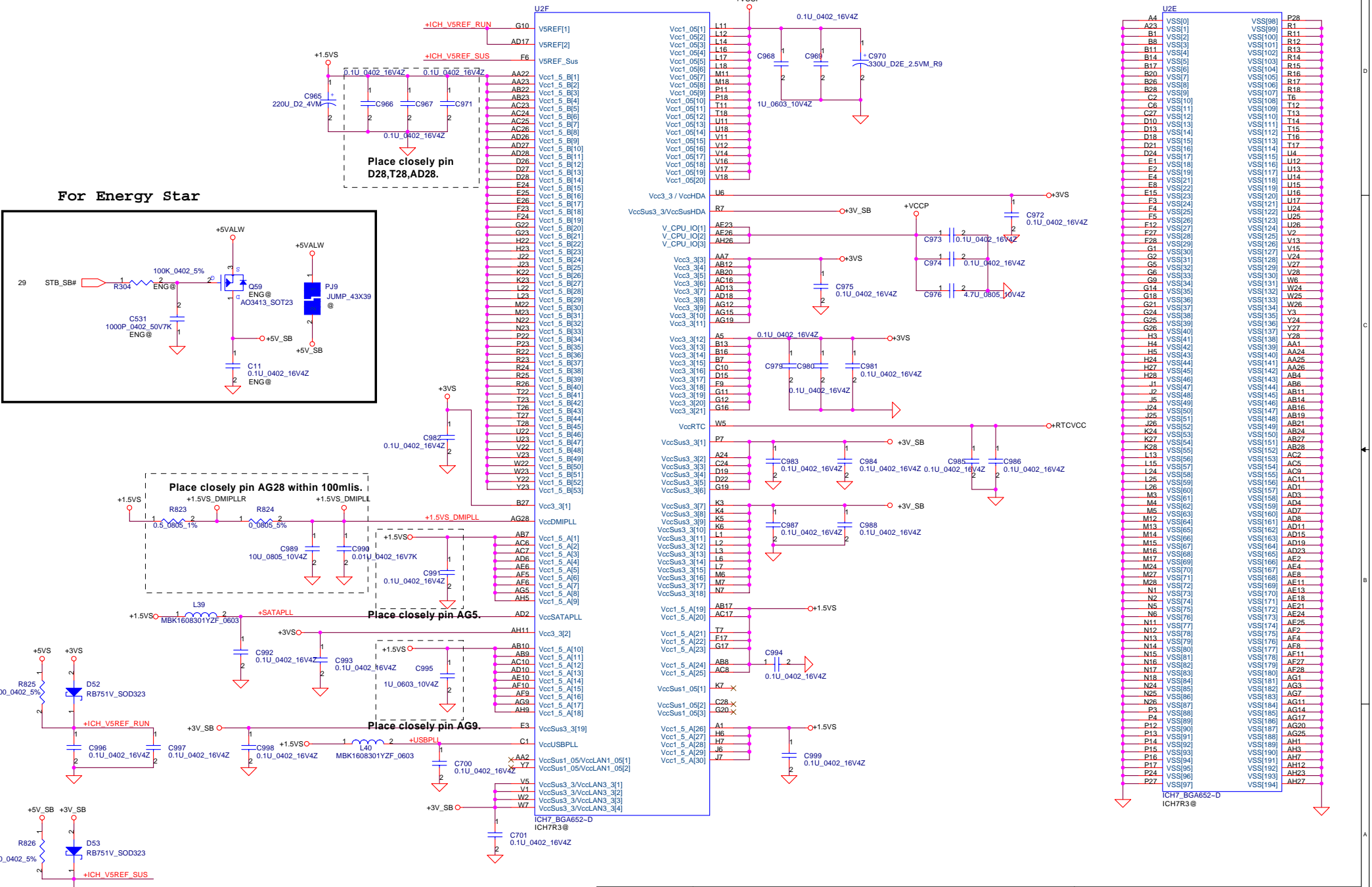
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Issued Date	2006/11/05	Deciphered Date	2009/11/05
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EC need tri-state or set as GPI when no driving above signal



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For Energy Star

Place closely pin AG28 within 100mils.

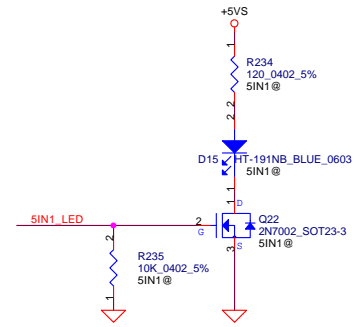
Place closely pin AG5.

Place closely pin AG9.

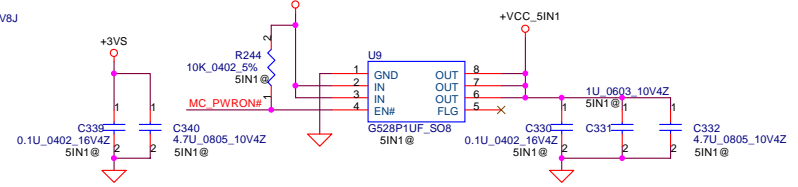
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Issued Date	2006/11/05	Deciphered Date
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Title		
Compal Electronics, Inc.		
ICH7-M(3/3)		
Size	Document Number	Rev
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Date:	Tuesday, February 06, 2007	Sheet 19 of 39

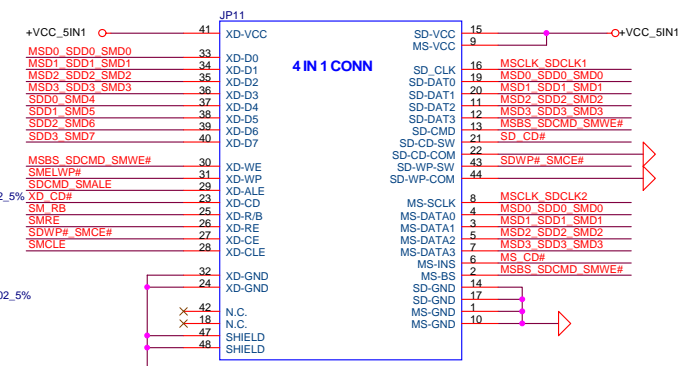
4 IN 1 LED



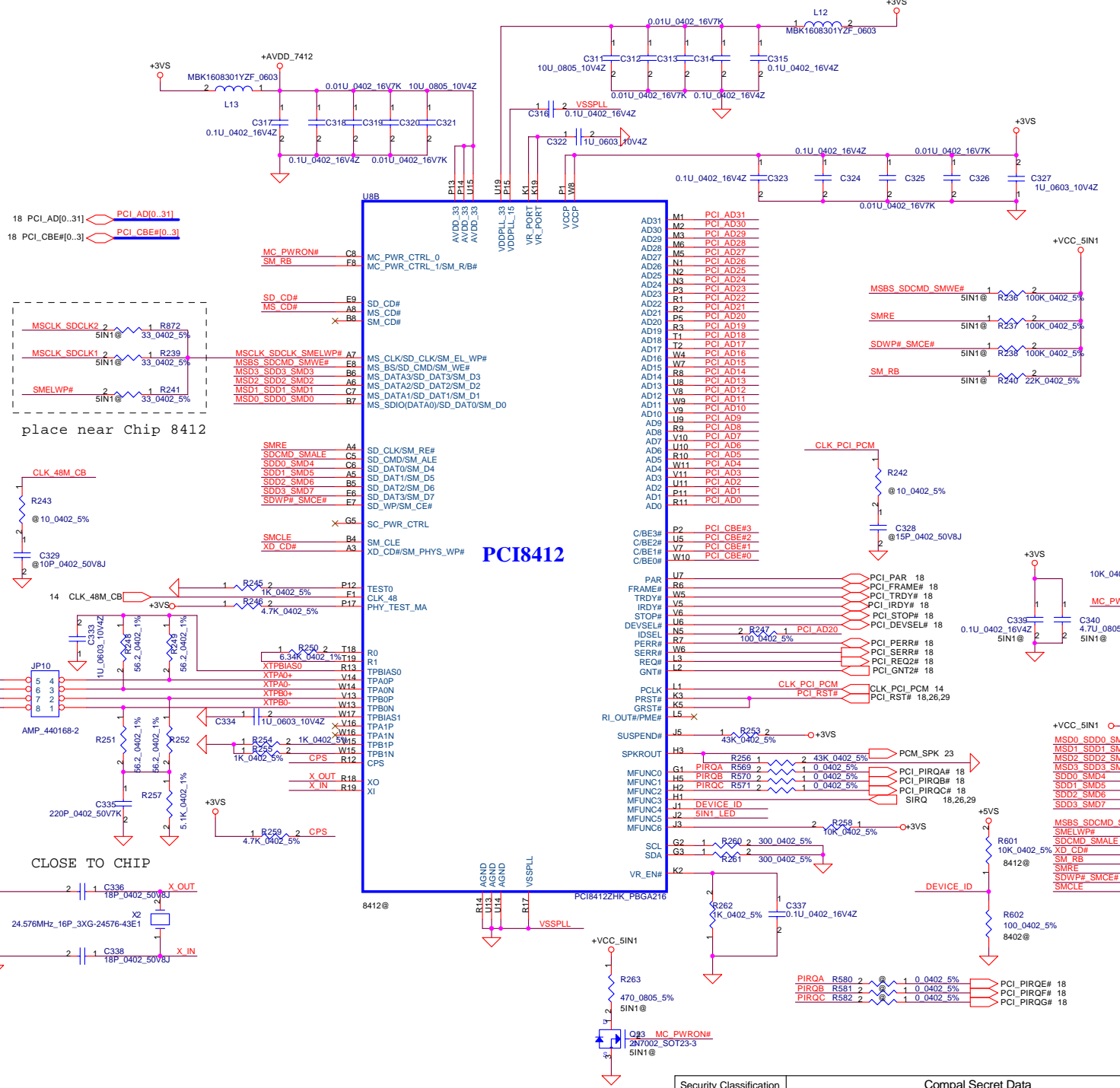
4 In 1 Card Power Switch



4 in 1 CardReader Conn.



Bottom Side, Normal Insertion



PCI8412

place near Chip 8412

CLOSE TO CHIP

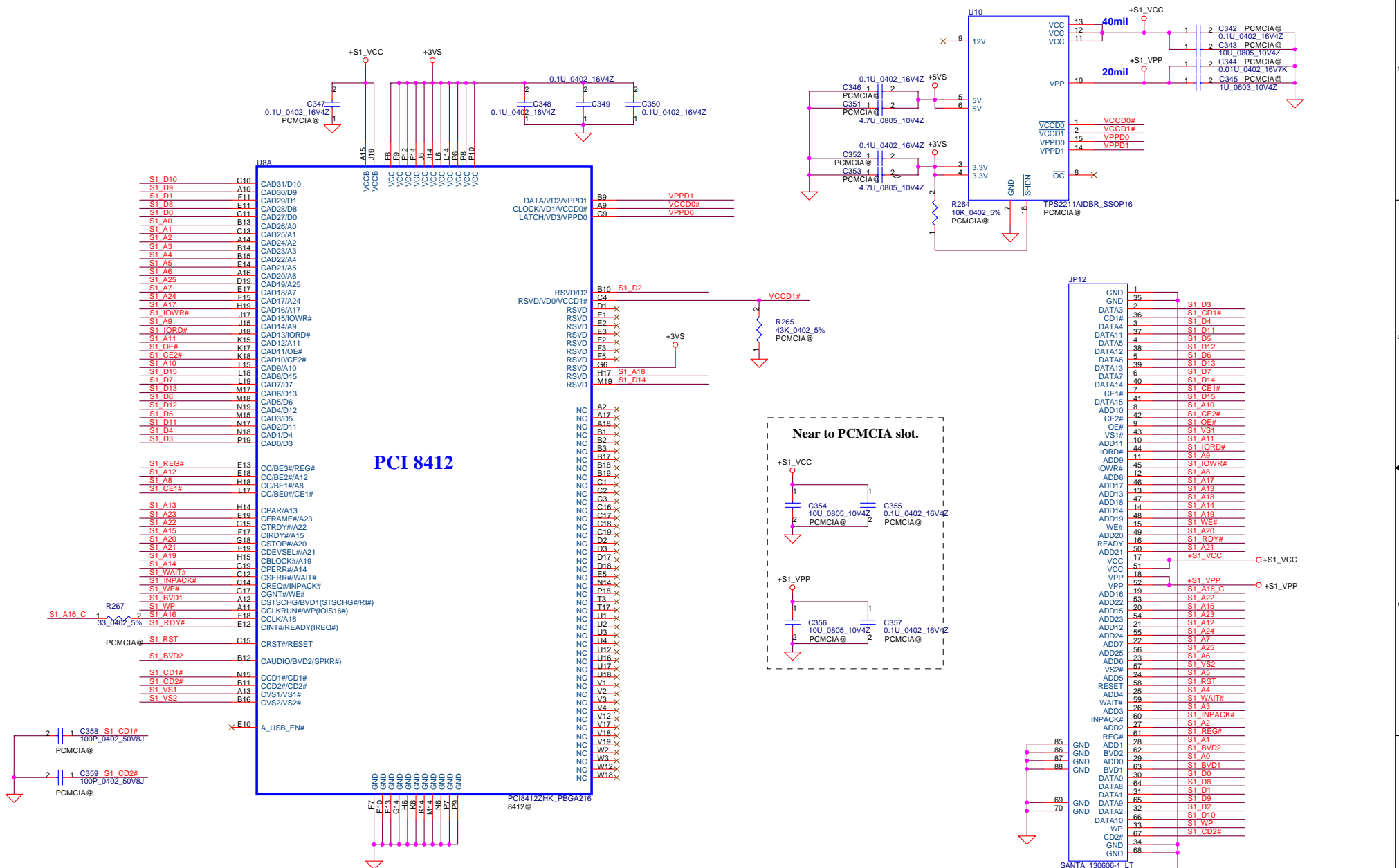
Security Classification	Compal Secret Data	
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		2009/11/13

Title		Compal Electronics, Inc.	
Size		Document Number	
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Rev 0.2

CardBus Power Switch



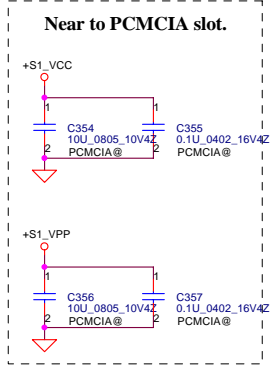
S1 D10	C10	CAD31/D10
S1 D9	A10	CAD30/D9
S1 D1	F11	CAD29/D1
S1 D8	E11	CAD28/D8
S1 D0	C11	CAD27/D0
S1 A0	B13	CAD26/A0
S1 A2	C13	CAD25/A1
S1 A3	B14	CAD23/A3
S1 A4	B15	CAD22/A4
S1 A5	E14	CAD21/A5
S1 A6	A16	CAD20/A6
S1 A25	D19	CAD19/A25
S1 A7	F17	CAD18/A7
S1 A24	F18	CAD17/A24
S1 A17	H19	CAD16/A17
S1 IOWR#	J17	CAD15/IOWR#
S1 A9	J15	CAD14/A9
S1 IORD#	J18	CAD13/IORD#
S1 A11	J18	CAD12/A11
S1 OE#	K17	CAD11/OE#
S1 CE2#	K18	CAD10/CE2#
S1 A10	L18	CAD9/A10
S1 D15	L18	CAD8/D15
S1 D7	L19	CAD7/D7
S1 D13	M17	CAD6/D13
S1 D6	M18	CAD5/D6
S1 D12	M18	CAD4/D12
S1 D5	M15	CAD3/D5
S1 D11	N17	CAD2/D11
S1 D4	N18	CAD1/D4
S1 D3	P19	CAD0/D3

S1 REG#	E13	CC/BE3#/REG#
S1 A12	E18	CC/BE2#/A12
S1 A8	H18	CC/BE1#/A8
S1 CE1#	L17	CC/BE0#/CE1#
S1 A13	H14	CPAR/A13
S1 A23	E19	CFRAME#/A23
S1 A22	G15	CTRDY#/A22
S1 A15	F17	CRDY#/A15
S1 A20	F19	CSTOP#/A20
S1 A19	H15	CDEVSEL#/A19
S1 A14	G19	CLOCK#/A14
S1 WAIT#	C12	CSERR#/WAIT#
S1 INPACK#	C12	CSERR#/INPACK#
S1 WE#	G17	CREQ#/WE#
S1 BVD1	A12	CGNT#/BVD1
S1 WP	A11	CCLKRUN#/WP
S1 A16	E18	CCLK/A16
S1 RDY#	E12	CINT#/RDY#

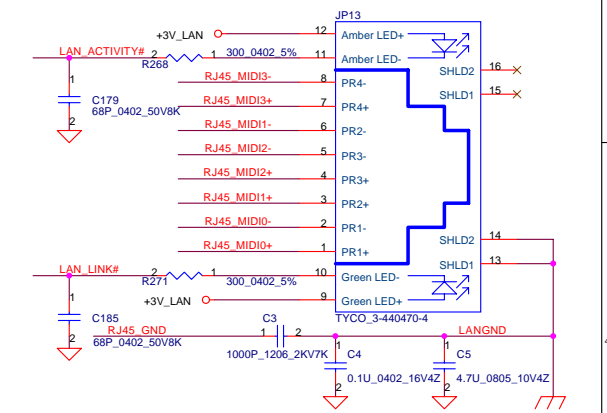
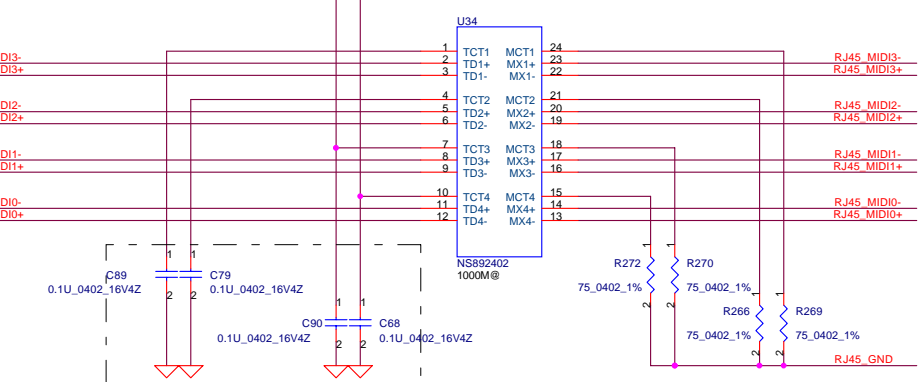
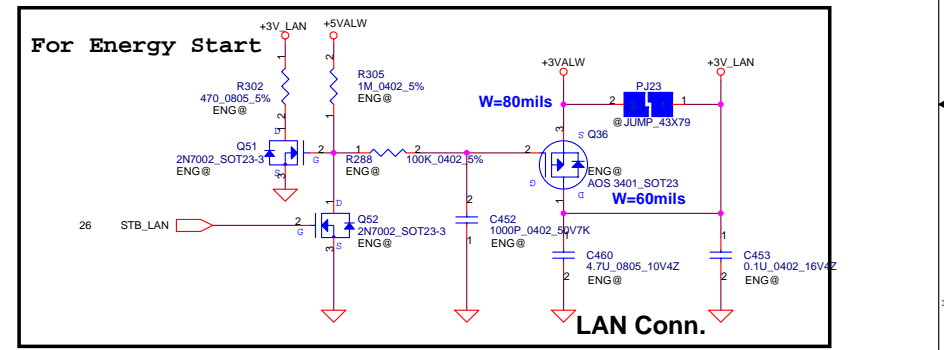
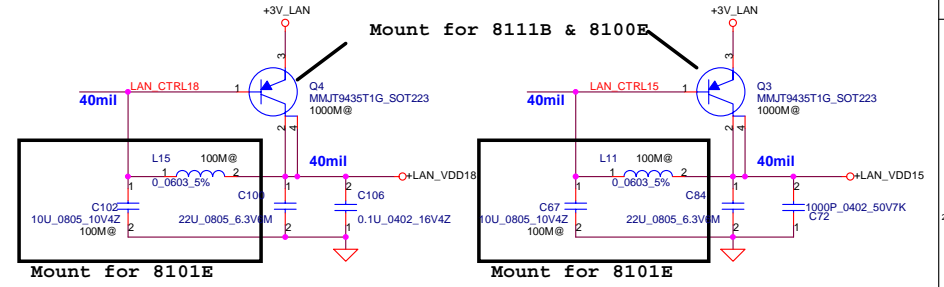
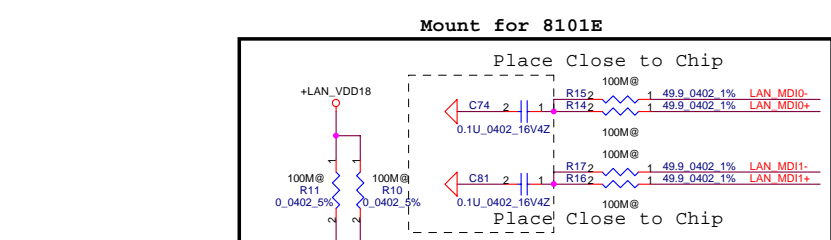
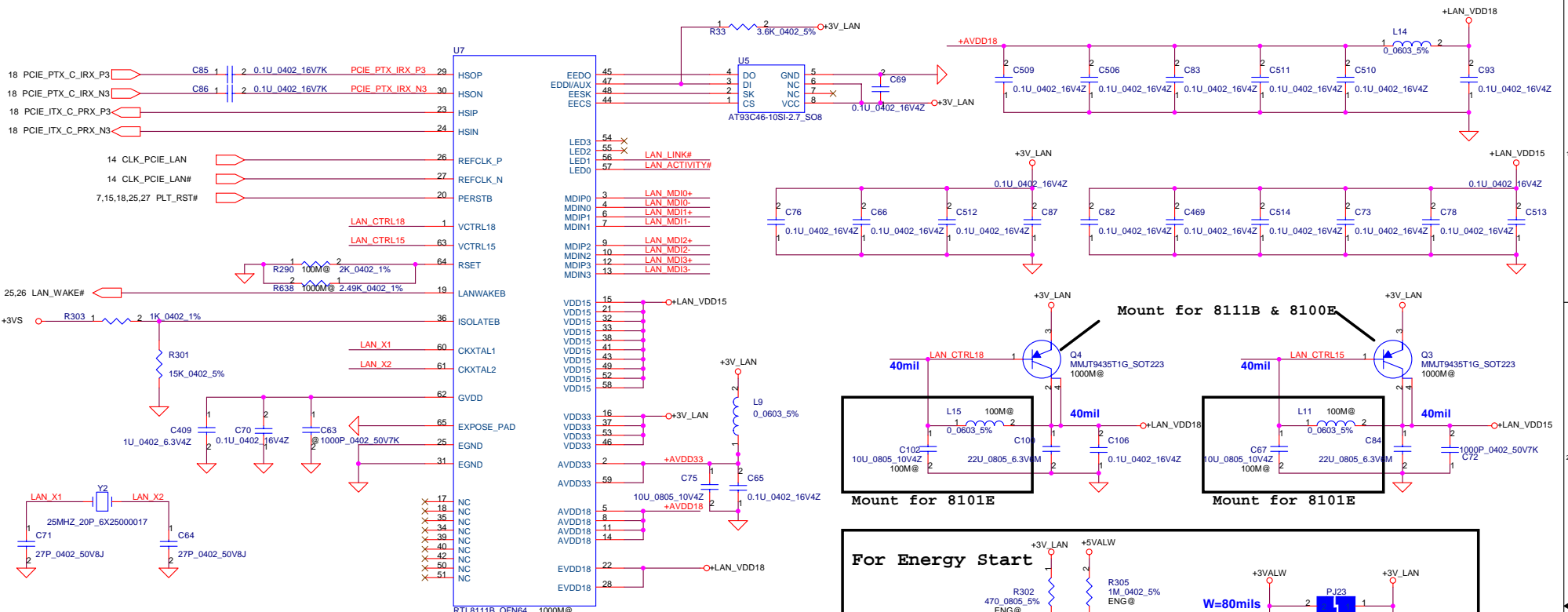
S1 RST	C18	CRST#/RST
S1 BVD2	B12	CAUDIO/BVD2
S1 CD1#	N15	CCD1#/CD1#
S1 CD2#	B11	CCD2#/CD2#
S1 VS1	A13	CVS1#/VS1#
S1 VS2	B16	CVS2#/VS2#

PCI 8412

PCI84122HK_PBG216
8412@

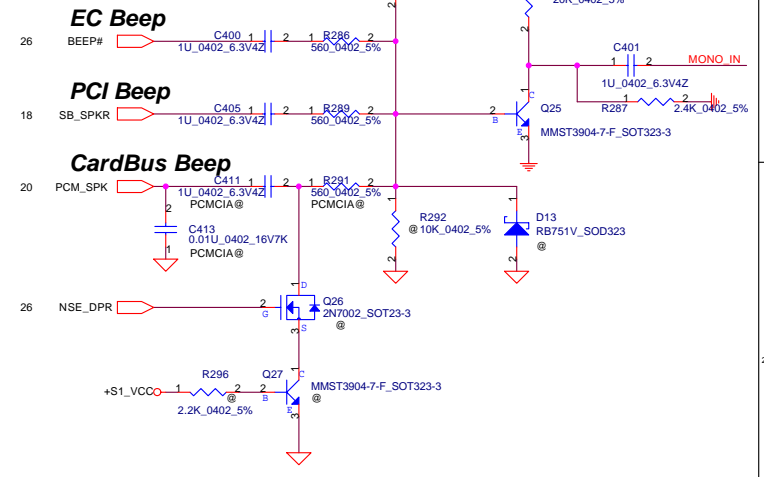
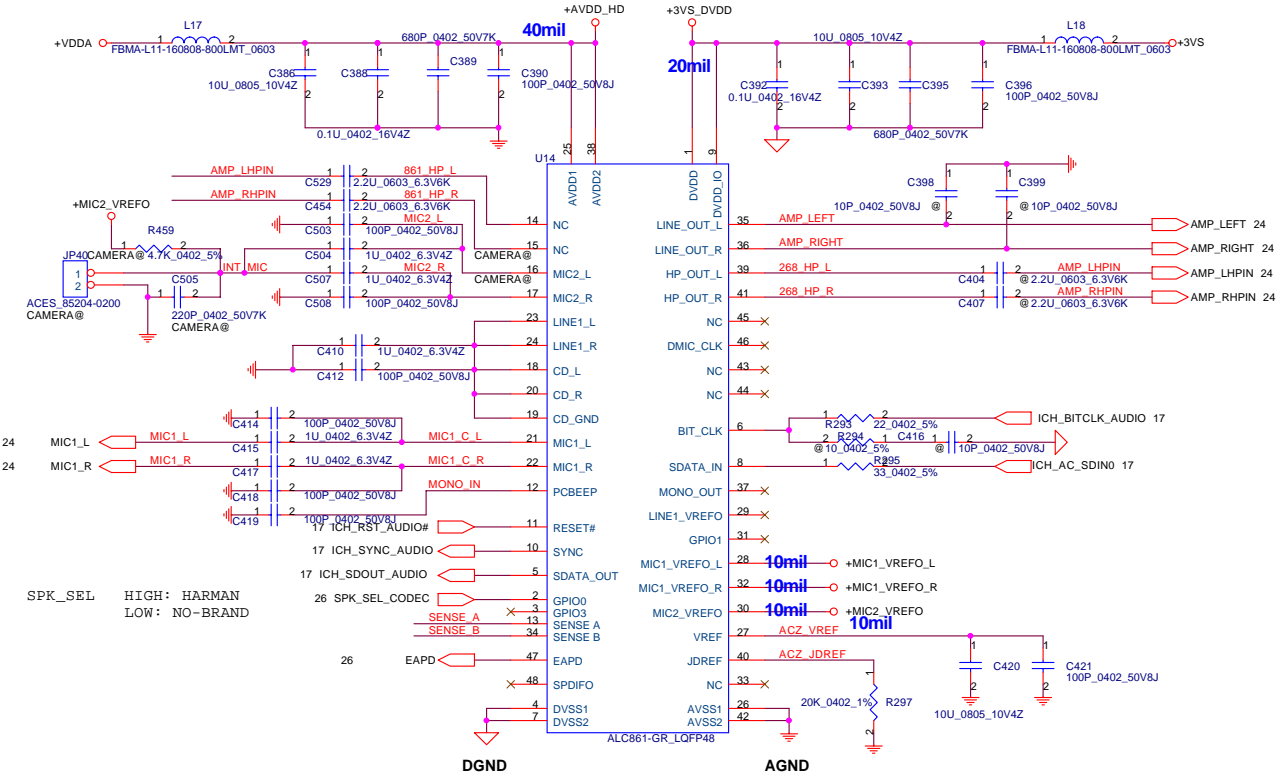


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Title PCI7412/CB/CB SLOT			Document Number ISRAE/MB LA-3711P
Date:	Tuesday, February 06, 2007	Sheet	21 of 39

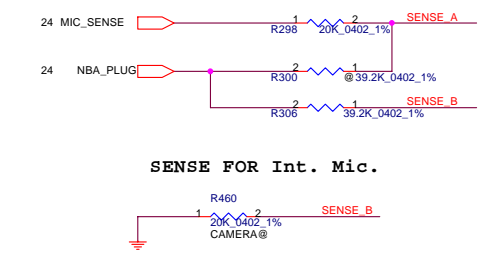


Security Classification			Compal Secret Data		
Issued Date	2006/10/31	Deciphered Date	2009/11/13	Title	RTL8100CL
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Date:	Tuesday, February 16, 2007	Sheet	22	of	39

HD Audio Codec

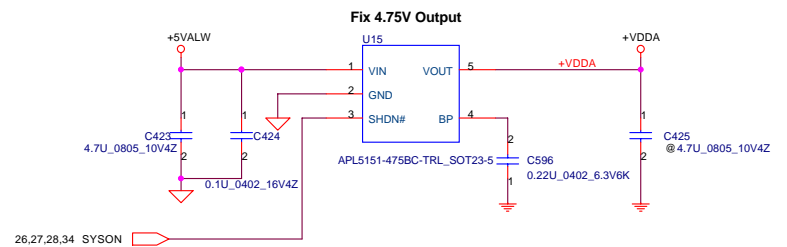


SPK_SEL HIGH: HARMAN
LOW: NO-BRAND

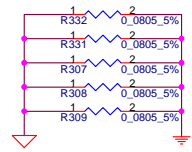


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

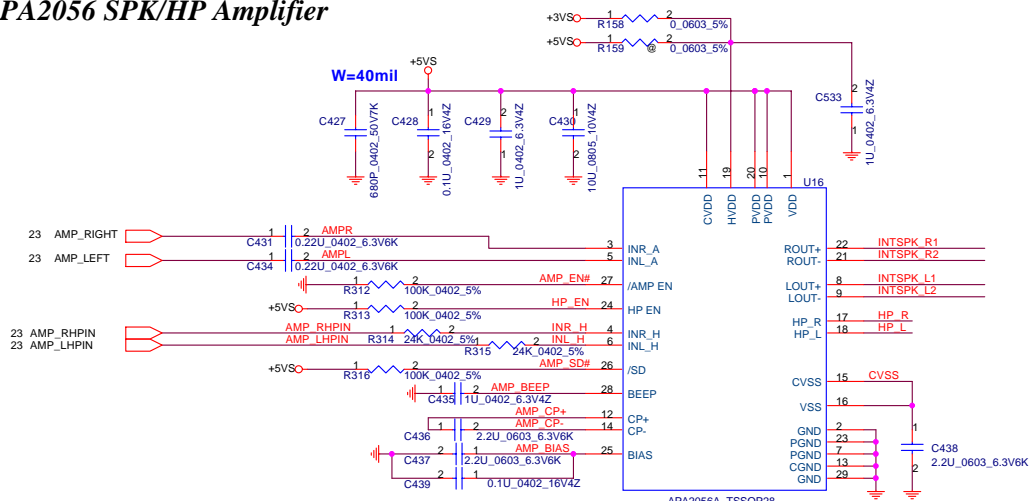
Regulator for CODEC



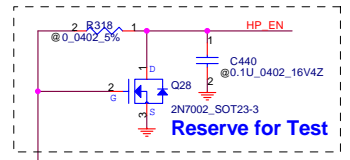
Moat Bridge



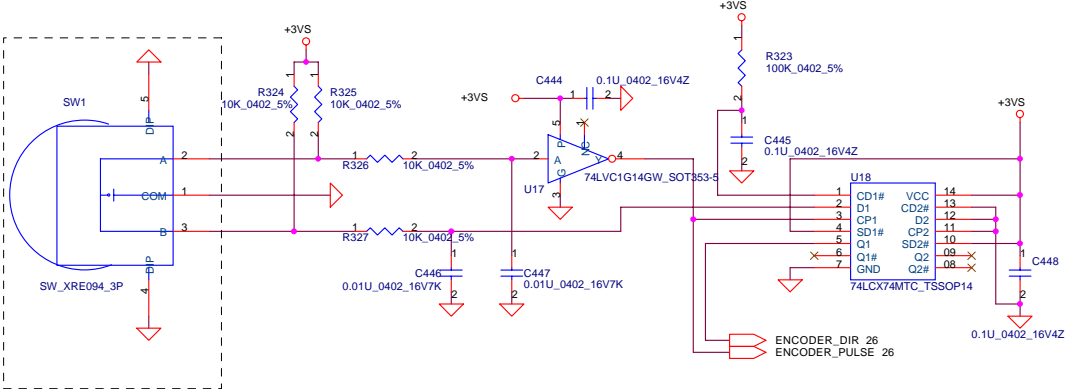
APA2056 SPK/HP Amplifier



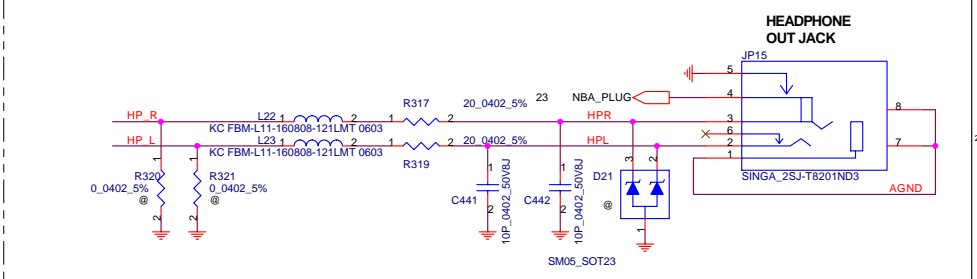
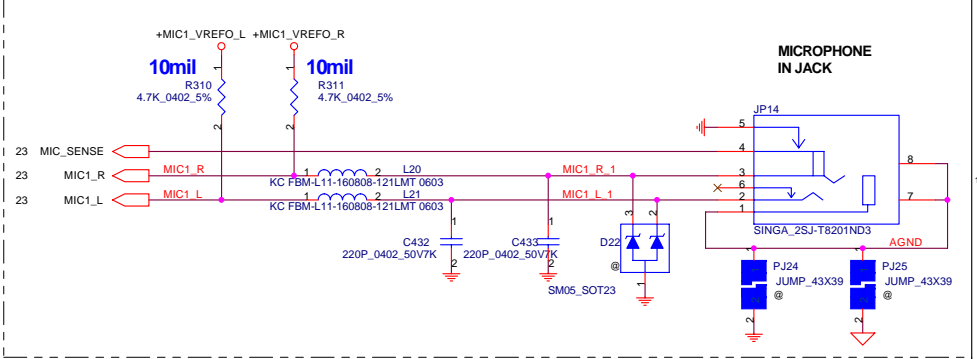
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



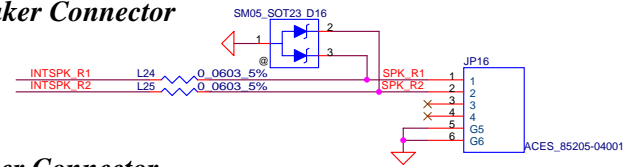
Volume Control



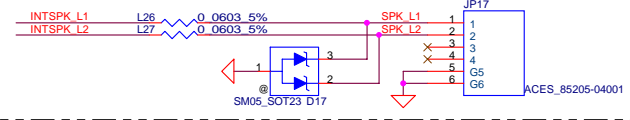
MP need to change P/N DEB00000600



Right Speaker Connector

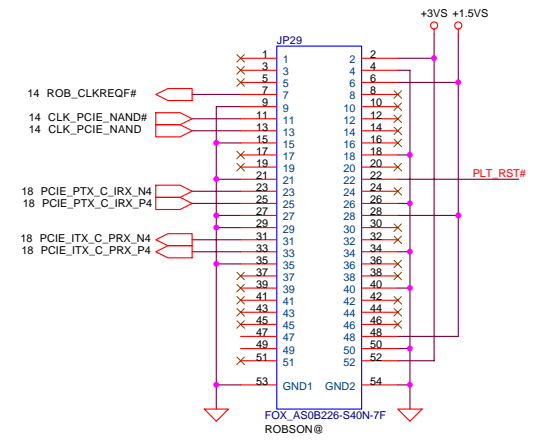


Left Speaker Connector

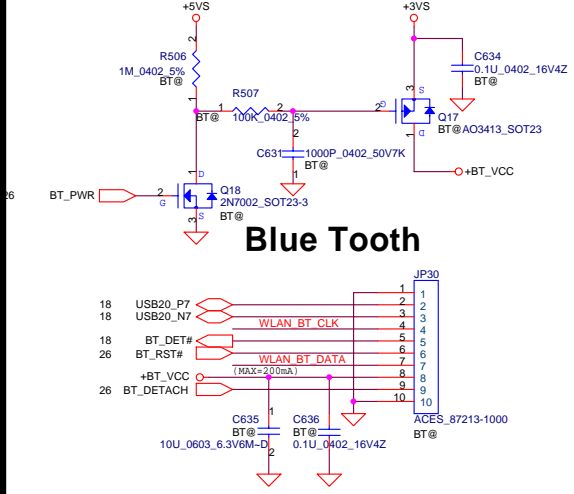


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Size	Document Number	Date		Rev	
Custom	ISRAE MB LA-3711P	Tuesday, February 06, 2007		24 of 39	

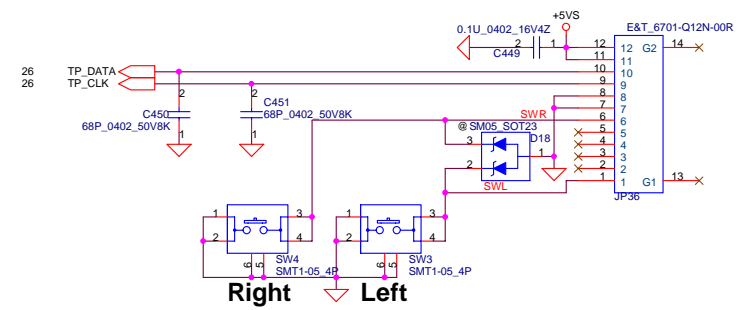
NAND mini Card(Robson support)



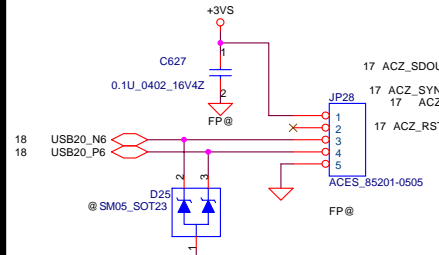
Blue Tooth



TP CONN.

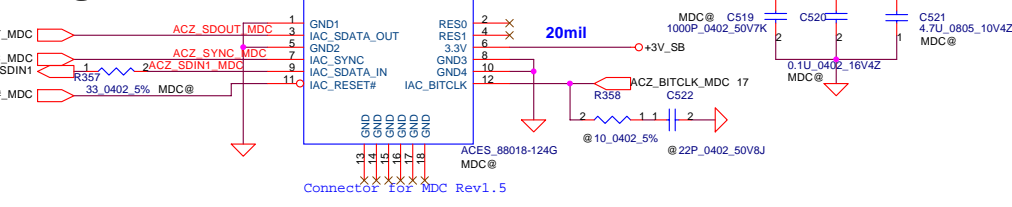


Fingerprint Conn

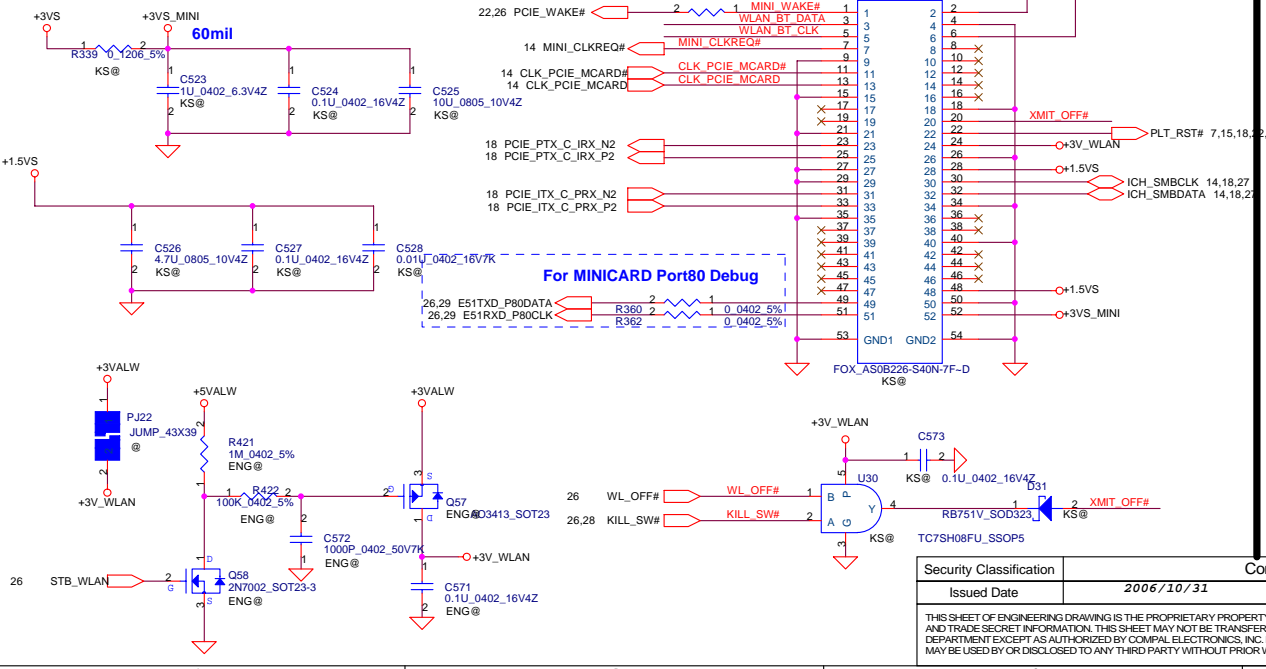


MDC

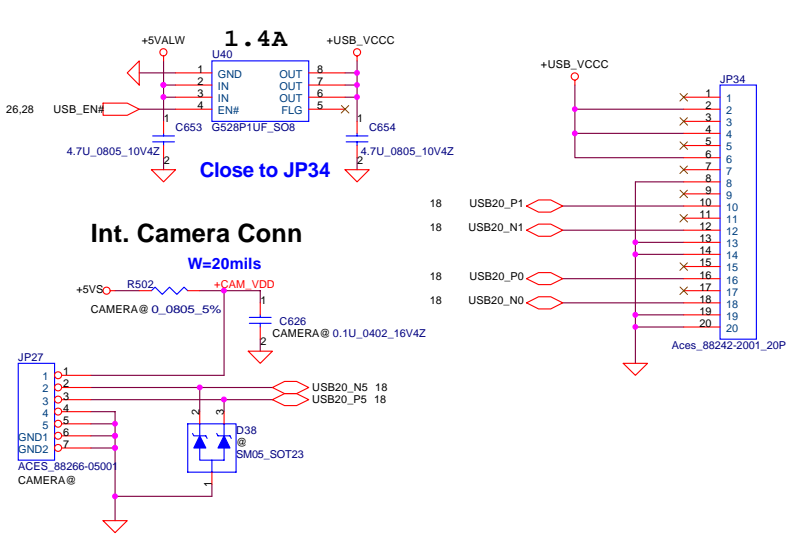
MDC Conn.



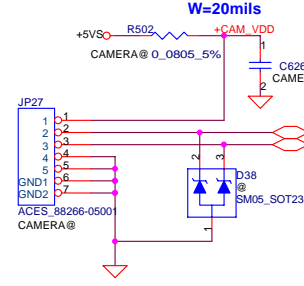
MINI CARD



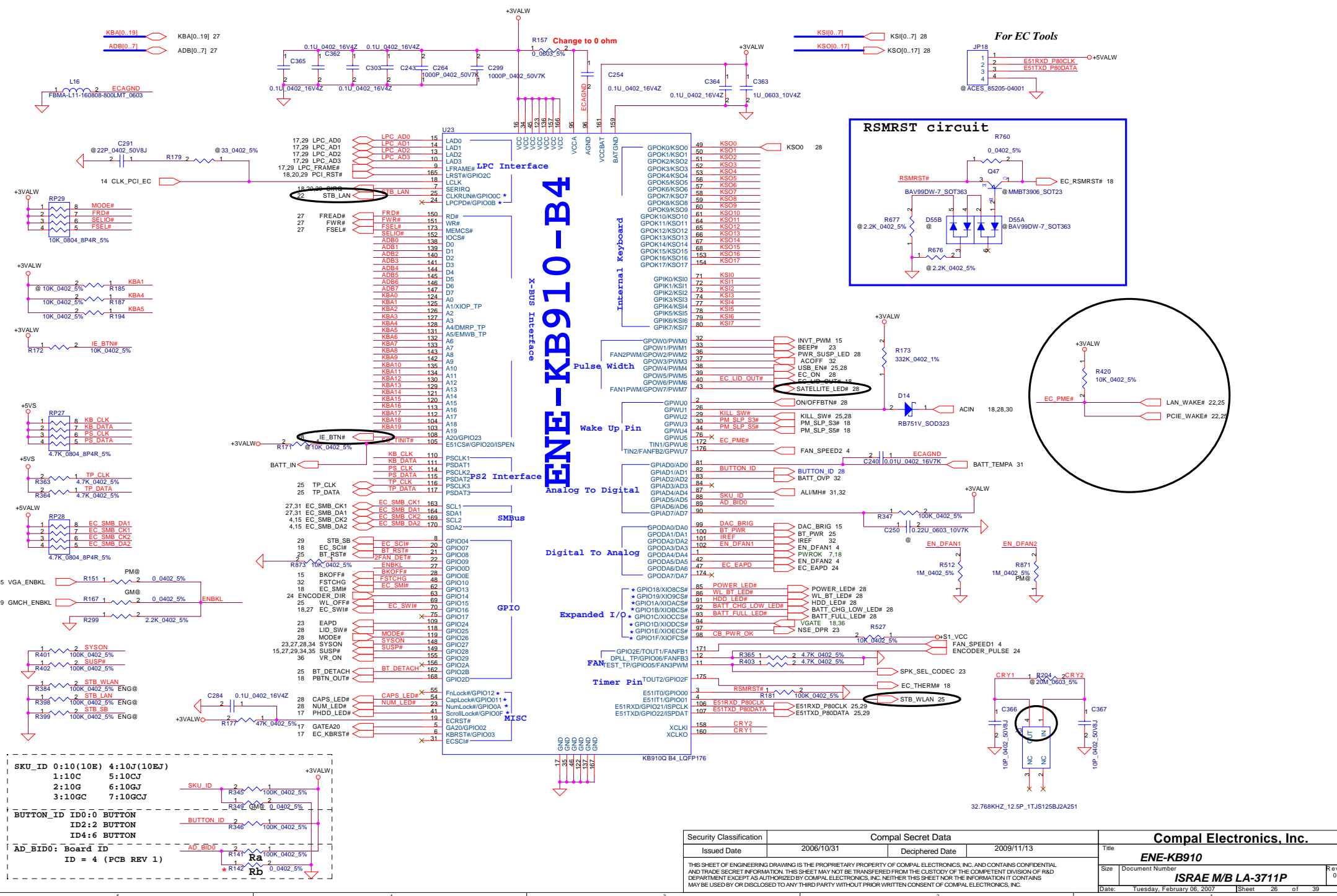
USB Board Connector



Int. Camera Conn

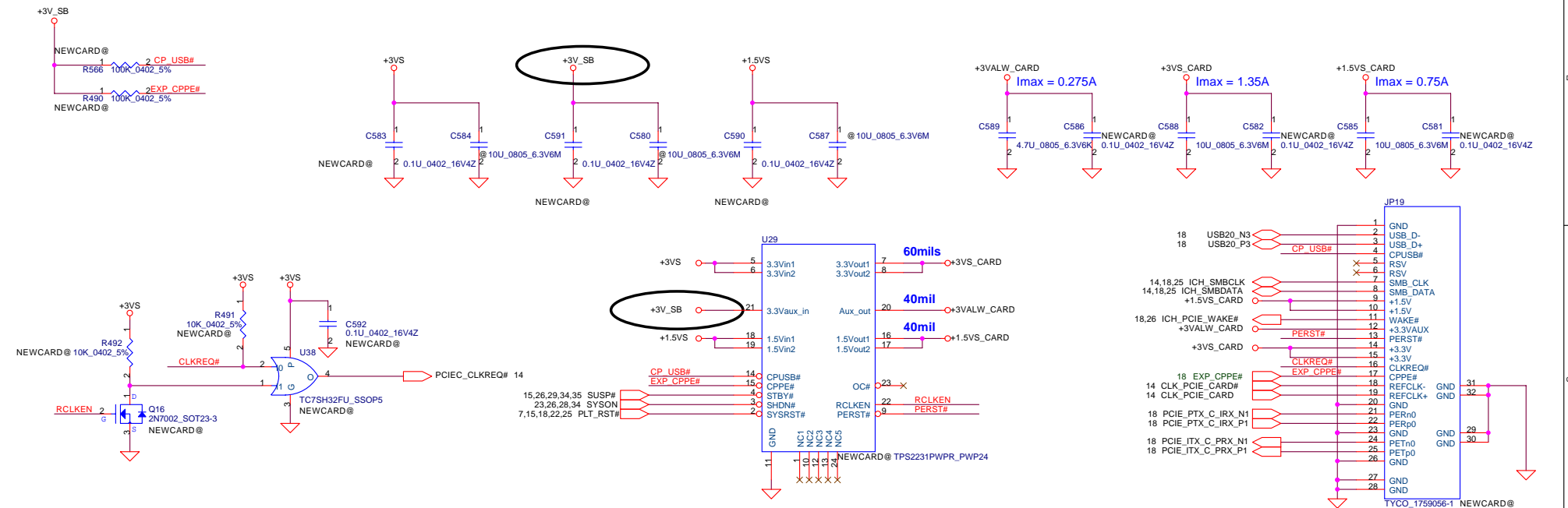


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<p>Size Document Number</p> <p>ISRAE M/B LA-3711P</p>			Rev 0.2
Date: Tuesday, February 06, 2007 Sheet 25 of 39			

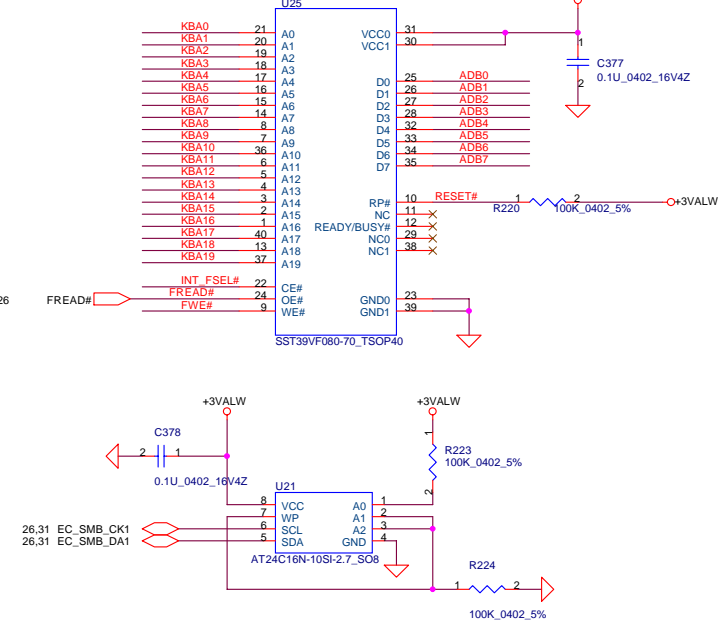


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2006/10/31		Deciphered Date		2009/11/13	
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2006/10/31		2009/11/13		ENE-KB910	
Size	Document Number	Title		Rev	
	ISRAE M/B LA-3711P	ISRAE M/B LA-3711P		0.2	
Date:	Tuesday, February 06, 2007	Sheet	26	of 39	

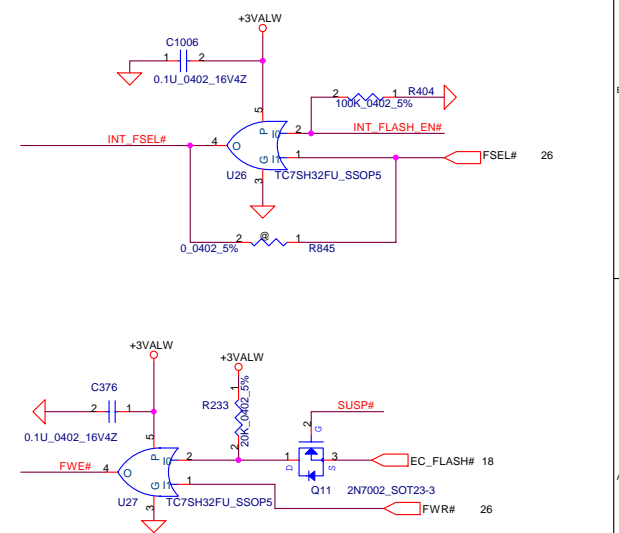
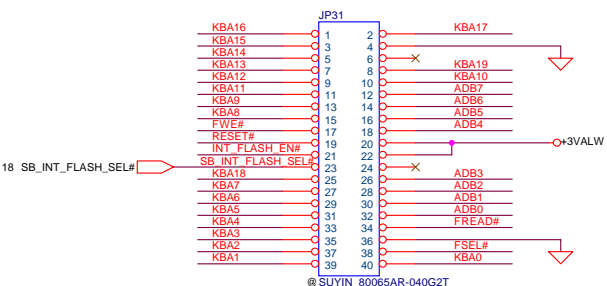
New Card



1MB Flash ROM

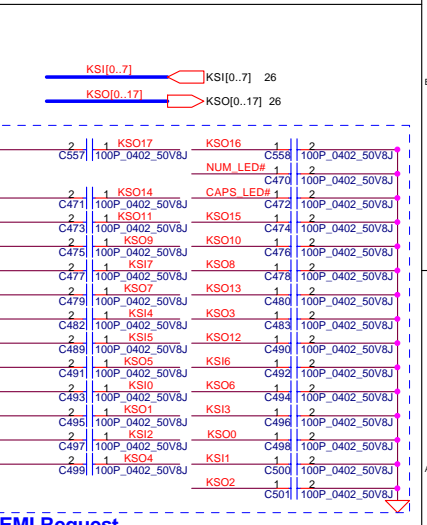
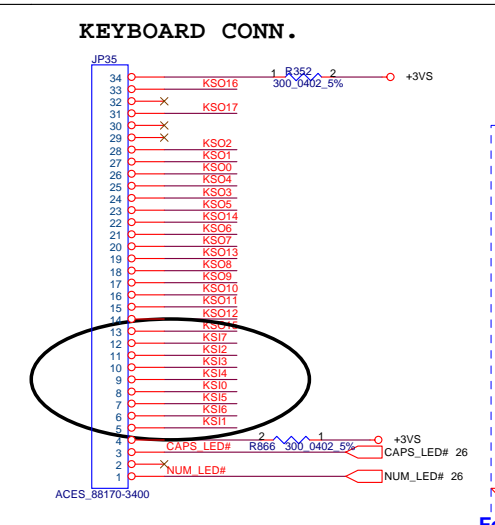
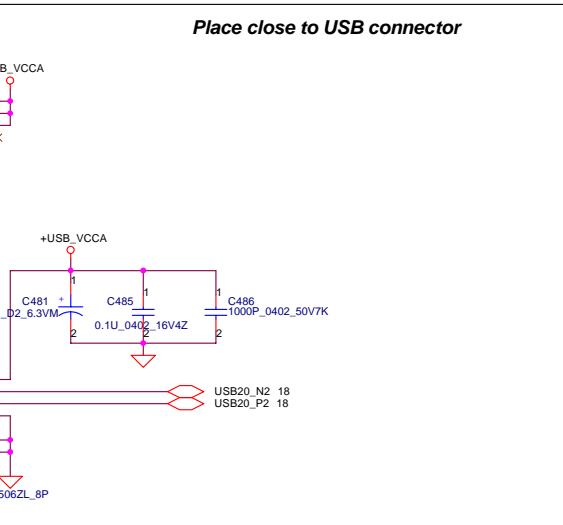
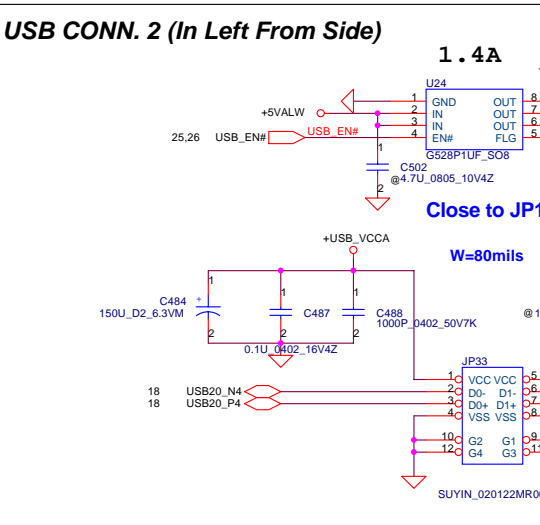
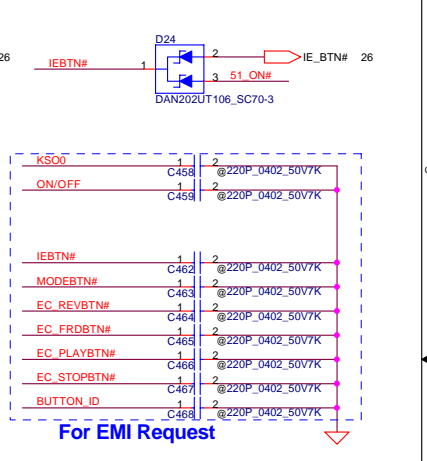
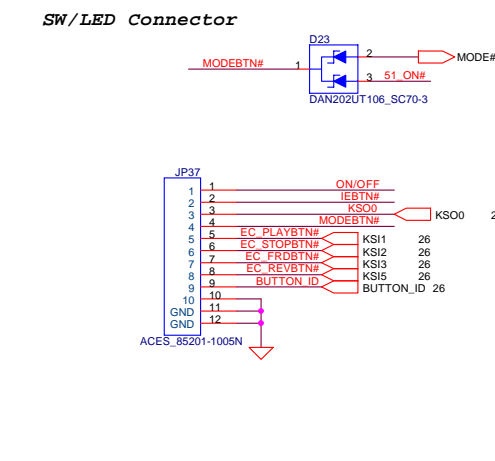
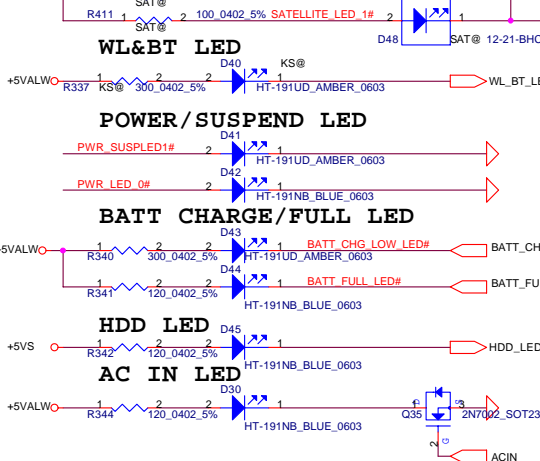
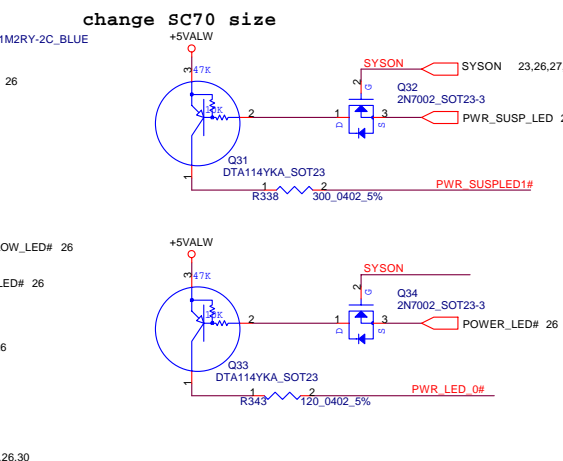
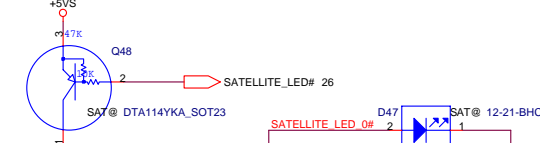
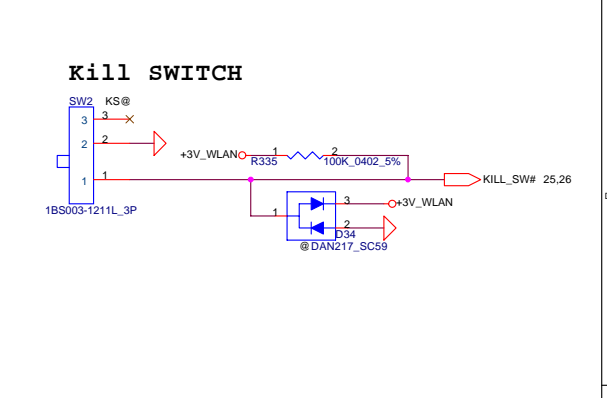
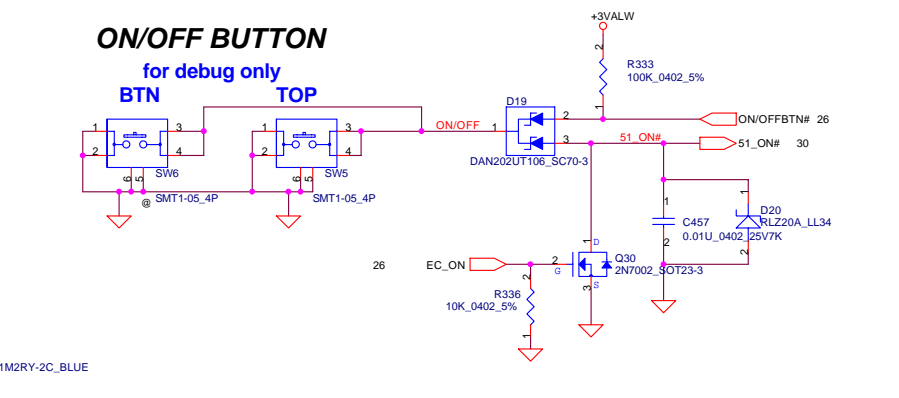
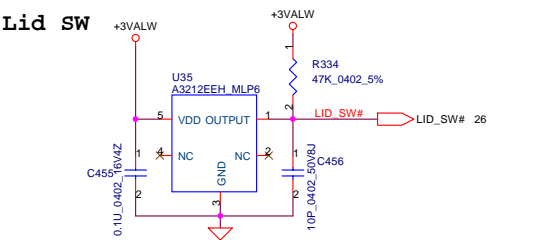


1MB ROM Socket



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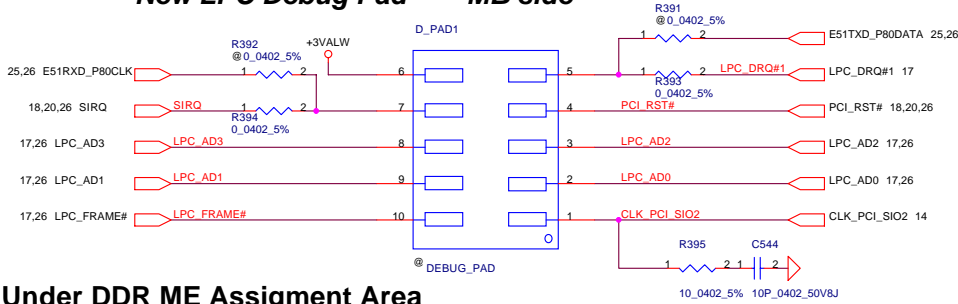
Compal Electronics, Inc.			
Title BIOS/TP-PAD/BT			
Size	Document Number	Rev 0.2	
ISRAE MB LA-3711P			
Date:	1/28/2007, February 06, 2007	Sheet	27 of 39



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Date:	Tuesday, February 05, 2007	Sheet	28	of 39

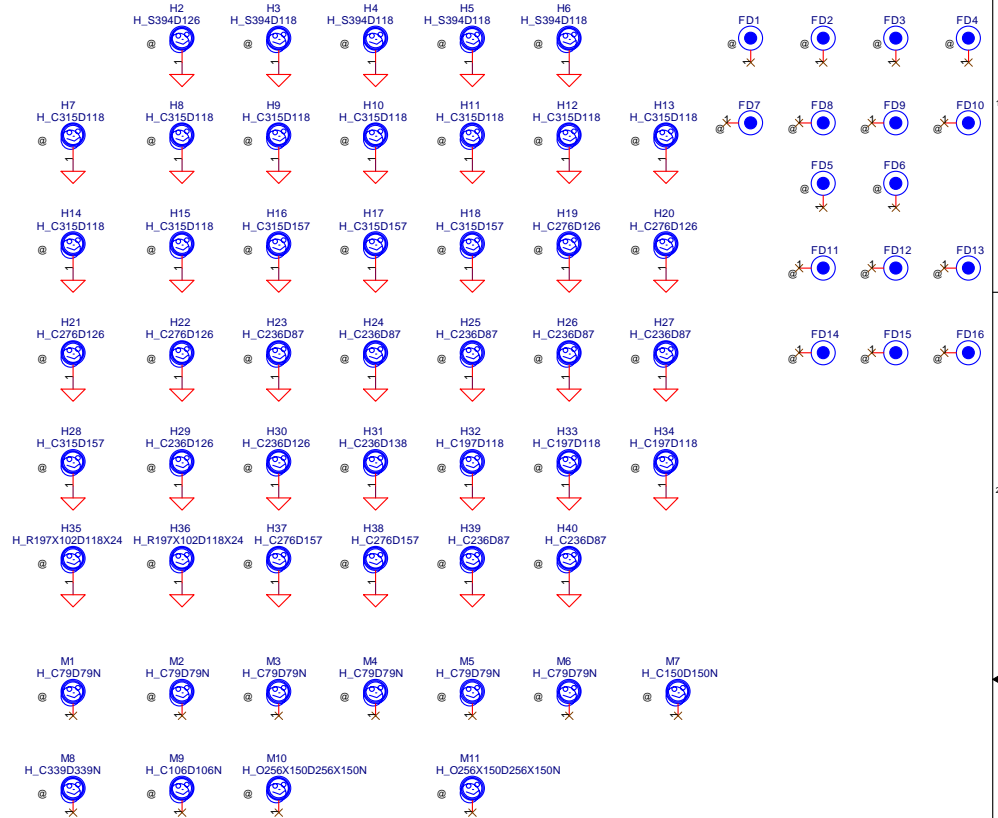
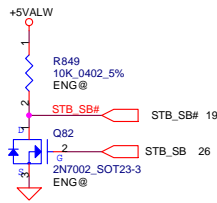
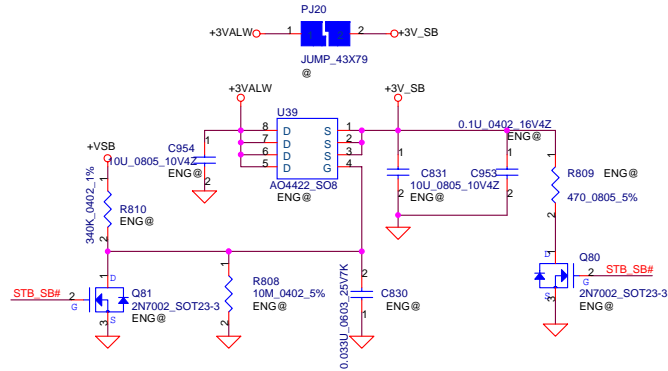
Screw Hole

New LPC Debug Pad ---- MB side

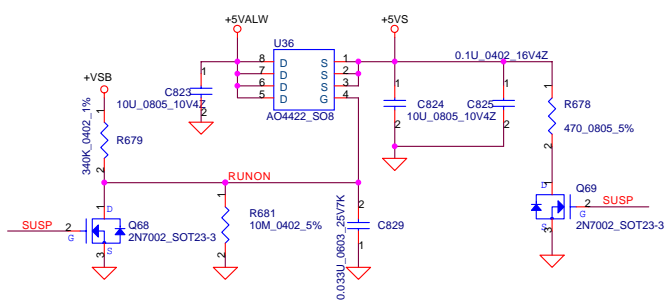


Under DDR ME Assignment Area

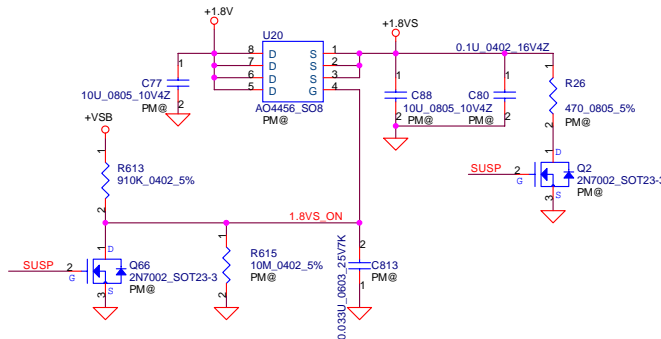
Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM



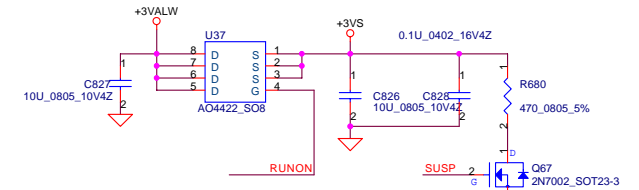
+5VALW to +5VS Transfer



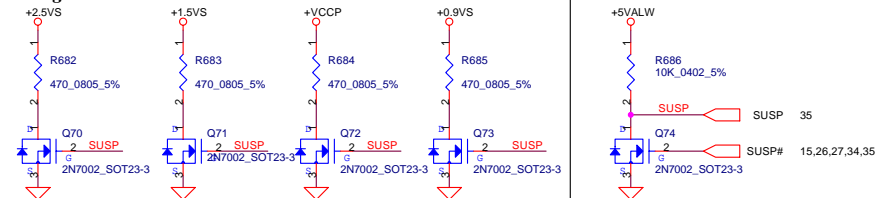
+1.8V to +1.8VS Transfer (Place close to VGA-Connector)



+3VALW to +3VS Transfer

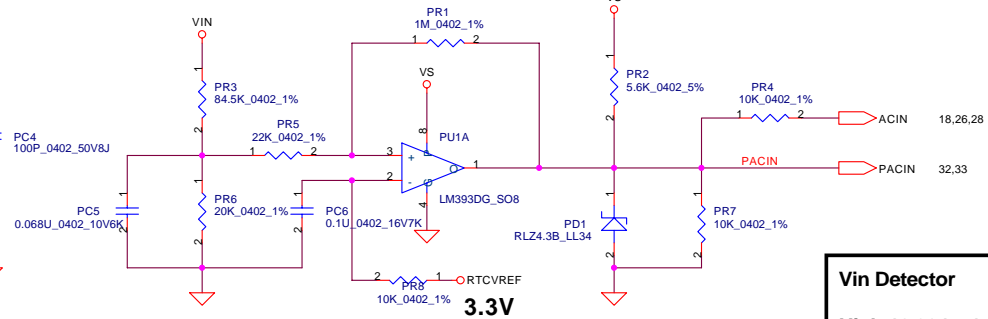
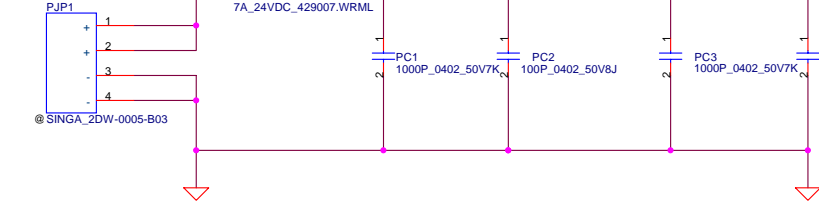


Discharge Circuit

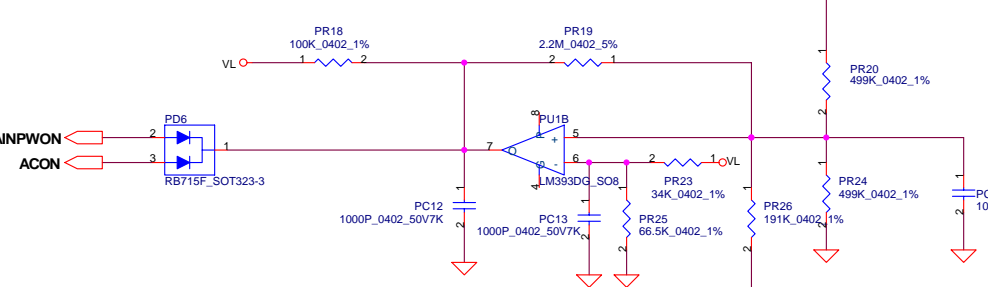
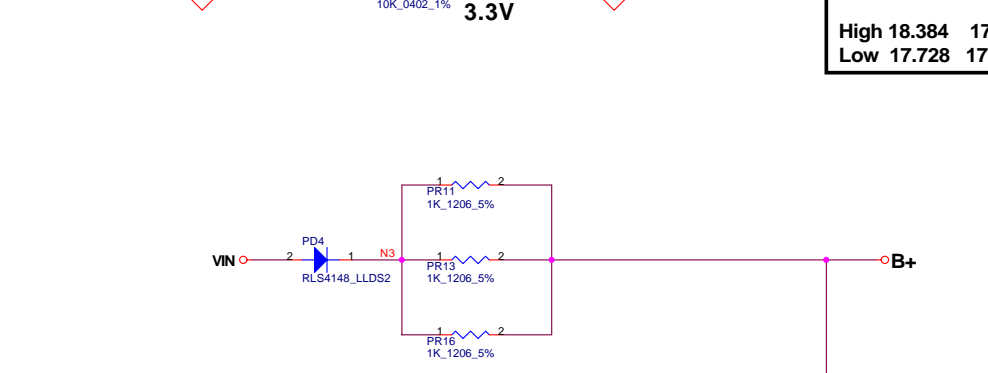
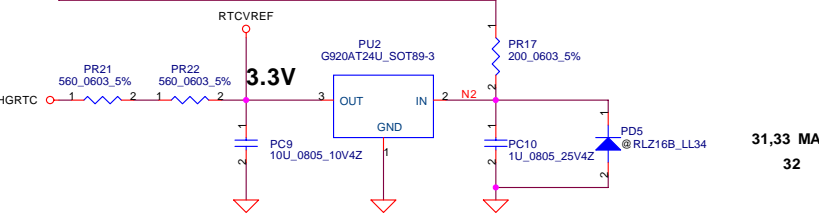
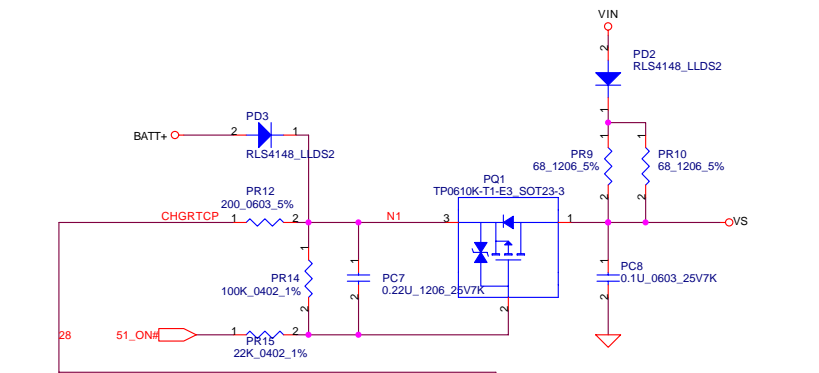


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				ISRAE MB LA-371IP	
				Date:	Tuesday, February 06, 2007
				Sheet	29 of 39
				Rev	0.2

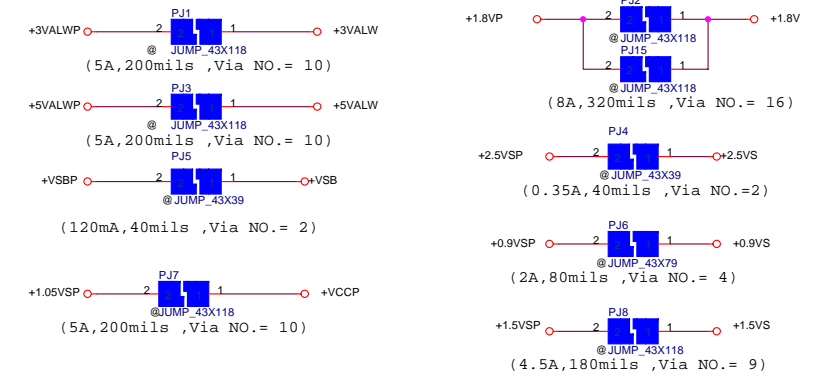
DC301001N00



Vin Detector
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



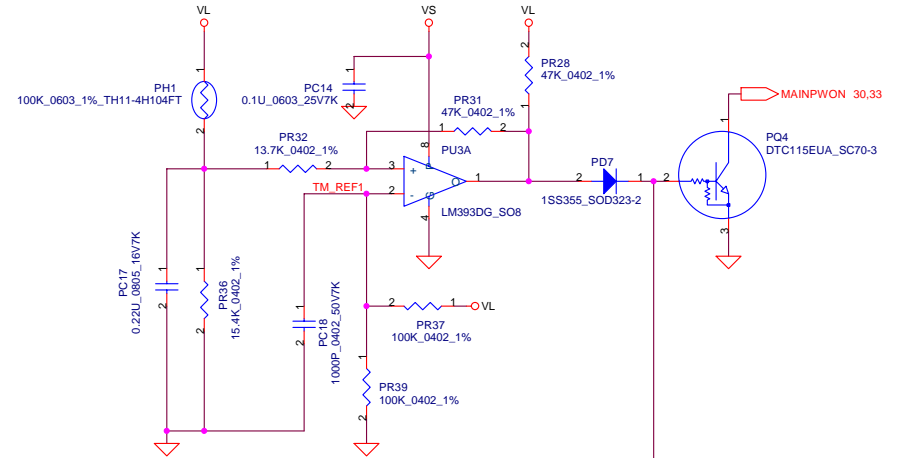
Precharge detector
15.97V/14.84V FOR
ADAPTOR



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Issued Date	2006/06/06	Deciphered Date	2009/06/05	Title	DCIN & DETECTOR
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Size	Document Number				Rev
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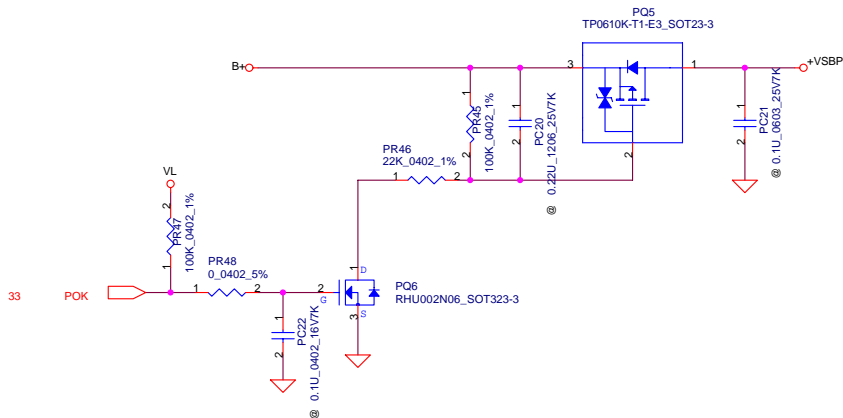
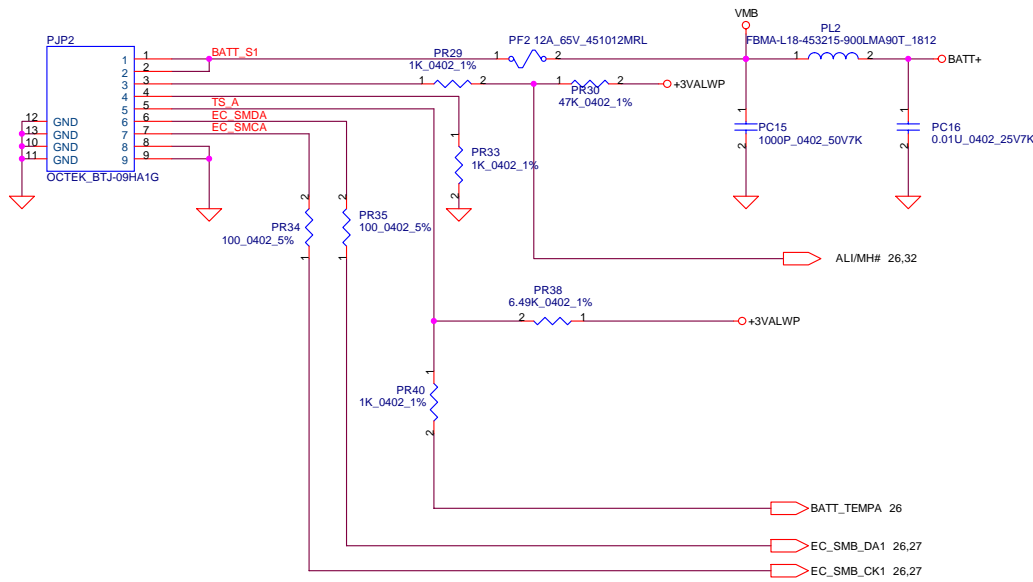
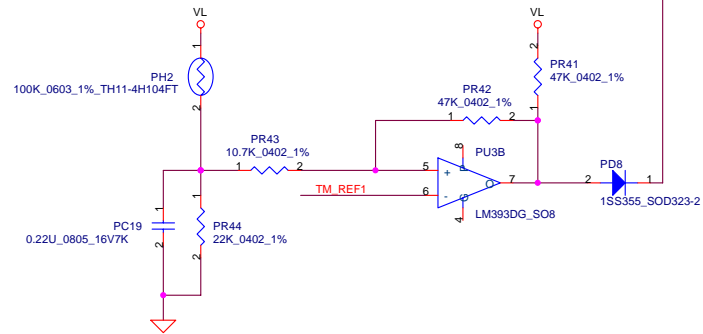
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C

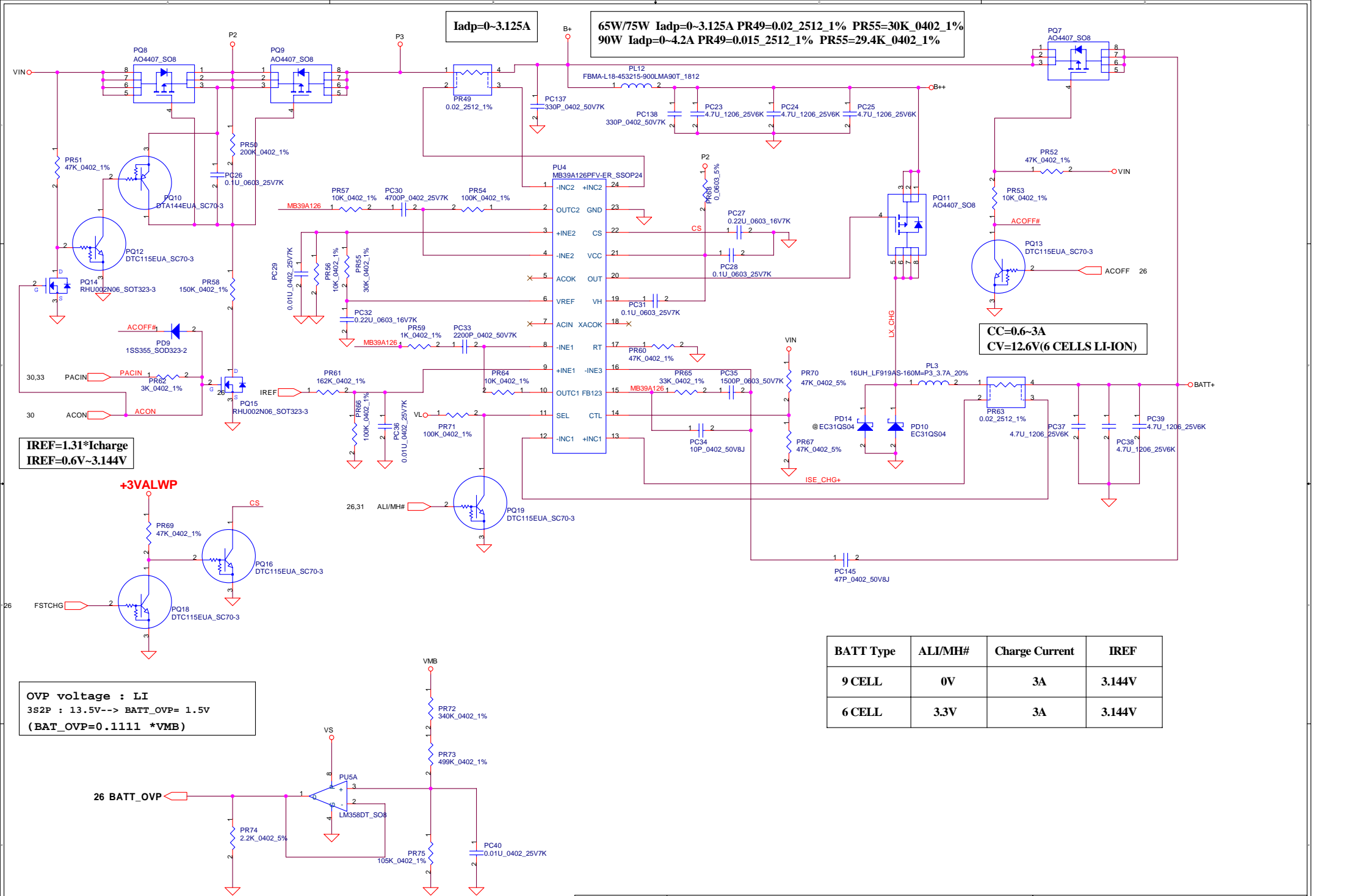


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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Iadp=0~3.125A

65W/75W Iadp=0~3.125A PR49=0.02_2512_1% PR55=30K_0402_1%
 90W Iadp=0~4.2A PR49=0.015_2512_1% PR55=29.4K_0402_1%

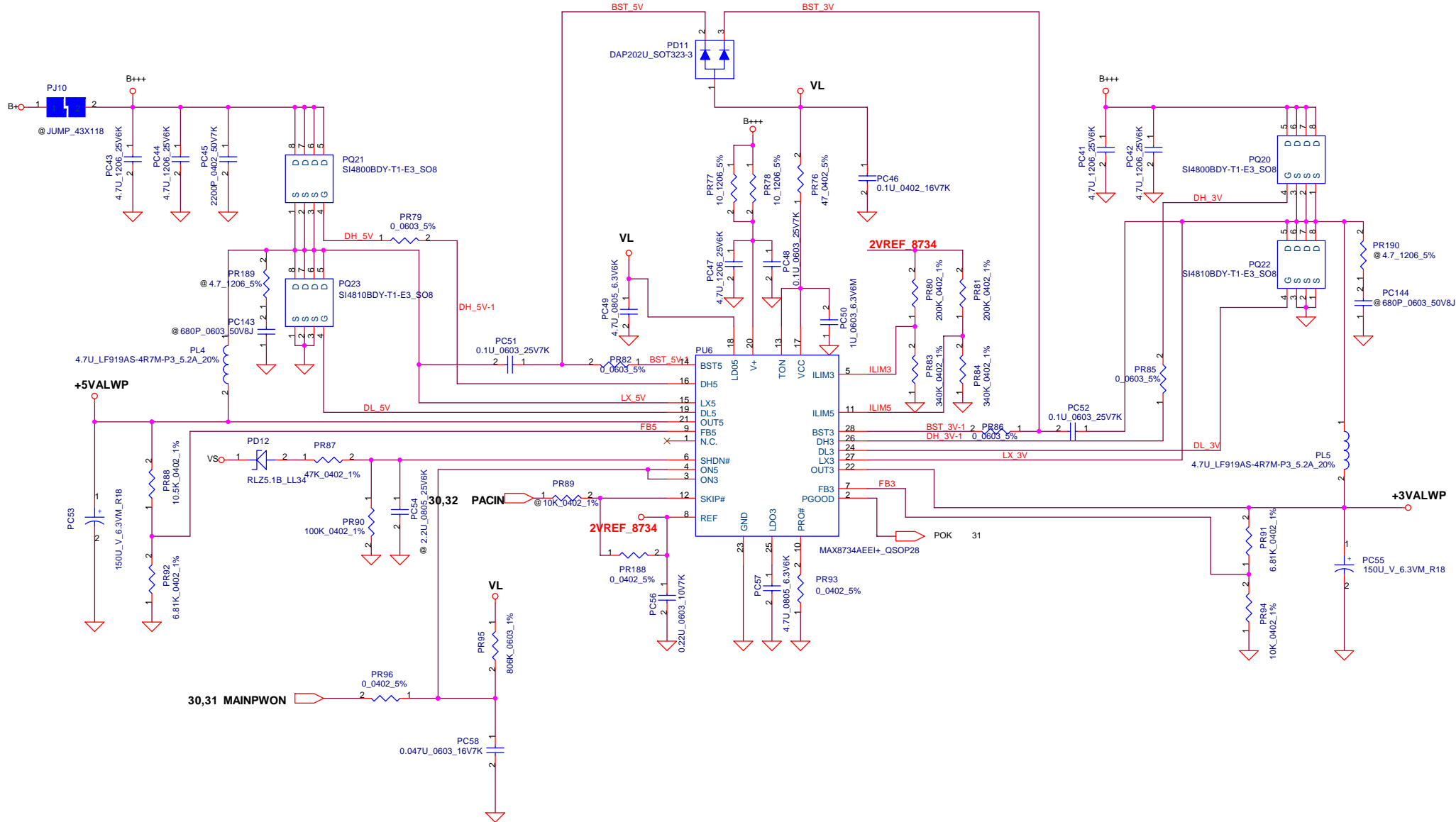
CC=0.6-3A
 CV=12.6V(6 CELLS LI-ION)

IREF=1.31*Icharge
 IREF=0.6V~3.144V

OVP voltage : LI
 3s2P : 13.5V--> BATT_OVP= 1.5V
 (BAT_OVP=0.1111 *VMB)

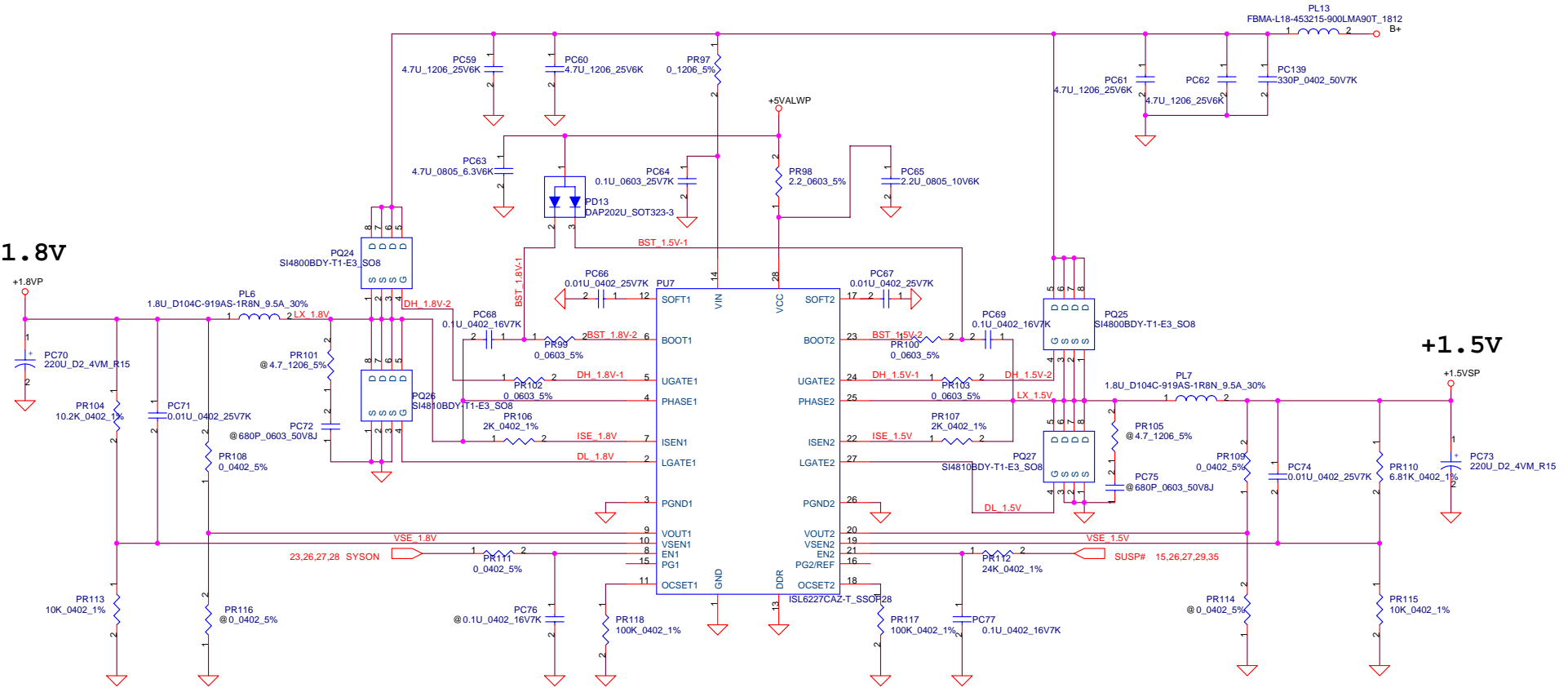
BATT Type	ALI/MH#	Charge Current	IREF
9 CELL	0V	3A	3.144V
6 CELL	3.3V	3A	3.144V

+3.3VALWP/+5VALWP



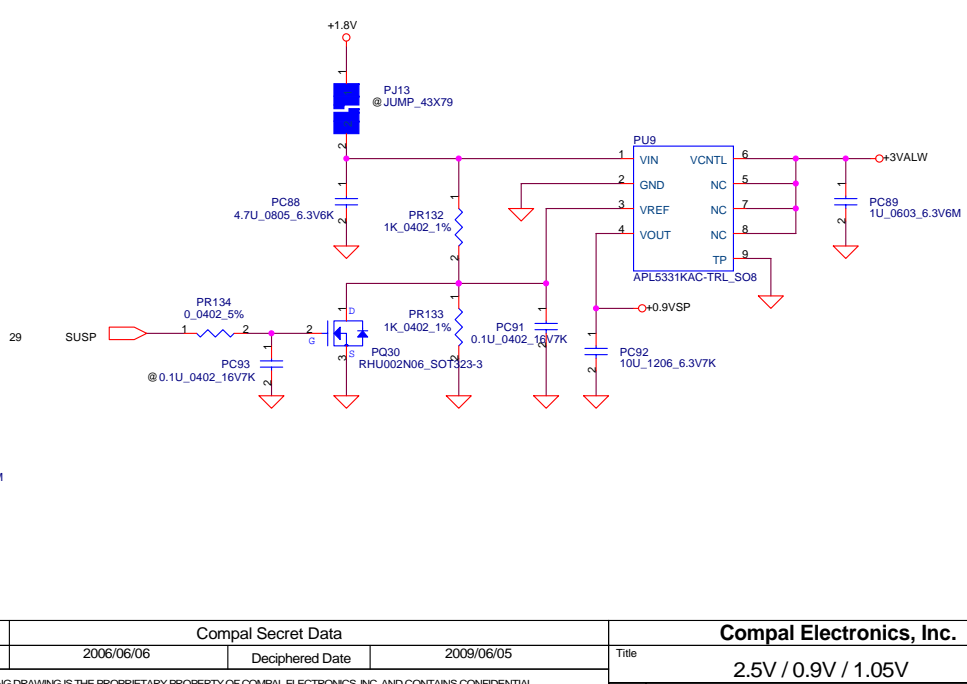
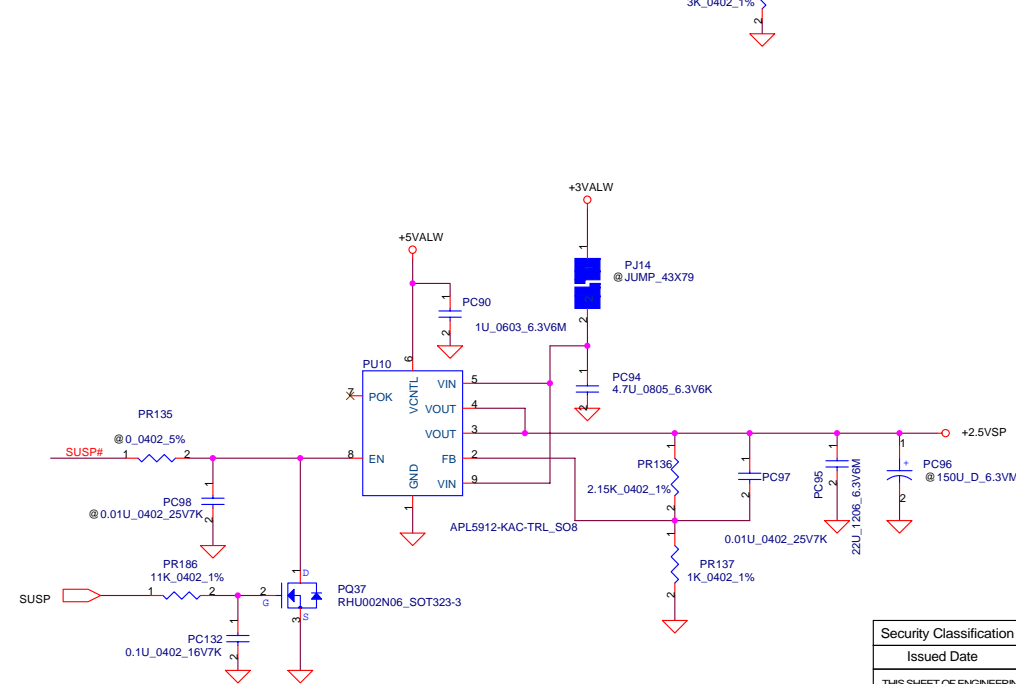
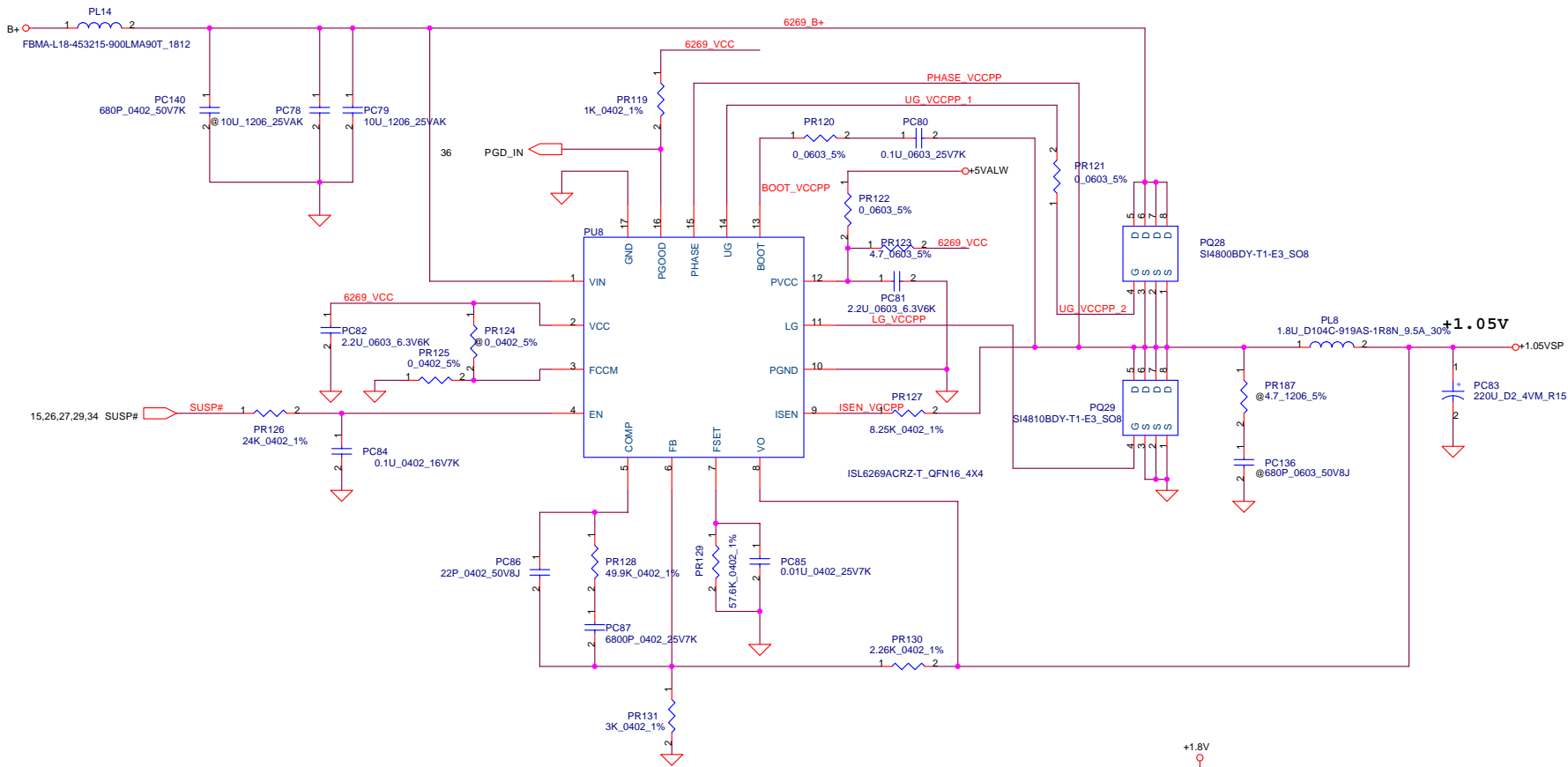
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+1.8V

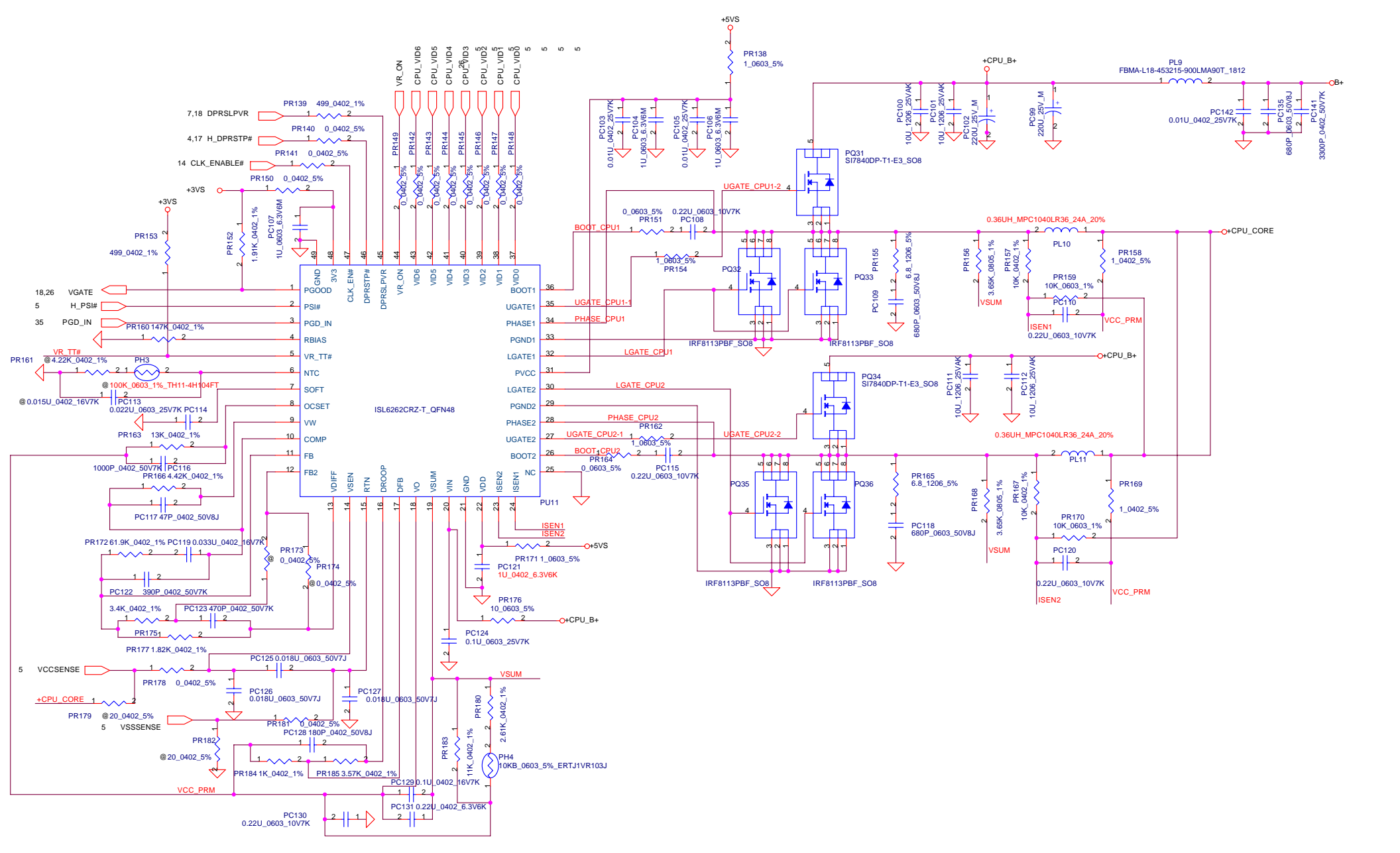


+1.5V

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HW4 Product Improvement Record (P.I.R.)

Phase: B to C		Date: 2007/01/24			Writer: Timo Teng		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
P17	Change Connector	JP24	SUYIN_06802-TK102	SUYIN_127043FB 022G345ZR_NR	Change layout footprint		
P18	Delete Component	R873 R874	100K_0402_5%	NC	All sku keep 5 in 1 and 1394 functions		
P22	Delete Component	R820	10K_0402_5%	NC	No need more than one pull-high resistor on the net		
P25	Delete Component	R195	10K_0402_5%	NC	No need more than one pull-high resistor on the net		
P26	Delete Component	Q65/Q77 R821/R822	MMBT3904/10K_0402_5%	NC	No engine start, so follow Dallas project.		
P20	Change net	R234	Connects to +3VS	Connects to +5VS	Blue LED needs to connect 5V	0.2	
P24	Modify footprint	JP14/JP15	SINGA_2SJ-S351	SINGA_2SJ-T820	For solving SMT soldering poor issue		
P25	Delete Component	U38/R503/C630	CIR/100_0805/4.7U	NC	No CIR support on spec.		
P26	Add Component	R873/2FAN_DET#	NC	10K_0402/2FAN_DET#	For separate ISRAE&ISKAE EC BIOS		
P28	Modify component	R410/R411	200_0402_5%	100_0402_5%	Emonoto-san request, the LEDs increase brigtness		
P28	Modify BOM Select	Q48/R410/R411/D47/D48	NC	SAT@	Reserve Sateiliate LED BOM select		
P29	Modify R Value	R613	820K_0402_1%	910K_0402_5%	For delaying and adjusting 1.8VS power sequence		
P22	Change Value	C89, C79, C90 C68, C74, C81	0.01uF_0402	0.1uF_0402	For solving EMI noise		

PIR (Product Improve Record)

FOR ISPD

LAN

U7
 RTL8101E
 100M@

TRANSFORMER

U34
 NS892404
 100M@

PCB

ZZZ1
 PCB ZKU LA-3711P REV0

Card BUS

U8
 8402
 8402@

SB

U2
 ICH7
 ICH7R1@

NB

U6
 945GM
 GMR3@

U6
 943GML
 GMLR3@

U6
 945GM
 GMR1@

U6
 943GML
 GMLR1@

U6
 945PM
 PMR1@

SKU ID

R349
 18K_0402_5%
 PM@

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POWER PIR LIST

page Reason for change

Modify list



Page	Reason for change	Modify list
DVT 35	Change +1.05V PWM IC	Change PU8 to ISL6269A(SA00000GU80), add PR122 (0ohm, SD013000080)
36	For EMI team request to add snubber and gate resistor Modify the CUP CORE load line and compensation	Add snuber PR155,PR165(6.8ohm_SD011680B80), PC109,PC118(680p_SE024681J80) and gate resistor PR154,PR162(1ohm_SD013100B8 Change PC103 to 0.022u(SE076223K80), PC104 to 2.2u(SE107225K80), PR185 to 4.42K(SD000004J80), PC129 to 0.1u(SE076104K80, add PC126 (0.018u_SE025183J80), delete PC105 and PC106
31	Modify the CPU OTP point from 84 degC to 87 degC for thermal team request	Change PR36 from 22K to 20K(SD034200280)
PVT 32,34, 35,36	For EMI team request to add bead to reduce board band	Add PL12,PL13,PL14(SM010020720);PC137,PC138,PC139(330p_SE074331K80);PC140(680p_SE074681K80);PC141(3300p_SE074332K80)
33	Reduce the power consumption on S3/S4	Add PR188(0_0402_5%) and unpop PR89
36	Solve the high frequency noise.	Change PC99 from 100U to 220U(SF22004M210)
Pre-MP 36	For EMI solution	Add PC142 (0.01u_0402)
36	PC99 was interfere with logic low so change to small size	Change PC99 from 220U to 100U and add PC143,PC144(68U_25V).

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