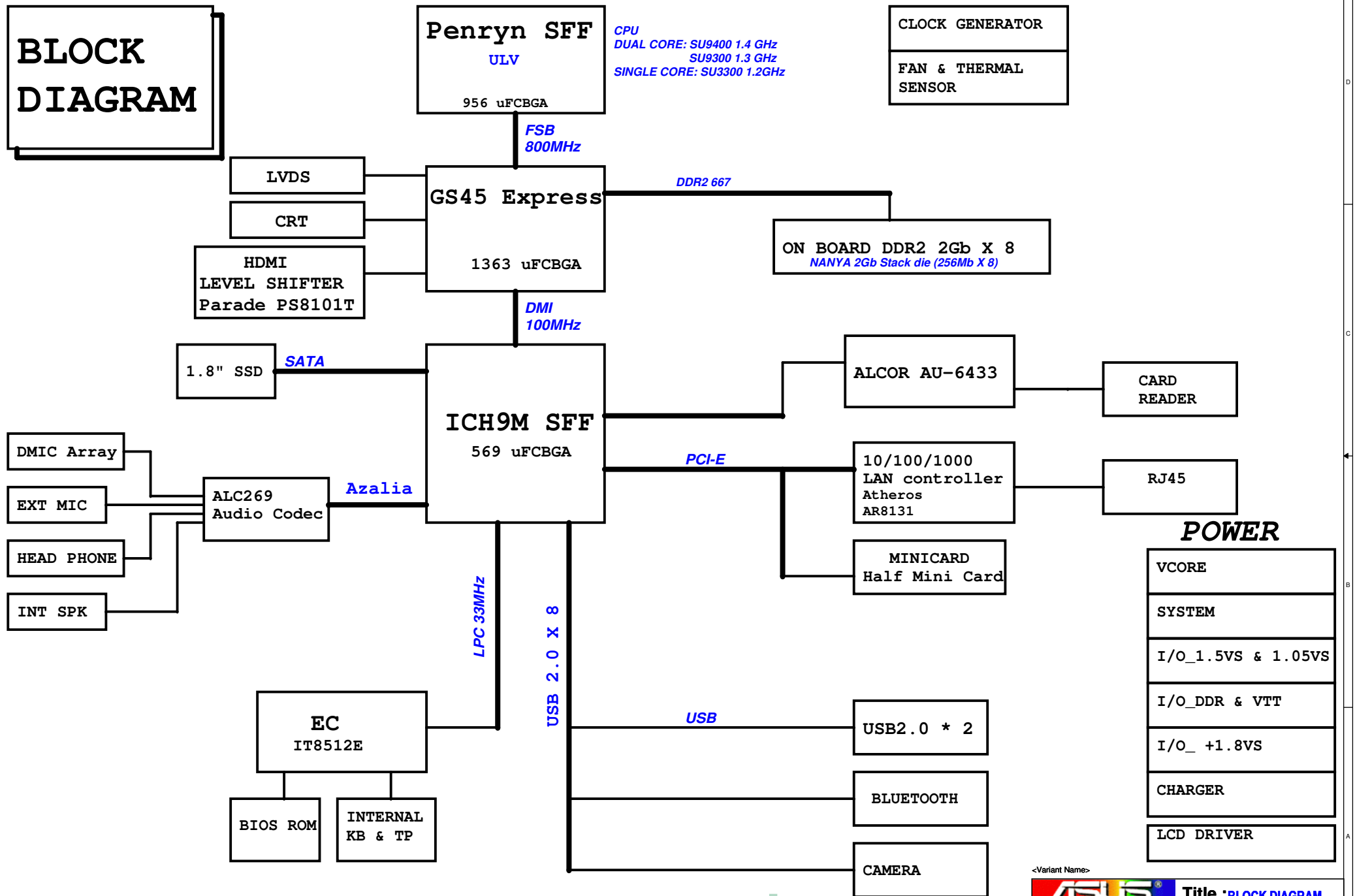
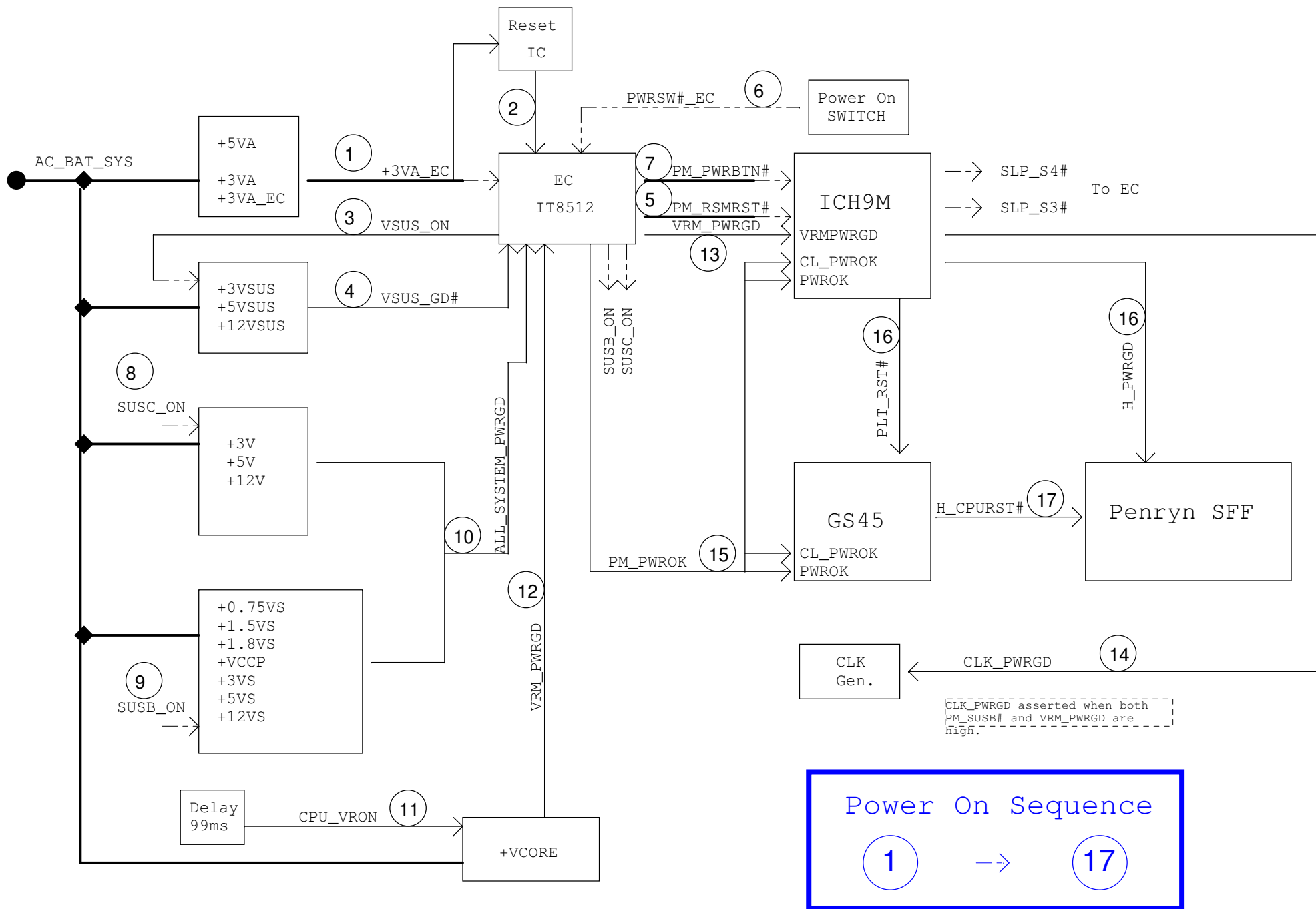
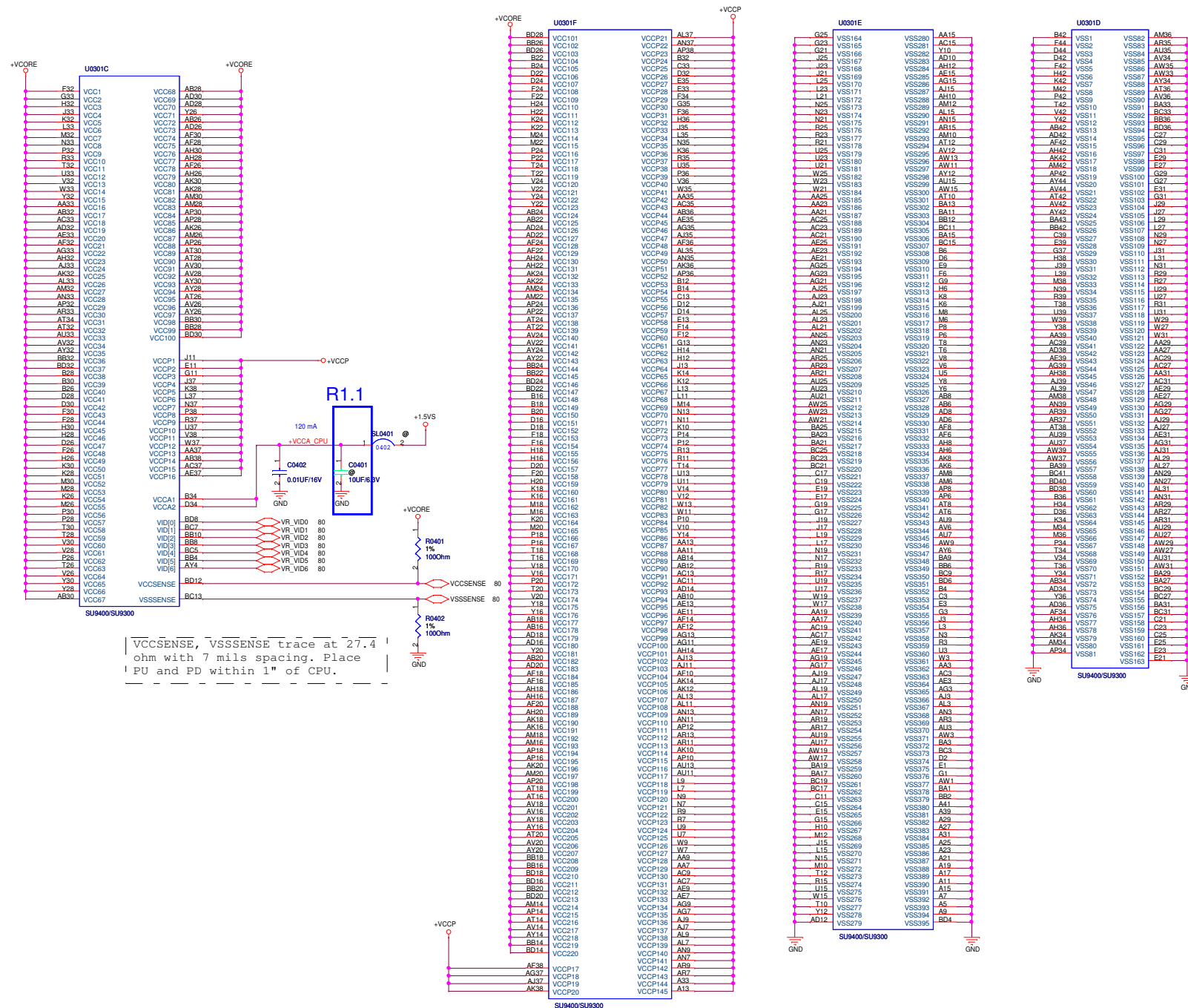
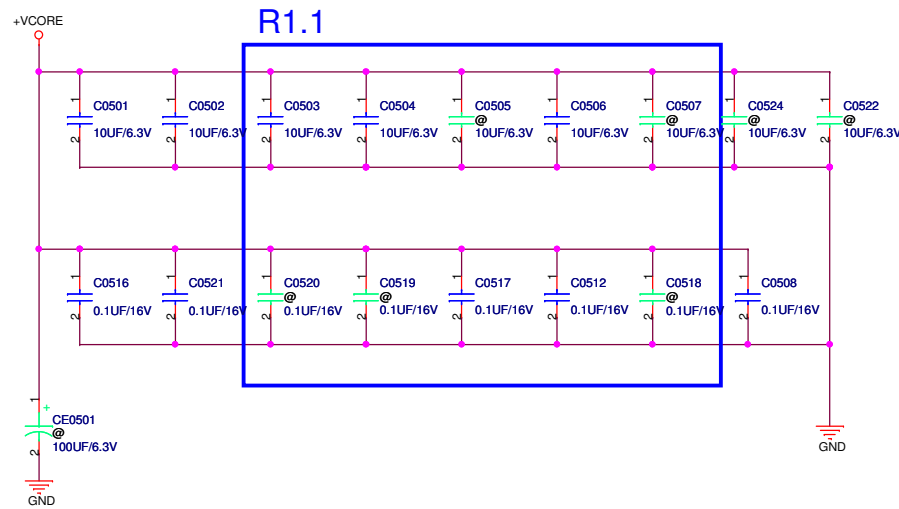


BLOCK DIAGRAM

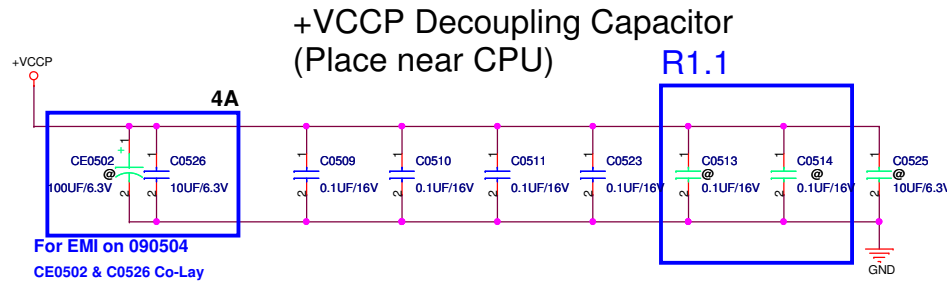








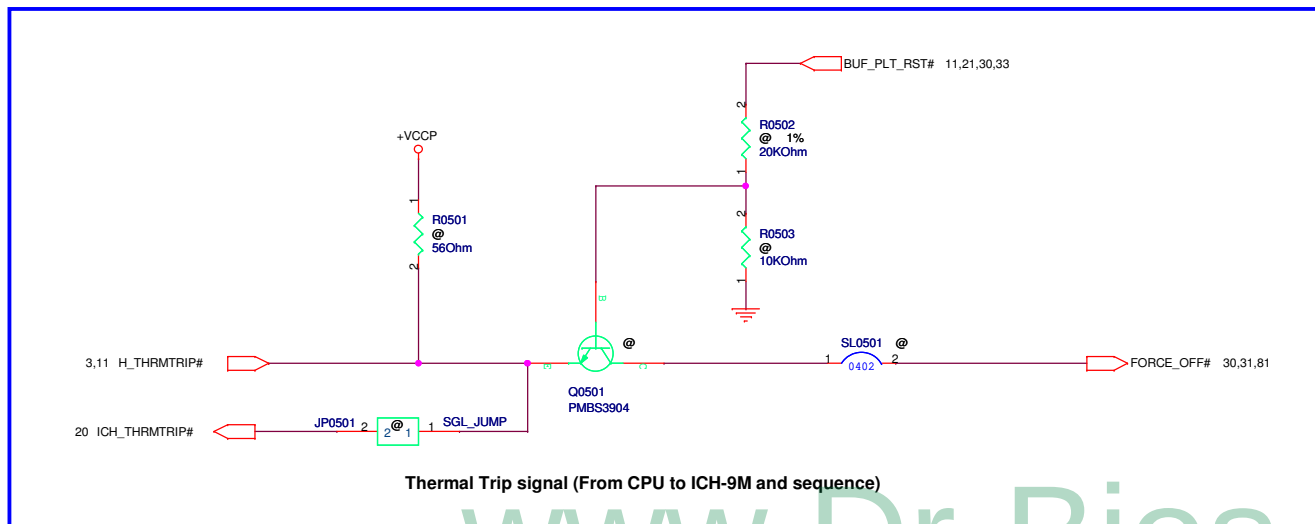
8A for Ultra Low Voltage CPU TDP 10W
DESIGN IP VCCORE
 10UF X10
 .1UF X 0



+VCCP Decoupling Capacitor
 (Place near CPU)

DESIGN IP VCCP
 100UF X 1
 10UF X 1
 .1UF X 3

R1.1 FOLLOW DESIGN IP



Thermal Trip signal (From CPU to ICH-9M and sequence)

Decoupling guide from Intel

VCCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	*12pcs
	270uF	*1pcs
VCCA	0.01uF	*1 pcs
	10uF	*1 pcs

<Variant Name>

ASUS		Title :CPU CAPACITORS	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size	Project Name	Rev	
Custom	UX30 MB	1.4	
Date: Friday, May 08, 2009	Sheet	5	of 93

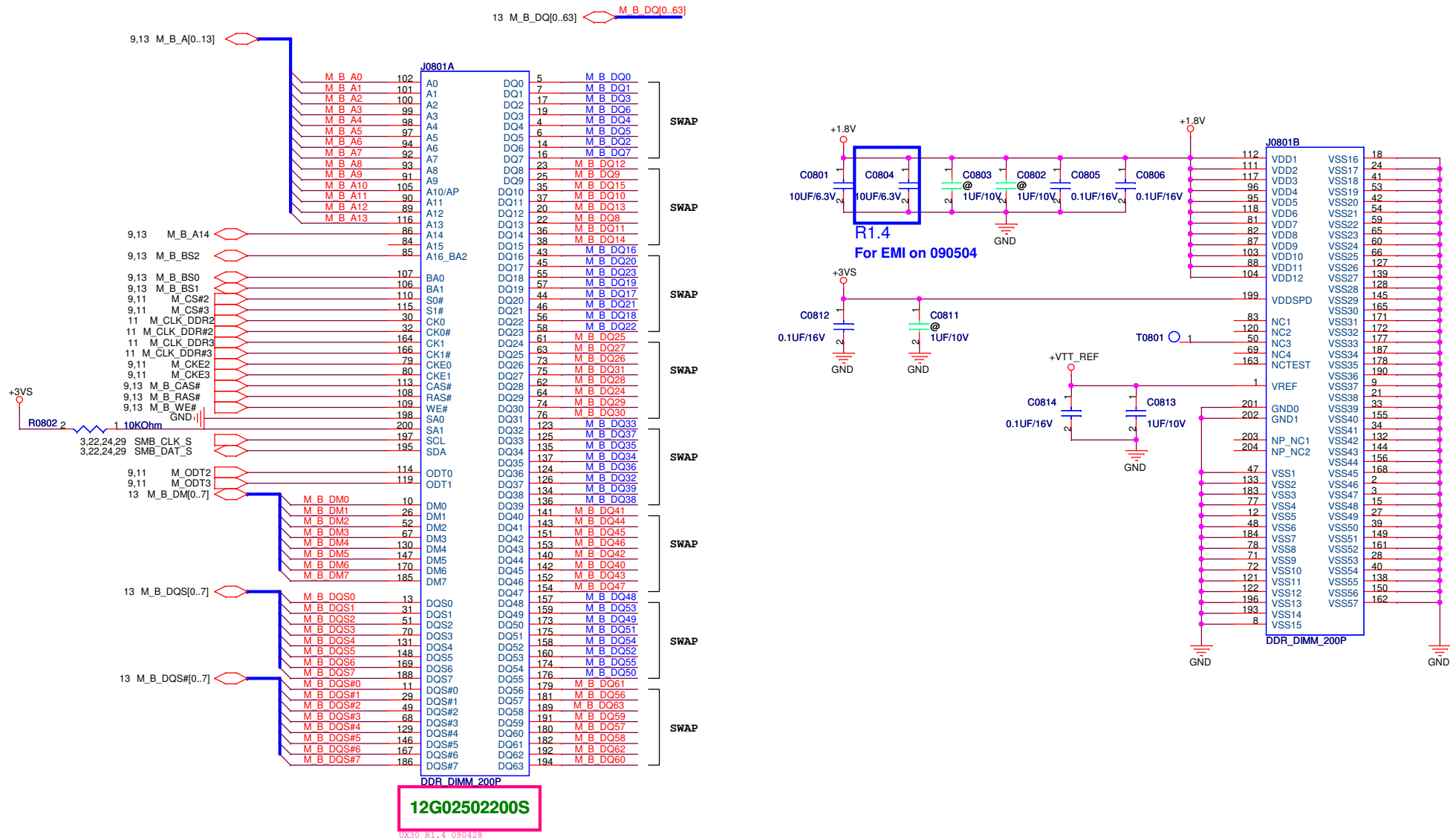


<Variant Name>

		Title :*
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>
Size Custom	Project Name UX30 MB	Rev 1.4
Date: <i>Monday, April 27, 2009</i>		Sheet 6 of 93

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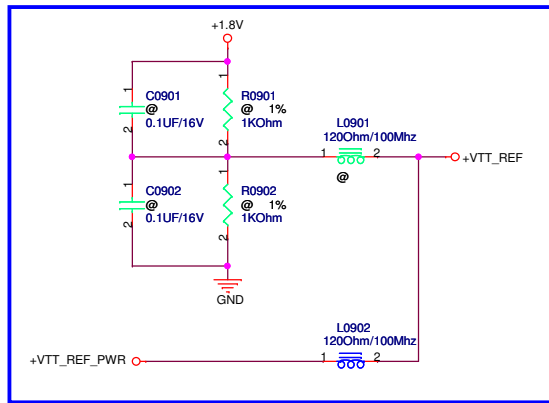
<Variant Name>		
		Title : SODIMM
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken
Size C	Project Name UX30 MB	Rev 1.4
Date: Tuesday, April 28, 2009	Sheet 7	of 93



<Variant Name>

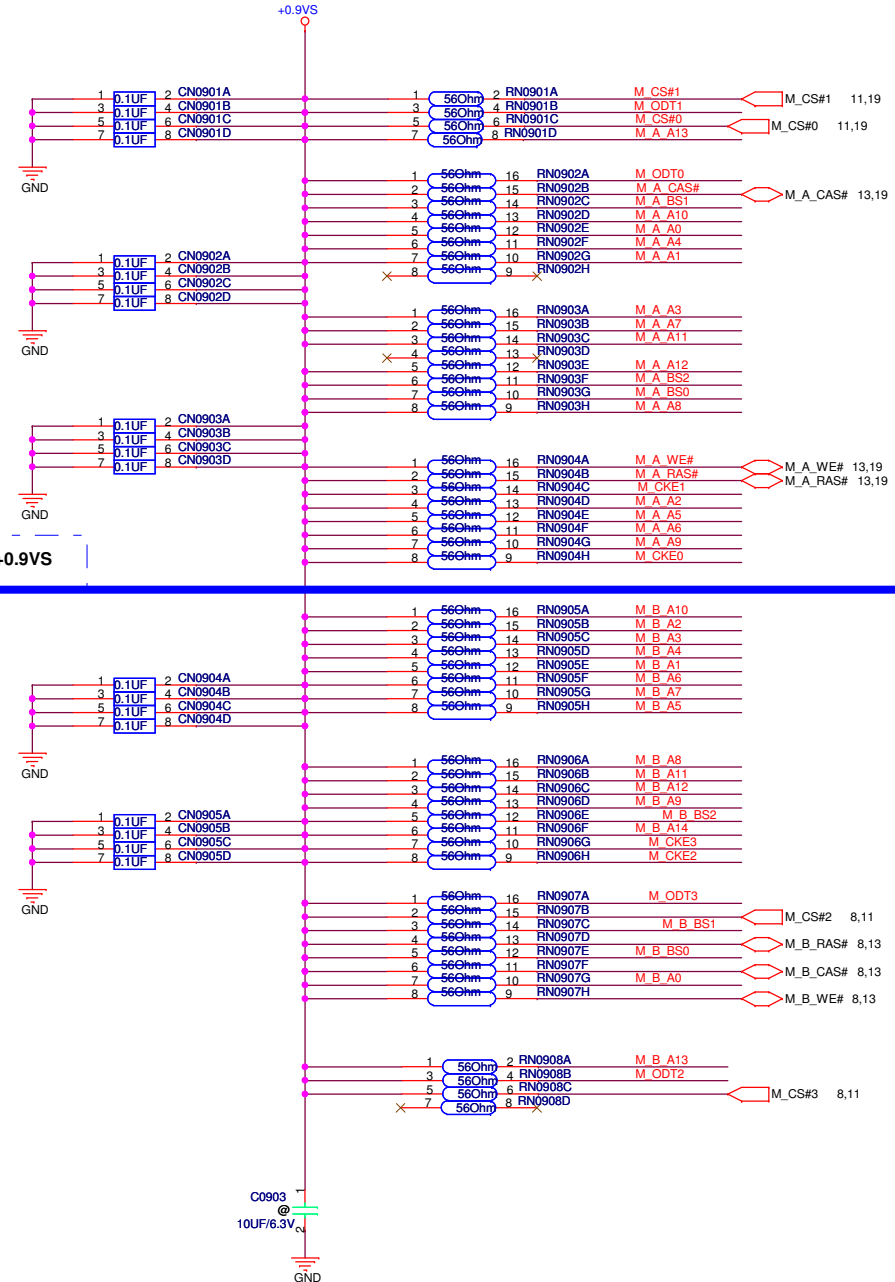
ASUS		M_DDR3 SP-DIMM CHANNEL B	
ASUSTeK COMPUTER INC		Engineer: UEI	
Size B	Project Name UX30 MB	Rev 1.4	
Date: Friday, May 08, 2009		Sheet 8 of 93	

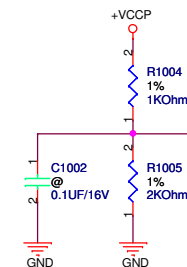
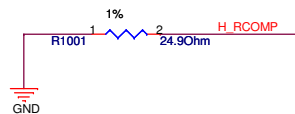
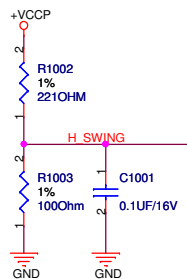
R1.1



M_A_A[0..14] 13,19
M_A_BS[0..2] 13,19
M_B_A[0..14] 8,13
M_B_BS[0..2] 8,13
M_CKE[0:3] 8,11,19
M_ODT[0:3] 8,11,19

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS





Place on Top

T1001

SL1001

0402

2 @ NB CPUSLP#

J11

H_CPURST#

H_CPUSLP#

HVREF

L17

K18

897605

H_D#0	J7	H_D#_0
H_D#1	H6	H_D#_1
H_D#2	L11	H_D#_2
H_D#3	J3	H_D#_3
H_D#4	H4	H_D#_4
H_D#5	G3	H_D#_5
H_D#6	K10	H_D#_6
H_D#7	K12	H_D#_7
H_D#8	L1	H_D#_8
H_D#9	M10	H_D#_9
H_D#10	M6	H_D#_10
H_D#11	N11	H_D#_11
H_D#12	L7	H_D#_12
H_D#13	K6	H_D#_13
H_D#14	M4	H_D#_14
H_D#15	K4	H_D#_15
H_D#16	P4	H_D#_16
H_D#17	W9	H_D#_17
H_D#18	V6	H_D#_18
H_D#19	V2	H_D#_19
H_D#20	P10	H_D#_20
H_D#21	W7	H_D#_21
H_D#22	N9	H_D#_22
H_D#23	P4	H_D#_23
H_D#24	U9	H_D#_24
H_D#25	V4	H_D#_25
H_D#26	U1	H_D#_26
H_D#27	W3	H_D#_27
H_D#28	V10	H_D#_28
H_D#29	U7	H_D#_29
H_D#30	W11	H_D#_30
H_D#31	U11	H_D#_31
H_D#32	AC11	H_D#_32
H_D#33	AC9	H_D#_33
H_D#34	Y4	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	AB6	H_D#_36
H_D#37	AB8	H_D#_37
H_D#38	AE10	H_D#_38
H_D#39	AA1	H_D#_39
H_D#40	AC3	H_D#_40
H_D#41	AC7	H_D#_41
H_D#42	AD12	H_D#_42
H_D#43	AB4	H_D#_43
H_D#44	Y6	H_D#_44
H_D#45	AD10	H_D#_45
H_D#46	AA11	H_D#_46
H_D#47	AB2	H_D#_47
H_D#48	AD4	H_D#_48
H_D#49	AE7	H_D#_49
H_D#50	AD2	H_D#_50
H_D#51	AD6	H_D#_51
H_D#52	AE3	H_D#_52
H_D#53	AG9	H_D#_53
H_D#54	AG7	H_D#_54
H_D#55	AE11	H_D#_55
H_D#56	AK6	H_D#_56
H_D#57	AF6	H_D#_57
H_D#58	AJ9	H_D#_58
H_D#59	AK6	H_D#_59
H_D#60	AE12	H_D#_60
H_D#61	AH4	H_D#_61
H_D#62	AJ7	H_D#_62
H_D#63	AE9	H_D#_63

HOST

H_SWING B6

H_RCOMP D4

H_CPURST# J11

H_CPUSLP# G9

HVREF L17

H_AVREF K18

897605

H_A#_3	L15	H_A#3
H_A#_4	B14	H_A#4
H_A#_5	C15	H_A#5
H_A#_6	D12	H_A#6
H_A#_7	E14	H_A#7
H_A#_8	G17	H_A#8
H_A#_9	B12	H_A#9
H_A#_10	J15	H_A#10
H_A#_11	D16	H_A#11
H_A#_12	C17	H_A#12
H_A#_13	D14	H_A#13
H_A#_14	K16	H_A#14
H_A#_15	F16	H_A#15
H_A#_16	B16	H_A#16
H_A#_17	C21	H_A#17
H_A#_18	D18	H_A#18
H_A#_19	J19	H_A#19
H_A#_20	B21	H_A#20
H_A#_21	D22	H_A#21
H_A#_22	G19	H_A#22
H_A#_23	J17	H_A#23
H_A#_24	L21	H_A#24
H_A#_25	L19	H_A#25
H_A#_26	C21	H_A#26
H_A#_27	D20	H_A#27
H_A#_28	K22	H_A#28
H_A#_29	F18	H_A#29
H_A#_30	K20	H_A#30
H_A#_31	F20	H_A#31
H_A#_32	F22	H_A#32
H_A#_33	B20	H_A#33
H_A#_34	A19	H_A#34
H_A#_35	A19	H_A#35

H_ADS#	E10	H_ADS#	3
H_ADSTB#_0	A15	H_ADSTB#0	3
H_ADSTB#_1	C19	H_ADSTB#1	3
H_BNR#	C9	H_BNR#	3
H_BPRI#	B8	H_BPRI#	3
H_BREQ#	C11	H_BREQ#	3
H_DEFER#	E5	H_DEFER#	3
H_DBSY#	D6	H_DBSY#	3
HPLL_CLK	AH10	H_DBSY#	3
HPLL_CLK#	AJ11	H_DBSY#	3
H_DPWR#	G11	H_DPWR#	3
H_DRDY#	H2	H_DRDY#	3
H_HIT#	C7	H_HIT#	3
H_HITM#	E8	H_HITM#	3
H_LOCK#	A11	H_LOCK#	3
H_TRDY#	D8	H_TRDY#	3

H_DINV#_0	L9	H_DINV#0	3
H_DINV#_1	N7	H_DINV#1	3
H_DINV#_2	AA7	H_DINV#2	3
H_DINV#_3	AG3	H_DINV#3	3

H_DSTBN#_0	K2	H_DSTBN#0	3
H_DSTBN#_1	N3	H_DSTBN#1	3
H_DSTBN#_2	AA3	H_DSTBN#2	3
H_DSTBN#_3	AF4	H_DSTBN#3	3

H_DSTBP#_0	L3	H_DSTBP#0	3
H_DSTBP#_1	M2	H_DSTBP#1	3
H_DSTBP#_2	Y2	H_DSTBP#2	3
H_DSTBP#_3	AF2	H_DSTBP#3	3

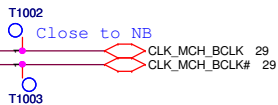
H_REQ#_0	J13	H_REQ#0	3
H_REQ#_1	L13	H_REQ#1	3
H_REQ#_2	C13	H_REQ#2	3
H_REQ#_3	G13	H_REQ#3	3
H_REQ#_4	G15	H_REQ#4	3

H_RS#_0	F4	H_RS#0	3
H_RS#_1	F2	H_RS#1	3
H_RS#_2	G7	H_RS#2	3

3 H_A#[35:3] H_A#[35:3]

3 H_REQ#[4:0] H_REQ#[4:0]

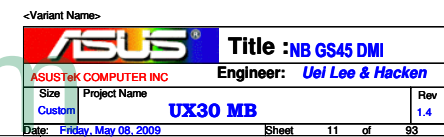
3 H_D#[63:0] H_D#[63:0]

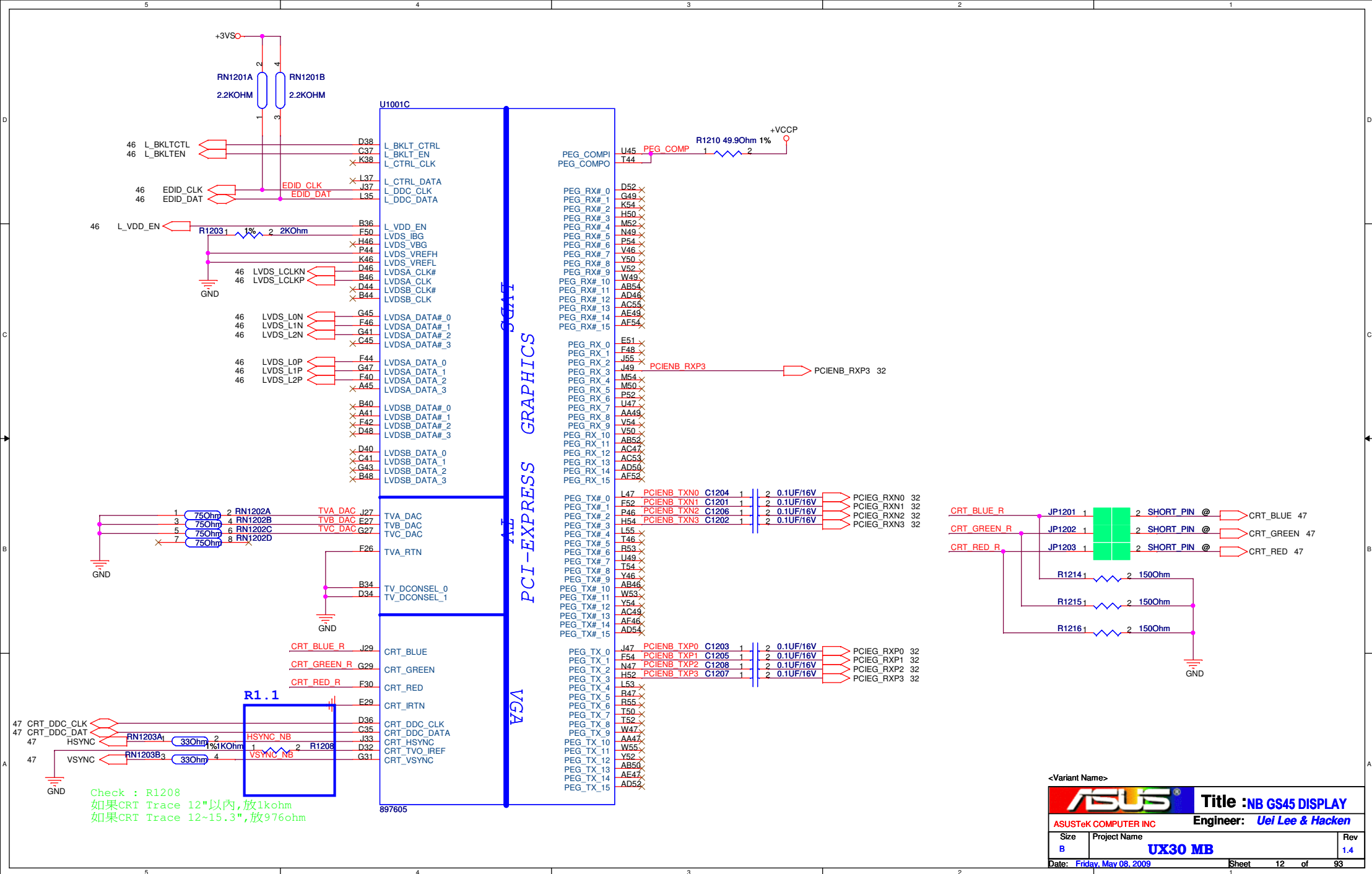


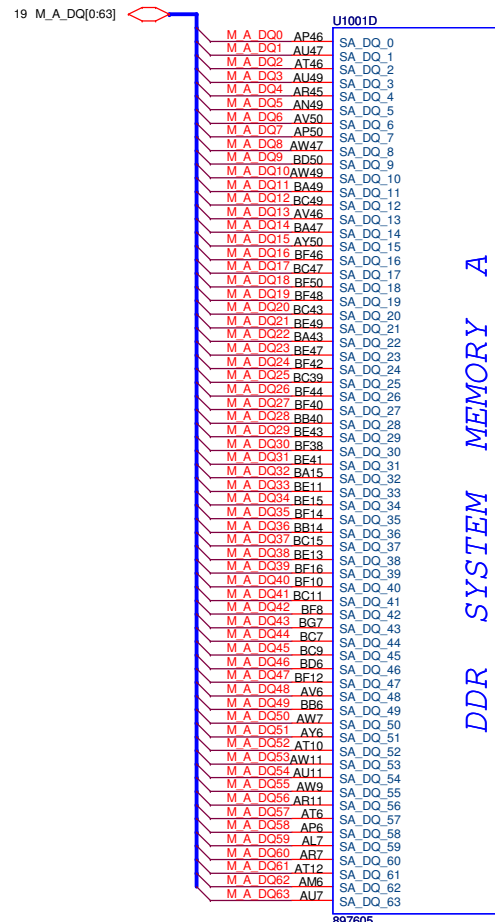
<Variant Name>

ASUS		Title :NB GS45 HOST	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size	Project Name	UX30 MB	Rev 1.4
Custom	Date: Friday, May 08, 2009	Sheet 10 of 93	

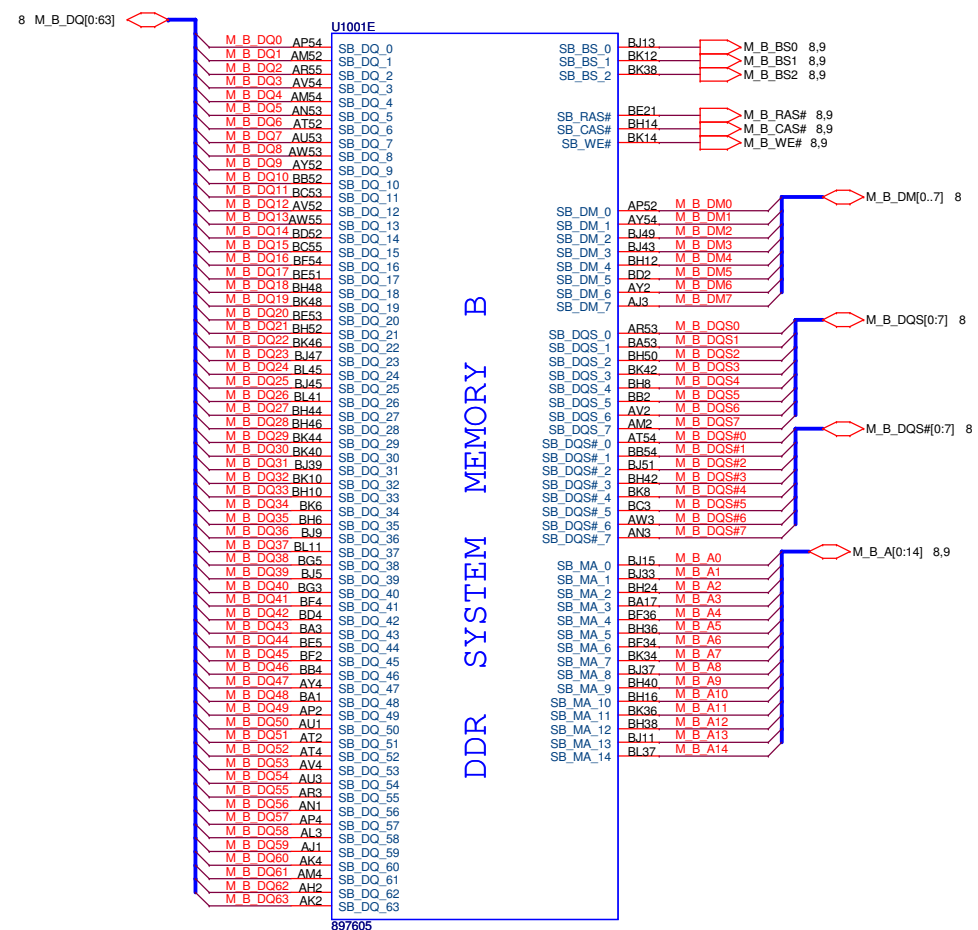
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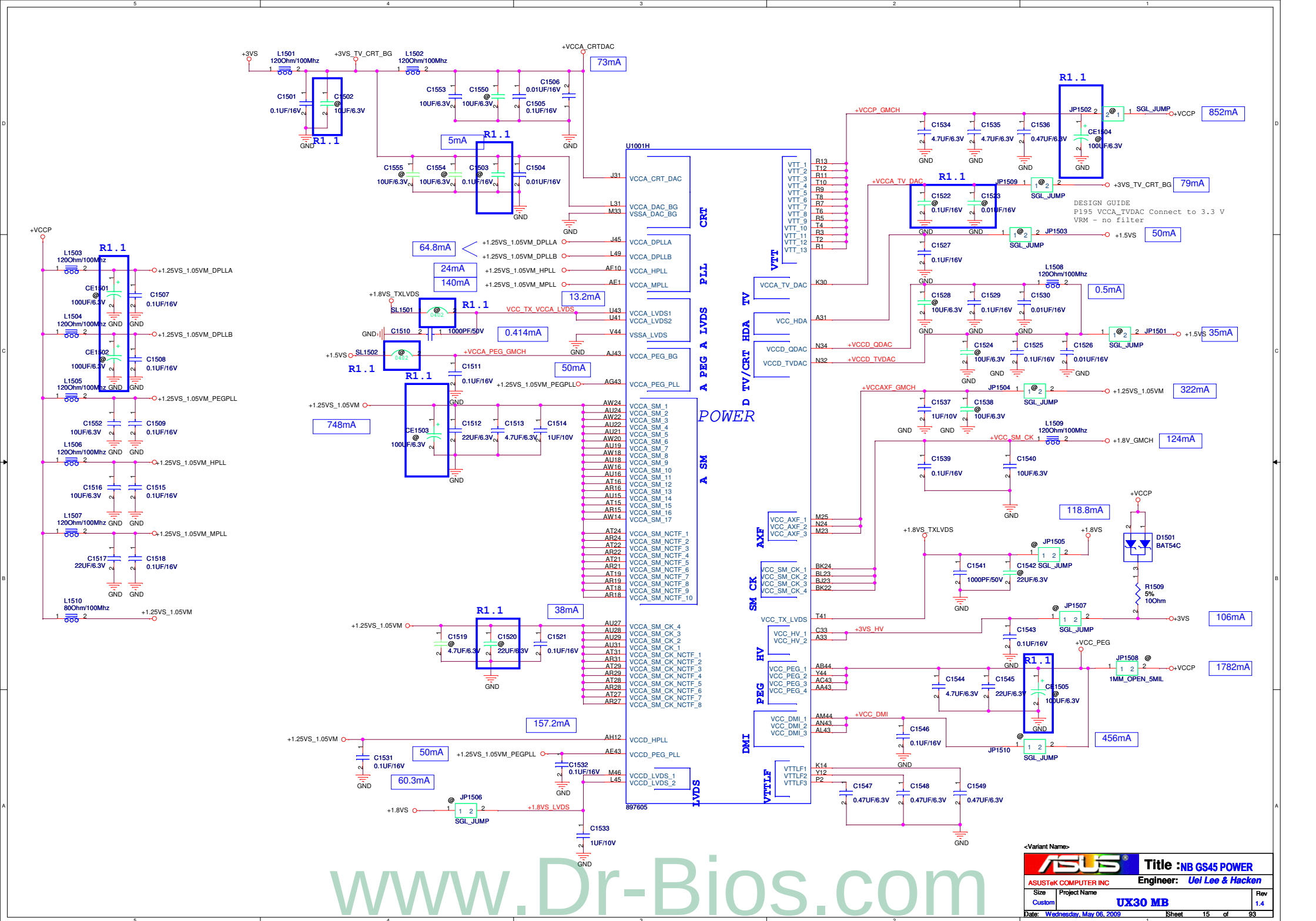


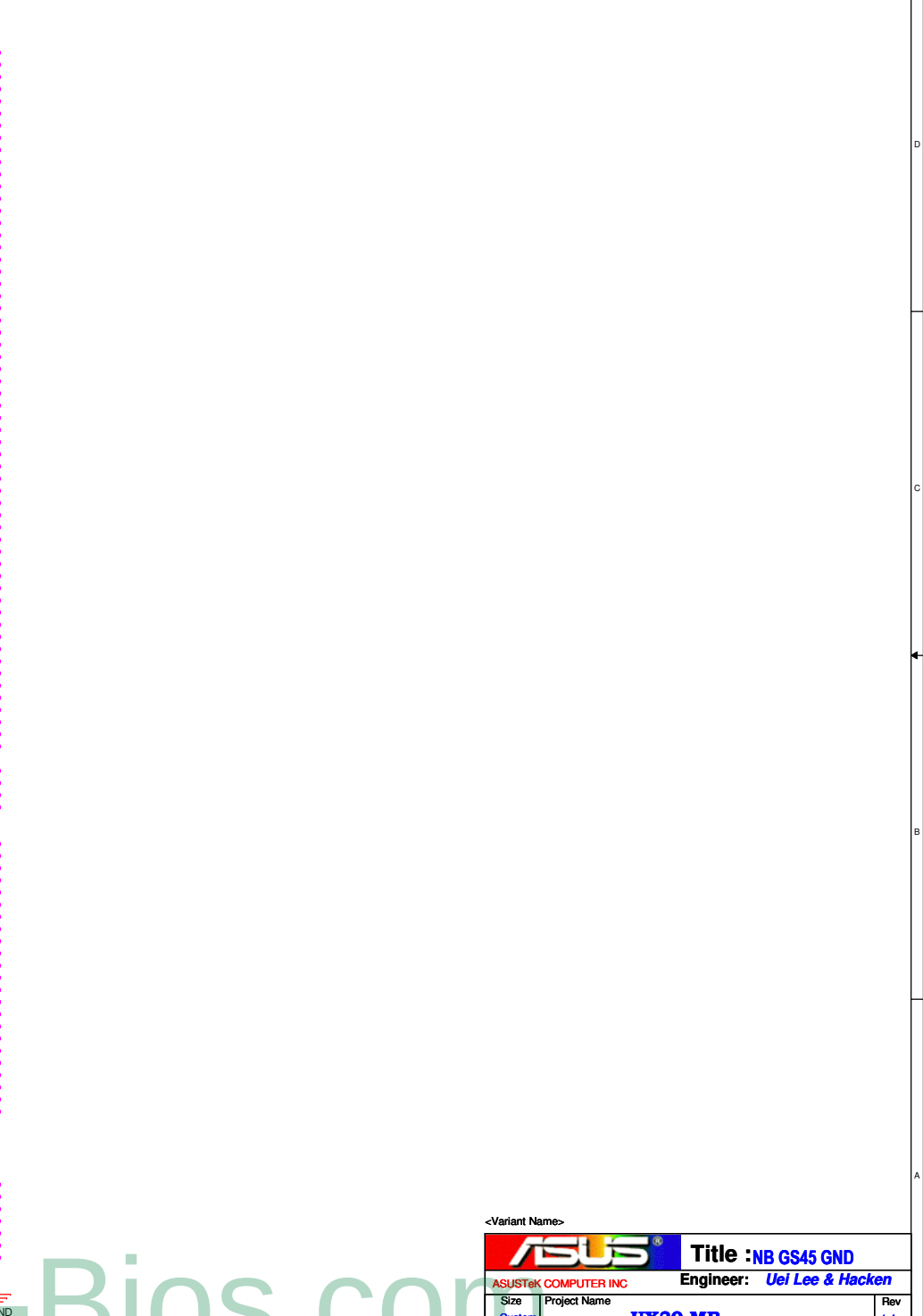
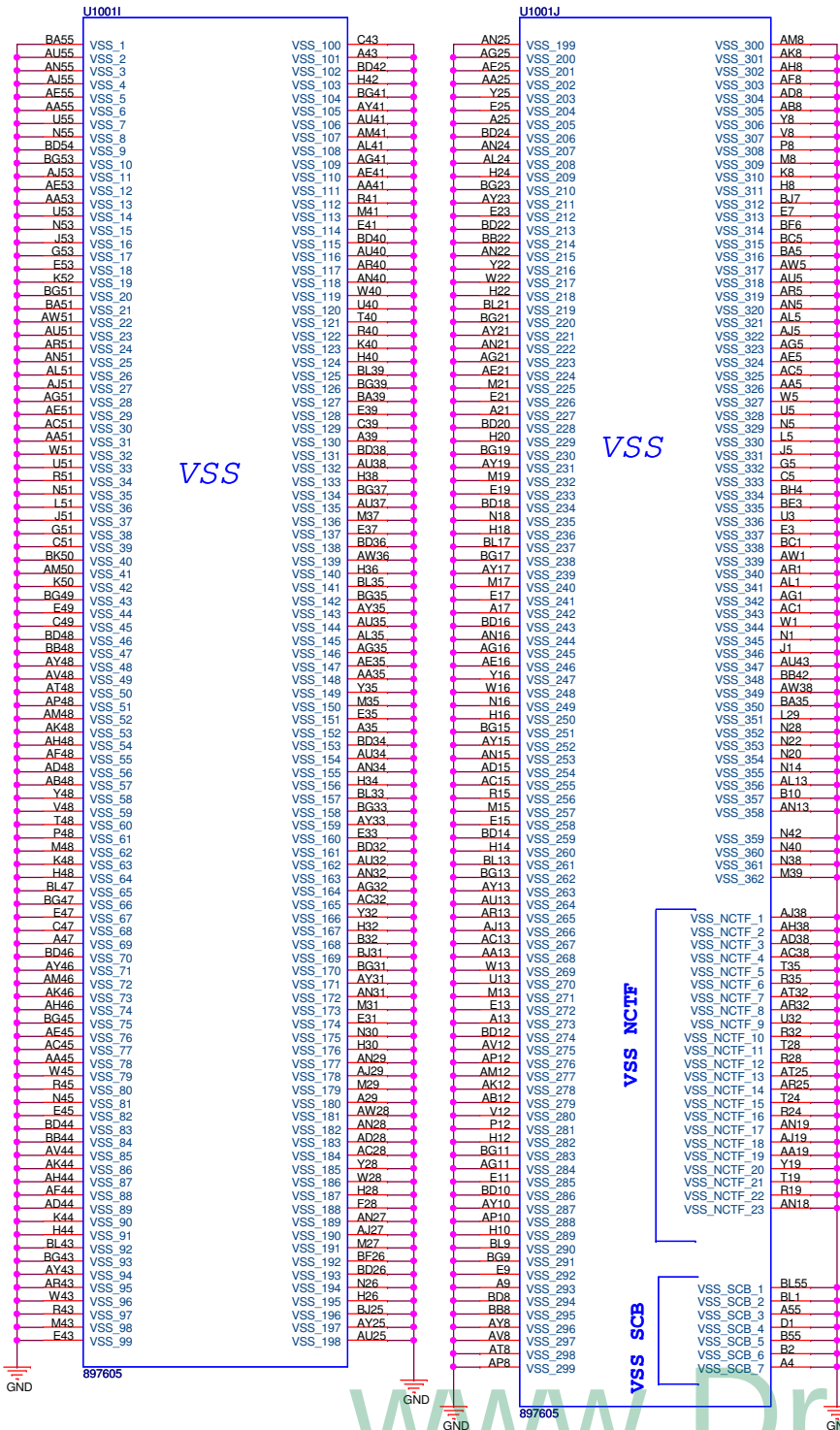
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B





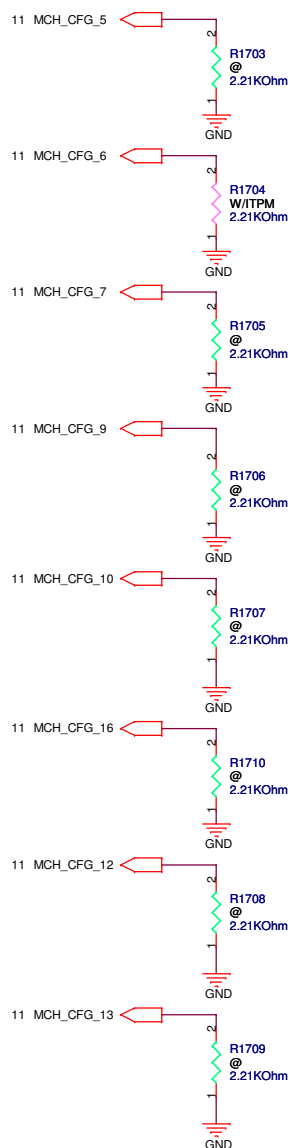


<Variant Name>

ASUS Title :NB GS45 GND

ASUSTeK COMPUTER INC Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	1.4
Date: Monday, April 27, 2009	Sheet 16 of 93	



CFG5 : DMI STRAP

H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)

H = ITPM Disable (Default)
L = ITPM enable (Can disable by SW)

CFG7 : Intel ME Crypto Strap

H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse

H = Normal (Default)
L = Lanes Reverse

CFG10 : PCIE Loopback

H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT

H = Enable (Default)
L = Disable

CFG12 : ALL-Z Mode

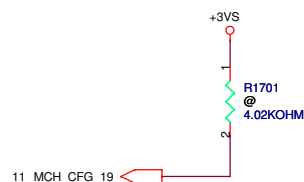
H = Disable (Default)
L = Enable

CFG13 : XOR Mode

H = Disable (Default)
L = Enable

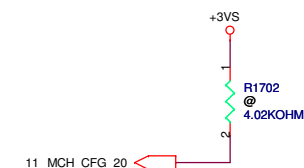
CFG [13:12] : XOR/ALL-Z

00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)



CFG19 : DMI Lane Reversal

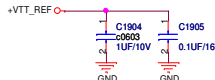
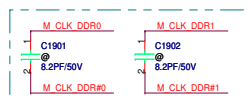
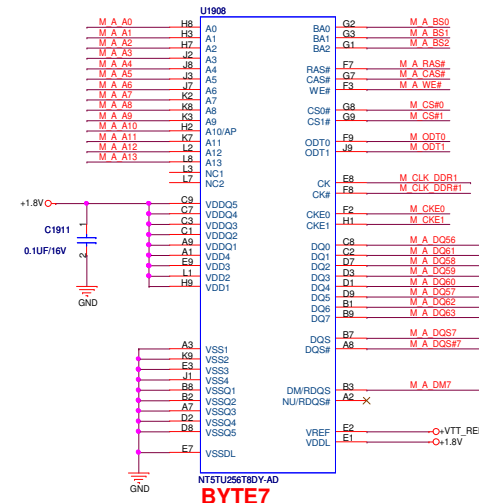
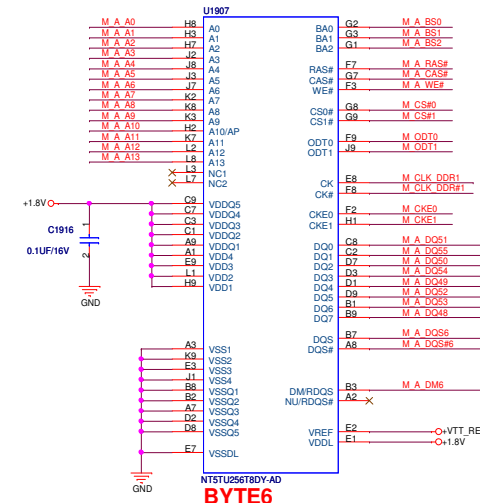
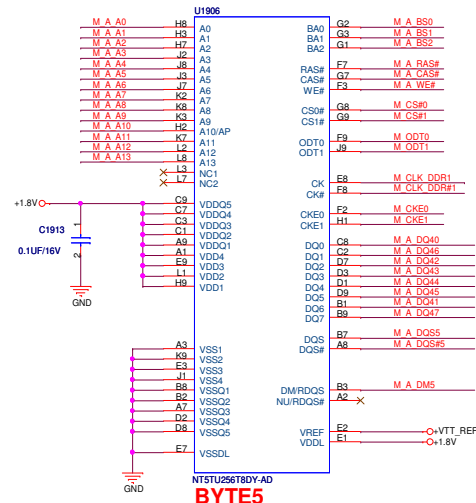
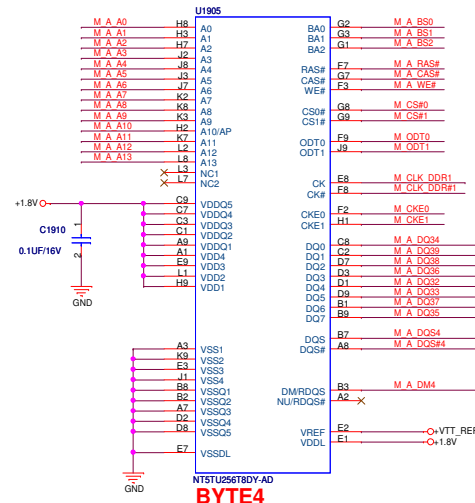
H = DMI Lane Reversal
L = Normal (Default)



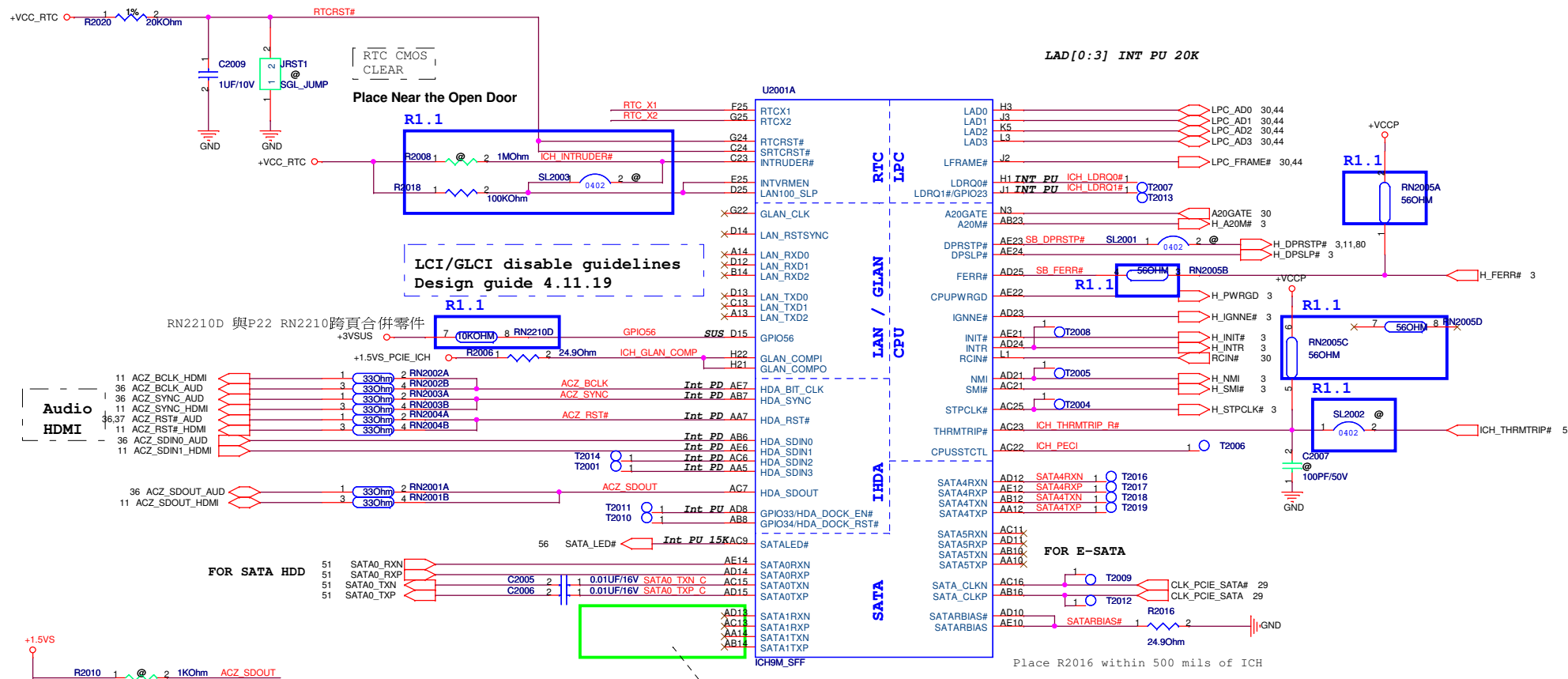
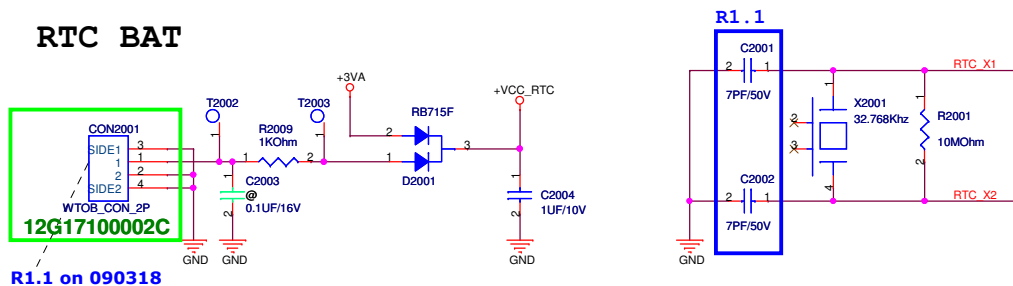
CFG20 : SDVO/PCIE CONCURRENT MODE

L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>



RTC BAT



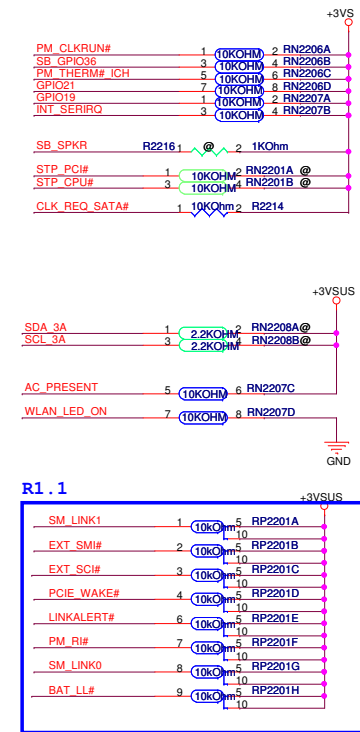
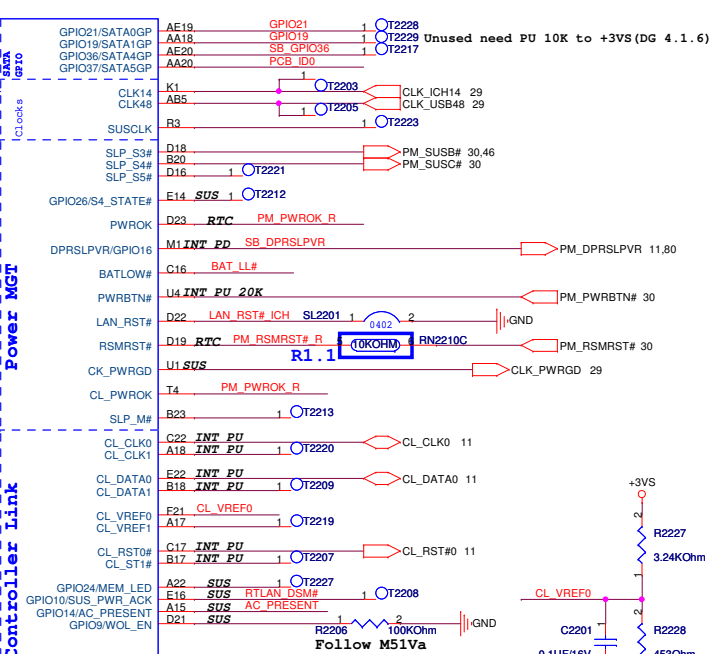
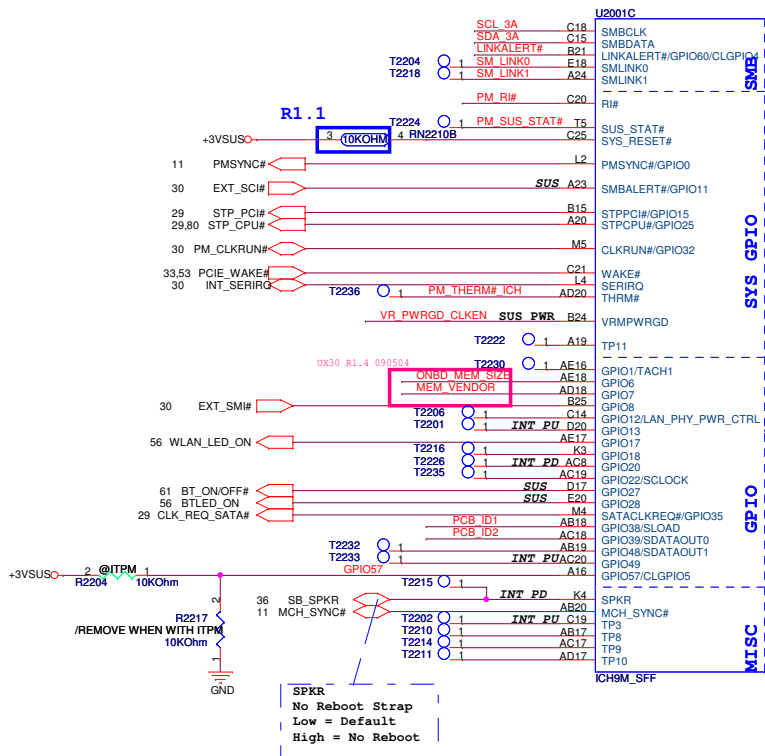
[ICH TP3, ACZ SDOUT] : XOR Chain Entrance Strap

00 = Reserved
01 = Enter XOR Chain
10 = Normal Operation (Default)
11 = Set PCIe Port Config Bit 1

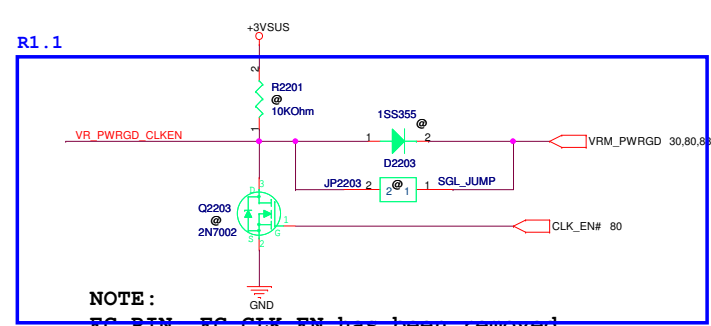
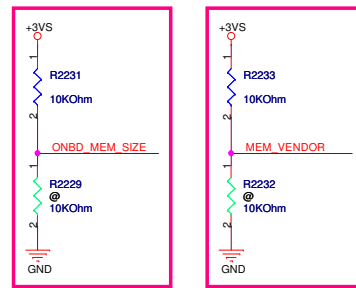
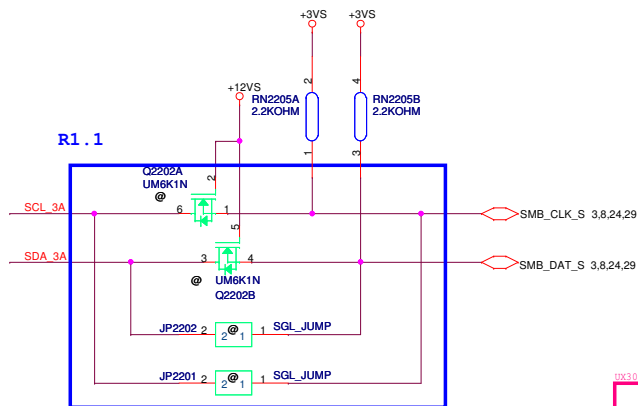
GPIO33:Flash Descriptor Security Override
High = Enable (Default)
Low = Overridden

R1.1 on 090401

Place R2016 within 500 mils of ICH

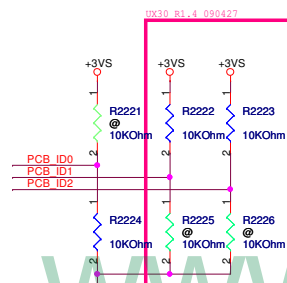


CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max



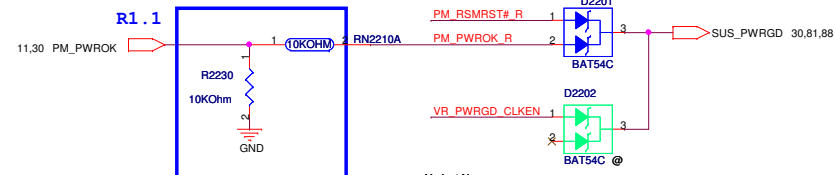
NOTE:
EC PIN. EC CLK EN has been removed.
Resolve CMOS DATA loss issue.

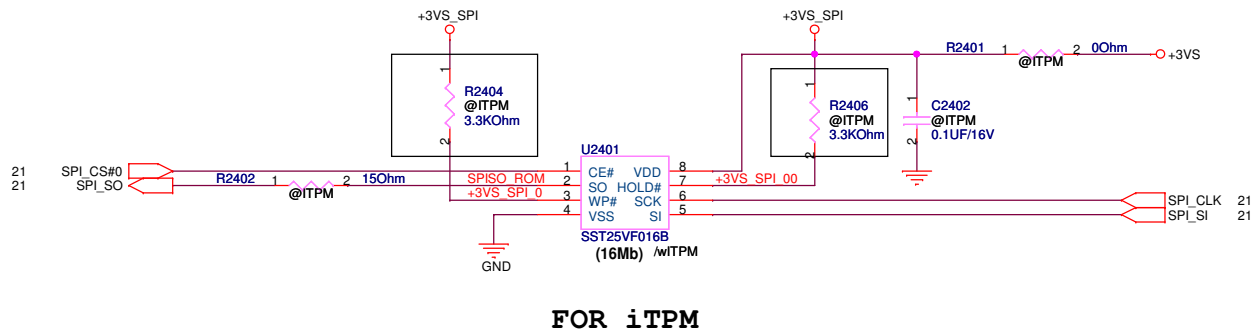
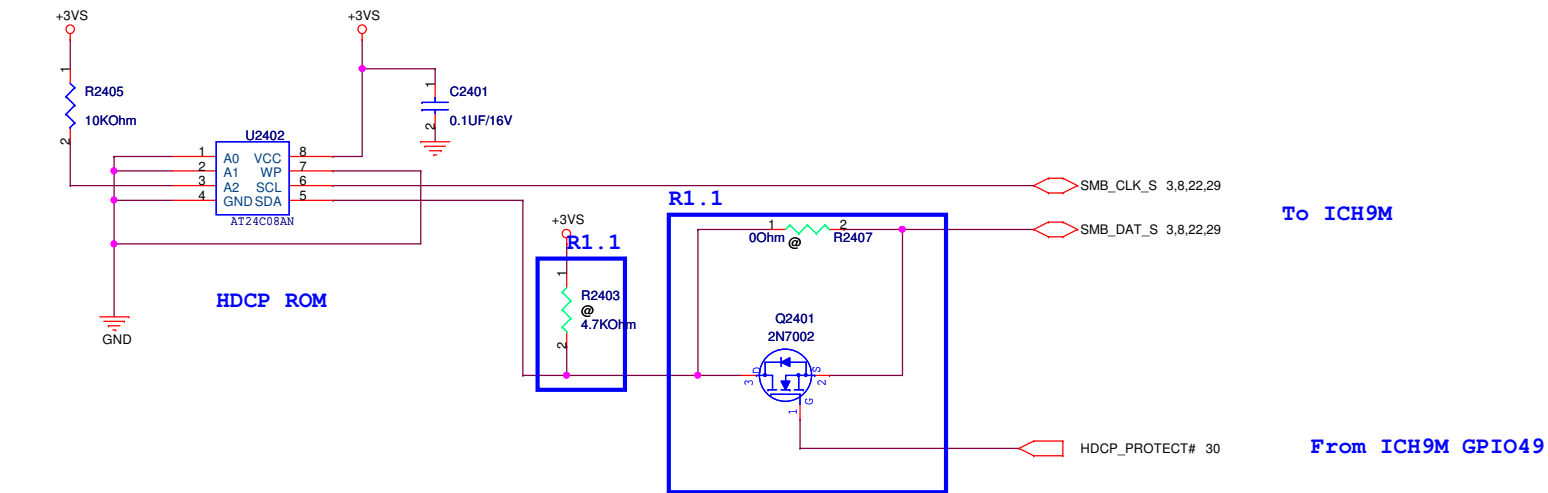
PCB ID	GPIO37	GPIO38	GPIO39
MBR1.0	0	0	0
MBR1.1	0	0	1
MBR1.3	0	1	0
MBR1.4	0	1	1
MBR2.0	1	0	0



UX30 R1.4 090504	
GPIO 6 Memory Size	
1	1GB
0	2GB

UX30 R1.4 090504	
GPIO 7 Memory Vendor	
1	SAMSUNG
0	NANYA





<Variant Name>		SB-ICH9M SPI ROM & HDCP	
		Title :	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009		Sheet	24 of 93

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

A

Project Name	
--------------	--

UX30 MB

Rev

1.4

Date: Monday, April 27, 2009

Sheet

25

of

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<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

Project Name

Rev

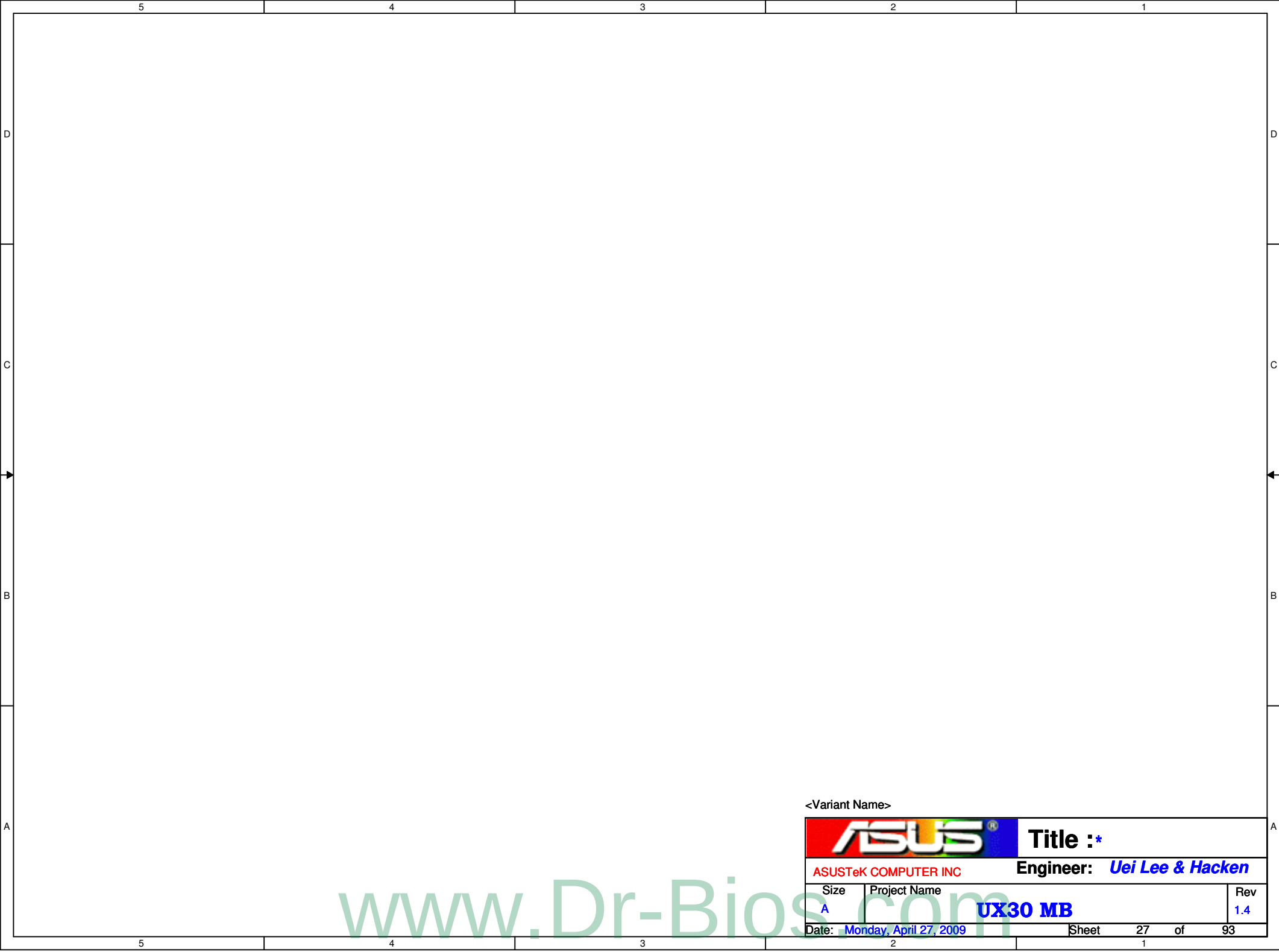
A

UX30 MB

1.4

Date: Monday, April 27, 2009

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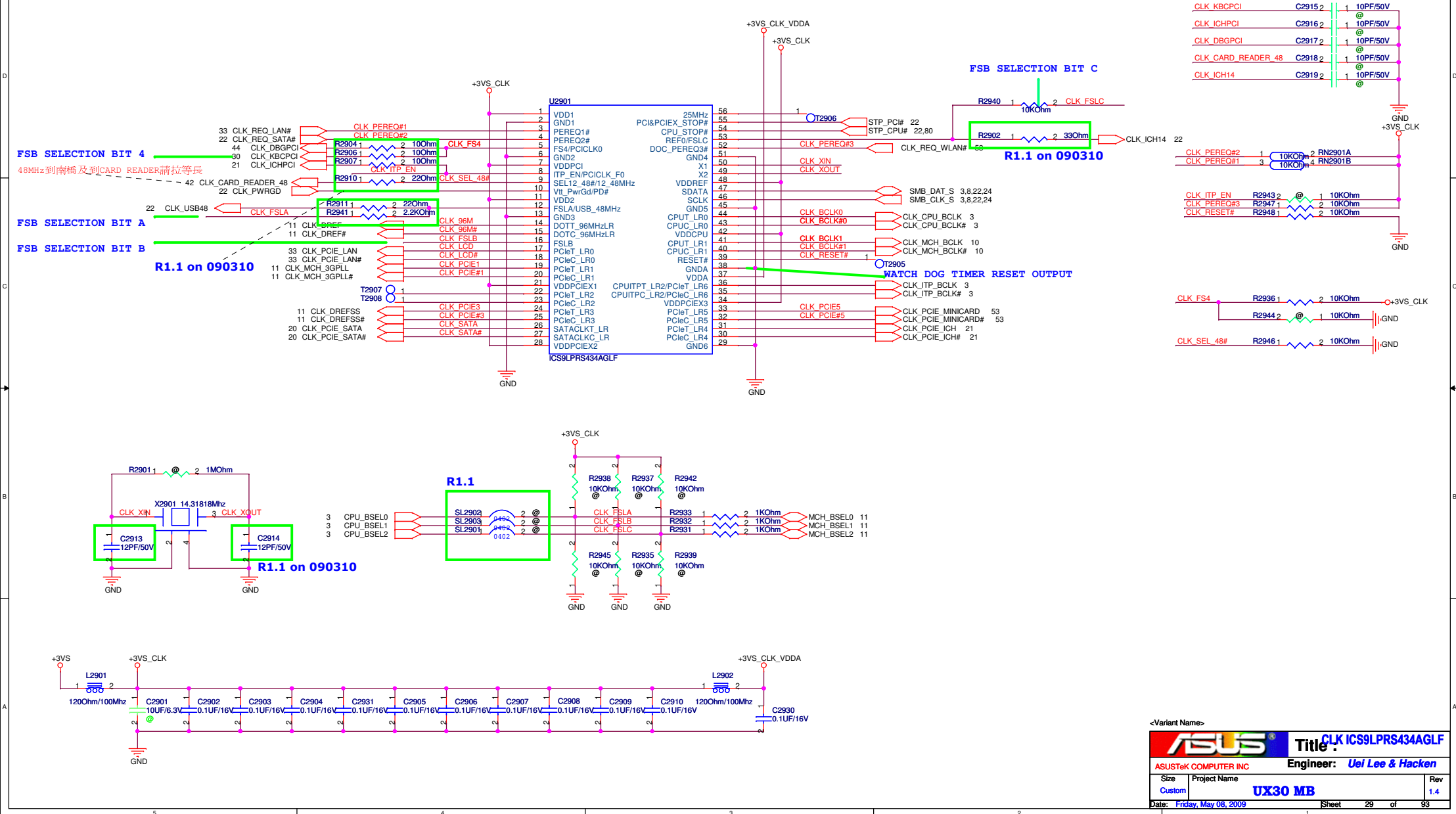


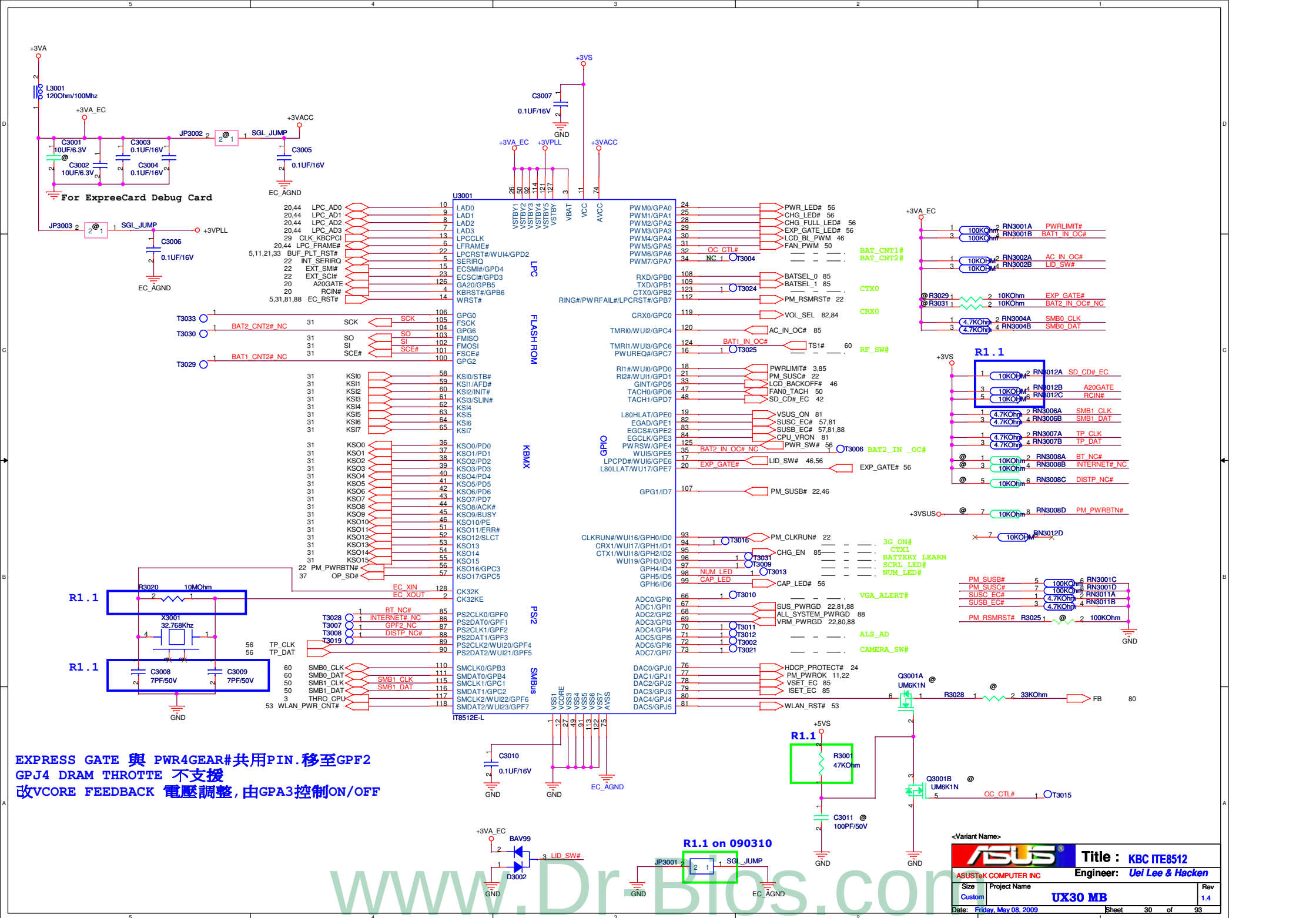
<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
<i>A</i>	UX30 MB		<i>1.4</i>
Date: <i>Monday, April 27, 2009</i>		Sheet	27 of 93

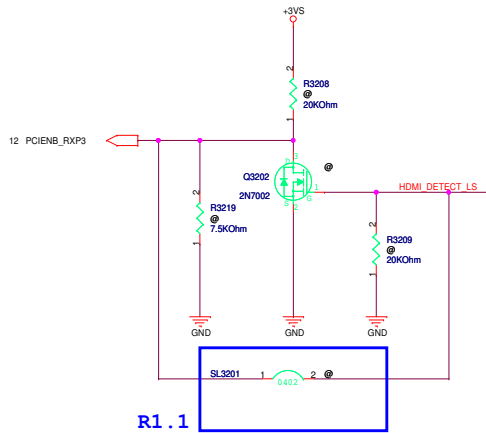
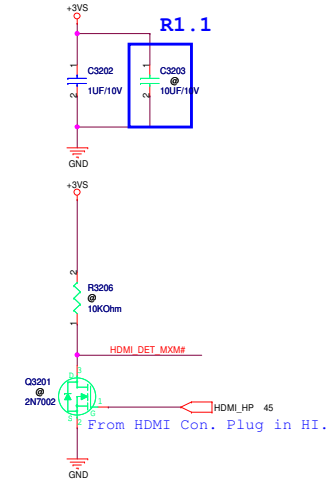
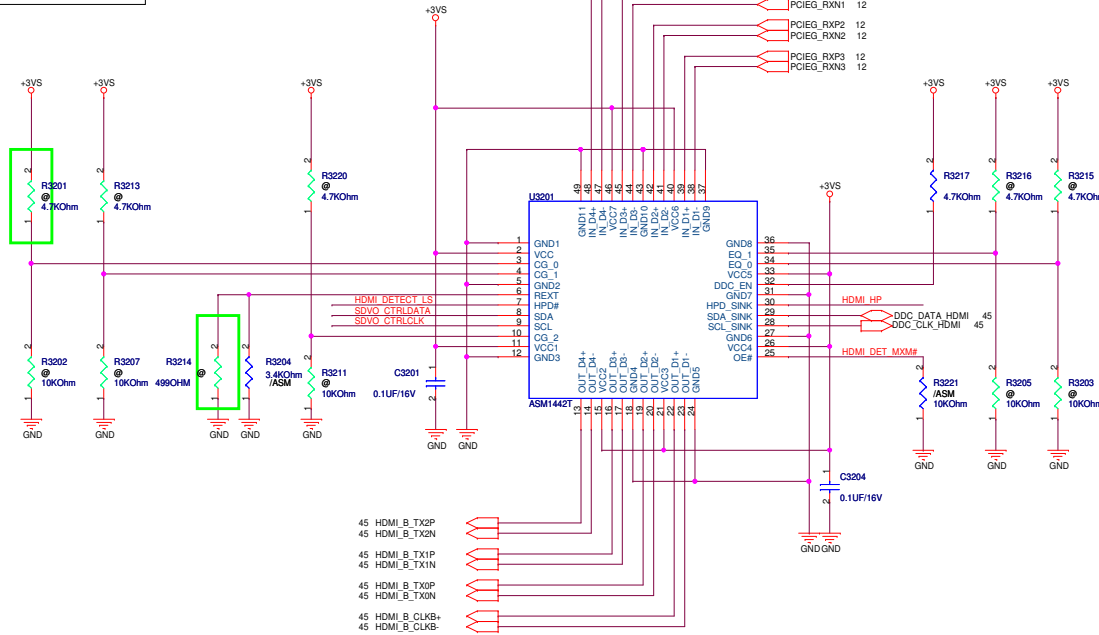
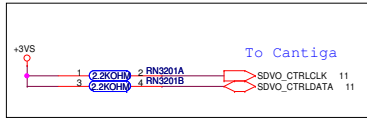
Sheet 28 of 93

CLK GEN





UMA LEVEL SHIFTERS



ASMedia ASM1442T

REMOVE:

R3201, R3214

MOUNT:

R3204, R3221

Parade PS8101T P/N:02G123000400

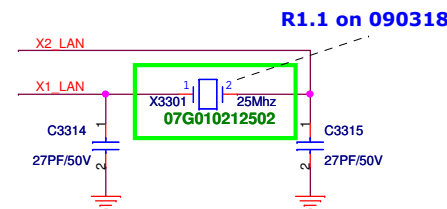
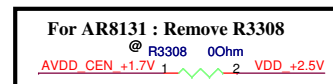
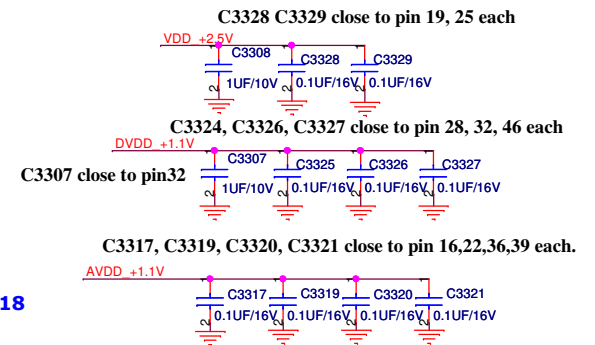
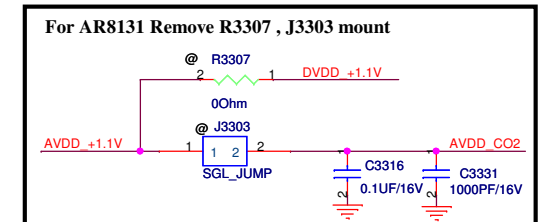
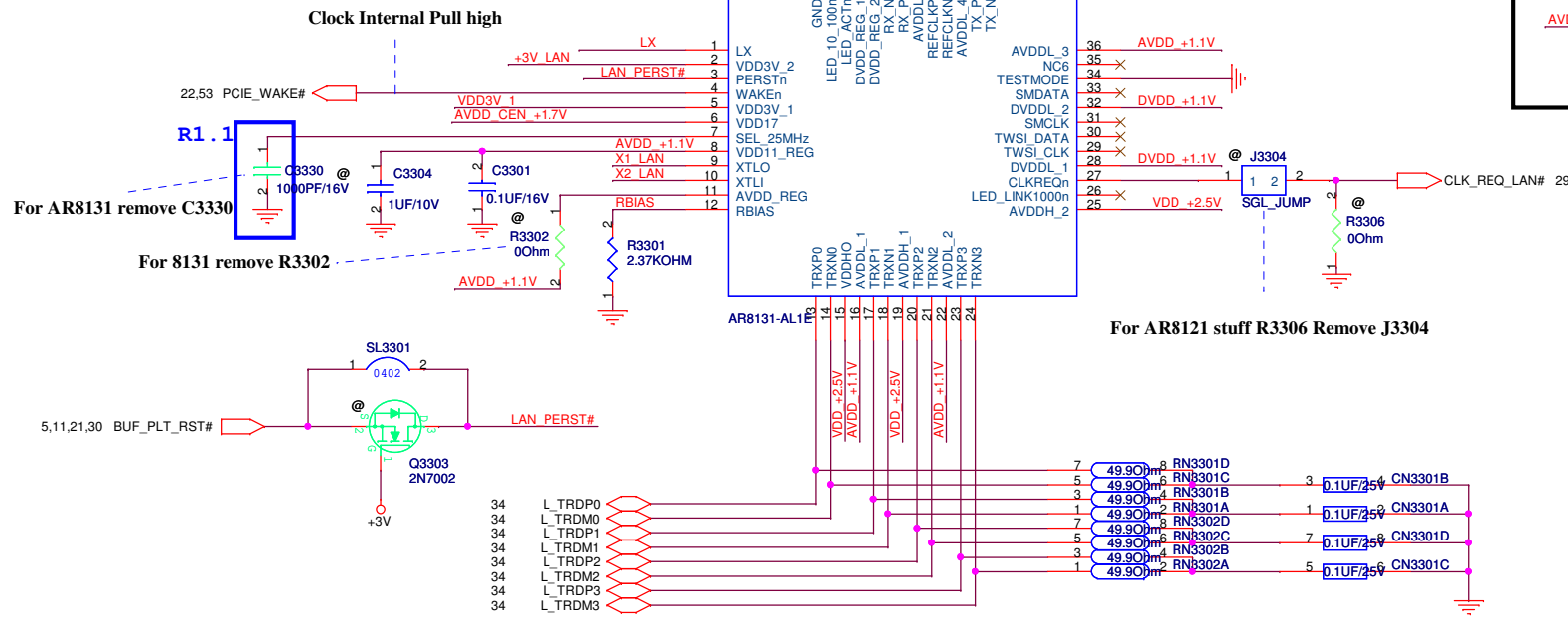
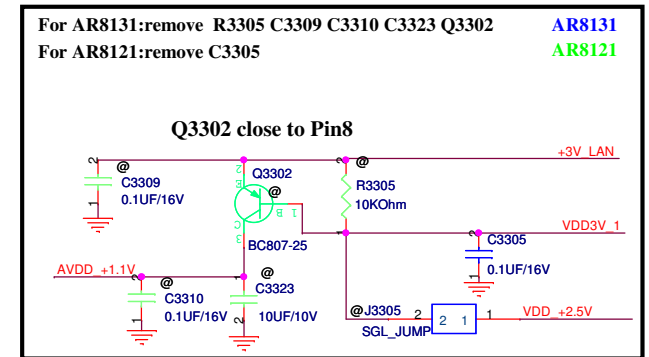
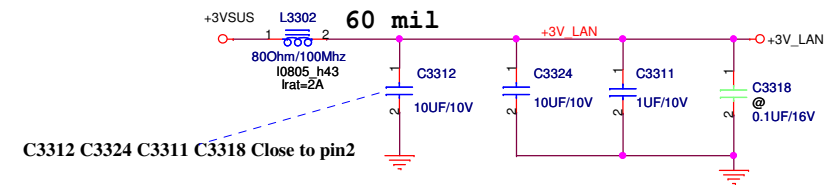
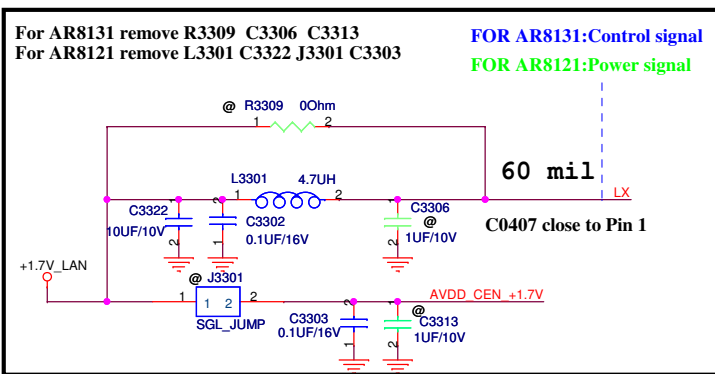
REMOVE:

R3204, R3221

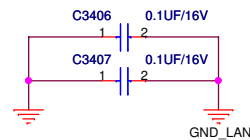
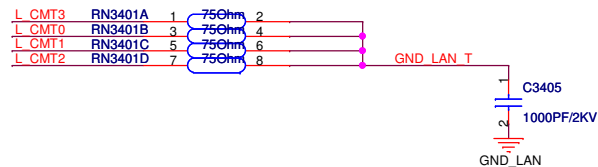
MOUNT:

R3201, R3214

綠色外框的零件是上PS8101T要補上的零件
/ASM ASM1442T才要上的零件.上PS8101T時請移除



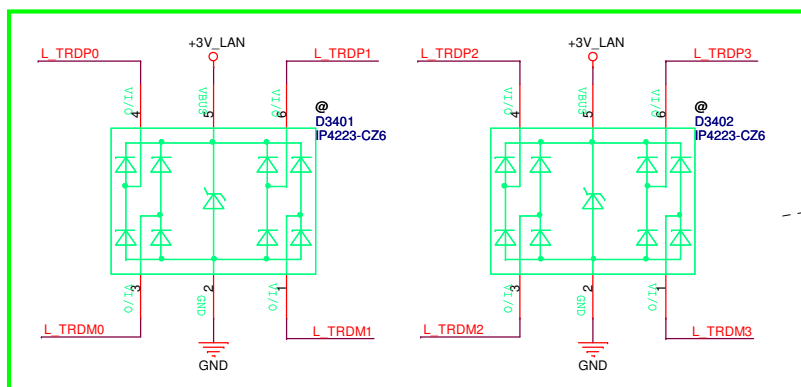
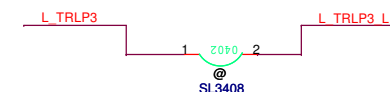
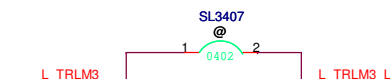
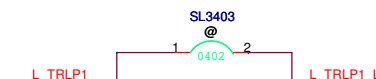
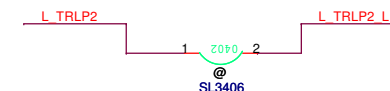
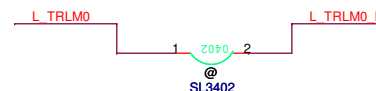
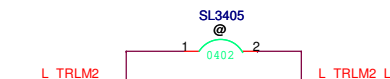
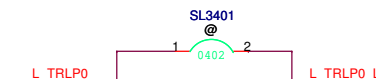
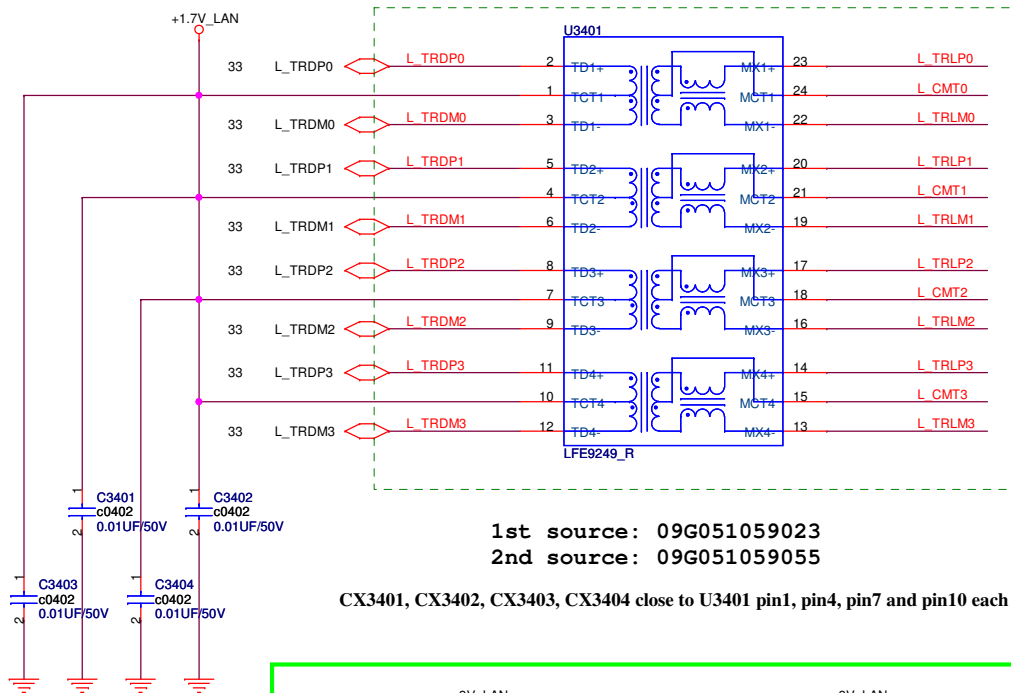
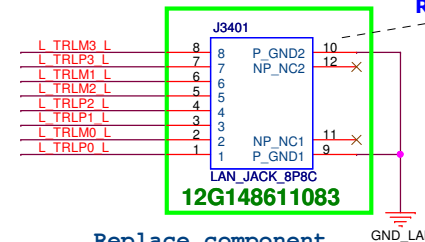
<Variant Name>		
ASUS		
Title :LAN AR8131-AR8121		
ASUSTeK COMPUTER INC Engineer: Uei Lee & Hacken		
Size	Project Name	Rev
B	UX30 MB	1.4
Date: Friday, May 08, 2009	Sheet	33 of 93



From EMI on 090216

For RJ-45

R1.1 on 090326



R1.1 on 090330

<Variant Name>

ASUS		Title :LAN RJ45 CONN	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size Custom	Project Name UX30 MB	Rev 1.4	
Date: Friday, May 08, 2009		Sheet 34 of 93	

D

C

B

A

<Variant Name>



Title :

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

Project Name	
--------------	--

Rev

A

UX30 MB

1.4

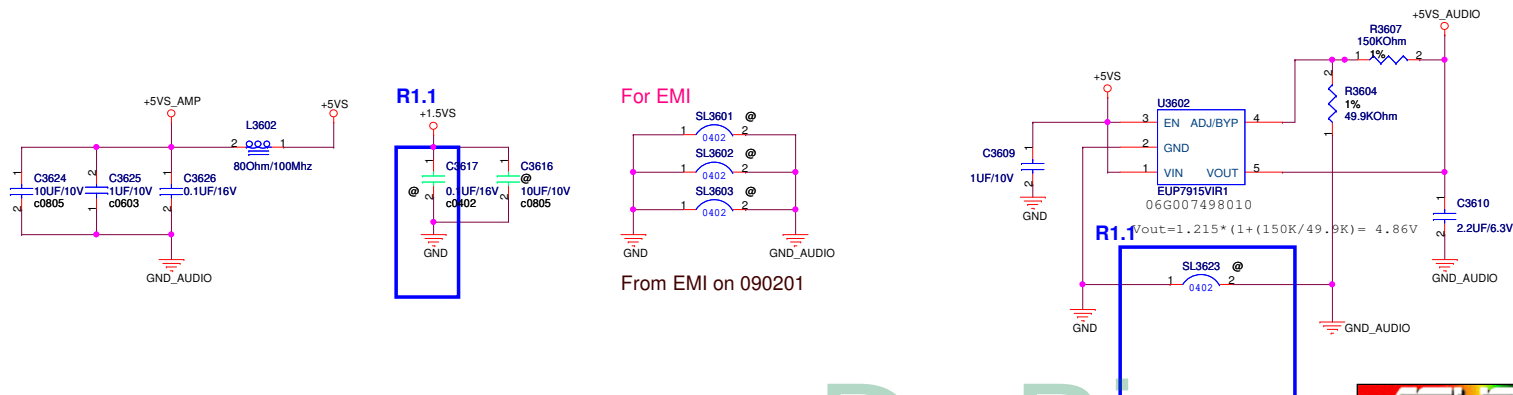
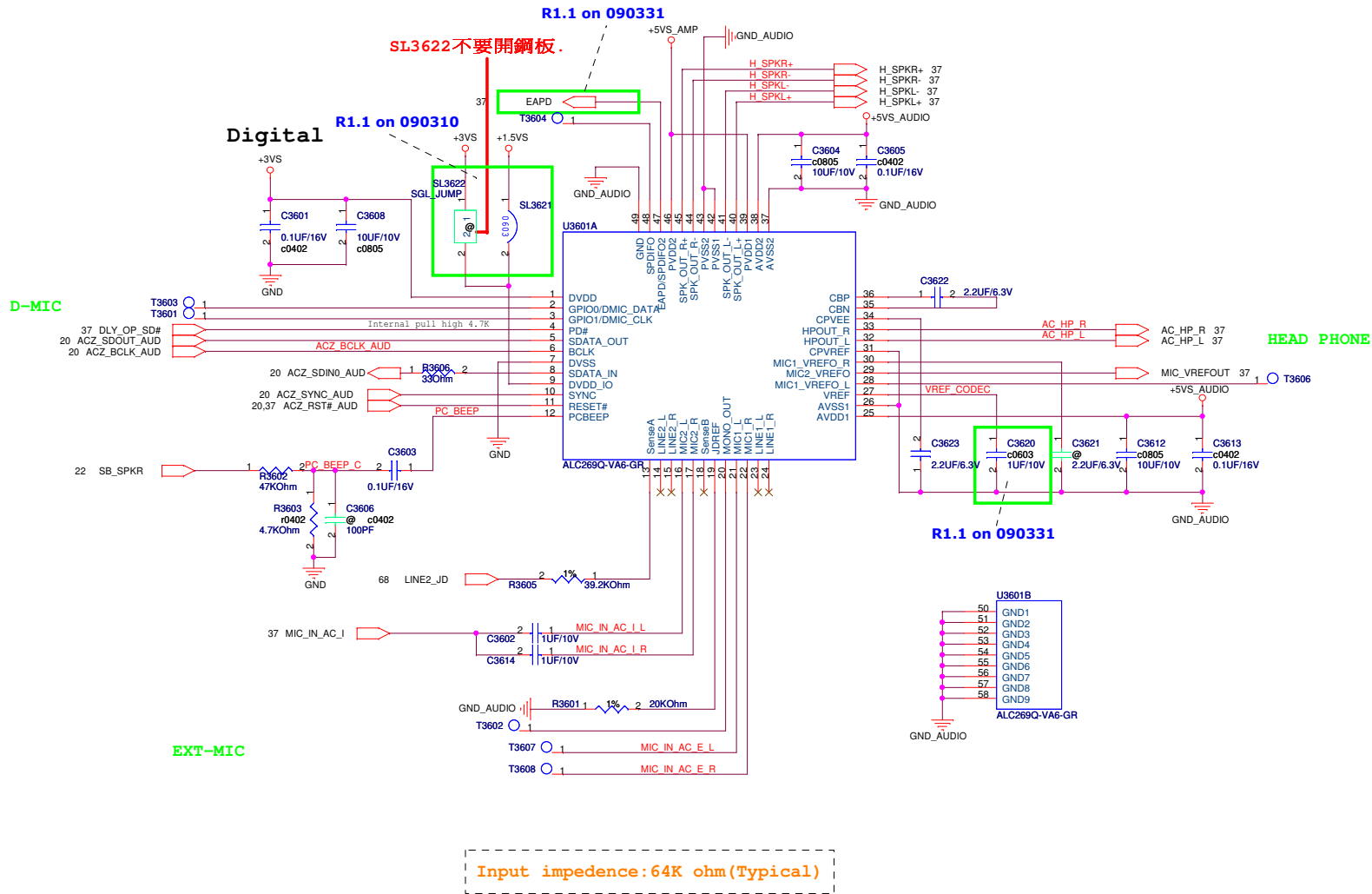
Date: Monday, April 27, 2009

Sheet

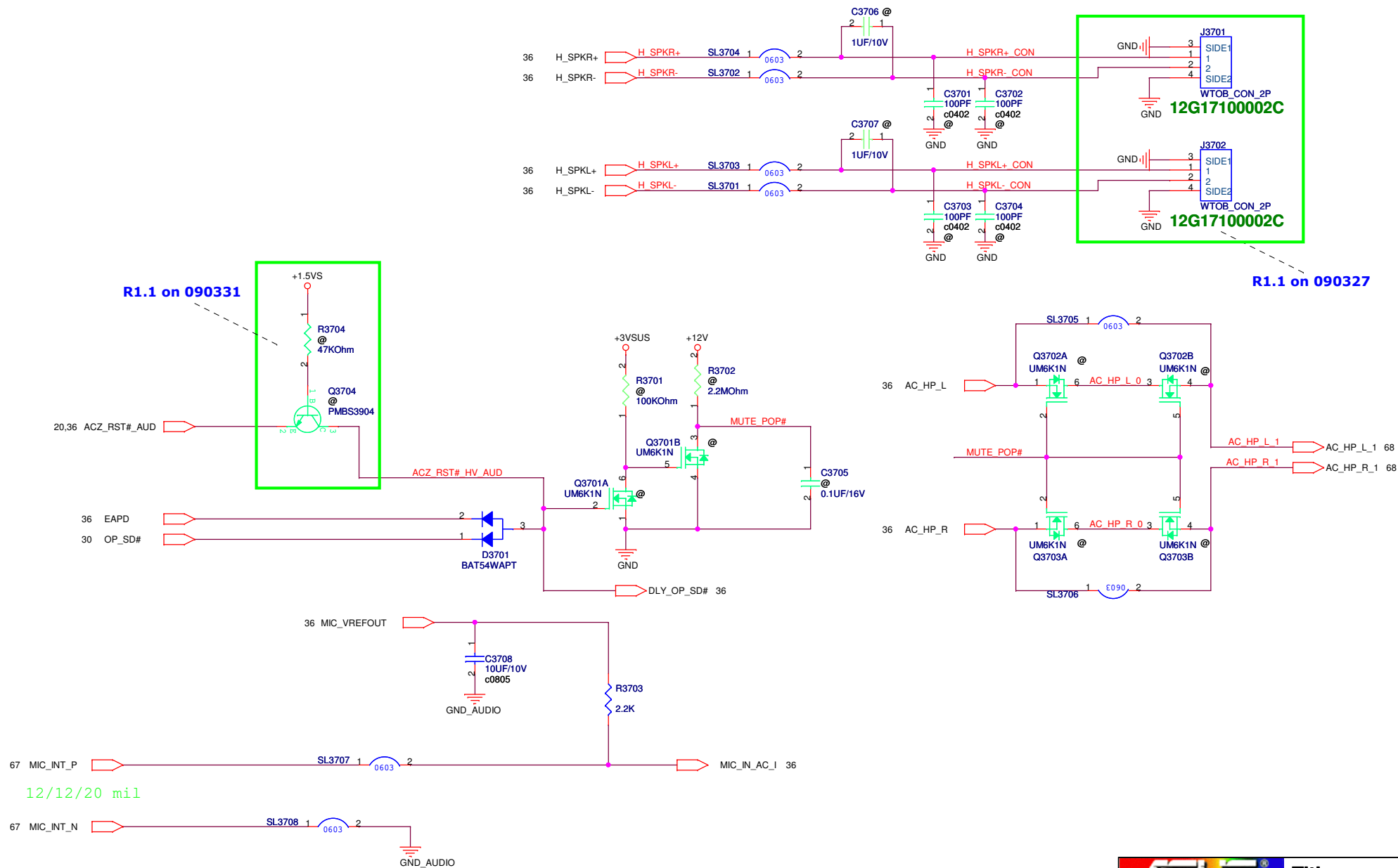
35

of

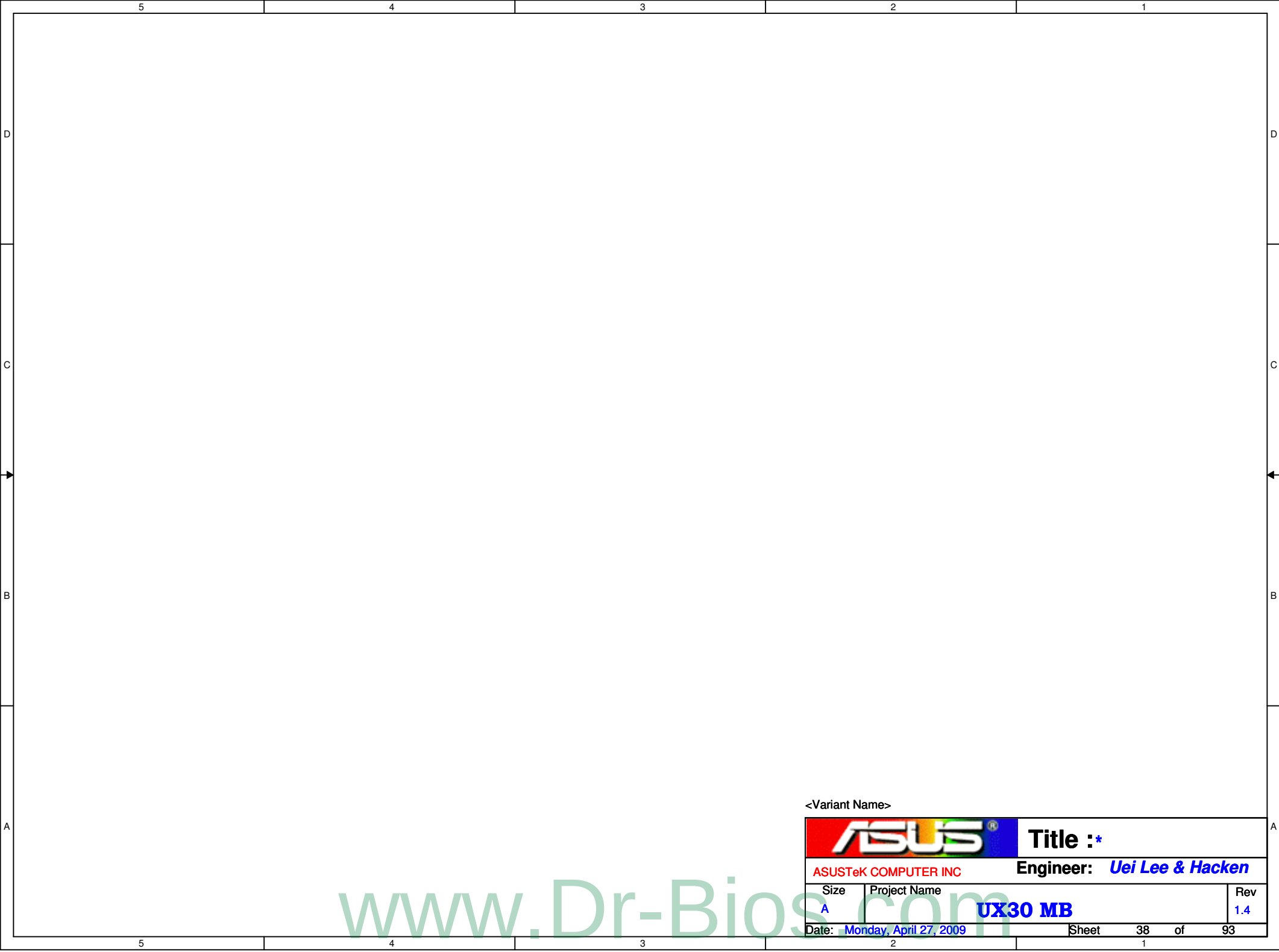
93



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ASUS		Title : PHONE JACK	
ASUSTeK COMPUTER INC. NB1		Engineer:	
Size B	Project Name UX30 MB	Rev 1.4	
Date: Friday, May 08, 2009		Sheet 37 of 93	



<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
<i>A</i>	UX30 MB		<i>1.4</i>
Date: <i>Monday, April 27, 2009</i>		Sheet	38 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	39 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	40 of 93

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

Project Name	
--------------	--

Rev

A

UX30 MB

1.4

Date: Monday, April 27, 2009

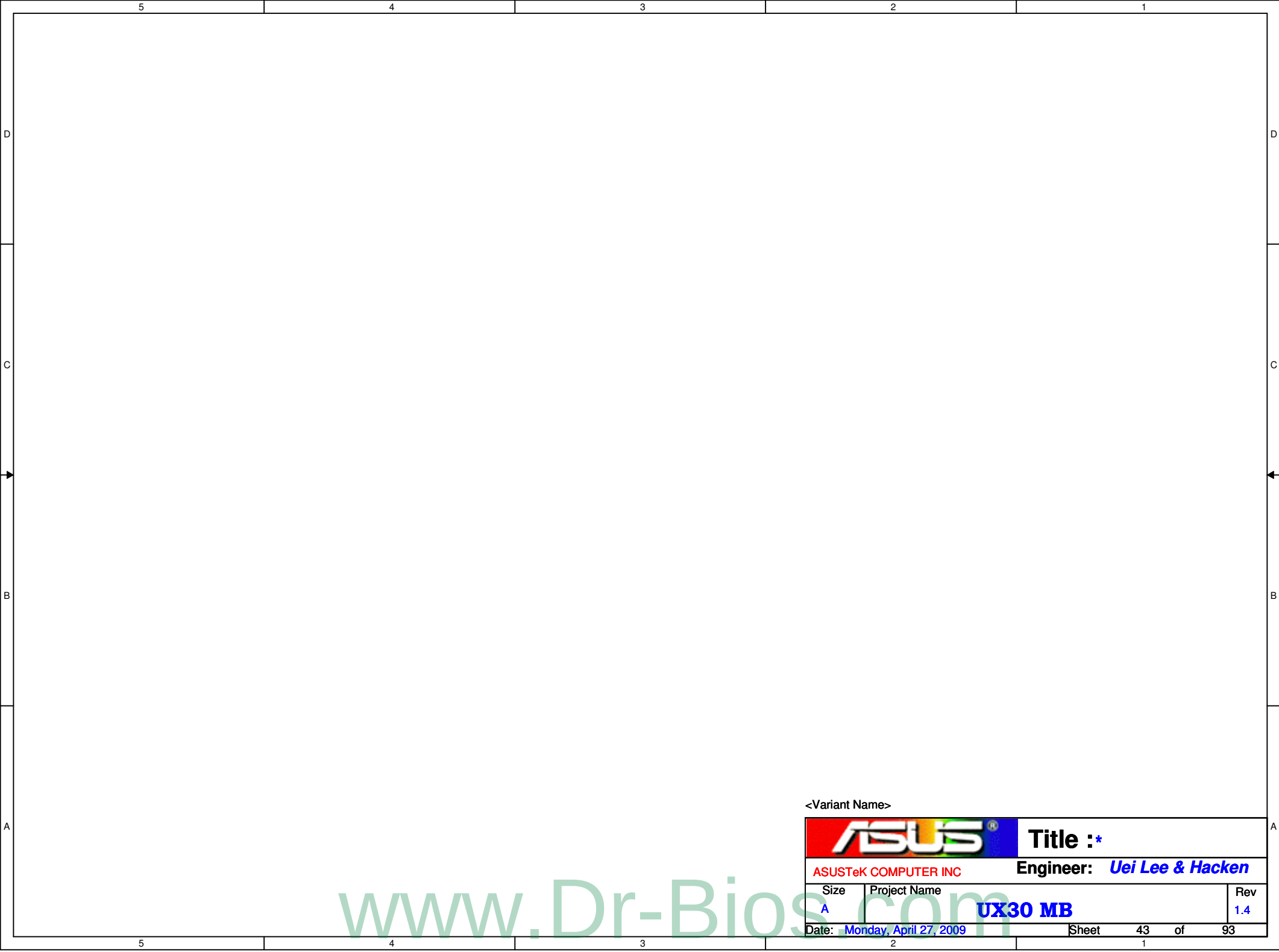
Sheet

41

of

93

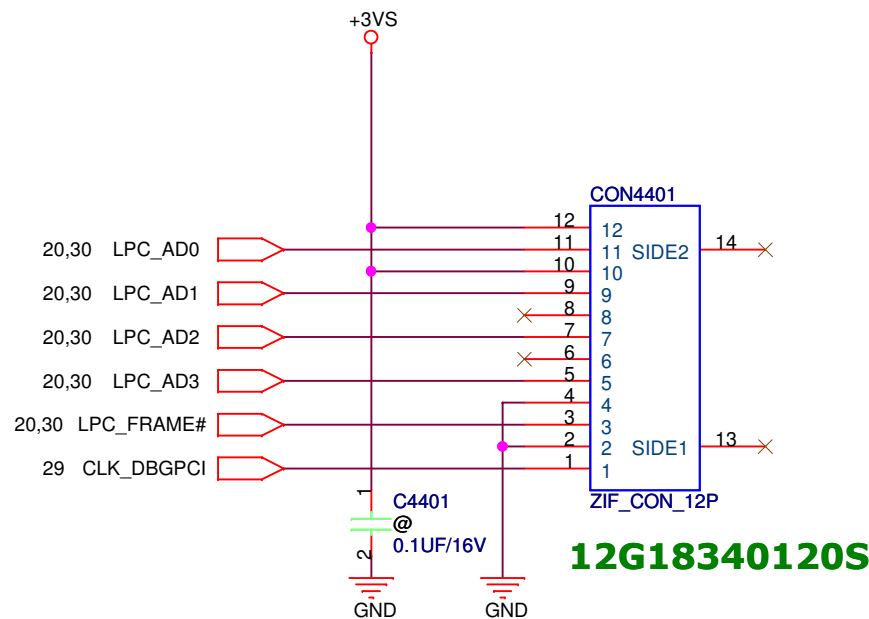
ASUSTeK COMPUTER INC	
Size	Project Name
A	UX
Date: Monday, April 27, 2009	



<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
<i>A</i>	UX30 MB		<i>1.4</i>
Date: <i>Monday, April 27, 2009</i>		Sheet	43 of 93

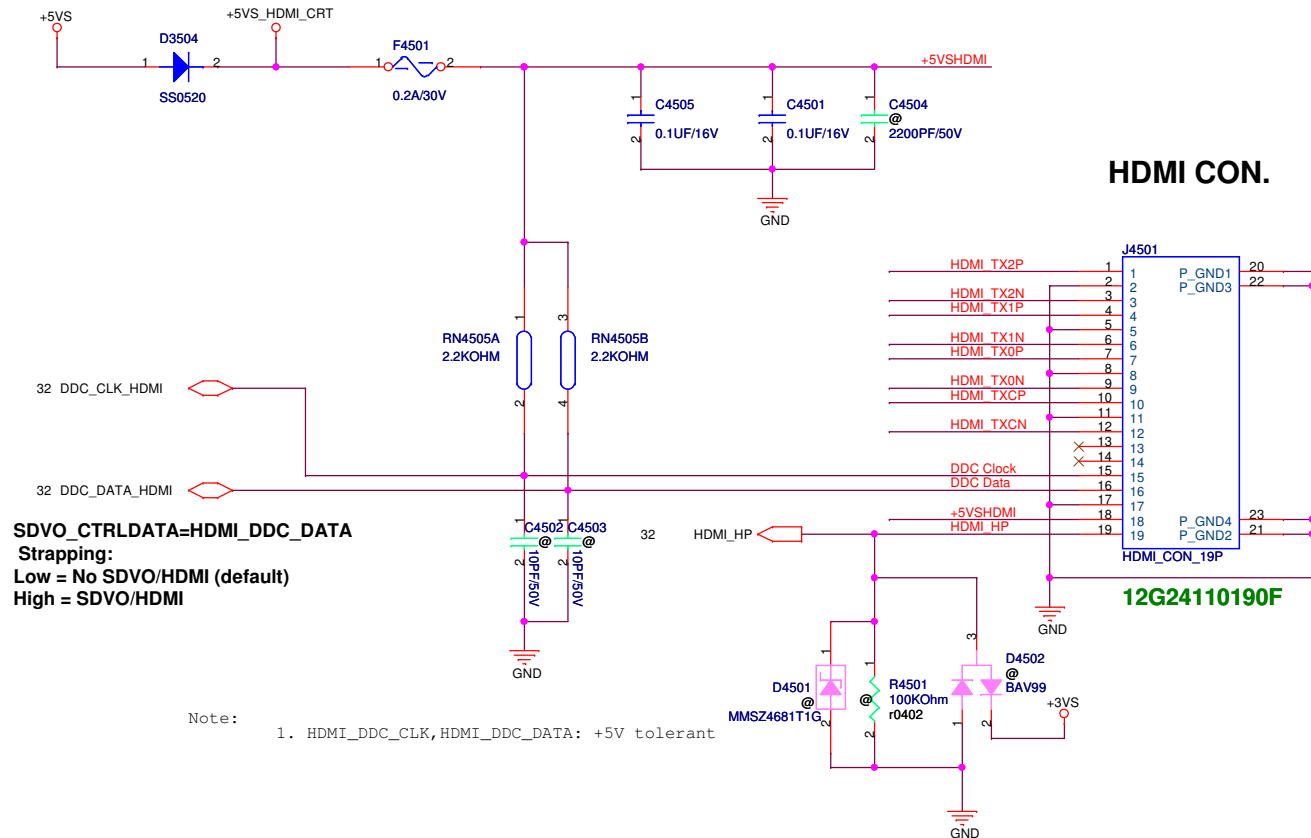
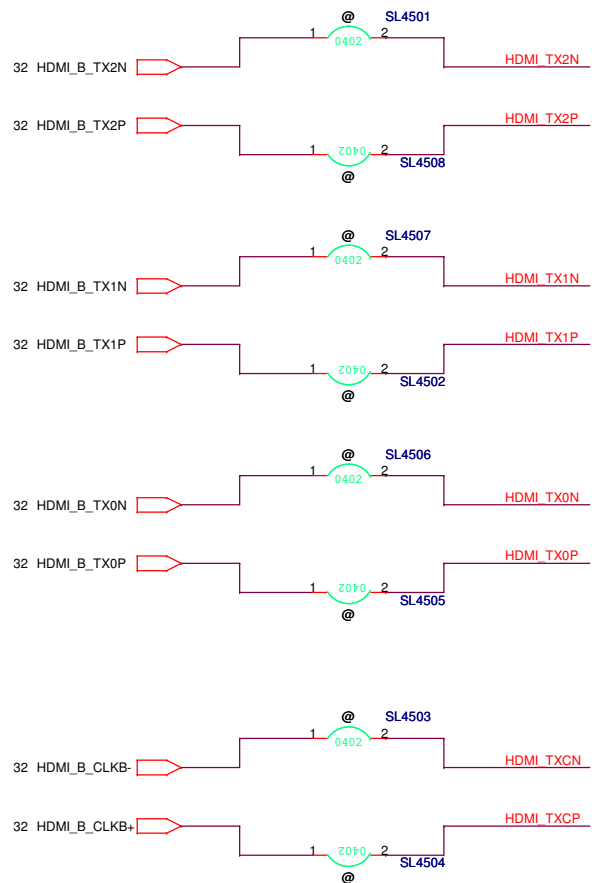
LPC DEBUG PORT



<Variant Name>

		Title :BUG DEBUG PORT	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: Friday, May 08, 2009		Sheet	44 of 93

From Level Shifter Close to CONNECTOR



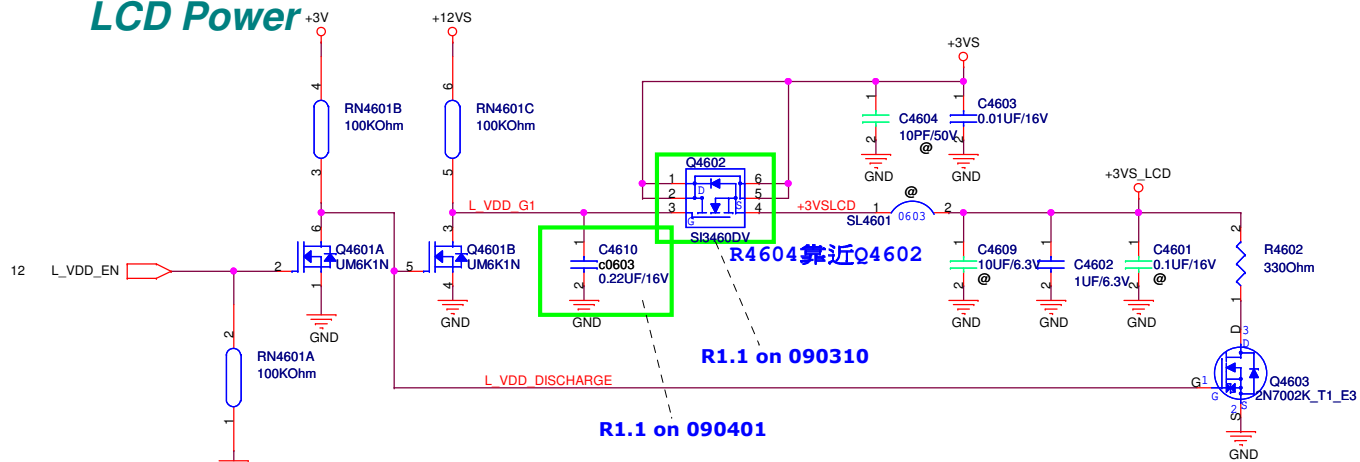
SDVO_CTRLDATA=HDMI_DDC_DATA
Strapping:
Low = No SDVO/HDMI (default)
High = SDVO/HDMI

Note: 1. HDMI_DDC_CLK, HDMI_DDC_DATA: +5V tolerant

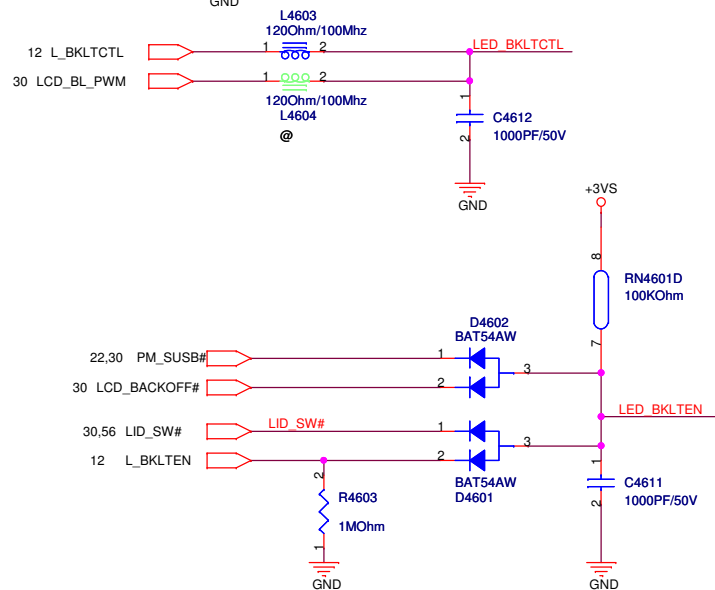
<Variant Name>

ASUS		Title :HDMI CONN	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4	
Date: Friday, May 08, 2009		Sheet 45 of 93	

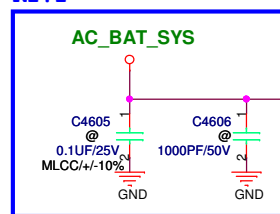
LCD Power



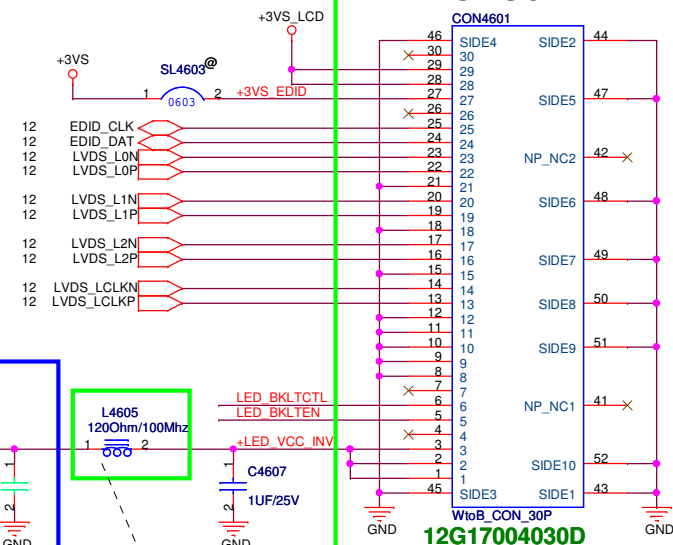
R1.1 on 090402



R1.1



R1.1 on 090330 for EMI

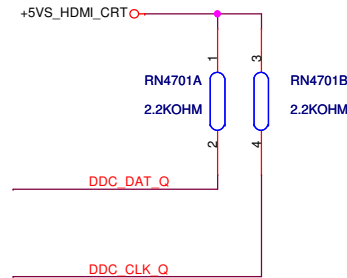
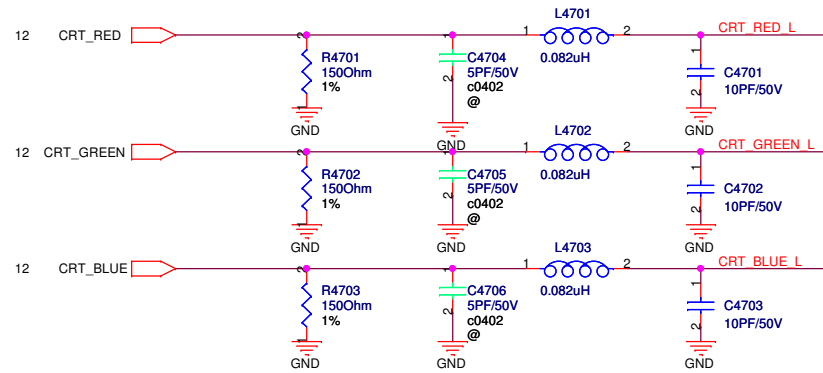
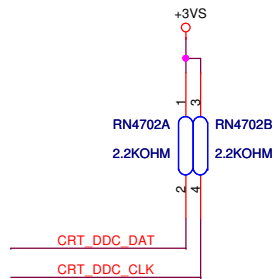


<Variant Name>

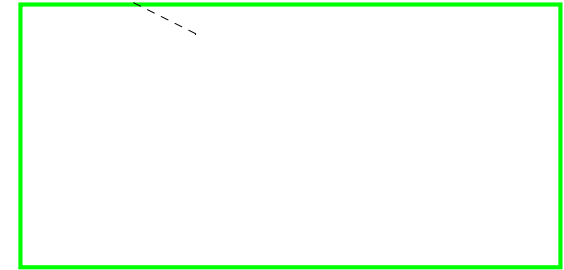
ASUS		Title :CRT LVDS CONN	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Date Friday, May 08, 2009	Rev 1.4
Sheet 46 of 93			

CRT Connector

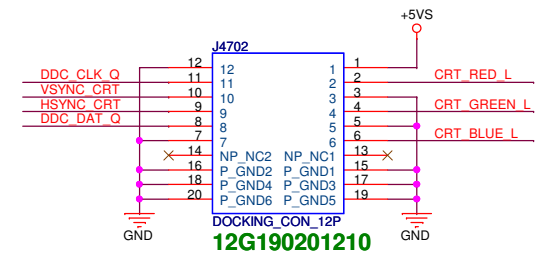
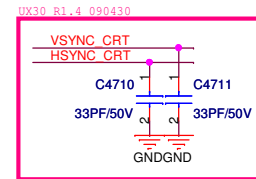
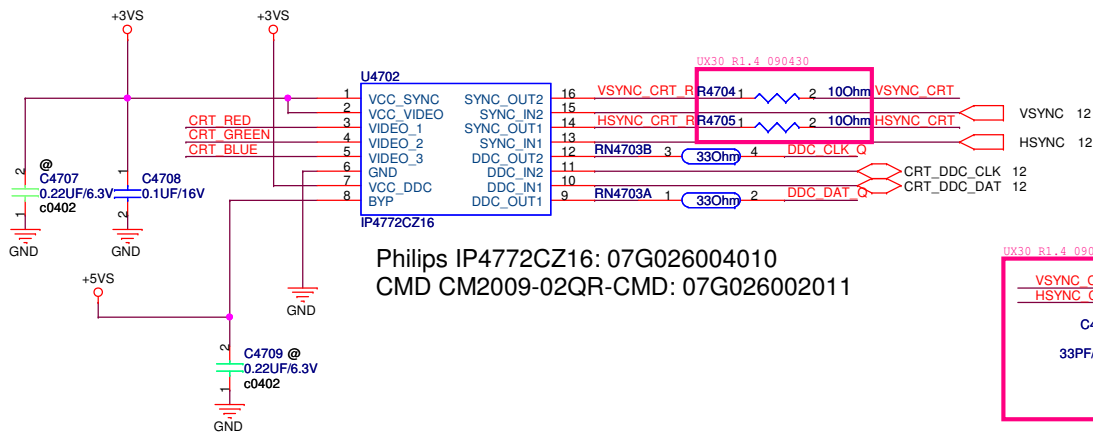
+3VSUS ○ +3VSUS 20,21,22,23,30,33,37,53,56,57,81,87,88
 +12VS ○ +12VS 22,46,53,87
 +5VS ○ +5VS 23,30,36,45,50,51,56,57,80,84,87
 +5VS_HDMI_CRT ○ +5VS_HDMI_CRT 45



R1.1 on 090327



PLACE ESD IC near J4701



ASUS		Title : CRT	
<OrgName>		Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Date: Friday, May 08, 2009	Rev 1.4
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<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

A

Project Name

UX30 MB

Rev

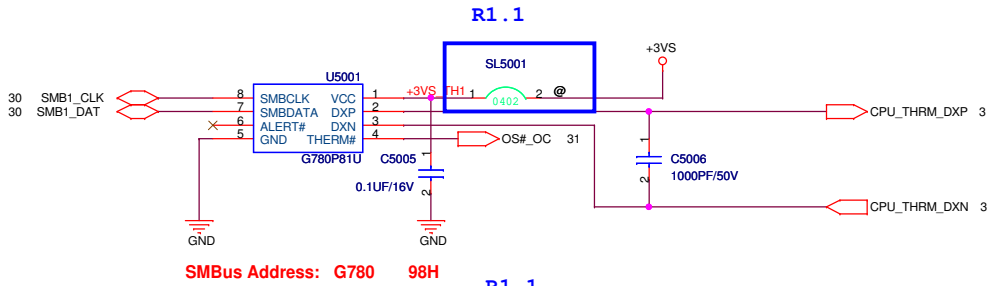
1.4

Date: Monday, April 27, 2009

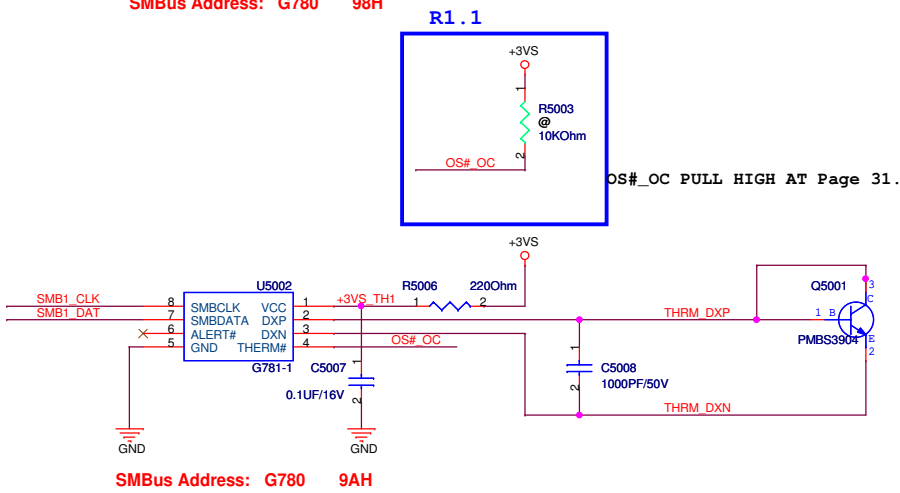
Sheet 49 of 93

Thermal Seneor

CPU



CHASSIS

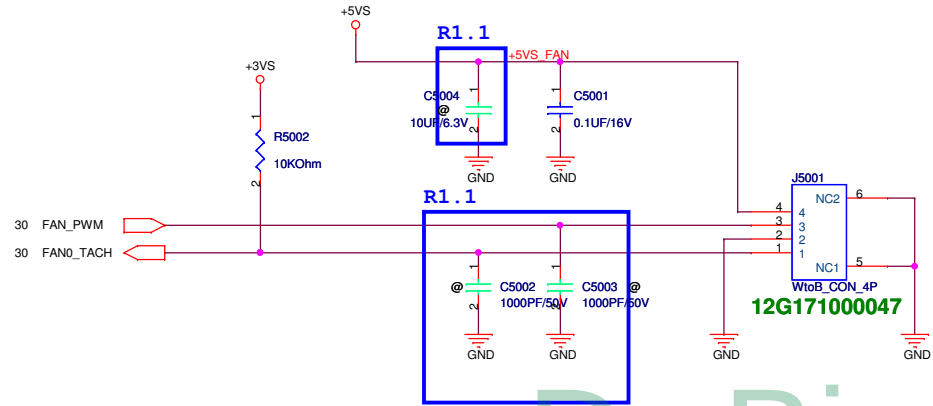


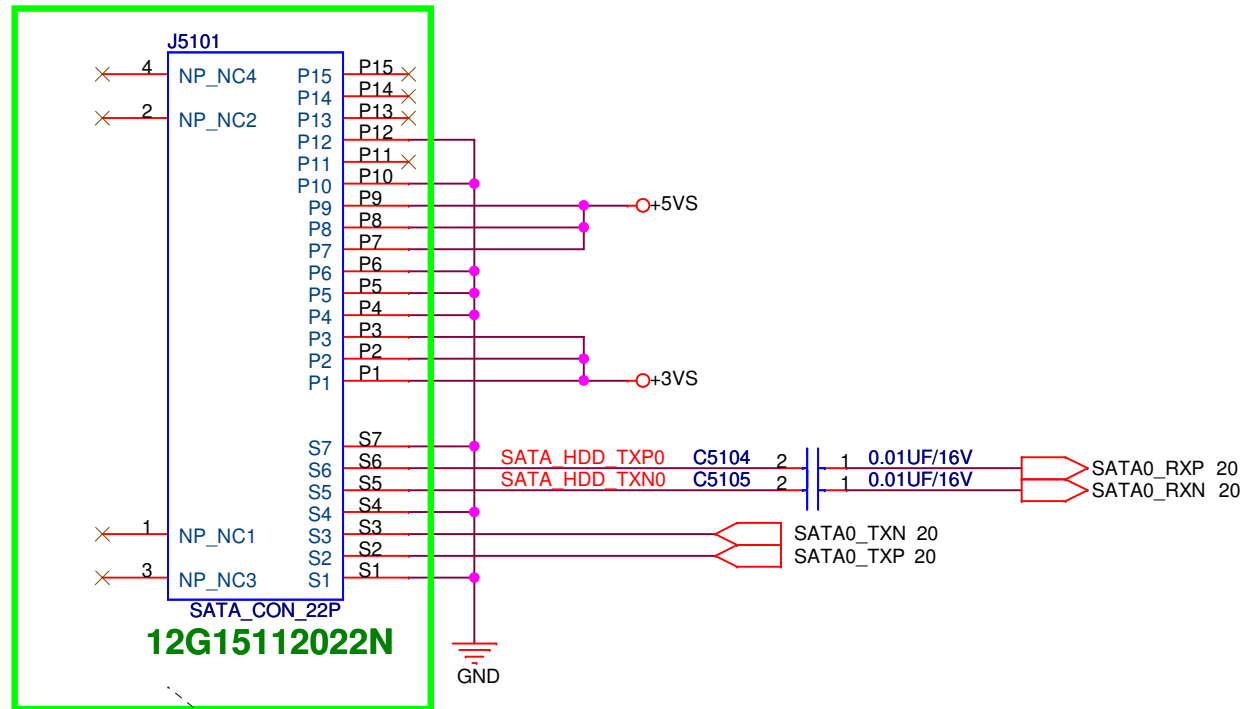
Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

Avoid FSB,Power

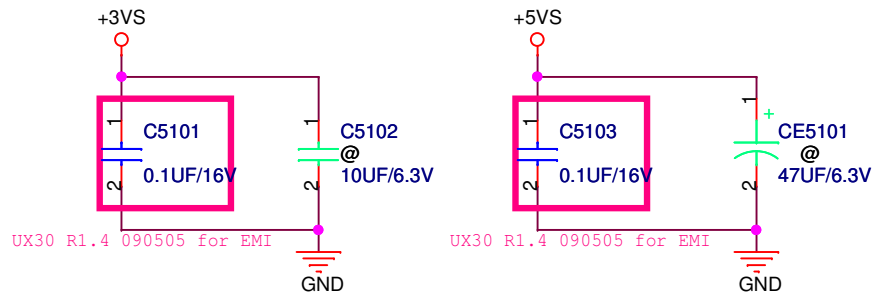
FAN CONN





R1.1 on 090401

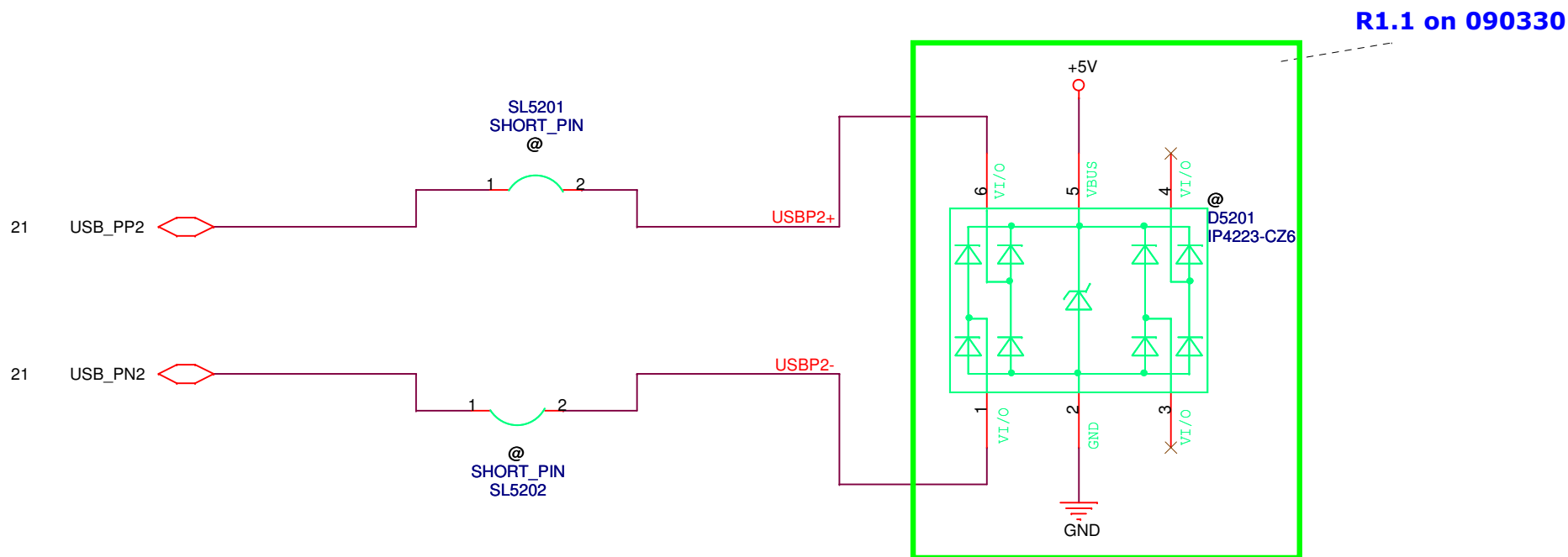
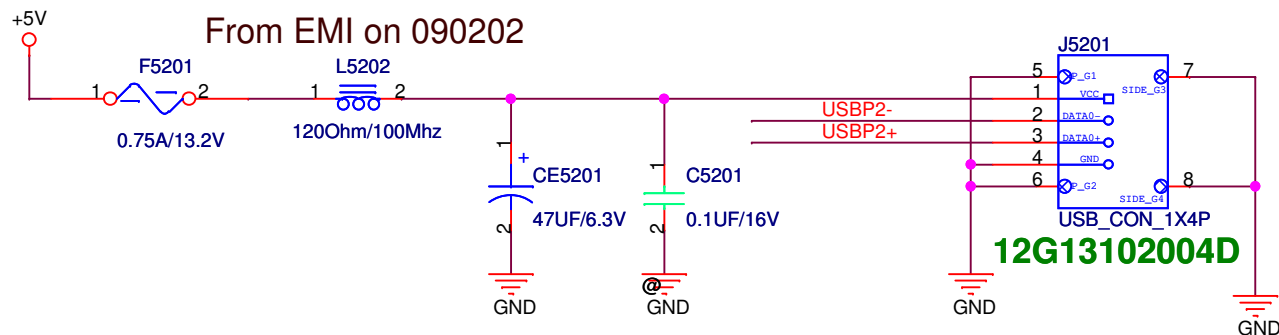
3VS 5VS 線寬拉80mils



<Variant Name>

ASUS		Title: XDD SATA HDD CONN	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size	Project Name	Rev	
A	UX30 MB	1.4	
Date: Friday, May 08, 2009	Sheet	51	of 93

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<Variant Name>

ASUS		Title :USB CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size A	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009		Sheet	52 of 93

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	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	54 of 93

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

Project Name	Project Manager	Project Start Date	Project End Date	Project Status	Project Budget	Project Risk	Project Complexity	Project Importance	Project Priority
Project A	John Doe	2023-01-01	2023-03-31	Completed	\$100,000	Low	Medium	High	High
Project B	Jane Smith	2023-04-01	2023-06-30	In Progress	\$200,000	Medium	High	Medium	Medium
Project C	Mike Johnson	2023-07-01	2023-09-30	On Hold	\$50,000	Low	Low	Low	Low
Project D	Sarah Brown	2023-10-01	2023-12-31	Planned	\$300,000	High	Very High	Very High	Very High

Rev

A

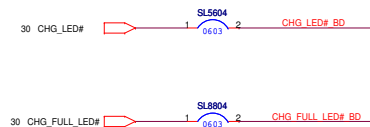
UX30 MB

1.4

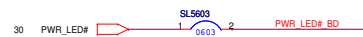
Date: Monday, April 27, 2009

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CHARGE LED



POWER LED



CAP LOCK LED

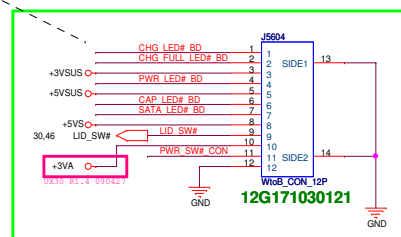


NUM LOCK LED



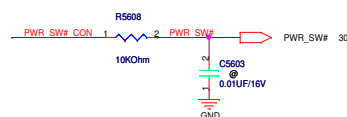
R1.1 on 090330

R1.1 on 090327



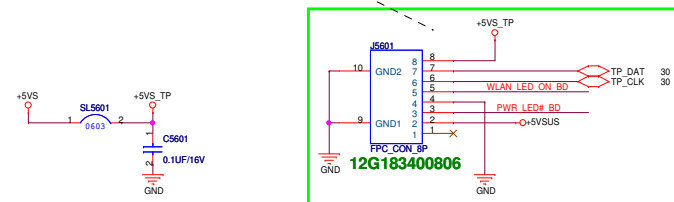
R1.1

POWER BTN

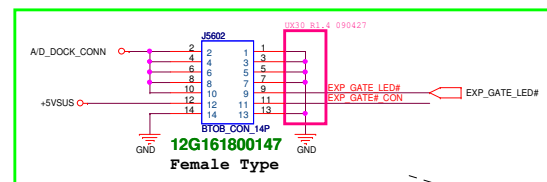


Touch-Pad

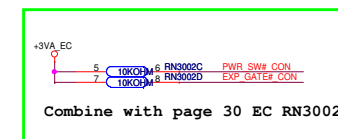
R1.1 on 090327



EXPRESS GATE BTN and DC-IN



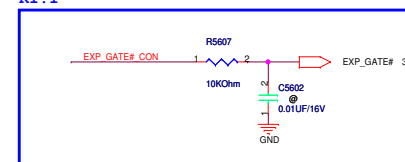
R1.1 on 090401



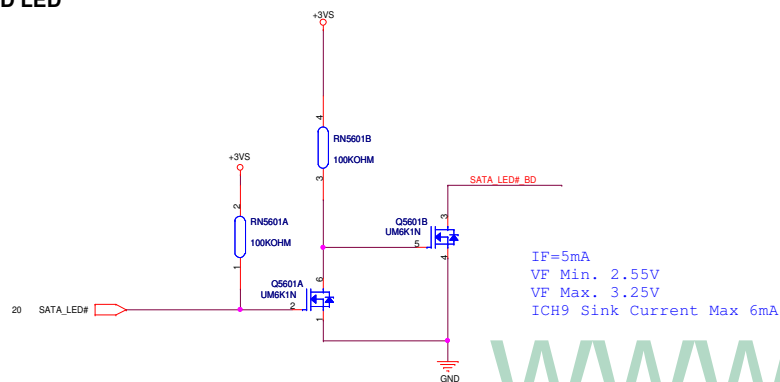
Combine with page 30 EC RN3002

EXPRESS GATE BTN

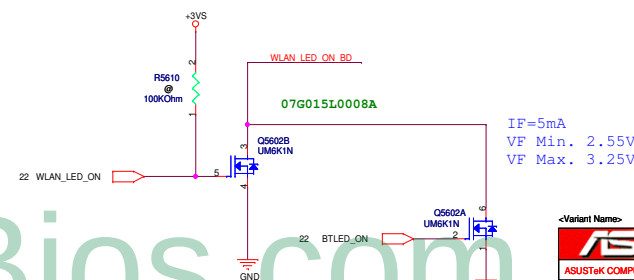
R1.1



HDD LED



WireLess/BT LED

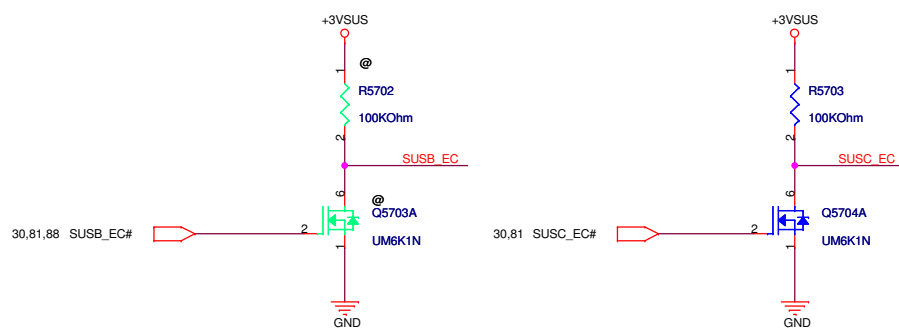
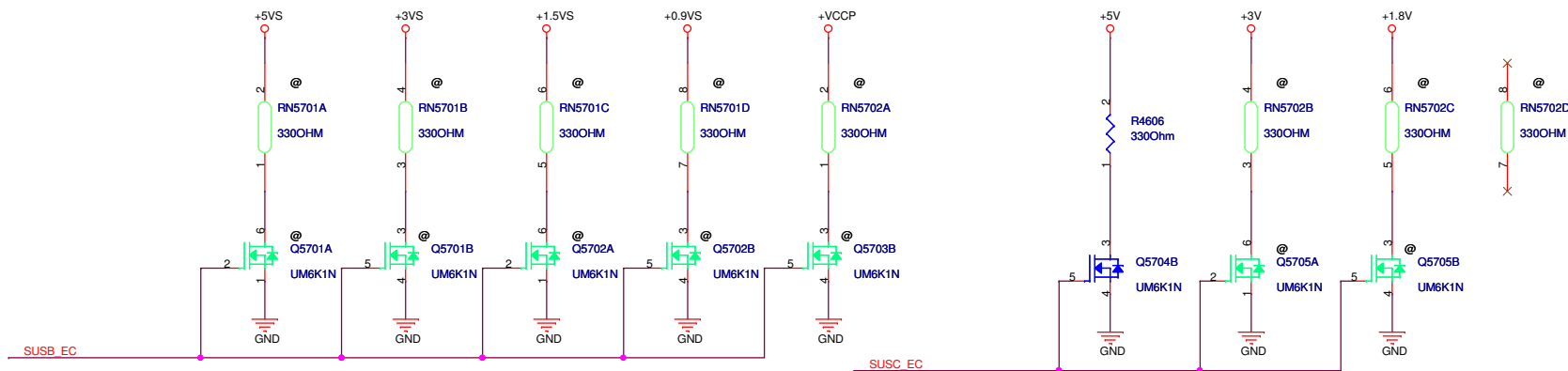


Title :			
ASUSTeK COMPUTER INC			
Engineer: Uei Lee & Hacken			
Size	Project Name	Rev	
C	UX30 MB	1.4	
Date: Friday, May 08, 2009	Sheet	56	of 93

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Discharge Circuit

+5VS		+5VS	23,30,36,45,47,50,51,56,80,84,87
+3VS		+3VS	3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,80,87,88
+1.5VS		+1.5VS	4,15,20,23,36,37,53,84
+VCCP		+VCCP	3,4,5,10,11,12,14,15,20,23,82
+5V		+5V	52,68,87
+3V		+3V	21,33,42,46,53,61,67,87
+1.8V		+1.8V	8,9,11,14,19,83,87
+0.9VS		+0.9VS	9,83
+3VSUS		+3VSUS	20,21,22,23,30,33,37,53,56,81,87,88



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D

C

B

A

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

Project Name	
--------------	--

Rev

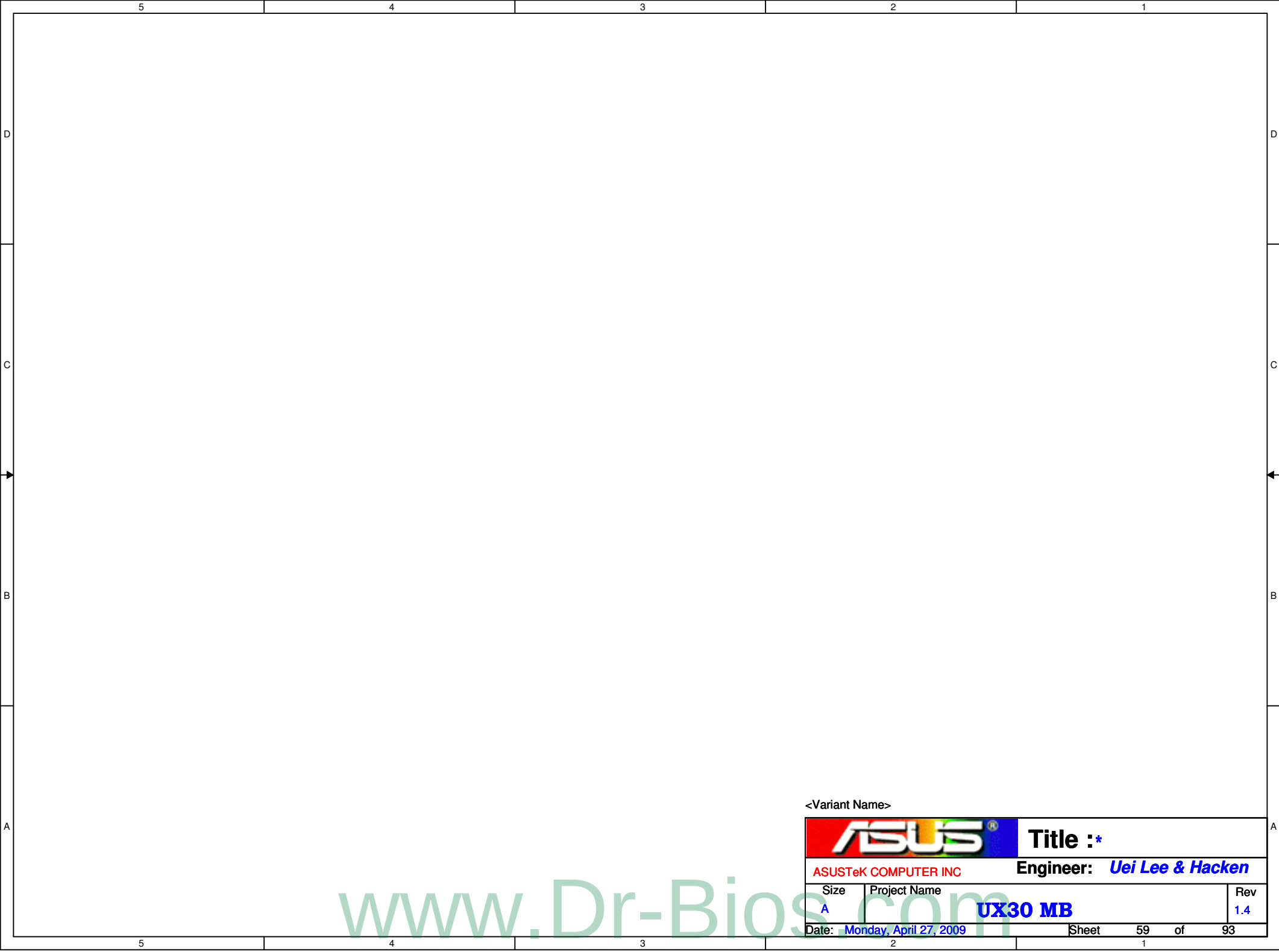
A

UX30 MB

1.4

Date: Monday, April 27, 2009

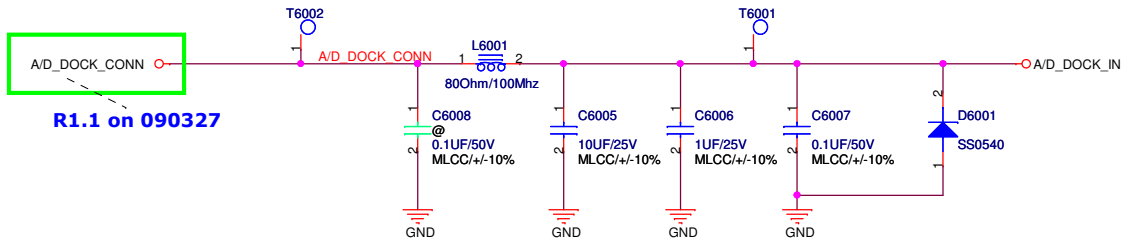
Sheet 58 of 93



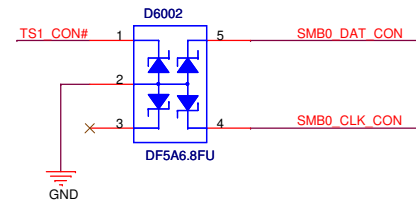
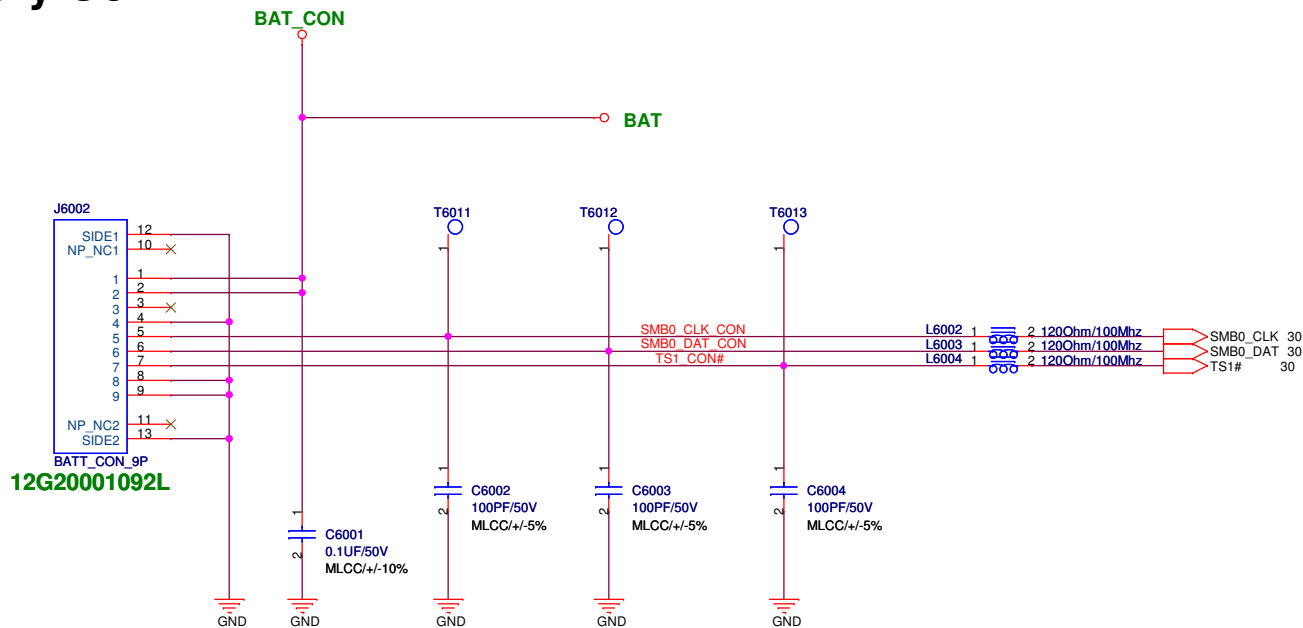
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		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	59 of 93

DC-IN



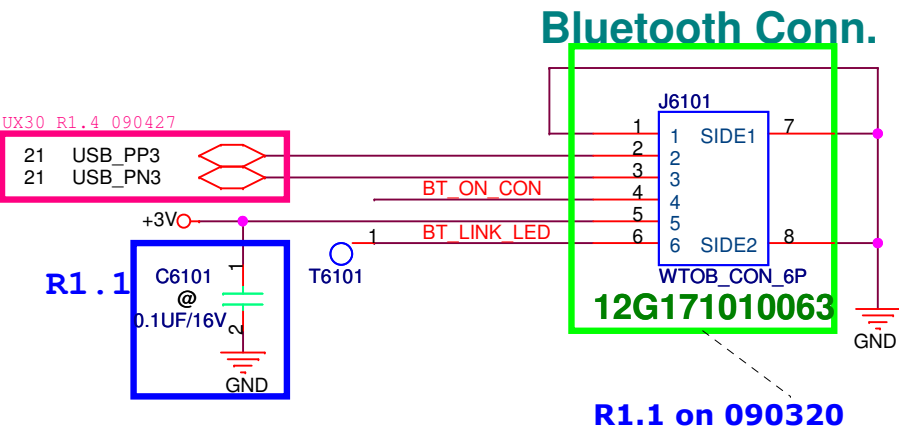
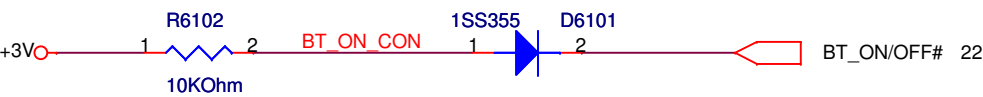
Battery Conn



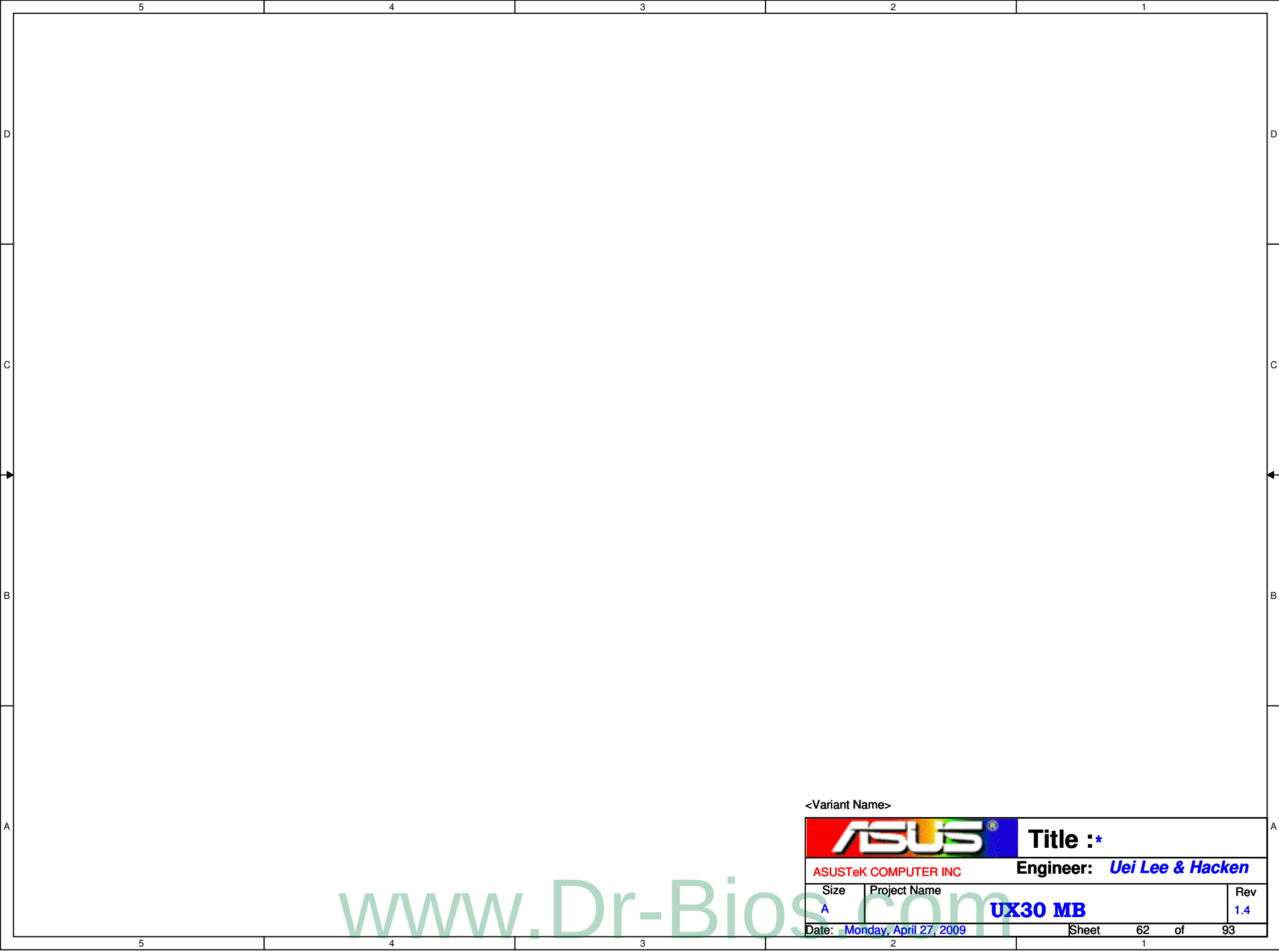
<Variant Name>

		Title :DC DC&BATT CONN	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009		Sheet 60	of 93

BT CON



<Variant Name>			
		Title : BT BLUETOOTH CONN	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: Friday, May 08, 2009		Sheet	61 of 93



<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	62 of 93

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D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

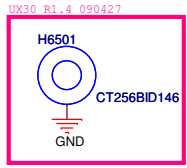
		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	63 of 93

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

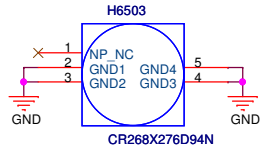
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		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	64 of 93

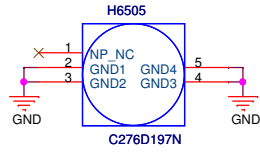
Screw Hole & SMT Nut



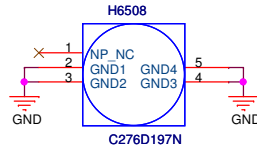
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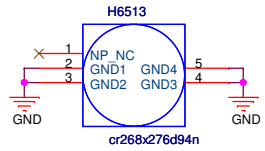
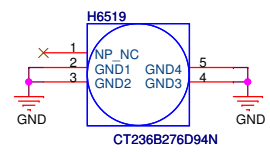
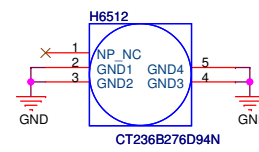
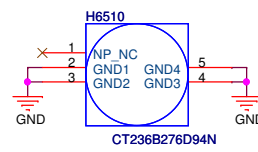
B



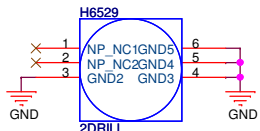
C



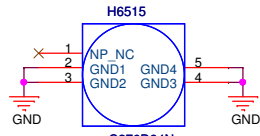
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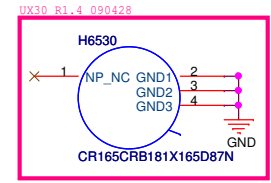
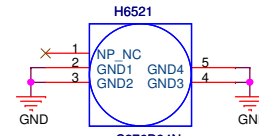
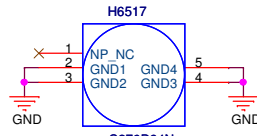
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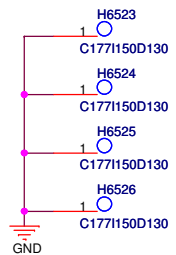
J



G



K



F CPU & NB 背架 螺絲孔

<Variant Name>		ME SCREW HOLE AMT NUT	
ASUS		Title :	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size	Project Name	Rev	
B	UX30 MB	1.4	
Date: Tuesday, April 28, 2009		Sheet 65 of 93	

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

A

Project Name

UX30 MB

Rev

1.4

Date: Monday, April 27, 2009

Sheet

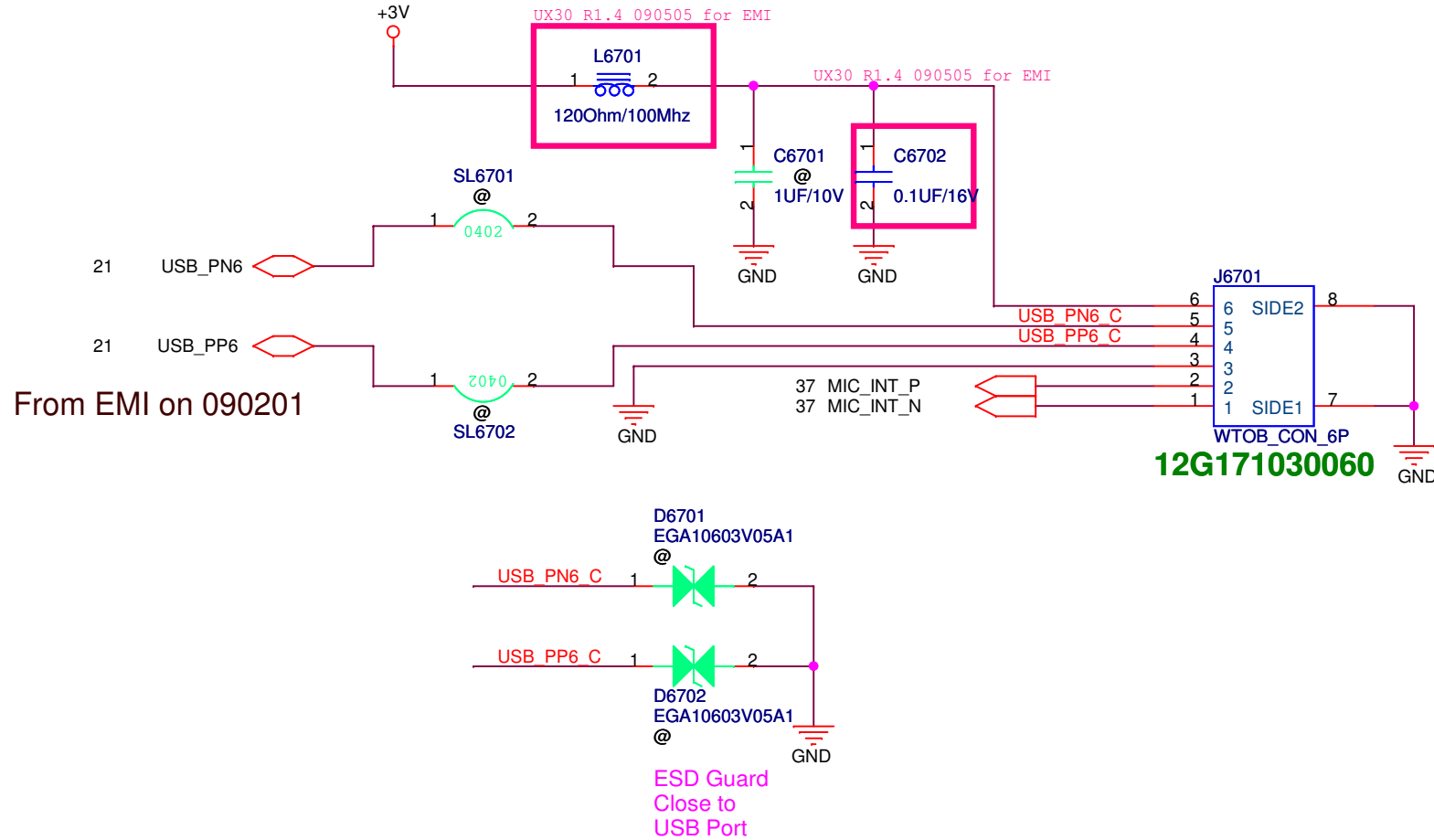
66

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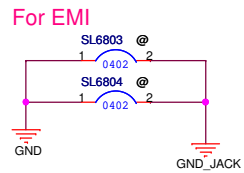
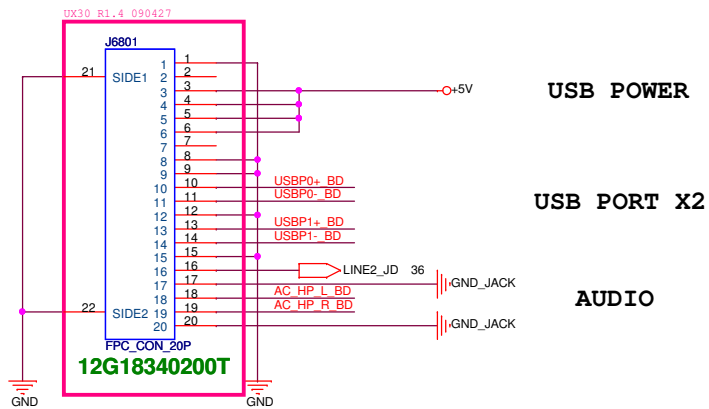
Camera Module

3V CAMERA MODULE

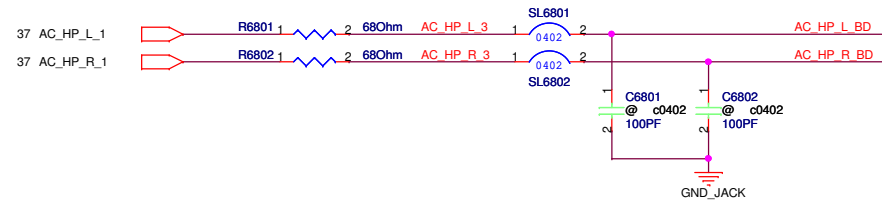


<Variant Name>

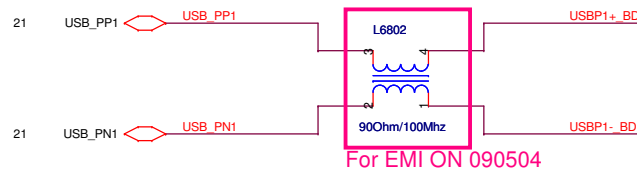
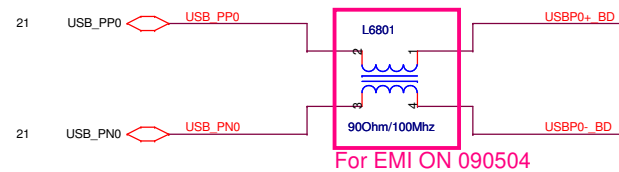
		Title : CMOS CAMERA	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009		Sheet	67 of 93



From EMI on 090202



USB PORT X2



SYSTEM

+VCCP   +VCCP 3,4,5,10,11,12,14,15,20,23,57,82
+VCC_GMCH   +VCC_GMCH 14
+VGFX_CORE   +VGFX_CORE 14

+3VS   +3VS 3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,57,80,87,88
+VCORE   +VCORE 4,5,80
+1.5VS   +1.5VS 4,15,20,23,36,37,53,57,84

+12VS   +12VS 22,46,53,87

AC_BAT_SYS   AC_BAT_SYS 46,80,81,82,83,85

+5V   +5V 52,57,68,87

BAT   BAT 60,85

+5VS   +5VS 23,30,36,45,47,50,51,56,57,80,84,87
+3VA   +3VA 20,30,56,81,85
+VCC_RTC   +VCC_RTC 20,23
+3V   +3V 21,33,42,46,53,57,61,67,87
+3VSUS   +3VSUS 20,21,22,23,30,33,37,53,56,57,81,87,88
+5VSUS   +5VSUS 23,56,81,82,83,85,87
+3VPLL   +3VPLL 30
+3VACC   +3VACC 30
+3VA_ECO   +3VA_EC 30,31,56

+5VA   +5VA 81
A/D_DOCK_IN   A/D_DOCK_IN 60,85
BAT_CON   BAT_CON 60,85

+5VS_AMP   +5VS_AMP 36
+12V   +12V 37,87

<Variant Name>

		Title : POWER SOURCE	
ASUSTeK COMPUTER INC		Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009		Sheet	69 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	70 of 93

D

C |

B

A

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size

Project Name	
--------------	--

Rev

A

UX30 MB

1.4

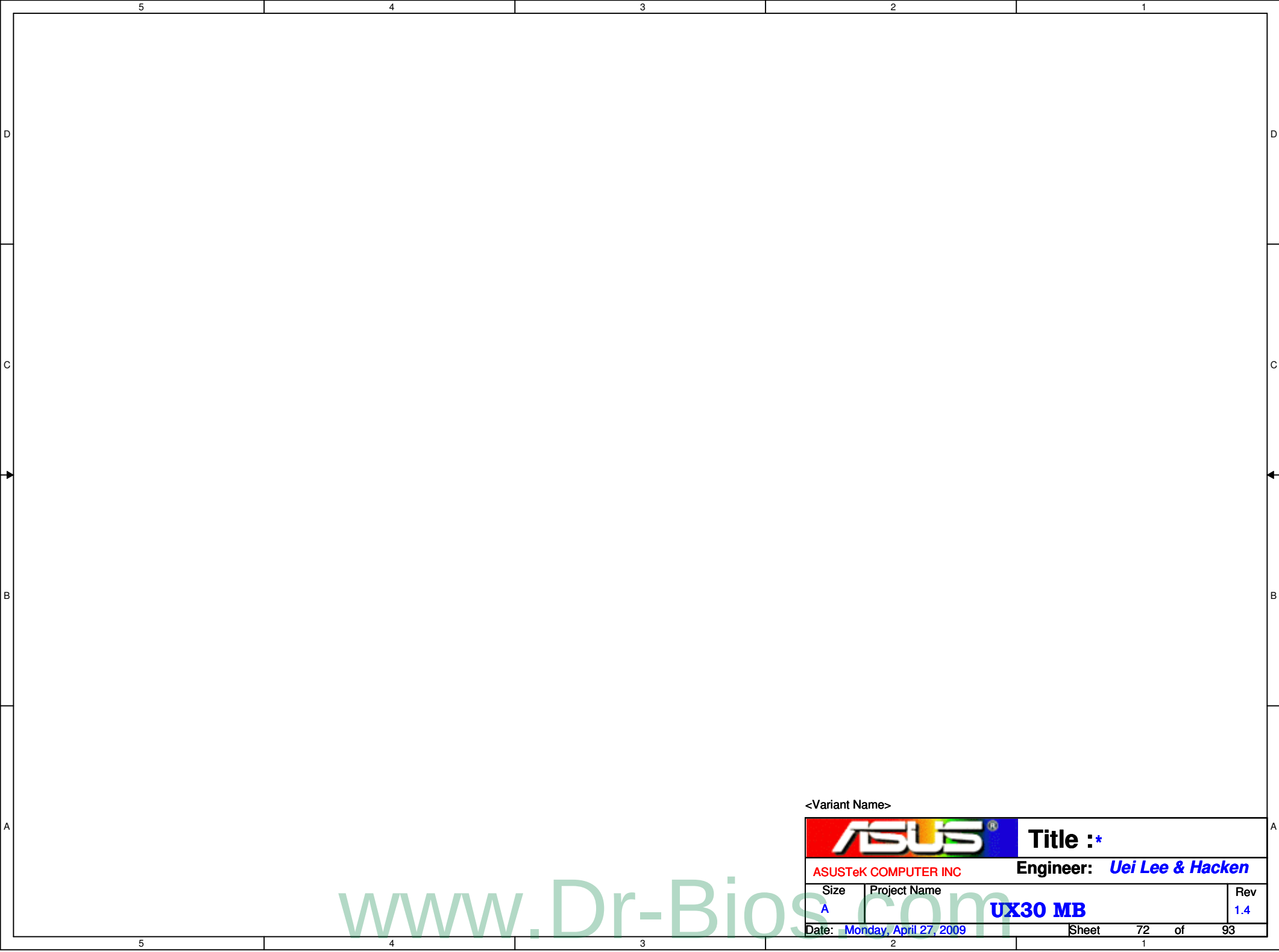
Date: Monday, April 27, 2009

Sheet

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<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	72 of 93

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D						D
C						C
B						B
A						A
	5	4	3	2	1	

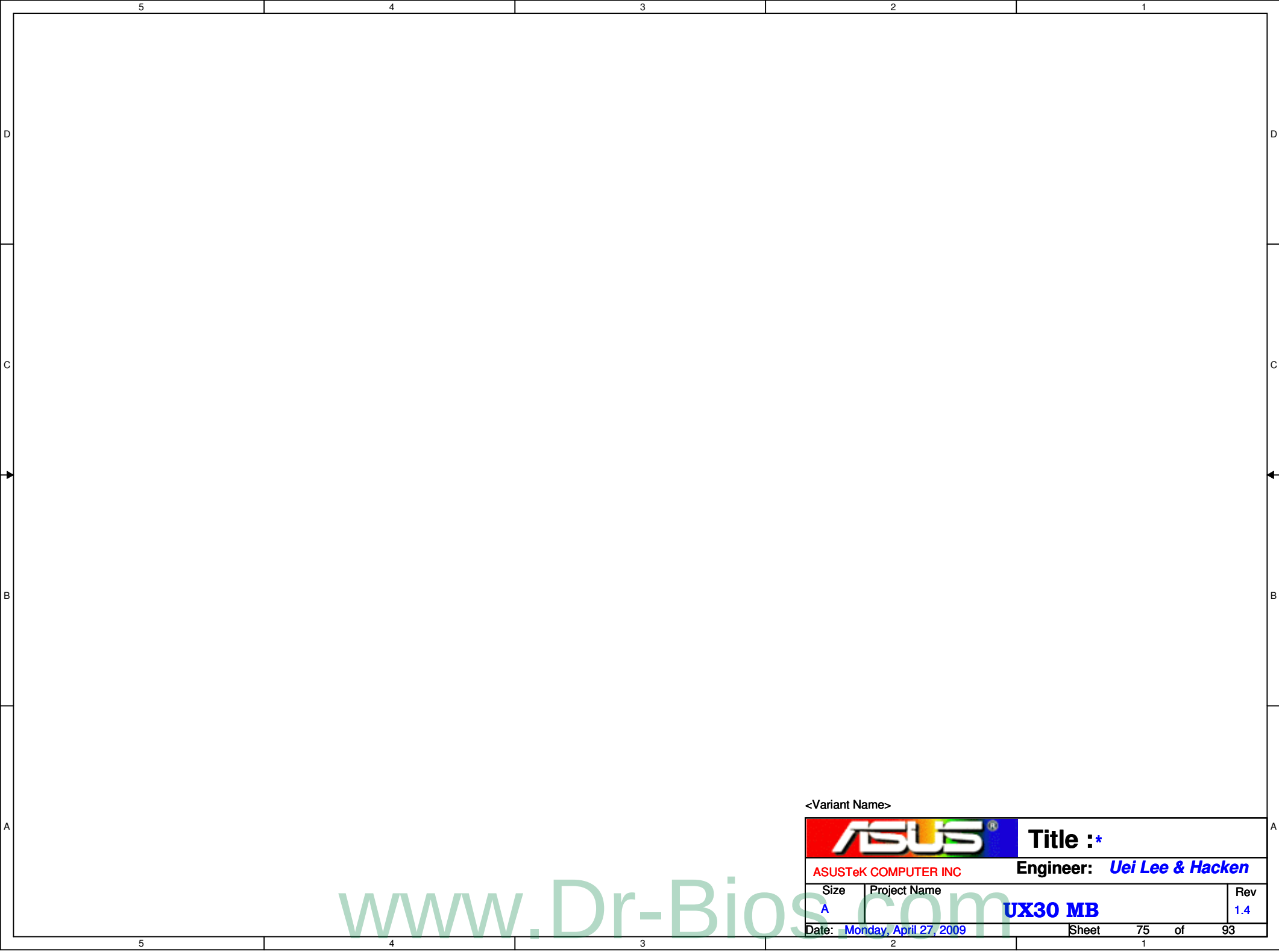
<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	73 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	74 of 93



<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	75 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	76 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	77 of 93

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

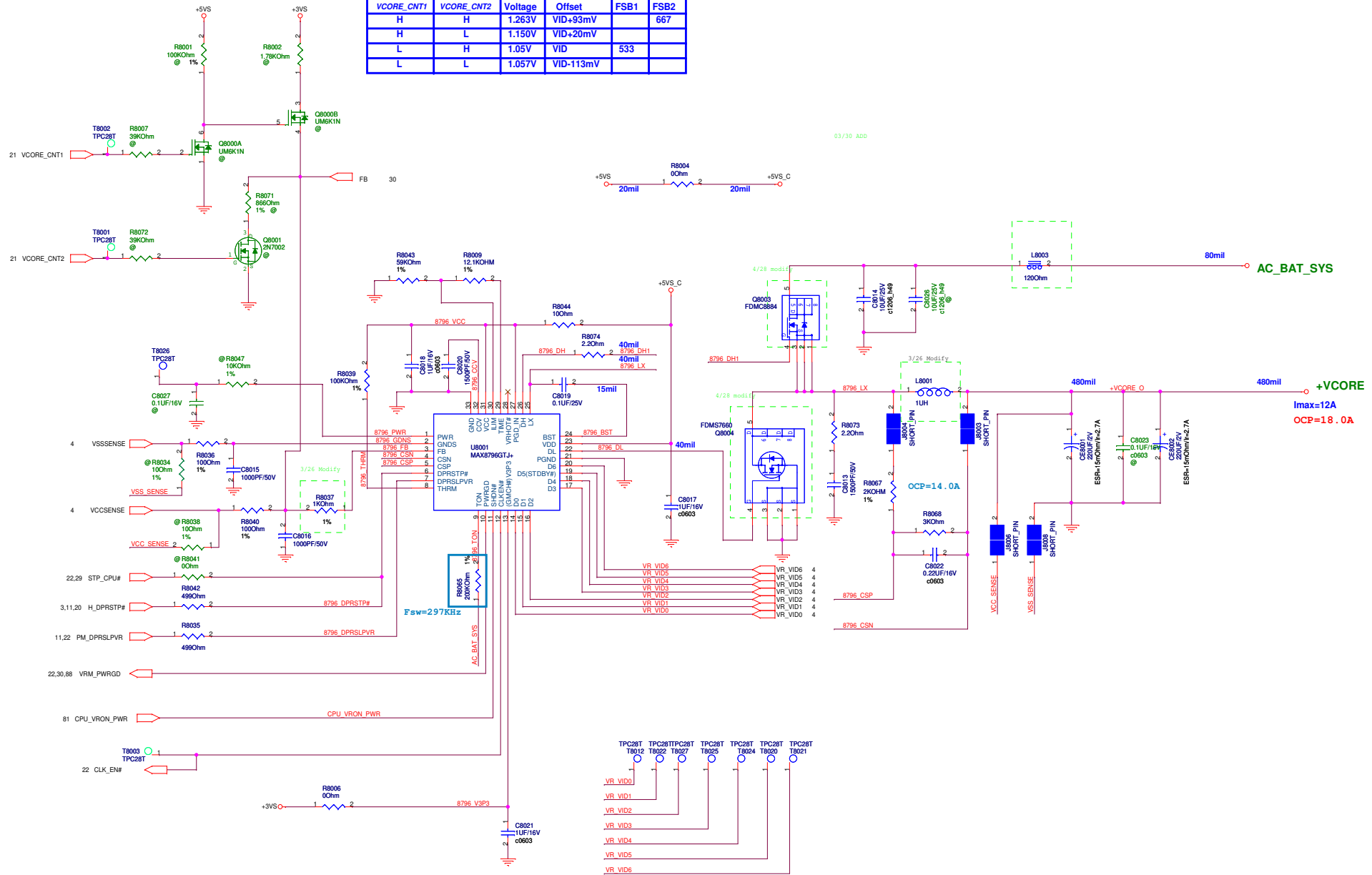
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ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	78 of 93

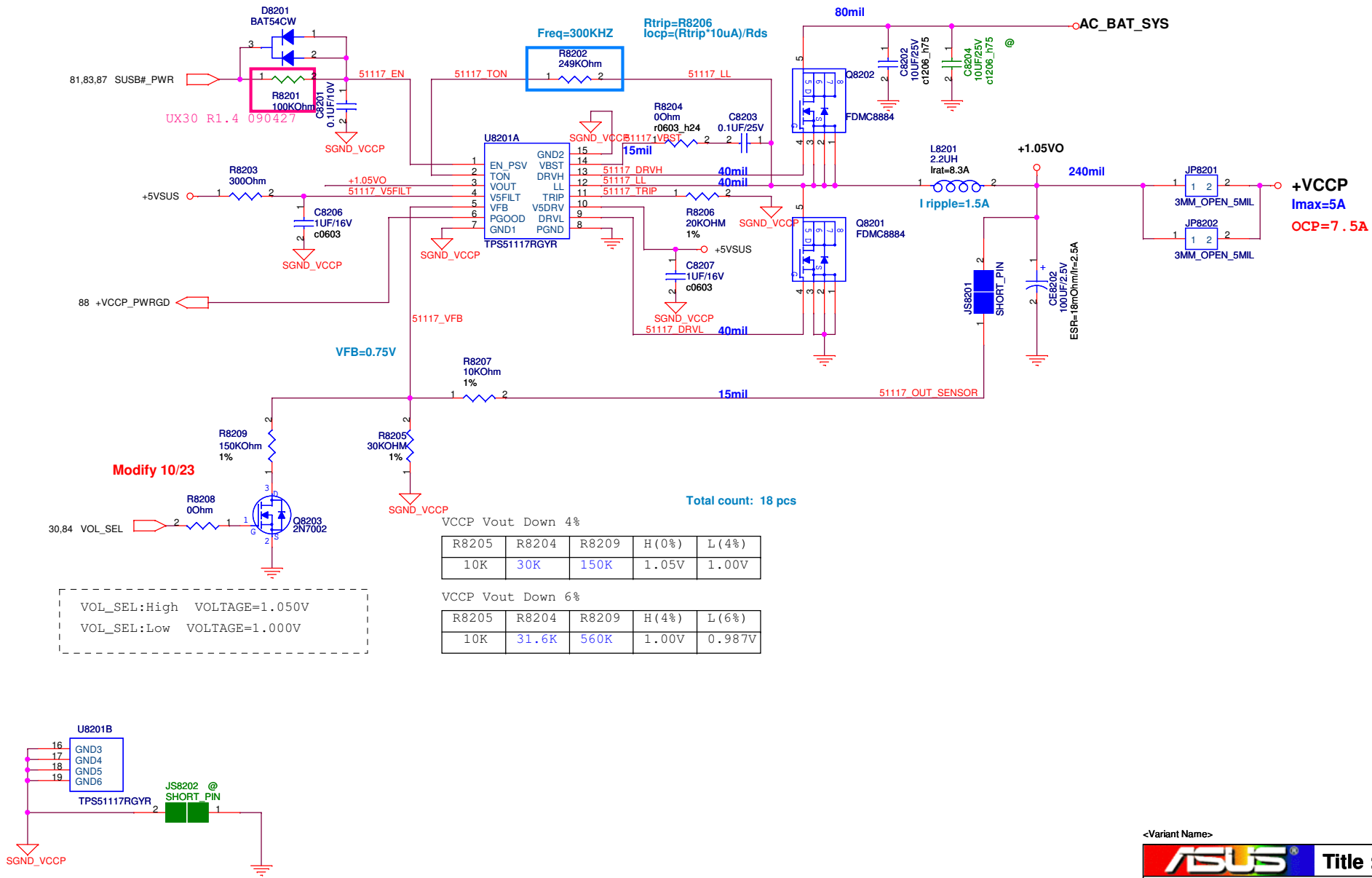
	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

<Variant Name>

		Title :*	
ASUSTeK COMPUTER INC		Engineer: <i>Uei Lee & Hacken</i>	
Size	Project Name		Rev
A	UX30 MB		1.4
Date: <i>Monday, April 27, 2009</i>		Sheet	79 of 93

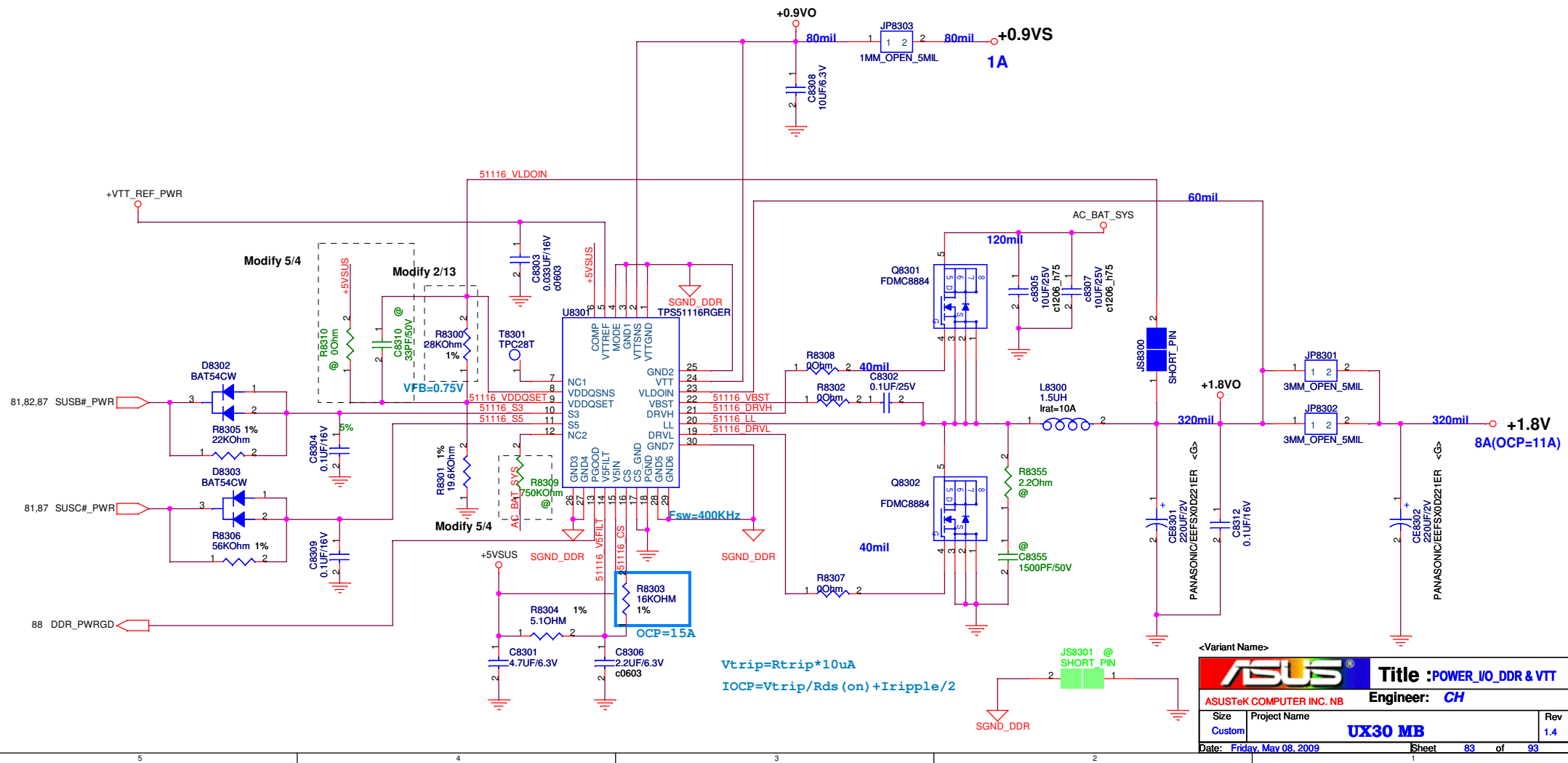
VCORE_CNT1	VCORE_CNT2	Voltage	Offset	FSB1	FSB2
H	H	1.263V	VID+93mV		667
H	L	1.150V	VID+20mV		
L	H	1.05V	VID	533	
L	L	1.057V	VID-113mV		





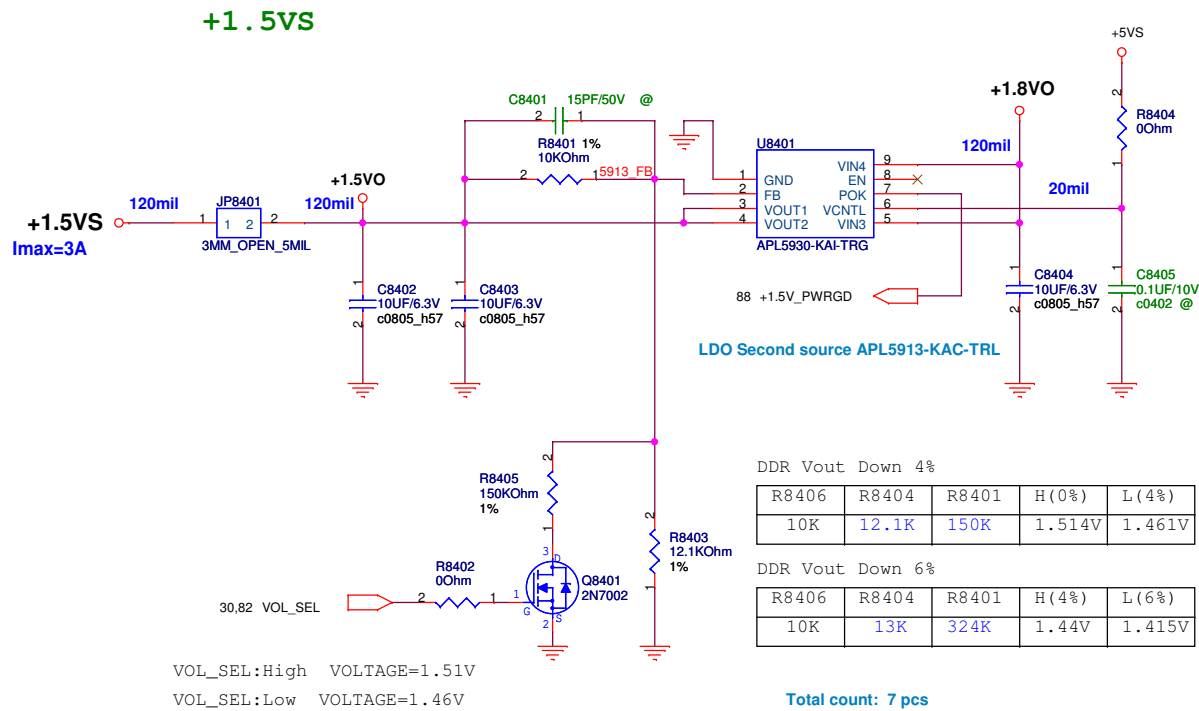
<Variant Name>

ASUS		Title :POWER_IO_+VCCP	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size B	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009		Sheet 82 of 93	



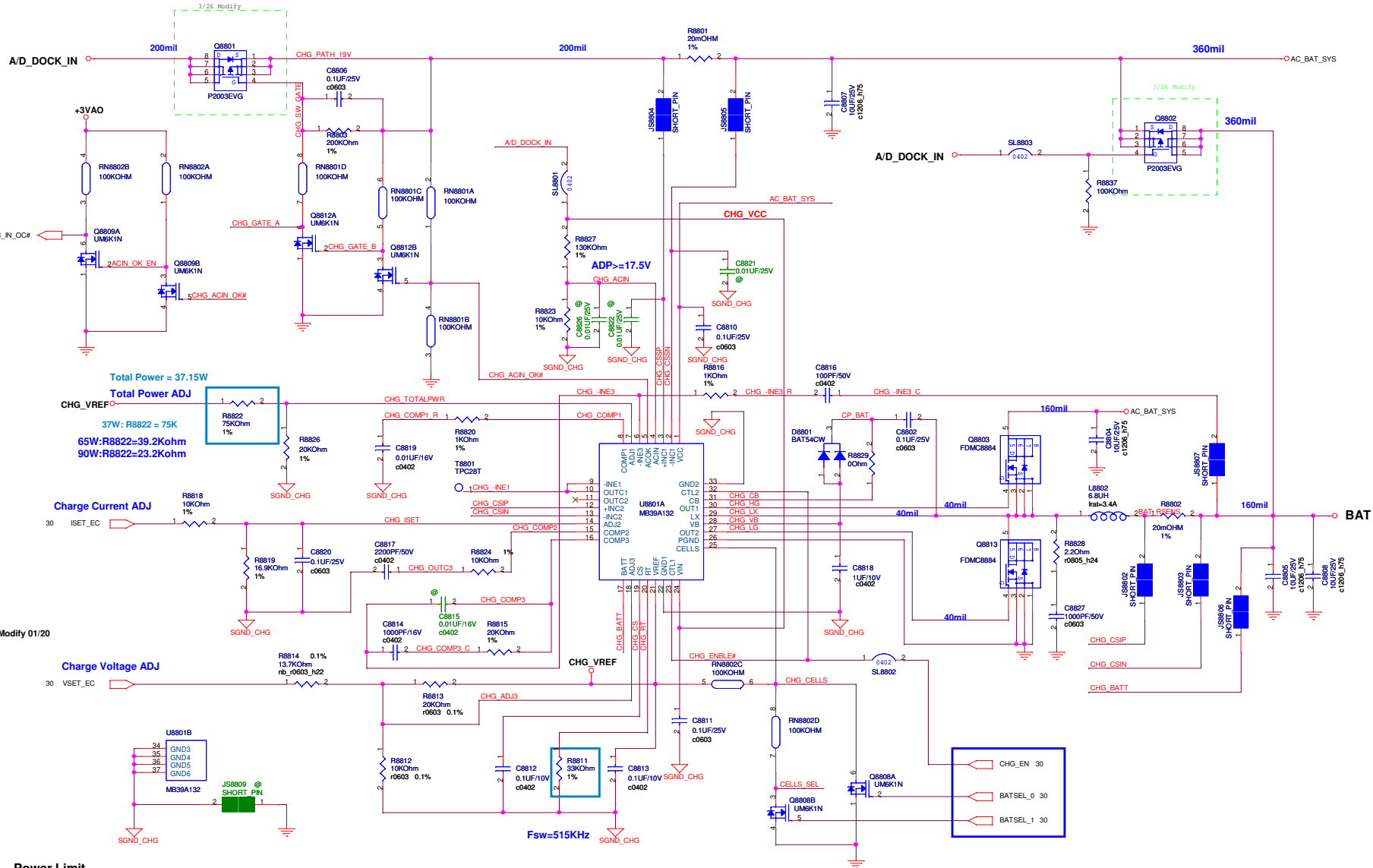
Total count: 29 pcs

ASUS Title : POWER_VO_DDR & VTT
ASUSTeK COMPUTER INC. NB Engineer: CH
Size Project Name
Custom **UX30 MB**
Date: Friday, May 08, 2009 Sheet 83 of 93



<Variant Name>

		Title : POWER_I/O_ +1.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size B	Project Name UX30 MB		Rev 1.4
Date: Friday, May 08, 2009	Sheet	84	of 93

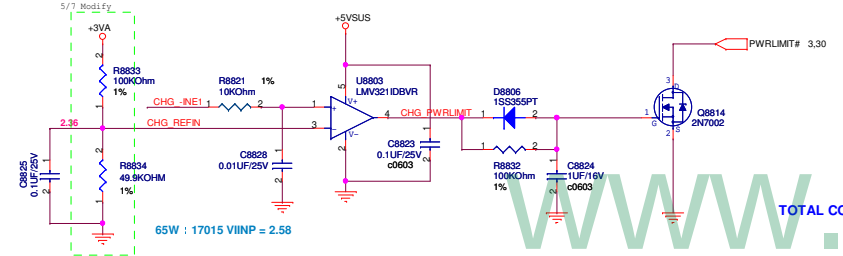


Total Power = 37.15W
 Total Power ADJ
 37W: R8822 = 75K
 65W: R8822 = 39.2Kohm
 90W: R8822 = 23.2Kohm

Charge Current ADJ
 ISET_EC

Charge Voltage ADJ
 VSET_EC

Power Limit
 Power Limit = 37.8W



BATTERY IN DETECT

<Variant Name>



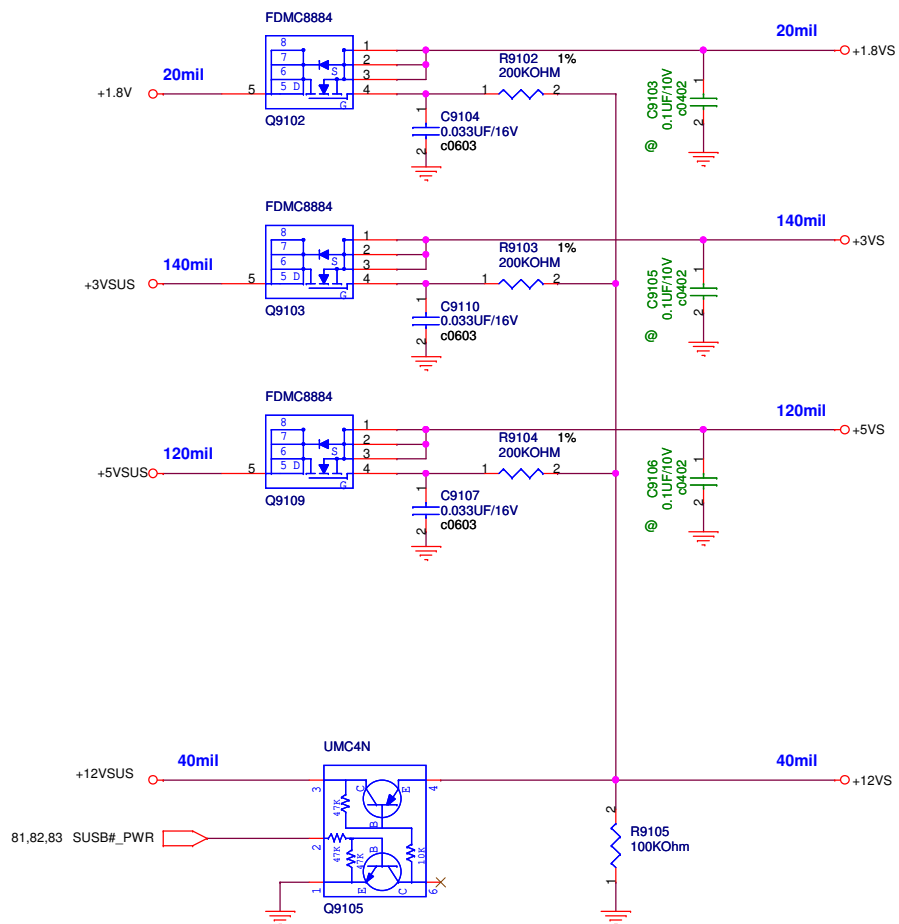
Title :POWER_DETECT

ASUSTeK COMPUTER INC. NB

Engineer: Aaron_Lin

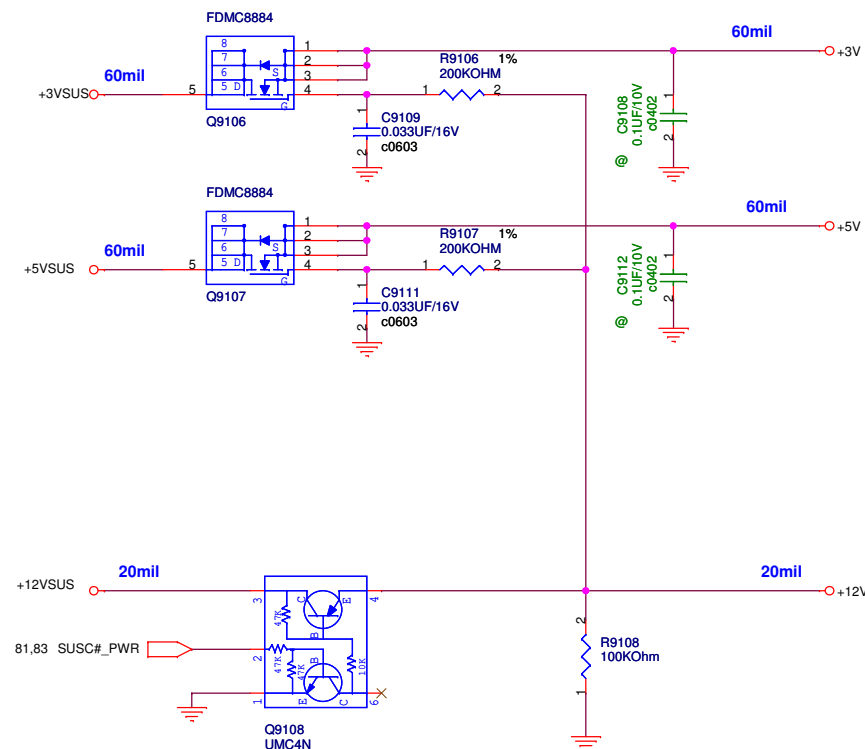
Size	Project Name	Rev
Custom	UX30 MB	1.4
Date: Friday, May 08, 2009		Sheet 86 of 93

SUSB#_PWR POWER



Total count: 19 pcs

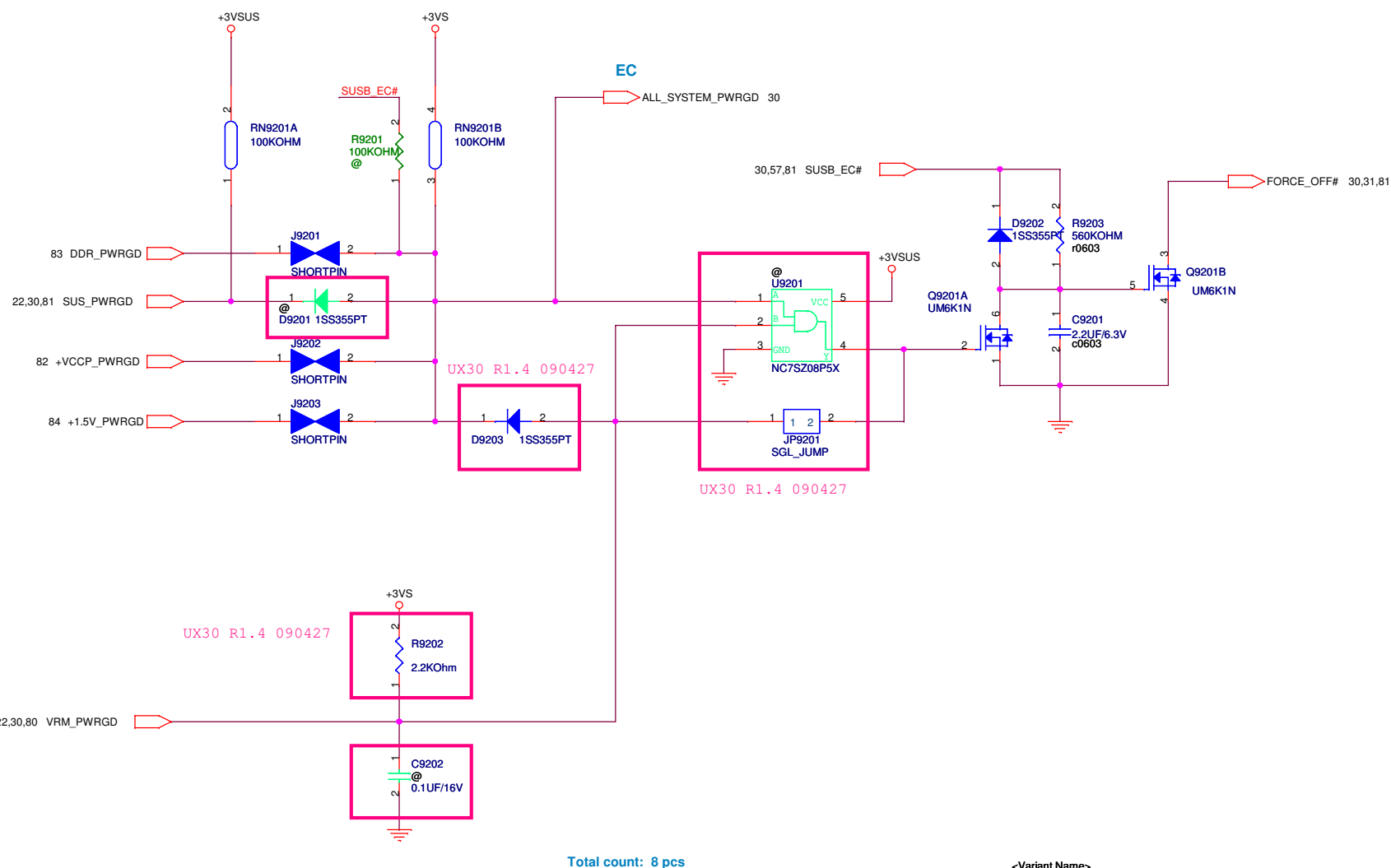
SUSC#_PWR POWER



<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Fred Shih	
Size B	Project Name UX30 MB	Rev 1.4	
Date: Friday, May 08, 2009	Sheet 87 of 93		

POWER GOOD DETECTOR



<Variant Name>		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size B	Project Name UX30 MB	Rev 1.4	
Date: Friday, May 08, 2009	Sheet 88 of 93		

AC_BAT_SYS ○ → AC_BAT_SYS 46,80,81,82,83,85
BAT ○ → BAT 60,85
BAT_CON ○ → BAT_CON 60,85

+3VAO ○ → +3VAO 81,85
+5VA ○ → +5VA 81
+3VA ○ → +3VA 20,30,56,81,85
+5VAO ○ → +5VAO 81
+5VO ○ → +5VO 81
+5VSUS ○ → +5VSUS 23,56,81,82,83,85,87
+5V ○ → +5V 52,57,68,87
+5VS ○ → +5VS 23,30,36,45,47,50,51,56,57,80,84,87
+3VO ○ → +3VO 81
+3VSUS ○ → +3VSUS 20,21,22,23,30,33,37,53,56,57,81,87,88
+3V ○ → +3V 21,33,42,46,53,57,61,67,87
+3VS ○ → +3VS 3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,57,80,87,88
+12VSUS ○ → +12VSUS 81,87
+12V ○ → +12V 37,87
+12VS ○ → +12VS 22,46,53,87
+1.8VO ○ → +1.8VO 83,84
+1.8V ○ → +1.8V 8,9,11,14,19,57,83,87
+1.8VS ○ → +1.8VS 15,87
+0.9VS ○ → +0.9VS 9,57,83
+0.9VO ○ → +0.9VO 83
+1.05VO ○ → +1.05VO 82
+VCCP ○ → +VCCP 3,4,5,10,11,12,14,15,20,23,57,82
+1.5VO ○ → +1.5VO 84
+1.5VS ○ → +1.5VS 4,15,20,23,36,37,53,57,84

+VCORE ○ → +VCORE 4,5,80

A/D_DOCK_IN ○ → A/D_DOCK_IN 60,85

Total sum count: 236 pcs

Modify 2/13

AC_BAT_SYS

40mil

www.Dr-Bios.com

<Variant Name>		
		Title : POWER_LED_VCC BOOST
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin
Size	Project Name	Rev
Custom	UX30 MB	1.4
Date: Friday, May 08, 2009		Sheet 91 of 93

E30 MB R1.1 Change List

1. Open Mask of JP3002 , JP3003 , JP8103 , JP8104 for SMT
2. Put on R2902 , C2913 , C2914 , JP3001 for SMT
3. Change R2911 from 22 Ohm to 10 Ohm for EA measure fail
4. Change R2910 from 22 Ohm to 10 Ohm and change net to CLK_SEL_48# for EA measure fail
5. Change Q4602 from SI3456BDV to SI3460BDV and add R4601 with 200K to GND for clear stocks
6. Change Q5302 from SI3456BDV to SI3460BDV and add R5307 with 200K to GND for clear stocks
7. Swap SL3621 and SL3622 for ACZ_Audio level change
8. Swap J4201 Pin 10 / 11 NET Name (SDCDN/XDWRN / SDWP/XDCLE/MSCLK) for SD Detection
9. Remove U3102 and C3105 for LID_SW# function for error design on MB
10. Add Q3704 and R3704 for Audio Level shift from +1.5VS to +3VS
11. Change BT Connector J6101 from 10 Pin to 6 Pin for N10 common use
12. Swap RTC Battery Connector CON2001 Pin Define for RTC common pin define
13. Change X3301 from 07G010S22500 to 07G010212502
14. Change R2904 , R2906 , R2907 from 22 Ohm to 10 Ohm for EA measure
15. Change J5601 from 6 pin to 8 pin and change pin define for PM spec change
16. Remove J4701 and related net for SR2 change
17. Change J3401 from 12G14830108D to 12G148611083 for ID design
18. Change J3701 , J3702 from 12G171030022 to 12G17100002C for Cost down
19. Change CON4601 from 12G170040308 to 12G170040308 for Cost down
20. Add H6530 for ME screw hole
21. Change J5604 from 12G171030140 to 12G171030121 for ID design
22. Remove J5603 , J6001 and change to J5602 on DC-IN BD for ME cost down
23. Change D3401 , D3402 , D5201 from 07G001250010 to 07G028075010 for EE Cost down
24. Change SL4602 to L4605 for EMI test
25. Add L8003 for EMI test
26. Delete Num_LED# function for Spec change

		Title : HISTORY	
<OrgName>		Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB		Rev 1.4
Date: Monday, April 27, 2009		Sheet 92	of 93

UX30 MB R1.4 Change List

- 1. Swap USB D+ , D- of BT on Page 61
- 2. Add C4710 , R4704 and C4711 , R4705 on Hsync and Vsync to improve CRT display quality on Page 47
- 3. Modify J5602 Pin 1 , 3 , 5 , 7 to GND for Apater use on Page 56
- 4. Change J6801 from 12G183402207 to 12G18340200T for cost down on Page 68
- 5. Change J5604 Pin 10 from +3VSUS to +3VA for Hall sensor on Page 56
- 6. Change H6501 from Screw Hole to a NUT for ME assembly on Page 65
- 7. Change PCB ID from R1.1 to R1.4 on Page 22
- 8. Add R2229 , R2231 on GPIO6 for On Board Memory Size and R2231 , R2232 on GPIO7 for Memory Vendor on Page 22
- 9. Change J5301 from 12G03010052K to 12G03010052P on Page 53
- 10. Change J0801 from 12G02502200F to 12G02502200S on Page 8
- 11. Change U3601 from 02G611005001 to 02G611005006 on Page 36

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