

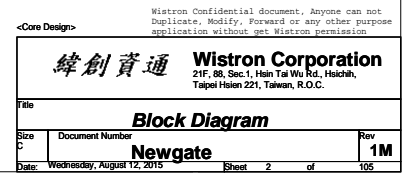
*Newgate*

*Schematics Document*

<Core Design>

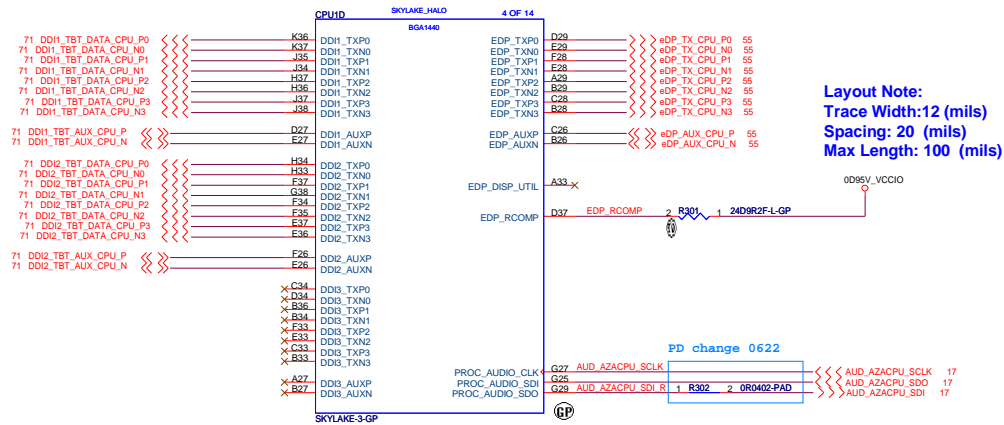
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Title			
<div>Cover Page</div>			
Size A	Document Number		Rev
	<div>Newgate</div>		<div>1M</div>
Date:	Wednesday, August 12, 2015	Sheet 1 of	105

**Project code : 4PD06A010001**  
**PCB P/N : 14307**  
**Revision : 1M**

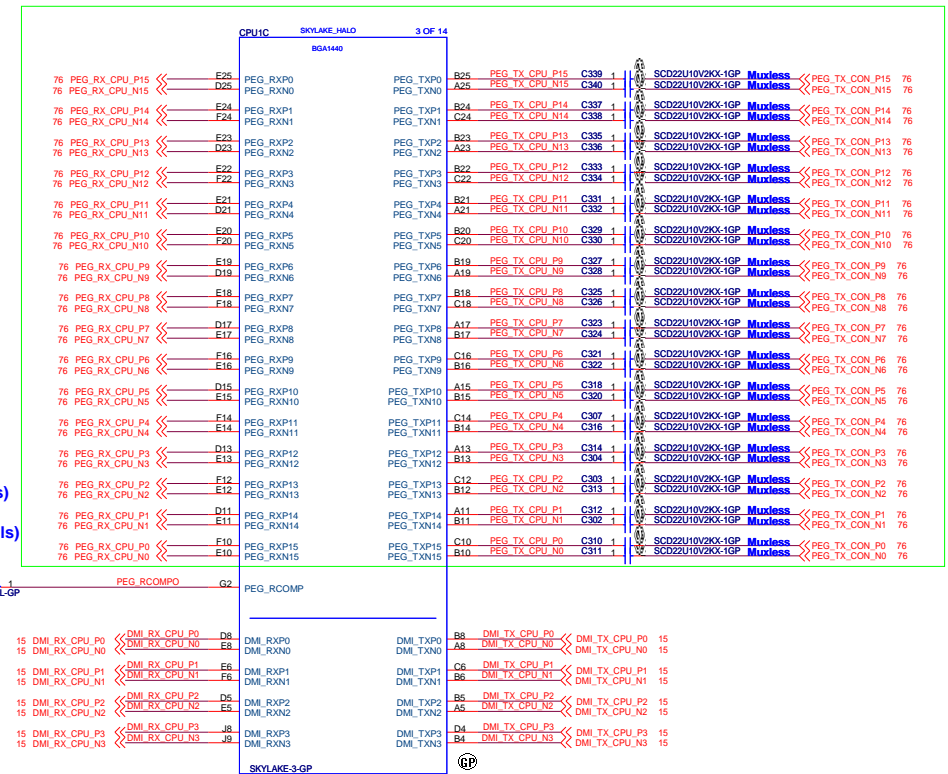
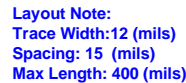


**SSID = CPU**

Royce 20150205 REVERSE PEG BUS for layout issue



**Layout Note:**  
Trace Width: 12 (mils)  
Spacing: 20 (mils)  
Max Length: 100 (mils)



&lt;Core Design&gt;

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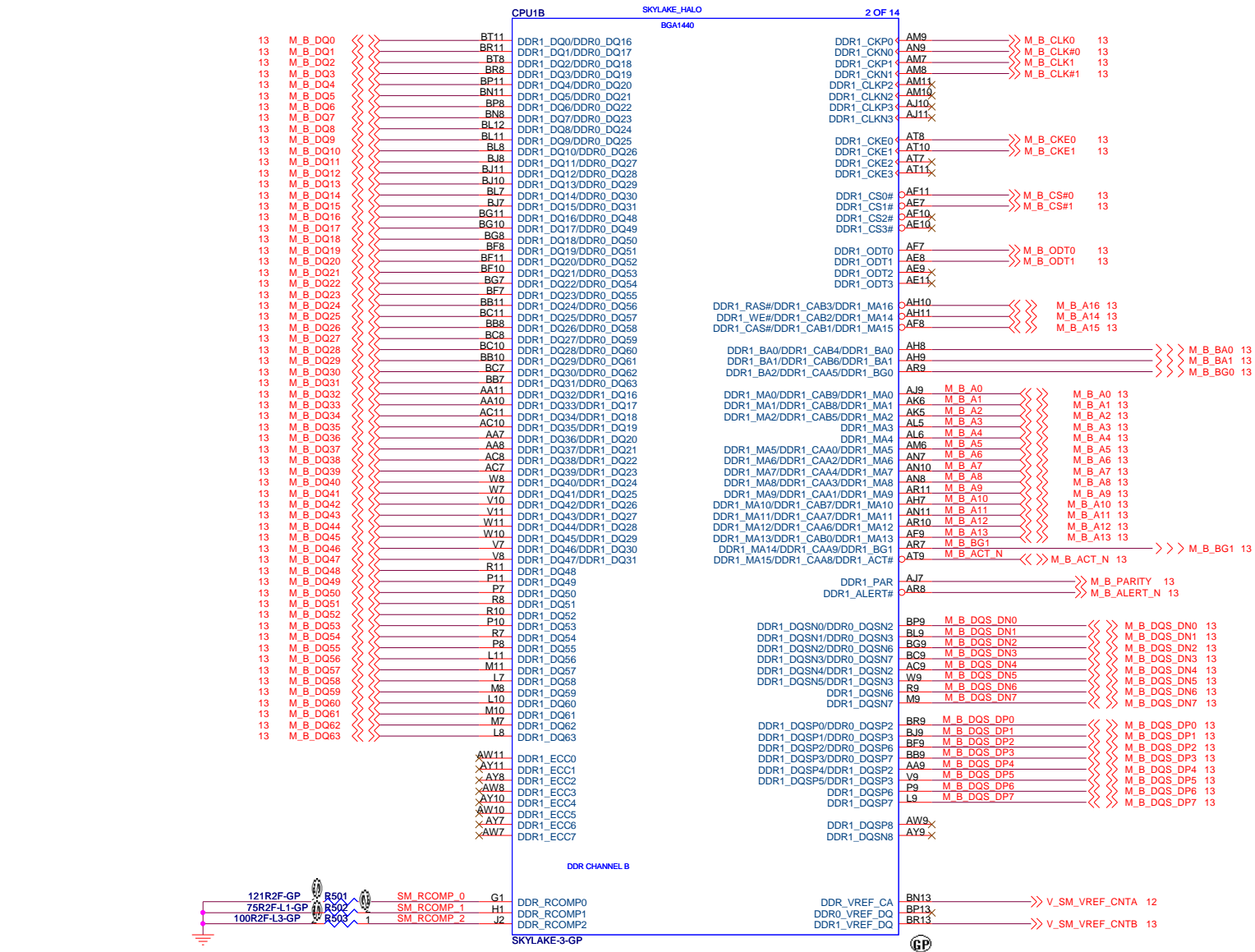
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Size	Document Number		Rev
Custom	<b>Newgate</b>		<b>SA</b>
Date:	Tuesday, August 18, 2015	Sheet 3 of	105



Title			
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Size A3	Document Number		Rev
	<b>Newgate</b>		<b>1M</b>
Date:	Tuesday, August 18, 2015	Sheet 4 of	105

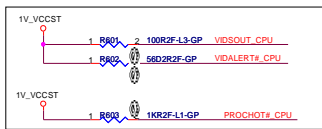


SSID = CPU



# AROUND\_CPU

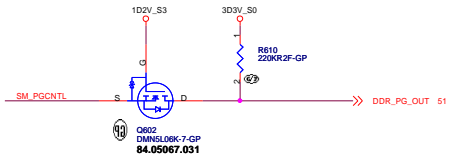
SSID = CPU



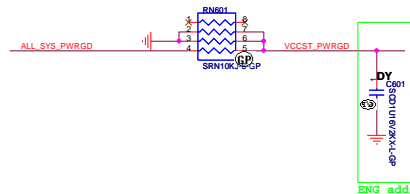
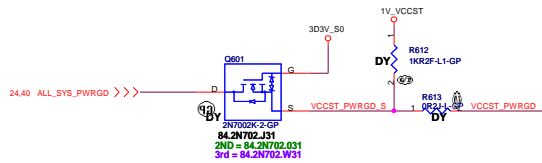
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18 PCH\_CPU\_P0BCLK\_R\_DP >>>  
18 PCH\_CPU\_P0BCLK\_R\_DN >>>  
18 PCH\_CPU\_NSSC\_CLK\_DP >>>  
18 PCH\_CPU\_NSSC\_CLK\_DN >>>

46 VIDALERT#\_CPU >>>  
46 VIDSCK\_CPU >>>  
46 VIDSOUT\_CPU >>>  
24,44,46 PROCHOT#\_CPU >>>

17,89 H\_PWRGD >>>  
16 PLTRST# >>>  
16 H\_PM\_SYNC >>>  
16 H\_PM\_DOWN >>>  
16 PCH\_PECI >>>  
16 H\_THERMTRIP# >>>



UN 0225



ENG add cap 0427

PEG Static Lane Reversal	
CFG2	1: Normal Operation: Lane # definition matches socket pin map definition 0: Lane Reversed

eDP Enable	
CFG4	1: Disable 0: Enable

PEG Training	
CFG7	1: (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled / function 2 disabled 01: Reserved - (Device 1 function 1 disabled / function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of "1" if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li>• <b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> <li>- 1 = (Default) Normal Operation; No stall.</li> <li>- 0 = Stall.</li> </ul> </li> <li>• <b>CFG[1]:</b> Reserved configuration lane.</li> <li>• <b>CFG[2]:</b> PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> <li>- 1 = Normal operation</li> <li>- 0 = Lane numbers reversed.</li> </ul> </li> <li>• <b>CFG[3]:</b> Reserved configuration lane.</li> <li>• <b>CFG[4]:</b> eDP enable: <ul style="list-style-type: none"> <li>- 1 = Disabled.</li> <li>- 0 = Enabled.</li> </ul> </li> <li>• <b>CFG[6:5]:</b> PCI Express* Bifurcation <ul style="list-style-type: none"> <li>- 00 = 1 x8, 2 x4 PCI Express*</li> <li>- 01 = reserved</li> <li>- 10 = 2 x8 PCI Express*</li> <li>- 11 = 1 x16 PCI Express*</li> </ul> </li> <li>• <b>CFG[7]:</b> PEG Training: <ul style="list-style-type: none"> <li>- 1 = (default) PEG Train immediately following RESET# de assertion.</li> <li>- 0 = PEG Wait for BIOS for training.</li> </ul> </li> <li>• <b>CFG[19:8]:</b> Reserved configuration lanes.</li> </ul>	I/O	GTL	SE	All processor lines. CFG[2], CFG[6-5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

## Processor Internal Pull-Up / Pull-Down Terminations

### Processor Internal Pull-Up / Pull-Down Terminations

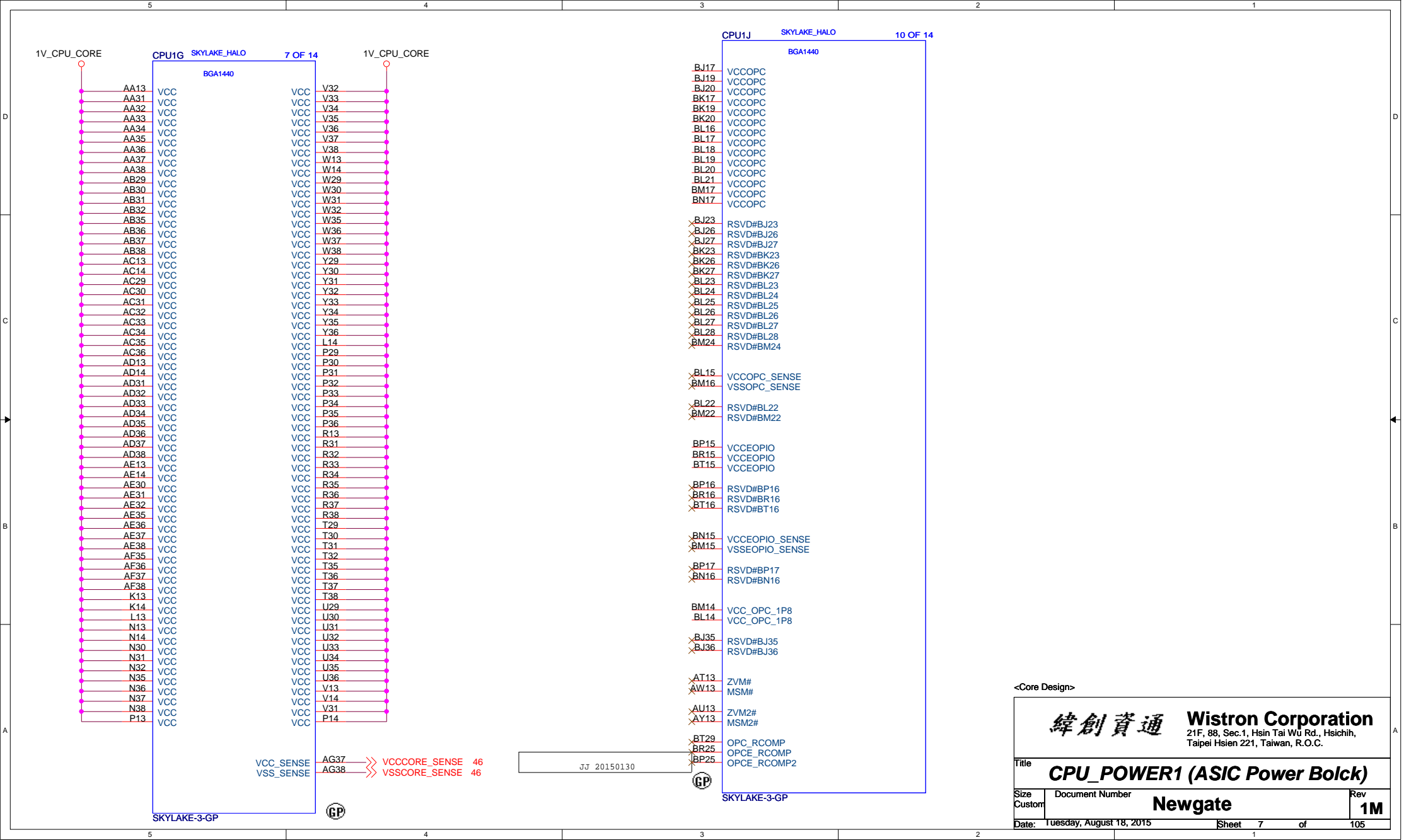
Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC <sub>IO</sub>	16-60 Ω
PREQ#	Pull Up	VCC <sub>ST</sub>	3 kΩ
PROC_TDI	Pull Up	VCC <sub>ST</sub> <sup>1</sup>	3 kΩ
PROC_TMS	Pull Up	VCC <sub>ST</sub> <sup>1</sup>	3 kΩ
CFG[19:0]	Pull Up	VCC <sub>IO</sub>	3 kΩ

#### Note:

1. For SKL-S it should be VCC<sub>ST</sub>

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CPU_CFG_CFG STRAP	
File	Rev
Size	Document Number
A2	1M
Date:	10/25/2015, August 18, 2015
Sheet	6 of 106



<Core Design>

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Title

CPU\_POWER1 (ASIC Power Bolck)

Size Custom

Document Number

Rev

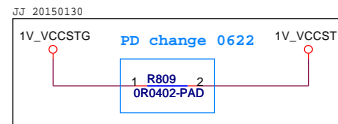
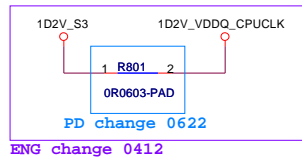
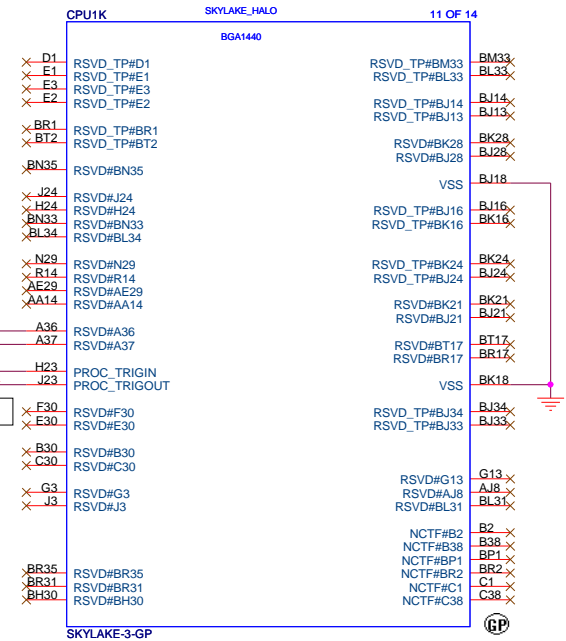
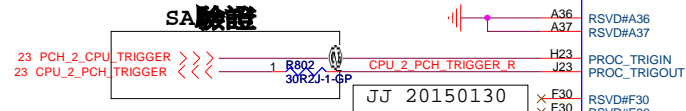
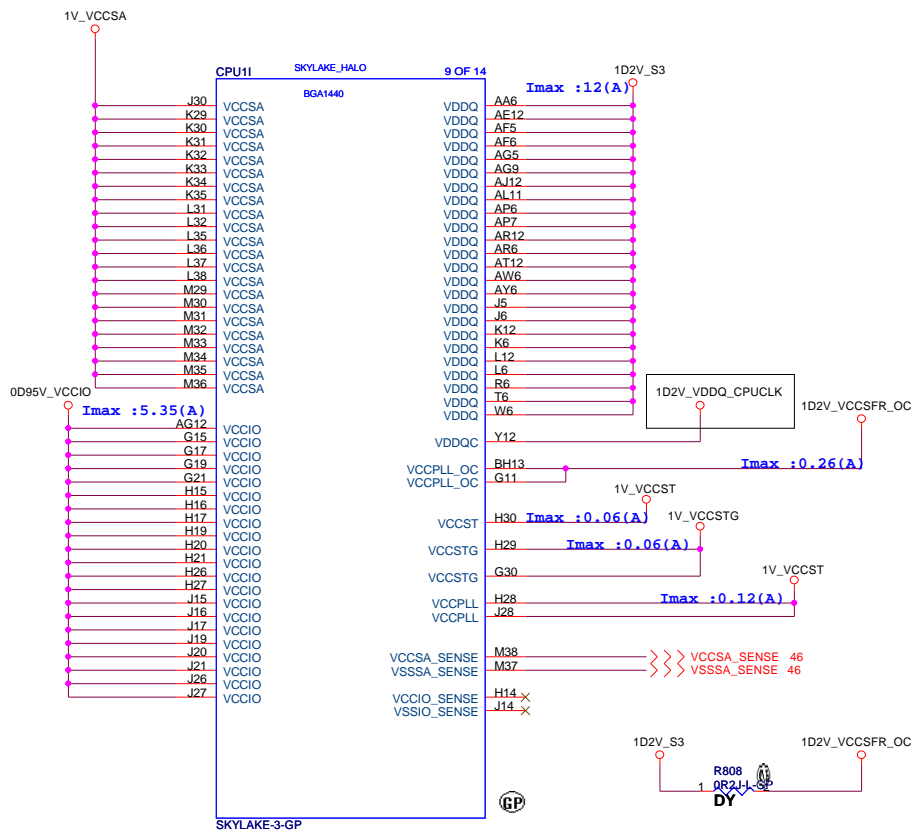
Newgate

1M

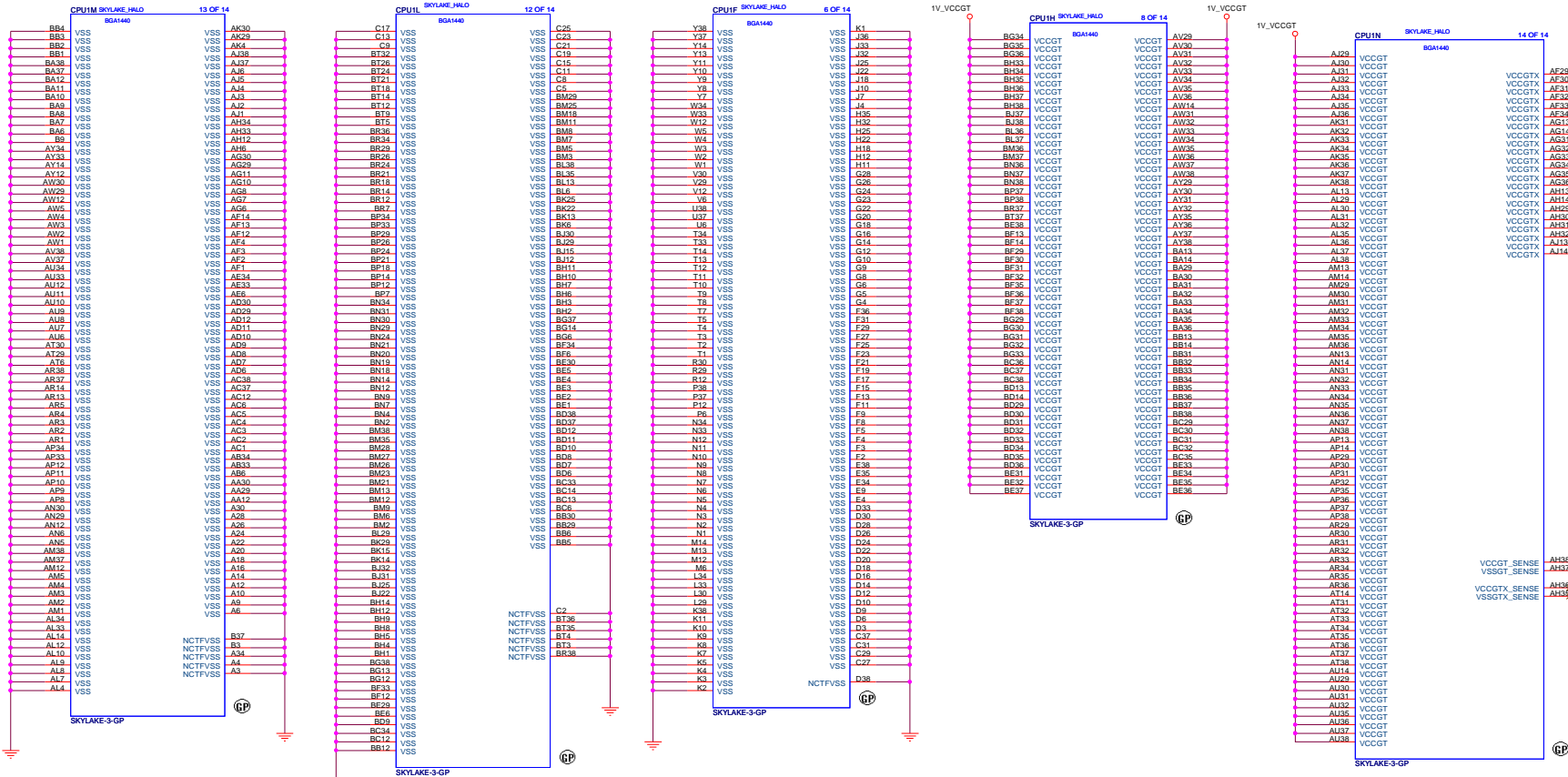
Date: Tuesday, August 18, 2015

Sheet 7 of 105

SSID = CPU



SSID = CPU



<Core Design>

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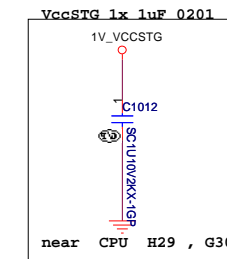
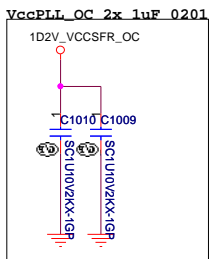
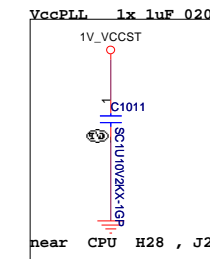
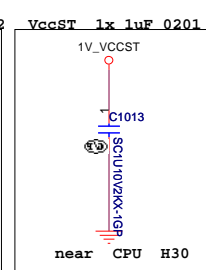
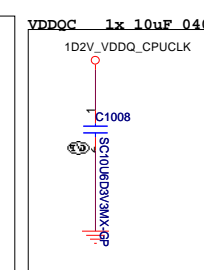
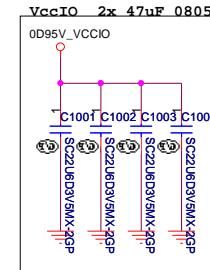
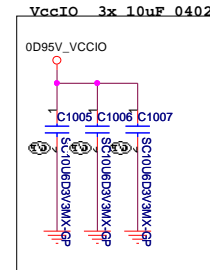
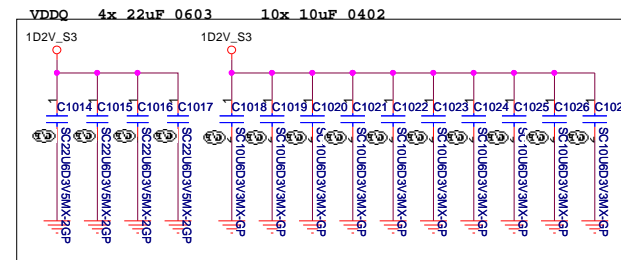
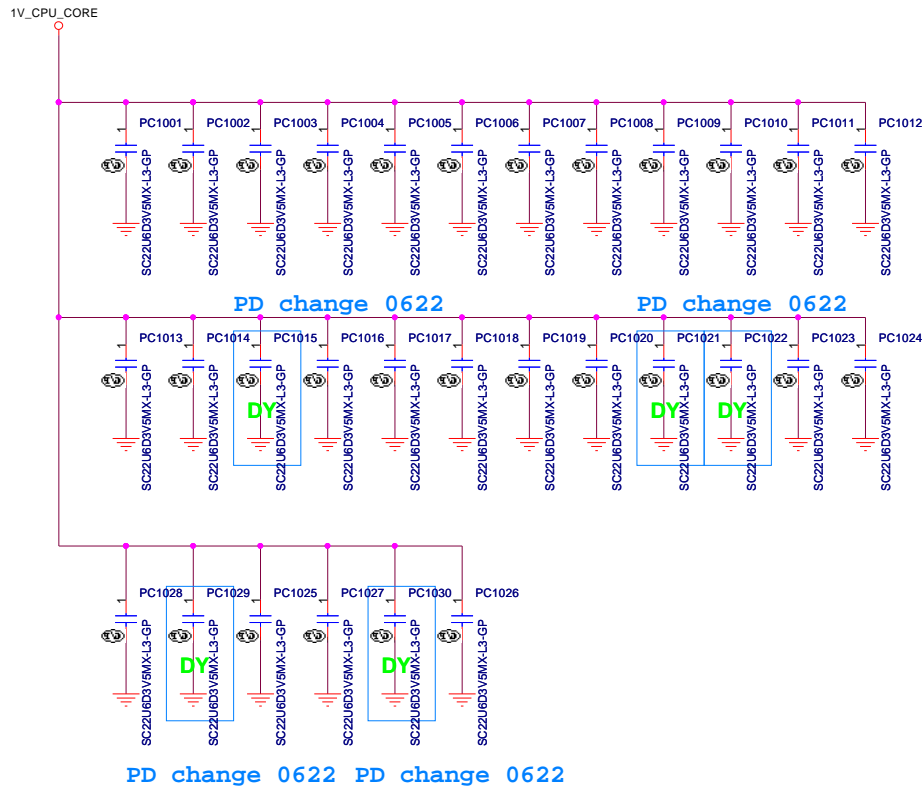
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File CPU\_POWER3(ASIC Power Bolck)

Size Document Number Newgate Rev 1M

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JJ 20150130

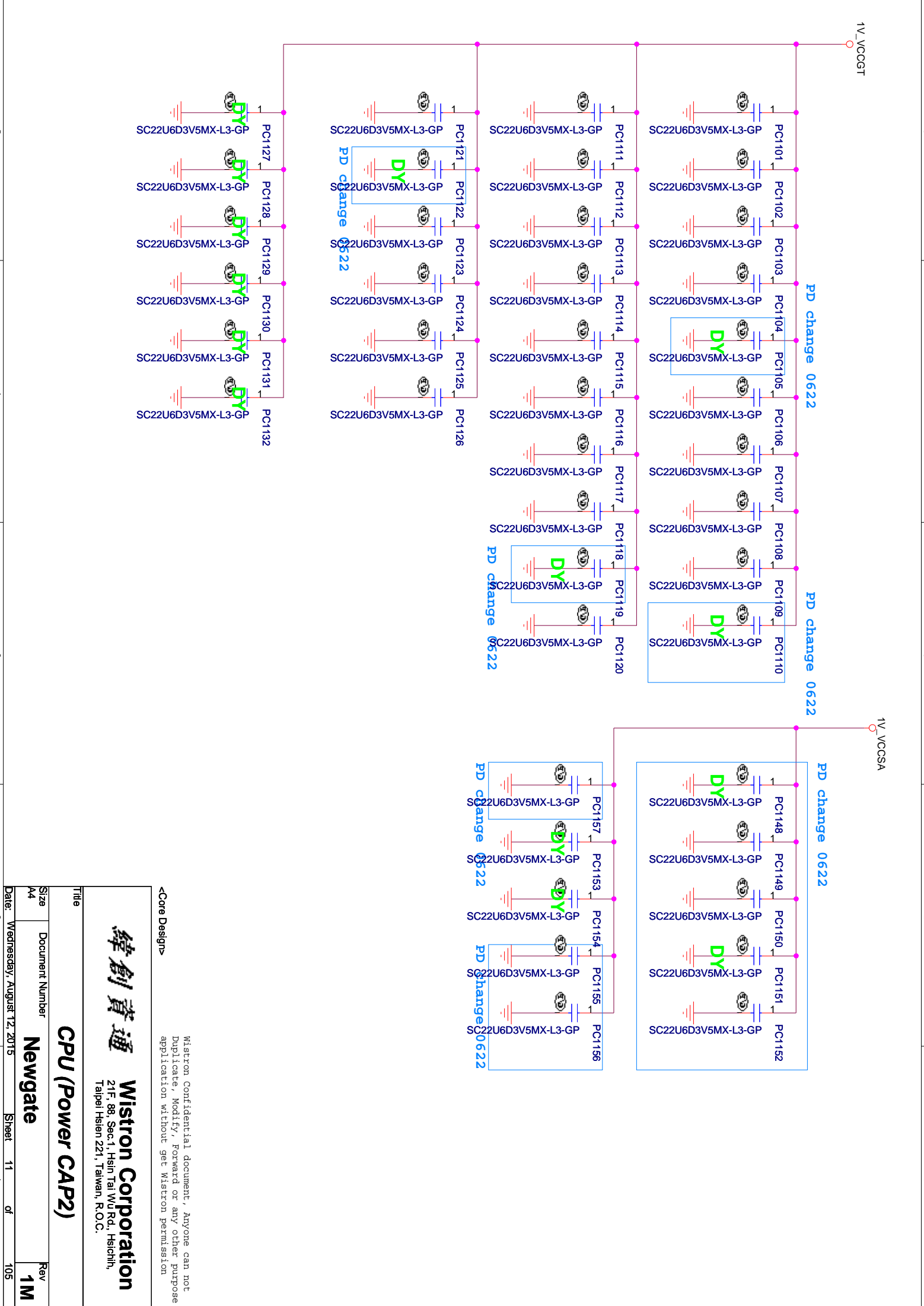
# Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
VccGT	6x 47uF 0805	8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
VccTx	8x 22uF 0603	4x 10uF 0402	
		12x 1uF 0201	
VccSA	1x 47uF 0805	1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
		4x 22uF 0603	Share supply with DRAM
VDDQ		10x 10uF 0402	
VDDQC		1x 10uF 0402	
VccIO	2x 47uF 0805	3x 10uF 0402	VR: +/-5% or +/-50mV Place close to VR output
VccST		1x 1uF 0201	
VccSTG		1x 1uF 0201	Share supply with 1.0V PCH rail
VccPLL		1x 1uF 0201	
VccPLL_OC		2x 1uF 0201	Supply from 1.2V VDDQ
VccCore		10x 10uF 0402	VR: +/-5% or +/-50mV
VccpPrio		3x 10uF 0402	VR: +/-5% or +/-50mV

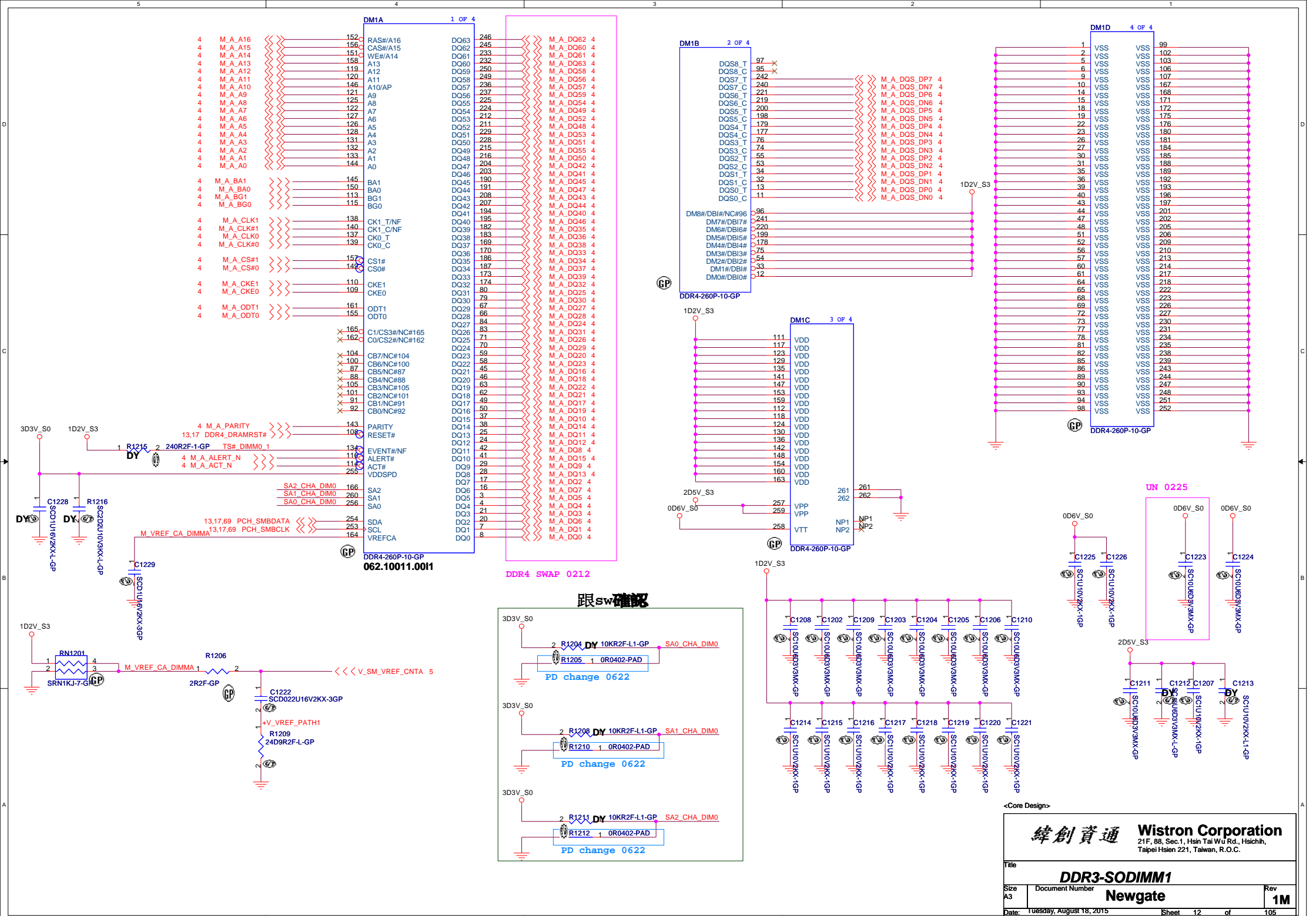
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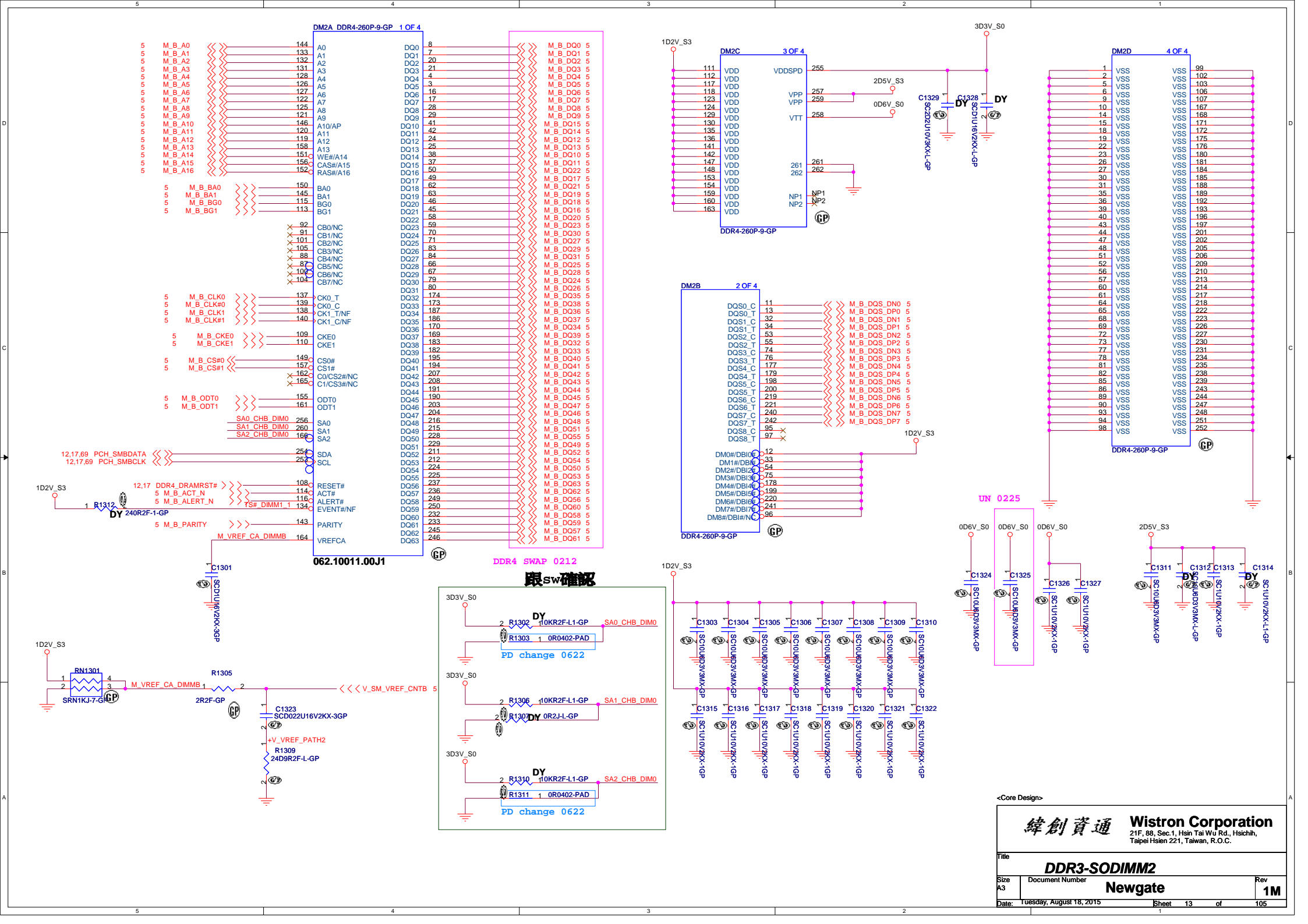
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010 CPU (Power CAP1)		
Size	Document Number	Rev
A3	Newgate	1M
Date:	Wednesday, August 12, 2015	Sheet 10 of 105

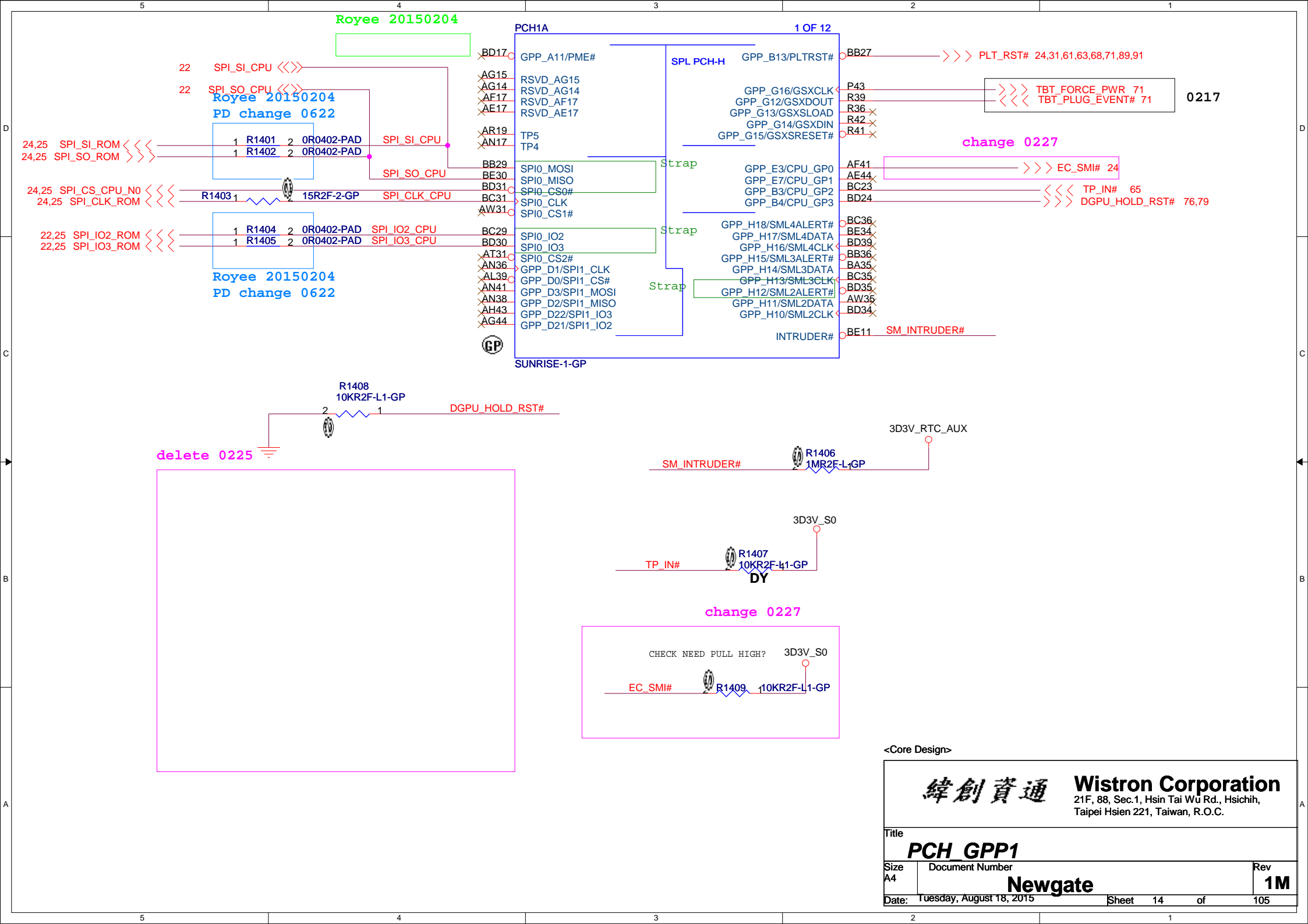


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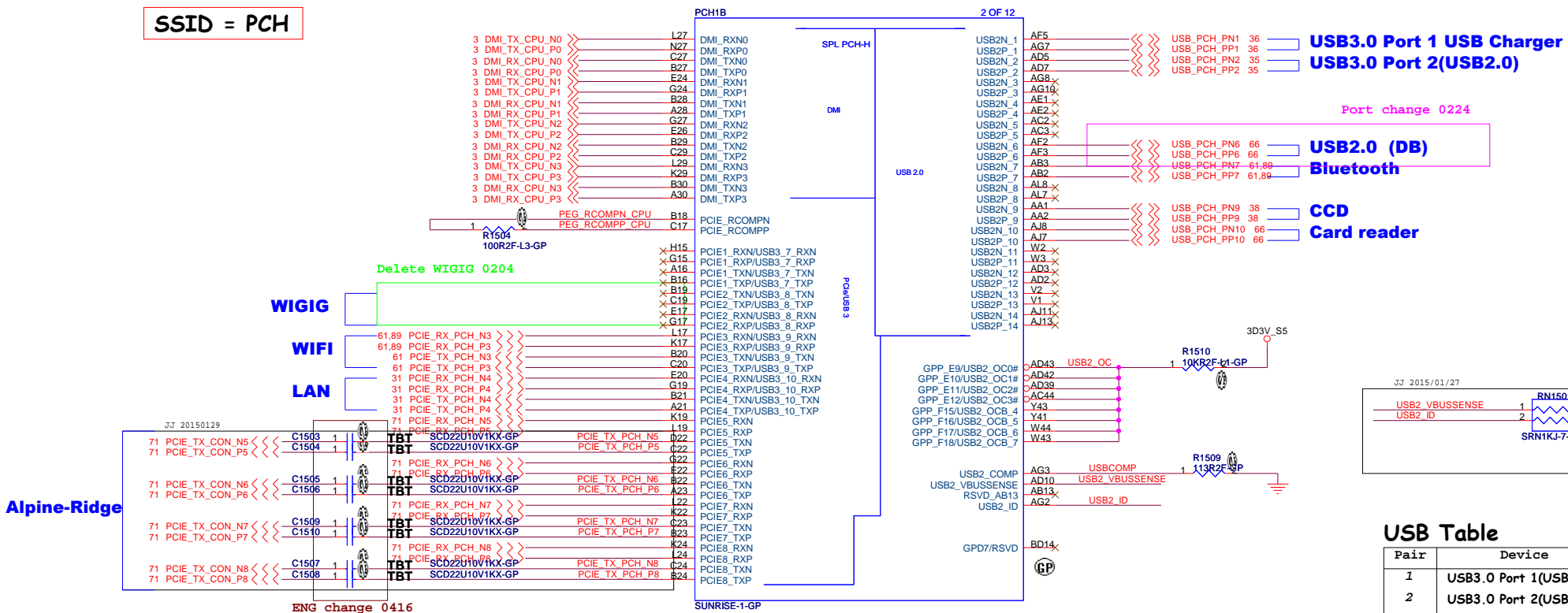








SSID = PCH



## USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

<Core Design>

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No.	Title	Date	Page
1	...	...	...
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**PCH PCIE DMI USB**

Size	A3
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Document Number

**Newgate**

Rev	1M
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Date: Tuesday, August 18, 2015

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SSID = PCH

Delete WIGIG 0204

change 0227

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38 FW\_GPIO <<<

MSATA

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63 PCIE\_TX\_PCH\_N11 <<<  
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63 PCIE\_RX\_PCH\_N11 <<<

MSATA

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63 PCIE\_RX\_PCH\_N12 <<<

UN 0225

PCH1C

3 OF 12

AV2 CL\_CLK  
AV3 CL\_DATA  
AW2 CL\_RST#

CLINK

SPL PCH-H

R44 GPP\_G8/FAN\_PWM\_0  
R43 GPP\_G9/FAN\_PWM\_1  
U39 GPP\_G10/FAN\_PWM\_2  
N42 GPP\_G11/FAN\_PWM\_3

FAN

U43 GPP\_G0/FAN\_TACH\_0  
U42 GPP\_G1/FAN\_TACH\_1  
U41 GPP\_G2/FAN\_TACH\_2  
M44 GPP\_G3/FAN\_TACH\_3  
U36 GPP\_G4/FAN\_TACH\_4  
P44 GPP\_G5/FAN\_TACH\_5  
T45 GPP\_G6/FAN\_TACH\_6  
T44 GPP\_G7/FAN\_TACH\_7

B33 PCIE11\_TXP  
C33 PCIE11\_TXN  
K31 PCIE11\_RXP  
L31 PCIE11\_RXN

AB33 GPP\_F10/SCLOCK  
AB35 GPP\_F11/SLOAD  
AA44 GPP\_F13/SDATAOUT0  
AA45 GPP\_F12/SDATAOUT1

B38 PCIE14\_TXN/SATA1B\_TXN  
C38 PCIE14\_TXP/SATA1B\_TXP  
D39 PCIE14\_RXN/SATA1B\_RXN  
E37 PCIE14\_RXP/SATA1B\_RXP

C36 PCIE13\_TXN/SATA0B\_TXN  
B36 PCIE13\_TXP/SATA0B\_TXP  
G35 PCIE13\_RXN/SATA0B\_RXN  
E35 PCIE13\_RXP/SATA0B\_RXP

A35 PCIE12\_TXP  
B35 PCIE12\_TXN  
H33 PCIE12\_RXP  
G33 PCIE12\_RXN

J45 PCIE20\_TXP  
K44 PCIE20\_TXN  
N38 PCIE20\_RXP  
N39 PCIE20\_RXN  
H44 PCIE19\_TXP  
H43 PCIE19\_TXN  
L39 PCIE19\_RXP  
L37 PCIE19\_RXN

SUNRISE-1-GP

HOST

PCIE9\_RXN/SATA0A\_RXN  
PCIE9\_RXP/SATA0A\_RXP  
PCIE9\_TXN/SATA0A\_TXN  
PCIE9\_TXP/SATA0A\_TXP

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GPP\_E0/SATAXPCIE0/SATAGP0  
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GPP\_F0/SATAXPCIE3/SATAGP3  
GPP\_F1/SATAXPCIE4/SATAGP4  
GPP\_F2/SATAXPCIE5/SATAGP5  
GPP\_F3/SATAXPCIE6/SATAGP6  
GPP\_F4/SATAXPCIE7/SATAGP7

GPP\_F21/EDP\_BKLTCTL  
GPP\_F20/EDP\_BKLTEN  
GPP\_F19/EDP\_VDDEN

THERMTRIP#  
PECI  
PM\_SYNC  
PLTRST\_CPU#  
PM\_DOWN

G31  
H31  
C31  
B31

G29  
E29  
C32  
B32

F41  
E41  
B39  
A39

D43  
E42  
A41  
A40

H42  
H40  
E45  
F45

K37  
G37  
G45  
G44

AD44

AG36  
AG35  
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AD35  
AD31  
AD38  
AC43  
AB44

W36  
W35  
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AJ3

AL3

AK2

AH2

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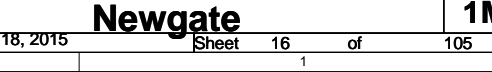
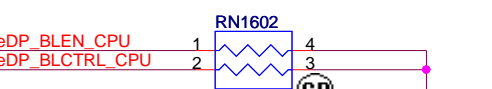
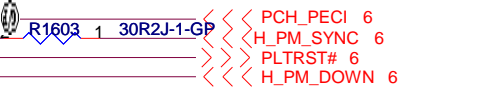
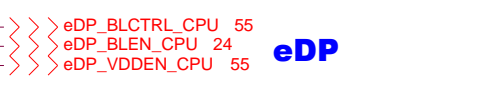
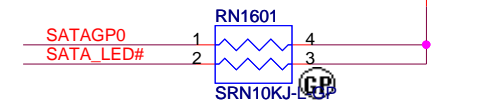
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MSATA

HDD

ODD

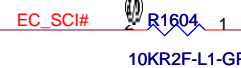
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1V\_VCCST



CHECK NEED PULL HIGH?



PCH\_THERMTRIP# R1602 1 620R2F-GP

AROUND PCH

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<Core Design>

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Title PCH\_PCIE\_SATA

Size A4 Document Number

Newgate

Rev

1M

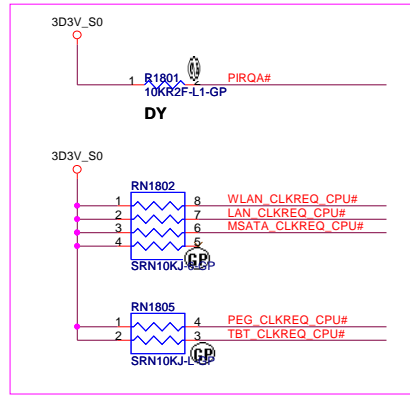
Date: Tuesday, August 18, 2015

Sheet 16 of 105

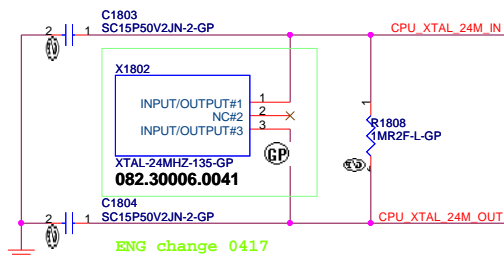


SSID = PCH

MP change 0807  
(not change net name)

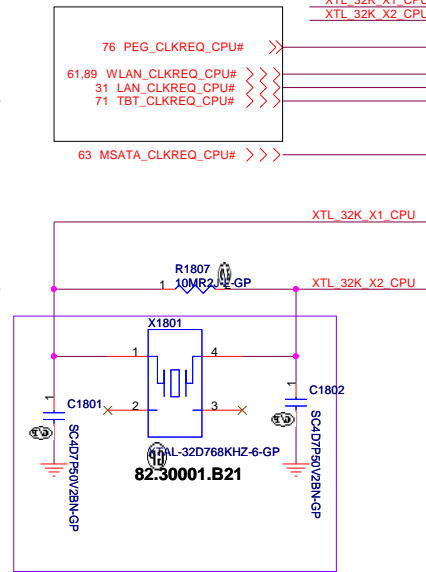


POWER modify 0223 SWAP 0303

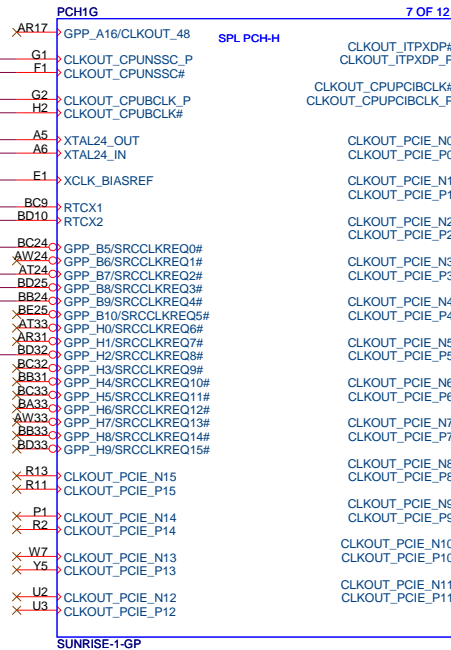
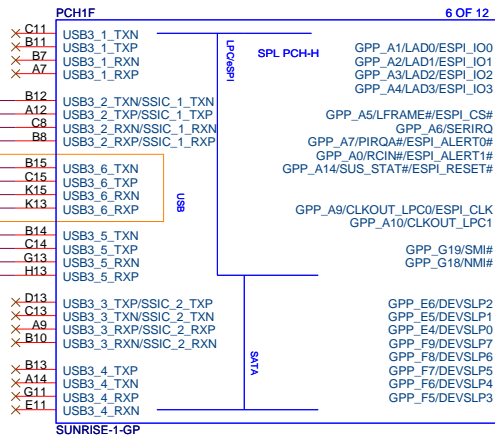


ENG change 0417

CHECK WITH SW( VGA)



ENG 0412 change



GPIO REVIEW CHECK

GPIO REVIEW CHECK

>>> DEVSLP\_PCH 63

GPIO REVIEW CHECK

>>> DEVSLP\_PCH 63

>>> DEVSLP\_PCH 63

>>> DEVSLP\_PCH 63

>>> DEVSLP\_PCH 63

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>>> DEVSLP\_PCH 63

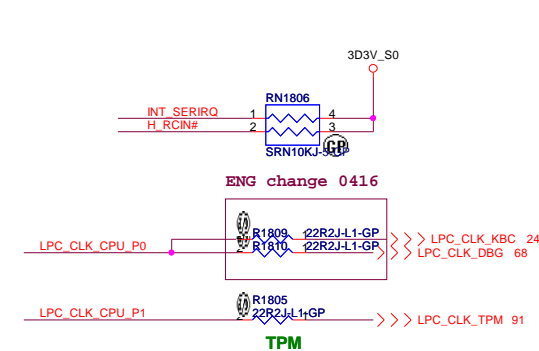
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>>> DEVSLP\_PCH 63

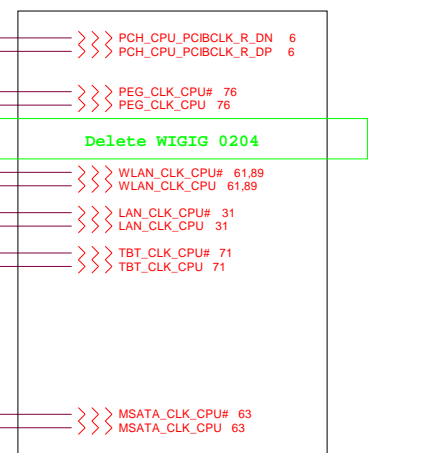
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>>> DEVSLP\_PCH 63



PEG CLOCK CHECK WITH SW

CHECK P and N

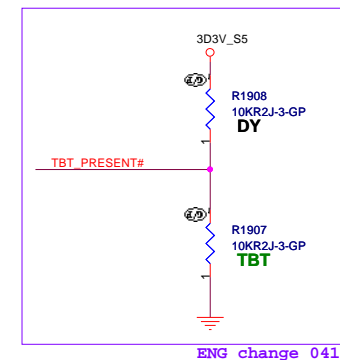
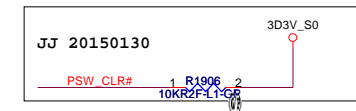
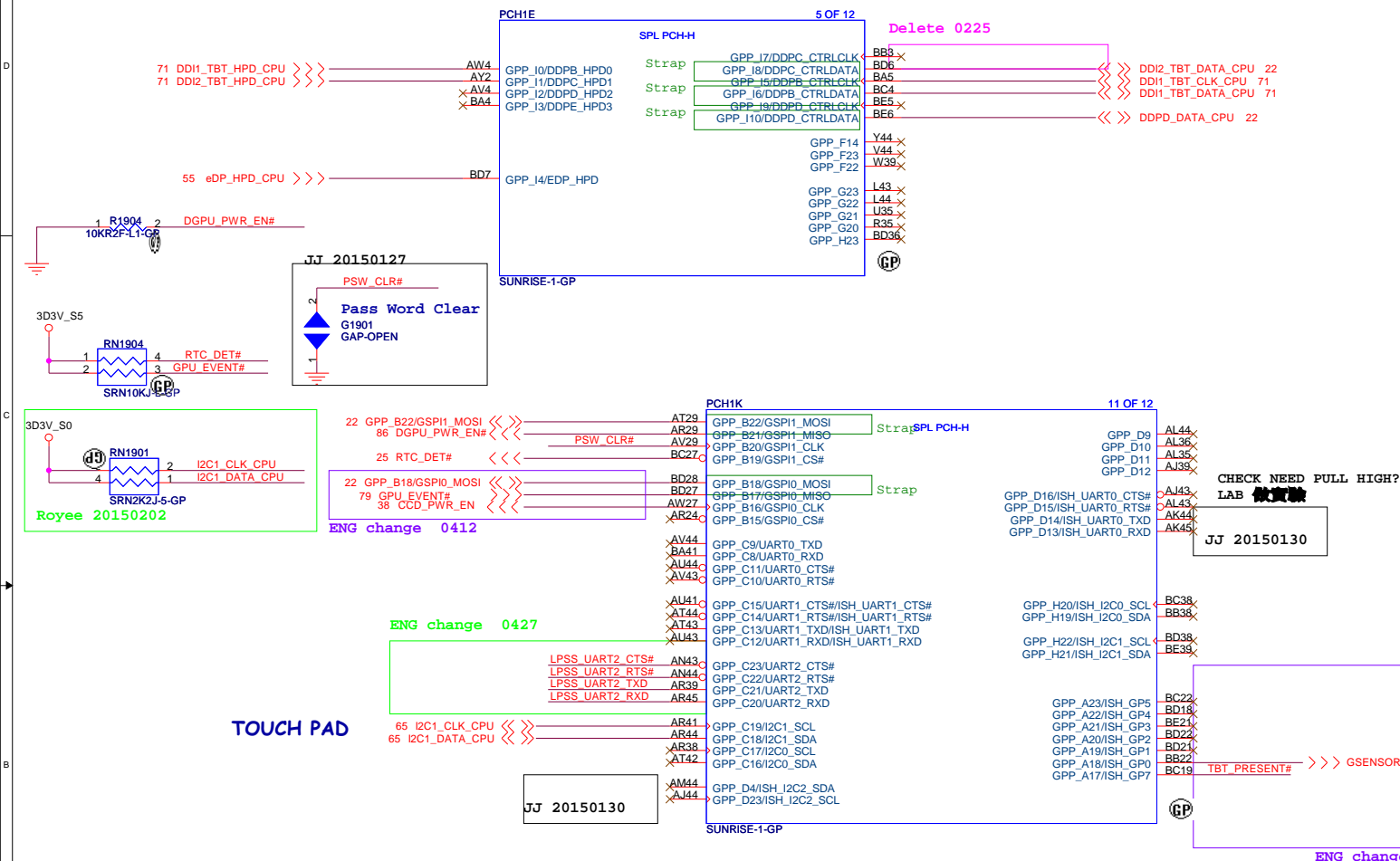


<Core Design>

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Title			
PCH USB3 CLOCK			
Size A3	Document Number		Rev
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Date:	Tuesday, August 18, 2015		Sheet 18 of 105

**SSID = PCH**



	HIGH	LOW
TBT_PRESENT#	NON TBT	WITH TBT

### <Core Design>

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Title

**PCH GPP2 GPP3**

Size  
A3

Document Number

**Newgate**

Rev	1M
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Date: Tuesday, August 18, 2015

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ENG change property 0505



SSID = PCH

**PCH1H** 8 OF 12

**CORE**

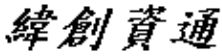
**MPHY**

**USB**

**SUNRISE-1-GP**

**GP**

<Core Design>

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Title <b>PCH_POWER_VCCPRIM_VCCMPHY</b>	
Size A4	Document Number <b>Newgate</b>
Date: Wednesday, August 12, 2015	Sheet 20 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

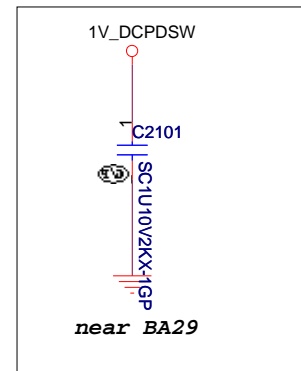
Size A4	Document Number <b>Newgate</b>	Rev <b>1M</b>
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Date: Wednesday, August 12, 2015 Sheet 20 of 105

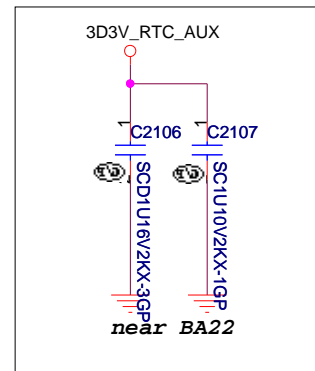


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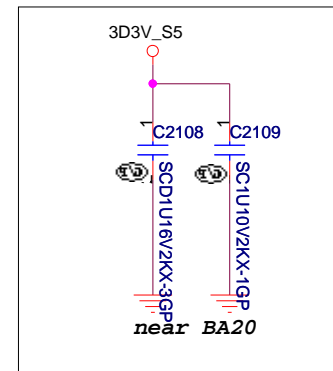
DcpDSW  
1x 1uF



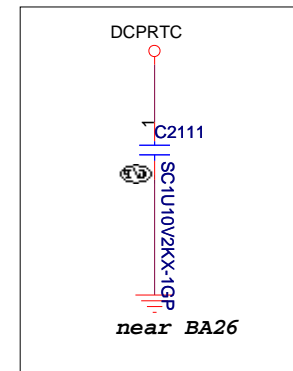
VccRTC  
1x1 uF 1x0.1 uF



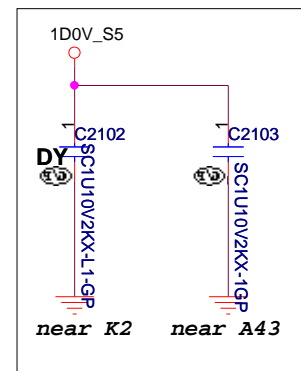
VccRTCPRIM  
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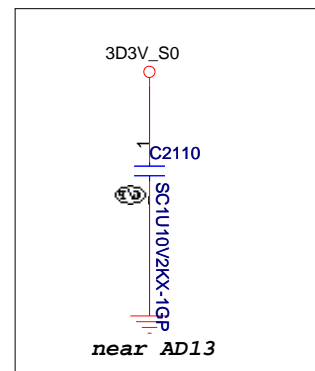
DcpRTC  
1x 0.1uF



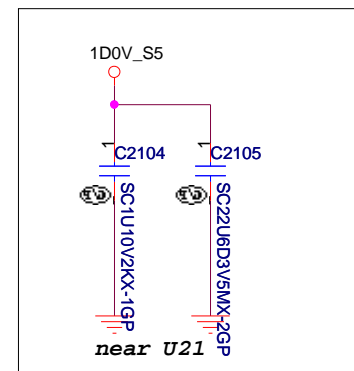
VccMPHYPLL / VccPCIE3PLL  
1x1 uF



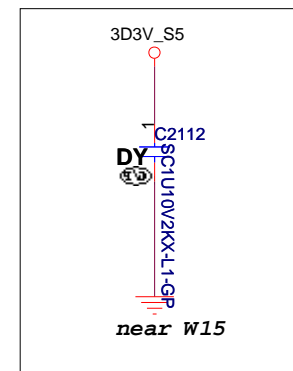
VccATS  
1x1 uF



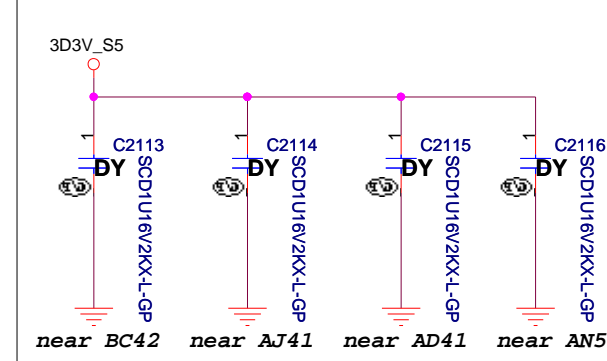
VccMPHY / VccPRIM / VccAPLLEBB  
1x1 uF 1x22 uF



VccDSW  
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG  
/ VccPRIM  
4x 0.1 uF



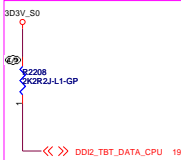
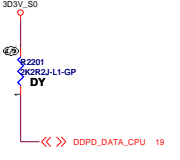
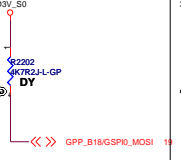
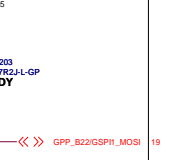
Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO)  
(Sheet 1 of 2)

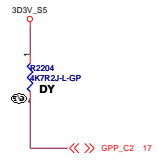
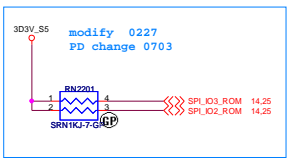
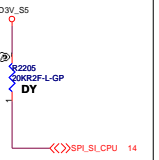
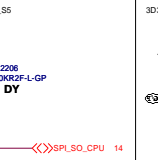

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/jumper / Edge)	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, ACL17, V28	1 uF 22 uF	0402 0805	1 1	E (<3 mm) E (<5 mm)	U21
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA36, AA38, AC13, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
V1.0DS W	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPT	BE41, BE42, BE43	-	-	-	-	-
V1.8A/ V1.8S/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
	VccHDA	BA15	-	-	-	-	-
	VccRTCPRIM	BA20	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA20
V3.3RTC	VccRTC	BA22	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA22
	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
V3.3DS W	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

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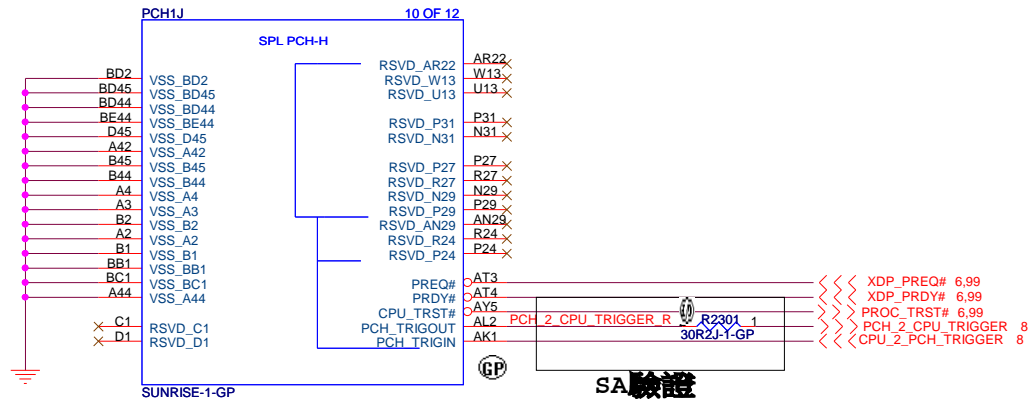
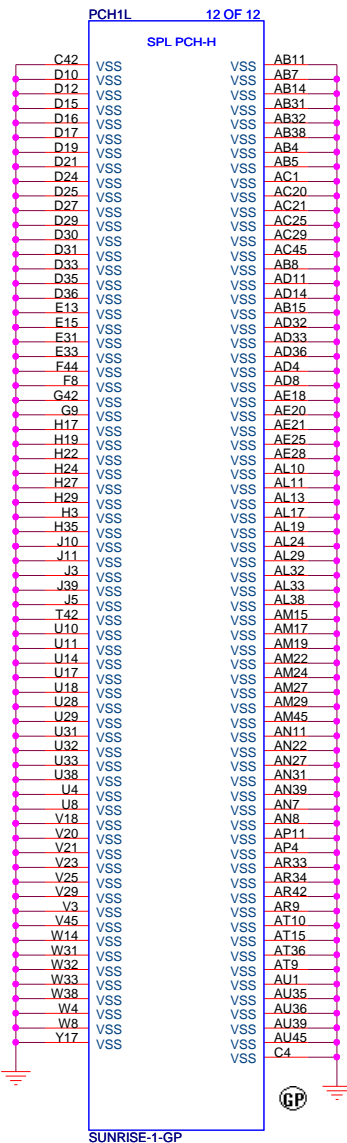
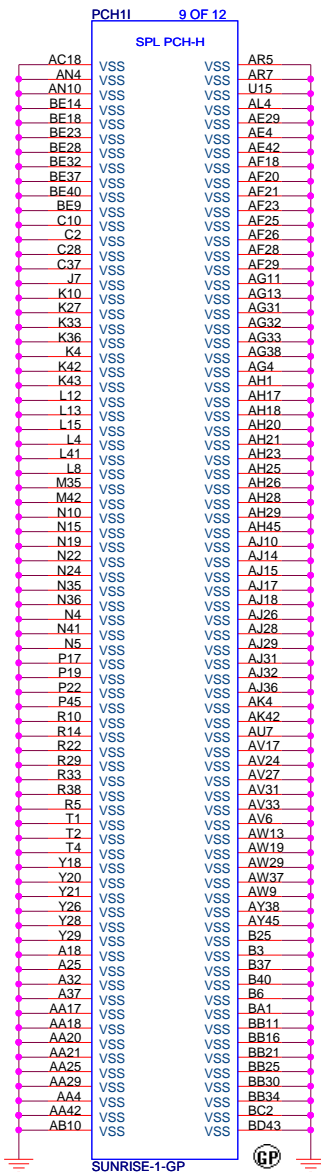
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Title		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 R97101	<div>change 0225</div> 					
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confidentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23
Schematic				<div>modify 0227 PD change 0703</div> 				
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

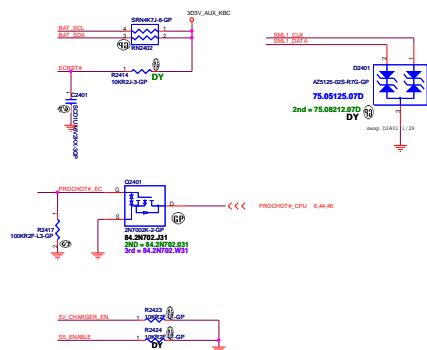
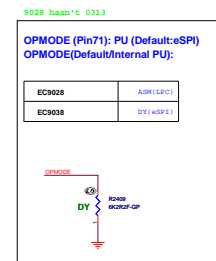
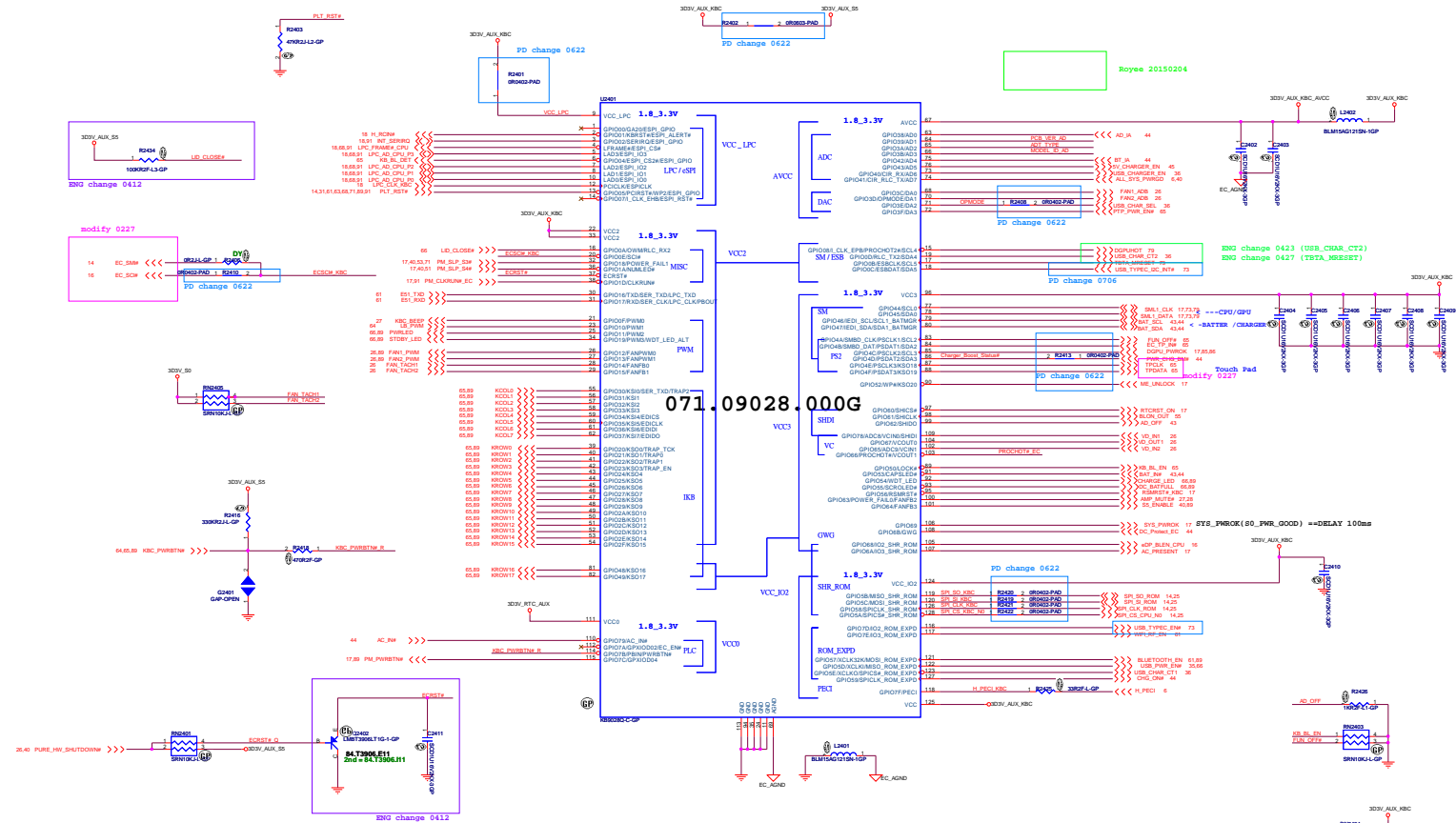
# SSID = PCH



<Core Design>

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Title			PCH_RSVD_VSS
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Wattage (W)	Full Core People	Fulling Machine	Typical Values	Max Value	AGI Timeline (days)
SA	100.0	10.0k	3.00W	300V	> 2875 V
SB	100.0	20.0k	2.70W	2.75W	> 2.67W
SC	100.0	30.0k	2.40W	2.40W	> 2.30W
SD	100.0	40.0k	2.20W	2.20W	> 2.10W
SE	100.0	50.0k	2.00W	2.00W	> 1.90W
Revised for project use	100.0	100.0k	1.60W	1.60W	> 1.50W
Revised for project use	100.0	100.0k	1.60W	1.60W	> 1.50W
Revised for project use	100.0	100.0k	1.30W	1.37W	> 1.20W
Revised for project use	100.0	100.0k	1.20W	1.20W	> 1.10W
Revised for project use	100.0	200.0k	1.00W	1.06W	> 0.90W

SWR Ratio	Pulsed Power	Pulsing Temp	Typical Voltage	Max Voltage	2% Tones Setting
20W	NA	100 °C	3.35V	NA	>=100V
30W	100.0%	NA	0.93V	NA	<=100V
40W	100.0%	100.0%	0.95V	0.95V	>=100V
50W	20.0%	100.0%	0.95V	0.95V	<=100V
60W	100.0%	100.0%	0.95V	0.95V	>=100V
70W	33.3%	100.0%	0.93V	0.93V	>=80V
80W	100.0%	100.0%	1.05V	1.05V	<=100V
90W	66.6%	100.0%	1.20V	1.20V	>=100V
100W	70.0%	100.0%	1.40V	1.40V	>=100V
Revised	100.0%	100.0%	1.65V	1.65V	>=100V

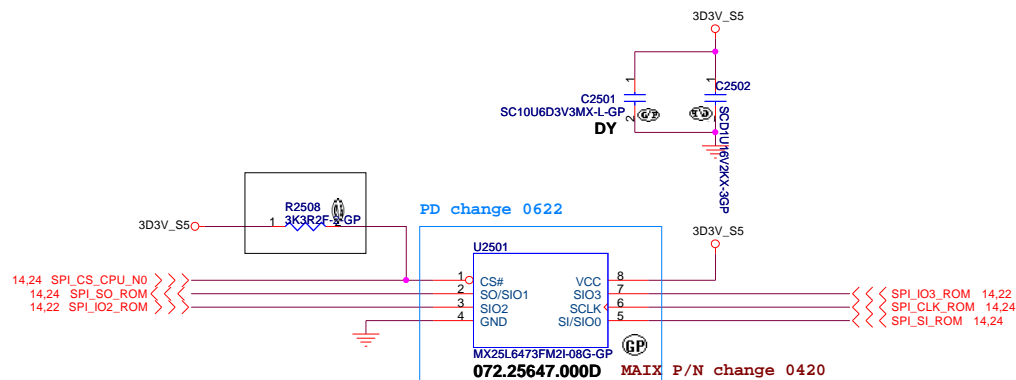


Model, n, m	Pull-In Register	Pull-Back Register	Typical Voltage
Rayleigh-SL_100A	100.0 K	10.0 K	3.000 V
Rayleigh-SL_945M	100.0 K	20.0 K	2.750 V
Rayleigh-SL_950M	100.0 K	33.0 K	2.481 V
Rayleigh-SL_960M	100.0 K	47.0 K	2.245 V
Newgate-SL_945M	100.0 K	64.9 K	2.081 V
Newgate-SL_950M	100.0 K	79.8 K	1.967 V
Newgate-SL_960M	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V



SSID = Flash.ROM

## SPI FLASH ROM (8M byte) for PCH



## SPI FLASH ROM (8M byte) for PCH

*SPI ROM Equal length need to less than 500mil*

SPI FLASH ROM (8M byte)

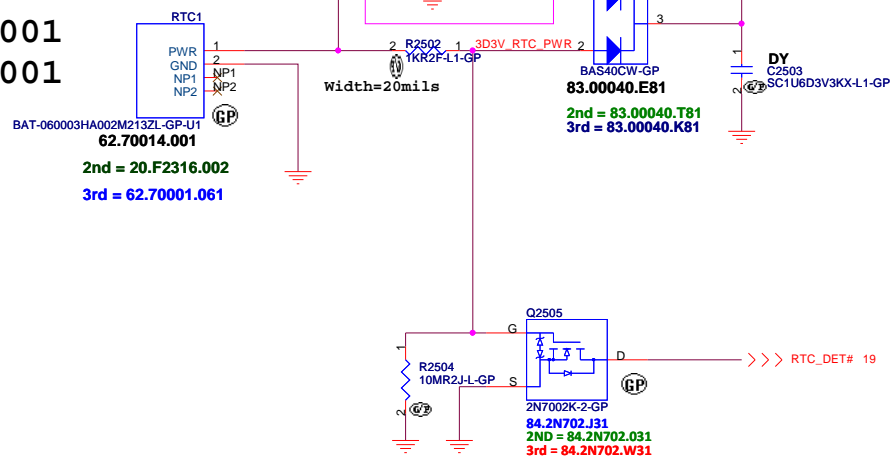
1st = 072.25647.000D (MXIC MX25L6473FM2I-08G)  
2nd= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)  
3rd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

Main Func = RTC

RTC BATTERY

1st= 23.22065.001

2nd= 23.20068.001



<Core Design>

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Flash(KBC+PCH)/RTC			
Size A3	Document Number	Rev 1M	
Date: Tuesday, August 18, 2015	Sheet 25 of 105	Newgate	

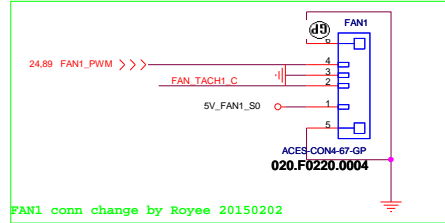
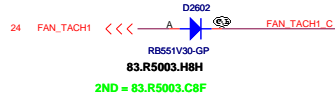
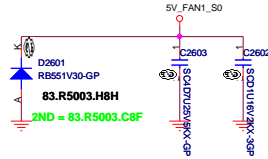
SSID = Thermal

ADB (Active Dusting Blower) function

AFTP TESTPOINT

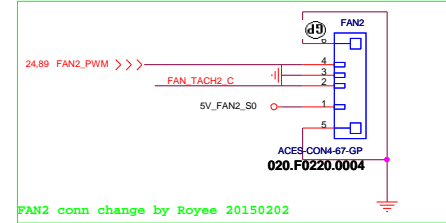
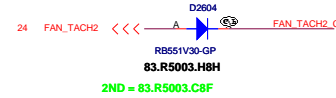
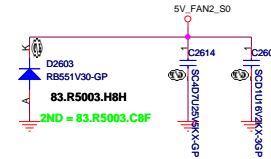
FAN\_TACH1\_C >>> FAN\_TACH1\_C 89  
FAN\_TACH2\_C >>> FAN\_TACH2\_C 89

\*Layout\* 15 mil

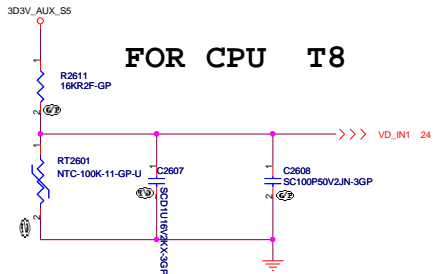


FAN1 conn change by Royee 20150202

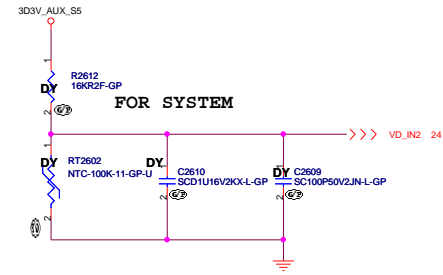
\*Layout\* 15 mil



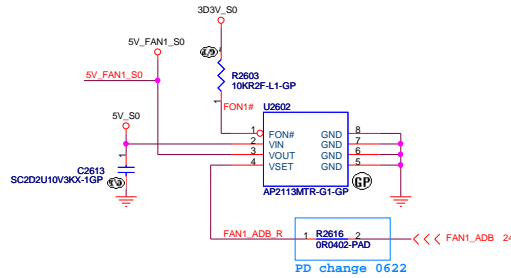
FAN2 conn change by Royee 20150202



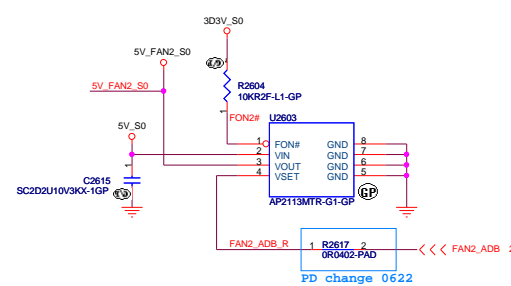
FOR CPU T8



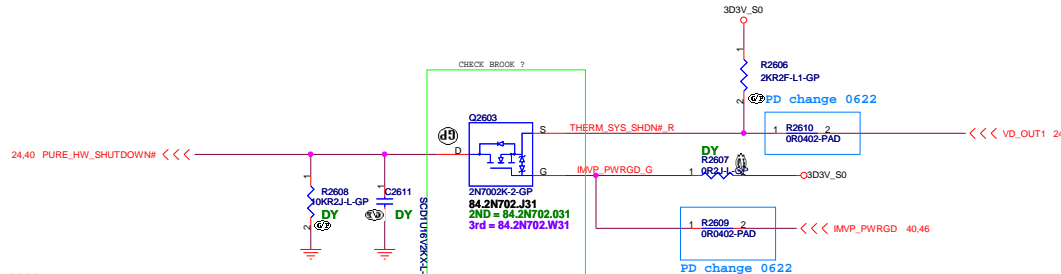
FOR SYSTEM



PD change 0622



PD change 0622



T8 = 85 degree

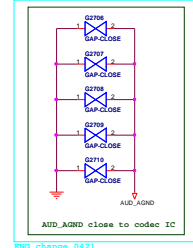
UN 0225

<Core Design>

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Taipai Hsien 221, Taiwan, R.O.C.

File	Thermal T8 and FAN	Rev	1M
Size	Document Number		
Custom	Newgate		
Date:	Thursday, August 18, 2015	Sheet	26 of 105

## SSID = AUDIO



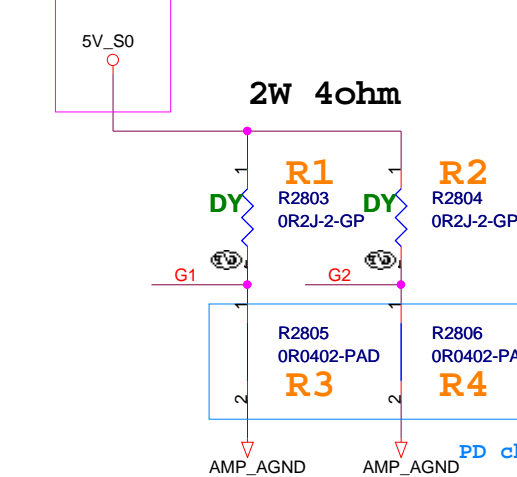
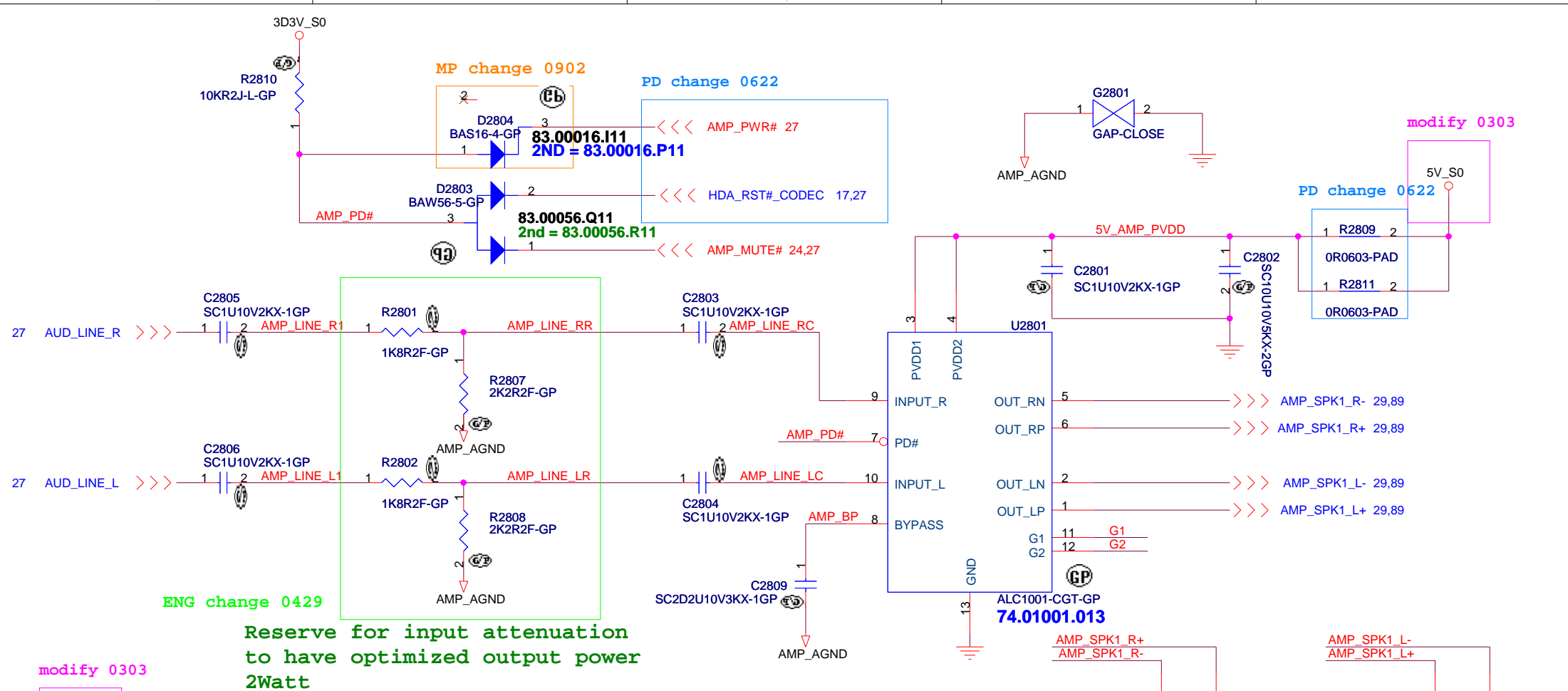
**Layout Note:**

Width>40mil, to improve Headphome Crosstalk noise  
Change it to sharp will be better.  
Add 2 vias (>0.5A) when trace layer change.

**Codec**  
**Analog**  
pin 12-33, 38-40

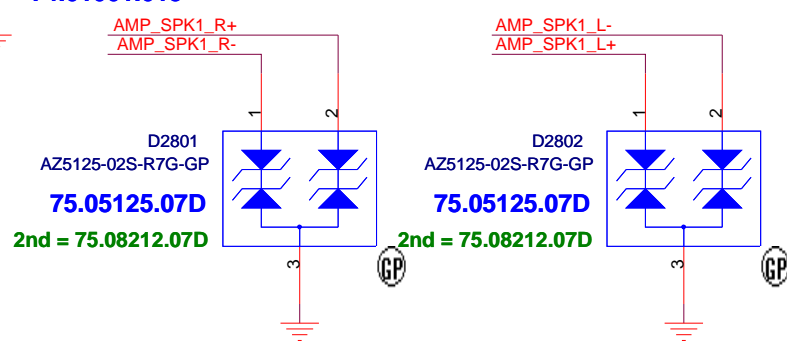
---

**Digital**  
pin 1-11, 34-37,  
42-48



Output Gain Table

R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



<Core Design>

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Title (Reserved)

Size A4 Document Number Newgate Rev 1M

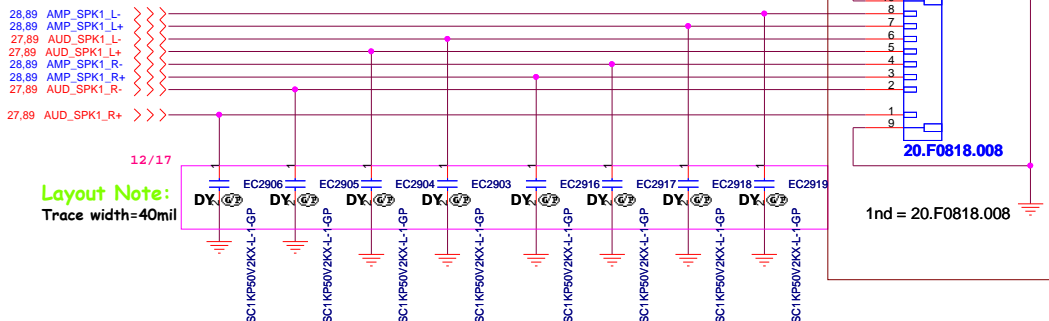
Date: Wednesday, September 02, 2015 Sheet 28 of 105



SSID = AUDIO

Check speaker spec and confirm 2nd with ME 0302

## Speaker



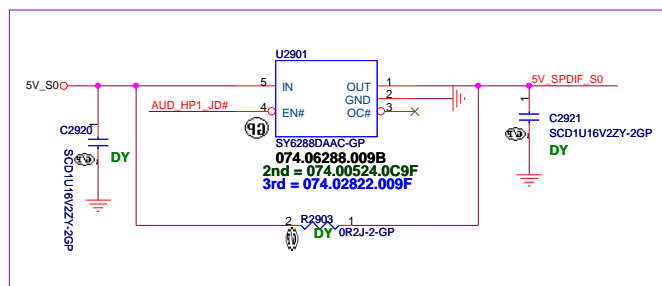
AMP\_SPK1\_L- <<< AMP\_SPK1\_L- 28.89  
AMP\_SPK1\_L+ <<< AMP\_SPK1\_L+ 28.89  
AUD\_SPK1\_L- <<< AUD\_SPK1\_L- 27.89  
AUD\_SPK1\_L+ <<< AUD\_SPK1\_L+ 27.89  
AMP\_SPK1\_R- <<< AMP\_SPK1\_R- 28.89  
AMP\_SPK1\_R+ <<< AMP\_SPK1\_R+ 28.89  
AUD\_SPK1\_R- <<< AUD\_SPK1\_R- 27.89  
AUD\_SPK1\_R+ <<< AUD\_SPK1\_R+ 27.89

AFTP TESTPOINT

AUD\_HP1\_JACK\_R2\_OUT <<< AUD\_HP1\_JACK\_R2\_OUT 89  
AUD\_HP1\_JACK\_L2\_OUT <<< AUD\_HP1\_JACK\_L2\_OUT 89  
LINE1\_L\_IN <<< LINE1\_L\_IN 89  
LINE1\_R\_IN <<< LINE1\_R\_IN 89  
5V\_SPDIF\_S0 <<< 5V\_SPDIF\_S0 89  
AUD\_SPDIF\_OUT <<< AUD\_SPDIF\_OUT 27.89

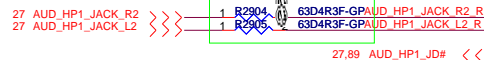
ENG add AFTP 0430

AFTP TESTPOINT

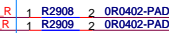


ENG change 0412

ENG change 0504



PD change 0622

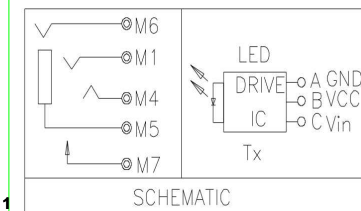
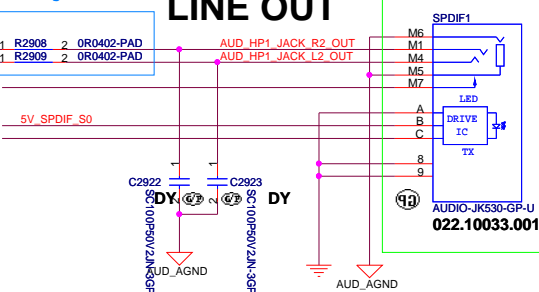


## LINE OUT

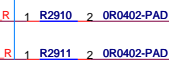
ENG connector change 0504

27.89 AUD\_HP1\_JD# <<<

27.89 AUD\_SPDIF\_OUT <<<



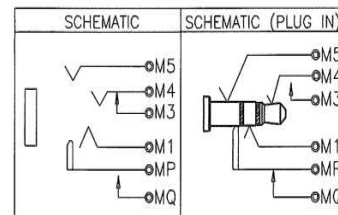
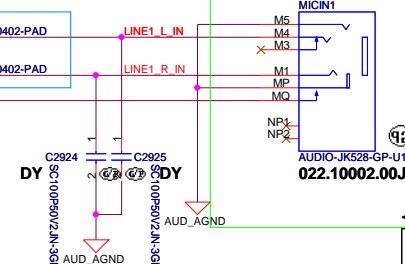
PD change 0622



## MIC IN

ENG connector change 0504

27.89 AUD\_MIC1\_JD# <<<



<Core Design>

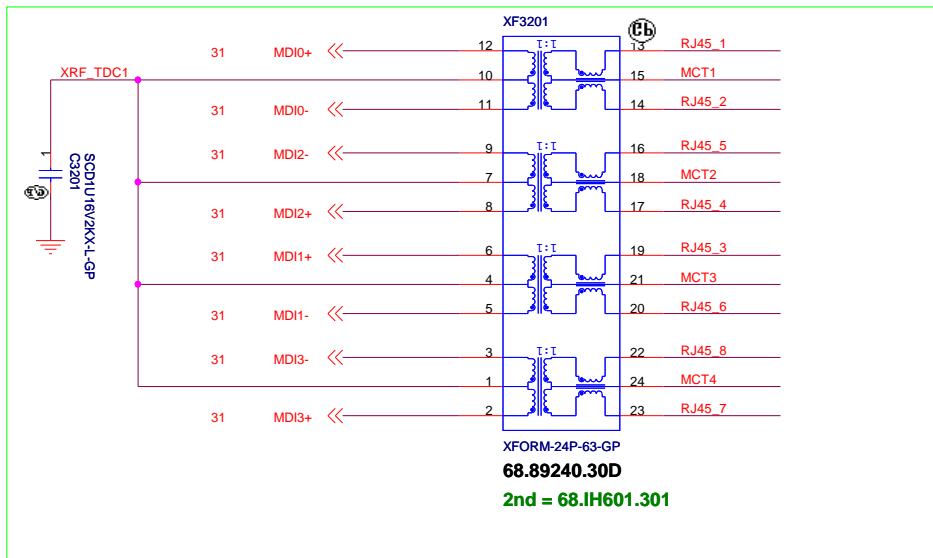
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Speaker/ALC255
Size	Document Number	Rev	
Custom	Newgate	1M	
Date:	Tuesday, August 16, 2015	Sheet	29 of 105

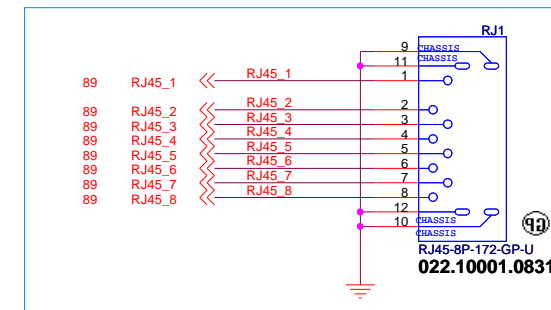


SSID = LAN

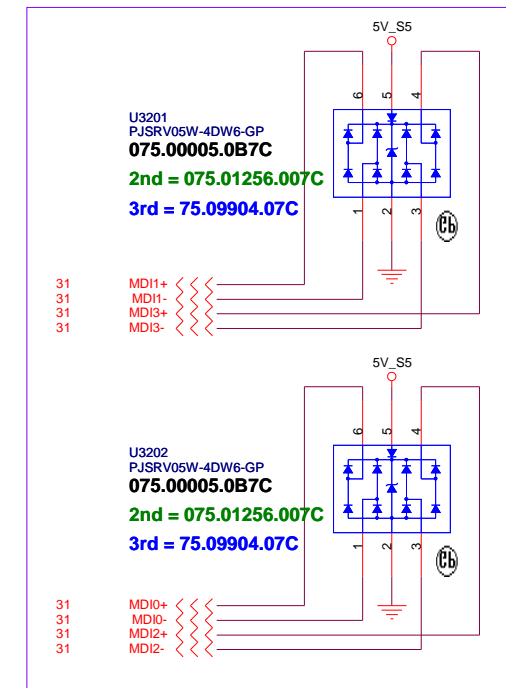
part change 0430



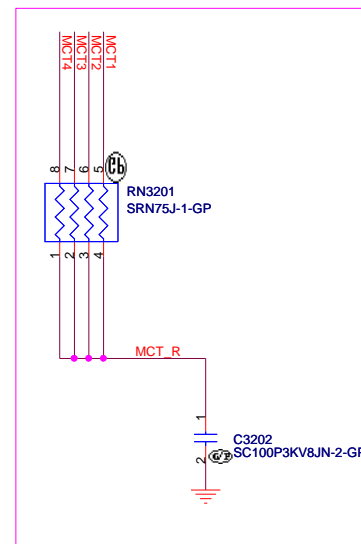
PD change 0624



ENG change 0412



SWAP 0228

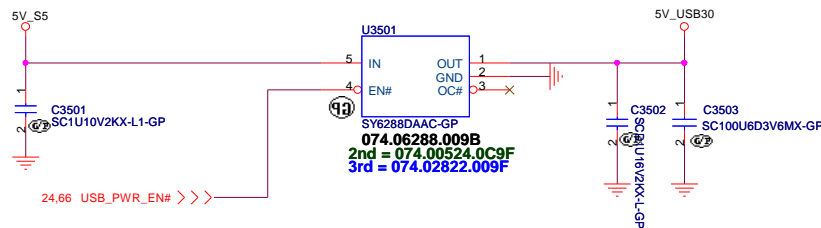


<Core Design>

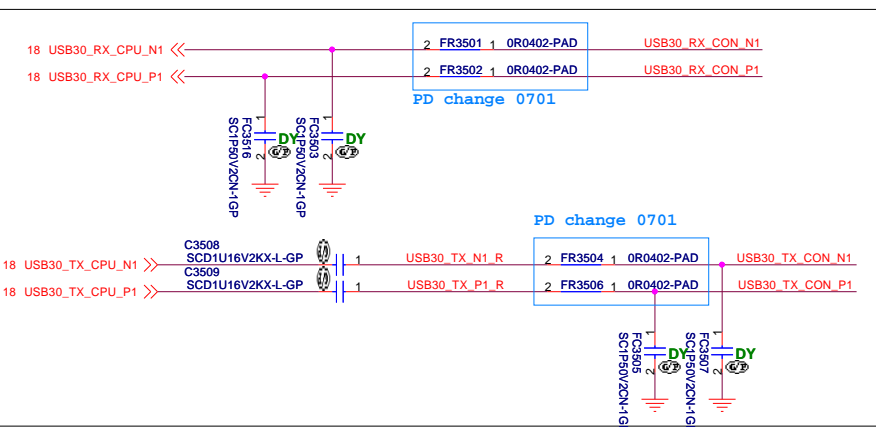
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
RJ45+Transformer		
Size	Document Number	Rev
B	Newgate	1M
Date:	Tuesday, August 18, 2015	Sheet 32 of 105

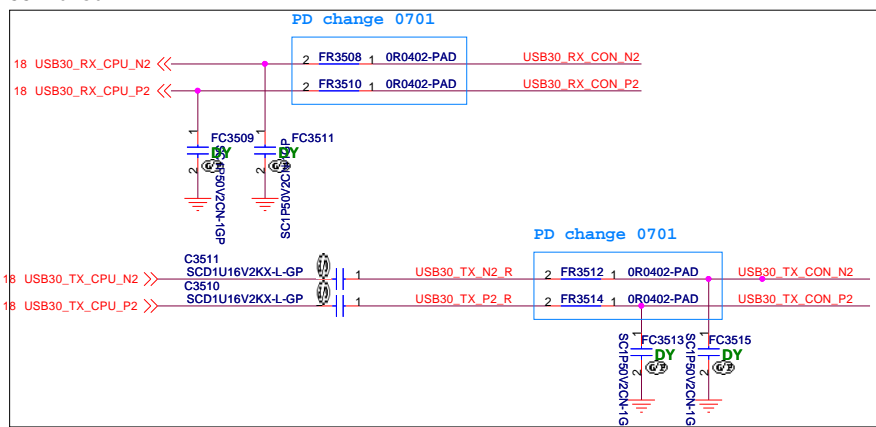
## Low Active 2A



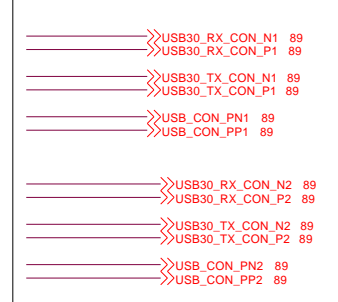
JJ 20150127



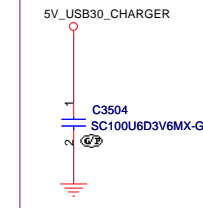
JJ 20150127



## AFTP TESTPOINT



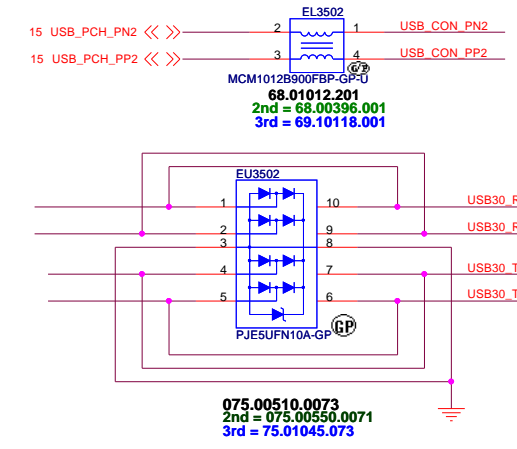
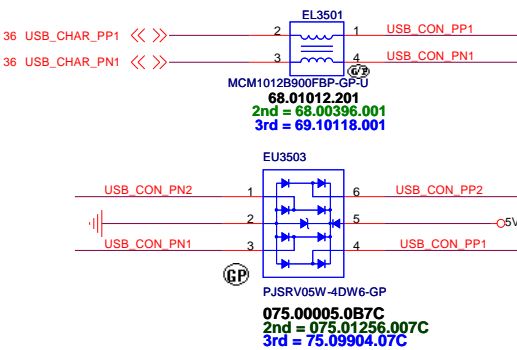
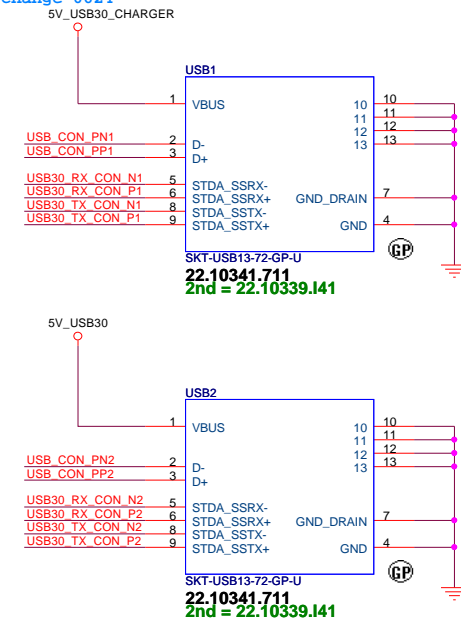
Close to USB1 0416



## USB 3.0 Connector Pin definition

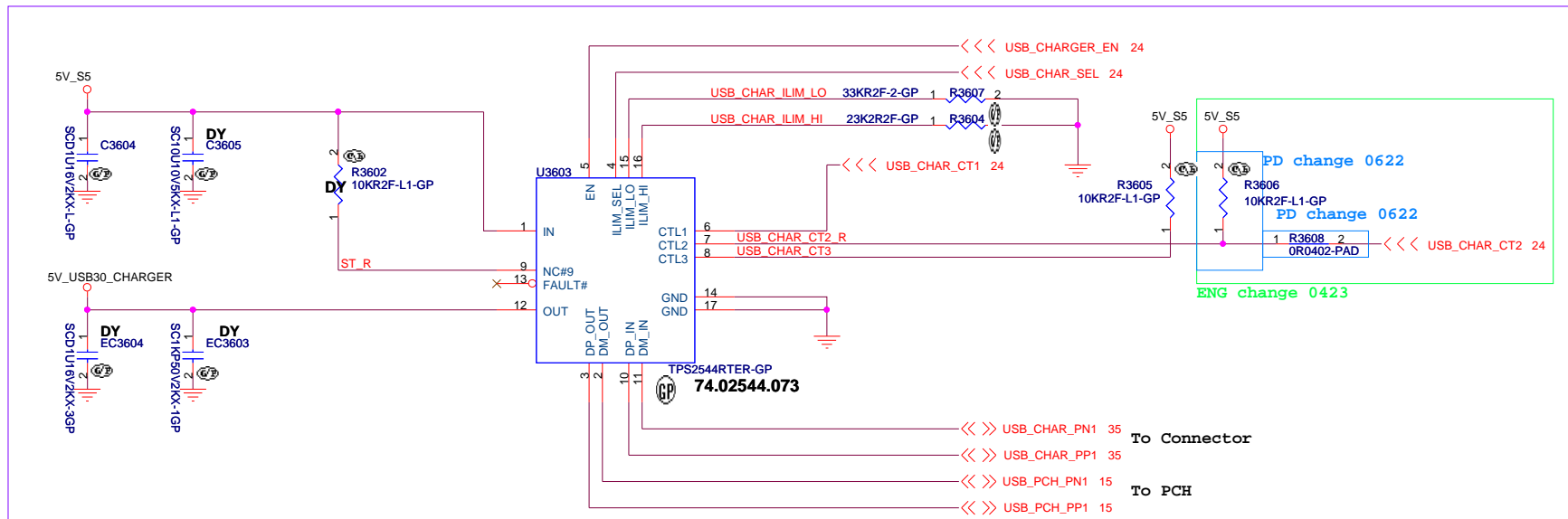
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

## USB3.0 conn change by Royee 20150202 PD change 0624



<Core Design>

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Title USB3.0 CONN	
Size A3	Document Number
Date: Tuesday, August 18, 2015	Sheet 35 of 105
Newgate	
Rev 1M	



ENG change 0412

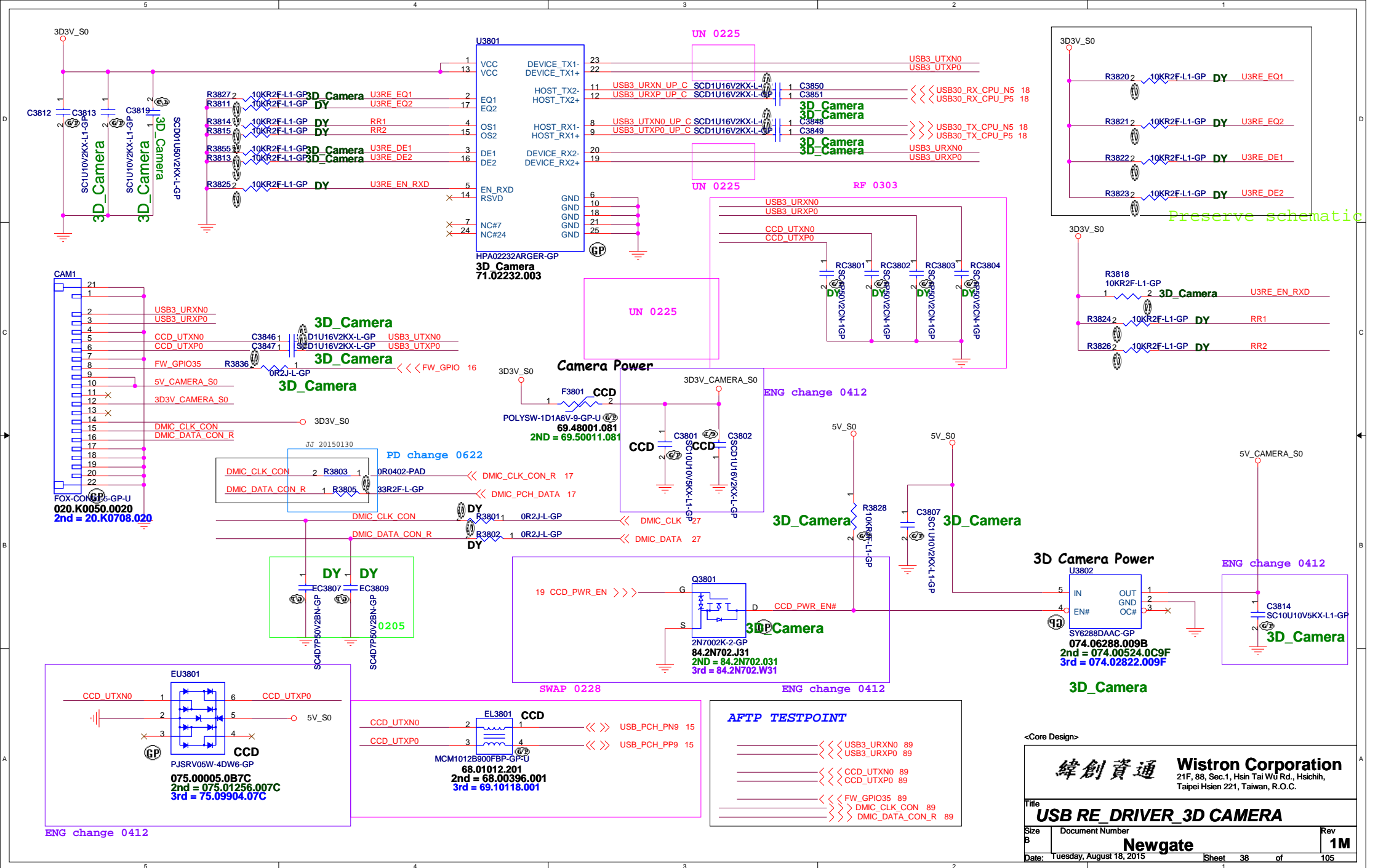
Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	Data lines disconnected
0	1	1	0	DCP_Auto	ILIM_LO	OFF	
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1 Charging mode
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	Data lines disconnected Load Detect function active
1	1	1	1	CDP	ILIM_HI	CDP	

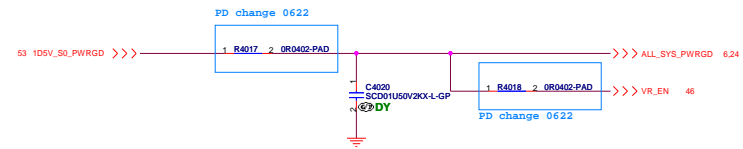
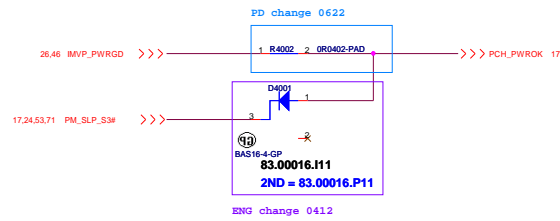
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

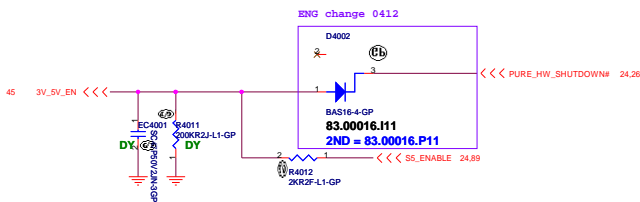
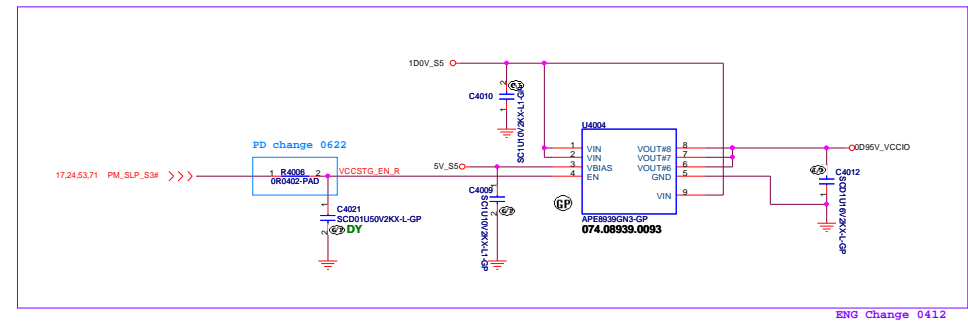
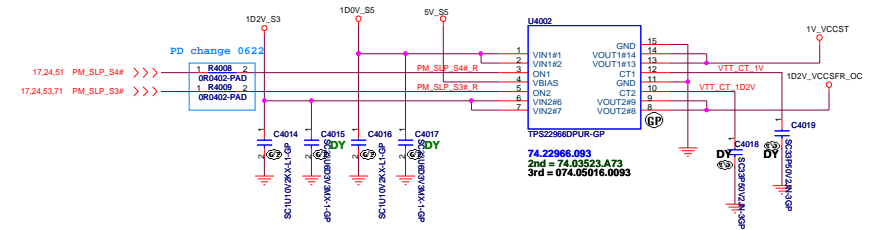
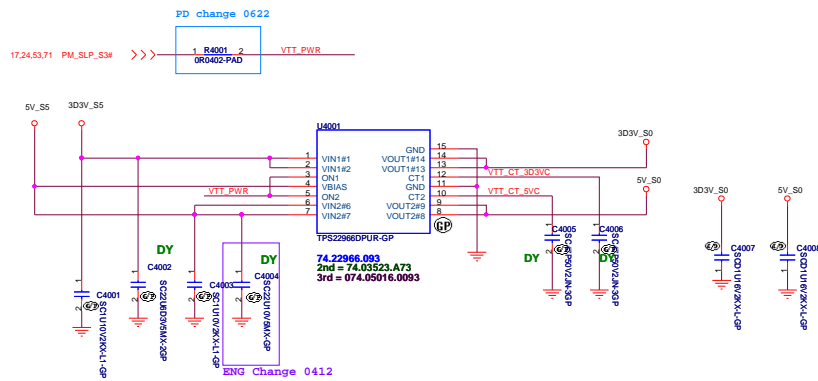
Title			<b>USB CHARGER</b>
Size B	Document Number	Rev	
	<b>Newgate</b>	<b>1M</b>	
Date:	Tuesday, August 18, 2015	Sheet	36 of 105



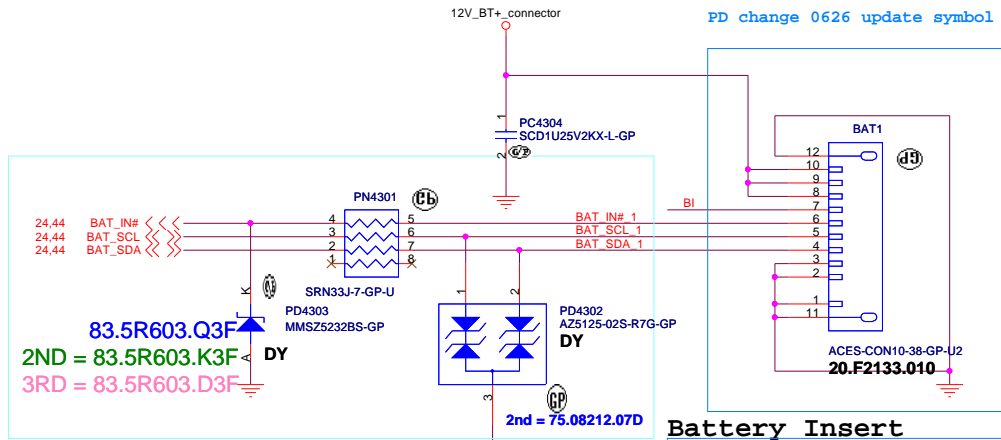
### Power Sequence



***ANNIE Run Power***

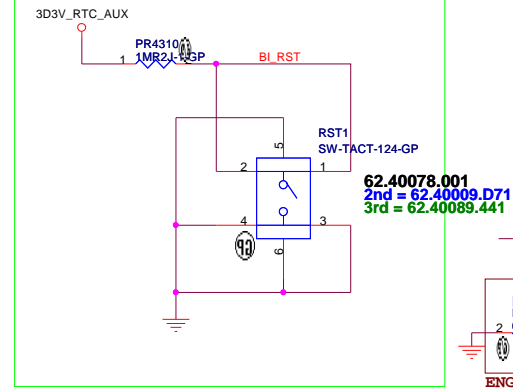


UN 0225



## Battery Reset

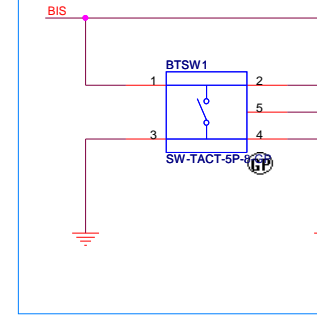
RST1 conn change by Royee 20150202



## Battery Insert

BTSW1 conn change by Royee 20150202

PD change 0624

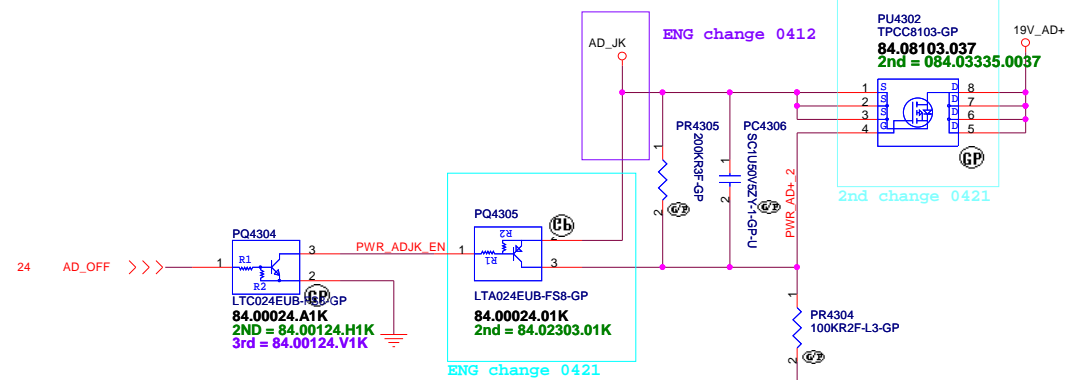
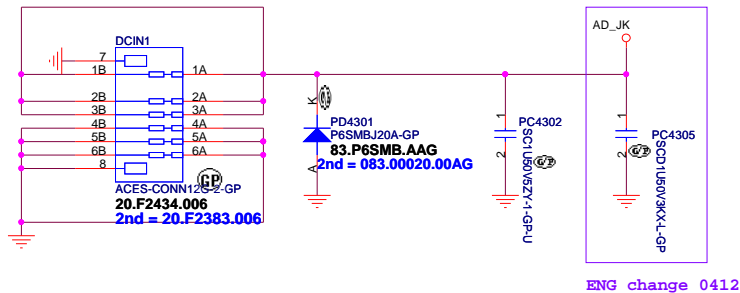


## AFTP TESTPOINT

89	BI	BI
89	BAT_IN#_1	BAT_IN#_1
89	BAT_SCL_1	BAT_SCL_1
89	BAT_SDA_1	BAT_SDA_1

## ANNIE solution

Adaptor in to generate DCBATOUT



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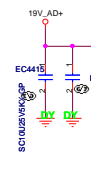
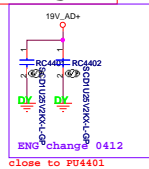
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title			DC IN / BATT Conn
Size	Document Number	Rev	
A3	Newgate	1M	
Date:	Tuesday, August 18, 2015	Sheet	43 of 105



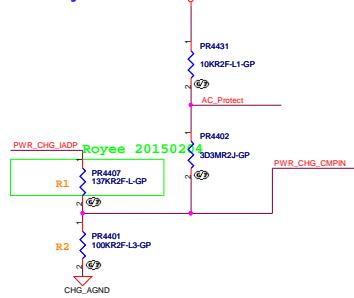
# SSID = Charger



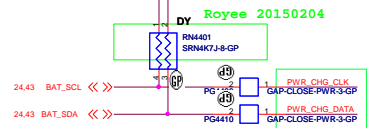
ENG change 0412

Adaptor	Protect	Sense	Amplifier	R1	R2
Watt	Current	Persent	Current	Resistor	Ratio
135.00 W	6.92 A	102%	7.06 A	10 m Ohm	40
120.00 W	6.15 A	102%	6.28 A	10 m Ohm	40
90.00 W	4.02 A	102%	4.71 A	10 m Ohm	40
				1.00 V	50 K

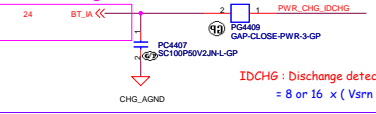
## Total Power Setting



## SMBus

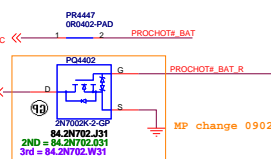
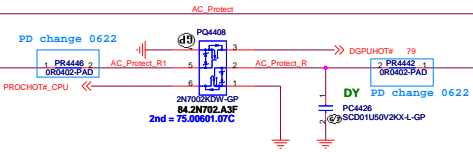
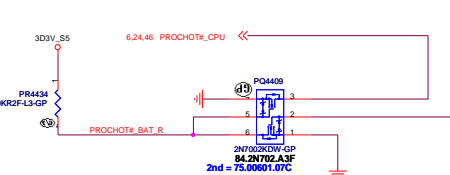


## net change 0223



PMON : Total system power

IADP : AC adapter detect current : = 20 or 40 x ( Vvac - Vacn ) / 10mohm



Charger Current=1.4~3.6A

Core Design

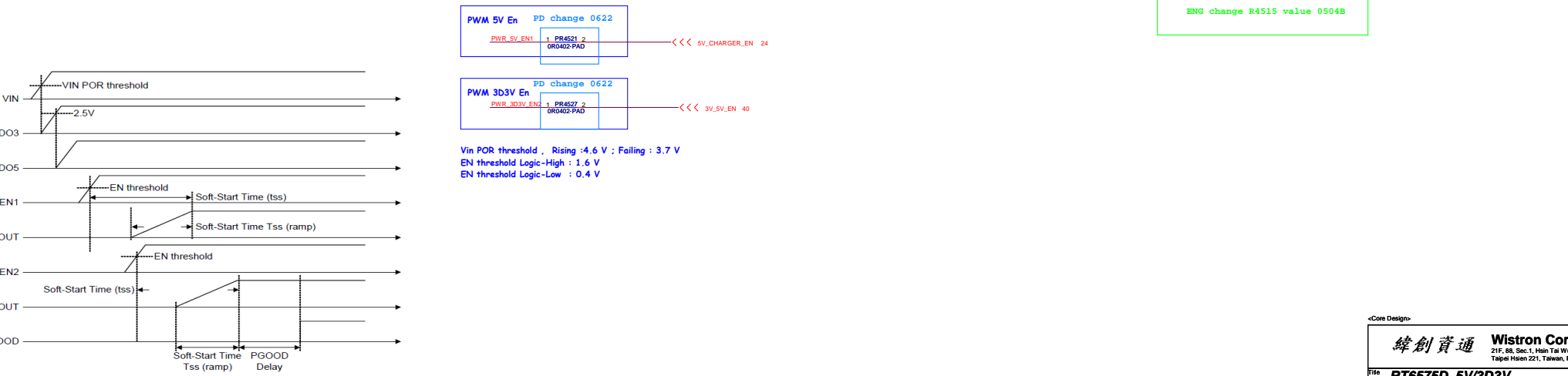
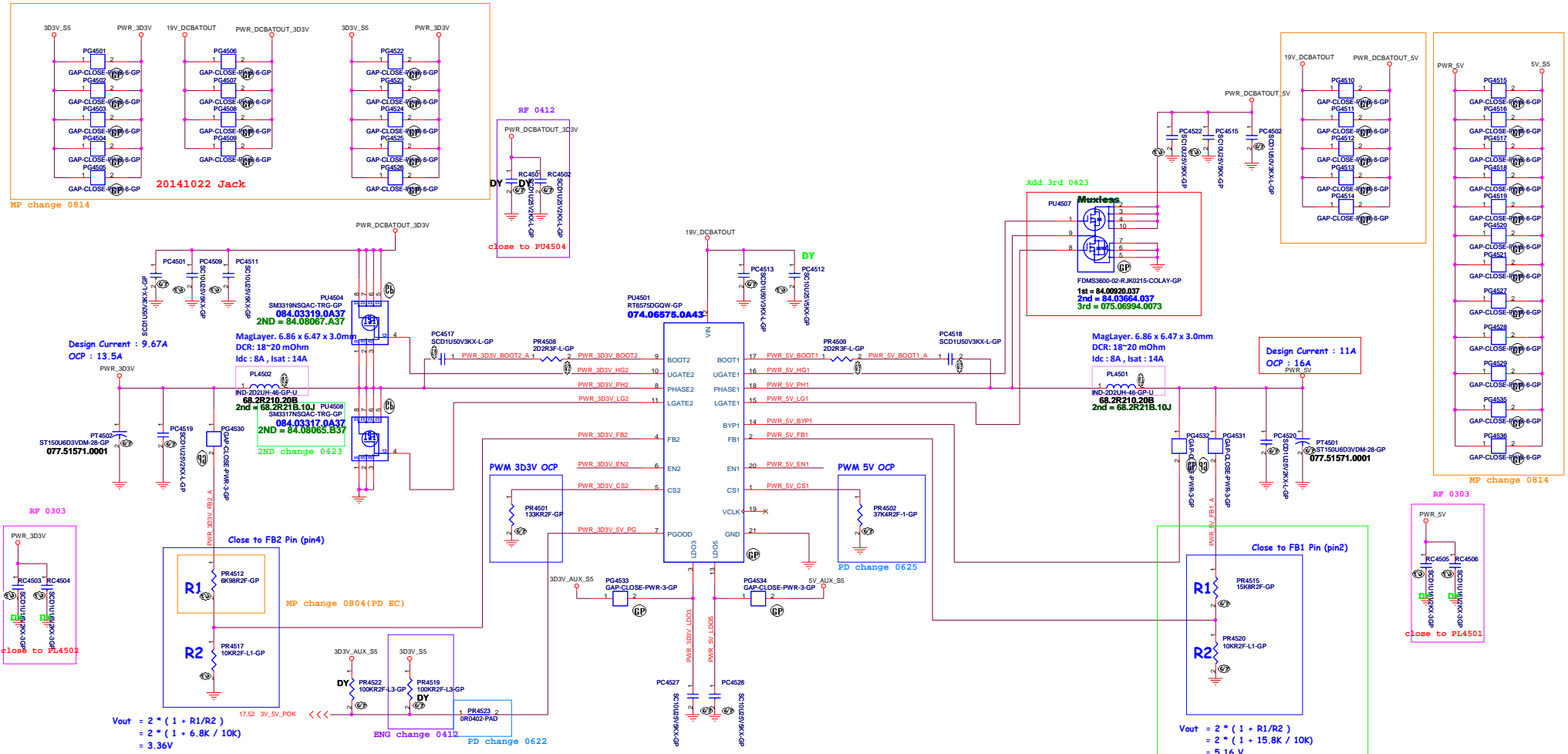
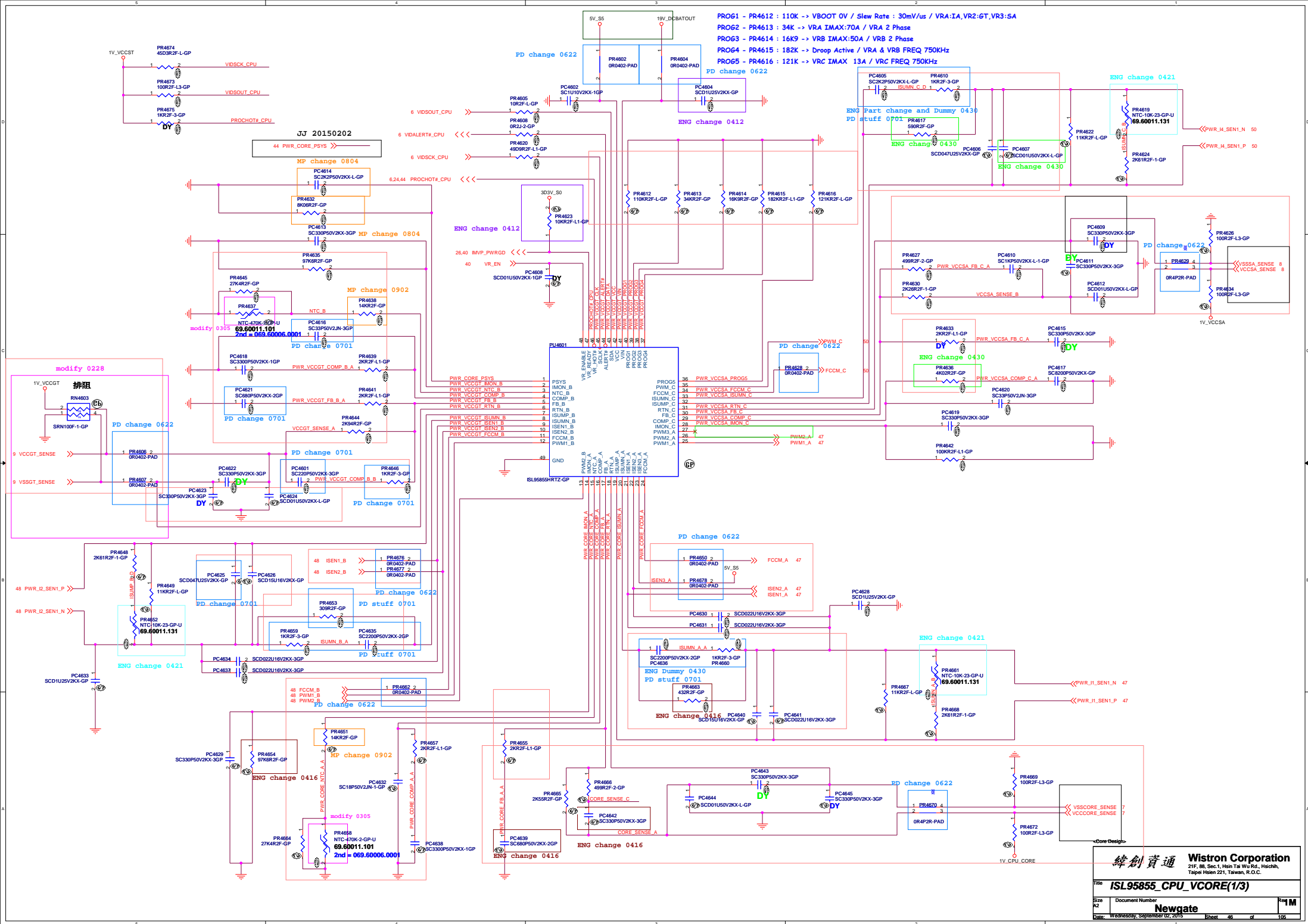
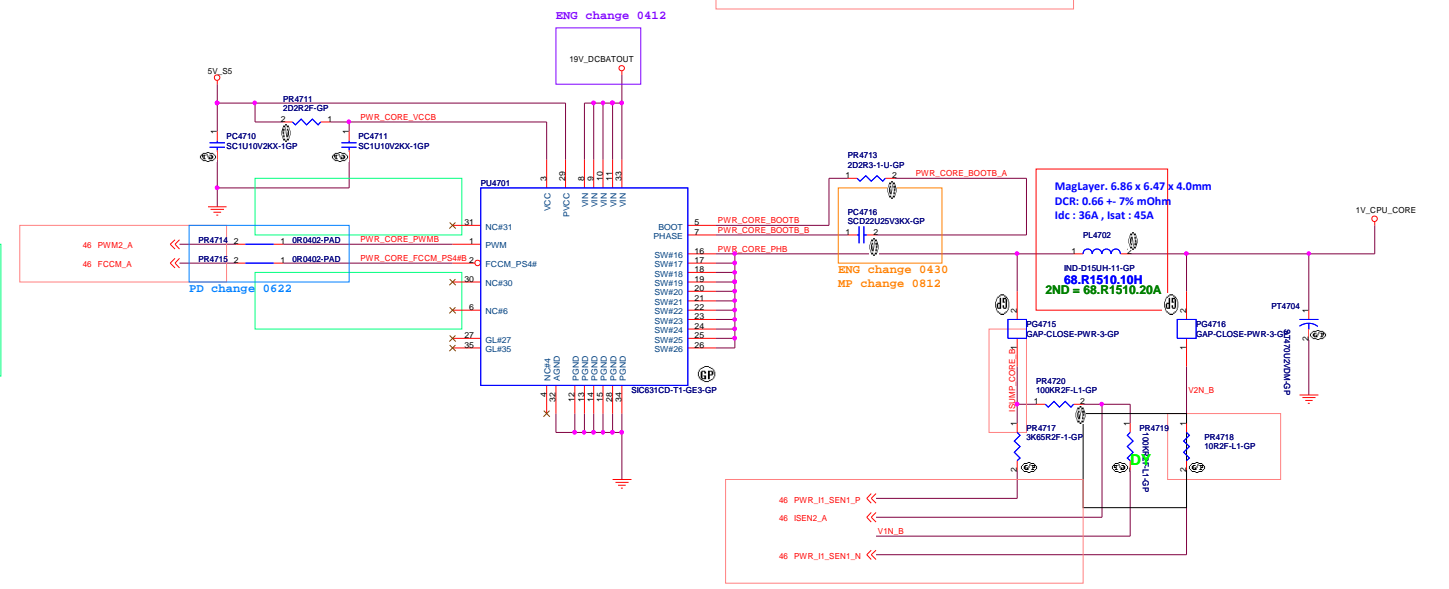
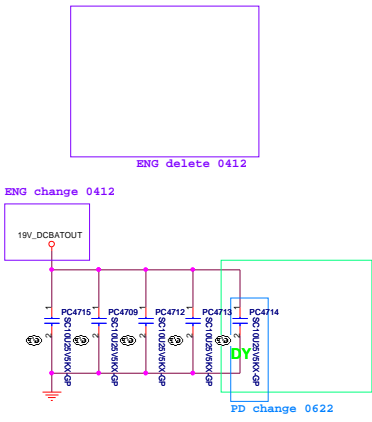
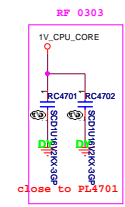
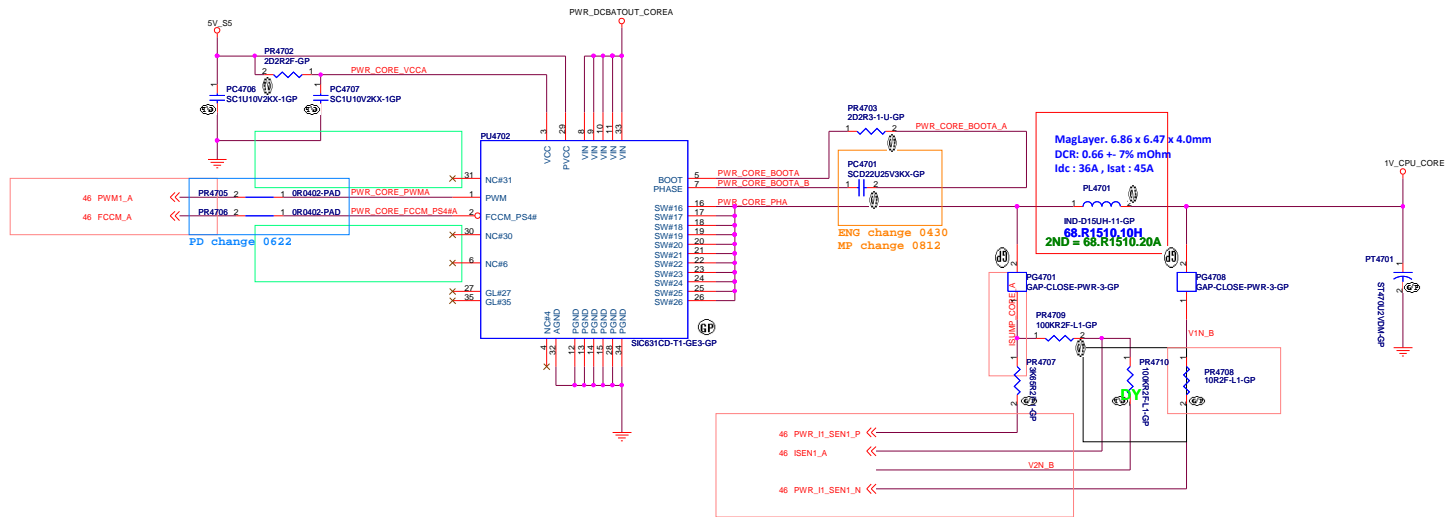
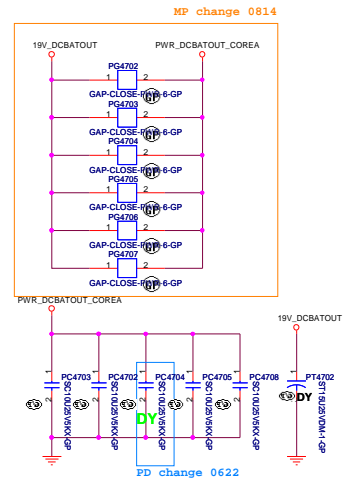
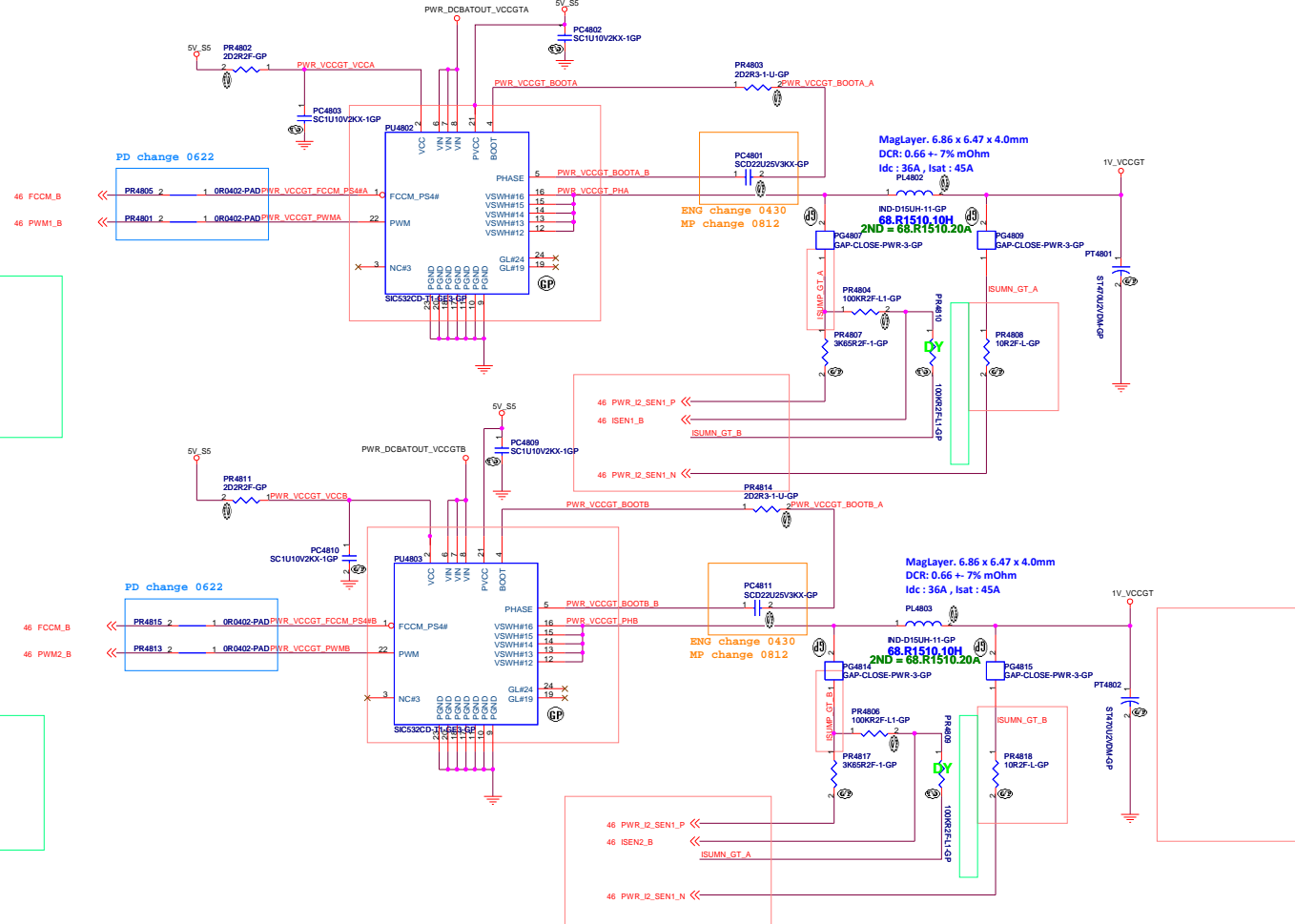
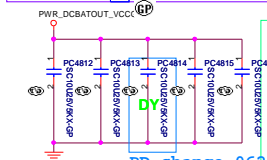


Figure 6. RT6575B Timing







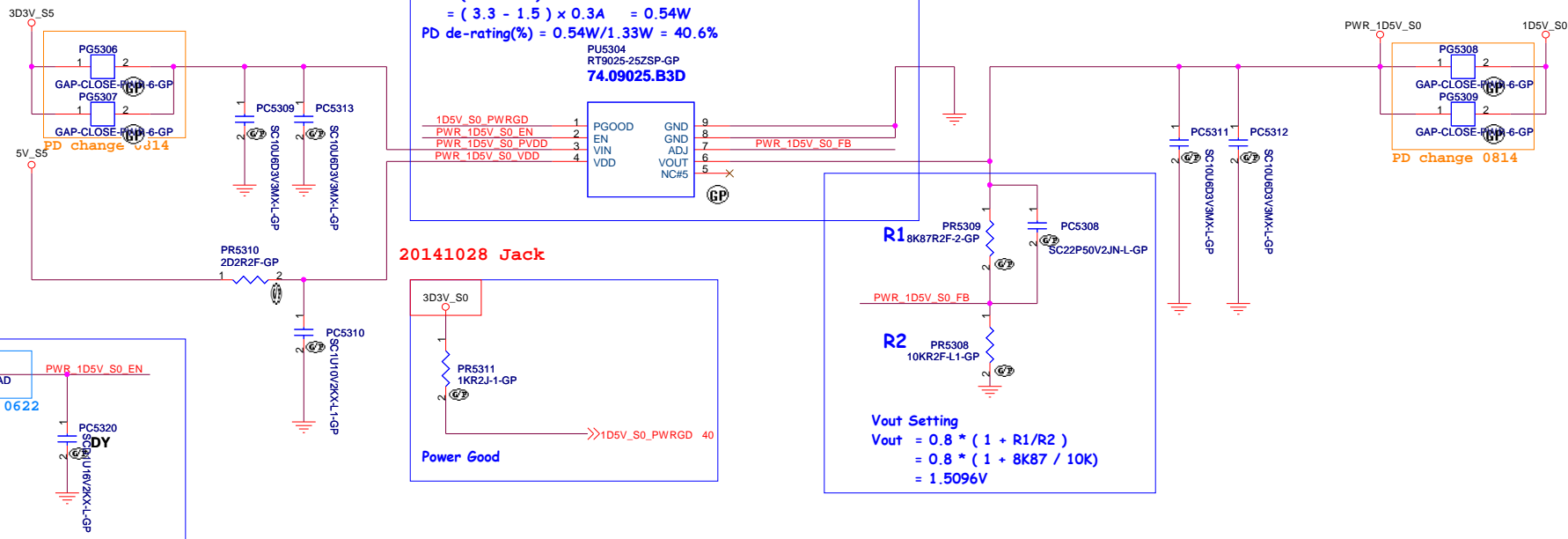


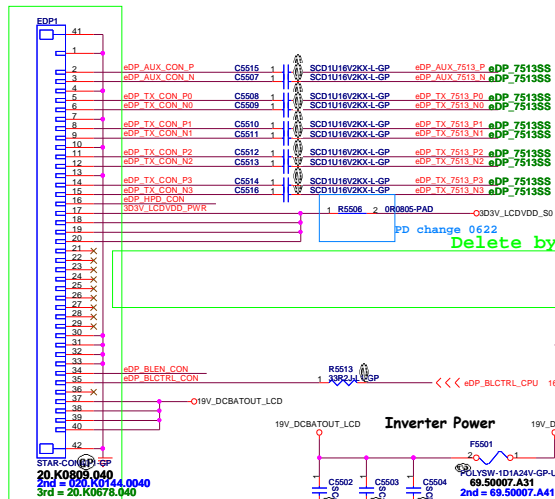




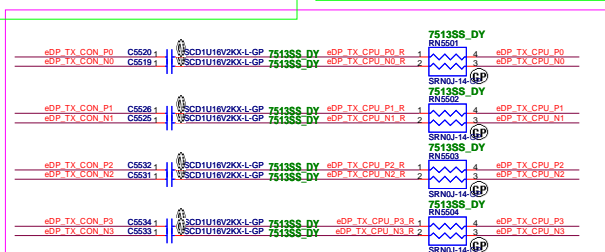


1D5V\_S0

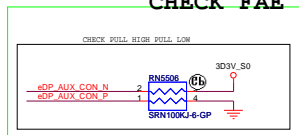




Delete USB P8 and I2C0 by Royee 20150202

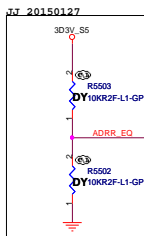
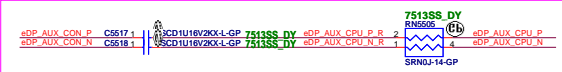


~~CHECK FAE~~

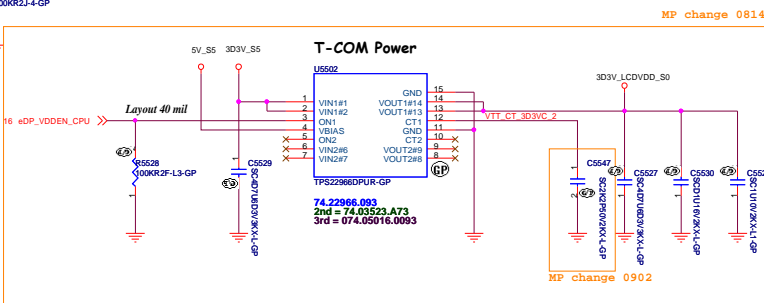
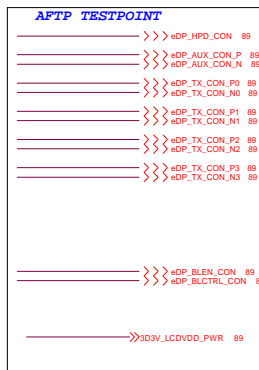
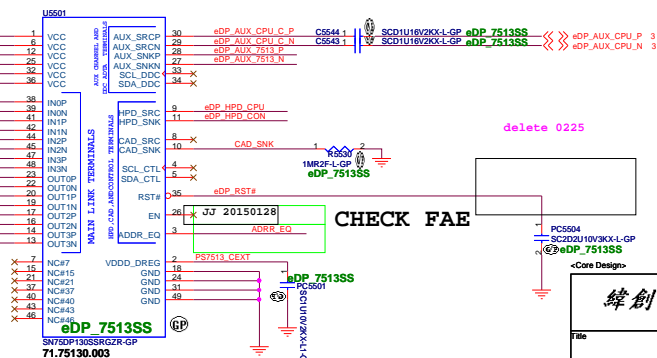


UN 0225

```
modify 0304 swap 0303
```



ADDR_EQ	3	3-level Input	I <sup>2</sup> C Target Address Select and EQ Configuration Input. If the I <sup>2</sup> C bus is used, this input setting selects the I <sup>2</sup> C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.
---------	---	---------------	--

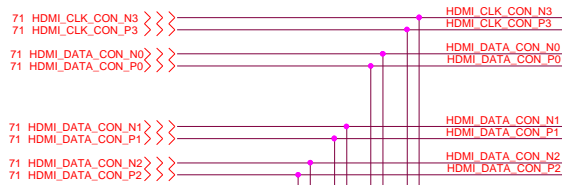


delete 0225

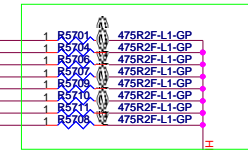
**CHECK FAE**

SSID = VIDEO

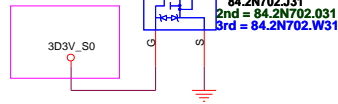
# HDMI Level Shifter & CONNECTOR



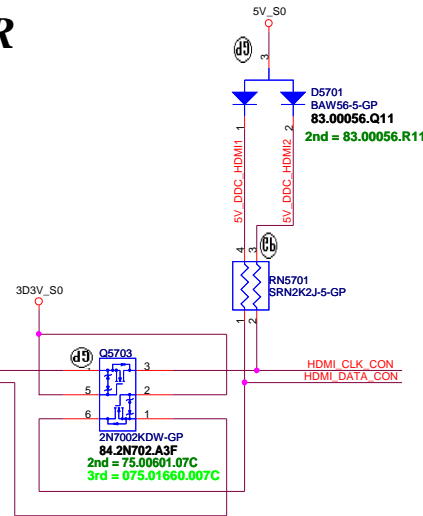
Change from 470 to 475 0204



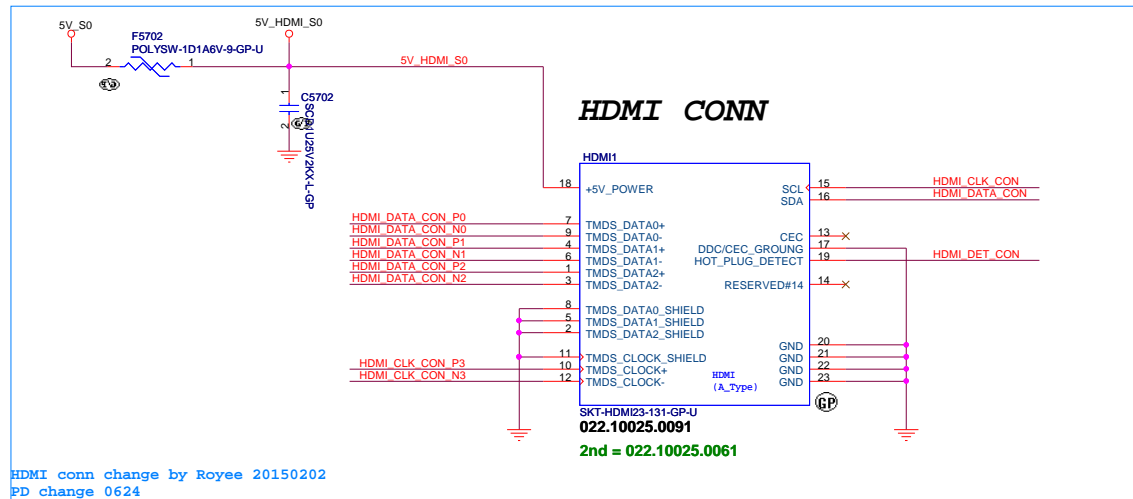
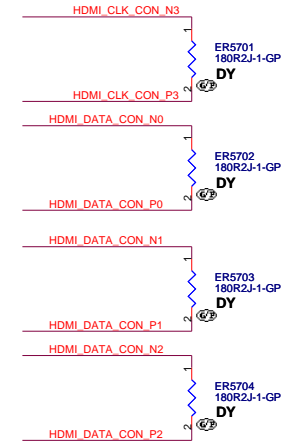
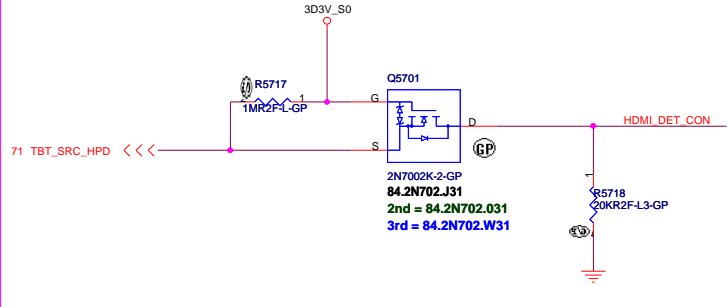
Change TBT 0209



71 TBT\_HDMI\_DDC\_CLK <<<  
71 TBT\_HDMI\_DDC\_DATA <<<



Change TBT 0209



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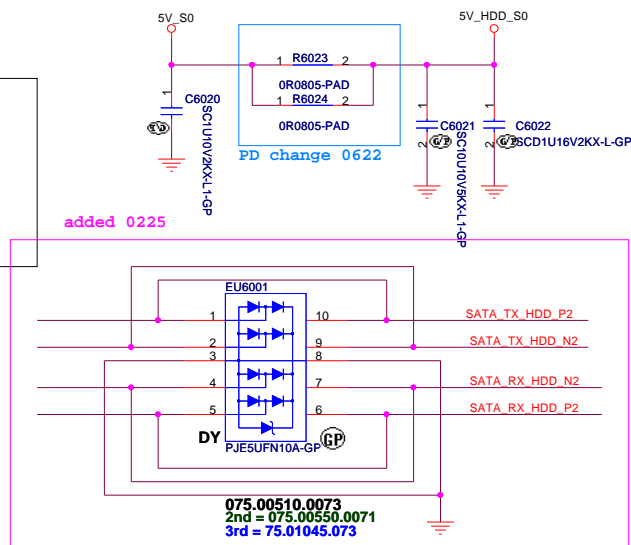
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Title			HDMI Level Shifter/Conn
Size	Document Number	Rev	1M
Custom	Newgate		
Date:	Tuesday, August 18, 2015	Sheet	57 of 105

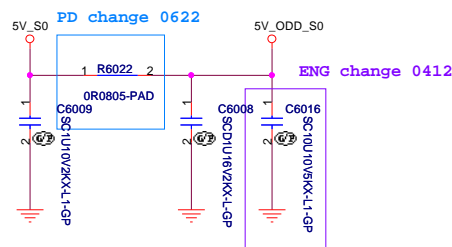
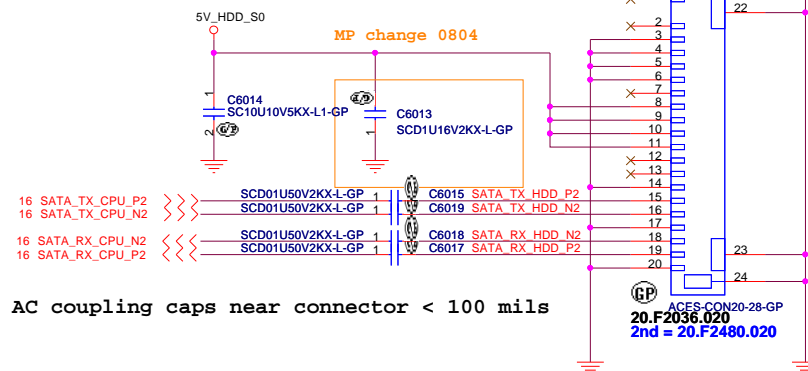
SSID = SATA

### AFTP TESTPOINT

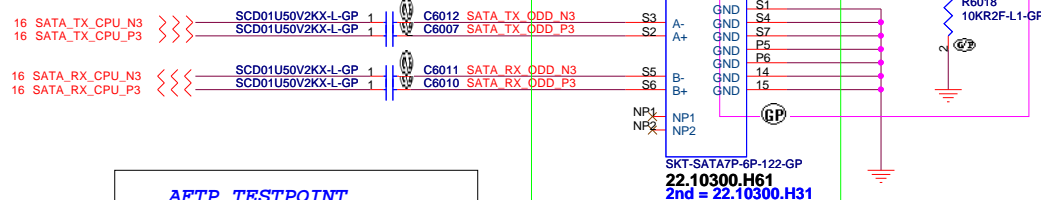
89 SATA\_TX\_HDD\_P2 >>>=  
89 SATA\_TX\_HDD\_N2 <<<=  
89 SATA\_RX\_HDD\_N2 <<<=  
89 SATA\_RX\_HDD\_P2 >>>=



## SATA HDD Connector



follow SLU 0225



### AFTP TESTPOINT

89 SATA\_TX\_ODD\_N3 >>>=  
89 SATA\_TX\_ODD\_P3 <<<=  
89 SATA\_RX\_ODD\_N3 <<<=  
89 SATA\_RX\_ODD\_P3 >>>=

PIN DEFINE	CONN	FFC
GND		20
GND	P5/P6	19
GND		18
ODD_DA	P4	17
NC		16
5V		15
5V		14
5V		13
5V	P2/P3	12
5V		11
5V		10
NC		9
PRSENT	P1	8
GND	S7	7
RXP	S6	6
RXN	S5	5
GND	S4	4
TXN	S3	3
TXP	S2	2
GND	S1	1

ODD1 conn change by Royee 20150202

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Title	HDD/ODD	
Size	Document Number	Rev
A3		1M
Date:	Tuesday, August 18, 2015	Sheet 60 of 105

## NGFF Connector (802.11a/b/g/n)

```

>>> PCIE_WAKE#_WLAN 89
WLAN_CLKREQ_CPU# 18,89
<<< WLAN_CLK_CPU# 18,89
WLAN_CLK_CPU 18,89
>>> PCIE_RX_PCH_N3 15,89
PCIE_RX_PCH_P3 15,89
<<< PCIE_TX_CON_N3 89
PCIE_TX_CON_P3 89
>>> USB_PCH_PN7 15,89
USB_PCH_PP7 15,89

```

```

===== >>> WIFI_RF_EN_CON      89
===== >>> BLUETOOTH_EN      24,89
===== >>> WLAN_RST#      89

===== <<< E51_RXD_R      89
===== <<< E51_TXD_R      89

```

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Title			
<b>Mini card-WLAN</b>			
Size Custom	Document Number		Rev
	<b>Newgate</b>		<b>1M</b>
Date:	Tuesday, August 18, 2015	Sheet 61 of	105

SSID = m-SATA

# Mini Card Connector (NGFF m-SATA)

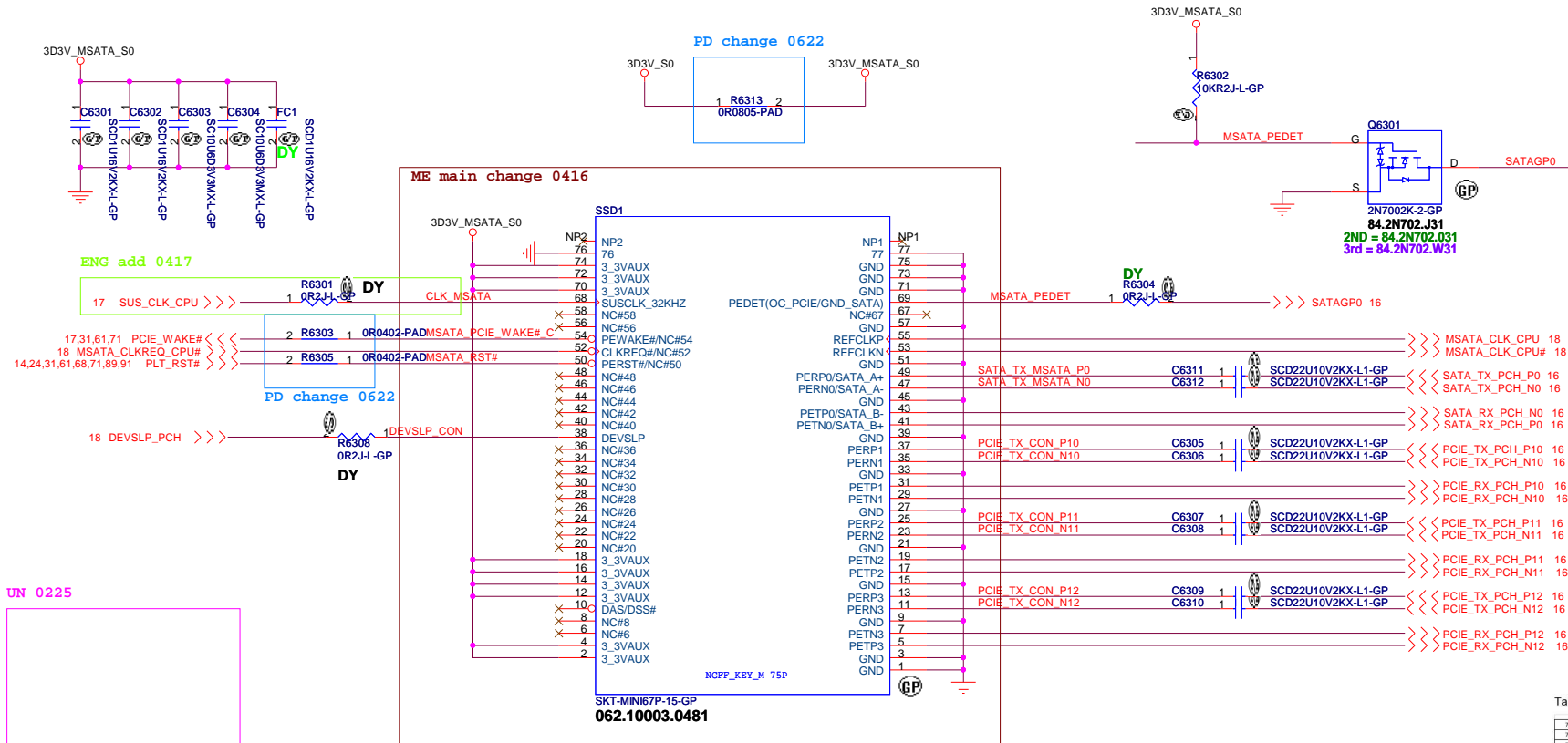


Table 34-5. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	1.0V	SSD	75	1.0V
72	1.0V	SSD	73	1.0V
70	1.0V	SSD	71	1.0V
68	1.0V	SSD	69	1.0V
66	1.0V	SSD	67	1.0V
64	1.0V	SSD	65	1.0V
62	1.0V	SSD	63	1.0V
60	1.0V	SSD	61	1.0V
58	1.0V	SSD	59	1.0V
56	1.0V	SSD	57	1.0V
54	1.0V	SSD	55	1.0V
52	1.0V	SSD	53	1.0V
50	1.0V	SSD	51	1.0V
48	1.0V	SSD	49	1.0V
46	1.0V	SSD	47	1.0V
44	1.0V	SSD	45	1.0V
42	1.0V	SSD	43	1.0V
40	1.0V	SSD	41	1.0V
38	1.0V	SSD	39	1.0V
36	1.0V	SSD	37	1.0V
34	1.0V	SSD	35	1.0V
32	1.0V	SSD	33	1.0V
30	1.0V	SSD	31	1.0V
28	1.0V	SSD	29	1.0V
26	1.0V	SSD	27	1.0V
24	1.0V	SSD	25	1.0V
22	1.0V	SSD	23	1.0V
20	1.0V	SSD	21	1.0V
18	1.0V	SSD	19	1.0V
16	1.0V	SSD	17	1.0V
14	1.0V	SSD	15	1.0V
12	1.0V	SSD	13	1.0V
10	1.0V	SSD	11	1.0V
8	1.0V	SSD	9	1.0V
6	1.0V	SSD	7	1.0V
4	1.0V	SSD	5	1.0V
2	1.0V	SSD	1	1.0V

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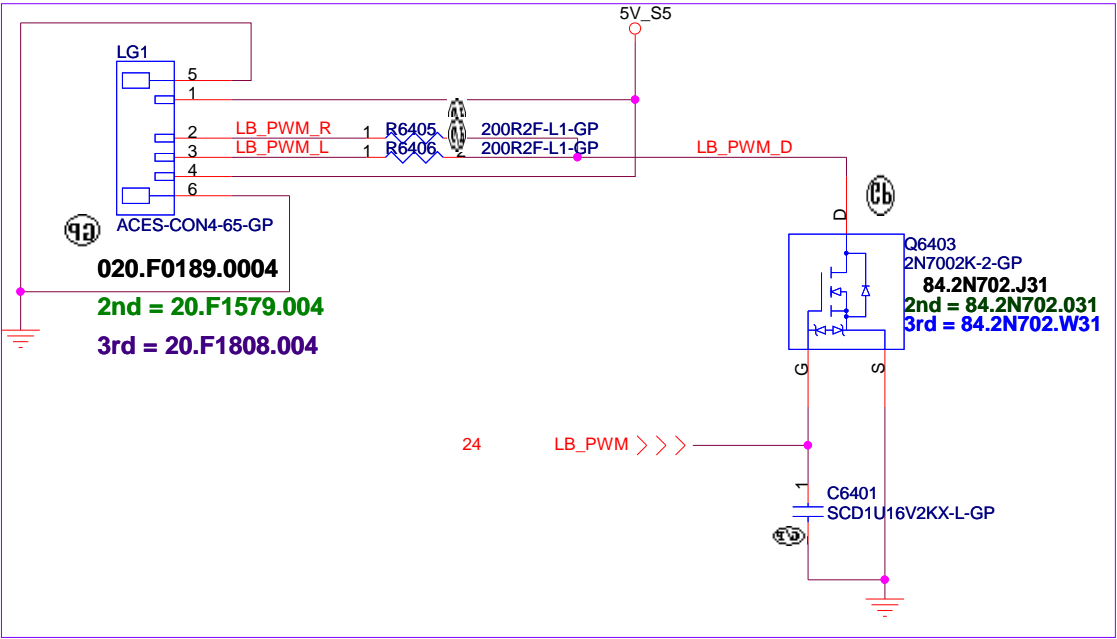
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Title			
SSD-NGFF			
Size	Document Number	Rev	
A3	Newgate	1M	
Date:	Tuesday, August 18, 2015	Sheet	63 of 105

SSID = User.Interface

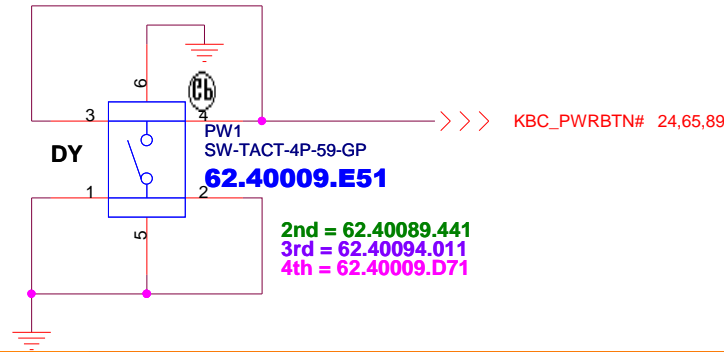
ENG change 0412

LG1 conn ENG change 0412



MP change 0804

## Power Button



LB\_PWM\_R <<< LB\_PWM\_R 89  
LB\_PWM\_L <<< LB\_PWM\_L 89

AFTP TESTPOINT

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Title		
LED Bard/Power Button		
Size	Document Number	Rev
A4	Newgate	1M
Date:	Tuesday, August 18, 2015	Sheet 64 of 105

I2C Addr. = 0X2C (Synaptics)



```

_____>>>EC_TP_CLK_C 89
_____>>>EC_TP_DATA_C 89
_____>>>I2C1_DATA_TP 89
_____>>>I2C1_CLK_TP 89
_____>>>TP_IN#_R 89
_____>>>TP_LID_CLOSE# 89

```

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## CHECK WITH SPEC



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VCC Pin 1

NC Pin 2

VCC Pin 3

GND Pin 4

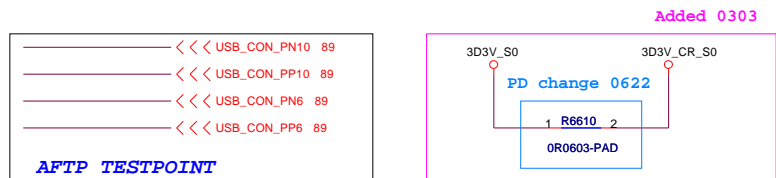
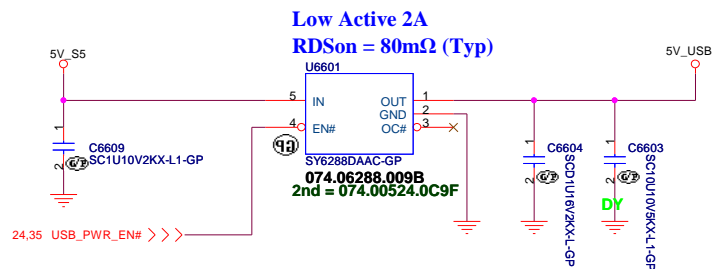
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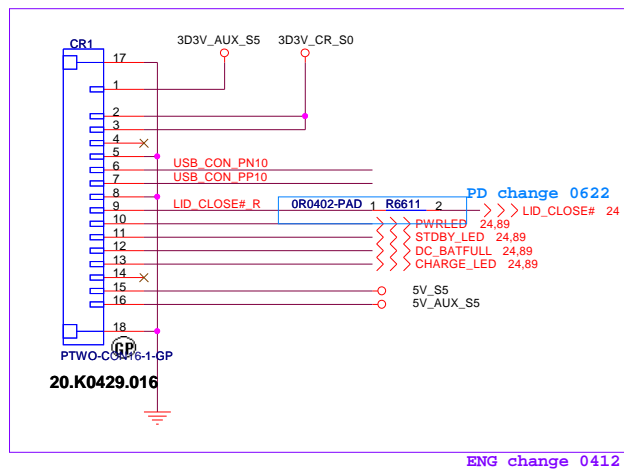
Title **LED Bard / Power Button**

Size	Document Number	Rev
Custom	<b>Newgate</b>	<b>11</b>
Date:	Tuesday, August 18, 2015	Sheet 65 of 105

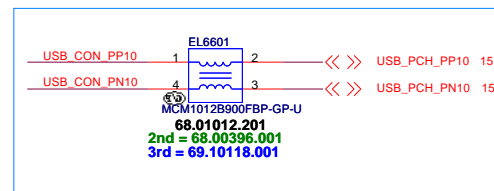




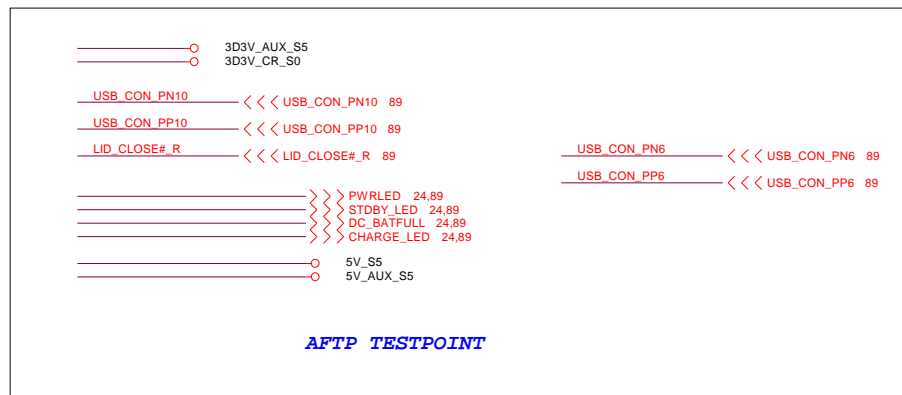
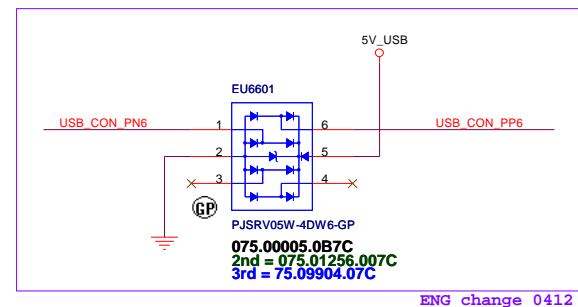
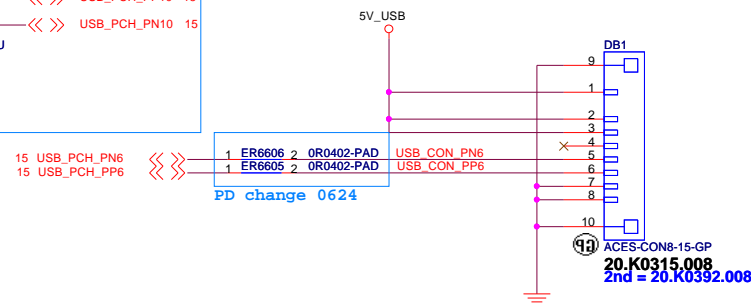
## Card Reader



PD change 0626



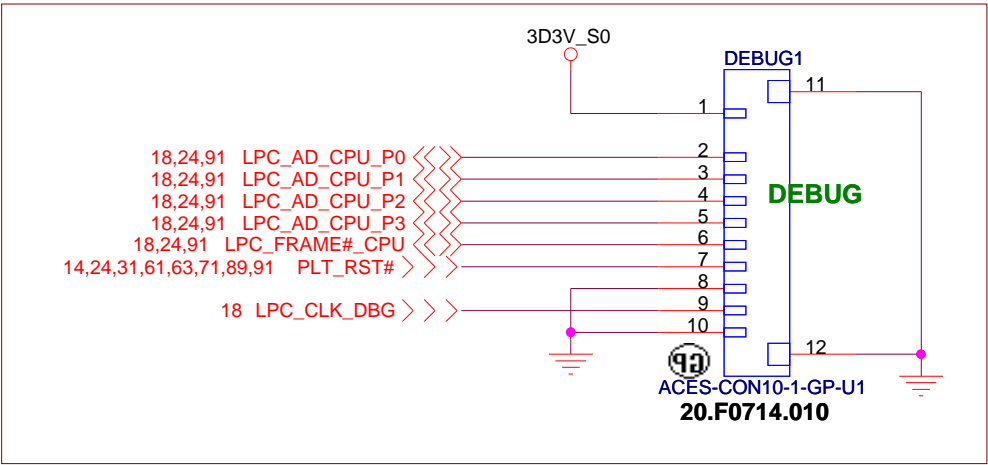
## USB2.0



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Title	
IO Board Connector	
Size A3	Document Number
Newgate	
Date: Tuesday, August 18, 2015	Sheet 66 of 105
Rev 1M	

ENG change 0416



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Title			
<div>Debug connector</div>			
Size A	Document Number		Rev
	Newgate		1M
Date:	Tuesday, August 18, 2015	Sheet 68 of	105

```
SSID = User.Interface
```

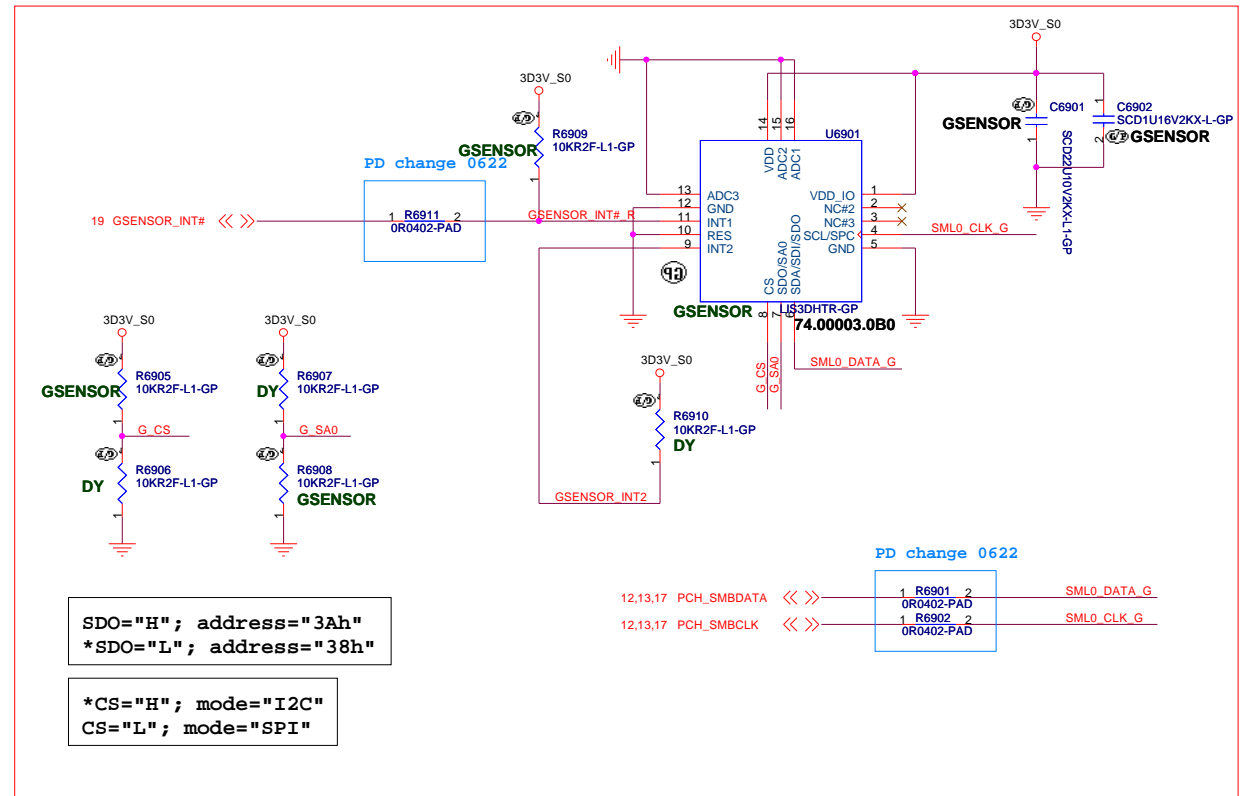
## G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Title	<b>G-SENSOR</b>
-------	-----------------

Size A3	Document Number <b>Newgate</b>
Date:	Tuesday, August 18, 2015

Rev  
**1M**

Date: Tuesday, August 18, 2015 Sheet 69 of 105

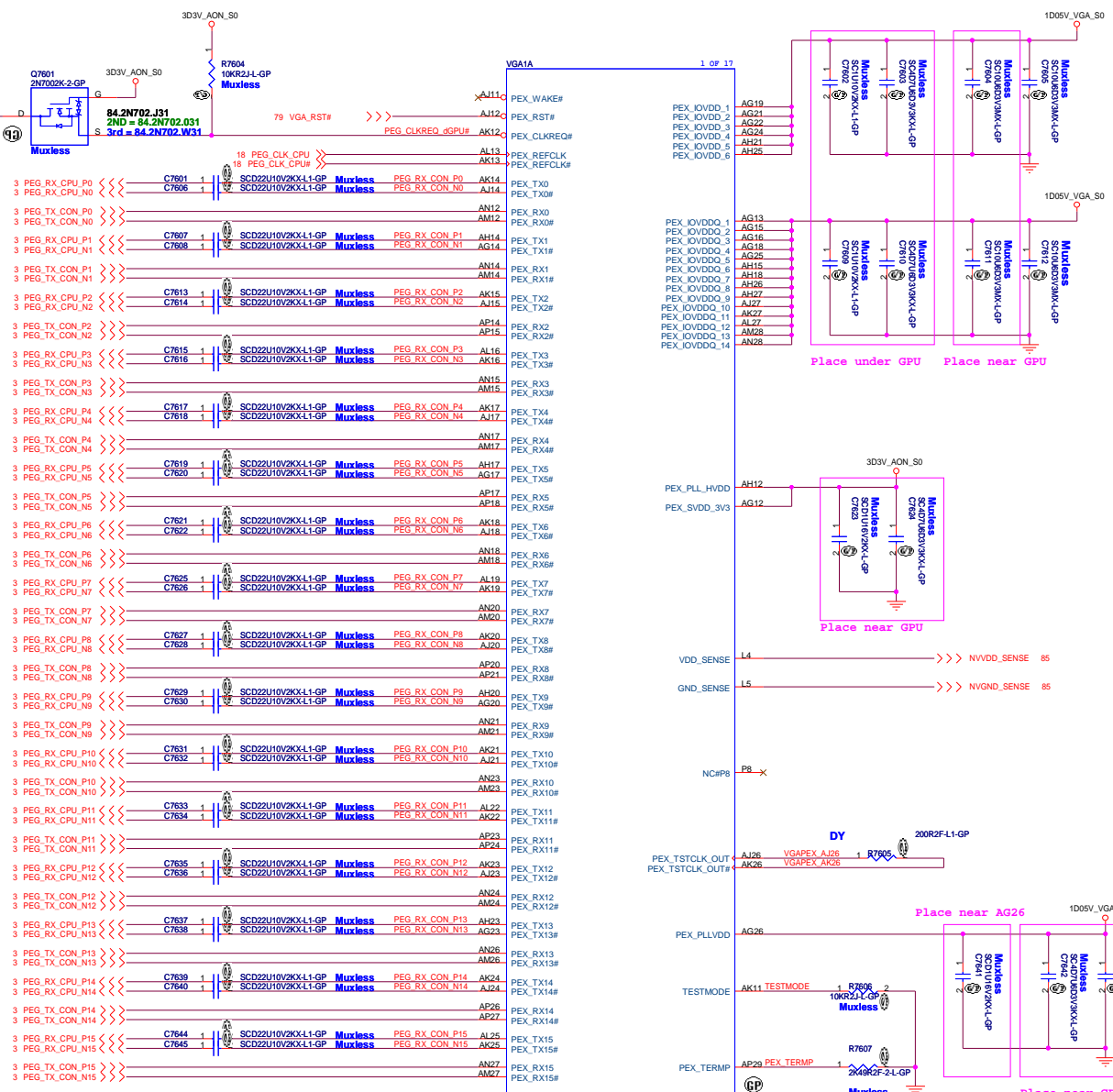
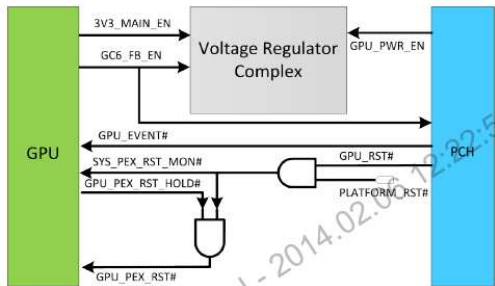
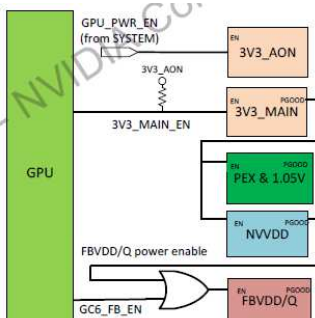




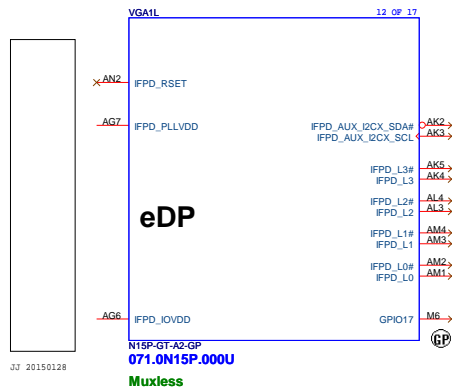
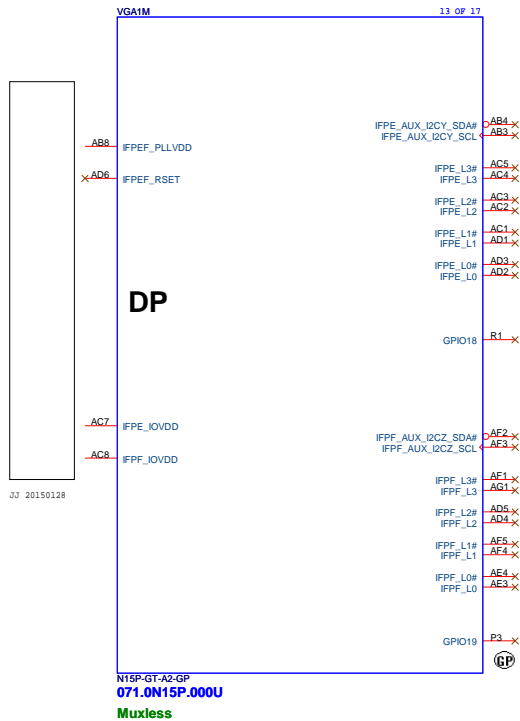
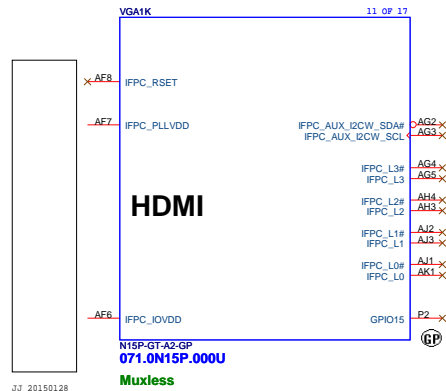
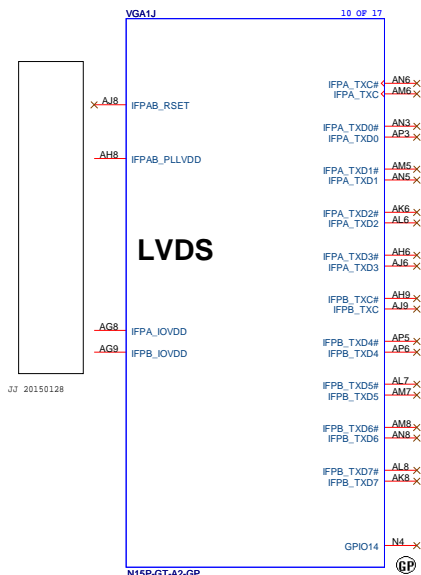


14.79 DGPU\_HOLD\_RST# >>> 1 R7903 VGA\_RST#  
OR2J-L-GP  
NON\_GC6

UN 0225



071.0N15P.000U  
Muxless







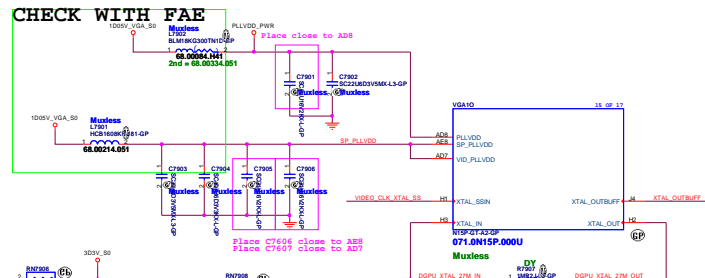
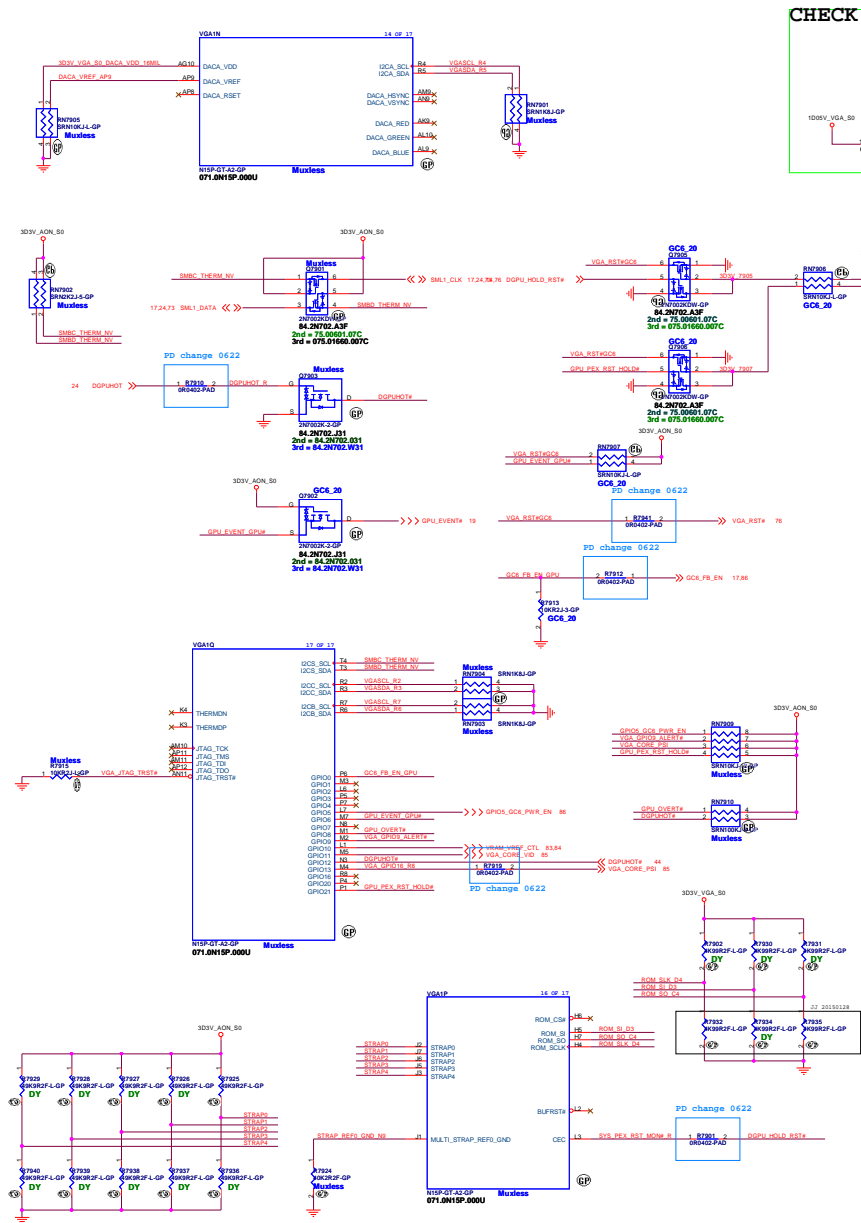


Table 8. N16P-GX GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V / 1.35V	128Mx16	Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	1347	Production ready
			Micron	EDW2032BBG-6A-F	B-die	0x5	2500	N/A	Production ready
			Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production ready
		256Mx16	Micron	EDW4032BAG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production ready
		128Mx32	Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Post production ready
			Micron	EDW4032BAG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production ready
			Hynix	H5G04H24AJR-T2C	A-die	0x6	2500	N/A	Post production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x8	2500	N/A	Post production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	2500	N/A	Post production candidate

Note:

1. For N16P-GX, the maximum allowable memory case temperature is 85 °C.
2. 8 Gb/s is supported in x32 configuration only (no x16 support planned).

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

4.99Kohm 64.49915.6DL  
10Kohm 64.10025.10L  
15Kohm 64.15025.6DL  
20Kohm 64.20025.6DL  
24.9Kohm 64.24925.6DL  
30.1Kohm 64.30125.6DL  
34.8Kohm 64.34825.6DL  
45Kohm 64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_CLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_S1	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	DEVID_SEL	PCIE_CFG	SMU_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_A0H and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_A0H and pull-down to GND for forward compatibility.			
STRAP2				
STRAP3				
STRAP4				

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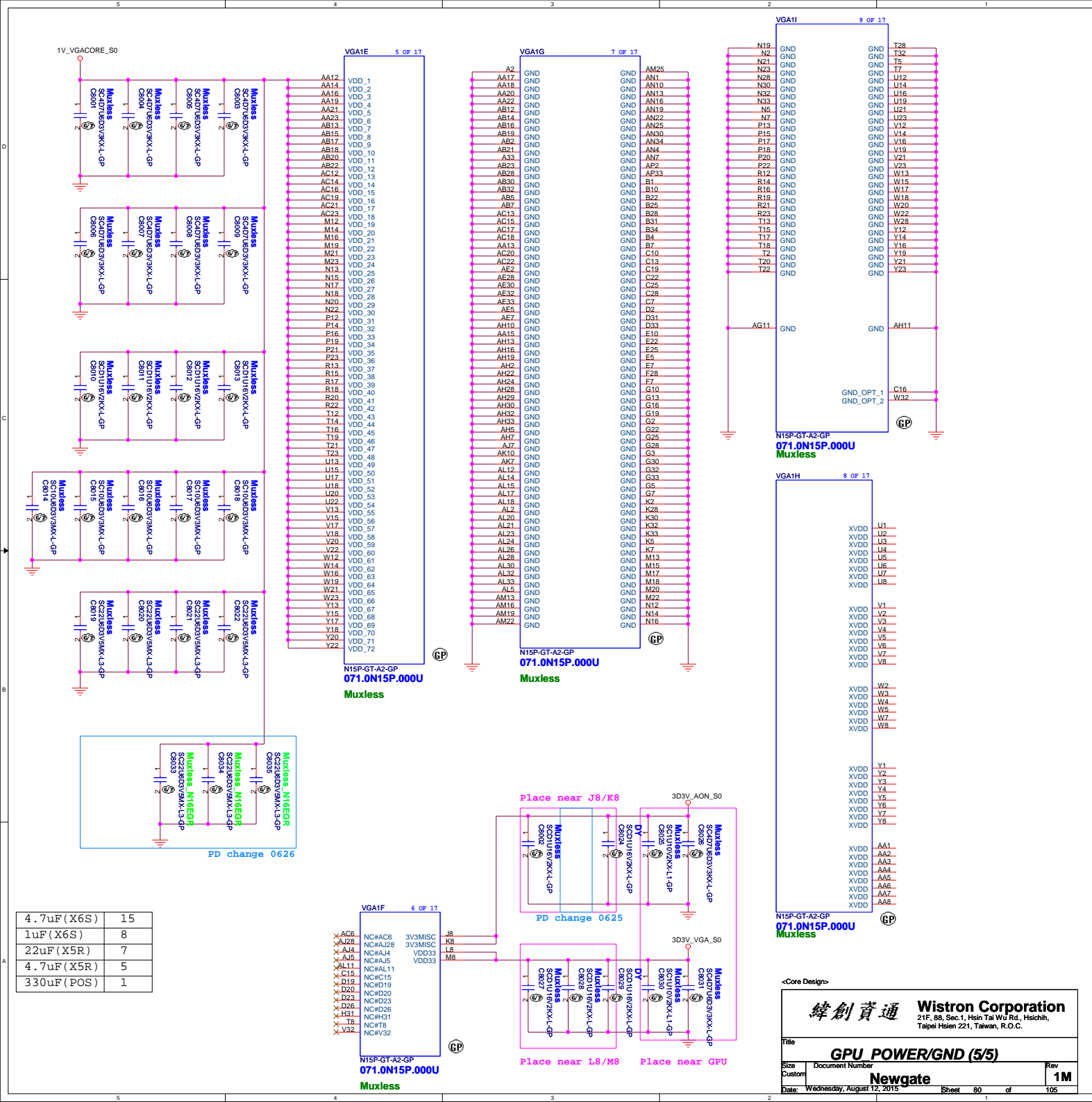
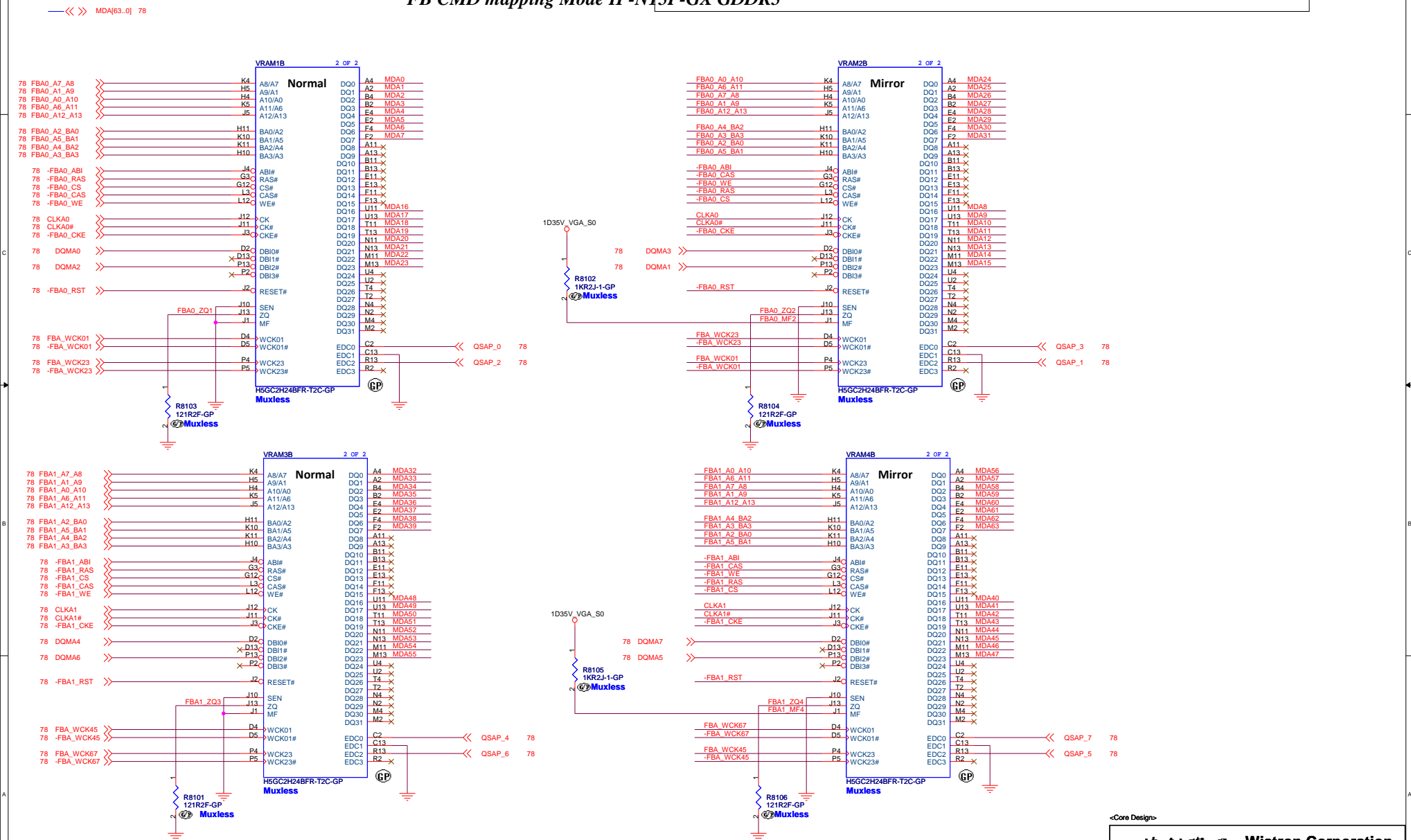


TABLE GDDR5 VIDEO MEMORY				
72.05224.A0U		72.20325.B0U		
	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

### FB CMD mapping Mode H -N15P-GX GDDR5

## LOGIC

CHECK PM AVL



<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
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**VRAM 1,2 (1/4)**Size  
Custom

Document Number
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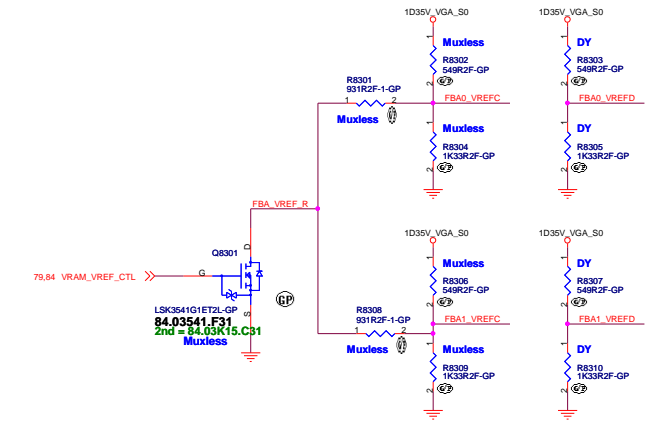
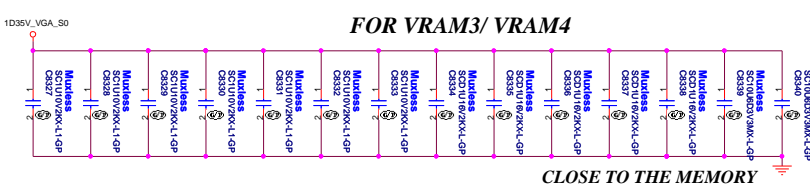
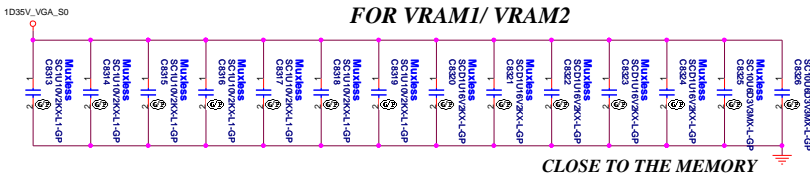
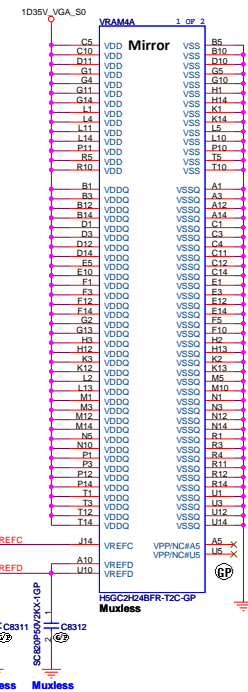
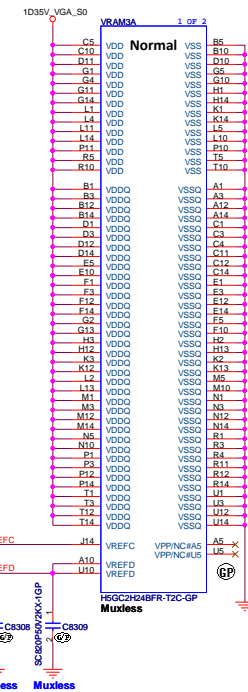
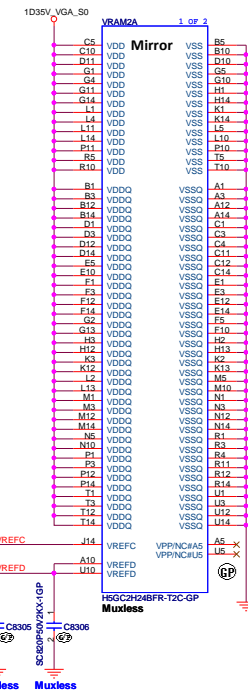
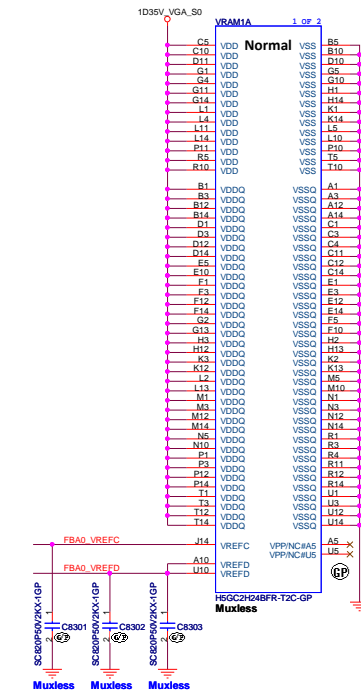
**Newgate**

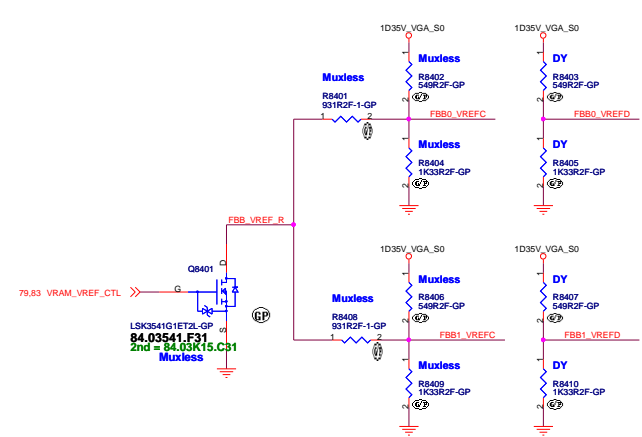
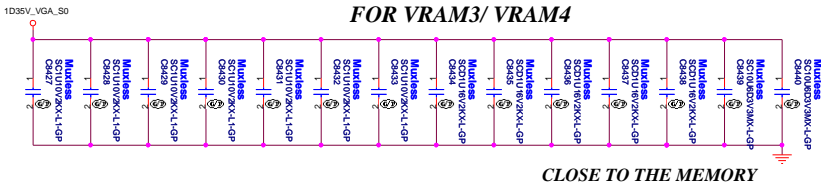
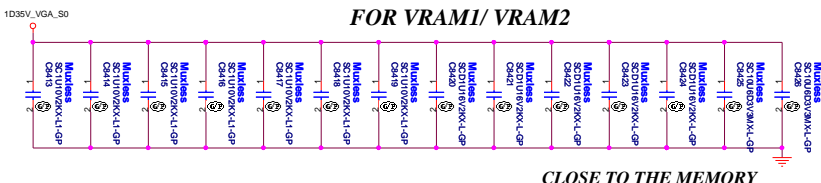
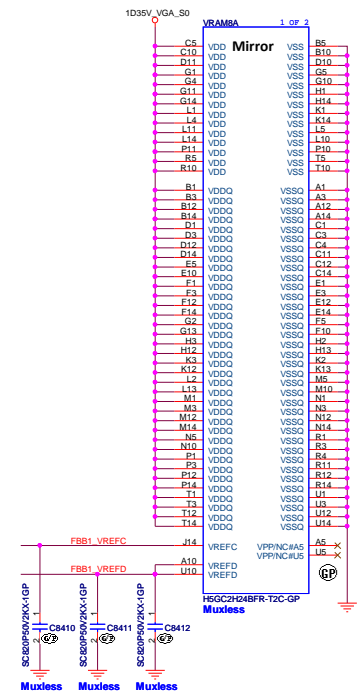
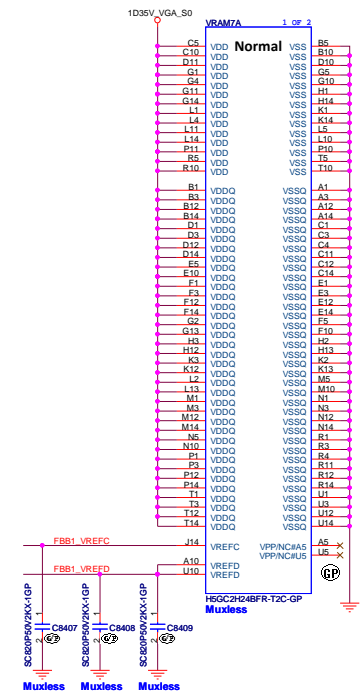
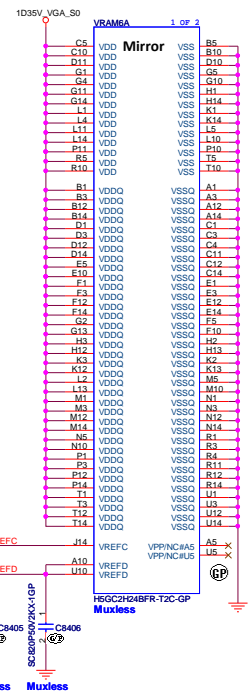
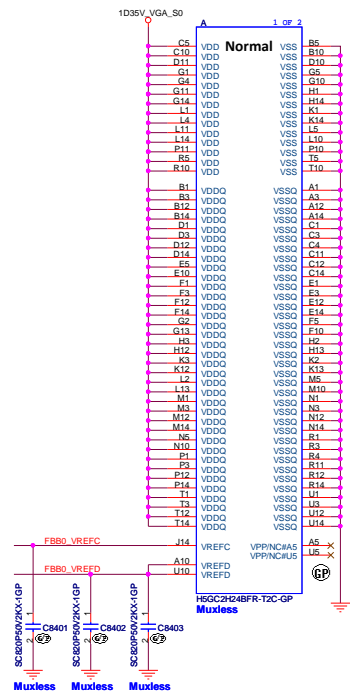
Rev	1M
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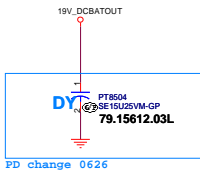
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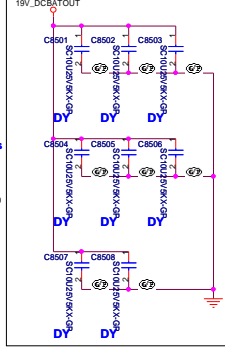
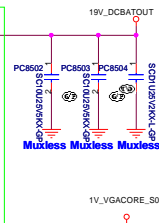
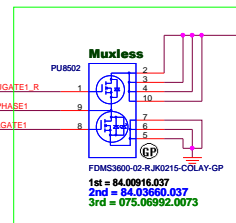


VGA : N15P 6X  
Config : B  
EDP-Continuous : 49A  
EDP-Peak : 76A

CHECK SPEC

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF

Add 3rd 0423

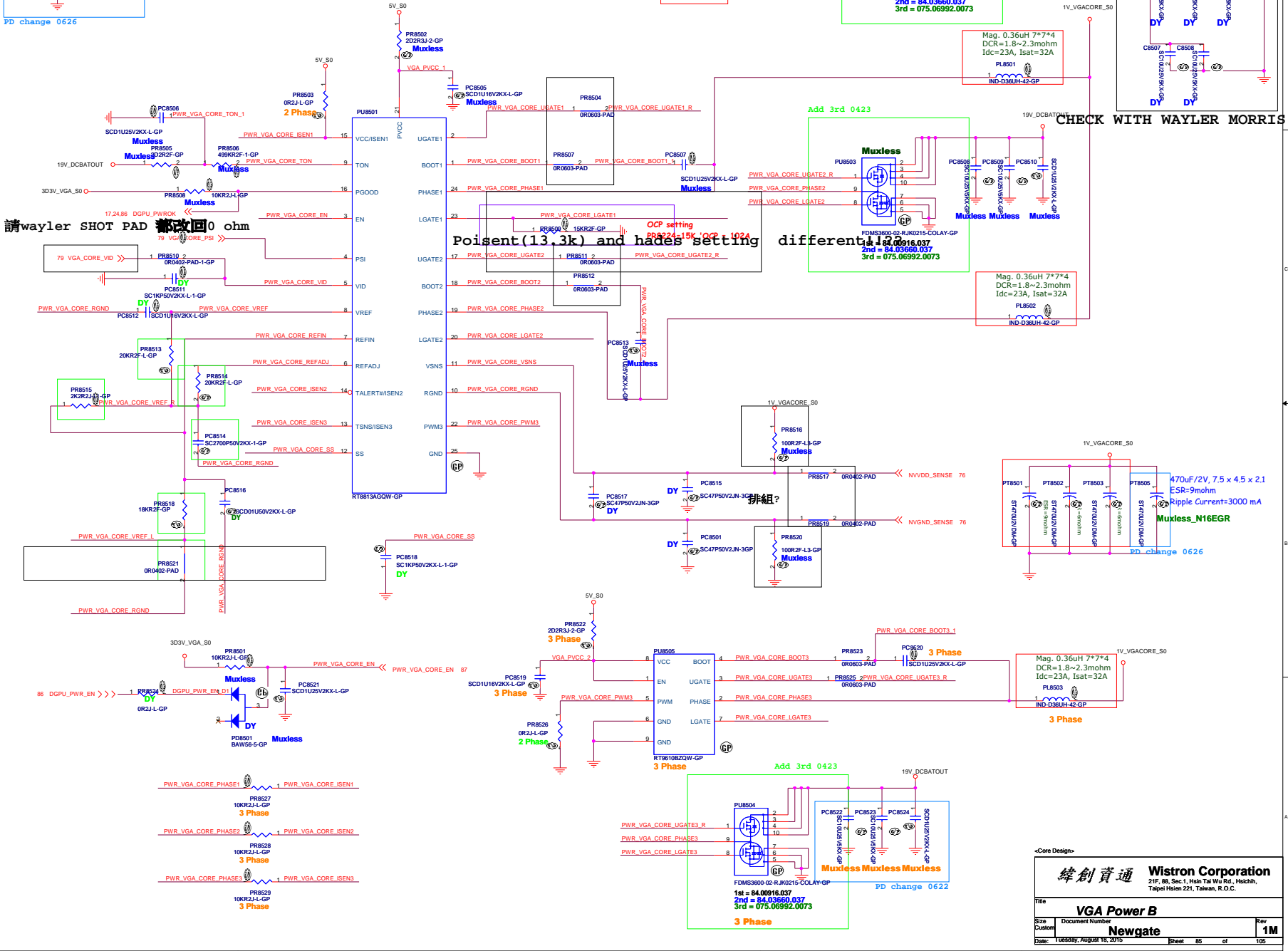


請wayler SHOT PAD 都改回0 ohm

Poisent(13.3k) and hades setting

different 1.640916.037

CHECK WITH WAYLER MORRIS



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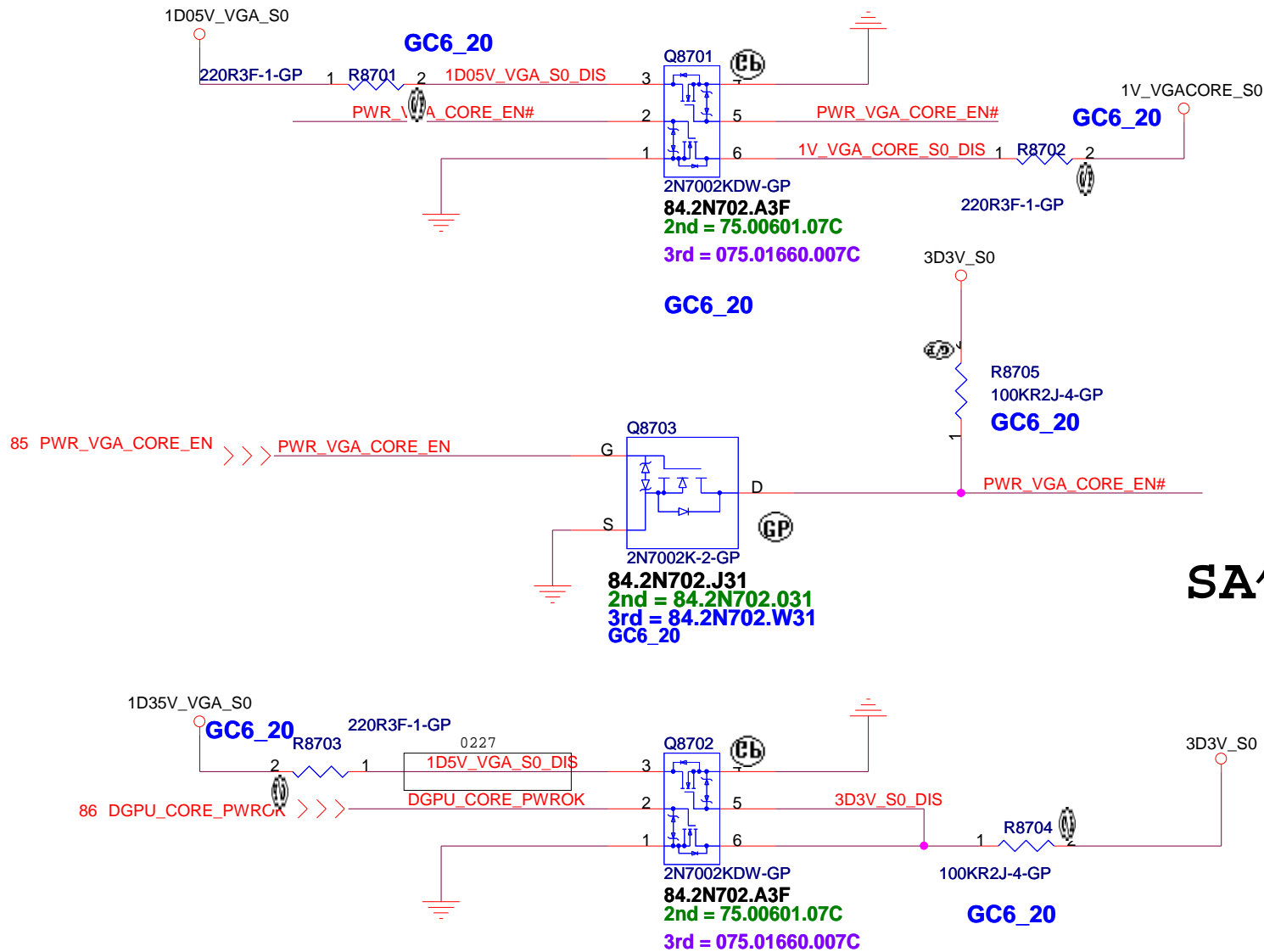
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File	VGA Power B	Rev	1M
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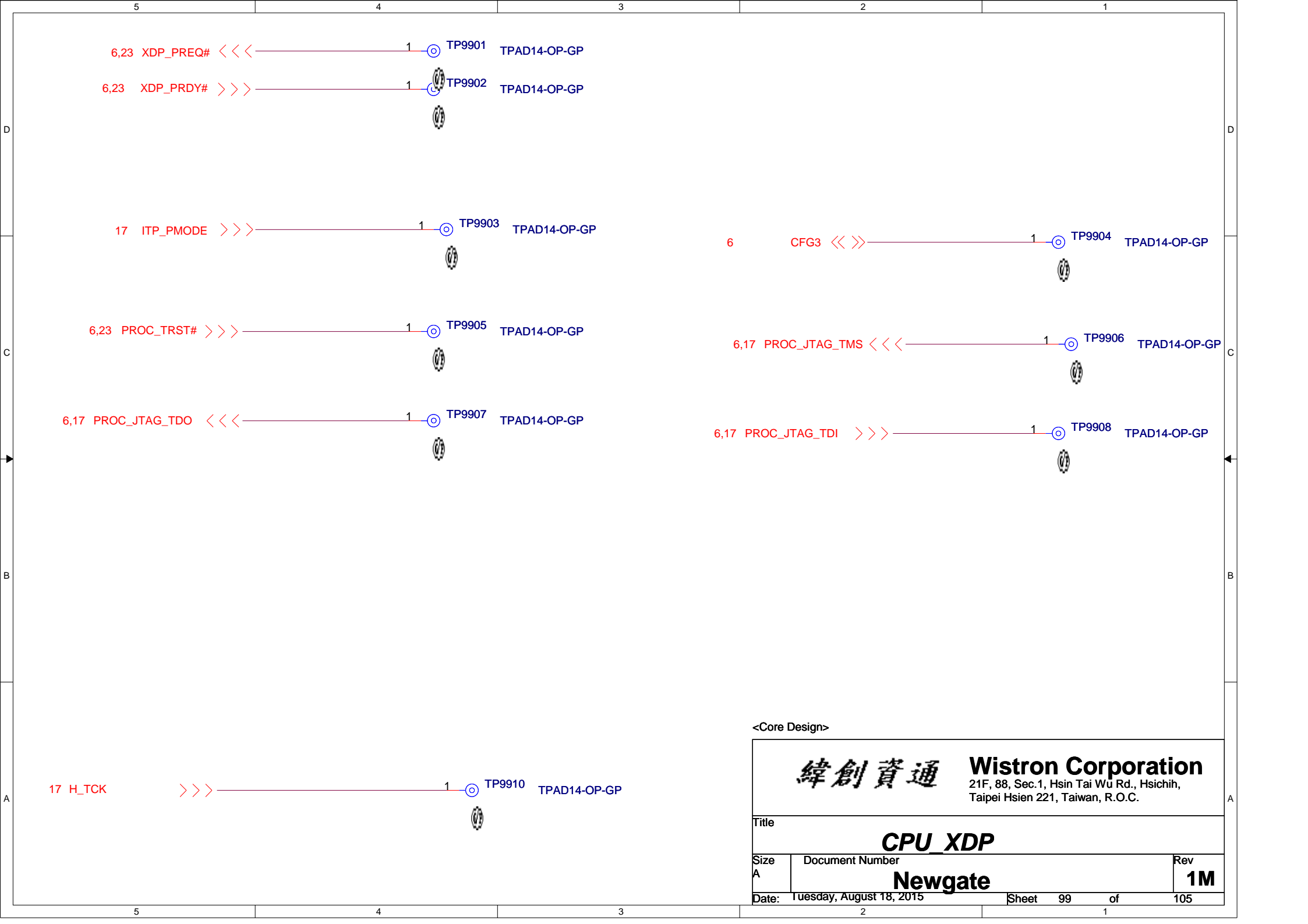




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Title			
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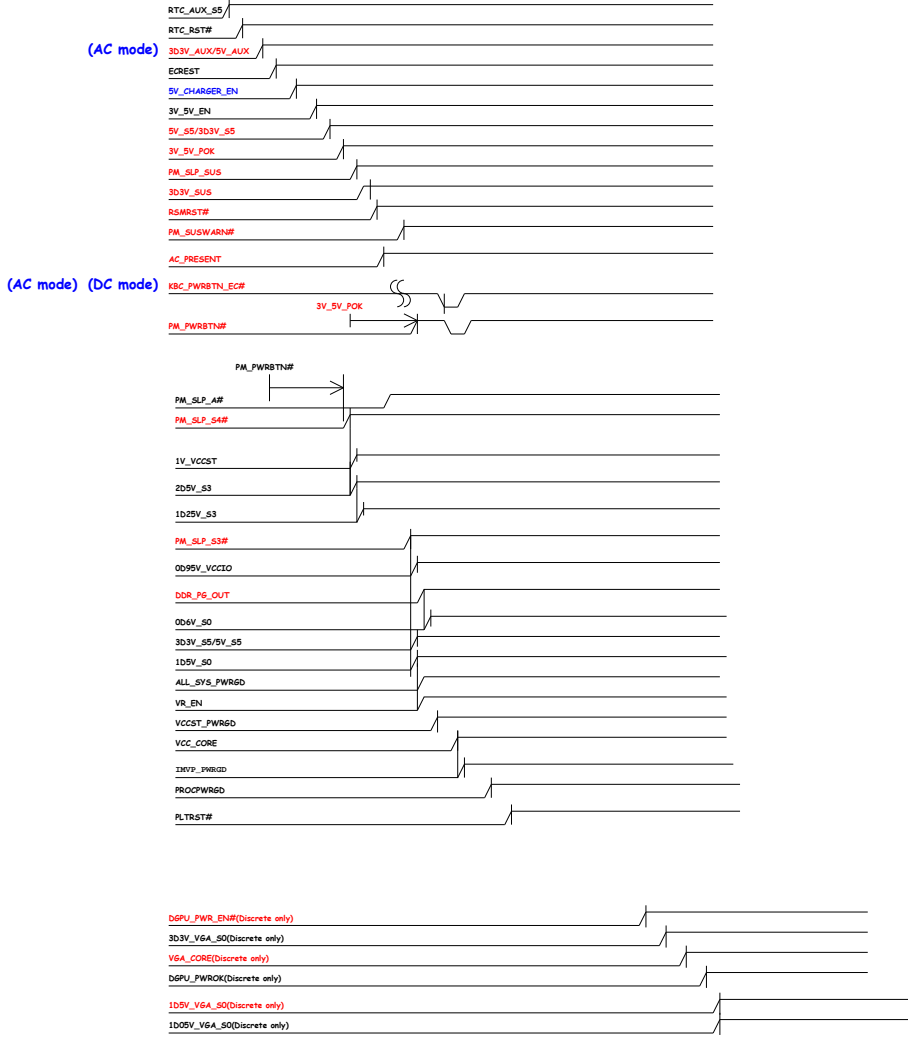
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D				D
C				C
B				B
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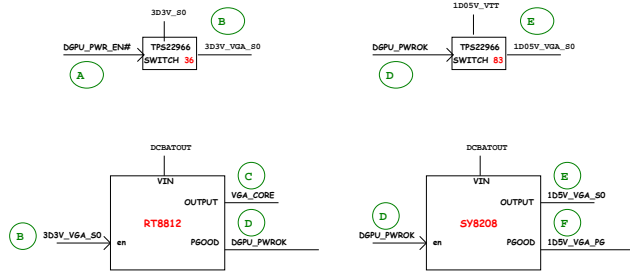
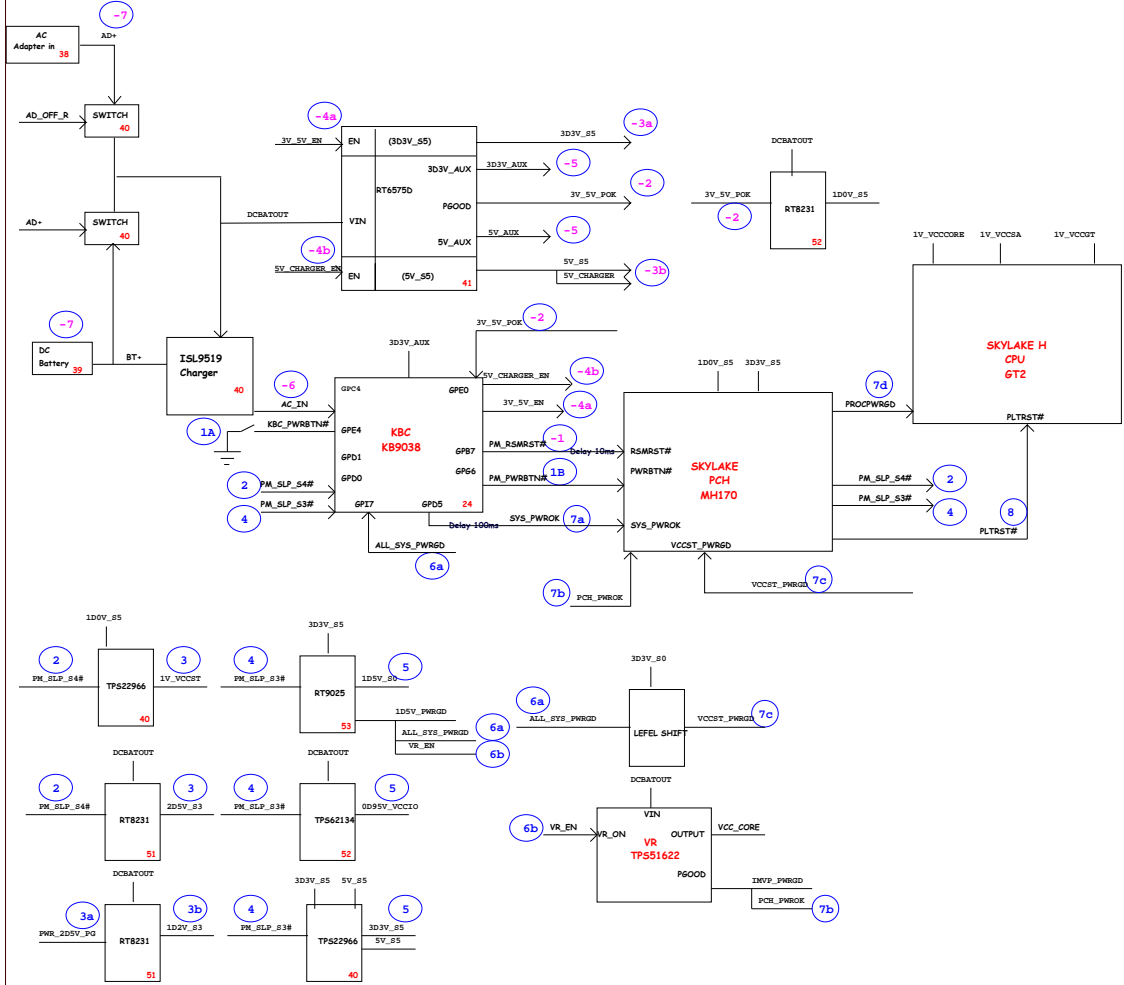
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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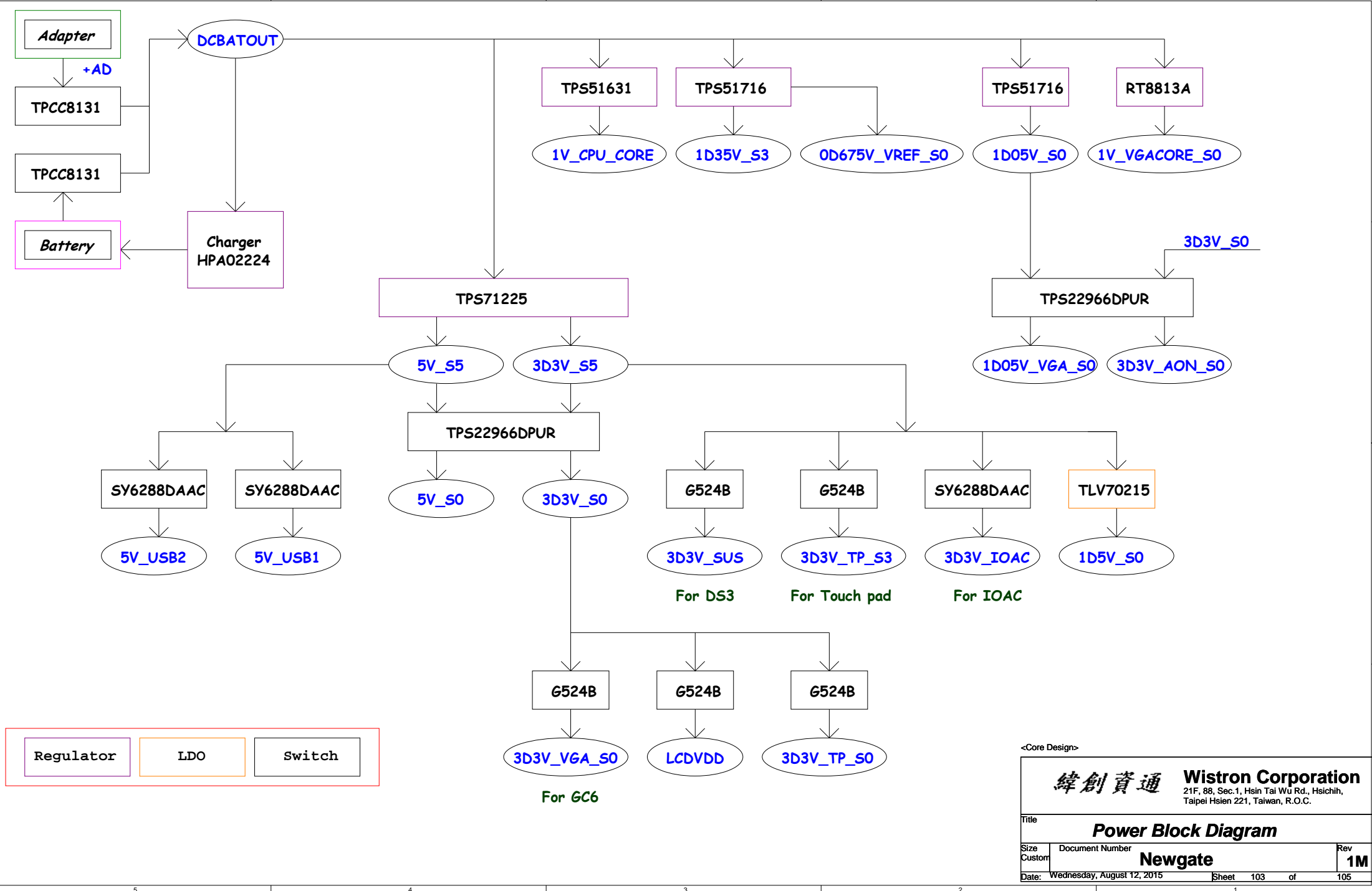
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Intel-Power Up Sequence



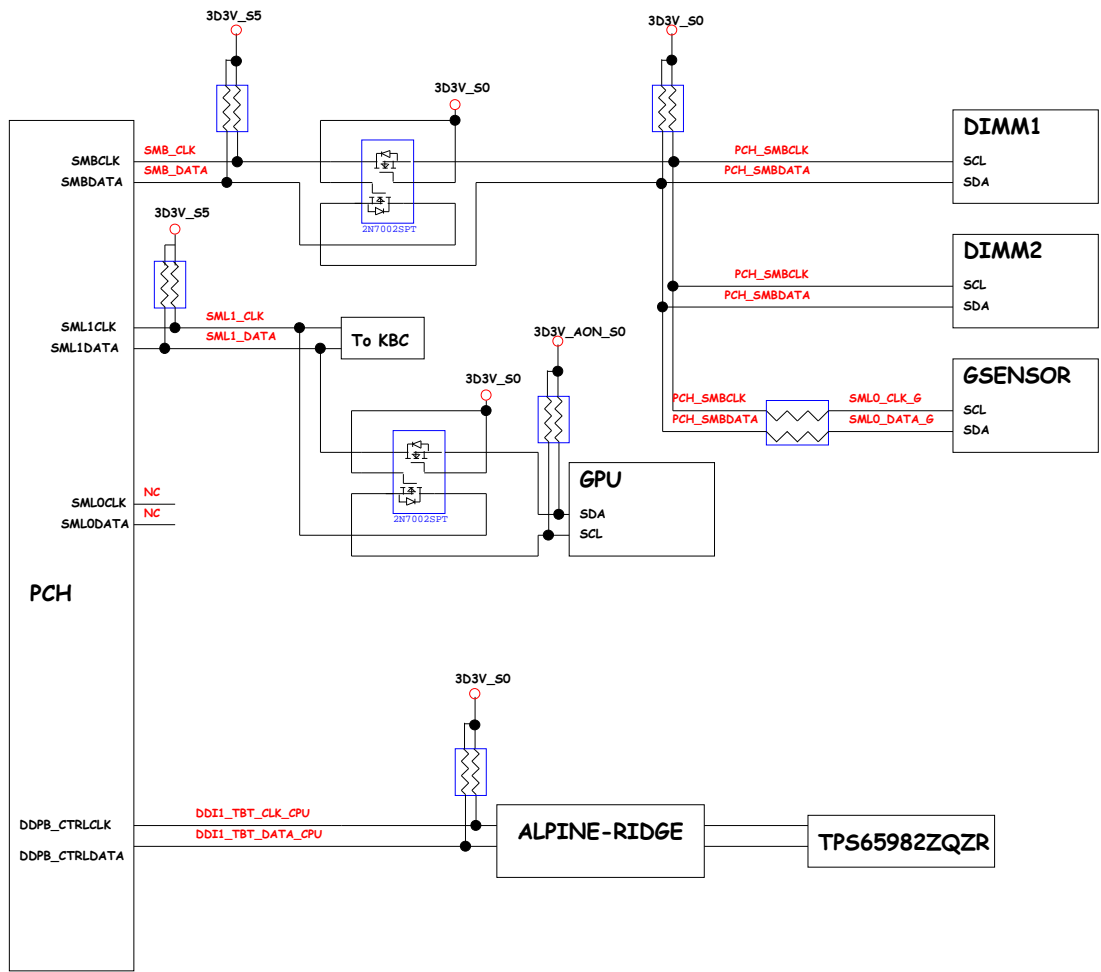
SKYLAKE H POWER UP SEQUENCE DIAGRAM



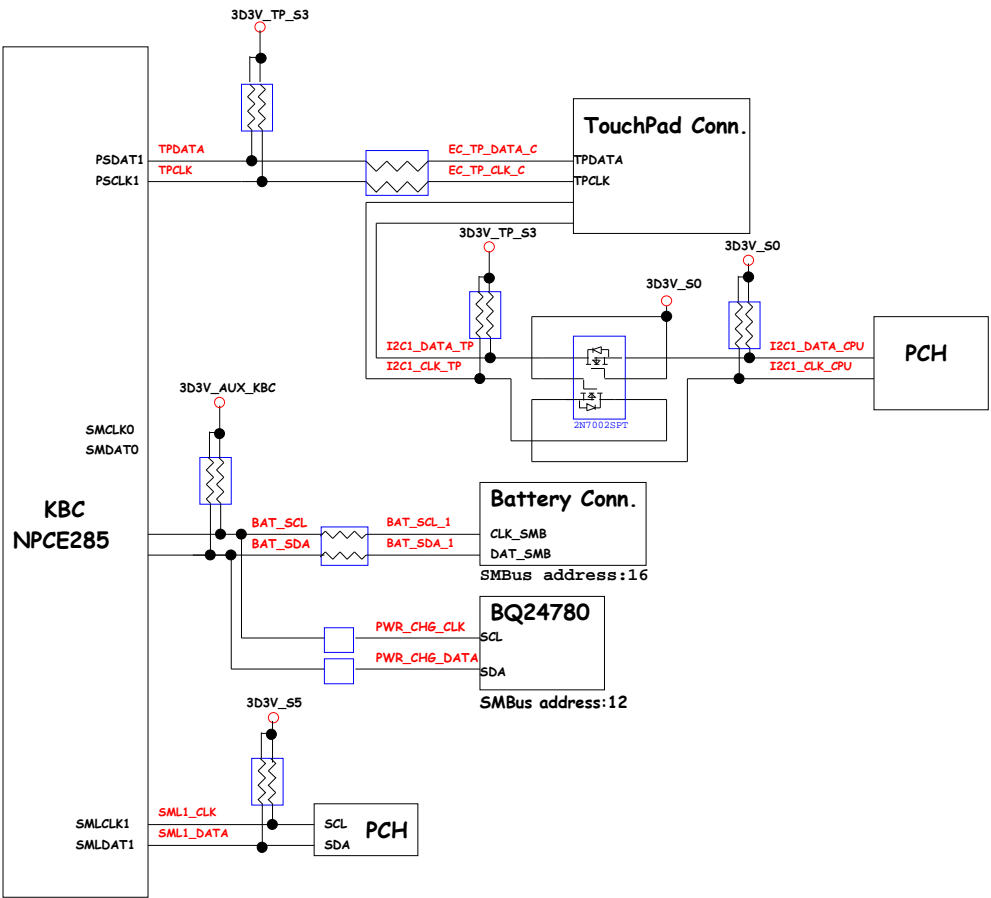




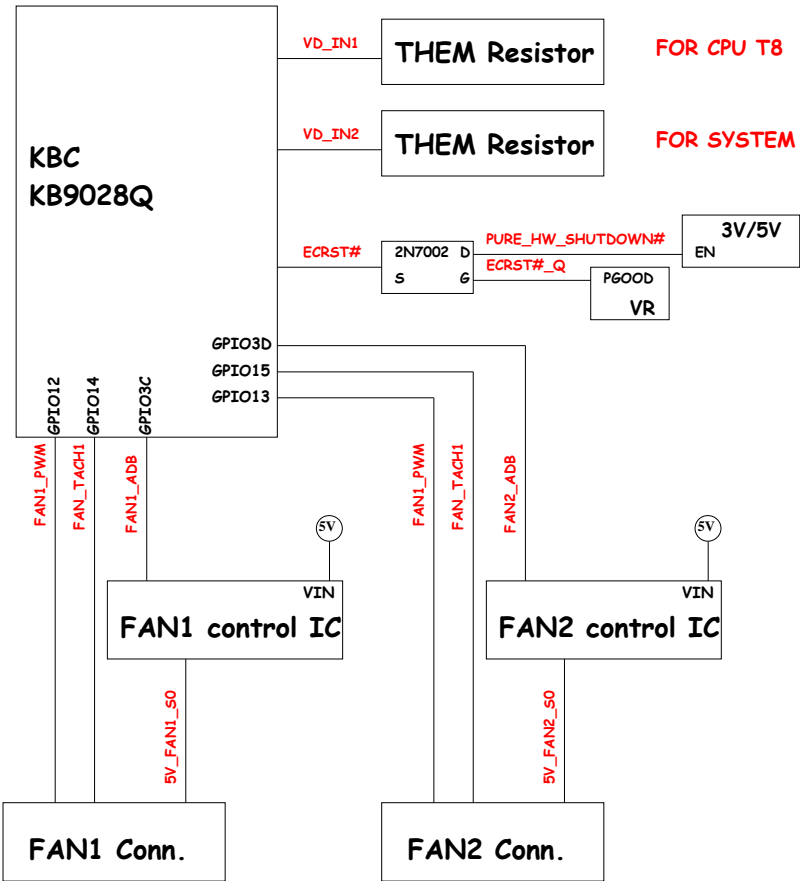
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

