Z06 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

DDR PWR TPS5116 P34 | CHARGER ISL6251 P30
THERMAL PROTECTION P37 | 3/5V SYS PWR ISL6237 P31
1.5V PWR DISCHARGER P36 | CPU CORE PWR OZ8116LN P33
VGA CORE OZ8118 P35 | +1.05V RT8202 P32

X'TAL 14.318MHz
CLOCK GENERATOR
ICS:
SELGO: SLG8SP512TTR
P2

Penryn 479
uFCPGA
P3, P4

Thermal Sensor
(G780P81U) P3

Fan Driver
(G991) P24

FSB
667/800/1067 Mhz

NVIDIA N10M-GE1
VRAM 512MB
P17-P22

PCIE 16X

EXT_LVDS
EXT_CRT
EXT_HDMI

SWITCH CIRCUIT
P23

CRT P23
LVDS P23
HDMI P23

HDMI switch (PS8122) P23

DDRII
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR2
667/800 MHz

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

LVDS
RGB
INT_LVDS
INT_CRT
INT_HDMI

X4 DMI interface

HDD (SATA) *1 P24
ODD (SATA) P24

SATA0
SATA1

SB ICH9M
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-1
PCIE-6

Mini Card WLAN USB2 P25
USB2

USB8
USB 2.0
Azalia

Ext USB Port x 2 USB 0,1 P25
Int USB Port x 1 USB 7 P25
Bluetooth USB5 P25
CCD USB11 P23

Media Cardreader (RTS5158E) USB2 P28
Card Reader Connector P28

X'TAL 25MHz
Broadcom Giga-LAN (BCM5764) P27
Transformer
RJ45 P27

LPC

EC (WPC775LDG) P29
X'TAL 32.768KHz

Audio CODEC (CX20561) P26
MDC 1.5 P26
RJ11 WIRE CONN.
SPI ROM P29
Touch Pad P24
MMB P24
K/B COON. P29

Audio Amplifier G1441 P26
Int. Speaker P26
S/PDIF P26
MIC Jack P26
Int. MIC P23

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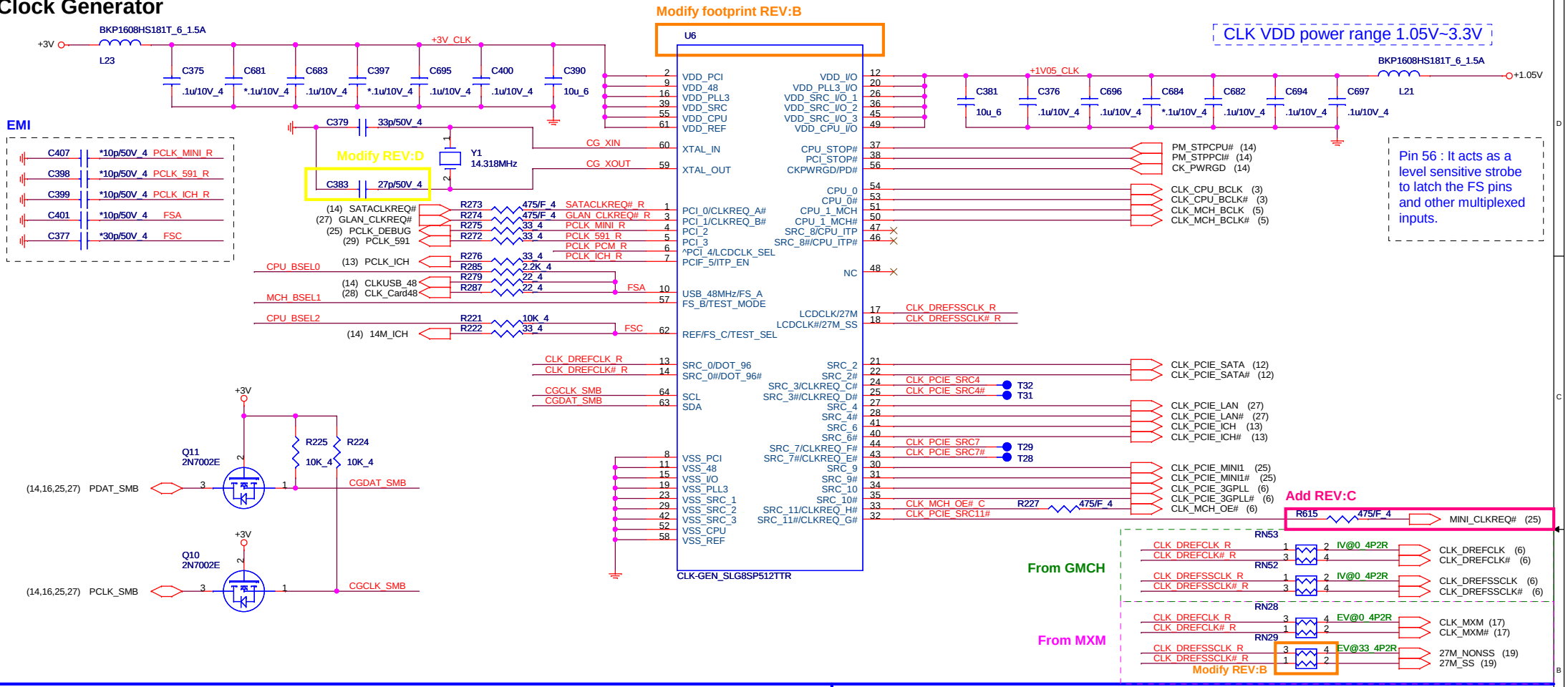
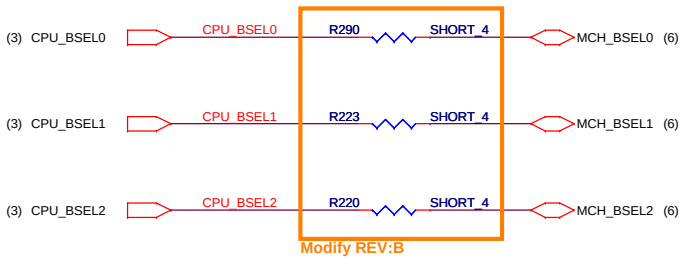
Clock Generator



CPU Clock select

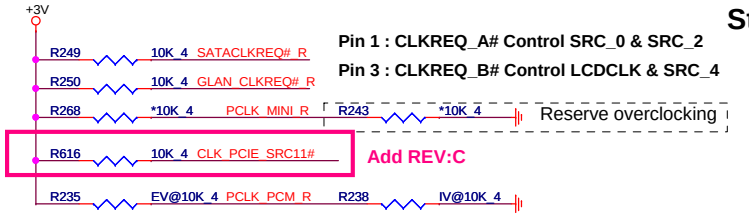
Pin 10/57/62 : For Pin CPU frequency selection



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



Pin 1 : CLKREQ_A# Control SRC_0 & SRC_2

Pin 3 : CLKREQ_B# Control LCDCLK & SRC_4

Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

PCLK_ICH_R R269 10K_4

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

CLOCK GENERATOR

Quanta Computer Inc.
PROJECT : Z06

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	CLOCK GENERATOR	2A
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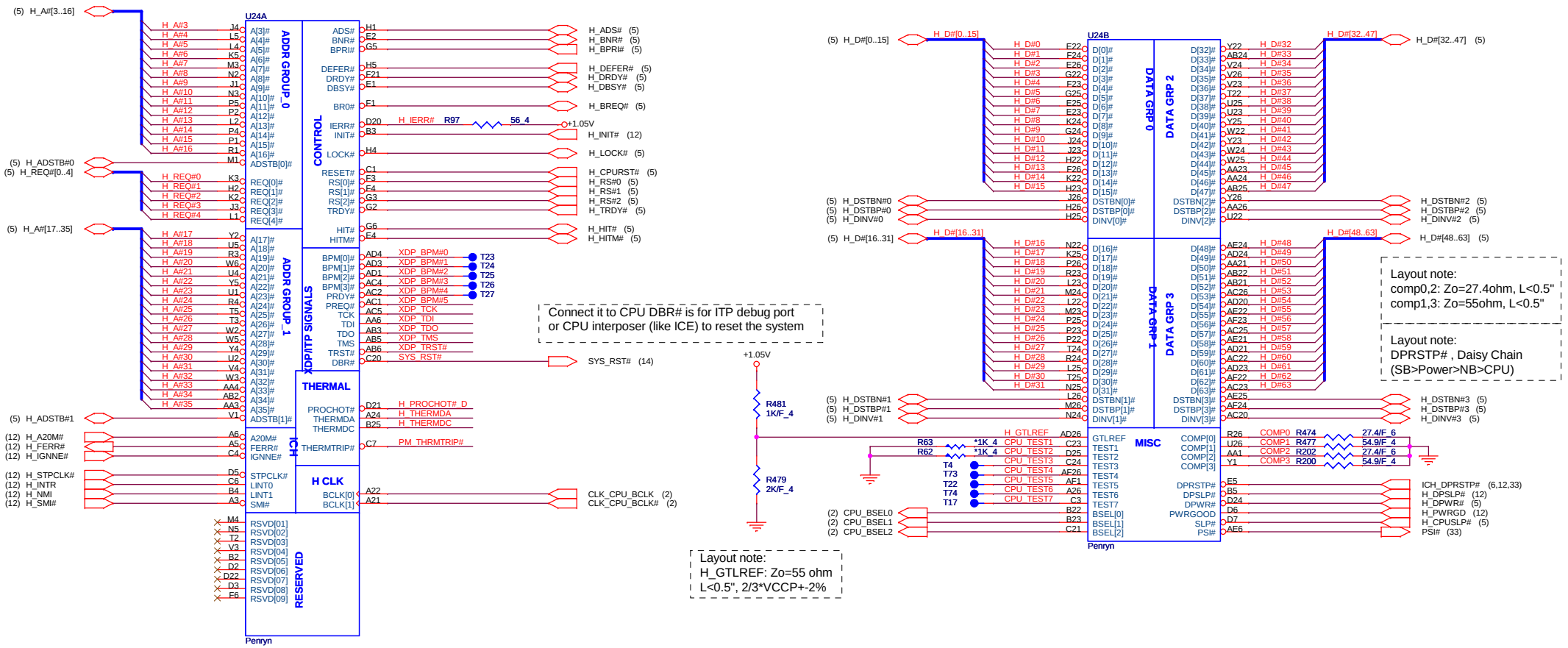
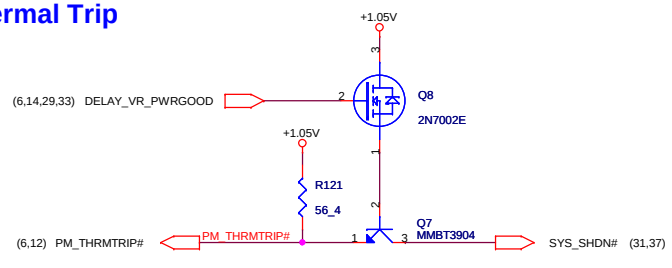
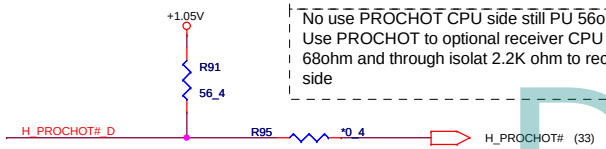


Thermal Trip



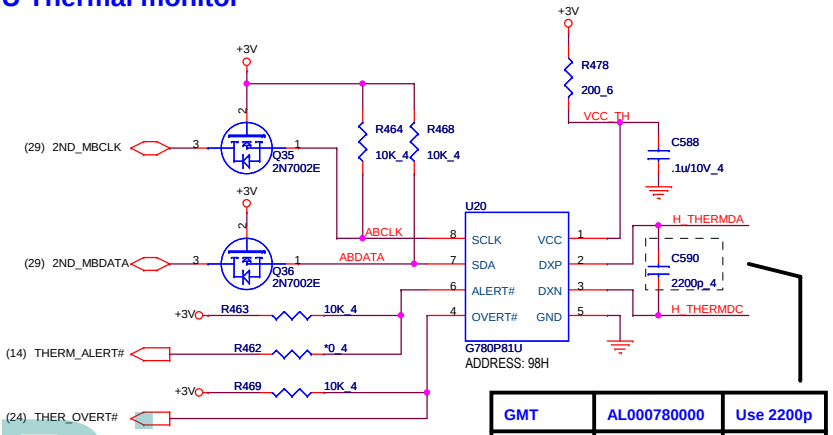
Processor hot



No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

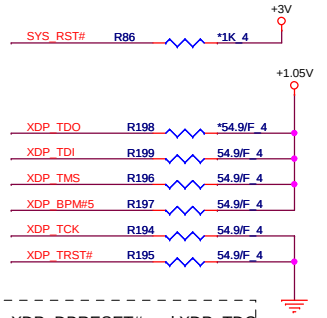
No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

CPU Thermal monitor



GMT	AL000780000	Use 2200p
NS	AL095245000	Use 2200p
WINDBOND	AL83L771K01	Use 2200p

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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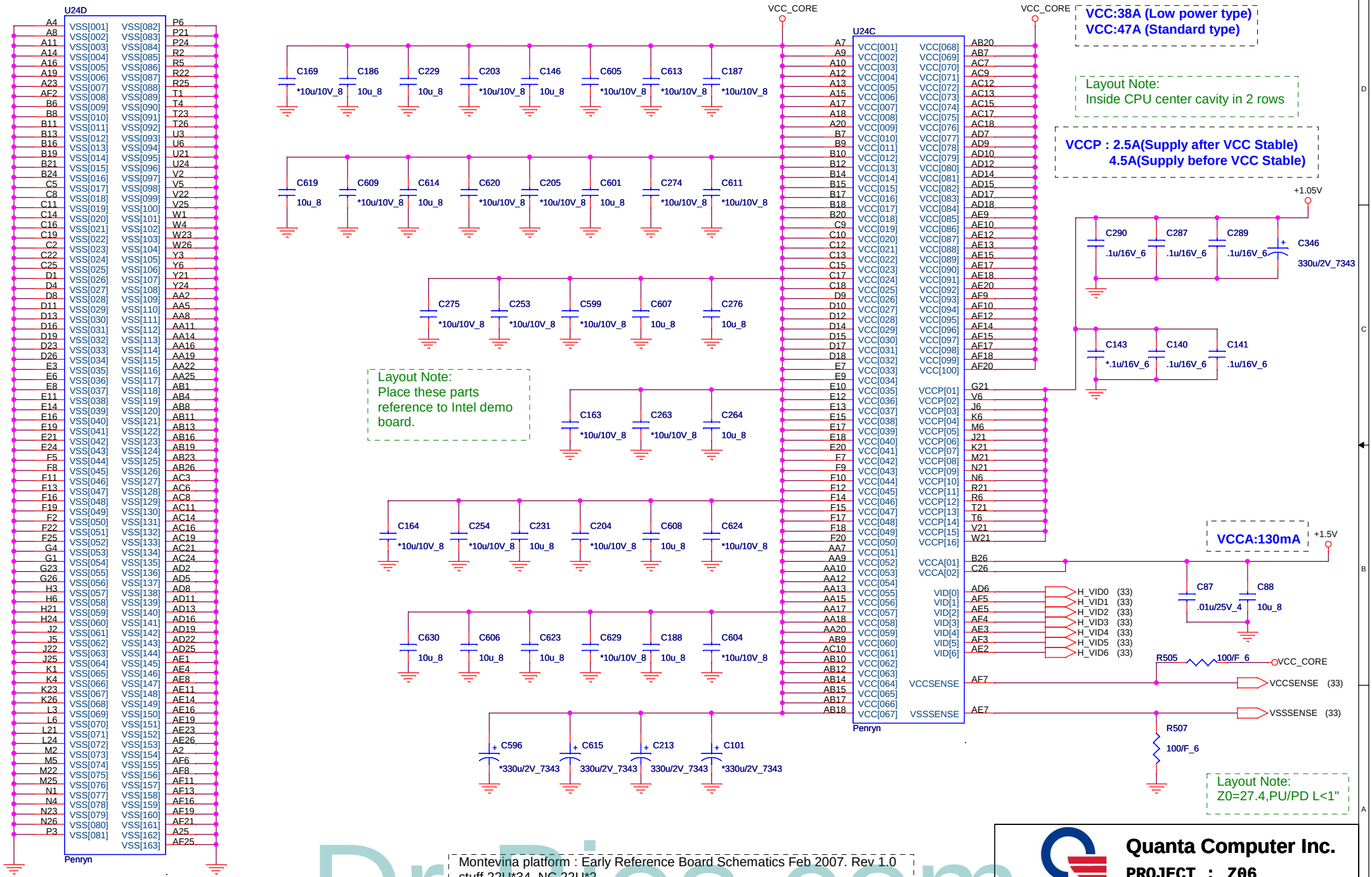
CPU 1/2


U24D
VSS[001] VSS[002] VSS[003] VSS[004] VSS[005] VSS[006] VSS[007] VSS[008] VSS[009] VSS[010] VSS[011] VSS[012] VSS[013] VSS[014] VSS[015] VSS[016] VSS[017] VSS[018] VSS[019] VSS[020] VSS[021] VSS[022] VSS[023] VSS[024] VSS[025] VSS[026] VSS[027] VSS[028] VSS[029] VSS[030] VSS[031] VSS[032] VSS[033] VSS[034] VSS[035] VSS[036] VSS[037] VSS[038] VSS[039] VSS[040] VSS[041] VSS[042] VSS[043] VSS[044] VSS[045] VSS[046] VSS[047] VSS[048] VSS[049] VSS[050] VSS[051] VSS[052] VSS[053] VSS[054] VSS[055] VSS[056] VSS[057] VSS[058] VSS[059] VSS[060] VSS[061] VSS[062] VSS[063] VSS[064] VSS[065] VSS[066] VSS[067] VSS[068] VSS[069] VSS[070] VSS[071] VSS[072] VSS[073] VSS[074] VSS[075] VSS[076] VSS[077] VSS[078] VSS[079] VSS[080] VSS[081] VSS[082] VSS[083] VSS[084] VSS[085] VSS[086] VSS[087] VSS[088] VSS[089] VSS[090] VSS[091] VSS[092] VSS[093] VSS[094] VSS[095] VSS[096] VSS[097] VSS[098] VSS[099] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163]
A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3
P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25
Penryn
VCC_CORE
C169 *10u/10V_8
C186 10u_8
C229 10u_8
C203 *10u/10V_8
C146 10u_8
C605 *10u/10V_8
C613 *10u/10V_8
C187 *10u/10V_8
C619 10u_8
C609 *10u/10V_8
C614 10u_8
C620 *10u/10V_8
C205 *10u/10V_8
C601 10u_8
C274 *10u/10V_8
C611 *10u/10V_8
C275 *10u/10V_8
C253 *10u/10V_8
C599 *10u/10V_8
C607 10u_8
C276 10u_8
Layout Note:
Place these parts reference to Intel demo board.
C163 *10u/10V_8
C263 *10u/10V_8
C264 10u_8
C164 *10u/10V_8
C254 *10u/10V_8
C231 10u_8
C204 *10u/10V_8
C608 10u_8
C624 *10u/10V_8
C630 10u_8
C606 10u_8
C623 10u_8
C629 *10u/10V_8
C188 10u_8
C604 *10u/10V_8
C596 *330u/2V_7343
C615 330u/2V_7343
C213 330u/2V_7343
C101 *330u/2V_7343
U24C
VCC[001] VCC[002] VCC[003] VCC[004] VCC[005] VCC[006] VCC[007] VCC[008] VCC[009] VCC[010] VCC[011] VCC[012] VCC[013] VCC[014] VCC[015] VCC[016] VCC[017] VCC[018] VCC[019] VCC[020] VCC[021] VCC[022] VCC[023] VCC[024] VCC[025] VCC[026] VCC[027] VCC[028] VCC[029] VCC[030] VCC[031] VCC[032] VCC[033] VCC[034] VCC[035] VCC[036] VCC[037] VCC[038] VCC[039] VCC[040] VCC[041] VCC[042] VCC[043] VCC[044] VCC[045] VCC[046] VCC[047] VCC[048] VCC[049] VCC[050] VCC[051] VCC[052] VCC[053] VCC[054] VCC[055] VCC[056] VCC[057] VCC[058] VCC[059] VCC[060] VCC[061] VCC[062] VCC[063] VCC[064] VCC[065] VCC[066] VCC[067] VCC[068] VCC[069] VCC[070] VCC[071] VCC[072] VCC[073] VCC[074] VCC[075] VCC[076] VCC[077] VCC[078] VCC[079] VCC[080] VCC[081] VCC[082] VCC[083] VCC[084] VCC[085] VCC[086] VCC[087] VCC[088] VCC[089] VCC[090] VCC[091] VCC[092] VCC[093] VCC[094] VCC[095] VCC[096] VCC[097] VCC[098] VCC[099] VCC[100]
A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18
AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20
VCCP[01] VCCP[02] VCCP[03] VCCP[04] VCCP[05] VCCP[06] VCCP[07] VCCP[08] VCCP[09] VCCP[10] VCCP[11] VCCP[12] VCCP[13] VCCP[14] VCCP[15] VCCP[16]
G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21
VCCA[01] VCCA[02]
B26 C26
VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]
AD6 AF5 AE5 AF4 AE3 AF3 AE2
H_VID0 (33) H_VID1 (33) H_VID2 (33) H_VID3 (33) H_VID4 (33) H_VID5 (33) H_VID6 (33)
VCCSENSE
AF7
VSSSENSE
AE7
Penryn
VCC:38A (Low power type)
VCC:47A (Standard type)
Layout Note:
Inside CPU center cavity in 2 rows
VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
+1.05V
C290 .1u/16V_6
C287 .1u/16V_6
C289 .1u/16V_6
C346 330u/2V_7343
C143 *.1u/16V_6
C140 .1u/16V_6
C141 .1u/16V_6
VCCA:130mA
+1.5V
C87 .01u/25V_4
C88 10u_8
R505 100/F_6
VCC_CORE
VCCSENSE (33)
VSSSENSE (33)
R507 100/F_6
Layout Note:
Z0=27.4,PU/PD L<1"
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2
CPU 2/2
Quanta Computer Inc.
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CPU Power
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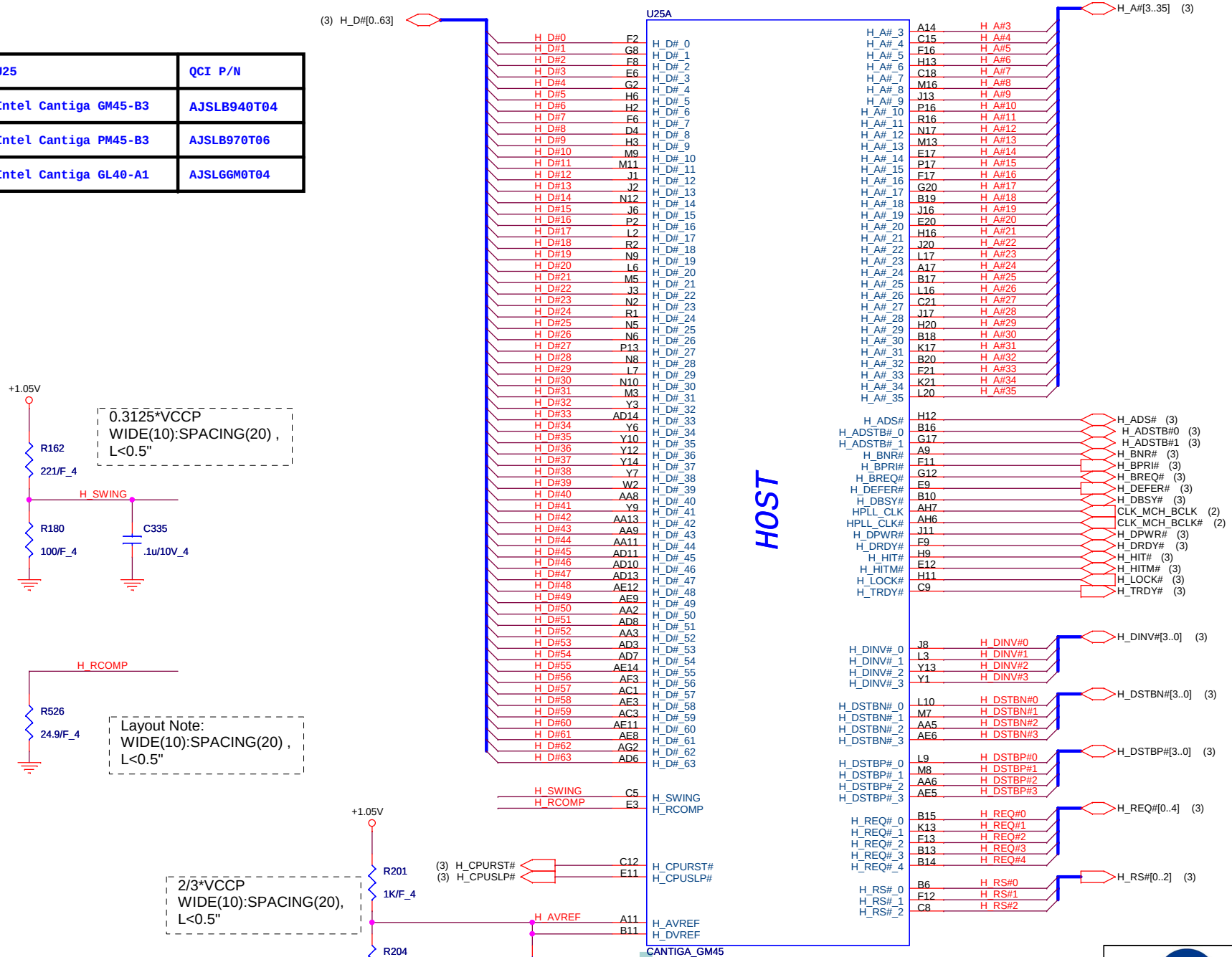
U25	QCI P/N
Intel Cantiga GM45-B3	AJSLB940T04
Intel Cantiga PM45-B3	AJSLB970T06
Intel Cantiga GL40-A1	AJSLGGM0T04



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : Z06

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	GMCH HOST	1A
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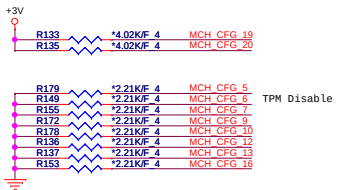
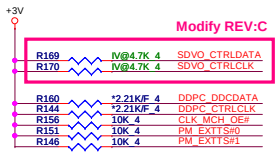
IV@
EV@

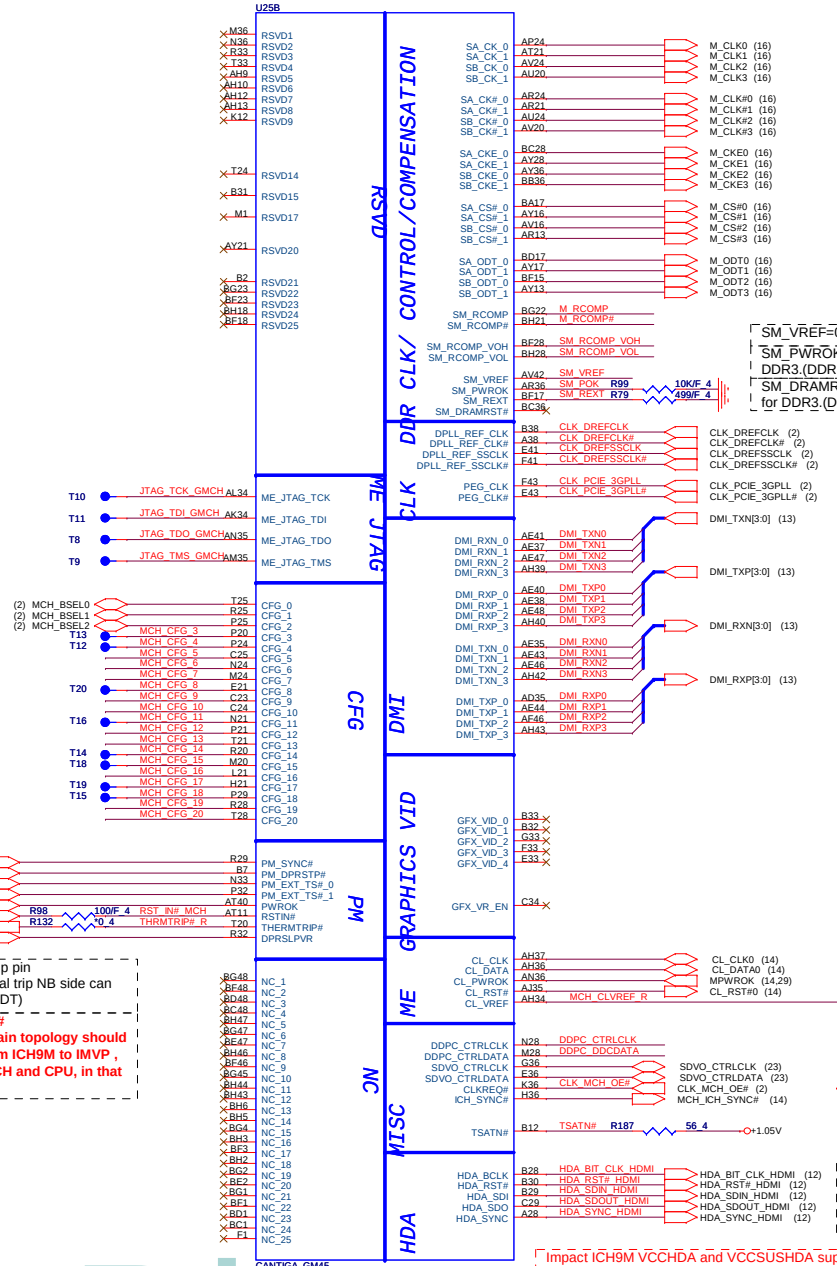
Strap table

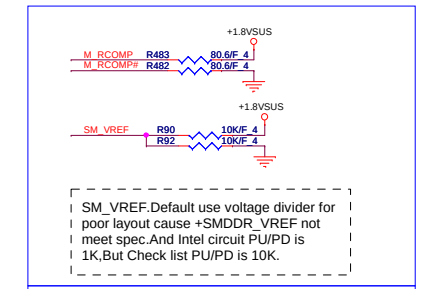
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

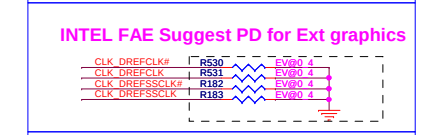
Strap pin

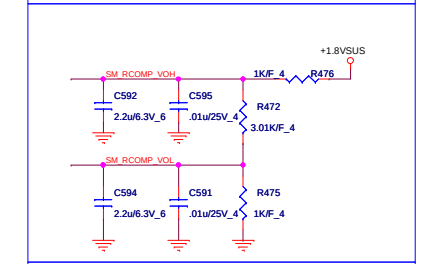


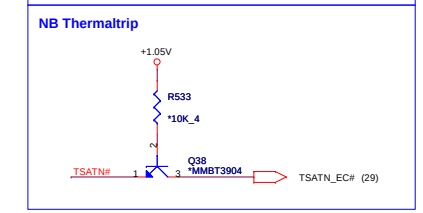


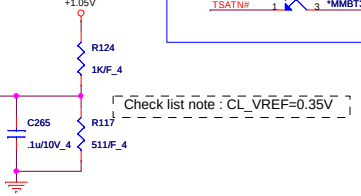












If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56- pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

GMCH (CANTIGA)

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IV@

EV@

SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U25C

(23) L_BKLT_CTRL
(23) INT_LVDS_BLON
R154 IV@10K_4 L_CTRL_CLK
+3V
R148 IV@10K_4 L_CTRL_DATA
(23) INT_LVDS_EDIDCLK
(23) INT_LVDS_EDIDDATA
(23) INT_LVDS_DIGON
R190 IV@2.4K/F_4 LVDS_IBG
R166 IV@0_4 LVDS_VREF
(23) INT_TXLCLKOUT-
(23) INT_TXLCLKOUT+
(23) INT_TXLOUT0-
(23) INT_TXLOUT1-
(23) INT_TXLOUT2-
(23) INT_TXLOUT0+
(23) INT_TXLOUT1+
(23) INT_TXLOUT2+

L32 L_BKLT_CTRL
G32 L_BKLT_EN
M32 L_CTRL_CLK
M33 L_CTRL_DATA
K33 L_DDC_CLK
J33 L_DDC_DATA
M29 L_VDD_EN
C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
C41 LVDSA_CLK#
C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK
H47 LVDSA_DATA#_0
E46 LVDSA_DATA#_1
G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
H48 LVDSA_DATA_0
D45 LVDSA_DATA_1
F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm

R174 SP@75_4 INT_TV_COMP F25
R161 SP@75_4 INT_TV_Y/G H25
R158 SP@75_4 INT_TV_C/R K25
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TVA_DAC
TVB_DAC
TVC_DAC

(23) INT_CRT_BLU INT_CRT_BLU E28
(23) INT_CRT_GRN INT_CRT_GRN G28
(23) INT_CRT_RED INT_CRT_RED J28
G29 CRT_IRTN
H32 CRT_DDC_CLK
J32 CRT_DDC_DATA
J29 CRT_HSYNC
E29 CRT_TVO_IREF
L29 CRT_VSYNC

(23) INT_CRT_DDCCLK
(23) INT_CRT_DDCDAT
(23) INT_HSYNC
R192 IV@30.1_4 HSYNC_G
CRTIREF
(23) INT_VSYNC
R193 IV@30.1_4 VSYNC_G

VGA

HSYNC/VSYNC serial R place close to NB

MXM STUFFED. (CRT)

HSYNC_G
VSYNC_G
R188 EV@0_4
R189 EV@0_4

CRTIREF pull down
for IV cantiga 1.02k ohm/F

CANTIGA_GM45

PCI-EXPRESS GRAPHICS

L<0.5" , If PCIE not support
still connect to +VCC_PEG

+1.05V
T37 EXP_A_COMPX R125 49.9/F_4
T36
PEG_COMPI
PEG_COMPO

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15
PEG_RXN[15:0] (17)

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AD36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15
PEG_RXP[15:0] (17)

PEG_TX#_0 J41 C_PEG_TXN0 C347 .1u/10V_4 PEG_TXN0
PEG_TX#_1 M46 C_PEG_TXN1 C670 .1u/10V_4 PEG_TXN1
PEG_TX#_2 M47 C_PEG_TXN2 C674 .1u/10V_4 PEG_TXN2
PEG_TX#_3 M40 C_PEG_TXN3 C350 .1u/10V_4 PEG_TXN3
PEG_TX#_4 M42 C_PEG_TXN4 C334 EV@.1U/10V_4 PEG_TXN4
PEG_TX#_5 R48 C_PEG_TXN5 C646 EV@.1U/10V_4 PEG_TXN5
PEG_TX#_6 N38 C_PEG_TXN6 C353 EV@.1U/10V_4 PEG_TXN6
PEG_TX#_7 T40 C_PEG_TXN7 C650 EV@.1U/10V_4 PEG_TXN7
PEG_TX#_8 U37 C_PEG_TXN8 C636 EV@.1U/10V_4 PEG_TXN8
PEG_TX#_9 U40 C_PEG_TXN9 C309 EV@.1U/10V_4 PEG_TXN9
PEG_TX#_10 Y40 C_PEG_TXN10 C280 EV@.1U/10V_4 PEG_TXN10
PEG_TX#_11 AA46 C_PEG_TXN11 C625 EV@.1U/10V_4 PEG_TXN11
PEG_TX#_12 AA37 C_PEG_TXN12 C250 EV@.1U/10V_4 PEG_TXN12
PEG_TX#_13 AA40 C_PEG_TXN13 C234 EV@.1U/10V_4 PEG_TXN13
PEG_TX#_14 AD43 C_PEG_TXN14 C212 EV@.1U/10V_4 PEG_TXN14
PEG_TX#_15 AC46 C_PEG_TXN15 C618 EV@.1U/10V_4 PEG_TXN15
PEG_TXN[15:0] (17,23)

PEG_TX_0 J42 C_PEG_TXP0 C348 .1u/10V_4 PEG_TXP0
PEG_TX_1 L46 C_PEG_TXP1 C669 .1u/10V_4 PEG_TXP1
PEG_TX_2 M48 C_PEG_TXP2 C673 .1u/10V_4 PEG_TXP2
PEG_TX_3 M39 C_PEG_TXP3 C349 .1u/10V_4 PEG_TXP3
PEG_TX_4 M43 C_PEG_TXP4 C333 EV@.1U/10V_4 PEG_TXP4
PEG_TX_5 R47 C_PEG_TXP5 C645 EV@.1U/10V_4 PEG_TXP5
PEG_TX_6 N37 C_PEG_TXP6 C352 EV@.1U/10V_4 PEG_TXP6
PEG_TX_7 T39 C_PEG_TXP7 C651 EV@.1U/10V_4 PEG_TXP7
PEG_TX_8 U36 C_PEG_TXP8 C637 EV@.1U/10V_4 PEG_TXP8
PEG_TX_9 U39 C_PEG_TXP9 C311 EV@.1U/10V_4 PEG_TXP9
PEG_TX_10 Y39 C_PEG_TXP10 C270 EV@.1U/10V_4 PEG_TXP10
PEG_TX_11 Y46 C_PEG_TXP11 C628 EV@.1U/10V_4 PEG_TXP11
PEG_TX_12 AA36 C_PEG_TXP12 C257 EV@.1U/10V_4 PEG_TXP12
PEG_TX_13 AA39 C_PEG_TXP13 C249 EV@.1U/10V_4 PEG_TXP13
PEG_TX_14 AD42 C_PEG_TXP14 C199 EV@.1U/10V_4 PEG_TXP14
PEG_TX_15 AD46 C_PEG_TXP15 C617 EV@.1U/10V_4 PEG_TXP15
PEG_TXP[15:0] (17,23)

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1.02Kohm to GND

CRTIREF
For IV: 1.02Kohm
For EV:0ohm
R186 SP@1.02K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R185 SP@150/F_4 INT_CRT_BLU
R173 SP@150/F_4 INT_CRT_GRN
R164 SP@150/F_4 INT_CRT_RED

Quanta Computer Inc.
PROJECT : Z06

Size	Document Number	Rev
	GMCH VGA	1A

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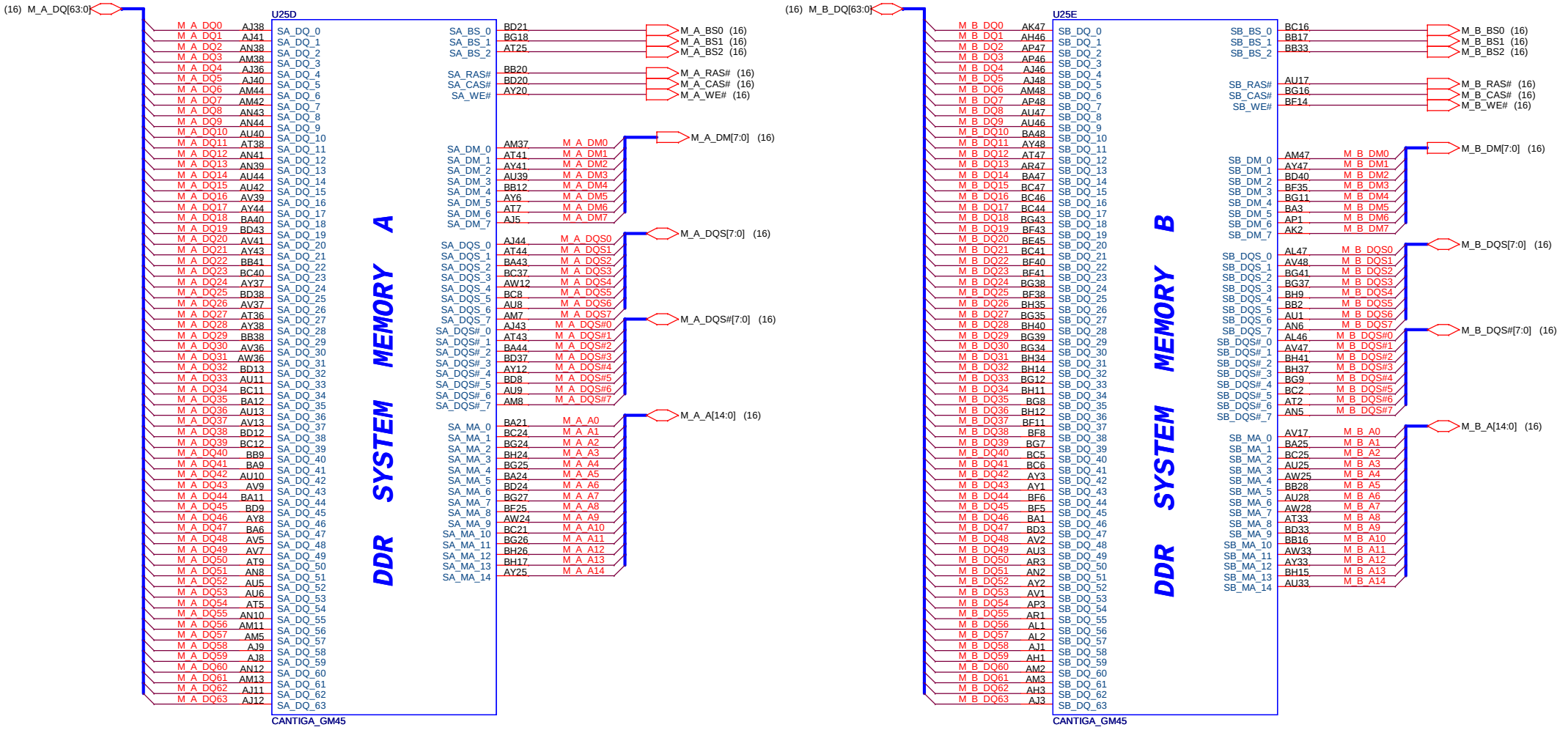

GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : Z06

Size	Document Number	Rev
	GMCH DDRII	1A

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IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM_TDP 10.5~12W
GS_TDP 7~8W
PM_TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+1.8VSUS
C81 22u_8
C82 22u_8
C158 .1u/10V_4
C86 330u/2V_7343

U25G

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

VCC_SM_1 AP33
VCC_SM_2 AN33
VCC_SM_3 BH32
VCC_SM_4 BG32
VCC_SM_5 BF32
VCC_SM_6 BD32
VCC_SM_7 BC32
VCC_SM_8 BB32
VCC_SM_9 BA32
VCC_SM_10 AY32
VCC_SM_11 AW32
VCC_SM_12 AV32
VCC_SM_13 AU32
VCC_SM_14 AT32
VCC_SM_15 AR32
VCC_SM_16 AP32
VCC_SM_17 AN32
VCC_SM_18 BH31
VCC_SM_19 BG31
VCC_SM_20 BF31
VCC_SM_21 BG30
VCC_SM_22 BH29
VCC_SM_23 BG29
VCC_SM_24 BF29
VCC_SM_25 BD29
VCC_SM_26 BC29
VCC_SM_27 BB29
VCC_SM_28 BA29
VCC_SM_29 AY29
VCC_SM_30 AW29
VCC_SM_31 AV29
VCC_SM_32 AU29
VCC_SM_33 AT29
VCC_SM_34 AR29
VCC_SM_35 AP29
VCC_SM_36/NC BA36
VCC_SM_37/NC BB24
VCC_SM_38/NC BD16
VCC_SM_39/NC BB21
VCC_SM_40/NC AW16
VCC_SM_41/NC AW13
VCC_SM_42/NC AT13

VCC SM POWER

+1.05V_AXG

VCC_AXG_NCTF_1 W28
VCC_AXG_NCTF_2 V28
VCC_AXG_NCTF_3 V26
VCC_AXG_NCTF_4 V25
VCC_AXG_NCTF_5 V25
VCC_AXG_NCTF_6 W24
VCC_AXG_NCTF_7 V24
VCC_AXG_NCTF_8 W23
VCC_AXG_NCTF_9 V23
VCC_AXG_NCTF_10 AM21
VCC_AXG_NCTF_11 AL21
VCC_AXG_NCTF_12 AK21
VCC_AXG_NCTF_13 W21
VCC_AXG_NCTF_14 V21
VCC_AXG_NCTF_15 U21
VCC_AXG_NCTF_16 AM20
VCC_AXG_NCTF_17 AK20
VCC_AXG_NCTF_18 W20
VCC_AXG_NCTF_19 U20
VCC_AXG_NCTF_20 AM19
VCC_AXG_NCTF_21 AL19
VCC_AXG_NCTF_22 AK19
VCC_AXG_NCTF_23 AJ19
VCC_AXG_NCTF_24 AH19
VCC_AXG_NCTF_25 AG19
VCC_AXG_NCTF_26 AF19
VCC_AXG_NCTF_27 AE19
VCC_AXG_NCTF_28 AB19
VCC_AXG_NCTF_29 AA19
VCC_AXG_NCTF_30 Y19
VCC_AXG_NCTF_31 W19
VCC_AXG_NCTF_32 V19
VCC_AXG_NCTF_33 U19
VCC_AXG_NCTF_34 AM17
VCC_AXG_NCTF_35 AK17
VCC_AXG_NCTF_36 AH17
VCC_AXG_NCTF_37 AG17
VCC_AXG_NCTF_38 AF17
VCC_AXG_NCTF_39 AE17
VCC_AXG_NCTF_40 AC17
VCC_AXG_NCTF_41 AB17
VCC_AXG_NCTF_42 Y17
VCC_AXG_NCTF_43 W17
VCC_AXG_NCTF_44 V17
VCC_AXG_NCTF_45 AM16
VCC_AXG_NCTF_46 AL16
VCC_AXG_NCTF_47 AK16
VCC_AXG_NCTF_48 AJ16
VCC_AXG_NCTF_49 AH16
VCC_AXG_NCTF_50 AG16
VCC_AXG_NCTF_51 AF16
VCC_AXG_NCTF_52 AE16
VCC_AXG_NCTF_53 AC16
VCC_AXG_NCTF_54 AB16
VCC_AXG_NCTF_55 AA16
VCC_AXG_NCTF_56 Y16
VCC_AXG_NCTF_57 W16
VCC_AXG_NCTF_58 V16
VCC_AXG_NCTF_59 U16
VCC_AXG_NCTF_60

VCC GFX NCTF

+1.05V_AXG

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

VCC_AXG_1 Y26
VCC_AXG_2 AE25
VCC_AXG_3 AB25
VCC_AXG_4 AA25
VCC_AXG_5 AE24
VCC_AXG_6 AC24
VCC_AXG_7 AA24
VCC_AXG_8 Y24
VCC_AXG_9 AE23
VCC_AXG_10 AC23
VCC_AXG_11 AB23
VCC_AXG_12 AA23
VCC_AXG_13 AJ21
VCC_AXG_14 AG21
VCC_AXG_15 AE21
VCC_AXG_16 AC21
VCC_AXG_17 AA21
VCC_AXG_18 Y21
VCC_AXG_19 AH20
VCC_AXG_20 AF20
VCC_AXG_21 AE20
VCC_AXG_22 AC20
VCC_AXG_23 AB20
VCC_AXG_24 AA20
VCC_AXG_25 T17
VCC_AXG_26 T16
VCC_AXG_27 AM15
VCC_AXG_28 AL15
VCC_AXG_29 AE15
VCC_AXG_30 AJ15
VCC_AXG_31 AH15
VCC_AXG_32 AG15
VCC_AXG_33 AF15
VCC_AXG_34 AB15
VCC_AXG_35 AA15
VCC_AXG_36 Y15
VCC_AXG_37 V15
VCC_AXG_38 U15
VCC_AXG_39 AN14
VCC_AXG_40 AM14
VCC_AXG_41 U14
VCC_AXG_42 T14

VCC GFX

Voltage regulator is shared between
the Graphics Core Rail,
VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL,
VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL,
VCCA_SM, VCC_AXF

+1.05V_AXG
IV@
R103 IV@10/F_4 AJ14
R111 IV@10/F_4 AH14
VCC_AXG_SENSE
VSS_AXG_SENSE

VCC SM LF

VCC_SM_LF1 AV44
VCC_SM_LF2 BA37
VCC_SM_LF3 AM40
VCC_SM_LF4 AV21
VCC_SM_LF5 AY5
VCC_SM_LF6 AM10
VCC_SM_LF7 BB13

1.8V
Internal connect to power

C118 .1u/10V_4
C176 .1u/10V_4
C121 .22u/6.3V_4
C127 .22u/6.3V_4
C178 .47u/6.3V_4
C113 1u_4
C128 1u_4

CANTIGA_GM45

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

+1.05V
C192 .1u/10V_4
C218 .22u/6.3V_4
C181 .22u/6.3V_4
C260 22u_8
C616 330u/2V_7343

Place close to
the GMCH

U25F

VCC_1 AG34
VCC_2 AC34
VCC_3 AB34
VCC_4 AA34
VCC_5 Y34
VCC_6 V34
VCC_7 U34
VCC_8 AM33
VCC_9 AK33
VCC_10 AJ33
VCC_11 AG33
VCC_12 AF33
VCC_13 AE33
VCC_14 AC33
VCC_15 AA33
VCC_16 Y33
VCC_17 W33
VCC_18 V33
VCC_19 U33
VCC_20 AH28
VCC_21 AF28
VCC_22 AC28
VCC_23 AA28
VCC_24 AJ26
VCC_25 AG26
VCC_26 AE26
VCC_27 AC26
VCC_28 AH25
VCC_29 AG25
VCC_30 AF25
VCC_31 AG24
VCC_32 AJ23
VCC_33 AH23
VCC_34 AF23
VCC_35 T32

VCC CORE POWER

+1.05V
IV@
R128 IV@0_8
R130 IV@0_8
R129 IV@0_8

+1.05V_AXG

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG
C622 IV@330u/2V_7343
C621 IV@330u/2V_7343
C228 IV@.47u/6.3V_4
SP@
C159 SP@1u_6
C223 IV@10u_8
C272 IV@22u_8
C267 IV@.1u_4
C261 IV@.1u_4
C273 IV@.1u_4

Place close to the GMCH
Cavity Capacitors

SP@:IV Sutff 1uf
EVstuff 0 ohm

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

+1.05V
VCC_NCTF_1 AM32
VCC_NCTF_2 AL32
VCC_NCTF_3 AK32
VCC_NCTF_4 AJ32
VCC_NCTF_5 AH32
VCC_NCTF_6 AG32
VCC_NCTF_7 AE32
VCC_NCTF_8 AC32
VCC_NCTF_9 AA32
VCC_NCTF_10 Y32
VCC_NCTF_11 W32
VCC_NCTF_12 U32
VCC_NCTF_13 AM30
VCC_NCTF_14 AL30
VCC_NCTF_15 AK30
VCC_NCTF_16 AH30
VCC_NCTF_17 AG30
VCC_NCTF_18 AF30
VCC_NCTF_19 AE30
VCC_NCTF_20 AC30
VCC_NCTF_21 AB30
VCC_NCTF_22 AA30
VCC_NCTF_23 Y30
VCC_NCTF_24 W30
VCC_NCTF_25 V30
VCC_NCTF_26 U30
VCC_NCTF_27 AL29
VCC_NCTF_28 AK29
VCC_NCTF_29 AJ29
VCC_NCTF_30 AH29
VCC_NCTF_31 AG29
VCC_NCTF_32 AE29
VCC_NCTF_33 AC29
VCC_NCTF_34 AA29
VCC_NCTF_35 Y29
VCC_NCTF_36 W29
VCC_NCTF_37 V29
VCC_NCTF_38 AL28
VCC_NCTF_39 AK28
VCC_NCTF_40 AL26
VCC_NCTF_41 AK26
VCC_NCTF_42 AK25
VCC_NCTF_43 AK24
VCC_NCTF_44 AK23

VCC NCTF POWER

CANTIGA_GM45

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : Z06

Size	Document Number	Rev
	GMCH VCC,NCTF	1A
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Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

If CRT have Flicker issue
STUFF 5.6 ohm

IV&EV Dis/Enable setting

Modify REV:C

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

SP@:INT use 1000pf
EXT use 0 ohm

SP@:INT use 1 U
EXT use 0 ohm

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	N/A
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

1210 10UH, 10%
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL_A/B

3.3V
73mA

3.3V
5mA

1.05V
FSB-1067
852mA

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

USE same GND plane

1.8V
13.2mA

1.5V
414uA

1.05V
24mA

1.05V
321.35mA

1.05V
DDR2-800
720mA

1.05V
50mA

1.05V
139.2mA

3.9 nH, 0.2 nH, 1A
DCR_max=32 m

VCCA_PEG_PLL
+1.25V for Teenah use(100mA)

1210 0.1uH, 20%, 1A,
DCR_max=0.078

1.8V
DDR2-800
124mA

0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA

ESR = 60 m

0805 100 nH, DCR=160 m

1.8V
118.8mA

1.05V
DDR2-800
26mA

CRB : 0 ohm
Check list : 2.2nH

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

3.3V
79mA

3.3V
105.3mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V
50mA

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
35mA

VCCD_QDAC share to TV and CRT

1.05V
157.2mA

1.05V
1782mA

1.05V
456mA

1.5V
48.363mA for CRT
5mA for TV

1.5V
0.5mA

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

MODIFY

FB 220 @100 MHz, 25%, 2A

1.05V
50mA

1.8V
60.31mA

ESR=60m ohm

1.05V
Internal connect to power

Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : Z06

Size	Document Number	Rev
	GMCH POWER	1A

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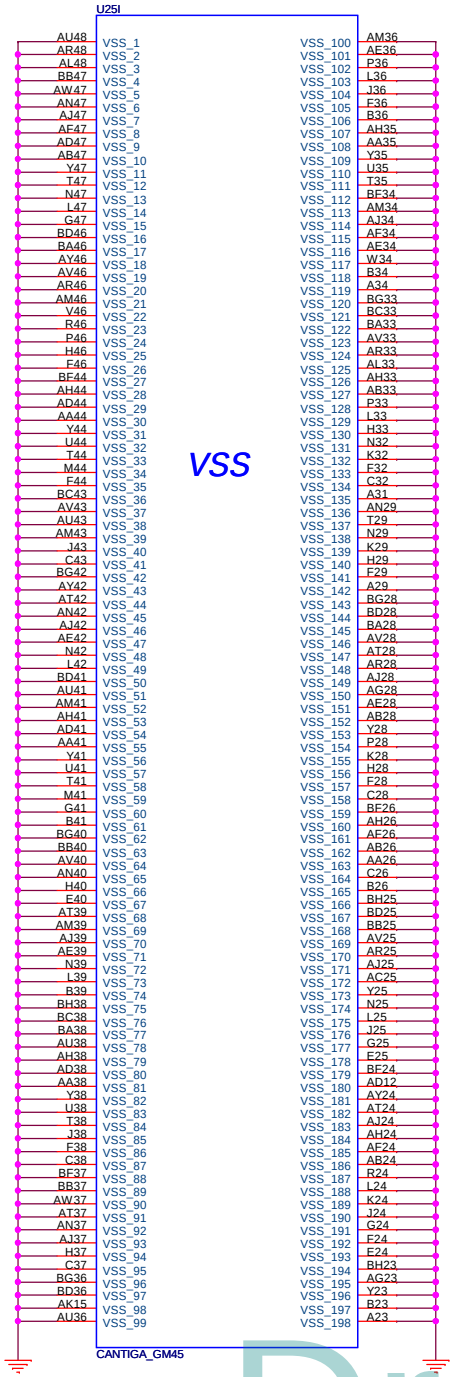

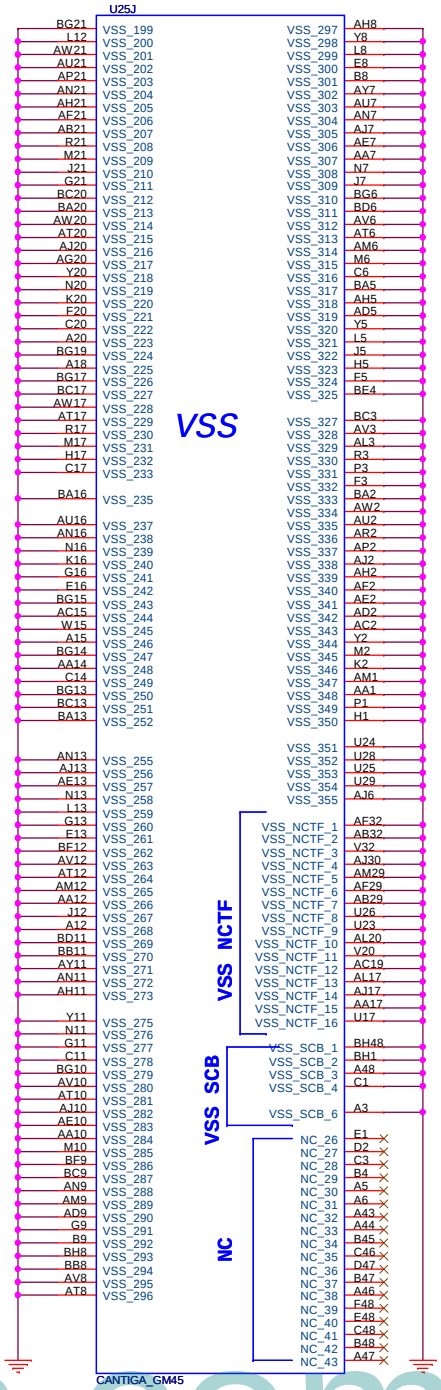

GMCH (CANTIGA)

Quanta Computer Inc.

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	GMCH VSS	1A
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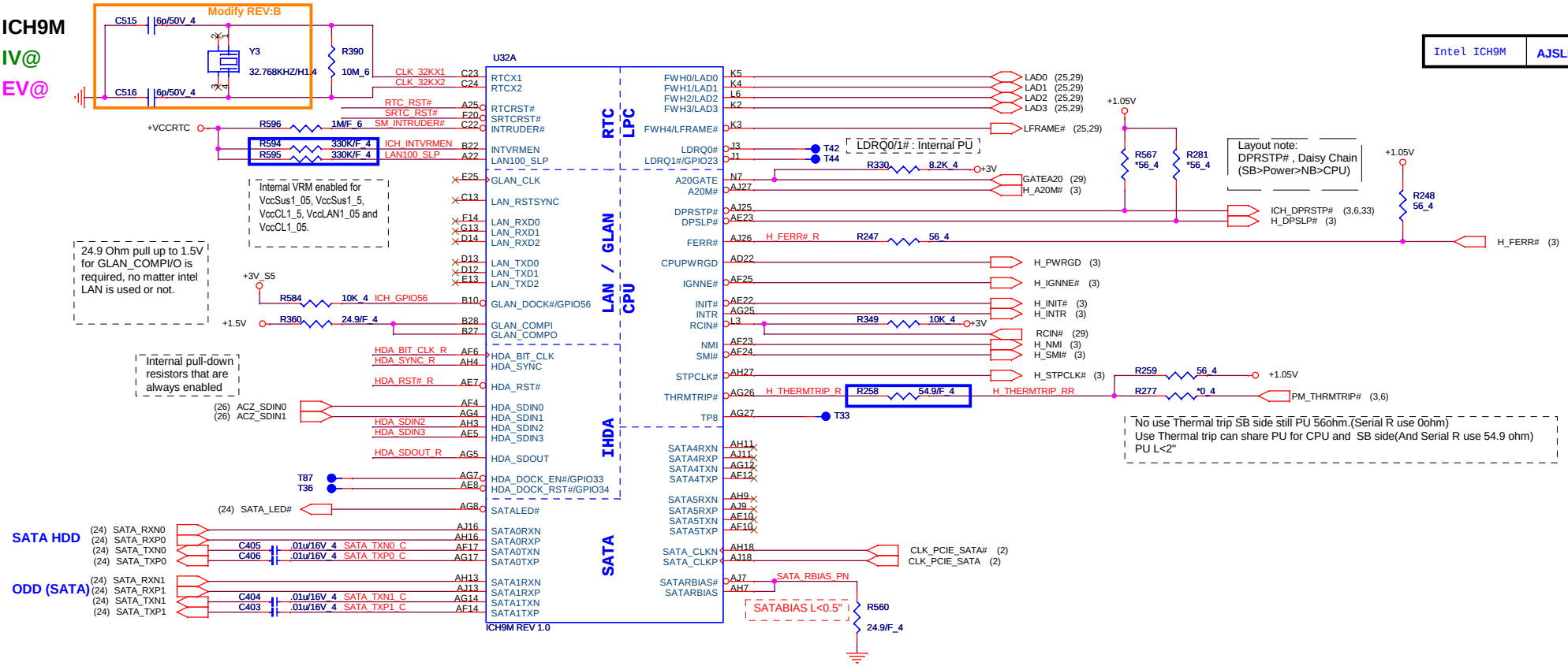
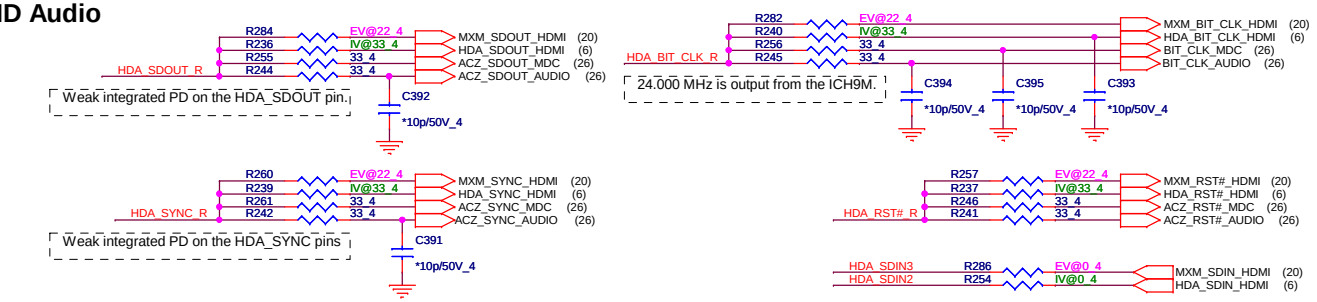
ICH9M
IV@
EV@

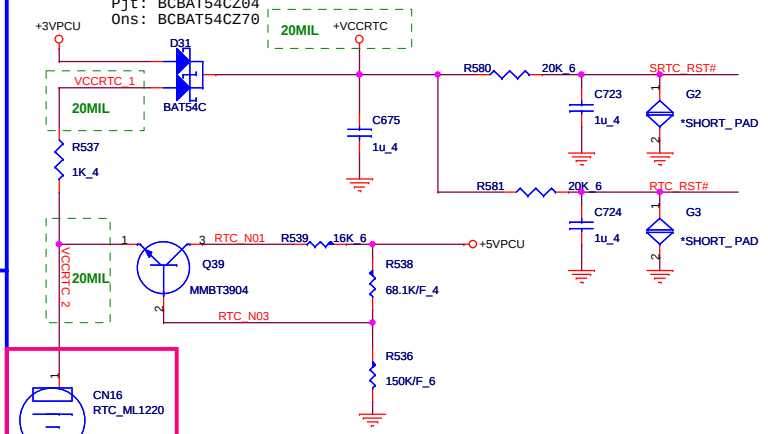
Intel ICH9M | AJSLB8Q0T03



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

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	ICH9M HOST	2A
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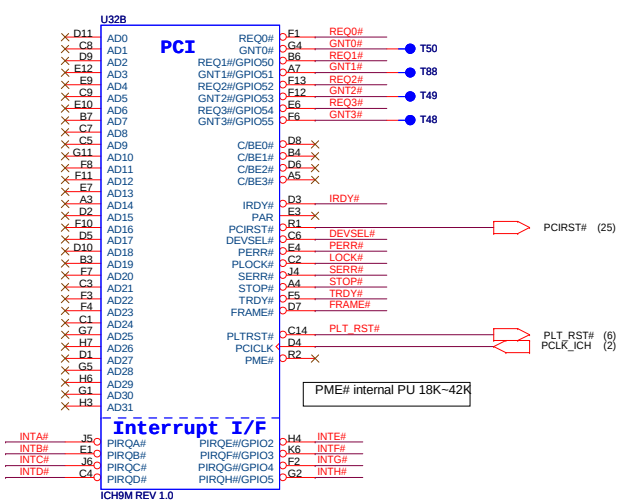
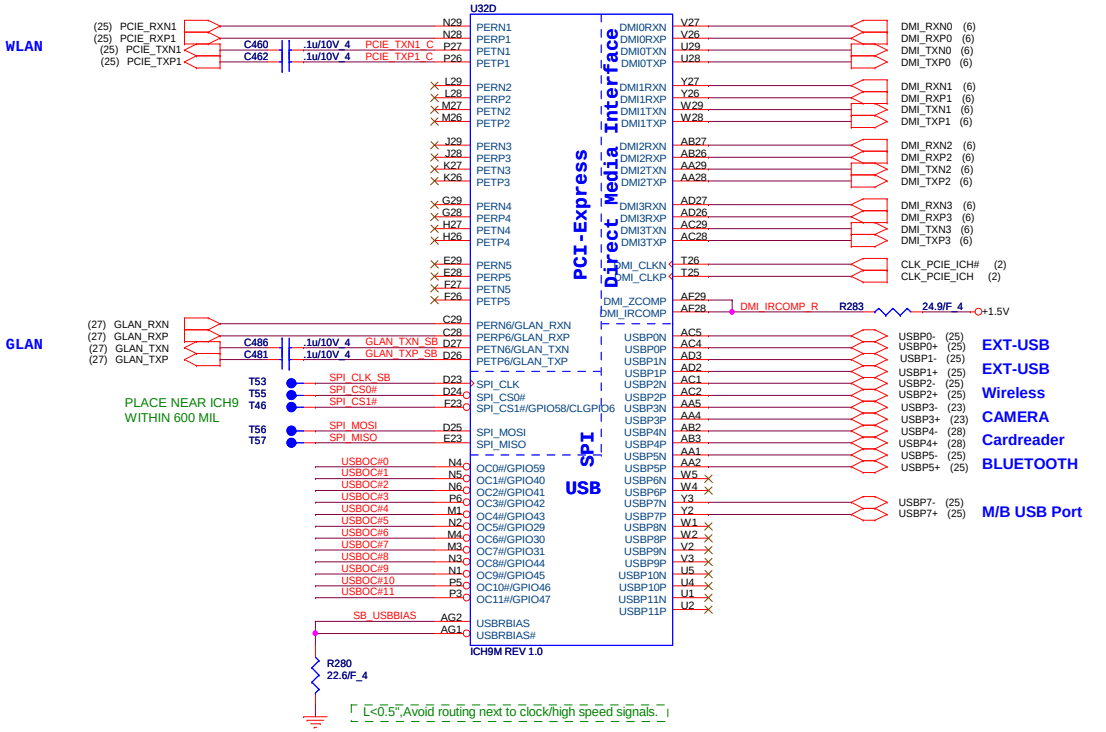
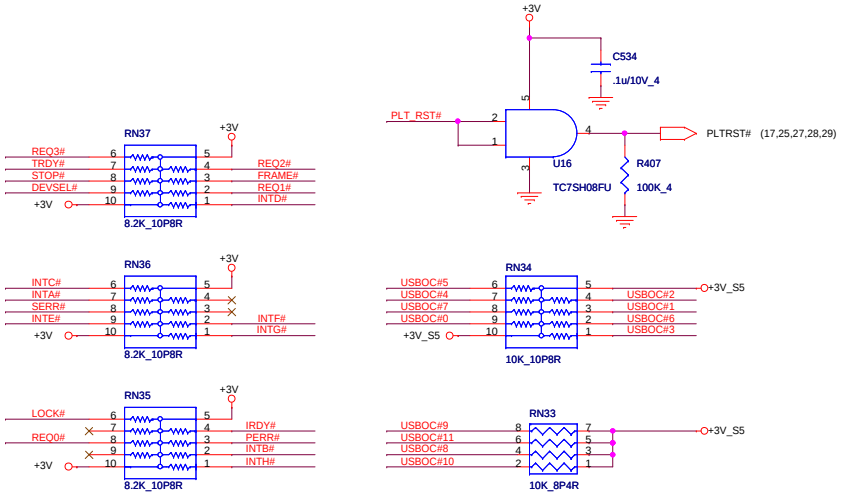
ICH9M







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R369 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / **LPC(Default)**	GNT0# R353 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		

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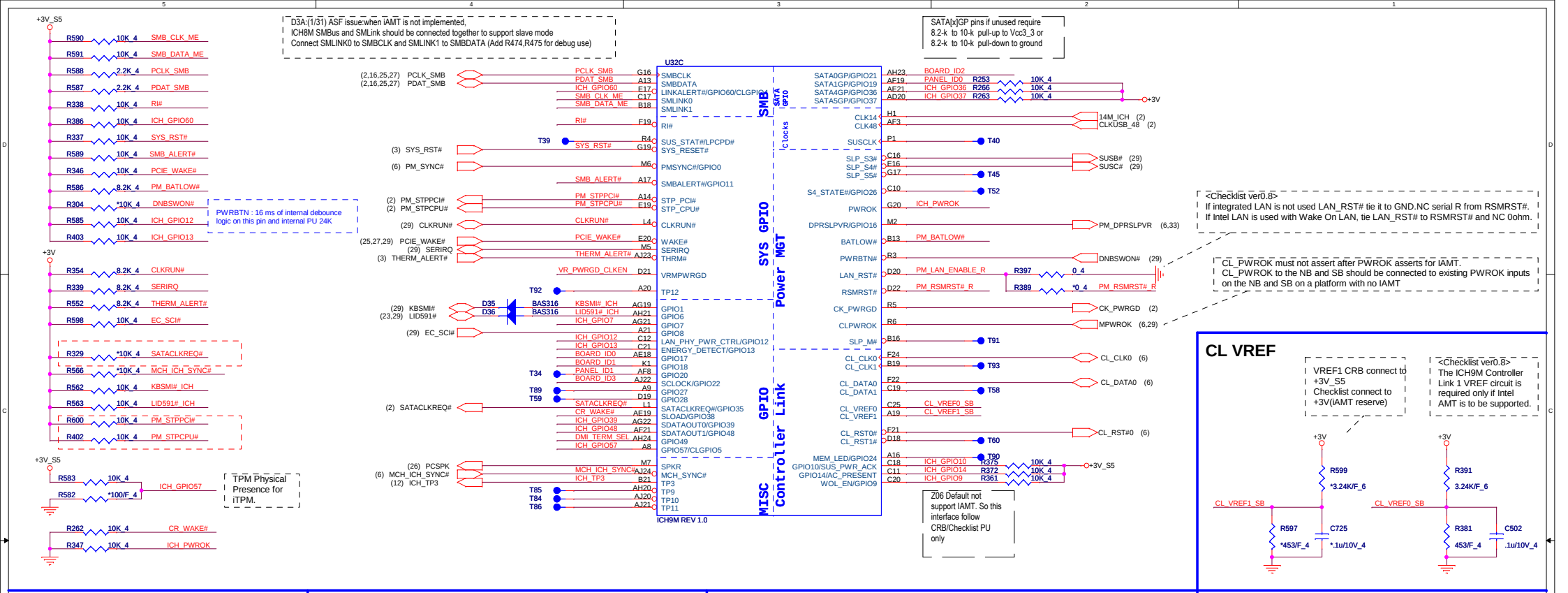


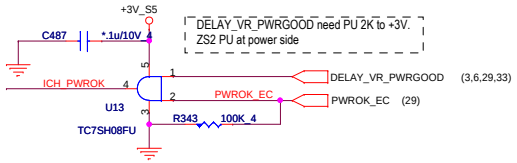
CL VREF

VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

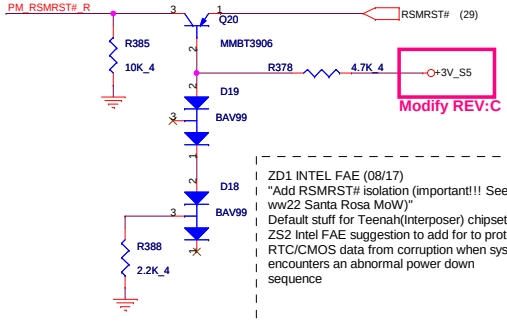
<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

Follow CHECK LIST V1.5

ICH PWROK

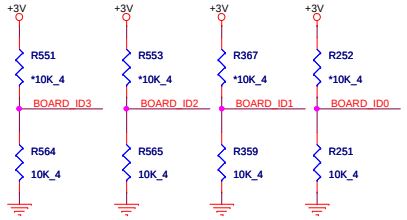


Resume RST



ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

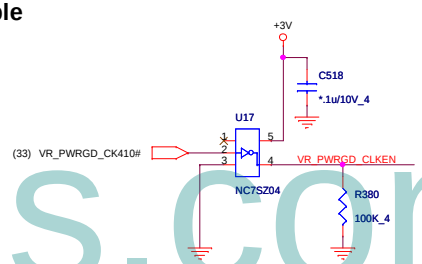


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R316 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R554 *1K_4

CLK Enable



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ICH9M

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

330 Ohms@ 100 MHz , 0805

5 Ohms @ 100 MHz , 0.7A

500 mA, 20%

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

1.05V , Powered by VCC1_05 in S0

If use SB MAC for LAN function. And support wake up need connect to relation power.

If use SB MAC for LAN function. And support wake up need connect to relation power.

Modify REV:D

MODIFY

Quanta Computer Inc.	
PROJECT : Z06	
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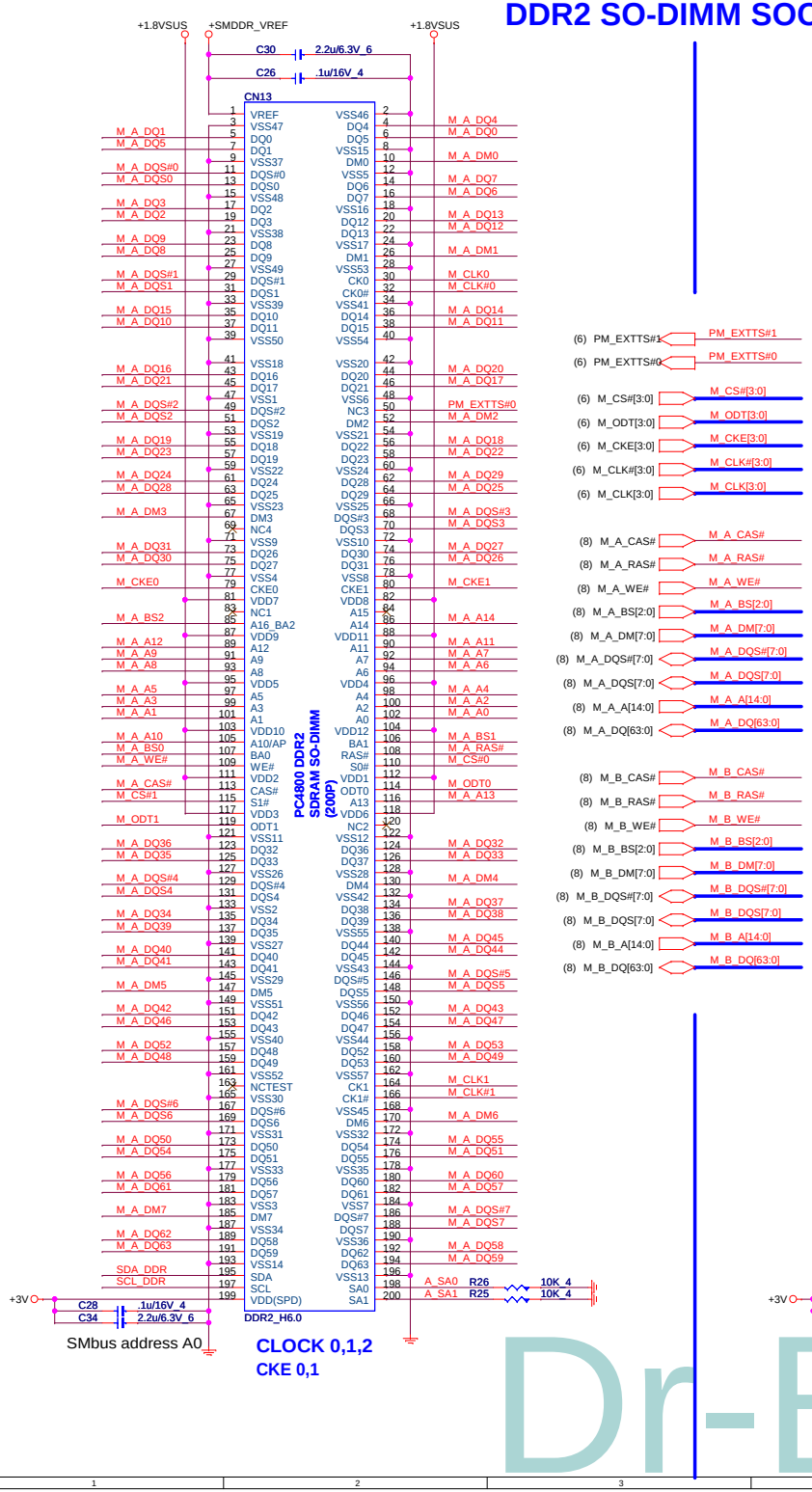
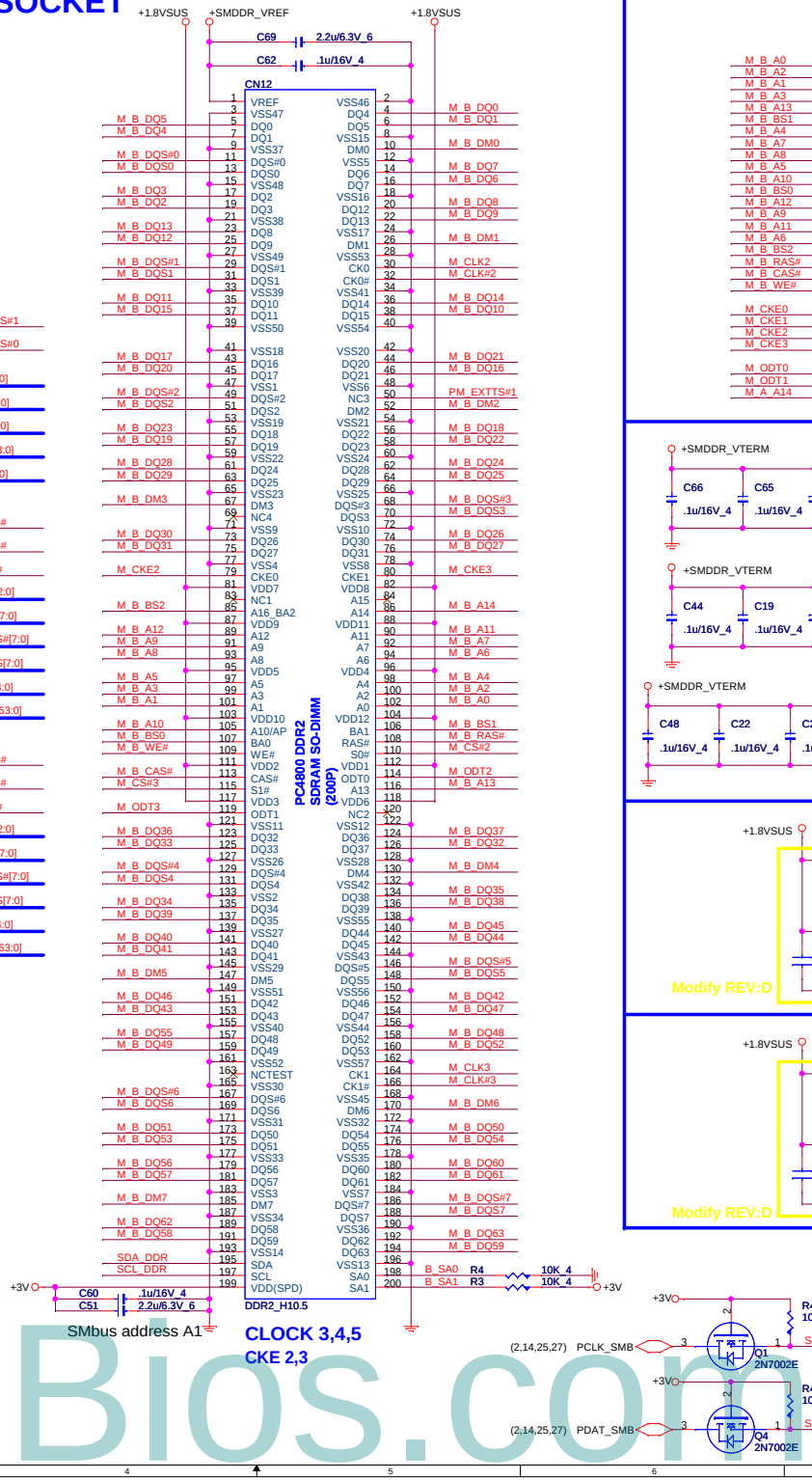
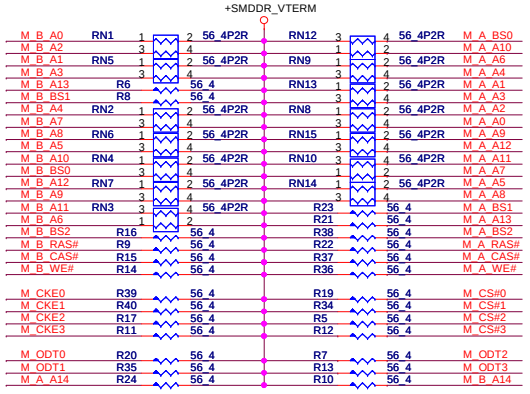
DDR2 SO-DIMM SOCKET

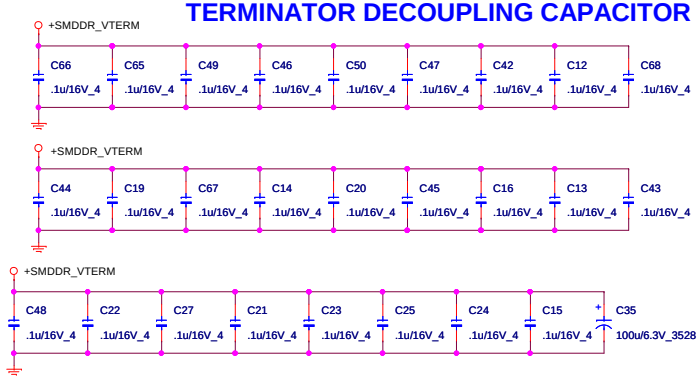




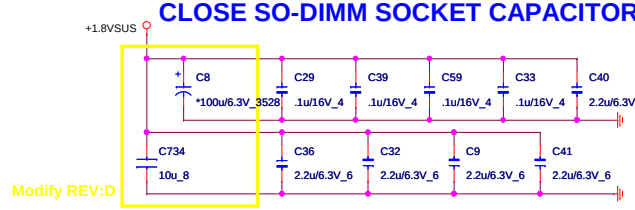
DDR2 TERMINATOR



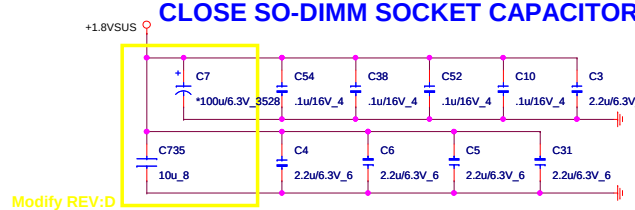
TERMINATOR DECOUPLING CAPACITOR



CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS



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	DDRII SO-DIMM	1A

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(2,3,6,7,10,12,13,14,15,16,19,20,23,24,25,26,27,29,31,33,35,36) +3V
(18,19,35) +VGA1.1V

U23A
EV@N10M-GE1-B-U2/H

+VGA1.1V
~ 500mA
C238 EV@22U_8
C236 EV@4.7U/6.3V_6
C211 EV@1U/6.3V_4
C191 EV@1U/6.3V_4
C246 EV@.1U/10V_4
C210 EV@.1U/10V_4
C209 EV@.47U/6.3V_4

+VGA1.1V
1600mA
C667 EV@22U_8
C657 EV@4.7U/6.3V_6
C237 EV@1U/6.3V_4
C259 EV@.47U/6.3V_4
C232 EV@.47U/6.3V_4
C227 EV@.1U/10V_4

Near BGA

+3V
R70 EV@0_6
+PEX_VDD3
C100 EV@1U/6.3V_4
C104 EV@.1U/10V_4
C107 EV@.1U/10V_4

(35) VGA_SENSE
SI-2 4/10 For Nvidia recommend.
100mA
12~16 mils width

+VGA1.1V
L48 EV@MLG1608B10NJ_6
+PEX_PLLVDD
C255 EV@4.7U/6.3V_6
C649 EV@4.7U/6.3V_6
C215 EV@1U/6.3V_4
C216 EV@.1U/10V_4
C648 EV@.01U/16V/X7R_4

PCI EXPRESS

FOR UMA iHDMI HPD
PEG_RXP3 R175 IV@0_4 HDMI_HP_IV# (23)

D30 *BAS316
PLTRST# (13,25,27,28,29)
R519 *100K/F_4
R525 EV@0_4

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U23B
EV@N10M-GE1-B-U2/H

MEMORY I/F A

(22) VMA_MA3 V32 FBA_CMD0
(22) VMA_MA0 W31 FBA_CMD1
(22) VMA_MA2 U31 FBA_CMD2
(22) VMA_MA1 Y32 FBA_CMD3
(22) VMA_MA3H AB35 FBA_CMD4
(22) VMA_MA4H AB34 FBA_CMD5
(22) VMA_MA5H W35 FBA_CMD6
W33 FBA_CMD7
W30 FBA_CMD8
(22) VMA_CS0# T34 FBA_CMD9
(22) VMA_WE# T35 FBA_CMD10
(22) VMA_BA0 AB31 FBA_CMD11
(22) VMA_CKE Y30 FBA_CMD12
(22) VMA_ODT Y34 FBA_CMD13
(22) VMA_MA2H W32 FBA_CMD14
(22) VMA_MA12 AA30 FBA_CMD15
(22) VMA_RAS# AA32 FBA_CMD16
(22) VMA_MA11 Y33 FBA_CMD17
(22) VMA_MA10 U32 FBA_CMD18
(22) VMA_BA1 Y31 FBA_CMD19
(22) VMA_MA8 U34 FBA_CMD20
(22) VMA_MA9 Y35 FBA_CMD21
(22) VMA_MA6 W34 FBA_CMD22
(22) VMA_MA5 V30 FBA_CMD23
(22) VMA_MA7 U35 FBA_CMD24
(22) VMA_MA4 U30 FBA_CMD25
(22) VMA_CAS# U33 FBA_CMD26
AB30 FBA_CMD27
(22) VMA_BA2 AB33 FBA_CMD28
T33 FBA_CMD29
W29 FBA_CMD30

Si-II Add

VMA_DM0 P30 FBA_DQM0
VMA_DM1 P32 FBA_DQM1
VMA_DM2 J30 FBA_DQM2
VMA_DM3 H34 FBA_DQM3
VMA_DM4 AF32 FBA_DQM4
VMA_DM5 AF35 FBA_DQM5
VMA_DM6 AL32 FBA_DQM6
VMA_DM7 AL34 FBA_DQM7

VMA_WDQS0 N31 FBA_DQS_WP0
VMA_WDQS1 L34 FBA_DQS_WP1
VMA_WDQS2 J32 FBA_DQS_WP2
VMA_WDQS3 H35 FBA_DQS_WP3
VMA_WDQS4 AE31 FBA_DQS_WP4
VMA_WDQS5 AC33 FBA_DQS_WP5
VMA_WDQS6 AJ32 FBA_DQS_WP6
VMA_WDQS7 AJ34 FBA_DQS_WP7

VMA_RDQS0 N32 FBA_DQS_RN0
VMA_RDQS1 L35 FBA_DQS_RN1
VMA_RDQS2 H31 FBA_DQS_RN2
VMA_RDQS3 G35 FBA_DQS_RN3
VMA_RDQS4 AD32 FBA_DQS_RN4
VMA_RDQS5 AC34 FBA_DQS_RN5
VMA_RDQS6 AJ31 FBA_DQS_RN6
VMA_RDQS7 AJ35 FBA_DQS_RN7

P29 FBA_WDS0
R29 FBA_WDS0*
L29 FBA_WDS1
M29 FBA_WDS1*
AD29 FBA_WDS2
AE29 FBA_WDS2*
AG29 FBA_WDS3
AH29 FBA_WDS3*

+1.8V
AA27 FBVDDQ_1
AA29 FBVDDQ_2
AA31 FBVDDQ_3
AB27 FBVDDQ_4
AB29 FBVDDQ_5
AC27 FBVDDQ_6
AD27 FBVDDQ_7
AE27 FBVDDQ_8
AJ28 FBVDDQ_9
B18 FBVDDQ_10
E21 FBVDDQ_11
G17 FBVDDQ_12
G18 FBVDDQ_13
G22 FBVDDQ_14
G8 FBVDDQ_15
G9 FBVDDQ_16
H29 FBVDDQ_17
J14 FBVDDQ_18
J15 FBVDDQ_19
J16 FBVDDQ_20
J17 FBVDDQ_21
J20 FBVDDQ_22
J21 FBVDDQ_23
J22 FBVDDQ_24
J23 FBVDDQ_25
J24 FBVDDQ_26
J29 FBVDDQ_27

R30 VMA_DQ0 FBA_D0
R32 VMA_DQ1 FBA_D1
P31 VMA_DQ2 FBA_D2
N30 VMA_DQ3 FBA_D3
L31 VMA_DQ4 FBA_D4
M32 VMA_DQ5 FBA_D5
M30 VMA_DQ6 FBA_D6
L30 VMA_DQ7 FBA_D7
P33 VMA_DQ8 FBA_D8
P34 VMA_DQ9 FBA_D9
N35 VMA_DQ10 FBA_D10
P35 VMA_DQ11 FBA_D11
N34 VMA_DQ12 FBA_D12
L33 VMA_DQ13 FBA_D13
L32 VMA_DQ14 FBA_D14
N33 VMA_DQ15 FBA_D15
K31 VMA_DQ16 FBA_D16
K30 VMA_DQ17 FBA_D17
G30 VMA_DQ18 FBA_D18
K32 VMA_DQ19 FBA_D19
G32 VMA_DQ20 FBA_D20
H30 VMA_DQ21 FBA_D21
F30 VMA_DQ22 FBA_D22
G31 VMA_DQ23 FBA_D23
H33 VMA_DQ24 FBA_D24
K35 VMA_DQ25 FBA_D25
K33 VMA_DQ26 FBA_D26
G34 VMA_DQ27 FBA_D27
K34 VMA_DQ28 FBA_D28
E33 VMA_DQ29 FBA_D29
E34 VMA_DQ30 FBA_D30
G33 VMA_DQ31 FBA_D31
AG30 VMA_DQ32 FBA_D32
AH31 VMA_DQ33 FBA_D33
AG32 VMA_DQ34 FBA_D34
AF31 VMA_DQ35 FBA_D35
AF30 VMA_DQ36 FBA_D36
AD30 VMA_DQ37 FBA_D37
AC32 VMA_DQ38 FBA_D38
AE30 VMA_DQ39 FBA_D39
AE32 VMA_DQ40 FBA_D40
AF33 VMA_DQ41 FBA_D41
AF34 VMA_DQ42 FBA_D42
AE35 VMA_DQ43 FBA_D43
AE33 VMA_DQ44 FBA_D44
AE34 VMA_DQ45 FBA_D45
AC35 VMA_DQ46 FBA_D46
AB32 VMA_DQ47 FBA_D47
AN33 VMA_DQ48 FBA_D48
AK32 VMA_DQ49 FBA_D49
AL33 VMA_DQ50 FBA_D50
AM33 VMA_DQ51 FBA_D51
AL31 VMA_DQ52 FBA_D52
AK30 VMA_DQ53 FBA_D53
AJ30 VMA_DQ54 FBA_D54
AH30 VMA_DQ55 FBA_D55
AM35 VMA_DQ56 FBA_D56
AH33 VMA_DQ57 FBA_D57
AH35 VMA_DQ58 FBA_D58
AH32 VMA_DQ59 FBA_D59
AH34 VMA_DQ60 FBA_D60
AM34 VMA_DQ61 FBA_D61
AL35 VMA_DQ62 FBA_D62
AJ33 VMA_DQ63 FBA_D63

T32 VMA_CLK0 FBA_CLK0
T31 VMA_CLK0# FBA_CLK0*
AC31 VMA_CLK1 FBA_CLK1
AC30 VMA_CLK1# FBA_CLK1*

VMA_CLK0 (22)
VMA_CLK0# (22)
VMA_CLK1 (22)
VMA_CLK1# (22)

(19,22,34) +1.8V
(17,19,35) +VGA1.1V

(22) VMA_DQ[63..0]
(22) VMA_DM[7..0]
(22) VMA_WDQS[7..0]
(22) VMA_RDQS[7..0]

R502 EV@10K/F_4 VMA_ODT
R498 EV@10K/F_4 VMA_CKE

for DDR2 need use
CMD11(CKE) and
CMD12(ODT)

+1.8V
R78 *1K/F_4
use internal Vref, ext
divider no stuff
R75 *1K/F_4
15mils width
J27 +FB_VREF1 FB_VREF
C93 EV@.1U/10V_4

For Debug only
T30 FBA_DEBUG *60.4/F_4 R100 +1.8V FBA_DEBUG

15mils width
L11 EV@BKP1608HS181T_6_1.5A
AG27 +FB_PLLAVDD FB_DLLAVDD0
AF27 FB_PLLAVDD0
+VGA1.1V
C94 EV@.1U/10V_4
C90 EV@.1U/10V_4
C214 EV@1U/6.3V_4
C235 EV@4.7U/6.3V_6

For Nvidia request

U23C
EV@N10M-GE1-B-U2/H

MEMORY I/F B

C17 FBC_CMD0 D11 FBC_D0
B19 FBC_CMD1 E11 FBC_D1
D18 FBC_CMD2 F10 FBC_D2
F21 FBC_CMD3 D8 FBC_D3
A23 FBC_CMD4 E8 FBC_D4
D21 FBC_CMD5 F9 FBC_D5
B23 FBC_CMD6 E8 FBC_D6
E20 FBC_CMD7 F12 FBC_D7
G21 FBC_CMD8 B11 FBC_D8
F20 FBC_CMD9 C13 FBC_D9
F19 FBC_CMD10 A11 FBC_D10
F23 FBC_CMD11 B8 FBC_D11
A22 FBC_CMD12 A8 FBC_D12
C22 FBC_CMD13 C8 FBC_D13
B17 FBC_CMD14 C11 FBC_D14
F24 FBC_CMD15 C10 FBC_D15
C25 FBC_CMD16 D12 FBC_D16
E22 FBC_CMD17 E13 FBC_D17
C20 FBC_CMD18 E17 FBC_D18
B22 FBC_CMD19 F15 FBC_D19
A19 FBC_CMD20 F16 FBC_D20
D22 FBC_CMD21 E16 FBC_D21
D20 FBC_CMD22 F14 FBC_D22
E19 FBC_CMD23 F13 FBC_D23
D19 FBC_CMD24 D13 FBC_D24
F18 FBC_CMD25 A13 FBC_D25
C19 FBC_CMD26 B13 FBC_D26
F22 FBC_CMD27 A14 FBC_D27
C23 FBC_CMD28 C16 FBC_D28
B20 FBC_CMD29 A17 FBC_D29
A20 FBC_CMD30 B16 FBC_D30
D16 FBC_D31

F11 FBC_DQM0 D24 FBC_D32
D10 FBC_DQM1 D26 FBC_D33
D15 FBC_DQM2 E25 FBC_D34
A16 FBC_DQM3 F25 FBC_D35
D27 FBC_DQM4 F27 FBC_D36
D28 FBC_DQM5 E28 FBC_D37
D34 FBC_DQM6 F28 FBC_D38
A34 FBC_DQM7 D29 FBC_D39
A25 FBC_D40

E10 FBC_DQS_WP0 B25 FBC_D41
A10 FBC_DQS_WP1 D25 FBC_D42
D14 FBC_DQS_WP2 C26 FBC_D43
C14 FBC_DQS_WP3 C28 FBC_D44
E26 FBC_DQS_WP4 B28 FBC_D45
B26 FBC_DQS_WP5 A28 FBC_D46
D32 FBC_DQS_WP6 A29 FBC_D47
A32 FBC_DQS_WP7 E29 FBC_D48
F29 FBC_D49
D9 FBC_DQS_RN0 D30 FBC_D50
B10 FBC_DQS_RN1 E31 FBC_D51
E14 FBC_DQS_RN2 C33 FBC_D52
B14 FBC_DQS_RN3 D33 FBC_D53
E26 FBC_DQS_RN4 F32 FBC_D54
A26 FBC_DQS_RN5 E32 FBC_D55
D31 FBC_DQS_RN6 B29 FBC_D56
A31 FBC_DQS_RN7 C29 FBC_D57
B31 FBC_D58

G11 FBC_WDS0 C31 FBC_D59
G12 FBC_WDS0* B32 FBC_D60
G14 FBC_WDS1 C32 FBC_D61
G15 FBC_WDS1* B34 FBC_D62
G24 FBC_WDS2 B35 FBC_D63
G25 FBC_WDS2*
G27 FBC_WDS3
G28 FBC_WDS3*

FBC_CLK0 E17
FBC_CLK0* D17
FBC_CLK1 D23
FBC_CLK1* E23

+1.8V
N27 FBVDDQ_28
P27 FBVDDQ_29
R27 FBVDDQ_30
T27 FBVDDQ_31
U27 FBVDDQ_32
U29 FBVDDQ_33
V27 FBVDDQ_34
V29 FBVDDQ_35
V34 FBVDDQ_36
W27 FBVDDQ_37
Y27 FBVDDQ_38

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R83 EV@30.1/F_4 +1.8V
FB_CAL_PU_GND L27 FB_CAL_PU_GND R84 EV@30.1/F_4
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R88 *30.1/F_4
R184 Install for DDR3
FBC_DEBUG G19 FBC_DEBUG R77 *60.4/F_4 +1.8V
R196 no stuff

G96 only
FB_DLLAVDD1 J19 +FB_PLLAVDD
FB_PLLAVDD1 J18
C99 EV@.1U/10V_4
C217 EV@.1U/10V_4

For NB9P-GS only

NB10M_GE1:FB_CAL_PD_VDDQ=30.1ohm;FB_CAL_PU_GND=30.1ohm
NB10M_GS1:FB_CAL_PD_VDDQ=30.1ohm;FB_CAL_PU_GND=36.5ohm

+1.8V
C157 EV@4.7U/6.3V_6
C74 EV@.47U/6.3V_4
C110 EV@.47U/6.3V_4
C129 EV@.1U/10V_4
C77 EV@4.7U/6.3V_6
C172 EV@.47U/6.3V_4
C108 EV@.47U/6.3V_4
C103 EV@.1U/10V_4
C193 EV@.1U/10V_4
C133 EV@.1U/10V_4
C179 EV@.1U/10V_4
C102 EV@.1U/10V_4
C638 EV@.1U/10V_4
C112 EV@.1U/10V_4

+1.8V
C97 EV@4.7U/6.3V_6
C109 EV@.47U/6.3V_4
C98 EV@.47U/6.3V_4
C91 EV@.1U/10V_4
C89 EV@4.7U/6.3V_6
C120 EV@.47U/6.3V_4
C96 EV@.47U/6.3V_4
C92 EV@.1U/10V_4
C111 EV@.1U/10V_4
C134 EV@.1U/10V_4
C85 EV@.1U/10V_4
C201 EV@.1U/10V_4
C155 EV@.1U/10V_4
C95 EV@.1U/10V_4

Quanta Computer Inc.
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	N10P (MEMORY I/F) 2/5	1A
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U23D
EV@N10M-GE1-B-U2/H

IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL

TMDS channel two

Display port output

Modify REV:C

NV: R,G,B +- 250ps length-matched

Close to GPU

PLACE CLOSE TO GPU

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

SI_modified
Nvidia request

SPREAD SPECTRUM

U1 *ICS91730AMLF-T

I2C ADDRESS: 0xD4H

NVidia suggest:
10 k pull-down only if no spread chip used.

05/12 (PV) FOR EMI Solution

Quanta Computer Inc.
PROJECT : Z06

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	N10P (DISPLAY) 3/5	1A

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U23E
EV@N10M-GE1-B-U2/H

MIOA
MIOA_VDDQ_1
MIOA_VDDQ_2
MIOA_VDDQ_3
MIOA_VDDQ_4
MIOA_CAL_PD_VDDQ
MIOA_CAL_PU_GND
MIOA_VREF
MIOA_D0 MIOA_D1 MIOA_D2 MIOA_D3 MIOA_D4 MIOA_D5 MIOA_D6 MIOA_D7 MIOA_D8 MIOA_D9 MIOA_D10 MIOA_D11 MIOA_D12 MIOA_D13 MIOA_D14
MIOA_CTL3 MIOA_HSYNC MIOA_VSYNC MIOA_DE
MIOA_CLKOUT MIOA_CLKOUT* MIOA_CLKIN
MIOA_CLKIN R488 EV@10K/F_4

MIOB
MIOB_VDDQ_1
MIOB_VDDQ_2
MIOB_VDDQ_3
MIOB_VDDQ_4
MIOB_CAL_PD_VDDQ
MIOB_CAL_PU_GND
MIOB_VREF
MIOB_D0 MIOB_D1 MIOB_D2 MIOB_D3 MIOB_D4 MIOB_D5 MIOB_D6 MIOB_D7 MIOB_D8 MIOB_D9 MIOB_D10 MIOB_D11 MIOB_D12 MIOB_D13 MIOB_D14 MIOB_D15 MIOB_D16 MIOB_D17
STRAP0 STRAP1 STRAP2
MIOB_CTL3 MIOB_HSYNC MIOB_VSYNC MIOB_DE
MIOB_CLKOUT MIOB_CLKOUT* MIOB_CLKIN
MIOB_CLKIN R497 EV@10K/F_4

MISC1 (GPIOS,JTAG,THERM,I2C)
THERMDN THERMDP
GFX_THMD- GFX_THMD+
JTAG_TCK JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TRST*
I2CS_SCL I2CS_SDA I2CC_SCL I2CC_SDA I2CD_SCL I2CD_SDA I2CE_SCL I2CE_SDA
MXMCLK MXMDATA I2CC_SCL_G I2CC_SDA_G I2CE_SCL_G I2CE_SDA_G
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19 GPIO20 GPIO21 GPIO22 GPIO23
EV_LVDS_BL_BRGHT
VGA_THERM# ALERT#
MXM_ACIN
HDMI_HP_EV (23)
EV_LVDS_BL_BRGHT (23)
EV_LVDS_VDDEN (23)
EV_LVDS_BLON (23)
GPU_VID0 (35)
GPU_VID1 (35)
VGA_THERM# (29)

MISC2(ROM)
BBIASN_NC BBIASP_NC
HDA_BCLK HDA_RST* HDA_SDI HDA_SDO HDA_SYNC
STRAP_REF_3V3 STRAP_REF_MIOB
ROM_CS* ROM_SI ROM_SO ROM_SCLK
I2CH_SCL I2CH_SDA
SPDIF
BUFRST* PGOOD_OUT*
RFU RFU_GND
HDCP_SCL HDCP_SDA
SPDIF_VGA
R470 *EV@24.3K/F_4
C585 *EV@0.01u/16V_4
R467 EV@35.7K/F_4
MXM_SPDIF_OUT (26)

HD Audio Level :3V
MXM_BIT_CLK_HDMI MXM_RST#_HDMI MXM_SDIN_HDMI_G MXM_SDOUT_HDMI MXM_SYNC_HDMI
R55 EV@10_4
R89 EV@40.2K/F_4
R87 EV@40.2K/F_4
STRAP_REF_3V3 STRAP_REF_MIOB

NVidia suggest:
Removed T14, T18, T19, T20, T29, T30, T32, T33 that reduce via counts

(2,3,6,7,10,12,13,14,15,16,17,19,23,24,25,26,27,29,31,33,35,36) +3V

R473 STUFF
20K ohm For Samsung , 64M*16
4.99K ohm For Hynix , 64M*16

NB9P-GS (G96) Straps
NB9M-GE (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR
R471 *4.99K/F_4
R58 EV@45.3K/F_4
R56 *4.99K/F_4
R473 EV@4.99K/F_4
R59 *4.99K/F_4
R57 EV@15K/F_4
ROM_SI ROM_SO ROM_SCLK

SEE Datasheet for details on G9x Straps!
R494 EV@45.3K/F_4
R491 *4.99K/F_4
R489 EV@24.9K/F_4
R493 *4.99K/F_4
R492 EV@10K/F_4
R490 *15K/F_4
STRAP0 STRAP1 STRAP2

09/09 (UT7G DB)
Change for N10P.

NVidia suggest:
Pull low 10KR for R95, R7 & R525
JTAG_TMS R522 EV@10K/F_4
JTAG_TDI R523 EV@10K/F_4
VGA_THERM# R76 EV@10K/F_4
ALERT# R85 EV@10K/F_4
I2CE_SCL_G R54 EV@2.2K_4
I2CE_SDA_G R53 EV@2.2K_4
JTAG_TCK R521 EV@10K/F_4
JTAG_TRST# R520 EV@10K/F_4
EV_LVDS_BL_BRGHT R487 EV@10K/F_4
MXM_RST#_HDMI R88 EV@10K/F_4
MXM_ACIN R80 EV@10K/F_4

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1111
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor		N10M (500MHz)	QCI P/N
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix			
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda			
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung			
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elpida			
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix		H5PS1G63EFR-20L	AKD5LG-TW02
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung		K4N1G164QE-HC20	AKD5LG-T510
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda			

PCI_DEVID: STRAP2 R489

NB9M-GE	0x06E	8	1000
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	0x064	9	1001
N10P-GE1	0x065	2	0010
N10M-GE1	0x06E	C	1100 default

CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)

HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

Change P/N
U2 EV@AT24C16B
A0 A1 A2 GND VCC WP SCL SDA
HDCP_SCL HDCP_SDA
C71 EV@.1U/10V_4
Waiting Confirm from Nvidia

SI modified
Nvidia suggest:
R52 EV@2.2K_4
R45 EV@2.2K_4
R44 *2.2K_4

R49 4.7K_4
R50 4.7K_4
(29) MXM_SMCLK
(29) MXM_SMDATA
Q2 2N7002E
Q3 2N7002E
MXMCLK (24)
MXMDATA (24)

RB1 *10K_4
MXM_ACIN
Q6 *EV@DTA114YUA
R74 *EV@10K_4
Q5 *EV@2N7002E
ACIN (29,30)
R82 *0_4

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NVVDD Decoupling

(35,36) +VGACORE

+VGACORE

+VGACORE

U23F

EV@N10M-GE1-B-U2/H

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

PLACE NEAR BALLS

NEAR BGA

+VGACORE

C123 EV@.022u/16V_4	C124 EV@.022u/16V_4	C114 EV@.022u/16V_4	C116 EV@.022u/16V_4	C148 EV@.022u/16V_4	C183 EV@4.7U/6.3V_6	C144 EV@330u/2V_7343
C165 EV@.022u/16V_4	C138 EV@.022u/16V_4	C166 EV@.022u/16V_4	C122 EV@.022u/16V_4	C125 EV@.022u/16V_4	C185 EV@4.7U/6.3V_6	
C136 EV@.1U/10V_4	C147 EV@.1U/10V_4	C117 EV@.1U/10V_4	C167 EV@.1U/10V_4	C139 EV@.1U/10V_4	C184 EV@4.7U/6.3V_6	
C168 EV@.1U/10V_4	C150 EV@.1U/10V_4	C115 EV@.1U/10V_4	C149 EV@.1U/10V_4	C137 EV@.1U/10V_4		

SI modified

Follow Design Guide DG-04131-001 4.7uFx3 and 0.022x10 uF and 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

power up sequence

PXE 1.2VDD

PXE 1.1VDD

I/O 3.3V

NVCORE

1.8VFBDDQ

U23G

EV@N10M-GE1-B-U2/H

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

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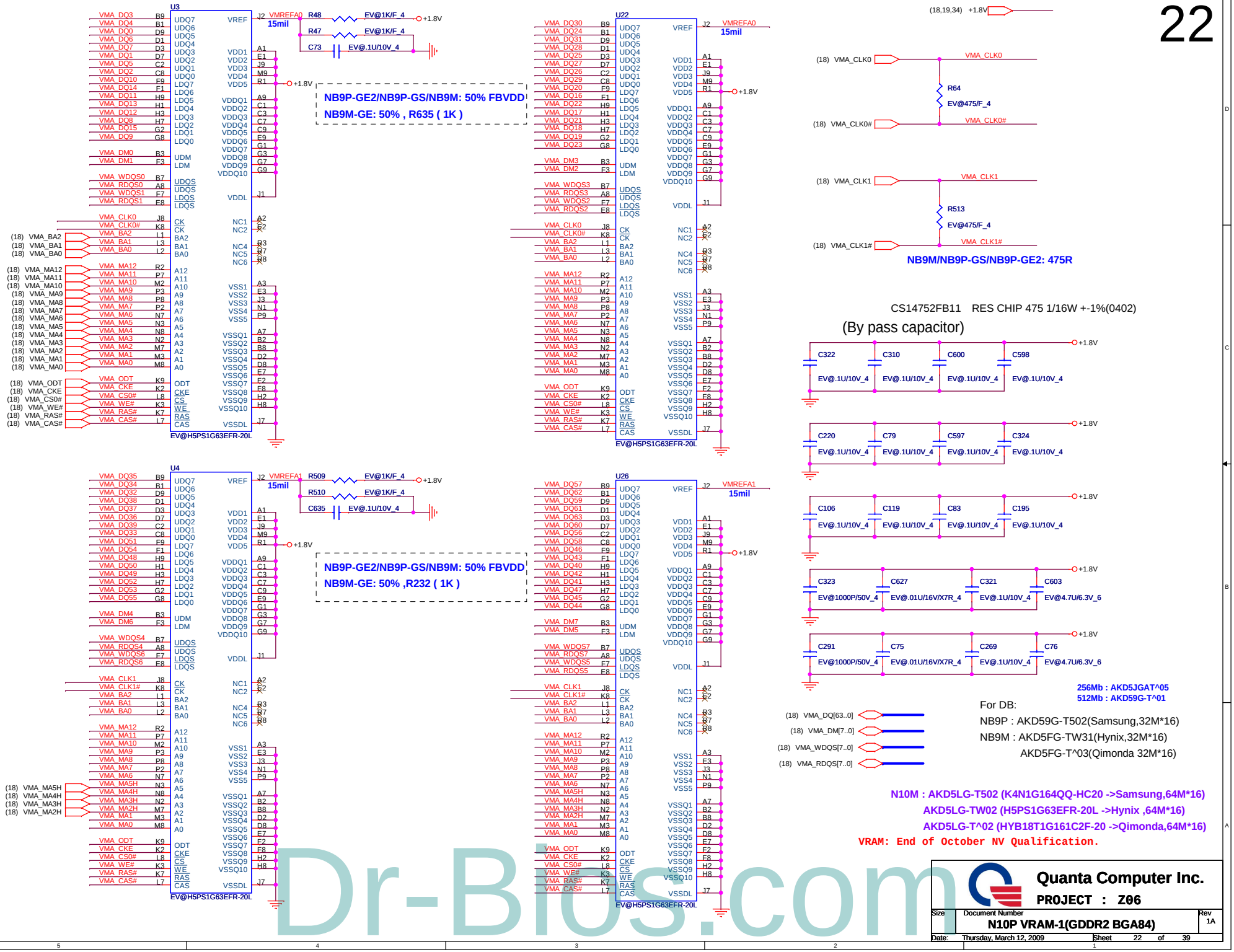

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Size	Document Number: N10P VRAM-1(GDDR2 BGA84)	Rev: 1A
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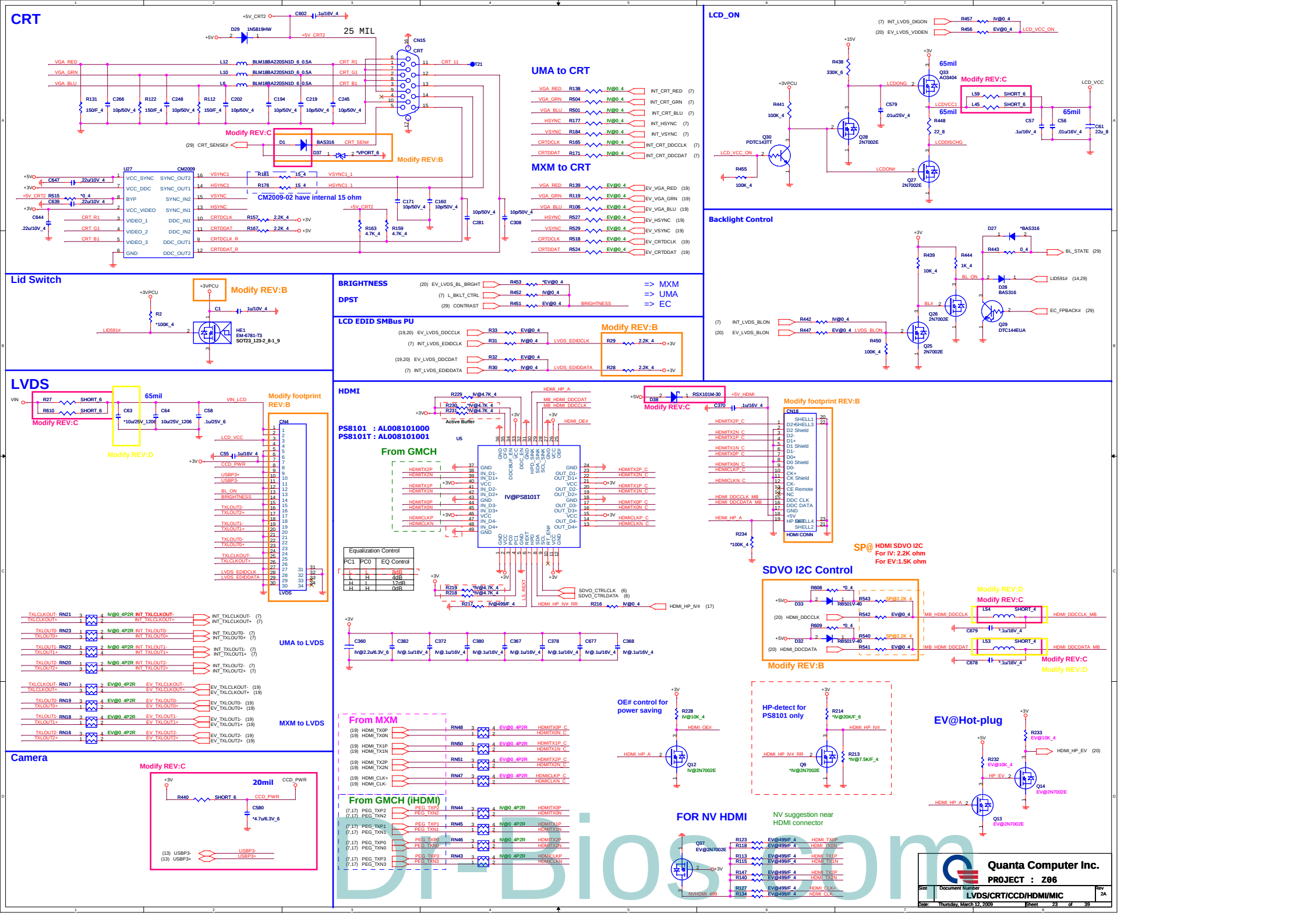
CRT
UMA to CRT
MXM to CRT
LCD_ON
Backlight Control
Lid Switch
BRIGHTNESS
DPST
LCD EDID SMBus PU
LVDS
HDMI
PS8101 : AL008101000
PS8101T : AL008101001
From GMCH
SDVO I2C Control
UMA to LVDS
MXM to LVDS
Camera
From MXM
From GMCH (iHDMI)
OE# control for power saving
HP-detect for PS8101 only
EV@Hot-plug
FOR NV HDMI
NV suggestion near HDMI connector
Modify REV:B
Modify REV:C
Modify REV:D
Modify footprint REV:B
CM2009-02 have internal 15 ohm
Quanta Computer Inc.
PROJECT : Z06
LVDS/CRT/CCD/HDMI/MIC
Thursday, March 12, 2009
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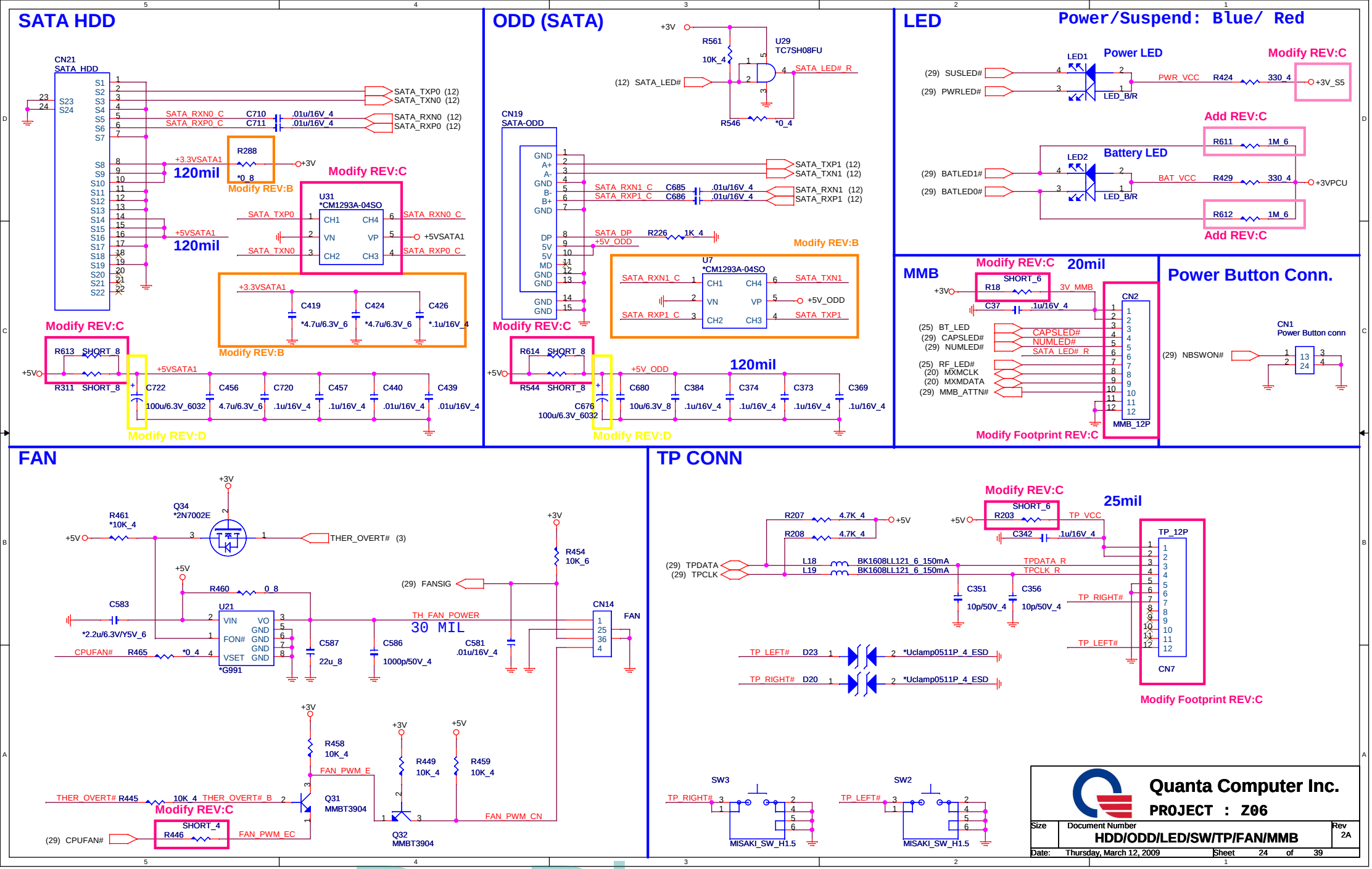
SATA HDD
CN21
SATA_HDD
SATA_TXP0 (12)
SATA_TXN0 (12)
SATA_RXN0 (12)
SATA_RXP0 (12)
SATA_RXN0_C
SATA_RXP0_C
C710 .01u/16V_4
C711 .01u/16V_4
R288
*0_8
+3.3VSATA1
120mil
+3V
Modify REV:C
Modify REV:B
U31
*CM1293A-04SO
SATA_TXP0
SATA_TXN0
SATA_RXN0_C
SATA_RXP0_C
+5VSATA1
120mil
C419 *4.7u/6.3V_6
C424 *4.7u/6.3V_6
C426 *.1u/16V_4
R613 SHORT_8
R311 SHORT_8
+5V
C722 100u/6.3V_6032
C456 4.7u/6.3V_6
C720 .1u/16V_4
C457 .1u/16V_4
C440 .01u/16V_4
C439 .01u/16V_4
Modify REV:D
ODD (SATA)
+3V
R561 10K_4
U29 TC7SH08FU
(12) SATA_LED#
SATA_LED# R
R546 *0_4
CN19
SATA-ODD
SATA_TXP1 (12)
SATA_TXN1 (12)
SATA_RXN1 (12)
SATA_RXP1 (12)
SATA_RXN1_C C685 .01u/16V_4
SATA_RXP1_C C686 .01u/16V_4
SATA_DP
+5V_ODD
R226 1K_4
U7
*CM1293A-04SO
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1
SATA_TXP1
+5V_ODD
R614 SHORT_8
R544 SHORT_8
C676 100u/6.3V_6032
C680 10u/6.3V_8
C384 .1u/16V_4
C374 .1u/16V_4
C373 .1u/16V_4
C369 .1u/16V_4
120mil
LED
Power/Suspend: Blue/ Red
LED1
Power LED
(29) SUSLED#
(29) PWRLED#
PWR_VCC
R424 330_4
+3V_S5
LED_B/R
Add REV:C
LED2
Battery LED
(29) BATLED1#
(29) BATLED0#
BAT_VCC
R429 330_4
+3VPCU
R611 1M_6
R612 1M_6
MMB
Modify REV:C
20mil
SHORT_6
R18
3V_MMB
C37 .1u/16V_4
CN2
(25) BT_LED
(29) CAPSLED#
(29) NUMLED#
(25) RF_LED#
(20) MXMCLK
(20) MXMDATA
(29) MMB_ATTN#
CAPSLED#
NUMLED#
SATA_LED# R
MMB_12P
Modify Footprint REV:C
Power Button Conn.
CN1
Power Button conn
(29) NBSWON#
FAN
Q34
*2N7002E
R461 *10K_4
THER_OVERT# (3)
R454 10K_6
(29) FANSIG
R460 0_8
C583 *2.2u/6.3V/Y5V_6
U21
VIN VO
FON#
VSET
*G991
CPUFANP#
R465 *0_4
TH_FAN_POWER
30 MIL
C587 22u_8
C586 1000p/50V_4
C581 .01u/16V_4
CN14
FAN
R458 10K_4
FAN_PWM_E
R449 10K_4
R459 10K_4
THER_OVERT# R445 10K_4
THER_OVERT# B
Q31 MMBT3904
Q32 MMBT3904
FAN_PWM_CN
FAN_PWM_EC
(29) CPUFAN#
SHORT_4
R446
TP CONN
Modify REV:C
25mil
R207 4.7K_4
R208 4.7K_4
SHORT_6
R203
TP_VCC
C342 .1u/16V_4
(29) TPDATA
(29) TPCLK
L18 BK1608LL121_6_150mA
L19 BK1608LL121_6_150mA
TPDATA_R
TPCLK_R
C351 10p/50V_4
C356 10p/50V_4
TP_12P
TP_RIGHT#
TP_LEFT#
TP_LEFT# D23
TP_RIGHT# D20
*Uclamp0511P_4_ESD
CN7
Modify Footprint REV:C
SW3
SW2
MISAKI_SW_H1.5
Quanta Computer Inc.
PROJECT : Z06
Size
Document Number
HDD/ODD/LED/SW/TP/FAN/MMB
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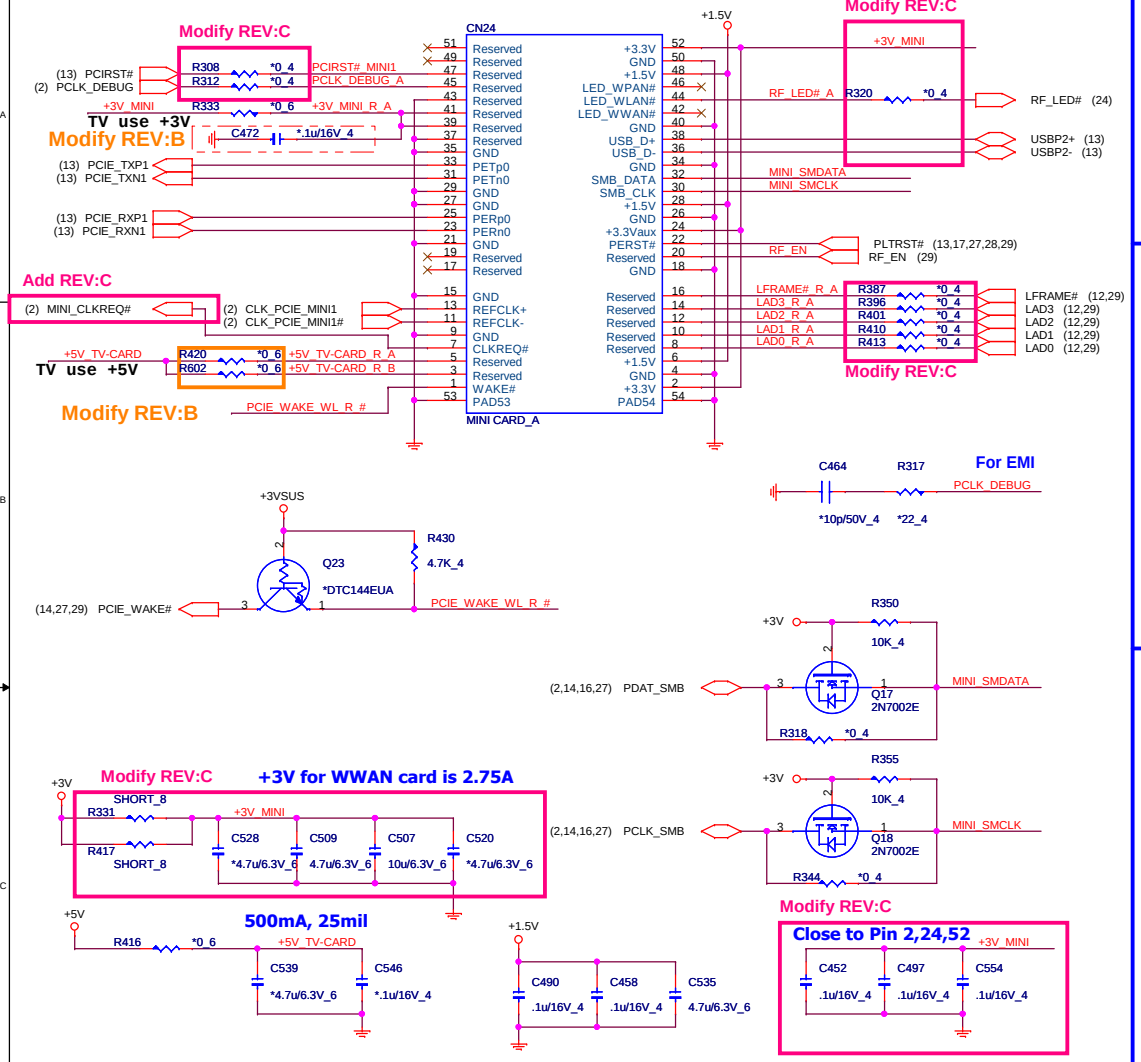
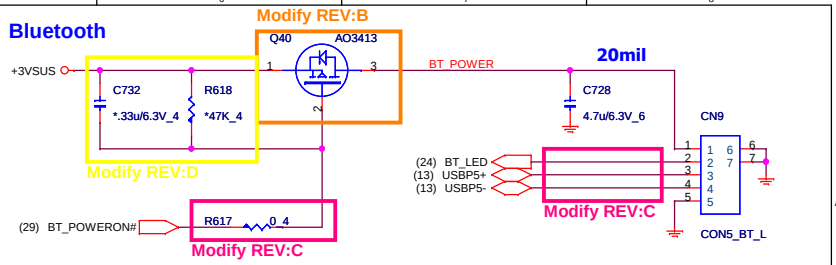
MINI-CARD

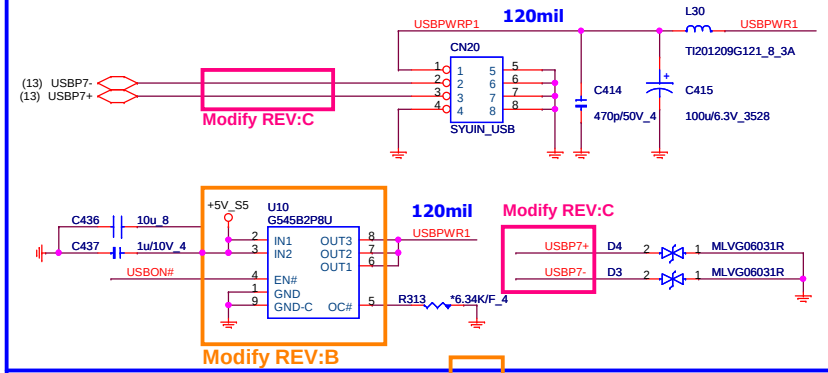


Bluetooth

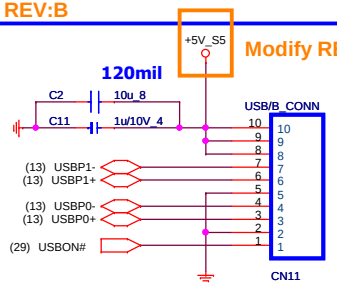


If stuff C732 & R618 , Pls will
R617 change to 4.7K ohm
(P/N : CS24702JB38)

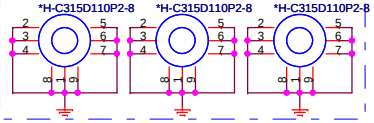
INT. USB



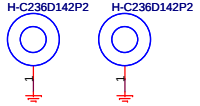
EXT. USB



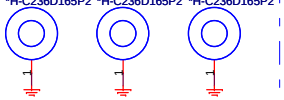
8 X 2.8



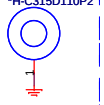
6 X 3.6



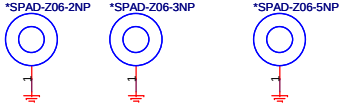
6 X 4.2

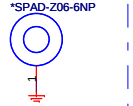


8 X 2.8

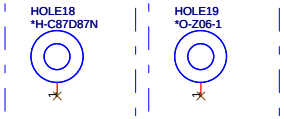


SOLDER MASK PAD

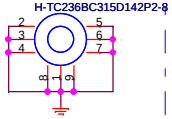




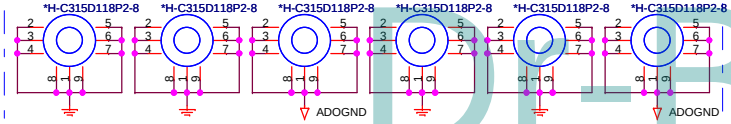
BOARD LOCK PAD



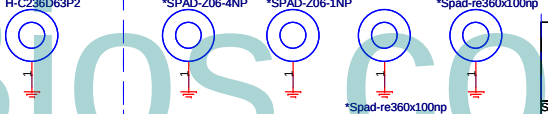
TOP 8 X 3.6
BOT 6 X 3.6



8 X 3.0



MDC 6 X 1.6



Quanta Computer Inc.
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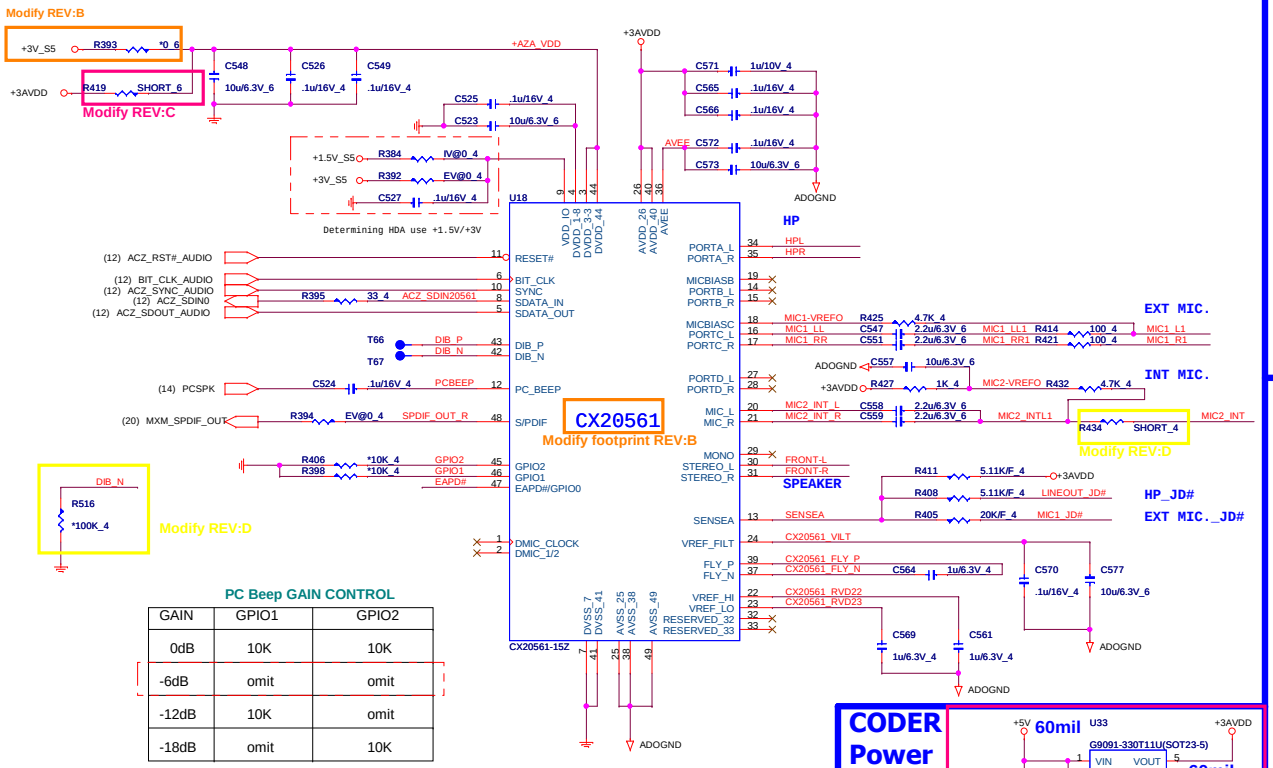
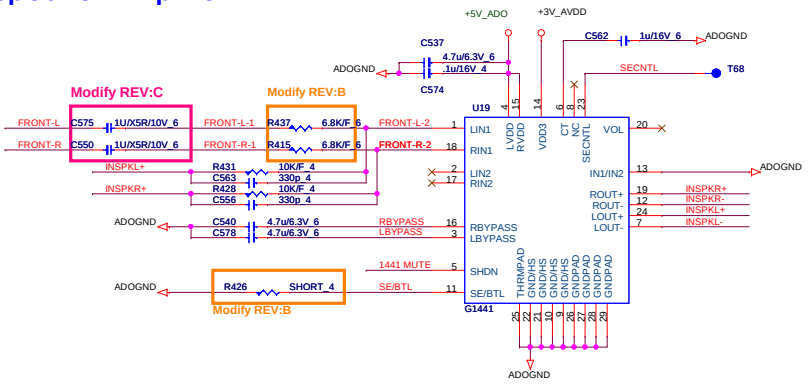
Codec CX20561-15Z (QFN)

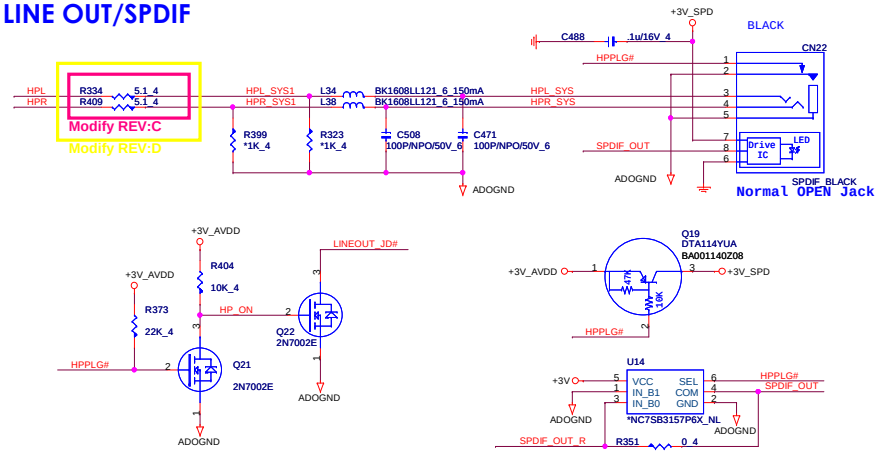


GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

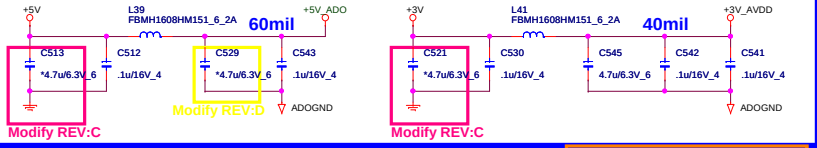
Speaker Amplifier



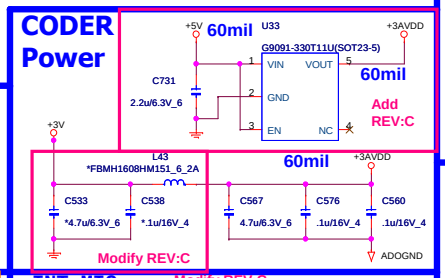
LINE OUT/SPDIF



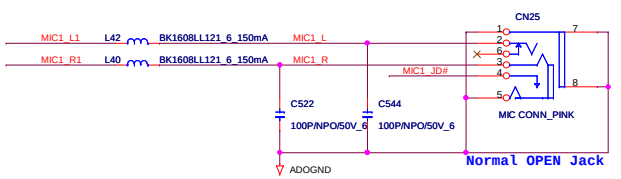
AMP Power



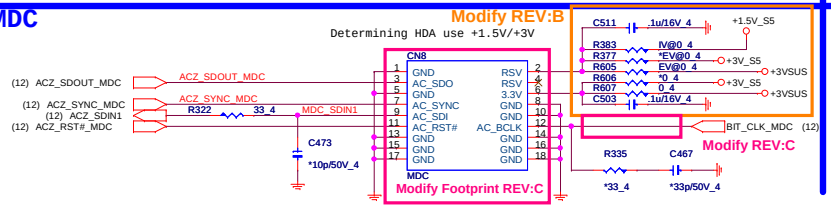
CODER Power



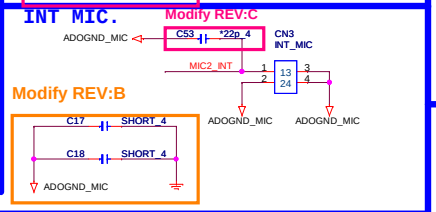
MIC



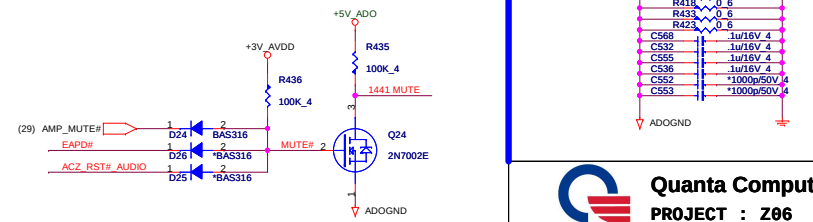
MDC



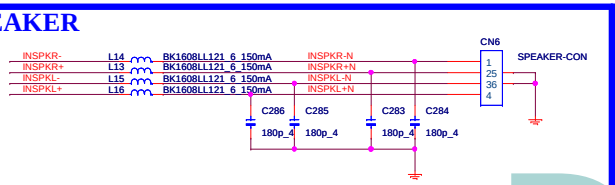
INT MIC.



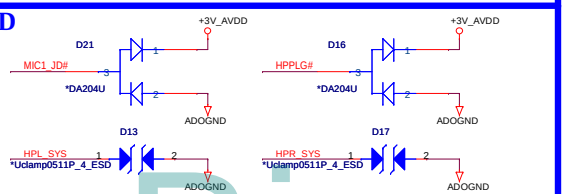
MUTE



SPEAKER



ESD



Quanta Computer Inc.	
PROJECT : Z06	
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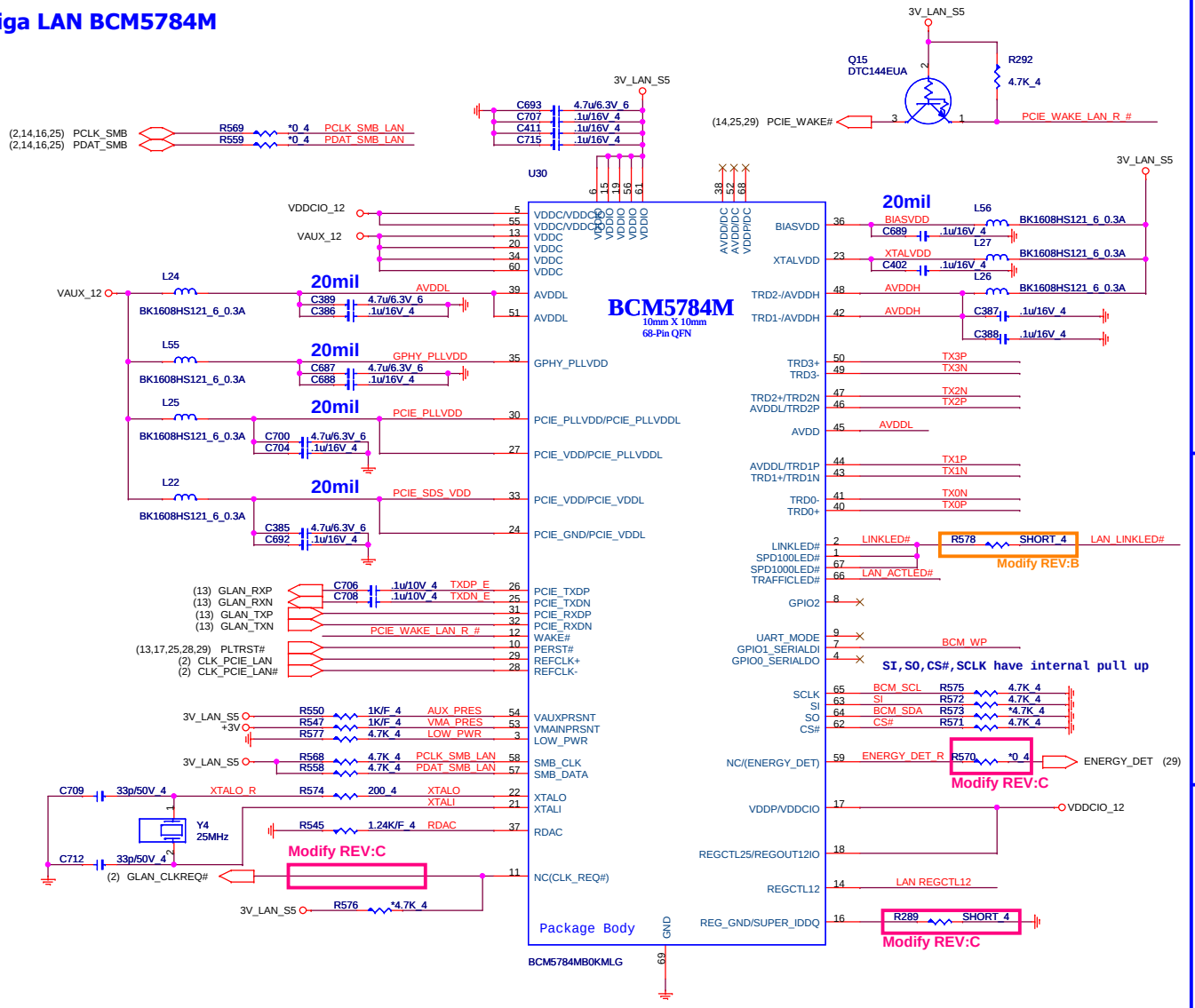
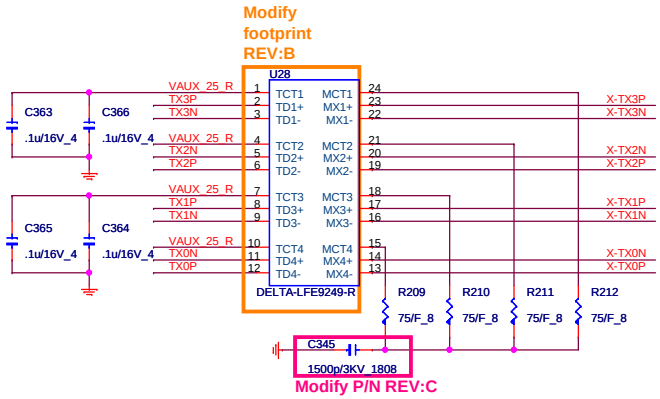
Giga LAN BCM5784M

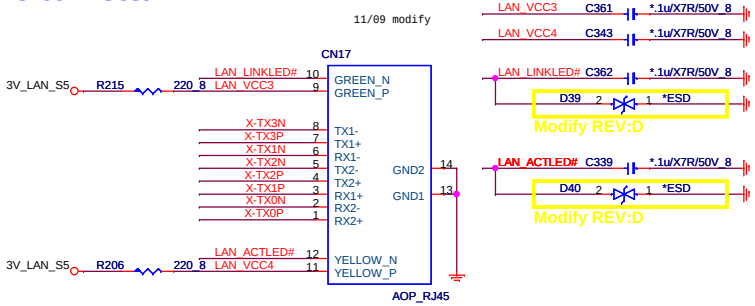


Transfomer

Source 1: DELTA LFE9249-R DB0ZR1LAN11
Source 2: BOT GST5009B DB0Z06LAN00

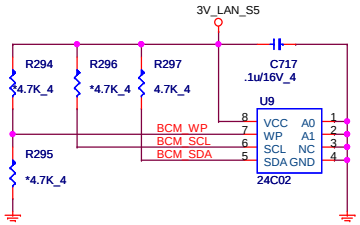


RJ45 connector



EMI

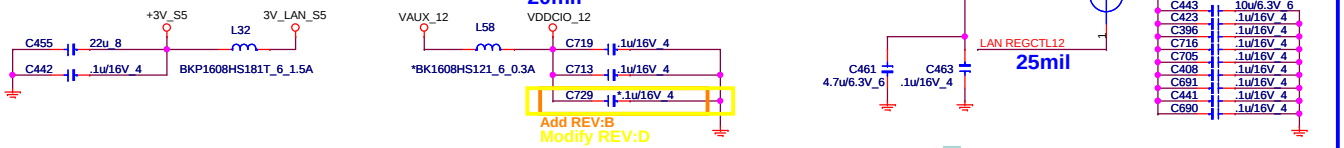
EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24LC02	1	0	0	0

LAN POWER



Quanta Computer Inc.
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	GigaLAN BCM5784M & RJ45	2A
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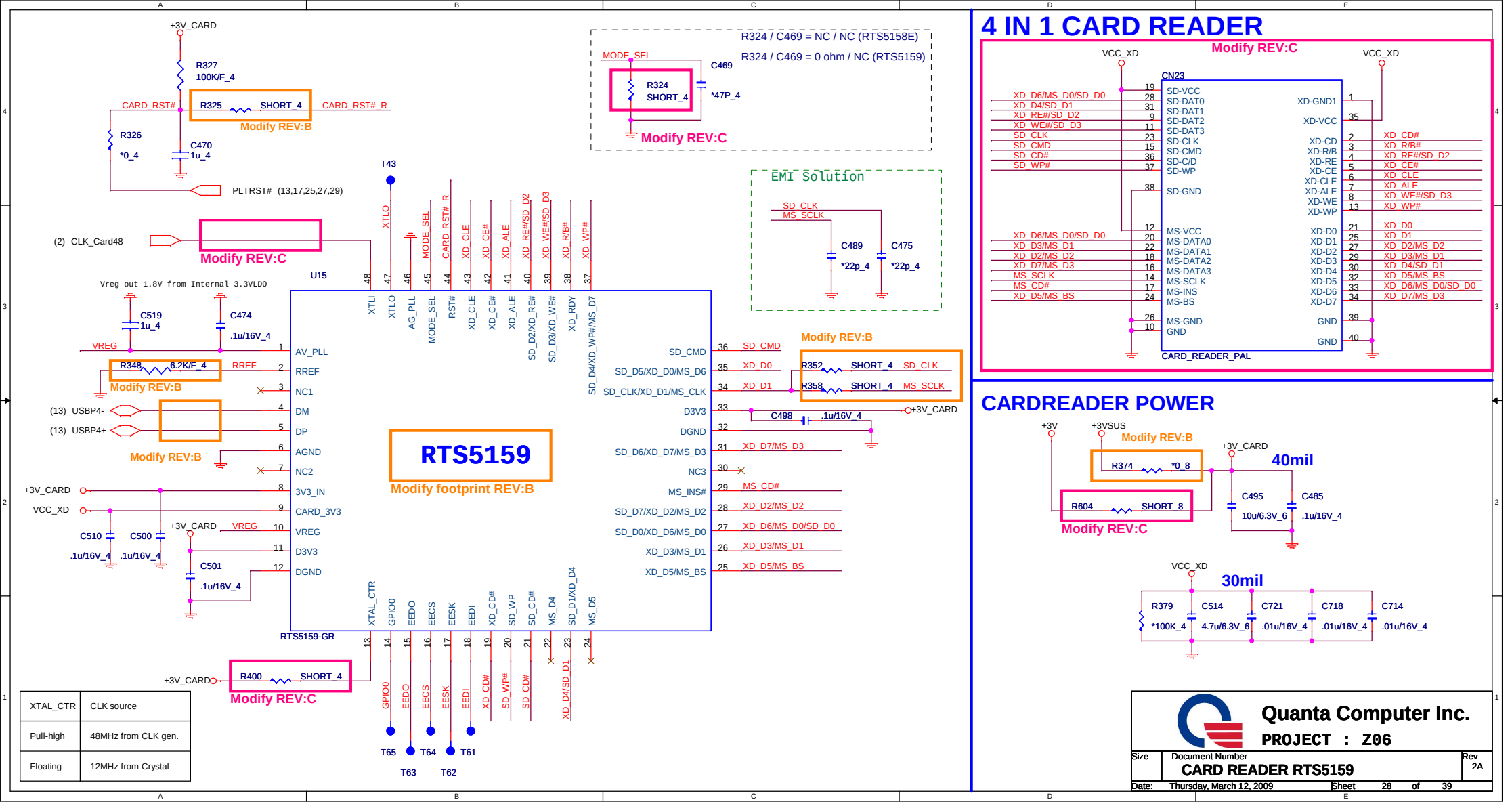
4 IN 1 CARD READER
Modify REV:C
VCC_XD
CN23
XD_D6/MS_D0/SD_D0
XD_D4/SD_D1
XD_RE#/SD_D2
XD_WE#/SD_D3
SD_CLK
SD_CMD
SD_CD#
SD_WP#
SD-VCC
SD-DAT0
SD-DAT1
SD-DAT2
SD-DAT3
SD-CLK
SD-CMD
SD-C/D
SD-WP
SD-GND
MS-VCC
MS-DATA0
MS-DATA1
MS-DATA2
MS-DATA3
MS-SCLK
MS-INS
MS-BS
MS-GND
GND
XD-GND1
XD-VCC
XD-CD
XD-R/B
XD-RE
XD-CE
XD-CLE
XD-ALE
XD-WE
XD-WP
XD-D0
XD-D1
XD-D2
XD-D3
XD-D4
XD-D5
XD-D6
XD-D7
CARD_READER_PAL
CARDREADER POWER
+3V
+3VSUS
Modify REV:B
+3V_CARD
40mil
R374
*0_8
R604
SHORT_8
Modify REV:C
C495
C485
10u/6.3V_6
.1u/16V_4
30mil
R379
*100K_4
C514
4.7u/6.3V_6
C721
.01u/16V_4
C718
C714
R327
100K/F_4
CARD_RST#
R325
SHORT_4
CARD_RST#_R
R326
*0_4
C470
1u_4
PLTRST# (13,17,25,27,29)
R324 / C469 = NC / NC (RTS5158E)
R324 / C469 = 0 ohm / NC (RTS5159)
MODE_SEL
R324
SHORT_4
C469
*47P_4
EMI Solution
SD_CLK
MS_SCLK
C489
*22p_4
C475
*22p_4
T43
(2) CLK_Card48
Modify REV:C
U15
Vreg out 1.8V from Internal 3.3VLDO
C519
1u_4
C474
.1u/16V_4
VREG
R348
6.2K/F_4
RREF
Modify REV:B
(13) USBP4-
(13) USBP4+
Modify REV:B
RTS5159
Modify footprint REV:B
RTS5159-GR
AV_PLL
RREF
NC1
DM
DP
AGND
NC2
3V3_IN
CARD_3V3
VREG
D3V3
DGND
XTLI
XTLO
AG_PLL
MODE_SEL
RST#
XD_CLE
XD_CE#
XD_ALE
SD_D2/XD_RE#
SD_D3/XD_WE#
XD_RDY
SD_D4/XD_WP#/MS_D7
SD_CMD
SD_D5/XD_D0/MS_D6
SD_CLK/XD_D1/MS_CLK
D3V3
DGND
SD_D6/XD_D7/MS_D3
NC3
MS_INS#
SD_D7/XD_D2/MS_D2
SD_D0/XD_D6/MS_D0
XD_D3/MS_D1
XD_D5/MS_BS
XTAL_CTR
GPIO0
EEDO
EECS
EESK
EEDI
XD_CD#
SD_WP
SD_CD#
MS_D4
SD_D1/XD_D4
MS_D5
XD_D4/SD_D1
R352
SHORT_4
SD_CLK
R358
SHORT_4
MS_SCLK
C498
.1u/16V_4
+3V_CARD
R400
SHORT_4
Modify REV:C
XD_CD#
XD_D0
XD_D1
XD_D7/MS_D3
MS_CD#
XD_D2/MS_D2
XD_D6/MS_D0/SD_D0
XD_D3/MS_D1
XD_D5/MS_BS
C510
.1u/16V_4
C500
.1u/16V_4
C501
.1u/16V_4
VCC_XD
+3V_CARD
VREG
XTAL_CTR | CLK source
Pull-high | 48MHz from CLK gen.
Floating | 12MHz from Crystal
Quanta Computer Inc.
PROJECT : Z06
Size
Document Number
CARD READER RTS5159
Rev
2A
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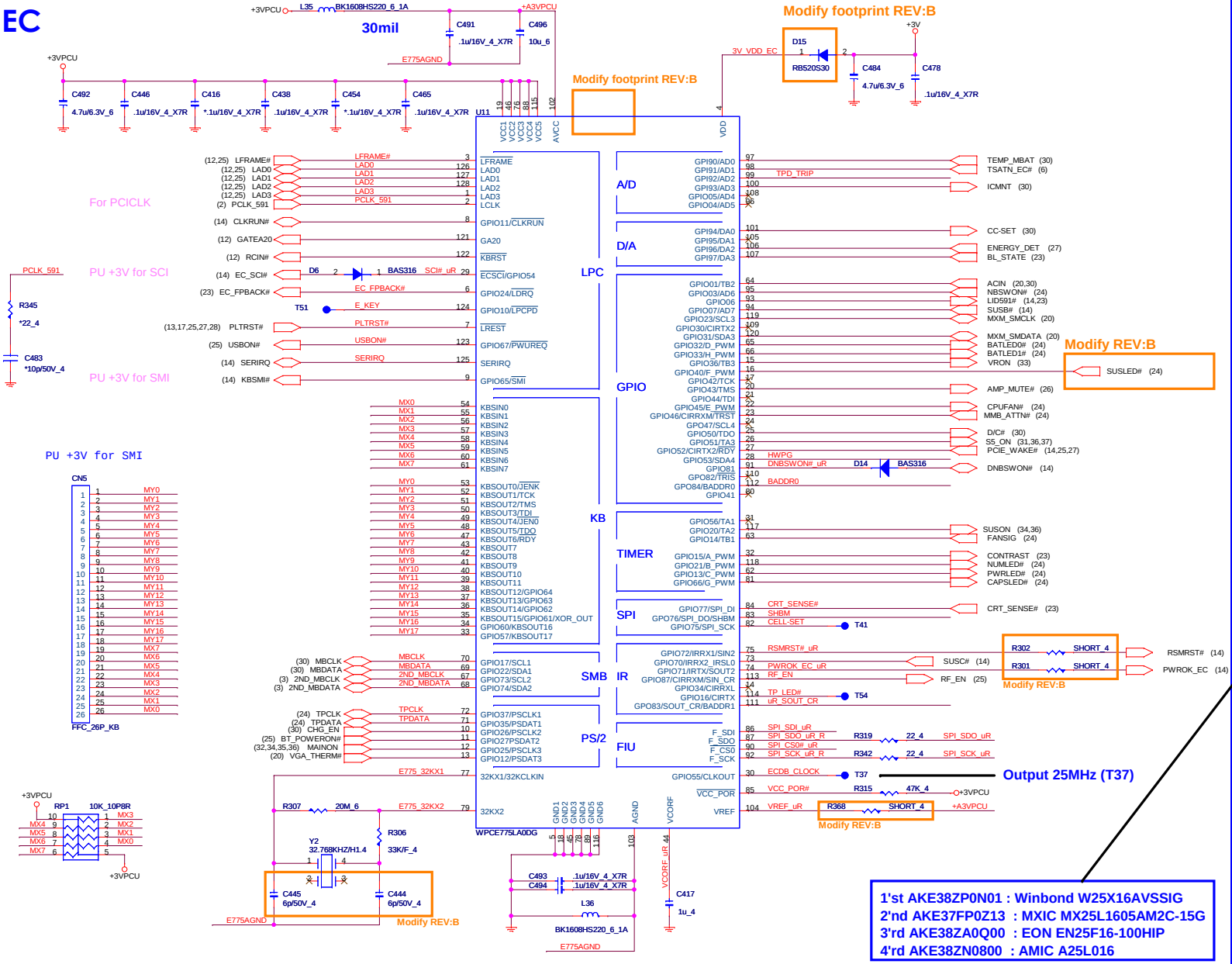
EC

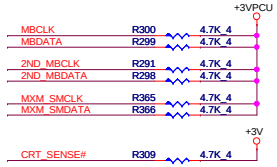


I/O ADDRESS SETTING

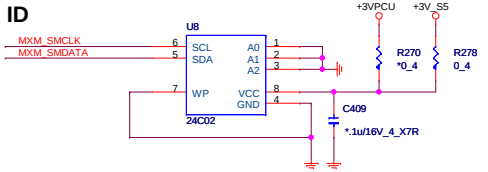
BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

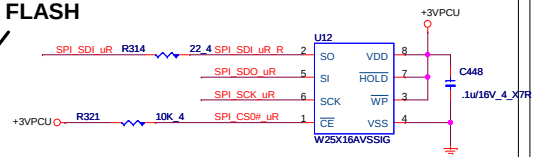
SM BUS PU



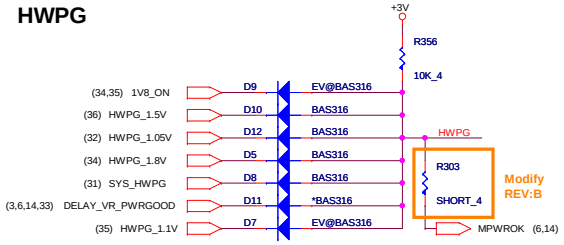
ACER ID



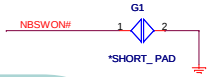
SPI FLASH



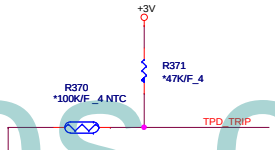
HWPG



POWER-ON PAD



Thermal Sensor



INTERNAL KEYBOARD STRIP SET

Quanta Computer Inc.
PROJECT : Z06

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	WPCE775C_0DG & FLASH	2A
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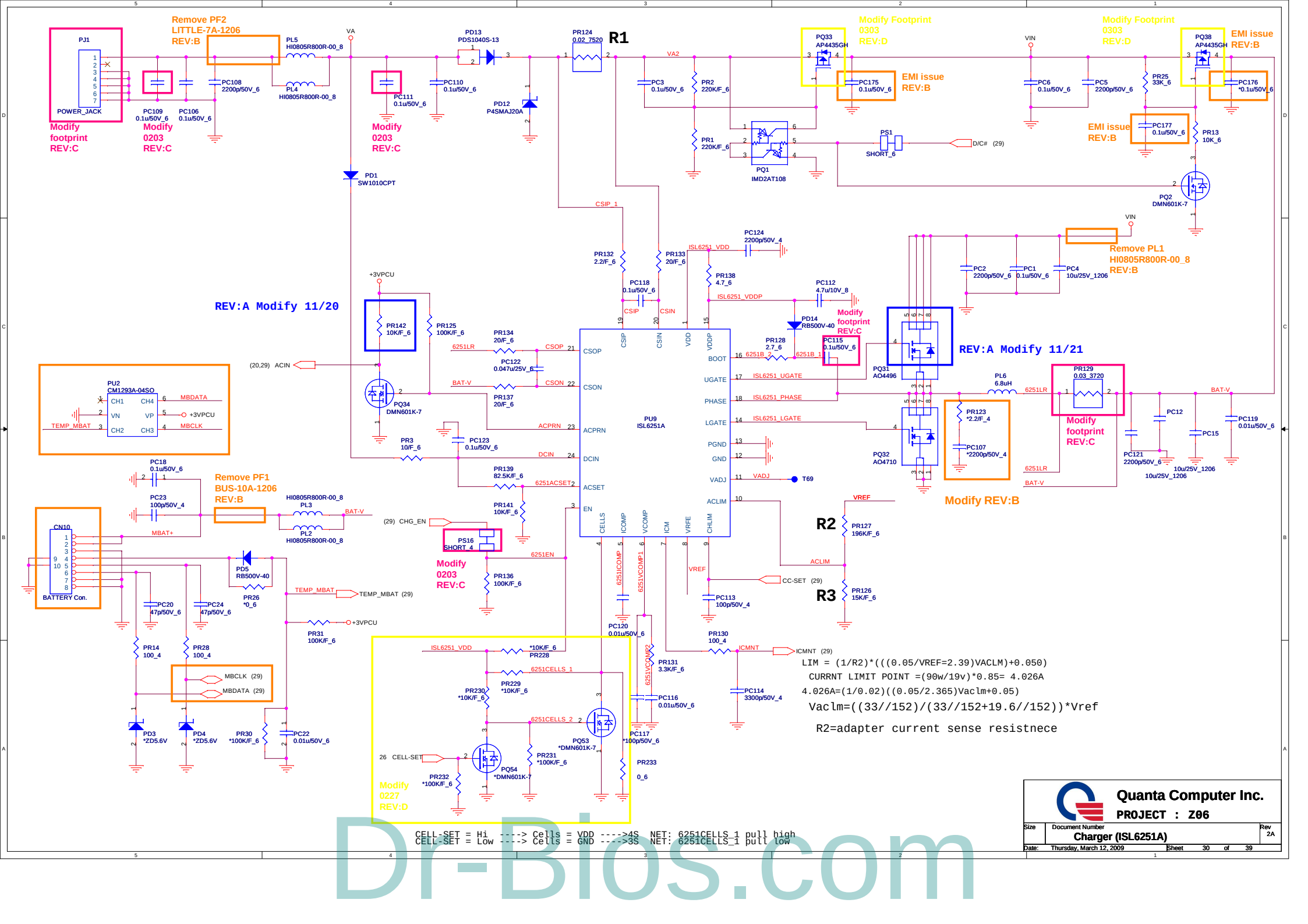
Remove PF2
LITTLE-7A-1206
REV:B
PJ1
POWER_JACK
PC109 0.1u/50V_6
PC106 0.1u/50V_6
PC108 2200p/50V_6
PL5 HI0805R800R-00_8
PL4 HI0805R800R-00_8
Modify footprint REV:C
Modify 0203 REV:C
VA
PC111 0.1u/50V_6
PD13 PDS1040S-13
PC110 0.1u/50V_6
PD12 P4SMAJ20A
PD1 SW1010CPT
PR124 0.02_7520
R1
Modify Footprint 0303 REV:D
PQ33 AP4435GH
PC175 0.1u/50V_6
EMI issue REV:B
VA2
PC3 0.1u/50V_6
PR2 220K/F_6
PR1 220K/F_6
PQ1 IMD2AT108
PS1 SHORT_6
D/C# (29)
VIN
PC6 0.1u/50V_6
PC5 2200p/50V_6
PR25 33K_6
PC177 0.1u/50V_6
PR13 10K_6
PQ38 AP4435GH
PC176 *0.1u/50V_6
PQ2 DMN601K-7
REV:A Modify 11/20
REV:A Modify 11/21
CSIP_1
PR132 2.2/F_6
PR133 20/F_6
PC118 0.1u/50V_6
CSIP
CSIN
ISL6251_VDD
PC124 2200p/50V_4
PR138 4.7_6
PC112 4.7u/10V_8
ISL6251_VDDP
PD14 RB500V-40
PC115 0.1u/50V_6
Modify footprint REV:C
+3VPCU
PR142 10K/F_6
PR125 100K/F_6
PR134 20/F_6
6251LR
CSOP
PC122 0.047u/25V_6
BAT-V
CSON
PR137 20/F_6
(20,29) ACIN
PQ34 DMN601K-7
PU2 CM1293A-04SO
CH1 CH4 MBDATA
VN VP +3VPCU
CH2 CH3 MBCLK
TEMP_MBAT
PU9 ISL6251A
CSOP CSON ACPRN DCIN ACSET EN
CSIP CSIN VDD VDDP
BOOT UGATE PHASE LGATE PGND GND VADJ ACLIM
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PR128 2.7_6
6251B_2
6251B_1
PQ31 AO4496
PQ32 AO4710
PL6 6.8uH
PR129 0.03_3720
Modify footprint REV:C
PR123 *2.2/F_4
PC107 *2200p/50V_4
Modify REV:B
Remove PL1
HI0805R800R-00_8
REV:B
PC2 2200p/50V_6
PC1 0.1u/50V_6
PC4 10u/25V_1206
PC12
PC15
PC121 2200p/50V_6
10u/25V_1206
PC119 0.01u/50V_6
PR3 10/F_6
PC123 0.1u/50V_6
DCIN
PR139 82.5K/F_6
6251ACSET
PR141 10K/F_6
PC18 0.1u/50V_6
PC23 100p/50V_4
Remove PF1
BUS-10A-1206
REV:B
HI0805R800R-00_8 PL3
HI0805R800R-00_8 PL2
BAT-V
MBAT+
(29) CHG_EN
PS16 SHORT_4
Modify 0203 REV:C
6251EN
PR136 100K/F_6
CN10
BATTERY Con.
PD5 RB500V-40
PR26 *0_6
TEMP_MBAT
TEMP_MBAT (29)
+3VPCU
PR31 100K/F_6
PC20 47p/50V_6
PC24 47p/50V_6
PR14 100_4
PR28 100_4
MBCLK (29)
MBDATA (29)
PD3 *ZD5.6V
PD4 *ZD5.6V
PR30 *100K/F_6
PC22 0.01u/50V_6
R2
R3
VREF
PR127 196K/F_6
ACLIM
CC-SET (29)
PR126 15K/F_6
PC113 100p/50V_4
6251ICOMP
6251VCOMP1
6251VCOMP2
PC120 0.01u/50V_6
PR130 100_4
ICMNT
ICMNT (29)
PR131 3.3K/F_6
PC116 0.01u/50V_6
PC114 3300p/50V_4
PC117 *100p/50V_6
PR233 0_6
ISL6251_VDD
*10K/F_6 PR228
6251CELLS_1
PR229 *10K/F_6
PR230 *10K/F_6
6251CELLS_2
PQ53 *DMN601K-7
PR231 *100K/F_6
26 CELL-SET
PQ54 *DMN601K-7
PR232 *100K/F_6
Modify 0227 REV:D
LIM = (1/R2)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((33//152)/(33//152+19.6//152))*Vref
R2=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ----->4S NET: 6251CELLS_1 pull high
CELL-SET = Low ----> Cells = GND ----->3S NET: 6251CELLS_1 pull low
Quanta Computer Inc.
PROJECT : Z06
Size
Document Number
Charger (ISL6251A)
Rev 2A
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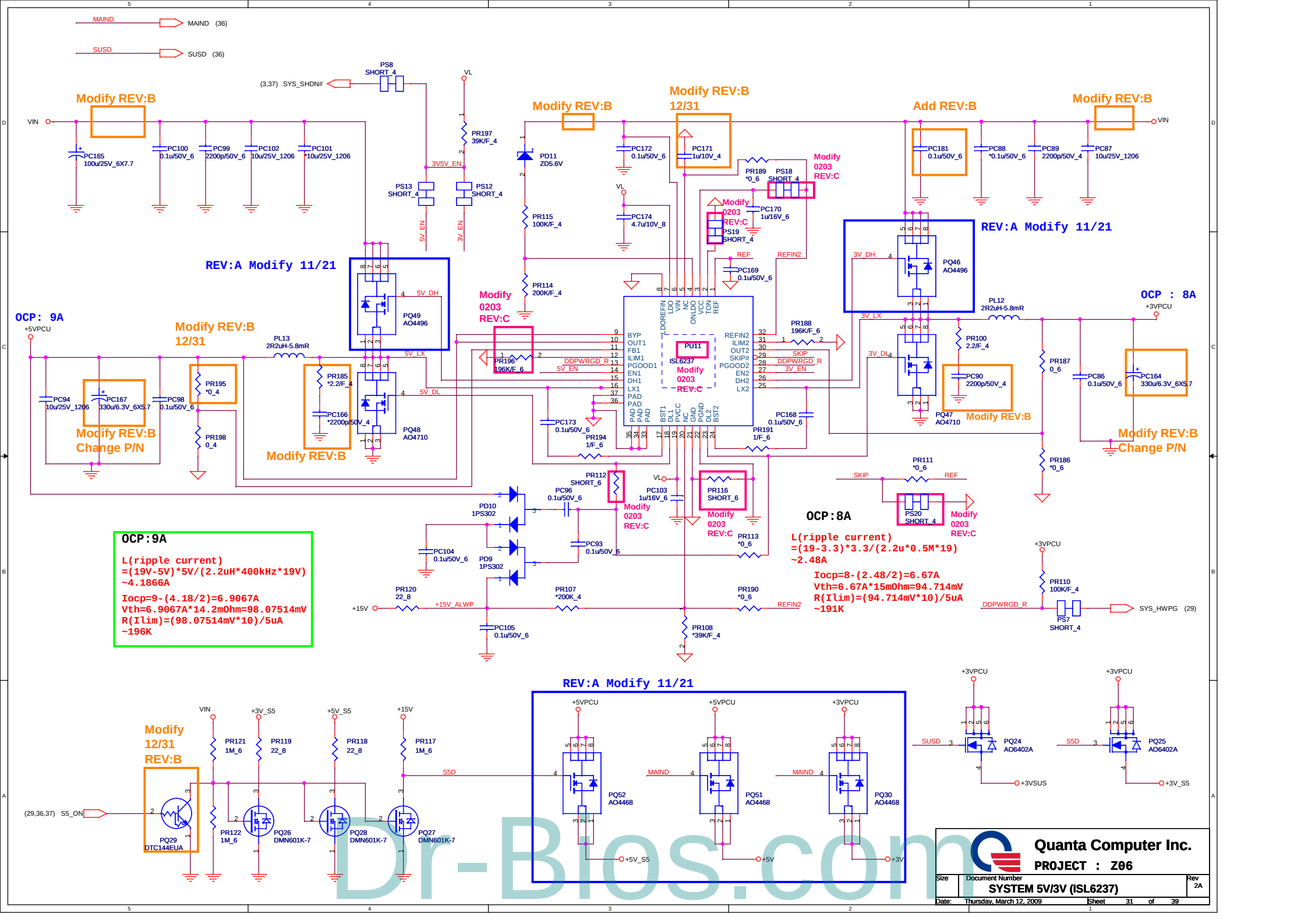
MAIND
MAIND (36)
SUSD
SUSD (36)
(3,37) SYS_SHDN#
PS8 SHORT_4
VL
VIN
Modify REV:B
PC165 100u/25V_6X7.7
PC100 0.1u/50V_6
PC99 2200p/50V_6
PC102 10u/25V_1206
PC101 *10u/25V_1206
PR197 39K/F_4
3V5V_EN
PS13 SHORT_4
PS12 SHORT_4
5V_EN
3V_EN
PD11 ZD5.6V
PR115 100K/F_4
PR114 200K/F_4
Modify REV:B
Modify REV:B 12/31
PC172 0.1u/50V_6
PC171 1u/10V_4
PC174 4.7u/10V_8
PR189 *0_6
PS18 SHORT_4
Modify 0203 REV:C
PC170 1u/16V_6
PS19 SHORT_4
Add REV:B
PC181 0.1u/50V_6
PC88 *0.1u/50V_6
PC89 2200p/50V_4
PC87 10u/25V_1206
Modify REV:B
REV:A Modify 11/21
PQ46 AO4496
3V_DH
3V_LX
3V_DL
PL12 2R2uH-5.8mR
OCP : 8A
+3VPCU
PR100 2.2/F_4
PC90 2200p/50V_4
PR187 0_6
PC86 0.1u/50V_6
PC164 330u/6.3V_6X5.7
Modify REV:B
Modify REV:B Change P/N
REV:A Modify 11/21
PQ49 AO4496
5V_DH
5V_LX
5V_DL
PQ48 AO4710
Modify 0203 REV:C
REF
REFIN2
PC169 0.1u/50V_6
PU11
ISL6237
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND GND DL2 BST2
PR188 196K/F_6
SKIP
DDPWRGD_R
5V_EN
3V_EN
PR196 196K/F_6
PC173 0.1u/50V_6
PR194 1/F_6
PC168 0.1u/50V_6
PR191 1/F_6
PQ47 AO4710
Modify REV:B
OCP: 9A
+5VPCU
PL13 2R2uH-5.8mR
PC94 10u/25V_1206
PC167 330u/6.3V_6X5.7
PC98 0.1u/50V_6
PR195 *0_4
PR198 0_4
Modify REV:B 12/31
Modify REV:B Change P/N
PR185 *2.2/F_4
PC166 *2200p/50V_4
Modify REV:B
PR112 SHORT_6
PC96 0.1u/50V_6
PC103 1u/16V_6
PR116 SHORT_6
Modify 0203 REV:C
PD10 1PS302
PD9 1PS302
PC104 0.1u/50V_6
PC93 0.1u/50V_6
PR113 *0_6
PR111 *0_6
SKIP
REF
PS20 SHORT_4
Modify 0203 REV:C
PR186 *0_6
OCP:8A
L(ripple current) =(19-3.3)*3.3/(2.2u*0.5M*19) ~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
OCP:9A
L(ripple current) =(19V-5V)*5V/(2.2uH*400kHz*19V) ~4.1866A
Iocp=9-(4.18/2)=6.9067A
Vth=6.9067A*14.2mOhm=98.07514mV
R(Ilim)=(98.07514mV*10)/5uA
~196K
PR120 22_8
+15V
+15V_ALWP
PR107 *200K_4
PR190 *0_6
REFIN2
PC105 0.1u/50V_6
PR108 *39K/F_4
PR110 100K/F_4
DDPWRGD_R
PS7 SHORT_4
SYS_HWPG (29)
REV:A Modify 11/21
PQ52 AO4468
PQ51 AO4468
PQ30 AO4468
+5V_S5
+5V
+3V
Modify 12/31 REV:B
PR121 1M_6
PR119 22_8
PR118 22_8
PR117 1M_6
S5D
(29,36,37) S5_ON
PQ29 DTC144EUA
PR122 1M_6
PQ26 DMN601K-7
PQ28 DMN601K-7
PQ27 DMN601K-7
PQ24 AO6402A
PQ25 AO6402A
SUSD
S5D
+3VSUS
+3V_S5
Quanta Computer Inc.
PROJECT : Z06
SYSTEM 5V/3V (ISL6237)
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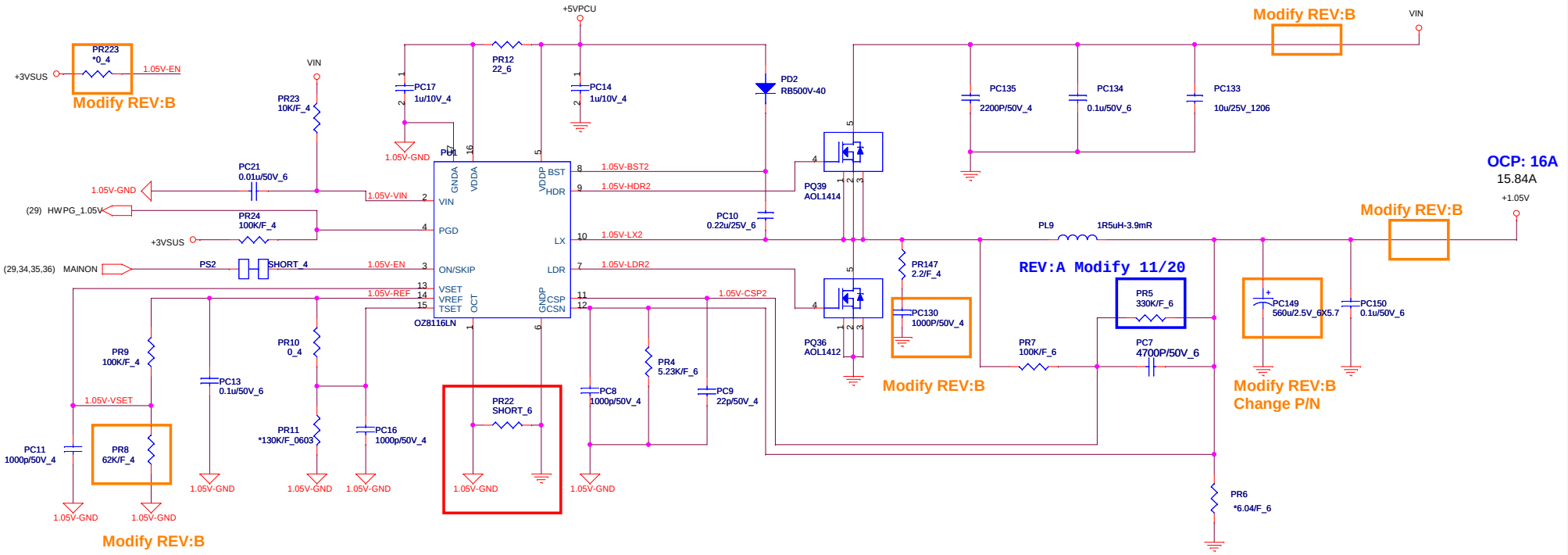
VTT 1.05V



Quanta Computer Inc.		
PROJECT : Z06		
Size	Document Number: +1.05V (OZ8116LN)	Rev 2A
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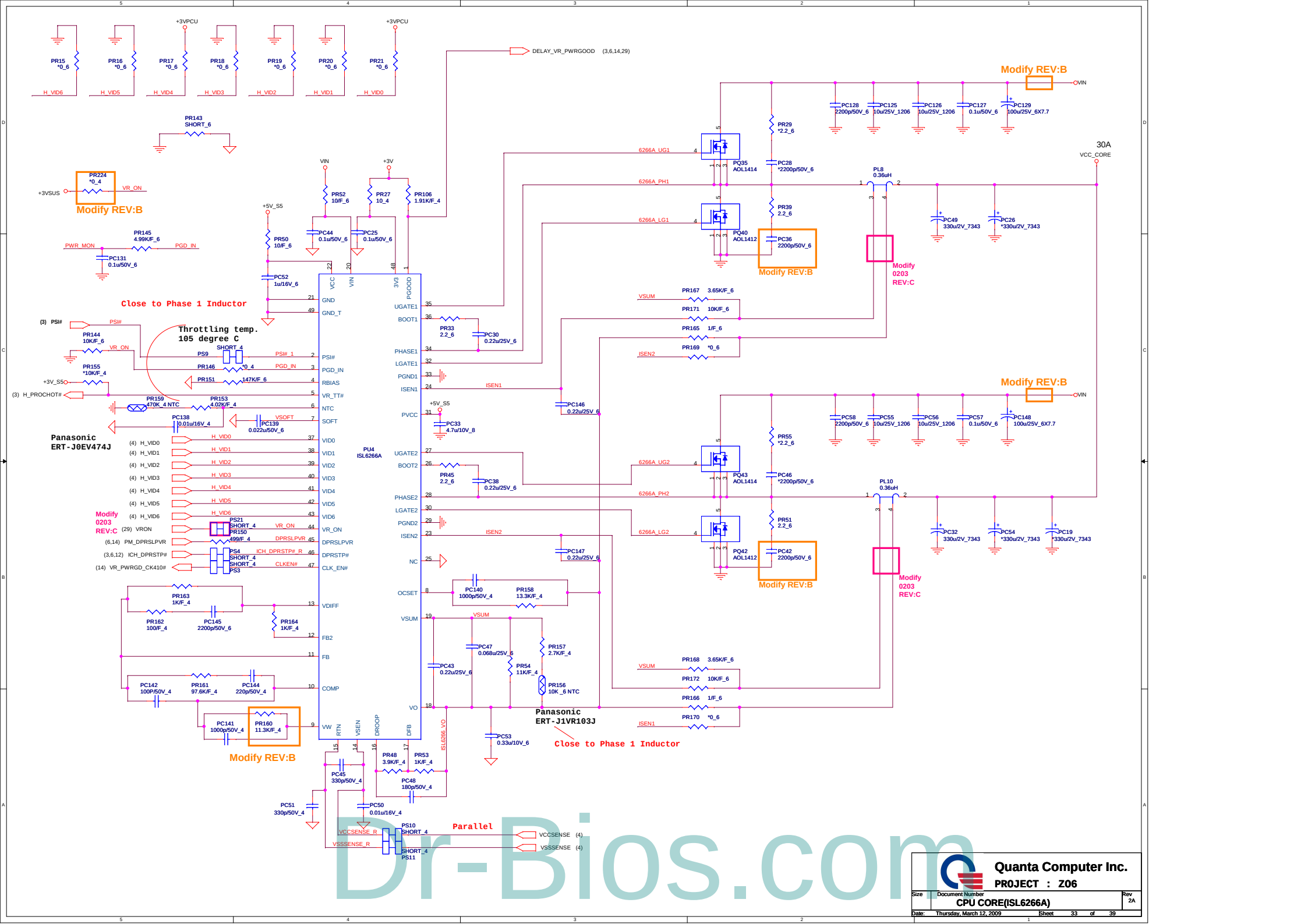

Quanta Computer Inc.		
PROJECT : Z06		
Size	Document Number: CPU CORE(ISL6266A)	Rev 2A
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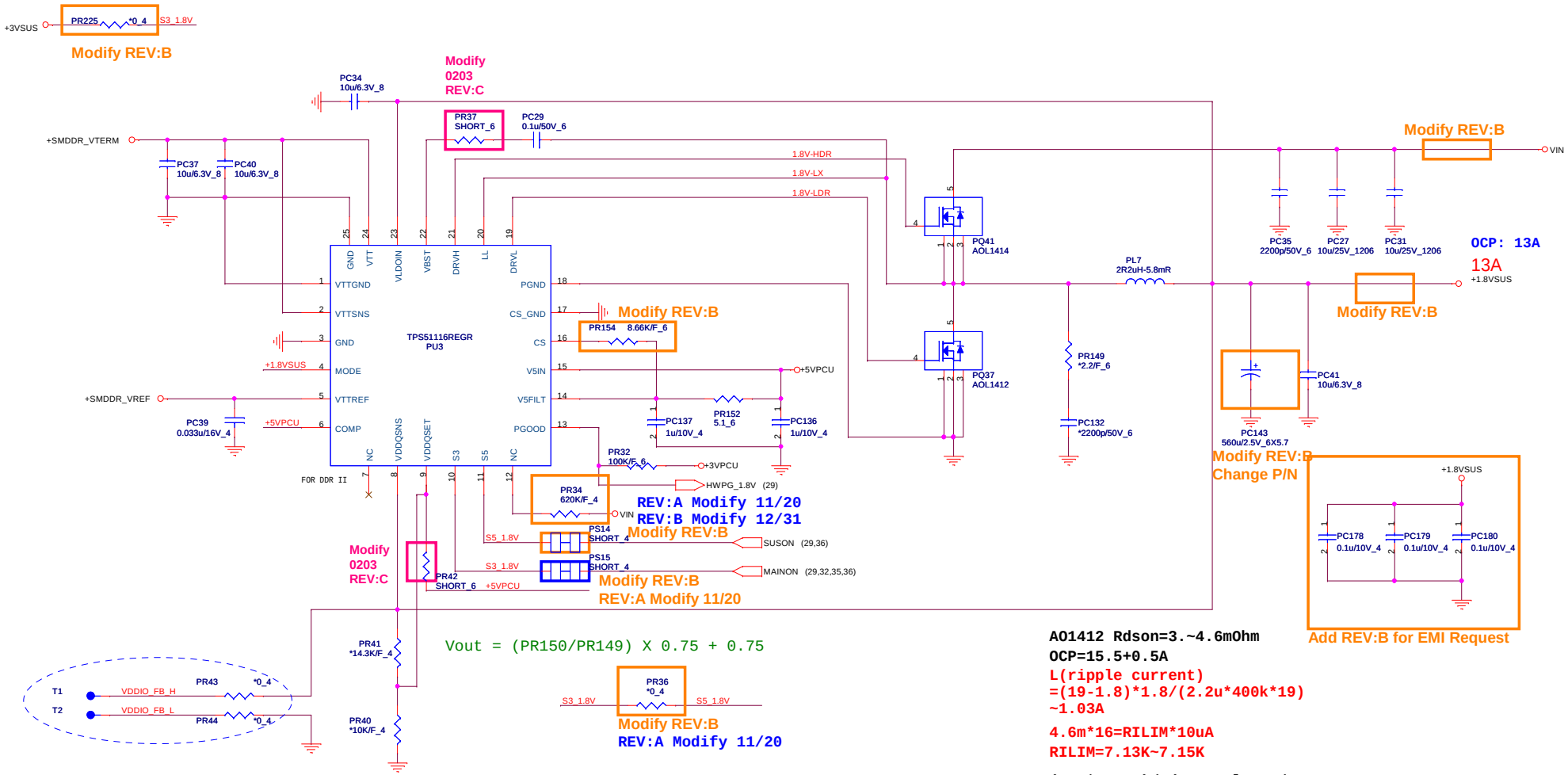

Quanta Computer Inc.		
PROJECT : Z06		
Size	Document Number: DDR 1.8V(TPS51116)	Rev 2A
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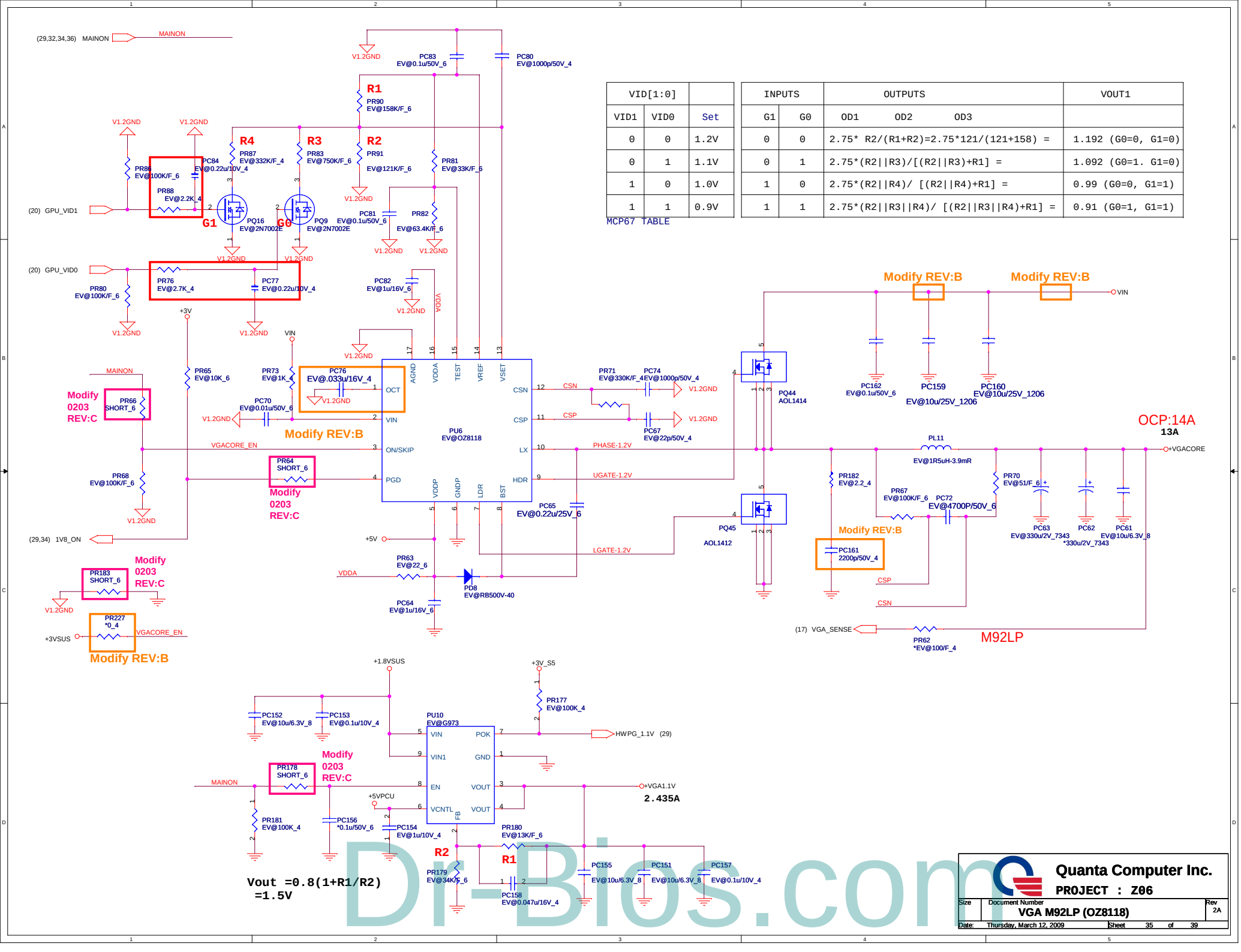

VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =	1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =	1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =	0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =	0.91 (G0=1, G1=1)

Quanta Computer Inc.
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Size	Document Number	Rev
	VGA M92LP (OZ8118)	2A
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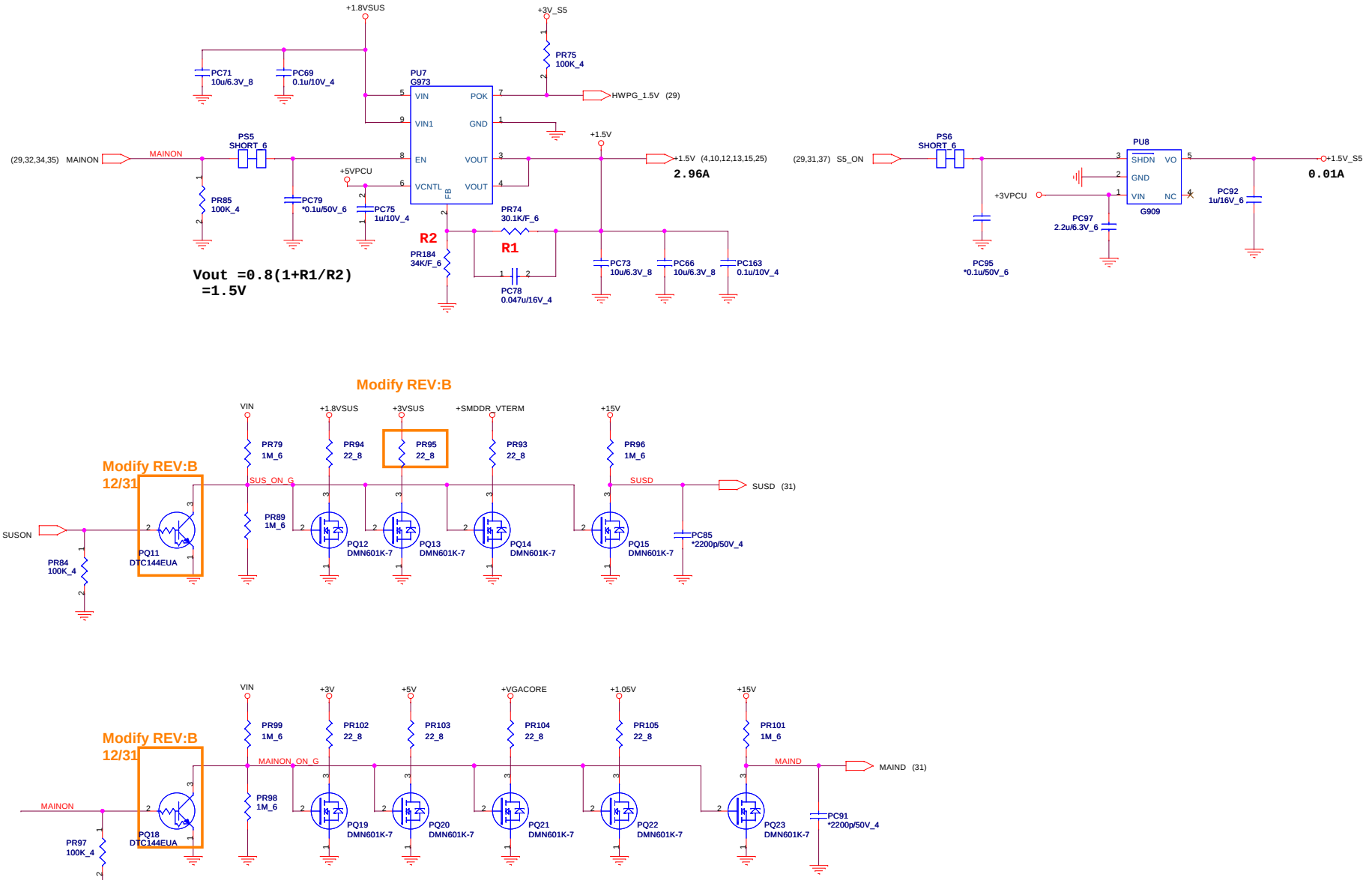

Quanta Computer Inc.		
PROJECT : Z06		
Size	Document Number: Discharge/1.5V	Rev: 2A
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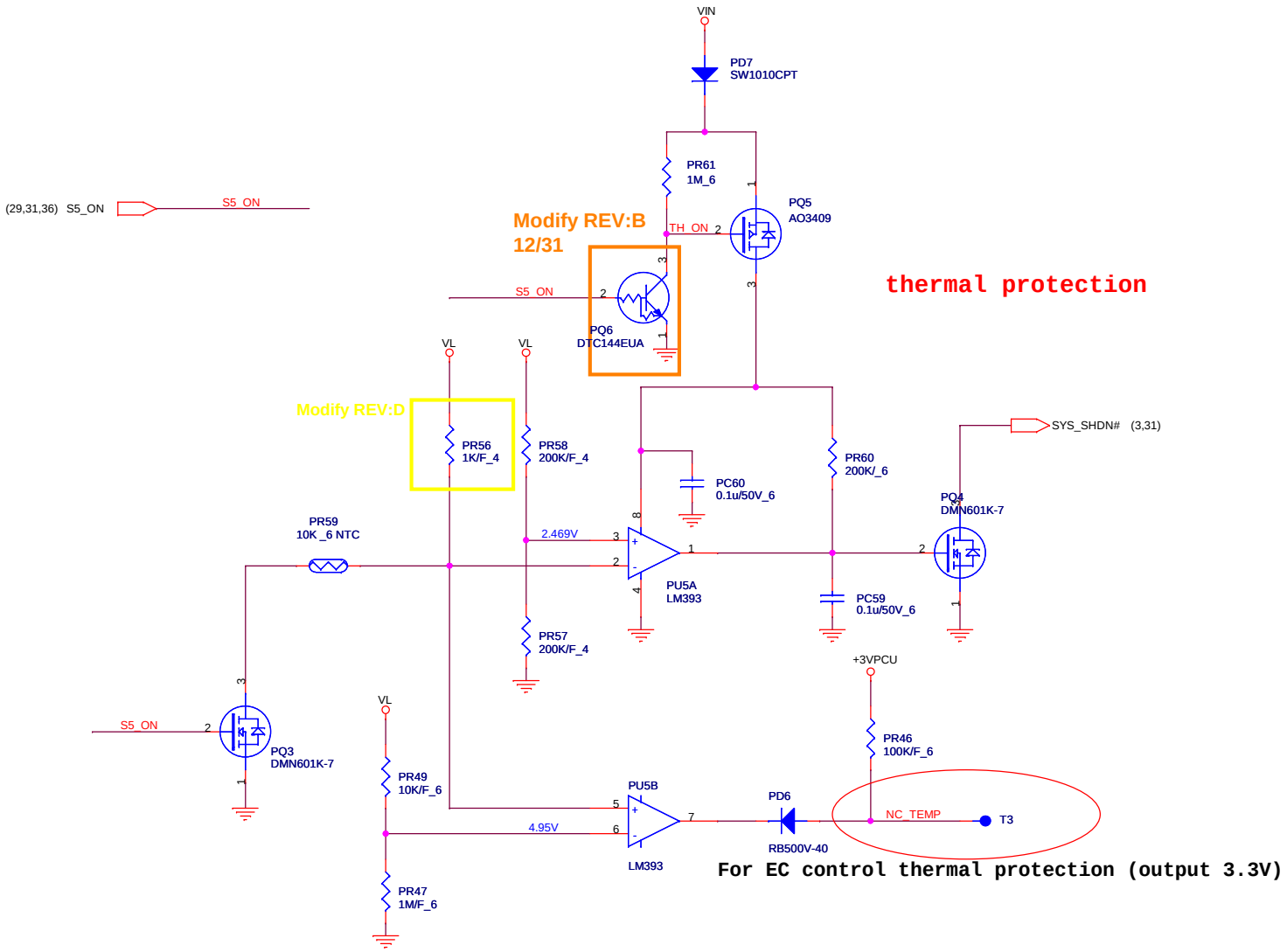

Quanta Computer Inc.

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	Thermal Protection	1A
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