# EL8 Block Diagram



VCC_CORE

GMCH_CORE

VCC1.1
VCC1.2
VCC1.5
1.5VSUS

VCC3
3V_STBY

VCC5
5V_STBY
+12V

Intel
Yorkfield/Wolfdale
Q9000/E8000
LGA775
Page 3,4

FSB(800/1067/1333HZ)

CLOCK GENERATOR
CK505
CV193
Page 2

800/1067 MHZ DDR III

CH A: DDRIII-UDIMM0/1
CH B: DDRIII-UDIMM0/1
Page 14,15,16,17

NB
Eaglelake
G45/P43
1254 pin
Page 5,7,8,9

PCI-E 2.0 16X

MXM CONNECTOR
Page 18

LVDS

LCD PANEL
23" Full HD

SDVO

LVDS Transmitter
CH7308B
Page 19

DMI

SATA - HDD(2.5)
Page 22
SATA 4

SATA - HDD(3.5)
Page 22
SATA 1

SATA - ODD
Page 22
SATA 2

eSATA
Page 22
SATA 3

WLAN
Page 25
USB-10

USB 2.0

Camera
Page 19
USB-1

BT KB/Mouse
Page 27

Bluetooth
Page 26
USB-2

USB*4(Rear)
Page 27
USB-6,7
8,9

Azalia

TV
Page 25
USB-11

USB*2(Side)
Page 26
USB-3,5

Touch Screen
Page 27
USB-0

SB
ICH10
676 pin
Page 10,11,12,13

PCI-Express 1X

PCIE-2
MINI CARD-1
WLAN
Page 25

PCIE-3
MINI CARD-2
TV card
Page 25

PCIE-1
LAN
RTL8111DL
Page 26

PCIE-4
Card Reader
JMB385
Page 27

WLAN antenna

TV antenna

RJ45

Media Slot

LPC

32.768KHz

ITE8512
Page 26

HP
Page 30

MIC IN
Page 30

INT SPK
Page 29

DMIC IN
Page 30

AUDIO CODEC
ALC888S-VC2
Page 29

LINE IN

5.1 Channel

IR
Blaster
Page 3

FAN
Page 26

FLASH
ROM
Page 28

CIR
Page 28

Daughter Board

MXM module
314 pin

B-CAS board
10 pin

Card Reader
20 pin

HP/MIC
Light SW
10 pin

Power button
LED
TBD



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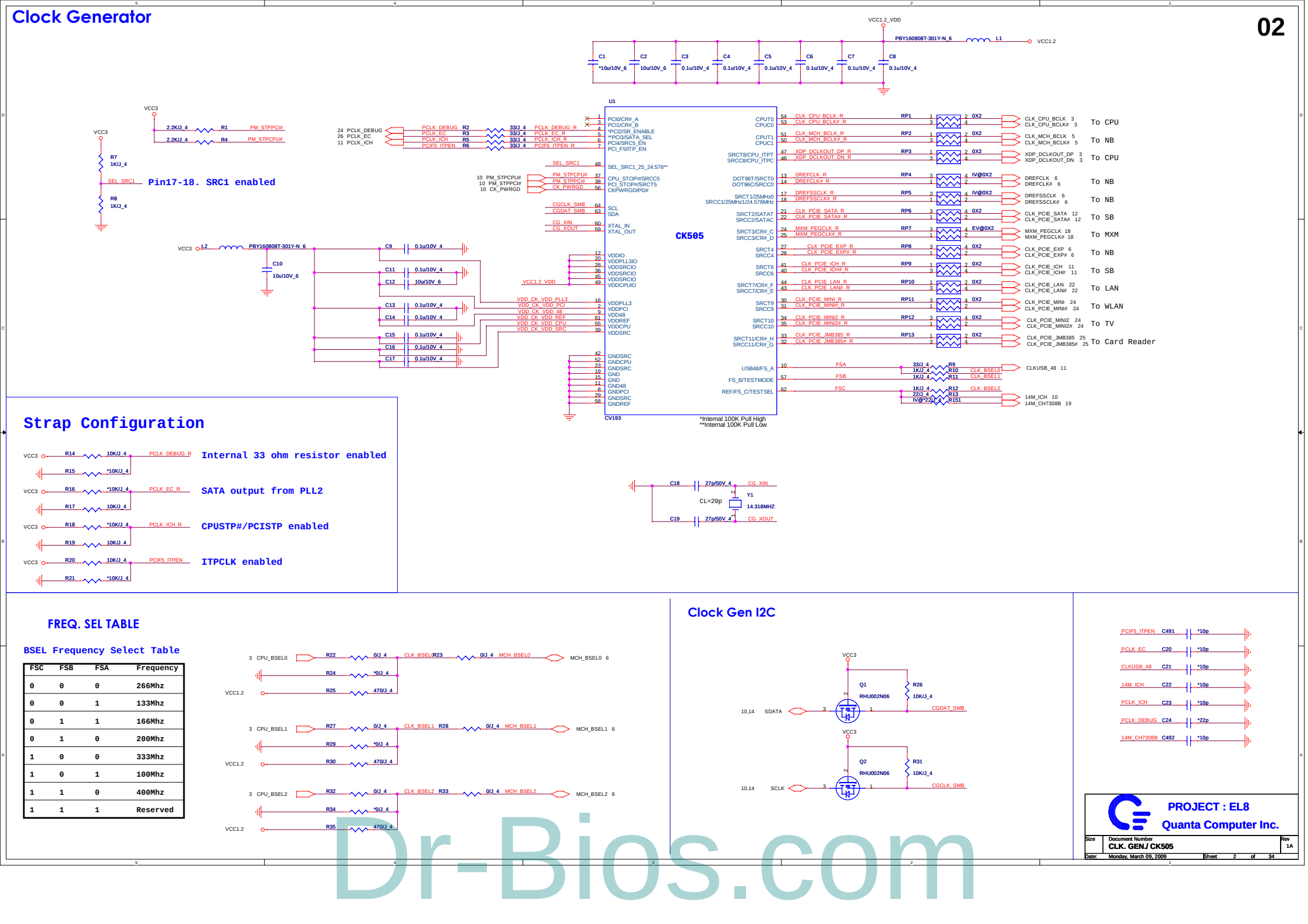
| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | 1A |
| Date: Monday, March 09, 2009 | Sheet 1 of 34 | |

# Clock Generator

02




## Strap Configuration




## FREQ. SEL TABLE

**BSEL Frequency Select Table**

| FSC | FSB | FSA | Frequency |
|---|---|---|---|
| 0 | 0 | 0 | 266Mhz |
| 0 | 0 | 1 | 133Mhz |
| 0 | 1 | 1 | 166Mhz |
| 0 | 1 | 0 | 200Mhz |
| 1 | 0 | 0 | 333Mhz |
| 1 | 0 | 1 | 100Mhz |
| 1 | 1 | 0 | 400Mhz |
| 1 | 1 | 1 | Reserved |




## Clock Gen I2C







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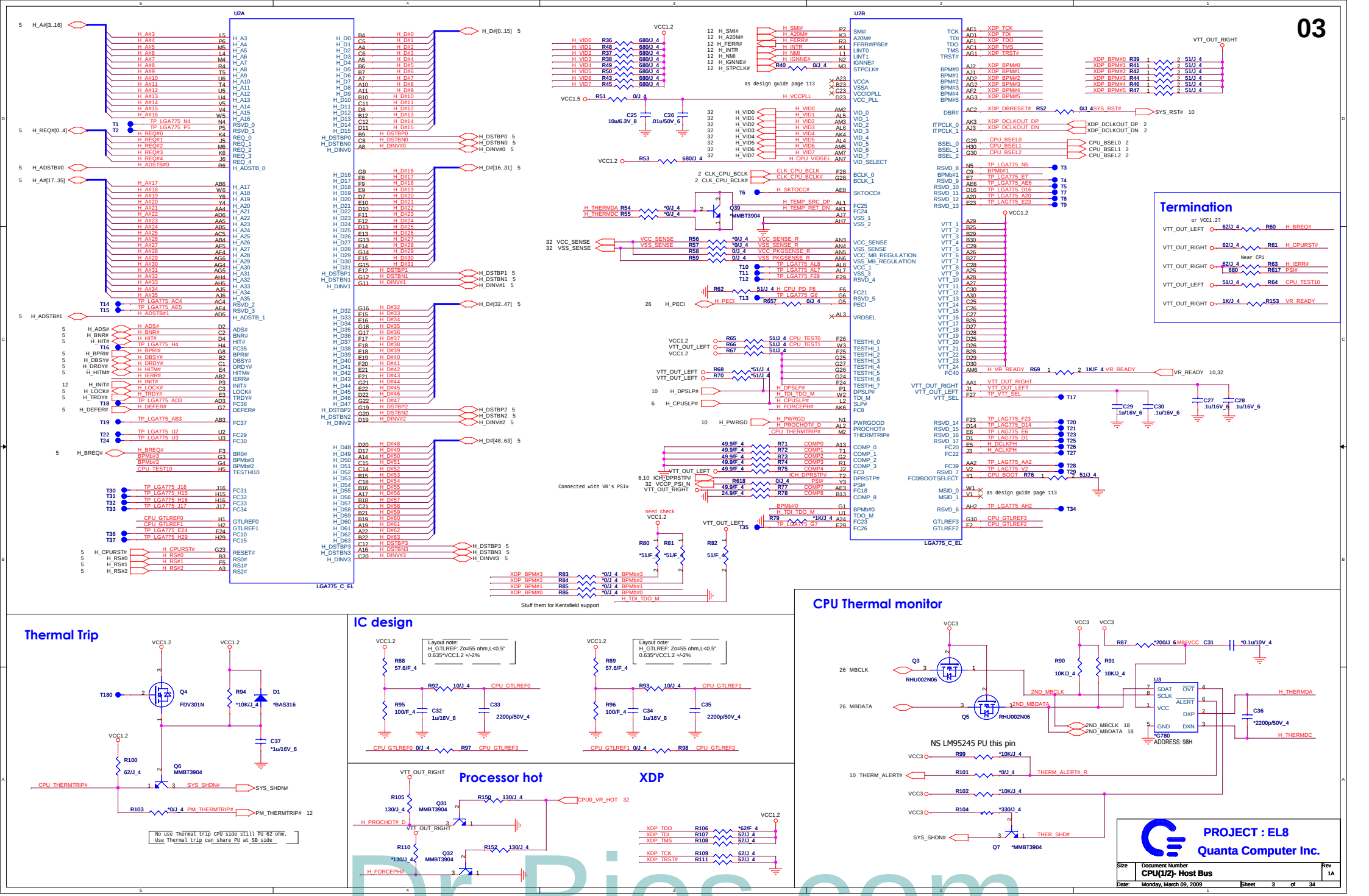
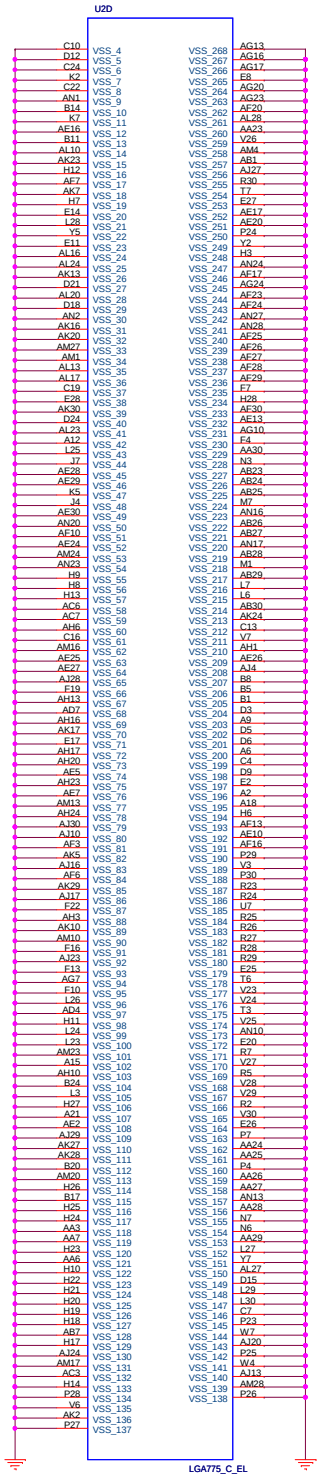
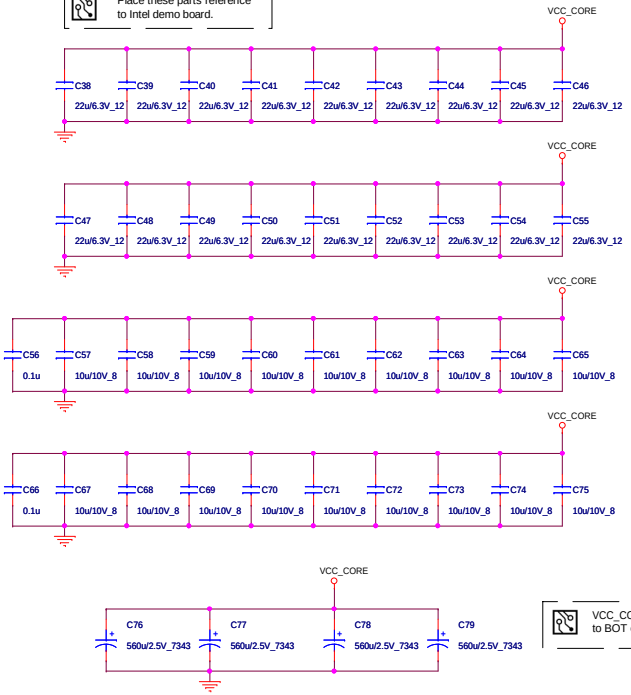
| Size | Document Number | Rev |
|---|---|---|
| | CLK. GEN./ CK505 | 1A |
| Date: Monday, March 09, 2009 | Sheet 2 of 34 | |

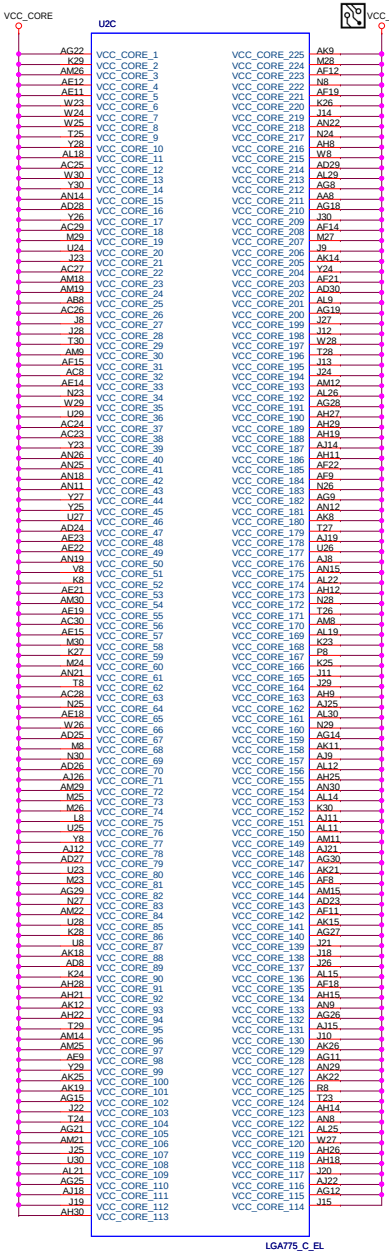

03
U2A
U2B
LGA775_C_EL
LGA775_C_EL
Termination
Thermal Trip
IC design
Processor hot
XDP
CPU Thermal monitor
NS LM95245 PU this pin
PROJECT : EL8
Quanta Computer Inc.
CPU(1/2)- Host Bus
Monday, March 09, 2009
Sheet 3 of 34
Stuff them for Kentsfield support
Connected with VR's PSI#
No use Thermal trip cPU side still PU 62 ohm.
Use Thermal trip can share PU at SB side




Place these parts reference to Intel demo board.




VCC_CORE Bulk CAPs place to BOT of CPU centeral




Yorkfield/Wolfdale CPU Power Status and max current table

| POWER PLANE | S0 | S3 | S4/S5 | Voltage | I(max) | Note |
|---|---|---|---|---|---|---|
| VCC_CORE | O | X | X | VID | 100A | Yorkfield@65W |
| VCC_CORE | O | X | X | VID | 75A | Wolfdale |
| VTT | O | X | X | VCC1.2 | 8A | After VCC stable |
| VTT | O | X | X | VCC1.2 | 7A | Before VCC stable |
| VCC_PLL | O | X | X | VCC1.5 | 260mA | |



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| Size | Document Number | Rev |
|---|---|---|
| | CPU(2/2)- Power | 1A |
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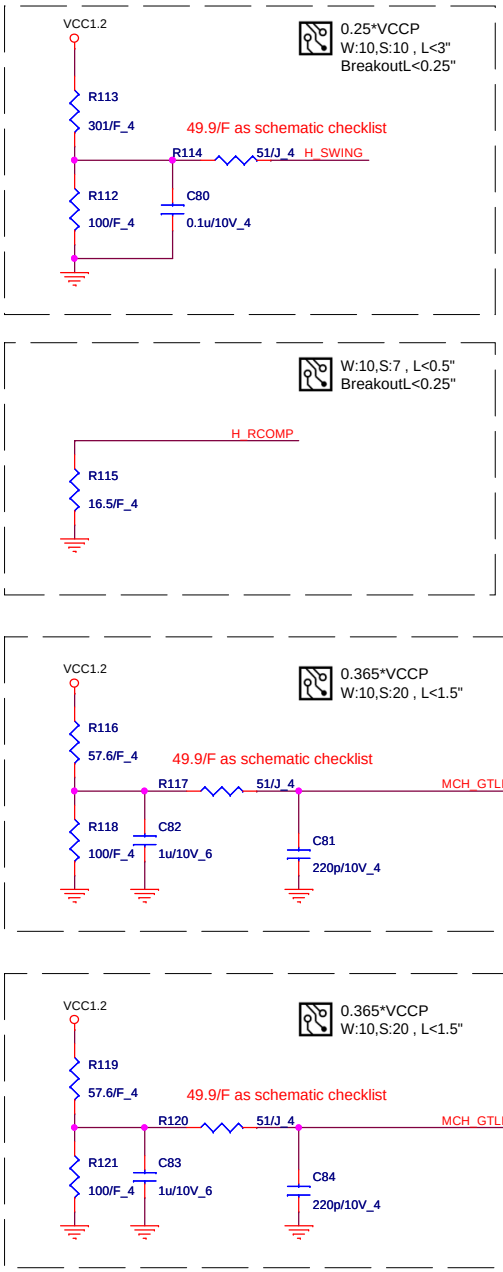


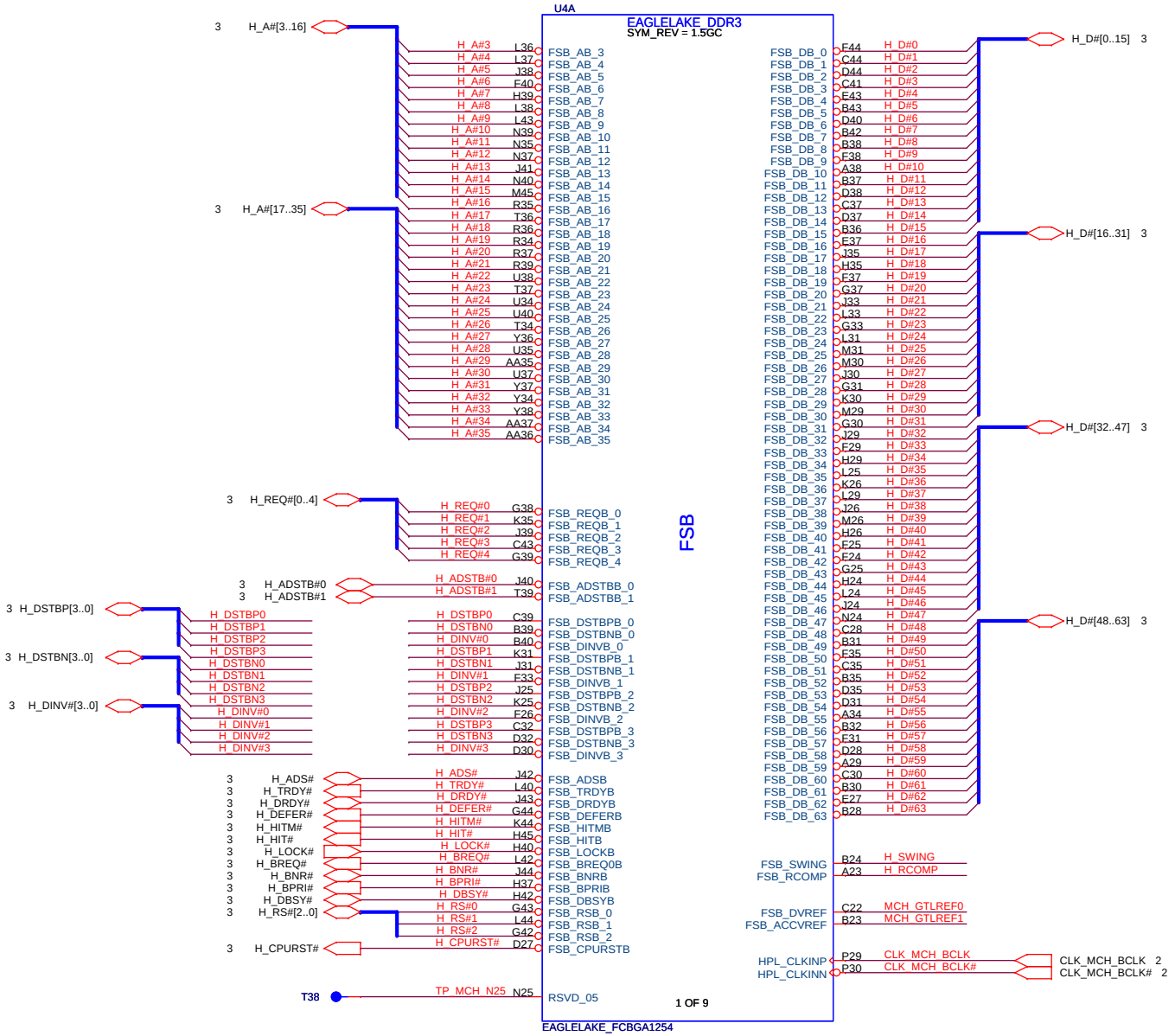




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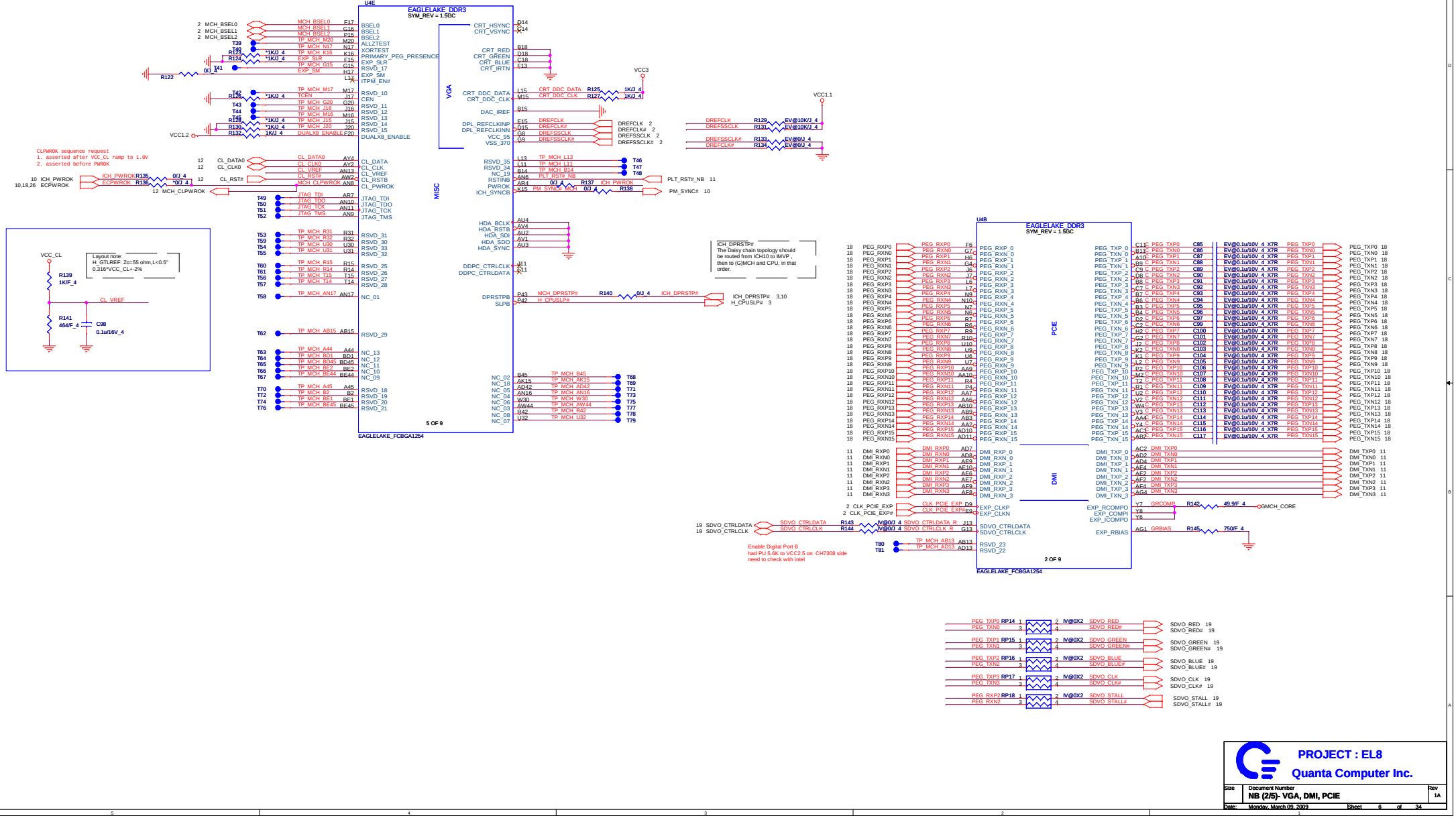
| Size | Document Number | Rev |
|---|---|---|
| | NB (1/5) HOST | 1A |
| Date: Monday, March 09, 2009 | Sheet 5 of 34 | |



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| Size | Document Number | Rev |
|---|---|---|
| | NB (2/5)- VGA, DMI, PCIE | 1A |
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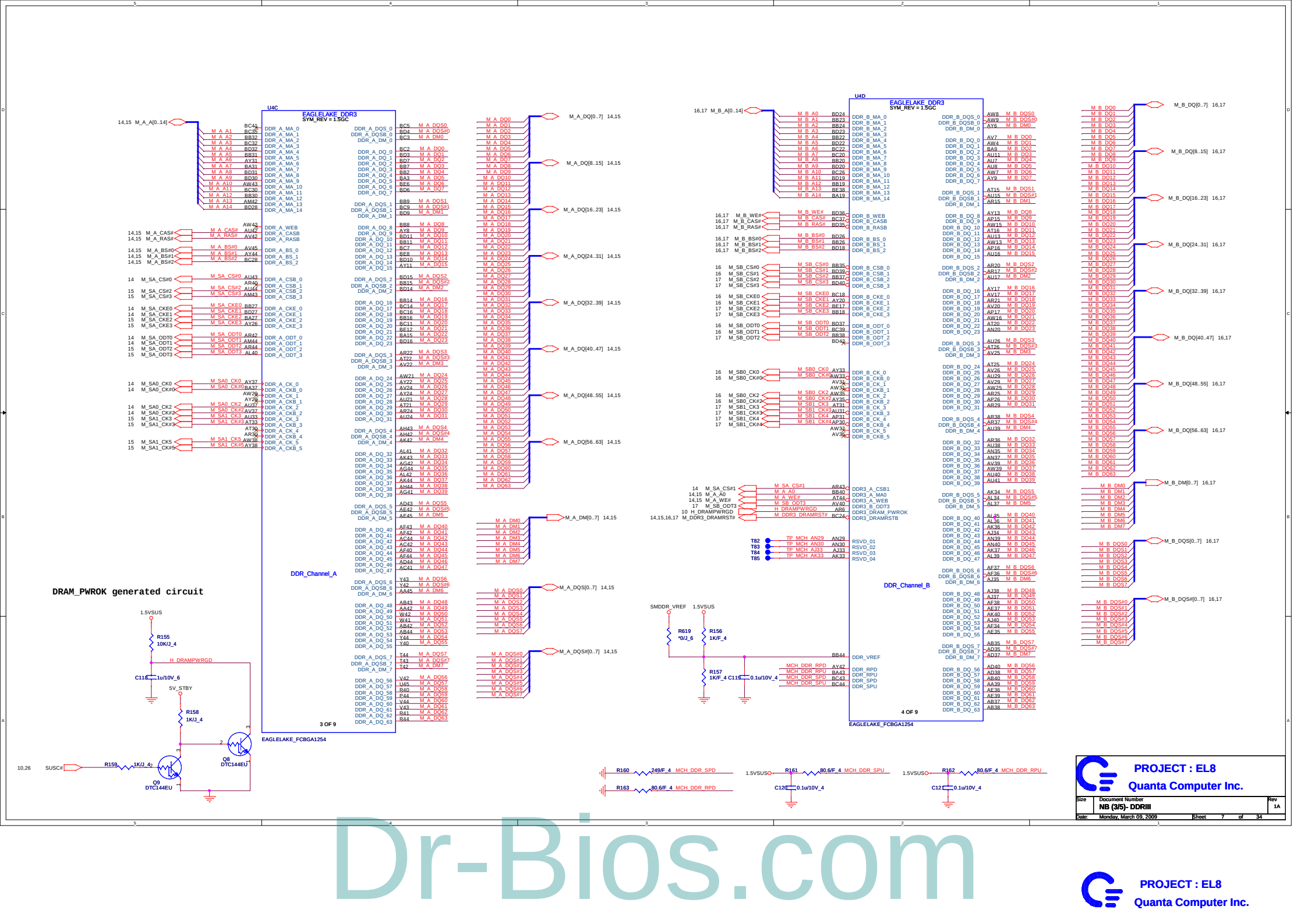




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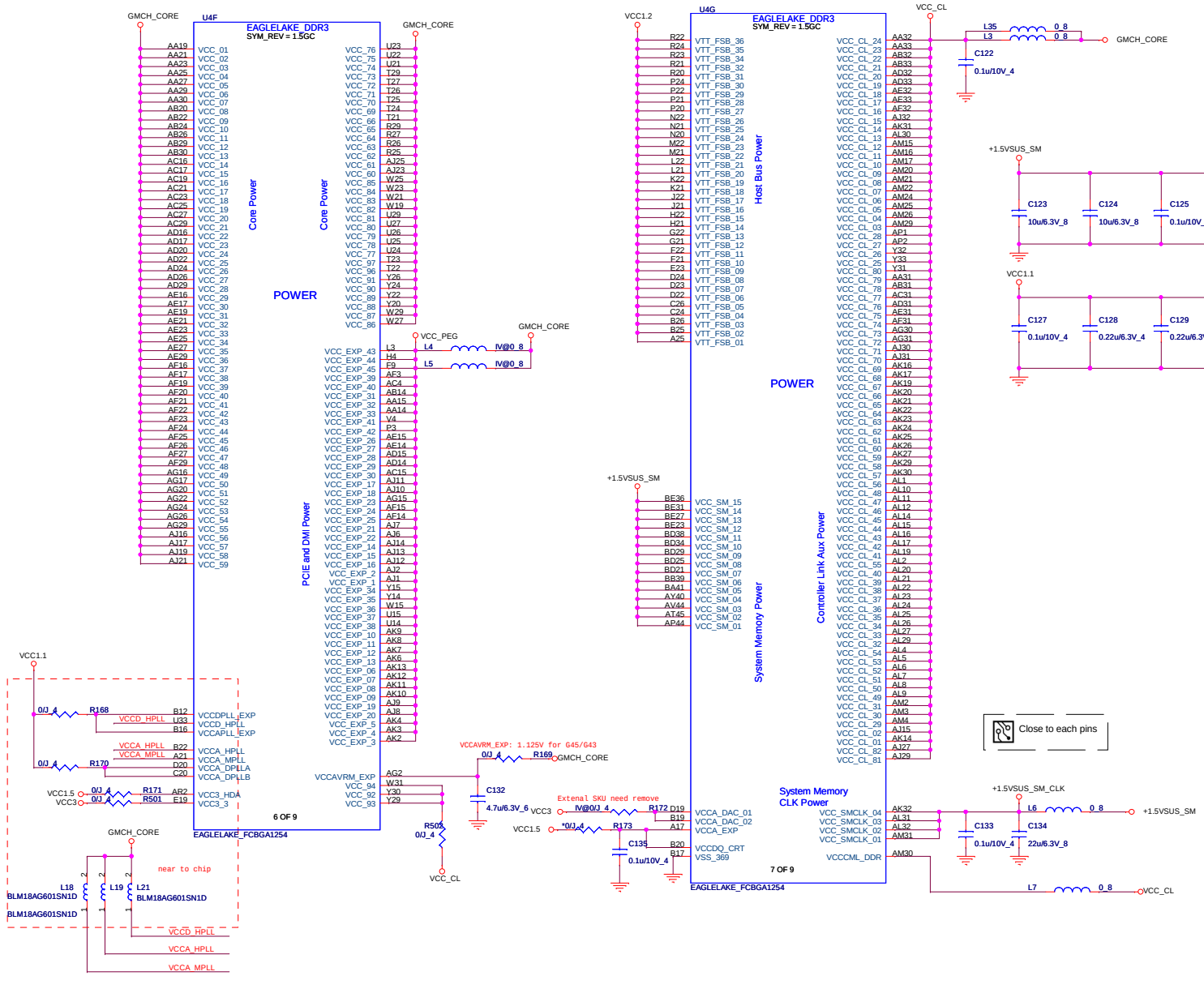


| SKU | G45 | P43 |
|---|---|---|
| GMCH_CORE | 1.125V | 1.1V |

## NB Power Status and max current table

| POWER PLANE | S0 | S3 | S4/S5 | Voltage | I(max) | Note |
|---|---|---|---|---|---|---|
| VCC_SM | O | O | X | 1.5VSUS | 1963mA | |
| VCC_SMCLK | O | O | X | 1.5VSUS | 288mA | |
| VCC_EXP | O | X | X | GMCH_CORE | 3082mA | SDVO, PCIE, DMI |
| VCCA_EXP | O | X | X | VCC1.5 | 6mA | SDVO, PCIE Analog |
| VTT_FSB | O | X | X | VCC1.2 | 914mA | |
| VCC | O | X | X | GMCH_CORE | 17984mA | |
| VCC_CL | O | X | X | GMCH_CORE | 4666mA | |
| VCC3_3 | O | X | X | VCC3 | 14mA | |
| VCCA_DAC | O | X | X | VCC3 | 74mA | |
| VCCDQ_CRT | O | X | X | VCC1.5 | 0mA | |
| VCCAPLL_EXP | O | X | X | VCC1.1 | 20mA | |
| VCCDPLL_EXP | O | X | X | VCC1.1 | X | |
| VCCA_DPLLA | O | X | X | VCC1.1 | 59mA | |
| VCCA_DPLLB | O | X | X | VCC1.1 | 59mA | |
| VCCA_HPLL | O | X | X | VCC1.1 | 31mA | |
| VCCD_HPLL | O | X | X | VCC1.1 | X | |
| VCCA_MPLL | O | X | X | VCC1.1 | 83mA | |



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| Size | Document Number | Rev |
|---|---|---|
| | NB (4/5)- Power | 1A |

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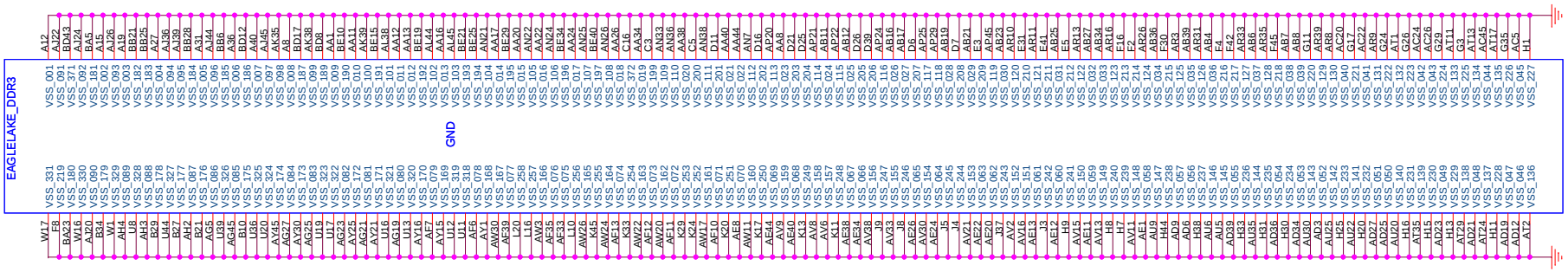


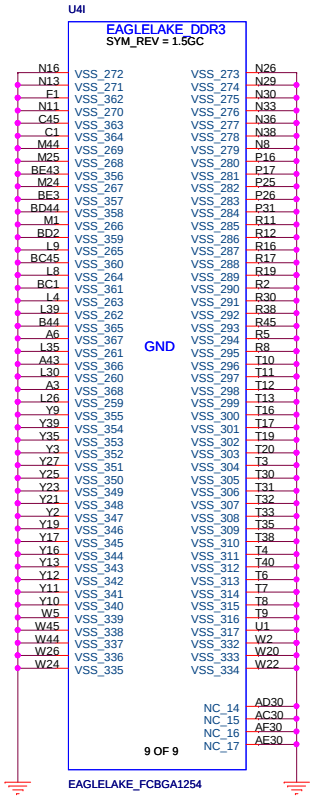




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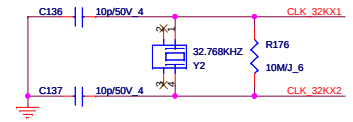
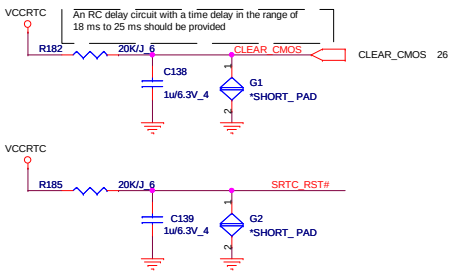
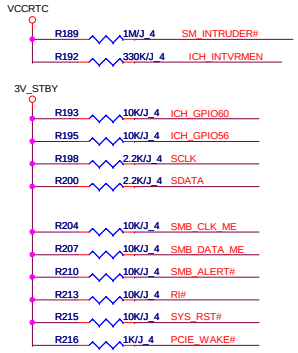
| Size | Document Number | Rev |
|---|---|---|
| | NB (5/5)- VSS | 1A |
| Date: Monday, March 09, 2009 | Sheet 9 of 34 | |

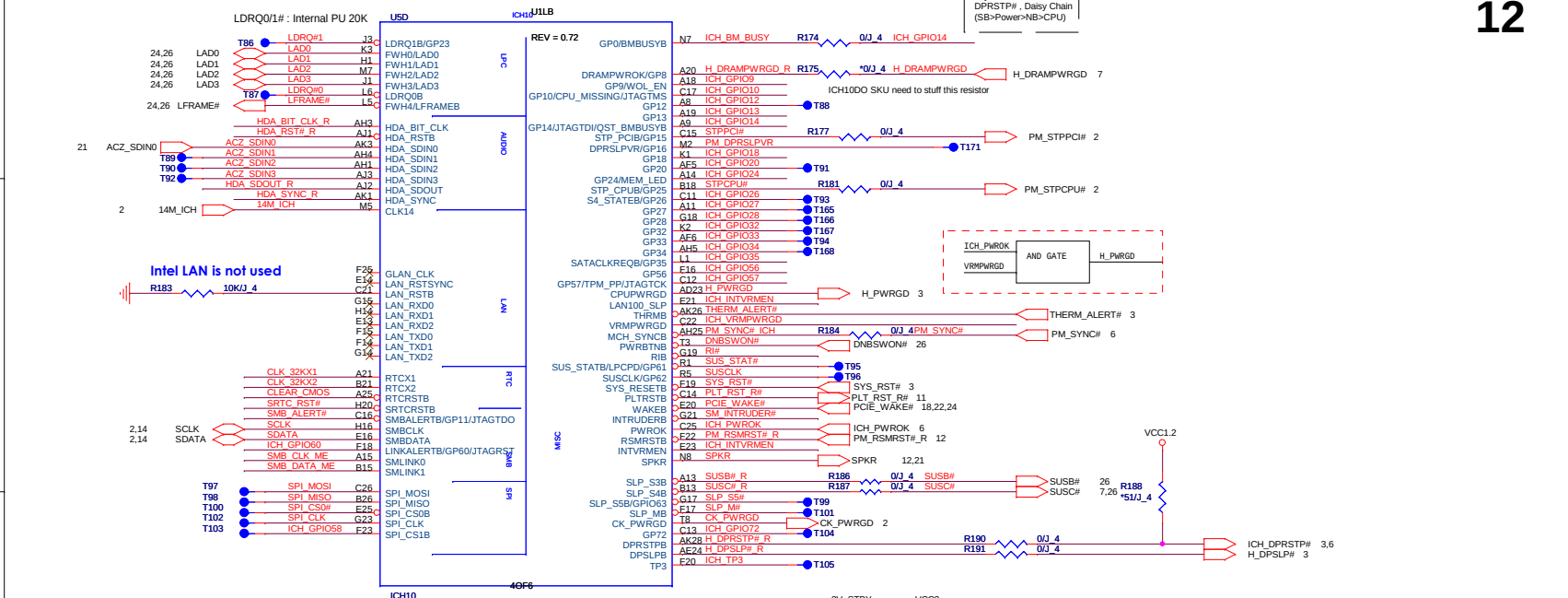
## RTC CRYSTAL



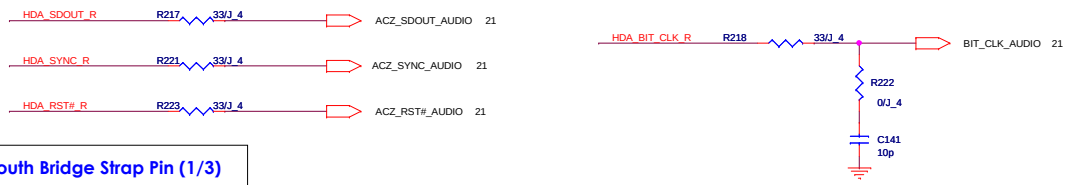

## RESET JUMP



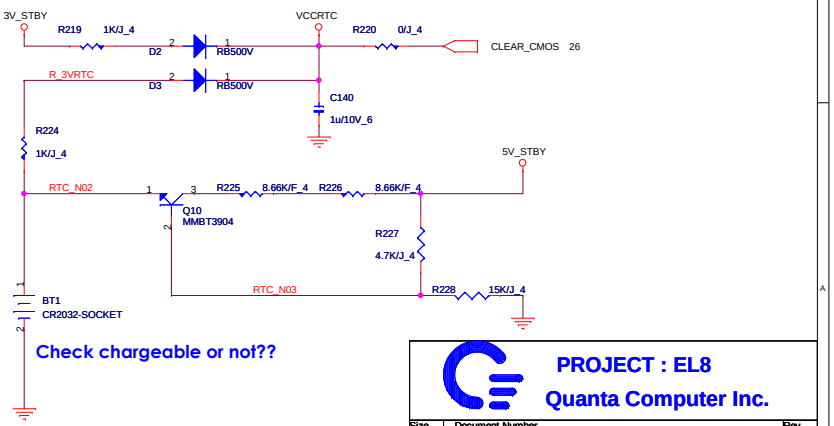




## HD Audio I/F(CODEC& iHDMI)




## RTC BATTERY




## South Bridge Strap Pin (1/3)

| Pin Name | Strap description | Sampled | Configuration | PU/PD |
|---|---|---|---|---|
| HDA_DOCK_EN/ GPIO33 | Flash Descriptor Security Override Strap | PWROK | 0 = The Flash Descriptor Security will be overridden.<br>1 = The security measures defined in the Flash Descriptor will be in effect | This strap should only be enabled in manufacturing environments using an external pull-up resistor. |
| SATALED# | PCI Express Lane Reversal (Lanes 1-4) | PWROK | Internal PU | |
| TP3 | XOR Chain Entrance | PWROK | ICH_TP3 R230 *1K/J_4 | |
| HDA_SDOUT | XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4) | PWROK | HDA_SDOUT R231 *3.3K/J_4 +3V_HDA_IO_ICH | |

| ICH_TP3 | HDA_SDOUT | Description |
|---|---|---|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal opration(Default) |
| 1 | 1 | Set PCIE port config bit 1 |

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| Size | Document Number | Rev |
|---|---|---|
| | SB (1/4)- HOST | 1A |
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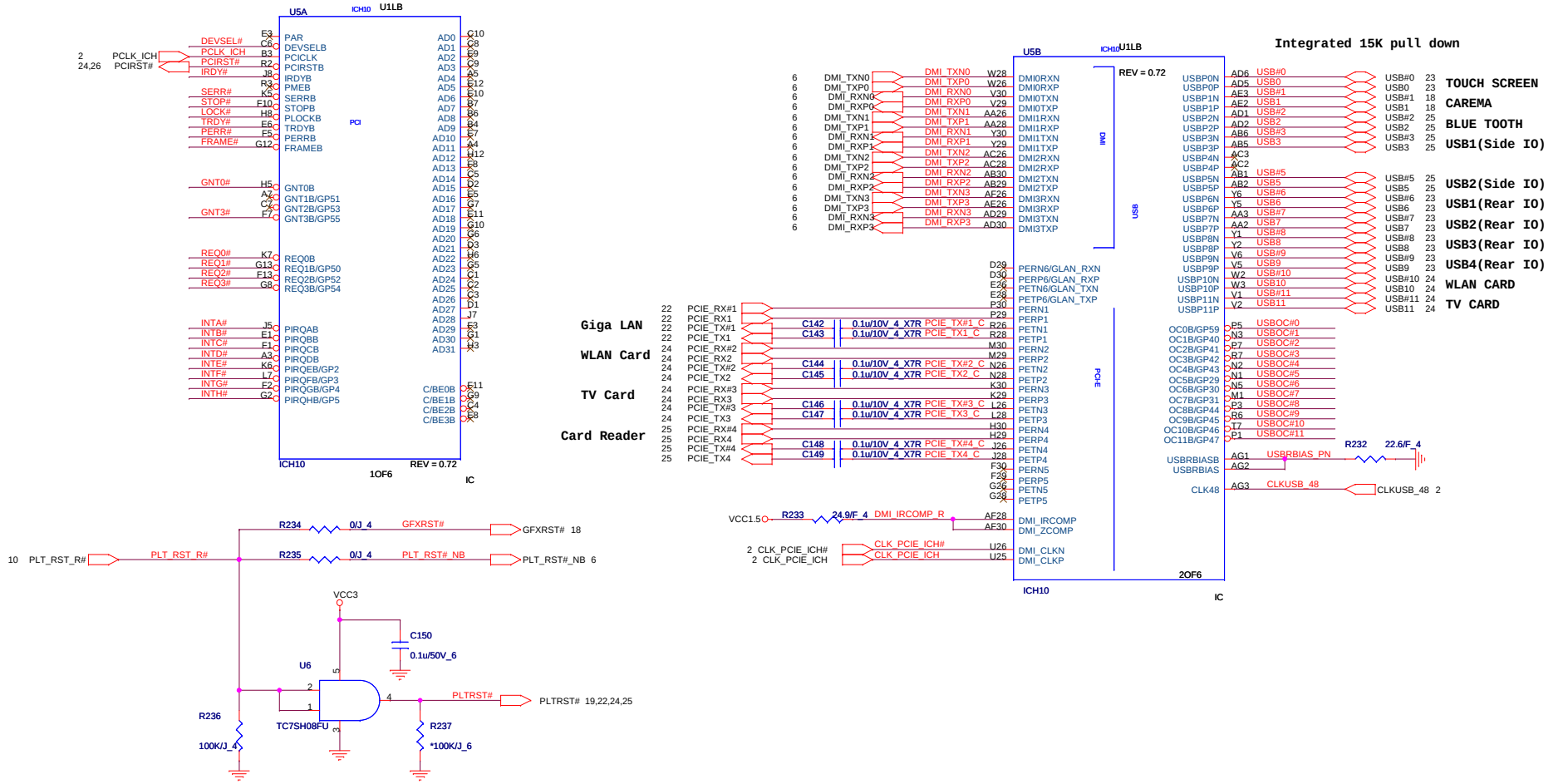
# PCI/PCI-E/USB/DMI/SPI

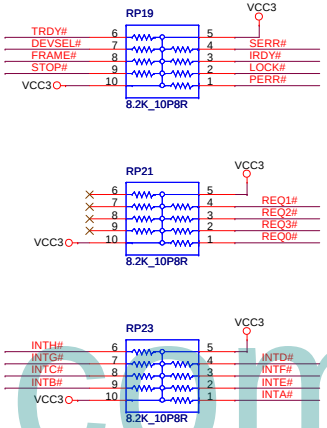




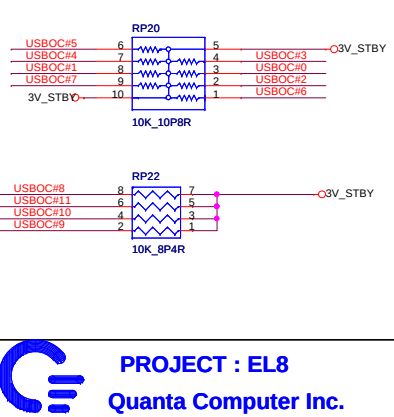

## South Bridge Strap Pin (2/3)

| Pin Name | Strap description | Sampled | Configuration | PU/PD |
|---|---|---|---|---|
| HDA_SYNC | PCI Express Port<br>Config 1 bit 0 (Port 1-4) | PWROK | 0 = Default<br>1 = Setting bit 0 | |
| GNT2# / GPIO53 | PCI Express Port<br>Config 2 bit 2 (Port 5-6) | PWROK | 0 = Setting bit 2<br>1 = Default | |
| GNT1# / GPIO51 | ESI Strap(Server Only) | PWROK | 0 = DMI for ESI-compatible<br>1 = Default | |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default | GNT3# R238 *1K/J_4 |
| | | | | |
| GNT0# | Boot BIOS Selection 0 | PWROK | PCI_GNT#0 / SPI_CS#1 / Boot Location<br>0 / 1 / SPI(Default)<br>1 / 0 / PCI<br>1 / 1 / LPC | GNT0# R239 *1K/J_4 |
| SPI_CS1# / GPIO58 / CLGPIO6 | Boot BIOS Selection 1 | CLPWROK | | |

## PCI PULL-UP




## USBOC# PULL-UP



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| Size | Document Number | Rev |
|---|---|---|
| | SB (2/4) PCIE/PCI/USB/DMI | 1A |

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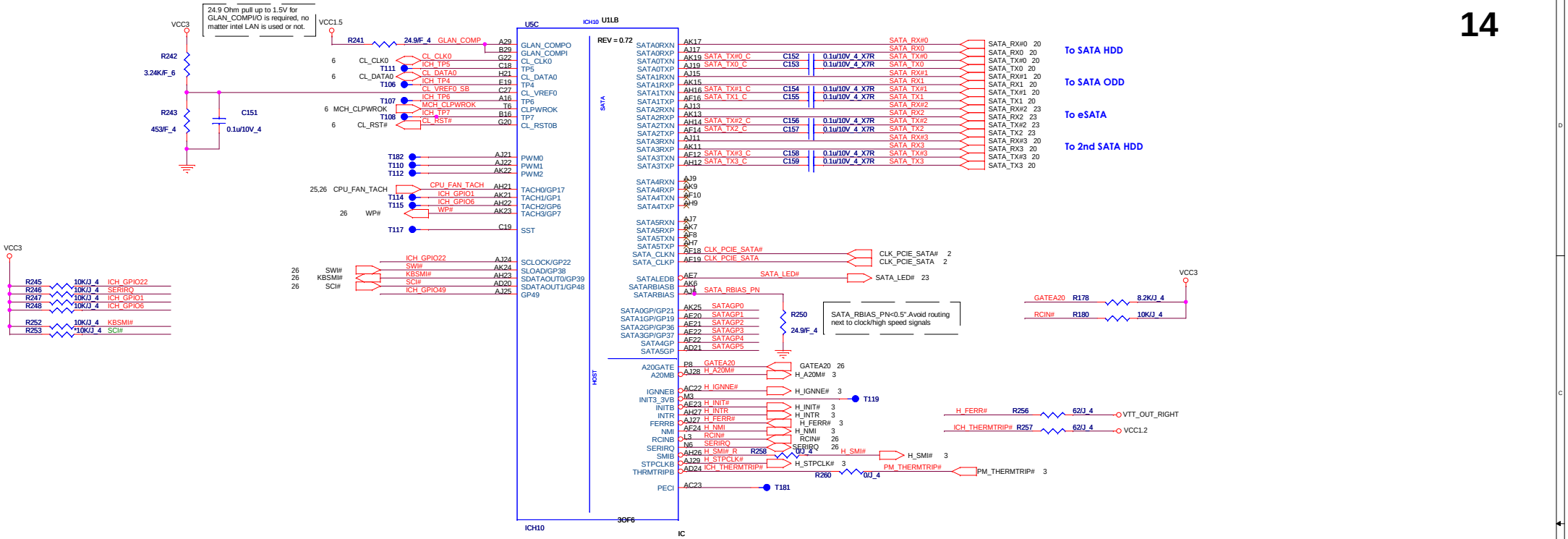


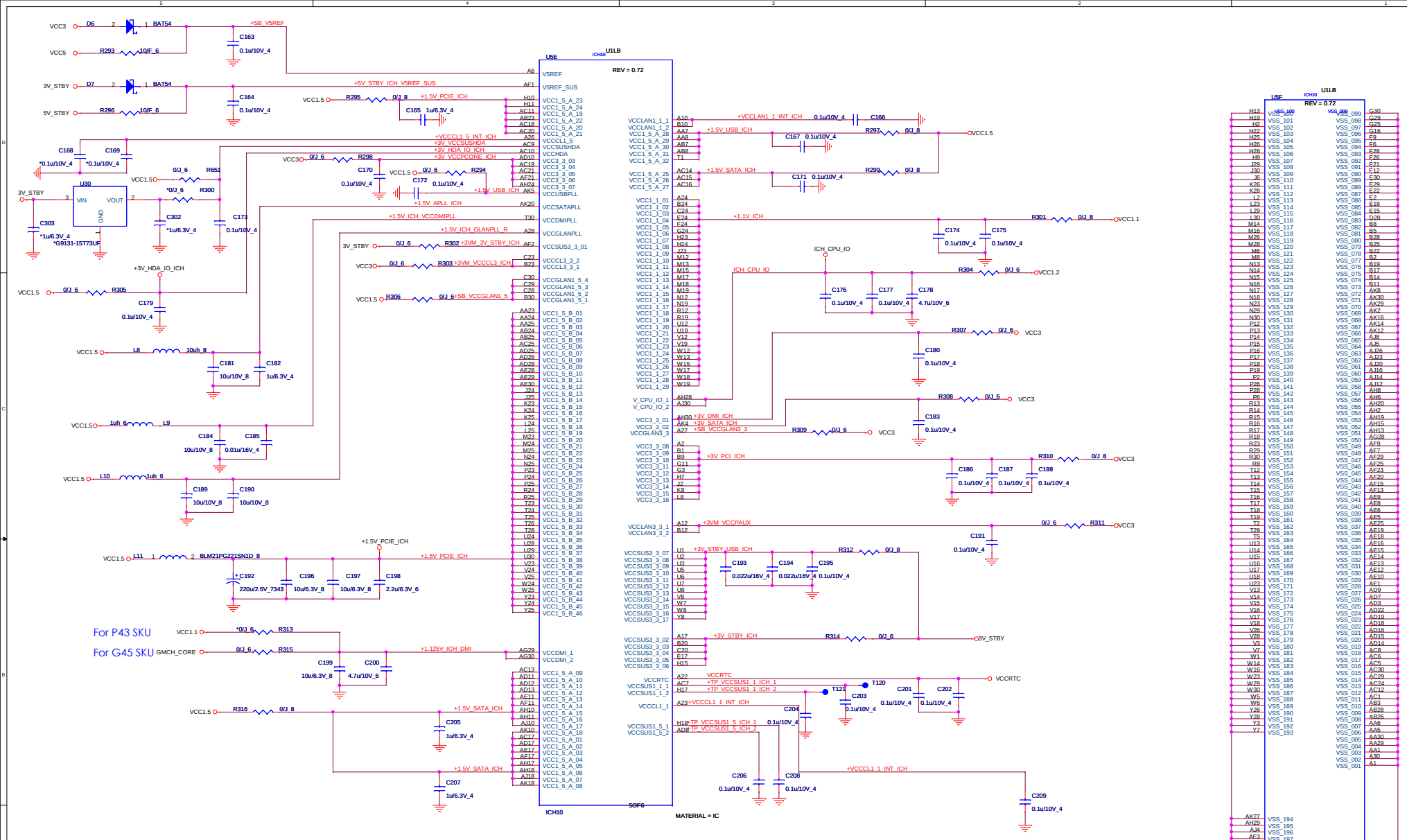

## South Bridge Strap Pin (3/3)

| Pin Name | Strap description | Sampled | Configuration | PU/PD |
|---|---|---|---|---|
| GPIO20 | Reserved | PWROK | | |
| SPKR | No Reboot | PWROK | 0 = Default<br>1 = No Reboot mode 10,21 | SPKR R286 *1K/J_4 VCC3 |
| GPIO49 | DMI Termination Voltage | PWROK | 0 = AC coupled<br>1 = DC coupled<br>Internal PU | ICH_GPIO49 R292 *1K/J_4 |

## Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

| Board ID | ID4 | ID3 | ID2 | ID1 | ID0 |
|---|---|---|---|---|---|
| NEW CARD CARD BUS | | | | | H<br>L |
| CCFL Panel LED Panel | | | | H<br>L | |
| W/ G-SENSOR W/O G-SENSOR | | | H<br>L | | |
| W/ TV W/O TV | | H<br>L | | | |
| W/ HDMI W/O HDMI | H<br>L | | | | |




## SB Power Status and max current table(1/2)

| POWER PLANE | S0 | S3 | S4/S5 | Voltage | I(max) | Note |
|---|---|---|---|---|---|---|
| VCCRTC | X | X | X | VCCRTC | 6uA | 6uA@G3 |
| V5REF | O | X | X | VCC5 | 2mA | |
| V5REF_SUS | O | O | O | 5V_STBY | 2mA | 2mA@S0,1mA@S3/S5 |
| VCC1_5_B | O | X | X | VCC1.5 | 646mA | |
| VCCSATAPLL | O | X | X | VCC1.5 | 47mA | |
| VCC1_5_A | O | X | X | VCC1.5 | 1644mA | |
| VCCUSBPLL | O | X | X | VCC1.5 | 11mA | |
| VCCLAN1_1 | X | X | X | 1.1V | X | Internal VR powered, S3/S5 powered when AMT actived |
| VCCLAN3_3 | O | X | X | VCC3 | 78mA | 78mA@S3/S5 powered when AMT actived |
| VCCGLANPLL | O | X | X | VCC1.5 | 23mA | |
| VCCGLAN1_5 | O | X | X | VCC1.5 | 80mA | |
| VCCGLAN3_3 | O | X | X | VCC3 | 1mA | |

## SB Power Status and max current table(2/2)

| POWER PLANE | S0 | S3 | S4/S5 | Voltage | I(max) | Note |
|---|---|---|---|---|---|---|
| VCC1_1 | O | X | X | VCC1.1 | 1.634A | ICH CORE |
| VCCDMIPLL | O | X | X | VCC1.5 | 23mA | |
| VCC_DMI | O | X | X | GMCH_CORE | 50mA | 1.125V@G45, 1.1V@P43 |
| V_CPU_IO | O | X | X | VCC1.2 | 2mA | |
| VCC3_3 | O | X | X | VCC3 | 308mA | |
| VCCHDA | O | X | X | VCC1.5 | 70mA | |
| VCCSUSHDA | O | O | O | RVCC1.5 | 70mA | |
| VCCSUS1_1 | X | X | X | 1.1V | X | Internal VR powered |
| VCCSUS1_5 | X | X | X | 1.5V | X | Internal VR powered |
| VCCSUS3_3 | O | O | O | 3V_STBY | 212mA | 53mA@S3/S5 |
| VCCCL1_1 | X | X | X | 1.1V | X | Internal VR powered |
| VCCCL1_5 | X | X | X | 1.5V | X | Internal VR powered |
| VCCCL3_3 | O | X | X | VCC3 | 73mA | S3/S5 powered when AMT actived |



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| Size | Document Number | Rev |
|---|---|---|
| | SB(4/4) POWER/VSS | 1A |

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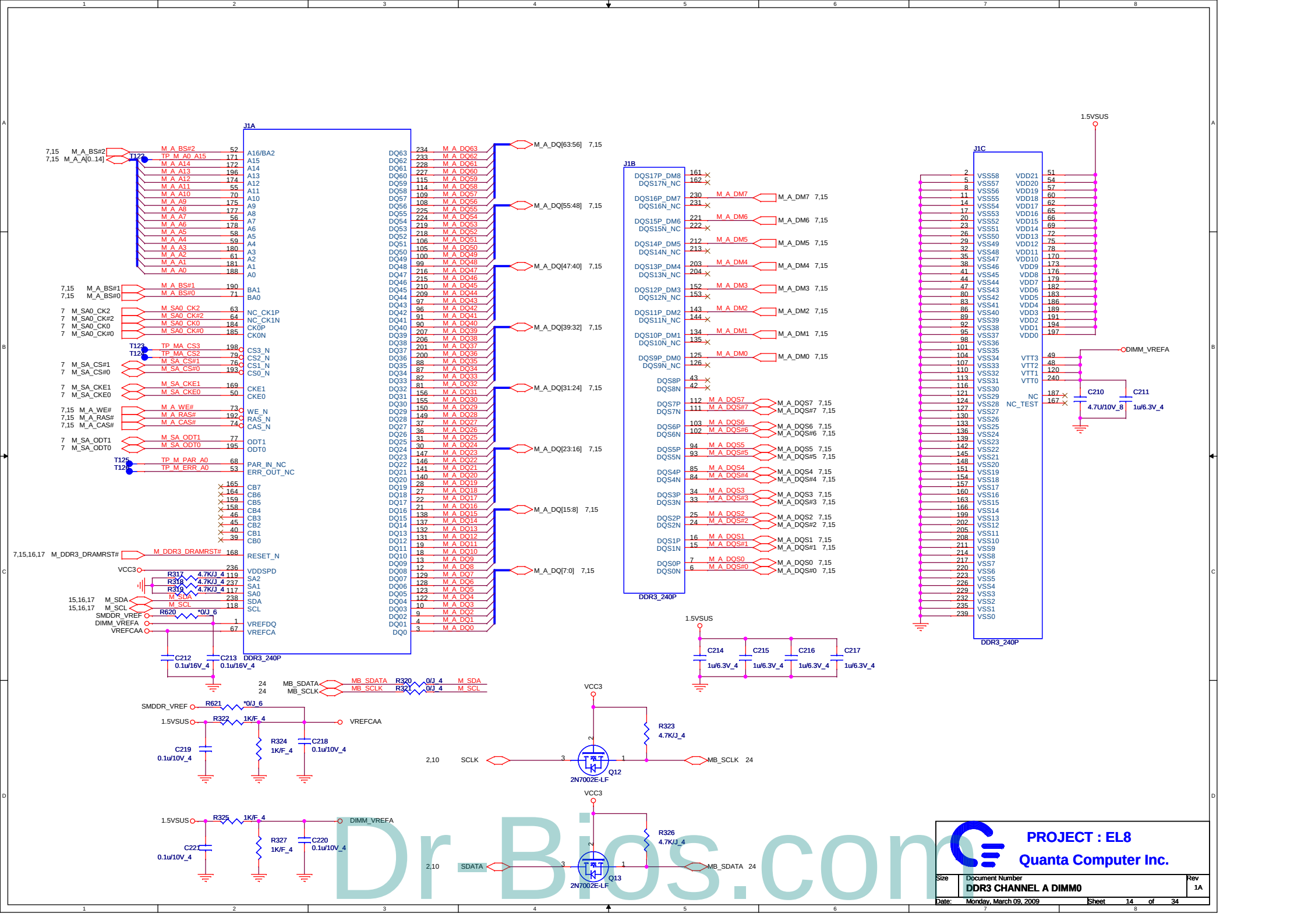
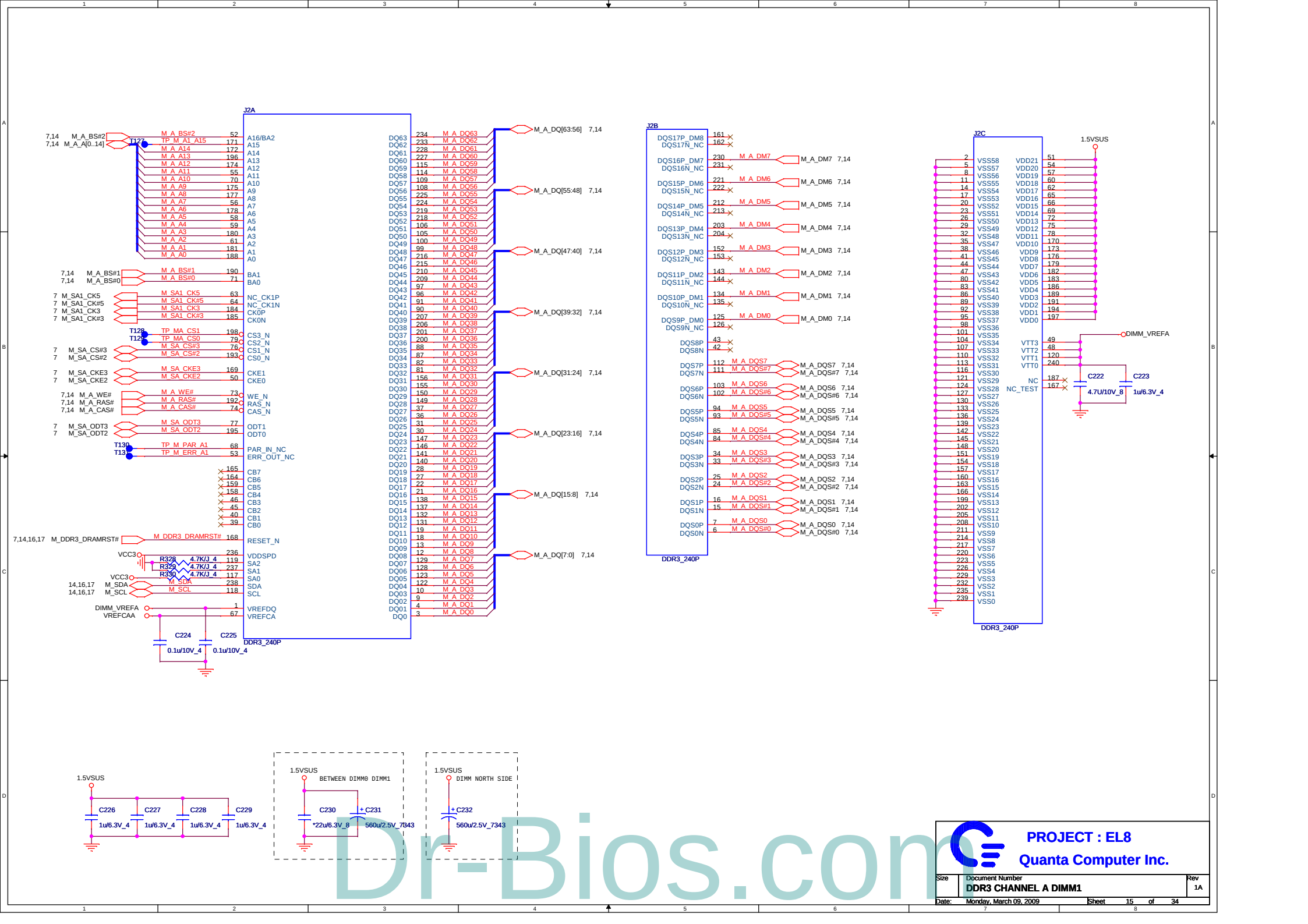

J1A
J1B
J1C
DDR3_240P
M_A_BS#2
TP_M_A0_A15
M_A_A14
M_A_A13
M_A_A12
M_A_A11
M_A_A10
M_A_A9
M_A_A8
M_A_A7
M_A_A6
M_A_A5
M_A_A4
M_A_A3
M_A_A2
M_A_A1
M_A_A0
M_A_BS#1
M_A_BS#0
M_SA0_CK2
M_SA0_CK#2
M_SA0_CK0
M_SA0_CK#0
TP_MA_CS3
TP_MA_CS2
M_SA_CS#1
M_SA_CS#0
M_SA_CKE1
M_SA_CKE0
M_A_WE#
M_A_RAS#
M_A_CAS#
M_SA_ODT1
M_SA_ODT0
TP_M_PAR_A0
TP_M_ERR_A0
M_DDR3_DRAMRST#
M_SDA
M_SCL
M_A_DQ[63:56]
M_A_DQ[55:48]
M_A_DQ[47:40]
M_A_DQ[39:32]
M_A_DQ[31:24]
M_A_DQ[23:16]
M_A_DQ[15:8]
M_A_DQ[7:0]
M_A_DM7
M_A_DM6
M_A_DM5
M_A_DM4
M_A_DM3
M_A_DM2
M_A_DM1
M_A_DM0
M_A_DQS7
M_A_DQS#7
M_A_DQS6
M_A_DQS#6
M_A_DQS5
M_A_DQS#5
M_A_DQS4
M_A_DQS#4
M_A_DQS3
M_A_DQS#3
M_A_DQS2
M_A_DQS#2
M_A_DQS1
M_A_DQS#1
M_A_DQS0
M_A_DQS#0
1.5VSUS
DIMM_VREFA
C210
C211
4.7U/10V_8
1u/6.3V_4
C212
C213
0.1u/16V_4
C214
C215
C216
C217
R317
R318
R319
4.7K/J_4
R620
*0/J_6
MB_SDATA
MB_SCLK
R320
R321
0/J_4
R621
R322
1K/F_4
R324
C218
C219
0.1u/10V_4
VREFCAA
SMDDR_VREF
R323
Q12
2N7002E-LF
SCLK
SDATA
R325
R327
C220
C221
R326
Q13
PROJECT : EL8
Quanta Computer Inc.
DDR3 CHANNEL A DIMM0
Monday, March 09, 2009
Sheet 14 of 34

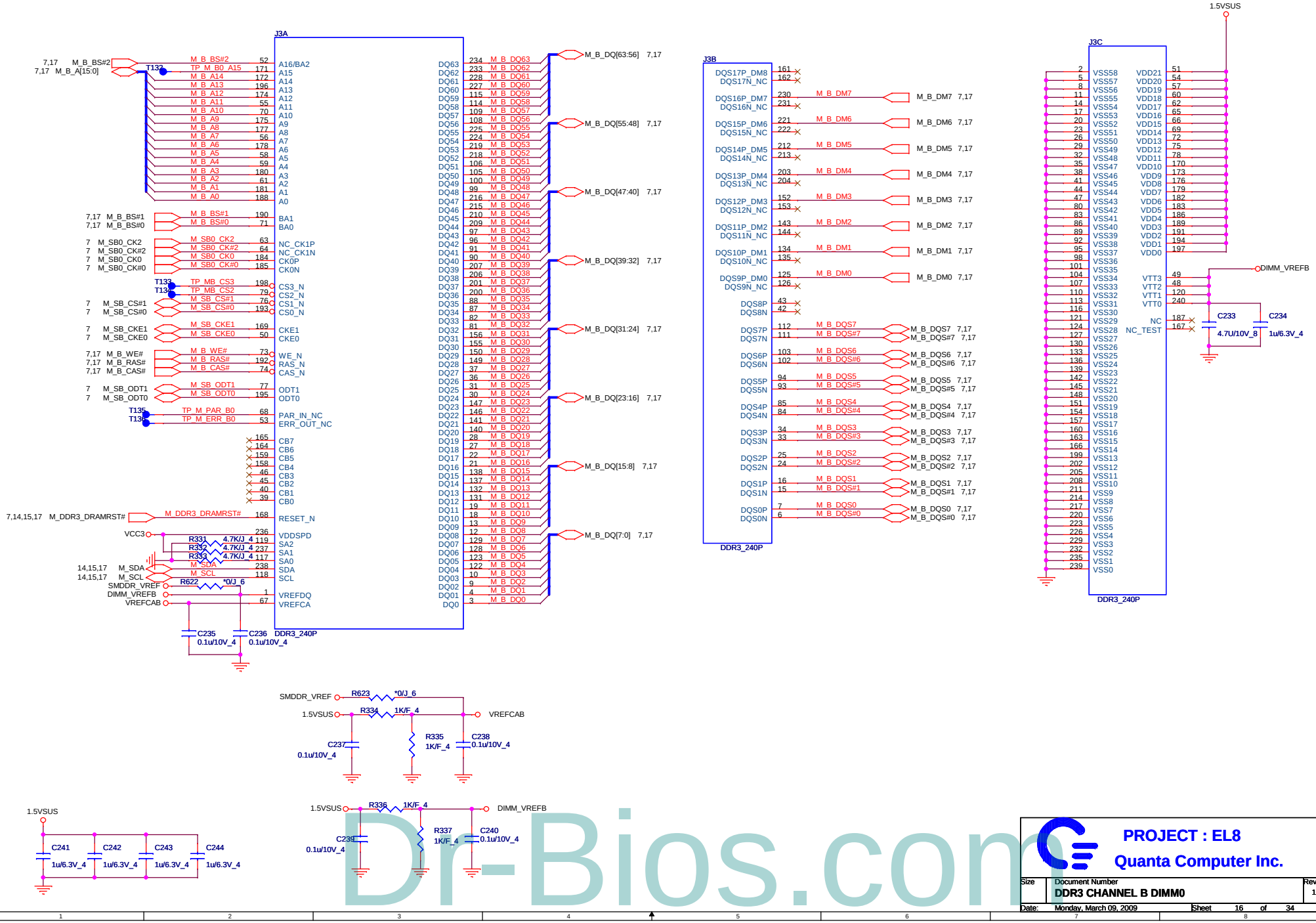





PROJECT : EL8

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 CHANNEL A DIMM1 | 1A |
| Date: Monday, March 09, 2009 | Sheet 15 of 34 | |

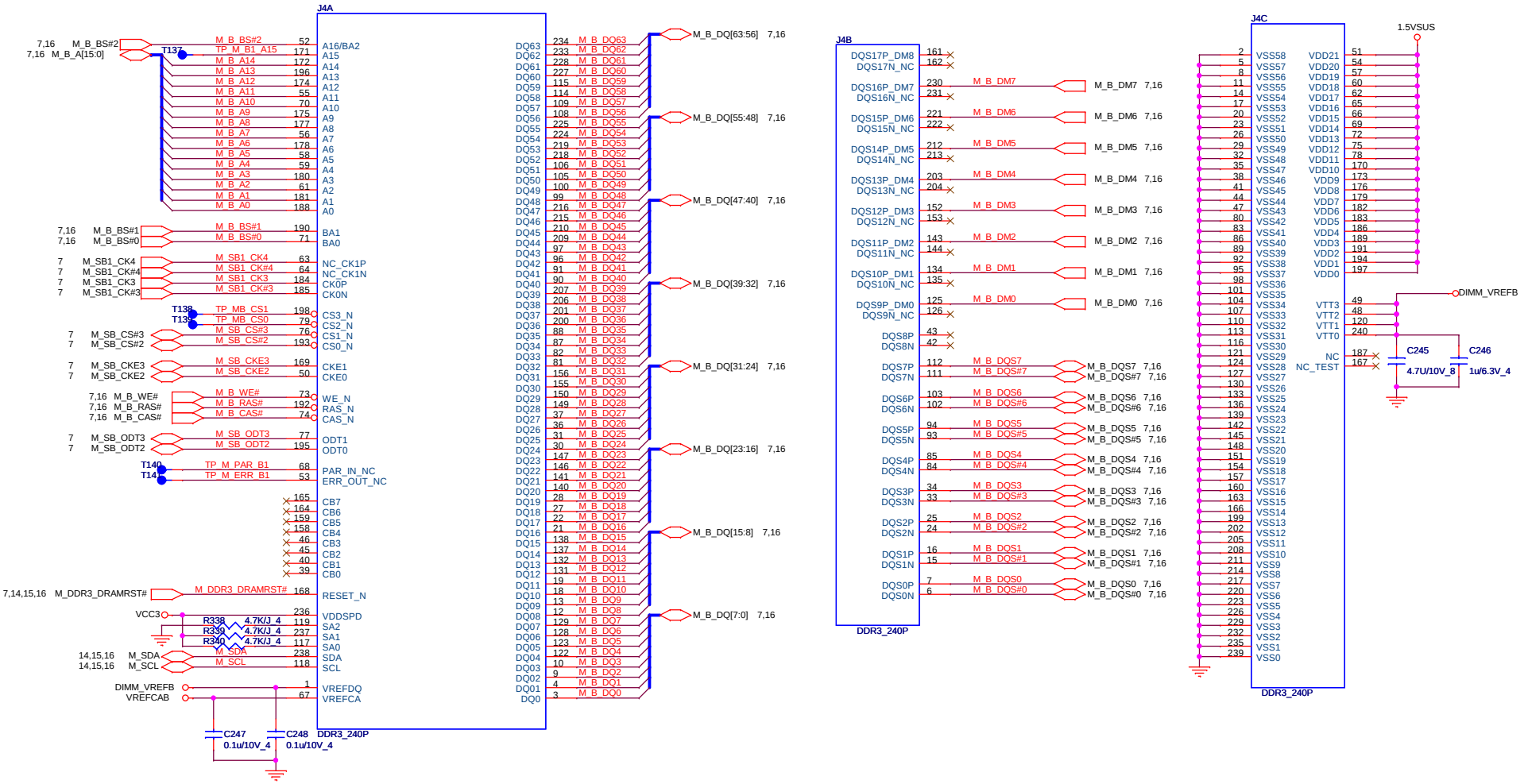





PROJECT : EL8

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 CHANNEL B DIMM0 | 1A |
| Date: Monday, March 09, 2009 | Sheet 16 of 34 | |



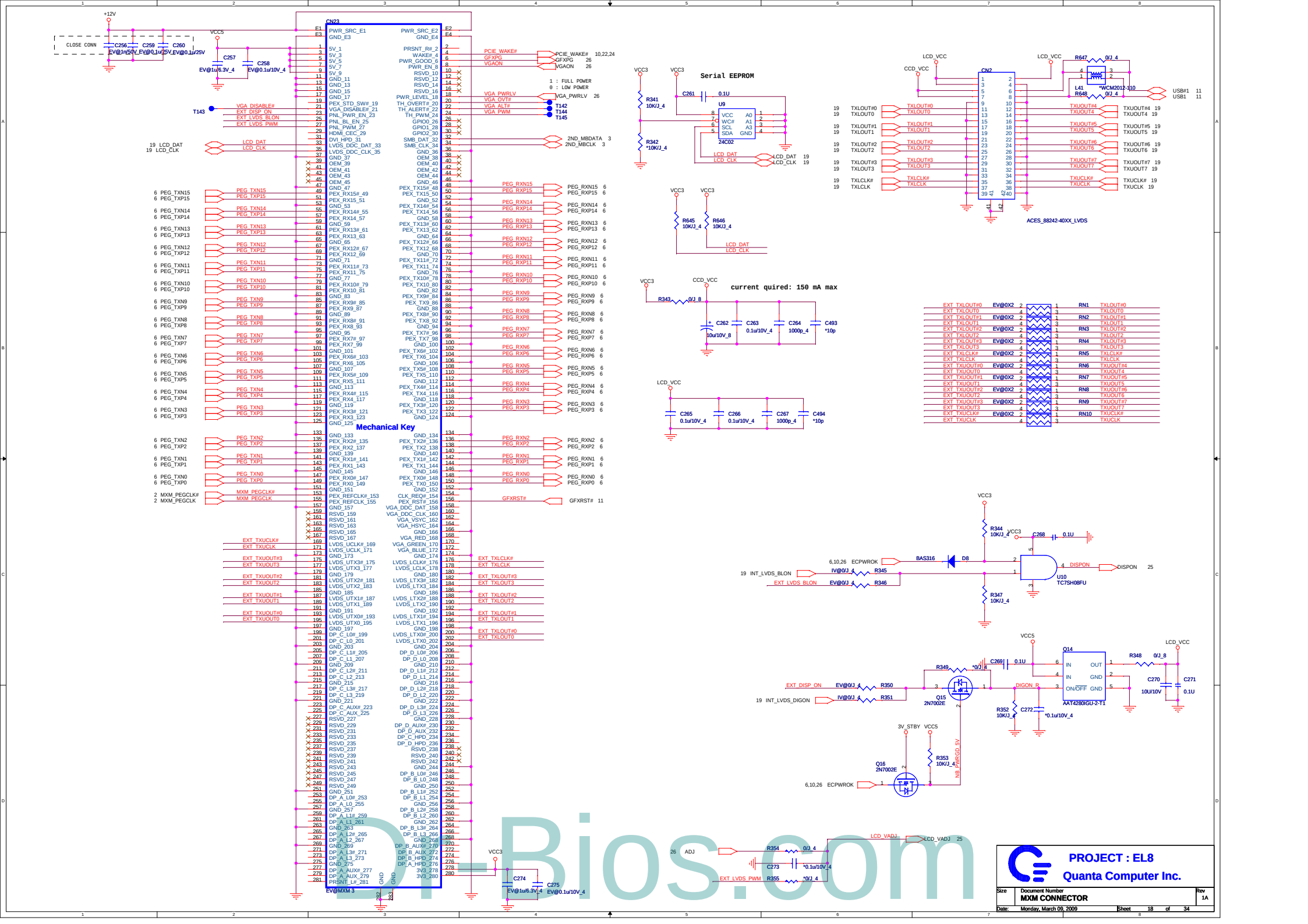


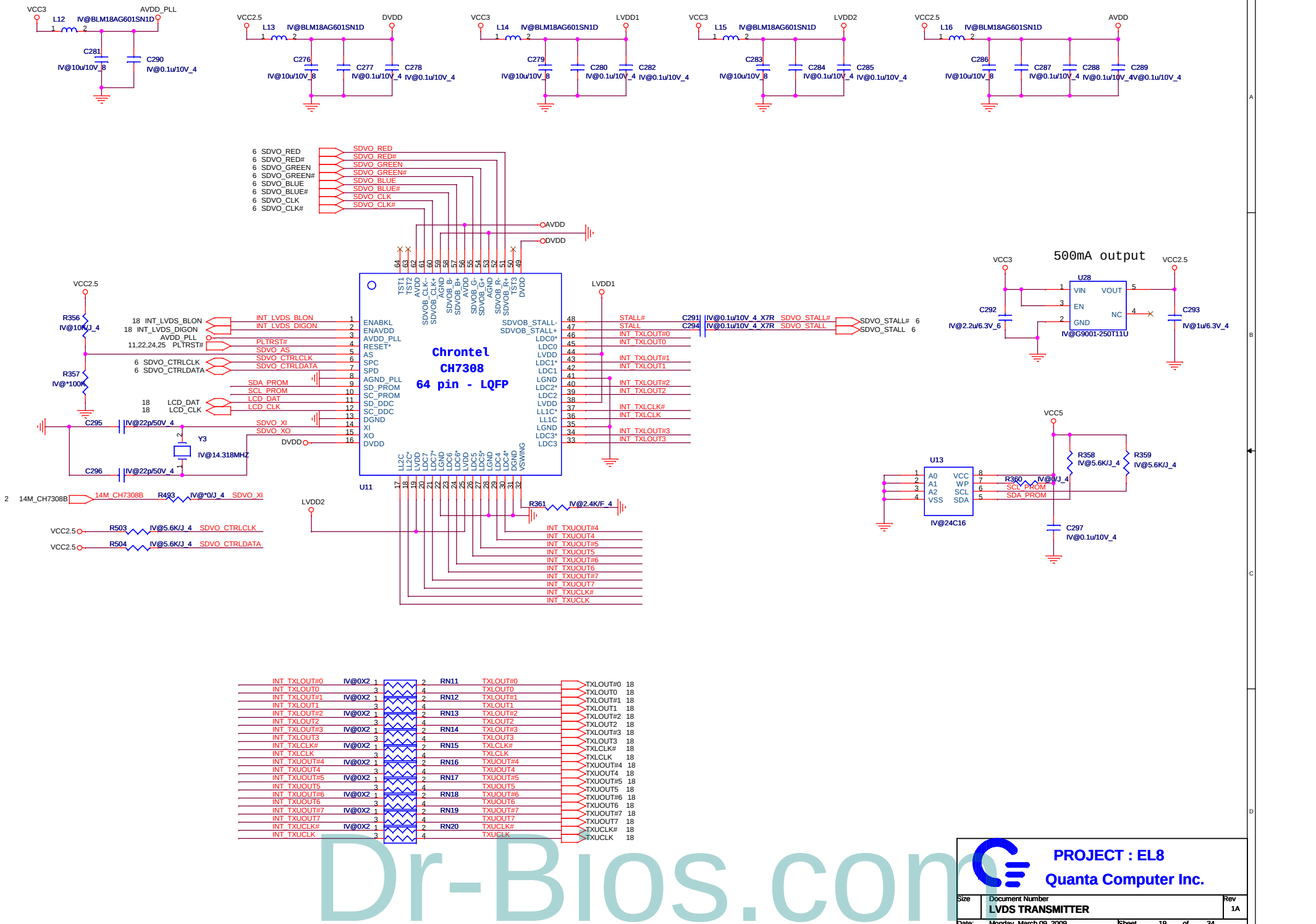

PROJECT : EL8

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 CHANNEL B DIMM1 | 1A |

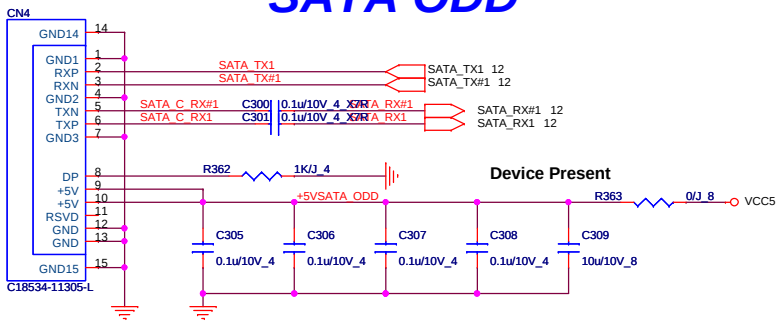
Date: Monday, March 09, 2009 Sheet 17 of 34

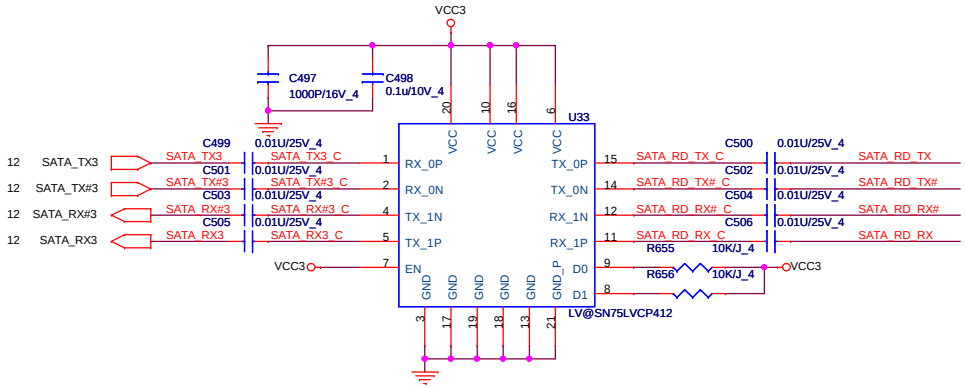

CN23
EV@MXM 3
Mechanical Key
Serial EEPROM
current quired: 150 mA max
CN2
ACES_88242-40XX_LVDS
PROJECT : EL8
Quanta Computer Inc.
MXM CONNECTOR
Monday, March 09, 2009
Sheet 18 of 34
Rev 1A


VCC3
AVDD_PLL
L12
IV@BLM18AG601SN1D
C281
IV@10u/10V_8
C290
IV@0.1u/10V_4
VCC2.5
DVDD
L13
C276
C277
C278
VCC3
LVDD1
L14
C279
C280
C282
VCC3
LVDD2
L15
C283
C284
C285
VCC2.5
AVDD
L16
C286
C287
C288
C289
SDVO_RED
SDVO_RED#
SDVO_GREEN
SDVO_GREEN#
SDVO_BLUE
SDVO_BLUE#
SDVO_CLK
SDVO_CLK#
AVDD
DVDD
Chrontel
CH7308
64 pin - LQFP
ENABKL
ENAVDD
AVDD_PLL
RESET*
AS
SPC
SPD
AGND_PLL
SD_PROM
SC_PROM
SD_DDC
SC_DDC
DGND
XI
XO
DVDD
SDVOB_STALL-
SDVOB_STALL+
LDC0*
LDC0
LVDD
LDC1*
LDC1
LGND
LDC2*
LDC2
LVDD
LL1C*
LL1C
LGND
LDC3*
LDC3
U11
INT_LVDS_BLON
INT_LVDS_DIGON
AVDD_PLL
PLTRST#
SDVO_AS
SDVO_CTRLCLK
SDVO_CTRLDATA
SDA_PROM
SCL_PROM
LCD_DAT
LCD_CLK
SDVO_XI
SDVO_XO
DVDD
R356
IV@10K/J_4
R357
IV@*100K
C295
IV@22p/50V_4
Y3
IV@14.318MHZ
C296
IV@22p/50V_4
14M_CH7308B
R493
IV@*0/J_4
SDVO_XI
R503
IV@5.6K/J_4
SDVO_CTRLCLK
R504
IV@5.6K/J_4
SDVO_CTRLDATA
VCC2.5
STALL#
STALL
INT_TXLOUT#0
INT_TXLOUT0
INT_TXLOUT#1
INT_TXLOUT1
INT_TXLOUT#2
INT_TXLOUT2
INT_TXLCLK#
INT_TXLCLK
INT_TXLOUT#3
INT_TXLOUT3
C291
C294
IV@0.1u/10V_4_X7R
SDVO_STALL#
SDVO_STALL
SDVO_STALL# 6
SDVO_STALL 6
LVDD2
R361
IV@2.4K/F_4
INT_TXUOUT#4
INT_TXUOUT4
INT_TXUOUT#5
INT_TXUOUT5
INT_TXUOUT#6
INT_TXUOUT6
INT_TXUOUT#7
INT_TXUOUT7
INT_TXUCLK#
INT_TXUCLK
500mA output
VCC3
VCC2.5
U28
VIN
VOUT
EN
NC
GND
C292
IV@2.2u/6.3V_6
C293
IV@1u/6.3V_4
IV@G9001-250T11U
VCC5
U13
A0
A1
A2
VSS
VCC
WP
SCL
SDA
R358
IV@5.6K/J_4
R359
IV@5.6K/J_4
R360
IV@0/J_4
SCL_PROM
SDA_PROM
IV@24C16
C297
IV@0.1u/10V_4
INT_TXLOUT#0
INT_TXLOUT0
INT_TXLOUT#1
INT_TXLOUT1
INT_TXLOUT#2
INT_TXLOUT2
INT_TXLOUT#3
INT_TXLOUT3
INT_TXLCLK#
INT_TXLCLK
INT_TXUOUT#4
INT_TXUOUT4
INT_TXUOUT#5
INT_TXUOUT5
INT_TXUOUT#6
INT_TXUOUT6
INT_TXUOUT#7
INT_TXUOUT7
INT_TXUCLK#
INT_TXUCLK
IV@0X2
RN11
RN12
RN13
RN14
RN15
RN16
RN17
RN18
RN19
RN20
TXLOUT#0
TXLOUT0
TXLOUT#1
TXLOUT1
TXLOUT#2
TXLOUT2
TXLOUT#3
TXLOUT3
TXLCLK#
TXLCLK
TXUOUT#4
TXUOUT4
TXUOUT#5
TXUOUT5
TXUOUT#6
TXUOUT6
TXUOUT#7
TXUOUT7
TXUCLK#
TXUCLK
PROJECT : EL8
Quanta Computer Inc.
Size
Document Number
LVDS TRANSMITTER
Rev
1A
Date: Monday, March 09, 2009
Sheet 19 of 34

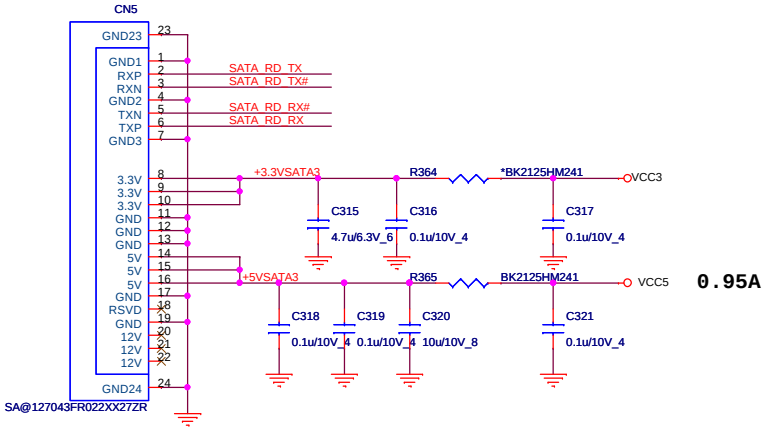
# SATA ODD

2.1A



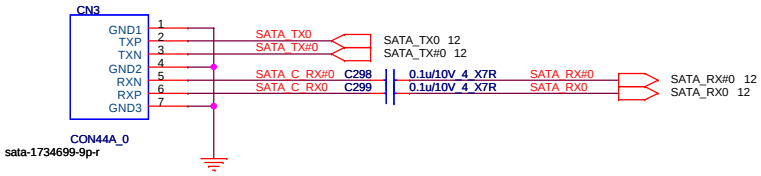




# 2nd SATA HDD(2.5")




0.95A

# SATA HDD(3.5")



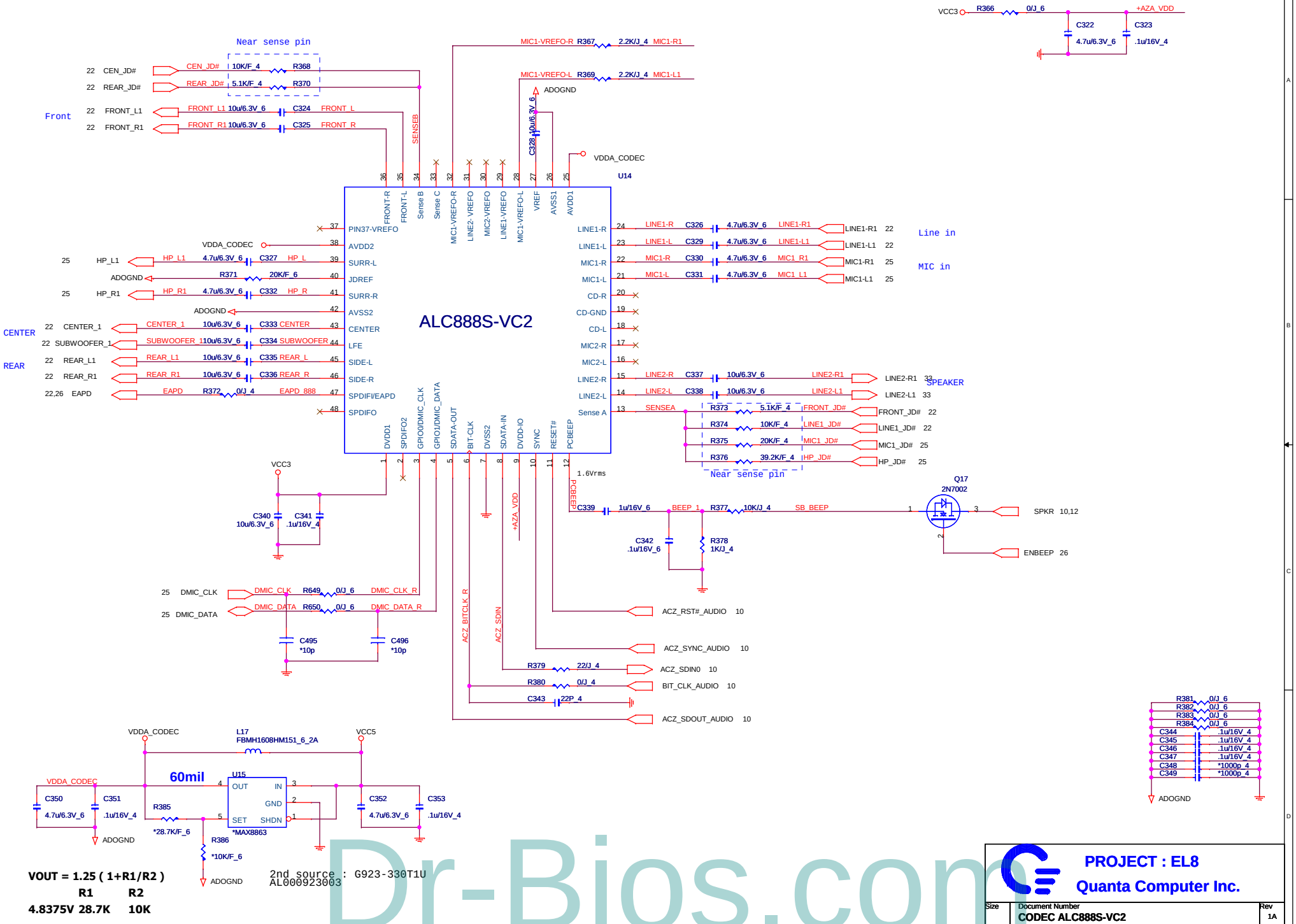



PROJECT : EL8

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | 3.5HDD/2.5HDD/ODD | 1A |
| Date: Monday, March 09, 2009 | Sheet 20 of 34 | |

# CODEC

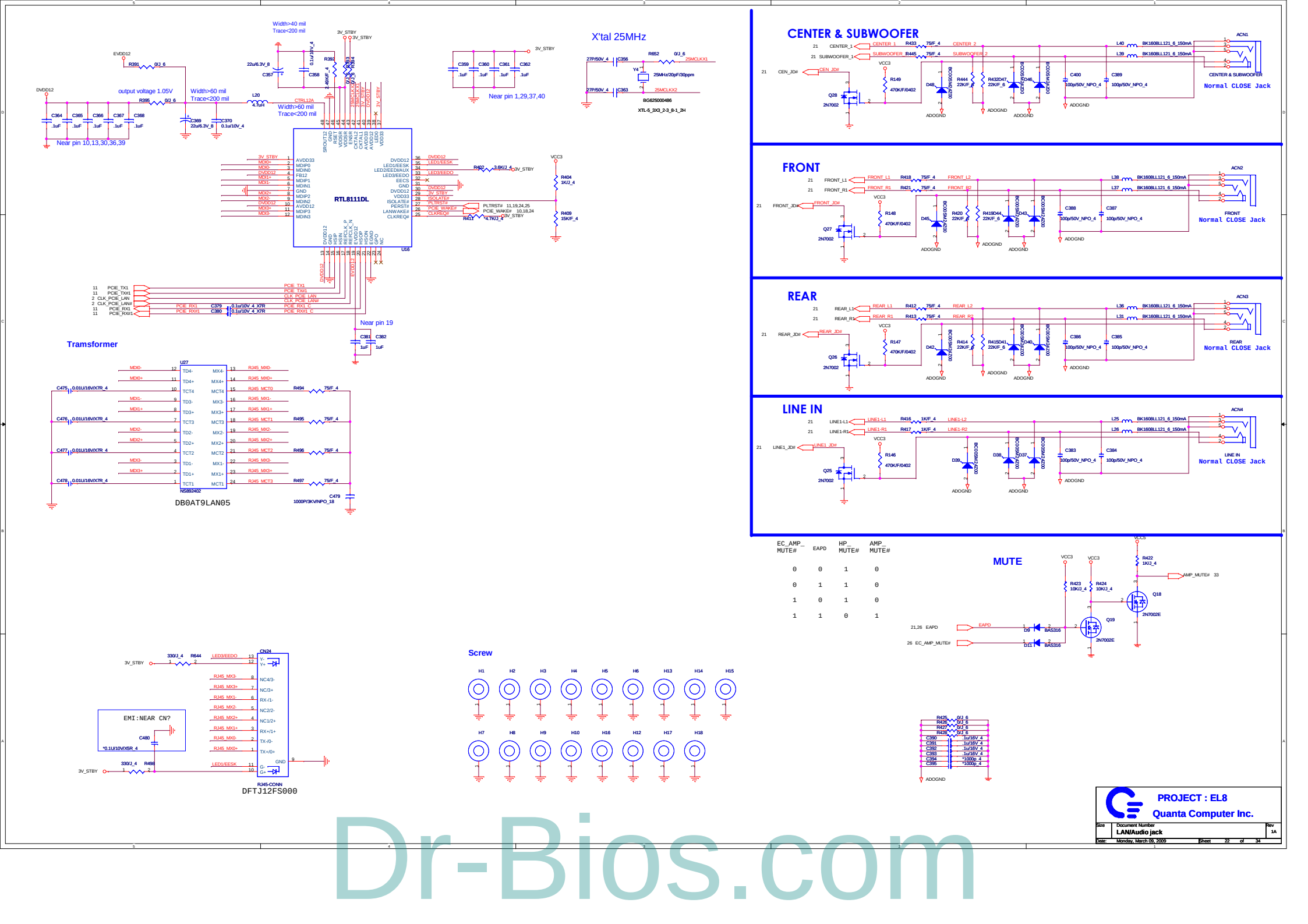




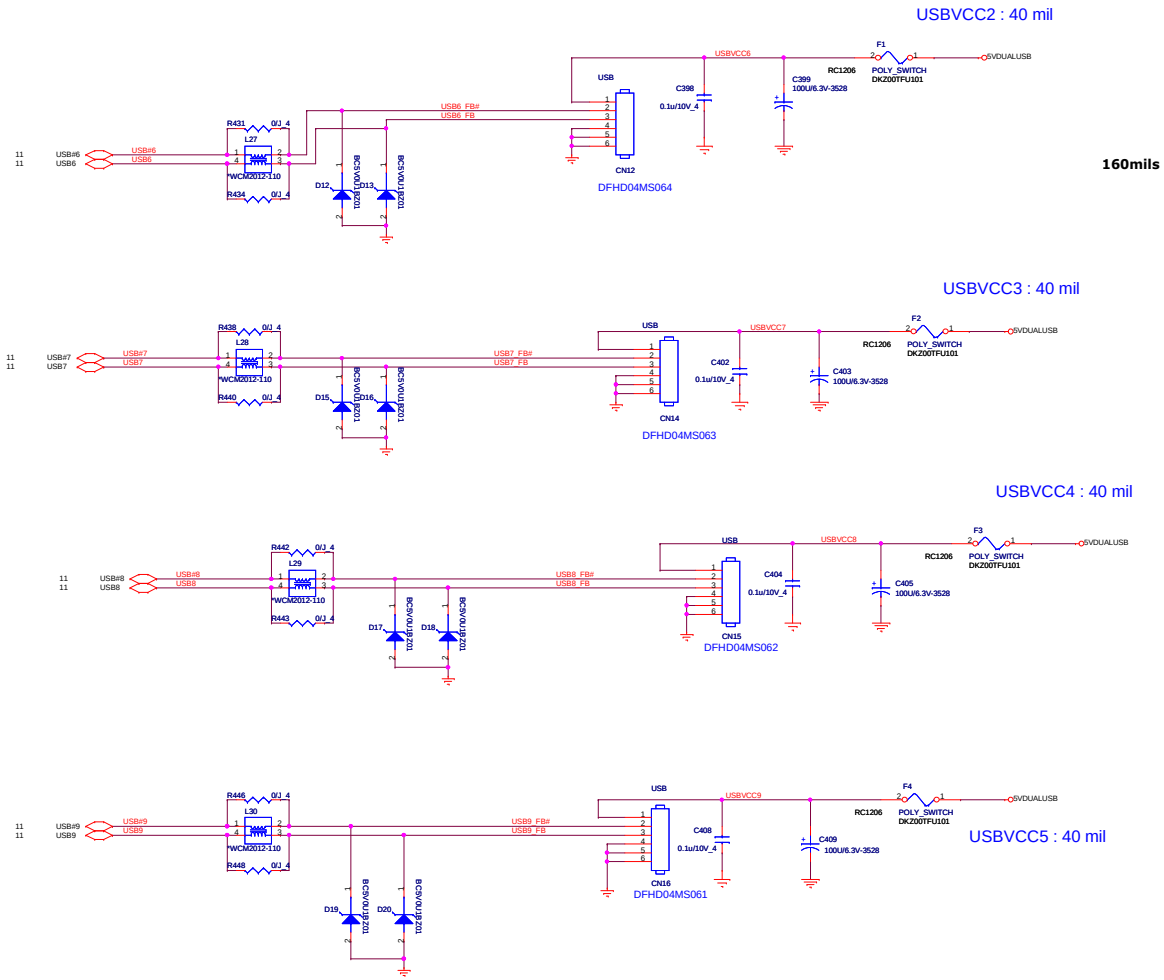

PROJECT : EL8

Quanta Computer Inc.

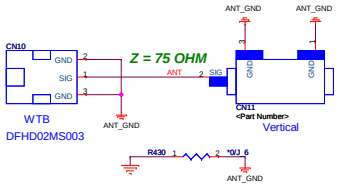
| Size | Document Number | Rev |
|---|---|---|
| | CODEC ALC888S-VC2 | 1A |
| Date: Monday, March 09, 2009 | Sheet 21 of 34 | |


CENTER & SUBWOOFER
FRONT
REAR
LINE IN
MUTE
Tramsformer
DB0AT9LAN05
DFTJ12FS000
Screw
X'tal 25MHz
RTL8111DL
Near pin 10,13,30,36,39
Near pin 1,29,37,40
Near pin 19
output voltage 1.05V
Width>40 mil
Trace<200 mil
Width>60 mil
Trace<200 mil
EMI:NEAR CN?
Normal CLOSE Jack
EC_AMP_MUTE#
EAPD
HP_MUTE#
AMP_MUTE#
PROJECT : EL8
Quanta Computer Inc.
Document Number
LAN/Audio jack
Monday, March 09, 2009
Sheet 22 of 34

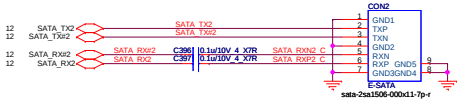
# REAR USB PORT X4



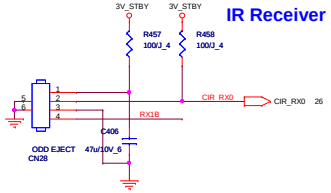

## TV ANT. CONNECTOR



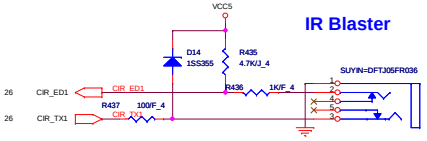

## ESATA CONN

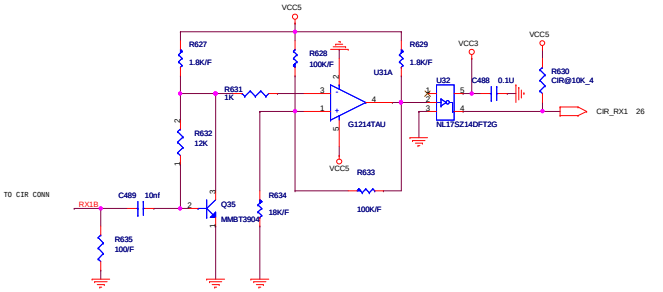



## IR Receiver

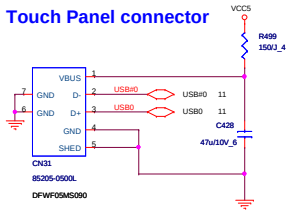



## IR Blaster

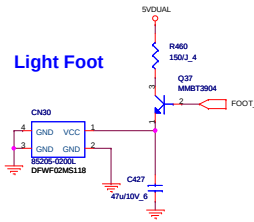


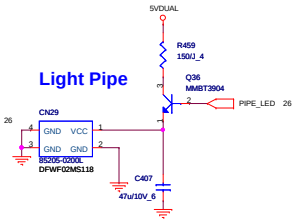

## Touch Panel connector



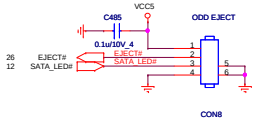

## Light Foot



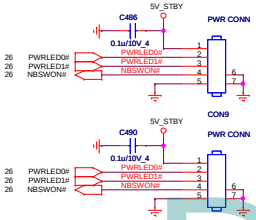

## Light Pipe



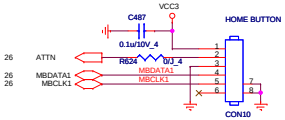

## ODD BUTTON

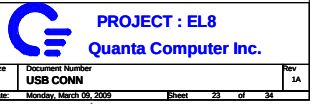


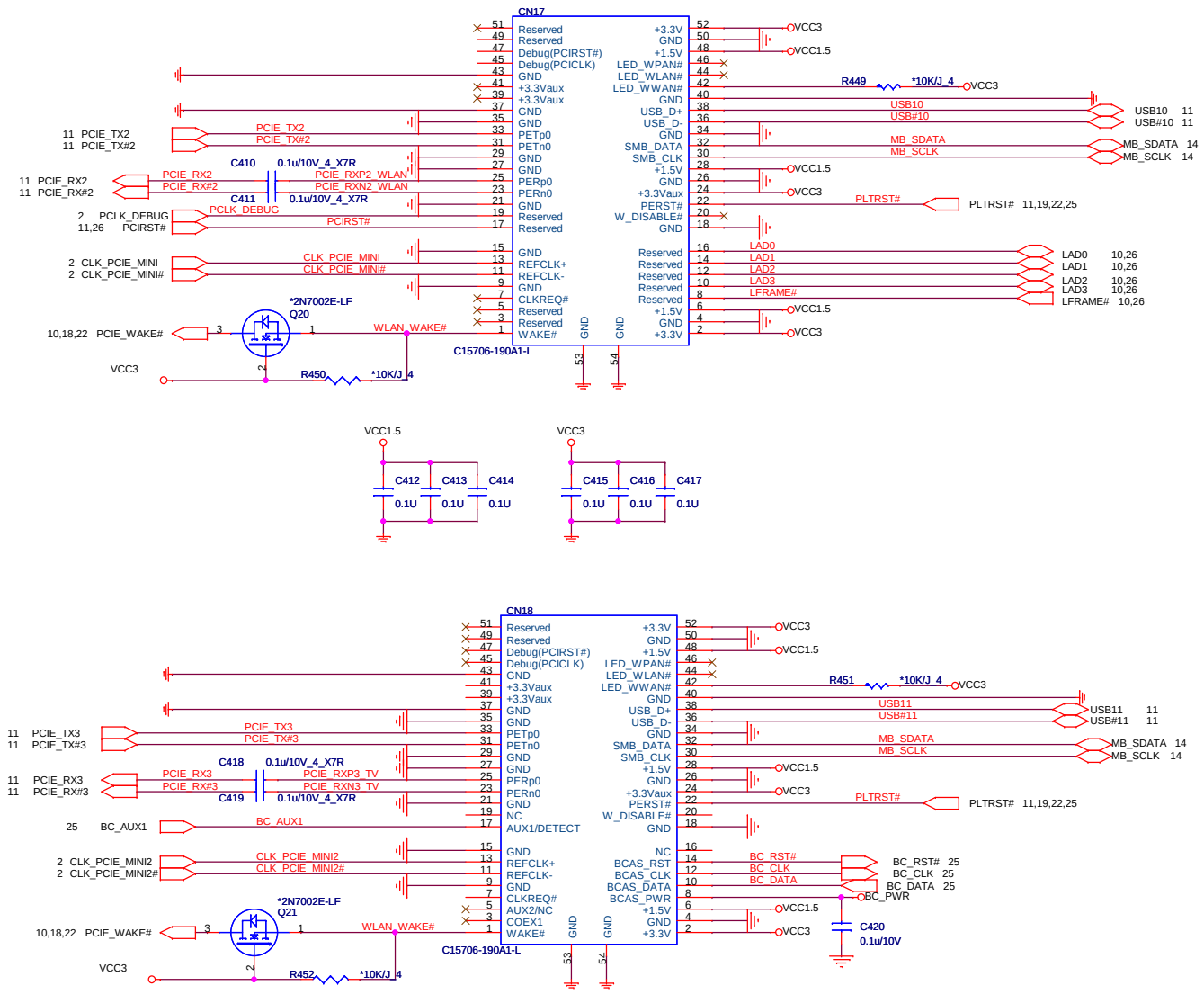

## POWER BUTTON




## HOME BUTTON








PROJECT : EL8

Quanta Computer Inc.

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|---|---|---|
| | MINI PCIE(WLAN/TV) | 1A |

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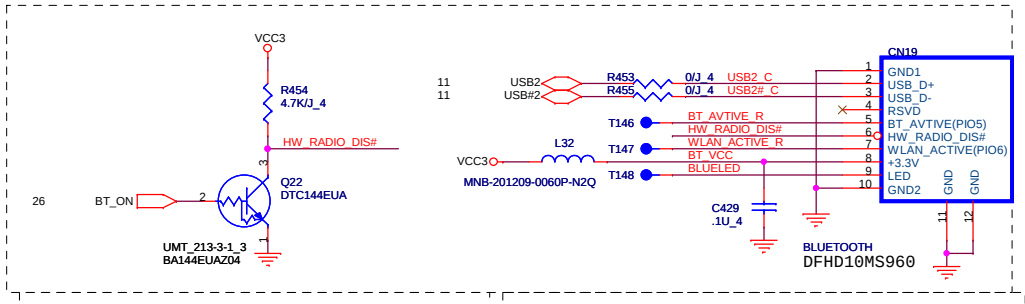


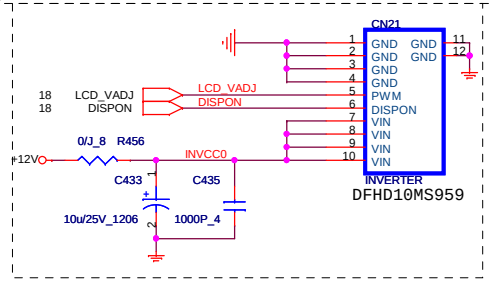


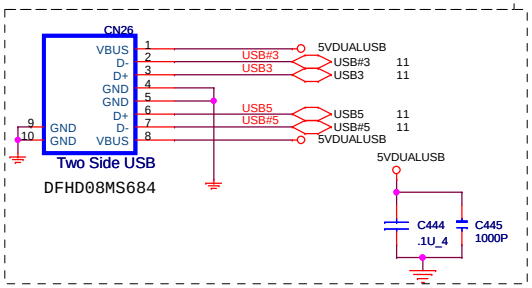


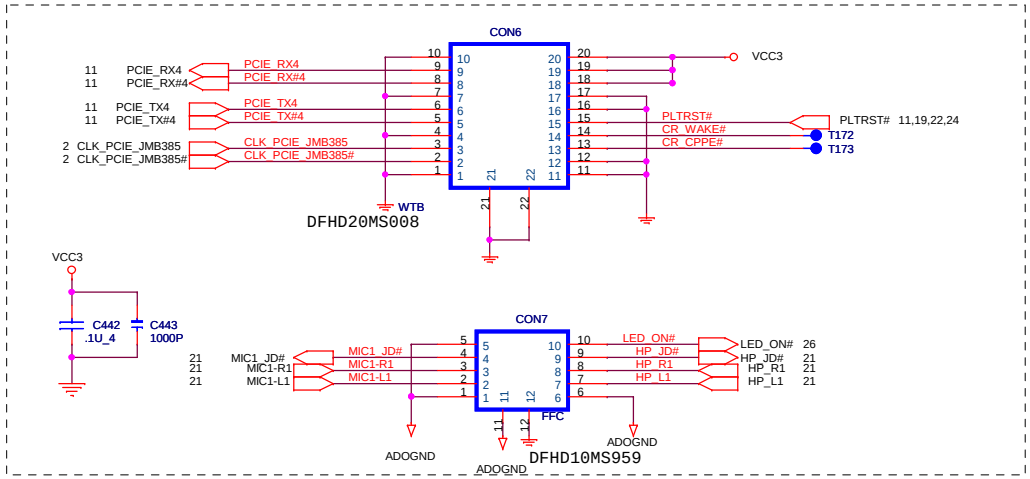


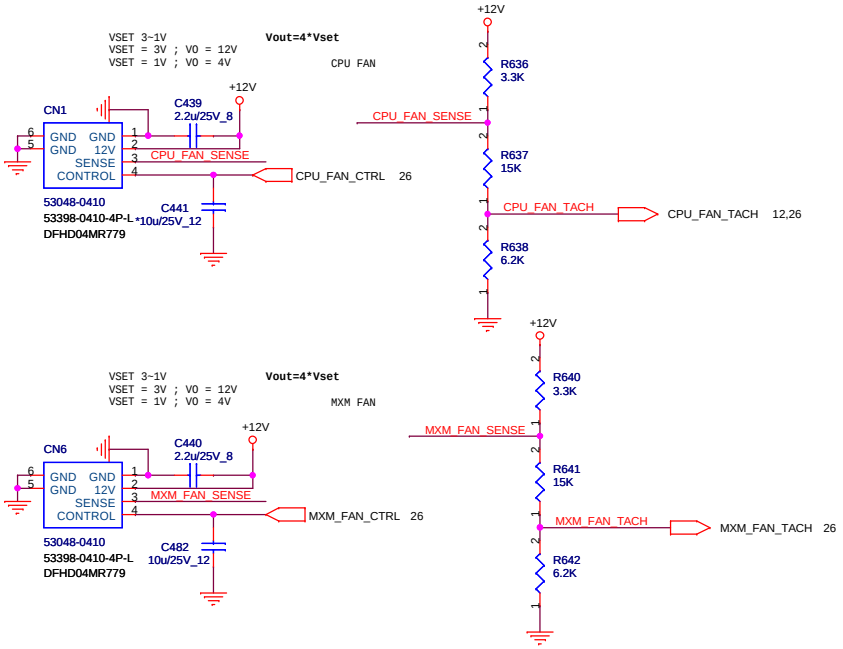


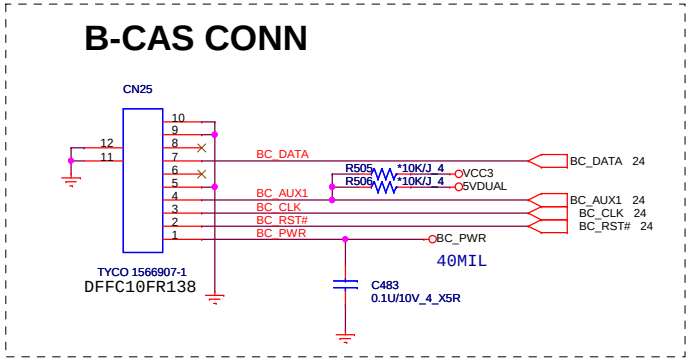


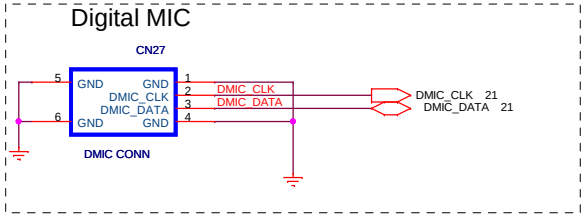


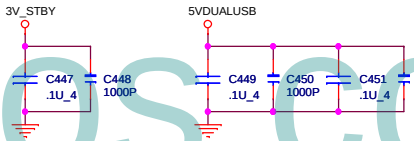




PROJECT : EL8
Quanta Computer Inc.

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|---|---|---|
| | CONNECTOR | 1A |

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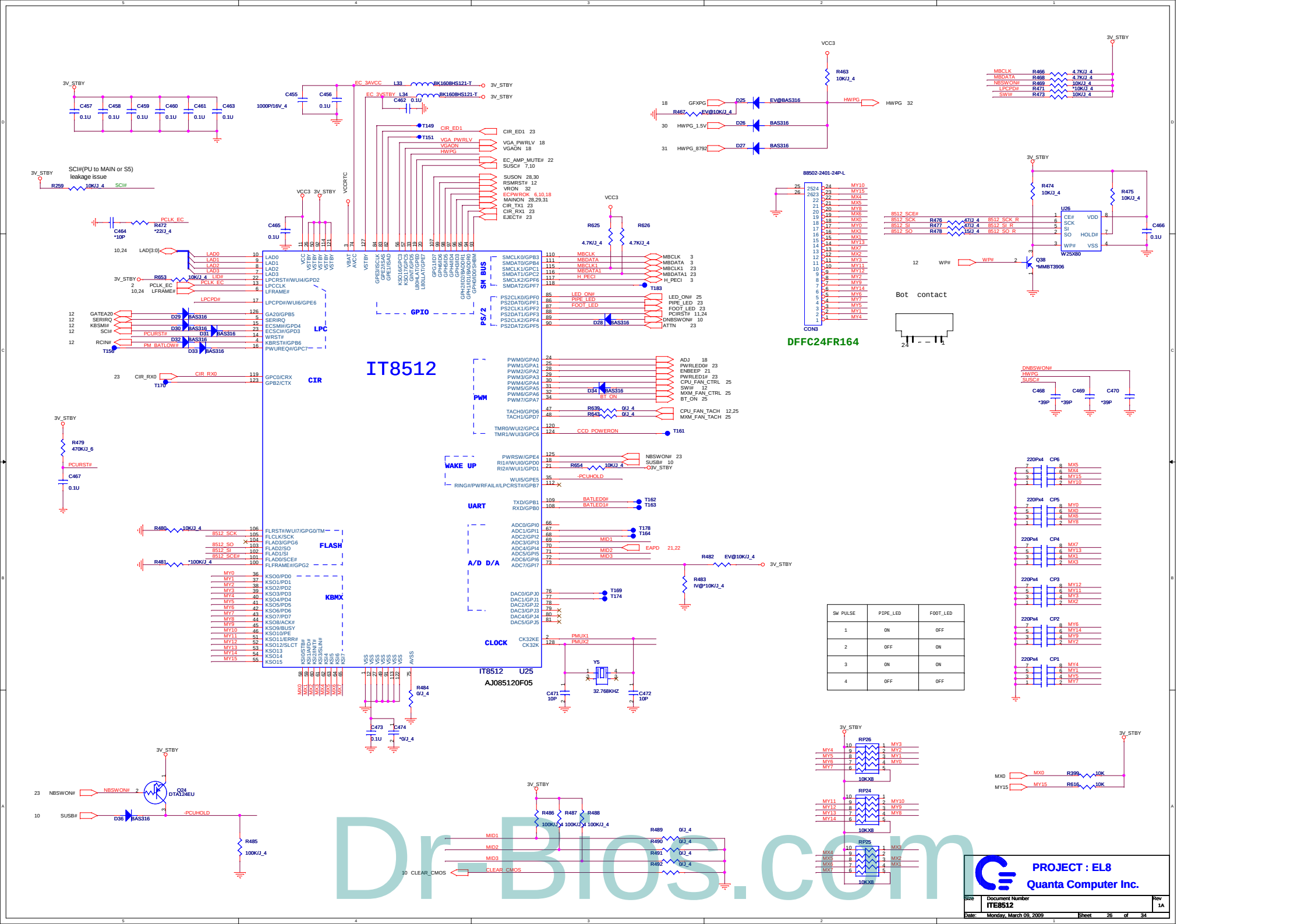
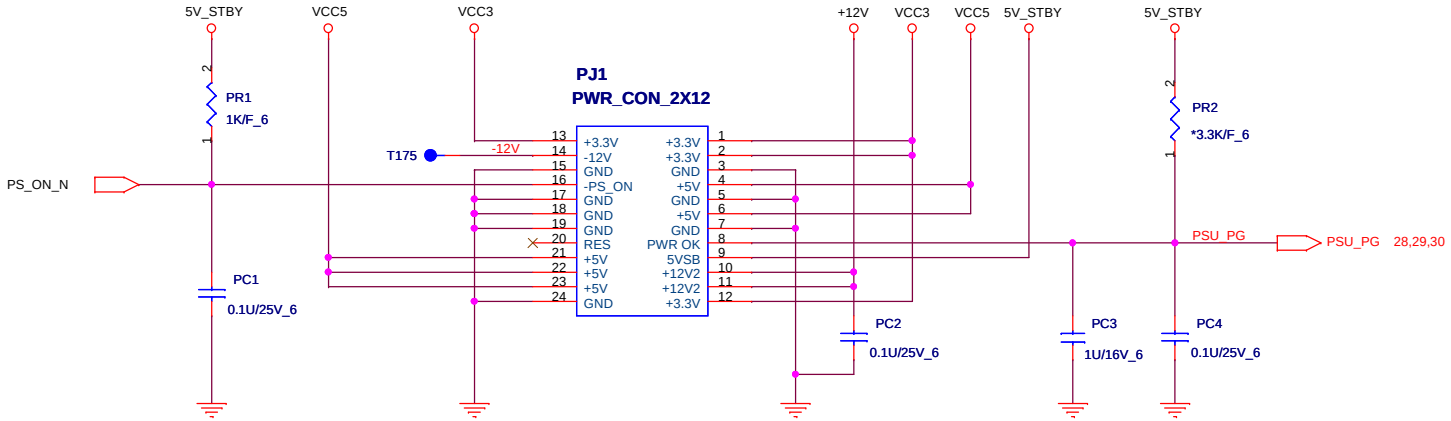
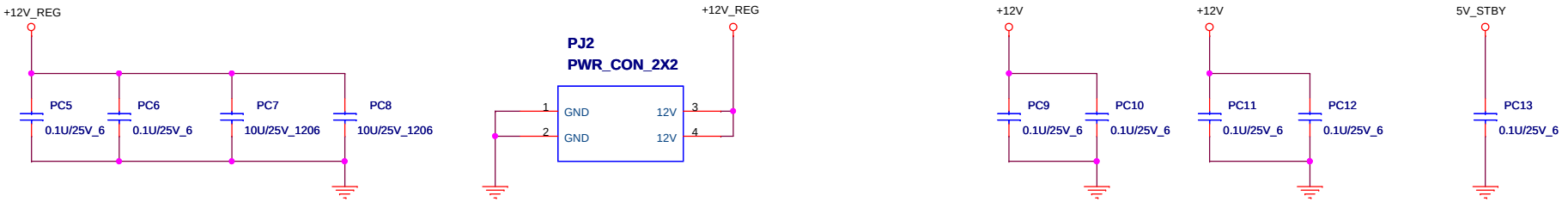

IT8512
IT8512 U25
AJ085120F05
LPC
CIR
GPIO
SM BUS
PS/2
PWM
WAKE UP
UART
A/D D/A
CLOCK
FLASH
KBMX
DFFC24FR164
Bot contact
88502-2401-24P-L
W25X80
DTA124EU
Dr-Bios.com
PROJECT : EL8
Quanta Computer Inc.
ITE8512
Monday, March 09, 2009

# PSU 24PIN Connector




P3V3_STB : Stand-by power source only
P3V3 : Normal power source only
P3V3_DUAL : Both power source switching

# 4PIN +12V_REG for CPU_CORE






Quanta Computer Inc.
PROJECT : EL8

| Size | Document Number | Rev |
|---|---|---|
| | PWR_CONNECTOR | 1A |
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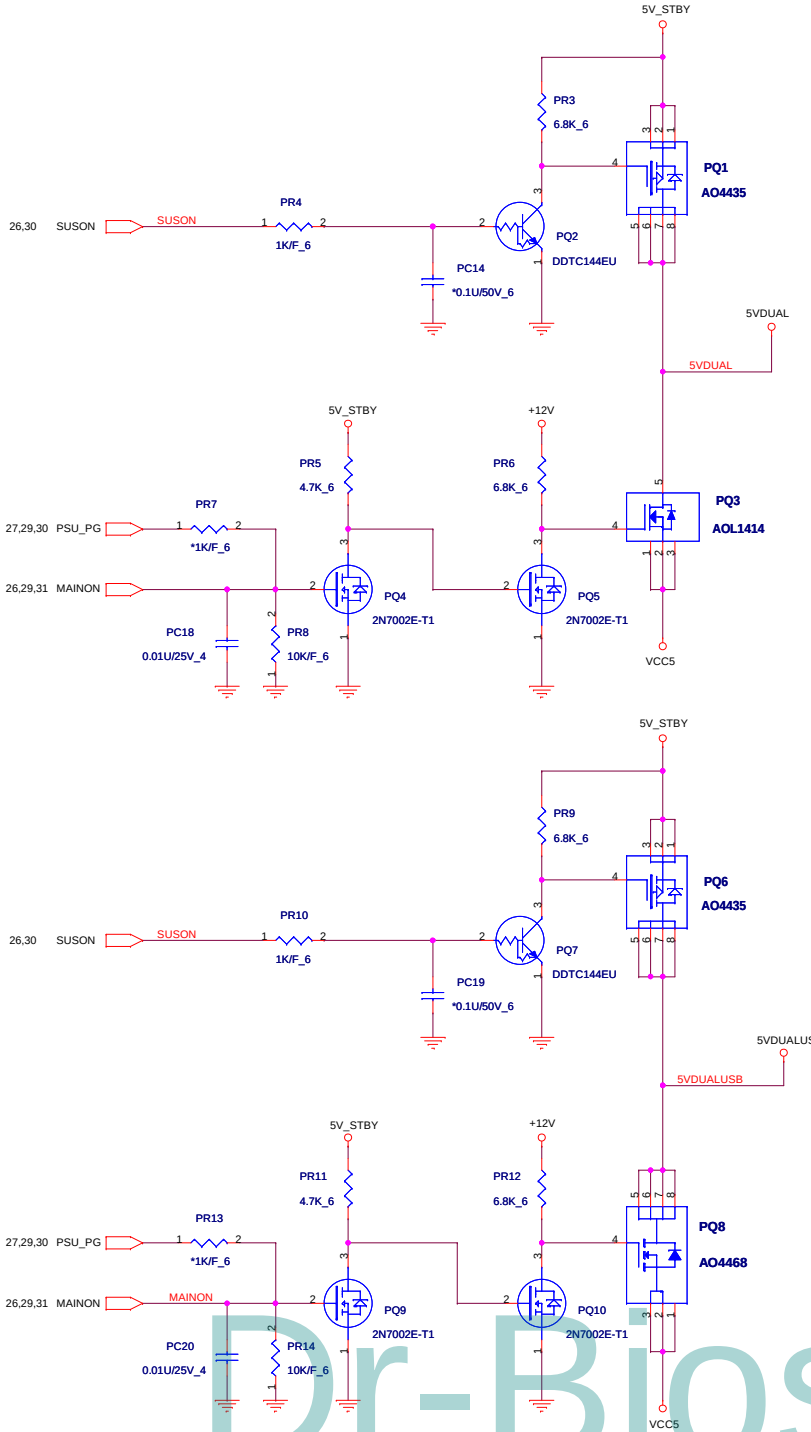
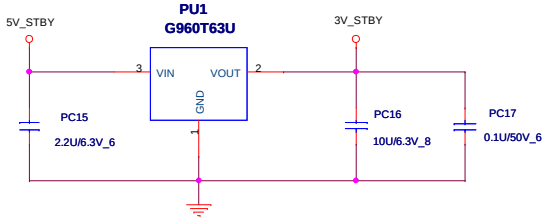
# 5VDUAL, 5VDUALUSB, 3V_STBY




for EC



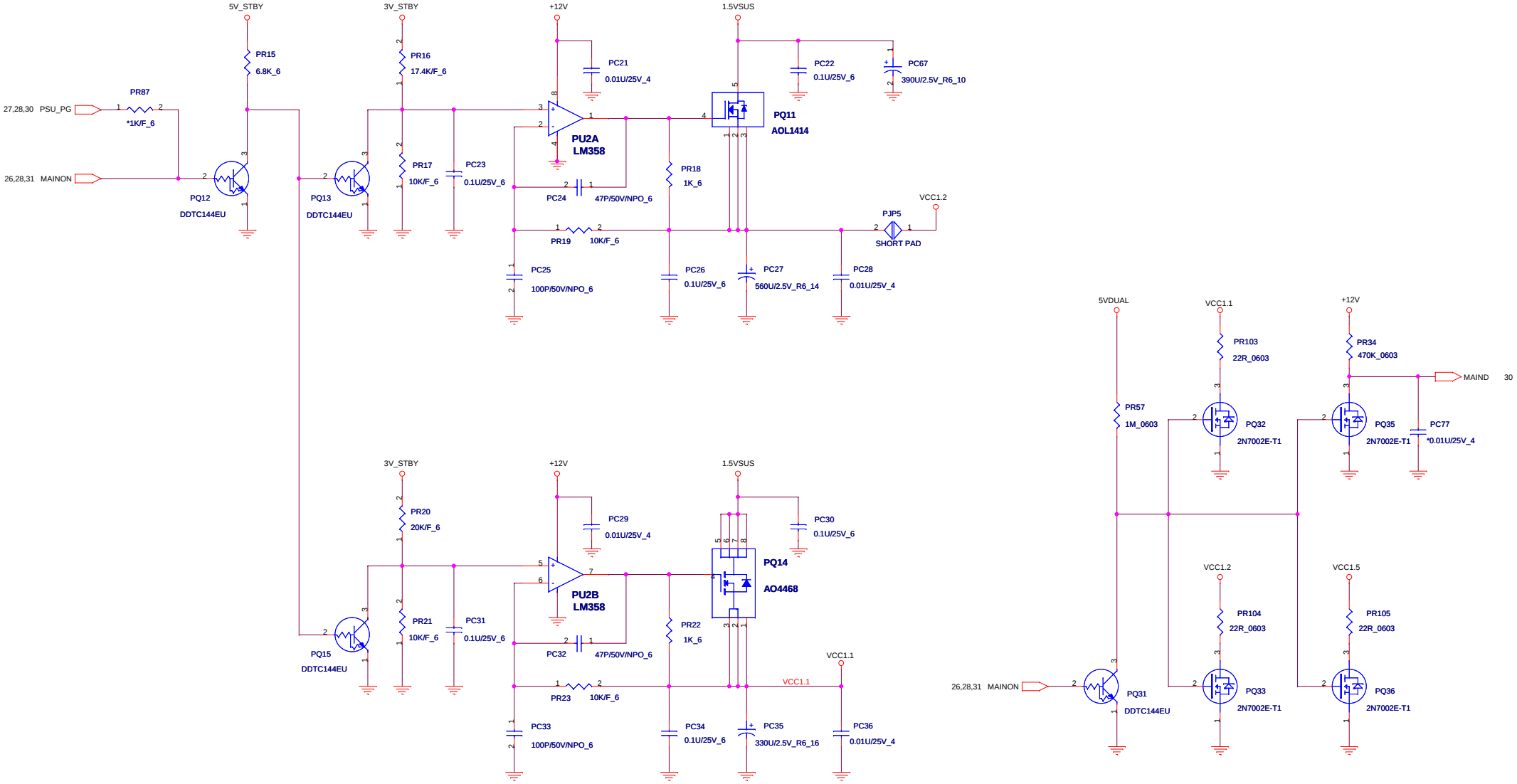



Quanta Computer Inc.

PROJECT : EL8

| Size | Document Number | Rev |
|---|---|---|
| | 5VDUAL, 5VDUALUSB & 3V_STBY | 1A |
| Date: Monday, March 09, 2009 | Sheet 28 of 34 | |

# VCC1.2, VCC1.1




For ICH10



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : EL8 | | |
| Size | Document Number: VCC1.1 & VCC1.2 | Rev 1A |
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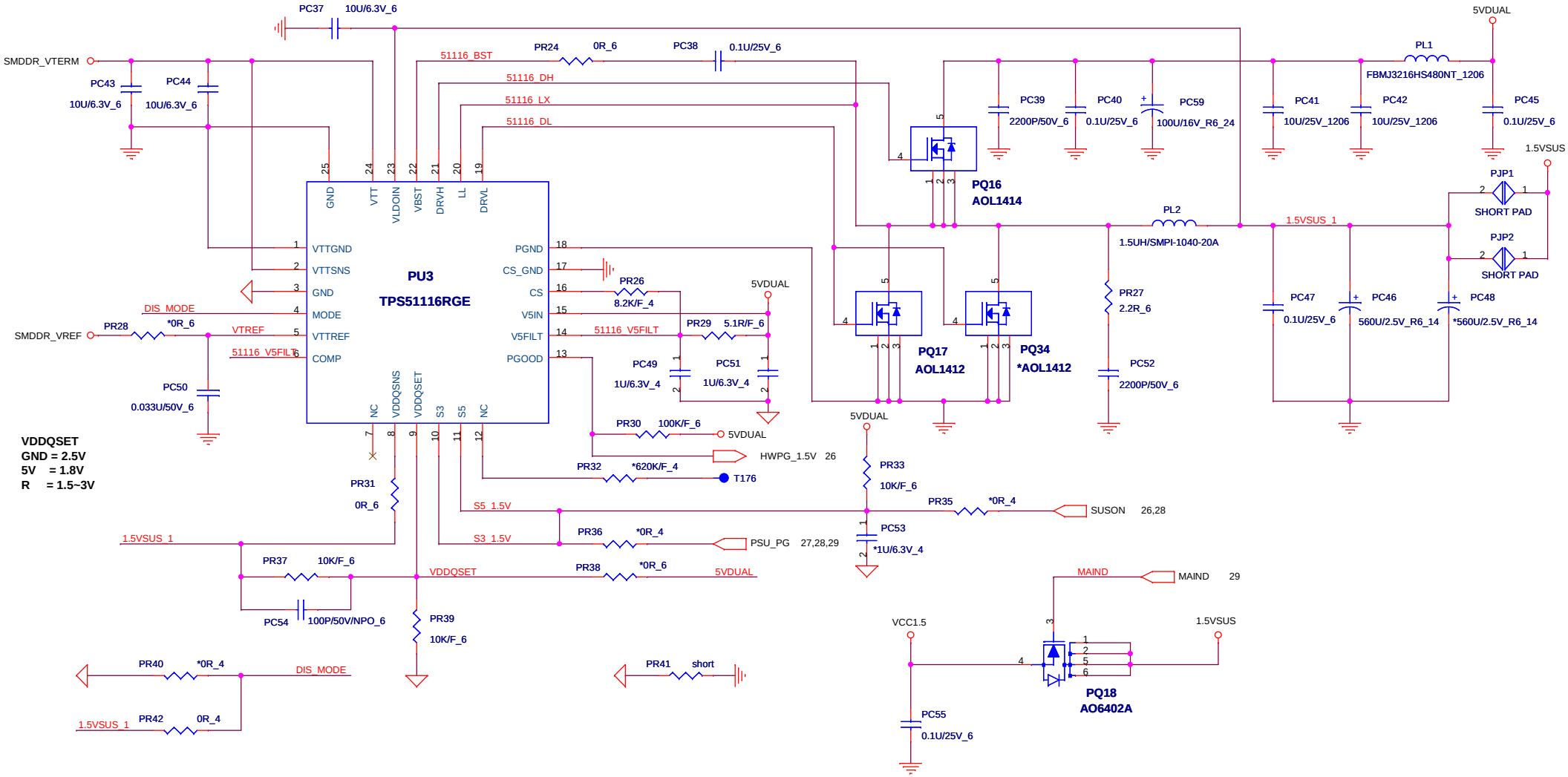
# DDR3 1.5V(TPS51116)




del_IL=(5V-1.5V)x1.5V/(1.5ux400Kx19V)=4.6A

(10uAxPR26/Rdson)+del_IL/2=Iocp

(10uAx8.2K/4.6m)+del_IL/2=20.1A

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
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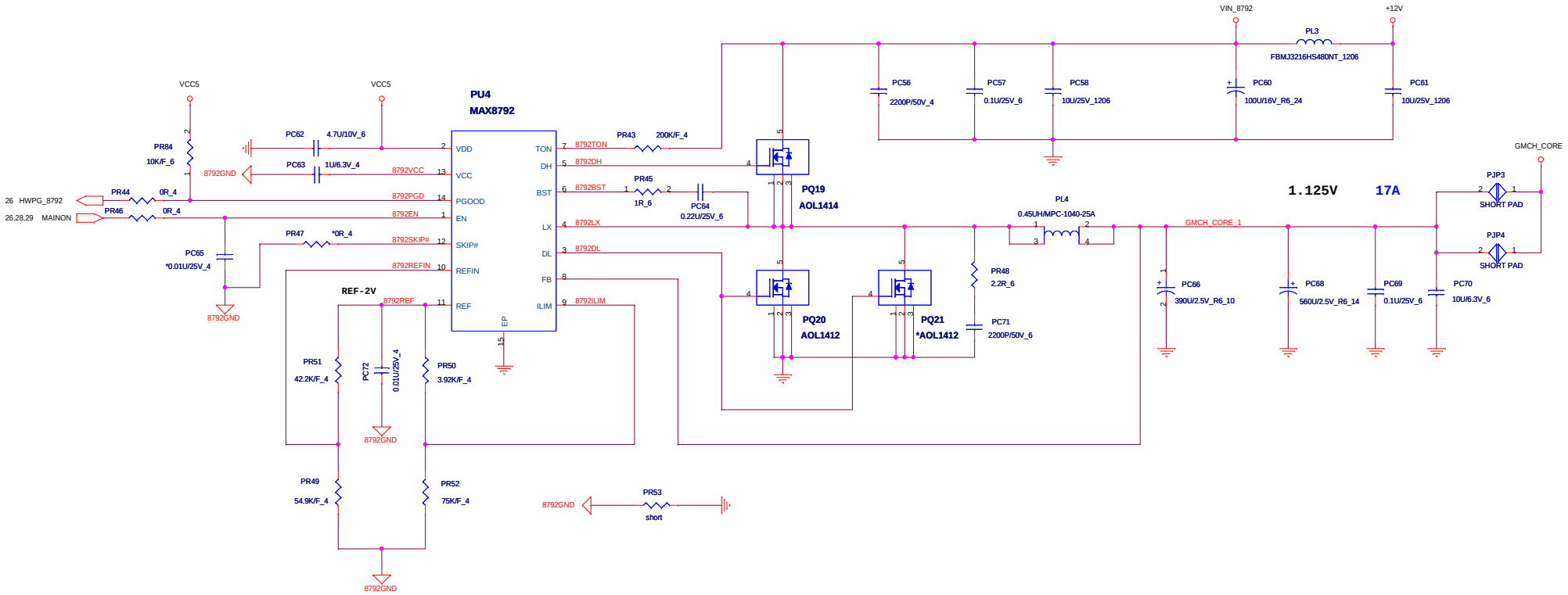
# G43 GMCH_CORE



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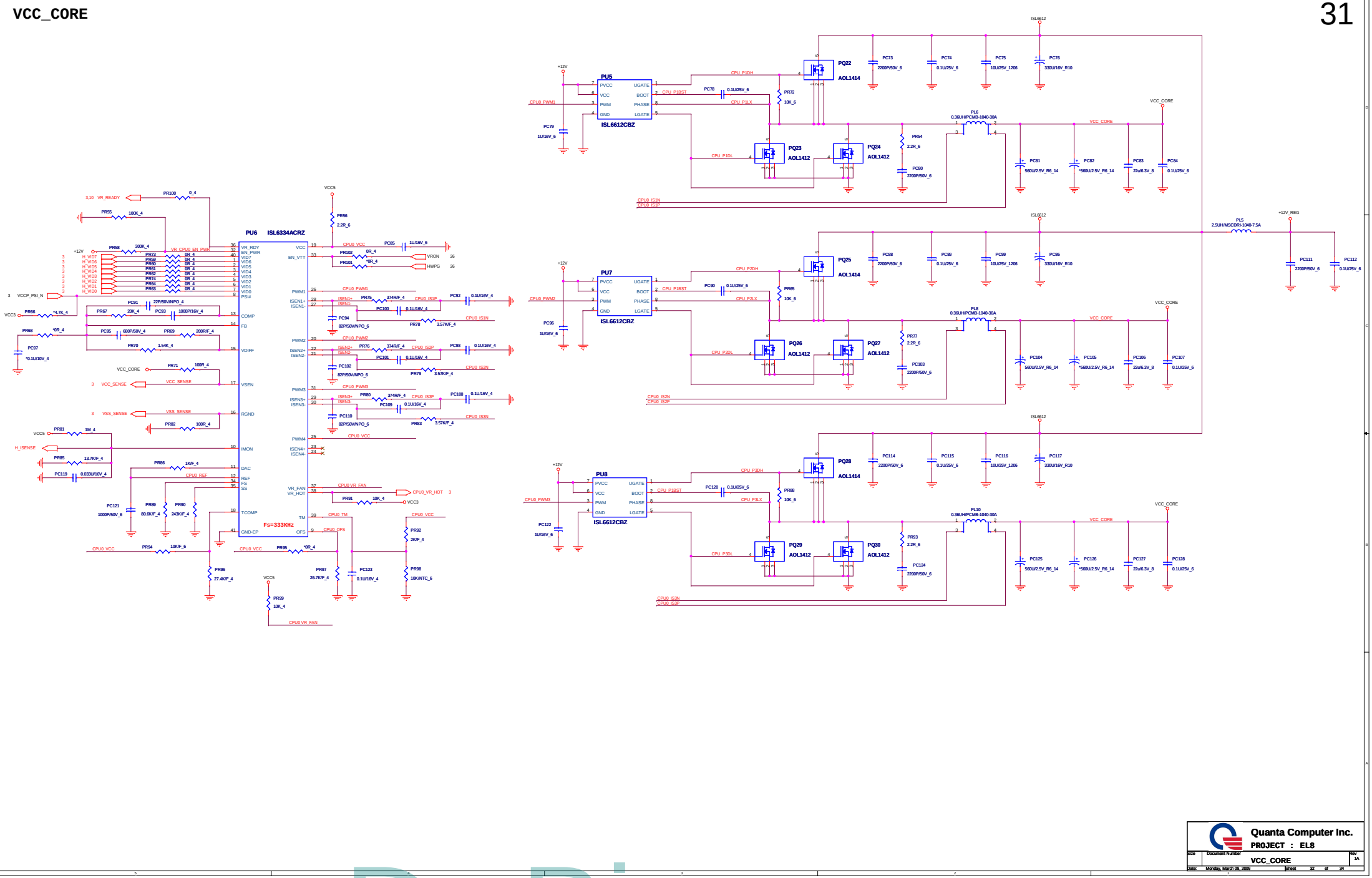
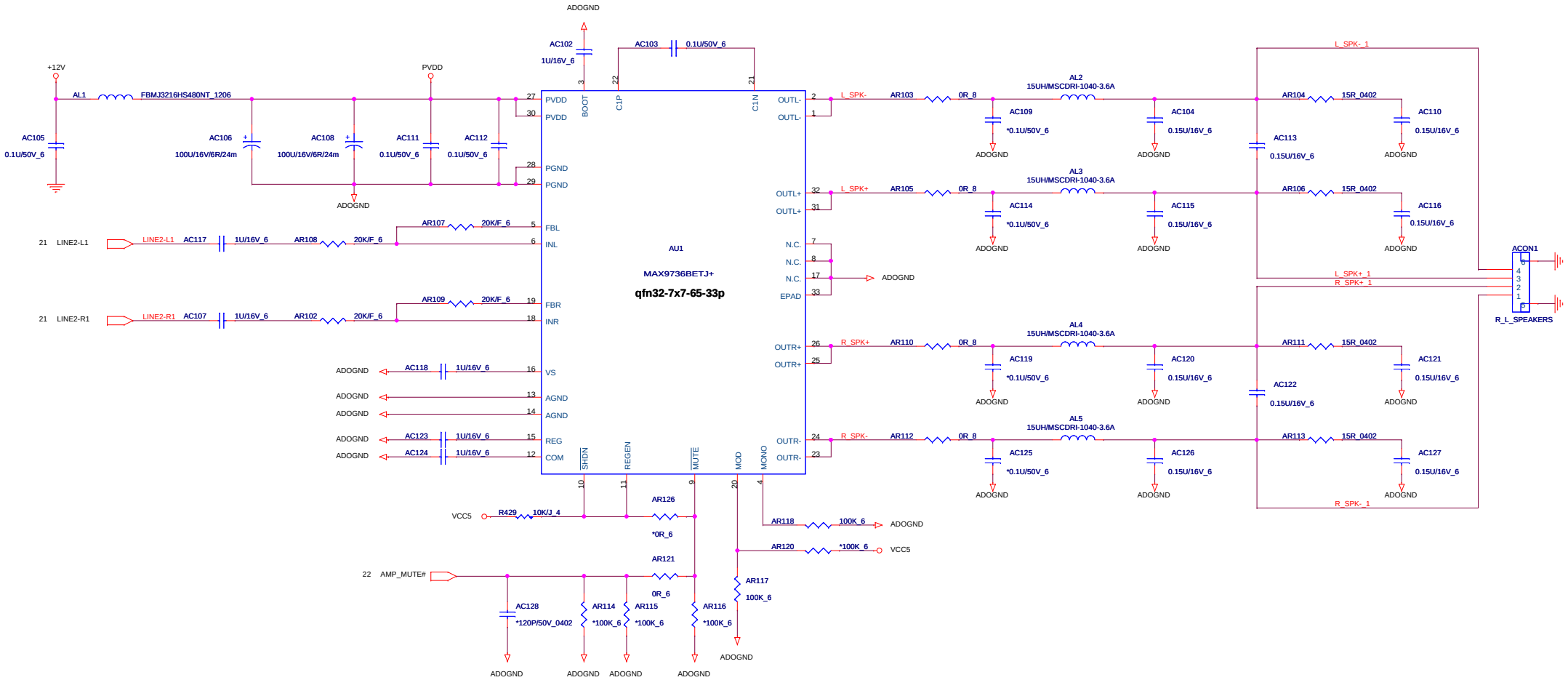

PU6 ISL6334ACRZ
Fs=333KHz
PU5 ISL6612CBZ
PU7 ISL6612CBZ
PU8 ISL6612CBZ
PQ22 AOL1414
PQ23 AOL1412
PQ24 AOL1412
PQ25 AOL1414
PQ26 AOL1412
PQ27 AOL1412
PQ28 AOL1414
PQ29 AOL1412
PQ30 AOL1412
PL6 0.36UH/PCMB-1040-30A
PL8 0.36UH/PCMB-1040-30A
PL10 0.36UH/PCMB-1040-30A
PL5 2.5UH/MSCDRI-1040-7.5A
VCC_CORE
+12V_REG
Quanta Computer Inc.
PROJECT : EL8
VCC_CORE
Monday, March 09, 2009

# Speaker AMP.





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|---|---|---|
| | Change List | 1A |

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