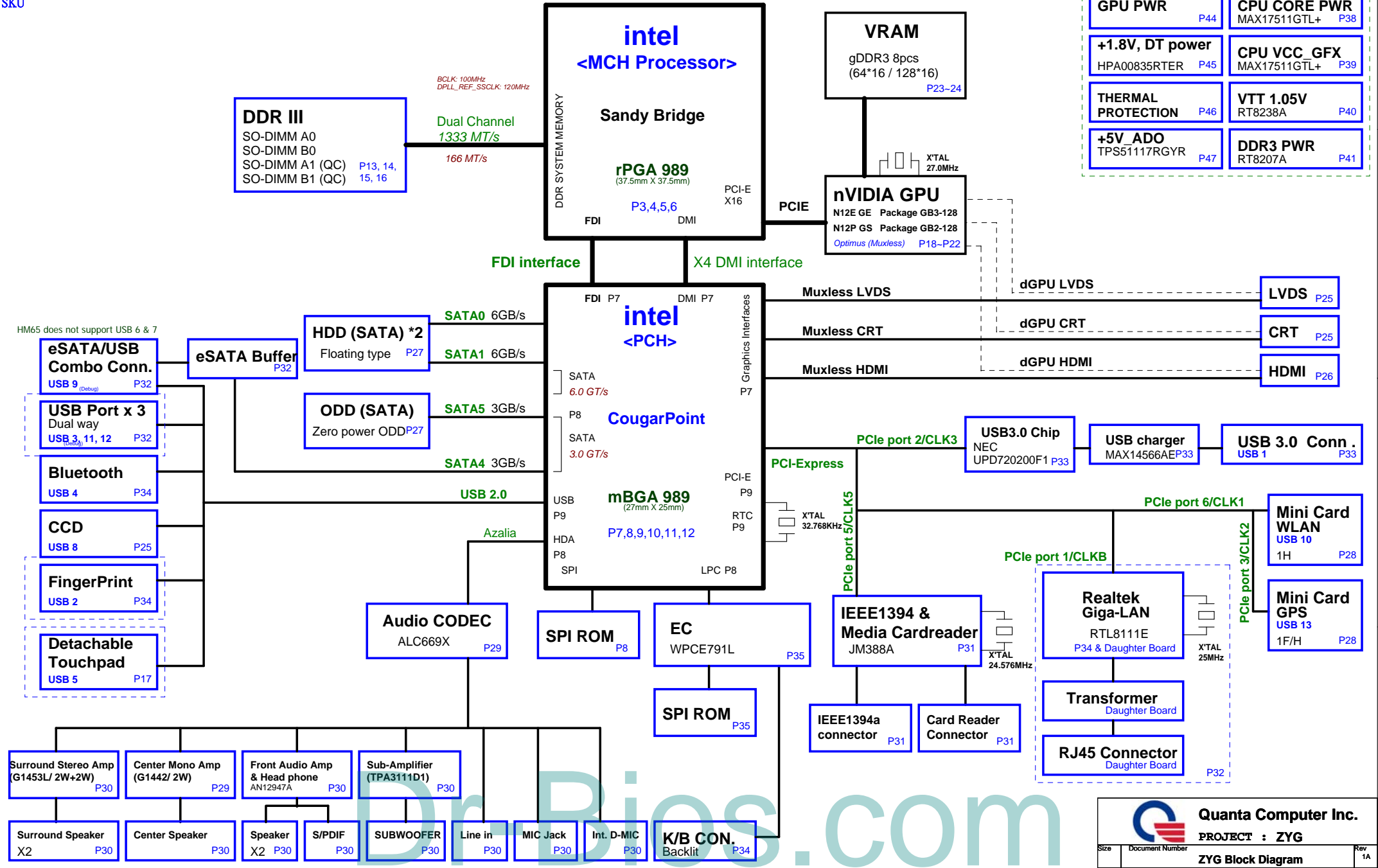


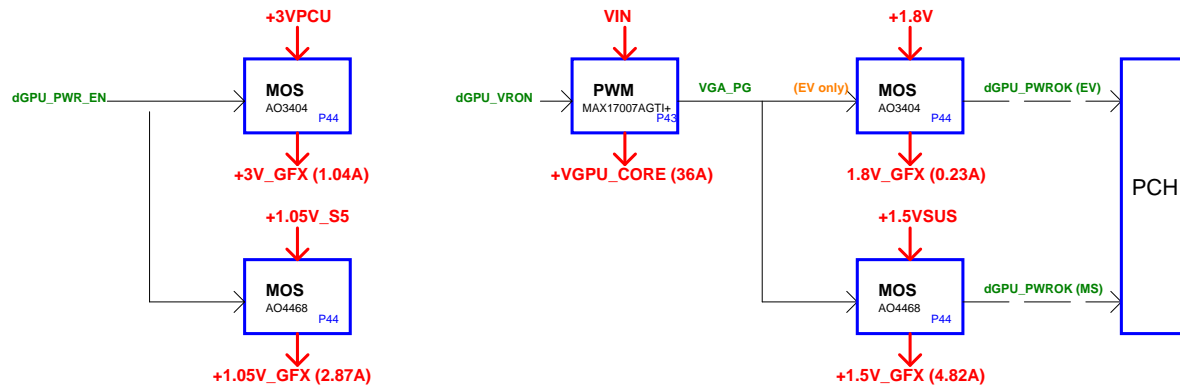
# ZYG SYSTEM BLOCK DIAGRAM

<b>+VCCSA</b> TPS51461 P42	<b>CHARGER</b> ISL88731A P36
<b>GPU CORE PWR</b> MAX17007AGTI+ P43	<b>3/5V SYS PWR</b> RT8223M P37
<b>GPU PWR</b> P44	<b>CPU CORE PWR</b> MAX17511GTL+ P38
<b>+1.8V, DT power</b> HPA00835RTER P45	<b>CPU VCC_GFX</b> MAX17511GTL+ P39
<b>THERMAL PROTECTION</b> P46	<b>VTT 1.05V</b> RT8238A P40
<b>+5V_ADO</b> TPS51117RGYR P47	<b>DDR3 PWR</b> RT8207A P41

EV@ --- GPU  
 MS@ --- iGPU & GPU  
 MUX@ --- N12P-GS  
 N12E@ --- N12E-GE  
 CPU --- Special  
 GPS@ --- GPS  
 BT@ --- BT  
 SKU

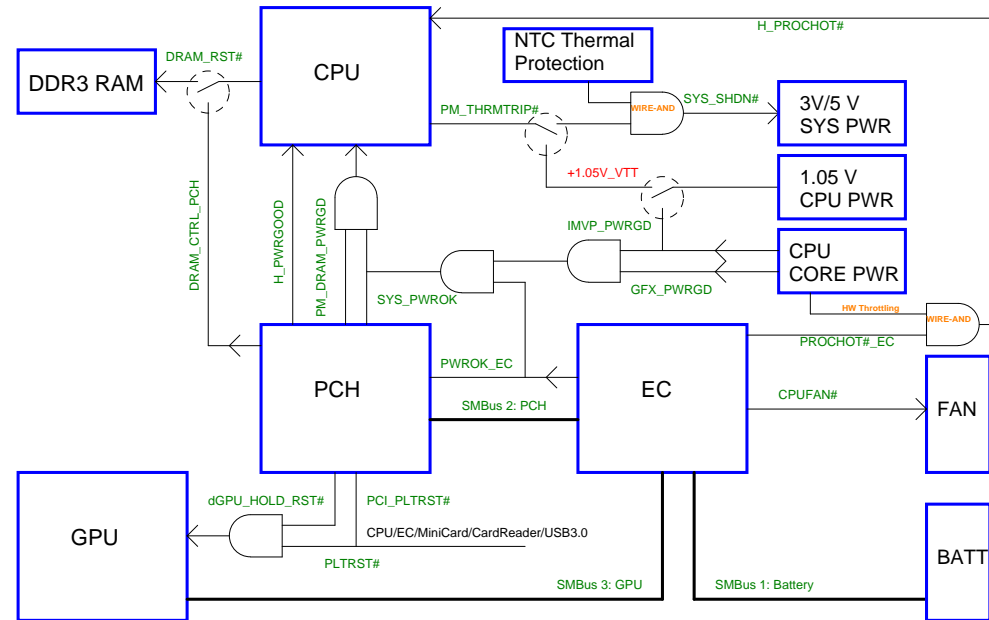


# GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



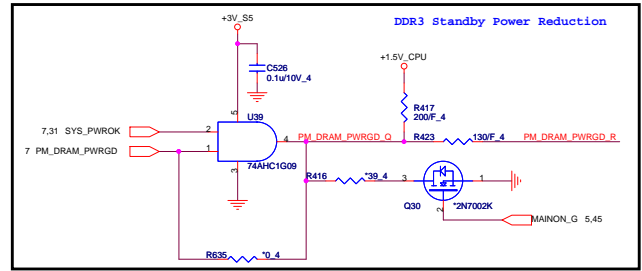
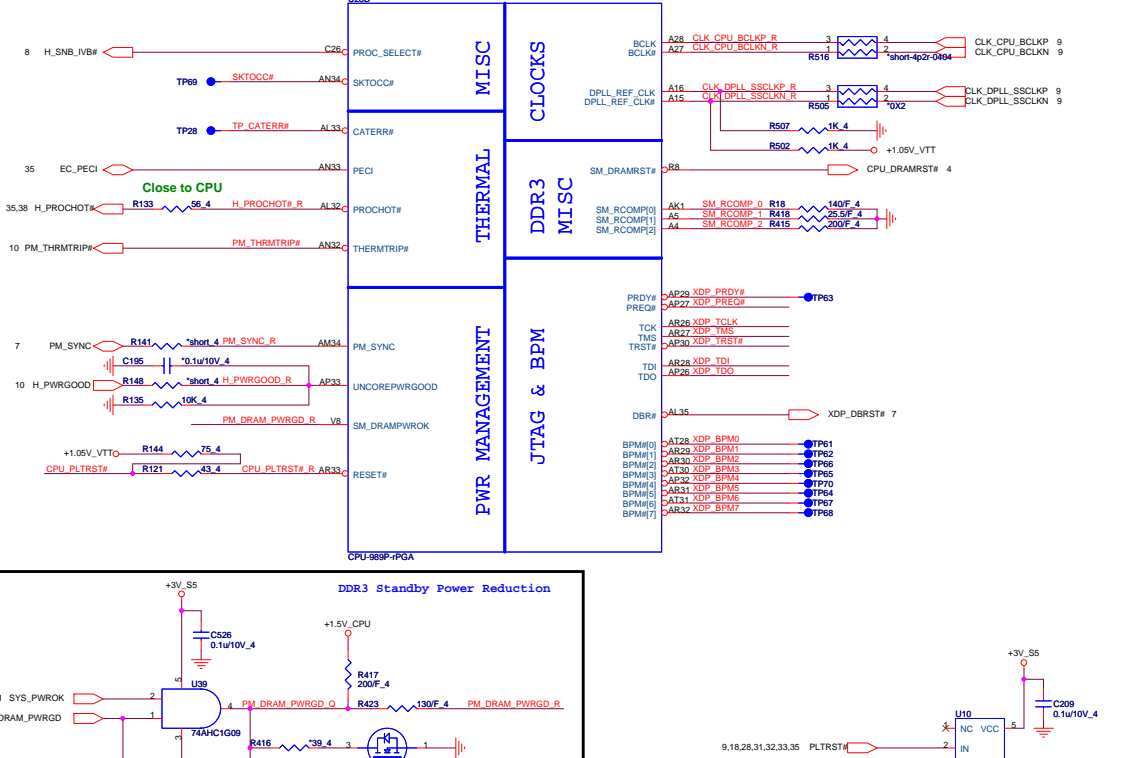
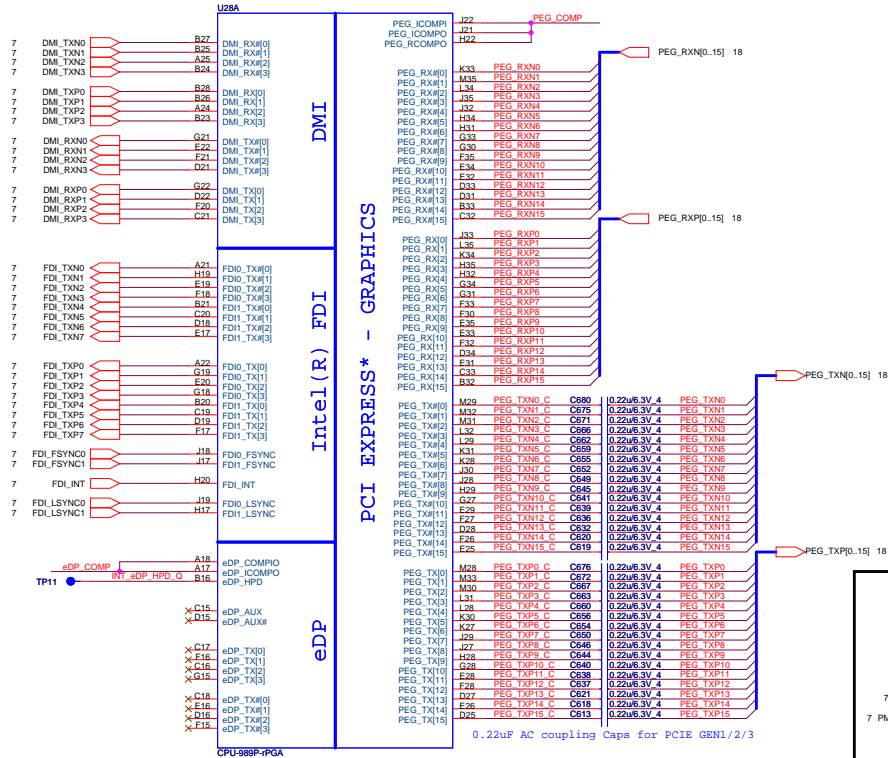
## Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	DDR3 RAM POWER	SUSON	S0-S3
+SMDDR_REF	+0.75V	SODIMM Reference Voltage	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/POWER	MAINON	S0
+1.8V	+1.8V	CPU/PCH POWER	MAINON	S0
+1.05V_S5	+1.05V	CPU/SODIMM CORE POWER	S5_ON	S0-S5
+1.05V_VTT	+1.05V	CPU VTT POWER	MAINON	S0
+1.05V_PCH	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
+VCC_GFX	variation	SNB GRAPHIC POWER	VR_ON	S0
+VCCSA	+0.8/0.9V	CPU SYSTEM ANAGENT AGENT	VTT_HWPG	S0
+1.05V_GFX	+1.05V	GPU IO/PLL POWER	dGPU_PWR_EN	Discrete enable
+3V_GFX	+3.3V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN	Discrete enable
+VGPU_CORE	+0.8125V~+1V	GPU CORE POWER	dGPU_VRON	Discrete enable
+1.5V_GFX	+1.5V	VRAM CORE POWER	VGA_PG	Discrete enable
+1.8V_GFX	+1.8V	GPU_CRE/LVDS/PLL POWER	VGA_PG	Discrete enable
+5V_ADO	+5V	AUDIO CODEC AMPLIFIER	MAINON	S0
+5V_DT	+5V	DT CHARGING	DT_CHG	TBD

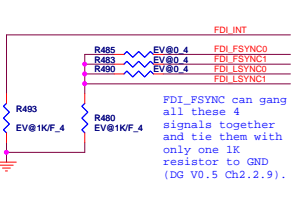


Dr-Bios.com

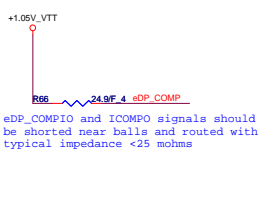
Sandy Bridge Processor (DMI,PEG,FDI)



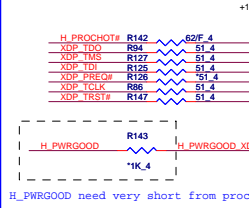
FDI Disabling (Discrete Only)



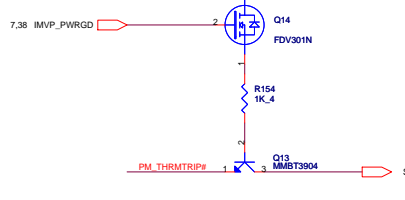
DP & PEG Compensation



Processor pull-up(CPU)

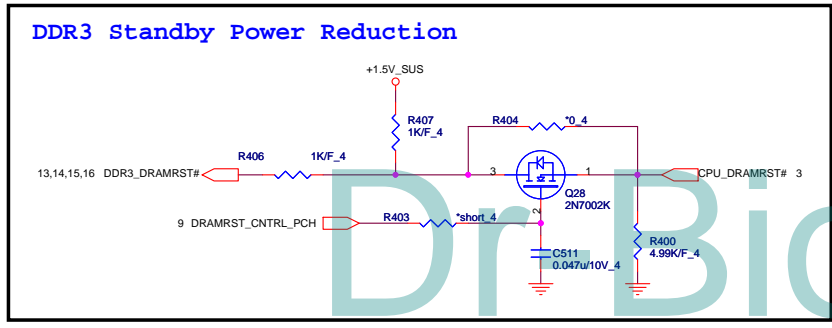
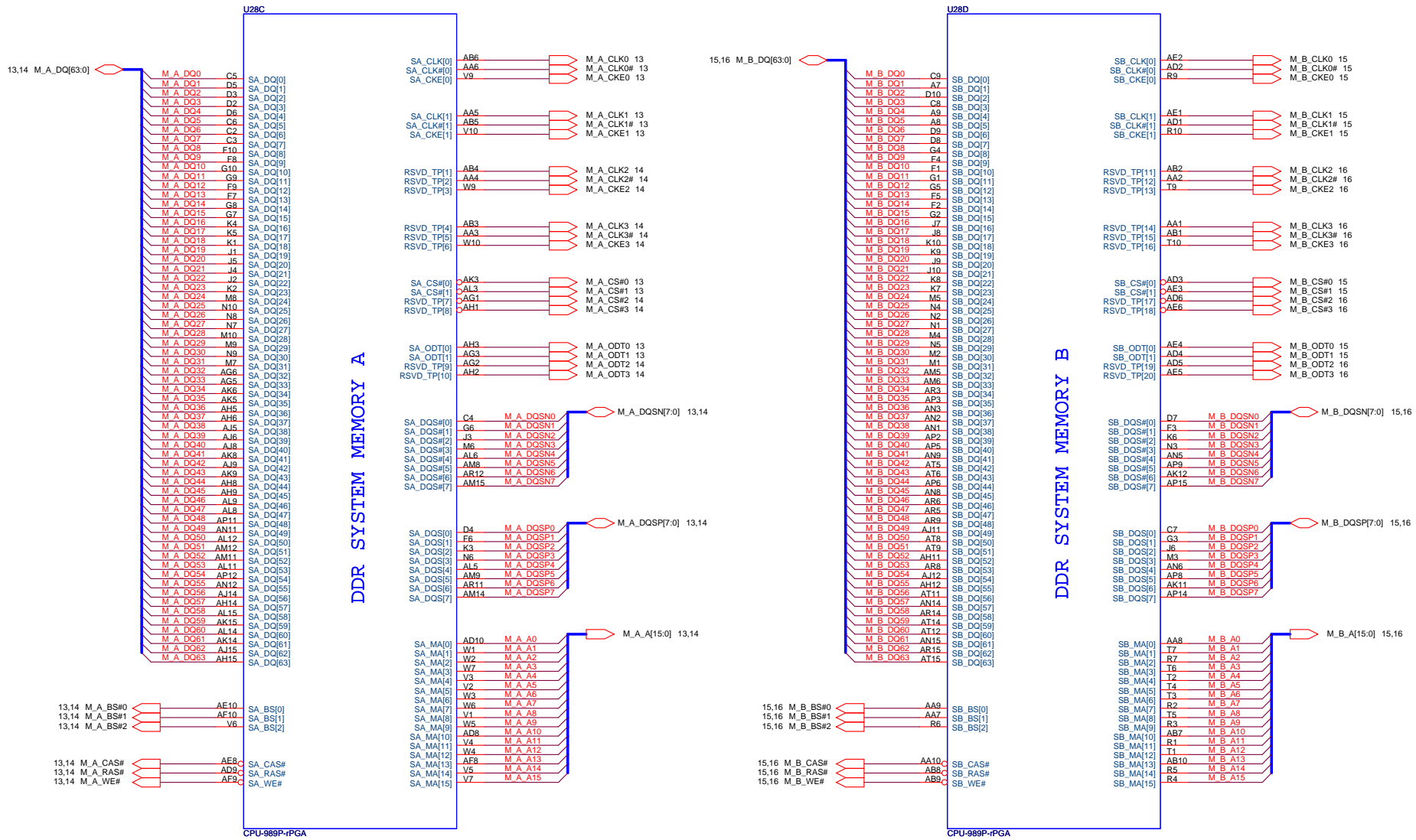


Processor pull-up(CPU)



**Quanta Computer Inc.**  
**PROJECT : ZYG**  
 Size Document Number **Sandy Bridge 1/4** Rev 1A  
 Date: Tuesday, February 22, 2011 Sheet 3 of 50

# Sandy Bridge Processor (DDR3)



**Quanta Computer Inc.**

**PROJECT : ZYG**

Size Document Number Rev  
 Date: Tuesday, February 22, 2011 Sheet 4 of 50

**Sandy Bridge 2/4**

1A

Sandy Bridge Processor (POWER)

CPU VTT SNB 45W : 8.5A

Spec 330uF/6mohm x 2  
Real 390uF/10mohm x 1  
22uF x 12  
22uF x 7 (Non-stuff)  
10uF x 3

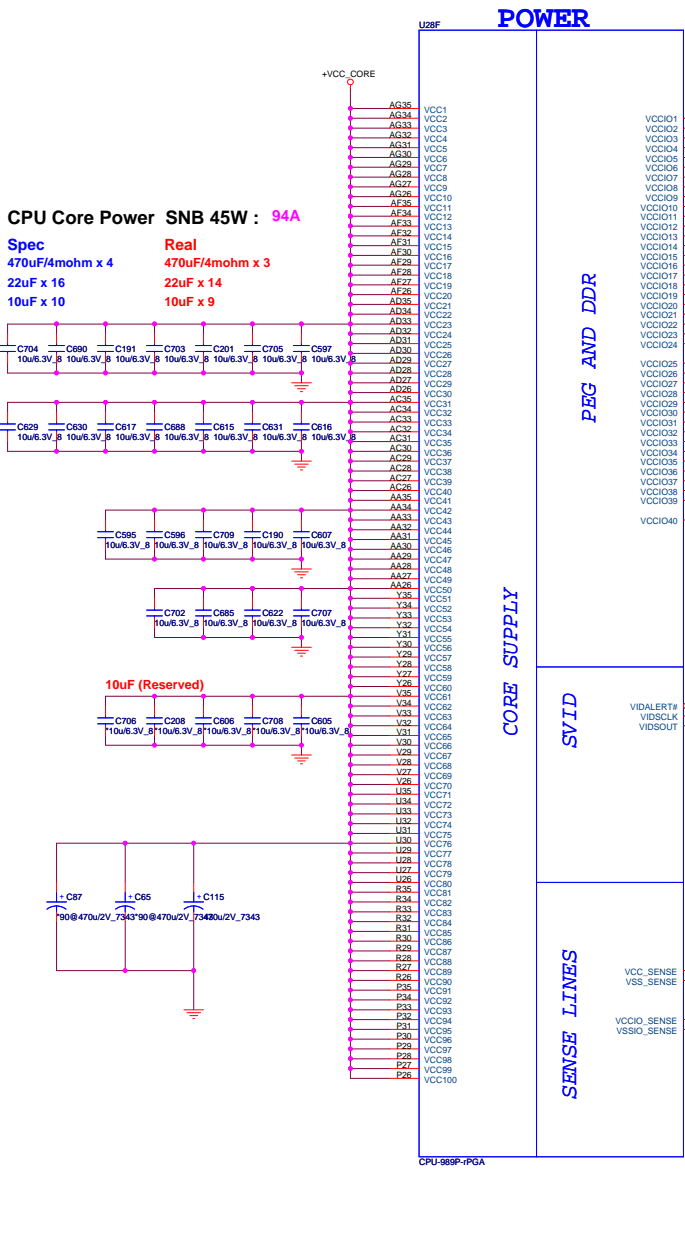
Spec 470uF/4mohm x 2  
Real 330uF/10mohm x 1  
22uF x 12  
22uF x 8  
10uF x 6

CPU VGT SNB 45W : 33A

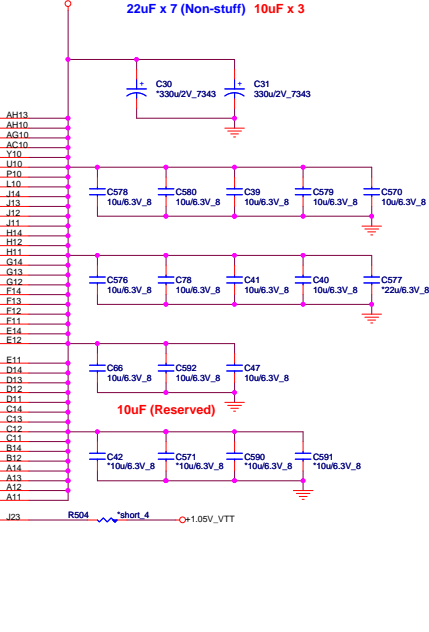
Spec 470uF/4mohm x 2  
Real 330uF/10mohm x 1  
22uF x 12  
22uF x 8  
10uF x 6

Sandy Bridge Processor (GRAPHIC POWER)

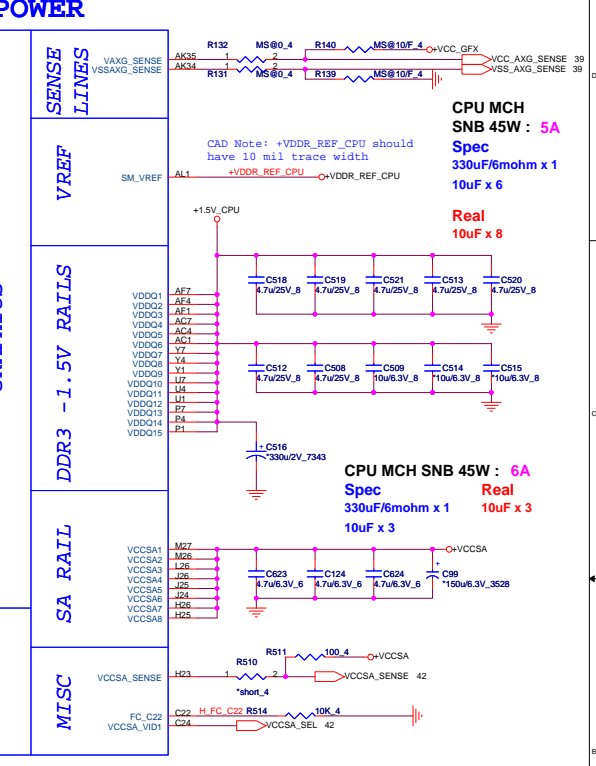
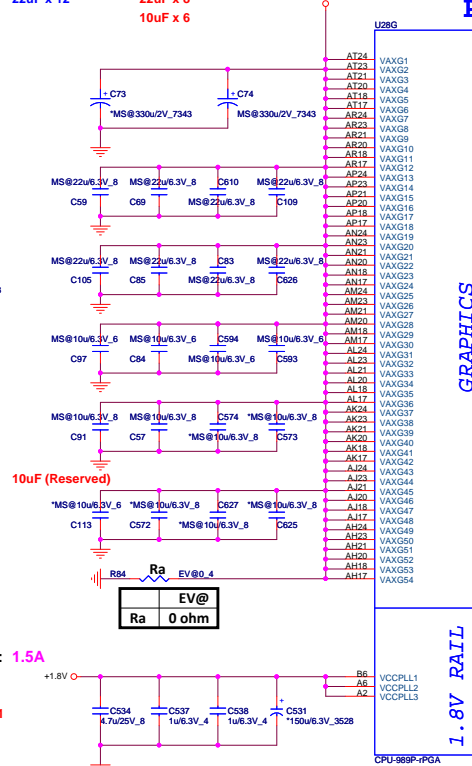
POWER



CPU Core Power SNB 45W : 94A  
Spec 470uF/4mohm x 4  
Real 470uF/4mohm x 3  
22uF x 16  
10uF x 10

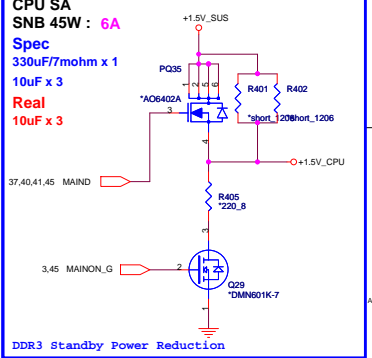
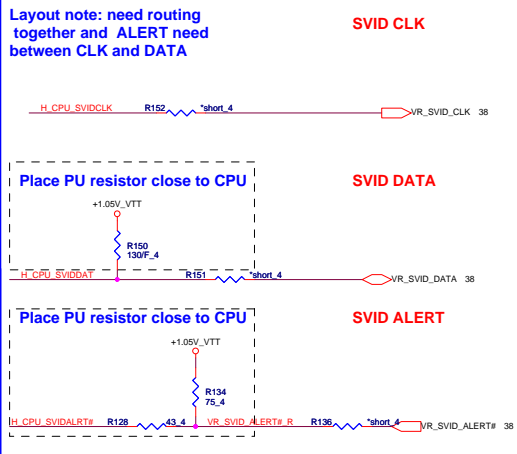


CPU VCCPL SNB 45W : 1.5A  
Spec 330uF/7mohm x 1  
Real 10uF x 1  
10uF x 1  
1uF x 2

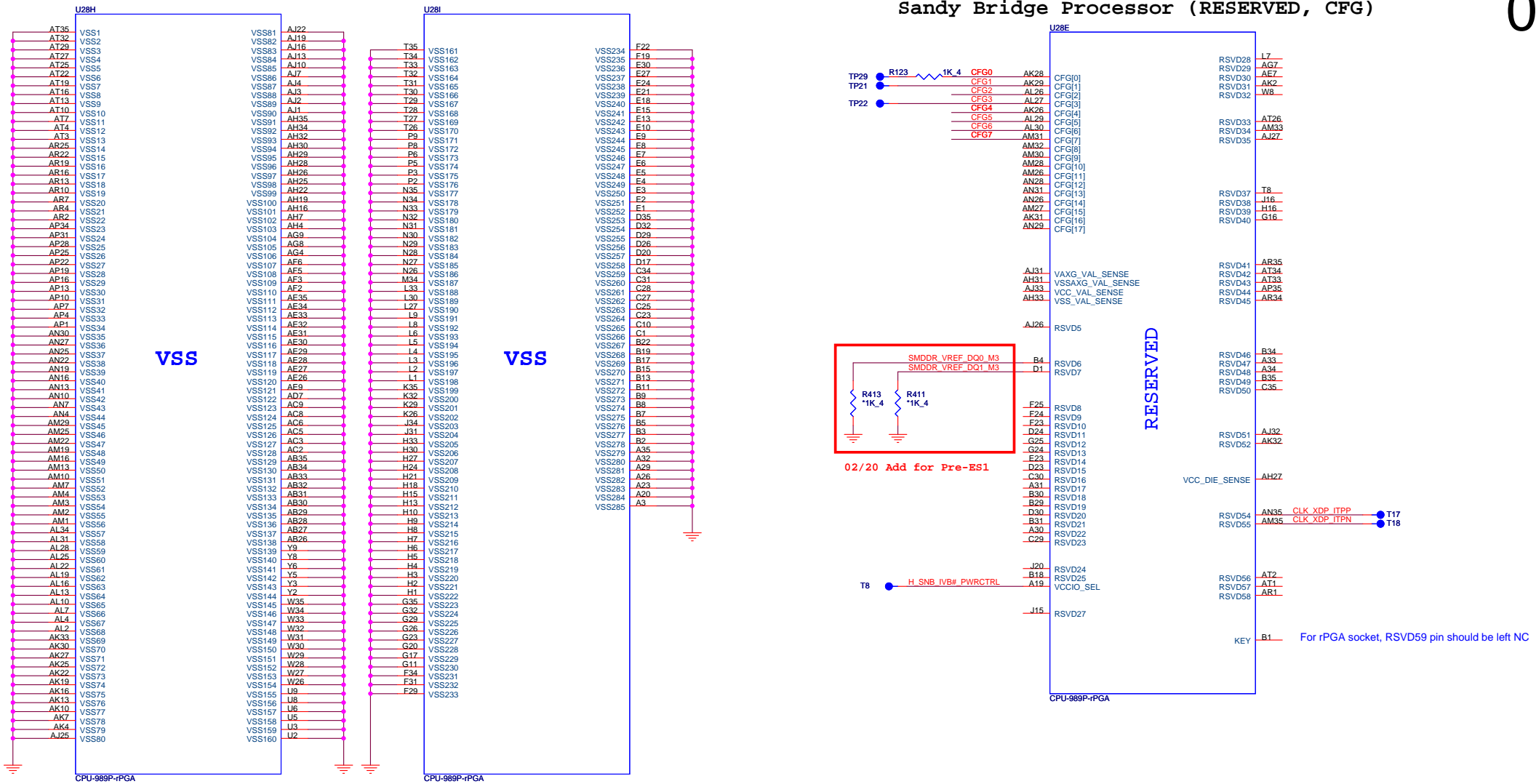


CPU MCH SNB 45W : 5A  
Spec 330uF/6mohm x 1  
Real 10uF x 8

CPU MCH SNB 45W : 6A  
Spec 330uF/6mohm x 1  
Real 10uF x 3



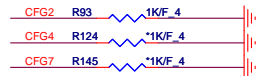
Quanta Computer Inc.  
PROJECT : ZYG  
Sandy Bridge 3/4  
Size Document Number Rev 1A  
Date: Tuesday, February 22, 2011 Sheet 5 of 50



**Processor Strapping**

The CFG signals have a default value of '1' if not terminated on the board.

CFG	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



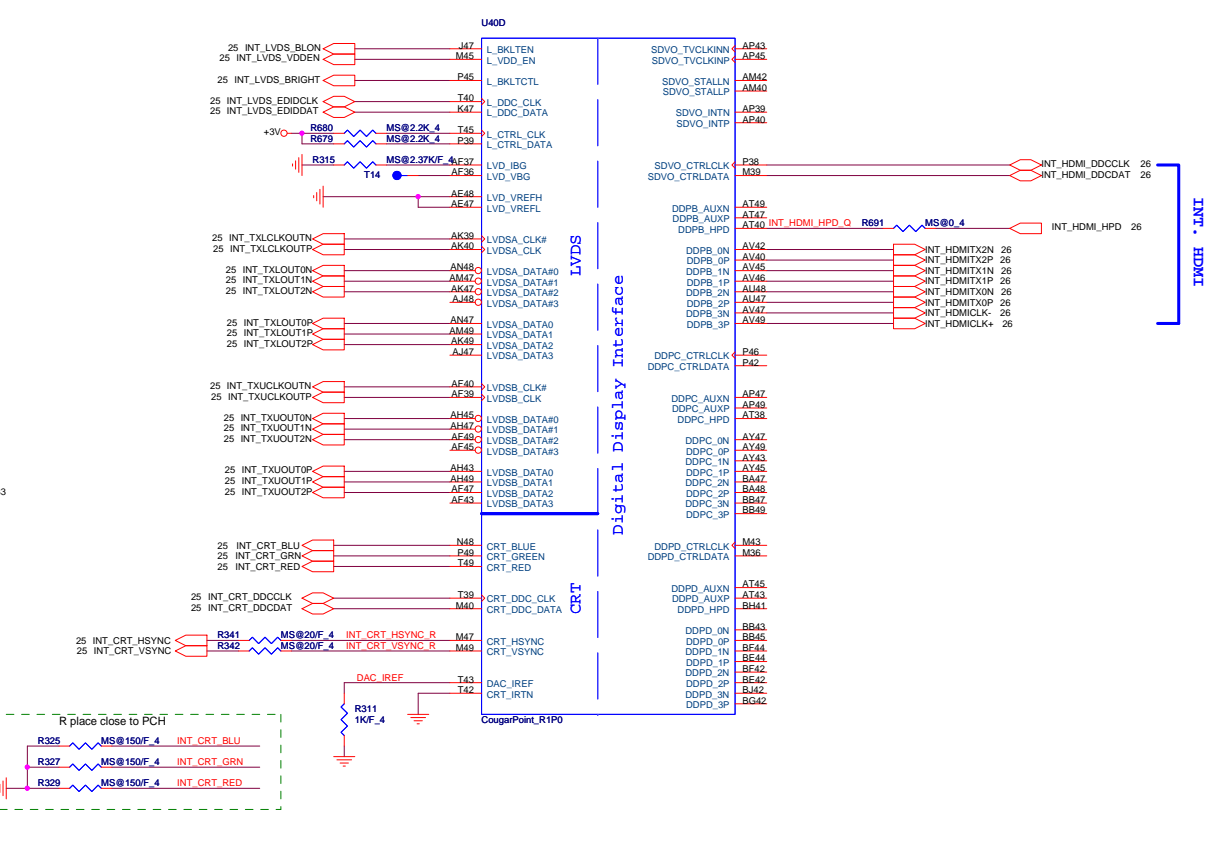
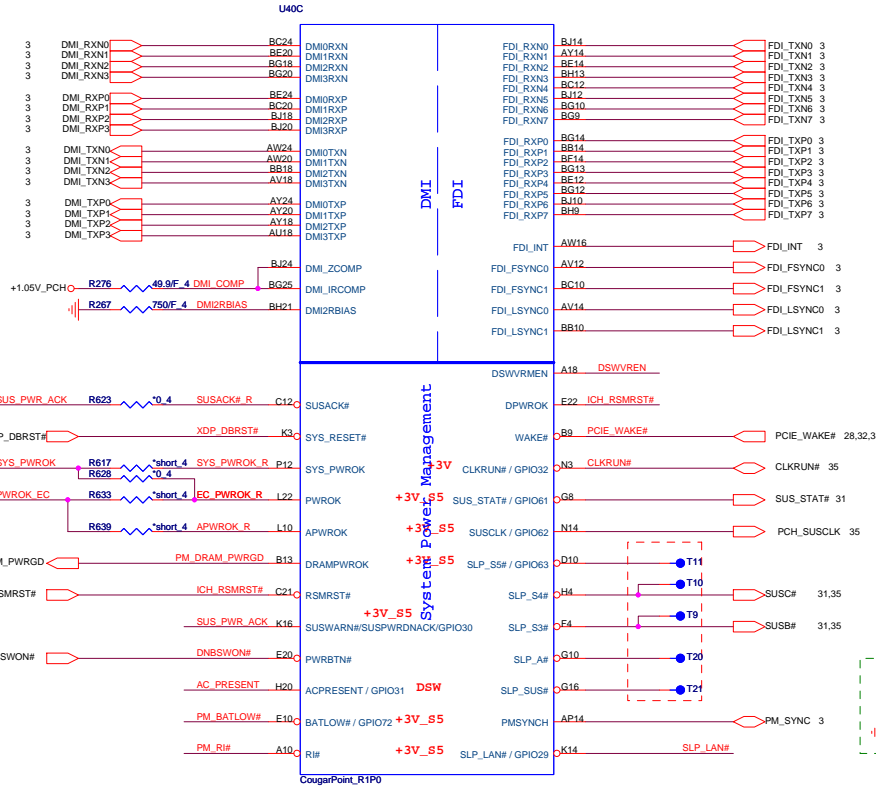
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

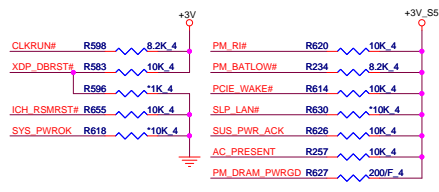
**Quanta Computer Inc.**  
**PROJECT : ZYG**

Size: Document Number: Rev 1A  
**Sandy Bridge 4/4**  
 Date: Monday, January 24, 2011 Sheet 6 of 50

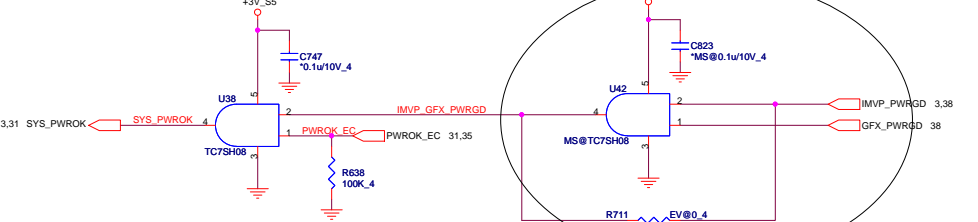
Cougar Point (DMI,FDI,PM)



PCH Pull-high/low(CLG)



System PWR\_OK(CLG)



12/6 Add this for SYS\_PWROK logic

**On Die DSW VR Enable**

- High = Enable (Default)
- Low = Disable

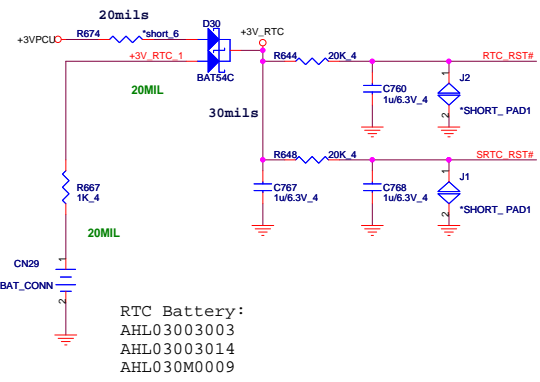
**Quanta Computer Inc.**

**PROJECT : ZYG**

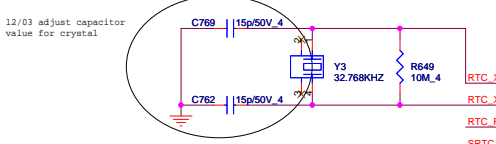
Size Document Number **Cougar Point 1/6** Rev 1A

Date: Tuesday, February 22, 2011 Sheet 7 of 50

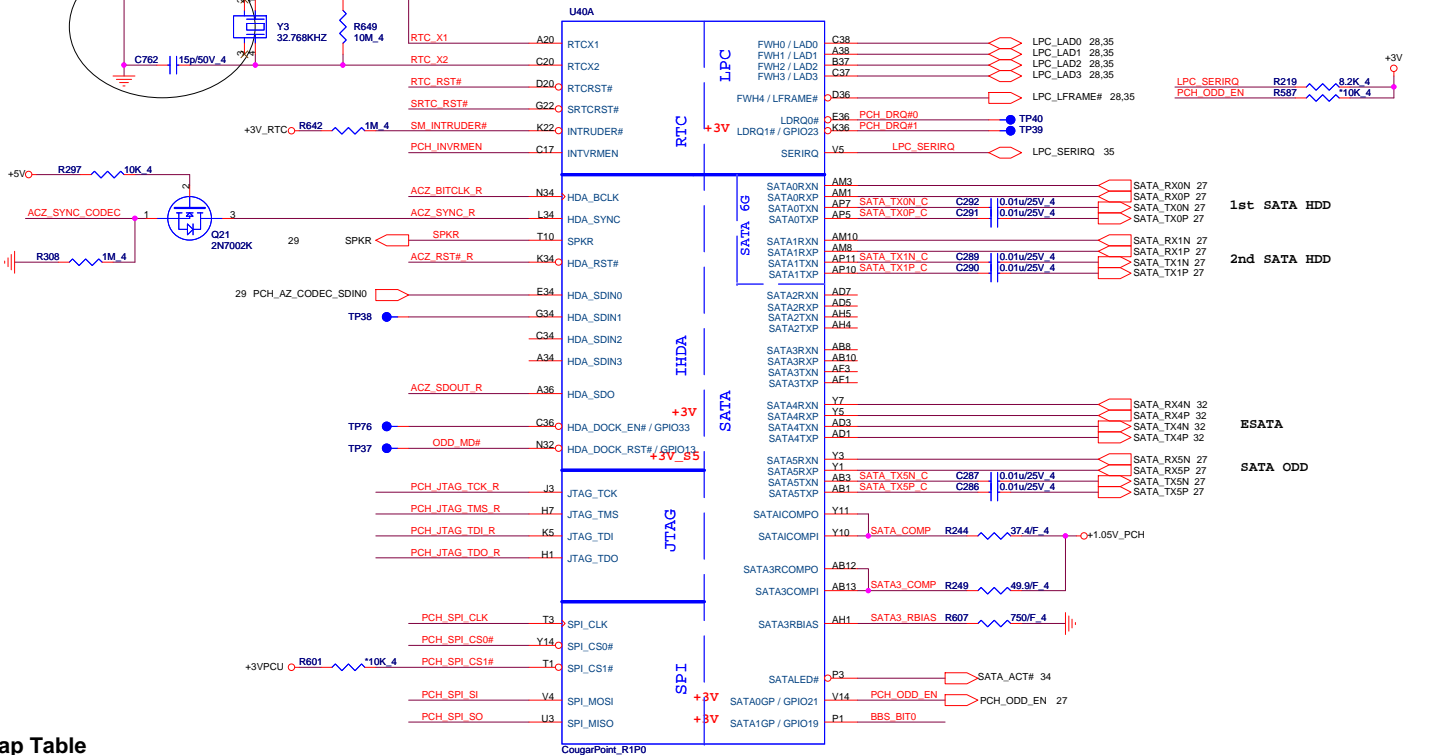
RTC Circuitry(RTC)



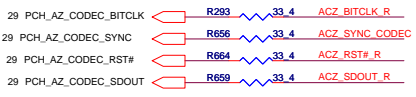
PCH2 ( CLG )



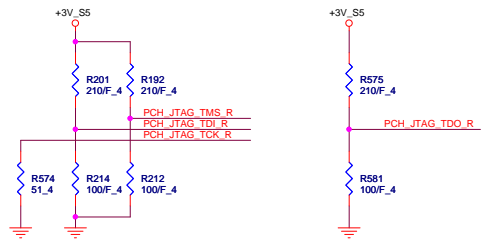
Cougar Point (HDA,JTAG,SATA)



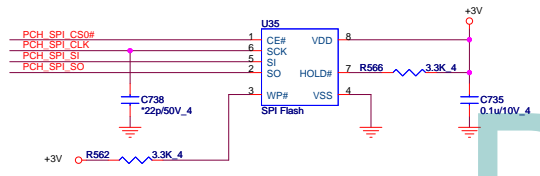
HDA Bus(CLG)



PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

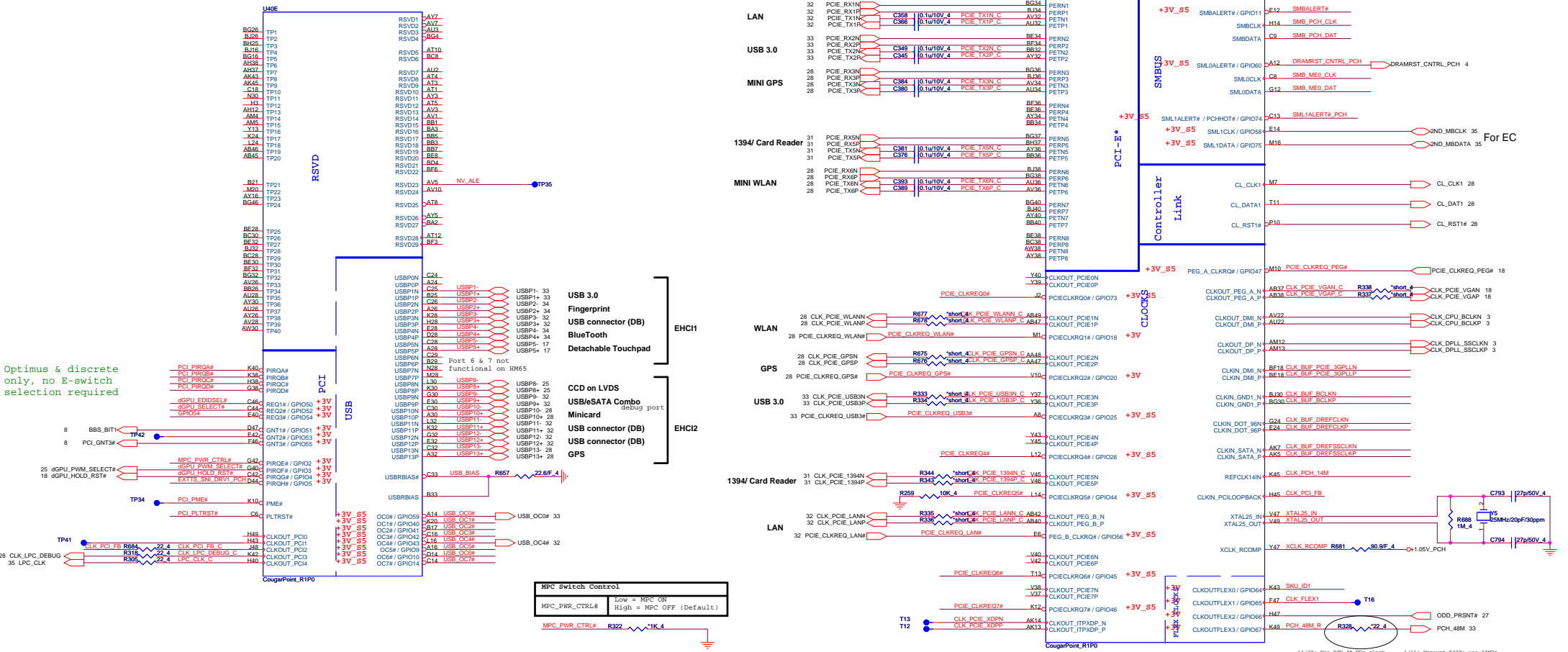


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_ R198 *1K_4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R672 *1K_4 PCI_GNT3# 9									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC_ R643 *330K_4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] R673 *1K_4 BBS_BIT1 9 R600 *1K_4 BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	ME_WR# R660 *short_4 ACZ_SDOUT_R									
DF_TV5	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R606 2.2K_4 O+1.8V R608 *1K_4 DF_TV5 10 H_SNB_IVB# 3									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R625 *1K_4 PLL_ODVR_EN 10									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5_ R296 *1K_4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	Need check schematic									
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										



Cougar Point-M (PCI,USB,NVRAM)

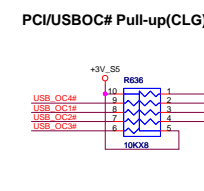
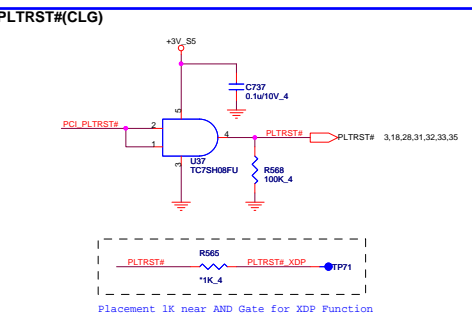


Optimize & discrete only, no E-switch selection required

**MPC Switch Control**

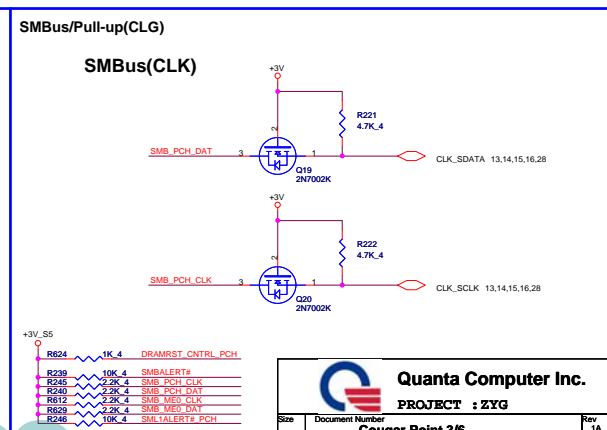
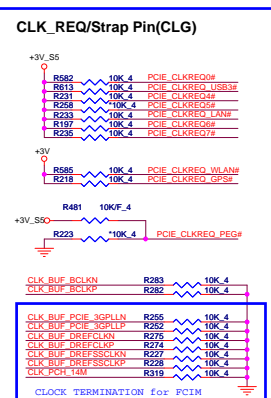
Low = MPC ON  
High = MPC OFF (Default)

MPC\_PWR\_CTRL# R322 \*1K.4



	GPU_PWR_CTRL# (GPIO6)	SKU_ID1 (GPIO1)	SKU_ID0 (GPIO2)	SKU_ID2 (GPIO3)	Setup Menu	
UMA Only	1	0	0	0	UMA	Hidden
Discrete Only	0 or 1	0	1	0	GPU	Hidden
Switchable	0	1	0	0	UMA-GPU	Discrete/SG
Optimize (Muxless)	0	1	1	1	UMA	UMA/SG

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)  
1 = GPU power is control by MW (pure Discrete SKU)



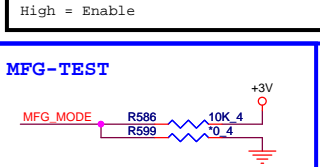
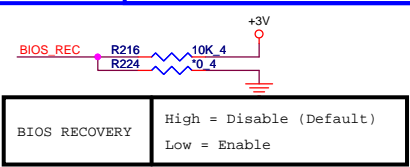
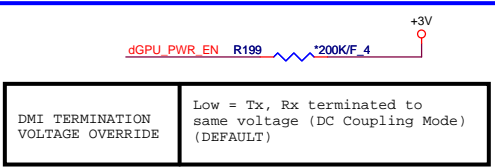
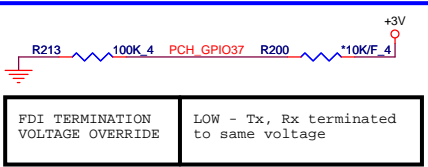
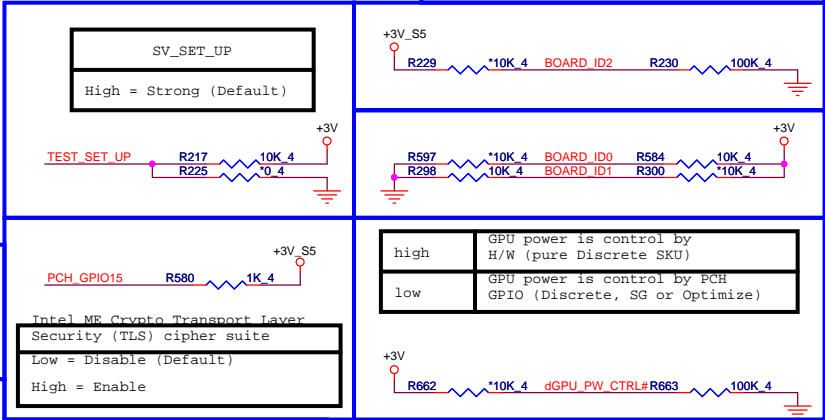
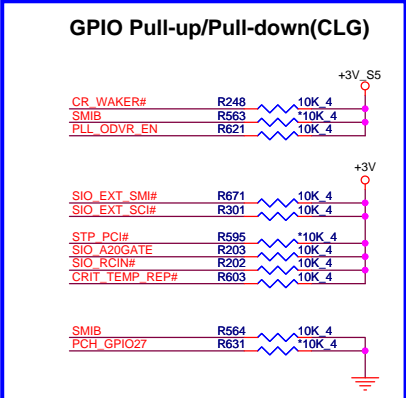
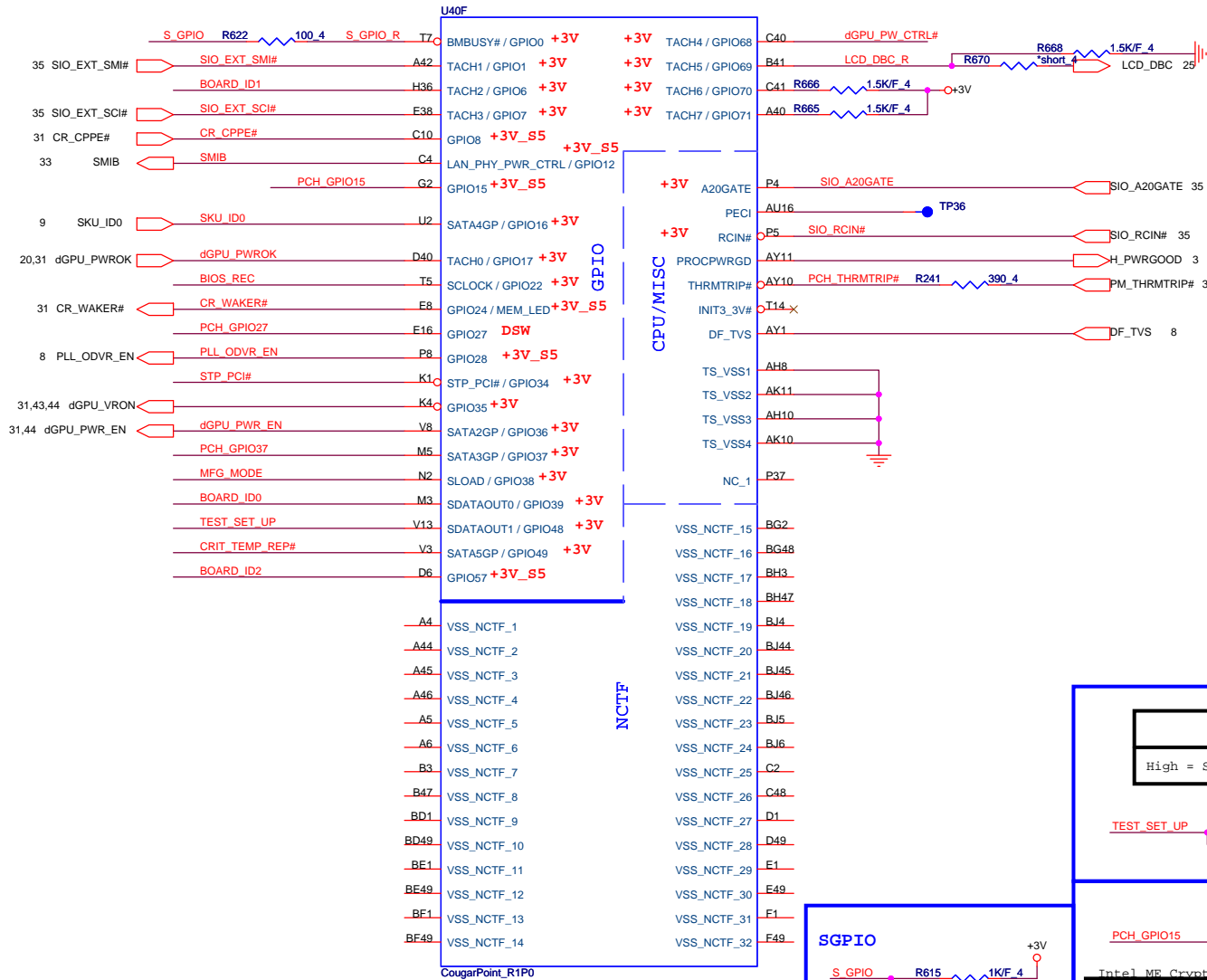
**Quanta Computer Inc.**

**PROJECT : ZYG**

Size Document Number Cougar Point 3/6 Rev 1A

Date: Tuesday, February 22, 2011 Sheet 9 of 30

### Cougar Point (GPIO,VSS\_NCTF,RSVD)



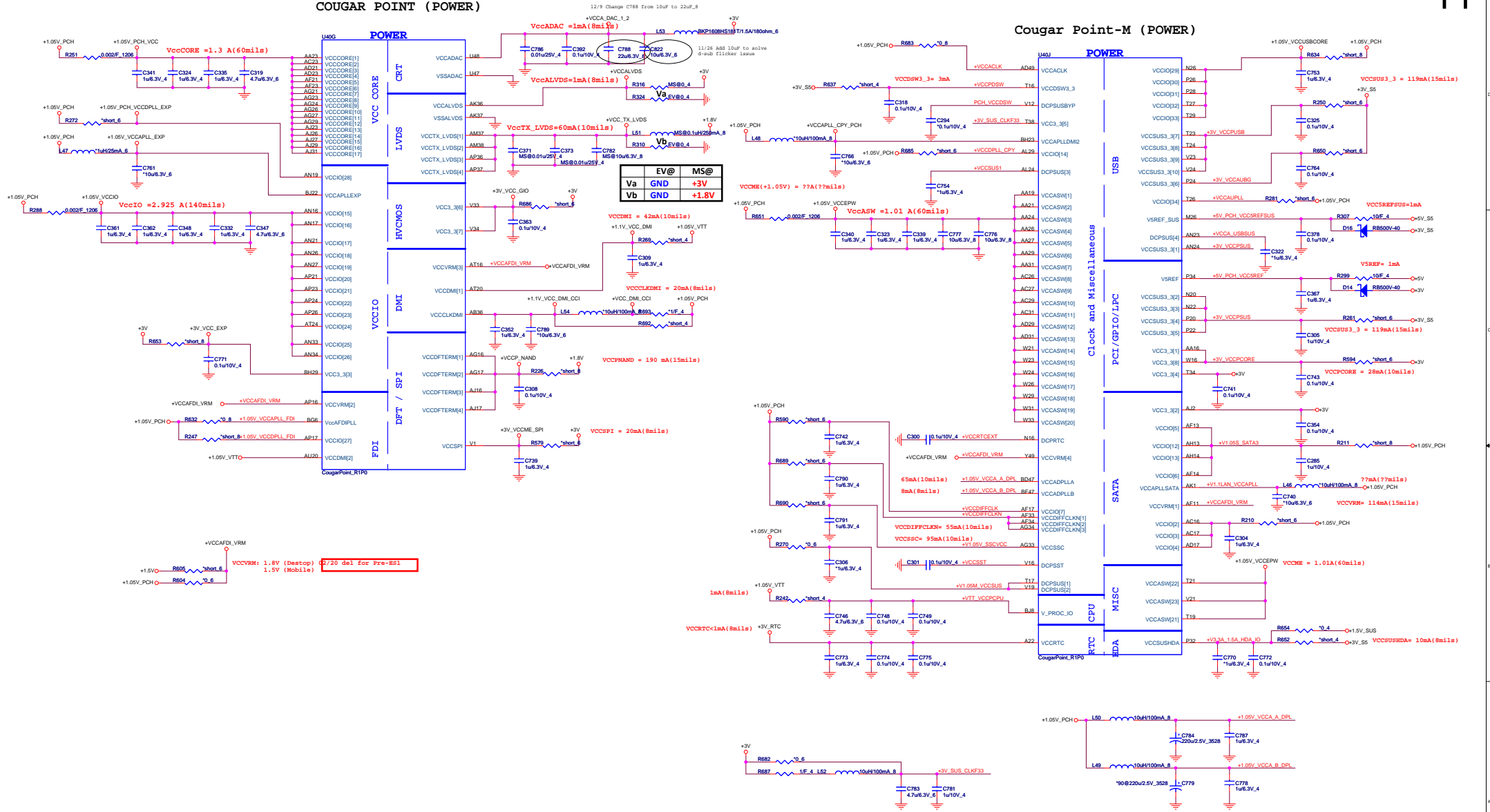
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PROJECT : ZYG

Size	Document Number	Rev
	<b>Cougar Point 4/6</b>	1A

Date: Tuesday, February 22, 2011 Sheet 10 of 50

COUGAR POINT (POWER)

Cougar Point-M (POWER)



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 PROJECT : ZYG  
**Cougar Point 5/6**  
 Date: Wednesday, February 23, 2011 Sheet 11 of 50

IBEX PEAK-M (GND)

U40H

H5	VSS[0]
AA17	VSS[1]
AA2	VSS[2]
AA3	VSS[3]
AA33	VSS[4]
AA34	VSS[5]
AB11	VSS[6]
AB15	VSS[7]
AB4	VSS[8]
AB43	VSS[9]
AB5	VSS[10]
AB7	VSS[11]
AC19	VSS[12]
AC2	VSS[13]
AC21	VSS[14]
AC24	VSS[15]
AC33	VSS[16]
AC34	VSS[17]
AC48	VSS[18]
AD10	VSS[19]
AD11	VSS[20]
AD12	VSS[21]
AD13	VSS[22]
AD19	VSS[23]
AD24	VSS[24]
AD26	VSS[25]
AD27	VSS[26]
AD33	VSS[27]
AD34	VSS[28]
AD36	VSS[29]
AD37	VSS[30]
AD38	VSS[31]
AD39	VSS[32]
AD4	VSS[33]
AD41	VSS[34]
AD42	VSS[35]
AD43	VSS[36]
AD44	VSS[37]
AD45	VSS[38]
AD46	VSS[39]
AD8	VSS[40]
AE2	VSS[41]
AE3	VSS[42]
AF10	VSS[43]
AF12	VSS[44]
AD14	VSS[45]
AD16	VSS[46]
AF16	VSS[47]
AF19	VSS[48]
AF24	VSS[49]
AF26	VSS[50]
AF27	VSS[51]
AF29	VSS[52]
AF31	VSS[53]
AF38	VSS[54]
AE4	VSS[55]
AF42	VSS[56]
AF46	VSS[57]
AF5	VSS[58]
AF7	VSS[59]
AF8	VSS[60]
AG19	VSS[61]
AG2	VSS[62]
AG31	VSS[63]
AG48	VSS[64]
AH11	VSS[65]
AH3	VSS[66]
AH38	VSS[67]
AH39	VSS[68]
AH40	VSS[69]
AH42	VSS[70]
AH46	VSS[71]
AH7	VSS[72]
AJ19	VSS[73]
AJ21	VSS[74]
AJ24	VSS[75]
AJ33	VSS[76]
AJ34	VSS[77]
AK12	VSS[78]
AK3	VSS[79]

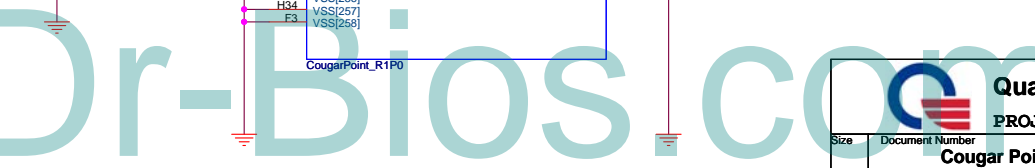
CougarPoint\_R1P0

U40I

AY4	VSS[159]
AY42	VSS[160]
AY46	VSS[161]
AY8	VSS[162]
B11	VSS[163]
B15	VSS[164]
B19	VSS[165]
B23	VSS[166]
B27	VSS[167]
B31	VSS[168]
B35	VSS[169]
B39	VSS[170]
B7	VSS[171]
F46	VSS[172]
BB12	VSS[173]
BB16	VSS[174]
BB20	VSS[175]
BB22	VSS[176]
BB24	VSS[177]
BB28	VSS[178]
BB30	VSS[179]
BB38	VSS[180]
BB4	VSS[181]
BB46	VSS[182]
BC14	VSS[183]
BC18	VSS[184]
BC22	VSS[185]
BC26	VSS[186]
BC32	VSS[187]
BC34	VSS[188]
BC36	VSS[189]
BC40	VSS[190]
BC42	VSS[191]
BC48	VSS[192]
BD46	VSS[194]
BD5	VSS[195]
BE22	VSS[196]
BE26	VSS[197]
BE40	VSS[198]
BE10	VSS[199]
BF12	VSS[200]
BF16	VSS[201]
BF20	VSS[202]
BF22	VSS[203]
BF24	VSS[204]
BF26	VSS[205]
BF28	VSS[206]
BD3	VSS[207]
BF30	VSS[208]
BF38	VSS[209]
BF40	VSS[210]
BF8	VSS[211]
BG17	VSS[212]
BG21	VSS[213]
BG33	VSS[214]
BG44	VSS[215]
BG8	VSS[216]
BH11	VSS[217]
BH15	VSS[218]
BH17	VSS[219]
BH19	VSS[220]
H10	VSS[221]
BH27	VSS[222]
BH31	VSS[223]
BH33	VSS[224]
BH35	VSS[225]
BH39	VSS[226]
BH43	VSS[227]
BH7	VSS[228]
D3	VSS[229]
D12	VSS[230]
D16	VSS[231]
D18	VSS[232]
D22	VSS[233]
D24	VSS[234]
D26	VSS[235]
D30	VSS[236]
D32	VSS[237]
D34	VSS[238]
D38	VSS[239]
D42	VSS[240]
DR	VSS[241]
AW22	VSS[242]
E18	VSS[243]
E28	VSS[244]
G18	VSS[245]
G20	VSS[246]
G26	VSS[247]
G28	VSS[248]
G36	VSS[249]
G48	VSS[250]
H12	VSS[251]
H16	VSS[252]
H22	VSS[253]
H24	VSS[254]
H26	VSS[255]
H30	VSS[256]
H32	VSS[257]
H34	VSS[258]
F3	VSS[259]

VSS[259]	H46
VSS[260]	K18
VSS[261]	K26
VSS[262]	K38
VSS[263]	K46
VSS[264]	K7
VSS[265]	L18
VSS[266]	L2
VSS[267]	L20
VSS[268]	L26
VSS[269]	L28
VSS[270]	L36
VSS[271]	L48
VSS[272]	M12
VSS[273]	P16
VSS[274]	M18
VSS[275]	M22
VSS[276]	M24
VSS[277]	M32
VSS[278]	M34
VSS[279]	M38
VSS[280]	M4
VSS[281]	M42
VSS[282]	M46
VSS[283]	M8
VSS[284]	N18
VSS[285]	P30
VSS[286]	N47
VSS[287]	P11
VSS[288]	P18
VSS[289]	T33
VSS[290]	P40
VSS[291]	P43
VSS[292]	P47
VSS[293]	P7
VSS[294]	R2
VSS[295]	R48
VSS[296]	T12
VSS[297]	T31
VSS[298]	T37
VSS[299]	T47
VSS[300]	W34
VSS[301]	T46
VSS[302]	T4
VSS[303]	T7
VSS[304]	V17
VSS[305]	V19
VSS[306]	V26
VSS[307]	V27
VSS[308]	V29
VSS[309]	V31
VSS[310]	V36
VSS[311]	V39
VSS[312]	V43
VSS[313]	W7
VSS[314]	W17
VSS[315]	W19
VSS[316]	W2
VSS[317]	W27
VSS[318]	W48
VSS[319]	Y12
VSS[320]	Y38
VSS[321]	Y4
VSS[322]	Y42
VSS[323]	Y46
VSS[324]	Y8
VSS[325]	BG29
VSS[326]	N24
VSS[327]	AJ3
VSS[328]	AD47
VSS[329]	B43
VSS[330]	BE10
VSS[331]	BG41
VSS[332]	G14
VSS[333]	H16
VSS[334]	T36
VSS[335]	BG22
VSS[336]	BG24
VSS[337]	C22
VSS[338]	AP13
VSS[339]	M14
VSS[340]	AP3
VSS[341]	AP1
VSS[342]	BE16
VSS[343]	BC16
VSS[344]	BC28
VSS[345]	BJ28
VSS[346]	
VSS[347]	
VSS[348]	
VSS[349]	
VSS[350]	
VSS[351]	
VSS[352]	

CougarPoint\_R1P0



**Quanta Computer Inc.**  
PROJECT : ZYG

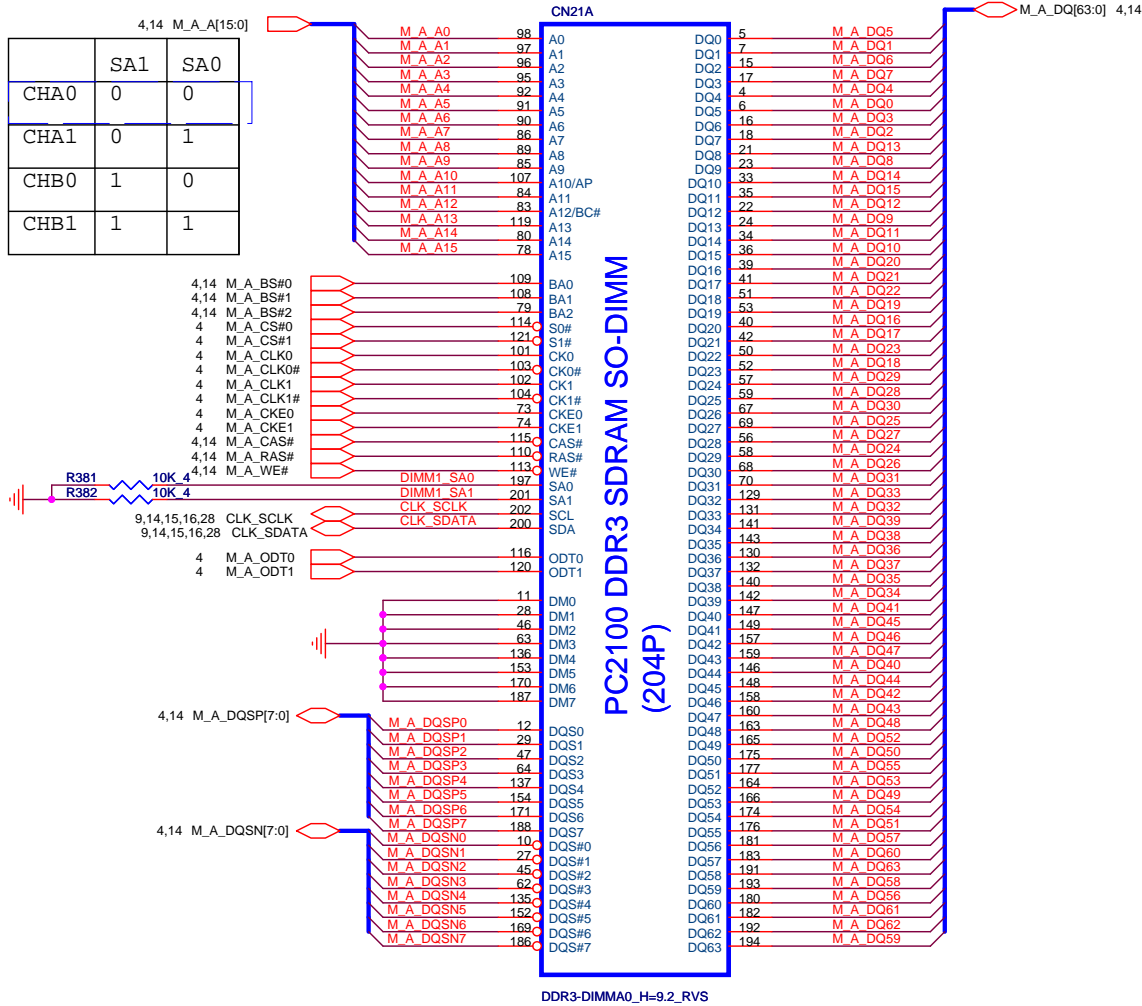
Cougar Point 6/6

Size Document Number Rev 1A

Date: Monday, February 14, 2011 Sheet 12 of 50

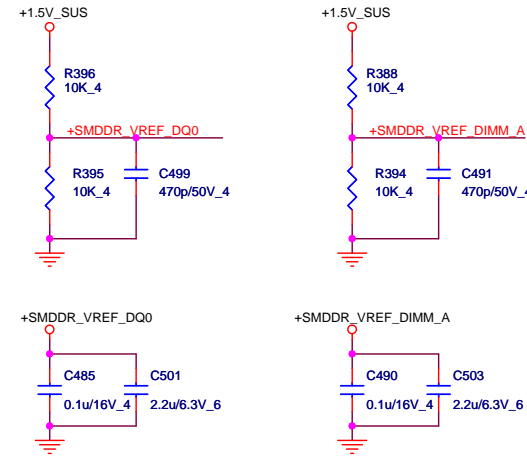
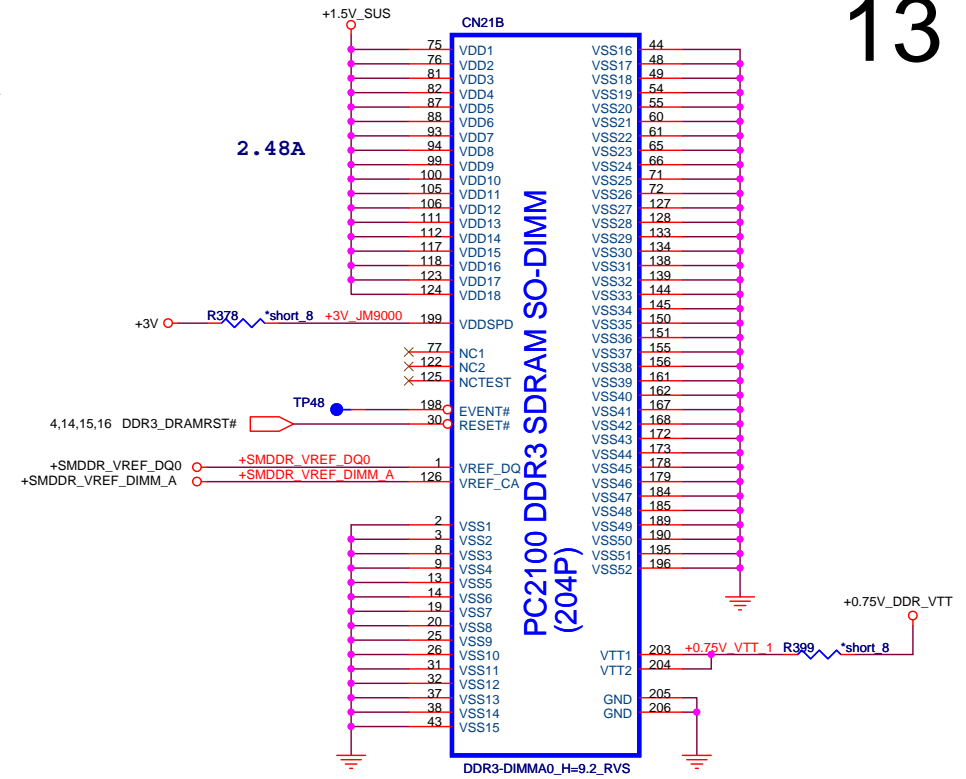
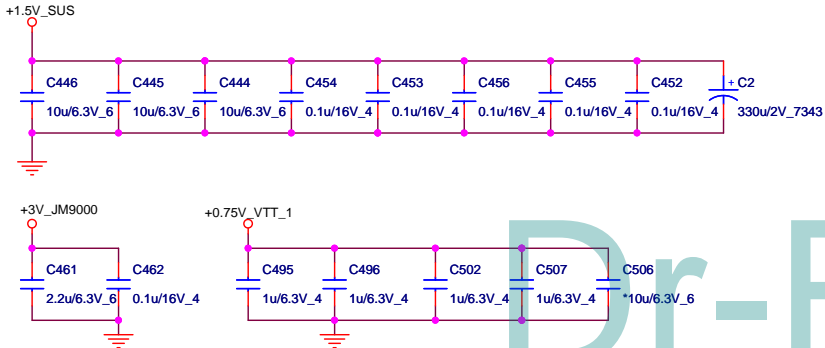
DDR3 DIMM-A0

CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

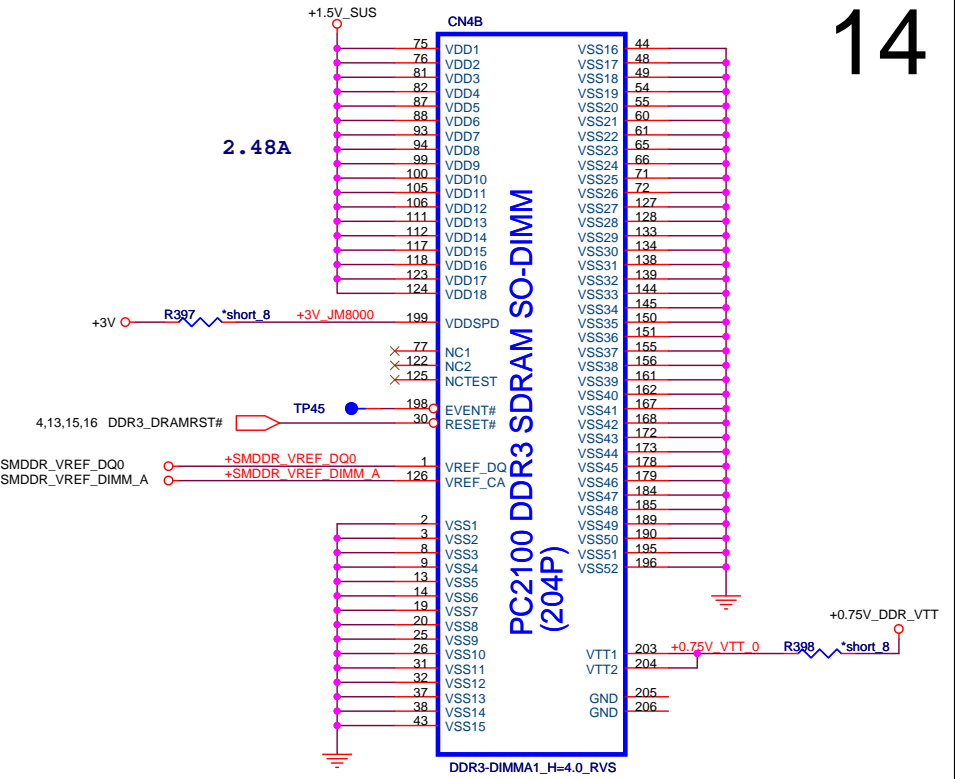
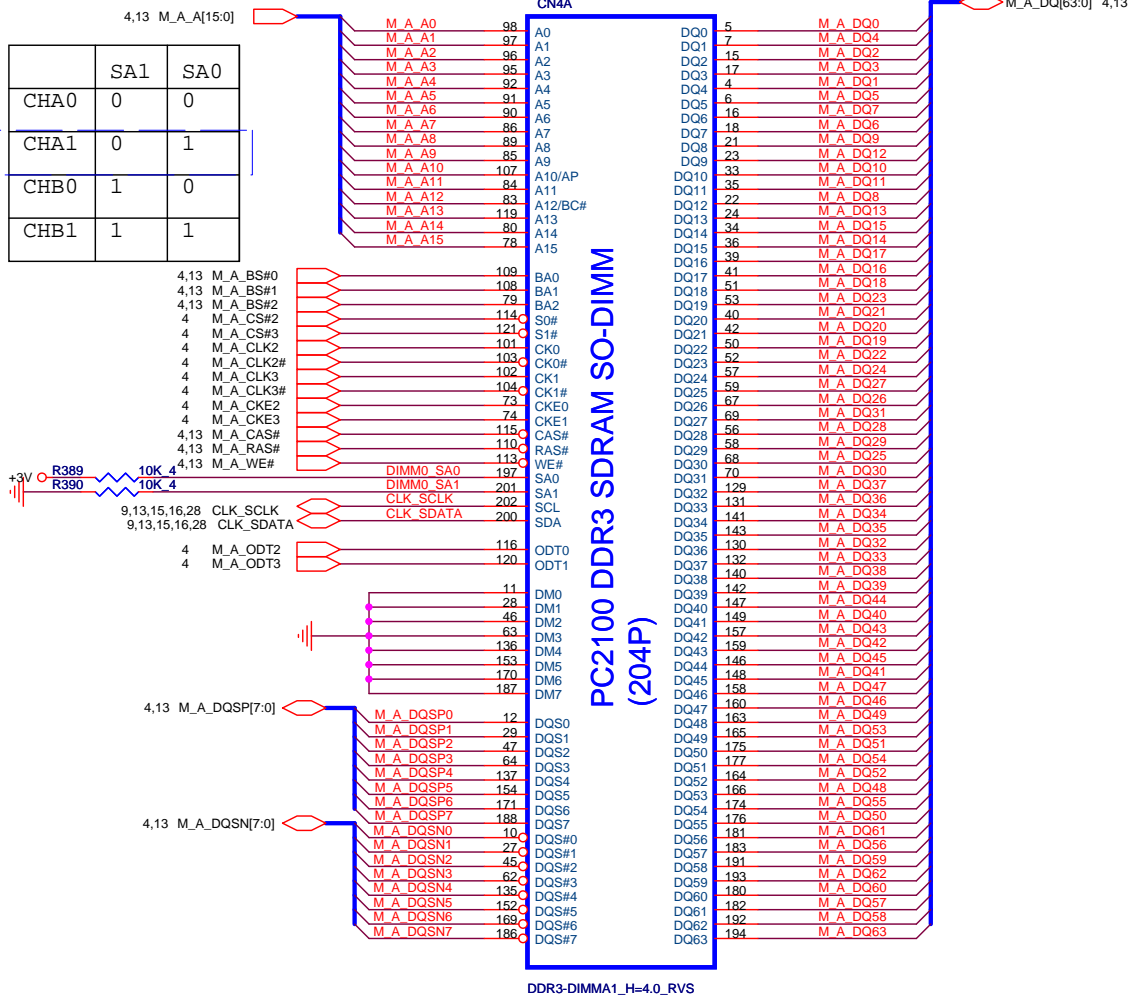


DDR3-DIMMA0\_H=9.2\_RVS

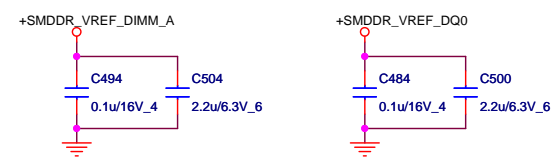
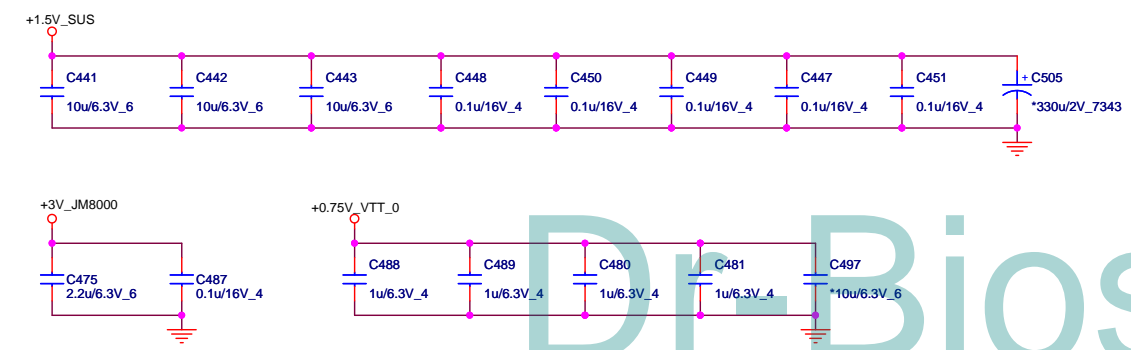
Place these Caps near So-Dimm0.



# DDR3 DIMM-A1

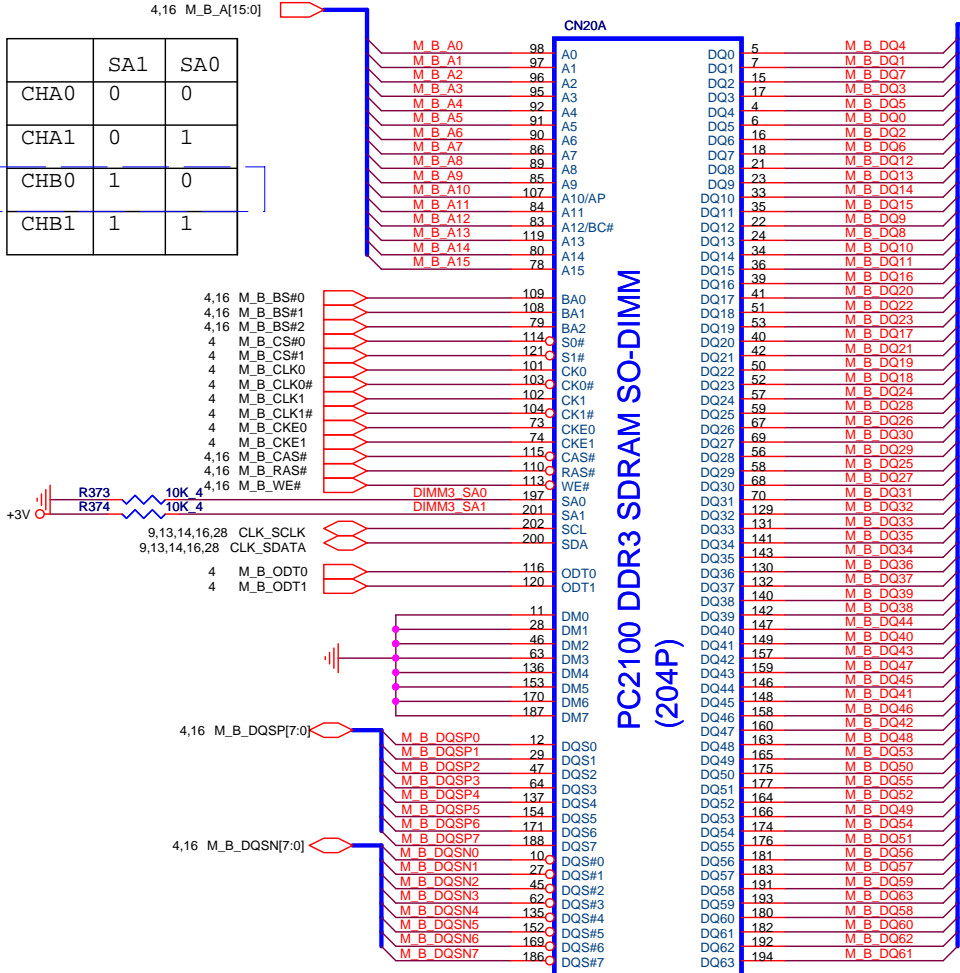


Place these Caps near So-Dimm0.



DDR3 DIMM-B0

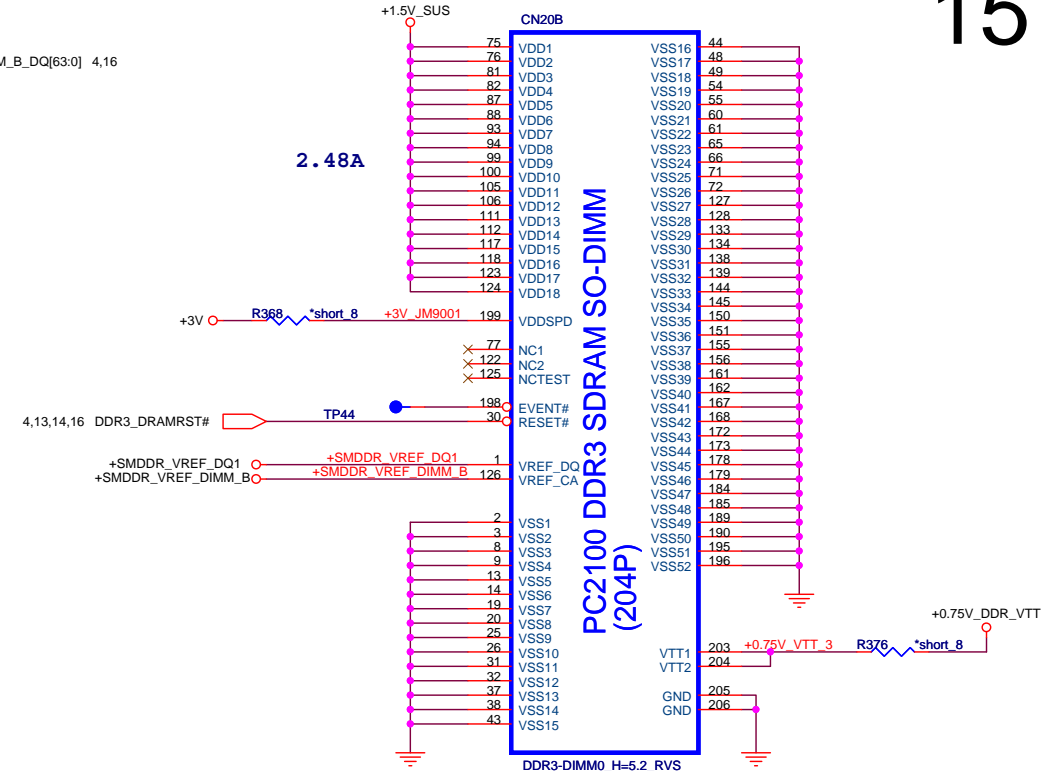
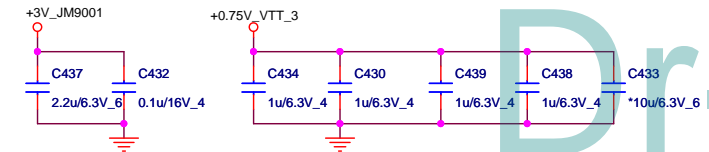
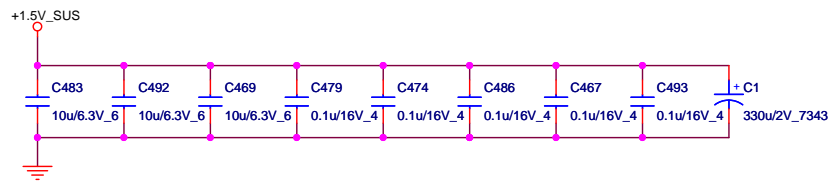
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



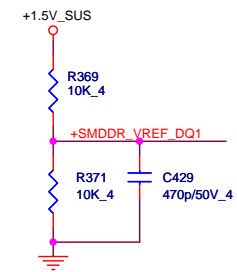
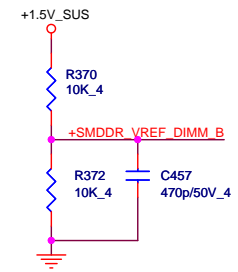
PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0\_H=5.2\_RVS

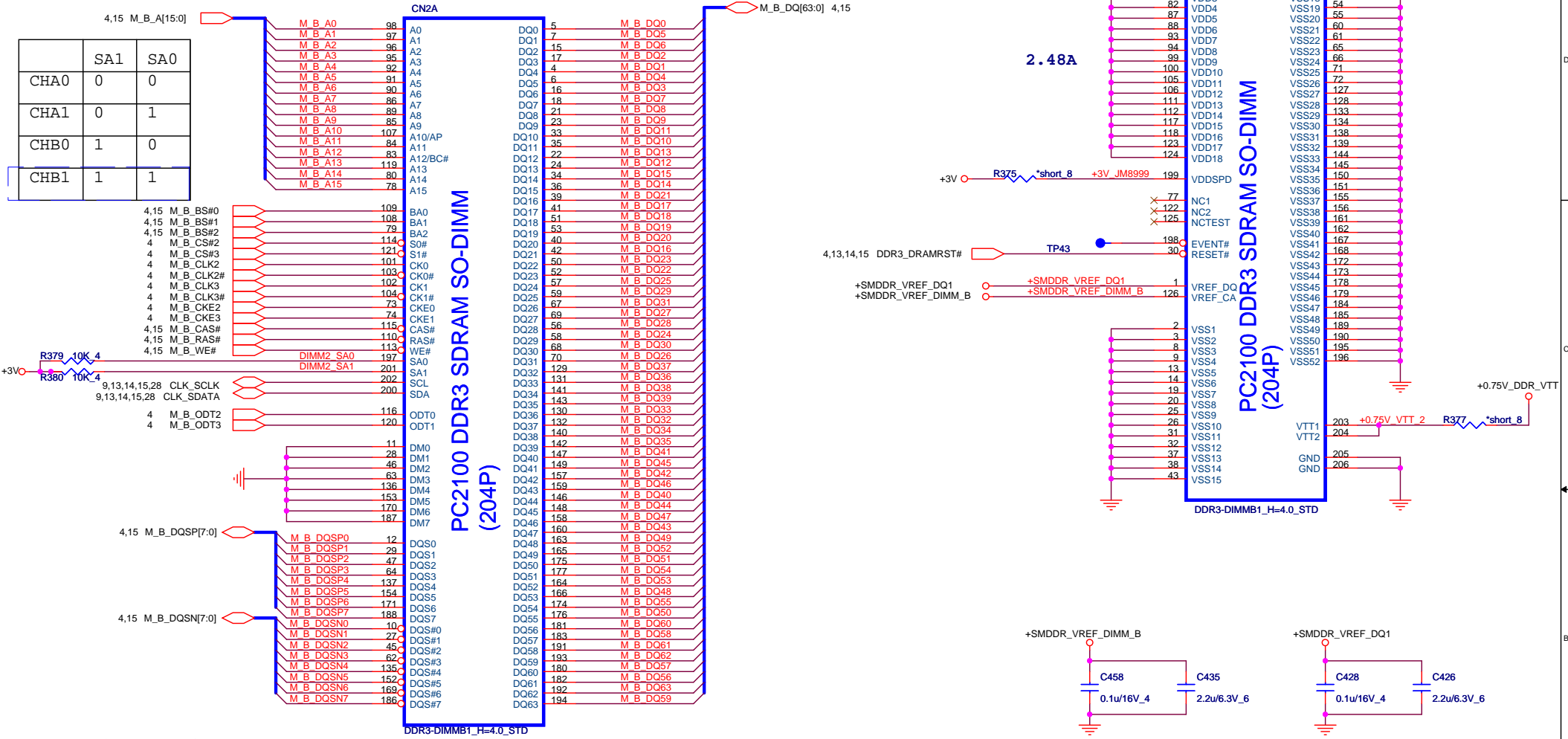
Place these Caps near So-Dimm1.



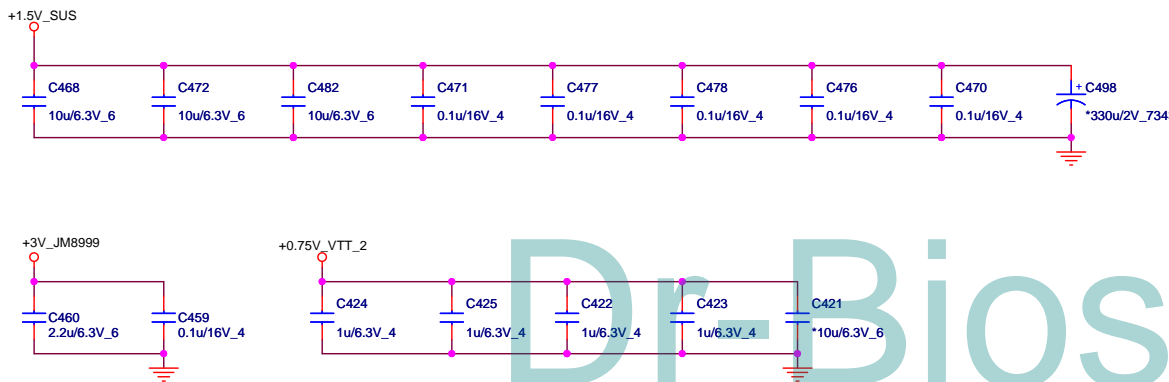
2.48A



# DDR3 DIMM-B1



Place these Caps near So-Dimm1.



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**PROJECT : ZYG**

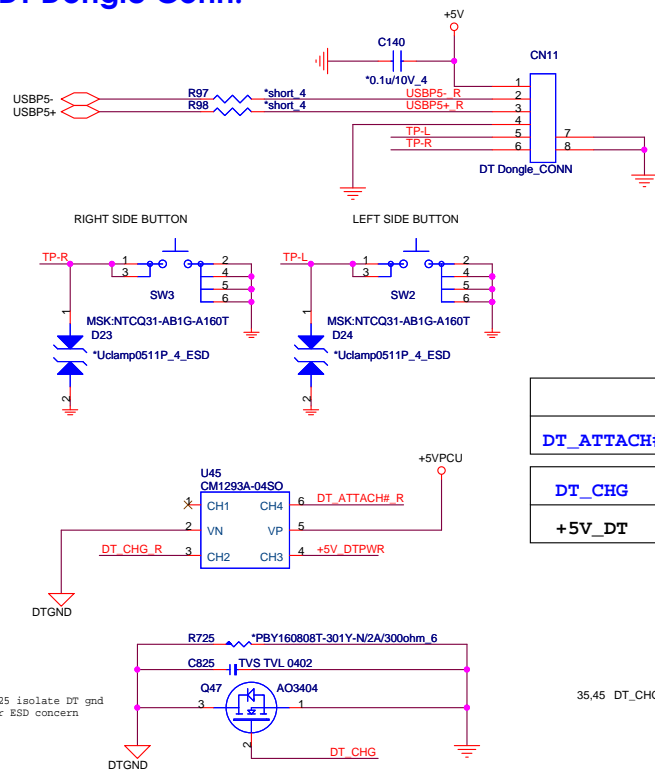
Size	Document Number	Rev
	<b>DDR3 SO-DIMM-B1</b>	1A
Date:	Tuesday, February 22, 2011	Sheet 16 of 50



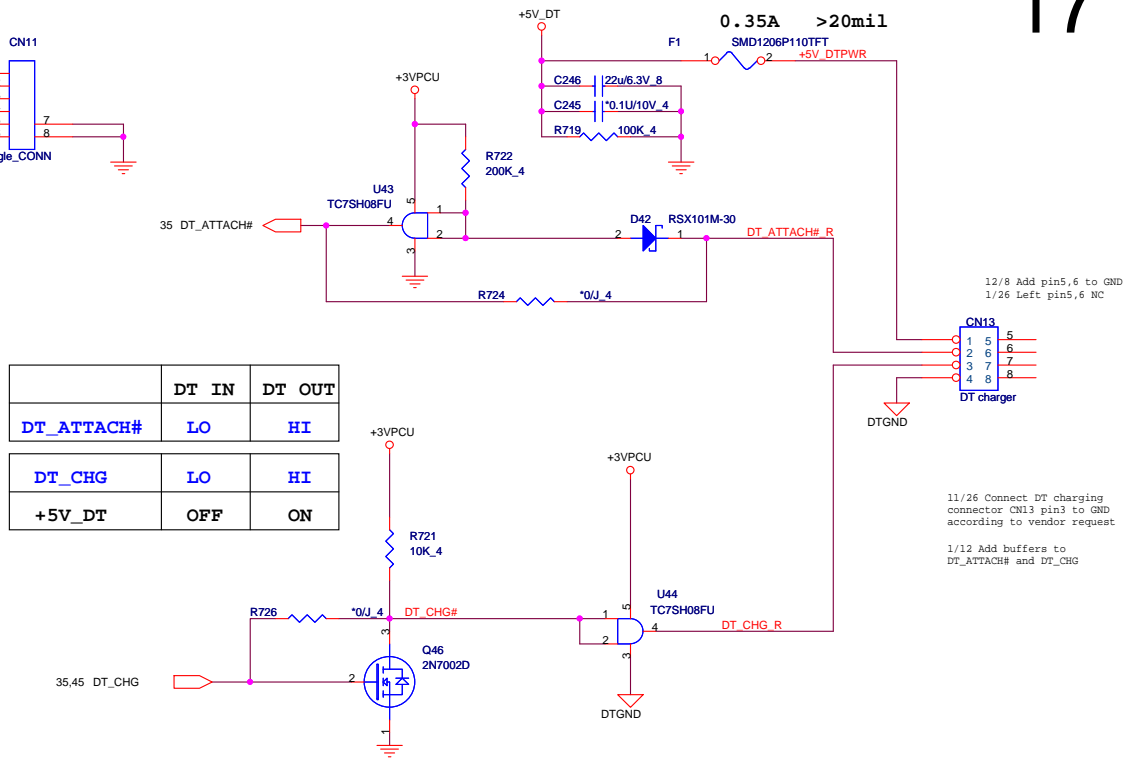
### CPU XDP Connector(CPU)

XDP_PREQ#	CLK_PCIE_XDPN
XDP_PRDY#	XDP_DBRST#
XDP_BPM0	SMB_PCH_DAT
XDP_BPM1	SMB_PCH_CLK
XDP_BPM2	XDP_TDO
XDP_BPM3	XDP_TRST#
XDP_BPM4	XDP_TDI
XDP_BPM5	XDP_TMS
XDP_BPM6	XDP_TCLK
XDP_BPM7	SYS_PWROK
DNBSWON#	PCH_JTAG_TCK
CFG0-----1k	H_PWRGOOD-----1k
CLK_PCIE_XDP	PLTRST#-----1k

### DT Dongle Conn.



### DT PW Conn.

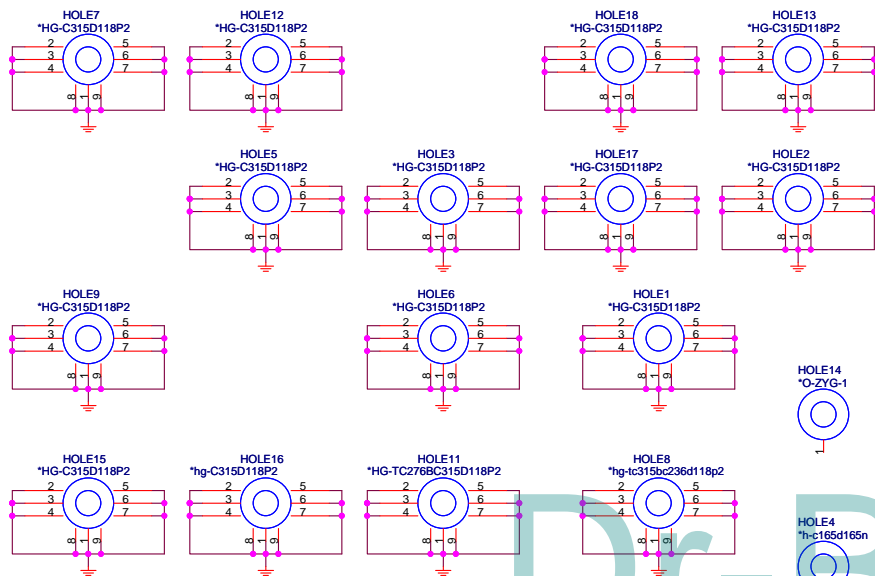


12/8 Add pin5,6 to GND  
1/26 Left pins,6 NC

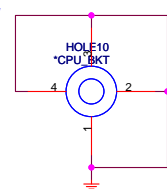
11/26 Connect DT charging connector CN13 pin3 to GND according to vendor request

1/12 Add buffers to DT\_ATTACH# and DT\_CHG

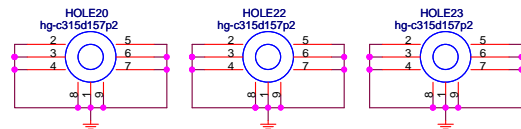
### SCREW HOLE



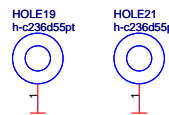
### BKT



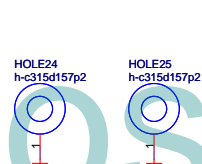
### GPU



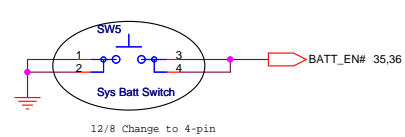
### MiniCard



### PCH



### Battery Power Reset

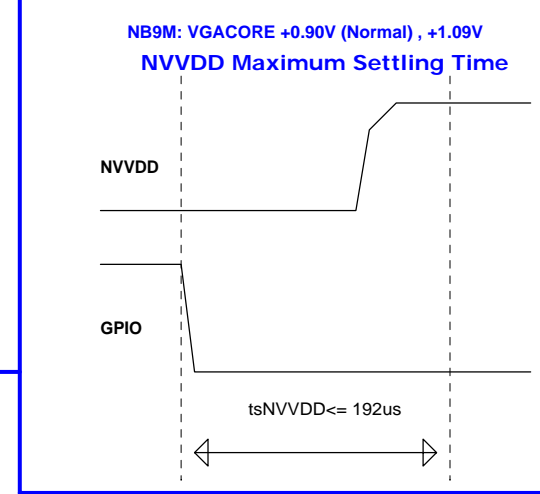
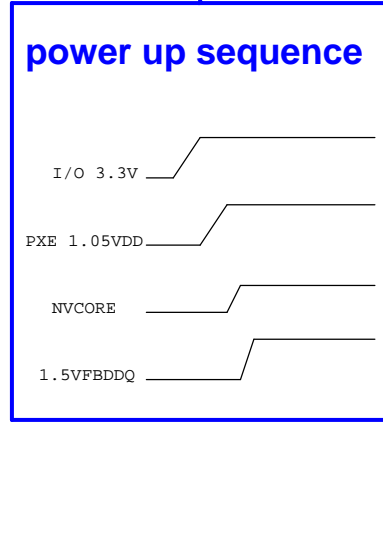
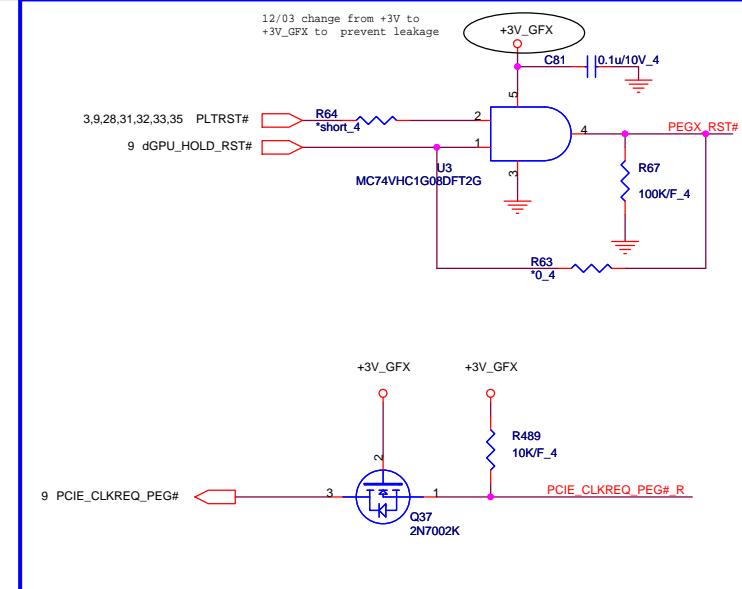
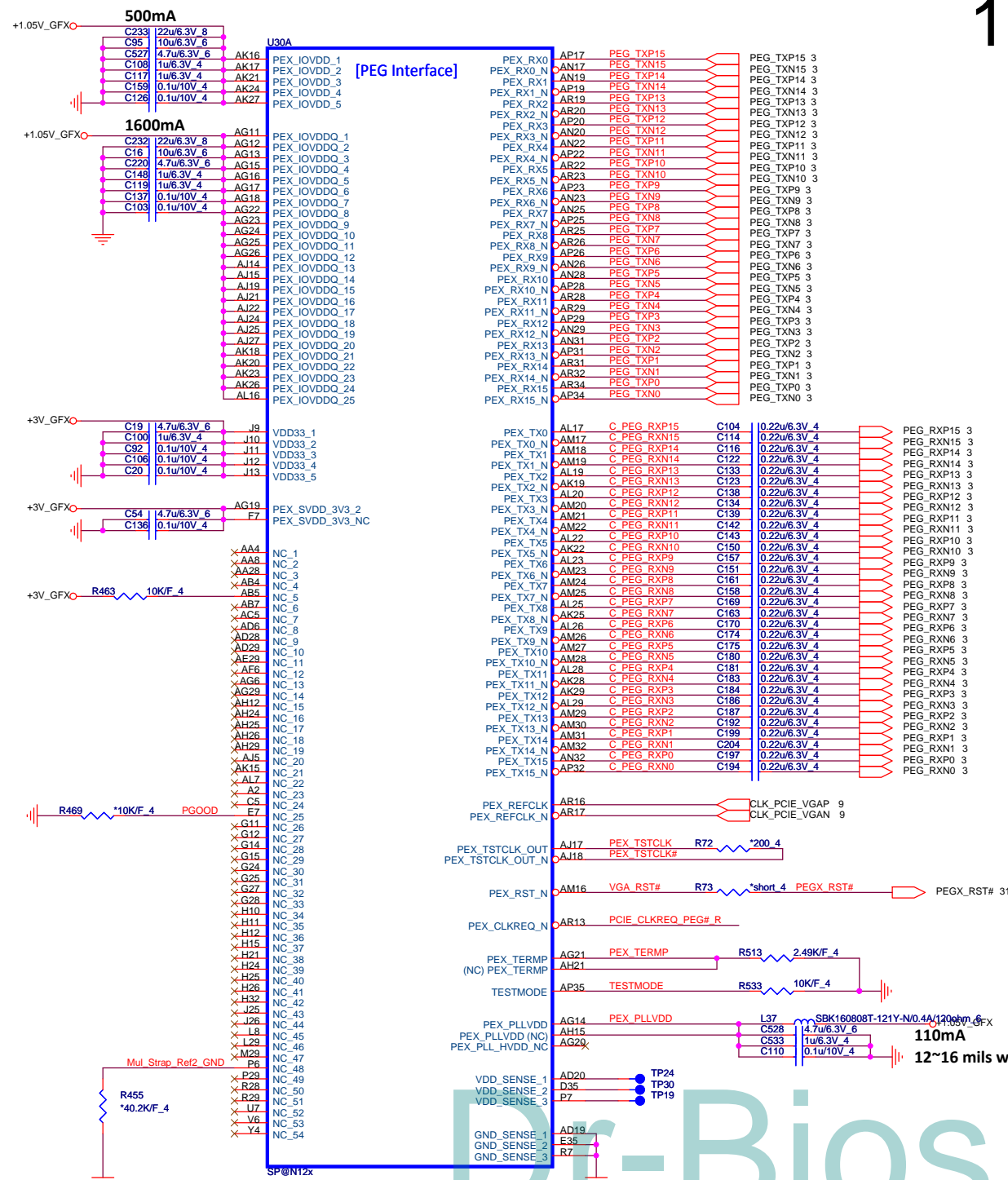


A-stage	SKU1	SKU2	SKU3	SKU4
GPU	N12E-GE	N12P-GS	N12P-GS	N12P-GS (dGPU)
VRAM	Hynix 2G	Hynix 1G	Sam 2G	Hynix 2G

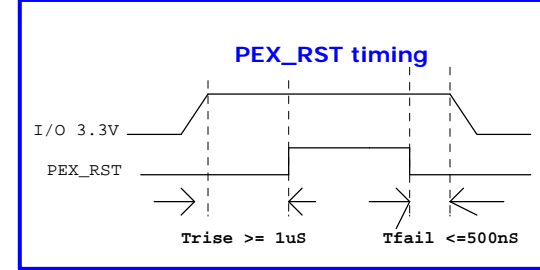
Dr-Bios.com

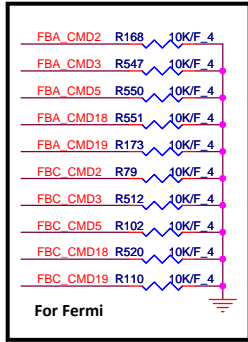
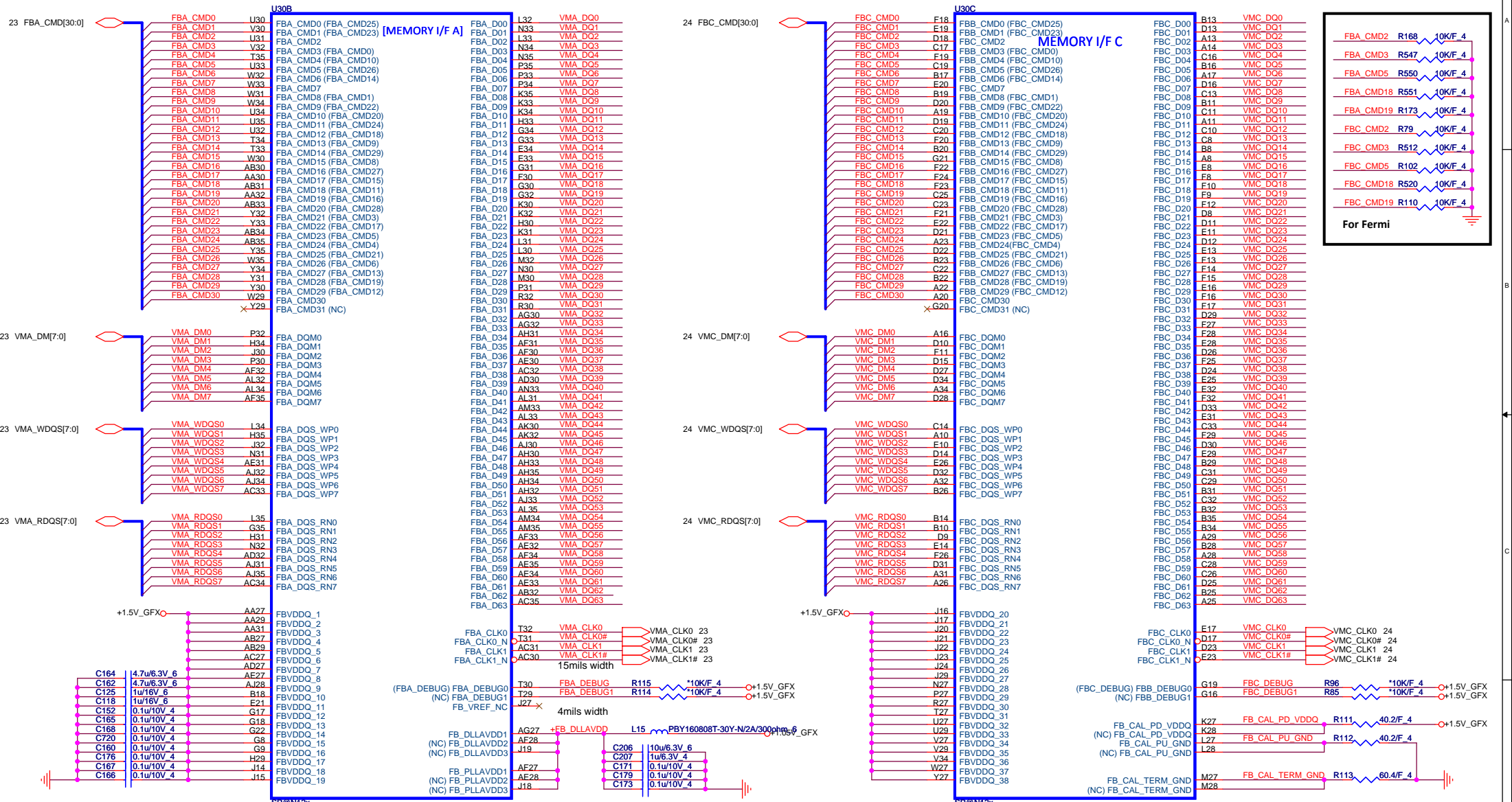
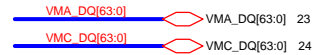
**Quanta Computer Inc.**  
PROJECT : ZYG

Size	Document Number	Rev
	<b>DT/ Batt. Rst / XDP/ Hole</b>	1A
Date:	Wednesday, February 23, 2011	Sheet 17 of 50



PEX_PLLVDD	GB2-128 / GB3-128	
	Under	Near
100nF ,10% X7R 0402	1	
1uF ,10% X7R 0603		1
4.7uF ,10% X5R 0603		1
120 Ohm 0603		
ESR 180 mOhm		1





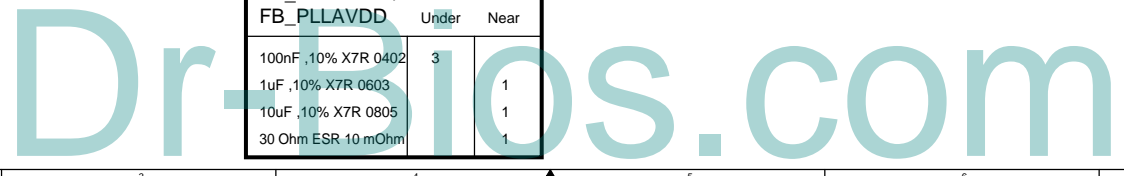
FBVDD	GB2-128 / GB3-128	
	Under	Near
0.1uF, 10% X7R 0603	8	
1uF, 10% X7R 0603		2
4.7uF, 10% X5R 0603		2

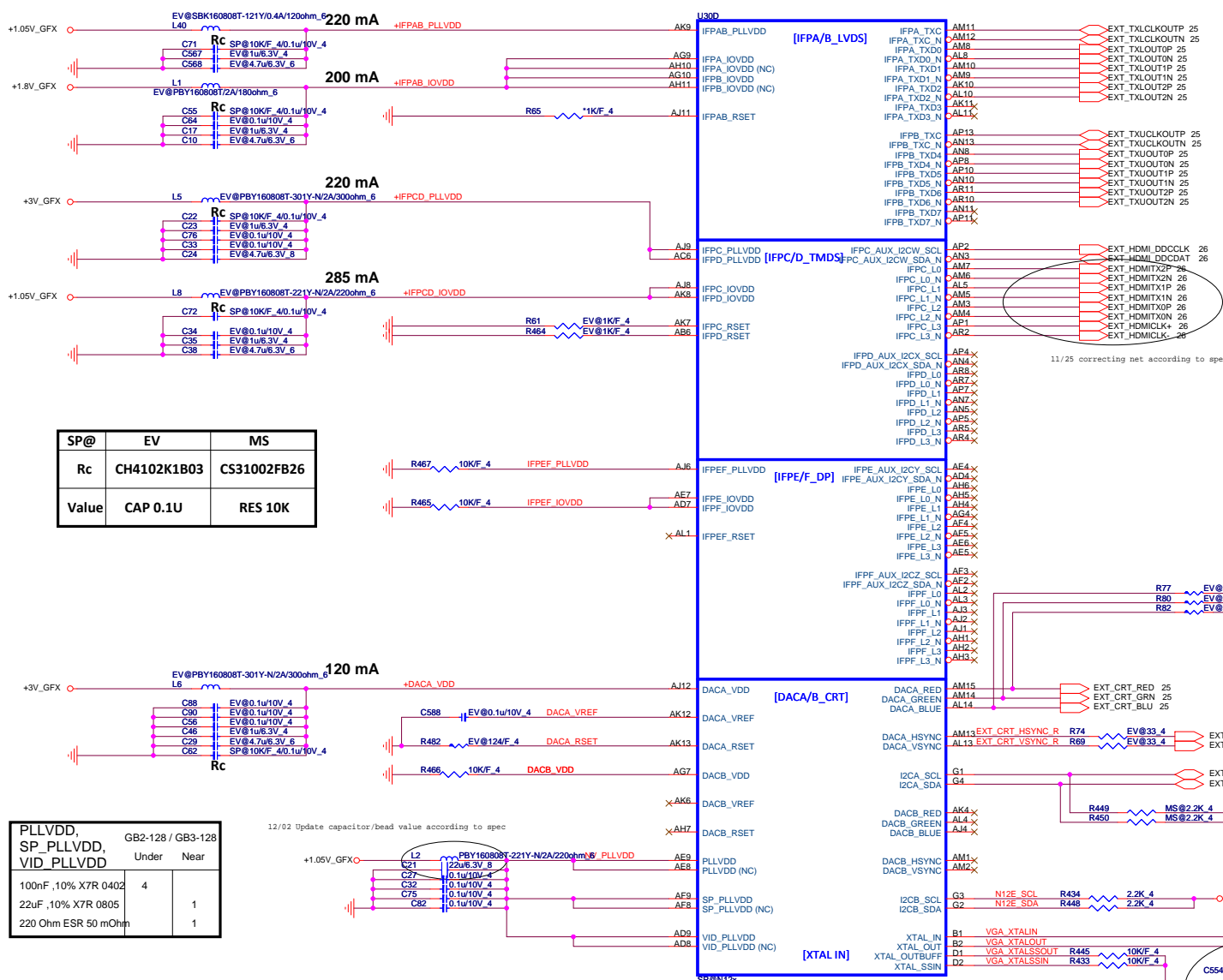
FB_DLLAVDD / FB_PLLAVDD	GB2-128 / GB3-128	
	Under	Near
100nF, 10% X7R 0402	3	
1uF, 10% X7R 0603		1
10uF, 10% X7R 0805		1
30 Ohm ESR 10 mOhm		1

**Quanta Computer Inc.**  
PROJECT : ZYG

Size: Document Number: **DGPU 2/5 (Memory)** Rev: 1A

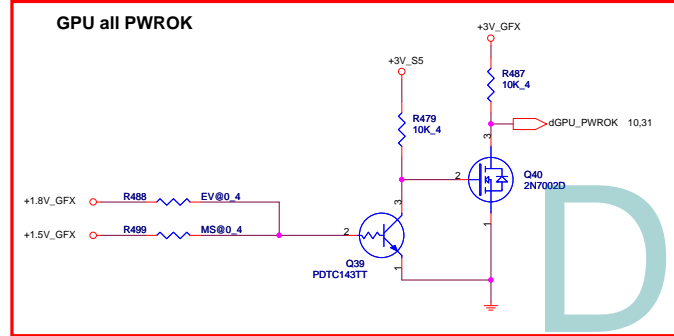
Date: Tuesday, February 22, 2011 Sheet: 19 of 50





SP@	EV	MS
Rc	CH4102K1B03	C331002FB26
Value	CAP 0.1U	RES 10K

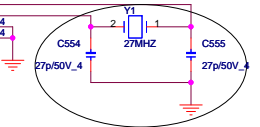
PLLVD, SP_PLLVD, VID_PLLVD	GB2-128 / GB3-128	Under	Near
100nF, 10% X7R 0402	4		1
22uF, 10% X7R 0805			1
220 Ohm ESR 50 mOhm			1



IFPAB_PLLVDD	GB2-128 / GB3-128	Under	Near
100nF, 10% X7R 0402	1		1
1uF, 10% X7R 0603			1
4.7uF, 10% X7R 0805			1
120 Ohm 0603 ESR 180 mOhm			1

DACx_VDD	GB2-128 / GB3-128	Under	Near
100nF, 10% X7R 0402	4		1
1uF, 10% X5R 0402			1
4.7uF, 10% X5R 0805			1
300 Ohm 0603 ESR 250 mOhm			1

IFPC/D/E_PLLVDD	GB2-128 / GB3-128	Under	Near
100nF, 10% X7R 0402	3		1
1uF, 10% X7R 0603			1
4.7uF, 10% X7R 0805			1
300 Ohm 0603 ESR 250 mOhm			1

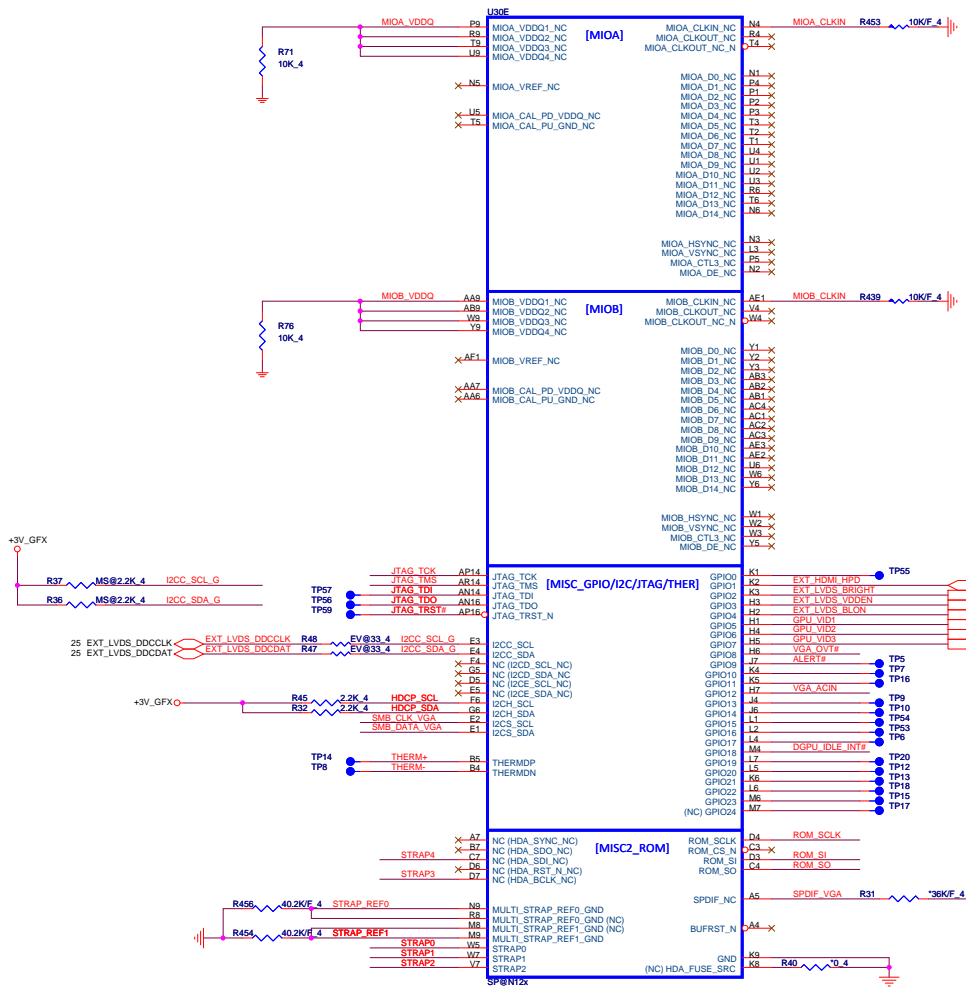


12/03 adjust capacitor value for crystal

**Quanta Computer Inc.**  
**PROJECT : ZYG**

Size	Document Number	Rev
	<b>DGPU 3/5 (Display)</b>	1A

Date: Tuesday, February 22, 2011 Sheet 20 of 50



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12P-GS	N12P-GS	N12P-GS	N12P-GS	N12E-GE	N12E-GE	N12E-GE	N12E-GE
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001	0001	0001	0001	0001	0001	0001	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLN_EN_TERM	1010	1010	1010	1010	0010	0010	0010	0010
ROM_SI	VRAM	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010	0110	0011	0011	0011	0011	0111
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100	0100	0100	0100	1110	1110	1110	1110
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	0110	0110	0110	0110	0110	0110	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111	1111	1111	1111	1111	1111	1111

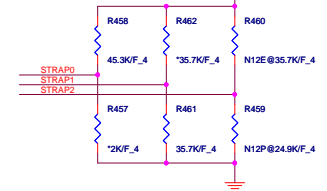
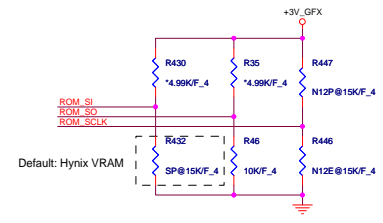
RAMCFG [3:0]	DESCRIPTION	Vendor PN	ROM_SI	QCI	QCI B/S
0010	Hynix DDR3 64Mx16x8, 1GB,900MHz	H5TQ1G63DFR-11C	PD 15K	AKD5LZWTW02	AKD5LZWTW05
0011	Samsung DDR3 64Mx16x8, 1GB,900MHz	K4W1G1646G-BC11	PD 20K	AKD5EGGT500	AKD5EGGT503
0110	Hynix DDR3 128Mx16x8, 2GB,900MHz	H5TQ2G63BFR-11C	PD 35K	AKD5MGWTW00	AKD5MGWTW03
0111	Samsung DDR3 128Mx16x8, 2GB,900MHz	K4W2G1646C-HC11	PD 45K	AKD5MGWT500	AKD5MGWT503

Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

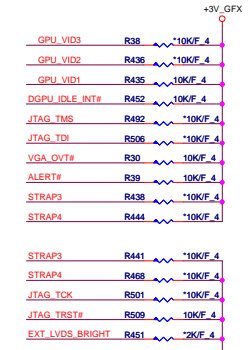
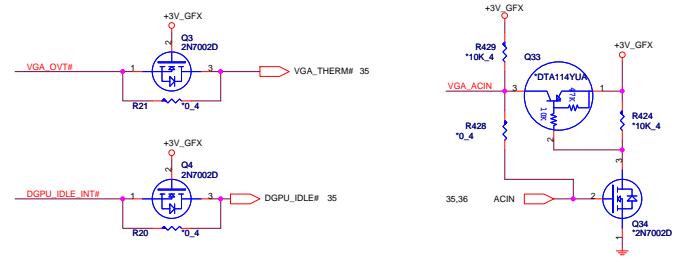
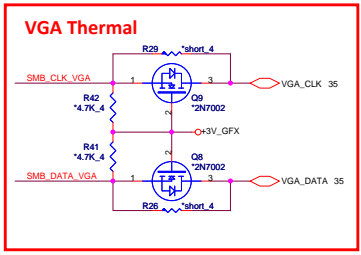
		QCI	B/S
N12E-GE	IC CTRL(1005P) N12E-GE-A1(BGA)	AJON12E0T00	AJON12E0T02
N12P-GS	IC CTRL(973P) N12P-GS-A1(BGA)	AJON12P0T04	AJON12P0T13

4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +/-1%(0402)]  
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +/-1%(0402)]  
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +/-1%(0402)]  
 20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +/-1%(0402)]  
 30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +/-1%(0402)]  
 35.7K/F 4: CS3352FB13 [RES CHIP 35.7K 1/16W +/-1%(0402)]  
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +/-1%(0402)]



**GPIO ASSIGNMENTS**

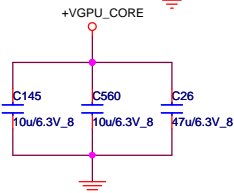
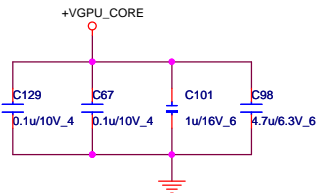
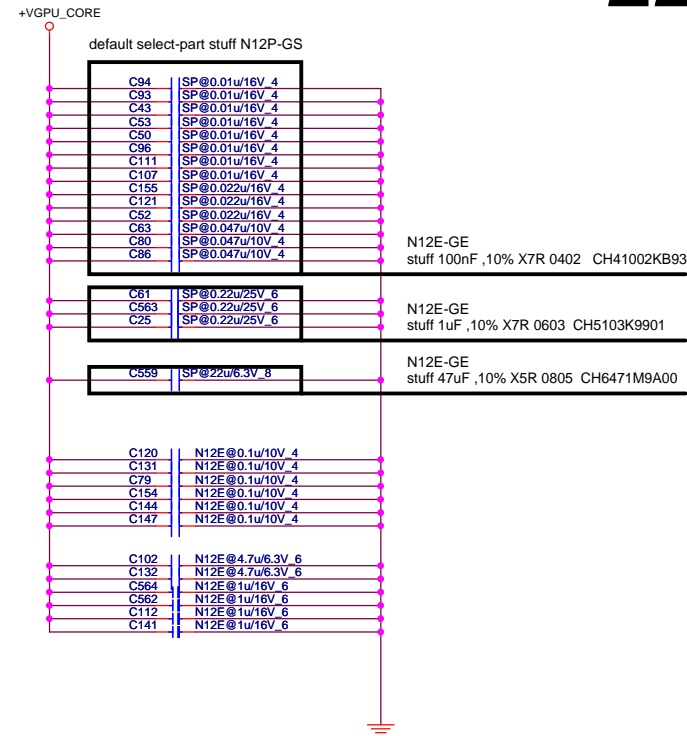
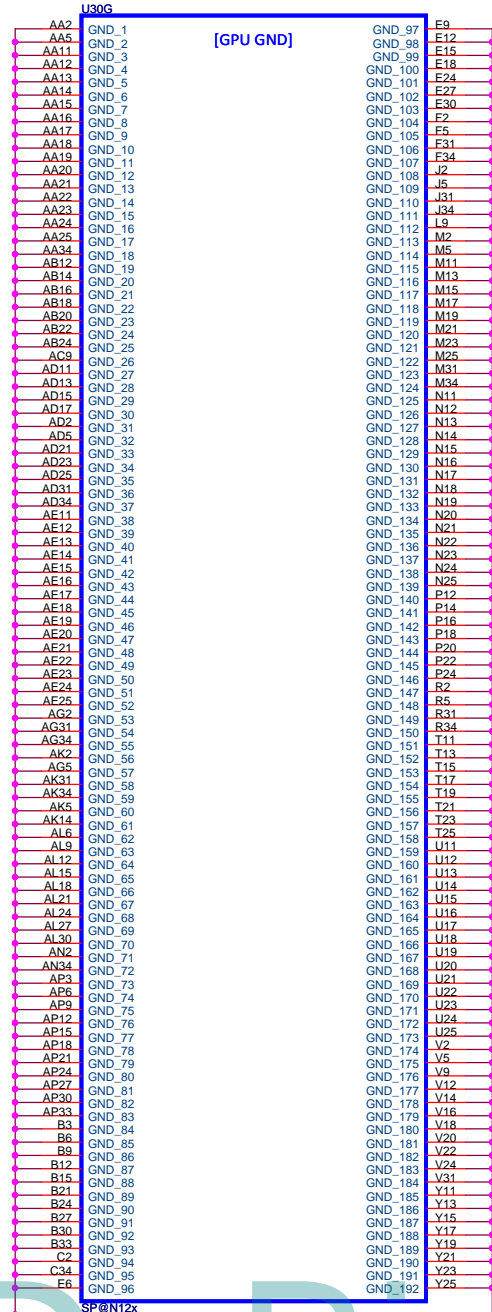
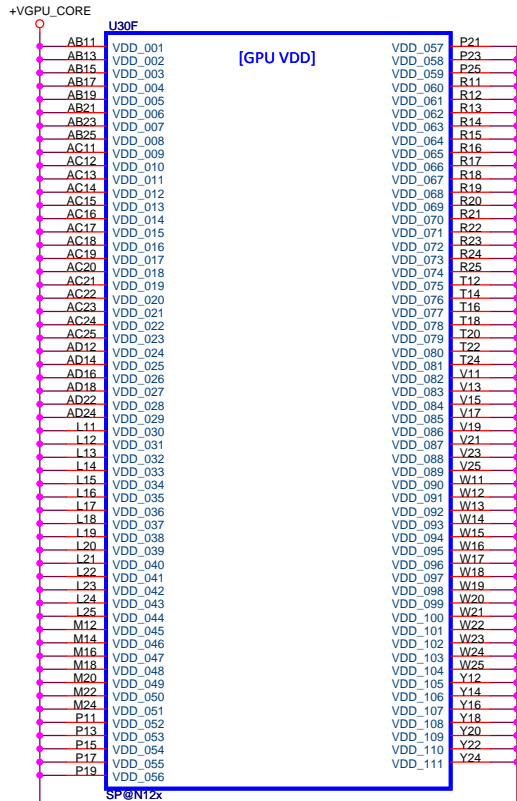
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 <span style="border: 1px solid green; padding: 2px;">11/13</span>
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	<span style="border: 1px solid green; padding: 2px;">PWR_LEVEL</span> <span style="border: 1px solid green; padding: 2px;">11/13</span>
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



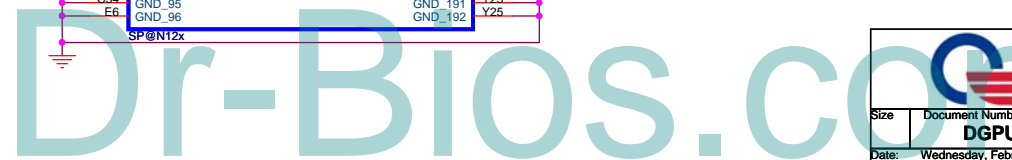
**Quanta Computer Inc.**  
 PROJECT : ZYG

Size	Document Number	Rev
	<b>DGPU 4/5 (MIO/GPIO)</b>	1A

Date: Tuesday, February 22, 2011 Sheet 21 of 50



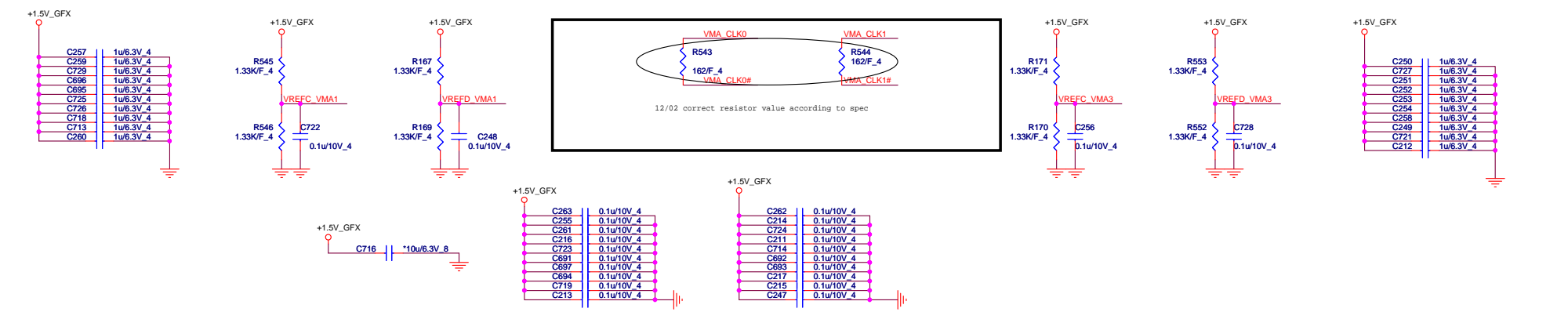
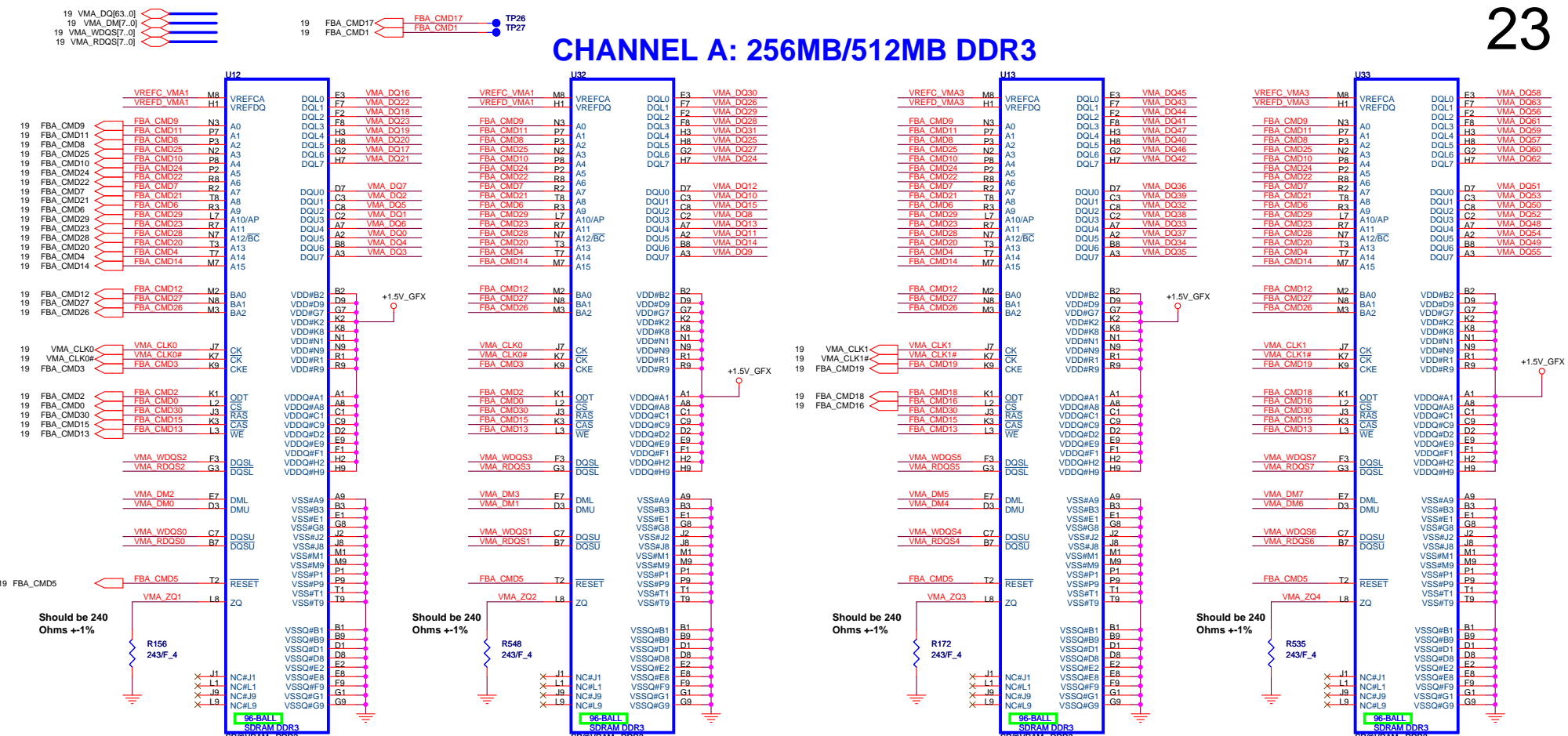
SPEC	GB2-128 12P-GS	GB3-128 12E-GE
10nF ,10% X7R 0402	8	
22nF ,10% X7R 0402	3	
47nF ,10% X7R 0402	3	
100nF ,10% X7R 0402	2	22
220nF ,10% X7R 0603	3	
1uF ,10% X7R 0603	1	8
4.7uF ,10% X5R 0603	1	3
10uF ,10% X5R 0805	2	2
22uF ,10% X5R 0805	1	
47uF ,10% X5R 0805	1	2
470uF	1	



**Quanta Computer Inc.**  
 PROJECT : ZYG

Size	Document Number	Rev
	<b>DGPU 5/5 (Power/Ground)</b>	1A
Date:	Wednesday, February 16, 2011	Sheet 22 of 50

# CHANNEL A: 256MB/512MB DDR3

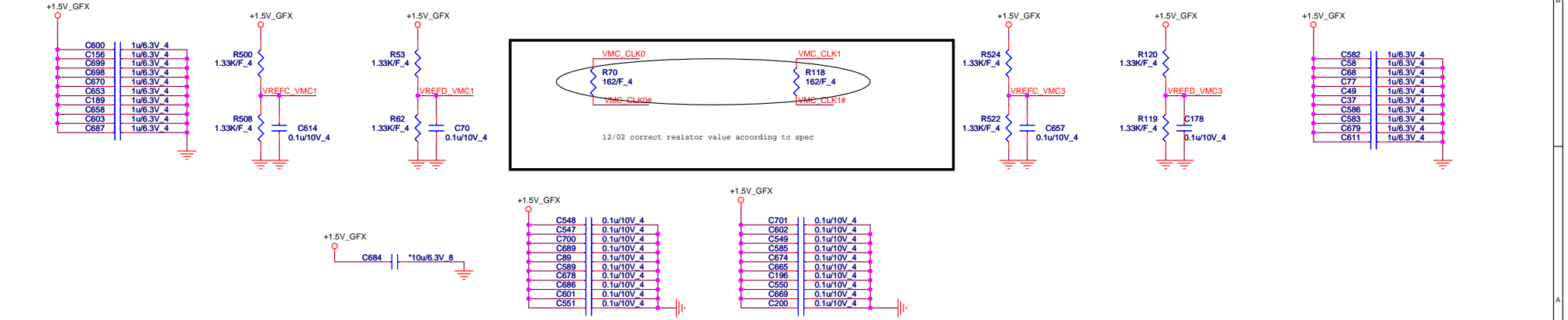
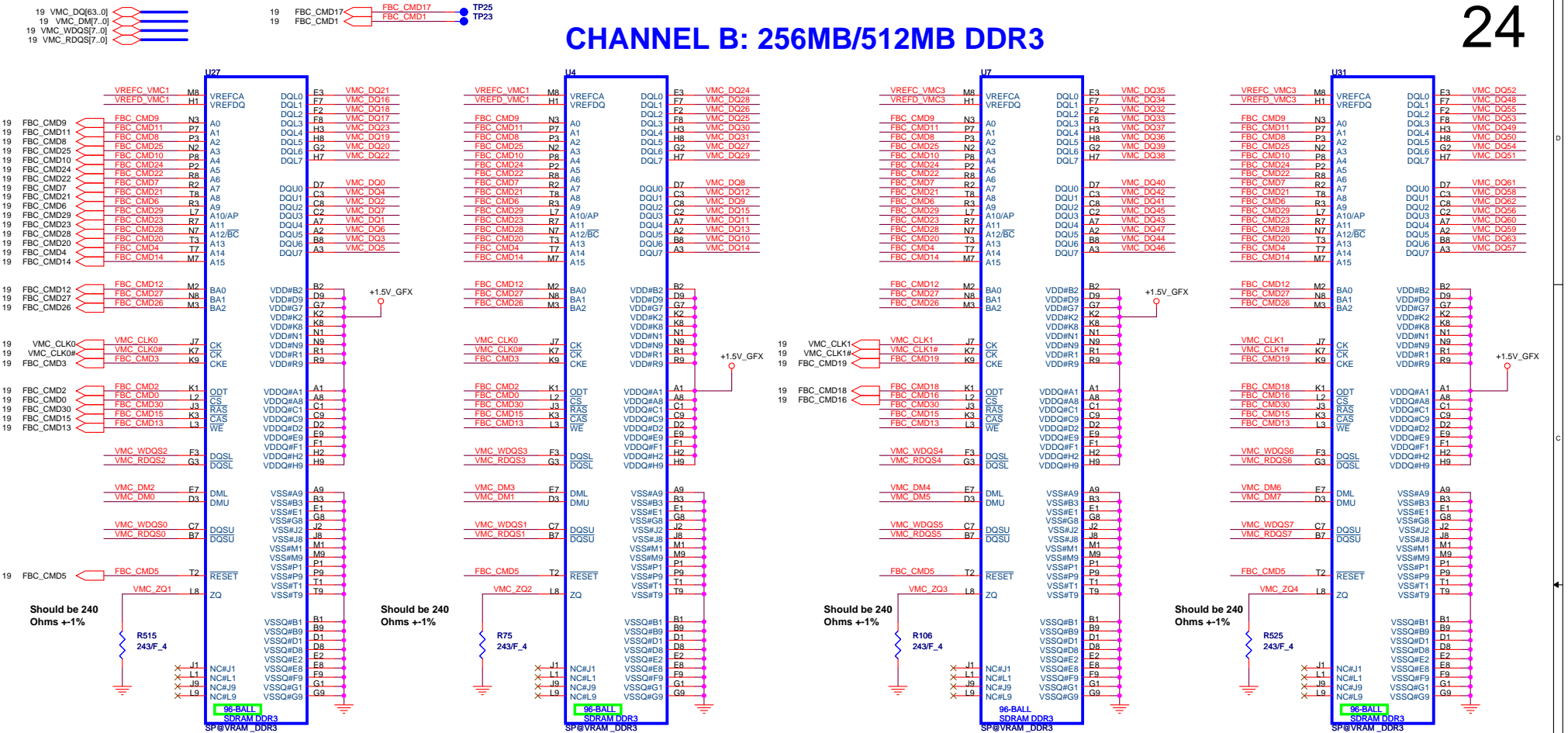


A-stage	SKU1	SKU2	SKU3	SKU4
GPU	N12E-GE	N12P-GS	N12P-GS	N12P-GS (dGPU)
VRAM	Hynix 2G	Hynix 1G	Sam 2G	Hynix 2G

VRAM	Description	Vendor P/N	QCI	QCI B/S	
Hynix	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)H5TQ1G63DFR-11C(FBGA)STNBSQ	H5TQ1G63DFR-11C	AKD5LZWTW02	AKD5LZWTW05
Samsung	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)K4W1G1646G-BC11 STN BSQ	K4W1G1646G-BC11	AKD5EGGT500	AKD5EGGT503
Hynix	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)H5TQ2G63BFR-11C(FBGA)STNBSQ	H5TQ2G63BFR-11C	AKD5MGWTW00	AKD5MGWTW03
Samsung	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)K4W2G1646G-HC11(FBGA)STNBSQ	K4W2G1646G-HC11	AKD5MGWT500	AKD5MGWT503

**Quanta Computer Inc.**  
**PROJECT : ZYG**  
**DGPU Memory 1/2 (DDR3)**

# CHANNEL B: 256MB/512MB DDR3



A-stage	SKU1	SKU2	SKU3	SKU4
GPU	N12E-GE	N12P-GS	N12P-GS	N12P-GS (dGPU)
VRAM	Hynix 2G	Hynix 1G	Sam 2G	Hynix 2G

VRAM	Description	Vendor P/N	QCI	QCI B/S	
Hynix	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)H5TQ1G63DFR-11C(FBGA)STNBSQ	H5TQ1G63DFR-11C	AKD5LZWTW02	AKD5LZWTW05
Samsung	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)K4W1G1646G-BC11 STN BSQ	K4W1G1646G-BC11	AKD5EGGT500	AKD5EGGT503
Hynix	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)H5TQ2G63BFR-11C(FBGA)STNBSQ	H5TQ2G63BFR-11C	AKD5MGWTW00	AKD5MGWTW03
Samsung	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)K4W2G1646G-HC11(FBGA)STNBSQ	K4W2G1646G-HC11	AKD5MGWT500	AKD5MGWT503

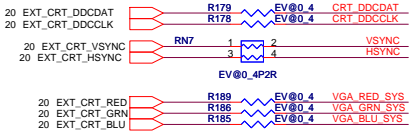
**Quanta Computer Inc.**  
**PROJECT : ZYG**  
 Size Document Number  
**DGPU Memory 2/2 (DDR3)**  
 Date: Tuesday, February 22, 2011 Sheet 24 of 50



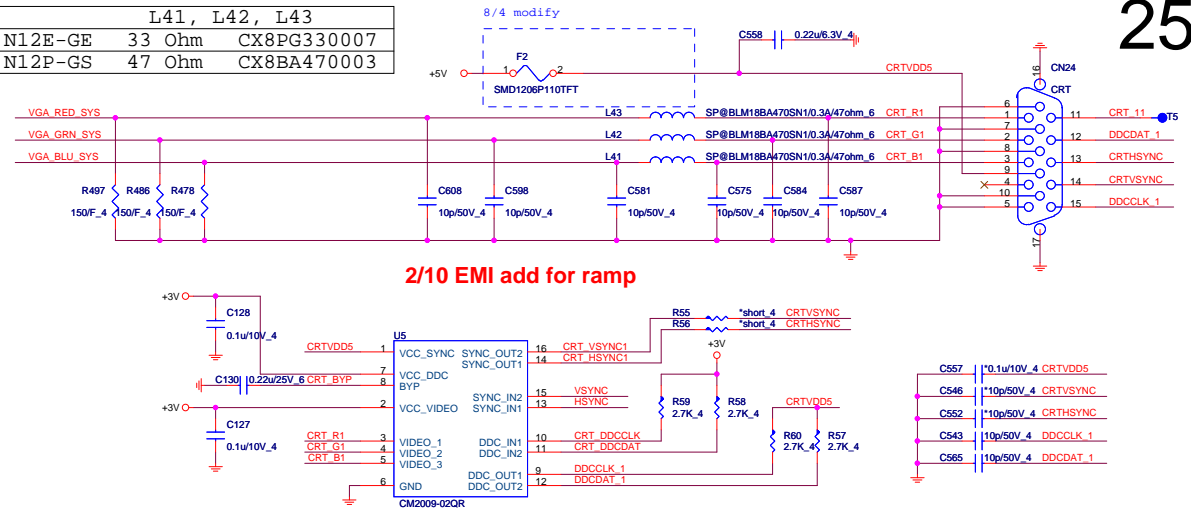
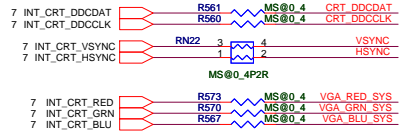
L41, L42, L43
N12E-GE 33 Ohm CX8PG330007
N12P-GS 47 Ohm CX8BA470003

CRT

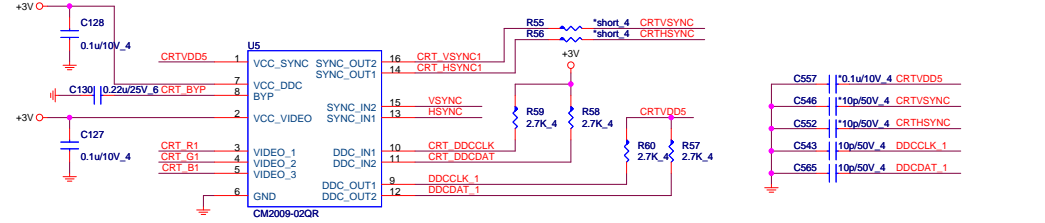
EV@ --- GPU only



MS@ --- iGPU & GPU Muxless

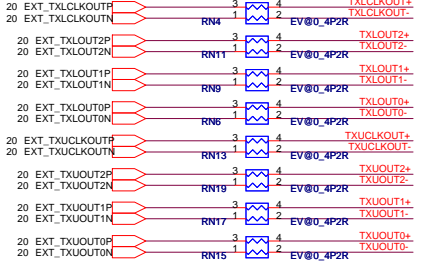


2/10 EMI add for ramp

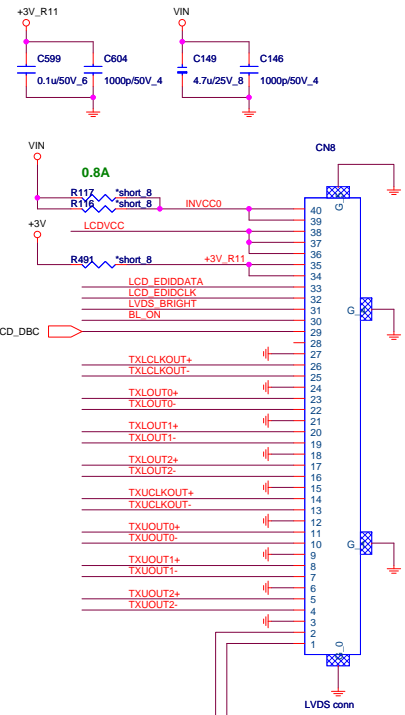
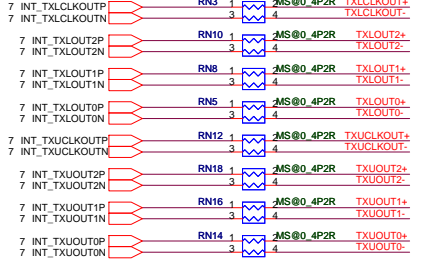


LVDS

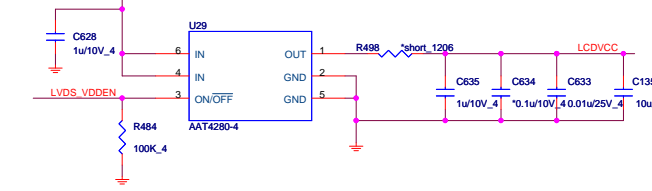
EV@ --- GPU only



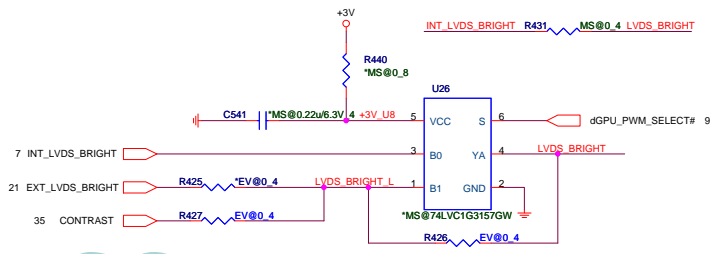
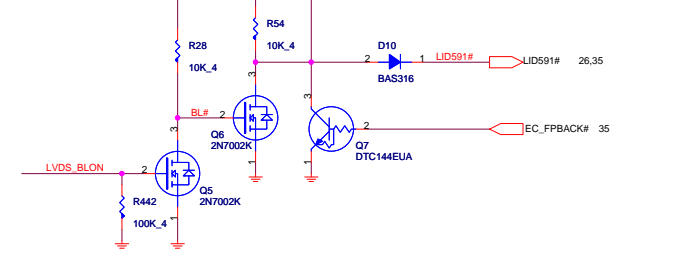
MS@ --- iGPU & GPU Muxless



LCD Power

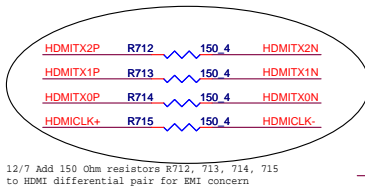


Backlight Control



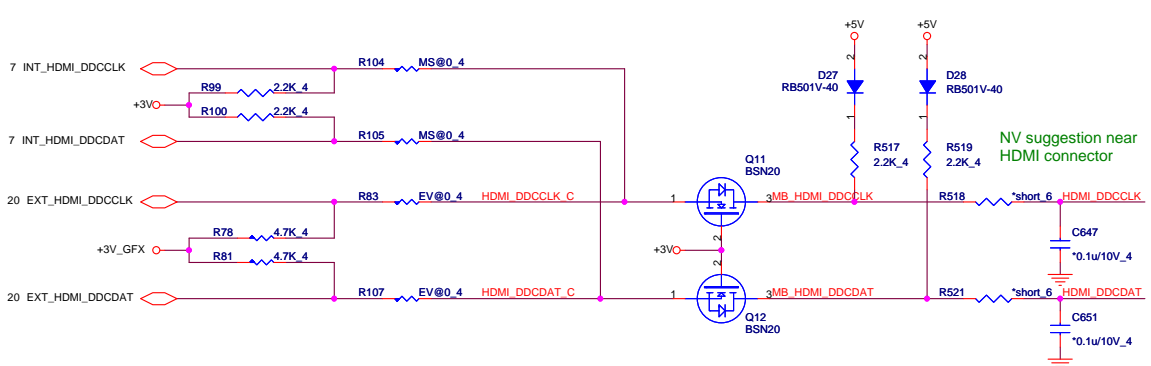
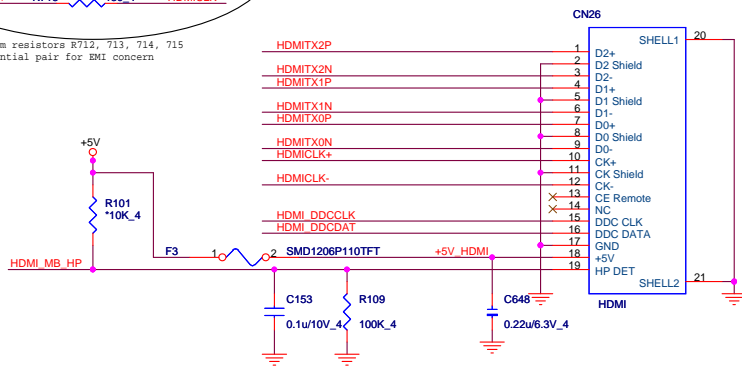
Dr-Bios.com

EV@ --- GPU  
MS@ --- iGPU & GPU  
Muxless



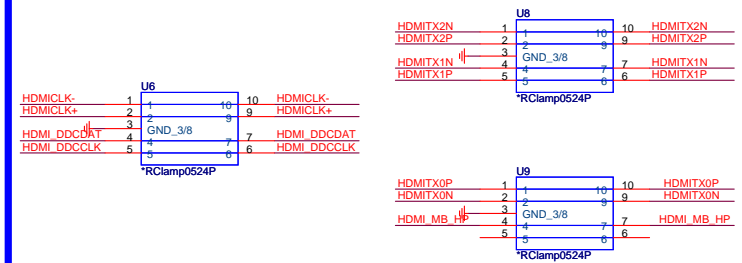
12/7 Add 150 Ohm resistors R712, 713, 714, 715 to HDMI differential pair for EMI concern

HDMI connector

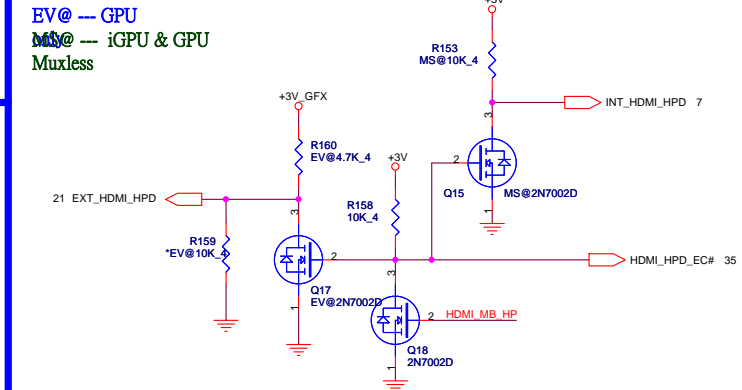


NV suggestion near HDMI connector

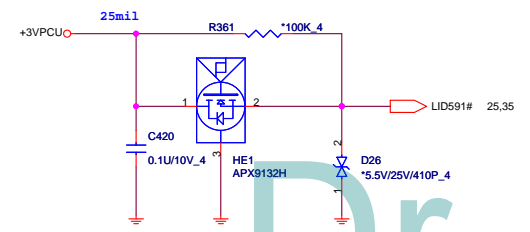
ESD Protect



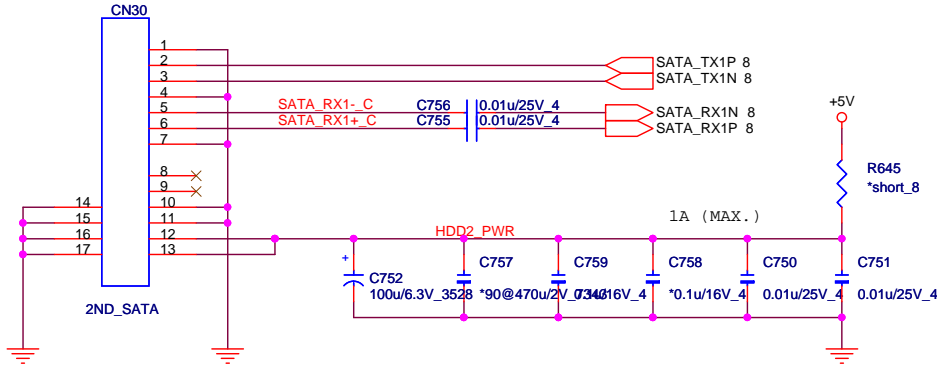
HDMI -detect



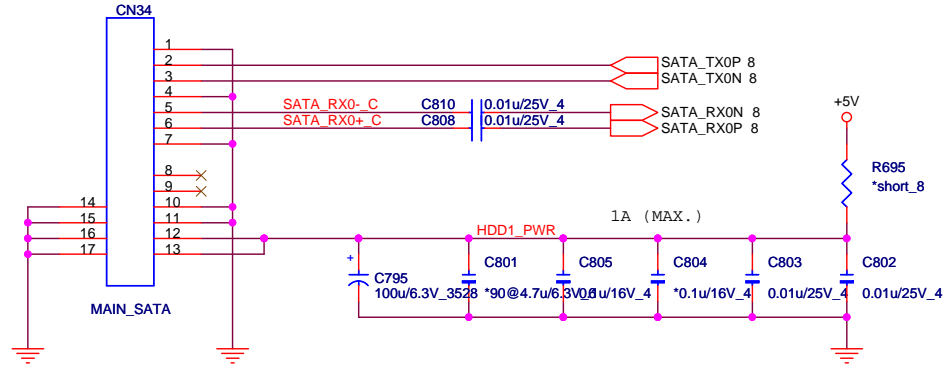
Lid Switch (Hall sensor)



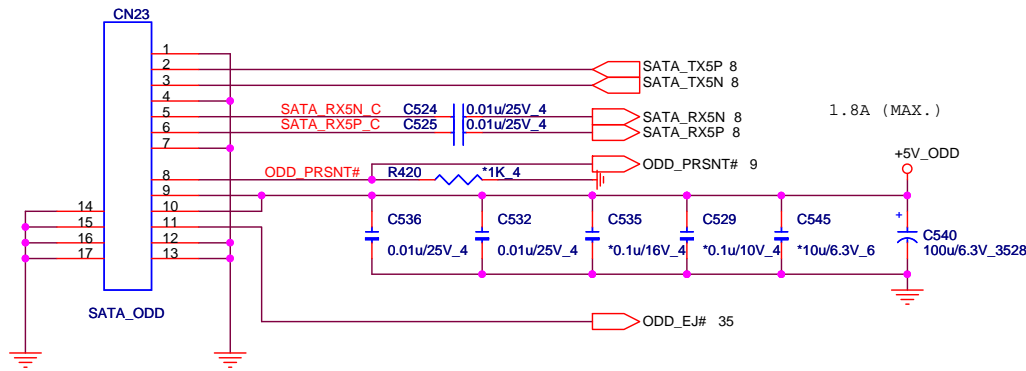
### 2nd SATA HDD (edge of board)



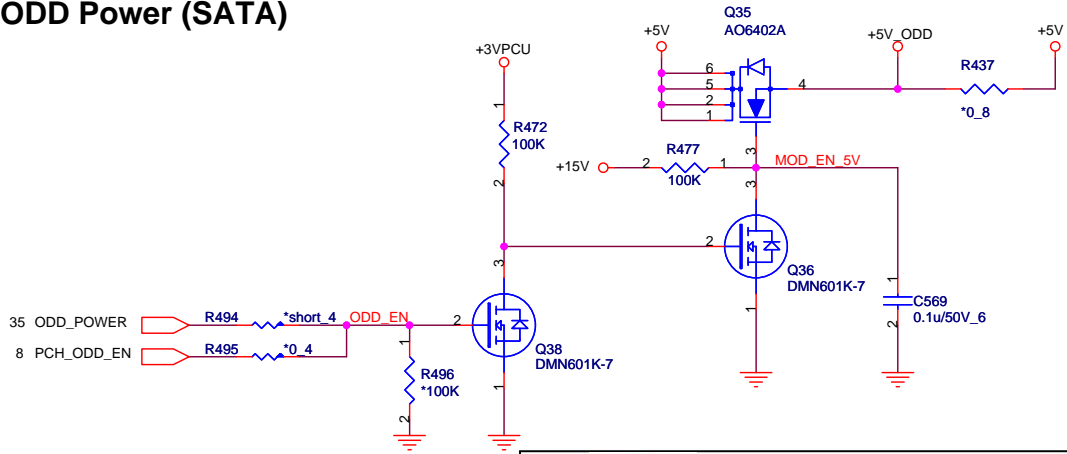
### MAIN SATA HDD



### ODD (SATA)



### ODD Power (SATA)



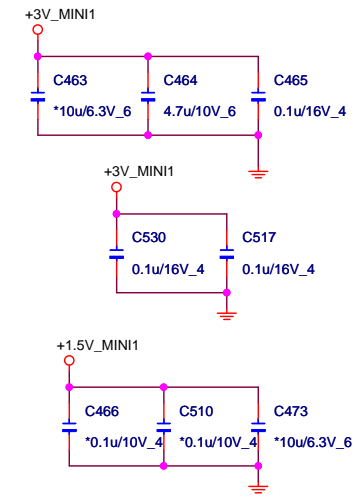
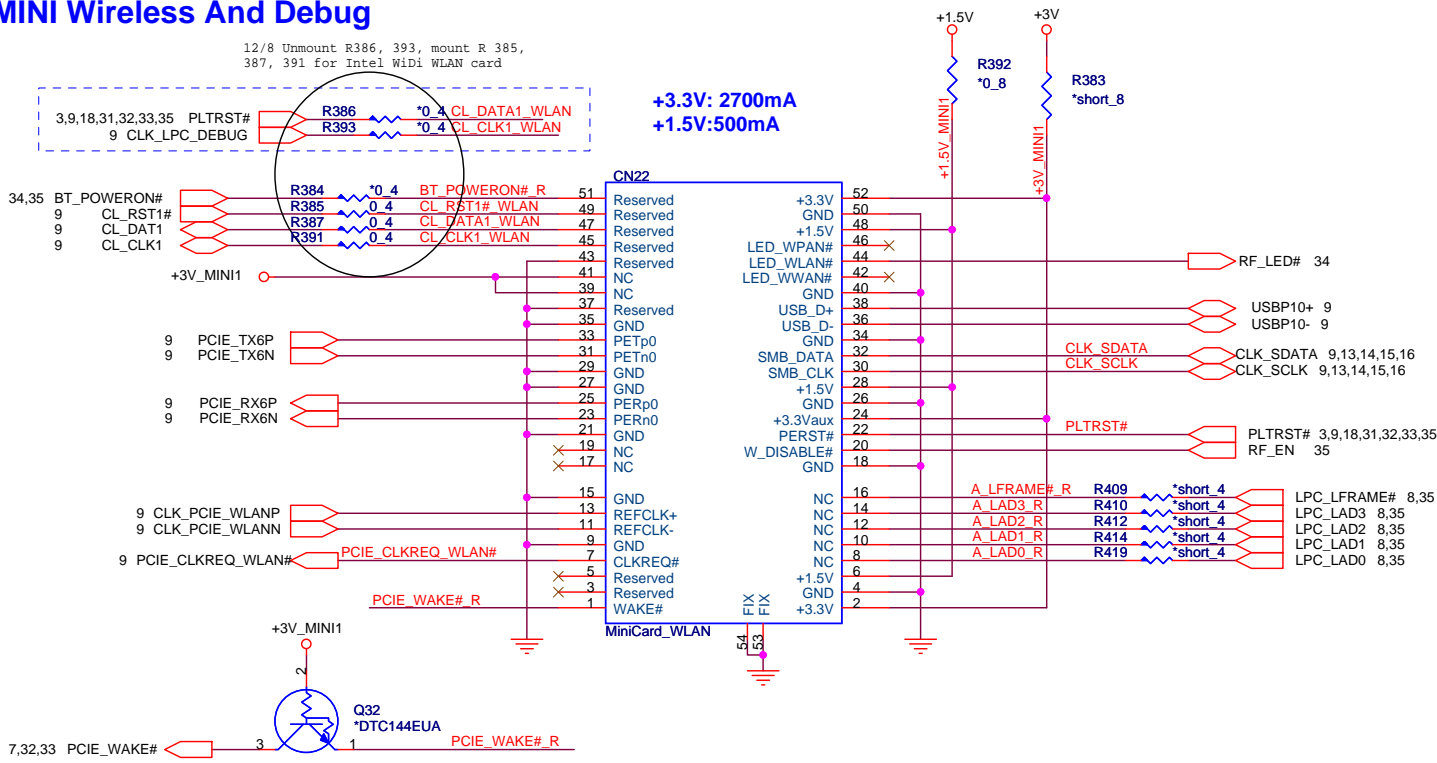
**Quanta Computer Inc.**  
**PROJECT : ZYG**

Size	Document Number	Rev
	<b>SATA-HDD/ODD</b>	1A

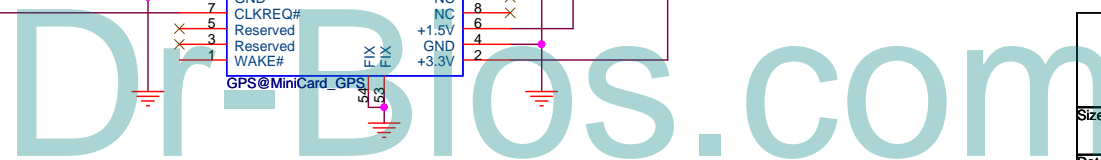
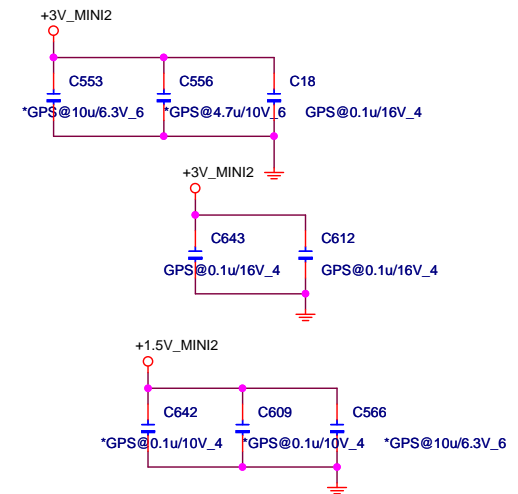
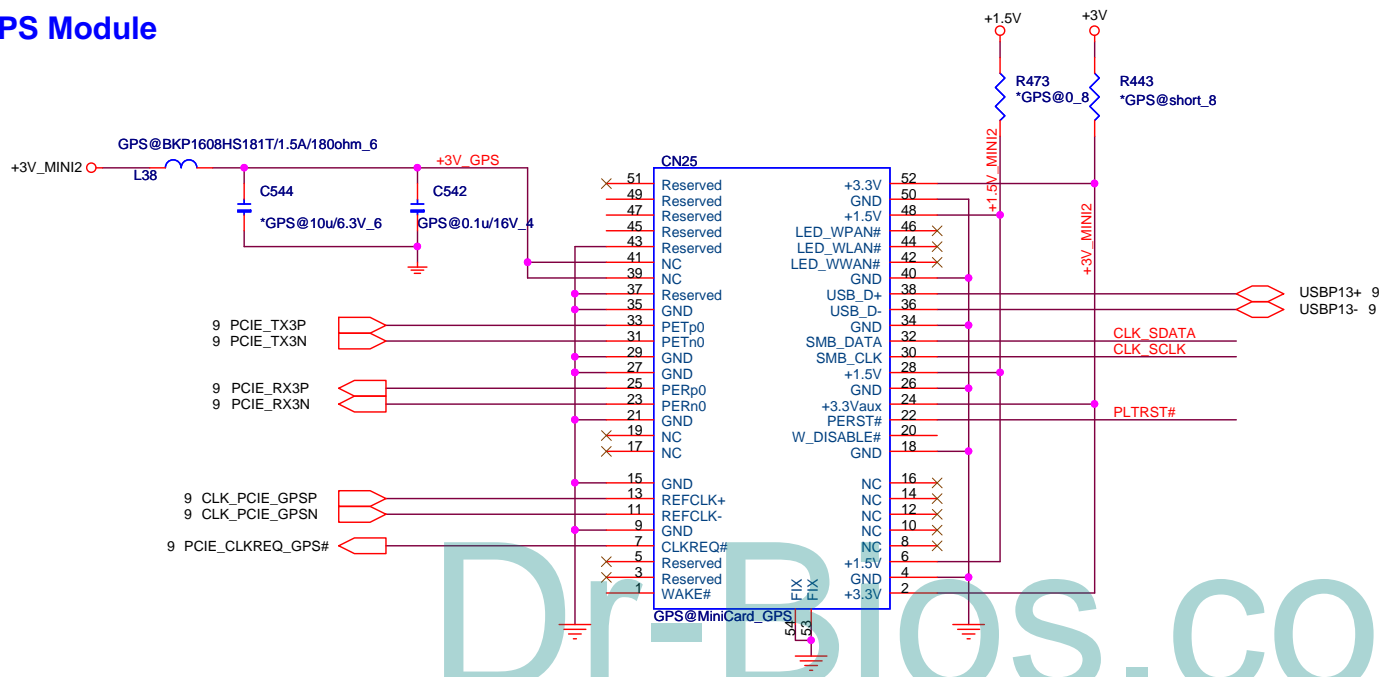
Date: Tuesday, February 22, 2011 Sheet 27 of 50

# MINI Wireless And Debug

12/8 Umount R386, 393, mount R 385, 387, 391 for Intel WiDi WLAN card



# MINI GPS Module



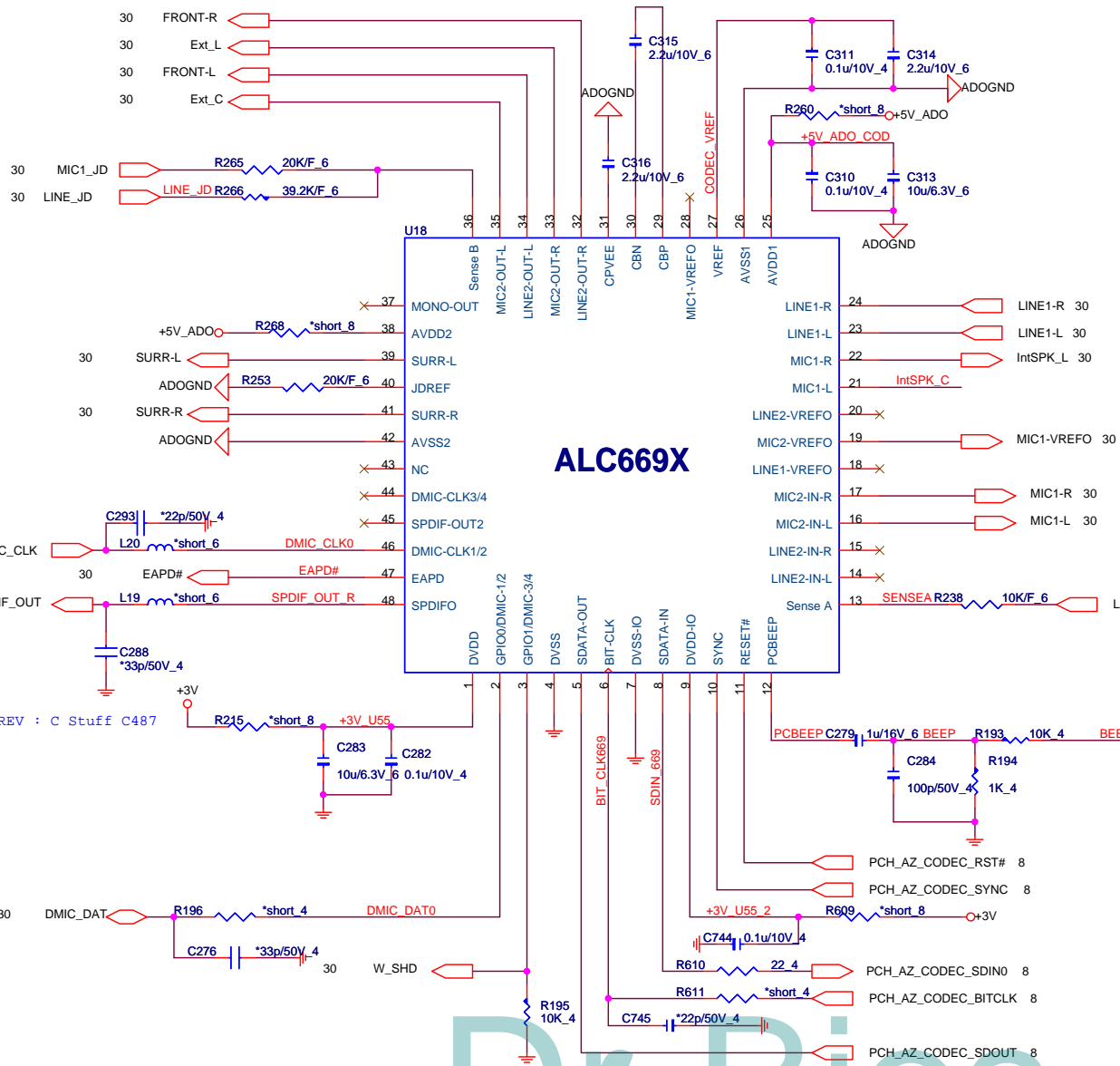
**Quanta Computer Inc.**  
**PROJECT : ZYG**

Size	Document Number	Rev
		1A

**MINI PCI-E card/TV**

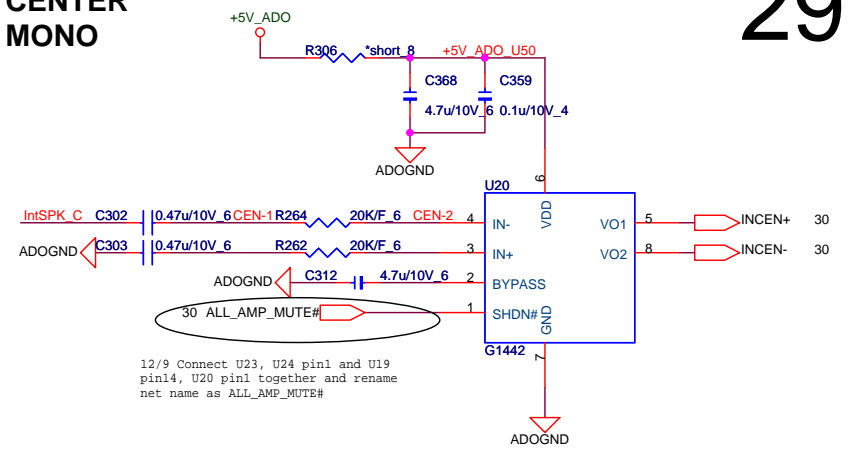
Date: Tuesday, February 22, 2011 Sheet 28 of 50

# CODEC(ALC669X)

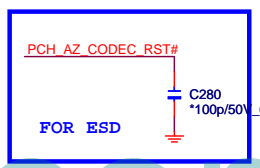
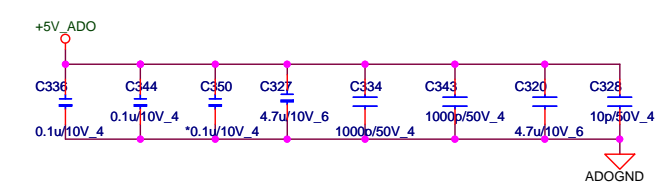


## ALC669X

# CENTER MONO

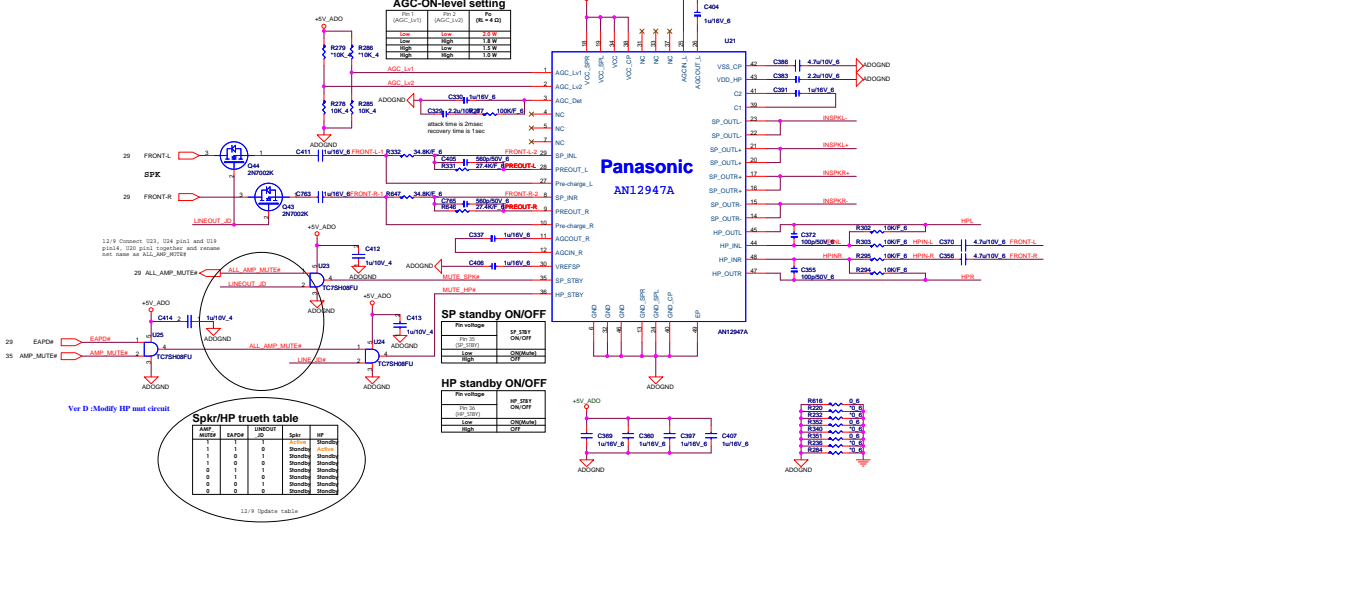


# CODEC/AMP Power

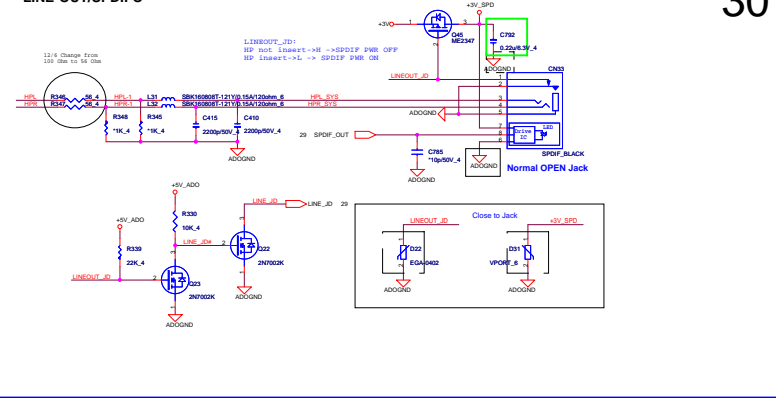


Dr-Bios.com

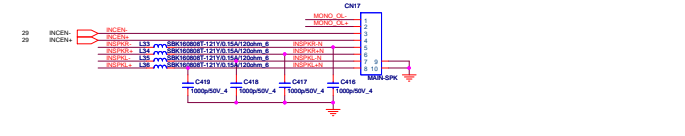
FRONT SPEAKER/HP AMP.



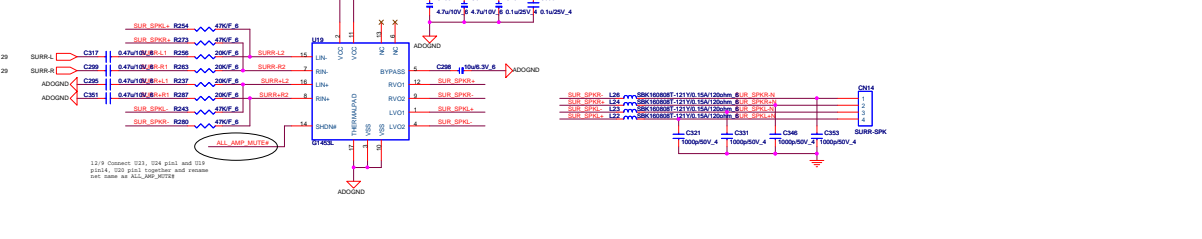
LINE-OUT/SPDIFO



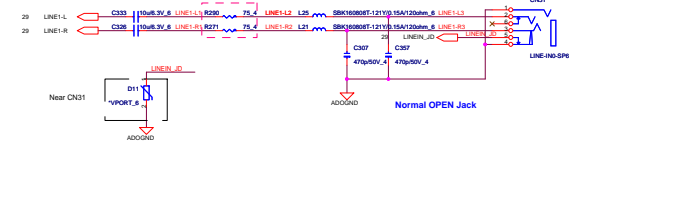
Main SPK/Center/Subwoofer



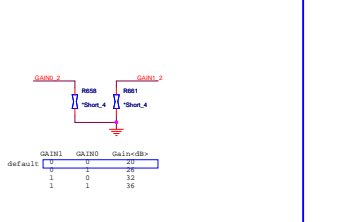
SURR-SPK



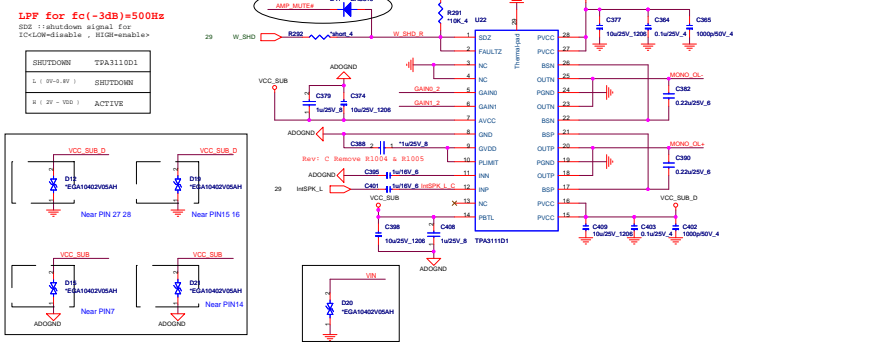
LINE IN



AMO GAIN



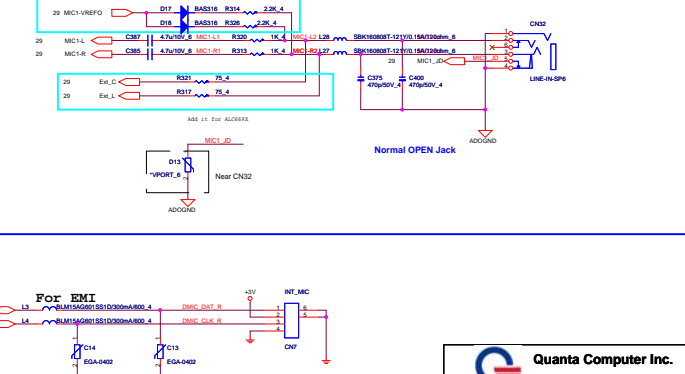
SUBWOOFER



SUBWOOFER Power(AMP)

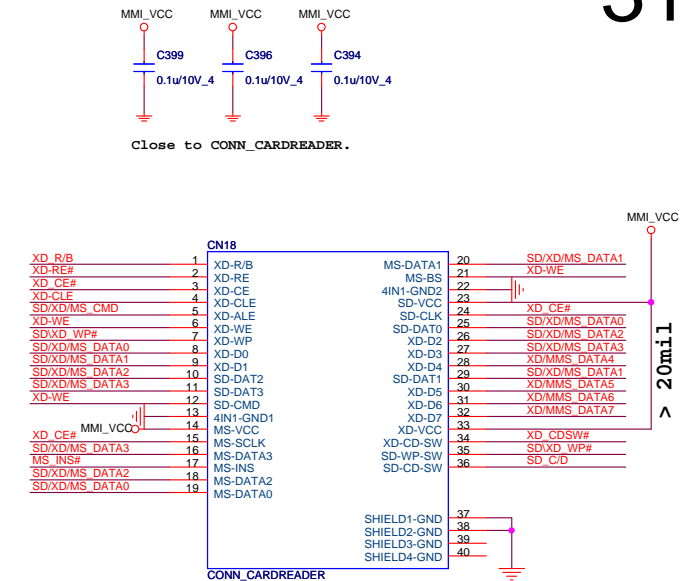
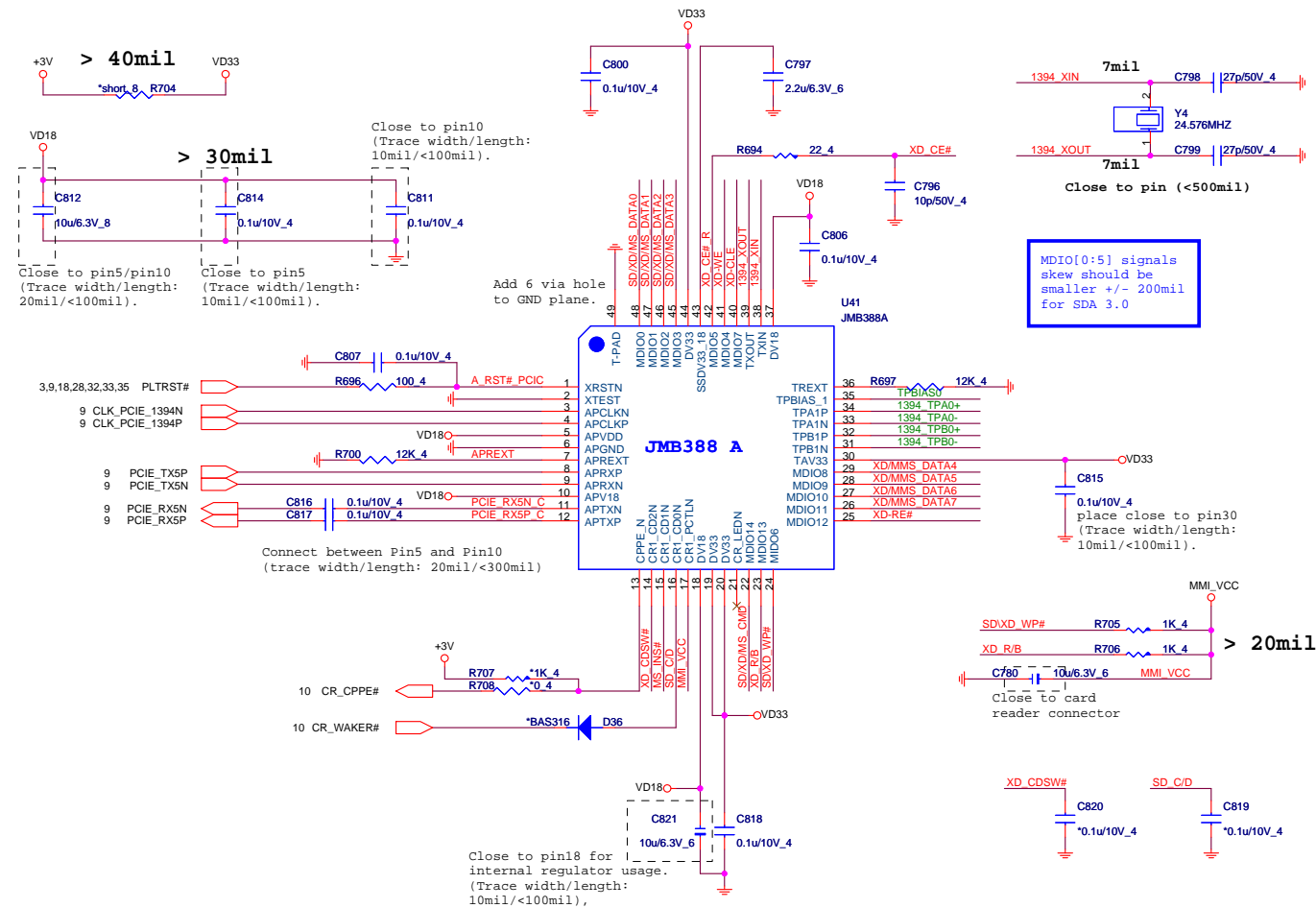


MIC

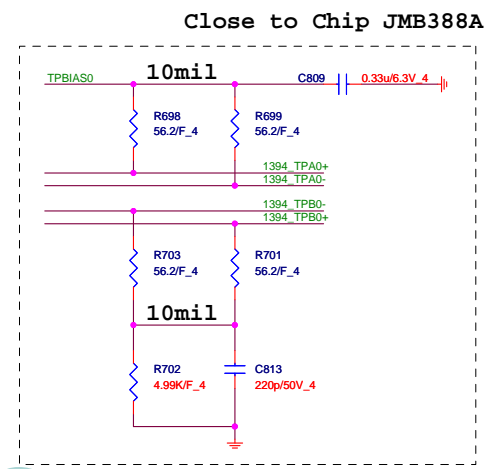


# Card Reader (JMB388A)

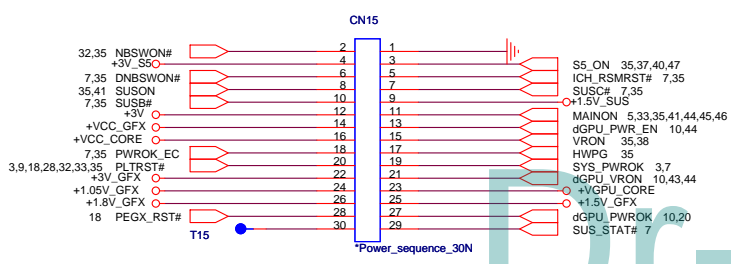
Chip Note:  
 1. All component must be closed to chip.  
 2. APREXT(pin7) & TREXT(pin36) trace width/length: 10mil/< 250mil



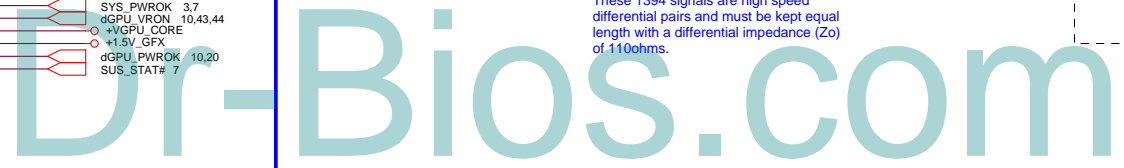
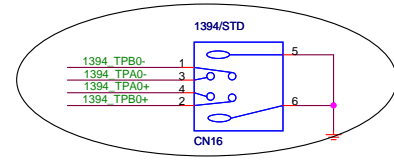
1394 [FIW]



## Power sequence



1/6 change 1394 connector fp and pin assignment

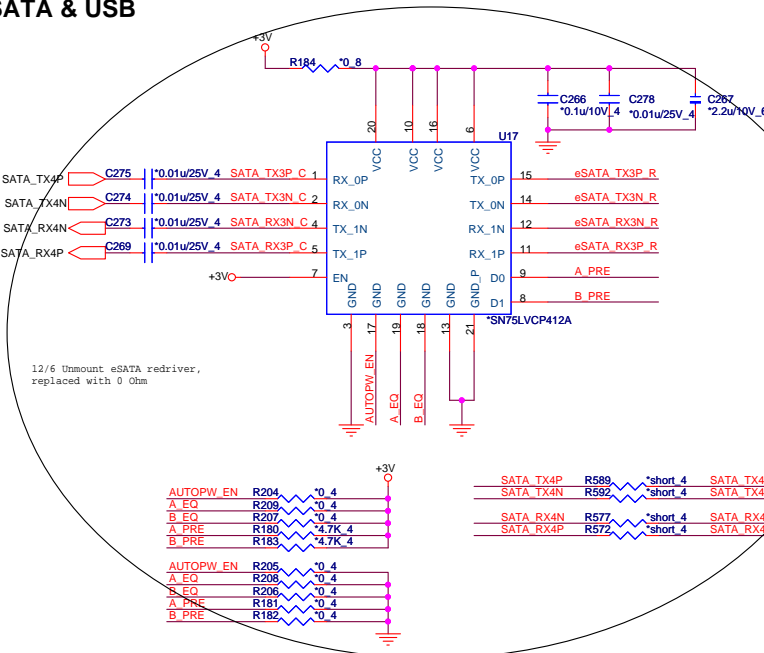


AL008511001

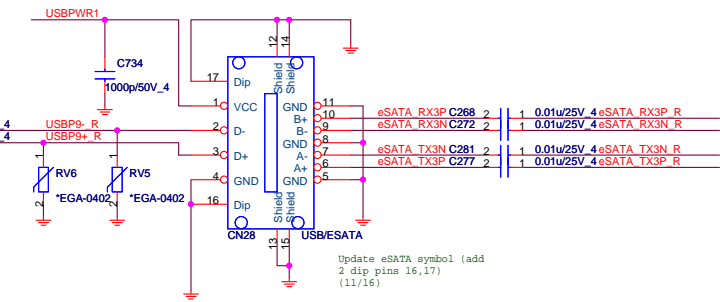
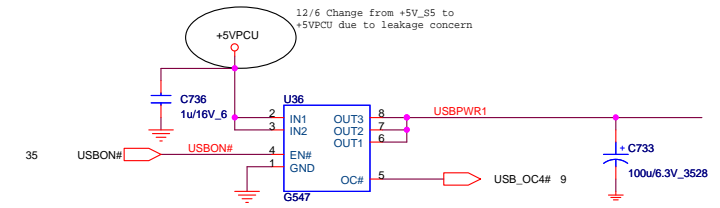
EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

ALLVC412000

EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

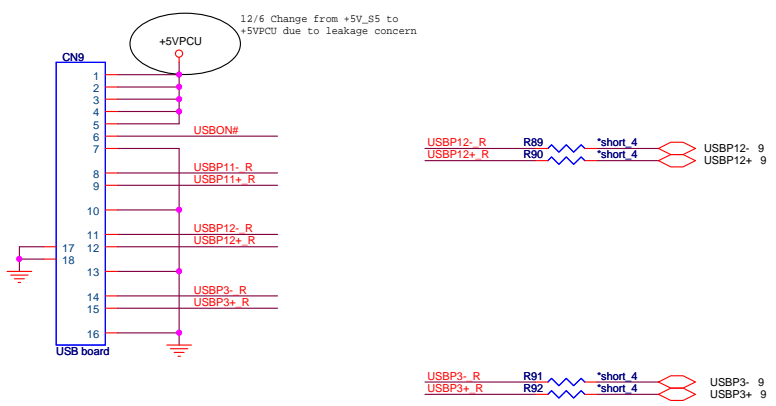


12/6 Unmount eSATA redriver, replaced with 0 Ohm

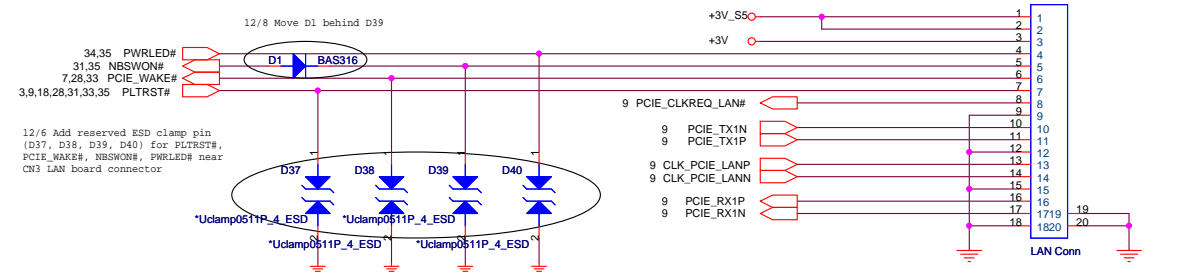


Update eSATA symbol (add 2 dip pins 16,17) (11/16)

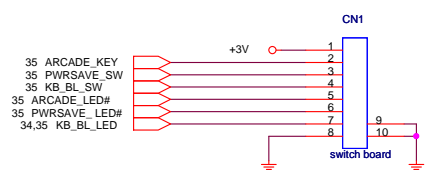
To USB DB



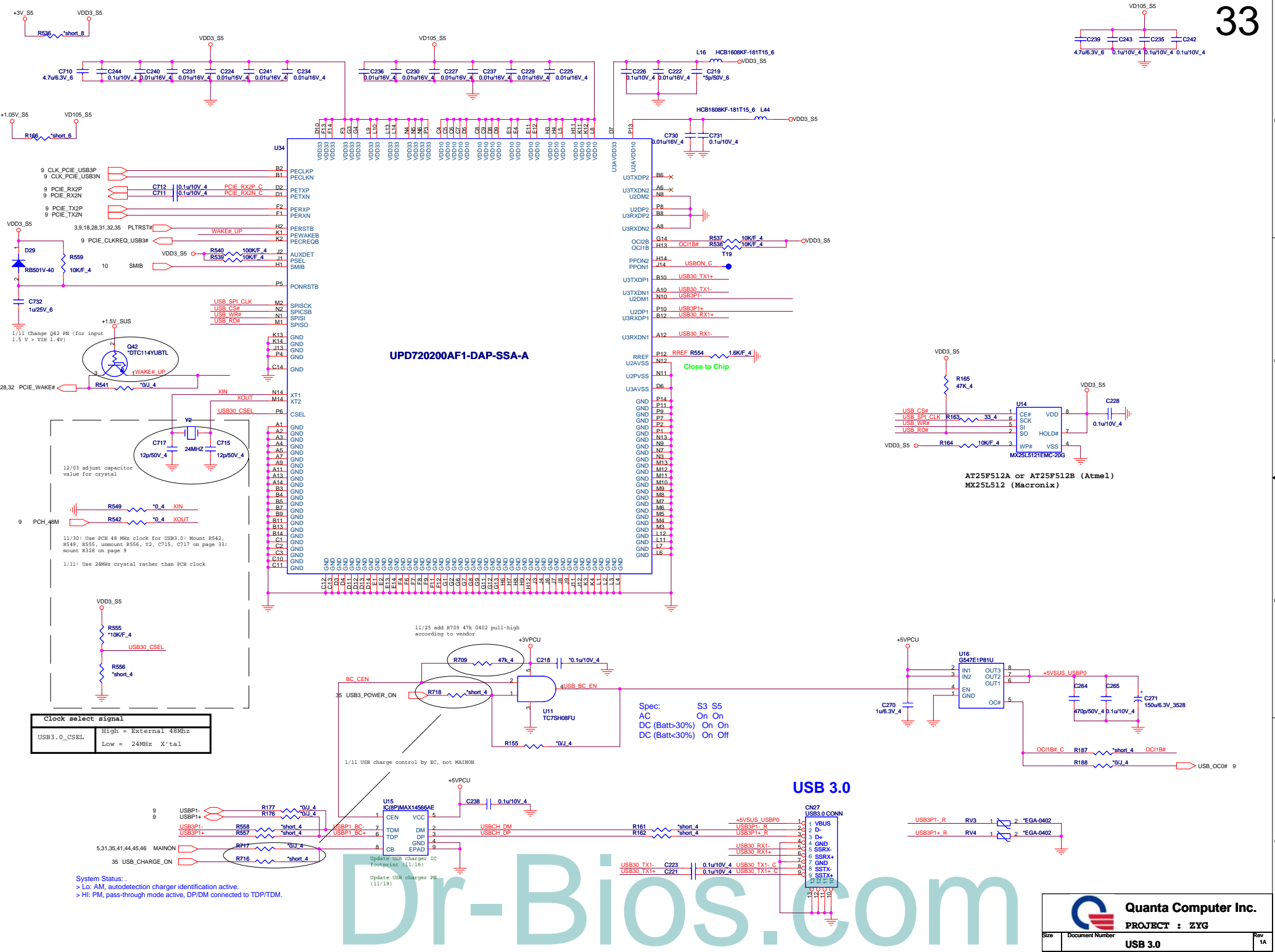
To PWR/LAN DB



To SW DB







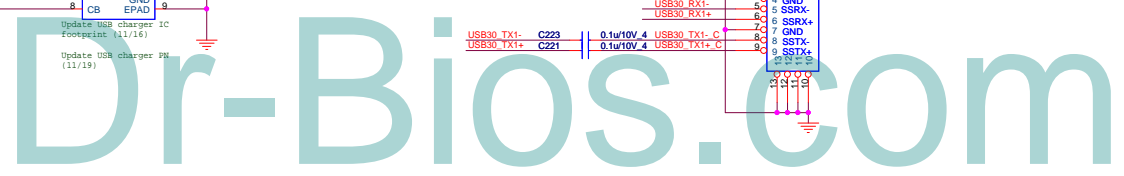
UPD72020AF1-DAP-SSA-A

USB 3.0

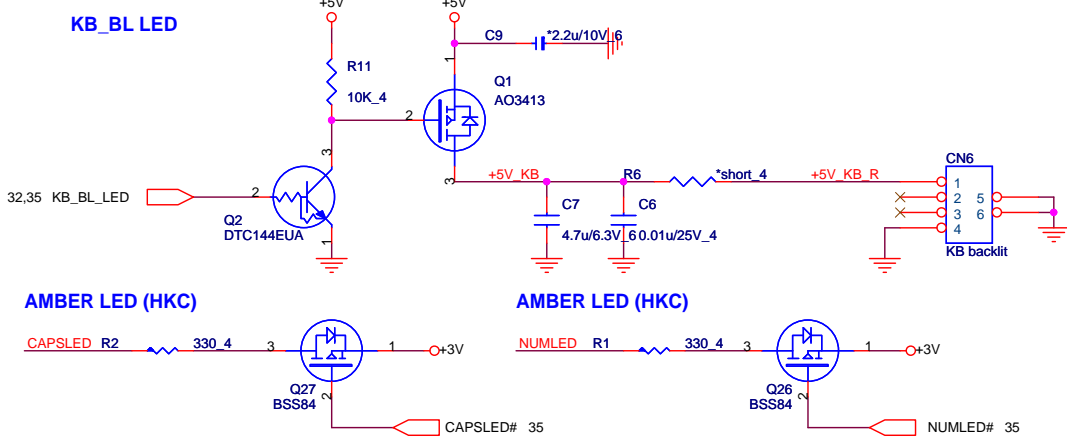
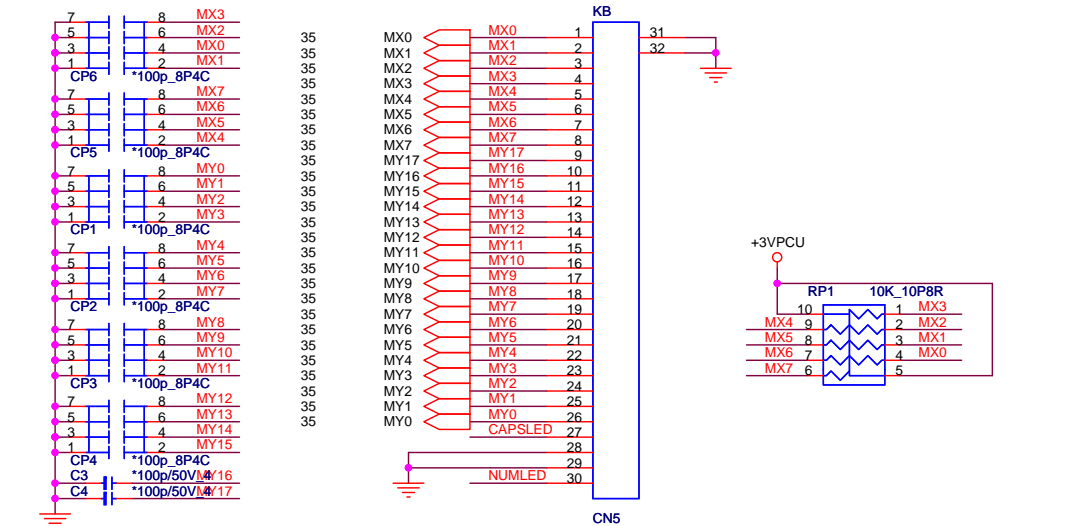
Clock select signal	
High = External 48Mhz	
Low = 24Mhz X'tal	

Spec: S3 S5  
 AC On On  
 DC (Batt>30%) On On  
 DC (Batt<30%) On Off

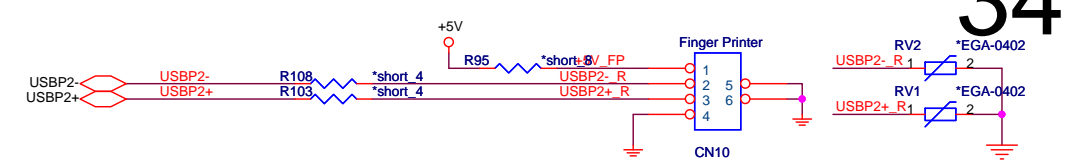
System Status :  
 > Lo: AM, autodetection charger identification active.  
 > Hi: PM, pass-through mode active, DP/DM connected to TDP/TDM.



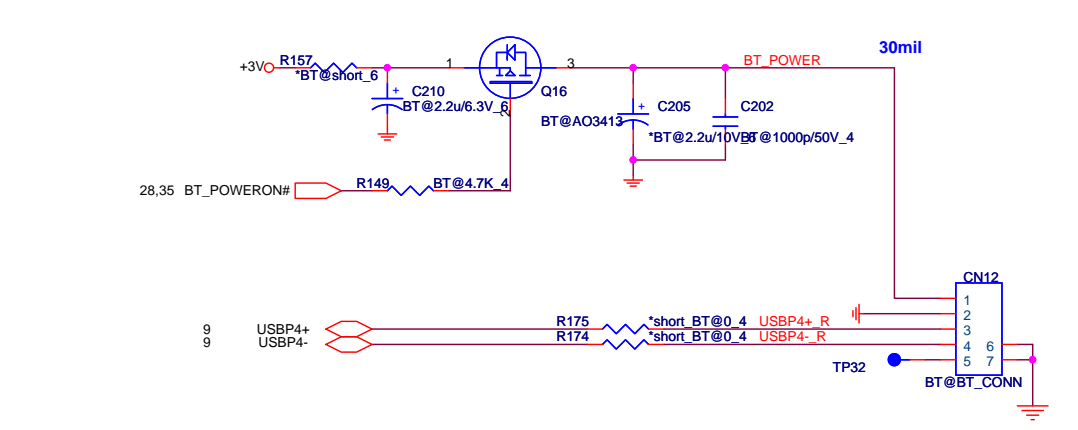
### INT K/B



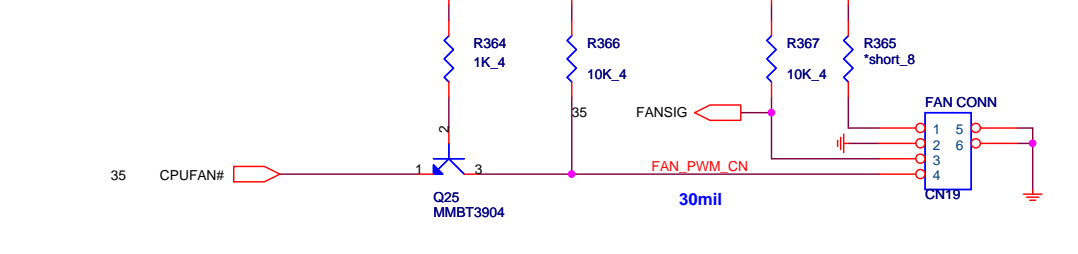
### Finger-Printer



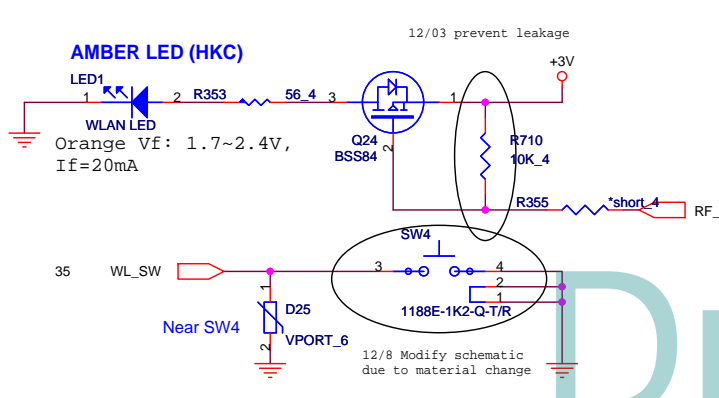
### BLUETOOTH



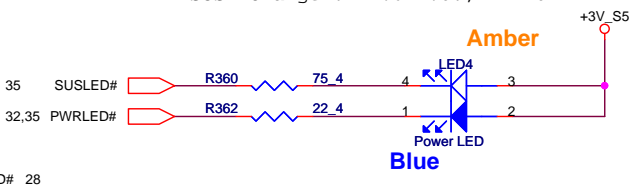
### CPU FAN



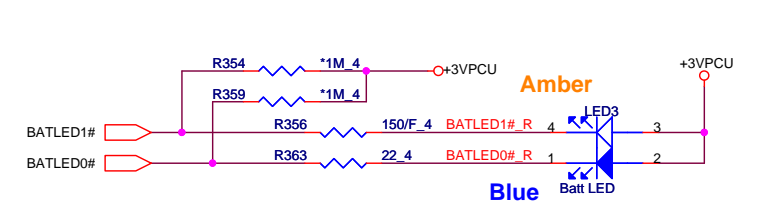
### WL LED



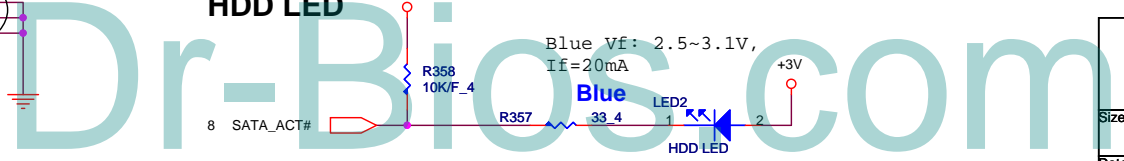
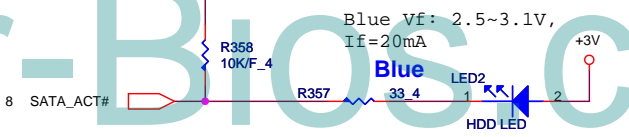
### PWR LED



### Battery LED



### HDD LED

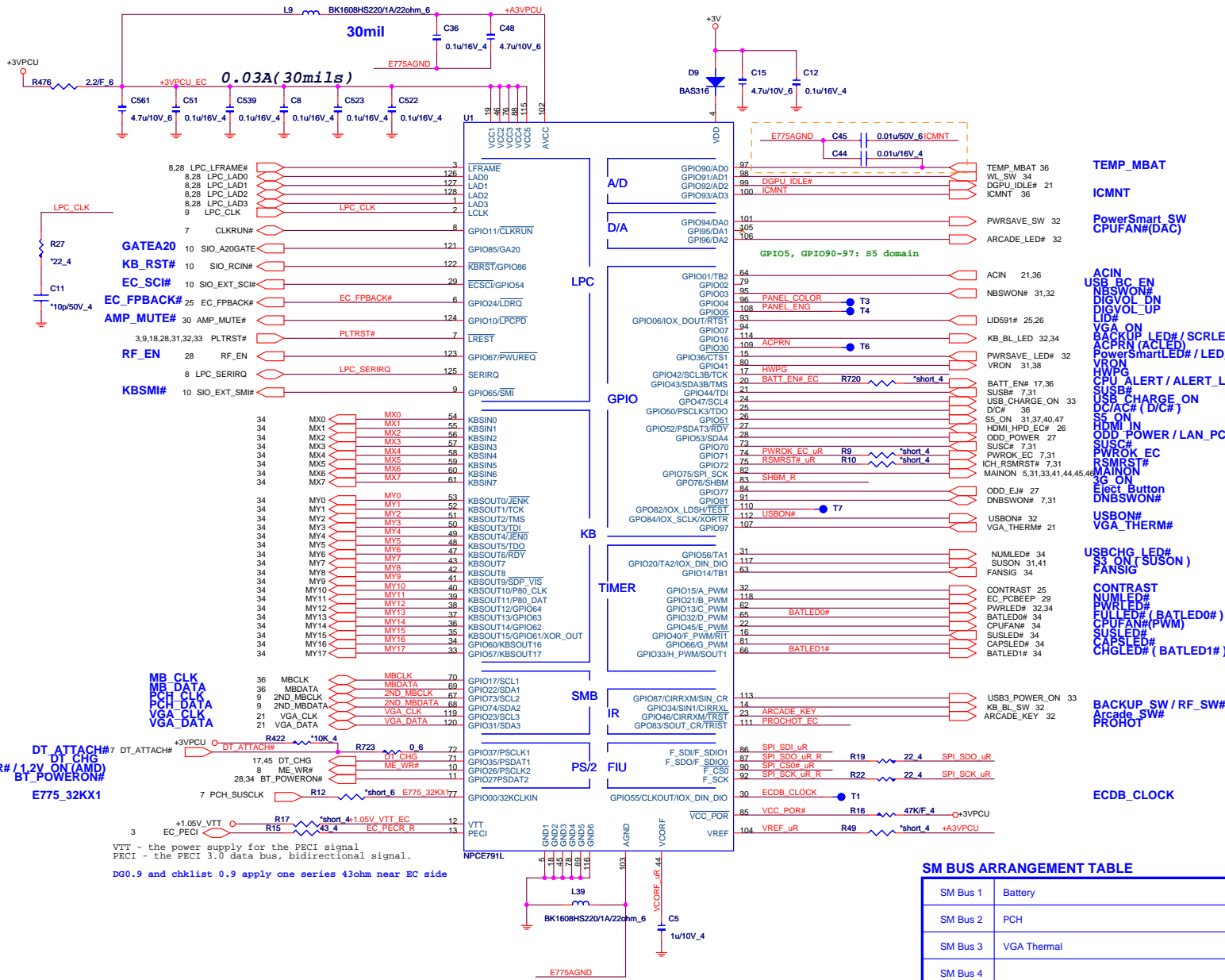


**Quanta Computer Inc.**  
PROJECT : ZYG

Size	Document Number	Rev
		1A

**KB/FAN/FP/BT/LED**

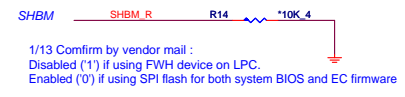
Date: Tuesday, February 22, 2011 Sheet 34 of 50



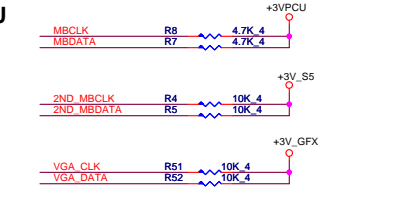
I/O ADDRESS SETTING

I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS



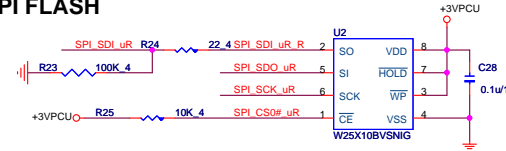
SM BUS PU



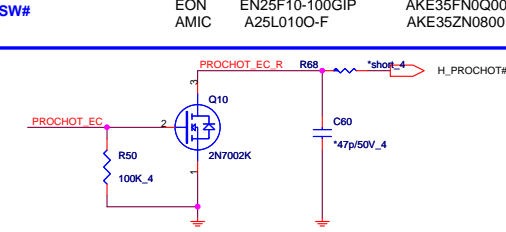
INTERNAL KEYBOARD STRIP SET



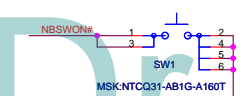
SPI FLASH

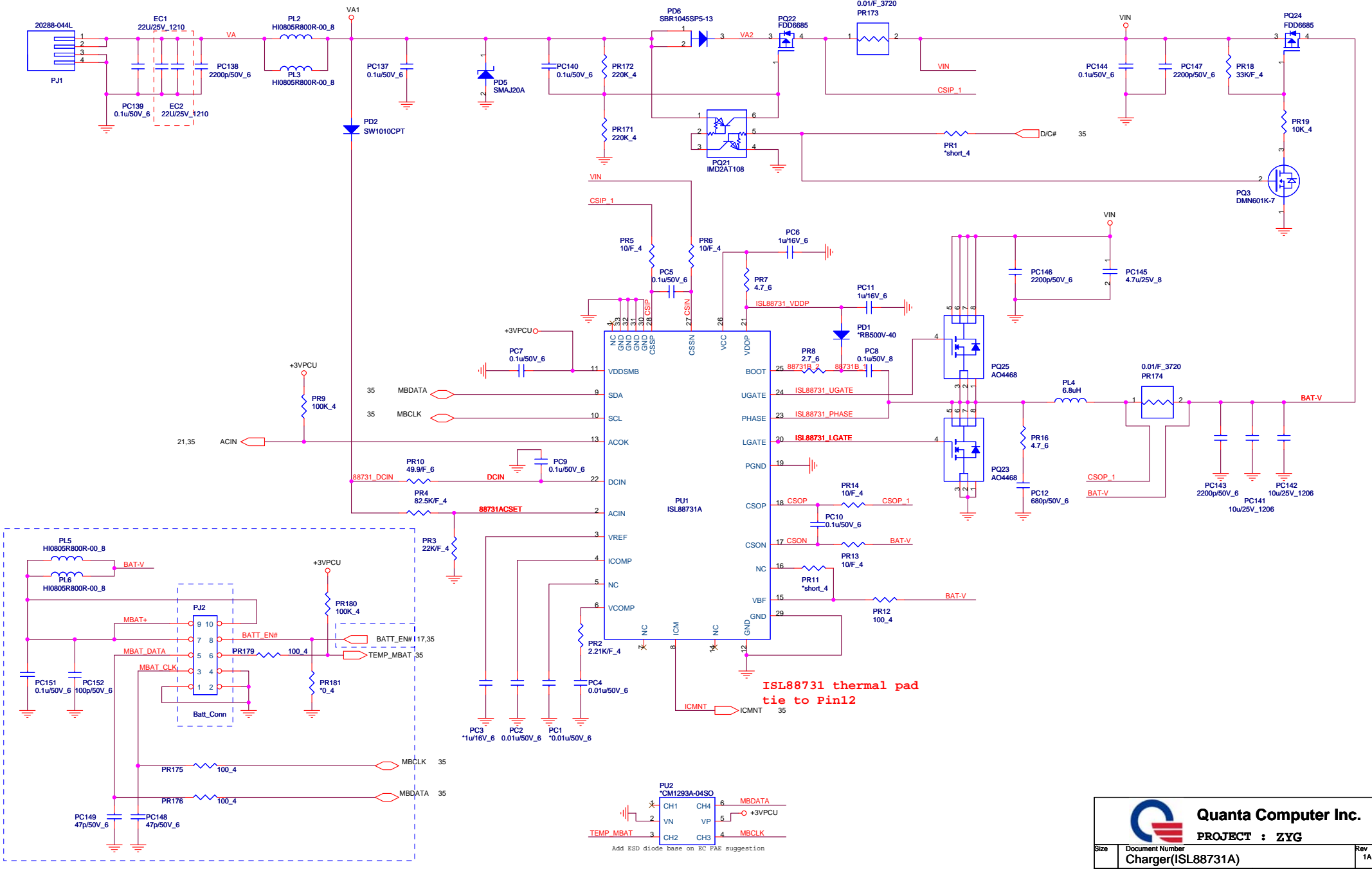


HWPG

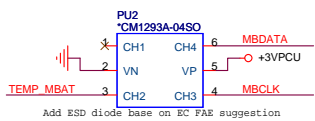


POWER-ON Switch





ISL88731 thermal pad tie to Pin12



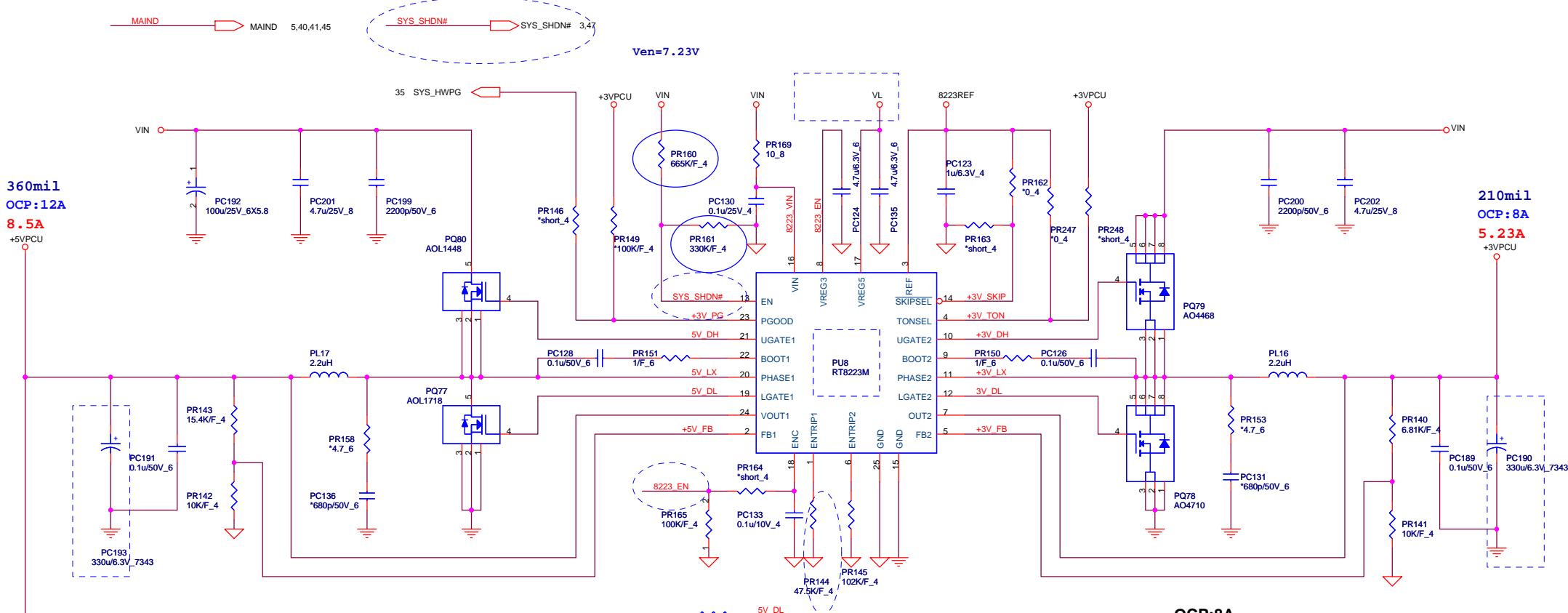
Add ESD diode base on EC FAE suggestion

		<b>Quanta Computer Inc.</b> <b>PROJECT : ZYG</b>	
Date: Tuesday, February 22, 2011		Charger (ISL88731A)	
Sheet		36 of 50	
Rev		1A	

360mil  
OCP:12A  
8.5A

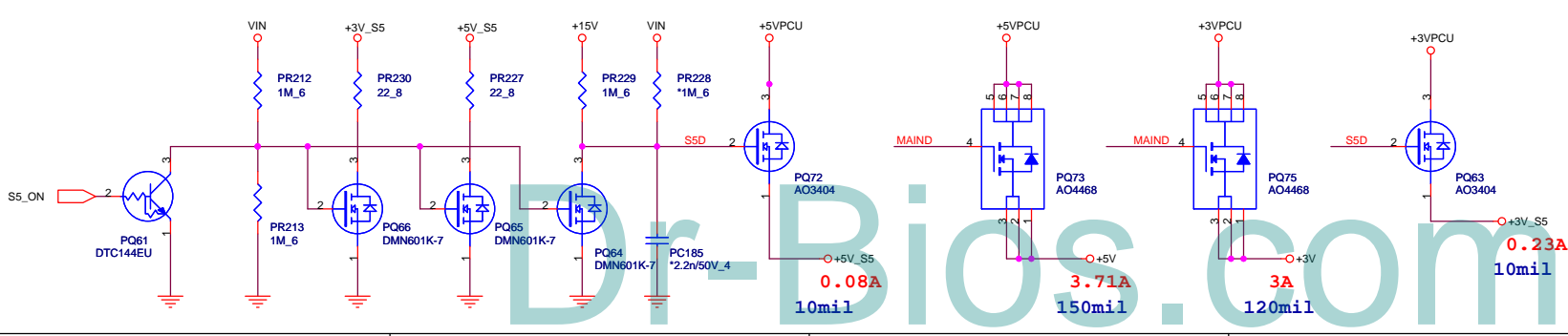
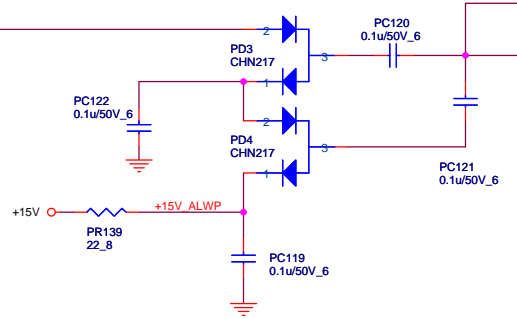
210mil  
OCP:8A  
5.23A

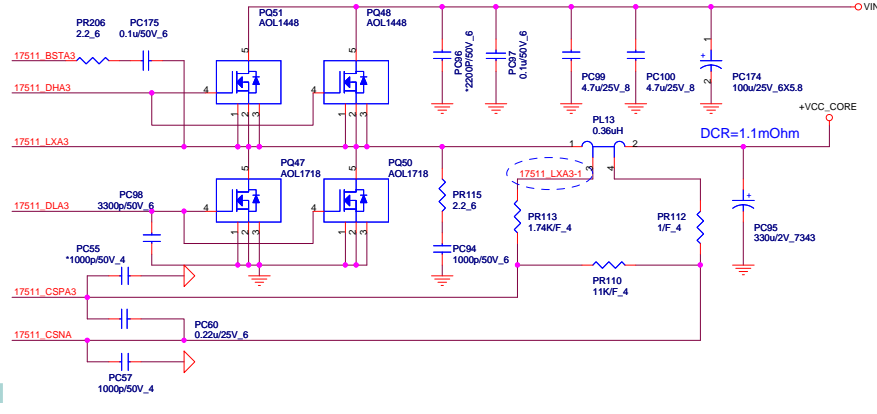
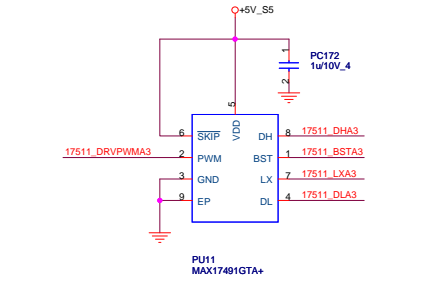
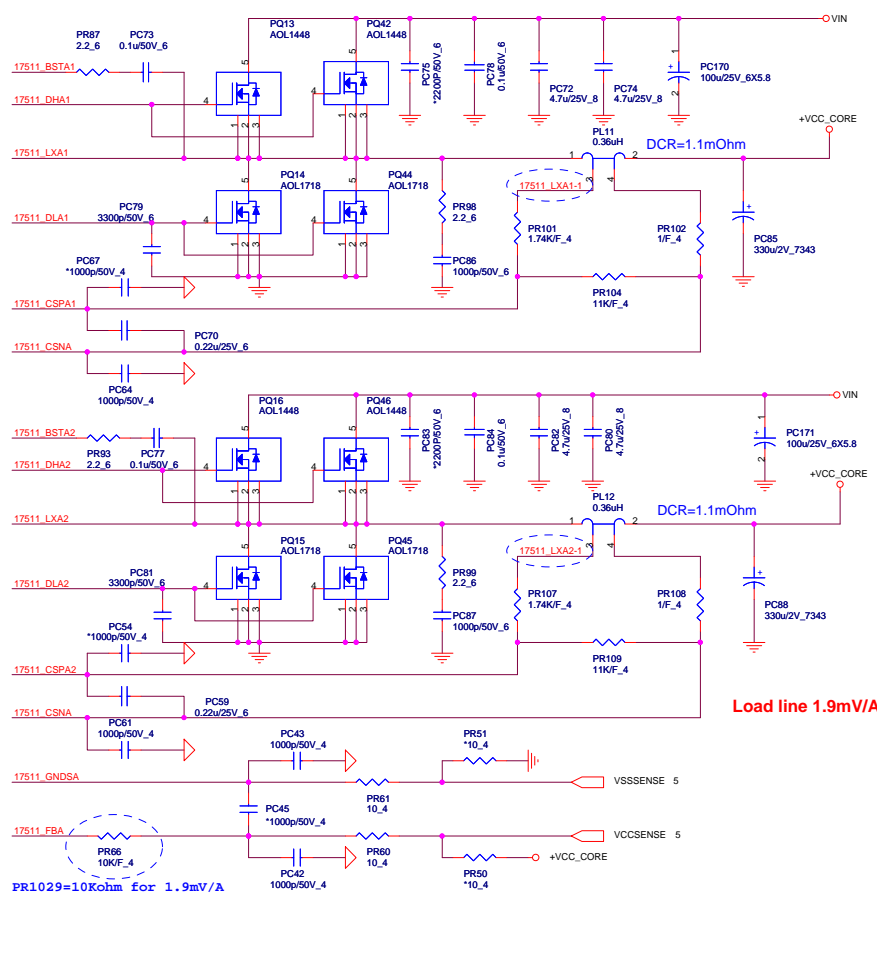
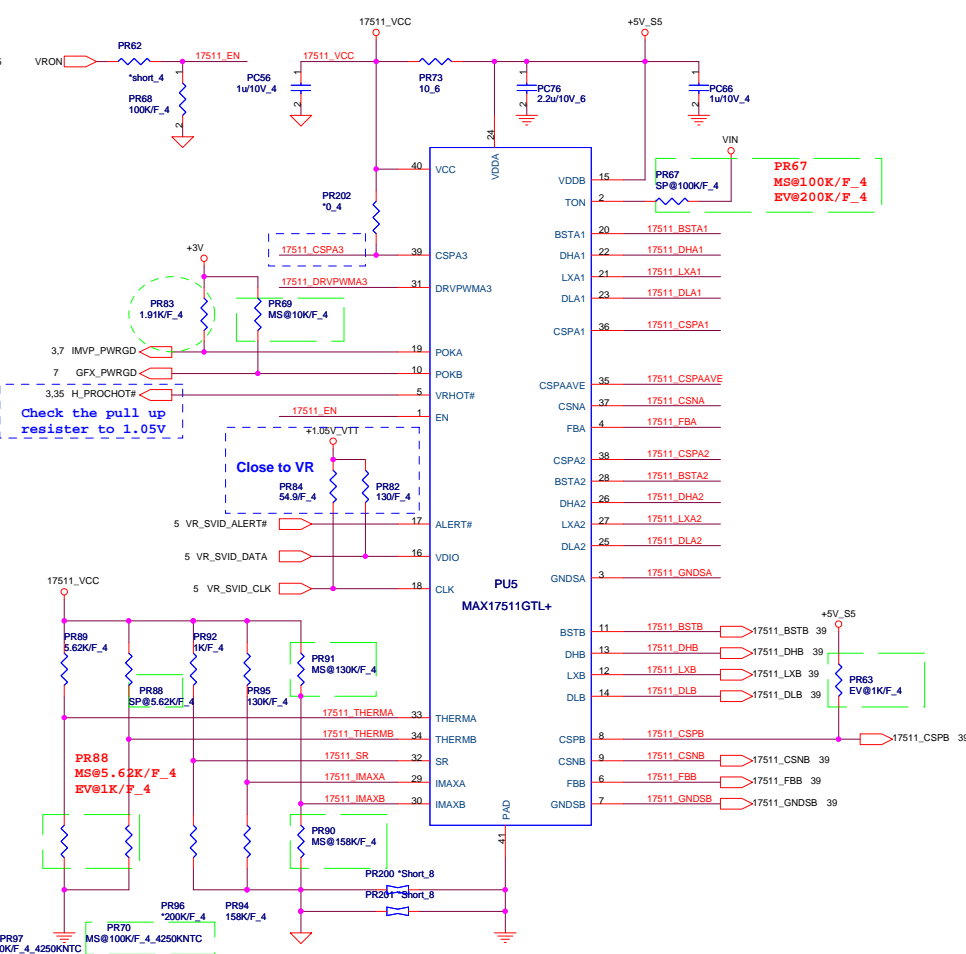
Ven=7.23V



**OCP:12A**  
 $L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 9) = 2.525\text{A}$   
 $I_{ocp} = 12 - (2.525/2) = 10.74\text{A}$   
 $V_{th} = 10.74\text{A} \cdot 4.3\text{m}\Omega = 46.17\text{mV}$   
 $R(\text{Ilim}) = (46.17\text{mV} \cdot 10) / 10\mu\text{A} \sim 46.17\text{K}$

**OCP:8A**  
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 9) \sim 1.9\text{A}$   
 $I_{ocp} = 8 - (1.9/2) = 7.05\text{A}$   
 $V_{th} = 7.05\text{A} \cdot 14.2\text{m}\Omega = 100.11\text{mV}$   
 $R(\text{Ilim}) = (100.11\text{mV} \cdot 10) / 10\mu\text{A} = 100.11\text{K}$

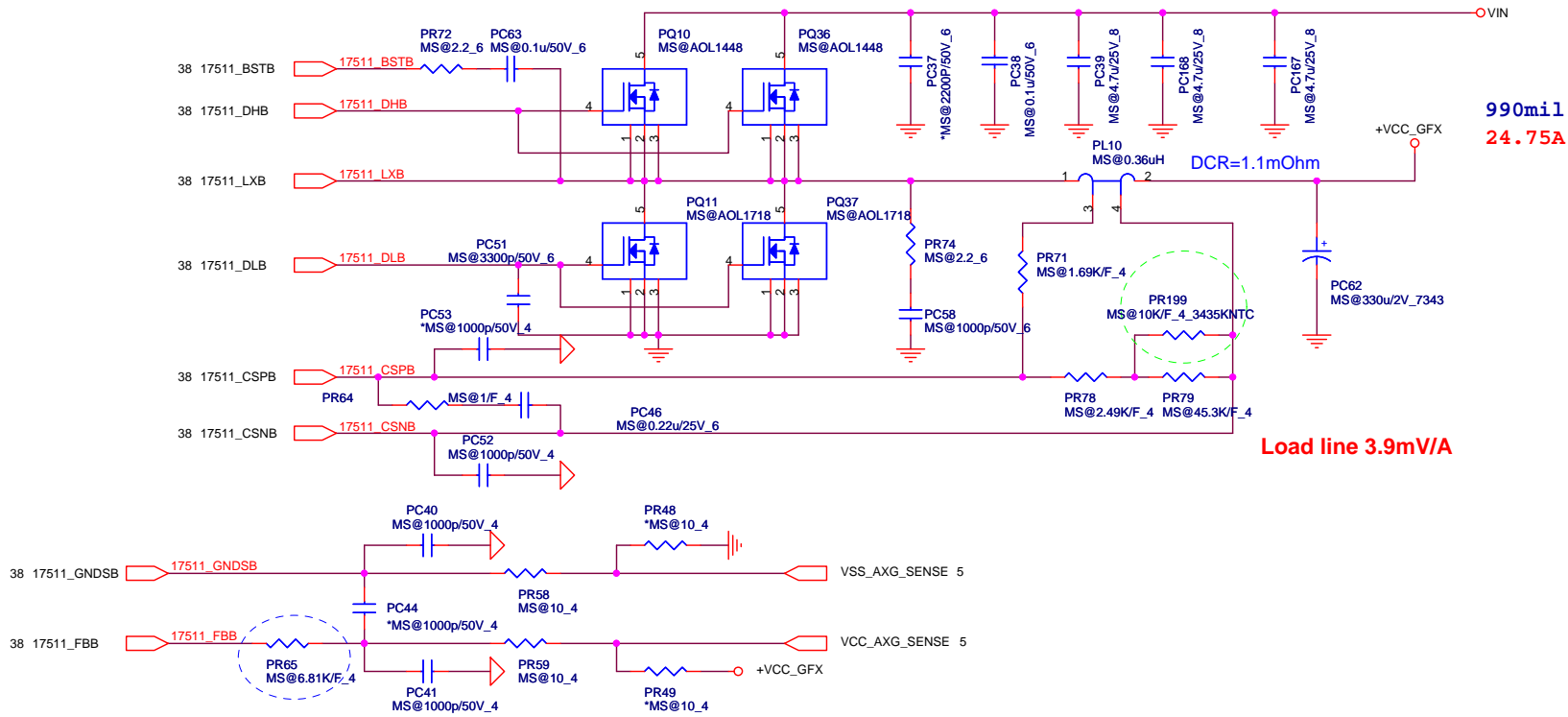




MS@ for Internal VGA (+VCC\_GFX enable)  
 EV@ for External VGA (+VCC\_GFX disable discrete only)  
 SP@ for IV@or EV@ selection  
 QC@ for Quad core CPU

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**Quanta Computer Inc.**  
**PROJECT : ZYG**  
**+VCC\_CORE (MAX17511)**  
 Size Document Number Rev 1A  
 Date: Tuesday, February 22, 2011 Sheet 38 of 50



PR1047=6.81Kohm is 3.9mV/A for GT2 GFX

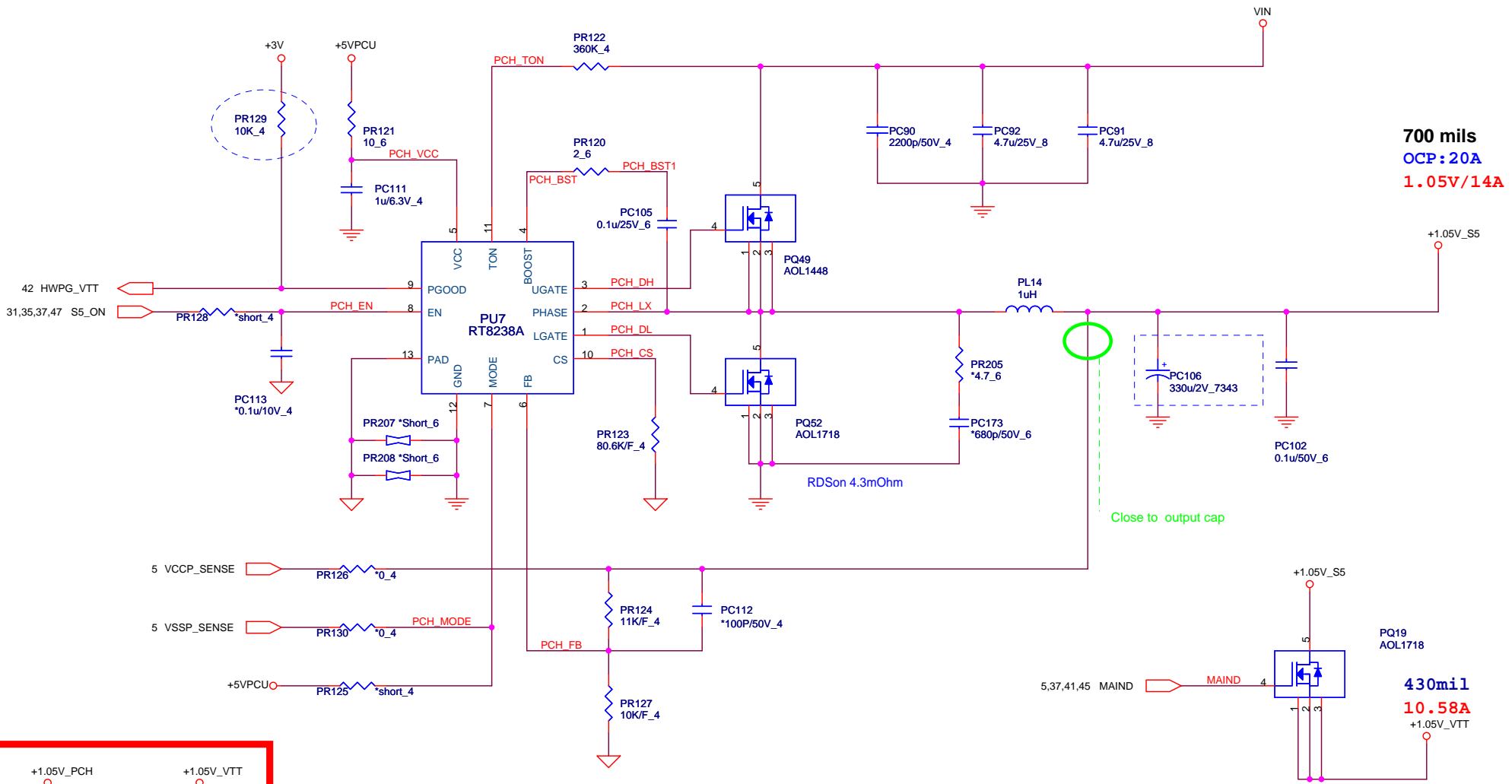
	Dual Core (35W)	Quad Core (45W)
CPU Conver	2-Phase	3-Phase
PR202	Populated	NC
PR95	150K/F_4 (CS41502FB18)	130K/F_4 (CS41302FB00)
PR94	200K/F_4 (CS42002FB12)	158K/F_4 (CS41582FB14)
PR111	NC	5.11K/F_4 (CS25112FB15)
PR100	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)
PR106	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)

	UMA (IV@) / Muxless (MS@)	External VGA (EV@)
PR63	NC	Populated
PR67	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR91	130K/F_4 (CS41302FB00)	NC
PR90	158K/F_4 (CS41582FB14)	NC
PR88	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR69	Populated	NC
PR70	Populated	NC



**Quanta Computer Inc.**  
PROJECT : ZYG

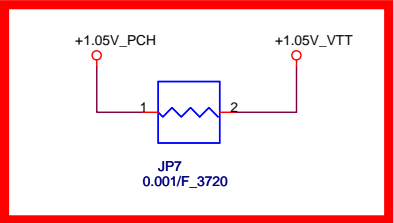
Size	Document Number	Rev
	<b>+VCC_GFX (MAX17511)</b>	1A
Date:	Tuesday, February 22, 2011	Sheet 39 of 50



**700 mils**  
**OCP : 20A**  
**1.05V/14A**

Close to output cap

**430mil**  
**10.58A**  
**+1.05V\_VTT**

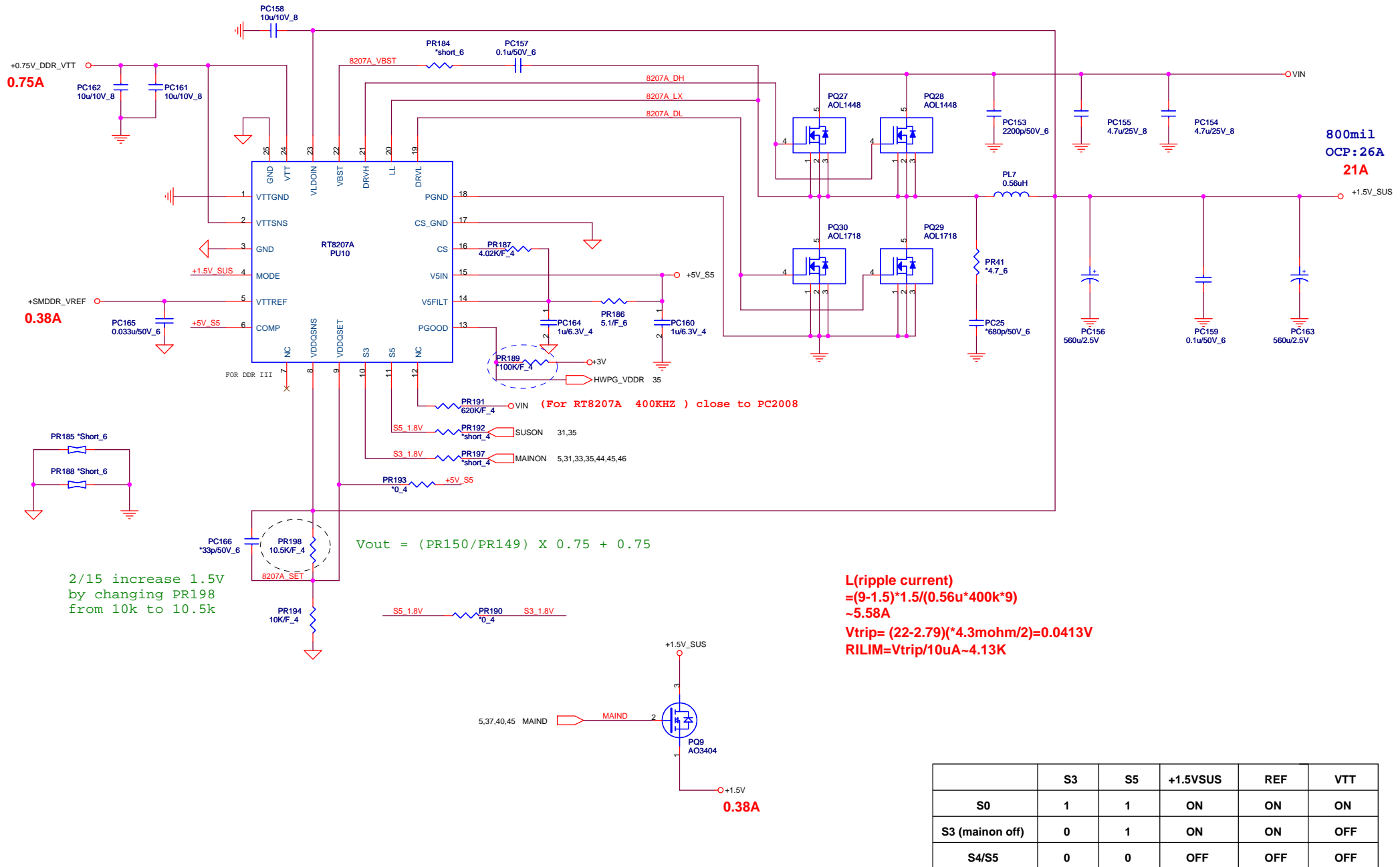


$$V_{OUT} = (1 + R_1/R_2) * 0.5$$

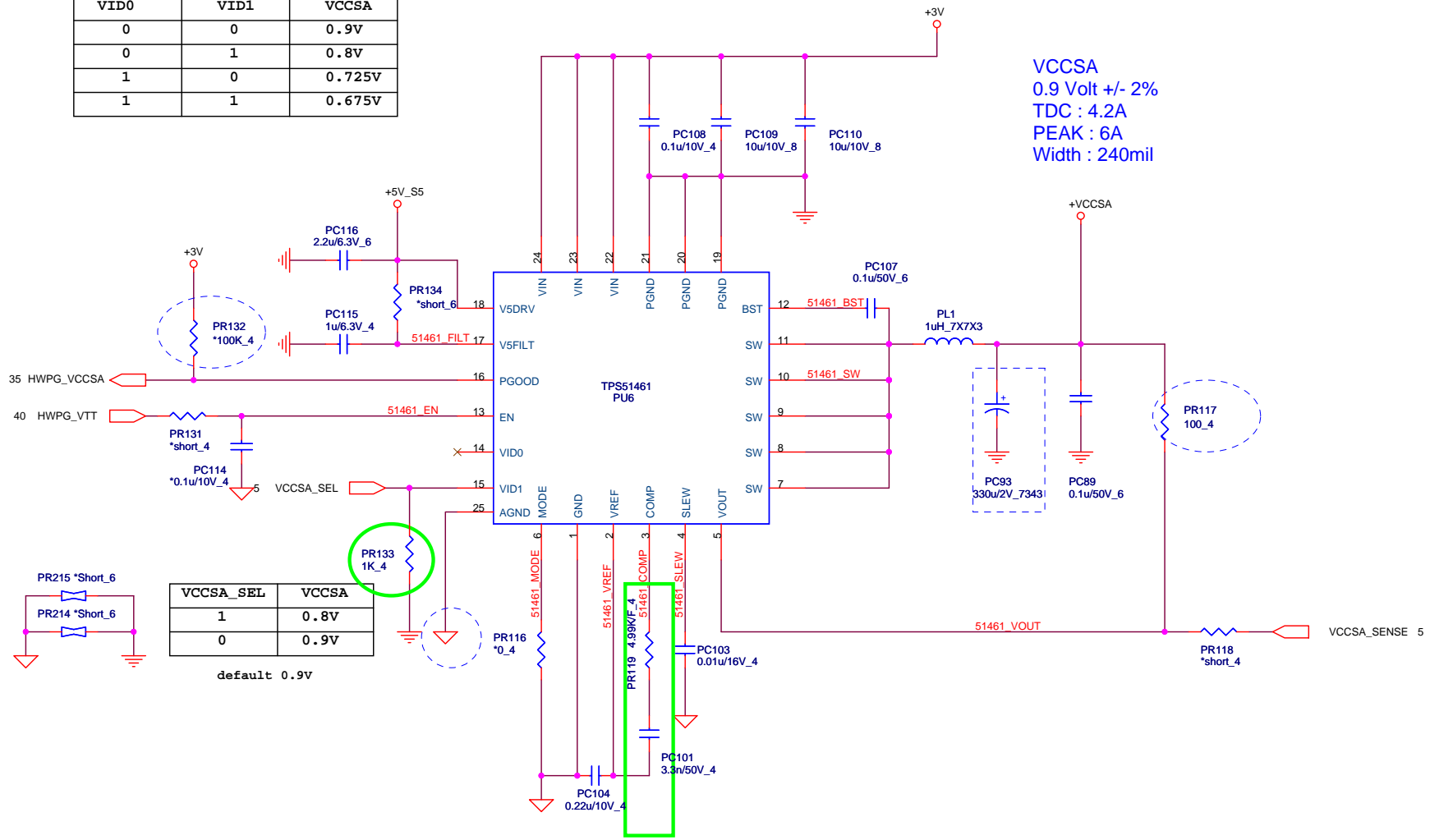
**Quanta Computer Inc.**  
**PROJECT : ZYG**

Size	Document Number	Rev
	<b>+PCH&amp;VTT (RT8238A)</b>	1A
Date: Tuesday, February 22, 2011	Sheet	40 of 50





VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



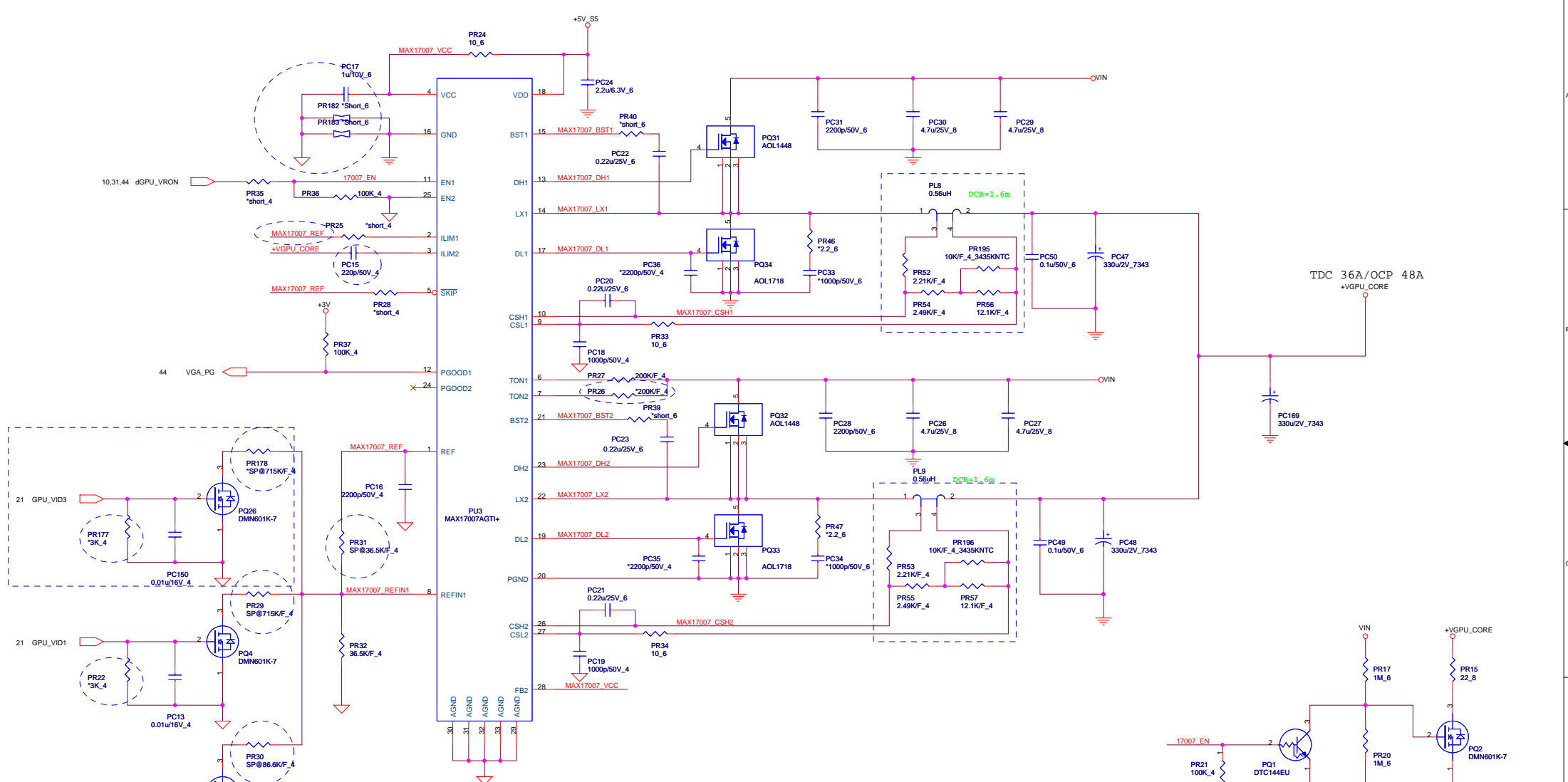
VCCSA  
 0.9 Volt +/- 2%  
 TDC : 4.2A  
 PEAK : 6A  
 Width : 240mil

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

**Quanta Computer Inc.**  
 PROJECT : ZYG

Size	Document Number	Rev
	VCCSA(TPS51461)	1A
Date:	Tuesday, February 22, 2011	Sheet 42 of 50

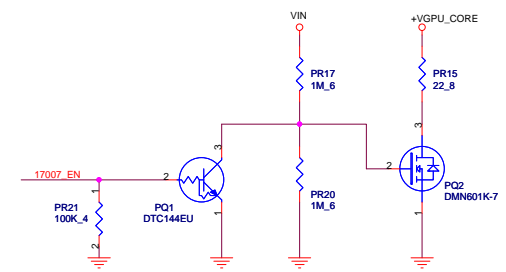


Default is 12P-GS

GPU_VID2	GPU_VID1	+VGPU_CORE (12P-GS / 12E-GE)
0	0	1.0V / 0.9125V
0	1	0.975V / 0.8625V
1	0	0.825V / 0.8125V

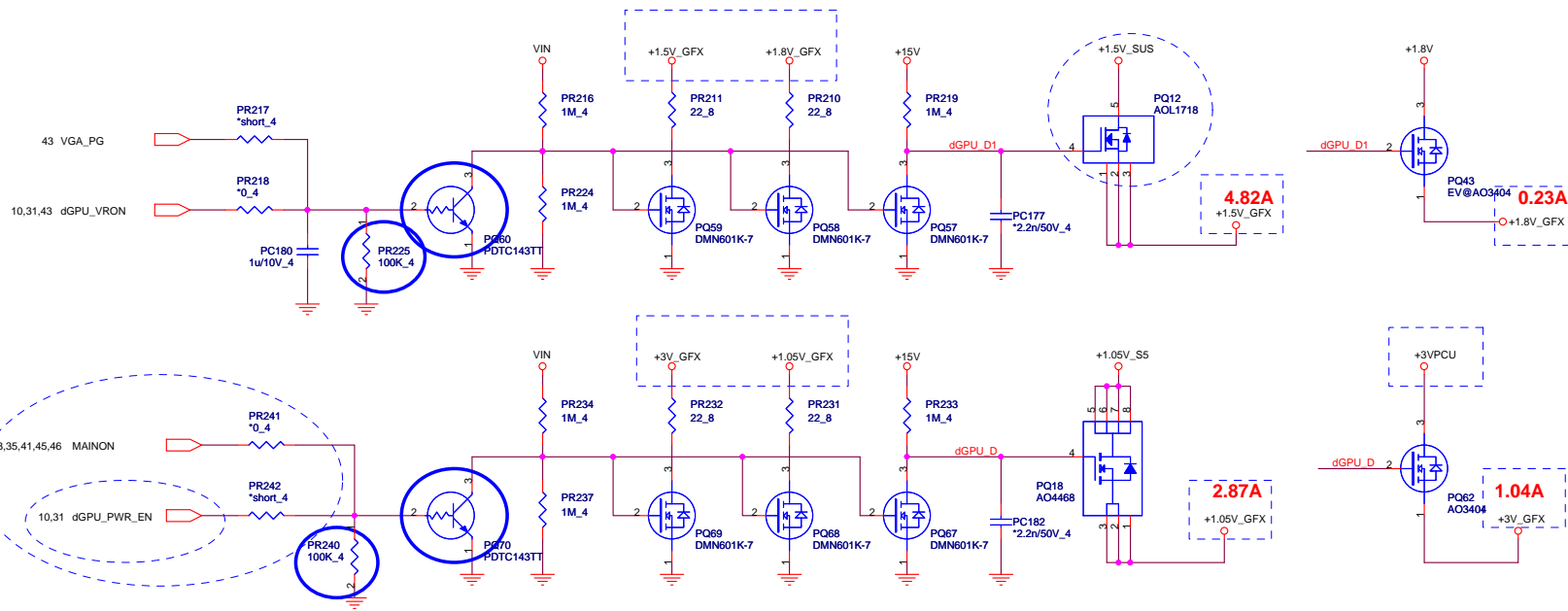
Default is 12P-GS

location	12P-GS	12E-GE
PR31	36.5K/F CS33652FB18	43.2K/F (CS34322FB16)
PR29	715K/F CS47152FB00	332K/F (CS43322FB15)
PR30	86.6K/F CS38662FB16	158K/F (CS41582FB14)

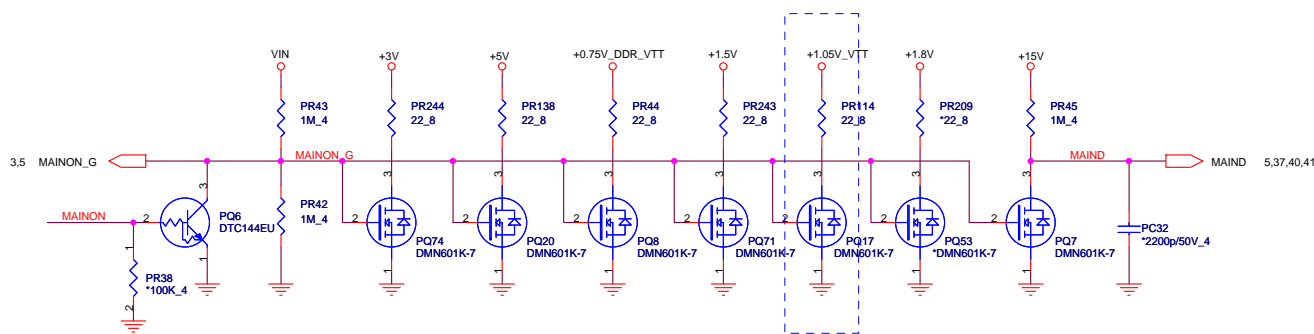
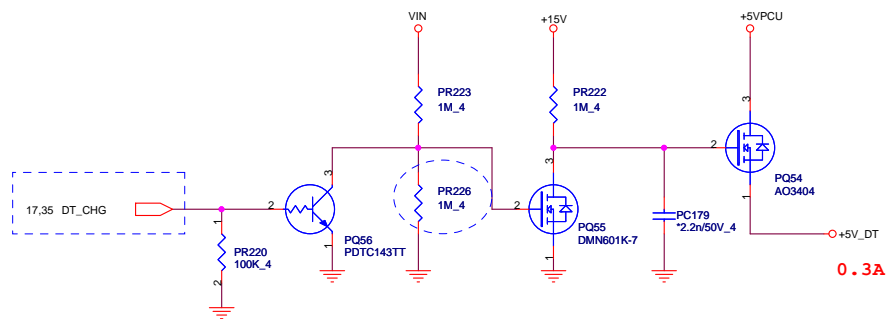
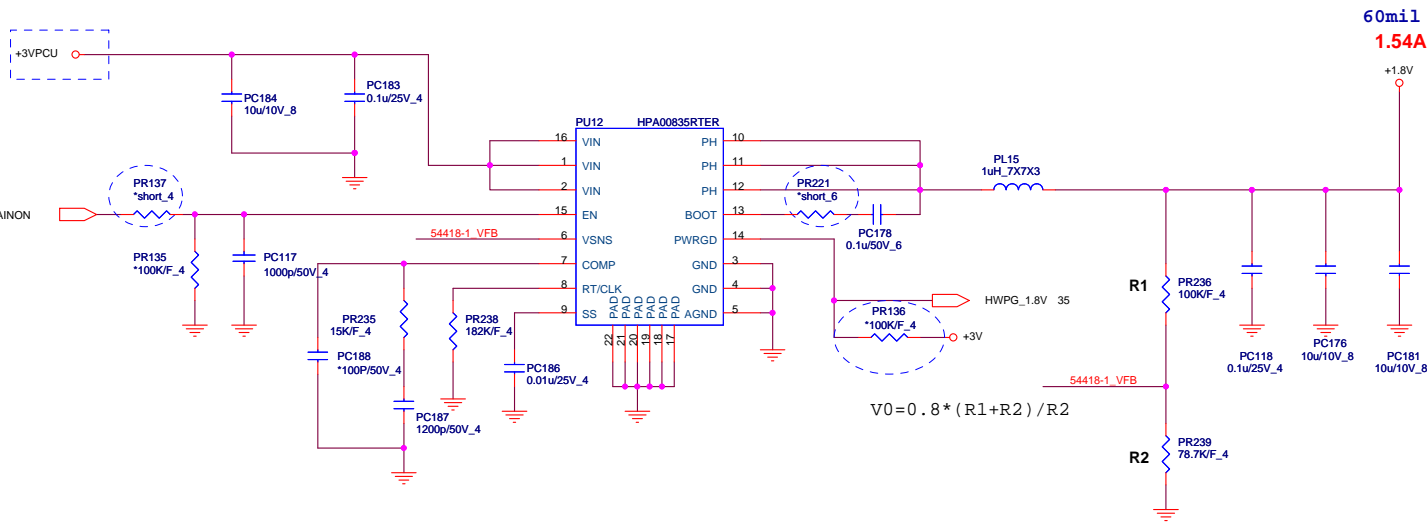


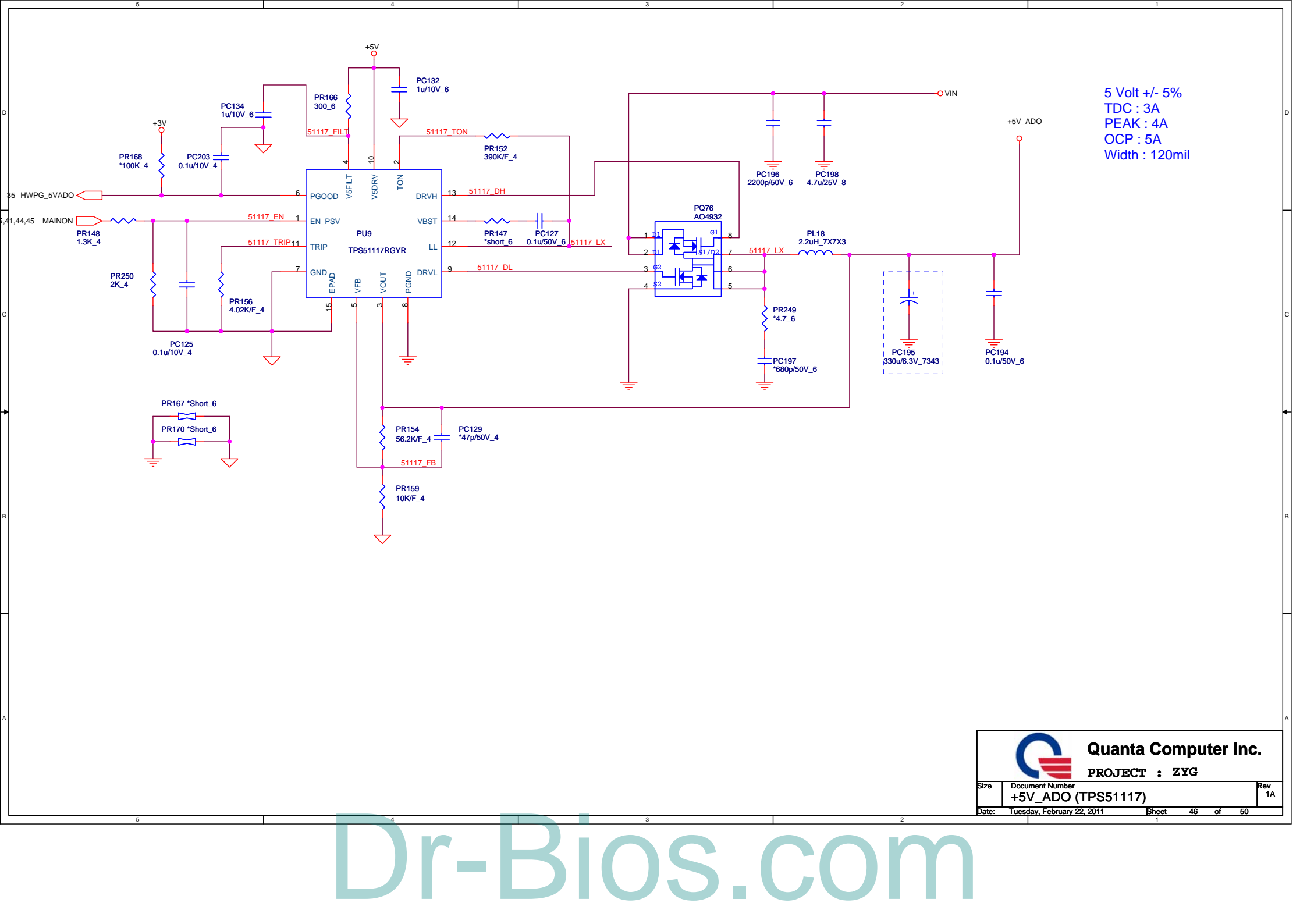
**Quanta Computer Inc.**  
**PROJECT : ZYG**

Size: Document Number: **GPU CORE(MAX17007)** Rev: 1A  
 Date: Tuesday, February 22, 2011 Sheet: 43 of 50




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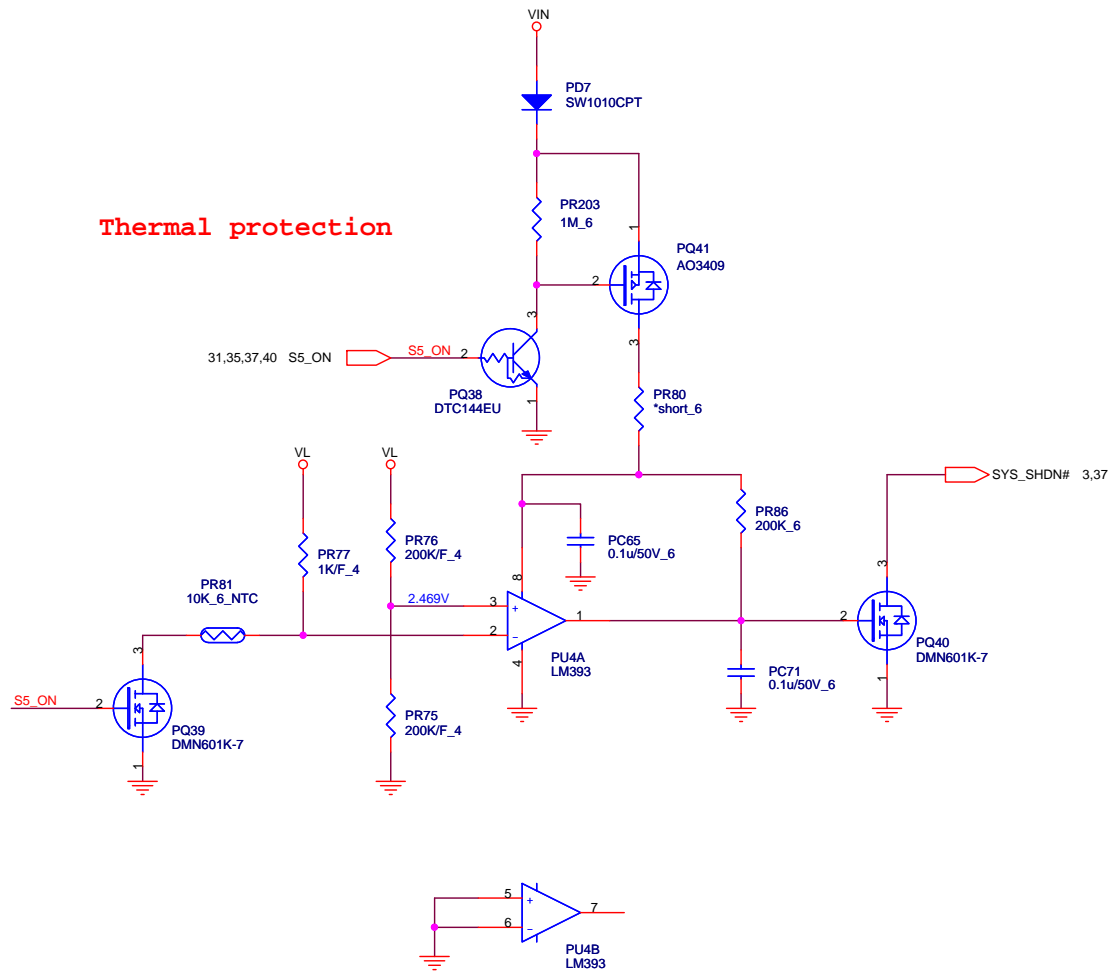


5 Volt +/- 5%  
 TDC : 3A  
 PEAK : 4A  
 OCP : 5A  
 Width : 120mil


 <b>Quanta Computer Inc.</b> PROJECT : ZYG		Size	Document Number	Rev
			<b>+5V_ADO (TPS51117)</b>	1A
Date:	Tuesday, February 22, 2011	Sheet	46	of 50

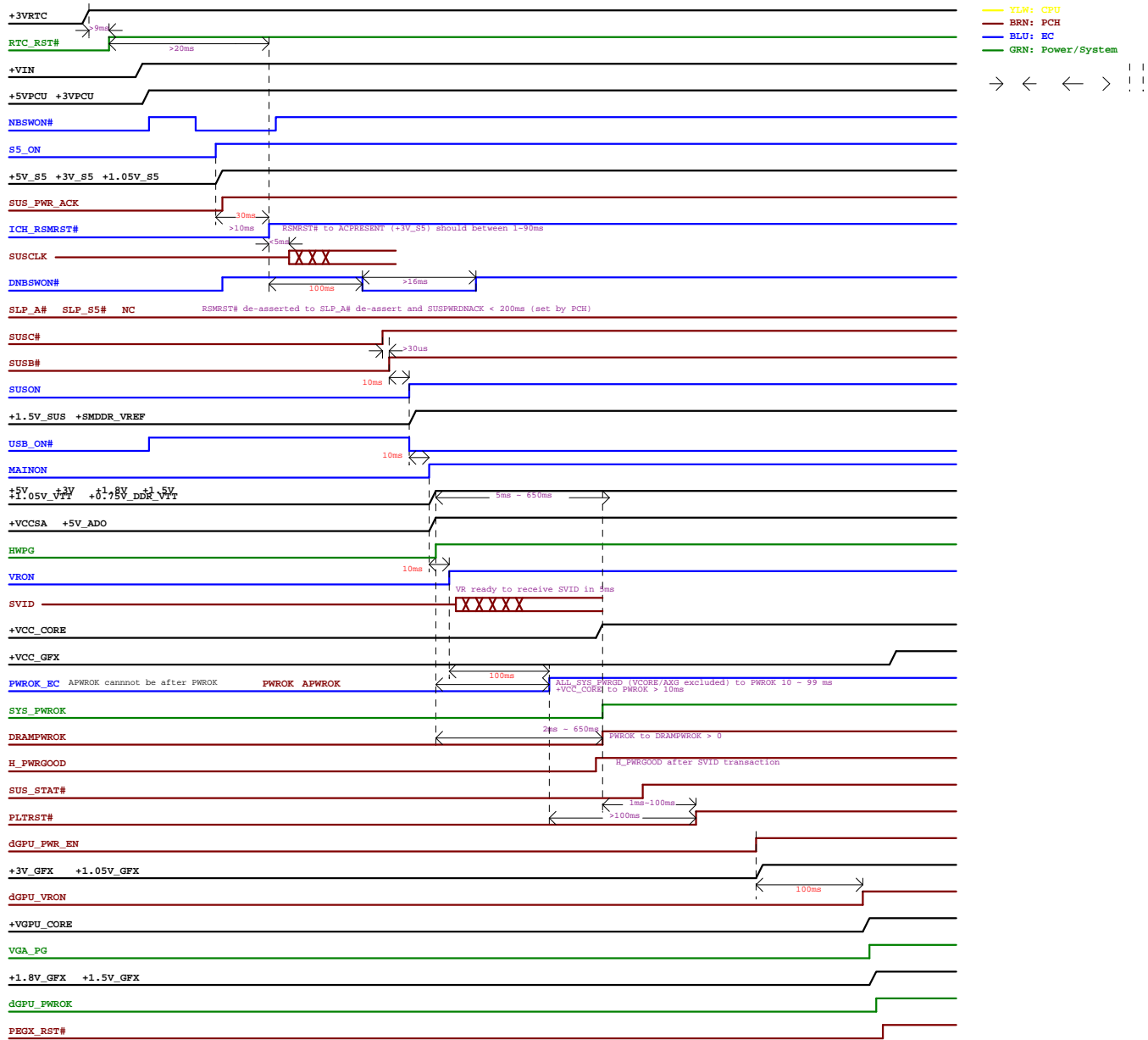
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Thermal protection



For EC control thermal protection (output 3.3V)

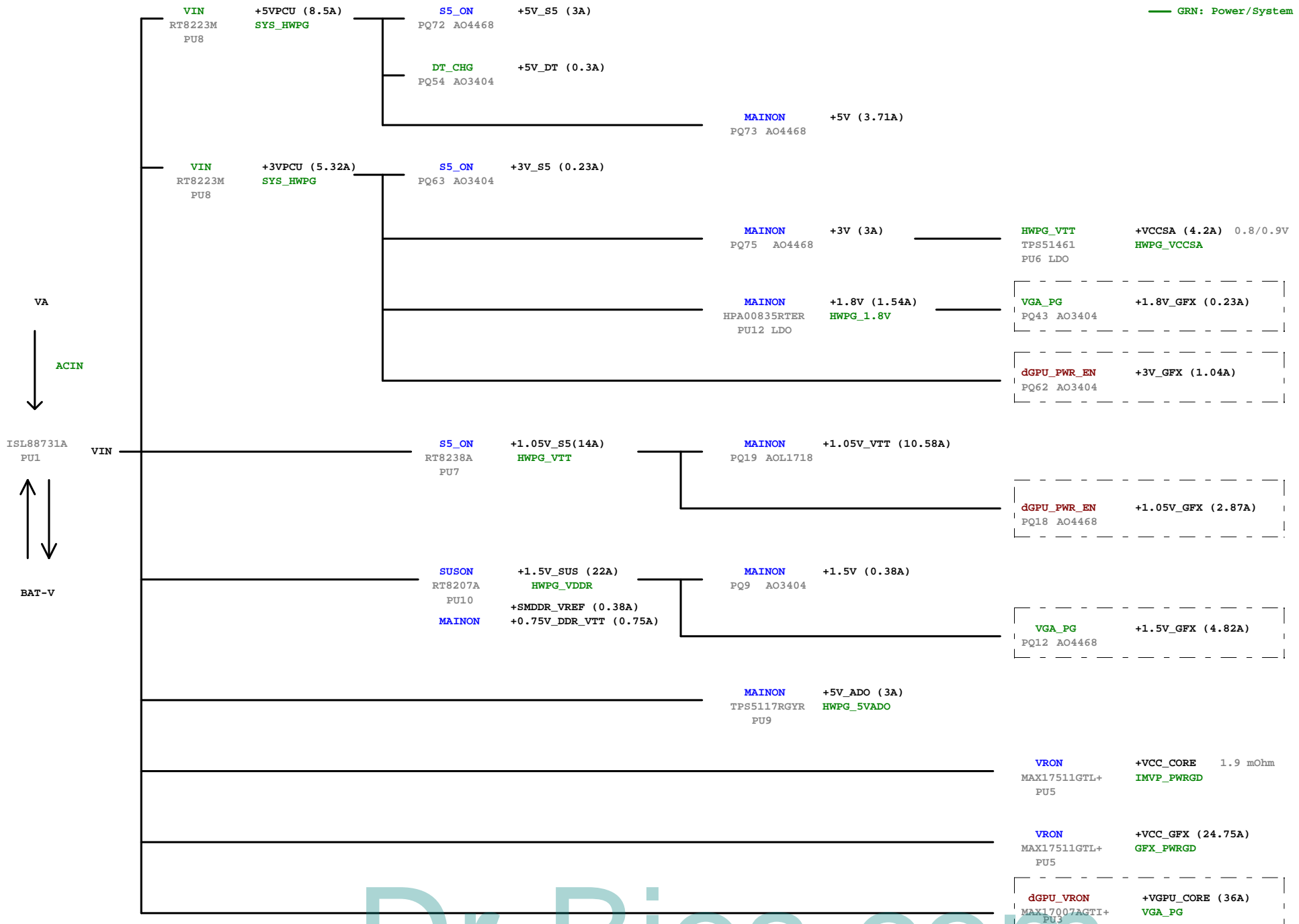
 <b>Quanta Computer Inc.</b> PROJECT : ZYG		Rev
		1A
Size	Document Number	Thermal protect
Date:	Tuesday, February 22, 2011	Sheet 47 of 50



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BRN: PCH  
 BLU: EC  
 GRN: Power/System




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File	<Title>	Rev	1A
Size	Document Number		
Custom	<Doc>		
Date:	Monday, November 15, 2010	Sheet	49 of 50

Model  
ZYG MB

**CHANGE LIST**

REV	TEXT	
C	2010/12/28 Create ZYG C-stage schematics based on "ZYG_MB_REV24_1220_FINAL.DSN" Rename net name SV_DET to BOARD_ID2 in page 10	
	2010/01/05 Update part description with "ZYG_C_Desc.0105.upd" Change SMS battery reset switch PN and footprint	
	2010/01/06 Change CN16 1394 connector footprint and pin assignment	
	2010/01/10 Construct rev.C07 shematics based on rev.C02 Delete TP58, TP60 Change TP7, TP17 footprint to TP3050 Change Hole 19, 21, 20, 22, 23, 24, 25 footprint	
	2010/01/11 Add R716, R719 (mounted) 717, 718 (unmounted) mount R155 and unmount U11, for EC controlling charger IC behavior Delete T6, R719, mount R718, U11, unmount R155, change netname ACPFN to USB3_POWER_ON to control USB charger and-gate Use crystal 24MHz clock for USB3.0: unmount R542, R549, R555, mount R556, Y2, C715, C717 on page 33; unmount R328 on page 9 Mount Q42 for USB wake up function Change Q42 PN (for input 1.5 V > VIN 1.4V) Add R720 and connect between EC pin 20 and BATT_EN#	
	2010/01/12 Change USB3_POWER_ON to EC pin 113, leaving pin 109 ACPFN and T6 Add costdown solution with "C_costdown_0112.upd" Add buffers (U43, U44, Q46, D42, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731) to DT_ATTACH# and DT_CHG Add reserved 0.1uF C2E4 for ESD concern Merge SV_DET to BOARD_ID2 Update power schematics	
	2010/01/13 Adjust R353 357 360 362 363 value for LED luminance Adjust mounting and value for CPU AGX power with "Costback_0113.upd" Add 22 Ohm R723 between DT_ATTACH# and EC for ESD prevention Add RV11, reserved 100k R719, mount R246 and change from 10uF_6 to 22uF_8 in DT dongle power Change EC GPIO37 (pin72) reserved pull-high from +3V_S5 to +3VPCU Update capacitor descriptions and values with "DescUPD1.upd", "DescUPD2.upd", "DescUPD3.upd" Change R723 from 2.2 Ohm 0603 to 0 Ohm 0402 Mount R719 100k Add R724 reserved 0 Ohm	
	2010/01/14 Change 0 ohm R723 from 0402 to 0603 Update 1394 CN16 PN to DFHS04PR511	
	C2	2010/01/25 Create ZYG C2-stage schematics based on "ZYG_MB_REV2_FINAL_GARY_UPD.DSN" Change DT connector/buffer ground as DTGND and connect to GND with R725 C825 C826
		2010/01/26 Left CN13 pins 6 NC Change R725 from 0 ohm to CX08T301024 (EMI CHIP PHY1608087-301Y-N (300+-25%,2A))
		2010/01/27 Update TOP/BOT with "C2_topbot_0127.upd"
	Ramp	2010/01/31 Create ZYG Ramp-stage schematics based on "ZYG_MB_REV2_05_0127_GARY.DSN" Change and mount D22, D31 from CY88SM10900(0603) to CY402V05800(0402)
		2010/02/14 Unmount Q42 to disable S3 wakeup function for USB 3.0 Change U40 from AJS1LH9D0T02 to AJS1L74P0T10 Change SMS PN to DHPATE2CK02
		2010/02/15 Change D31 back to CY88SM10900(0603) Mount C822 for CRT Increase 1.5V by changing PR198 from 10k to 10.5k to avoid 3Dmark running hangup
2010/02/16 Change L41, L42, L43 to CX8BA470003/CX8PG330007 for N12P/N12E Update U36 to ALD00547000 (USB power switch 2A) Change C13, C14 to CY402V05800 (ESD varistor)		
2010/02/17 Change 0-Ohm to short pad with "RampShortPadUPD0217.upd" Delete L13, L7, L45, L10, L11, L12, L17, L14, L18 Dismount PU2 Change PQ12 from A04468 to A0LL1718		
2010/02/18 delete C826 change C825 PN to BCO40201L200 change U44 pins from +5V_DTPWR to +3VPCU rename net N129824580 to DT_CHG_R Add U45 Dismount R725 Add Q47		
2010/02/22 Delete RV9, RV10, RV11 Change R694 from shortpad to 0 Ohm Change L3, L4 to CX5AG601001 (600 ohm, 300mA) Add pin7, 8 floating on CN13 Delete TP33, change DT_GND to pin3 of U45, swap pin4, 6 of U45 Rename N129824552 to DT_CHG#, add R726, Q48 Delete Q48, R726; connect DT_CHG and DT_CHG# with R726 (0 ohm) Delete Q48, R726; connect DT_CHG and DT_CHG# with R726 (0 ohm) Change R694 from 0 ohm to 22 ohm for EMI concern Update TOP/BOT with "TOPBOT_ramp0222.upd" Change R722 to 200k_4 (TOP) Mount C796 with 10p cap Change Q47 to A083404 M08 (TOP)		
2010/02/23 Change Q47 to A083404 M08 (TOP) TEXT		


**Quanta Computer Inc.**  
 PROJECT : ZYG  
 Change list  
 Date: Wednesday, February 24, 2011 10:56:50 AM

DOC NO.	PROJECT MODEL :	ZYG	APPROVED BY:	DATE:
	PART NUMBER:		DRAWING BY:	REVISION: C

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