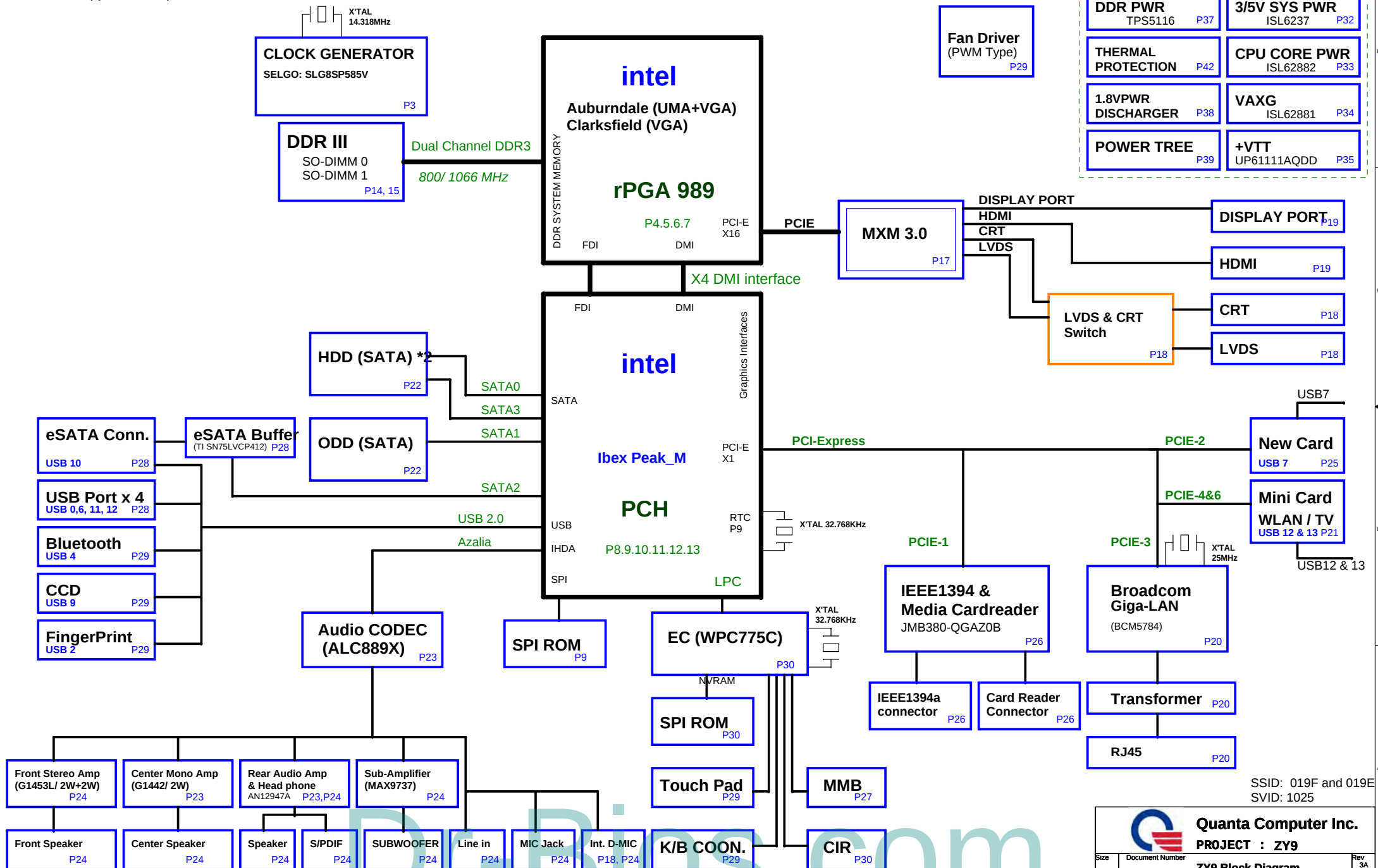


31ZY9MB0000
ZY9 MB ASSY(DC/GM/MXM)ASSY W/O CPU
31ZY9MB0010
ZY9 MB ASSY(QC/GM/MXM)ASSY W/O CPU

ZY9 SYSTEM BLOCK DIAGRAM



SSID: 019F and 019E
SVID: 1025

Table of Contents

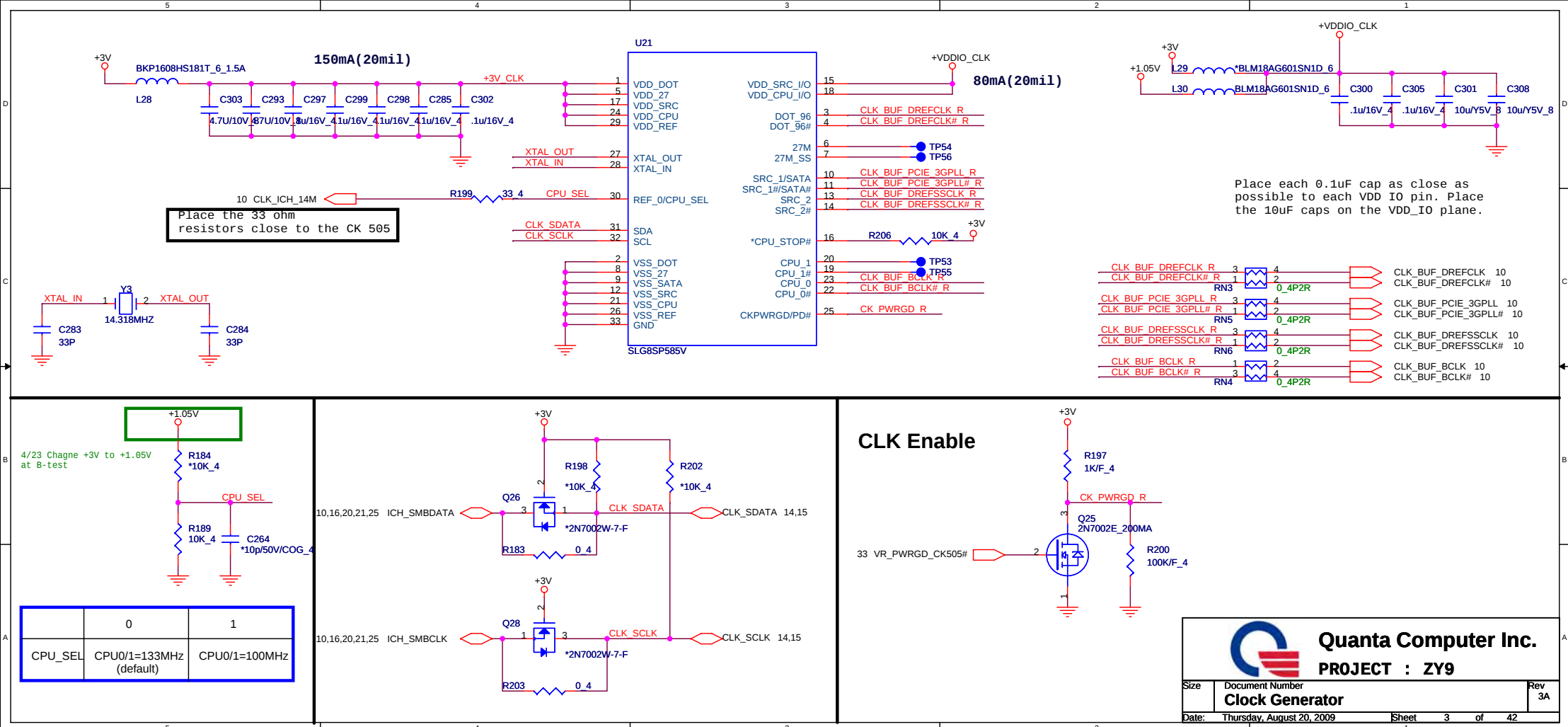
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	Clock Generator (SLG8SP585V)
4-7	CPU (Clarksfield)
8-13	PCH (Ibex Peak-M)
14-15	DDRIII SO-DIMM
16	BRAIDWOOD
17	MXM3.0
18	CRT/LVDS Conn
19	HDMI / Display port
20	LAN (BCM5784M)
21	MINI PCIE
22	SATA HDD/ODD
23-24	Audio CODEC(ALC889X) /Phone Jack
25	NEW CARD
26	Card Reader (JMB380) / 1394
27	MMB /LED
28	USB / E-SATA
29	KB / FAN /TP /CCD /BT
30	EC /FLASH /CIR
31	Charger (ISL88731)
32	5V /3V (ISL6237)
33	CPU Core (ISL62882)
34	+VTT (UP6111AQDD)
35	+1.05V (UP6111AQDD)
36	DDR 1.5V (TPS51116)
37	Discharge /1.8V
38	POWER TREE TABLE
39	PCH POWER PLANE
40	POWER Management
41	Thermal protection
42	change list

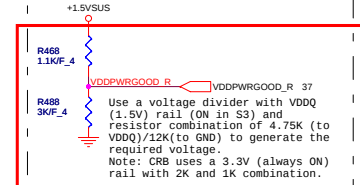
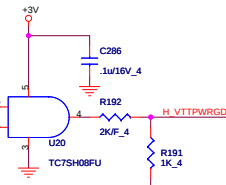
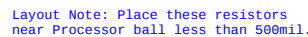
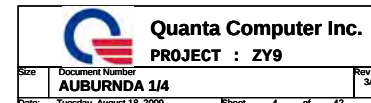
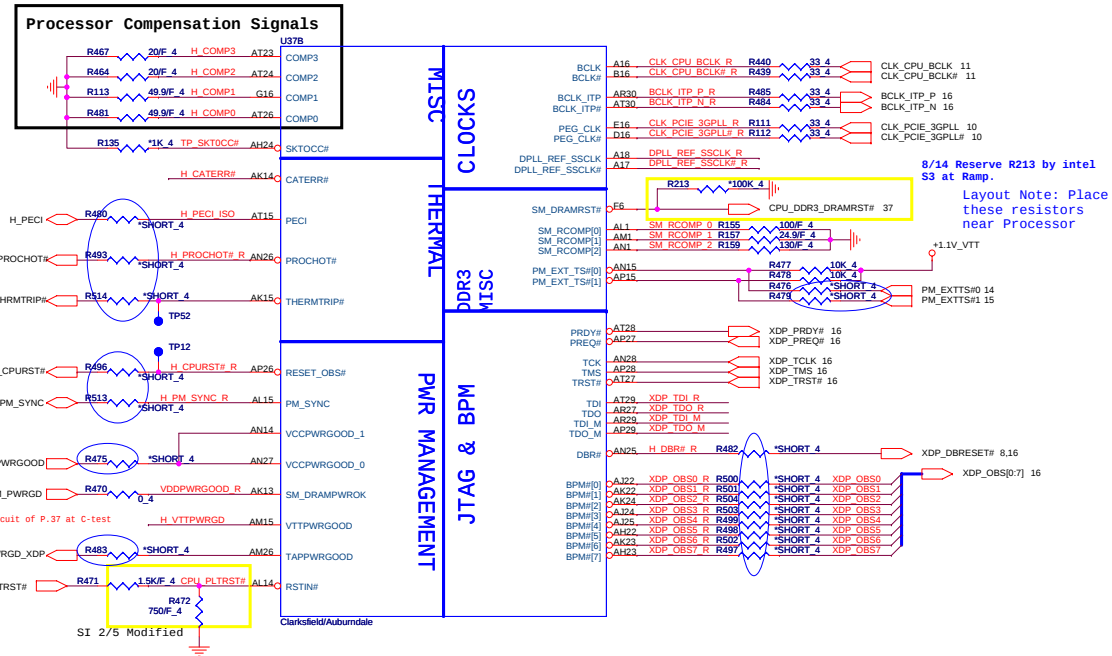
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

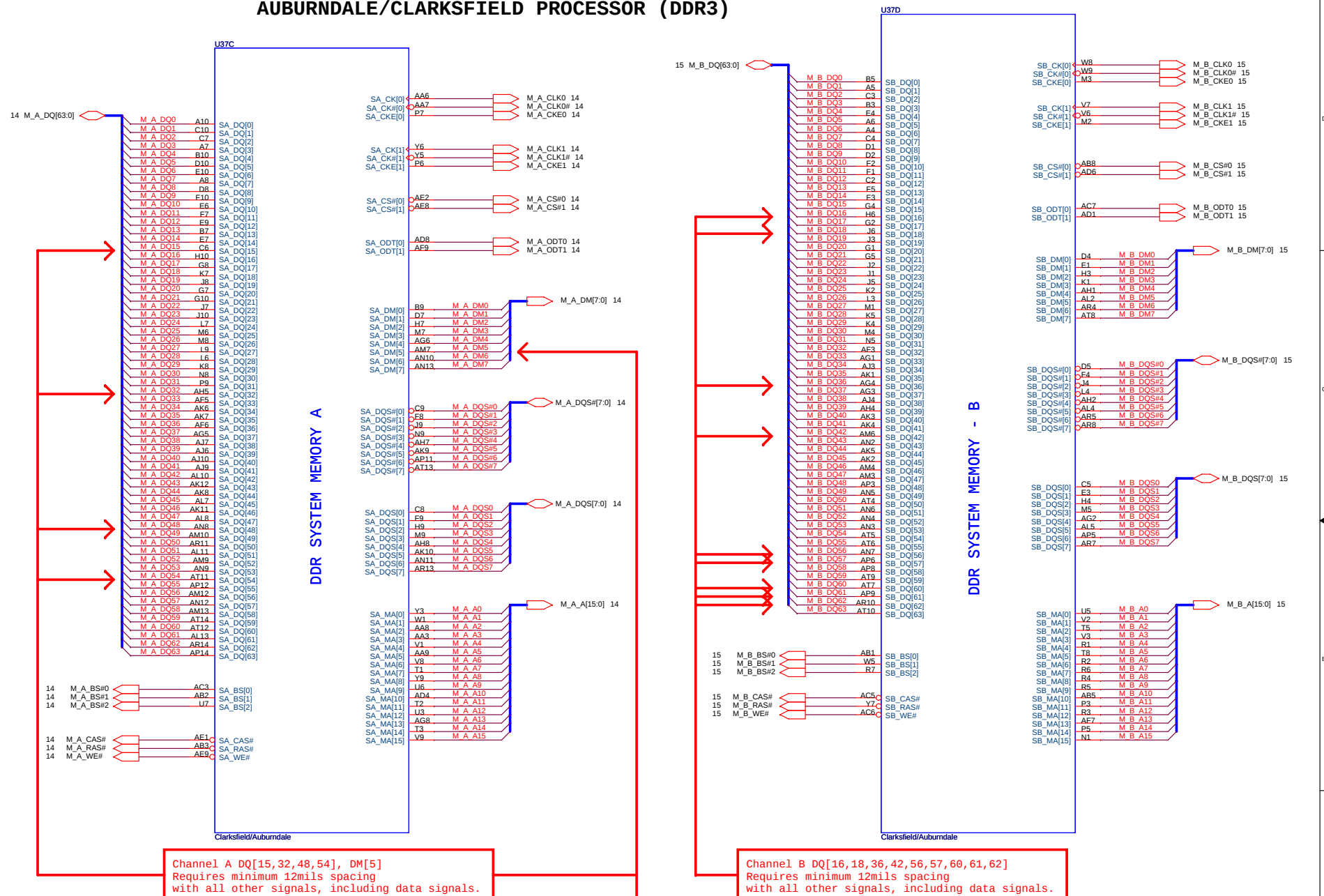
GND PLANE	PAGE	DESCRIPTION
▽ LANGND	20	
▽ E775AGND	30	
▽ ADOGND	23.24	
≡ GND	ALL	

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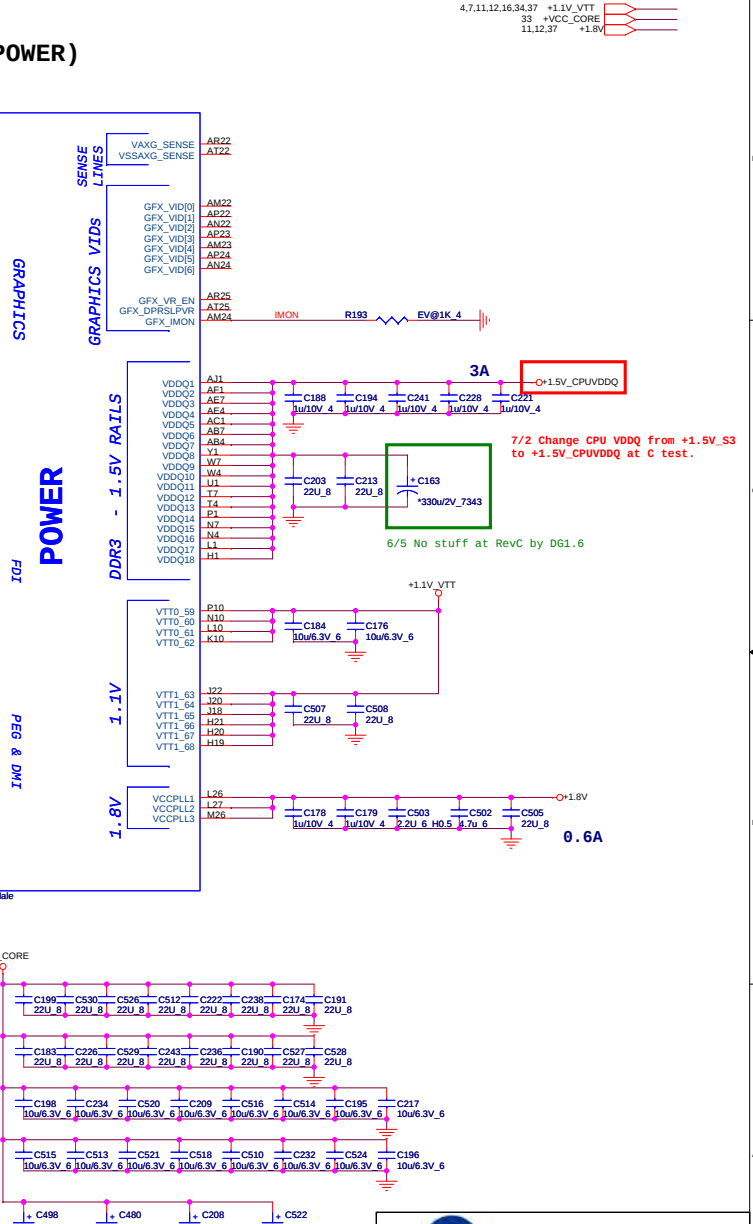
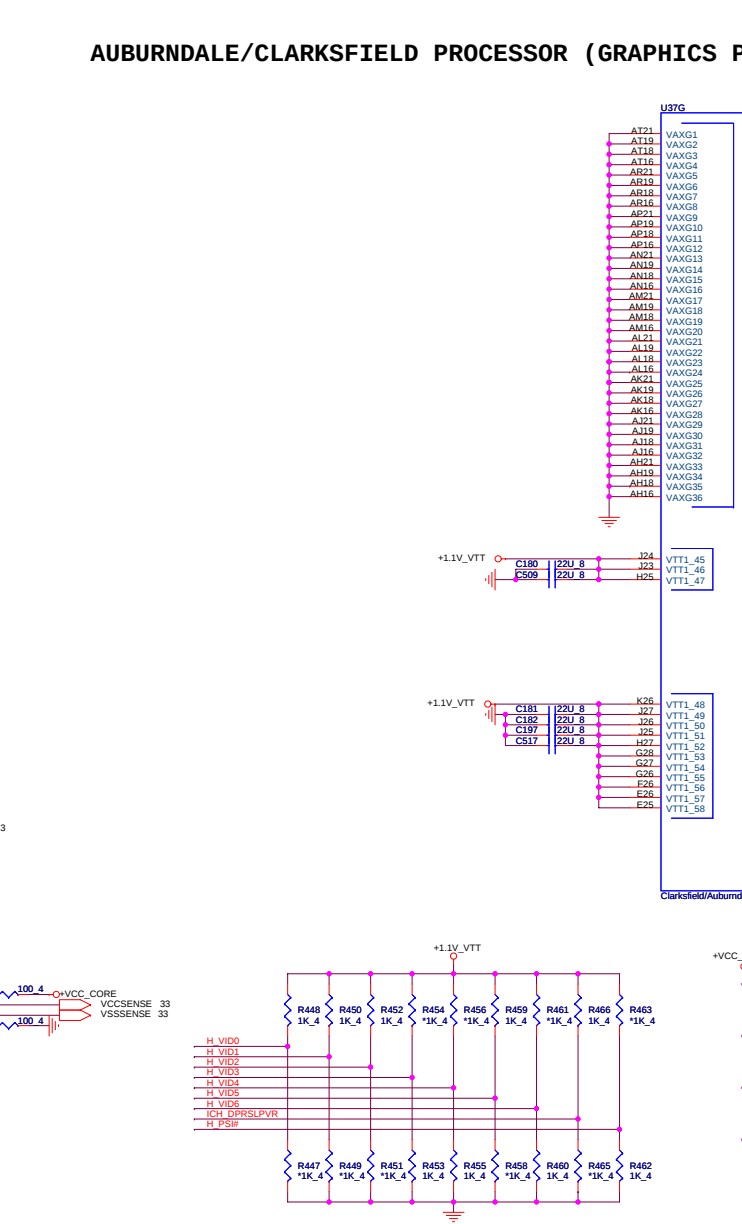
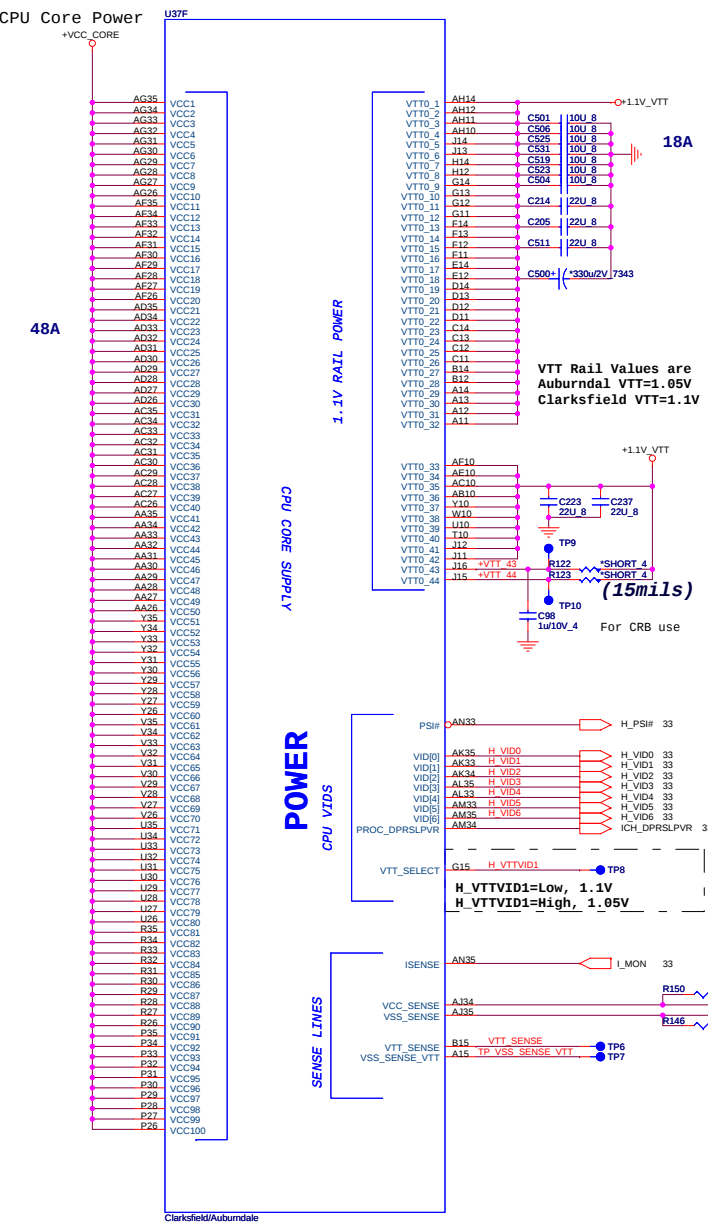
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



DM signals are not present on Clarkfield processor. All DM signal can be left as NC on Clarkfield and connect directly to GND on So-DIMM side for Clarkfield design only

4.7,11,12,16,34,37 +1.1V_VTT
33 +VCC_CORE
11,12,37 +1.8V

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Note:
For Validating DMP VR R6451 should be STUFF
and R6451 NO STUFF

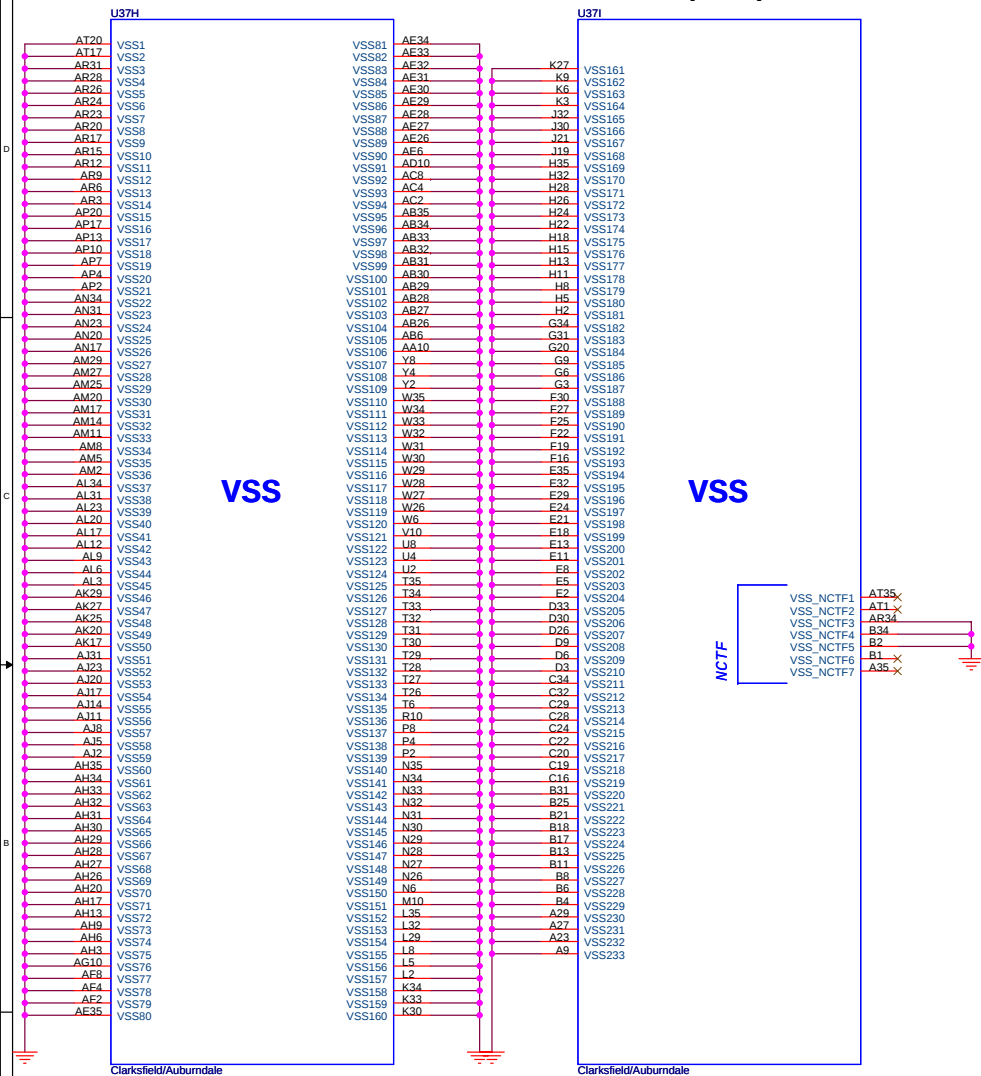
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

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PROJECT : ZY9

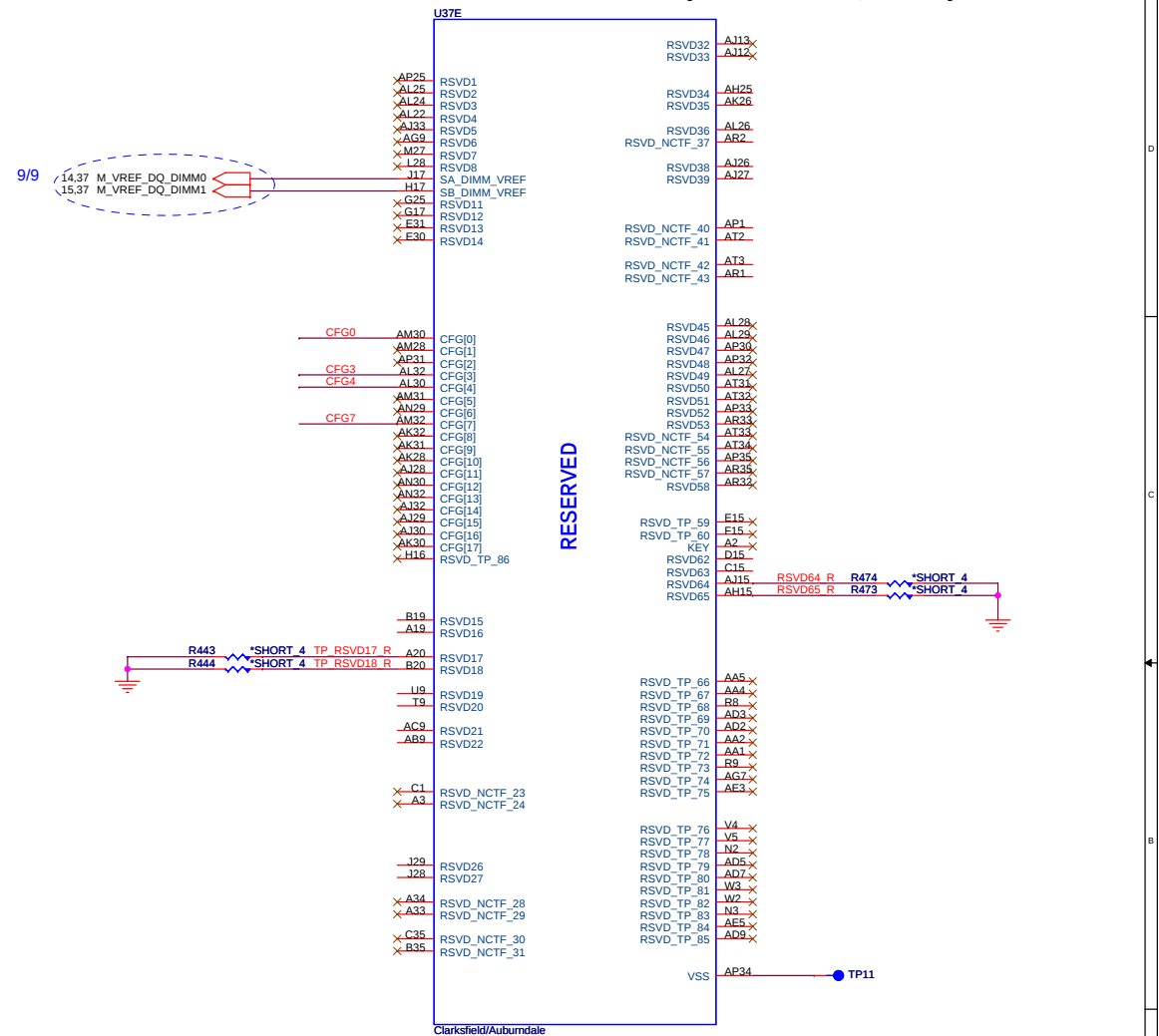
Size	Document Number	Rev
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AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

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PROJECT : ZY9

Size

Document Number

AUBURNDA 4/4

Rev

3A

Date

Tuesday, August 18, 2009

Sheet

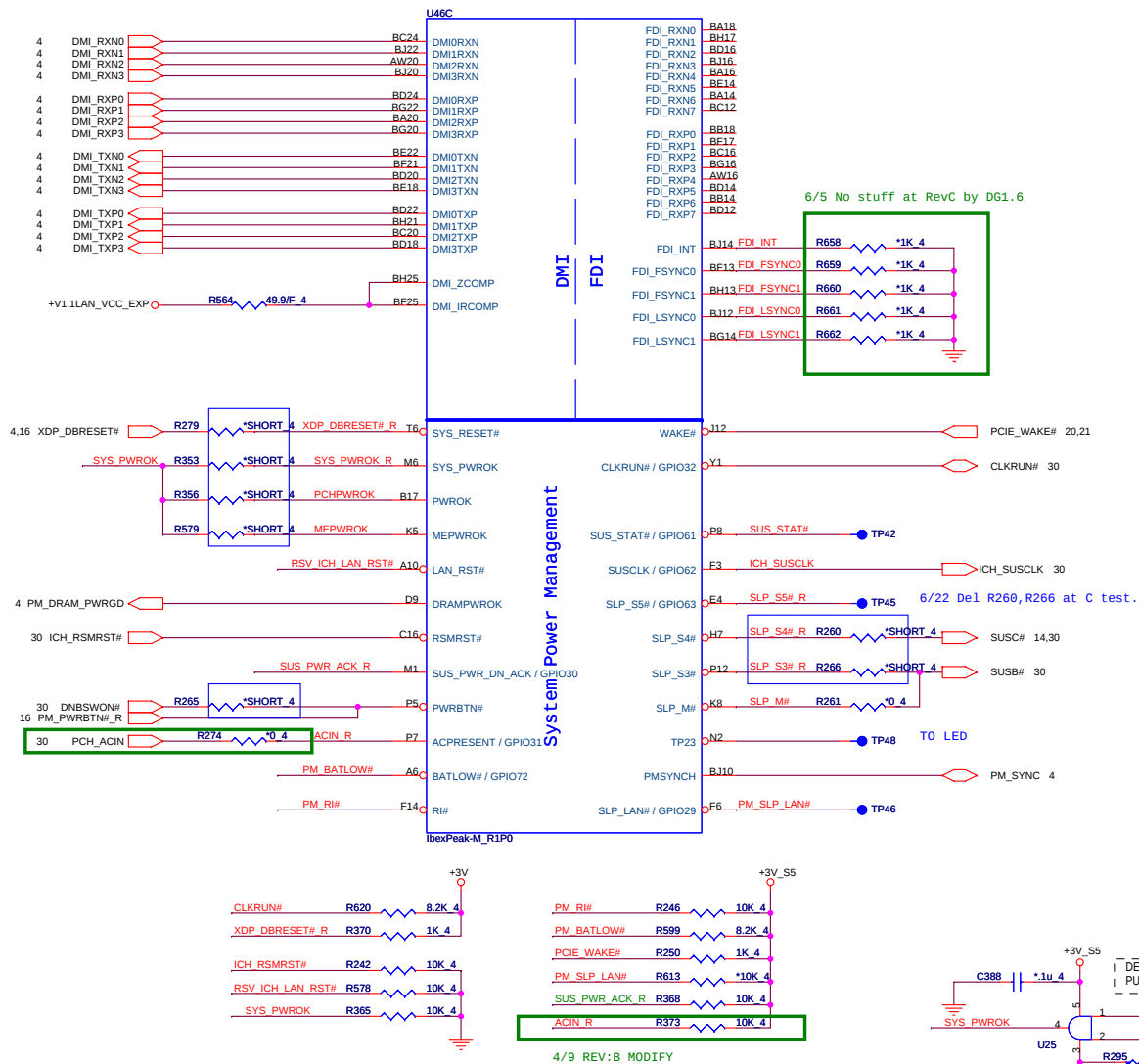
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of

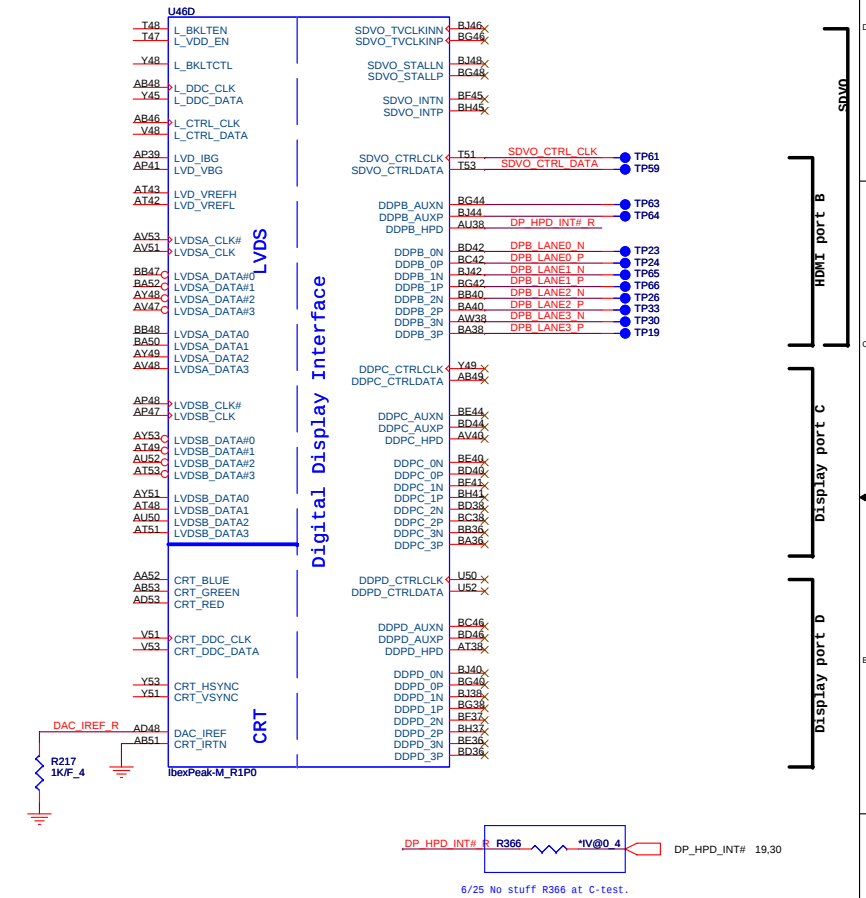
42

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IBEX PEAK-M (DMI, FDI, GPIO)



IBEX PEAK-M (LVDS, DDI)



RTC Circuitry

CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

IBEX PEAK-M (HDA, JTAG, SATA)

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

7/1 change from +3V_S5 to +3V by intel.

HDA DOCK_EN# R233 *1K 4
6/21 Non stuff R233 by Intel at C-test.

Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

For PCH 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI

iTPM ENABLE/DISABLE

TPM Function	R591
Enable	Mount
Disable	NC (Default)

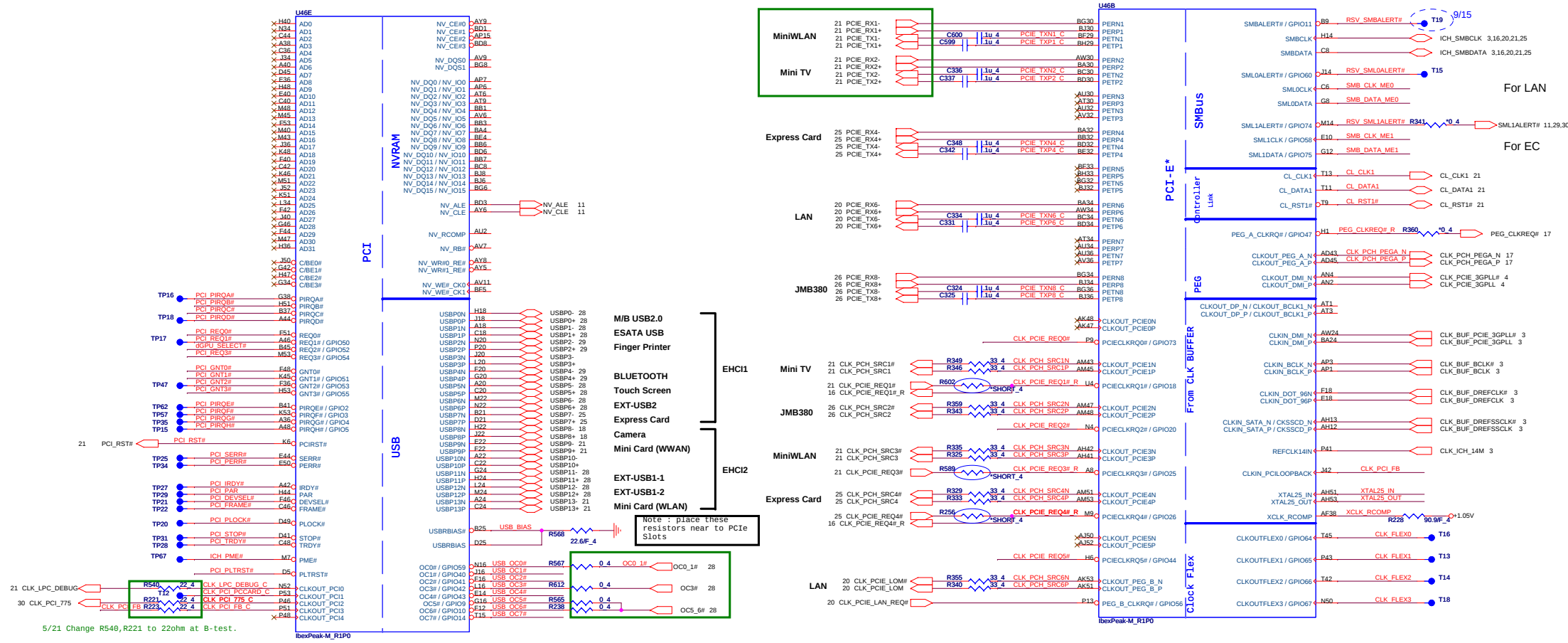
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PROJECT : ZY9
IBEX PEAK-M 2/6
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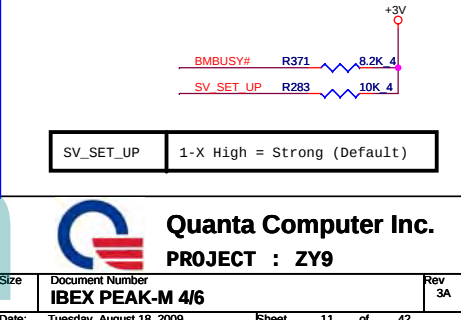
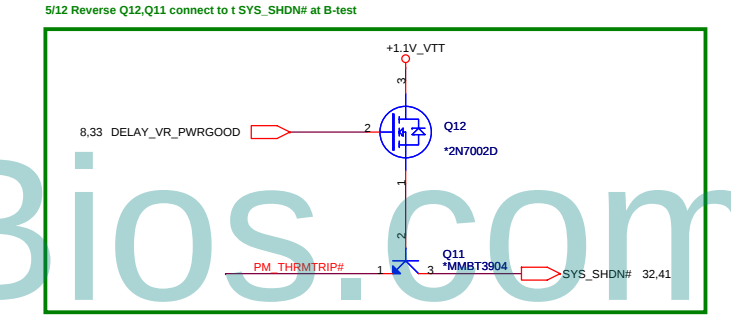
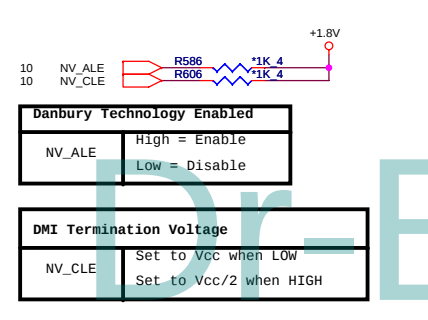
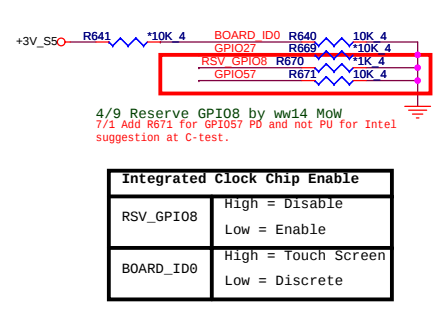
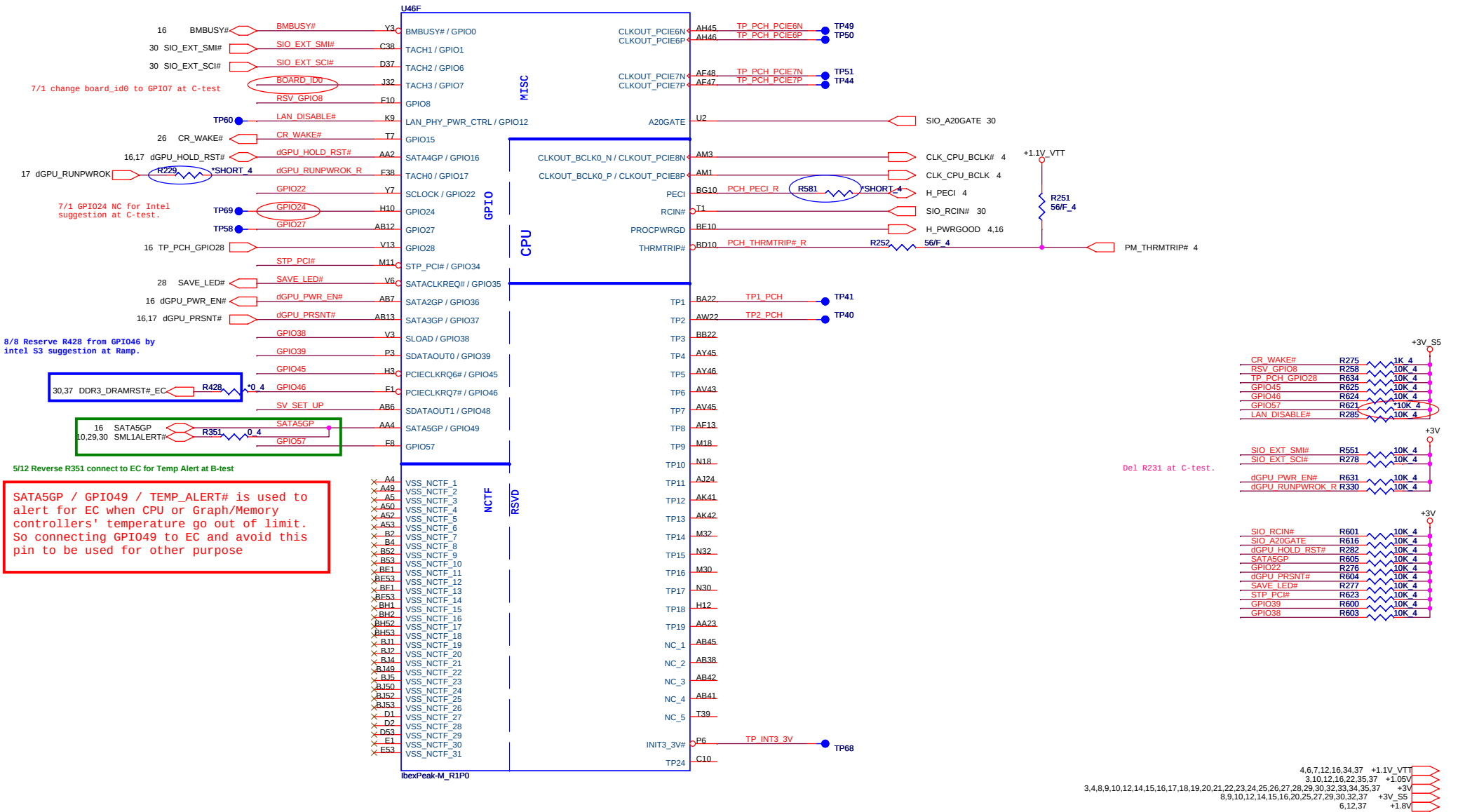
IBEX PEAK-M (PCI, USB, NVRAM)

5/14 Change PCIe sequence between CN21 and CN23 by BIOS at B-test.

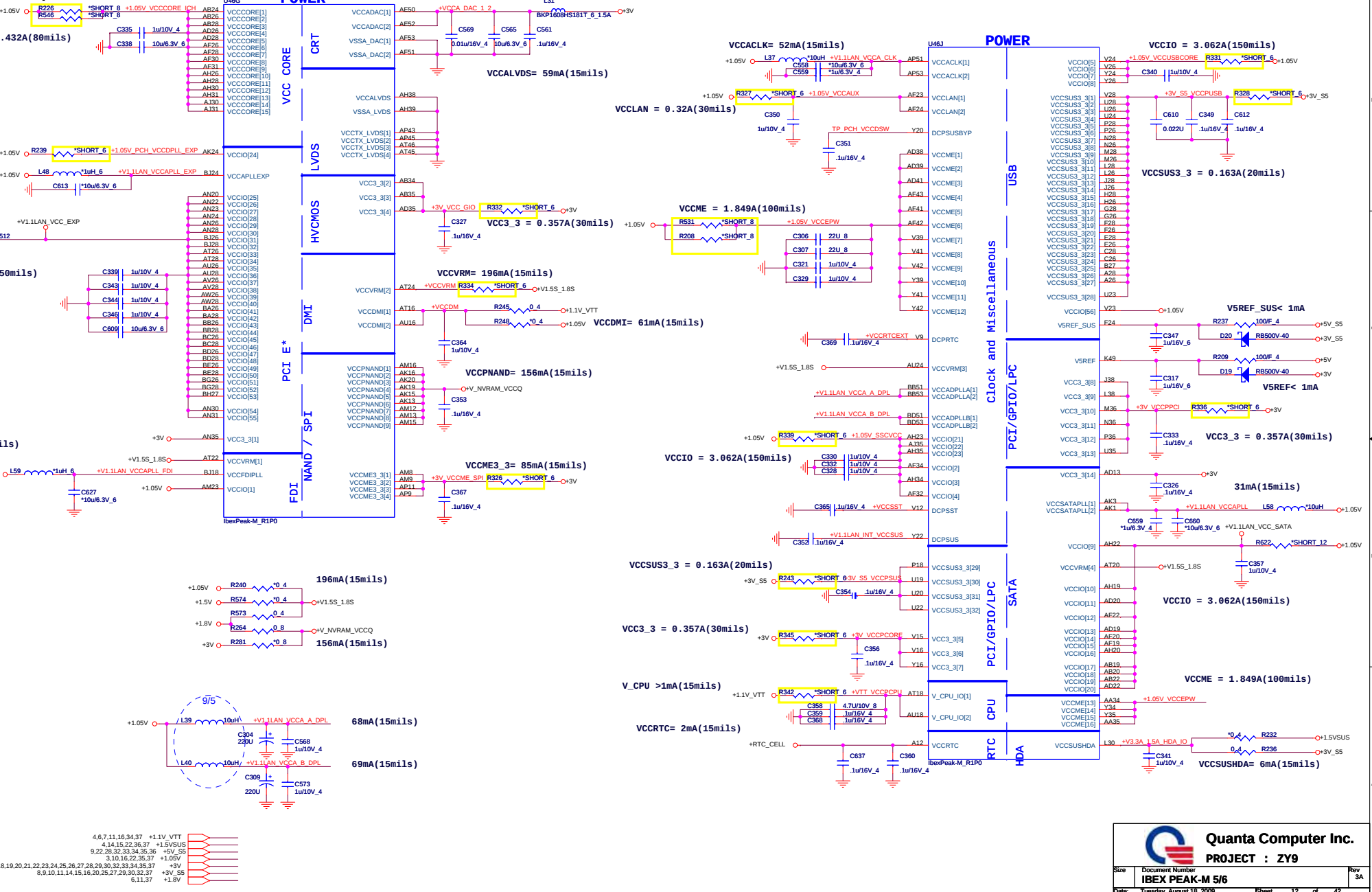
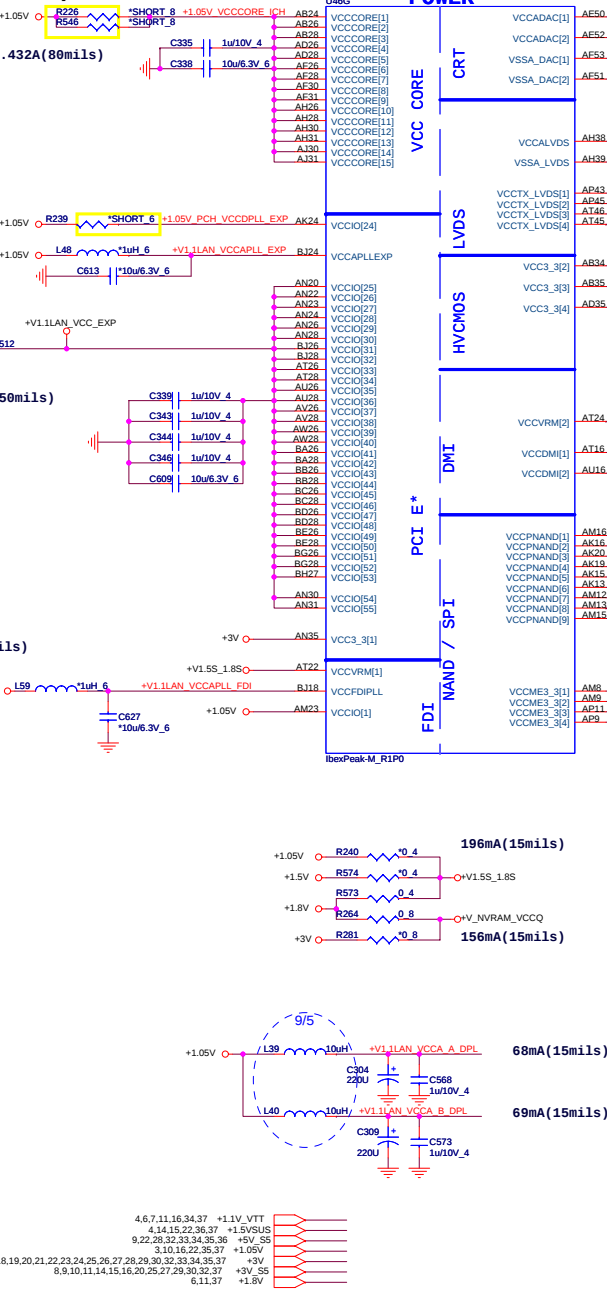
IBEX PEAK-M (PCI-E, SMBUS, CLK)



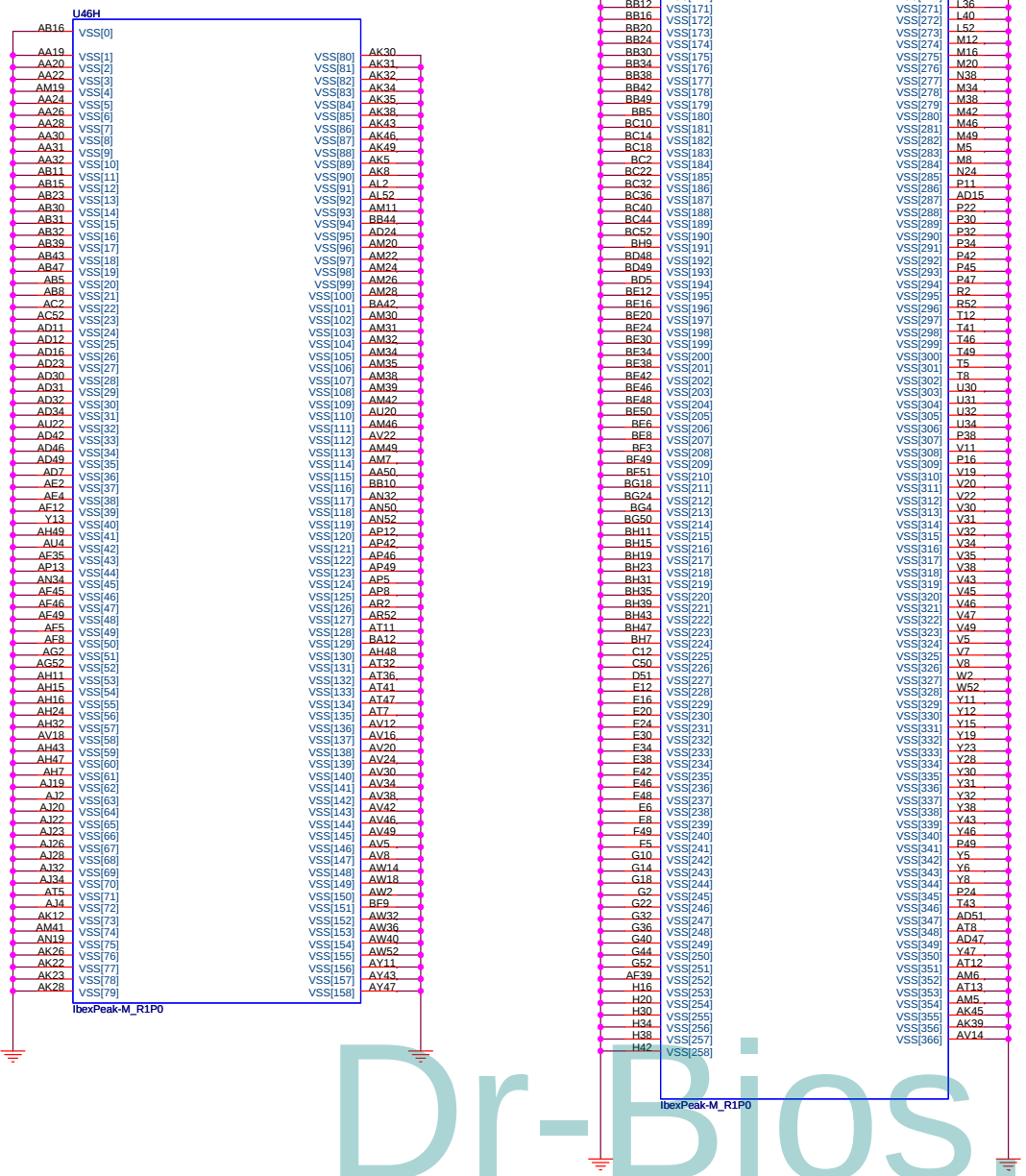
IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



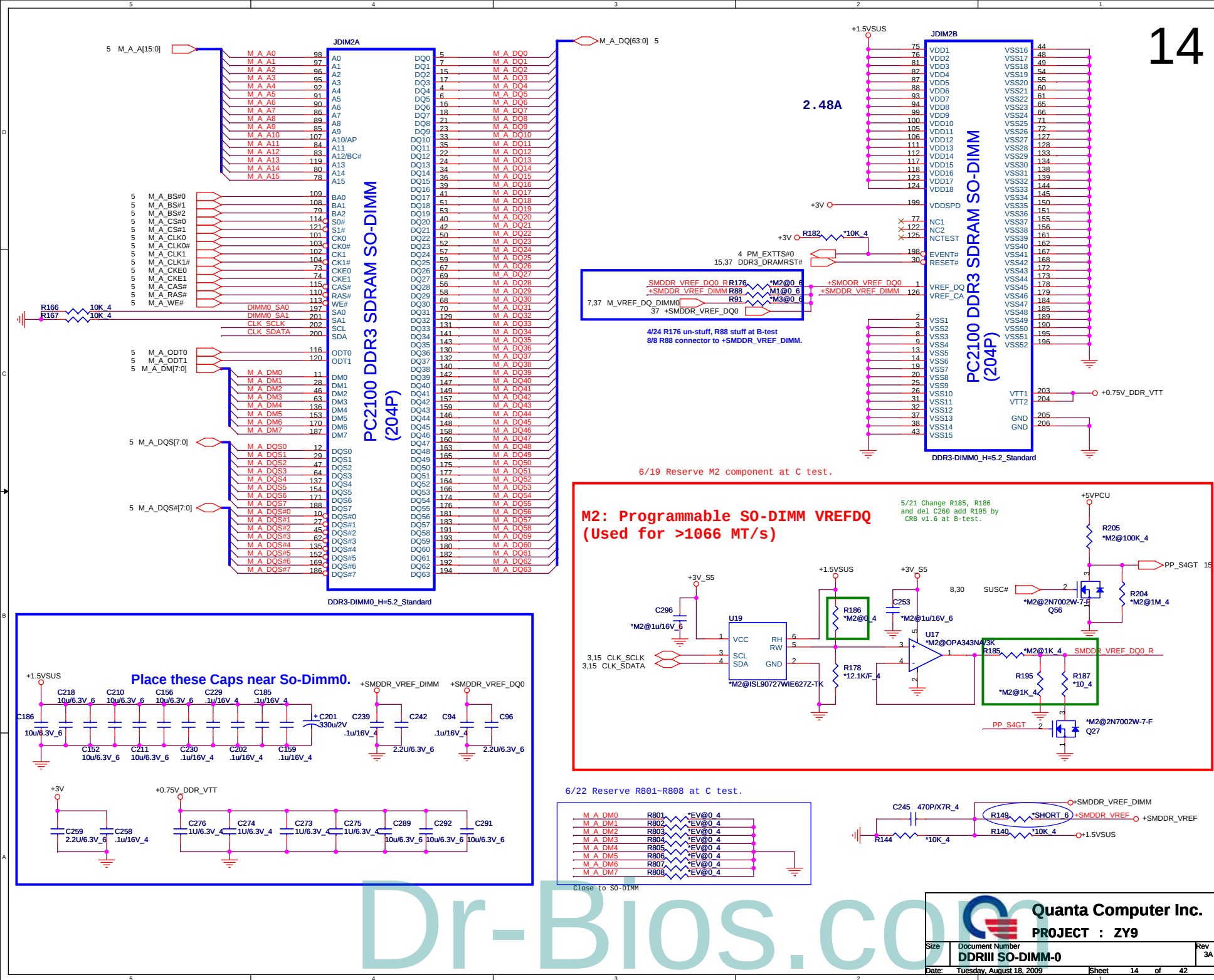
5
POWER)

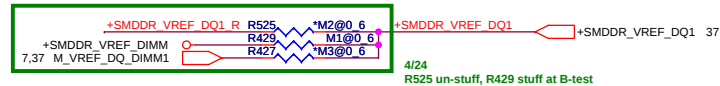
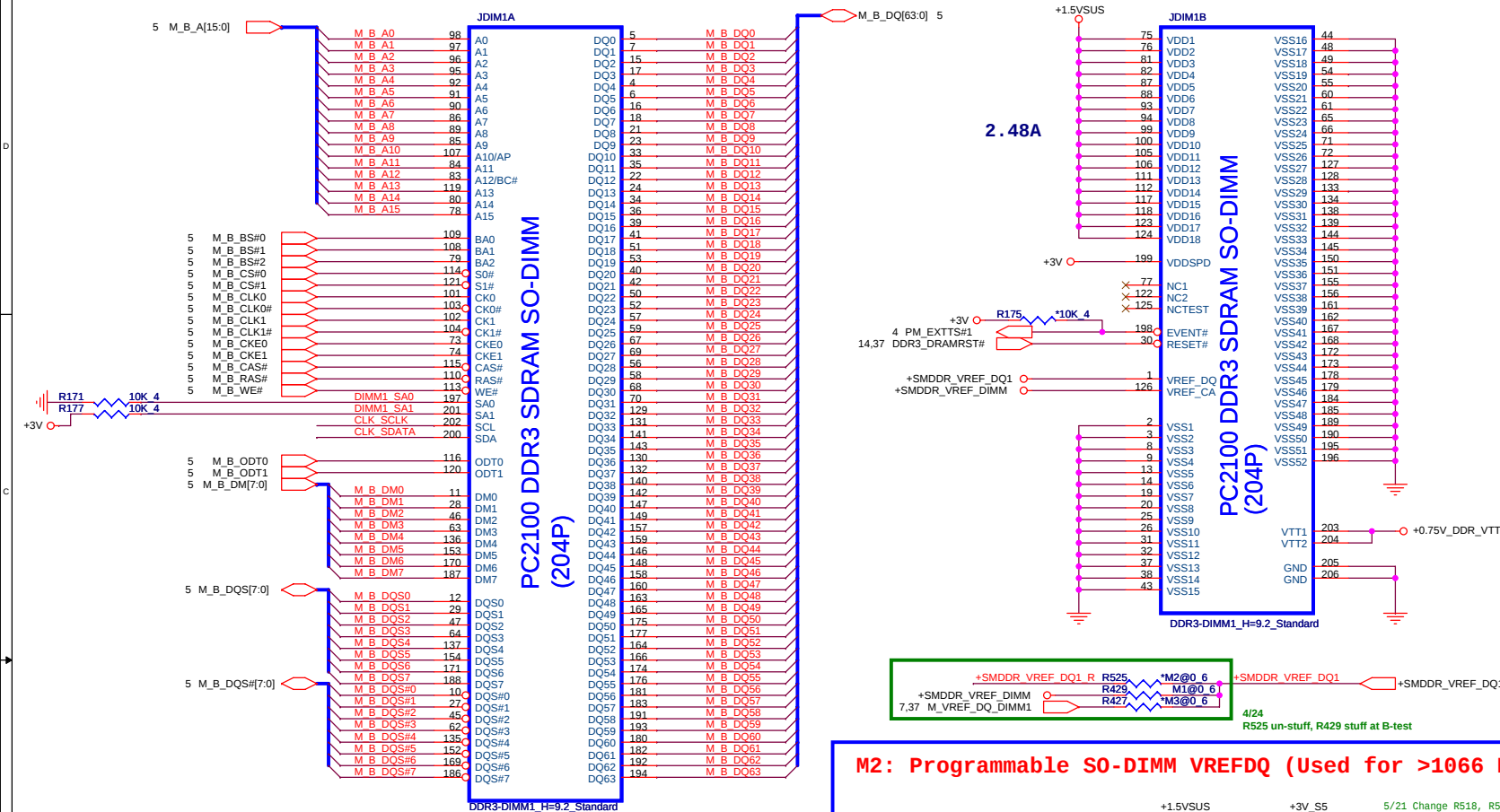


IBEX PEAK-M (GND)

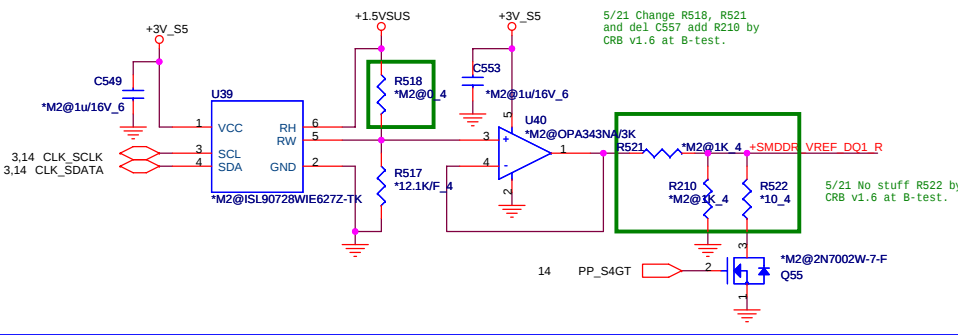


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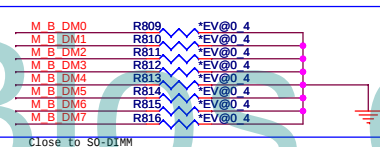


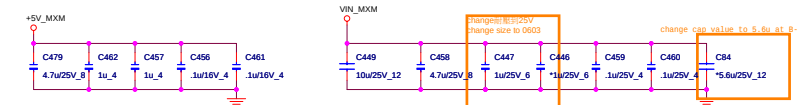
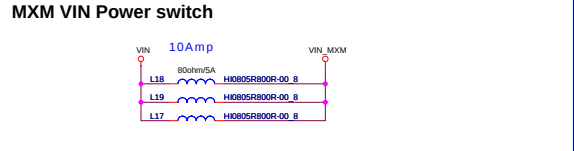
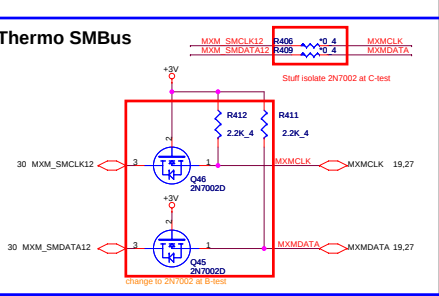
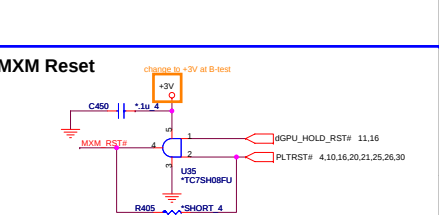
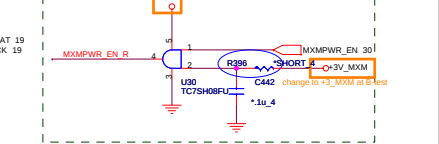
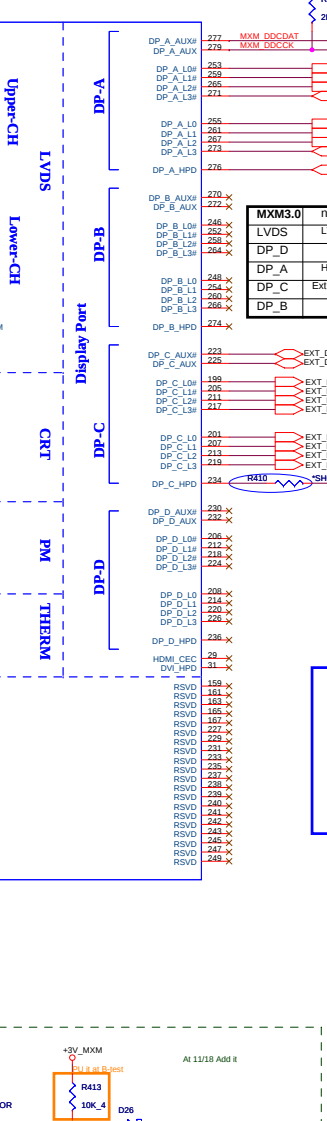
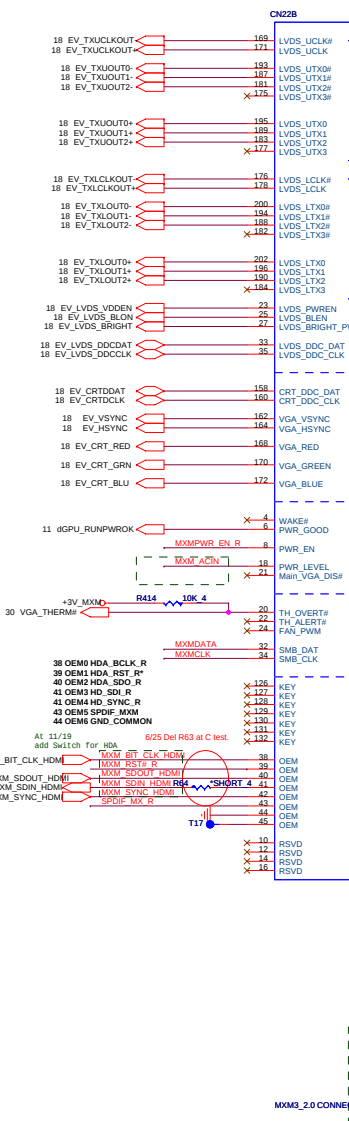
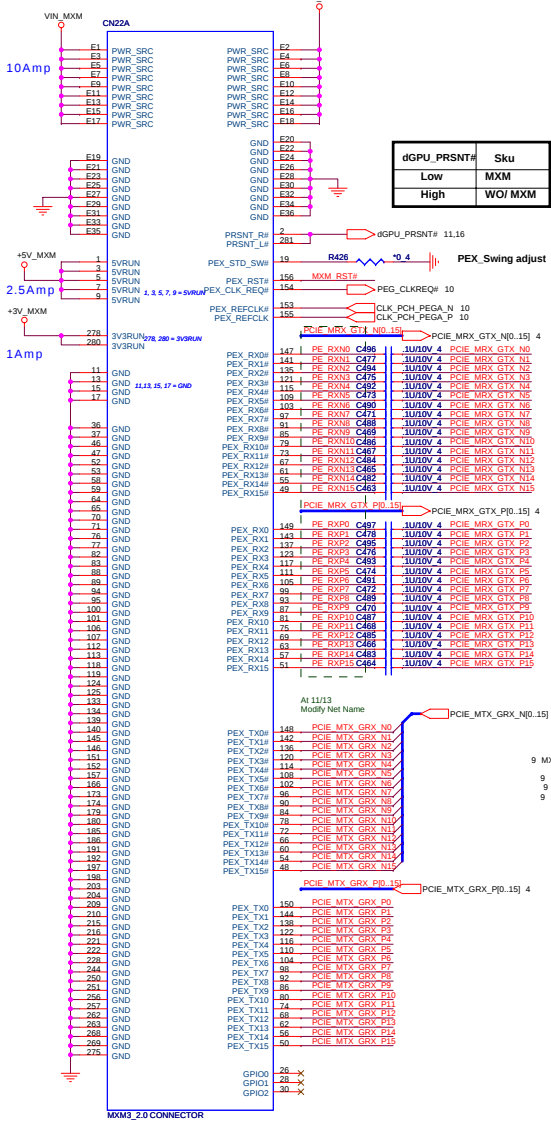
M2: Programmable SO-DIMM VREFDQ (Used for >1066 MT/s)



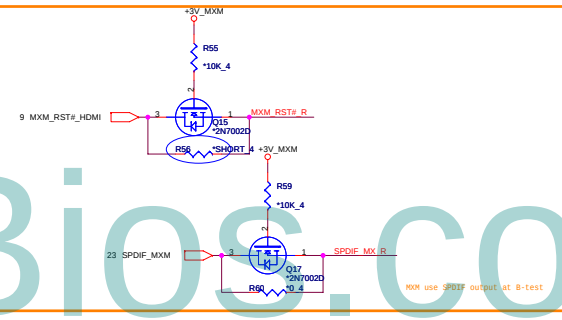
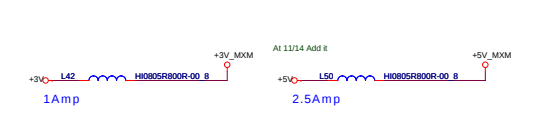
6/19 Reserve M2 component at C test.

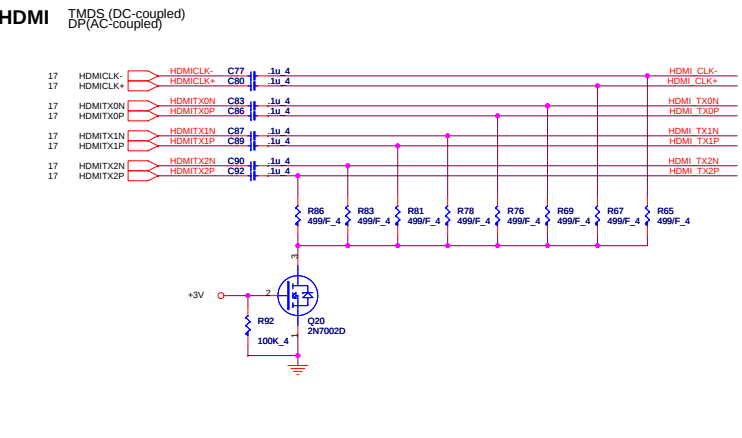
6/22 Reserve R809-R816 at C test.



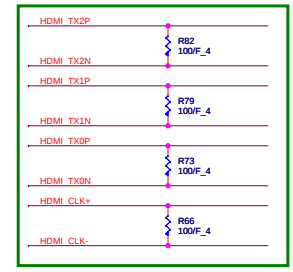


MXM 3V/5V Power switch



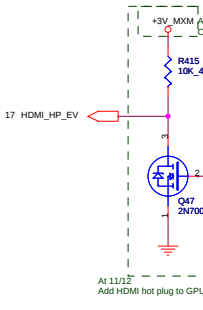


5/14 Stuff R82,R79,R73,R66 by EMI at B test.

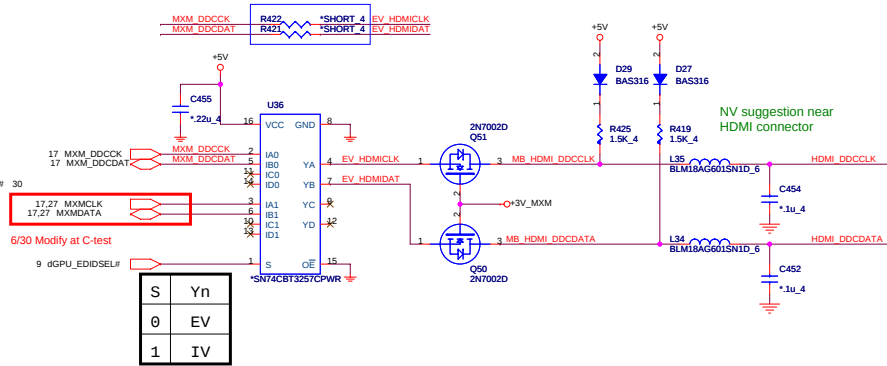


Close CN27

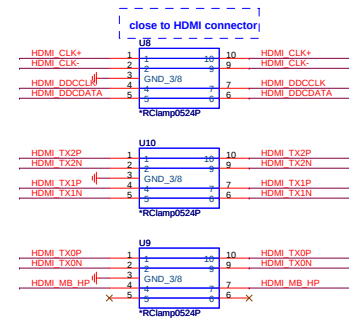
HDMI Hot-PLUG to SB and GPU



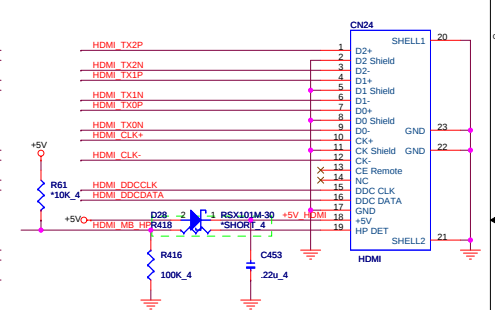
SDVO I2C Control **Bypass(default)**



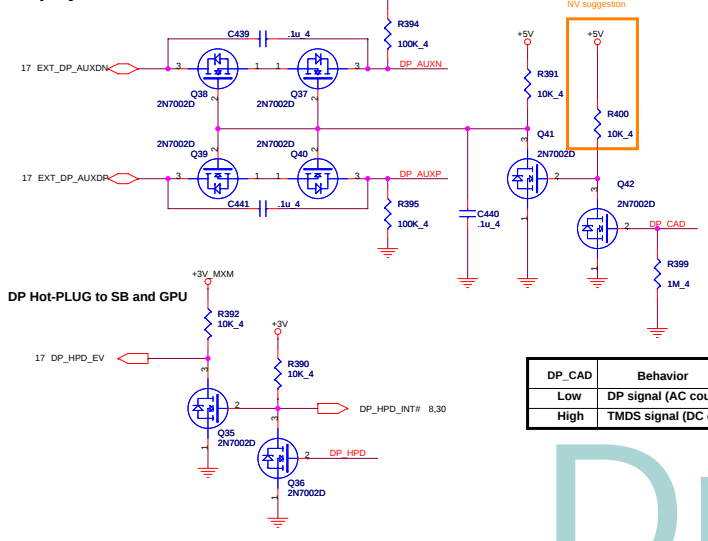
ESD Protect



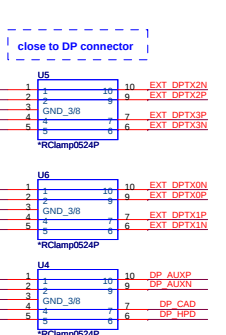
HDMI connector



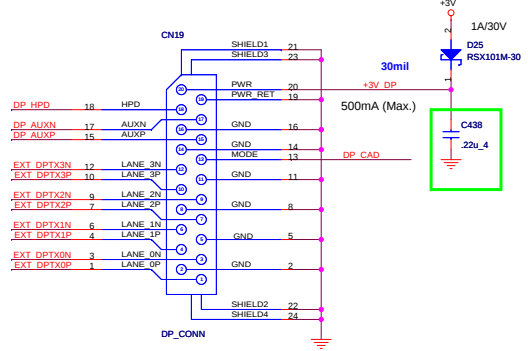
DisplayPort



ESD Protect



DP connector

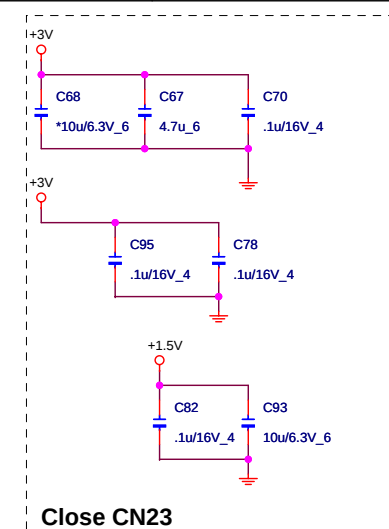
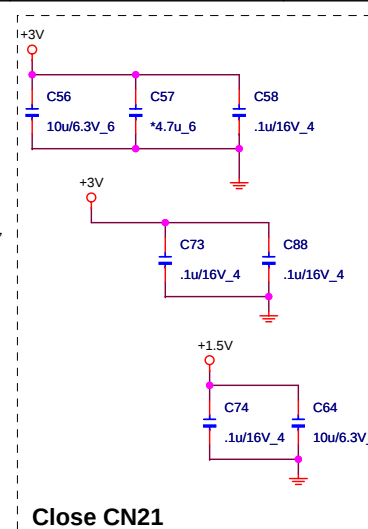


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

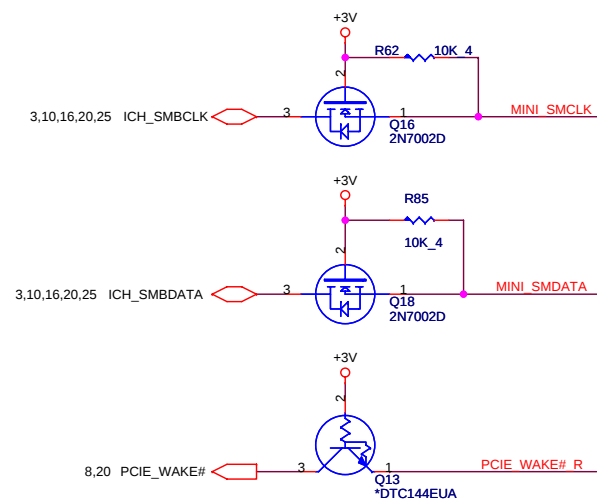
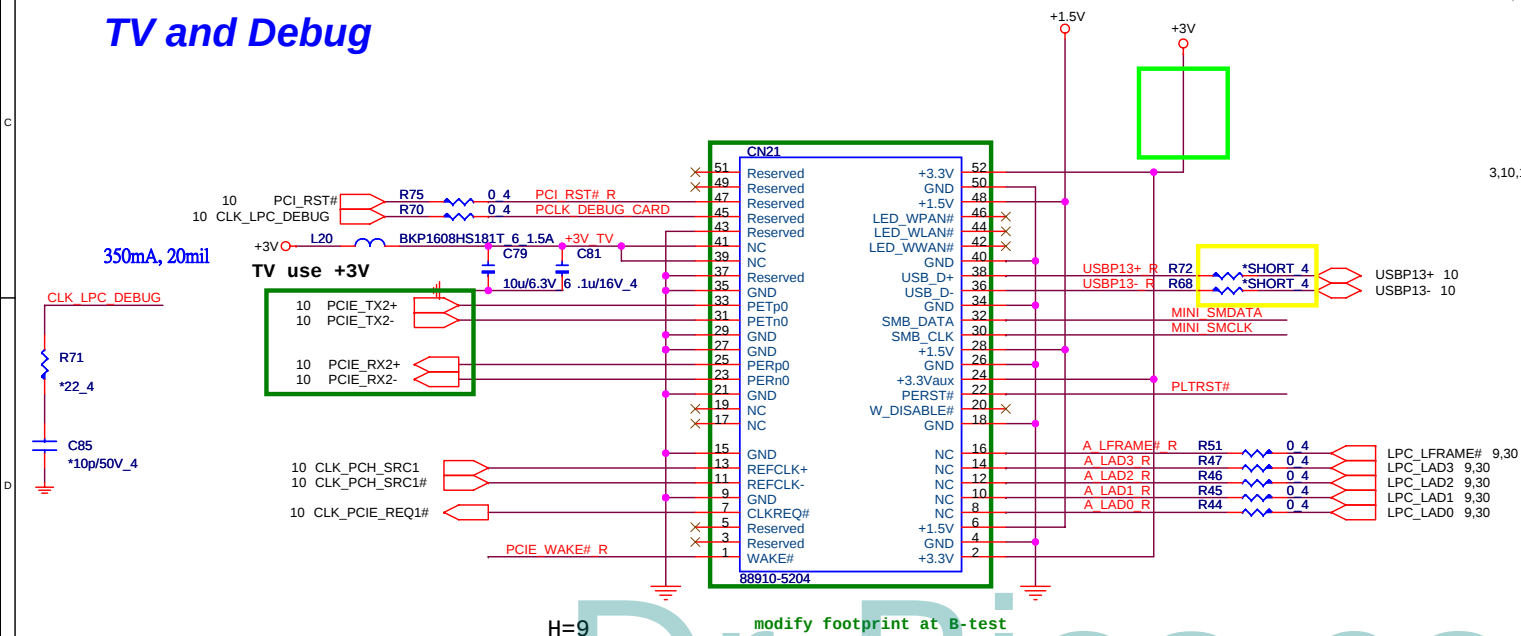
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+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

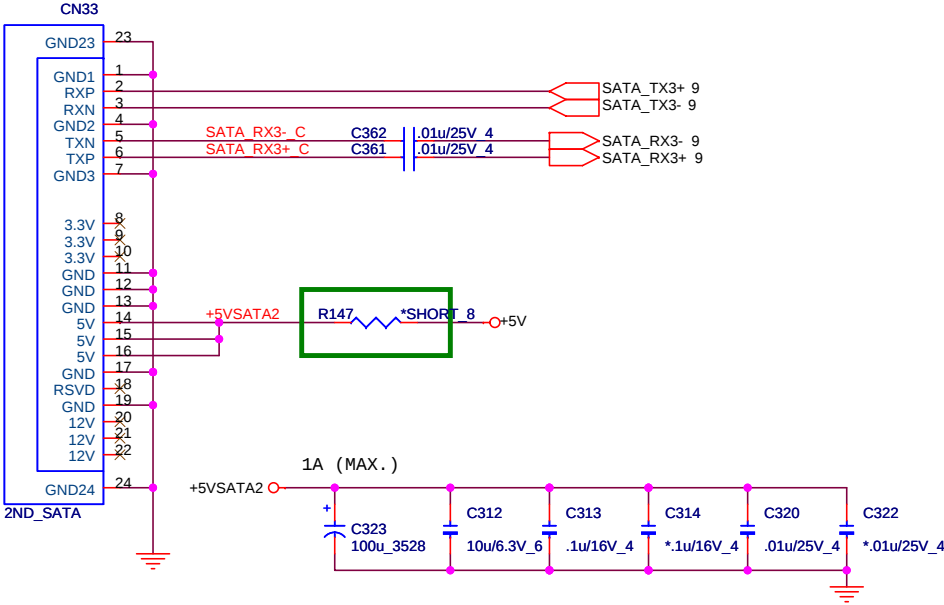
Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



TV and Debug

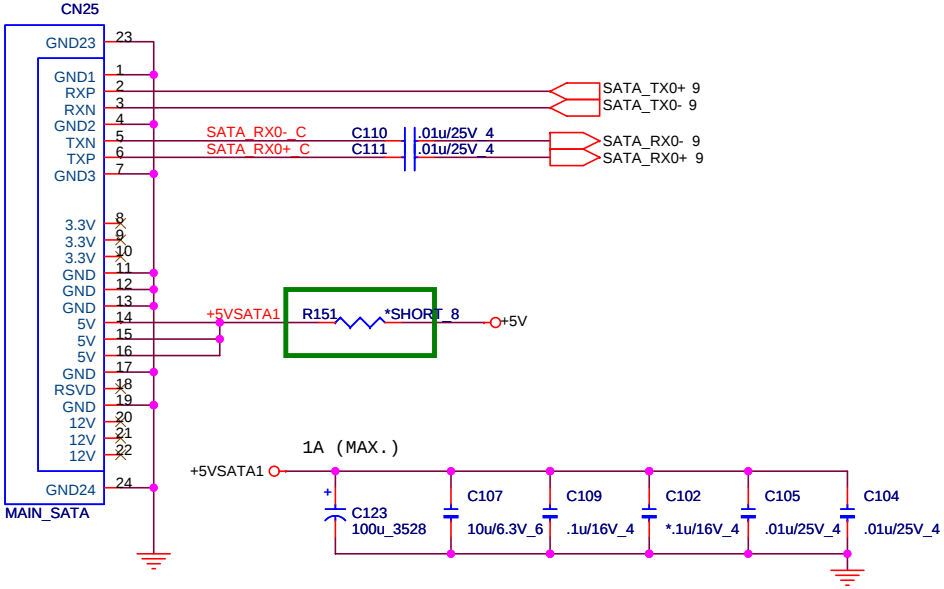


2nd SATA HDD (edge of board)

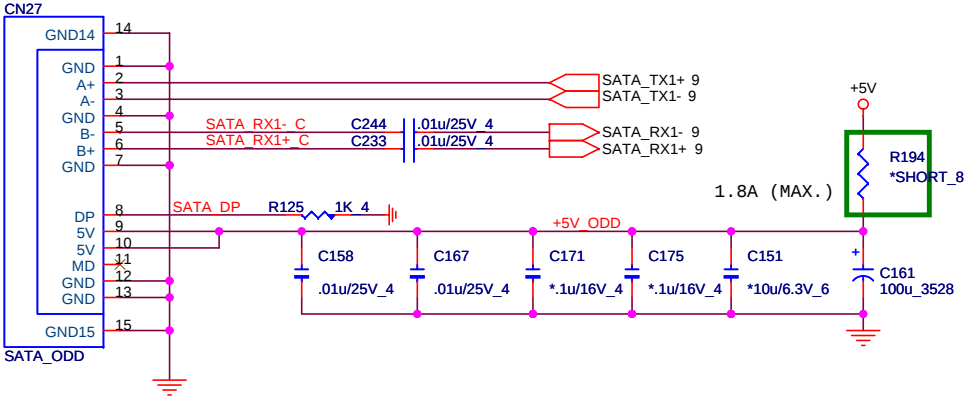


5/13 Add R147,R151,R197 for power consumption measure at B-test.

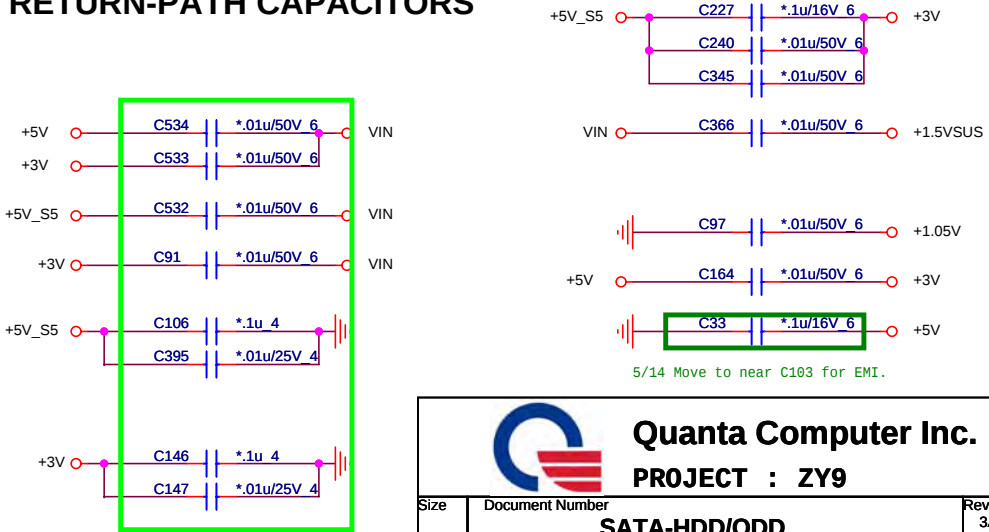
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS



5/14 Move to near C103 for EMI.

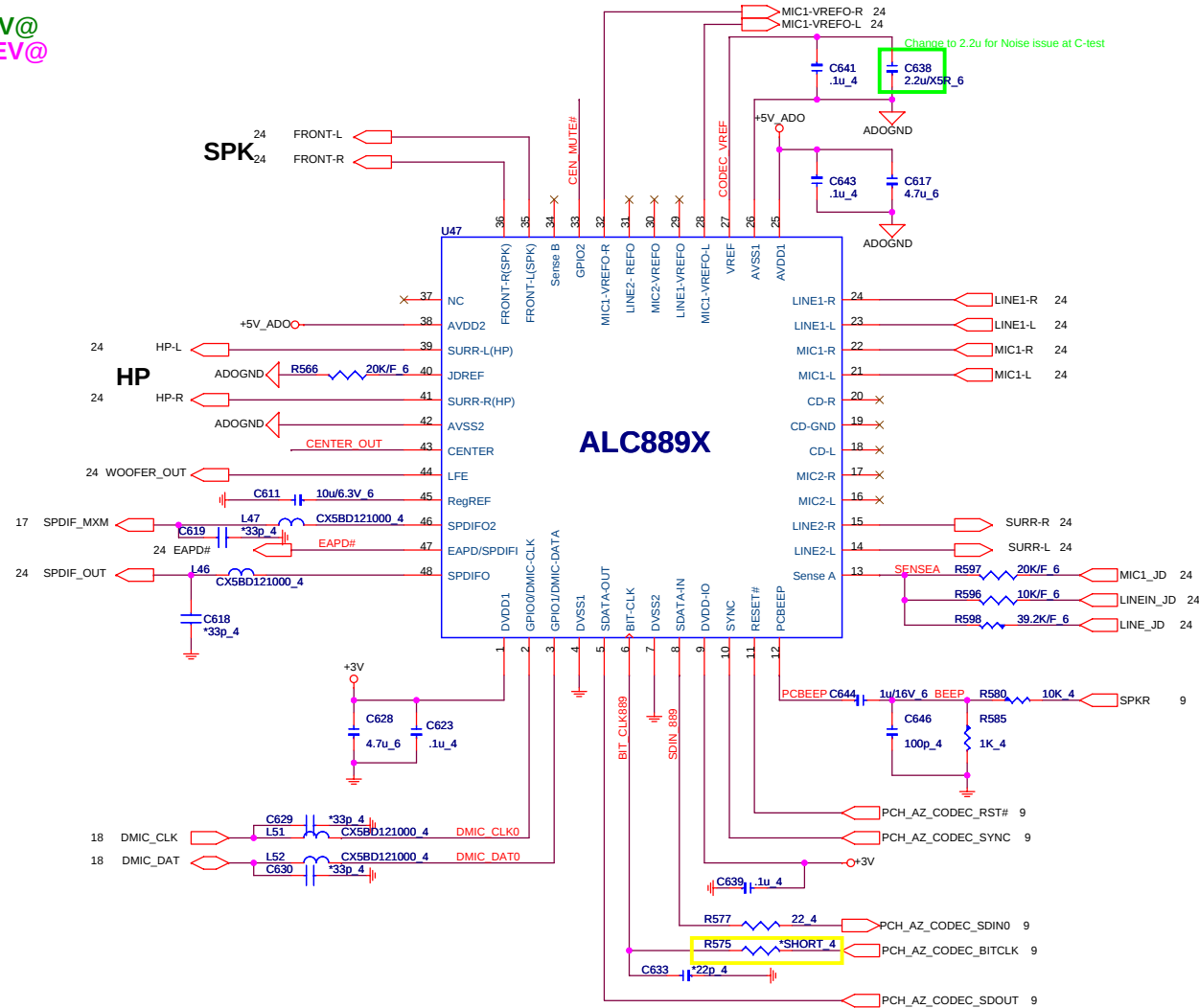


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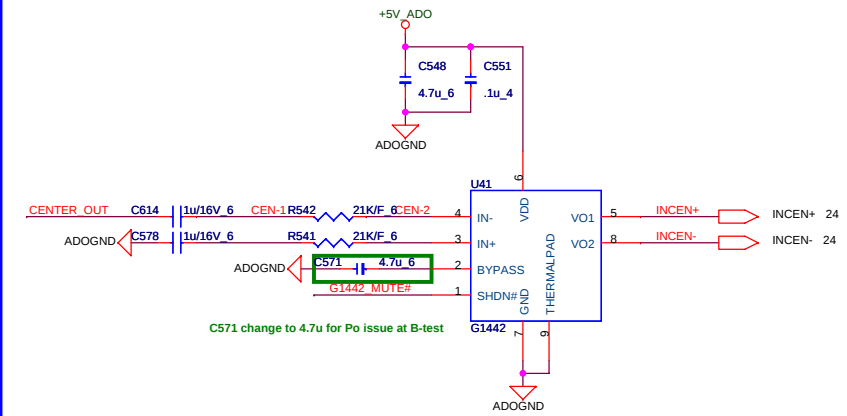
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Size	Document Number	Rev
	SATA-HDD/ODD	3A
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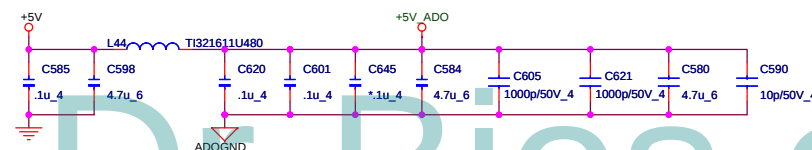
CODEC(ALC889X)

IV@
EV@

CENTER MONO



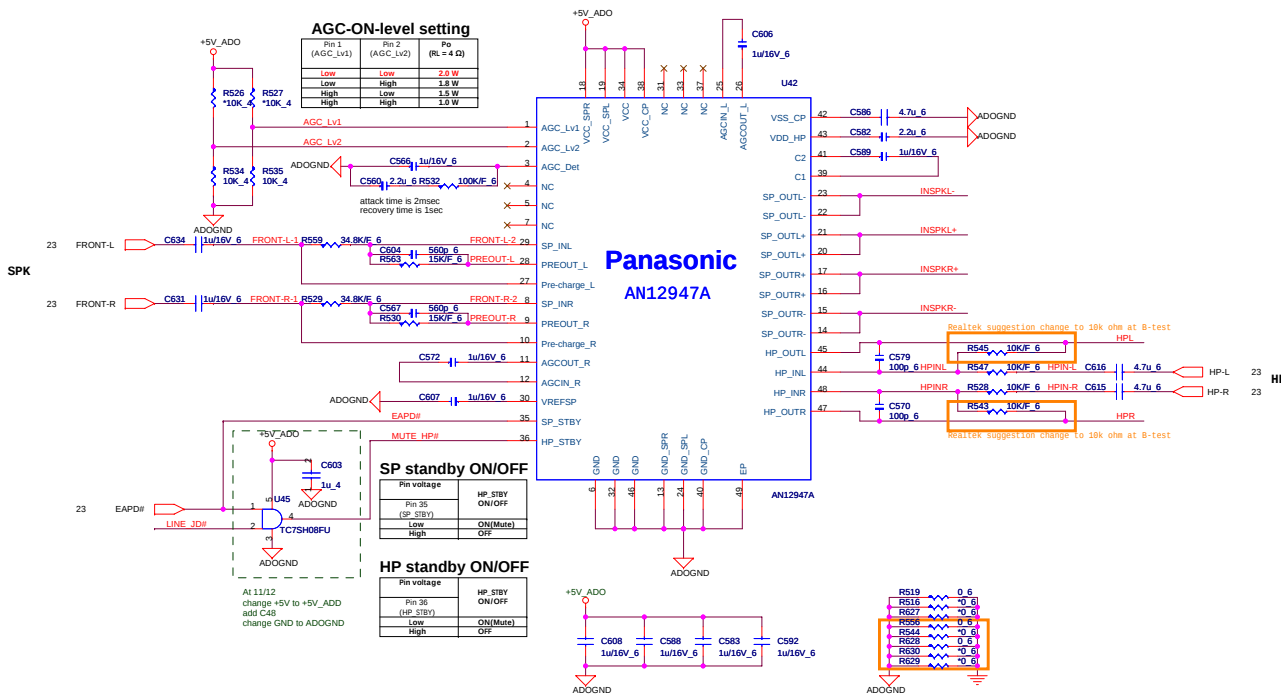
CODEC/AMP Power



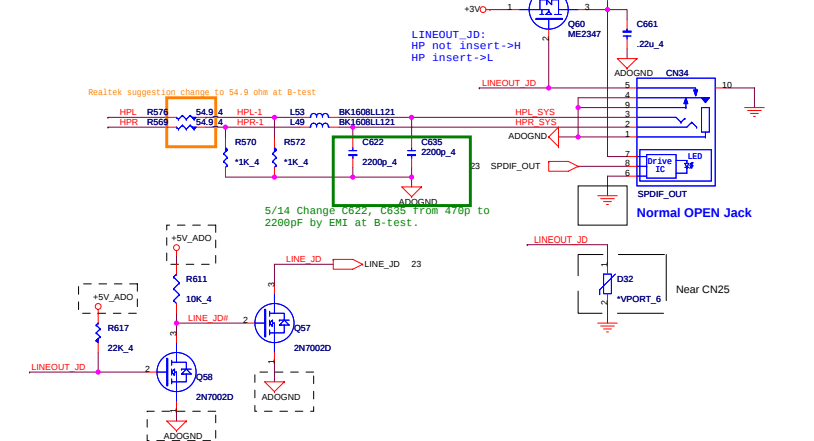
Quanta Computer Inc.
PROJECT : ZY9

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	3A
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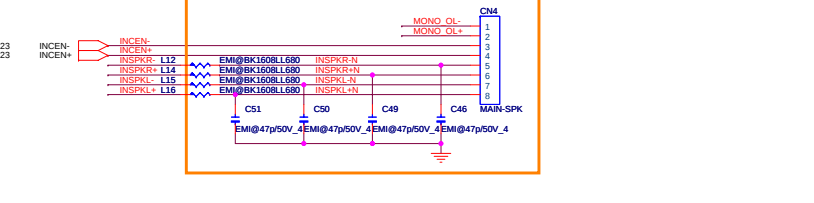
SPEAKER/HP AMP.



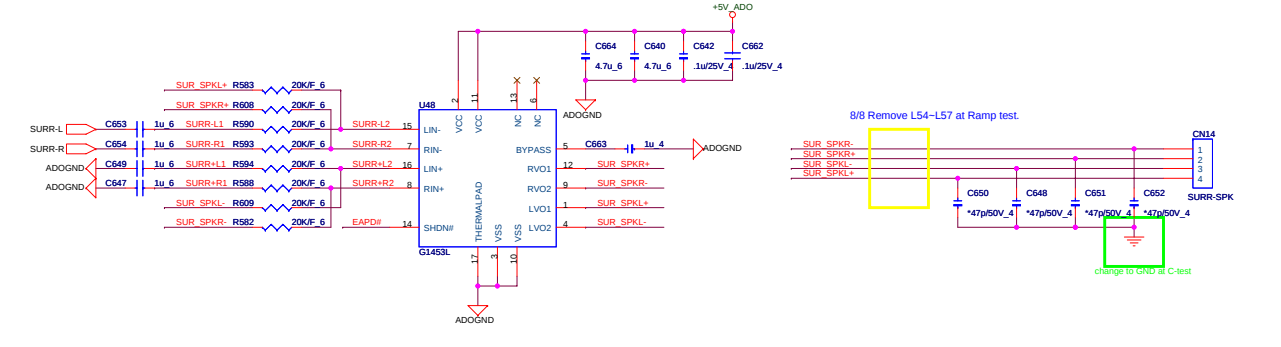
LINE-OUT/SPDIFO



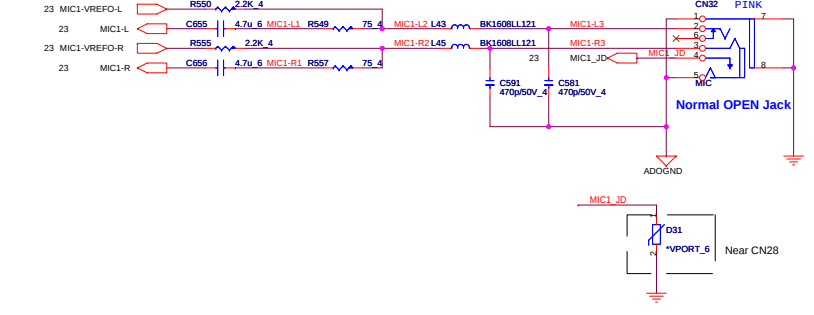
Main SPK/Center/Subwoofer EMI



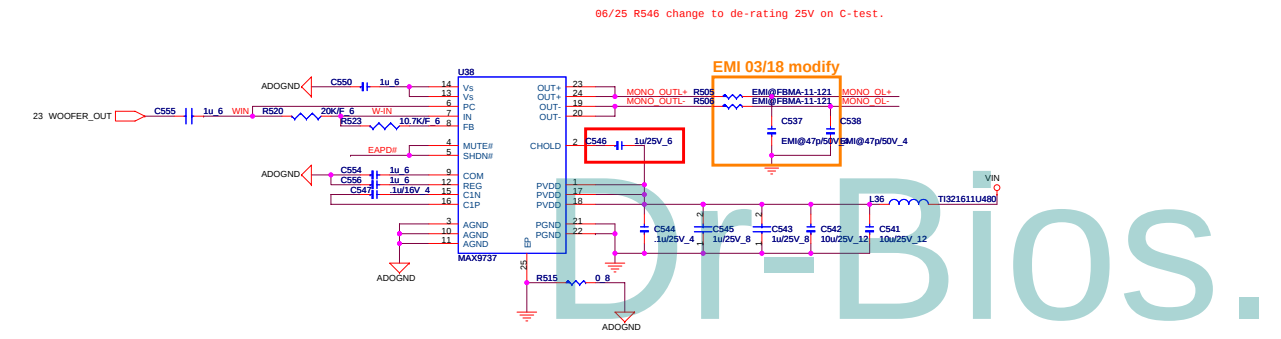
SURR-SPK



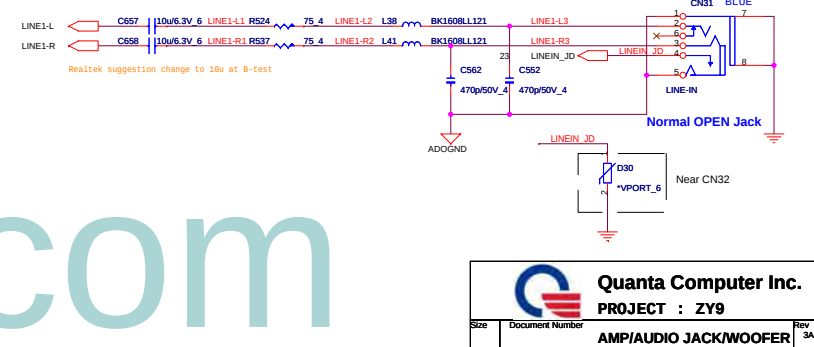
MIC



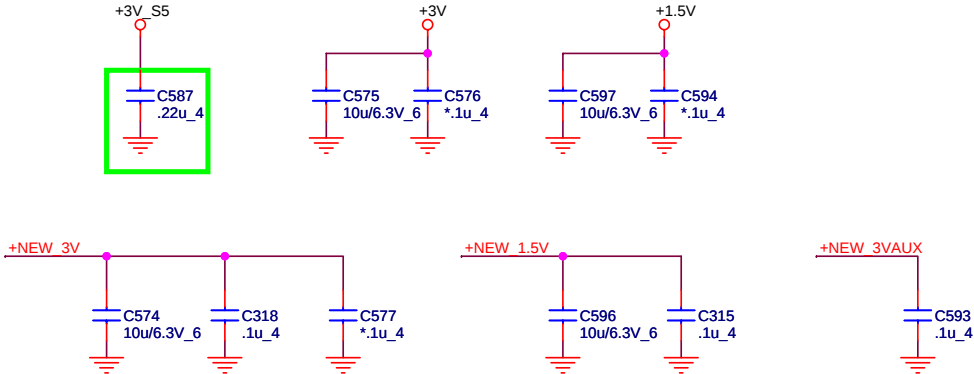
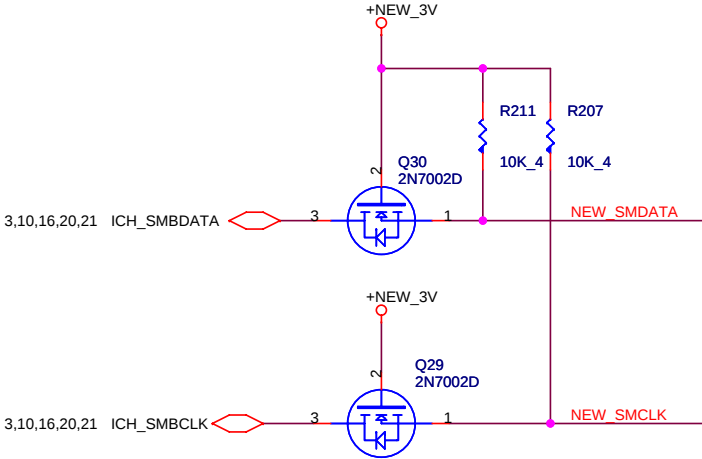
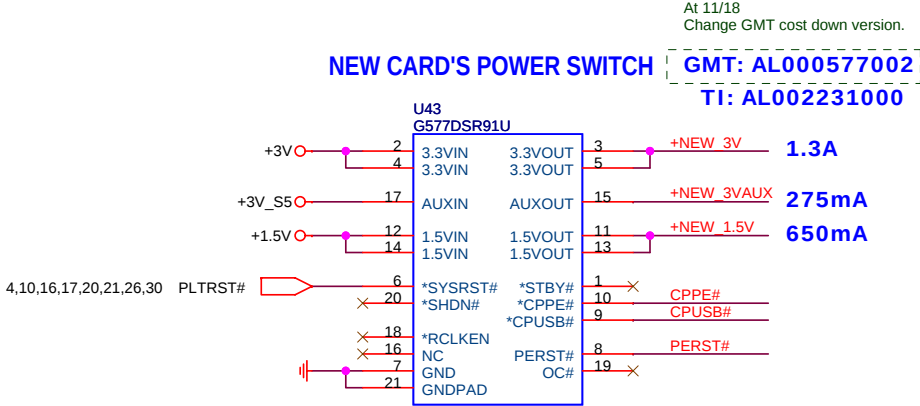
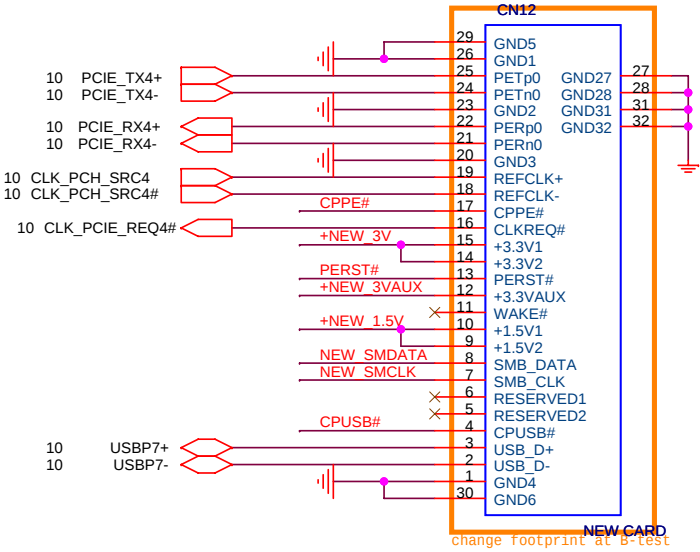
SUBWOOFER



LINE IN



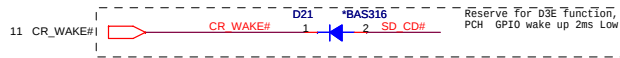
NEW CARD



 **Quanta Computer Inc.**
PROJECT : ZY9

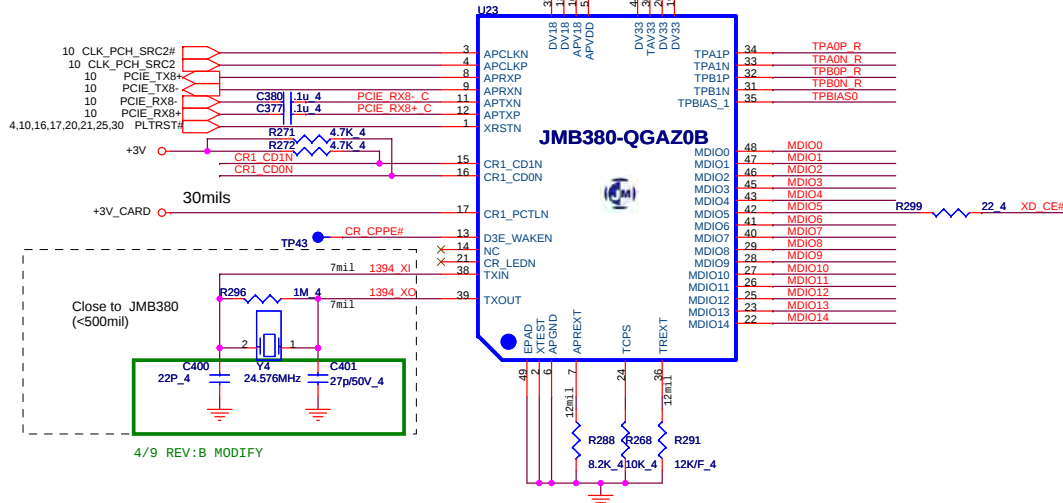
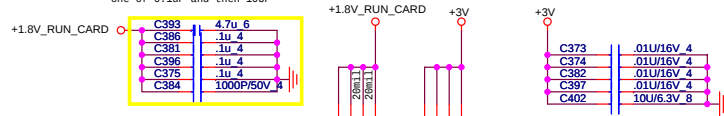
Size	Document Number	Rev
	NEW CARD	3A
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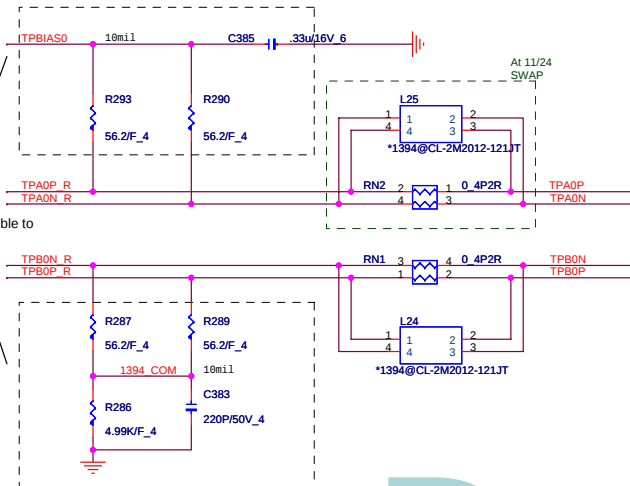


8/14 Stuff C393 and C625, exchange C384 and C386 value by JMicon at Ramp.

please 1000PF is nearest to pin5, one of 0.1uF and then 180F

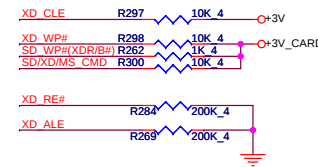
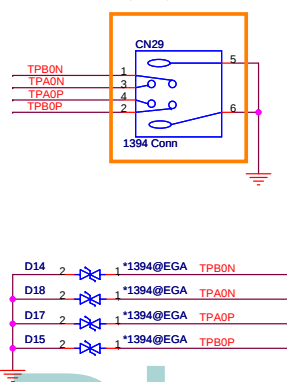


As close as possible to JMB380



1394 Connector

modify footprint at B-test

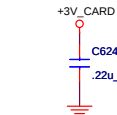


JMB 380 Note:

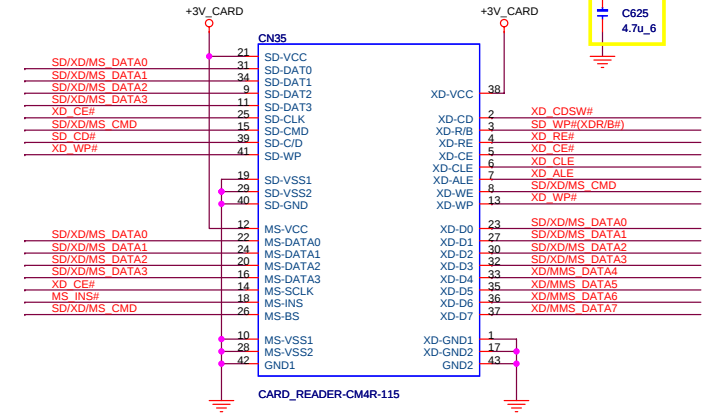
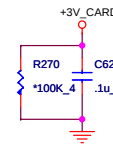
SD/MMC	MS	XD
MDIO0	SD DAT0	MS D0
MDIO1	SD DAT1	MS D1
MDIO2	SD DAT2	MS D2
MDIO3	SD DAT3	MS D3
MDIO4	SD CMD	MS BS
MDIO5	SD CLK	MS SCLK
MDIO6	SD WP	XD WP#
MDIO7	SD DAT4	XD CLE
MDIO8	SD DAT5	XD D4
MDIO9	SD DAT6	XD D5
MDIO10	SD DAT7	XD D6
MDIO11	SD DAT8	XD D7
MDIO12	SD DAT9	XD RE#
MDIO13	SD DAT10	XD R/B#
MDIO14	SD DAT11	XD ALE
CR1 LEDN	SD1 LED#	MS1 LED#
CR1 PCTLN	SD1 PCTLMS1	PCTLMS1 PCTL#
CR1 CD0	SD1 CD#	XD CV#
CR1 CD1	MS1 CD#	XD CD#

5 IN 1 CARD READER

As close as possible to CN24 Pin21



As close as possible to CN24 Pin12



EMI 8/6 REV:D MODIFY to short pad.

MDIO0	R632	*SHORT 4	SD/XDMS DATA0
MDIO1	R633	*SHORT 4	SD/XDMS DATA1
MDIO2	R642	*SHORT 4	SD/XDMS DATA2
MDIO3	R643	*SHORT 4	SD/XDMS DATA3
MDIO4	R644	*SHORT 4	SD/XDMS CMD
MDIO5	R645	*SHORT 4	XD WP#
MDIO6	R646	*SHORT 4	XD CLE
MDIO7	R647	*SHORT 4	XD D4
MDIO8	R648	*SHORT 4	XD D5
MDIO9	R649	*SHORT 4	XD D6
MDIO10	R650	*SHORT 4	XD D7
MDIO11	R651	*SHORT 4	XD RE#
MDIO12	R652	*SHORT 4	XD R/B#
MDIO13	R653	*SHORT 4	XD ALE
MDIO14	R654	*SHORT 4	MS INS#
CR1 CDIN	R655	*SHORT 4	SD CD#



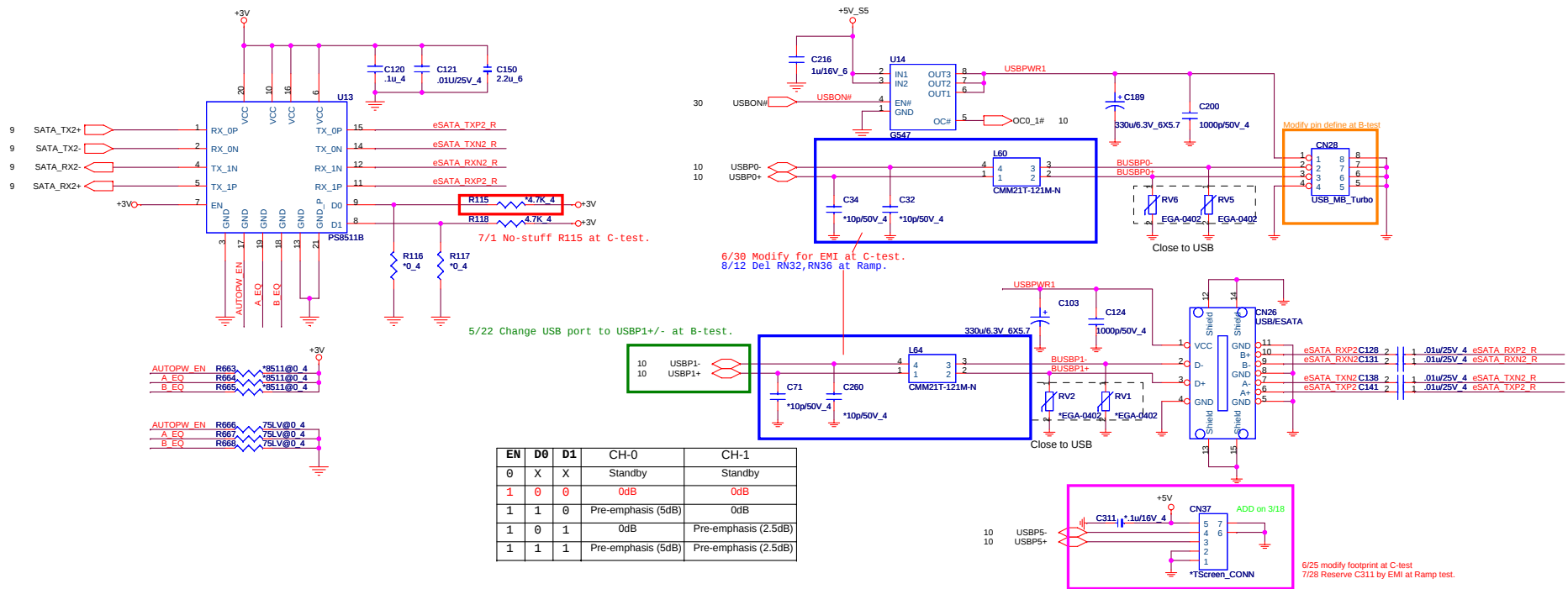
Quanta Computer Inc.
PROJECT : ZY9

Size	Document Number	Rev
	JMB380 Card Reader & 1394	3A

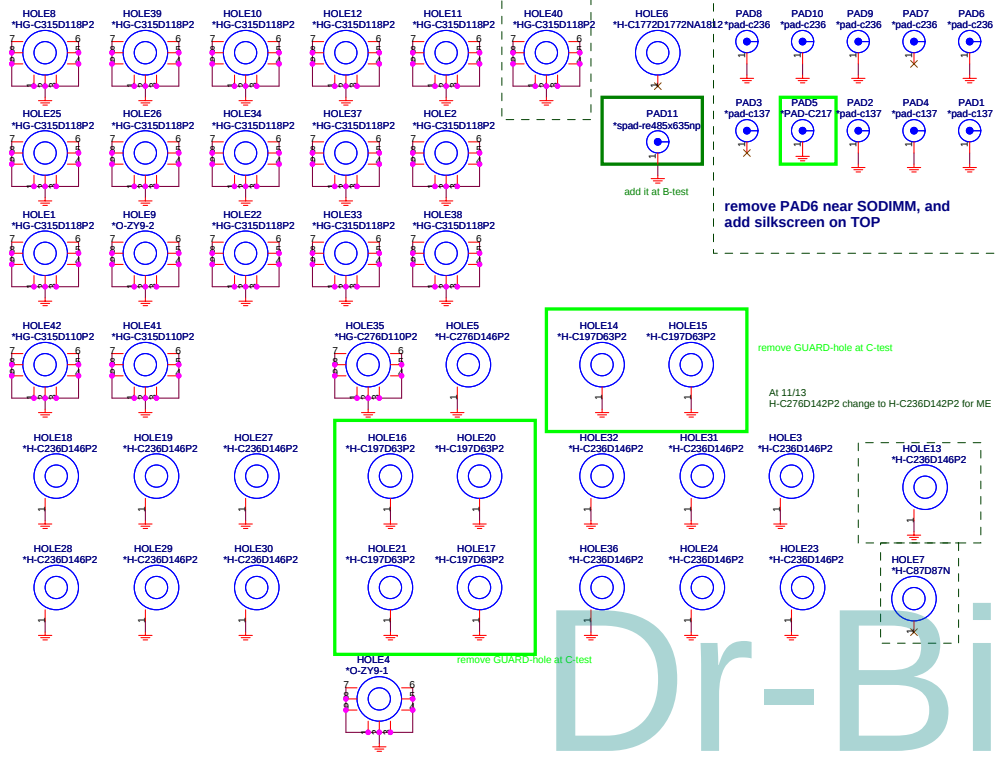
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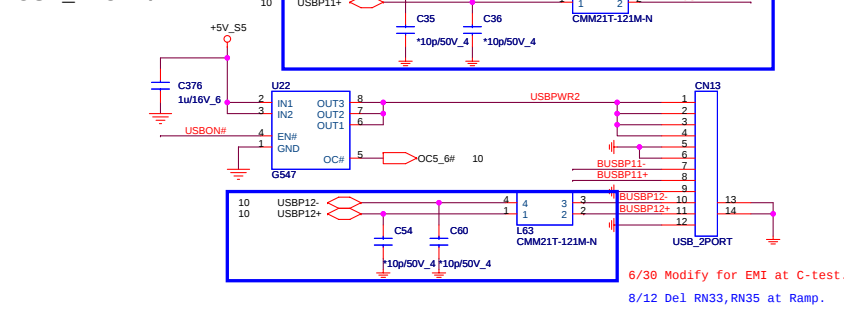
USB & ESATA



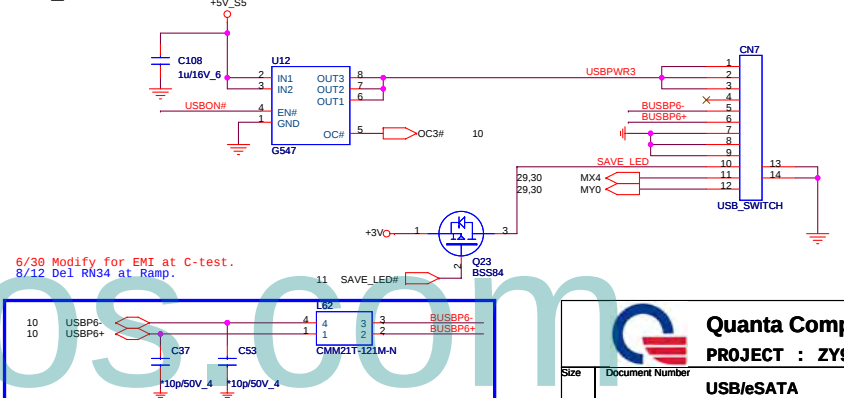
HOLES



USB_2PORT/B

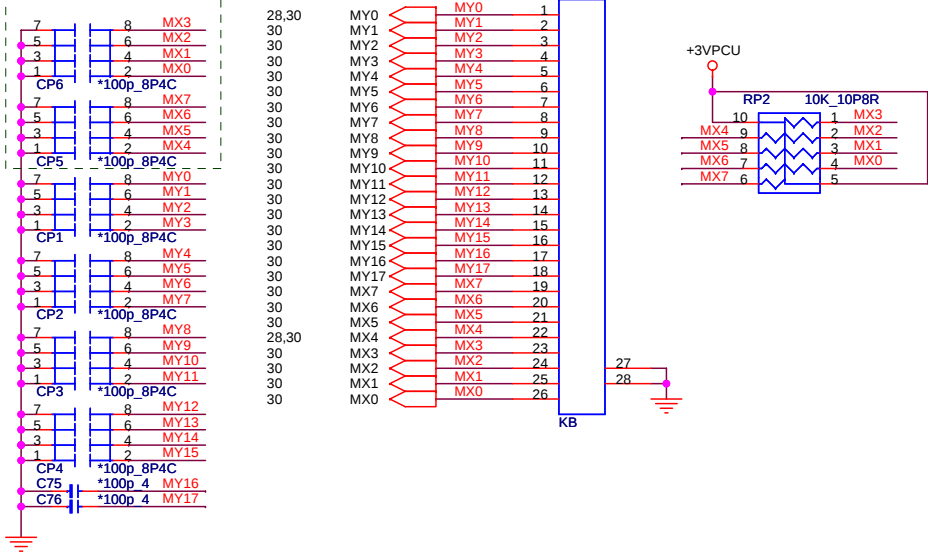


USB_SWITCH/B

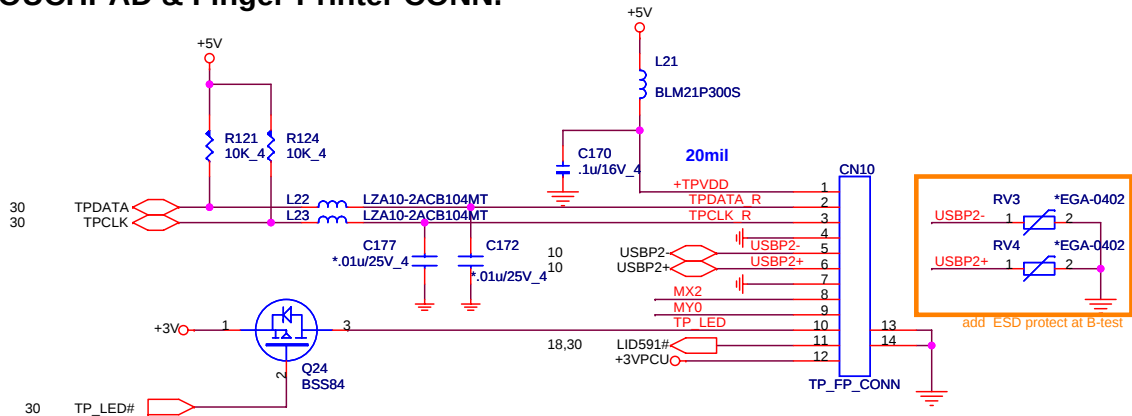


INT K/B

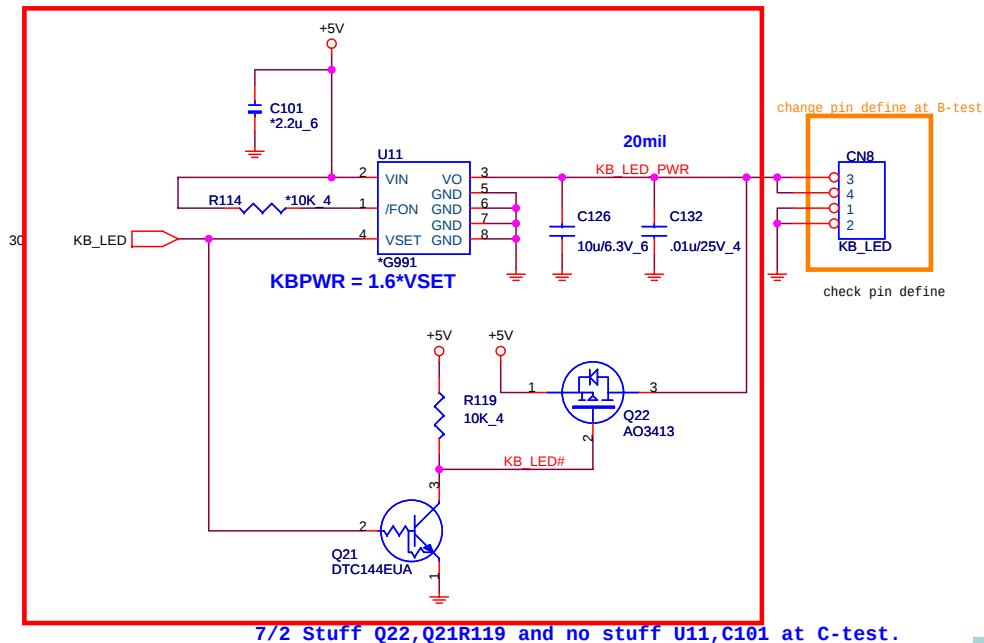
At 11/18
SWAP



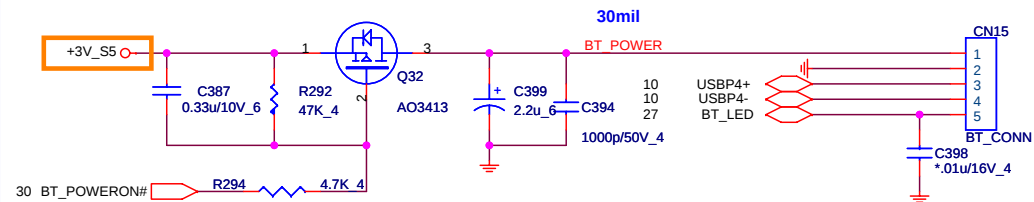
TOUCHPAD & Finger-Printer CONN.



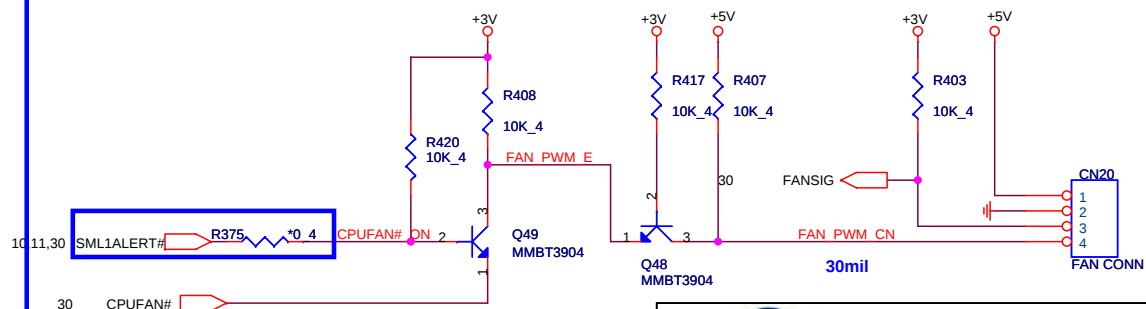
Keyboard LED control



BLUETOOTH CONNECTOR



CPU FAN



5/13 Reserve R375 by EC at B-test.
6/25 Stuff R375 by EC at C-test.
7/22 Un-stuff R375 by EC at Ramp.

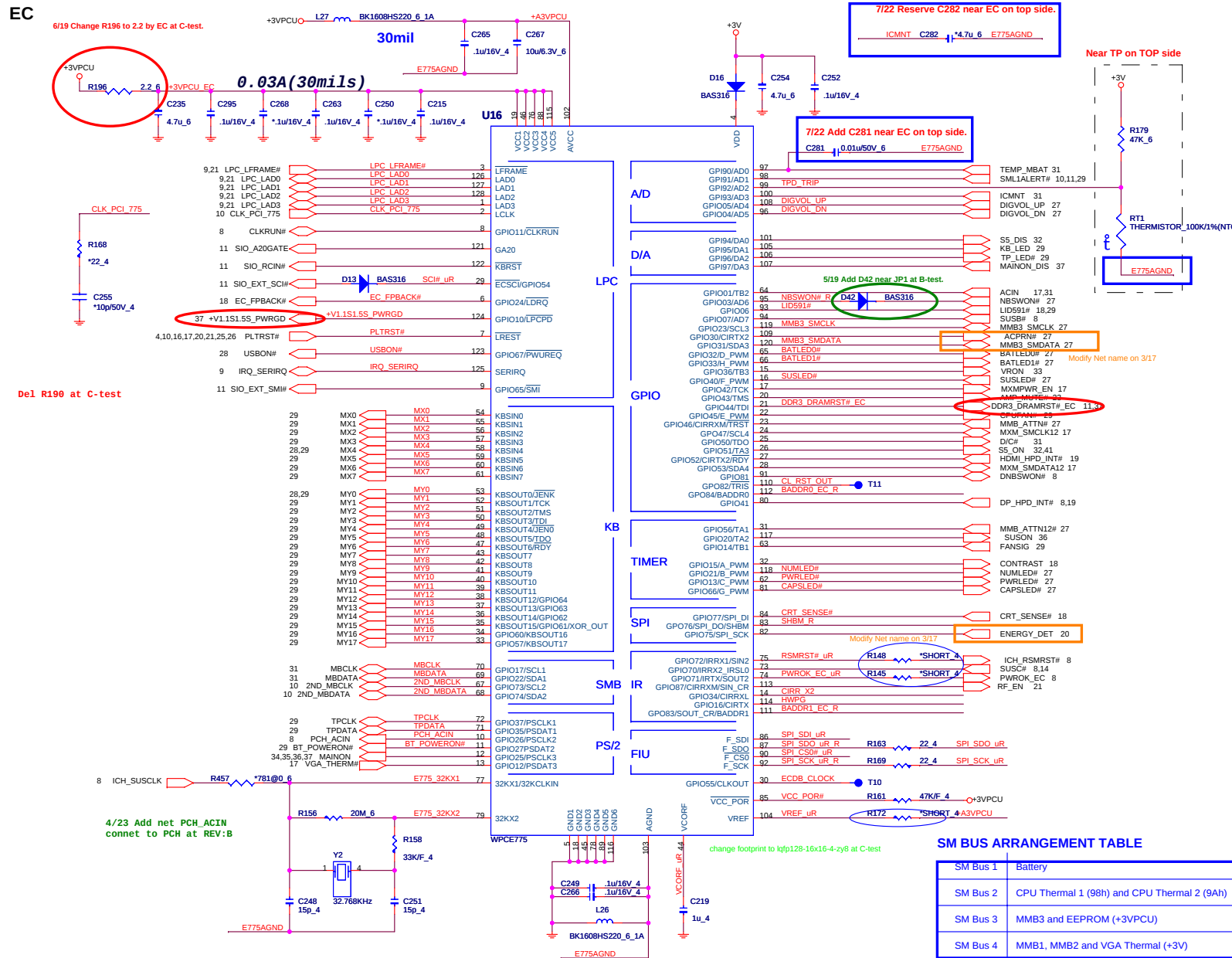


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Size	Document Number	Rev
	KB/FAN/TP+FP/BT	3A

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I/O ADDRESS SETTING

I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

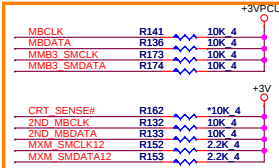
SHBM=0: Enable shared memory with host BIOS



7/1 Add R12 by EC at C-test

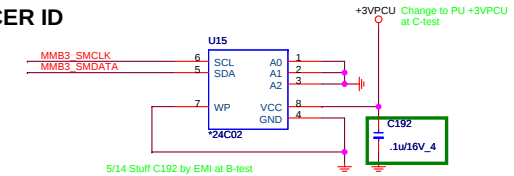
1/13 Confirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

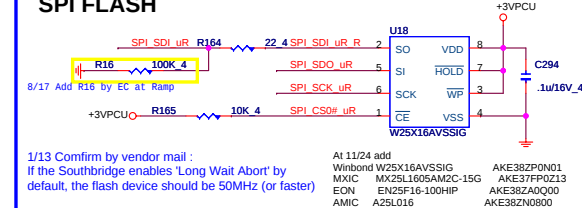


change to 10K ohm,
2nd MBCLK/MBDATA and MXM_SMCLK12/MXM_SMDATA12 PU to +3V at B-test

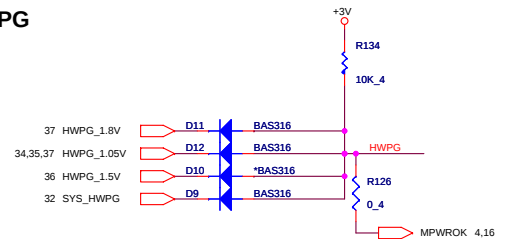
ACER ID



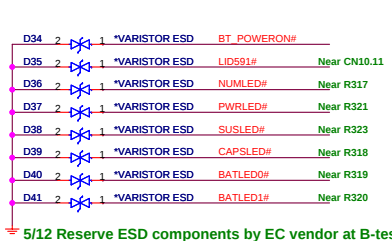
SPI FLASH



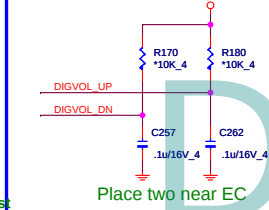
HWPG



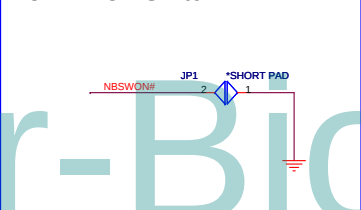
ESD Protection



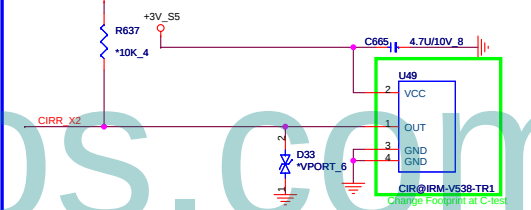
VR Cap.



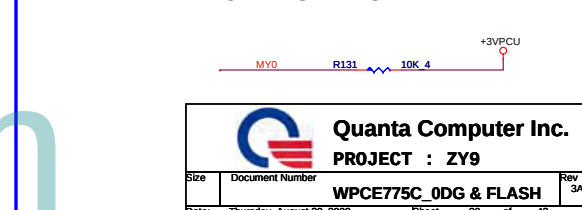
POWER-ON Switch

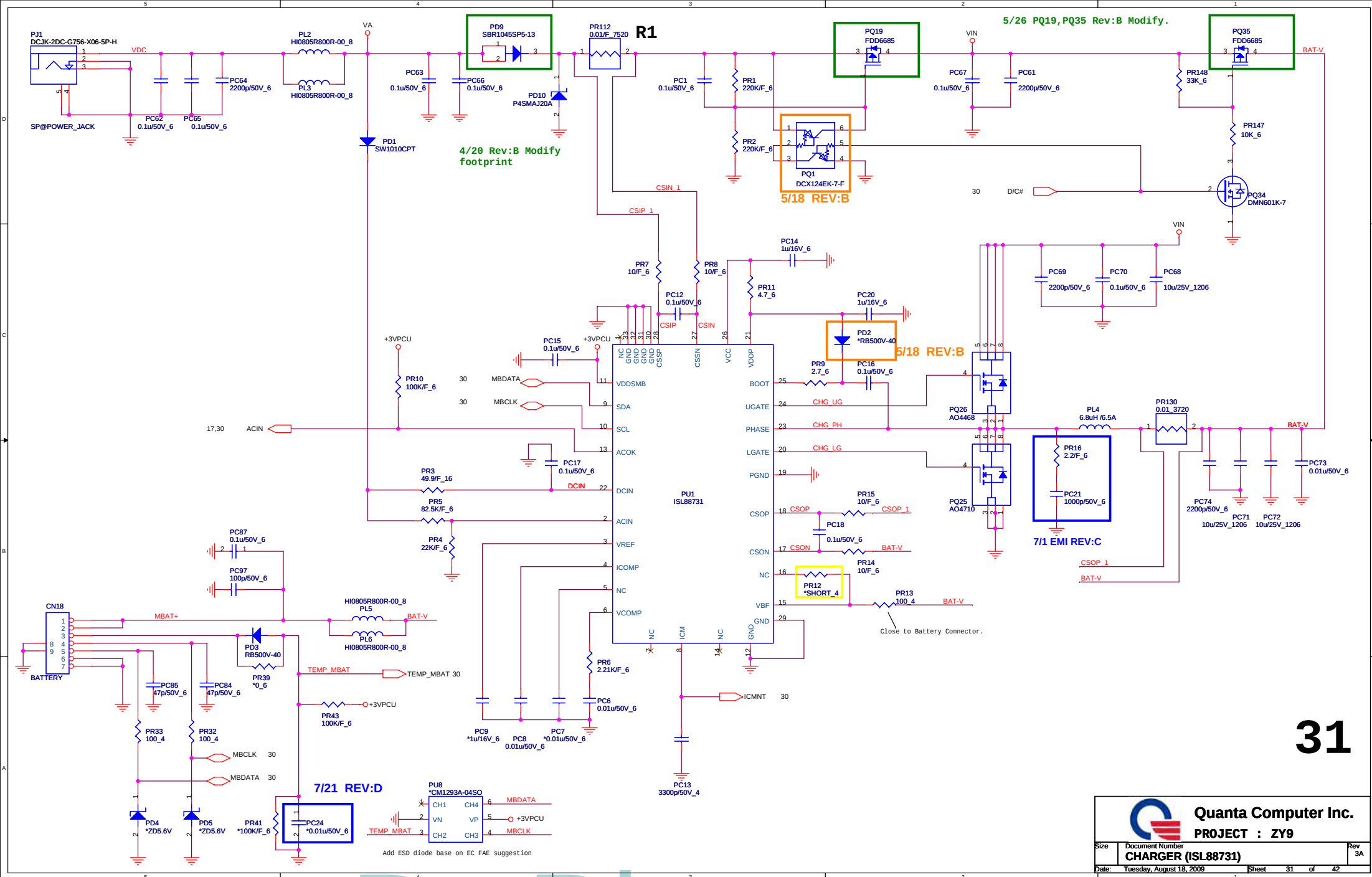


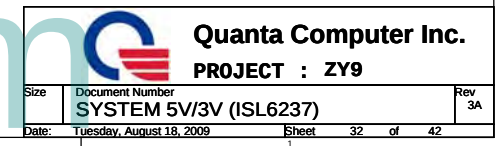
CIR

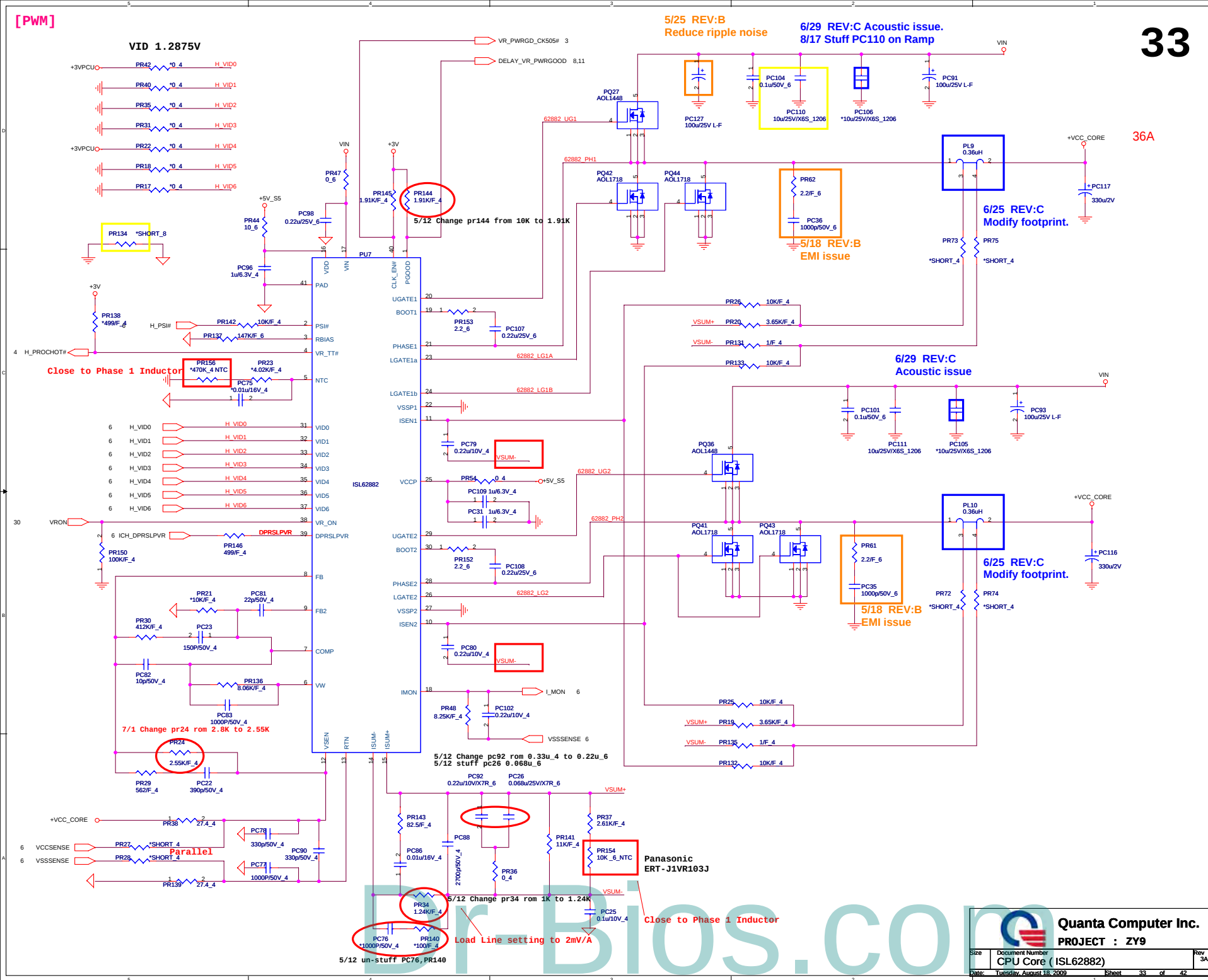


INTERNAL KEYBOARD STRIP SET



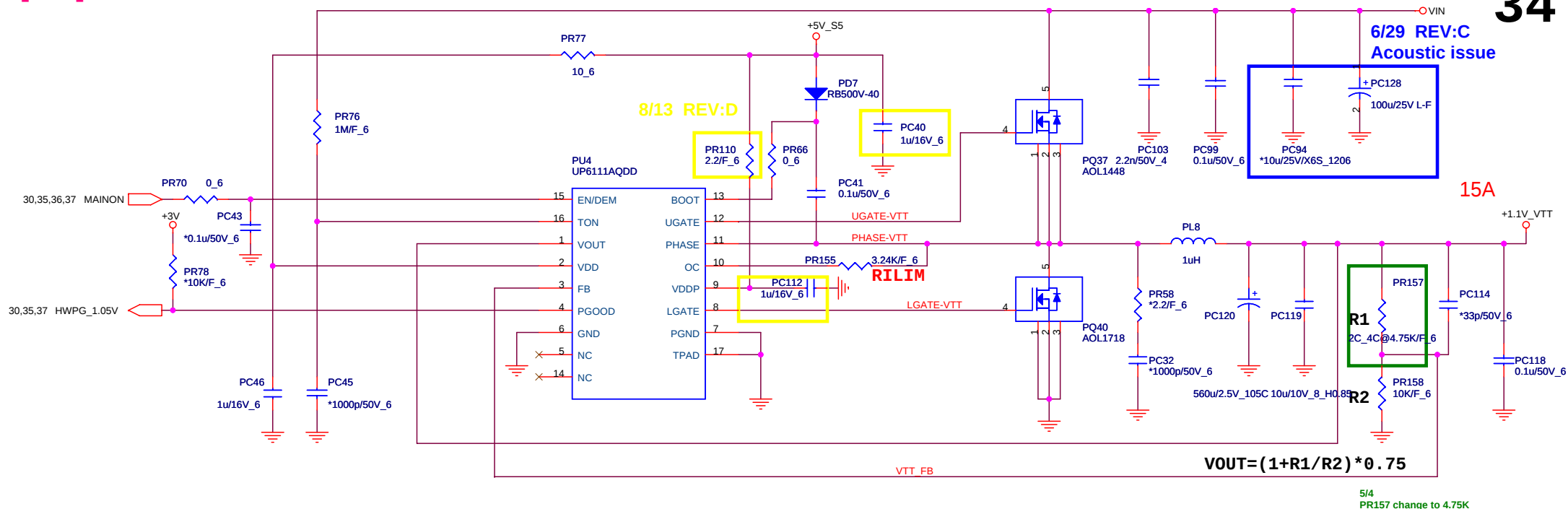






6/29 REV:C
Acoustic issue

15A



A01718 Rdson=3~4.3mOhm

Aurbundale (1.05V)

Clarksfield(1.1V)

R1 = 4.02K (CS24023F928)

R1 = 4.75K (CS24753F919)

L(ripple current)

$$= (19 - 1.05) * 1.05 / (1u * 272k * 19)$$

~3.64A

4.3m*15=RILIM*20uA

RILIM=3.24K(3.22K)

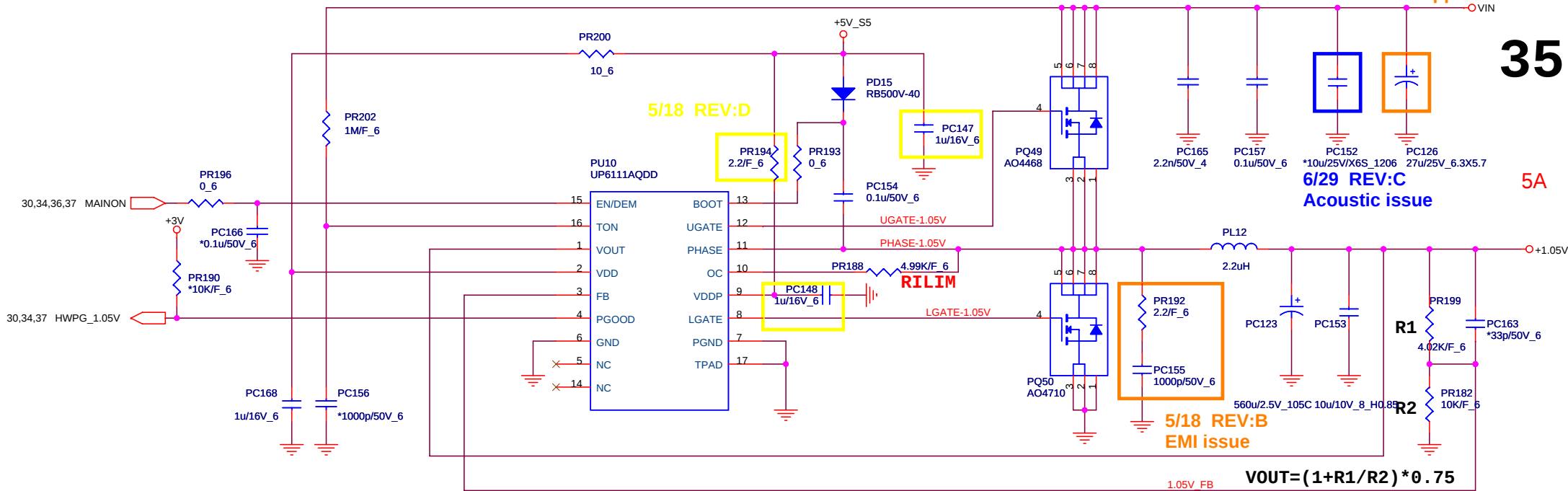


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Size	Document Number	Rev
	+VTT (UP6111A)	3A
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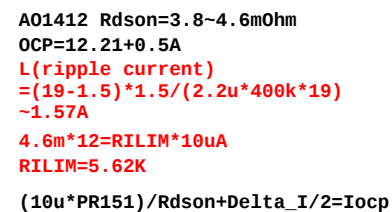
[PWM]

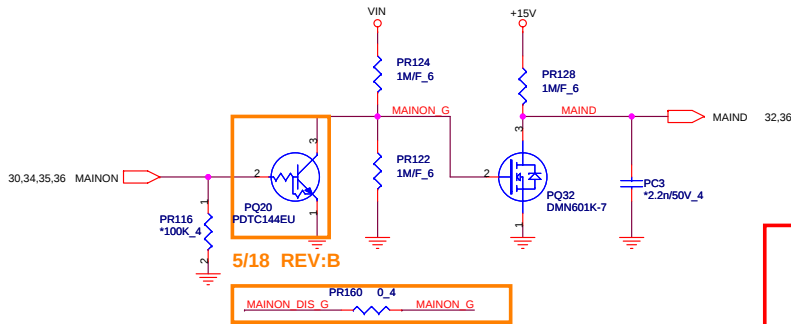
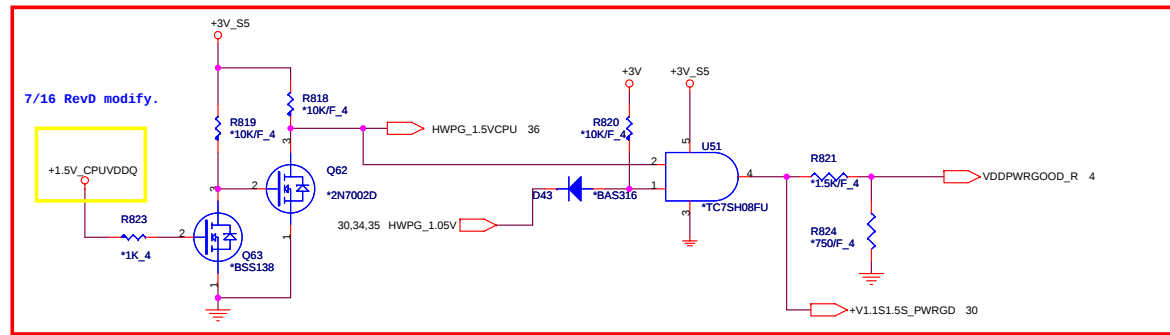


A04710 $R_{ds(on)} = 11.8 \sim 14.2 \text{ m}\Omega$
 OCP = 7.2 - 0.8A
 $L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (2.2 \mu * 272 \text{ k} * 19)$
 $\sim 1.6577 \text{ A}$
 $14.2 \text{ m} * 7 = \text{RILIM} * 20 \mu \text{A}$
 $\text{RILIM} = 4.99 \text{ K} (4.97 \text{ K})$

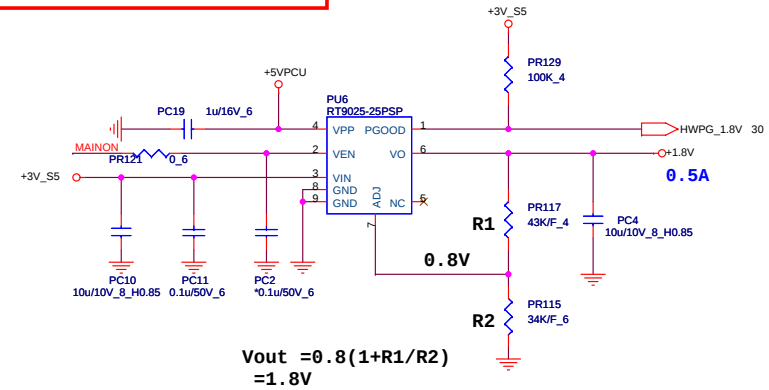
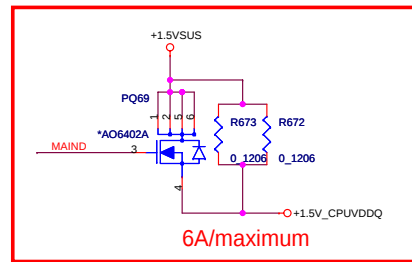
Quanta Computer Inc.
PROJECT : ZY9

Size	Document Number	Rev
	+1.05V(UP6111AQDD)	3A
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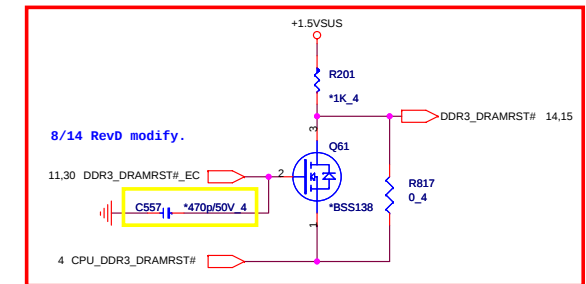
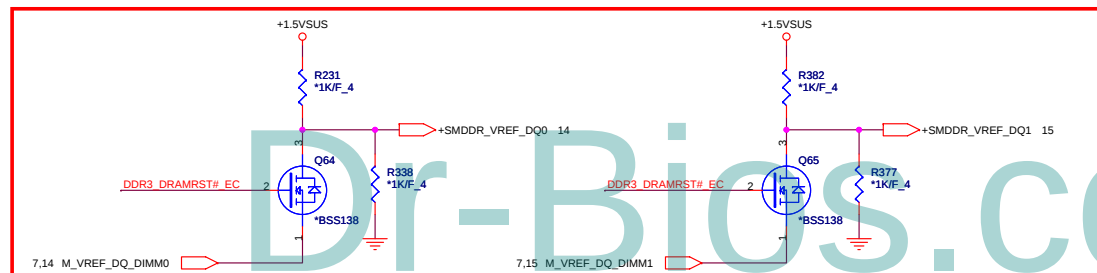
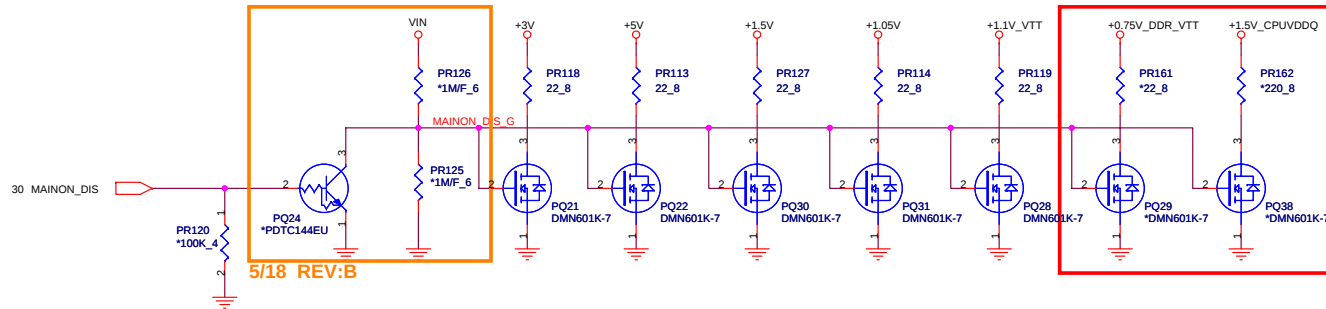
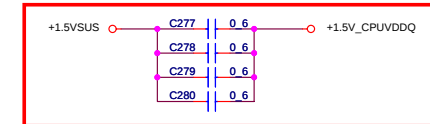


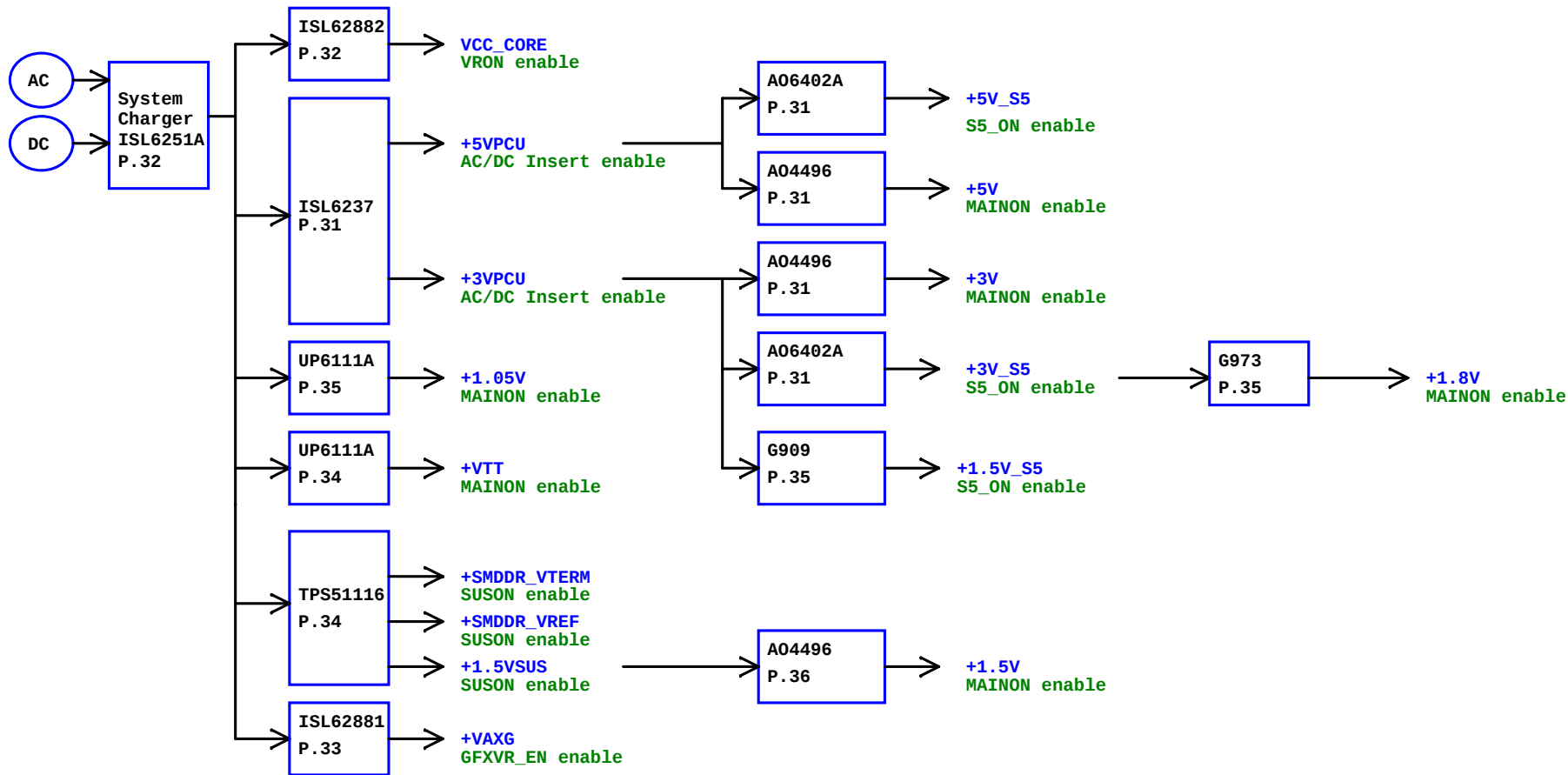


5/25 stuff PR160, no stuff PQ24, PR126, PR125 at B test.



S3 power solution: C277-C280 stuff 0.1uF cap;
Normal : Stuff 0ohm to short.





Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.5VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC, Cardreader (OZ129T)
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M

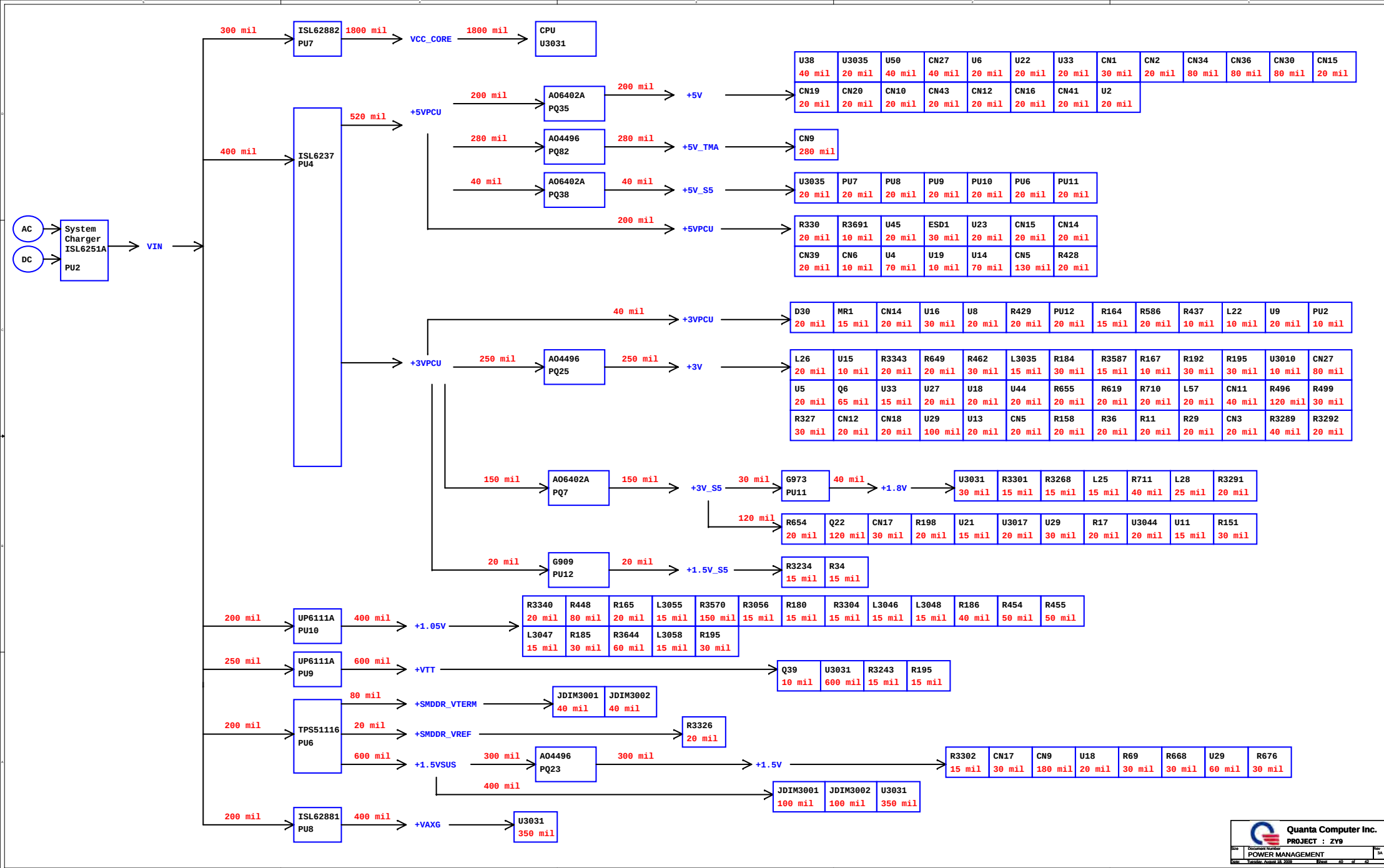
PCH POWER PLANE

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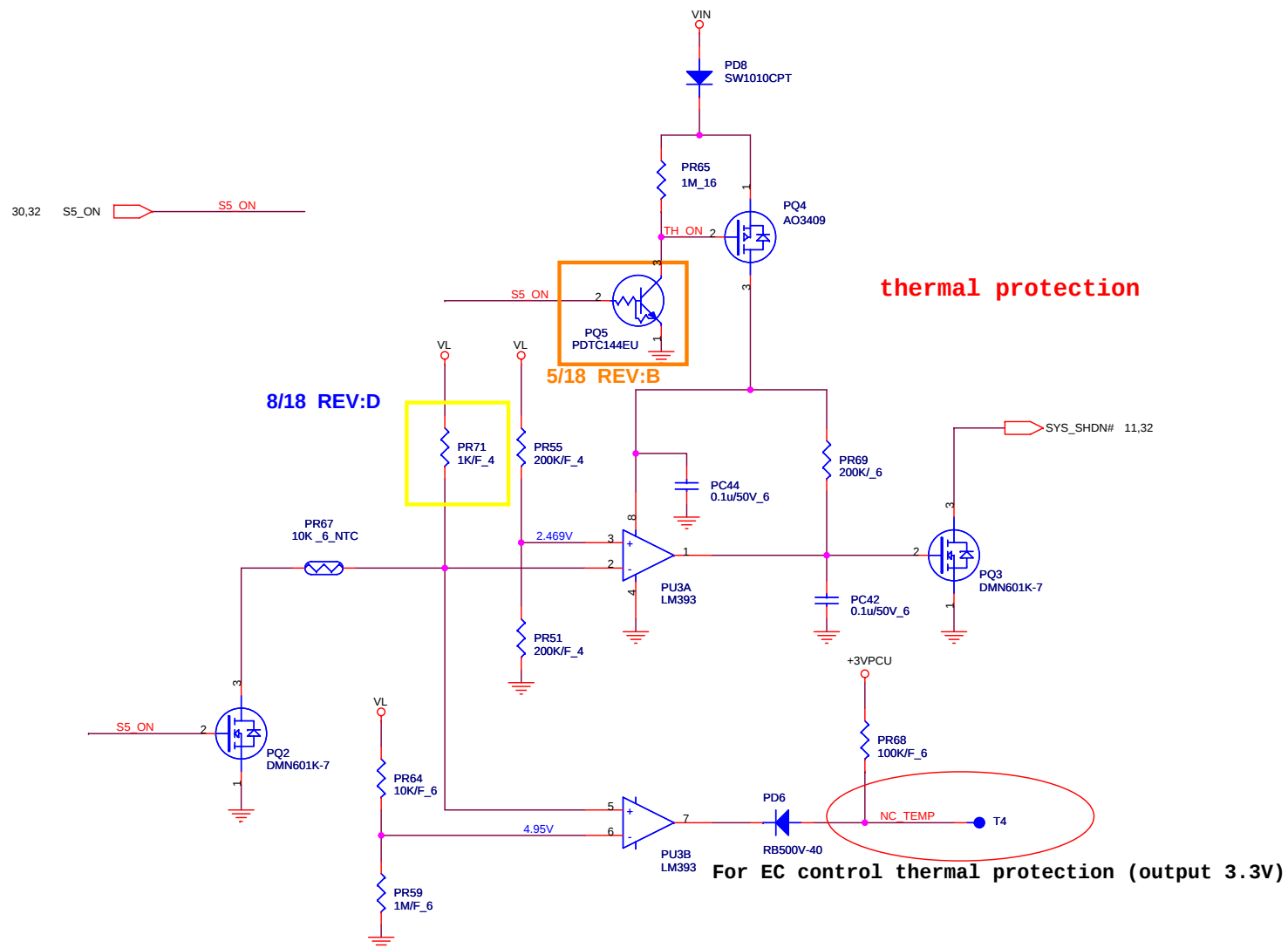
LOGIC	SUPPLY	LEVEL	S0	S3	S4	S5
Fast Flash	VccpNAND	+1.8V/+3.3V	ON	OFF	OFF	OFF
Core	DcpSusByp	+1.05V	ON	OFF	OFF	OFF
CPU	V_CPU_IO	+VTT	ON	OFF	OFF	OFF
PCI	V5REF	+5V/+3V	ON	OFF	OFF	OFF
USB	V5REF_Sus	+5V_S5/+3V_S5	ON	ON	ON	ON
DisplayPort, SATA, PCI	VCC3_3	+3V	ON	OFF	OFF	OFF
Core	VccCore	+1.05V	ON	OFF	OFF	OFF
PCIE/DMI	VccDMI	+VTT/+1.05V	ON	OFF	OFF	OFF
Fast Flash	VccME3_3	+3V	ON	OFF	OFF	OFF
PCIE/DMI,SATA,USB	VccIO	+1.05V	ON	OFF	OFF	OFF
Core	VccLAN	+1.05V	ON	OFF	OFF	OFF
Core	VccME	+1.05V	ON	OFF	OFF	OFF
RTC	VccRTC	+VCCRTC	ON	ON	ON	ON
USB&PCI	VccSus3_3	+3V_S5	ON	ON	ON	ON
IntelR HD Audio	VccSusHDA	+1.5V_S5	ON	ON	ON	ON
Core	VccVRM	+V1.5S_1.8S	ON	OFF	OFF	OFF
CLK	VccAClk	+1.05V	ON	OFF	OFF	OFF
CRT	VccADAC	+3V	ON	OFF	OFF	OFF
DPLL	VccADPLL	+1.05V	ON	OFF	OFF	OFF
DPLL	VccADPLLb	+1.05V	ON	OFF	OFF	OFF
PCie/DMI	VccapIEXP	+1.05V	ON	OFF	OFF	OFF
IntelR FDI	VccFDIPLL	+1.05V	ON	OFF	OFF	OFF
SATA	VccSATAPLL	+1.05V	ON	OFF	OFF	OFF
Display	VccTX_LVDS	+1.8V	ON	OFF	OFF	OFF

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PCH POWER PLANE		
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Model			ZY9	
Model	REV	CHANGE LIST	FROM	To
ZY9 MB	1A	FIRST RELEASED: E200807-???? (PCB: DA0ZY8MB6A0)	X	1A
	4/9 modify	Page4 : R488 change from 4.75K to 1.1Kohm & R488 change from 12K to 3Kohm by D61.52 Page8 : Add R373 to pull up ACIN on PCH side, R274 net PCH_ACIN connector to EC pin19. Page10 : Stuff R227, R257; remove R222, R224 Q2, Q5, Q15-Q20, Q29-Q31, Q35-Q43, Q45-Q47, Q50, Q51, Q57-Q59 : 2N7002E(BAM700200F6) change to 2N7002D(BAM700200H2) with ESD protection by SMT. Page21: Modify LAN connector footprint and material by safety. Page21: Modify CN21,CN23 footprint. Page28: Add PAD11. Page31: Chang PD9 footprint to power-6, 5-1, 84-3p by SMT. Page37 : Stuff PQ28,PQ30,PQ31,PR114,PR119,PR127 by S3 discharge issue. Page3 : Chagne CPU_SEL PU +3V to +1.05V at B-test by SLG. Page14 : R176 un-stuff, R88 stuff at B-test. Page15 : R525 un-stuff, R429 stuff at B-test. Page23 : Change C571 to 4.7u for Po issue when boot at B-test Page26 : Chagne C400 to 22pF, C401 change to 27pF at B-test by HHC. Page32 : Del power net ISL6237_3V and all JP. Page33 : Stuff PR61,PR62,PC35,PC36 by EMI. Page20 : Change CN16 footprint to rj45-jm36111-n2a22-7h-12p-h by safety test. Page34 : Change PR157 from 4.02K to 4.75K ohm for Clarksfied CPU. Page18 : Remove R438, R639 and Reserve RV7,RV8 by ESD at B-test. Page23 : Add U50, C666 and R561 for Po issue by Realtek at B-test. Page11: Reverse R351 connect GPIO48 to EC for Temp Alert & Reverse Q12,Q11 connect to t SYS_SHDN# at B-test. Page30 : Add ESD components D34-D41 with EC signals ; Stuff C192 by EMI & Add D42 near JP1 at B-test. Page29 : Reserve R375 connect to Temp_Alert from PCH at B-test. Page22 : Add R147,R151,R197 for power consumption measure & move C33 near C103 for EMI at B-test. Page21: Change PCIE bus sequence between CN21 and CN23 by BIOS at B-test. Page24 : Change C622, C635 to CH22206KB16 by EMI at B-test. Page34 : Add PR110 at B-test. Page35 : Add PR194 at B-test. Page9 : 5/21 Change R233 to 1Kohm by Intel at B-test. Page14: 5/21 No stuff R187 and change R185,R186; del C260 add R195 by CRB v1.6 at B-test. Page15: 5/21 No stuff R522 and change R518,R521; del C557 add R210 by CRB v1.6 at B-test. Page18: 5/21 change L9,L10,L13(CX8BA750006) from 47ohm to 75ohm by EMI at B-test. Page27: 5/22 Add R212 by pipe LED at B-test. Page10: 5/22 change ESATA USB port10 to port1 and rename OC0_1f, OC3f,OC5_6f; R565 connect to OC5_6f by BIOS at B-test. Page28: 5/22 change ESATA USB port10 to port1 and rename OC0_1f, OC3f,OC5_6f by BIOS at B-test. Page32: 5/25 stuff PR123, no stuff PQ12,PR111,PR159 at B test. Page37: 5/25 stuff PR160, no stuff PQ24,PR126,PR125 at B test. Page31: 5/25 Change PQ19, PQ35 to FDD6685 by power at B test.	1A	2A
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5/4 modify	Page20 : Change CN16 footprint to rj45-jm36111-n2a22-7h-12p-h by safety test. Page34 : Change PR157 from 4.02K to 4.75K ohm for Clarksfied CPU. Page18 : Remove R438, R639 and Reserve RV7,RV8 by ESD at B-test. Page23 : Add U50, C666 and R561 for Po issue by Realtek at B-test. Page11: Reverse R351 connect GPIO48 to EC for Temp Alert & Reverse Q12,Q11 connect to t SYS_SHDN# at B-test. Page30 : Add ESD components D34-D41 with EC signals ; Stuff C192 by EMI & Add D42 near JP1 at B-test. Page29 : Reserve R375 connect to Temp_Alert from PCH at B-test. Page22 : Add R147,R151,R197 for power consumption measure & move C33 near C103 for EMI at B-test. Page21: Change PCIE bus sequence between CN21 and CN23 by BIOS at B-test. Page24 : Change C622, C635 to CH22206KB16 by EMI at B-test. Page34 : Add PR110 at B-test. Page35 : Add PR194 at B-test. Page9 : 5/21 Change R233 to 1Kohm by Intel at B-test. Page14: 5/21 No stuff R187 and change R185,R186; del C260 add R195 by CRB v1.6 at B-test. Page15: 5/21 No stuff R522 and change R518,R521; del C557 add R210 by CRB v1.6 at B-test. Page18: 5/21 change L9,L10,L13(CX8BA750006) from 47ohm to 75ohm by EMI at B-test. Page27: 5/22 Add R212 by pipe LED at B-test. Page10: 5/22 change ESATA USB port10 to port1 and rename OC0_1f, OC3f,OC5_6f; R565 connect to OC5_6f by BIOS at B-test. Page28: 5/22 change ESATA USB port10 to port1 and rename OC0_1f, OC3f,OC5_6f by BIOS at B-test. Page32: 5/25 stuff PR123, no stuff PQ12,PR111,PR159 at B test. Page37: 5/25 stuff PR160, no stuff PQ24,PR126,PR125 at B test. Page31: 5/25 Change PQ19, PQ35 to FDD6685 by power at B test.	1A	2A	
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