Compal Confidential

PEW71/91/51 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

NV N11P-GV2H and N11P-GE,N12P-GS N12P-GV-OP With Optimus

2010-12-29

REV:1.0

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Model Name : PEW71/91/51
File Name : LA5894P

Fan Control
page 41

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-VB-GRT
133/120/100/96/14.318MHZ to PCH
page 12

NV N11P-GV2H
NV N11P-GE
NV N12P-GS
page 22,23,24,25,26,27

PEG(DIS) 100MHz PCI-E 2.0x16 5GT/s PER LANE
133MHz

Intel
Arrandale (UMA/DIS)
Processor
rPGA988A
page 4,5,6,7,8,9

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 800/1066

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
page 10,11

LVDS(DIS)
HDMI(DIS)
CRT(DIS)

HDMI Conn.
page 30

CRT Conn.
page 29

LVDS Conn.
page 28

FDI x8 (UMA)
100MHz
2.7GT/s

DMI x4
100MHz
1GB/s x4

USB conn x3
USB port 1
USB port 0, 2 on USB/B
page 35

Bluetooth Conn
USB port 11
page 35

CMOS Camera
USB port 8
page 28

Card Reader
RTS5160
USB port 9
page 35

USBx14
3.3V 48MHz

HDMI(UMA)
HDMI Level Shift
page 30

LVDS(UMA)
CRT(UMA)
TMDS(UMA)

Intel
Ibex Peak-M
PCH
page 13,14,15,16
17,18,19,20,21

HD Audio
3.3V 24MHz

HDA Codec
ALC272X
page 39

PCI-Express x 8 (ARD PCIE2.0 2.5GT/s)
100MHz

SATA x 6 (GEN1 1.5GT/S ,GEN2 3GT/S)
100MHz

SPI

port 2
MINI Card x2
WLAN, WWAN
USB port 12,13
page 34

port 1
LAN(GbE)
BCM57780
page 32

RJ45
page 33

port 0
SATA HDD Conn.
page 31

port 1
SATA CDROM Conn.
page 31

SPI ROM x1
page 13

Audio AMP
TI TPS6017
page 40

Int. Speaker
page 40

Phone Jack x 2
page 40

LPC BUS
33MHz

ENE KB926
page 36

Touch Pad
page 37

Int.KBD
page 37

EC ROM
page 37

CPU XDP
page 5

PCH XDP
page 21

Sub-board

LS-5891P
USB/B 2 Ports
USB Port 0,2
page 35

LS-5896P
Card Reader
USB Port9
RTS5160
page 35

LS-5893P
Power/B
page 38

LS-5894P
LID_SW/B

LS-5895P
3G
USB Port10,13
page 35

RTC CKT.
page 15

Power On/Off CKT.
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DC/DC Interface CKT.
page 42

Power Circuit DC/DC
page 43~53

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config move to page 56

VRAM BOM Config
X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM

X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA ONLY	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
UMA ONLY & OPTIMUS	UMOP@
3G	3G@
Blue Tooth	BT@
OPTIMUS	OPT@
NonSG SKU	NonSG@
NEW71	71@
NEW91	91@
N11P-GV2H	GV2H@
N11P-GE1	GE1@
N11P-GV2H-A2	GV2HA2@
N11P-GV2H-A3	GV2HA3@
Non OPT SKU	NonOPT@
SG or OPT	SGOPT@
N11P-GE	GE@
N12P-GS	GS@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

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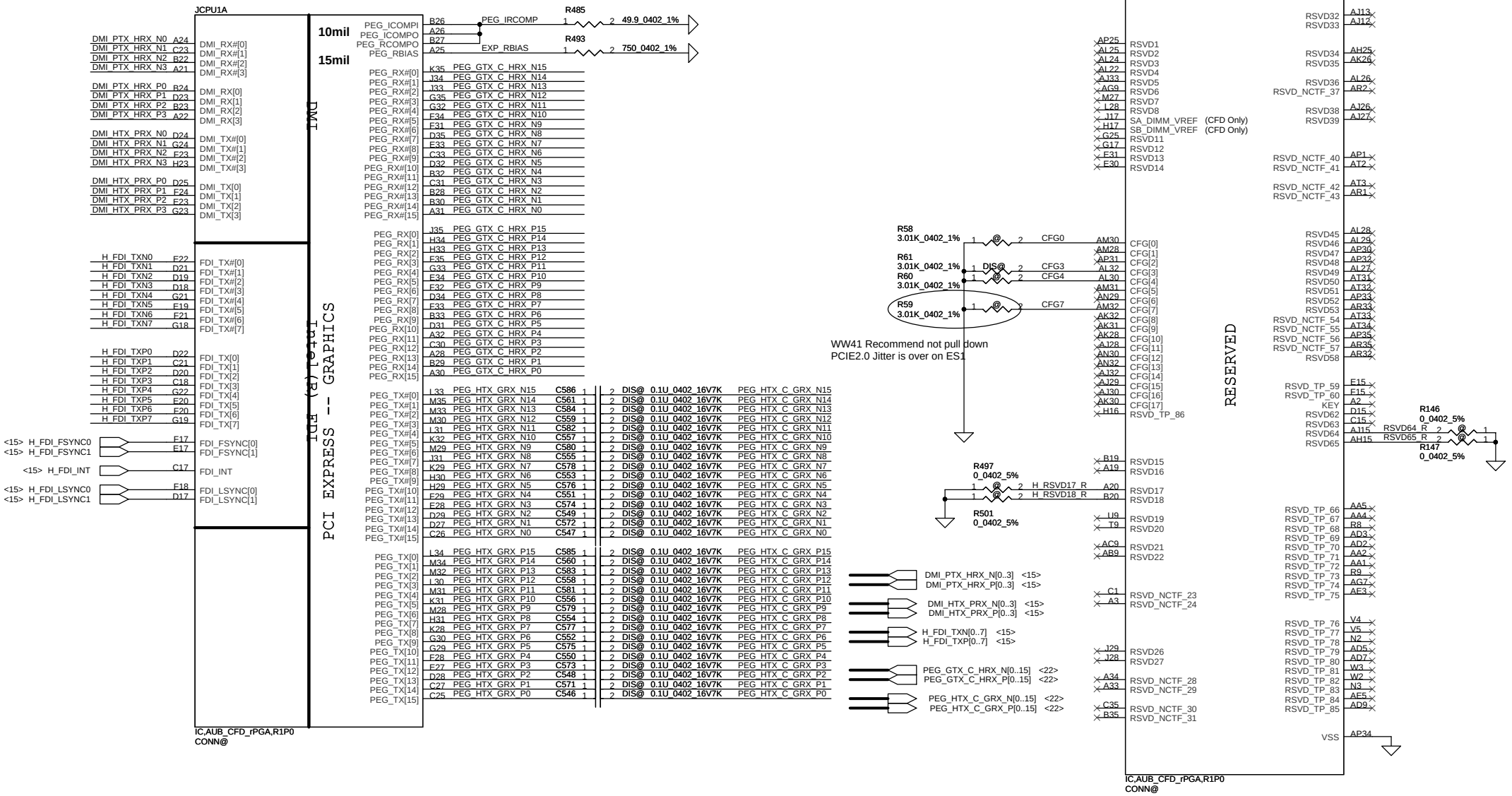

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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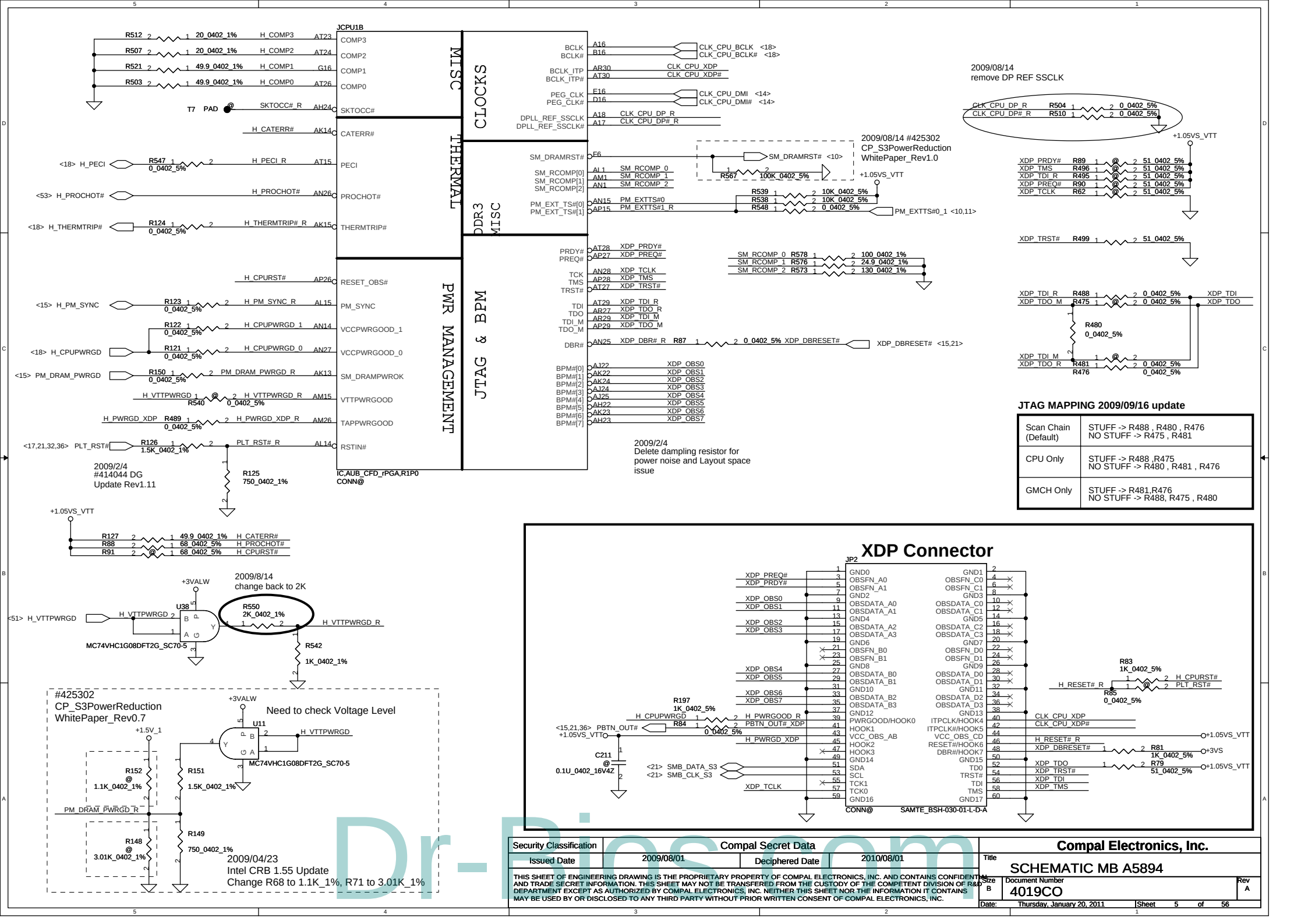
JCPU1B
MISC
CLOCKS
THERMAL
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT
IC,AUB_CFD_rPGA,R1P0
CONN@
2009/2/4
#414044 DG
Update Rev1.11
2009/2/4
Delete dampling resistor for
power noise and Layout space
issue
2009/08/14
remove DP REF SSCLK
2009/08/14 #425302
CP_S3PowerReduction
WhitePaper_Rev1.0
JTAG MAPPING 2009/09/16 update
Scan Chain (Default)
STUFF -> R488 , R480 , R476
NO STUFF -> R475 , R481
CPU Only
STUFF -> R488 ,R475
NO STUFF -> R480 , R481 , R476
GMCH Only
STUFF -> R481,R476
NO STUFF -> R488, R475 , R480
2009/8/14
change back to 2K
MC74VHC1G08DFT2G_SC70-5
#425302
CP_S3PowerReduction
WhitePaper_Rev0.7
Need to check Voltage Level
2009/04/23
Intel CRB 1.55 Update
Change R68 to 1.1K_1%, R71 to 3.01K_1%
XDP Connector
JP2
SAMTE_BSH-030-01-L-D-A
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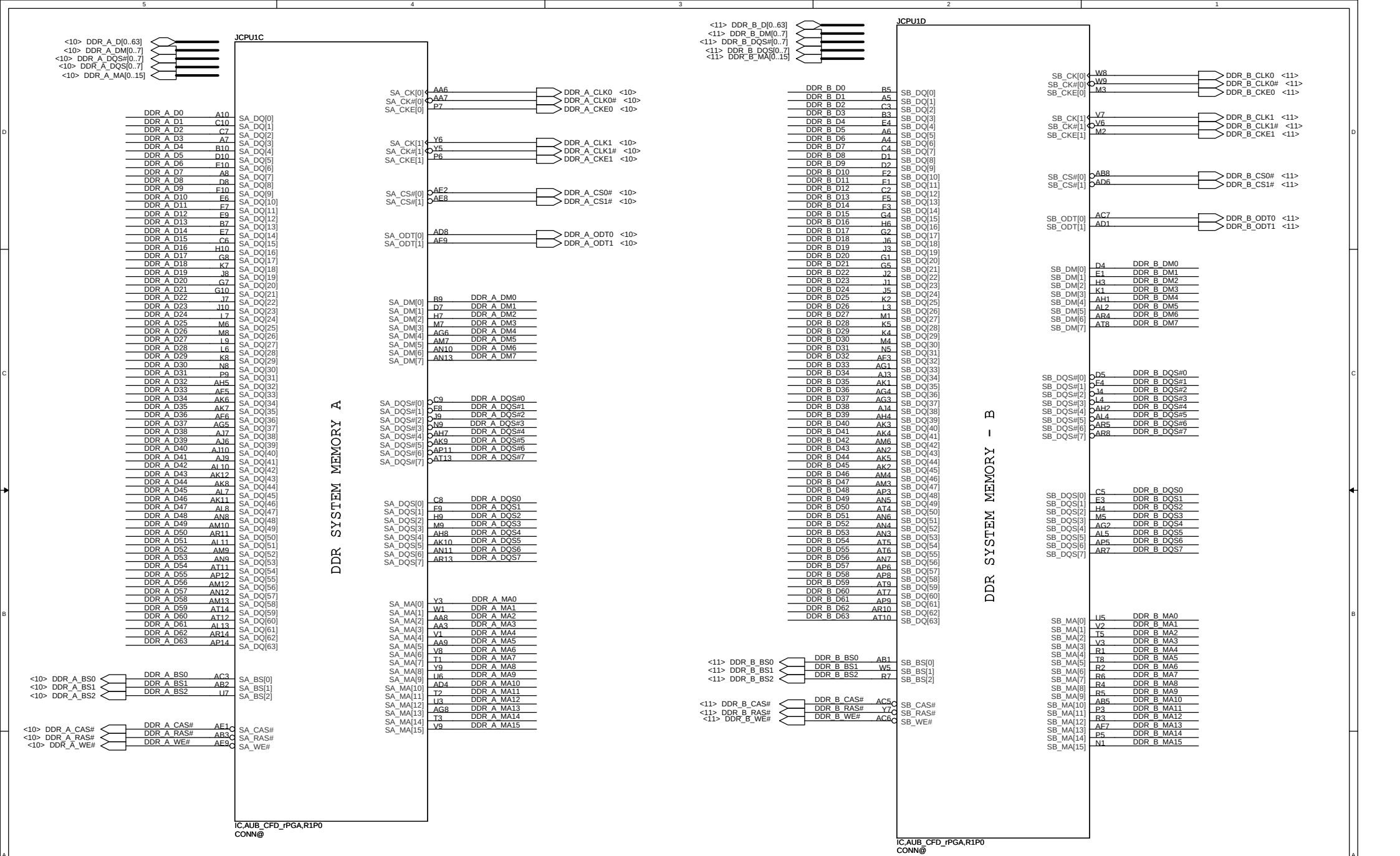

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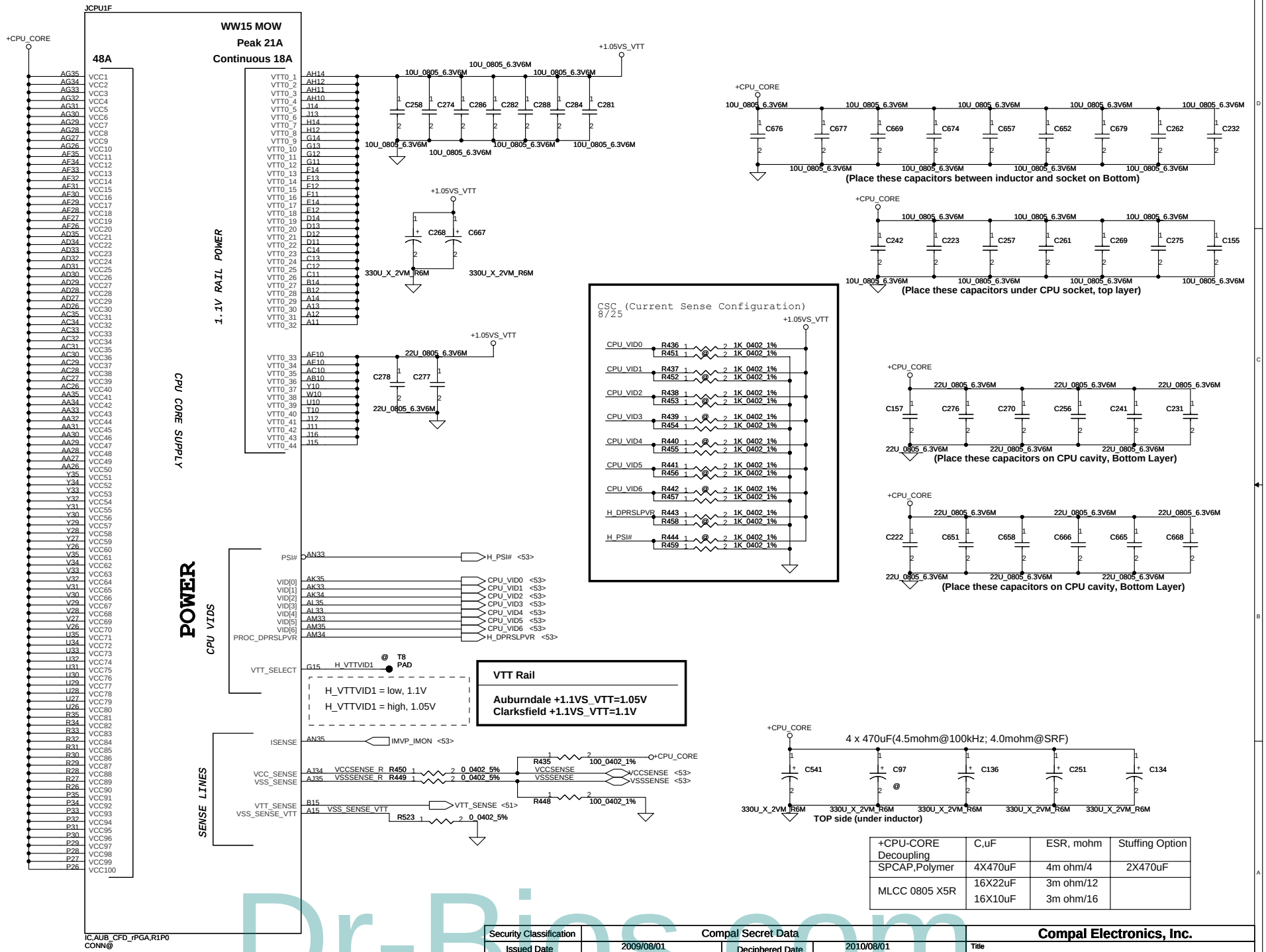

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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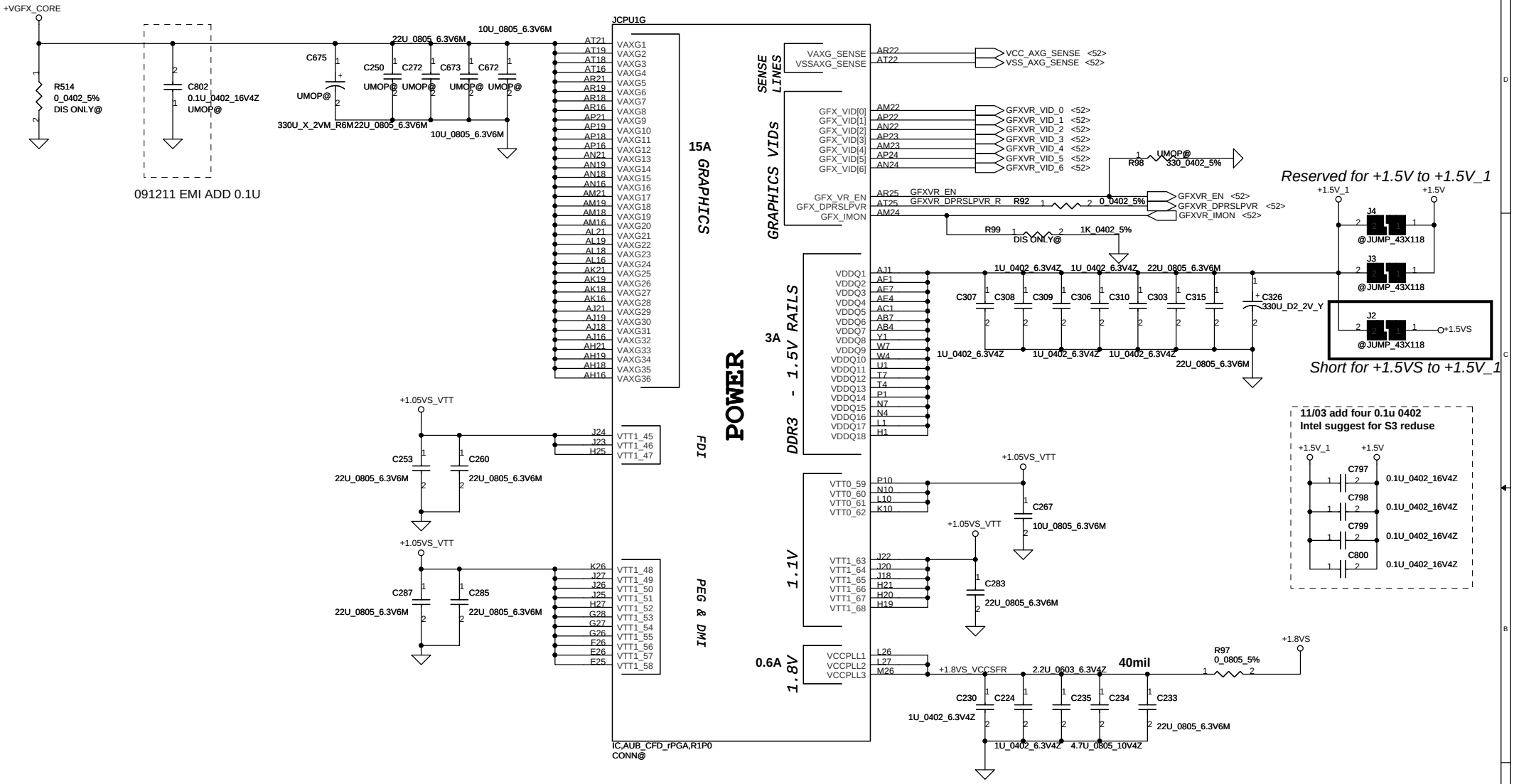

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DIMMA VREFDQ M1 Circuit

+1.5V

R222 1K_0402_1%

+DIMM_VREFDQA

20mil

R227 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V

R203 1K_0402_1%

+DIMM_VREFCA

20mil

R201 1K_0402_1%

<6> DDR_A_DQS#[0..7]
<6> DDR_A_D[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

+1.5V

R254 0_0402_5% @

R274 1K_0402_1%

<5> SM_DRAMRST#

Q17 BSS138LT1G_SOT23-3

DIMM_DRAMRST#

DIMM_DRAMRST# <11>

C422 0.047U_0402_16V7K

<18> RST_GATE

RST_GATE

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

C354 10U_0805_6.3V6M
C355 10U_0805_6.3V6M
C356 10U_0805_6.3V6M
C405 10U_0805_6.3V6M
C404 10U_0805_6.3V6M
C406 10U_0805_6.3V6M
C362 0.1U_0402_16V4Z
C363 0.1U_0402_16V4Z
C399 0.1U_0402_16V4Z
C400 0.1U_0402_16V4Z
C425 330U_2.5V_M_R15 @

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

C391 1U_0402_6.3V4Z
C388 1U_0402_6.3V4Z
C397 1U_0402_6.3V4Z
C396 1U_0402_6.3V4Z
C394 10U_0805_6.3V6M

+DIMM_VREFDQA

C401 0.1U_0402_16V4Z

C402 2.2U_0603_6.3V4Z

+1.5V

JDIMM1

	1	VREF_DQ	VSS1	2			
	3	VSS2	DQ4	4	DDR_A_D4		
DDR_A_D0	5	DQ0	DQ5	6	DDR_A_D5		
DDR_A_D1	7	DQ1	VSS3	8			
	9	VSS4	DQS#0	10	DDR_A_DQS#0		
DDR_A_DM0	11	DM0	DQS0	12	DDR_A_DQS0		
	13	VSS5	VSS6	14			
DDR_A_D2	15	DQ2	DQ6	16	DDR_A_D6		
DDR_A_D3	17	DQ3	DQ7	18	DDR_A_D7		
	19	VSS7	VSS8	20			
DDR_A_D8	21	DQ8	DQ12	22	DDR_A_D12		
DDR_A_D9	23	DQ9	DQ13	24	DDR_A_D13		
	25	VSS9	VSS10	26			
DDR_A_DQS#1	27	DQS#1	DM1	28	DDR_A_DM1		
DDR_A_DQS1	29	DQS1	RESET#	30	DIMM_DRAMRST#		
	31	VSS11	VSS12	32			
DDR_A_D10	33	DQ10	DQ14	34	DDR_A_D14		
DDR_A_D11	35	DQ11	DQ15	36	DDR_A_D15		
	37	VSS13	VSS14	38			
DDR_A_D16	39	DQ16	DQ20	40	DDR_A_D20		
DDR_A_D17	41	DQ17	DQ21	42	DDR_A_D21		
	43	VSS15	VSS16	44			
DDR_A_DQS#2	45	DQS#2	DM2	46	DDR_A_DM2		
DDR_A_DQS2	47	DQS2	VSS17	48			
	49	VSS18	DQ22	50	DDR_A_D22		
DDR_A_D18	51	DQ18	DQ23	52	DDR_A_D23		
DDR_A_D19	53	DQ19	VSS19	54			
	55	VSS20	DQ28	56	DDR_A_D28		
DDR_A_D24	57	DQ24	DQ29	58	DDR_A_D29		
DDR_A_D25	59	DQ25	VSS21	60			
	61	VSS22	DQS#3	62	DDR_A_DQS#3		
DDR_A_DM3	63	DM3	DQS3	64	DDR_A_DQS3		
	65	VSS23	VSS24	66			
DDR_A_D26	67	DQ26	DQ30	68	DDR_A_D30		
DDR_A_D27	69	DQ27	DQ31	70	DDR_A_D31		
	71	VSS25	VSS26	72			
<6> DDR_A_CKE0 DDR_A_CKE0	73	CKE0	CKE1	74	DDR_A_CKE1	DDR_A_CKE1 <6>	
	75	VDD1	VDD2	76			
	77	NC1	A15	78	DDR_A_MA15		
<6> DDR_A_BS2 DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14		
	81	VDD3	VDD4	82			
DDR_A_MA12	83	A12/BC#	A11	84	DDR_A_MA11		
DDR_A_MA9	85	A9	A7	86	DDR_A_MA7		
	87	VDD5	VDD6	88			
DDR_A_MA8	89	A8	A6	90	DDR_A_MA6		
DDR_A_MA5	91	A5	A4	92	DDR_A_MA4		
	93	VDD7	VDD8	94			
DDR_A_MA3	95	A3	A2	96	DDR_A_MA2		
DDR_A_MA1	97	A1	A0	98	DDR_A_MA0		
	99	VDD9	VDD10	100			
<6> DDR_A_CLK0 DDR_A_CLK0	101	CK0	CK1	102	DDR_A_CLK1	DDR_A_CLK1 <6>	
<6> DDR_A_CLK0# DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1#	DDR_A_CLK1# <6>	
	105	VDD11	VDD12	106			
DDR_A_MA10	107	A10/AP	BA1	108	DDR_A_BS1	DDR_A_BS1 <6>	
<6> DDR_A_BS0 DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS#	DDR_A_RAS# <6>	
	111	VDD13	VDD14	112			
<6> DDR_A_WE# DDR_A_WE#	113	WE#	S0#	114	DDR_A_CS0#	DDR_A_CS0# <6>	
<6> DDR_A_CAS# DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0	DDR_A_ODT0 <6>	
	117	VDD15	VDD16	118			
DDR_A_MA13	119	A13	ODT1	120	DDR_A_ODT1	DDR_A_ODT1 <6>	
<6> DDR_A_CS1# DDR_A_CS1#	121	S1#	NC2	122			
	123	VDD17	VDD18	124			
	125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA	R202 1 2 0_0402_5%	
	127	VSS27	VSS28	128			
DDR_A_D32	129	DQ32	DQ36	130	DDR_A_D36		
DDR_A_D33	131	DQ33	DQ37	132	DDR_A_D37		
	133	VSS29	VSS30	134			
DDR_A_DQS#4	135	DQS#4	DM4	136	DDR_A_DM4		
DDR_A_DQS4	137	DQS4	VSS31	138			
	139	VSS32	DQ38	140	DDR_A_D38		
DDR_A_D34	141	DQ34	DQ39	142	DDR_A_D39		
DDR_A_D35	143	DQ35	VSS33	144			
	145	VSS34	DQ44	146	DDR_A_D44		
DDR_A_D40	147	DQ40	DQ45	148	DDR_A_D45		
DDR_A_D41	149	DQ41	VSS35	150			
	151	VSS36	DQS#5	152	DDR_A_DQS#5		
DDR_A_DM5	153	DM5	DQS5	154	DDR_A_DQS5		
	155	VSS37	VSS38	156			
DDR_A_D42	157	DQ42	DQ46	158	DDR_A_D46		
DDR_A_D43	159	DQ43	DQ47	160	DDR_A_D47		
	161	VSS39	VSS40	162			
DDR_A_D48	163	DQ48	DQ52	164	DDR_A_D52		
DDR_A_D49	165	DQ49	DQ53	166	DDR_A_D53		
	167	VSS41	VSS42	168			
DDR_A_DQS#6	169	DQS#6	DM6	170	DDR_A_DM6		
DDR_A_DQS6	171	DQS6	VSS43	172			
	173	VSS44	DQ54	174	DDR_A_D54		
DDR_A_D50	175	DQ50	DQ55	176	DDR_A_D55		
DDR_A_D51	177	DQ51	VSS45	178			
	179	VSS46	DQ60	180	DDR_A_D60		
DDR_A_D56	181	DQ56	DQ61	182	DDR_A_D61		
DDR_A_D57	183	DQ57	VSS47	184			
	185	VSS48	DQS#7	186	DDR_A_DQS#7		
DDR_A_DM7	187	DM7	DQS7	188	DDR_A_DQS7		
	189	VSS49	VSS50	190			
DDR_A_D58	191	DQ58	DQ62	192	DDR_A_D62		
DDR_A_D59	193	DQ59	DQ63	194	DDR_A_D63		
	195	VSS51	VSS52	196			
	197	SA0	EVENT#	198	PM_EXTTS#0_1	PM_EXTTS#0_1 <5,11>	
	199	VDDSPD	SDA	200	D_CK_SDATA	D_CK_SDATA <11,12>	
	201	SA1	SCL	202	D_CK_SCLK	D_CK_SCLK <11,12>	
	203	VTT1	VTT2	204		+0.75VS	
	205	G1	G2	206			

FOX_AS0A626-U8RN-7F

+1.5V

+DIMM_VREFCA

20mil

C358 2.2U_0603_6.3V4Z

C361 0.1U_0402_16V4Z

+3VSO

R218 10K_0402_5%

C403 2.2U_0603_6.3V4Z

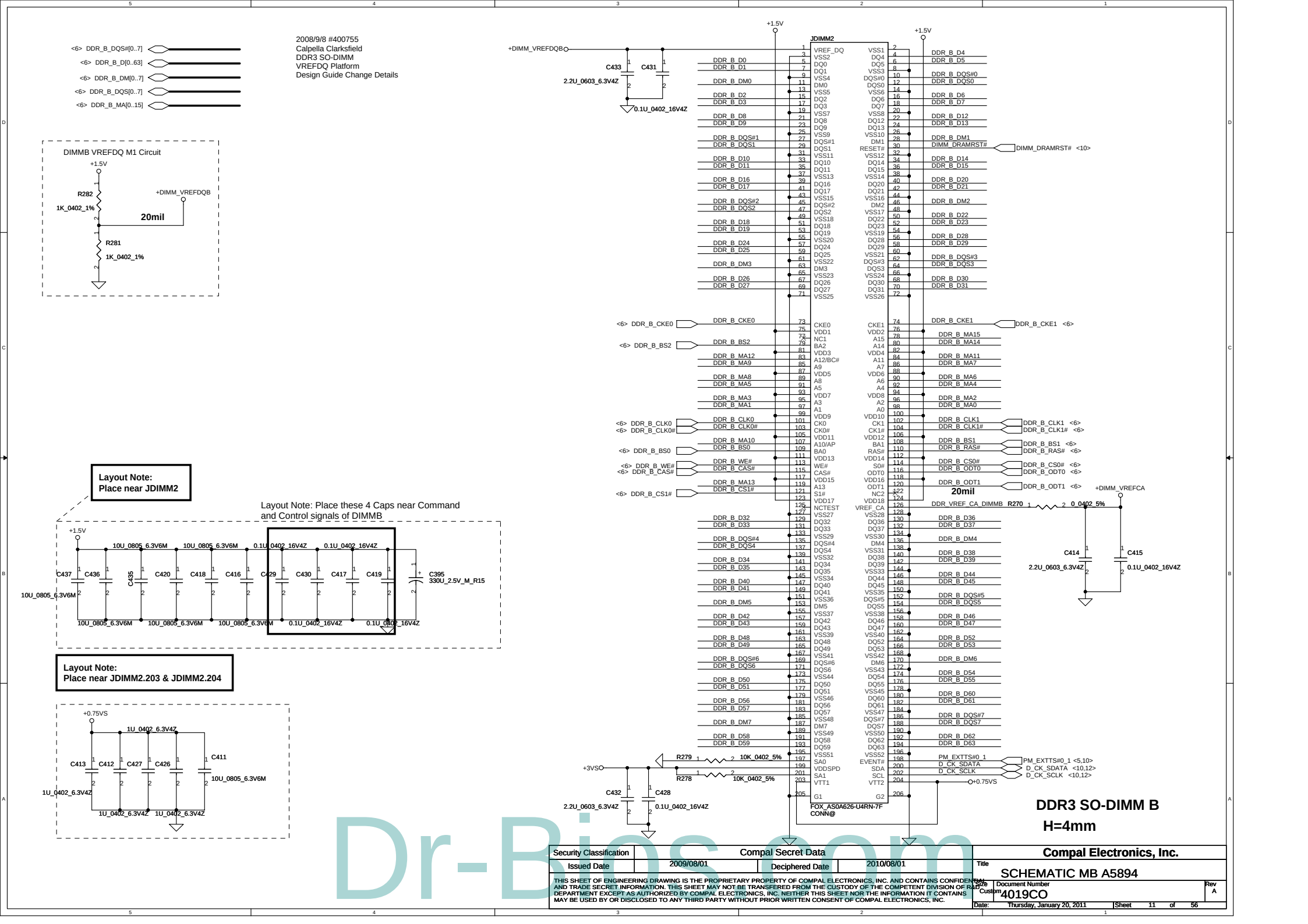
C398 0.1U_0402_16V4Z

R217 10K_0402_5%

DDR3 SO-DIMM A
H=8mm

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.			
Title: SCHEMATIC MB A5894			
Size: Custom	Document Number: 4019CO		Rev: A
Date: Thursday, January 20, 2011	Sheet 10 of 56		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<6> DDR_B_D[0..63]
<6> DDR_B_DM[0..7]
<6> DDR_B_DQS[0..7]
<6> DDR_B_MA[0..15]
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details
DIMMB VREFDQ M1 Circuit
+1.5V
R282
1K_0402_1%
+DIMM_VREFDQB
20mil
R281
1K_0402_1%
JDIMM2
+1.5V
+DIMM_VREFDQB
C433
C431
2.2U_0603_6.3V4Z
0.1U_0402_16V4Z
DDR_B_D0
DDR_B_D1
DDR_B_DM0
DDR_B_D2
DDR_B_D3
DDR_B_D8
DDR_B_D9
DDR_B_DQS#1
DDR_B_DQS1
DDR_B_D10
DDR_B_D11
DDR_B_D16
DDR_B_D17
DDR_B_DQS#2
DDR_B_DQS2
DDR_B_D18
DDR_B_D19
DDR_B_D24
DDR_B_D25
DDR_B_DM3
DDR_B_D26
DDR_B_D27
VREF_DQ
VSS1
VSS2
DQ0
DQ1
VSS4
DM0
VSS5
DQ2
DQ3
VSS7
DQ8
DQ9
VSS9
DQS#1
DQS1
VSS11
DQ10
DQ11
VSS13
DQ16
DQ17
VSS15
DQS#2
DQS2
VSS18
DQ18
DQ19
VSS20
DQ24
DQ25
VSS22
DM3
VSS23
DQ26
DQ27
VSS25
DQ4
DQ5
VSS3
DQS#0
DQS0
VSS6
DQ6
DQ7
VSS8
DQ12
DQ13
VSS10
DM1
RESET#
VSS12
DQ14
DQ15
VSS14
DQ20
DQ21
VSS16
DM2
VSS17
DQ22
DQ23
VSS19
DQ28
DQ29
VSS21
DQS#3
DQS3
VSS24
DQ30
DQ31
VSS26
DDR_B_D4
DDR_B_D5
DDR_B_DQS#0
DDR_B_DQS0
DDR_B_D6
DDR_B_D7
DDR_B_D12
DDR_B_D13
DDR_B_DM1
DIMM_DRAMRST#
DDR_B_D14
DDR_B_D15
DDR_B_D20
DDR_B_D21
DDR_B_DM2
DDR_B_D22
DDR_B_D23
DDR_B_D28
DDR_B_D29
DDR_B_DQS#3
DDR_B_DQS3
DDR_B_D30
DDR_B_D31
DIMM_DRAMRST# <10>
<6> DDR_B_CKE0
DDR_B_CKE0
<6> DDR_B_BS2
DDR_B_BS2
DDR_B_MA12
DDR_B_MA9
DDR_B_MA8
DDR_B_MA5
DDR_B_MA3
DDR_B_MA1
<6> DDR_B_CLK0
<6> DDR_B_CLK0#
DDR_B_MA10
<6> DDR_B_BS0
DDR_B_BS0
DDR_B_WE#
<6> DDR_B_WE#
<6> DDR_B_CAS#
DDR_B_CAS#
DDR_B_MA13
DDR_B_CS1#
<6> DDR_B_CS1#
CKE0
VDD1
NC1
BA2
VDD3
A12/BC#
A9
VDD5
A8
A5
VDD7
A3
A1
VDD9
CK0
CK0#
VDD11
A10/AP
BA0
VDD13
WE#
CAS#
VDD15
A13
S1#
VDD17
NCTEST
VSS27
DQ32
DQ33
VSS29
DQS#4
DQS4
VSS32
DQ34
DQ35
VSS34
DQ40
DQ41
VSS36
DM5
VSS37
DQ42
DQ43
VSS39
DQ48
DQ49
VSS41
DQS#6
DQS6
VSS44
DQ50
DQ51
VSS46
DQ56
DQ57
VSS48
DM7
VSS49
DQ58
DQ59
VSS51
SA0
VDDSPD
SA1
VTT1
G1
CKE1
VDD2
A15
A14
VDD4
A11
A7
VDD6
A6
A4
VDD8
A2
A0
VDD10
CK1
CK1#
VDD12
BA1
RAS#
VDD14
S0#
ODT0
VDD16
ODT1
NC2
VDD18
VREF_CA
VSS28
DQ36
DQ37
VSS30
DM4
VSS31
DQ38
DQ39
VSS33
DQ44
DQ45
VSS35
DQS#5
DQS5
VSS38
DQ46
DQ47
VSS40
DQ52
DQ53
VSS42
DM6
VSS43
DQ54
DQ55
VSS45
DQ60
DQ61
VSS47
DQS#7
DQS7
VSS50
DQ62
DQ63
VSS52
EVENT#
SDA
SCL
VTT2
G2
DDR_B_CKE1
DDR_B_MA15
DDR_B_MA14
DDR_B_MA11
DDR_B_MA7
DDR_B_MA6
DDR_B_MA4
DDR_B_MA2
DDR_B_MA0
DDR_B_CLK1
DDR_B_CLK1#
DDR_B_BS1
DDR_B_RAS#
DDR_B_CS0#
DDR_B_ODT0
DDR_B_ODT1
20mil
DDR_B_CKE1 <6>
DDR_B_CLK1 <6>
DDR_B_CLK1# <6>
DDR_B_BS1 <6>
DDR_B_RAS# <6>
DDR_B_CS0# <6>
DDR_B_ODT0 <6>
DDR_B_ODT1 <6>
+DIMM_VREFCA
DDR_VREF_CA_DIMMB
R270
0_0402_5%
C414
C415
2.2U_0603_6.3V4Z
0.1U_0402_16V4Z
DDR_B_D32
DDR_B_D33
DDR_B_DQS#4
DDR_B_DQS4
DDR_B_D34
DDR_B_D35
DDR_B_D40
DDR_B_D41
DDR_B_DM5
DDR_B_D42
DDR_B_D43
DDR_B_D48
DDR_B_D49
DDR_B_DQS#6
DDR_B_DQS6
DDR_B_D50
DDR_B_D51
DDR_B_D56
DDR_B_D57
DDR_B_DM7
DDR_B_D58
DDR_B_D59
DDR_B_D36
DDR_B_D37
DDR_B_DM4
DDR_B_D38
DDR_B_D39
DDR_B_D44
DDR_B_D45
DDR_B_DQS#5
DDR_B_DQS5
DDR_B_D46
DDR_B_D47
DDR_B_D52
DDR_B_D53
DDR_B_DM6
DDR_B_D54
DDR_B_D55
DDR_B_D60
DDR_B_D61
DDR_B_DQS#7
DDR_B_DQS7
DDR_B_D62
DDR_B_D63
PM_EXTTS#0_1
D_CK_SDATA
D_CK_SCLK
PM_EXTTS#0_1 <5,10>
D_CK_SDATA <10,12>
D_CK_SCLK <10,12>
+0.75VS
+3VSO
R279
10K_0402_5%
R278
10K_0402_5%
C432
C428
2.2U_0603_6.3V4Z
0.1U_0402_16V4Z
FOX_AS0A626-U4RN-7F
CONN@
Layout Note:
Place near JDIMM2
Layout Note: Place these 4 Caps near Command
and Control signals of DIMMB
+1.5V
10U_0805_6.3V6M
0.1U_0402_16V4Z
C437
C436
C435
C420
C418
C416
C429
C430
C417
C419
C395
330U_2.5V_M_R15
Layout Note:
Place near JDIMM2.203 & JDIMM2.204
+0.75VS
1U_0402_6.3V4Z
C413
C412
C427
C426
C411
10U_0805_6.3V6M
DDR3 SO-DIMM B
H=4mm
Security Classification
Compal Secret Data
Issued Date
2009/08/01
Deciphered Date
2010/08/01
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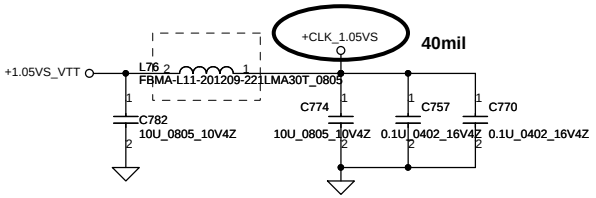
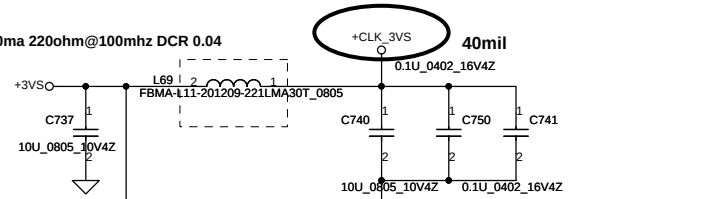
Title
SCHEMATIC MB A5894
Size
Custom
Document Number
4019CO
Rev
A
Date:
Thursday, January 20, 2011
Sheet
11
of
56

SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



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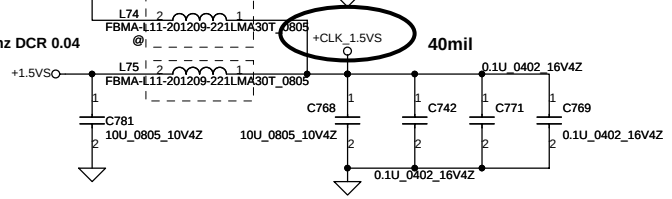
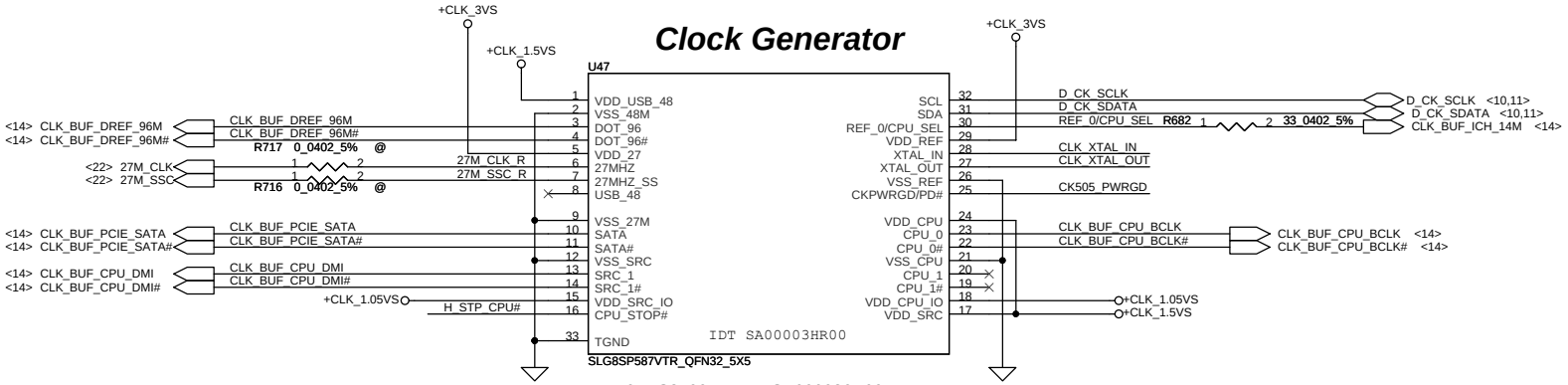


Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00

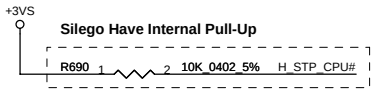
SILEGO: SLG8SP587V(WF), SA00002XY10

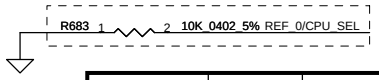
Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00

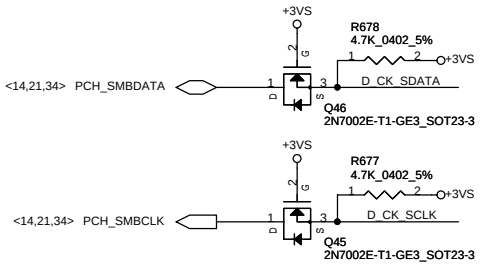
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

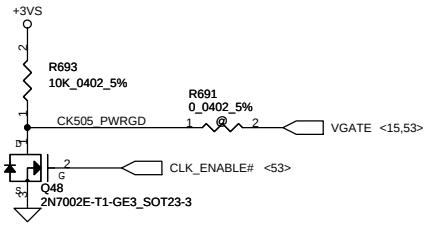
IDT 9LVS3199AKLFT NC

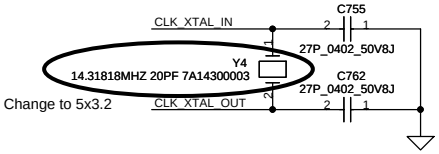




PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

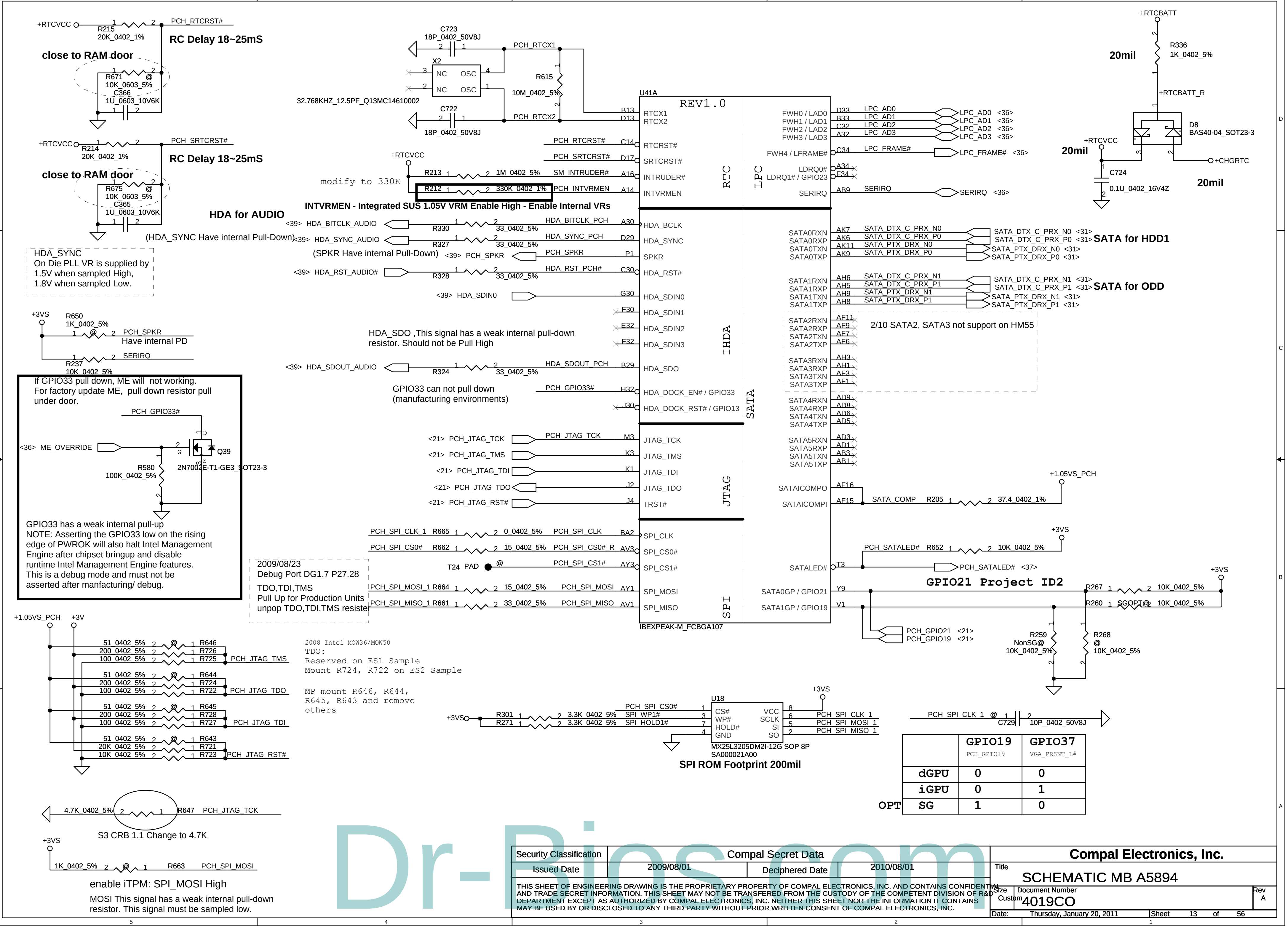






Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Title	SCHEMATIC MB A5894		
Size: Custom	Document Number: 4019CO		Rev: A
Date: Thursday, January 20, 2011	Sheet 12 of 56		



	GPIO19 (PCH_GPIO19)	GPIO37 (VGA_PRSNT_L#)
dGPU	0	0
iGPU	0	1
OPT SG	1	0

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: SCHEMATIC MB A5894

Size: Custom — Document Number: 4019CO — Rev: A

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

U41B REV1.0

For PCIE LAN

<32> PCIE_DTX_C_PRX_N1 — C335 0.1U_0402_16V7K — PCIE_PTX_DRX_N1 BF29 — PERN1
<32> PCIE_DTX_C_PRX_P1 — C339 0.1U_0402_16V7K — PCIE_PTX_DRX_P1 BH29 — PERP1
<32> PCIE_PTX_C_DRX_N1 — PCIE_DTX_C_PRX_N1 BG30 — PETN1
<32> PCIE_PTX_C_DRX_P1 — PCIE_DTX_C_PRX_P1 BJ30 — PETP1

For Wireless LAN

<34> PCIE_DTX_C_PRX_N2 — C332 0.1U_0402_16V7K — PCIE_PTX_DRX_N2 BC30 — PERN2
<34> PCIE_DTX_C_PRX_P2 — C334 0.1U_0402_16V7K — PCIE_PTX_DRX_P2 BD30 — PERP2
<34> PCIE_PTX_C_DRX_N2 — PCIE_DTX_C_PRX_N2 AW30 — PETN2
<34> PCIE_PTX_C_DRX_P2 — PCIE_DTX_C_PRX_P2 BA30 — PETP2

AU30 PERN3 / AT30 PERP3 / AU32 PETN3 / AV32 PETP3

BA32 PERN4 / BB32 PERP4 / BD32 PETN4 / BE32 PETP4

For Mini2

2009/08/25: remove PCIE5

BE33 PERN5 / BH33 PERP5 / BG32 PETN5 / BJ32 PETP5

BA34 PERN6 / AW34 PERP6 / BC34 PETN6 / BD34 PETP6

2/10 PCIE7, PCIE8 not support on HM55

AT34 PERN7 / AU34 PERP7 / AU36 PETN7 / AV36 PETP7

BG34 PERN8 / BJ34 PERP8 / BG36 PETN8 / BJ36 PETP8

PCI-E* Controller Link

SMBus

SMBALERT# / GPIO11 B9 — EC_LID_OUT# — EC_LID_OUT# <36>
SMBCLK H14 — PCH_SMBCLK — PCH_SMBCLK <12,21,34>
SMBDATA C8 — PCH_SMBDATA — PCH_SMBDATA <12,21,34>
SML0ALERT# / GPIO60 J14 — PCH_GPIO60
SML0CLK C6
SML0DATA G8
SML1ALERT# / GPIO74 M14 — PCH_GPIO74
SML1CLK / GPIO58 E10 — PCH_SML1CLK
SML1DATA / GPIO75 G12 — PCH_SML1DAT

CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

+3V — R636 10K_0402_5%

DGPU_PWR_EN <18,21,38,42>

R275 Change form 10K to 0 ohm 20100629

R275 0_0402_5% DIS@

PEG_A_CLKRQ# / GPIO47 H1 — PEG_CLKREQ# R — PEG_CLKREQ# <22>

Q18 DIS@

R247 @ 2.2K_0402_5%
R276 @ 2.2K_0402_5%

2N7002E-T1-GE3_SOT23-3

PEG

CLKOUT_PEG_A_N AD43 — CLK_PEG_VGA# <22>
CLKOUT_PEG_A_P AD45 — CLK_PEG_VGA <22>
CLKOUT_DMI_N AN4 — CLK_CPU_DMI# <5>
CLKOUT_DMI_P AN2 — CLK_CPU_DMI <5>

CLKOUT_DP_N / CLKOUT_BCLK1_N AT1
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3

From CLK BUFFER

For PCIE LAN

<32> CLK_PCIE_LAN# — AK48 — CLKOUT_PCIE0N
<32> CLK_PCIE_LAN — AK47 — CLKOUT_PCIE0P
<32> LAN_CLKREQ# — R258 0_0402_5% — PCH_GPIO73 P9 — PCIECLKRQ0# / GPIO73

For Wireless LAN

<34> CLK_PCIE_MINI1# — AM43 — CLKOUT_PCIE1N
<34> CLK_PCIE_MINI1 — AM45 — CLKOUT_PCIE1P
<34> MINI1_CLKREQ# — R266 0_0402_5% — PCH_GPIO18 U4 — PCIECLKRQ1# / GPIO18
<21> PCH_GPIO18

AM47 CLKOUT_PCIE2N / AM48 CLKOUT_PCIE2P

<21> PCH_GPIO20 — PCH_GPIO20 N4 — PCIECLKRQ2# / GPIO20

AH42 CLKOUT_PCIE3N / AH41 CLKOUT_PCIE3P

PCH_GPIO25 A8 — PCIECLKRQ3# / GPIO25

2009/08/25: Change back to +3V remove mini2

+3V — R241 10K_0402_5% — MINI2_CLKREQ# 1

2009/08/25: remove mini2 clk

AM51 CLKOUT_PCIE4N / AM53 CLKOUT_PCIE4P

MINI2_CLKREQ# 1 — M9 — PCIECLKRQ4# / GPIO26

AJ50 CLKOUT_PCIE5N / AJ52 CLKOUT_PCIE5P

PCH_GPIO44 H6 — PCIECLKRQ5# / GPIO44

+3VS — 10K_0402_5% R265 MINI1_CLKREQ# — 10K_0402_5% R649 PCH_GPIO20

AK53 CLKOUT_PEG_B_N / AK51 CLKOUT_PEG_B_P

PCH_GPIO56 P13 — PEG_B_CLKRQ# / GPIO56

Clock Flex

REFCLK14IN P41 — CLK_BUF_ICH_14M <12>
R163 10_0402_5% C319 10P_0402_50V8J
1109 RF request

CLKIN_PCILOOPBACK J42 — CLK_PCI_FB <17>

CLKIN_DMI_N AW24 — CLK_BUF_CPU_DMI# <12>
CLKIN_DMI_P BA24 — CLK_BUF_CPU_DMI <12>
CLKIN_BCLK_N AP3 — CLK_BUF_CPU_BCLK# <12>
CLKIN_BCLK_P AP1 — CLK_BUF_CPU_BCLK <12>
CLKIN_DOT_96N F18 — CLK_BUF_DREF_96M# <12>
CLKIN_DOT_96P F18 — CLK_BUF_DREF_96M <12>
CLKIN_SATA_N / CKSSCD_N AH13 — CLK_BUF_PCIE_SATA# <12>
CLKIN_SATA_P / CKSSCD_P AH12 — CLK_BUF_PCIE_SATA <12>

XTAL25_IN AH51 — XTAL25_IN
XTAL25_OUT AH53 — XTAL25_OUT

XCLK_RCOMP AF38 — XCLK_RCOMP R170 90.9_0402_1% — +1.05VS_PCH

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

R563 DIS ONLY@ 0_0402_5%
C693 UMOP@ 27P_0402_50V8J
R564 1M_0402_5% UMOP@
Y2 25MHZ_20PF_7A25000012 UMOP@
C694 27P_0402_50V8J UMOP@

Change to 5x3.2

CLKOUTFLEX0 / GPIO64 T45
CLKOUTFLEX1 / GPIO65 P43 — PROJECT_ID1
CLKOUTFLEX2 / GPIO66 T42 — PROJECT_ID0
CLKOUTFLEX3 / GPIO67 N50

Project Structure ID

+3VS
R156 10K_0402_5% OPT@
R144 10K_0402_5% NonOPT@
R157 10K_0402_5% @
R167 10K_0402_5%

IBEXPEAK-M_FCBGA107

Schematic_Checklist_Rev1.6

GPIO18	Main (core) power well (+V3.3S)	Muxed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)
GPIO25	Resume (Sus) well (+V3.3A)	Muxed with PCIECLKREQ3# If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

+3V

10K_0402_5% R623 EC_LID_OUT#
2.2K_0402_5% R602 PCH_SMBCLK
2.2K_0402_5% R626 PCH_SMBDATA
10K_0402_5% R208 PCH_GPIO60
2.2K_0402_5% R639 PCH_SML1CLK
2.2K_0402_5% R249 PCH_SML1DAT
10K_0402_5% R207 PCH_GPIO74
10K_0402_5% R244 PCH_GPIO44
10K_0402_5% R206 PCH_GPIO56
10K_0402_5% R257 PCH_GPIO73

+3V — 9/1: Change to +3VS — 2009/08/13: Change back to +3V
10K_0402_5% R624 PCH_GPIO25

Project Structure

	GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
	0	0	0	NEW70
	0	0	1	NEW80
	0	1	0	NEW90
*Discrete	1	0	0	NEW71/91
*Optimus	1	1	0	NEW71/91

+3VS — PCH_SML1CLK 6 — Q19A 2N7002DWH_SOT363-6 — 1 EC_SMB_CK2 — EC_SMB_CK2 <22,36>

Pull high +3VS at KB926 side

+3VS — PCH_SML1DAT 3 — Q19B 2N7002DWH_SOT363-6 — 4 EC_SMB_DA2 — EC_SMB_DA2 <22,36>

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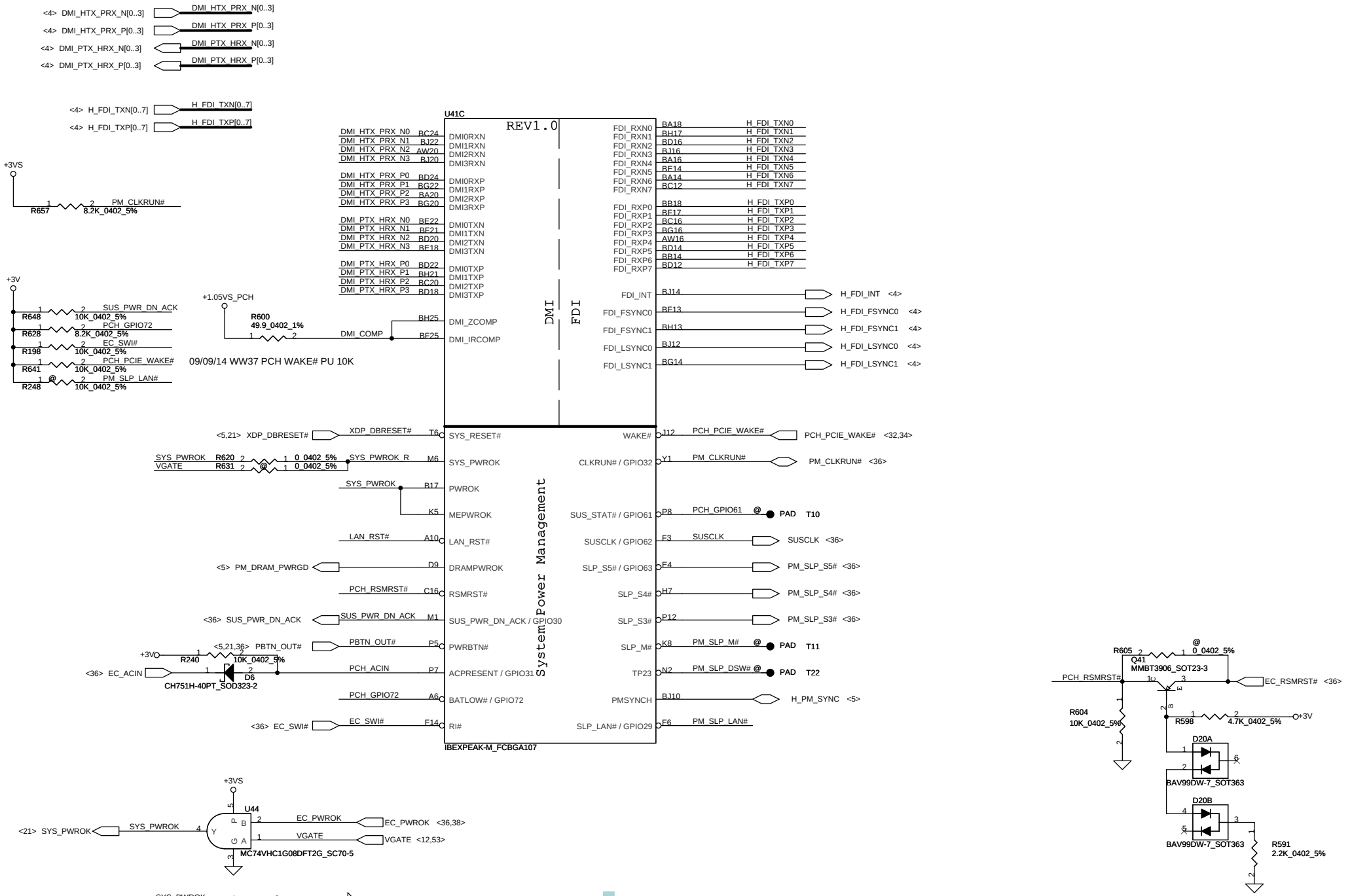

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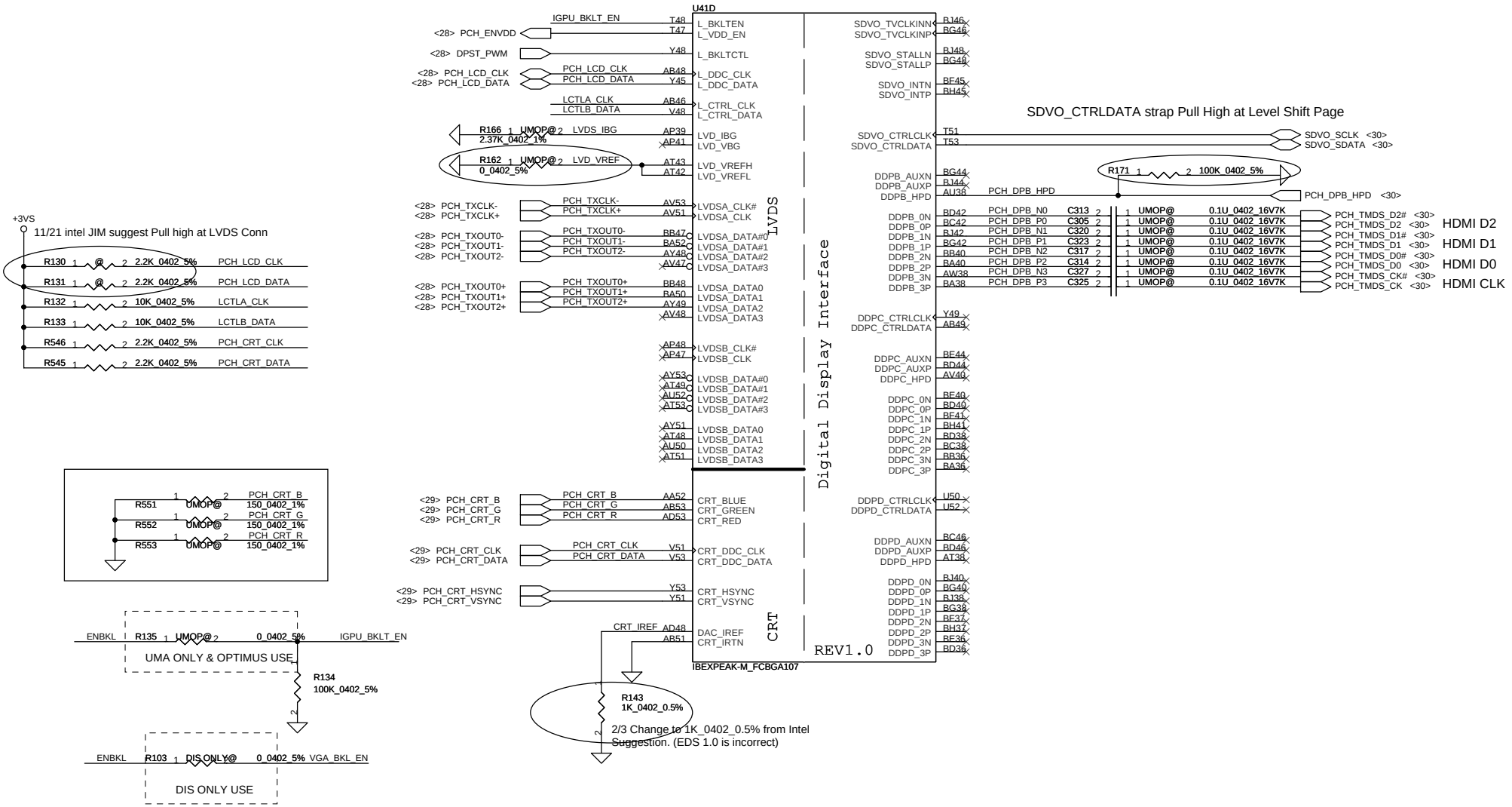

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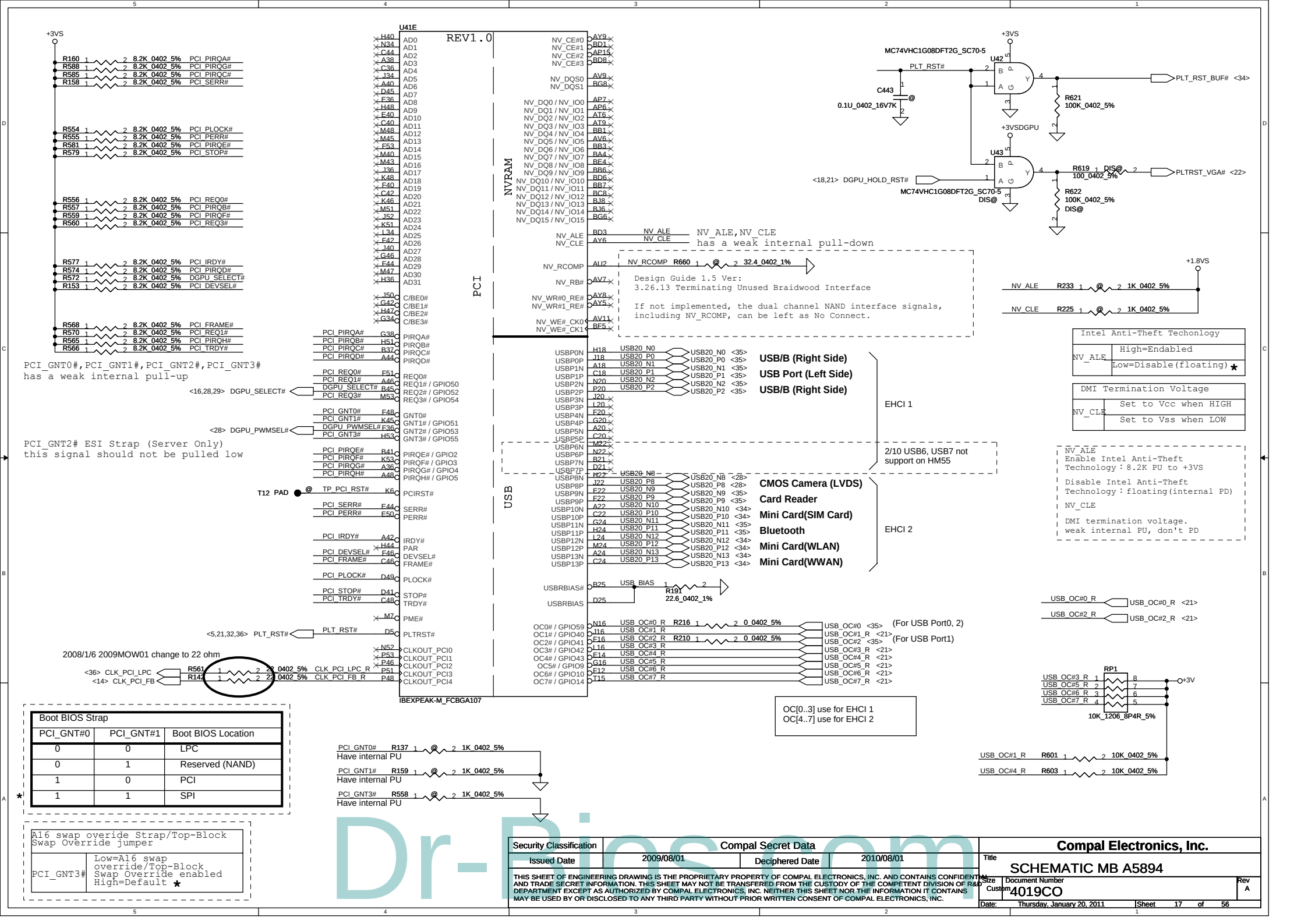

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

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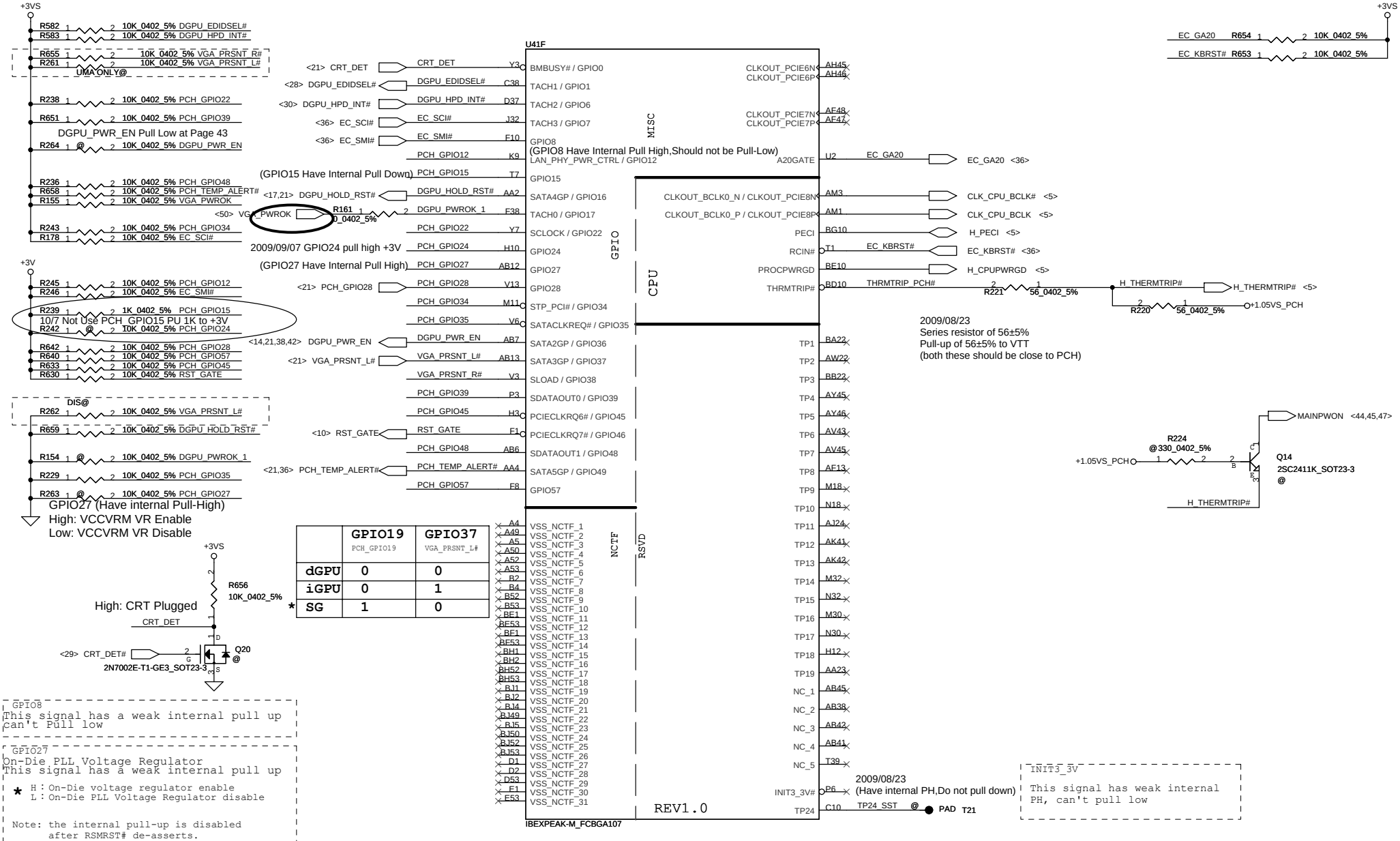

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO8
This signal has a weak internal pull up can't Pull low

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts.
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

GPIO15
* L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

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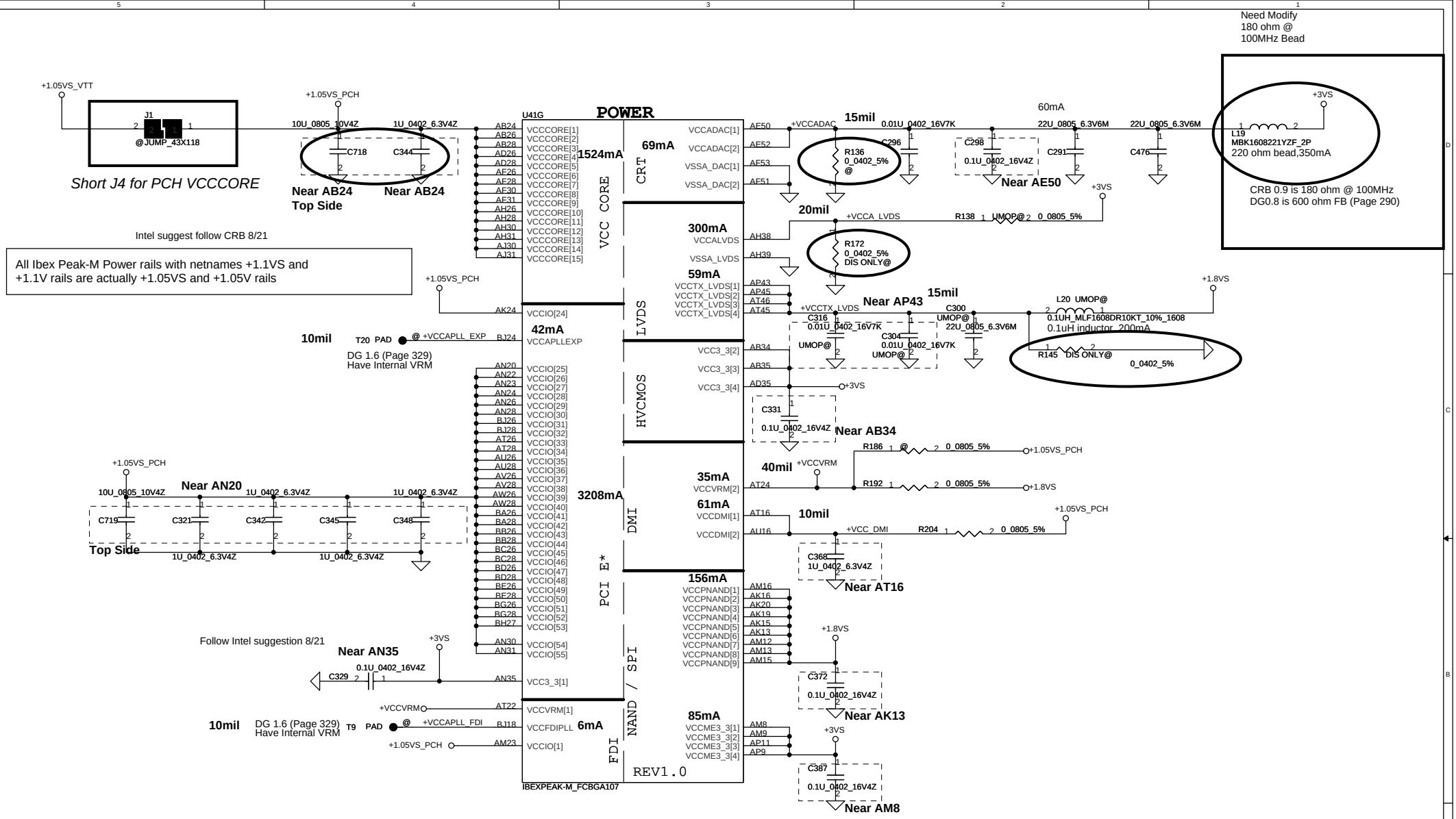

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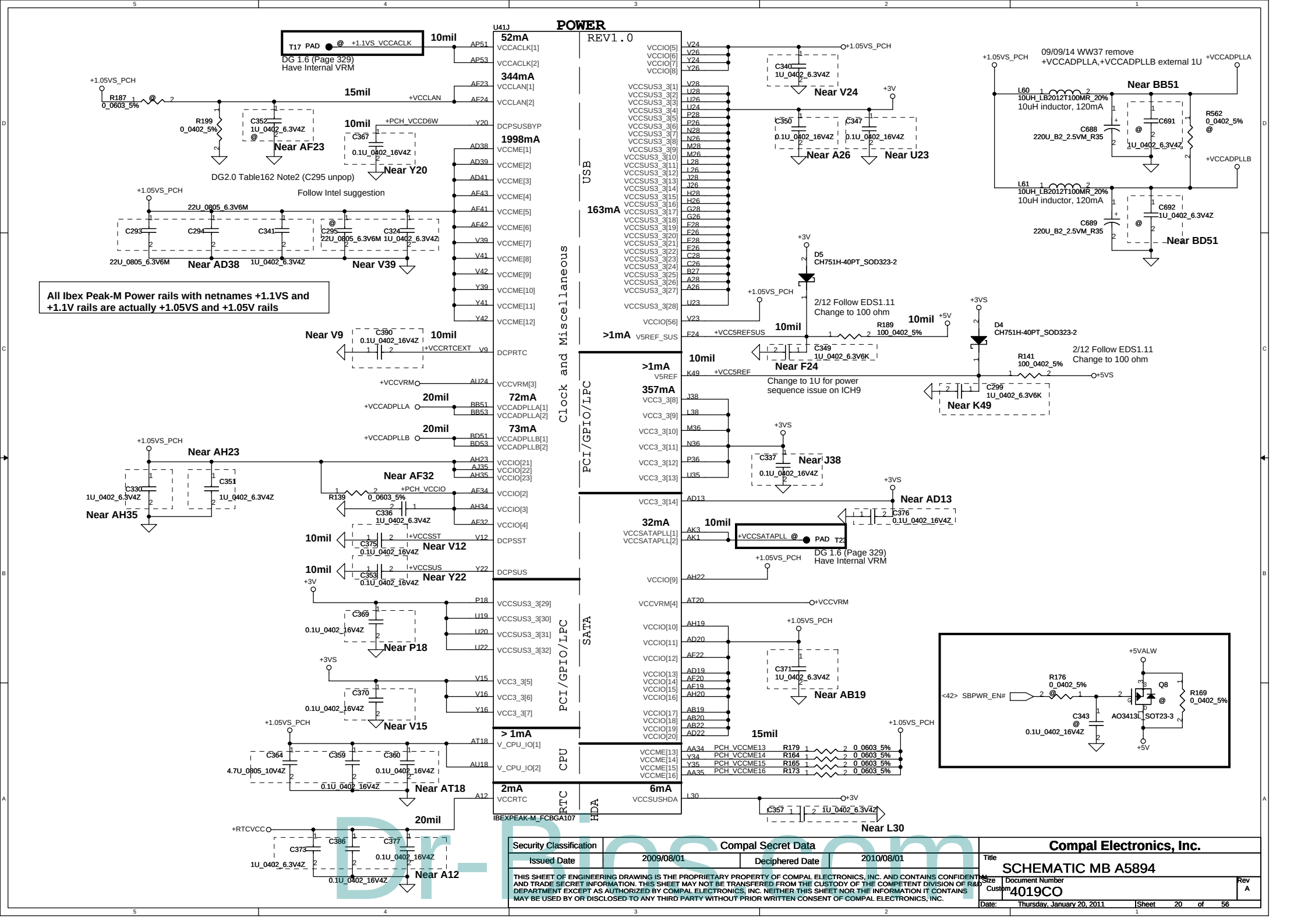
POWER
REV1.0
U41J
IBEXPEAK-M_FCBGA107
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails
DG 1.6 (Page 329) Have Internal VRM
DG2.0 Table162 Note2 (C295 unpop)
Follow Intel suggestion
09/09/14 WW37 remove +VCCADPLLA,+VCCADPLLB external 1U
10uH inductor, 120mA
2/12 Follow EDS1.11 Change to 100 ohm
Change to 1U for power sequence issue on ICH9
Near BB51
Near BD51
Near V24
Near A26
Near U23
Near V9
Near V39
Near AD38
Near AH23
Near AH35
Near AF23
Near AF32
Near V12
Near Y22
Near Y20
Near P18
Near V15
Near AT18
Near A12
Near F24
Near K49
Near J38
Near AD13
Near AB19
Near L30
52mA
344mA
1998mA
163mA
>1mA
357mA
72mA
73mA
32mA
> 1mA
2mA
6mA
15mil
10mil
20mil
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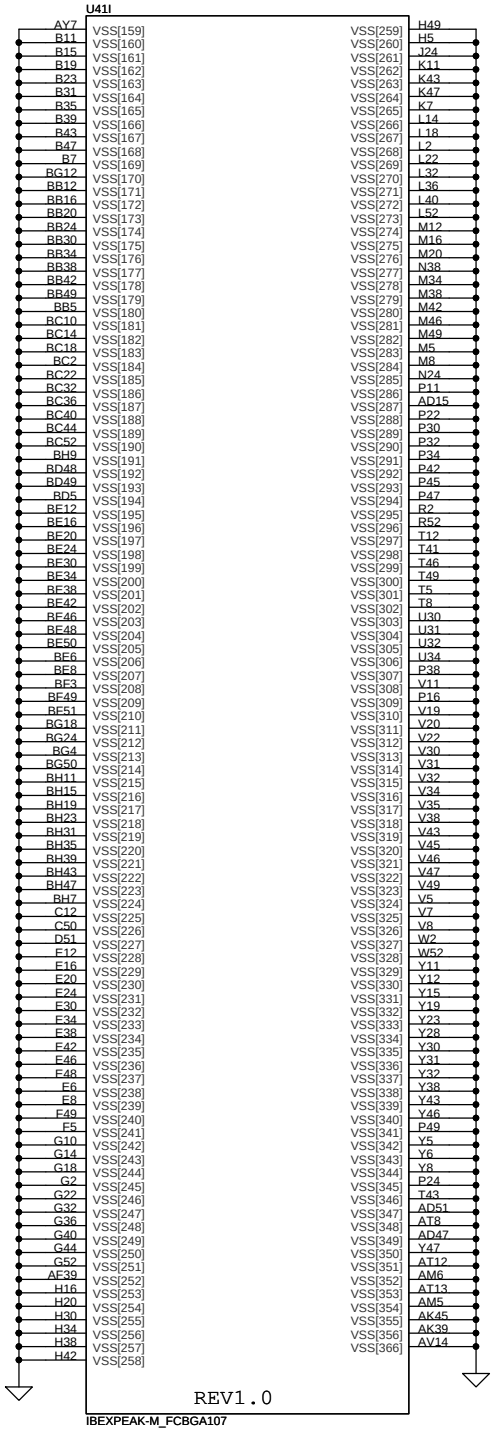
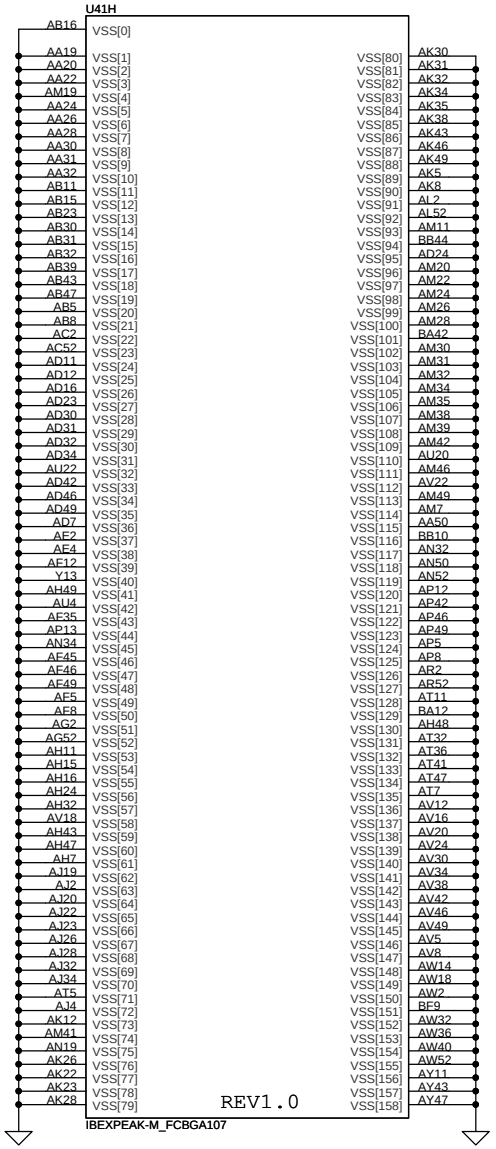
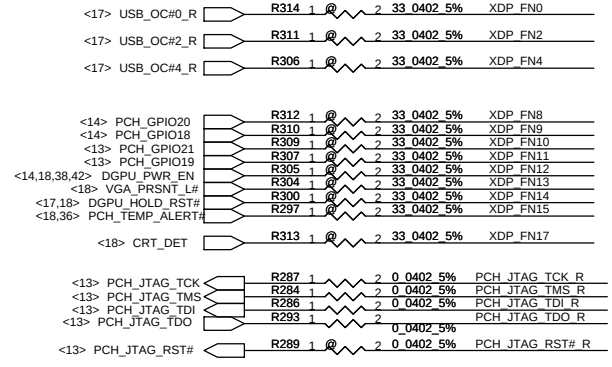
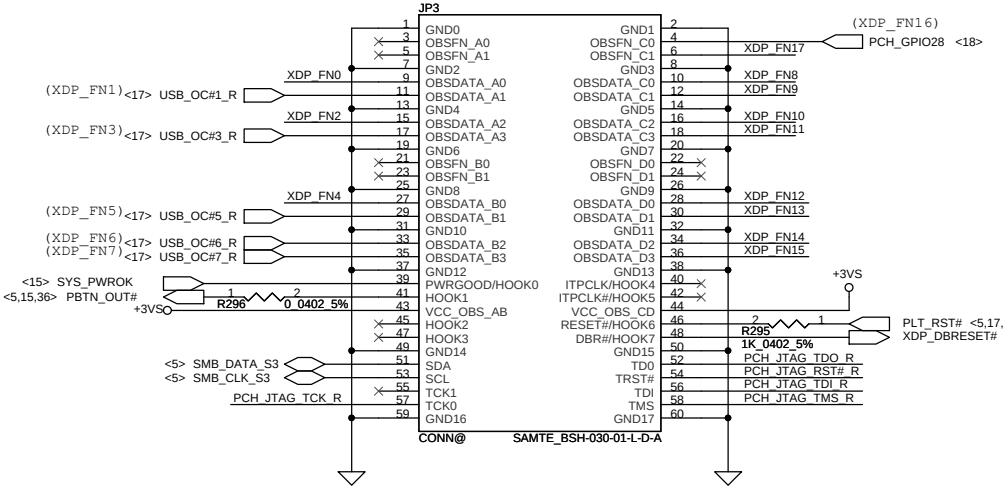
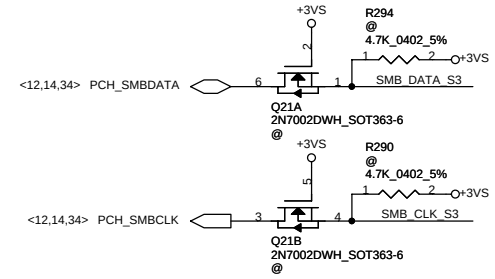
PCH XDP Port











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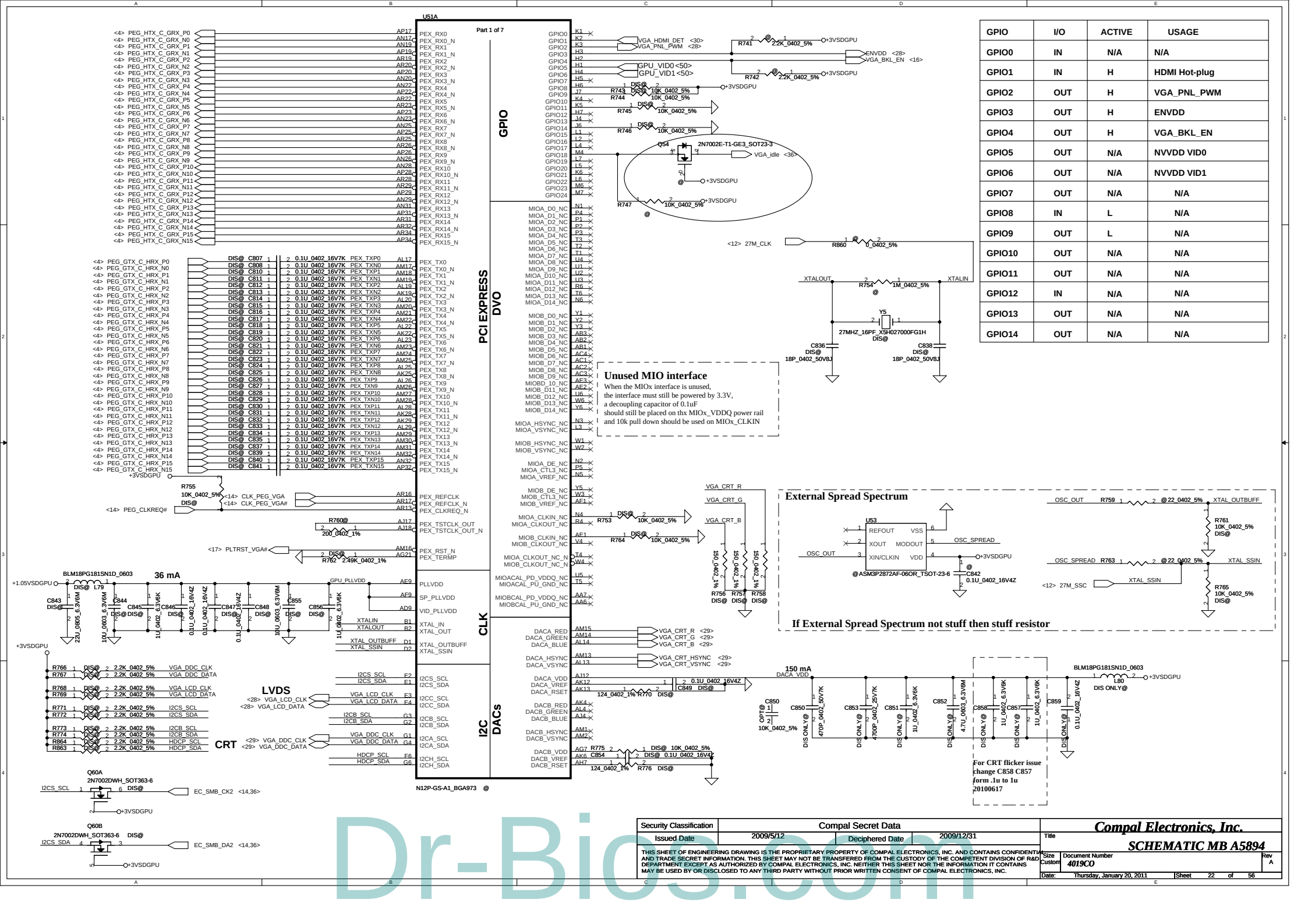

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

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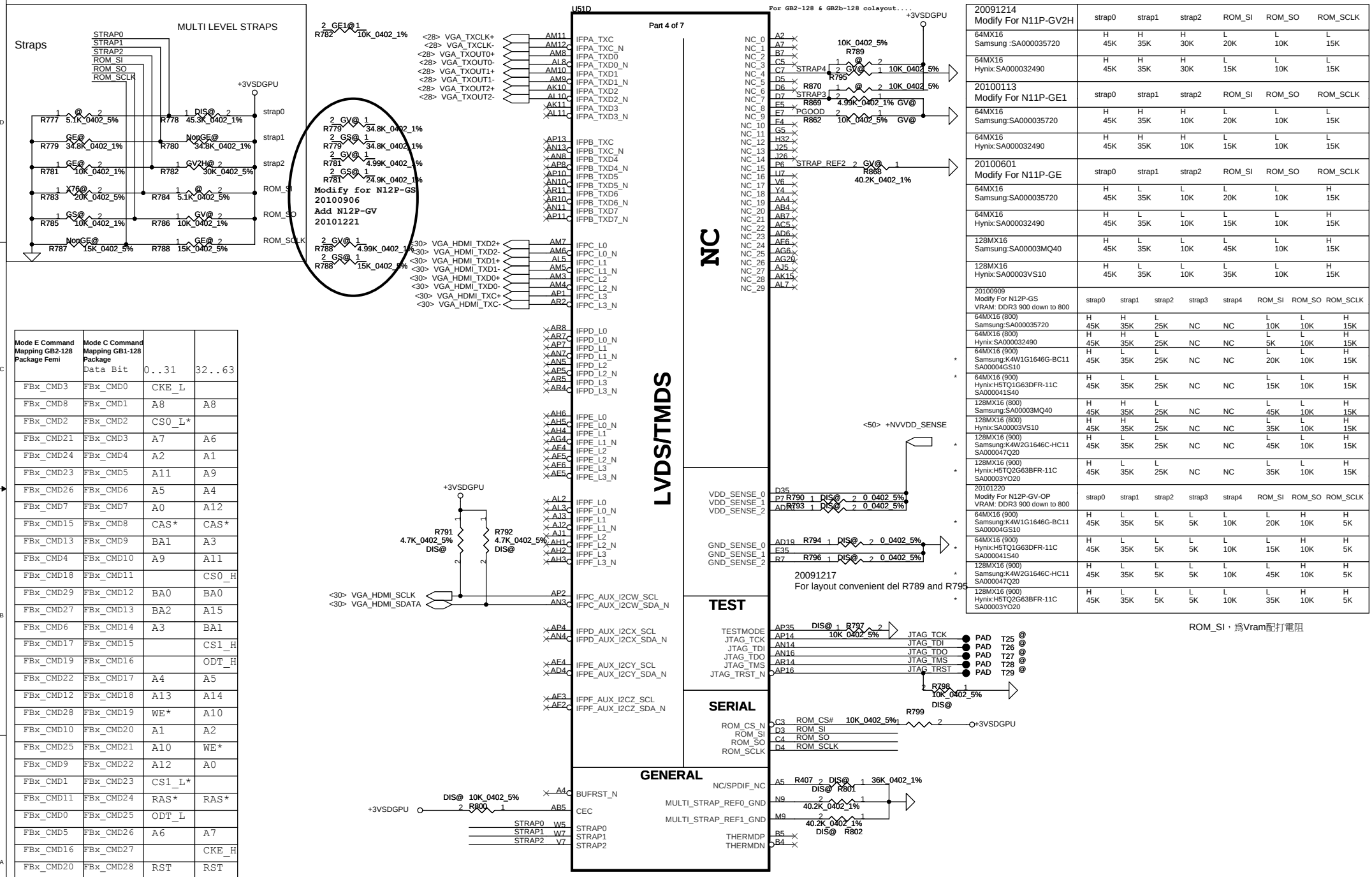

20091214 Modify For N11P-GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung :SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K
20100113 Modify For N11P-GE1	**strap0**	**strap1**	**strap2**	**ROM_SI**	**ROM_SO**	**ROM_SCLK**
64MX16 Samsung:SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K
20100601 Modify For N11P-GE	**strap0**	**strap1**	**strap2**	**ROM_SI**	**ROM_SO**	**ROM_SCLK**
64MX16 Samsung:SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K
64MX16 Hynix:SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K
128MX16 Samsung:SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K
128MX16 Hynix:SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K

20100909 Modify For N12P-GS VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (800) Samsung:SA000035720	H 45K	H 35K	L 25K	NC	NC	L 10K	L 10K	H 15K
64MX16 (800) Hynix:SA000032490	H 45K	H 35K	L 25K	NC	NC	L 5K	L 10K	H 15K
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 25K	NC	NC	L 20K	L 10K	H 15K
64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 25K	NC	NC	L 15K	L 10K	H 15K
128MX16 (800) Samsung:SA00003MQ40	H 45K	H 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (800) Hynix:SA00003VS10	H 45K	H 35K	L 25K	NC	NC	L 35K	L 10K	H 15K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 25K	NC	NC	L 35K	L 10K	H 15K

20101220 Modify For N12P-GV-OP VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	H 10K	H 5K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	H 10K	H 5K
128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 5K	L 5K	L 10K	L 35K	H 10K	H 5K

Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package		
	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0	CKE_L	
FBx_CMD8	FBx_CMD1	A8	A8
FBx_CMD2	FBx_CMD2	CS0_L*	
FBx_CMD21	FBx_CMD3	A7	A6
FBx_CMD24	FBx_CMD4	A2	A1
FBx_CMD23	FBx_CMD5	A11	A9
FBx_CMD26	FBx_CMD6	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD15	FBx_CMD8	CAS*	CAS*
FBx_CMD13	FBx_CMD9	BA1	A3
FBx_CMD4	FBx_CMD10	A9	A11
FBx_CMD18	FBx_CMD11		CS0_H
FBx_CMD29	FBx_CMD12	BA0	BA0
FBx_CMD27	FBx_CMD13	BA2	A15
FBx_CMD6	FBx_CMD14	A3	BA1
FBx_CMD17	FBx_CMD15		CS1_H
FBx_CMD19	FBx_CMD16		ODT_H
FBx_CMD22	FBx_CMD17	A4	A5
FBx_CMD12	FBx_CMD18	A13	A14
FBx_CMD28	FBx_CMD19	WE*	A10
FBx_CMD10	FBx_CMD20	A1	A2
FBx_CMD25	FBx_CMD21	A10	WE*
FBx_CMD9	FBx_CMD22	A12	A0
FBx_CMD1	FBx_CMD23	CS1_L*	
FBx_CMD11	FBx_CMD24	RAS*	RAS*
FBx_CMD0	FBx_CMD25	ODT_L	
FBx_CMD5	FBx_CMD26	A6	A7
FBx_CMD16	FBx_CMD27		CKE_H
FBx_CMD20	FBx_CMD28	RST	RST
FBx_CMD14	FBx_CMD29	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
FBx_CMD31			
		LOW	HIGH

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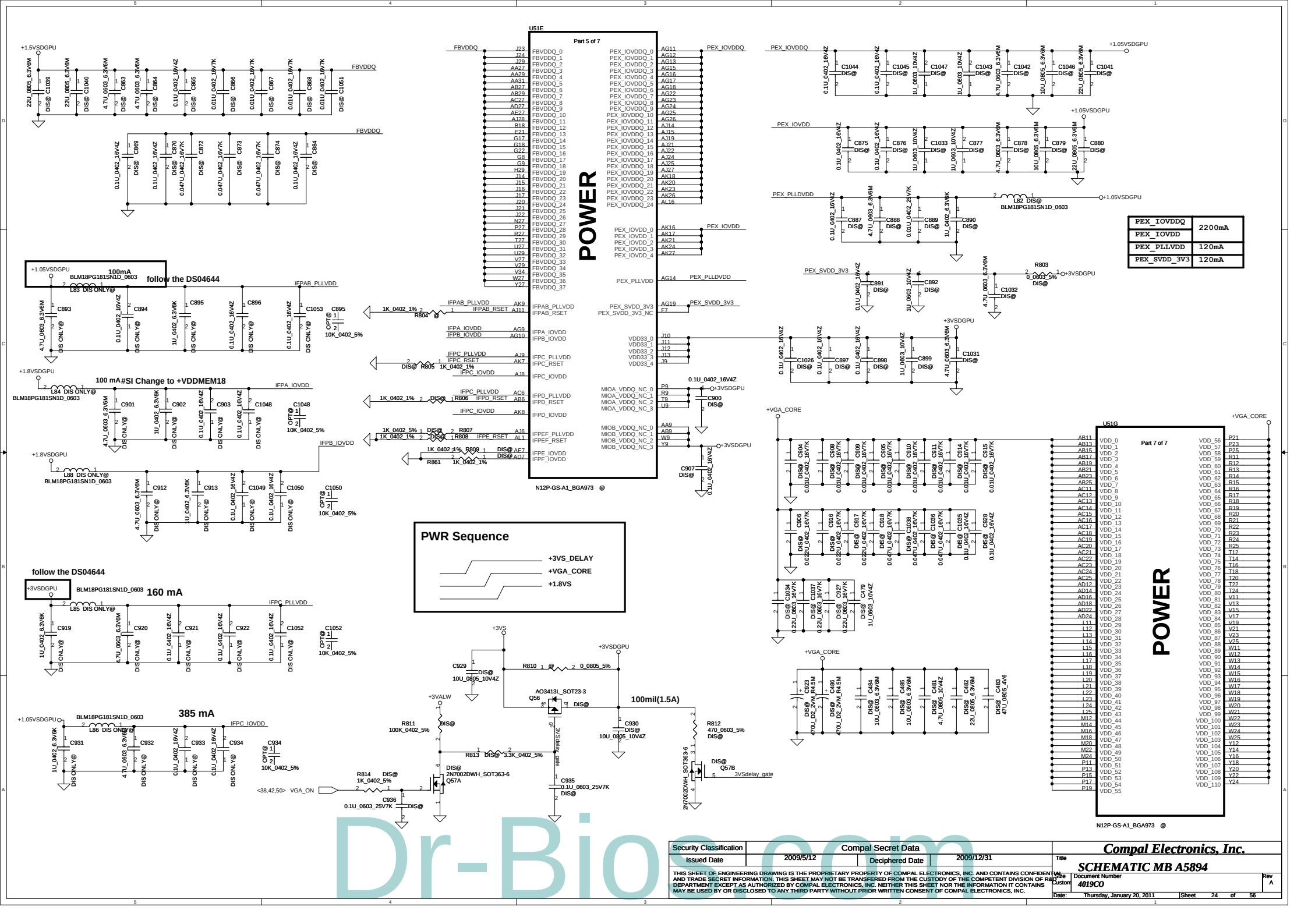

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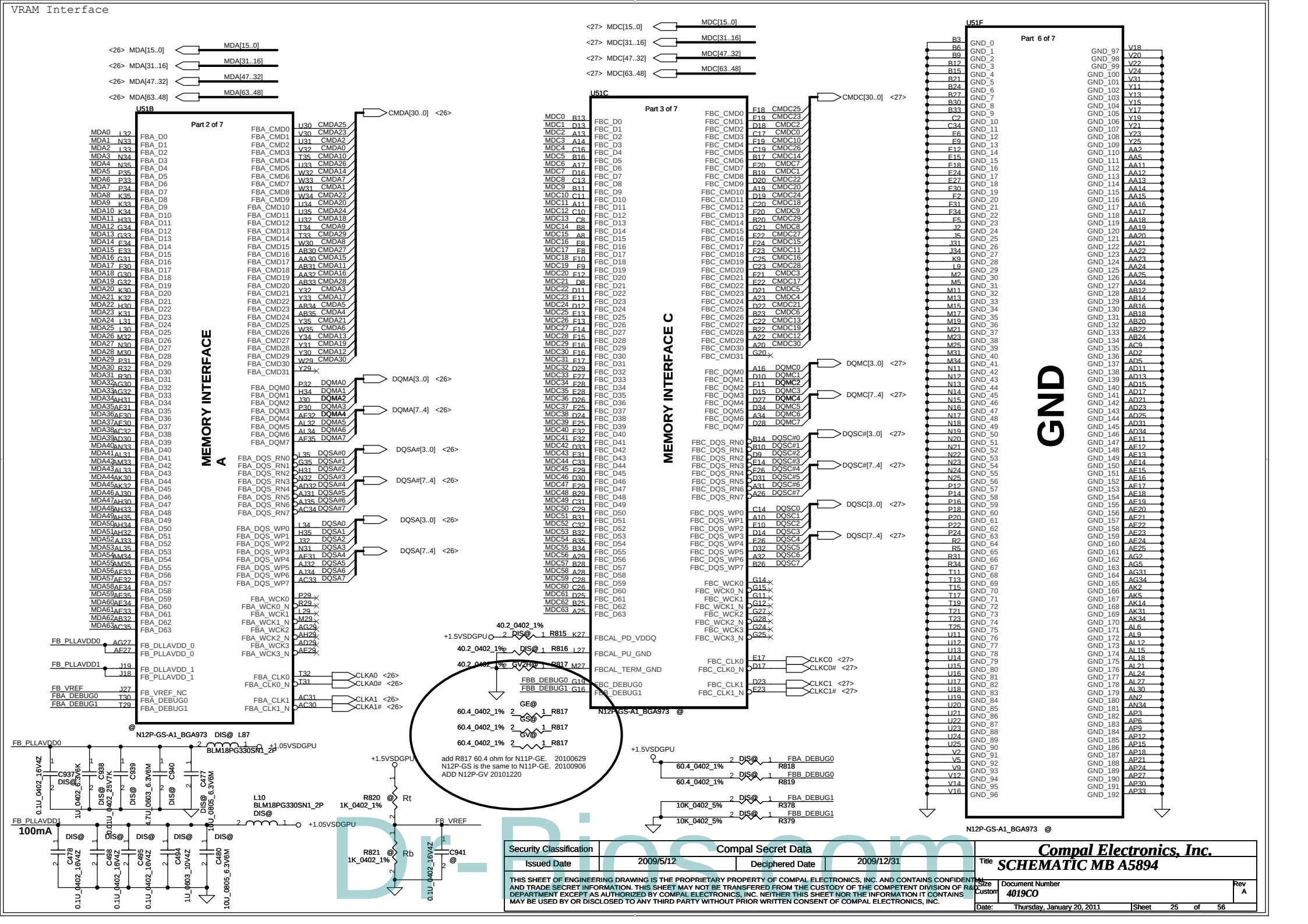

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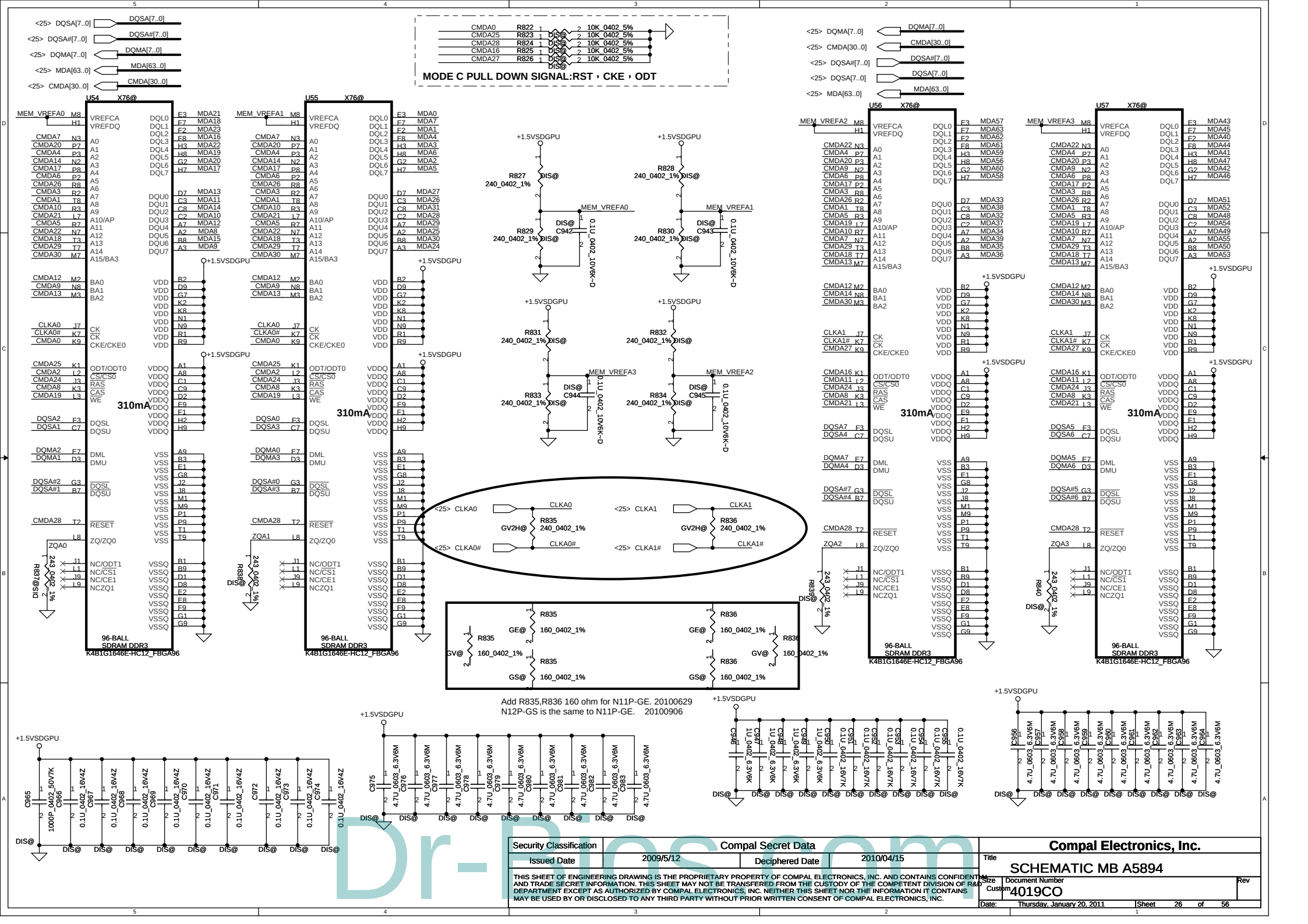

Add R835,R836 160 ohm for N11P-GE. 20100629
N12P-GS is the same to N11P-GE. 20100906

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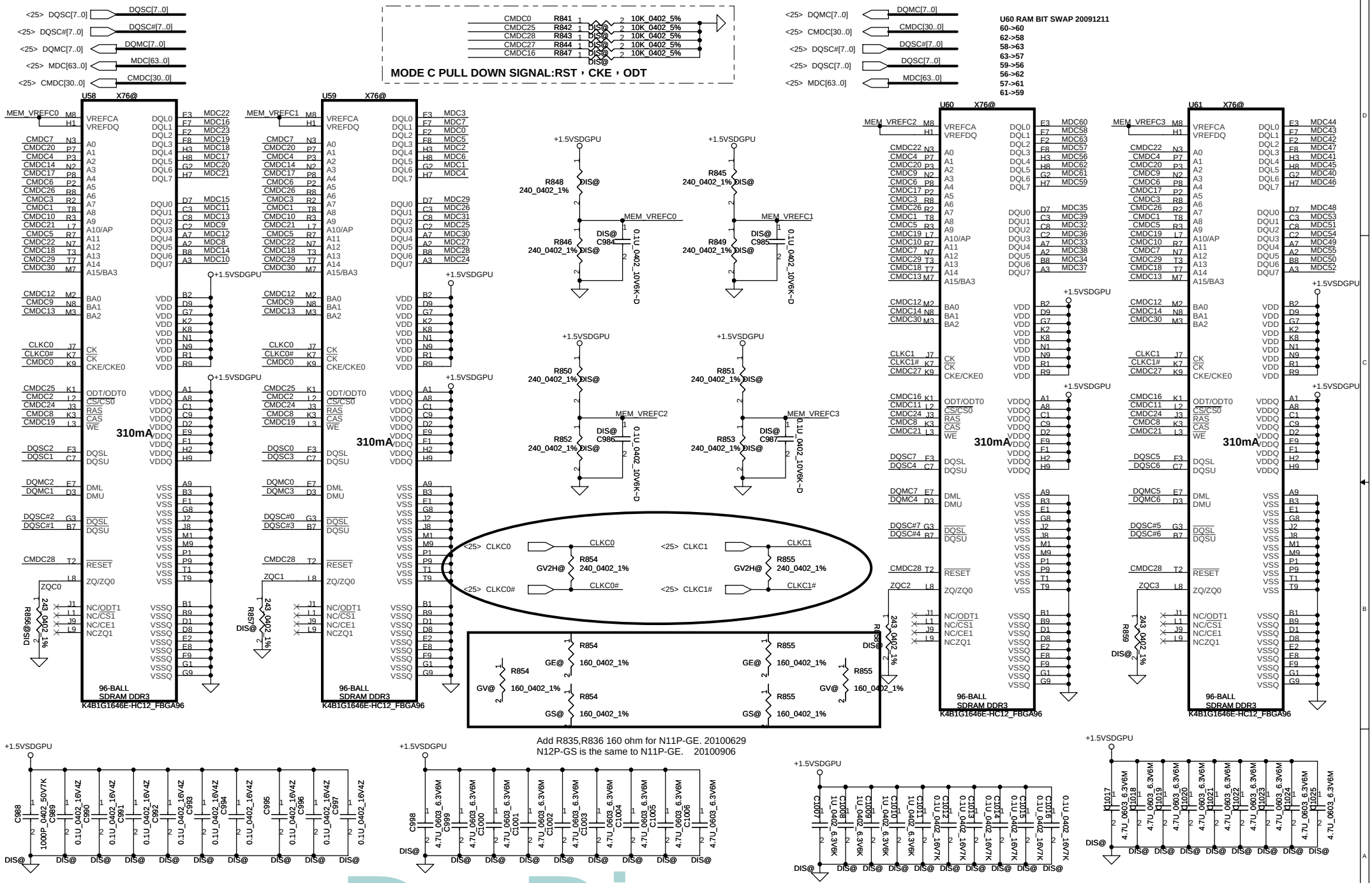

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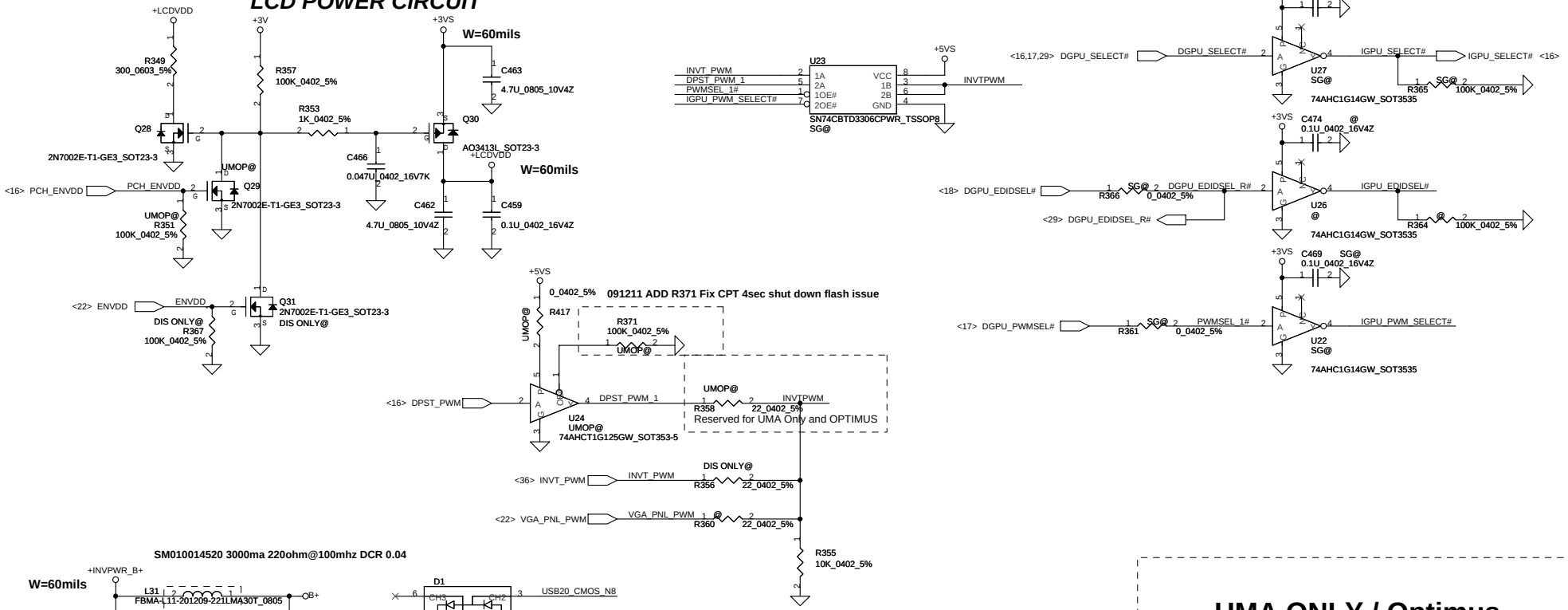
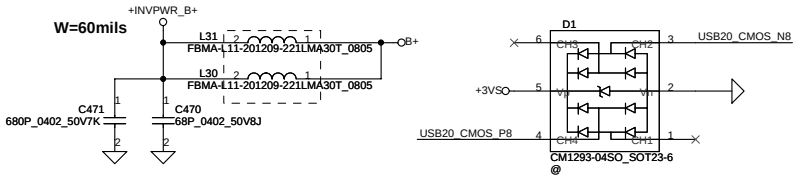
LCD POWER CIRCUIT



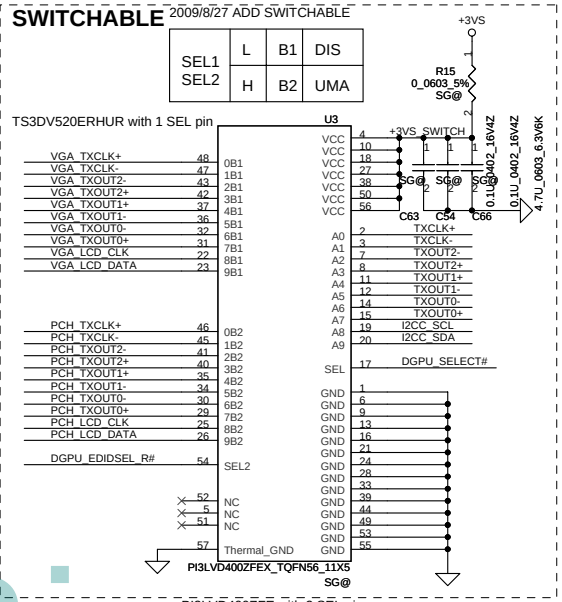
SM010014520 3000ma 220ohm@100mhz DCR 0.04



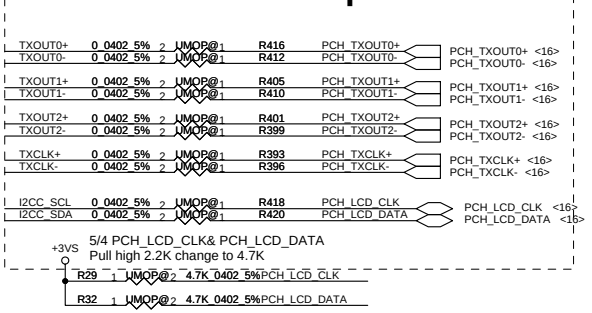
SWITCHABLE

2009/8/27 ADD SWITCHABLE

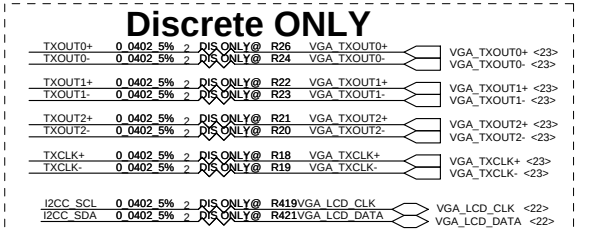
SEL1	L	B1	DIS
SEL2	H	B2	UMA



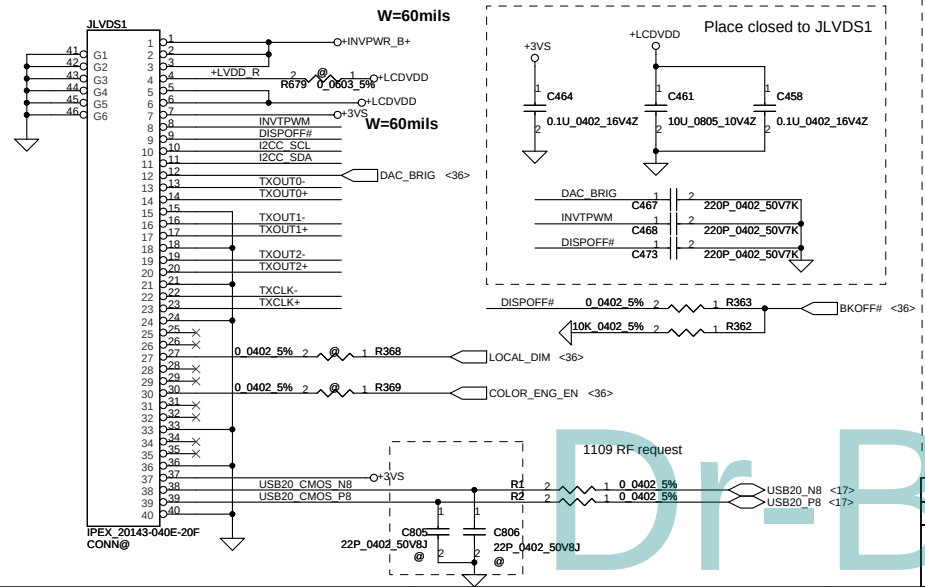
UMA ONLY / Optimus



Discrete ONLY



LCD/LED PANEL Conn.



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UMA ONLY & OPTIMUS

R372 UMOP@ FCM2012CF-800T06_2P
R376 UMOP@ FCM2012CF-800T06_2P
R377 UMOP@ FCM2012CF-800T06_2P

UMOP@ C607 10P_0402_50V8J
UMOP@ C592 10P_0402_50V8J
UMOP@ C567 10P_0402_50V8J
UMOP@ C603 10P_0402_50V8J
UMOP@ C593 10P_0402_50V8J
UMOP@ C569 10P_0402_50V8J

Change to 0 ohm for CRT EA rising falling time

R372 0_0805_5% DIS ONLY@
R376 0_0805_5% DIS ONLY@
R377 0_0805_5% DIS ONLY@

CRT_R → CRT_R_1 → L48 FCM2012CF-800T06_2P → CRT_R_2
CRT_G → CRT_G_1 → L41 FCM2012CF-800T06_2P → CRT_G_2
CRT_B → CRT_B_1 → L39 FCM2012CF-800T06_2P → CRT_B_2

R466 150_0402_1%
R464 150_0402_1%
R446 150_0402_1%
150_0402_1%

C607 C592 C567 6P_0402_50V8J DIS ONLY@

For CRT flicker issue
Change C607 C592 C567
Form 8p to 6p
20100617

C618 C598 C590 22P_0402_50V8J UMOP@

C603 C593 C569 15P_0402_50V8J DIS ONLY@

For CRT flicker issue
Change C603 C593 C569
Form 12p to 15p
20100617

D17 D16 D14 BAV99_SOT-23

+5VS → D2 CH491DPT_SOT23-3 → F1 1.1A_6V_SMD1812P110TF → +R_CRT_VCC → +CRT_VCC
W=40mils
W=40mils
C171 0.1U_0402_16V4Z

+3VS

JCRT1
T13 PAD @
C-H_13-12201513CP CONN@
CRT_DET# <18>

C110 100P_0402_50V8J
DSUB_12
DSUB_15
R41 100K_0402_5% @
C208 68P_0402_50V8J
C126 68P_0402_50V8J
+CRT_VCC

L2 MBC1608121YZF_0603 → CRT_HSYNC_2
L1 MBC1608121YZF_0603 → CRT_VSYNC_2
C178 10P_0402_50V8J
C164 10P_0402_50V8J

C194 0.1U_0402_16V4Z
R67 10K_0402_5%
U7 74AHCT1G125GW_SOT353-5
CRT_HSYNC → CRT_HSYNC_1
+CRT_VCC

C111 0.1U_0402_16V4Z
U5 74AHCT1G125GW_SOT353-5
CRT_VSYNC → CRT_VSYNC_1

D33 D25 BAV99_SOT-23

20091214 For NV Recommand

+3VS
R48 4.7K_0402_5%
R78 4.7K_0402_5%
CRT_DDC_DATA → Q3 2N7002E-T1-GE3_SOT23-3 → DSUB_12
CRT_DDC_CLK → Q2 2N7002E-T1-GE3_SOT23-3 → DSUB_15

SWITCHABLE

2009/08/27

+3VS
0.1U_0402_16V4Z
C273 SG@
C290 SG@
C271 SG@
C280 SG@ 0.1U_0402_16V4Z
0.1U_0402_16V4Z
0.1U_0402_16V4Z

U10 PI3V712-AZLEX_TQFN32_6X3-D SG@

VGA_CRT_R	0B1	CRT_R
VGA_CRT_G	1B1	CRT_G
VGA_CRT_B	2B1	CRT_B
VGA_CRT_HSYNC	3B1	CRT_HSYNC
VGA_CRT_VSYNC	4B1	CRT_VSYNC
VGA_DDC_CLK	5B1	
VGA_DDC_DATA	6B1	SEL1 → DGPU_SELECT# <16,17,28>
	SEL2 → DGPU_EDIDSEL_R# <28>	
PCH_CRT_R	0B2	CRT_DDC_CLK
PCH_CRT_G	1B2	CRT_DDC_DATA
PCH_CRT_B	2B2	
PCH_CRT_HSYNC	3B2	
PCH_CRT_VSYNC	4B2	
PCH_CRT_CLK	5B2	
PCH_CRT_DATA	6B2	

L	B1	DIS
H	B2	UMA

Discrete only

<22> VGA_CRT_R	VGA_CRT_R	R537 DIS ONLY@	0_0402_5%	CRT_R
<22> VGA_CRT_G	VGA_CRT_G	R535 DIS ONLY@	0_0402_5%	CRT_G
<22> VGA_CRT_B	VGA_CRT_B	R533 DIS ONLY@	0_0402_5%	CRT_B
<22> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R531 DIS ONLY@	0_0402_5%	CRT_HSYNC
<22> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R529 DIS ONLY@	0_0402_5%	CRT_VSYNC
<22> VGA_DDC_CLK	VGA_DDC_CLK	R527 DIS ONLY@	0_0402_5%	CRT_DDC_CLK
<22> VGA_DDC_DATA	VGA_DDC_DATA	R526 DIS ONLY@	0_0402_5%	CRT_DDC_DATA

VGA_DDC_DATA and VGA_DDC_CLK Pull high at Page22

UMA only & Optimus

<16> PCH_CRT_R	PCH_CRT_R	R536 UMOP@	0_0402_5%	CRT_R
<16> PCH_CRT_G	PCH_CRT_G	R534 UMOP@	0_0402_5%	CRT_G
<16> PCH_CRT_B	PCH_CRT_B	R532 UMOP@	0_0402_5%	CRT_B
<16> PCH_CRT_HSYNC	PCH_CRT_HSYNC	R530 UMOP@	0_0402_5%	CRT_HSYNC
<16> PCH_CRT_VSYNC	PCH_CRT_VSYNC	R528 UMOP@	0_0402_5%	CRT_VSYNC
<16> PCH_CRT_CLK	PCH_CRT_CLK	R544 UMOP@	0_0402_5%	CRT_DDC_CLK
<16> PCH_CRT_DATA	PCH_CRT_DATA	R543 UMOP@	0_0402_5%	CRT_DDC_DATA

PCH DDC PU 2.2K on Page 17

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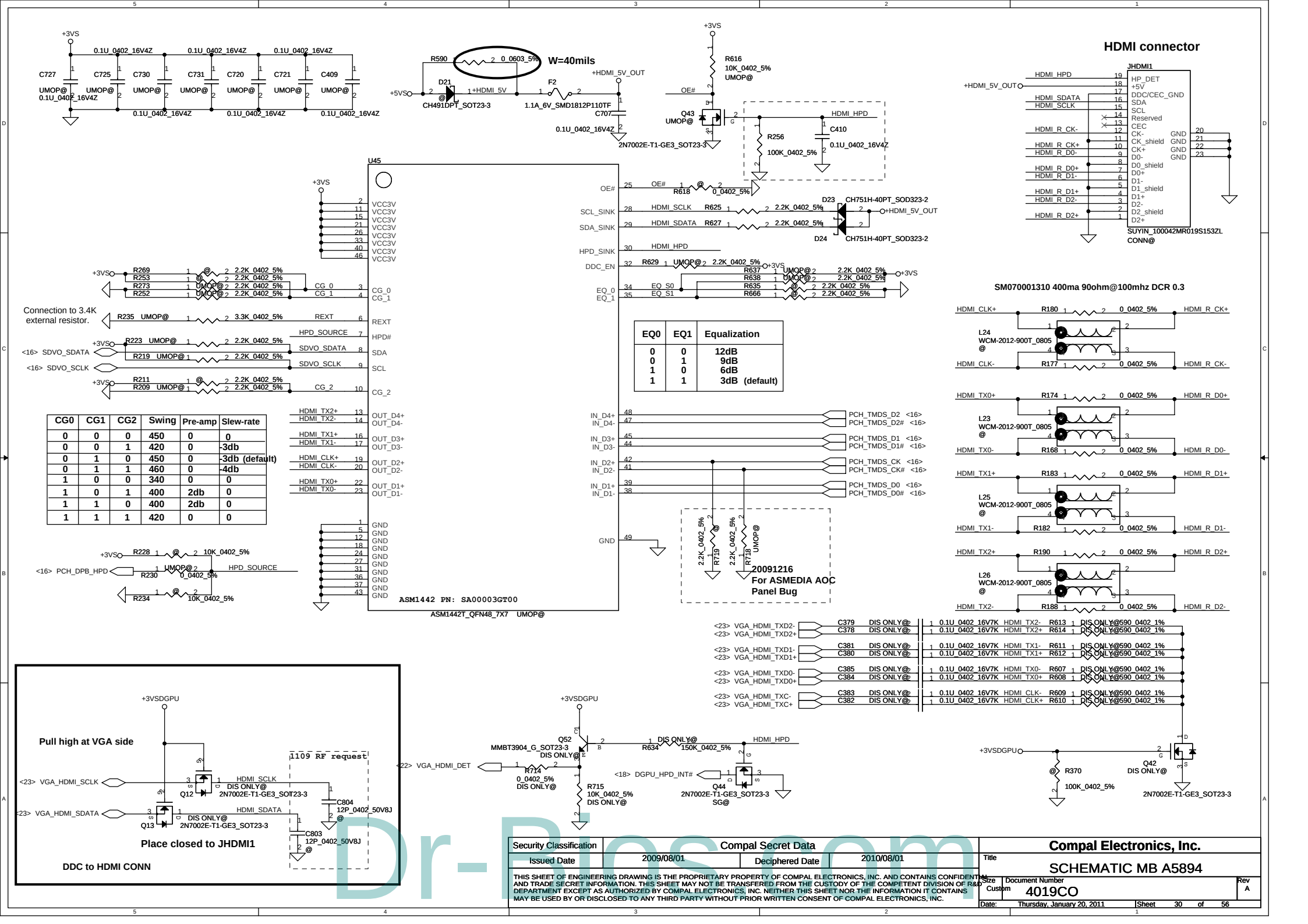

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

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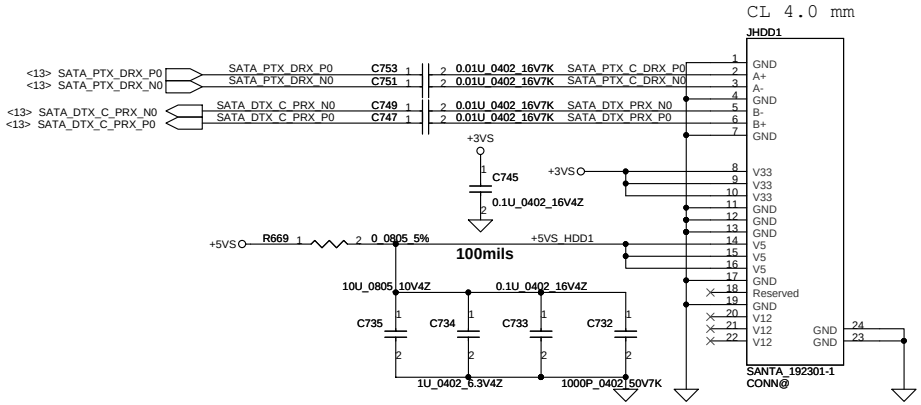
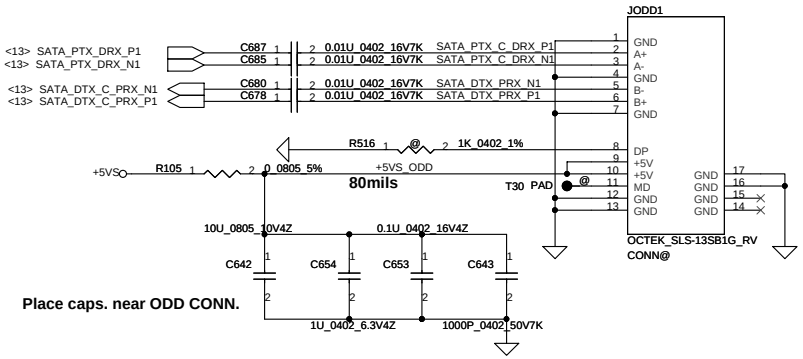
SATA HDD1 Conn.



SATA ODD Conn.



Place caps. near ODD CONN.

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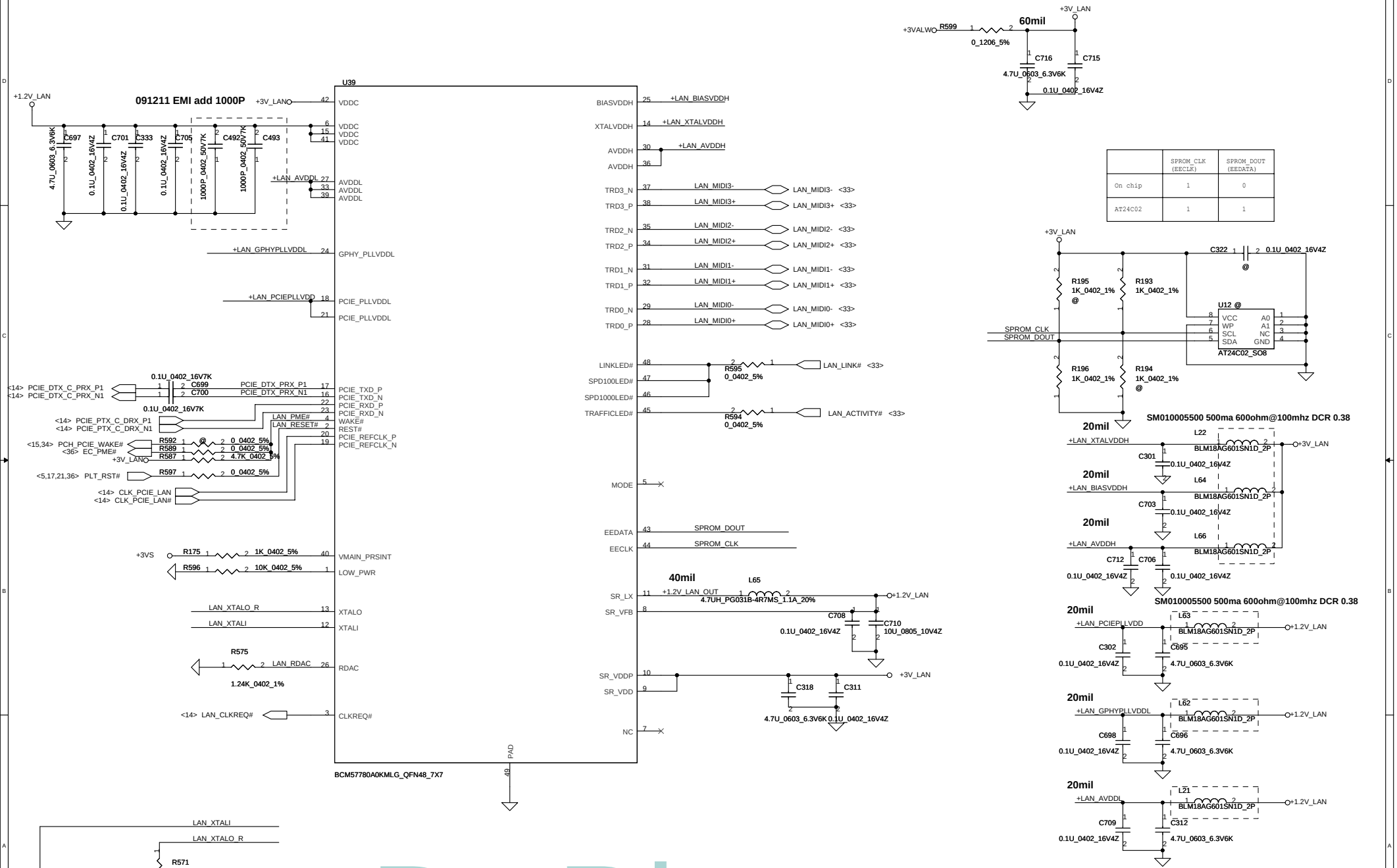

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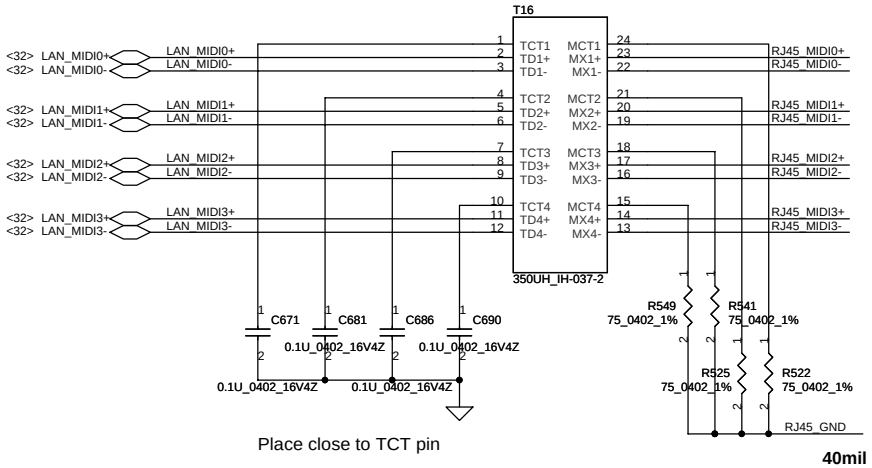
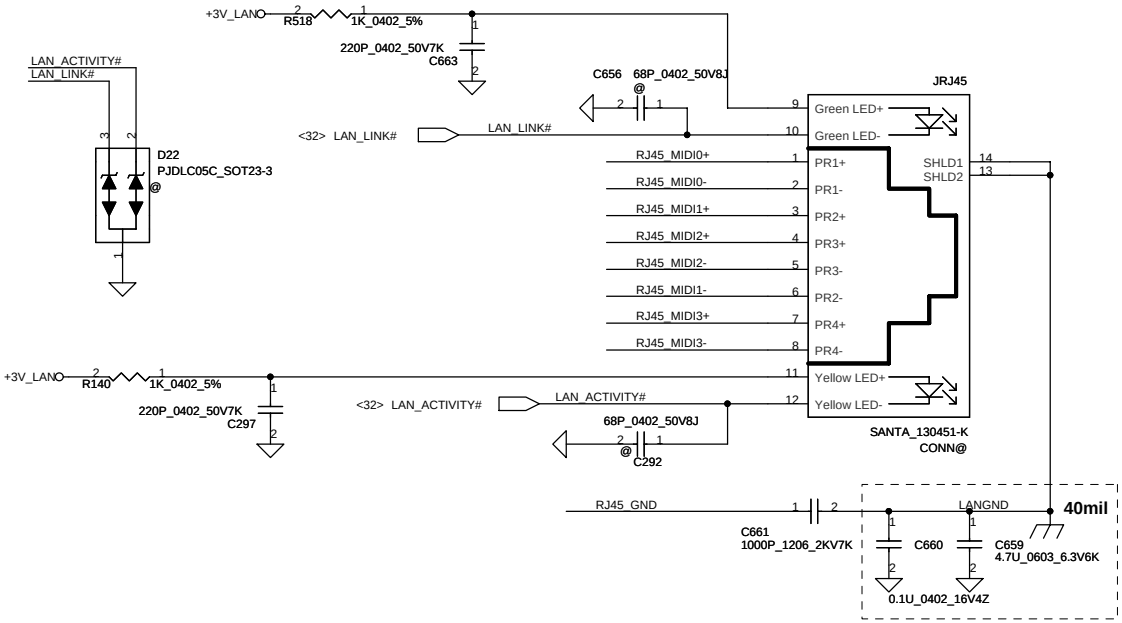
LAN Connector



BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



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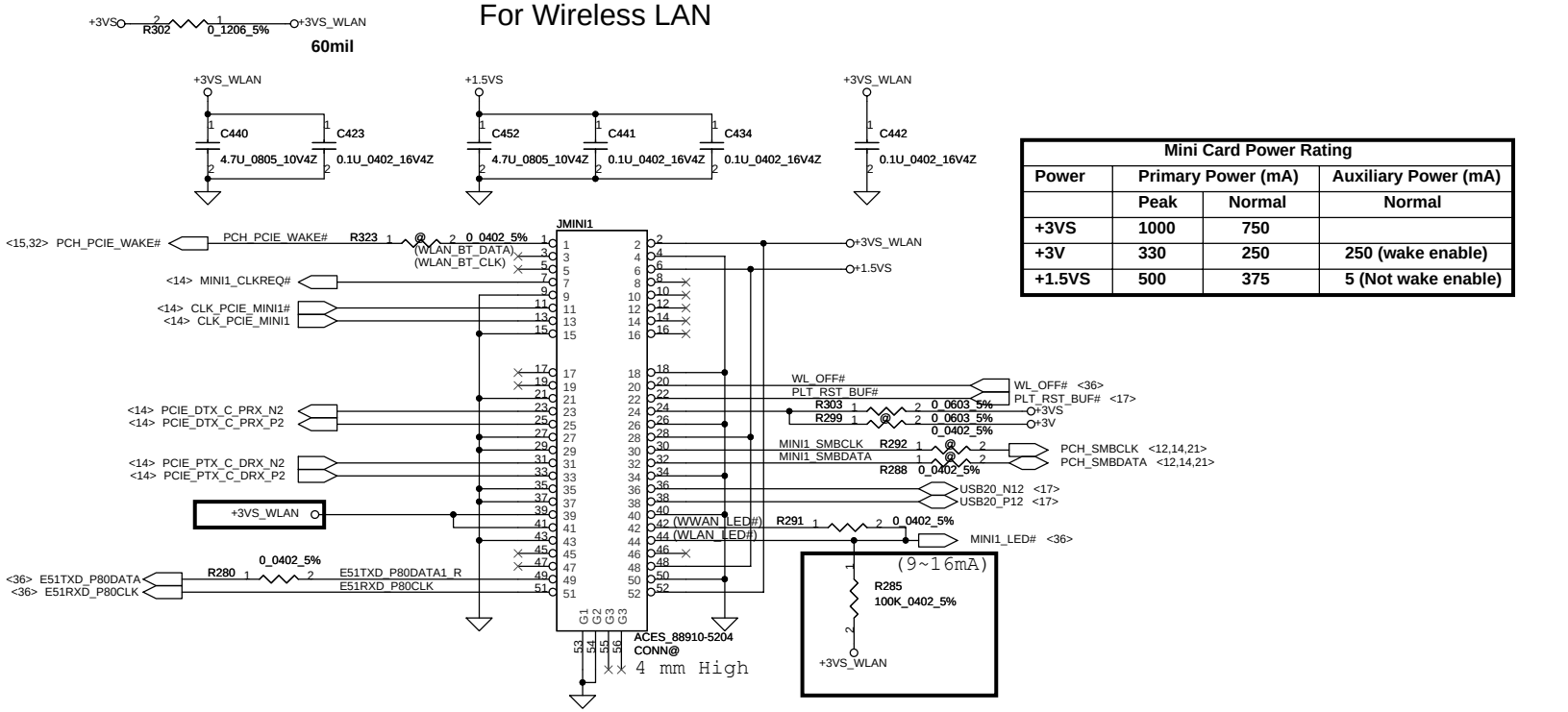
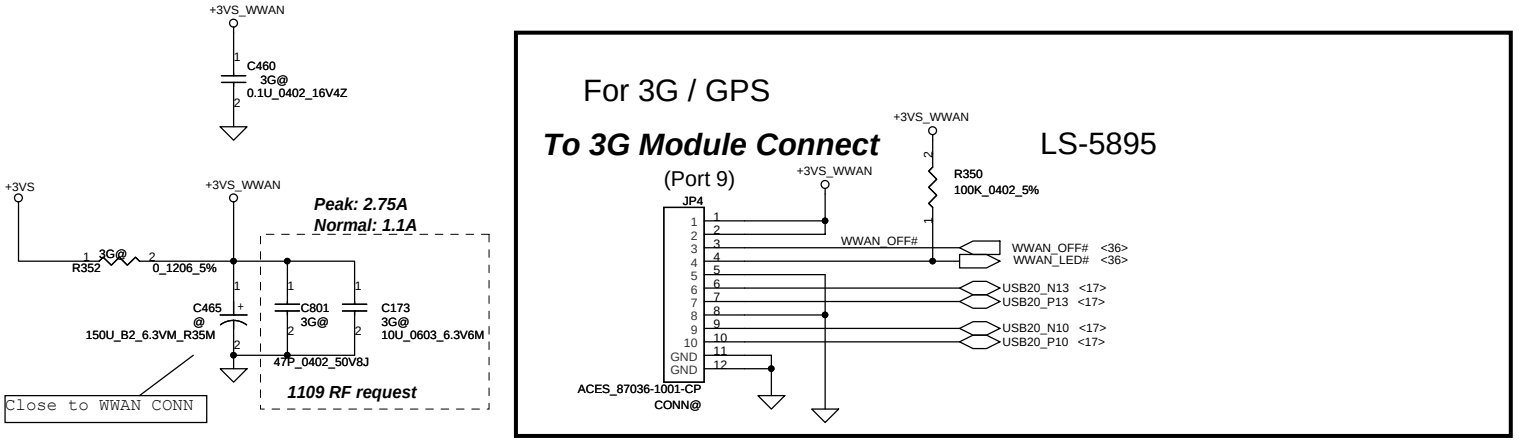


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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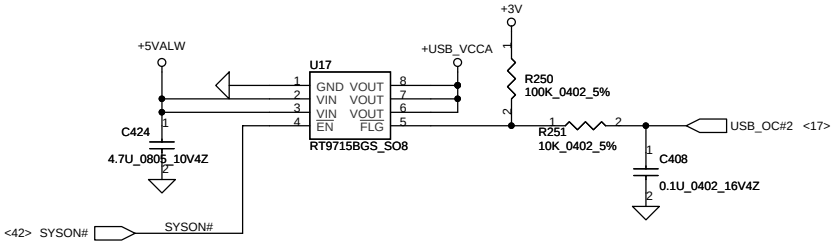
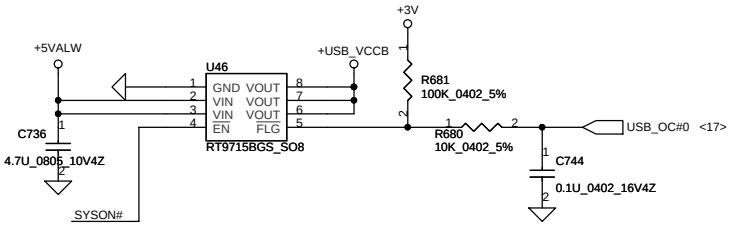
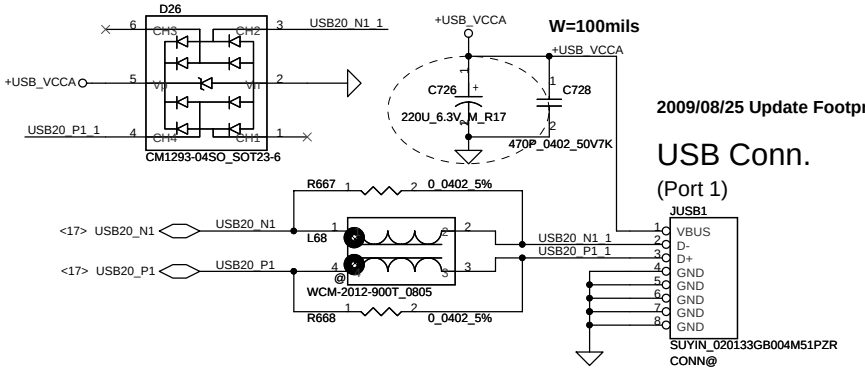




2009/08/14 CHANGE cap



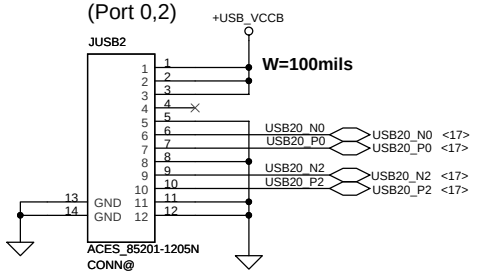
2009/08/25 Update Footprint(follow NAL00)

USB Conn.

(Port 1)

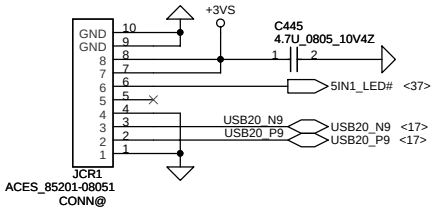
USB/B Conn. LS-5891

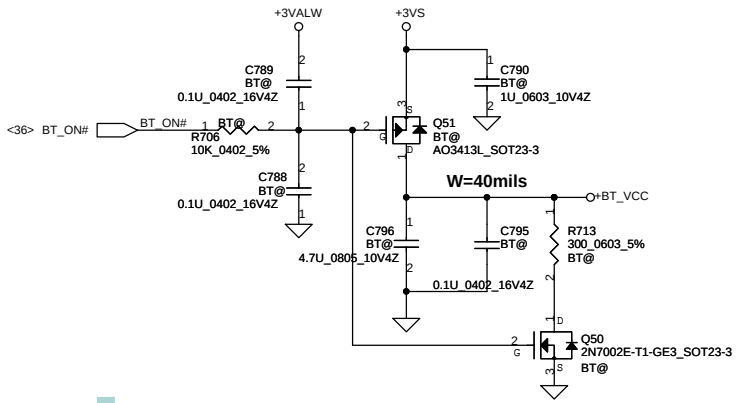
(Port 0,2)



2009/08/24 CHANGE Conn to FFC Type

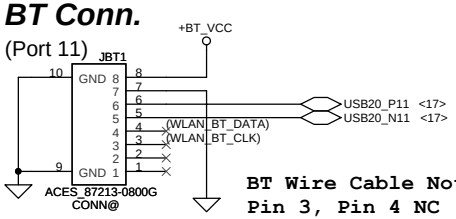
Card Reader Conn. LS-5896





BT Conn.

(Port 11)



BT Wire Cable Note:
Pin 3, Pin 4 NC

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SM010015410 300ma 80ohm@100mhz DCR 0.3

For EC Tools

Place on RAM door

Place on MiniCard

Board ID definition, Please see page 3.

Project ID definition, Please see page 3.

For Low PWR Pannel use

U32 — KB926QFD3_LQFP128_14X14

<BOM Structure>

PCH_TEMP_ALERT# Pull high at Page 18 (PCH side)

SM010015410 300ma 80ohm@100mhz DCR 0.3

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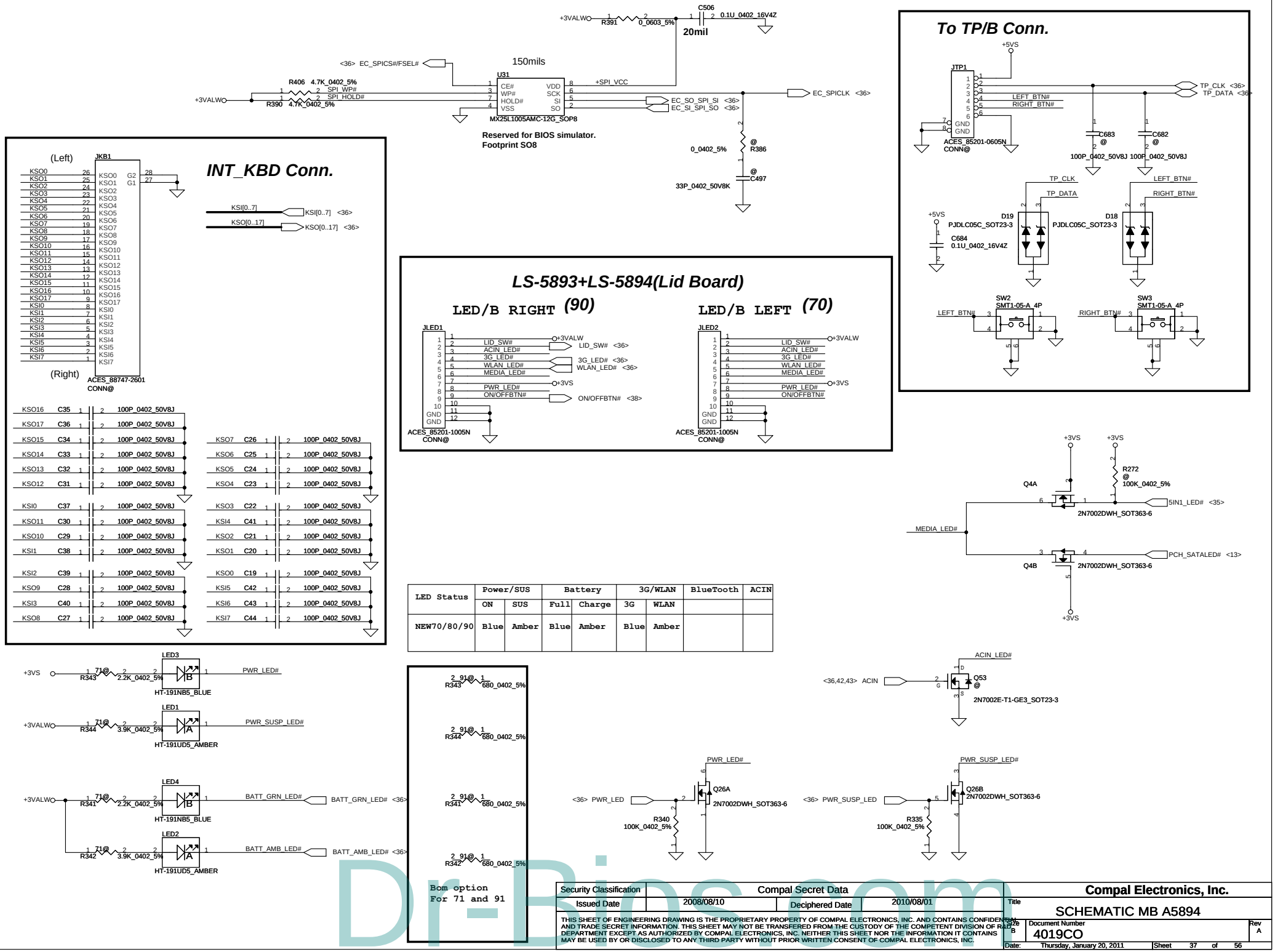

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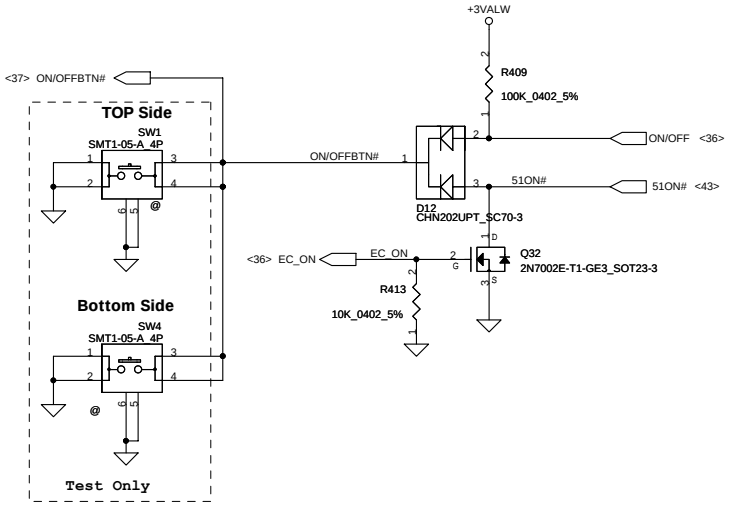
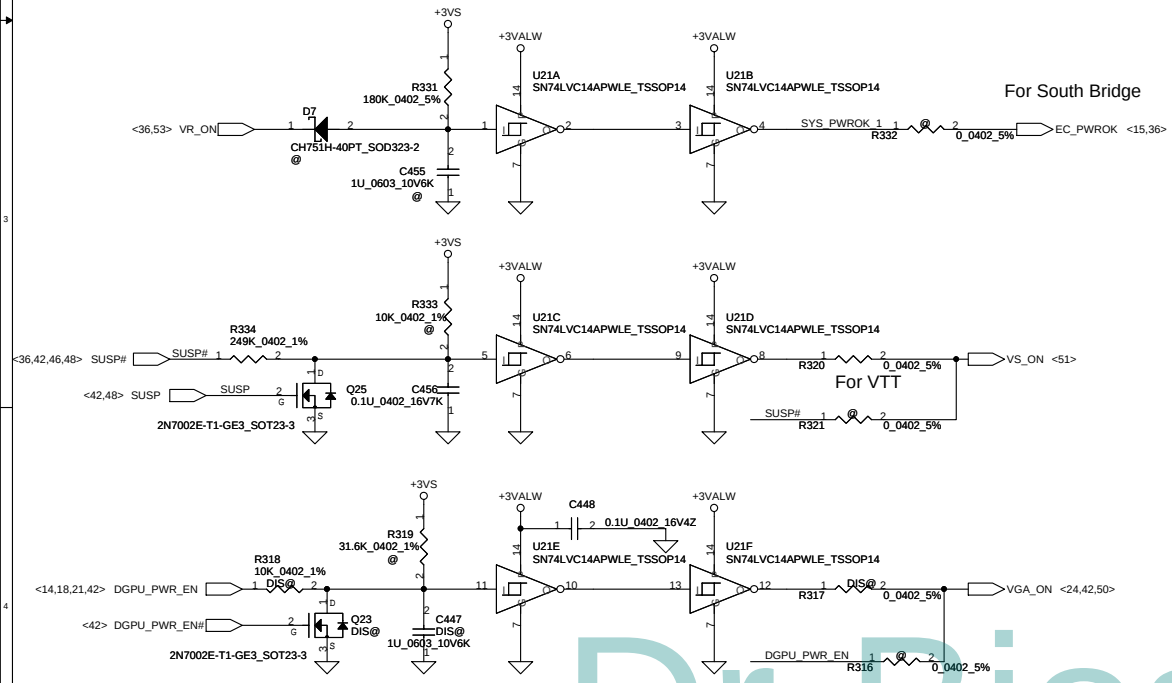
Power Button

ON/OFF switch



Power ON Circuit



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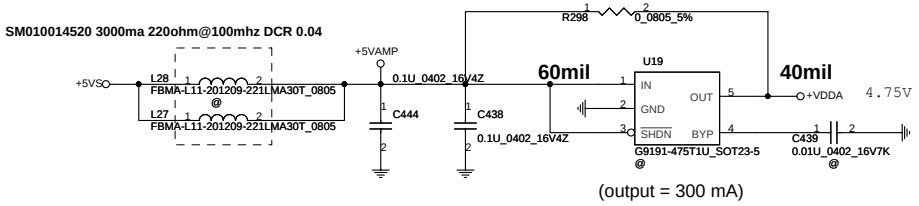
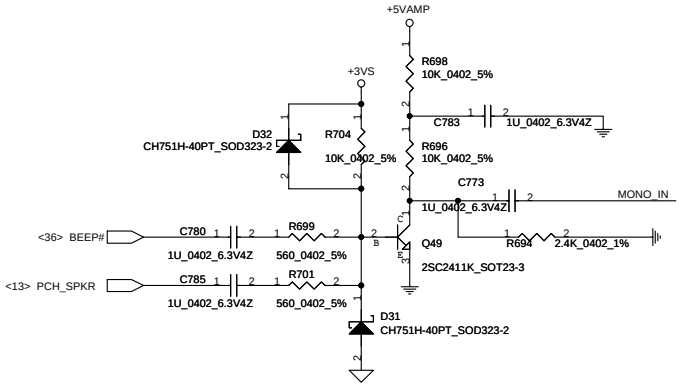
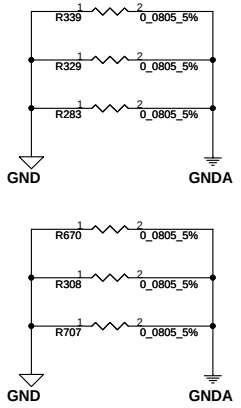
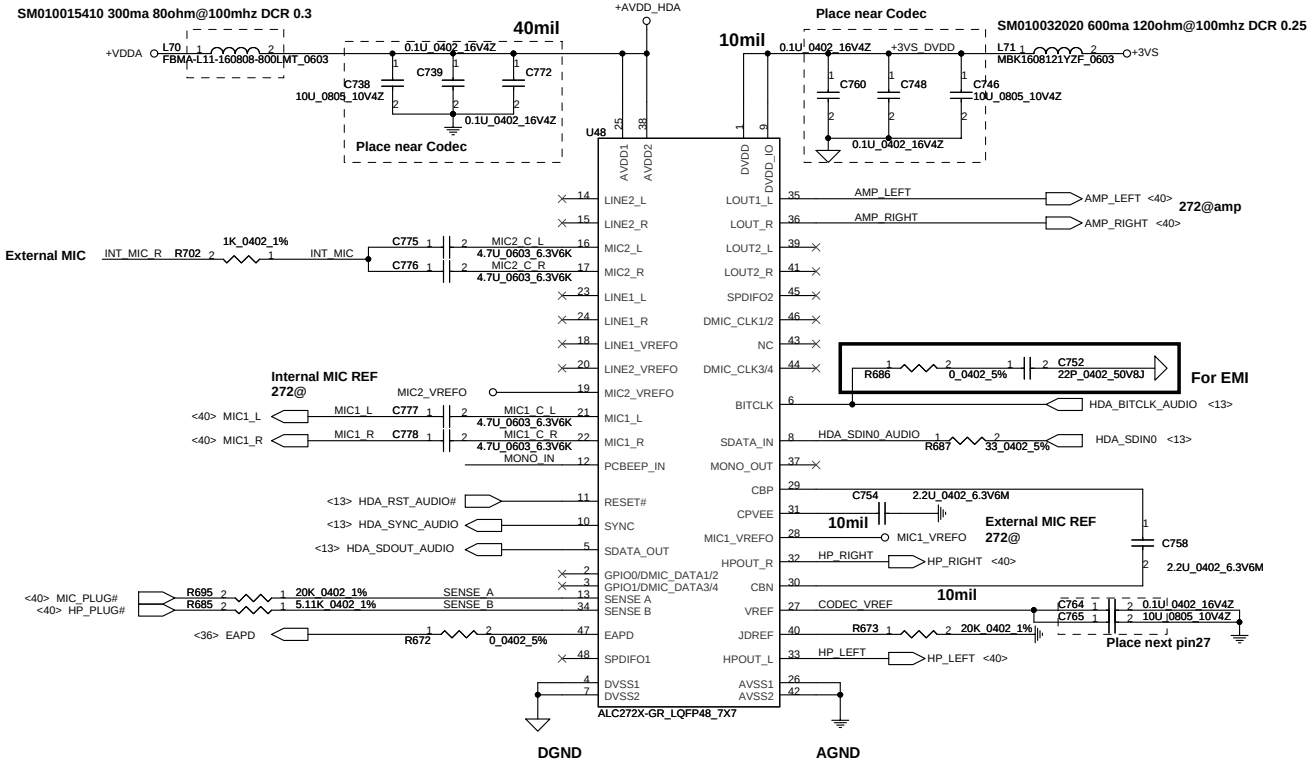


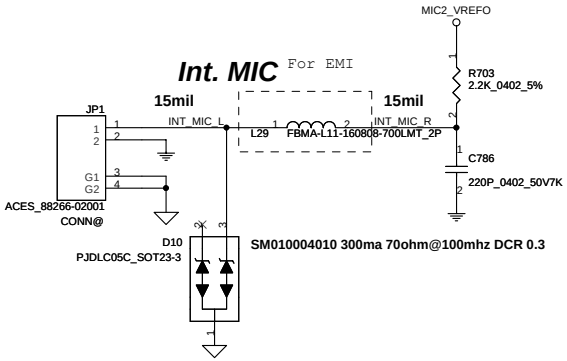
(output = 300 mA)





HD Audio Codec





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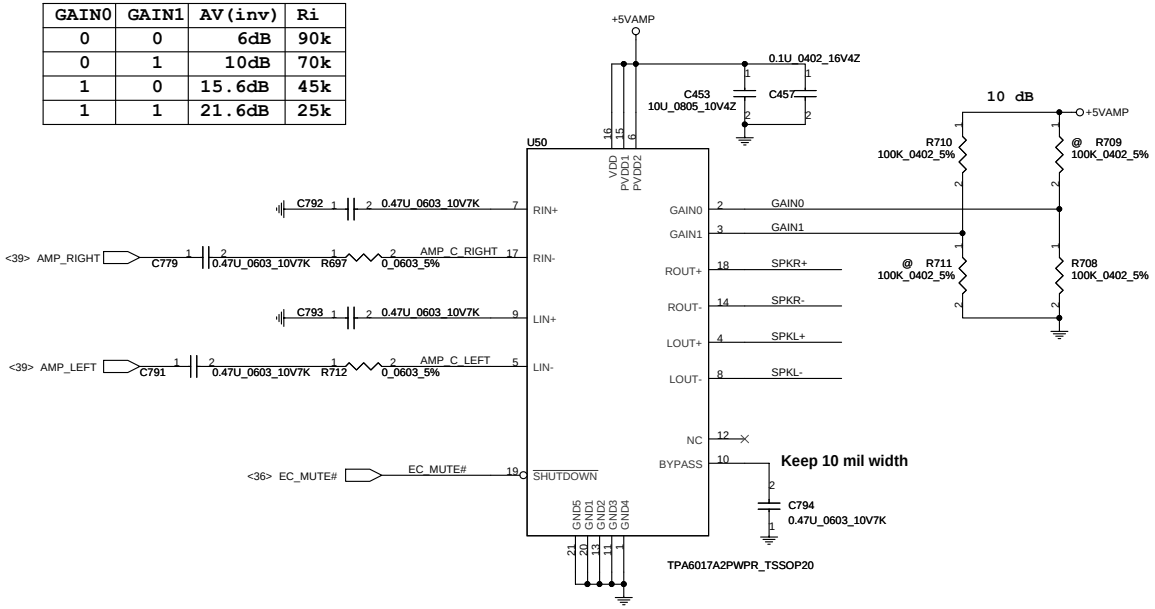
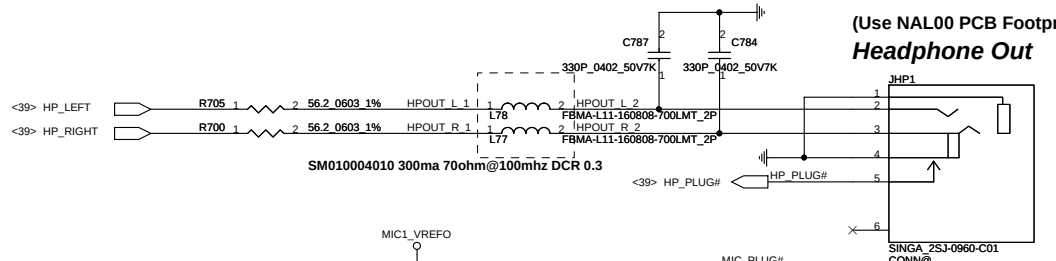
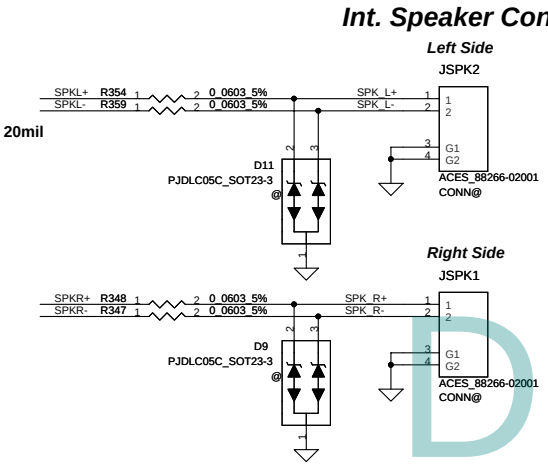
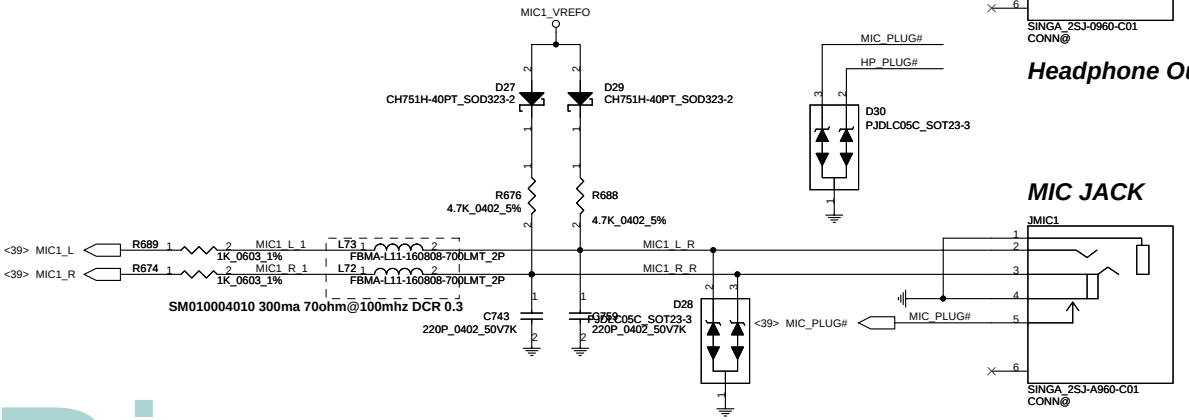
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k









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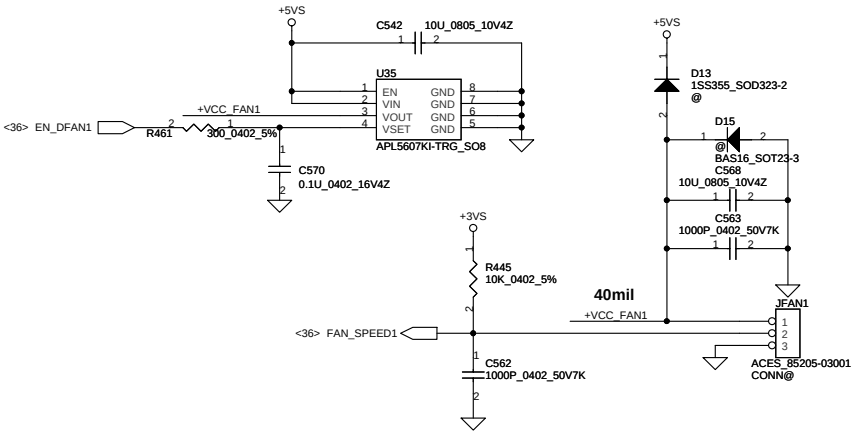
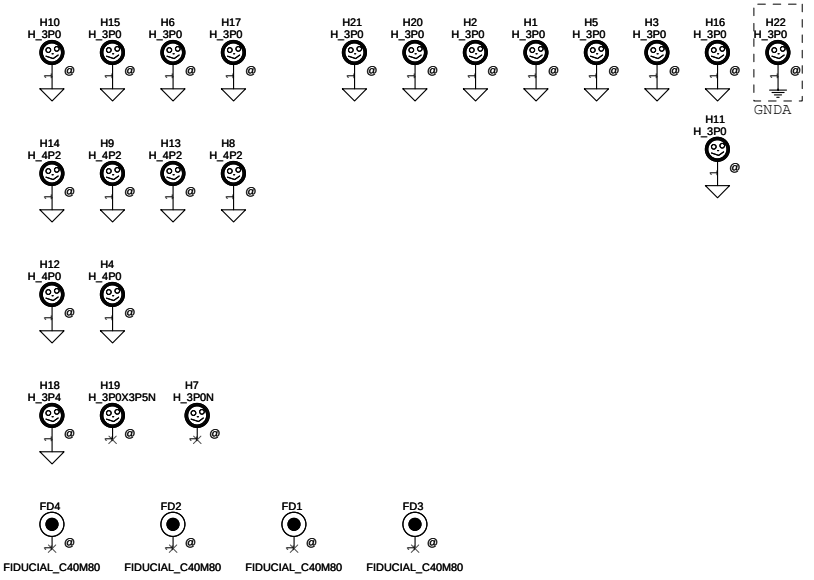
FAN1 Conn





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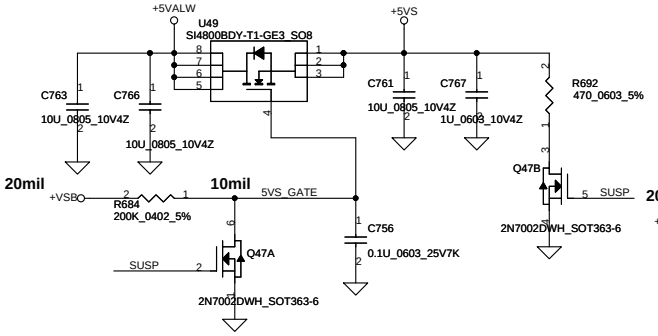
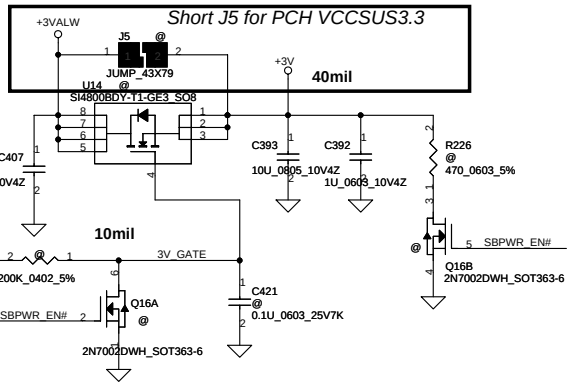
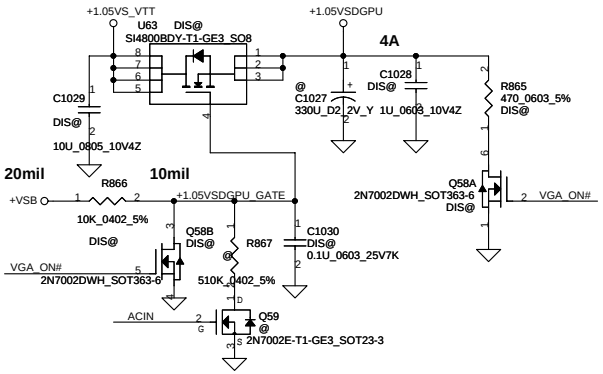
+5VALW TO +5VS



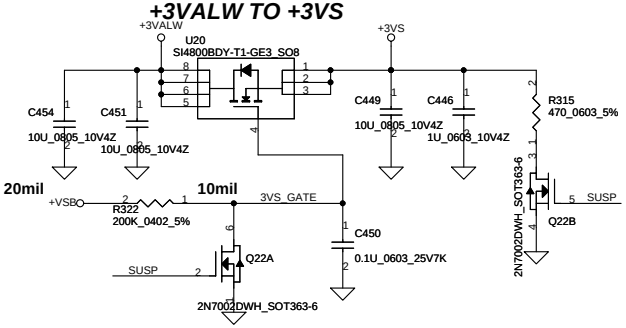
+3VALW TO +3V(PCH AUX Power)



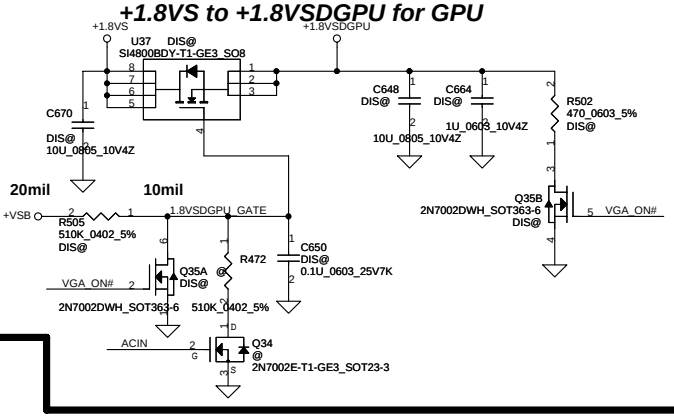
+1.05VS_VTT to +1.05VSDGPU for GPU

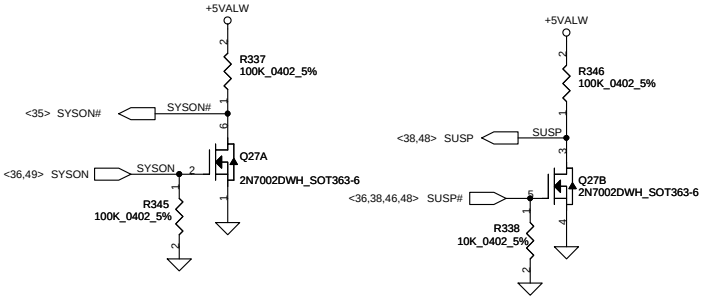


+3VALW TO +3VS

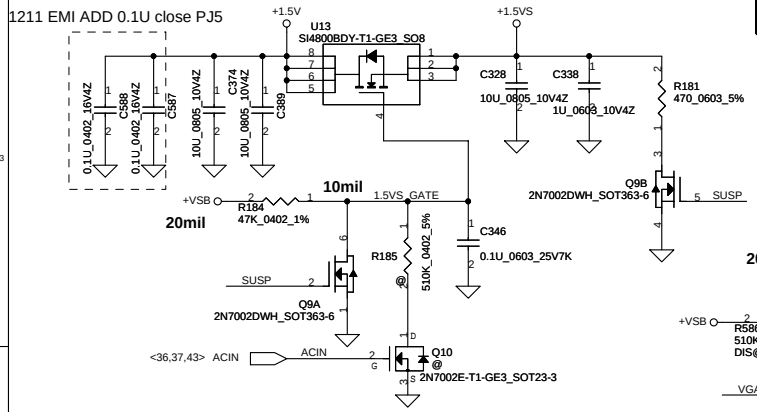


+1.8VS to +1.8VSDGPU for GPU

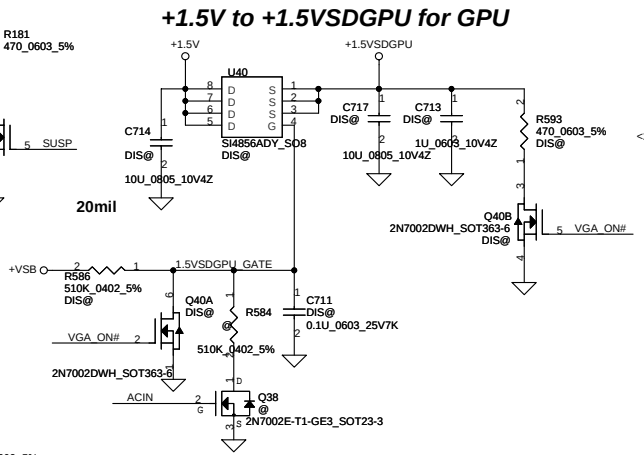


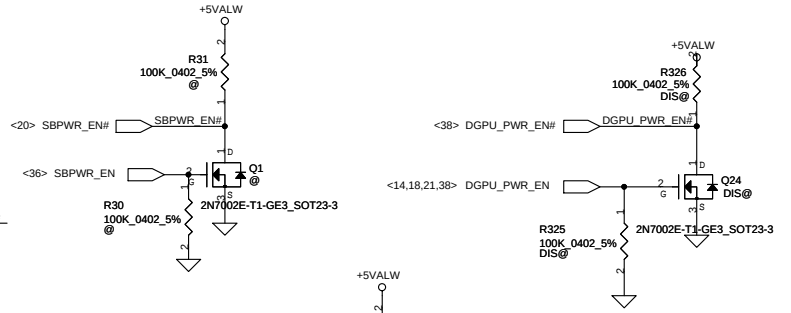


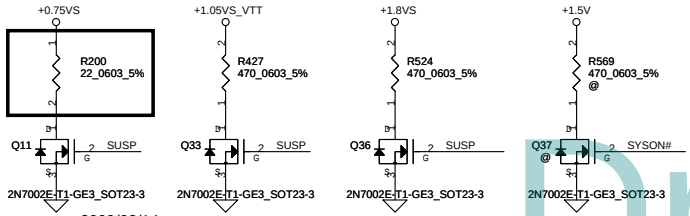
+1.5V to +1.5VS

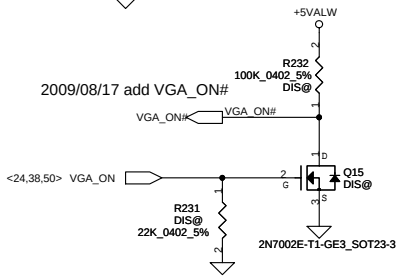


+1.5V to +1.5VSDGPU for GPU









2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

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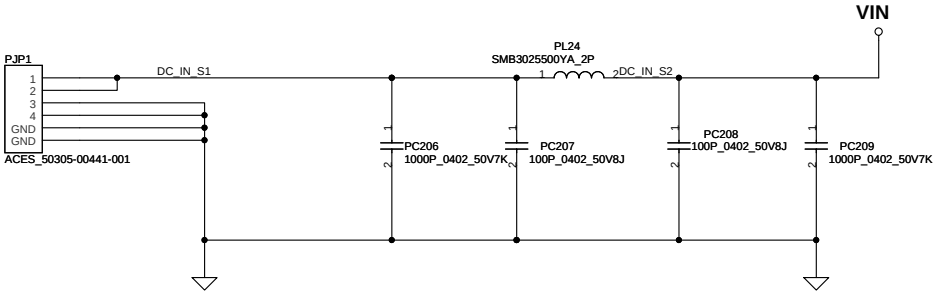
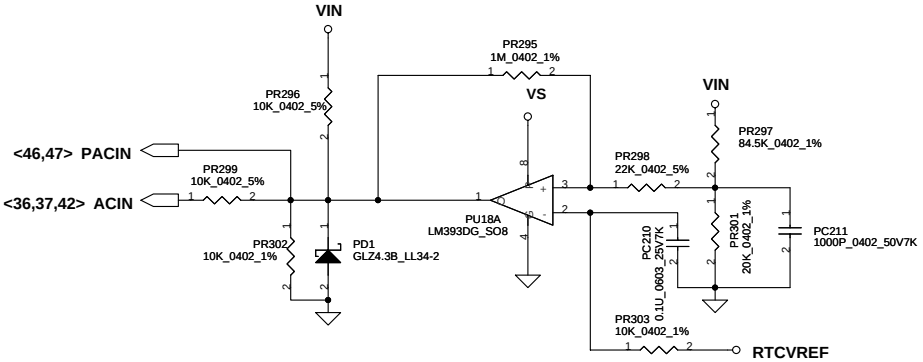
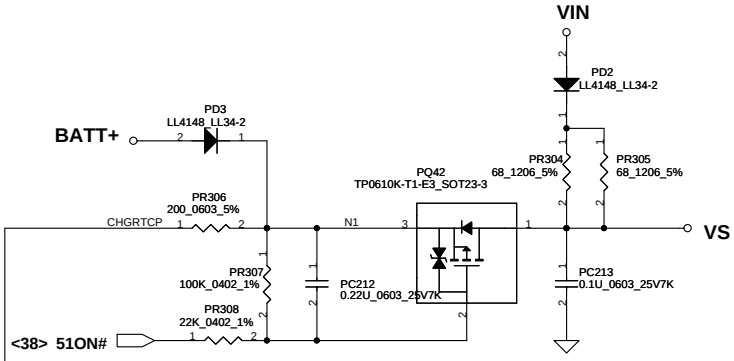
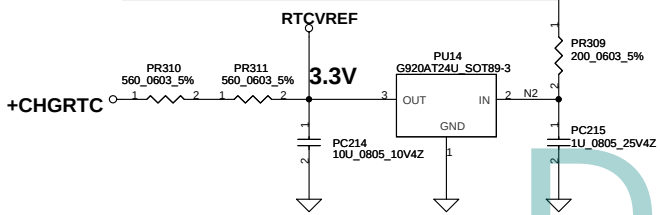


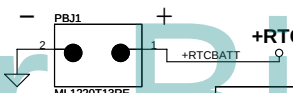


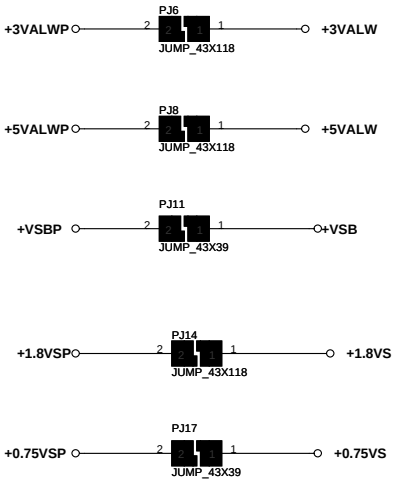
Vin Dectector

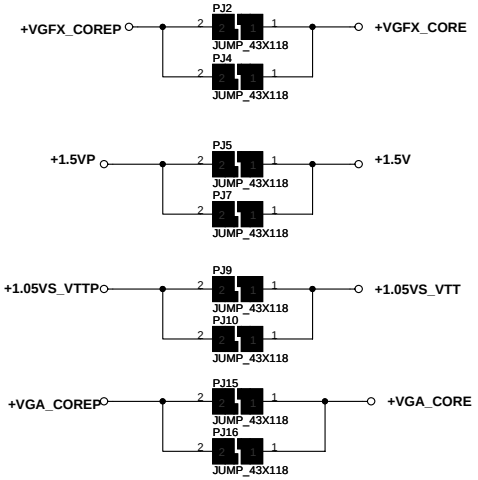
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V











Security Classification	Compal Secret Data		
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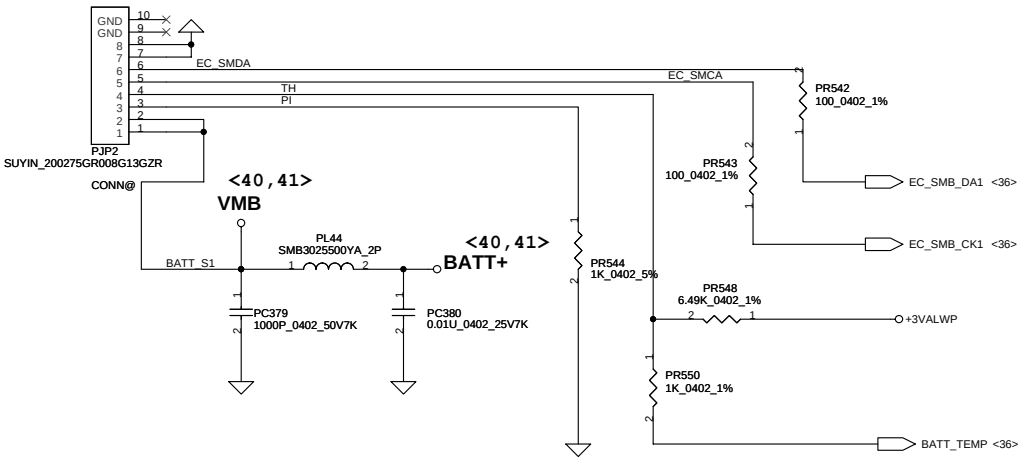
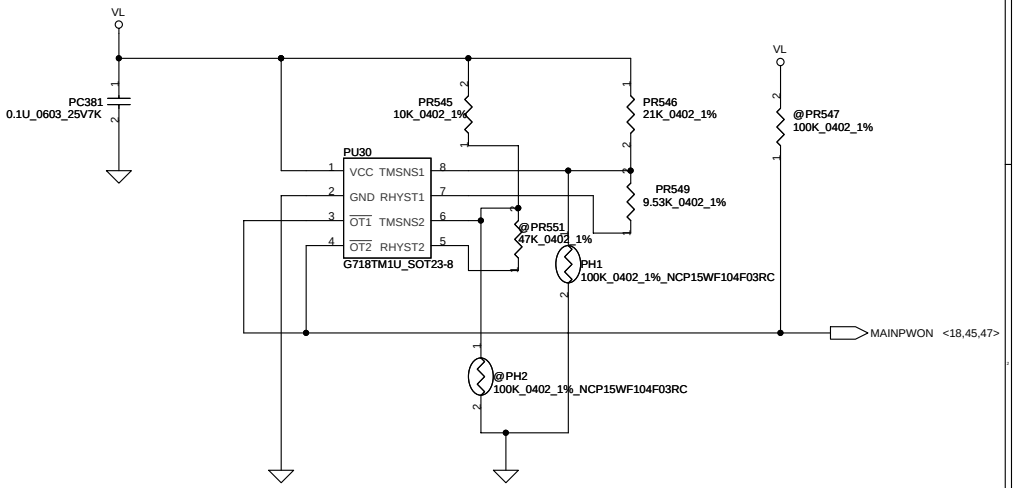
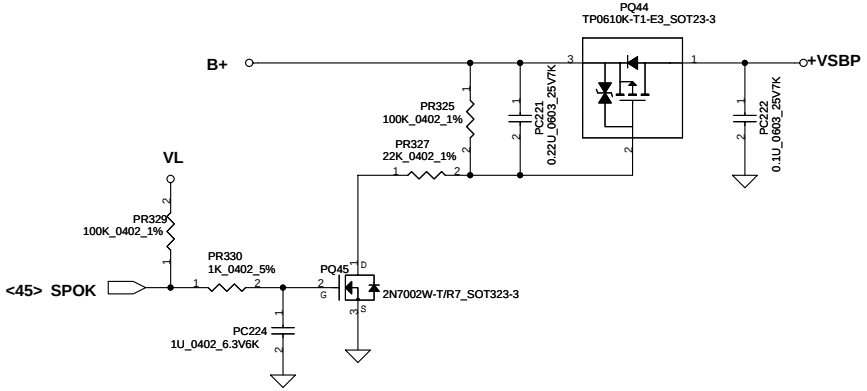


PH1 under CPU botten side :

CPU thermal protection at 92 degree C





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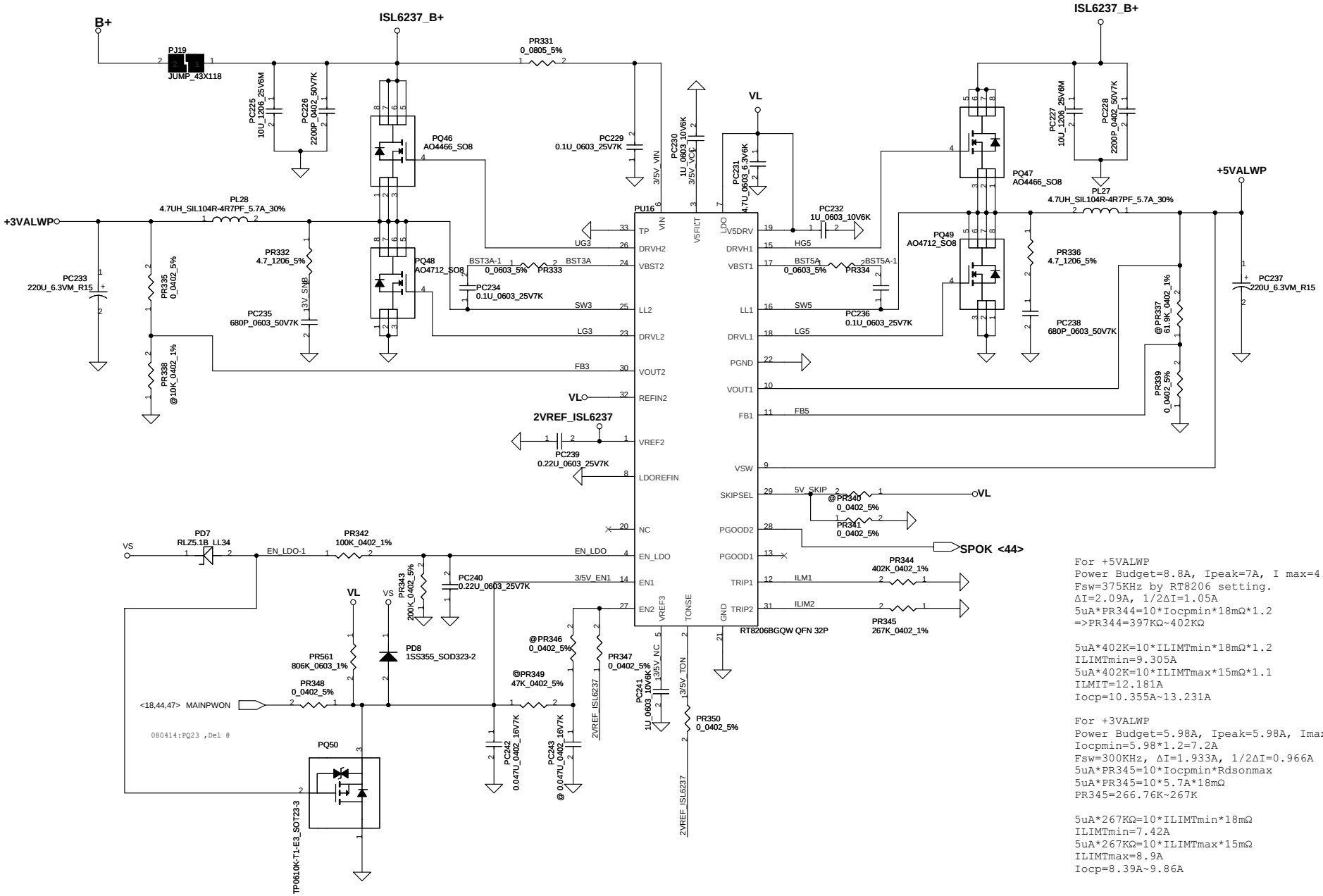

For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=375KHz by RT8206 setting.
ΔI=2.09A, 1/2ΔI=1.05A
5uA*PR344=10*Iocpmin*18mΩ*1.2
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.2
ILIMTmin=9.305A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=10.355A~13.231A

For +3VALWP
Power Budget=5.98A, Ipeak=5.98A, Imax=4.2A
Iocpmin=5.98*1.2=7.2A
Fsw=300KHz, ΔI=1.933A, 1/2ΔI=0.966A
5uA*PR345=10*Iocpmin*Rdsonmax
5uA*PR345=10*5.7A*18mΩ
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ
ILIMTmin=7.42A
5uA*267KΩ=10*ILIMTmax*15mΩ
ILIMTmax=8.9A
Iocp=8.39A~9.86A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

Compal Electronics, Inc.

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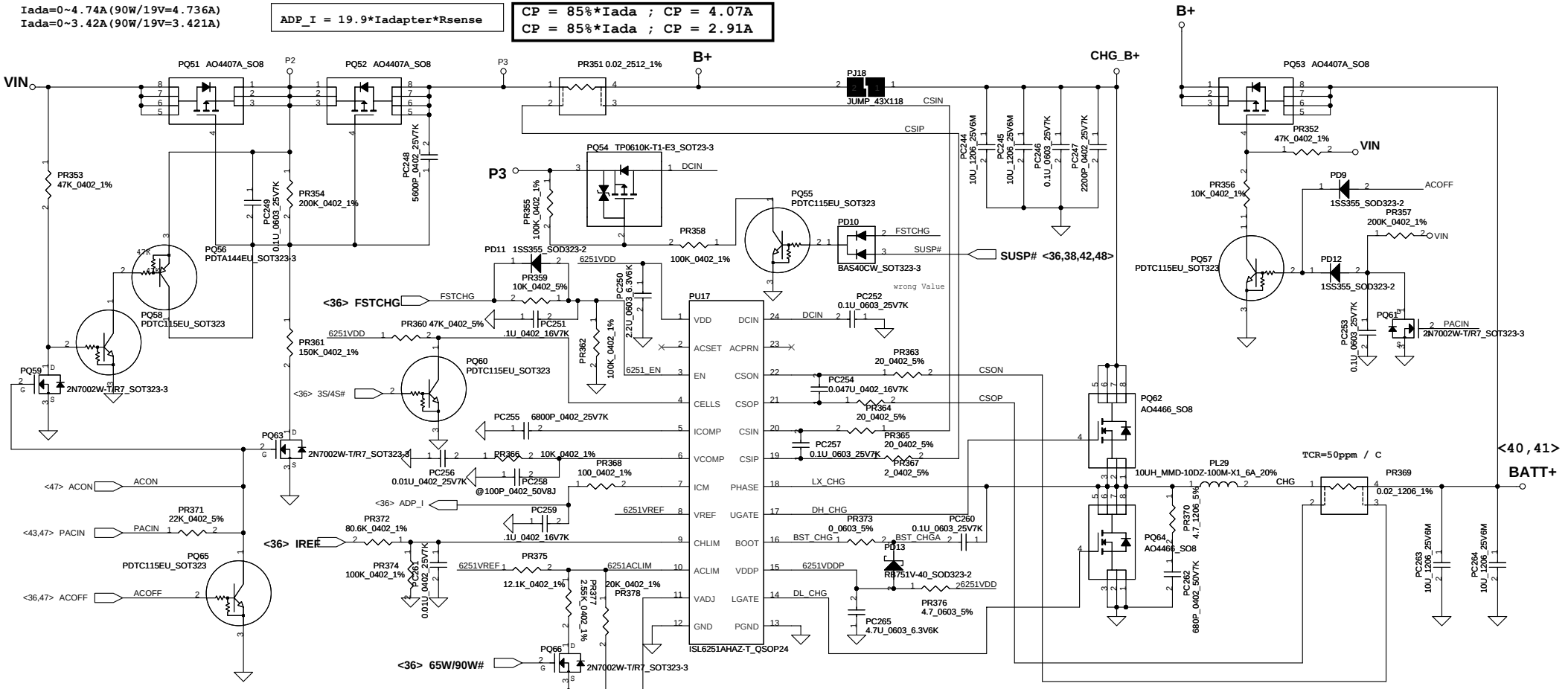
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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Compal Electronics, Inc.

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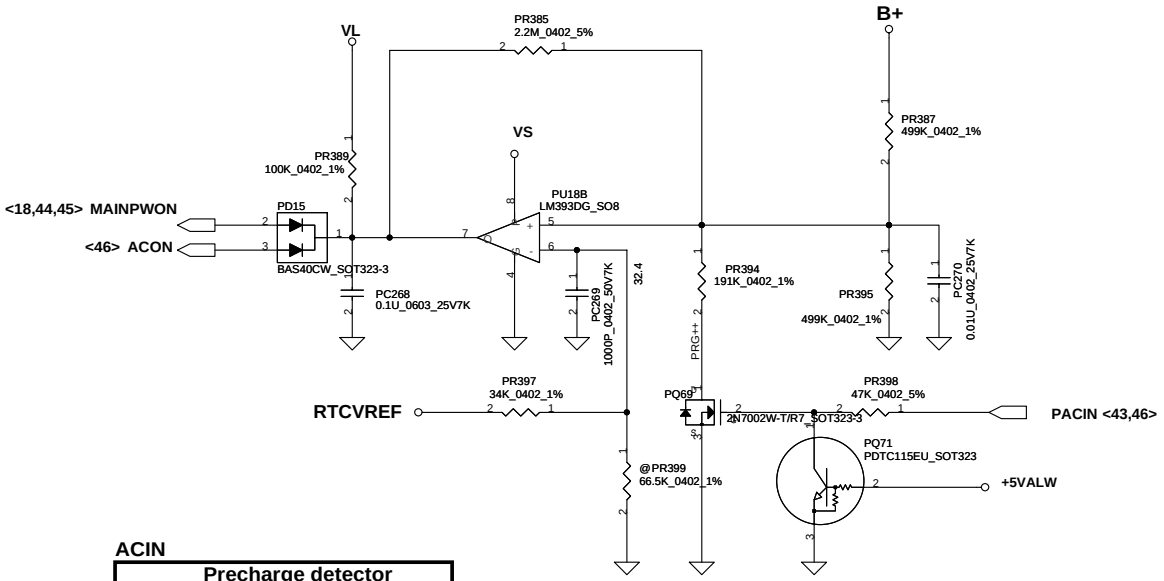

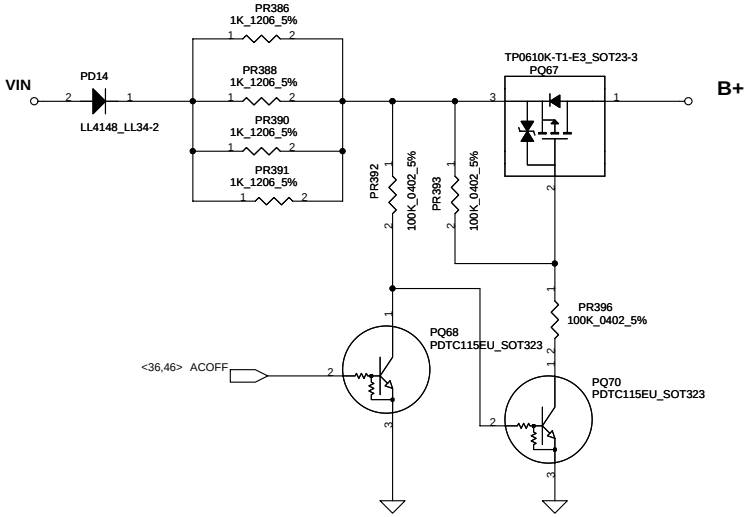

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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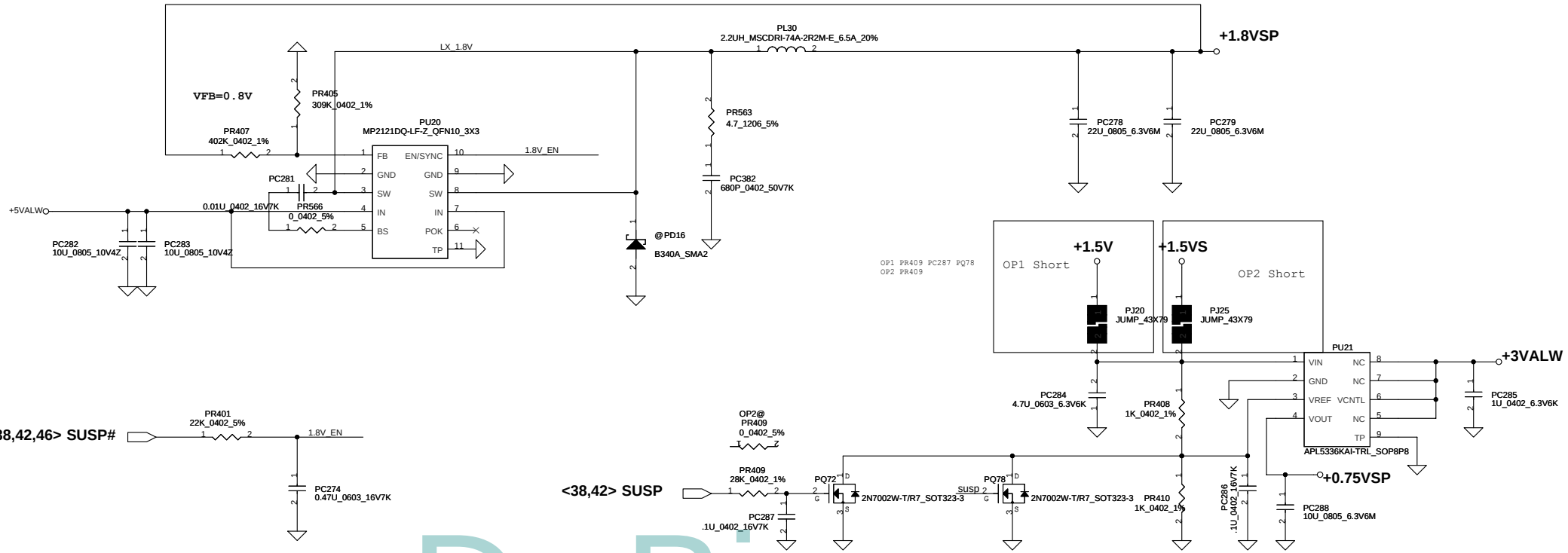

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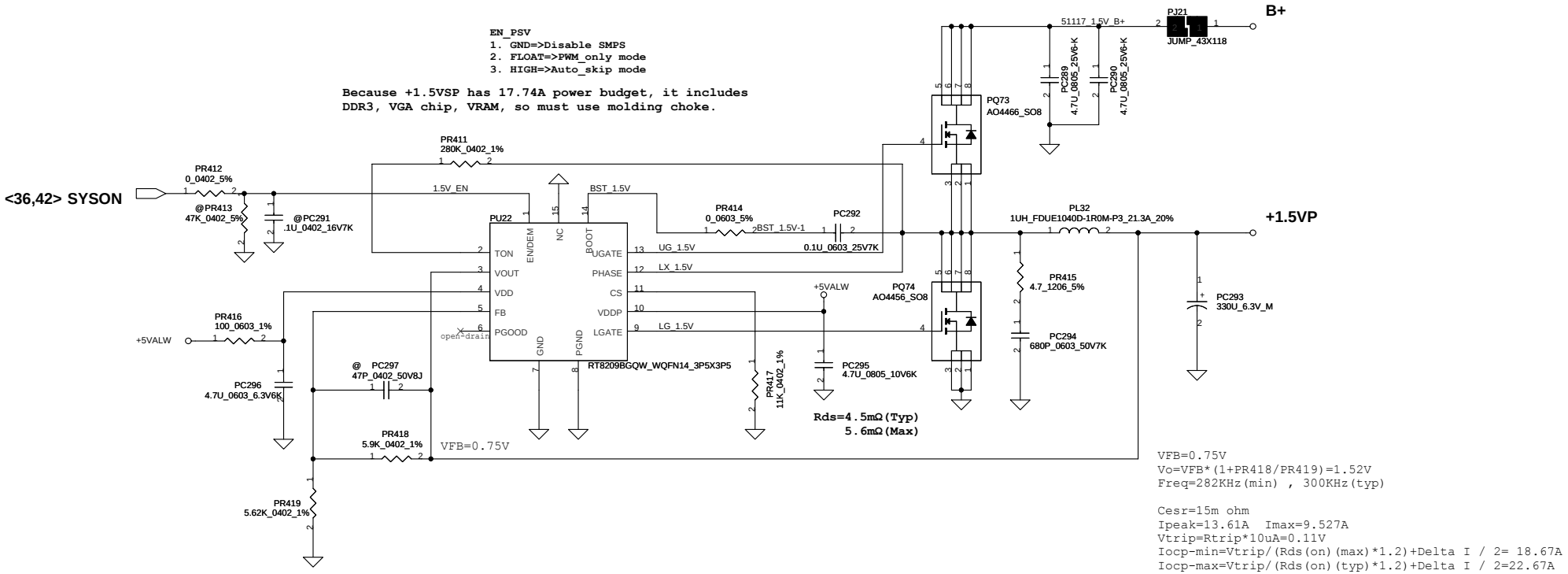

VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=13.61A Imax=9.527A
Vtrip=Rtrip*10uA=0.11V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 18.67A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=22.67A
Iocpmin=18.67A
ΔI=((19-1.5)*(1.5/19))/(L*Freq)=4.605A
1/2ΔI=2.3A

Iocp=18.67A~22.67A

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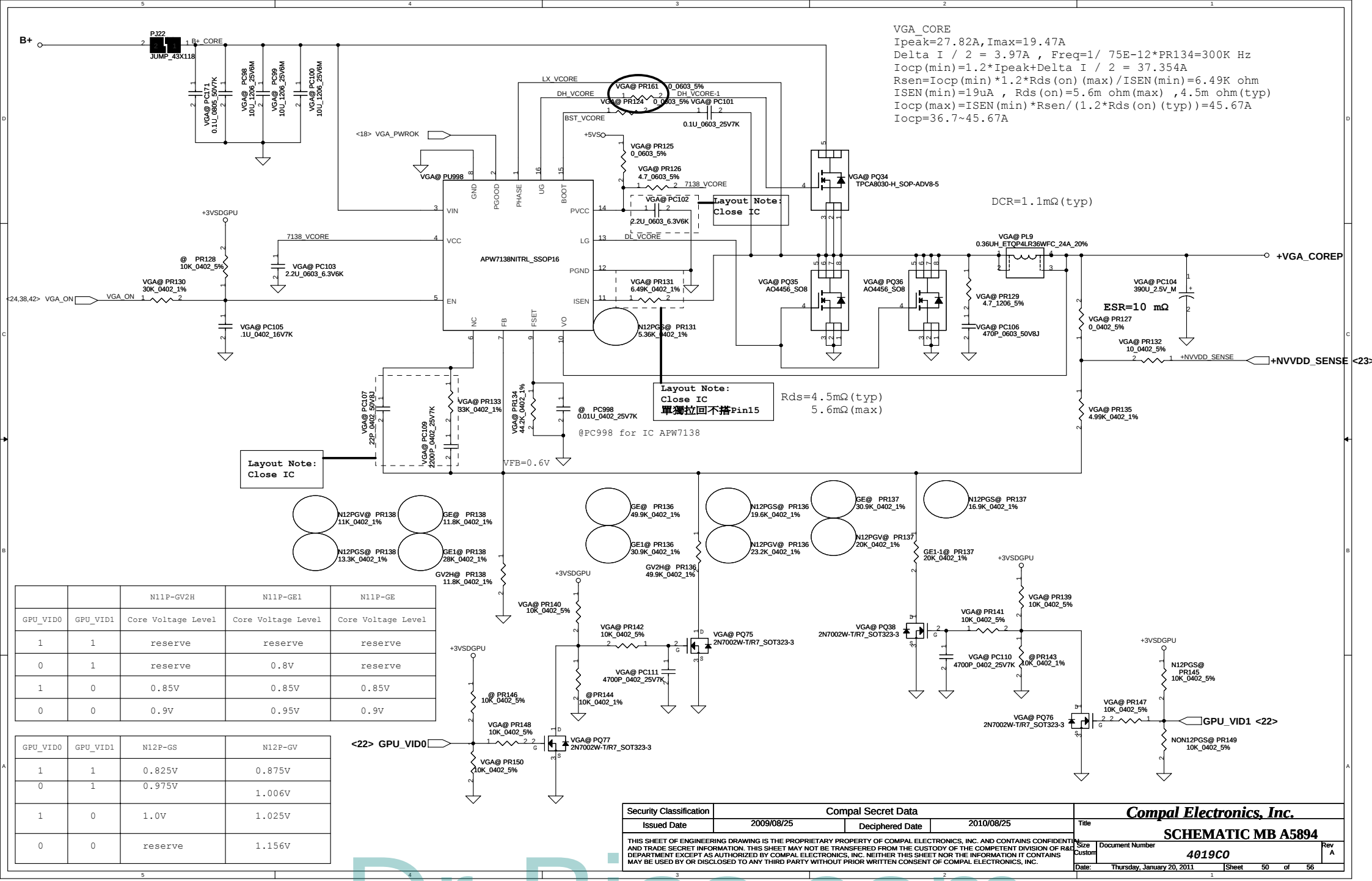

		N11P-GV2H	N11P-GE1	N11P-GE
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	reserve	reserve	reserve
0	1	reserve	0.8V	reserve
1	0	0.85V	0.85V	0.85V
0	0	0.9V	0.95V	0.9V

GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
1	1	0.825V	0.875V
0	1	0.975V	1.006V
1	0	1.0V	1.025V
0	0	reserve	1.156V

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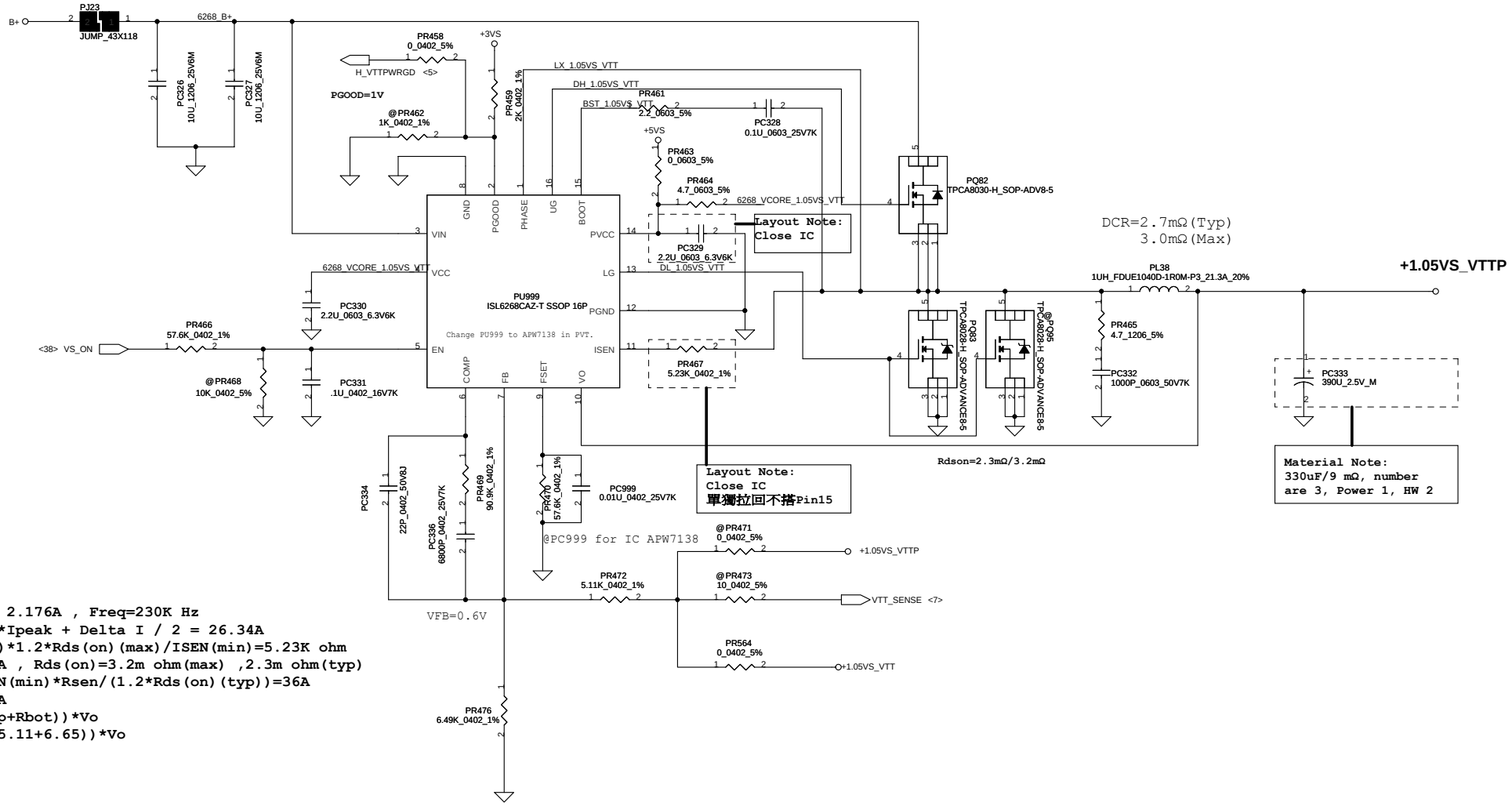

+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V

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Issued Date	2009/4/15	Deciphered Date	2010/08/01

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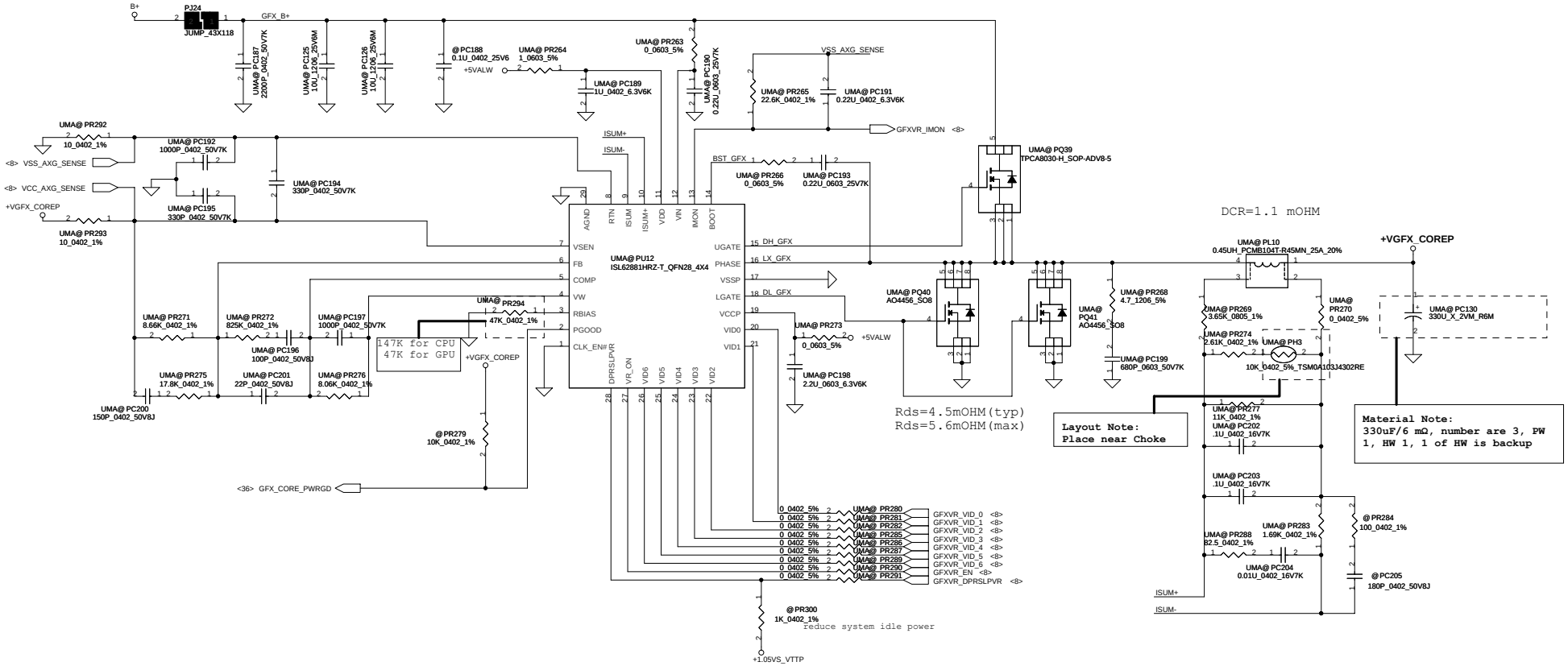
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



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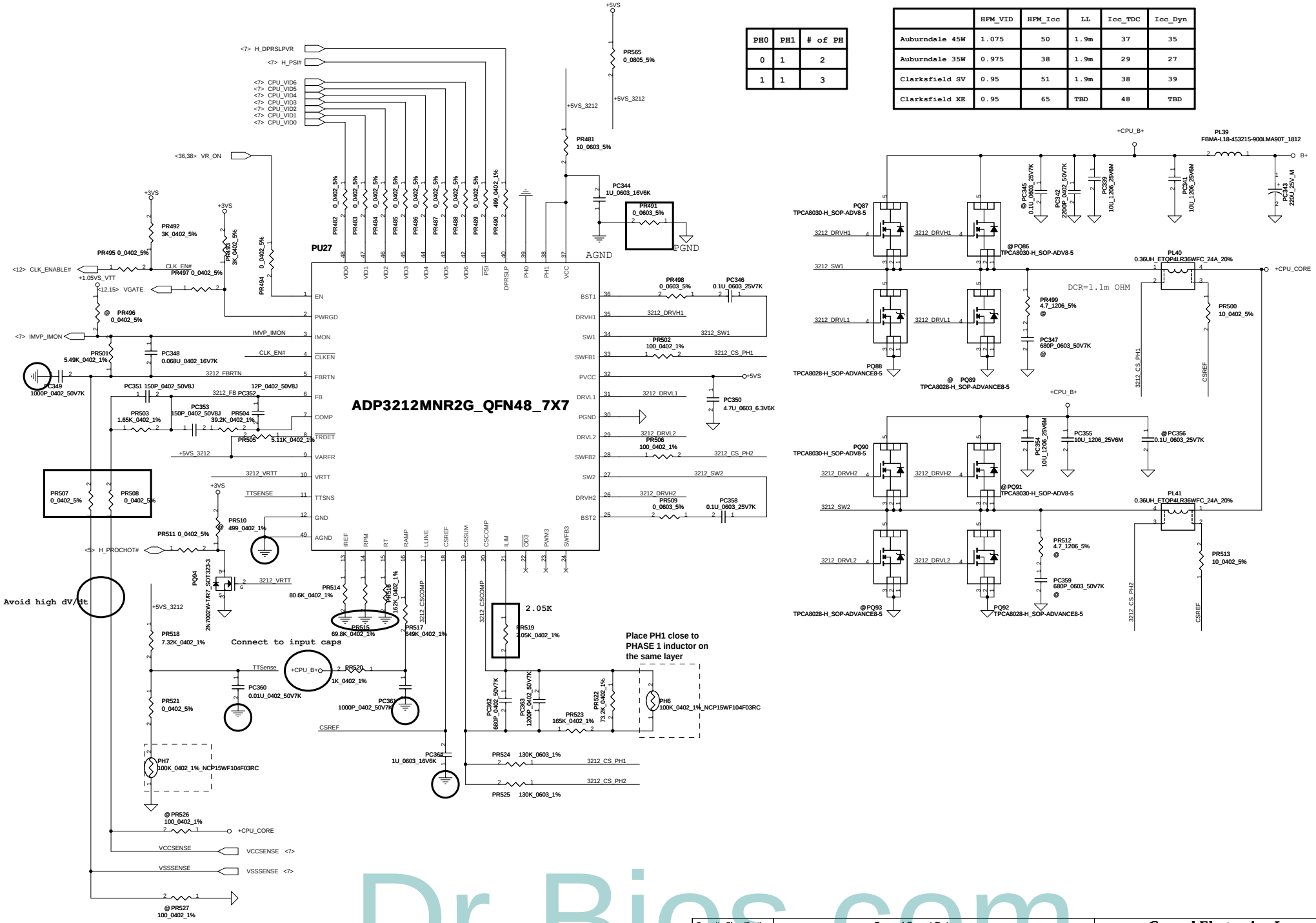
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify VGA_COREP circuit	update VGA_COREP Vout by NV spec.	0.1	50	change PR136 from SD034604280 to SD034499280. Delete PR137 SD034309280. Change PR138 SD034147280 to SD034118280.	2010-0615	PVT
2							
3	Modify VGA_COREP circuit	Modify N12PGS to let Vboot=0.975V, that is VID0=0, VID1=1	0.2	50	Add PR145 SD028100280. delete PR149 SD028100280.	2010-1102	MP
4	Modify +1.5VP circuit	Because run 3Dmark has voltage too low, increase 1.5V.	0.2	49	Change PR419 from SD034576180 to SD034562180. Only for N12PGS.	2010-1102	MP
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

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A -->Modify item

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20091214 Modify For N11P-GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung :SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K
20100113 Modify For N11P-GE1	**strap0**	**strap1**	**strap2**	**ROM_SI**	**ROM_SO**	**ROM_SCLK**
64MX16 Samsung:SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K
20100601 Modify For N11P-GE	**strap0**	**strap1**	**strap2**	**ROM_SI**	**ROM_SO**	**ROM_SCLK**
64MX16 Samsung:SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K
64MX16 Hynix:SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K
128MX16 Samsung:SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K
128MX16 Hynix:SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K

20100909 Modify For N12P-GS VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (800) Samsung:SA000035720	H 45K	H 35K	L 25K	NC	NC	L 10K	L 10K	H 15K
64MX16 (800) Hynix:SA000032490	H 45K	H 35K	L 25K	NC	NC	L 5K	L 10K	H 15K
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 25K	NC	NC	L 20K	L 10K	H 15K
64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 25K	NC	NC	L 15K	L 10K	H 15K
128MX16 (800) Samsung:SA00003MQ40	H 45K	H 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (800) Hynix:SA00003VS10	H 45K	H 35K	L 25K	NC	NC	L 35K	L 10K	H 15K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 25K	NC	NC	L 35K	L 10K	H 15K

20101220 Modify For N12P-GV VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	H 10K	H 5K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	H 10K	H 5K
128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 5K	L 5K	L 10K	L 35K	H 10K	H 5K

ROM_SI，爲Vram配打電阻

BOM Config		
PEW71 SKU N11P-GE 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL21
PEW71 SKU N11P-GV2H-A3 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869BOL22
PEW51 SKU N11P-GV2H-A3 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869BOL31 *沒打
PEW51 SKU N11P-GE 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL32
PEW51 SKU N11P-GE 2G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL33 *沒打
PEW71 SKU N11P-GE 1G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7621@,GE@	431869BOL23
PEW71 SKU N11P-GE 2G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7601@,GE@	431869BOL24
PEW71/91 SKU N12P-GS 1G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7621@,GS@	431869BOL26
PEW71/91 SKU N12P-GS 2G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7601@,GS@	431869BOL27
PEW51 SKU N12P-GS 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GS@,NonOPT@	431869BOL34

以上爲LA5893PR10, Footprint:GB1-128

SMT MB A5894 PEW71 GS OPT 1G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GS@	4319COBOL01
SMT MB A5894 PEW71 GS OPT 2G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GS@	4319COBOL02
SMT MB A5894 PEW71 GV OPT 512M WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GV@	4319COBOL03
SMT MB A5894 PEW71 GV OPT 1G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GV@	4319COBOL04

以上爲LA5894PR10, Footprint:GB2-128 Compability GB2B-128

PCB

ZZZ
LA-5894P REV0 M/B

GV2HA2@ U51
N11P-GV2H-A2_BGA969

GV2HA3@ U51
N11P-GV2H-A3_BGA969

GE1@ U51
N11P-GE1-A3 BGA 969P

GE@ U51
N11P-GE-A1 BGA 969P

GS@ U51
N12P-GS-A1 BGA 973P

GV@ U51
N12P-GV-OP-B-A1 BGA 973P

ZZZ3 X7601@
X76248BOL01
ALT. GROUP PARTS 2G HYN

ZZZ2 X7622@
X76198BOL22
ALT. GROUP PARTS 1G HYN

ZZZ1 X7621@
X76198BOL21
ALT. GROUP PARTS 1G SAM

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