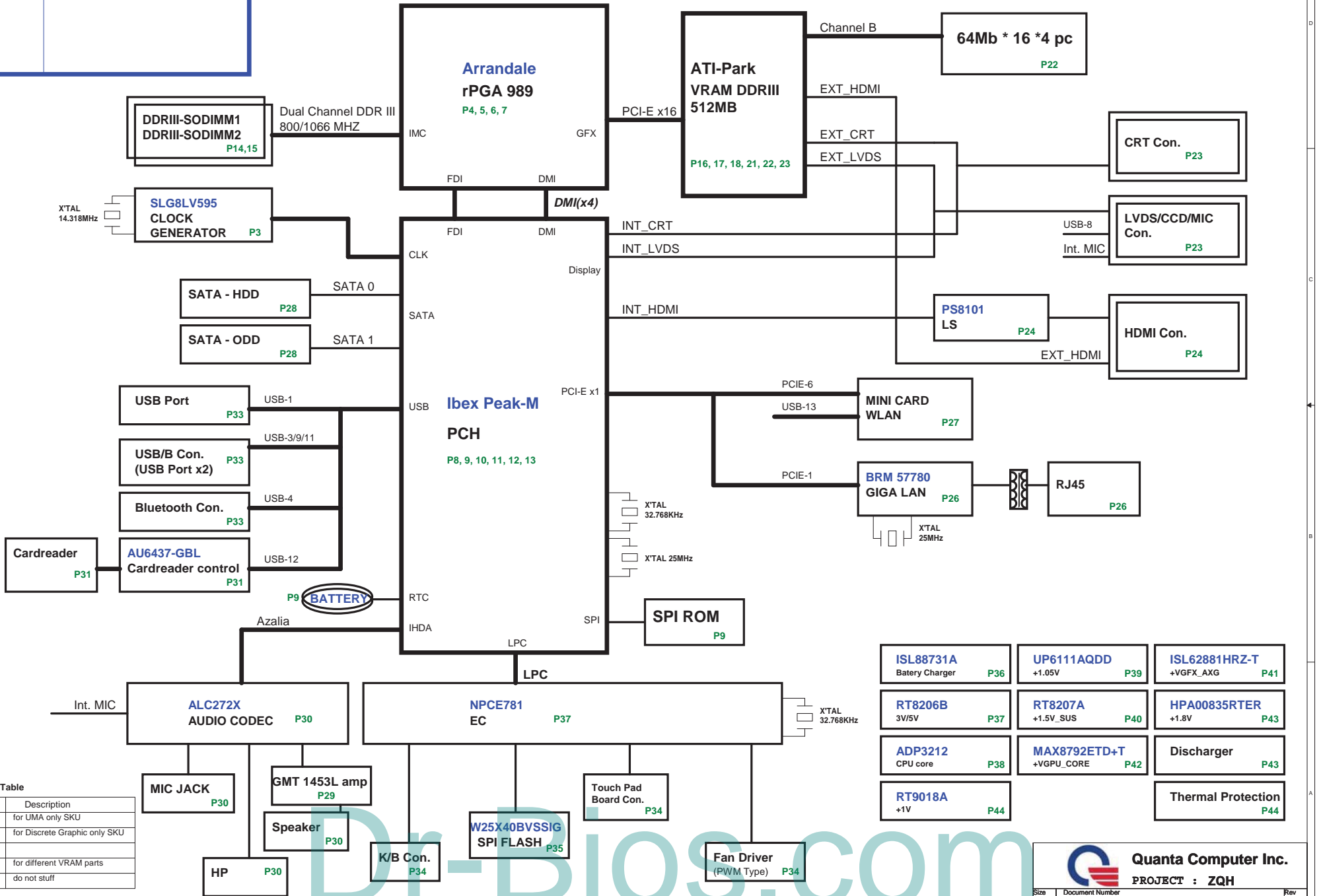


ZQH SYSTEM BLOCK DIAGRAM

BOM P/N	Description



BOM Option Table

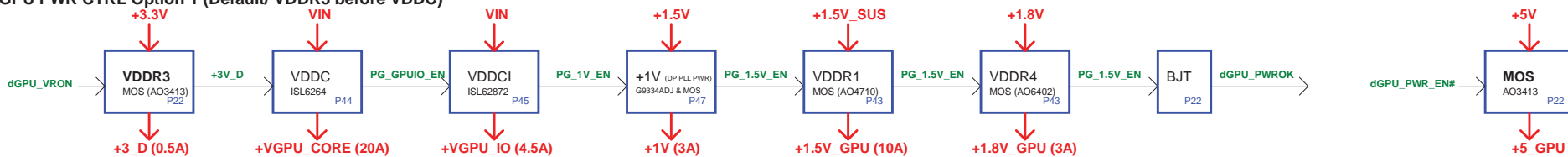
Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

Quanta Computer Inc.
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Block Diagram

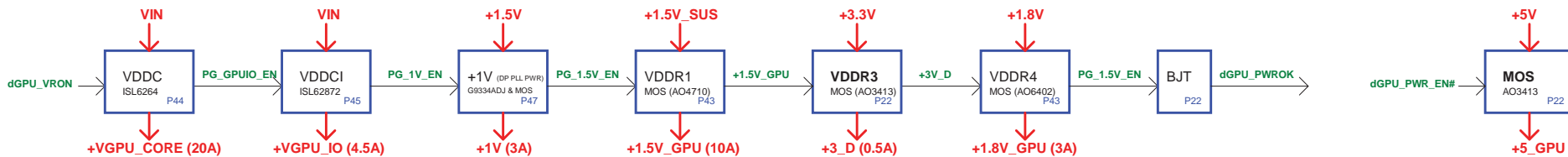
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GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



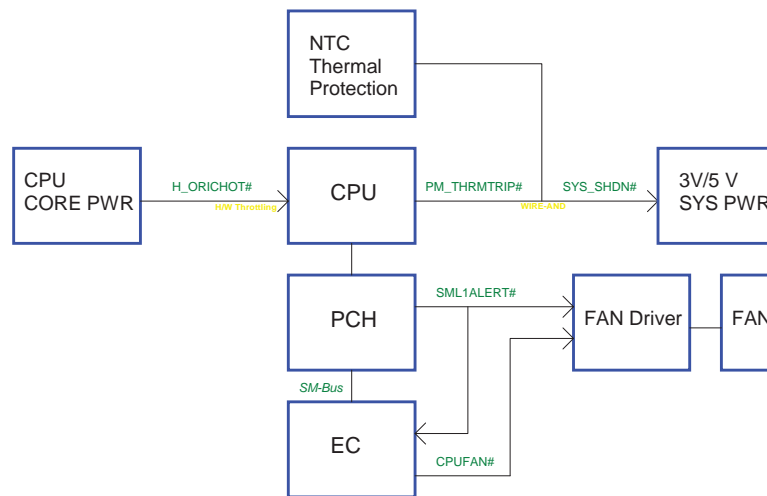
GPU PWR CTRL Option 2 (VDDR3 after VDDC)



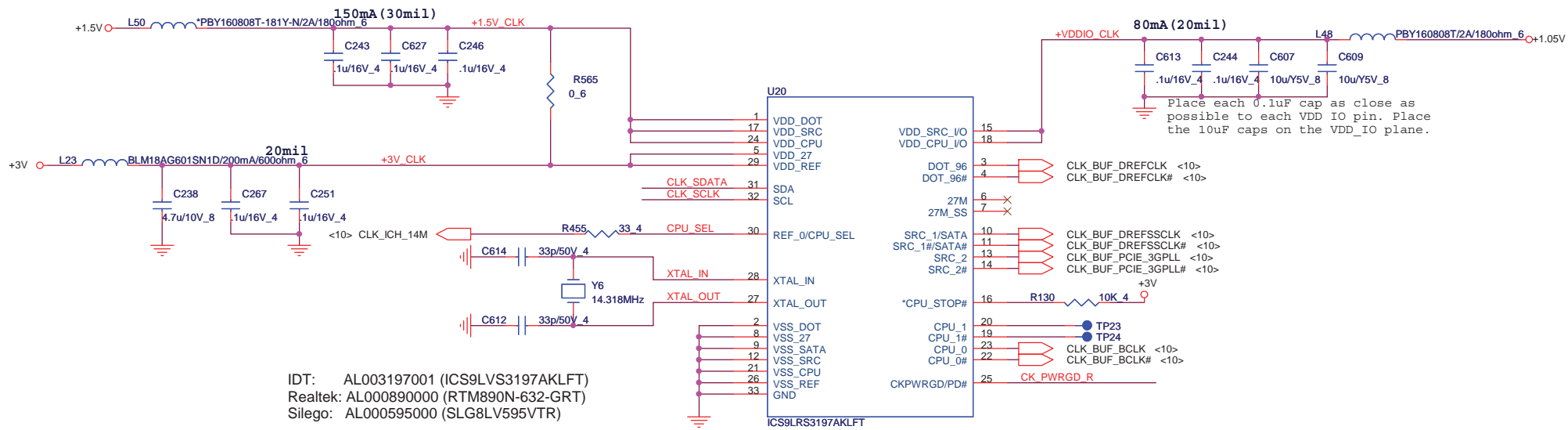
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIQ_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

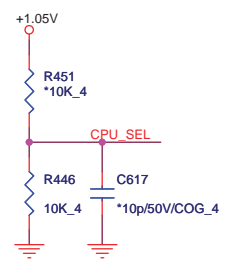
Thermal Follow Chart



Dr-Bios.com

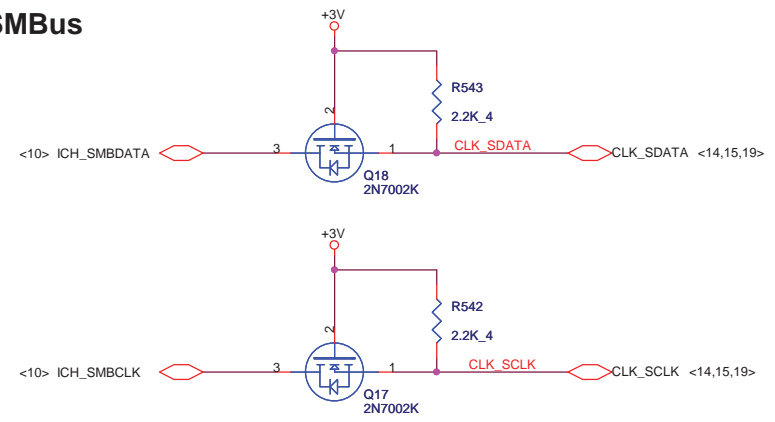


CPU_CLK select

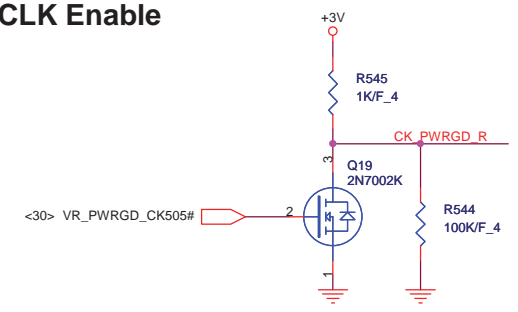



	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

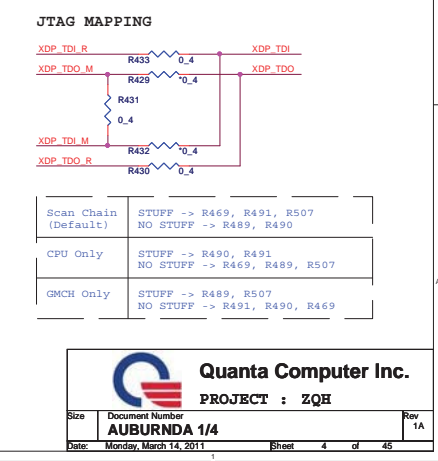
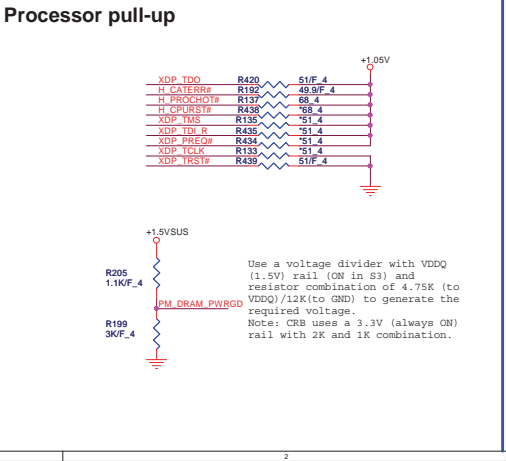
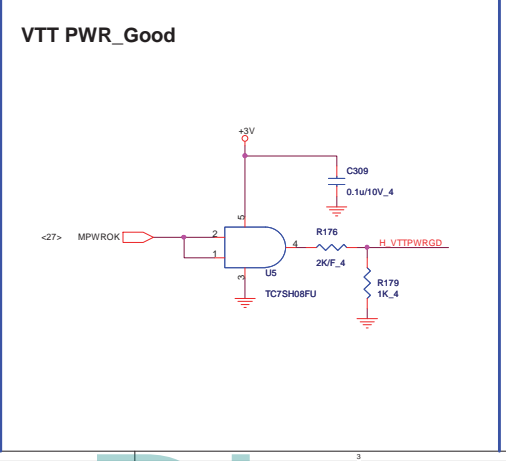
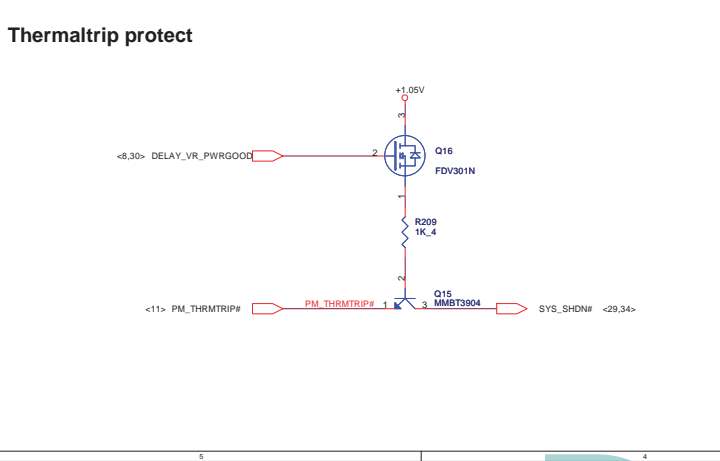
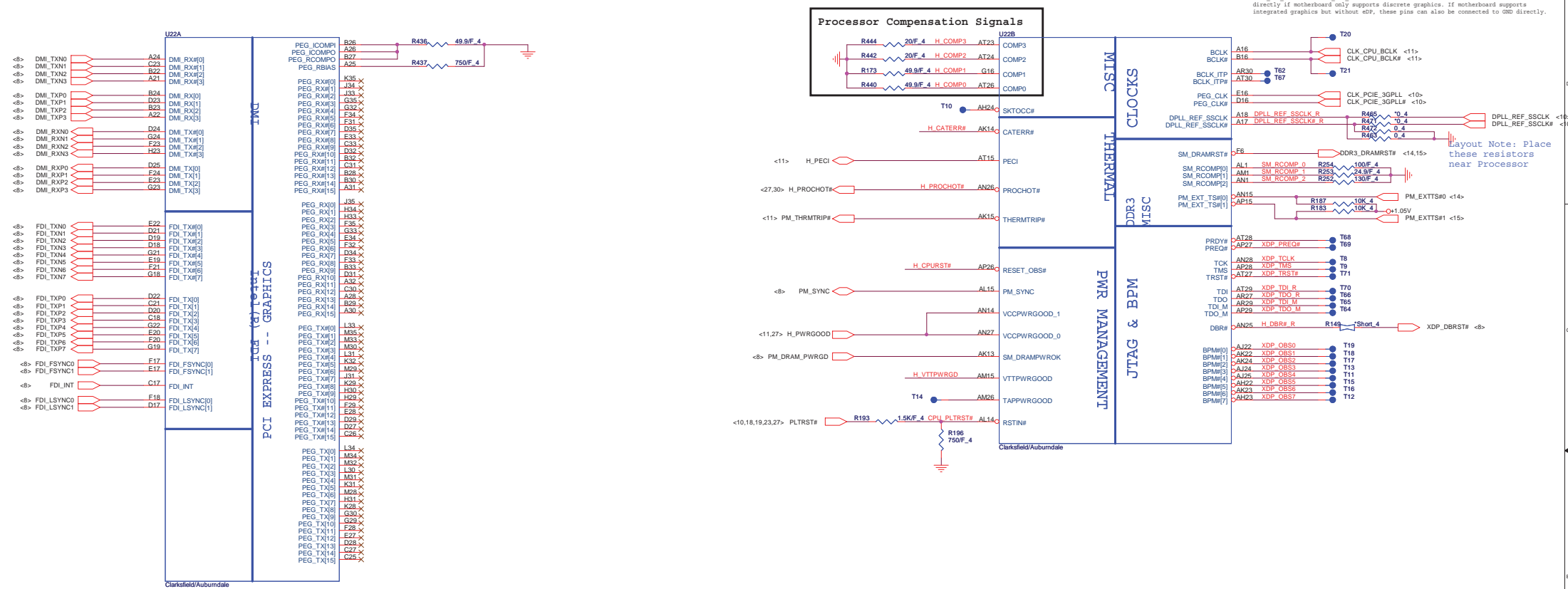


CLK Enable

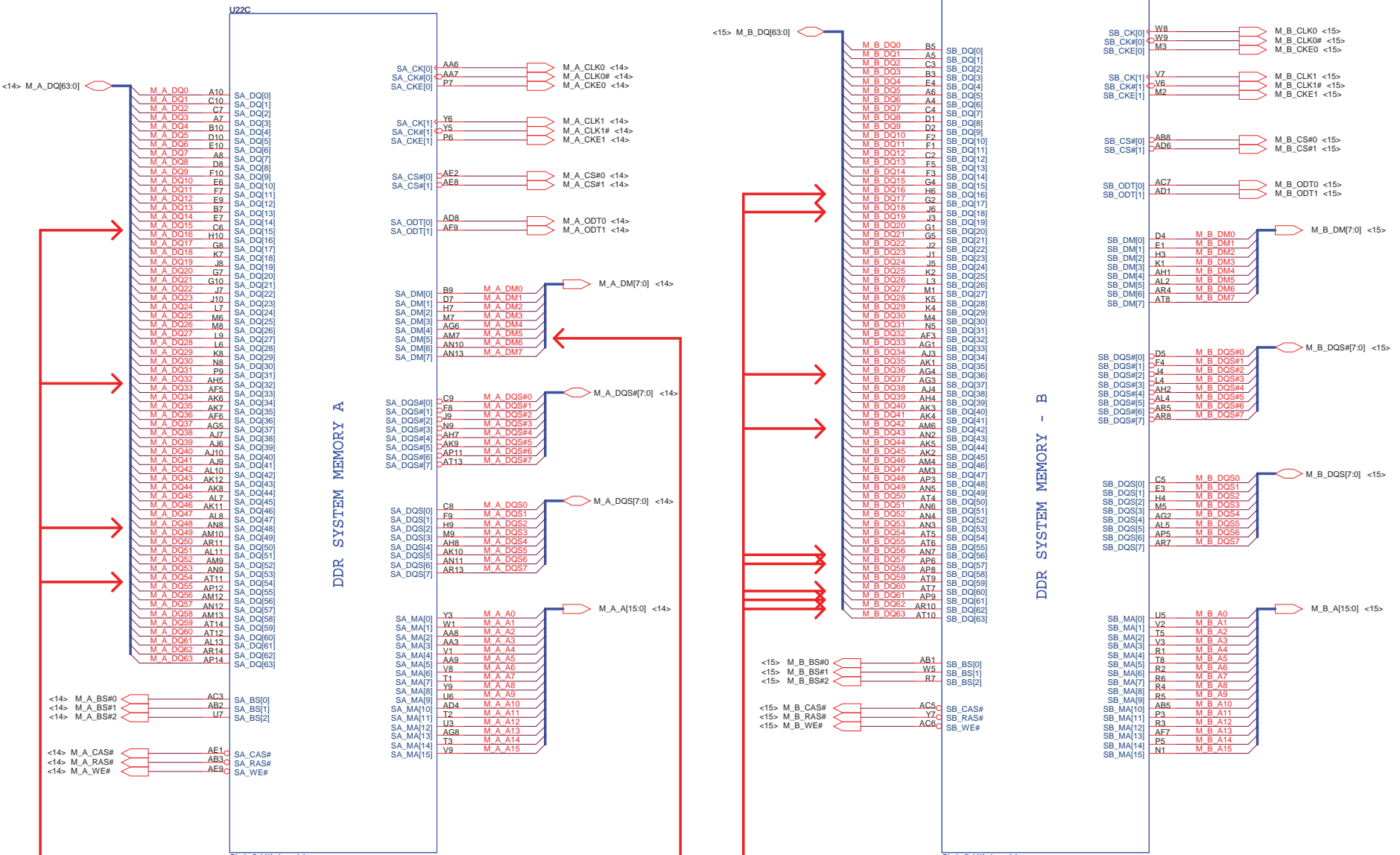



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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

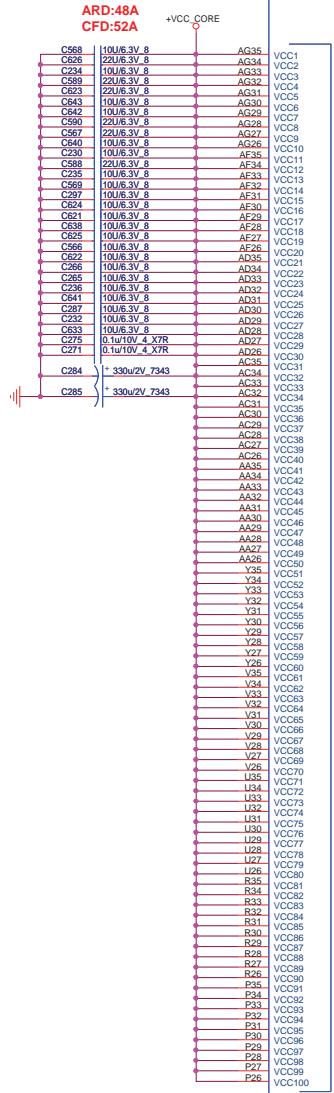


Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



CPU Core Power

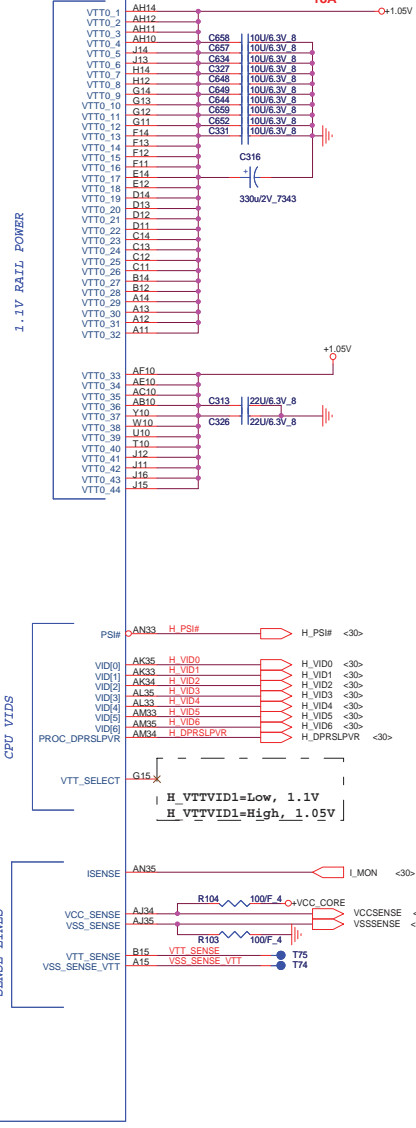


Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

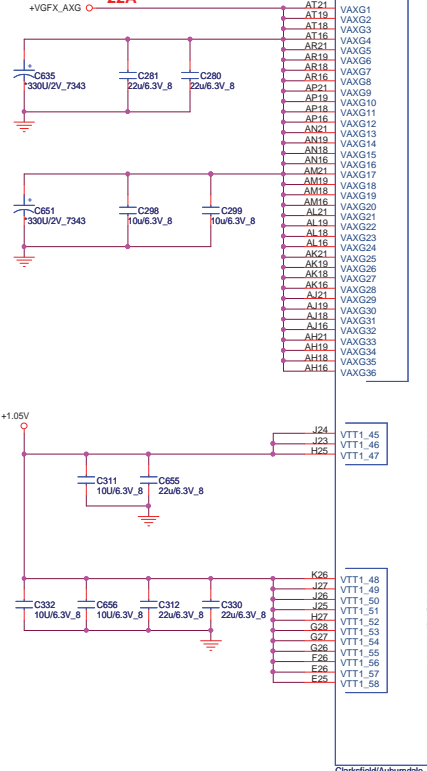
VTT Rail Values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

18A 1.05V

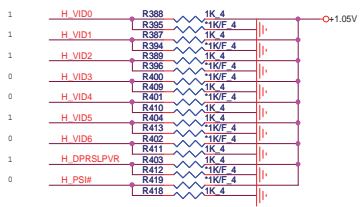


AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

22A

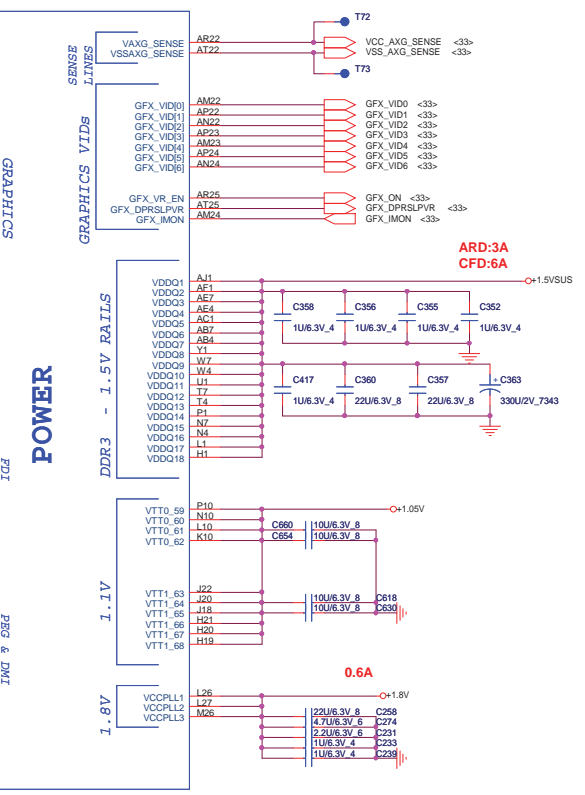


Clarksfield/Auburndale



Note:
For Validating IMVP VR R6451 should be STUFF
and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

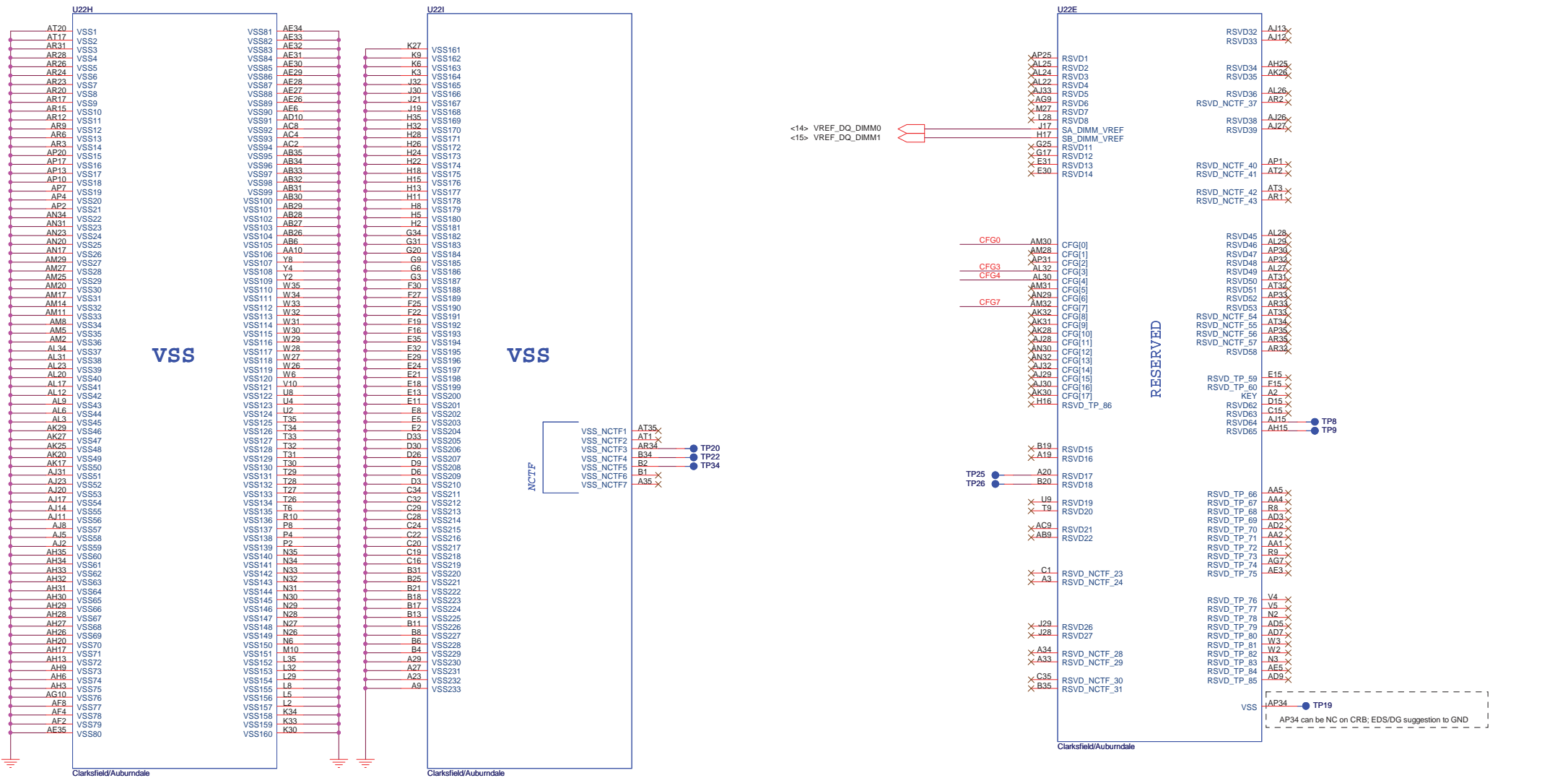


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AUBURNDALE/CLARKSFIELD PROCESSOR (GND)


AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

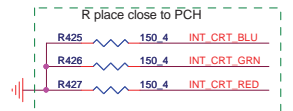
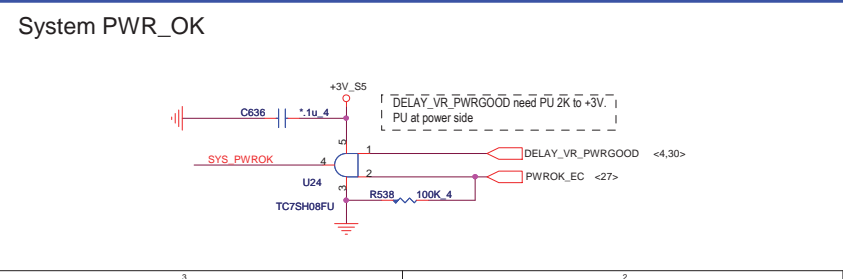
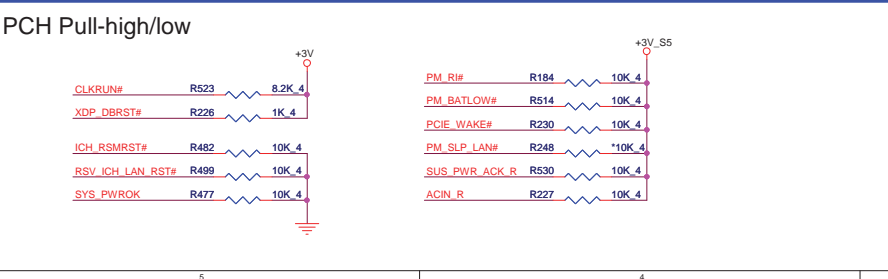
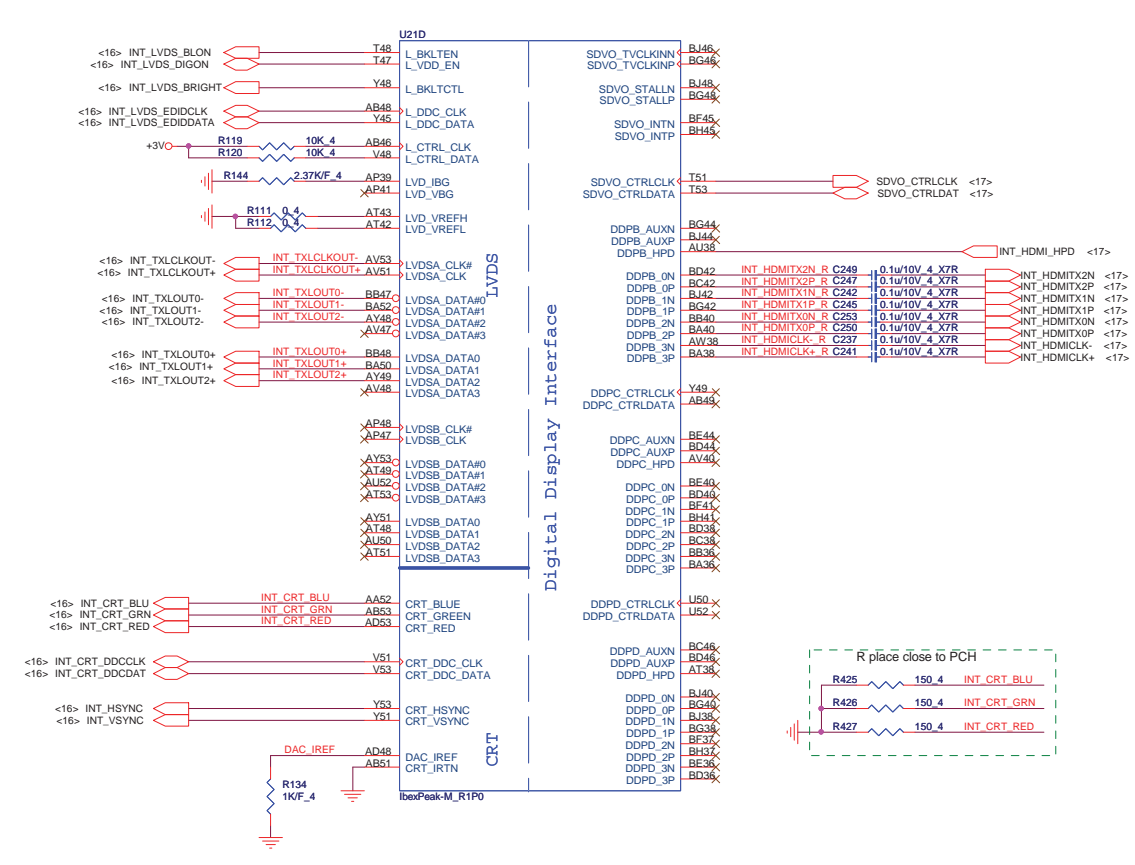
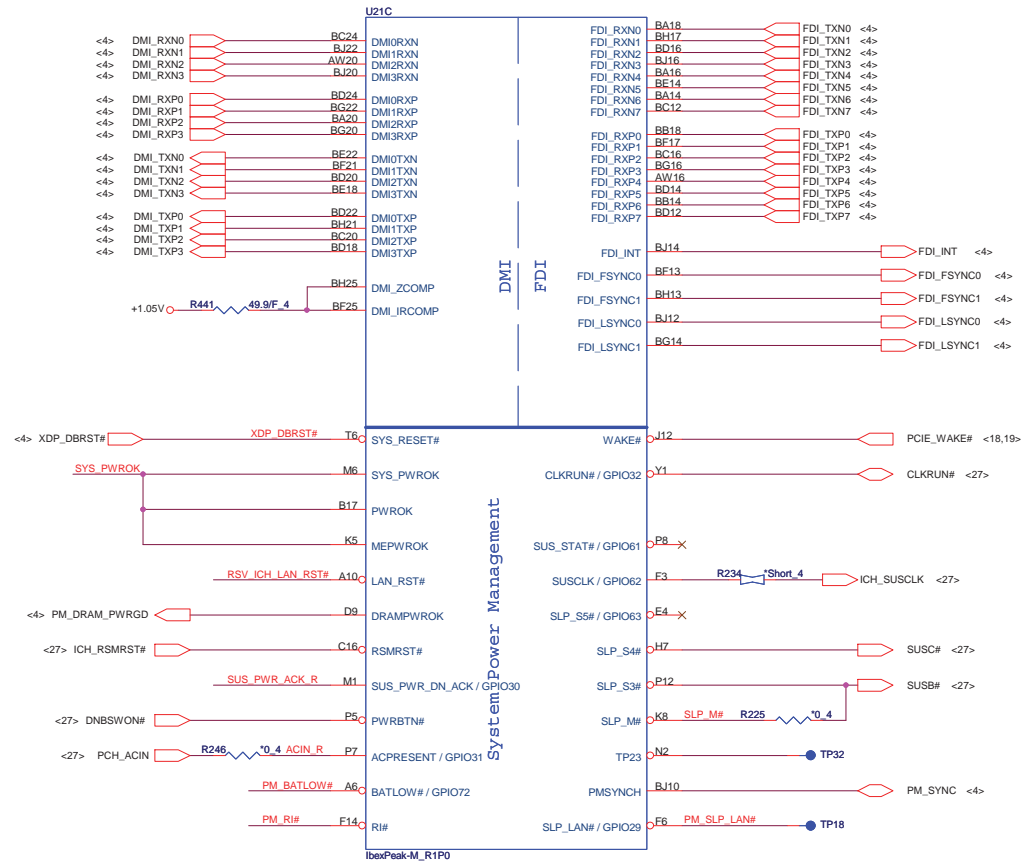


Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 ~3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 ~3.01K_F_4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 ~3.01K
				CFG7 R126 ~3.01K_F_4



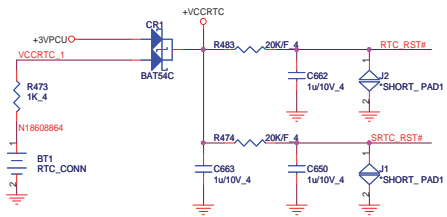

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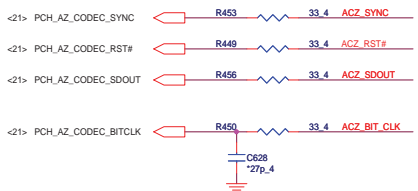
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RTC Circuitry

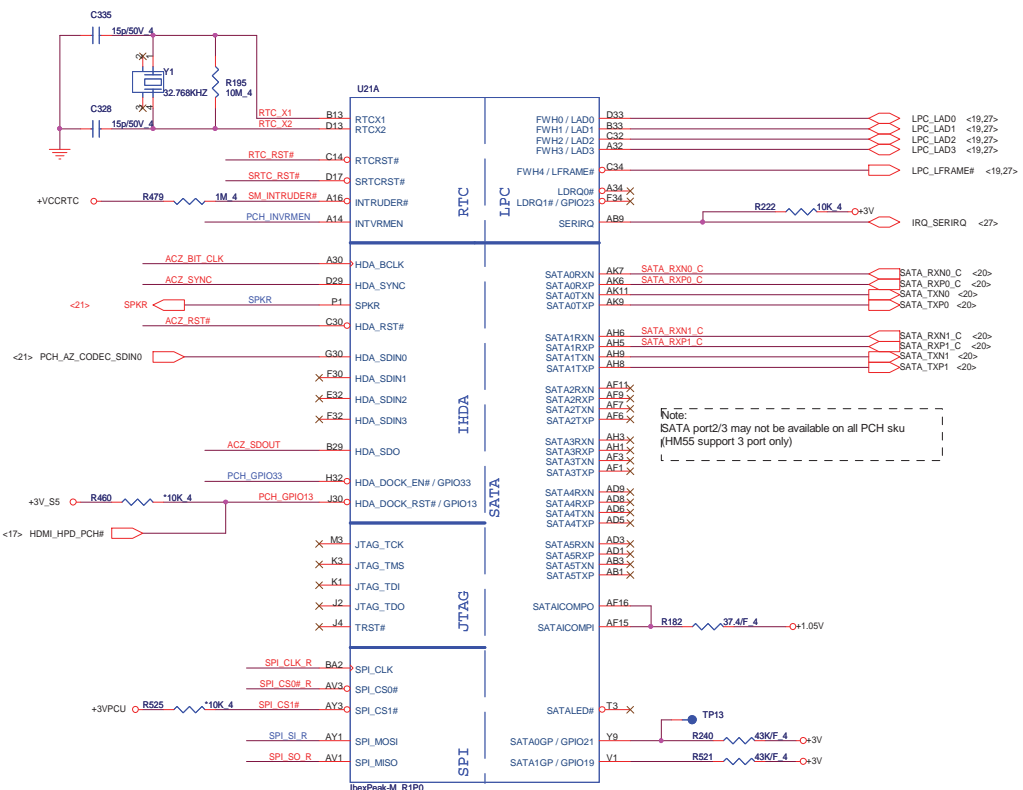
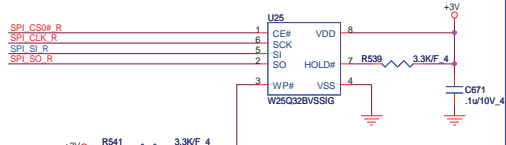


HDA_SYNC (PCH strap pin)
 Internal weak pull-down
 VCCVRM=>+1.8V (default)
 external pull-up
 VCCVRM=>+1.5V

HDA Bus

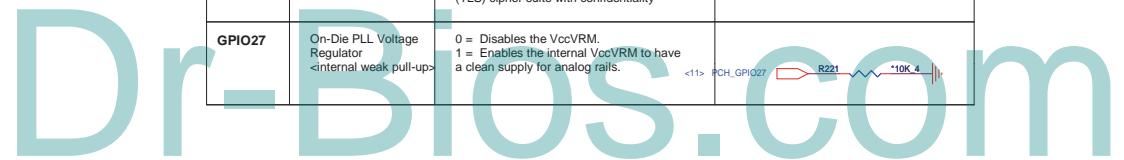


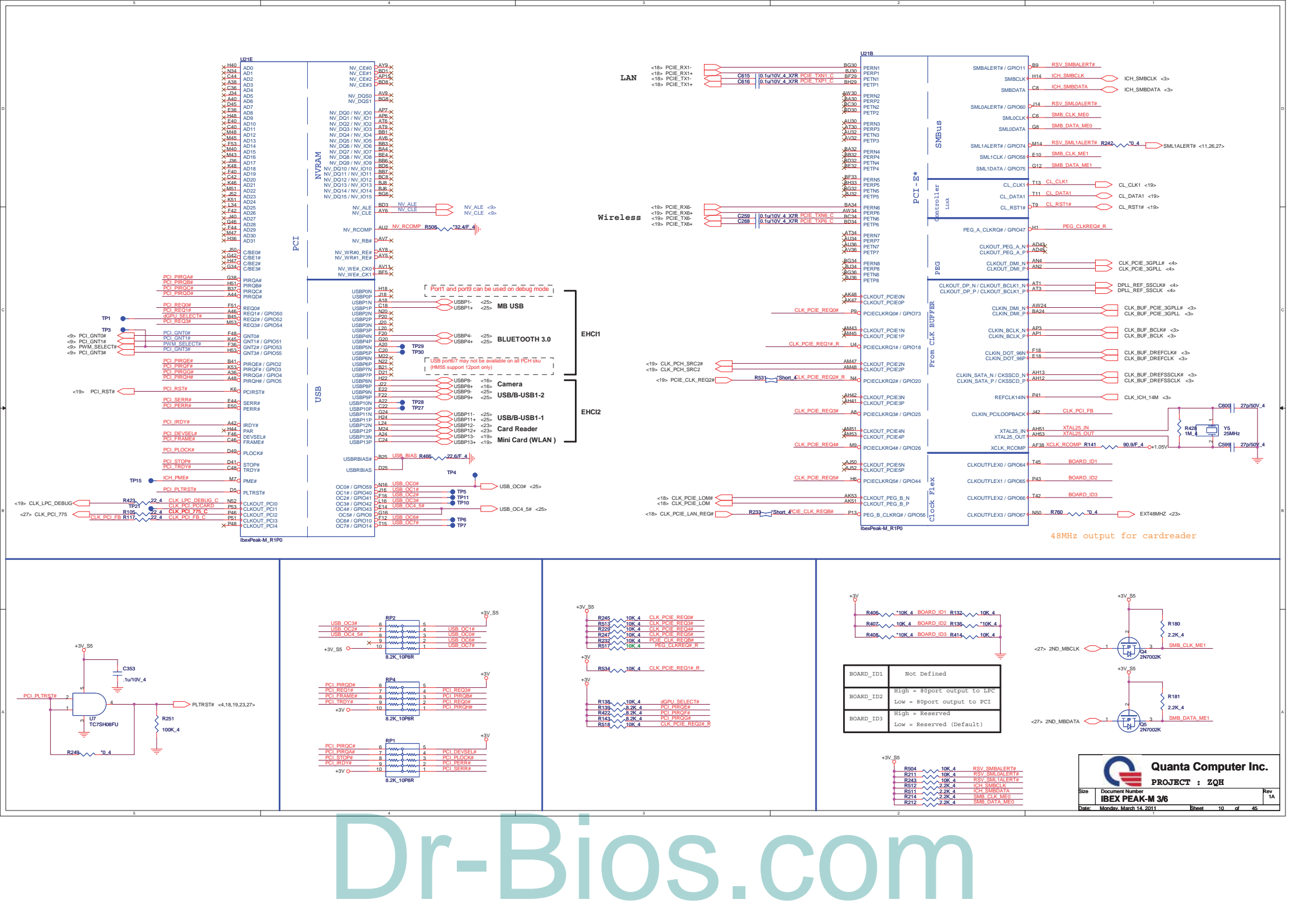
PCH SPI



PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 1K 4 SPKR
HDA_DOCK# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 1K 4 R146 10K 4
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K 4 R122 1K 4 R133 1K 4 R131 1K 4
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 1K 4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 10K 4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 1K 4
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 1K 4
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	SSV_GPIO8 R204 10K 4 R203 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R244 1K 4
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 10K 4





LAN
<18> PCIe_RX1+
<18> PCIe_RX1+
<18> PCIe_TX1+
<18> PCIe_TX1+

Wireless
<18> PCIe_RX6-
<18> PCIe_RX6+
<18> PCIe_TX6-
<18> PCIe_TX6+

EHCI1

EHCI2

U21B

PCI E

Form CLK BUFFER

CLK_PCIE_REQ#

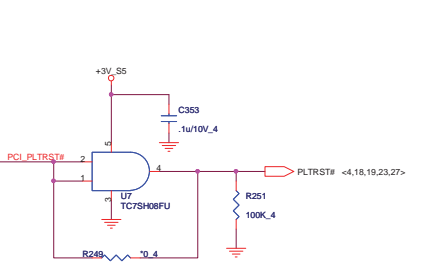
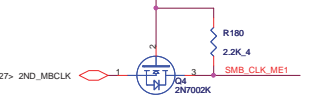
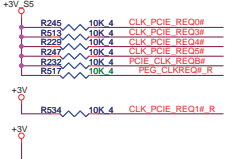
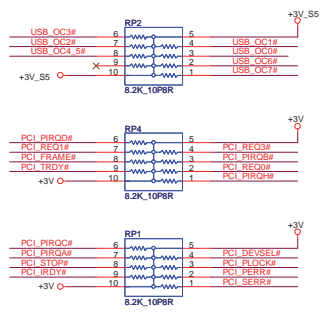
ibexPeak-M_R1P0

48MHz output for cardreader

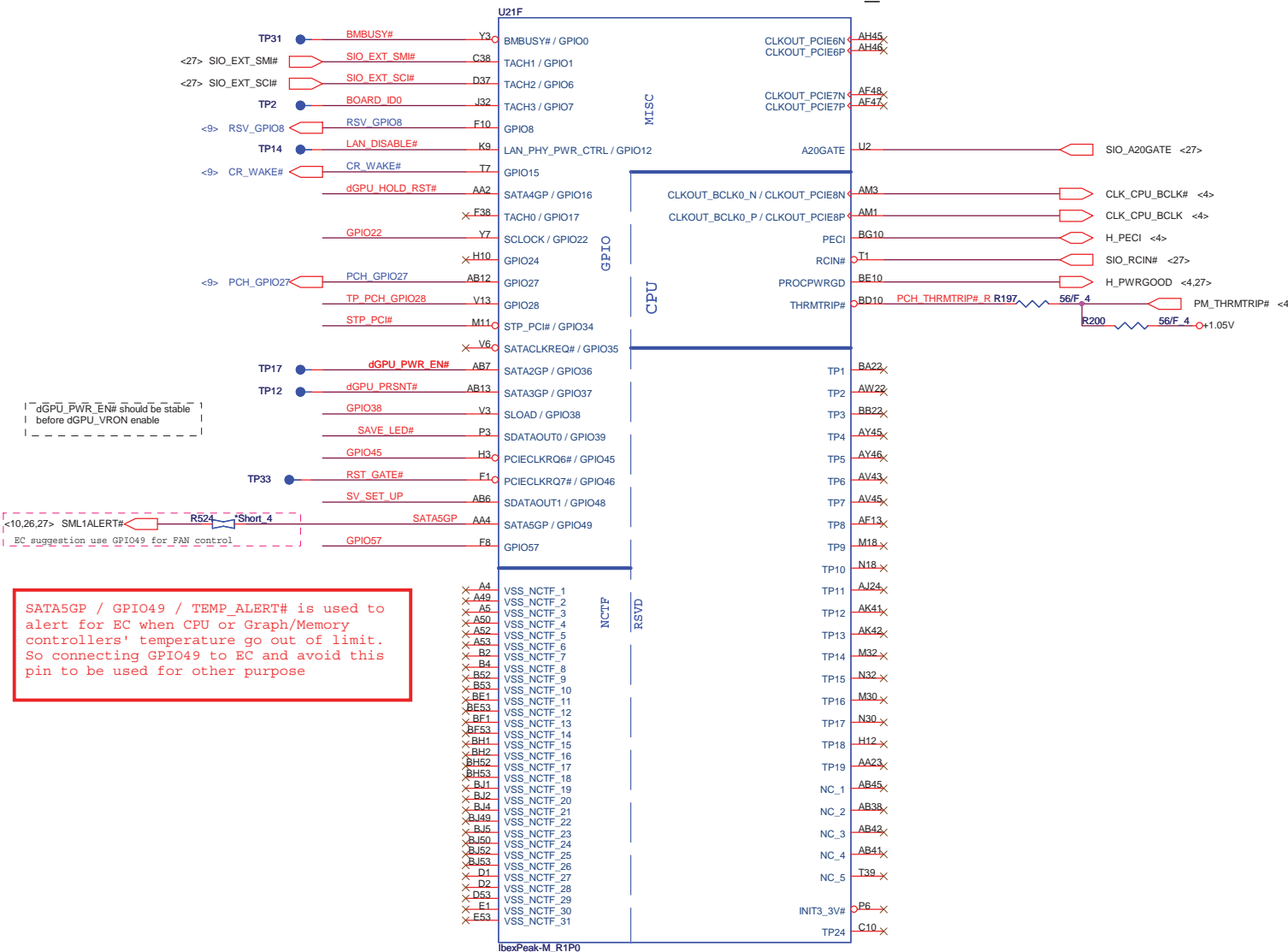
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BOARD_ID1	Not Defined
BOARD_ID2	High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3	High = Reserved Low = Reserved (Default)

R204	10K 4	RSV_SMBALERT#
R211	10K 4	RSV_SMLALERT#
R243	10K 4	RSV_SMLALERT#
R212	2.2K 4	ICH_SMBCLK
R214	2.2K 4	ICH_SMBDATA
R212	2.2K 4	SMB_CLK_MED
R212	2.2K 4	SMB_DATA_MED



IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



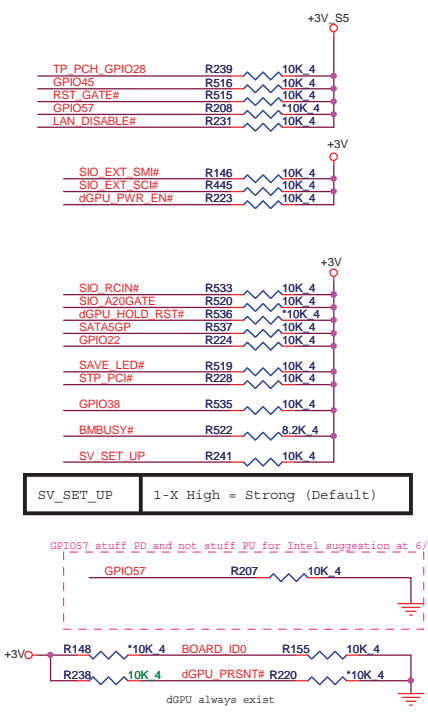
dGPU_PWR_EN# should be stable before dGPU_VRON enable

<10,26,27> SML1ALERT# R524 Short 4
EC suggestion use GPIO49 for FAN control

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

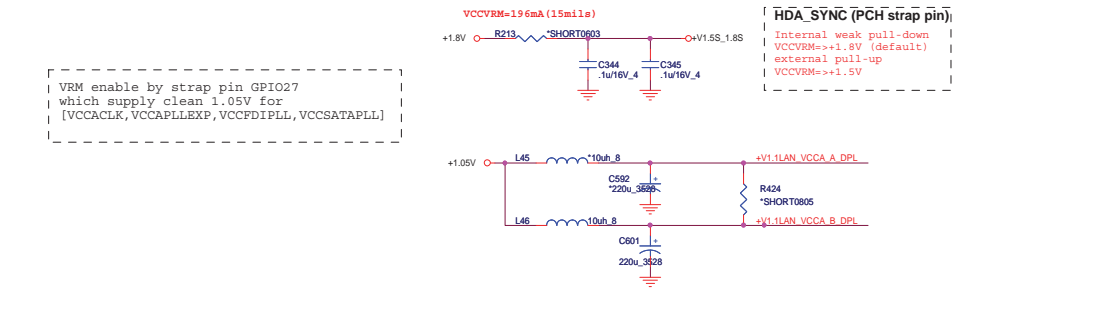
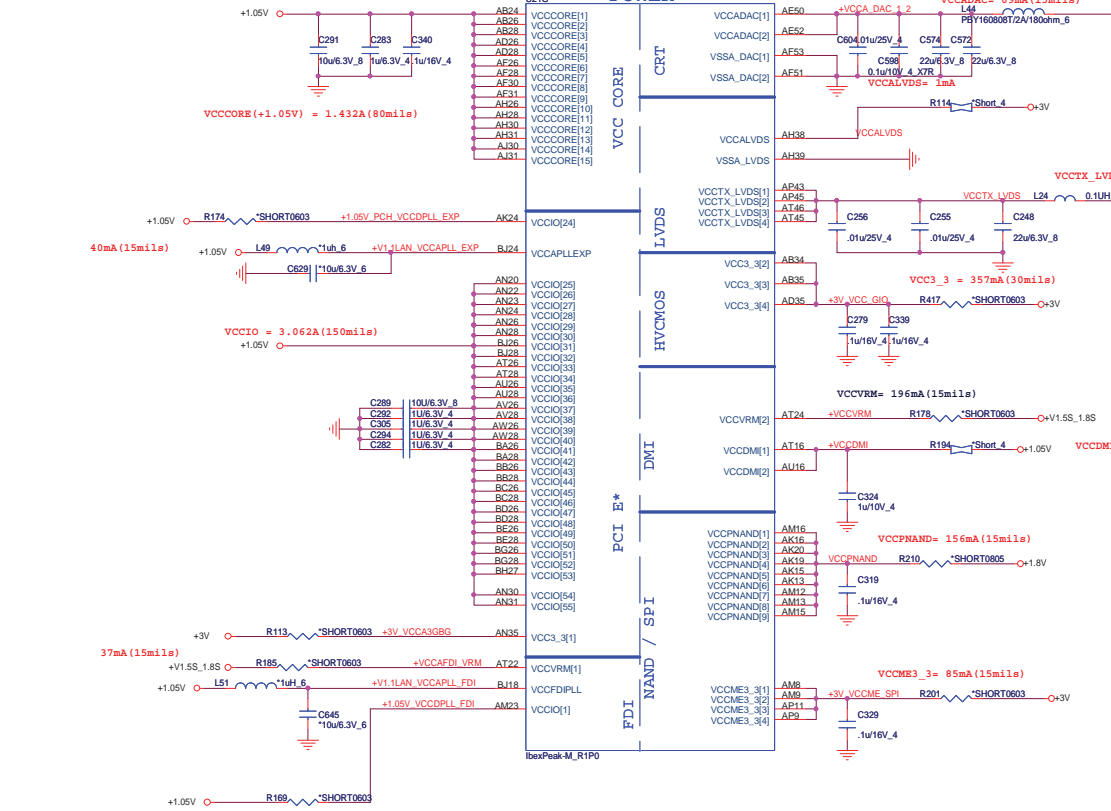
GPU_RST#

GPIO Pull-up/Pull-down



SV_SET_UP 1-X High = Strong (Default)

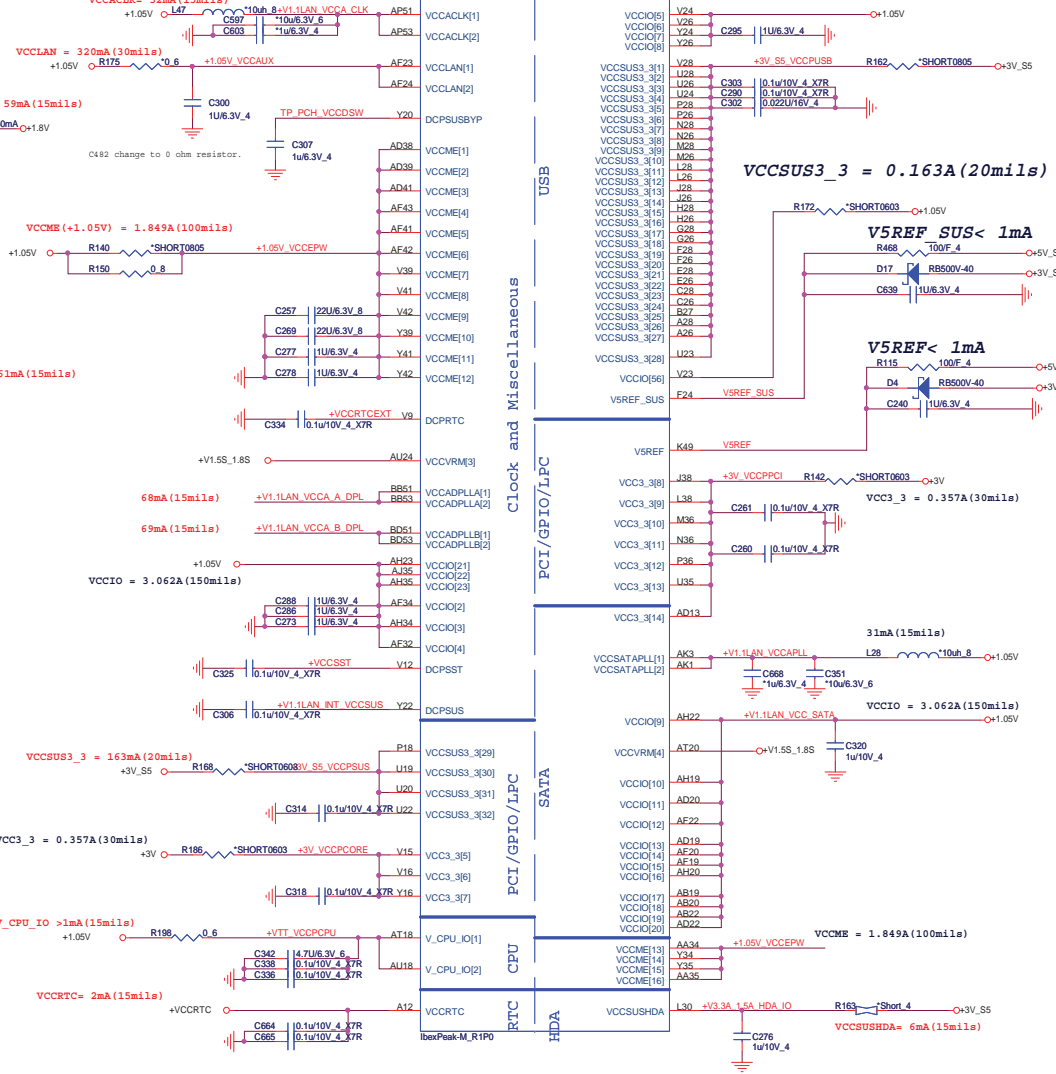
BOARD_ID0	High = 15"
	Low = 14"
RSV_GPIO8	High = Disable
	Low = Enable



VRM enable by strap pin GPIO27 which supply clean 1.05V for [VCCACLK, VCCAPLLEXP, VCCFDIPLL, VCCSATAPLL]

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM => +1.8V (default)
external pull-up
VCCVRM => +1.5V

3.3 V. This rail should be powered up during S5 system state. Note that Thermal Sensor shares the same power supply rail with DAC. The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



VCCIO = 3.208A (150mils)

VCCSUS3_3 = 0.163A (20mils)

V5REF SUS < 1mA

V5REF < 1mA

VCC3_3 = 0.357A (30mils)

VCCIO = 3.062A (150mils)

VCCIO = 3.062A (150mils)

VCCME = 1.849A (100mils)

VCCSUSHDA = 6mA (15mils)

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U21H		U21	
AB16	VSS[0]	AK30	VSS[80]
AA19	VSS[1]	AK31	VSS[81]
AA20	VSS[2]	AK32	VSS[82]
AA22	VSS[3]	AK34	VSS[83]
AM19	VSS[4]	AK35	VSS[84]
AA24	VSS[5]	AK38	VSS[85]
AA26	VSS[6]	AK43	VSS[86]
AA28	VSS[7]	AK46	VSS[87]
AA30	VSS[8]	AK49	VSS[88]
AA31	VSS[9]	AK5	VSS[89]
AA32	VSS[10]	AK8	VSS[90]
AB11	VSS[11]	AL2	VSS[91]
AB15	VSS[12]	AL52	VSS[92]
AB23	VSS[13]	AM11	VSS[93]
AB30	VSS[14]	BB44	VSS[94]
AB31	VSS[15]	AD24	VSS[95]
AB32	VSS[16]	AM20	VSS[96]
AB39	VSS[17]	AM22	VSS[97]
AB43	VSS[18]	AM24	VSS[98]
AB47	VSS[19]	AM26	VSS[99]
AB5	VSS[20]	AM28	VSS[100]
AB8	VSS[21]	AM30	VSS[101]
AC2	VSS[22]	AM31	VSS[102]
AC52	VSS[23]	AM32	VSS[103]
AD11	VSS[24]	AM34	VSS[104]
AD12	VSS[25]	AM35	VSS[105]
AD16	VSS[26]	AM38	VSS[106]
AD23	VSS[27]	AM39	VSS[107]
AD30	VSS[28]	AM42	VSS[108]
AD31	VSS[29]	AM46	VSS[109]
AD32	VSS[30]	AM49	VSS[110]
AD34	VSS[31]	AV22	VSS[111]
AU22	VSS[32]	AM7	VSS[112]
AD42	VSS[33]	AA50	VSS[113]
AD46	VSS[34]	BB10	VSS[114]
AD49	VSS[35]	AN32	VSS[115]
AD7	VSS[36]	AN50	VSS[116]
AE2	VSS[37]	AN52	VSS[117]
AE4	VSS[38]	AP12	VSS[118]
AF12	VSS[39]	AP21	VSS[119]
Y13	VSS[40]	AP42	VSS[120]
AH49	VSS[41]	AP46	VSS[121]
AU4	VSS[42]	AP5	VSS[122]
AF35	VSS[43]	AP8	VSS[123]
AF13	VSS[44]	AR2	VSS[124]
AN34	VSS[45]	AR52	VSS[125]
AF45	VSS[46]	AT11	VSS[126]
AF46	VSS[47]	BA12	VSS[127]
AF49	VSS[48]	AT11	VSS[128]
AF5	VSS[49]	AH48	VSS[129]
AF8	VSS[50]	AT32	VSS[130]
AG2	VSS[51]	AT36	VSS[131]
AG52	VSS[52]	AT41	VSS[132]
AH11	VSS[53]	AT47	VSS[133]
AH15	VSS[54]	AT7	VSS[134]
AH16	VSS[55]	AV12	VSS[135]
AH24	VSS[56]	AV16	VSS[136]
AH32	VSS[57]	AV20	VSS[137]
AV18	VSS[58]	AV24	VSS[138]
AH43	VSS[59]	AV30	VSS[139]
AH47	VSS[60]	AV34	VSS[140]
AH7	VSS[61]	AV38	VSS[141]
AJ19	VSS[62]	AV42	VSS[142]
AJ2	VSS[63]	AV46	VSS[143]
AJ20	VSS[64]	AV49	VSS[144]
AJ22	VSS[65]	AV5	VSS[145]
AJ23	VSS[66]	AW14	VSS[146]
AJ26	VSS[67]	AW18	VSS[147]
A28	VSS[68]	AW19	VSS[148]
AJ32	VSS[69]	AW2	VSS[149]
AJ34	VSS[70]	AW32	VSS[150]
AT5	VSS[71]	AW36	VSS[151]
AJ4	VSS[72]	AW40	VSS[152]
AM41	VSS[73]	AW52	VSS[153]
AN19	VSS[74]	AY11	VSS[154]
AK26	VSS[75]	AY43	VSS[155]
AK22	VSS[76]	AY47	VSS[156]
AK23	VSS[77]		VSS[157]
AK28	VSS[78]		VSS[158]
	VSS[79]		

IbexPeak-M_R1P0

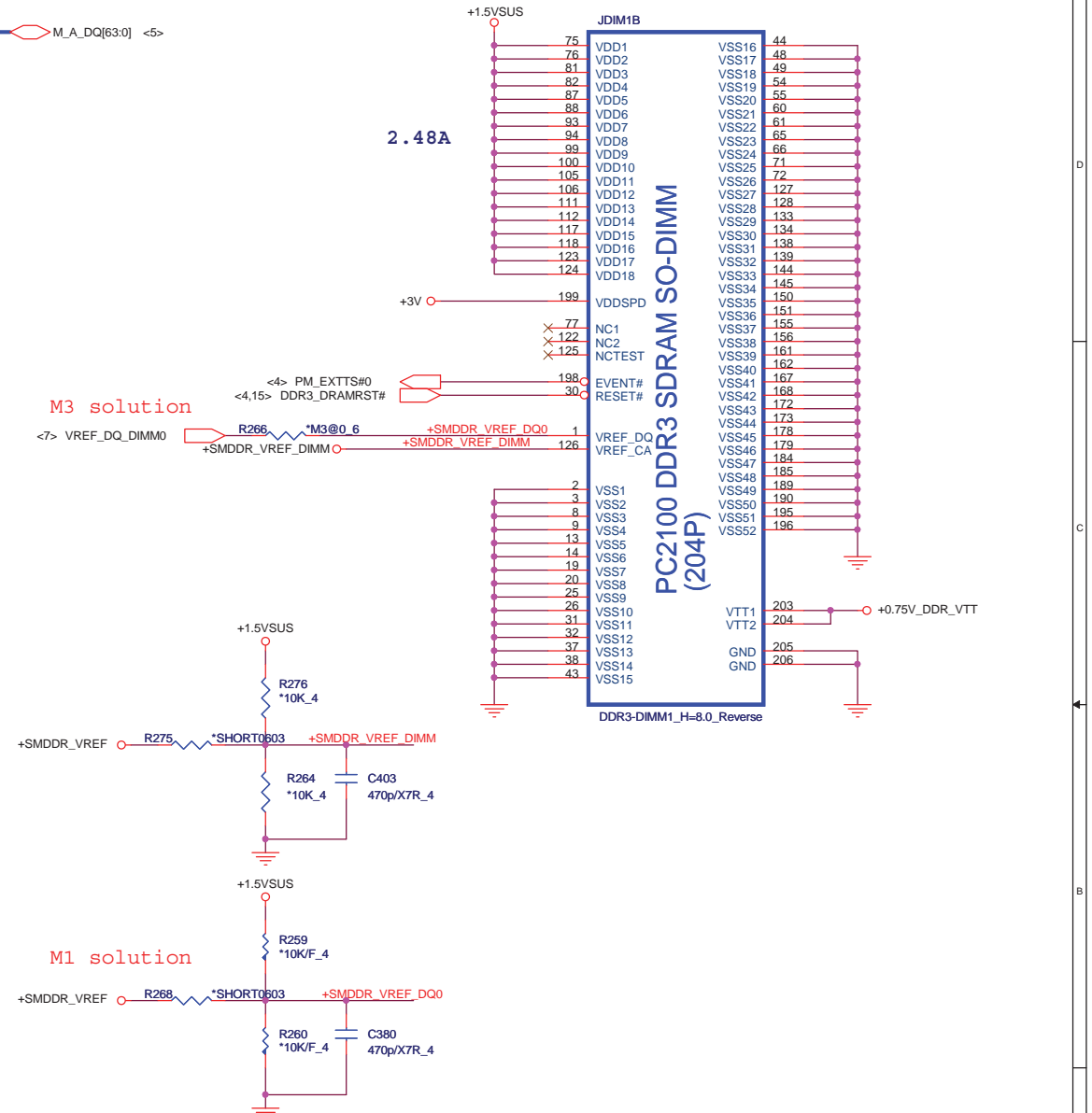
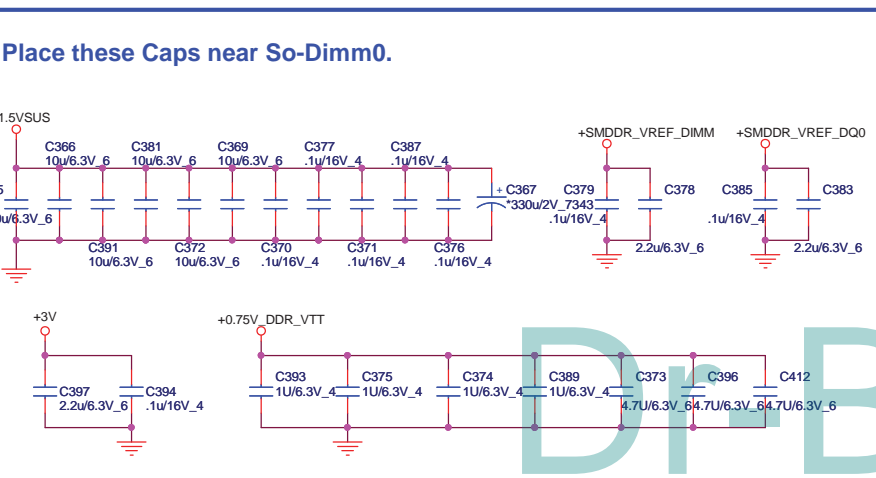
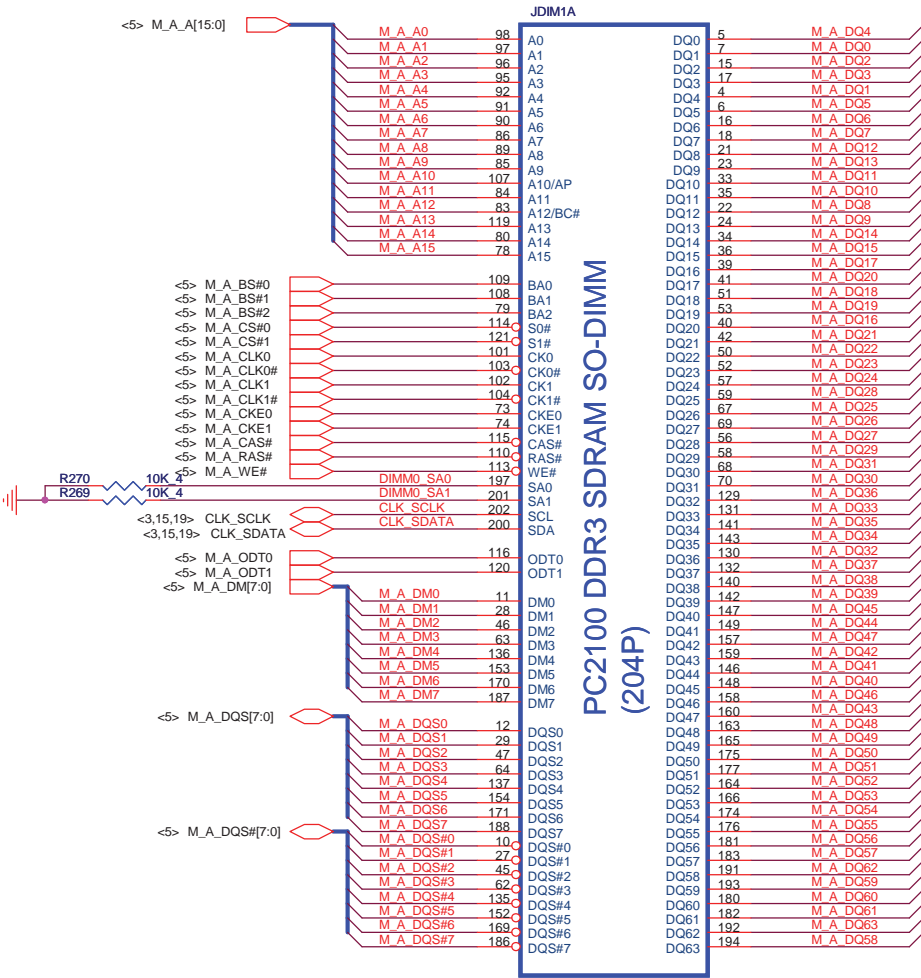
U21		H49	
AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L22
B7	VSS[169]	VSS[269]	L32
BG12	VSS[170]	VSS[270]	L36
BB12	VSS[171]	VSS[271]	L40
BB16	VSS[172]	VSS[272]	L52
BB20	VSS[173]	VSS[273]	M12
BB24	VSS[174]	VSS[274]	M16
BB30	VSS[175]	VSS[275]	M20
BB34	VSS[176]	VSS[276]	M34
BB38	VSS[177]	VSS[277]	M38
BB42	VSS[178]	VSS[278]	M42
BB49	VSS[179]	VSS[279]	M46
BB5	VSS[180]	VSS[280]	M49
BC10	VSS[181]	VSS[281]	M5
BC14	VSS[182]	VSS[282]	M8
BC18	VSS[183]	VSS[283]	P11
BC2	VSS[184]	VSS[284]	AD15
BC22	VSS[185]	VSS[285]	P22
BC32	VSS[186]	VSS[286]	P30
BC40	VSS[187]	VSS[287]	P32
BC44	VSS[188]	VSS[288]	P34
BC44	VSS[189]	VSS[289]	P42
CS52	VSS[190]	VSS[290]	P45
BH9	VSS[191]	VSS[291]	P47
BD48	VSS[192]	VSS[292]	R2
BD49	VSS[193]	VSS[293]	R52
BD5	VSS[194]	VSS[294]	T12
BE12	VSS[195]	VSS[295]	T41
BE16	VSS[196]	VSS[296]	T46
BE20	VSS[197]	VSS[297]	T49
BE24	VSS[198]	VSS[298]	T5
BE30	VSS[199]	VSS[299]	T8
BE34	VSS[200]	VSS[300]	U30
BE38	VSS[201]	VSS[301]	U31
BE42	VSS[202]	VSS[302]	U32
BE46	VSS[203]	VSS[303]	U34
BE48	VSS[204]	VSS[304]	P38
BE50	VSS[205]	VSS[305]	V11
BE6	VSS[206]	VSS[306]	P16
BE8	VSS[207]	VSS[307]	V19
BF3	VSS[208]	VSS[308]	V20
BF49	VSS[209]	VSS[309]	V22
BF51	VSS[210]	VSS[310]	V30
BG18	VSS[211]	VSS[311]	V31
BG24	VSS[212]	VSS[312]	V32
BG4	VSS[213]	VSS[313]	V34
BH11	VSS[214]	VSS[314]	V35
BH15	VSS[215]	VSS[315]	V38
BH19	VSS[216]	VSS[316]	V43
BH23	VSS[217]	VSS[317]	V45
BH31	VSS[218]	VSS[318]	V46
BH35	VSS[219]	VSS[319]	V47
BH39	VSS[220]	VSS[320]	V49
BH43	VSS[221]	VSS[321]	V7
BH47	VSS[222]	VSS[322]	V8
BH7	VSS[223]	VSS[323]	W2
C12	VSS[224]	VSS[324]	W52
C50	VSS[225]	VSS[325]	Y11
D51	VSS[226]	VSS[326]	Y12
E12	VSS[227]	VSS[327]	Y15
E16	VSS[228]	VSS[328]	Y19
E20	VSS[229]	VSS[329]	Y23
E24	VSS[230]	VSS[330]	Y28
E30	VSS[231]	VSS[331]	Y30
E34	VSS[232]	VSS[332]	Y31
E38	VSS[233]	VSS[333]	Y32
E42	VSS[234]	VSS[334]	Y38
E46	VSS[235]	VSS[335]	Y43
E48	VSS[236]	VSS[336]	Y46
E6	VSS[237]	VSS[337]	P49
E8	VSS[238]	VSS[338]	V6
F49	VSS[239]	VSS[339]	Y8
F5	VSS[240]	VSS[340]	P24
G10	VSS[241]	VSS[341]	T43
G14	VSS[242]	VSS[342]	AD51
G18	VSS[243]	VSS[343]	ATR
G2	VSS[244]	VSS[344]	AD47
G22	VSS[245]	VSS[345]	Y47
G32	VSS[246]	VSS[346]	AT12
G36	VSS[247]	VSS[347]	AM6
G40	VSS[248]	VSS[348]	AT13
G44	VSS[249]	VSS[349]	AM5
G52	VSS[250]	VSS[350]	AK45
AF39	VSS[251]	VSS[351]	AK39
H16	VSS[252]	VSS[352]	AV14
H20	VSS[253]	VSS[353]	
H30	VSS[254]	VSS[354]	
H34	VSS[255]	VSS[355]	
H38	VSS[256]	VSS[356]	
H42	VSS[257]	VSS[356]	
	VSS[258]		

IbexPeak-M_R1P0

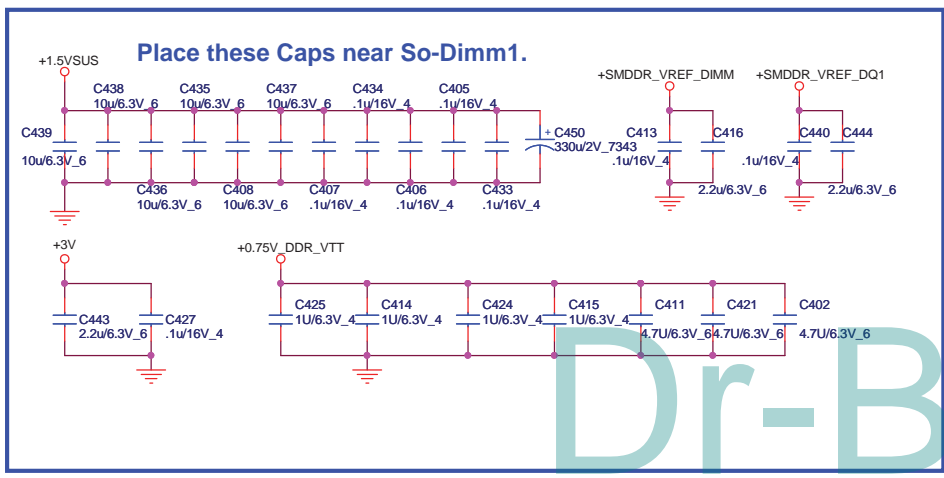
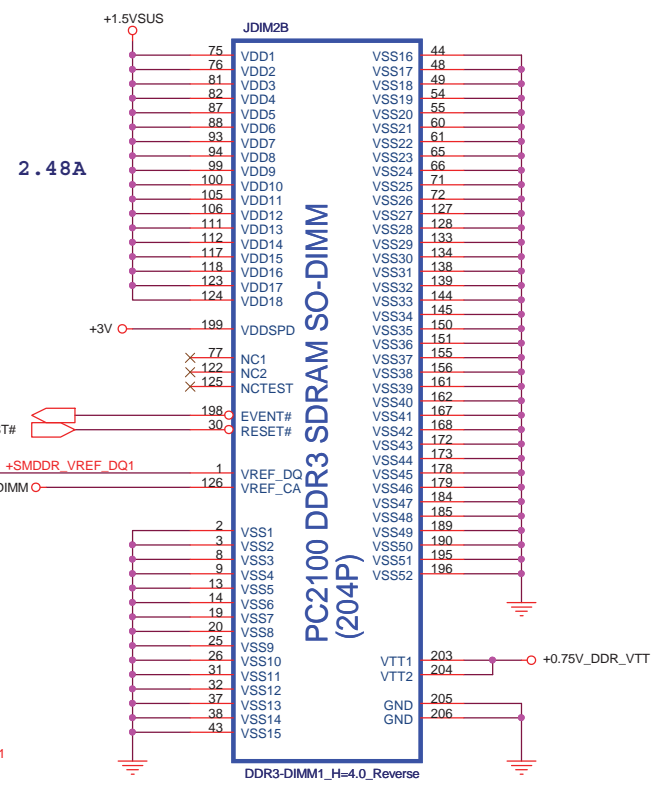
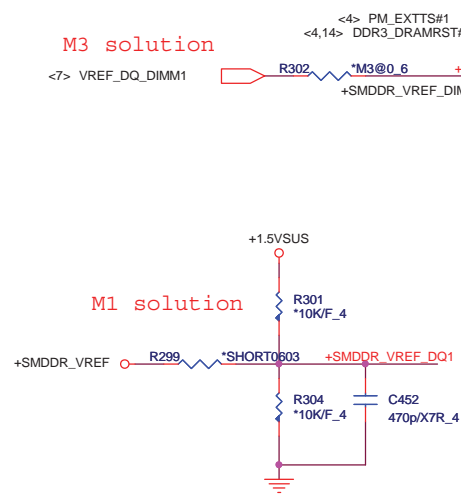
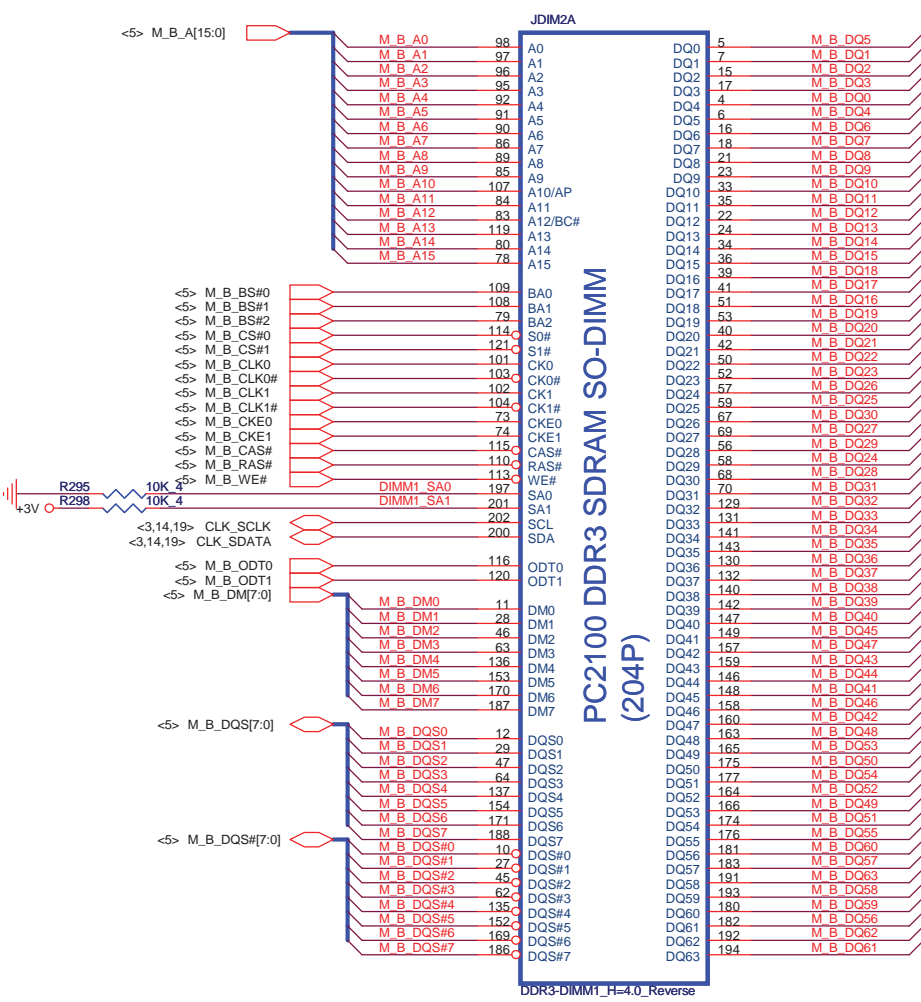


Quanta Computer Inc.
PROJECT : ZQH

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	IBEX PEAK-M 6/6	1A
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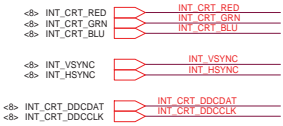
DrBios.com



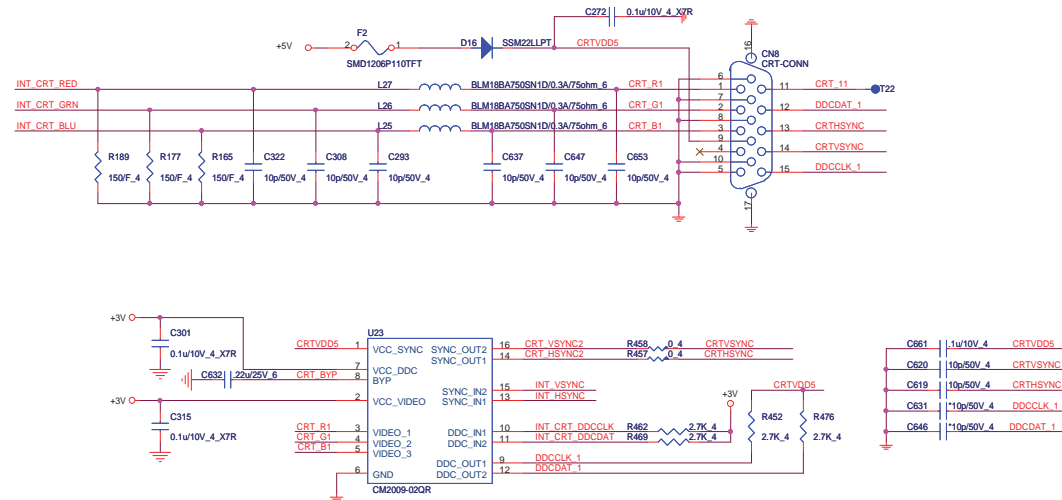
Dr-Bios.com

CRT Switch

0_ohm Resistor place close to Joint-Point

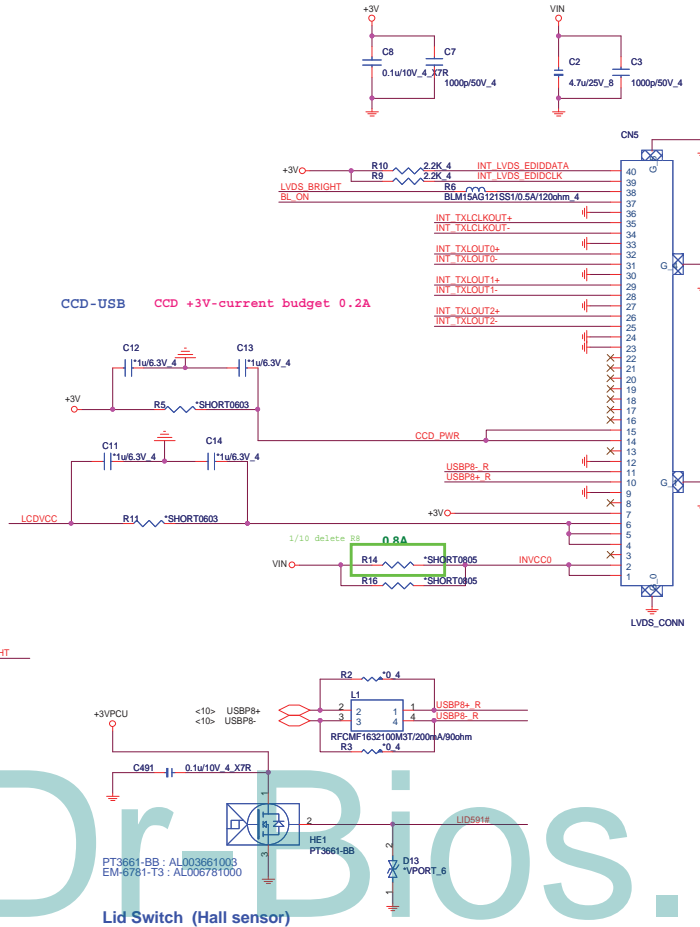
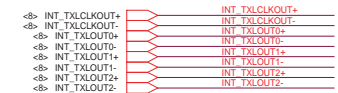


CRT



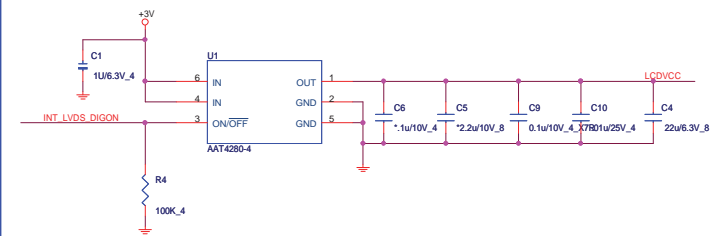
LVDS

0_ohm Resistor place close to Joint-Point

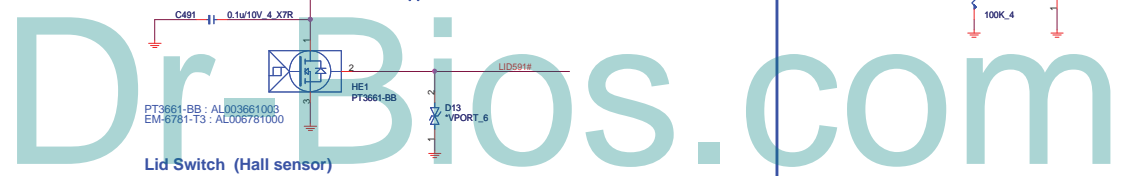
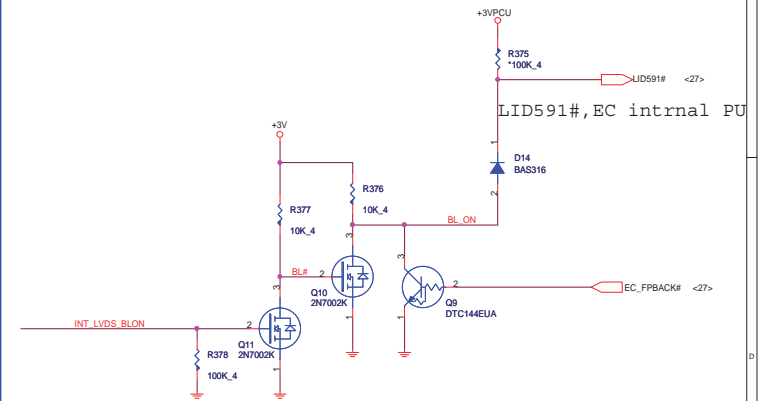


Lid Switch (Hall sensor)

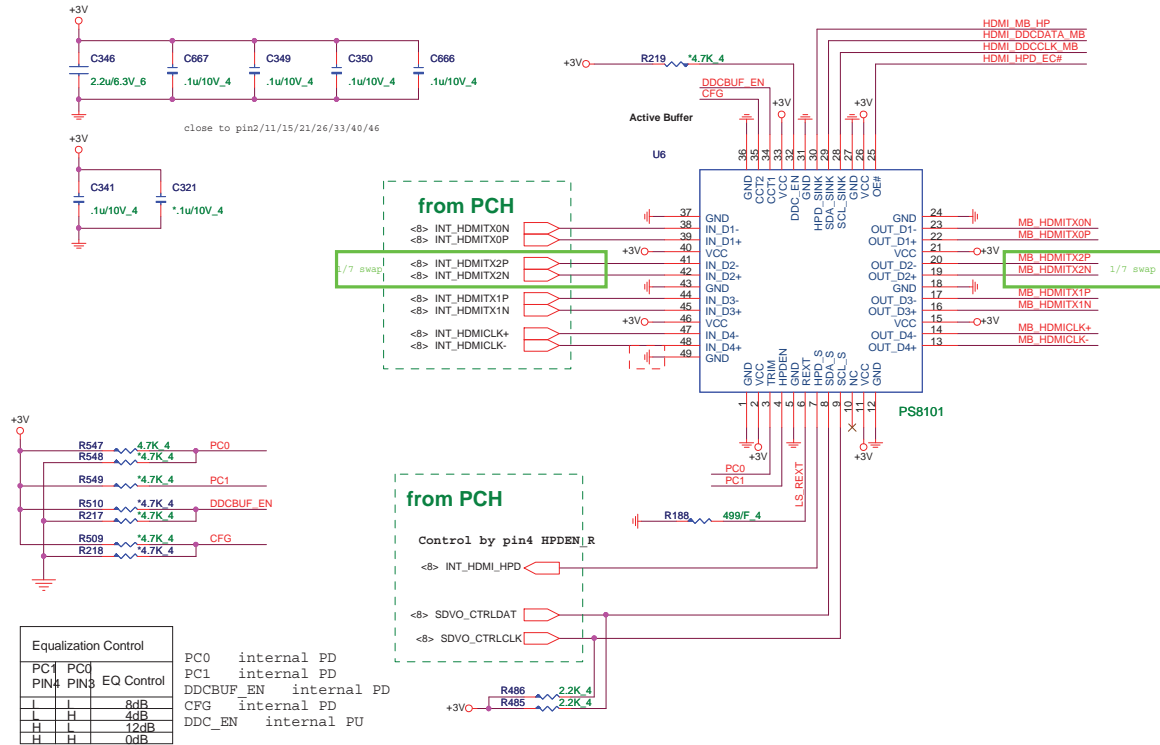
LCD Power



Backlight Control



HDMI LEVEL SHIFTER

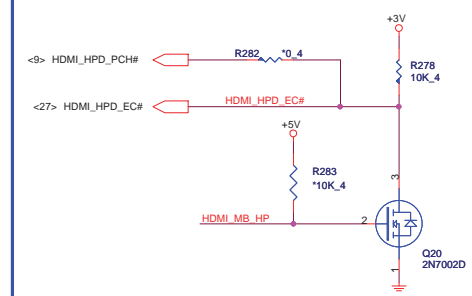


Equalization Control

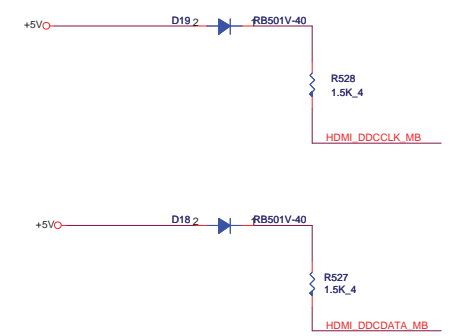
PC1	PC0	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
 PC1 internal PD
 DDCBUF_EN internal PD
 CFG internal PD
 DDC_EN internal PU

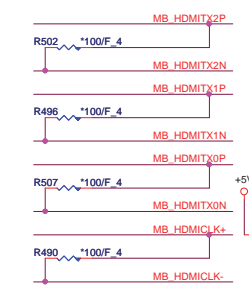
HDMI-detect



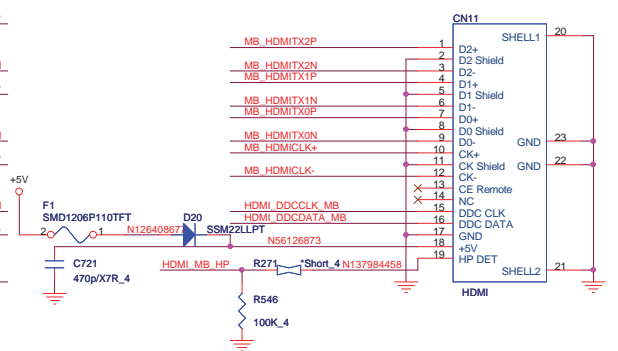
I2C



EMI



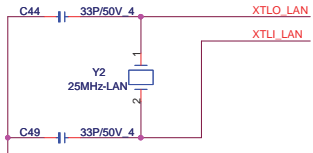
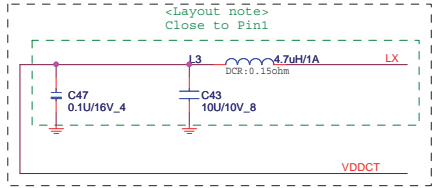
HDMI connector



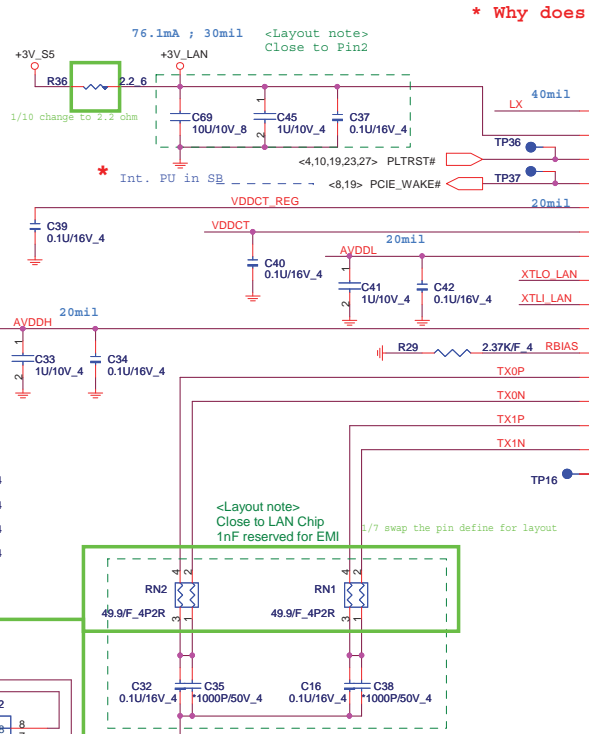
Dr-Bios.com

LAN (LAN)

<BOM note>
 If center tap power come from internal switch regulator
 => Stuff 52SWR@ (Default)
 If center tap power come from internal LDO
 => Stuff 52LDO@

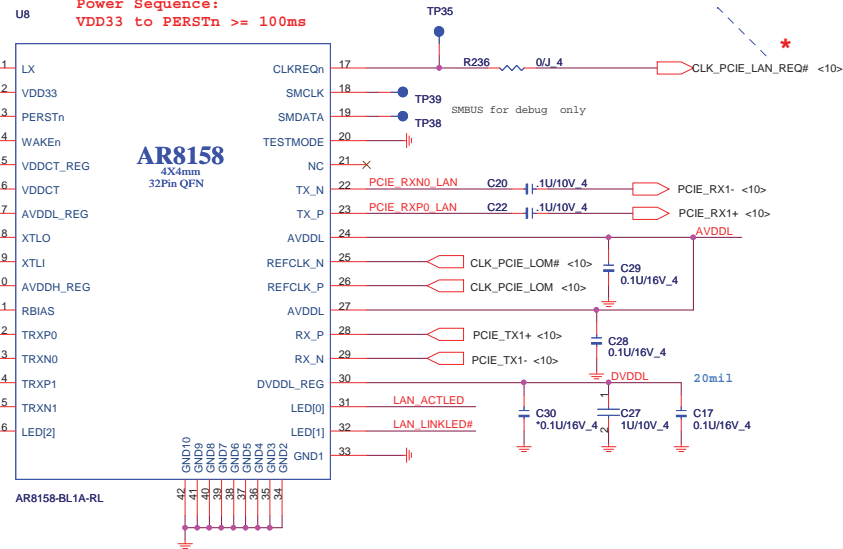


- TXOP C48 6.8PF/50V_4
- TXON C46 6.8PF/50V_4
- TX1P C51 6.8PF/50V_4
- TX1N C52 6.8PF/50V_4



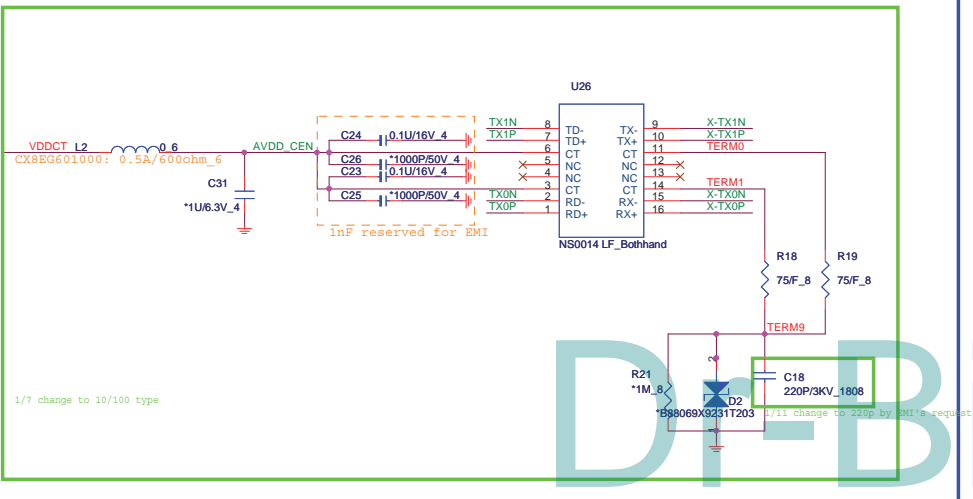
* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERStn >= 100ms

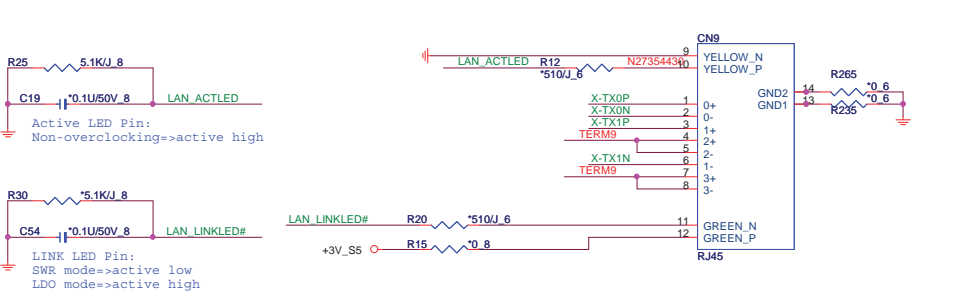


+3V_S5	2	VDD33	7	AVDDL_REG	+1.1V regulator output (For all the analog 1.1V supply pins)
+1.1V analog power	24/27	AVDDL	10	AVDDH_REG	+2.7V regulator output
			30	DVDDL_REG	+1.1V regulator output (For all the digital 1.1V supply pins)
			5	VDDCT_REG	+1.8V regulator output (For VDDCT when LDO mode)
+1.7V analog power	6	VDDCT	1	LX	+1.7V Switching regulator (For VDDCT when switching mode)

TRANSFORMER (LAN)



RJ45 Connector (LAN)



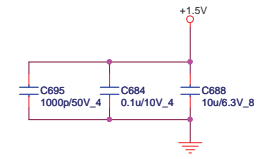
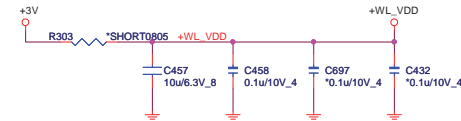
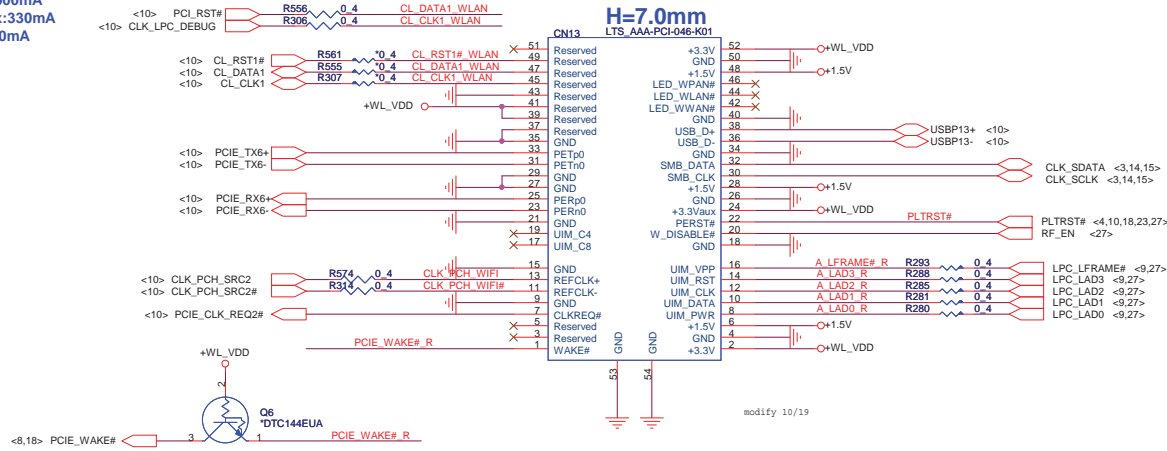
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA

Debug

Check LED signal. (active high or low)

H=7.0mm
 LTS AAA-PCI-046-K01

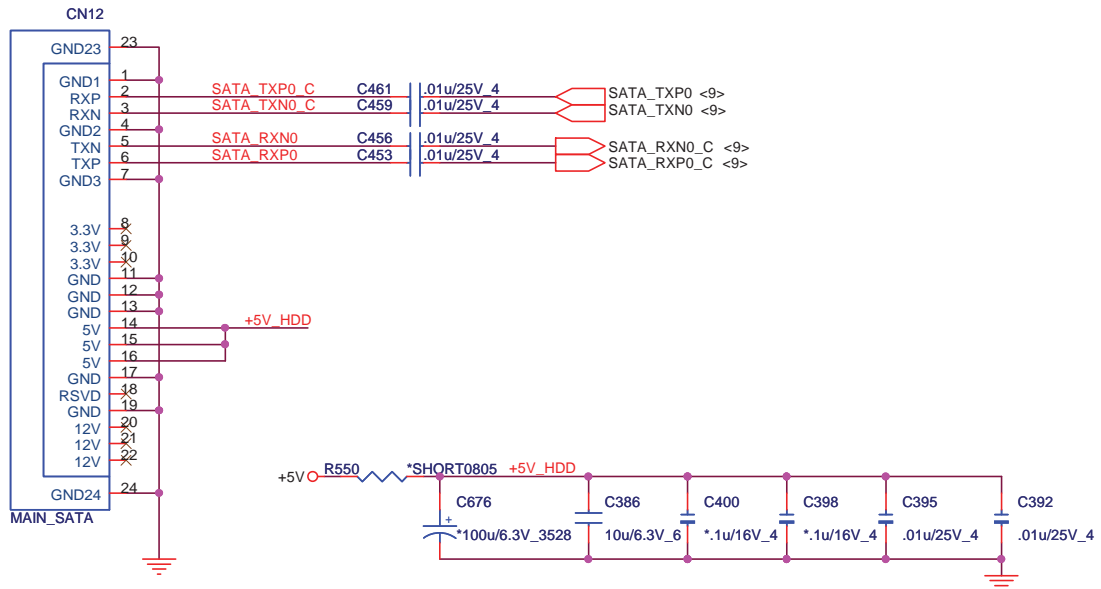


Debug

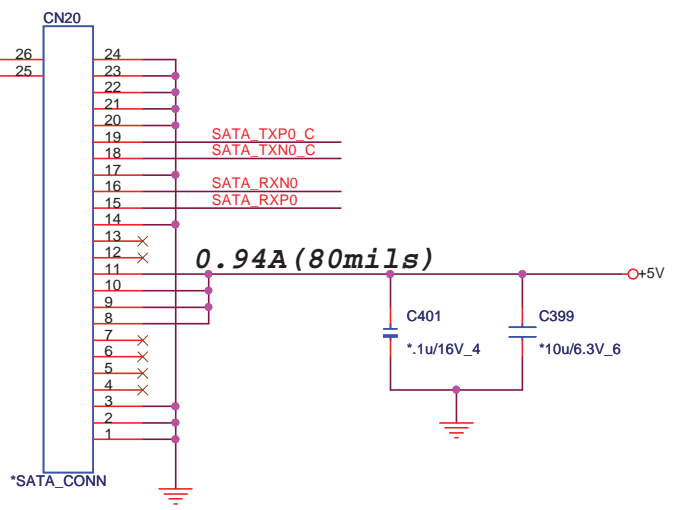
Dr-Bios.com

		Quanta Computer Inc. PROJECT : ZQH	
		Size: Document Number MINI PCI-E card/TV	Rev: 1A
Date: Monday, March 14, 2011		Sheet 19 of 45	

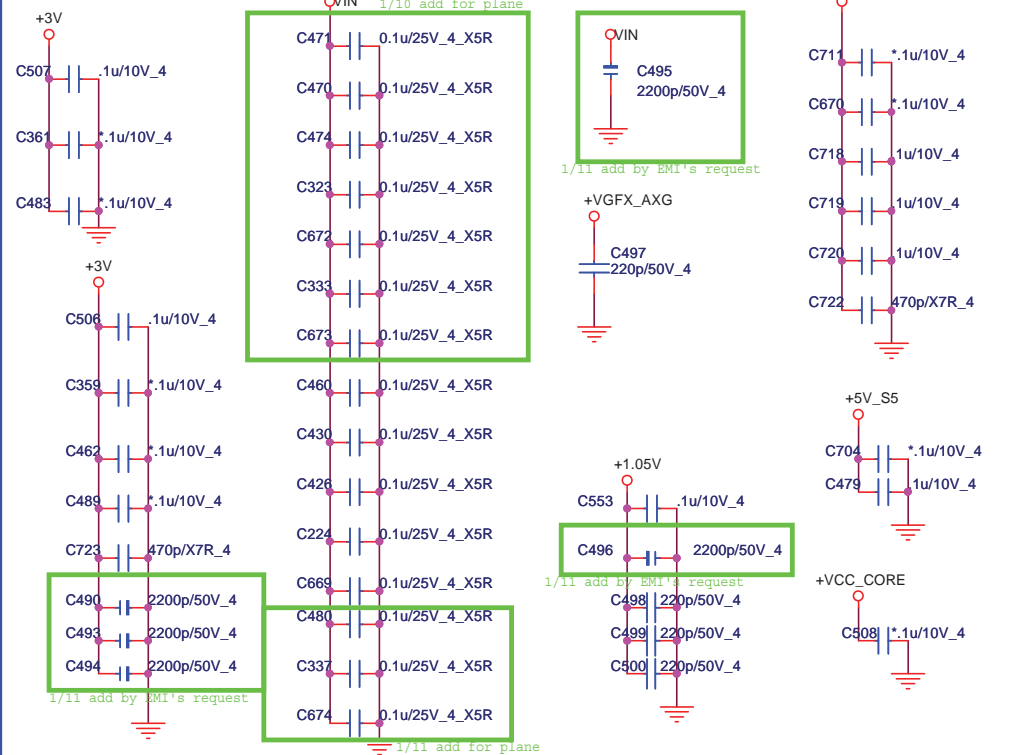
MAIN SATA HDD



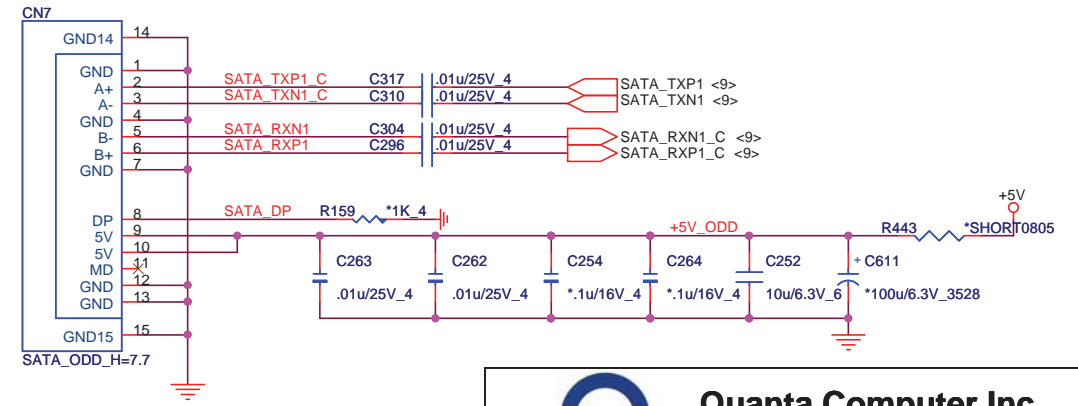
2.5" SATA HDD




EE RETURN-PATH CAPACITORS



ODD (SATA)

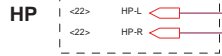




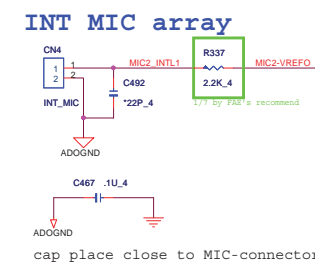
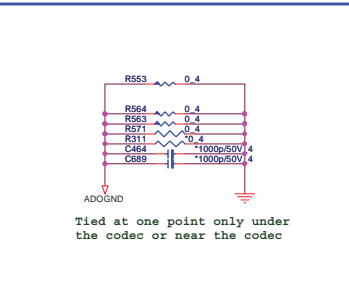
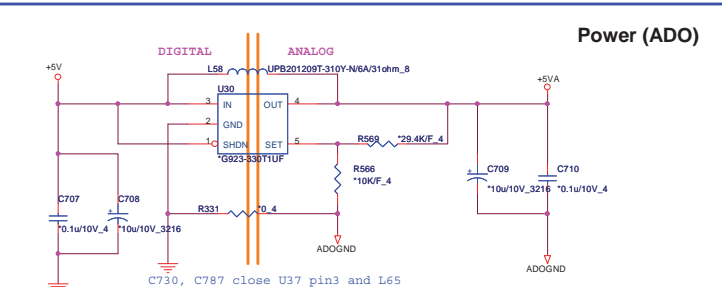
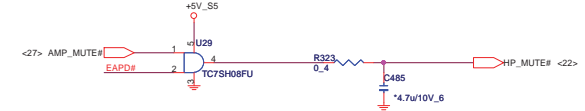
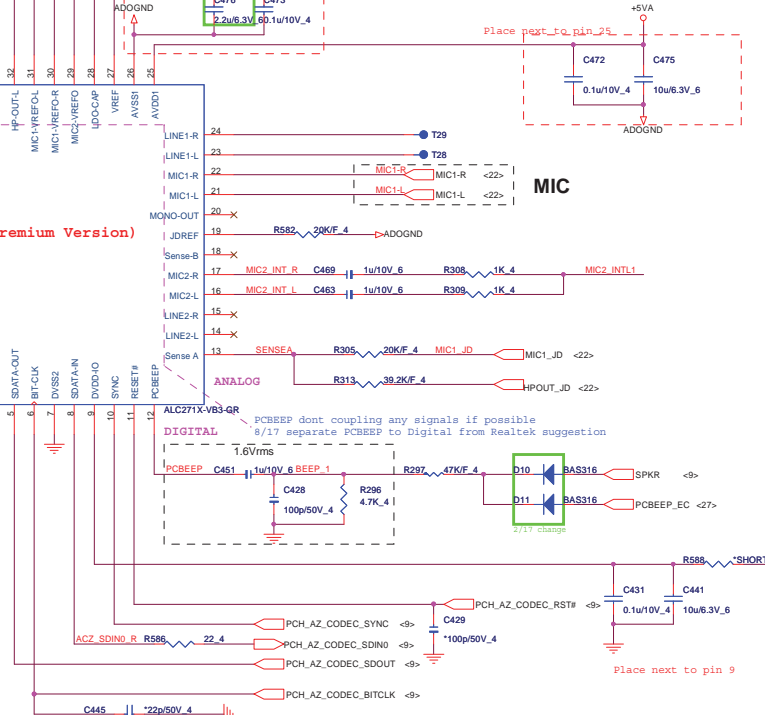
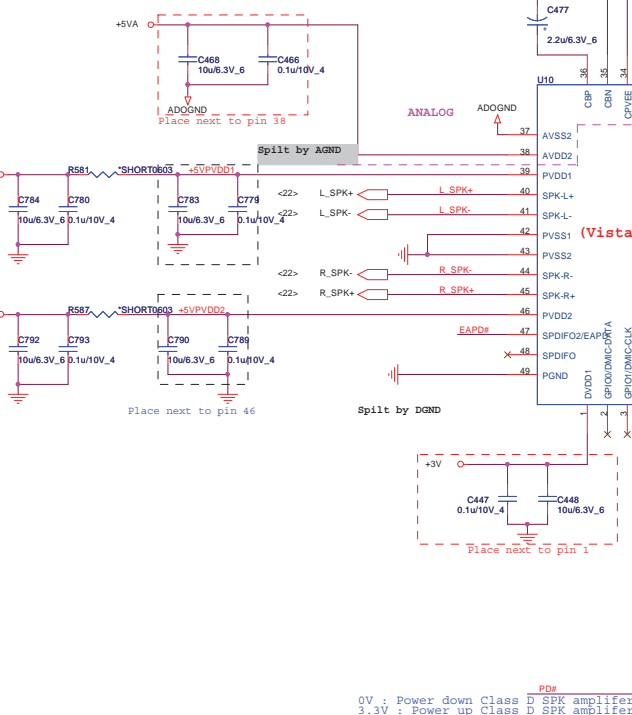
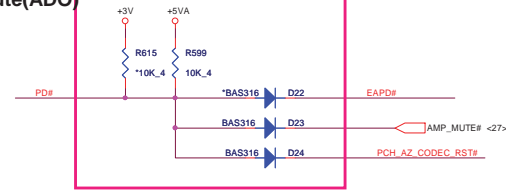
Quanta Computer Inc.
PROJECT : ZQH

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	SATA-HDD/ODD/USB-ESATA	1A
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Codec(ADO)

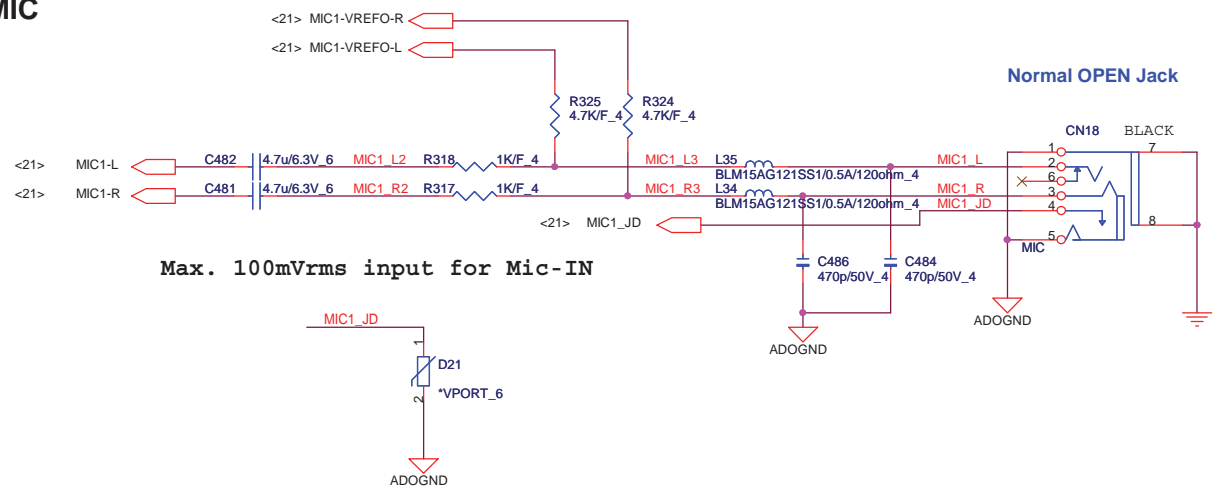


Mute(ADO)

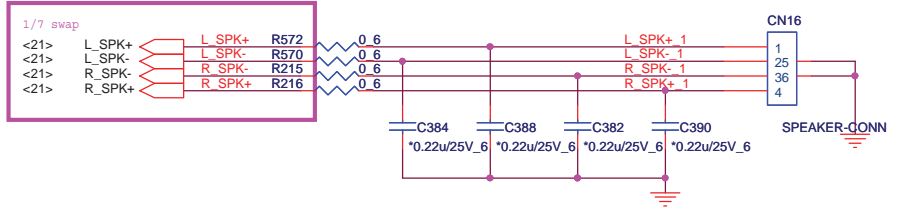


Quanta Computer Inc.
 PROJECT : QJE
 Size Document Number REALTEK ALC663&888/MDC Rev 1A
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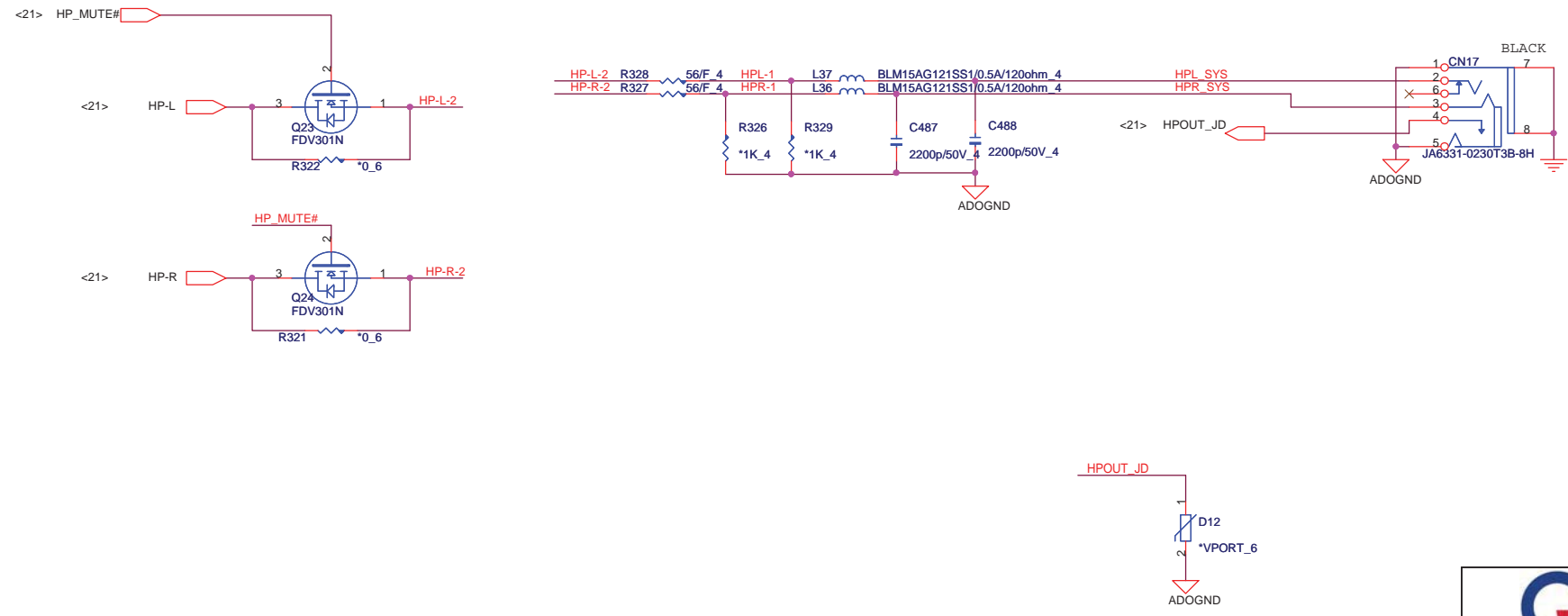
MIC



Internal Speaker



HP/SPDIF



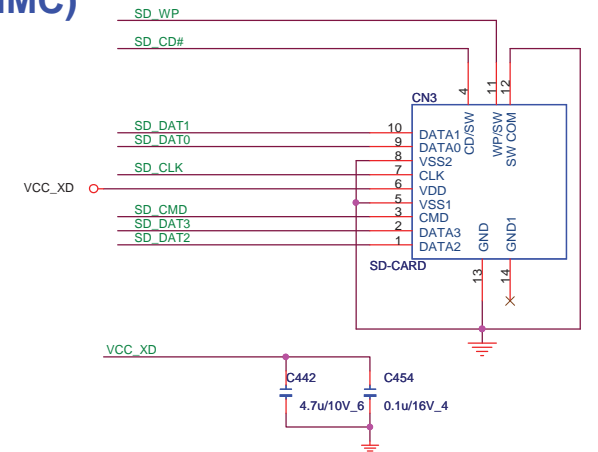
		Quanta Computer Inc. PROJECT : ZQH	
		Size Document Number AMP /AUDIO JACK CONN	Rev 1A
Date: Monday, March 14, 2011		Sheet 22 of 35	Page 1

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CARD READER Controller AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

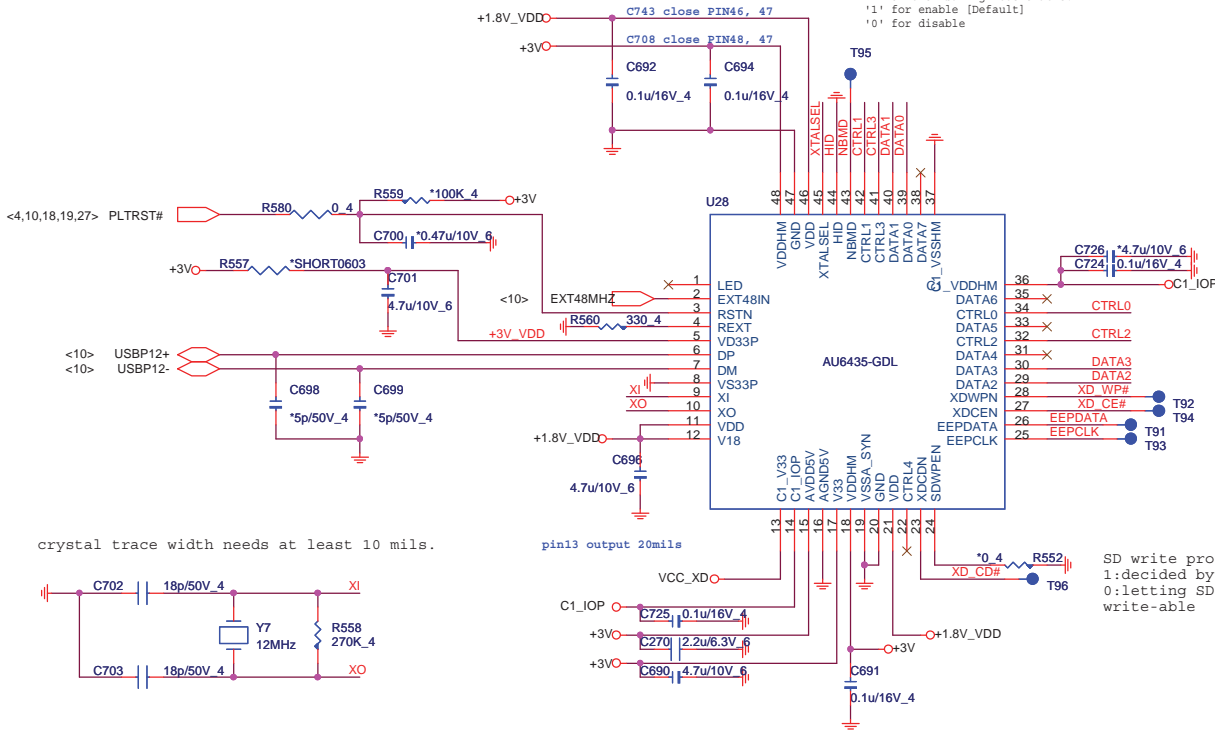
Main	DFHS11FR011
Second	DFHS11FR033



PIN45=Clock input selection
'1' for 48MHz input [Default, Internal PU]
'0' for 12MHz input



PIN43=Power saving mode enable.
'1' for enable [Default]
'0' for disable



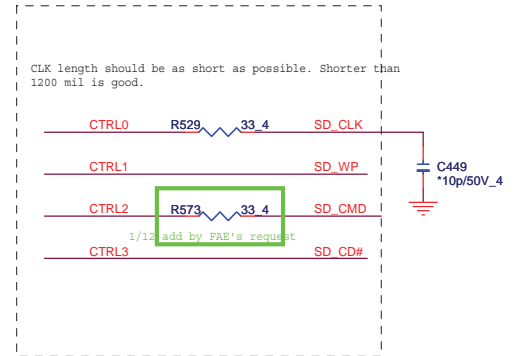
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

CTRL0, CTRL1 trace length shorter,
and surround with GND.

The trace length difference for each card interfaces should be smaller than 500 mil



Close to connector



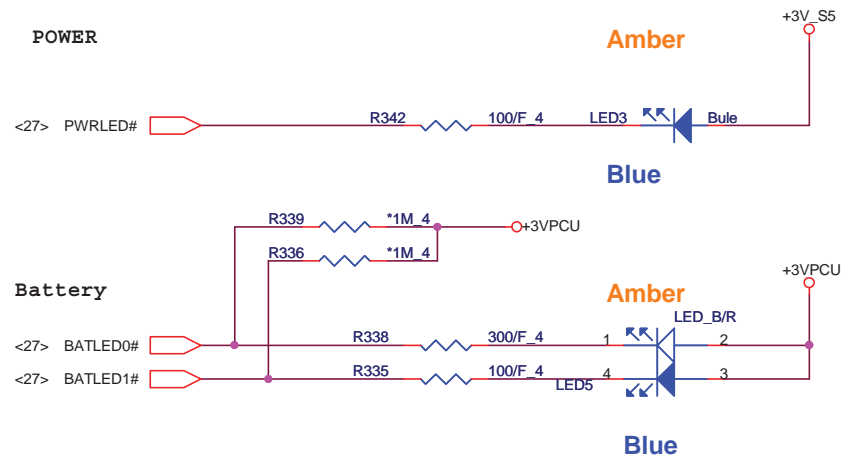
crystal trace width needs at least 10 mils.


pin13 output 20mils

SD write protect
1:decided by SDWP[Default]
0:letting SD always
write-able



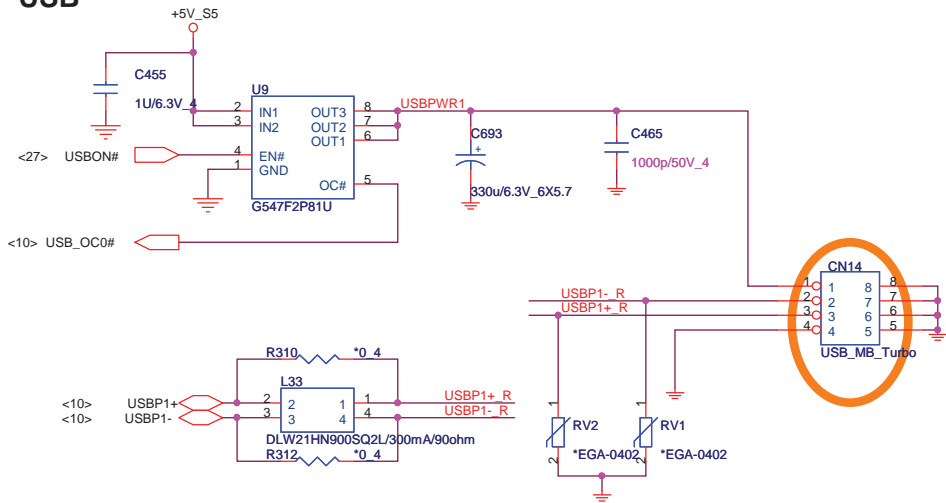
LED



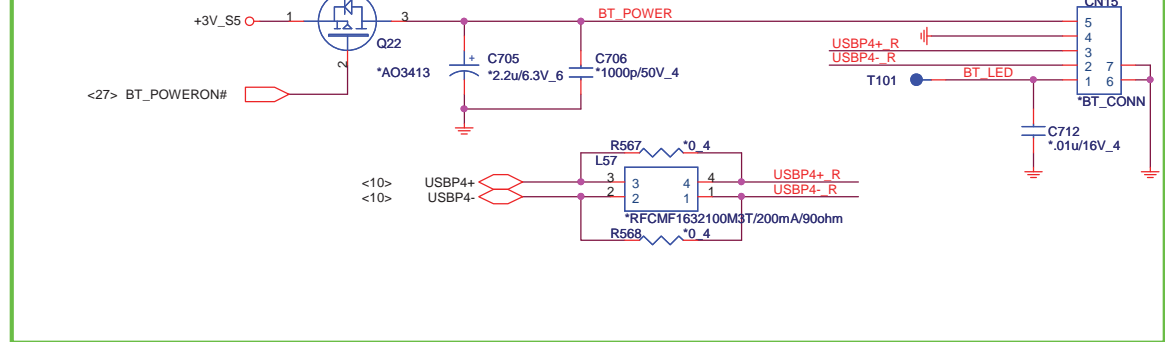
		Quanta Computer Inc.
		PROJECT : ZQH
Size	Document Number	Rev 1A
POWER/MMB/LAUNCH/LED		
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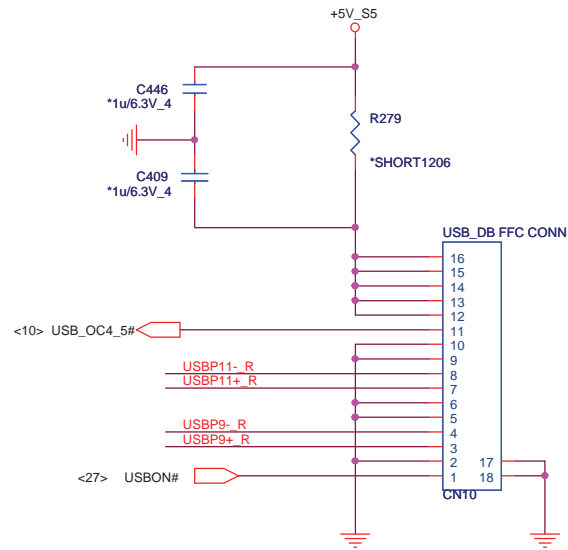
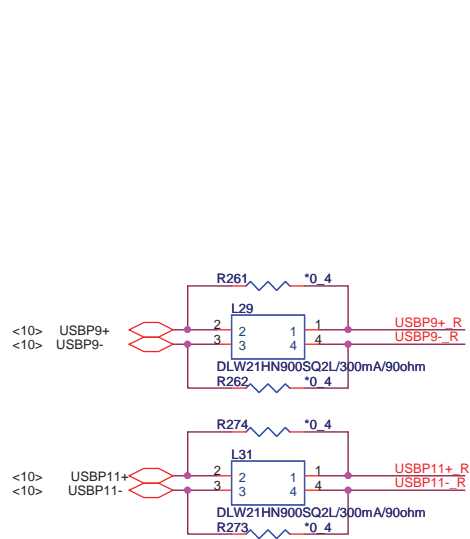
USB




BLUETOOTH CONNECTOR for 3.0



USB/B

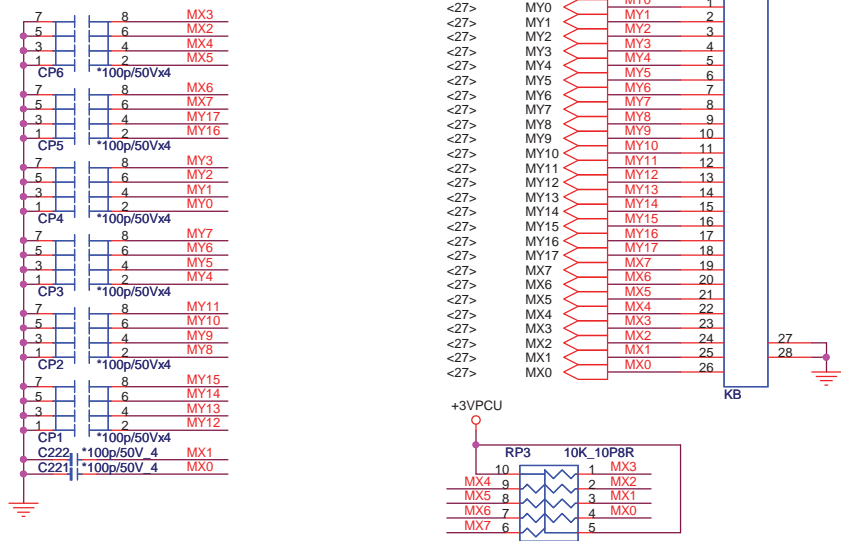




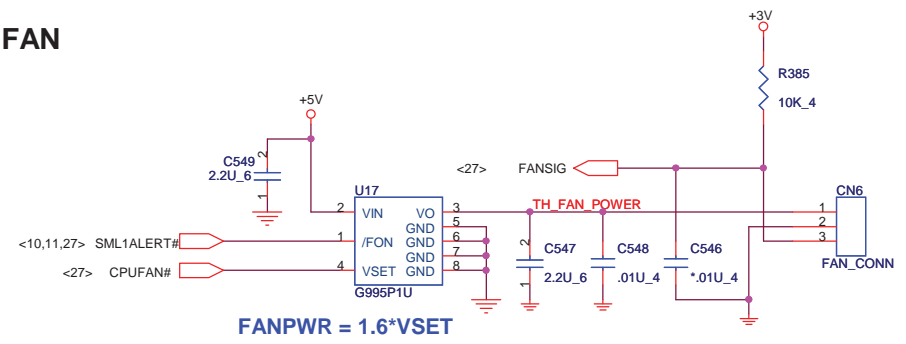
Quanta Computer Inc.
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	USB/ BT	1A
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K/B

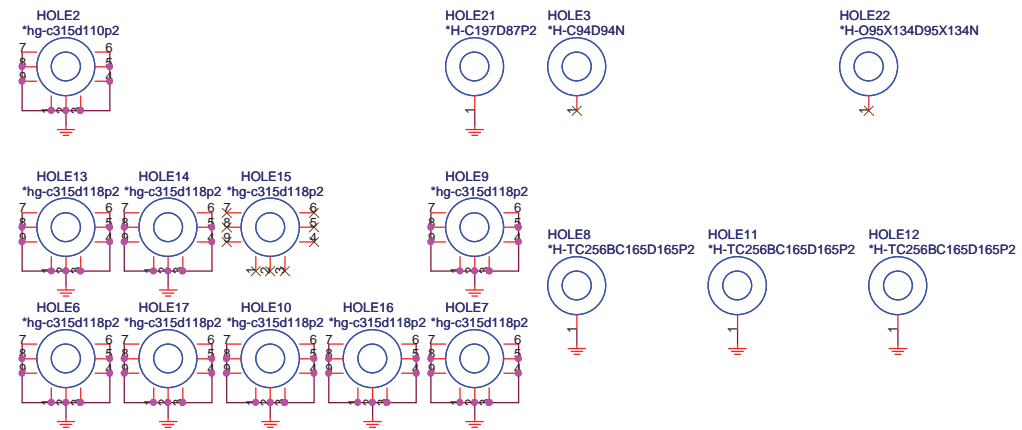


CPU FAN

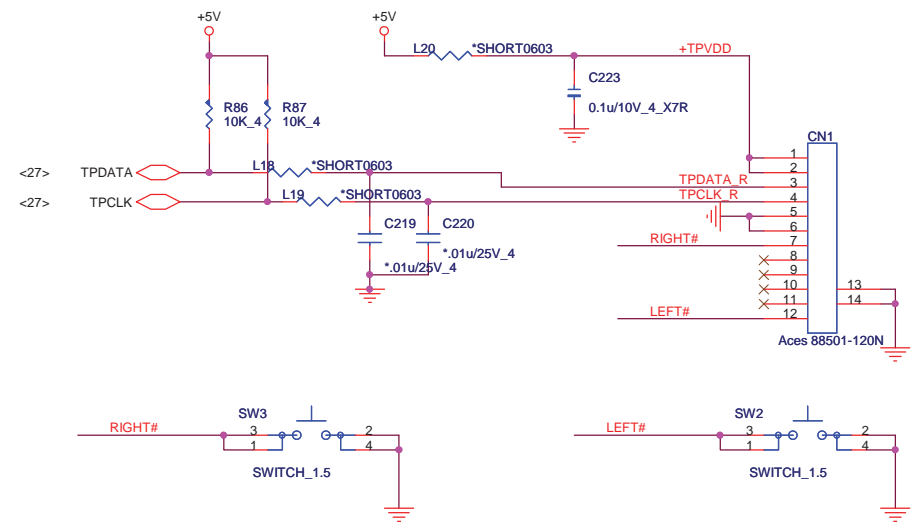



FANPWR = 1.6*VSET

HOLE



TOUCHPAD & Switch CONN.

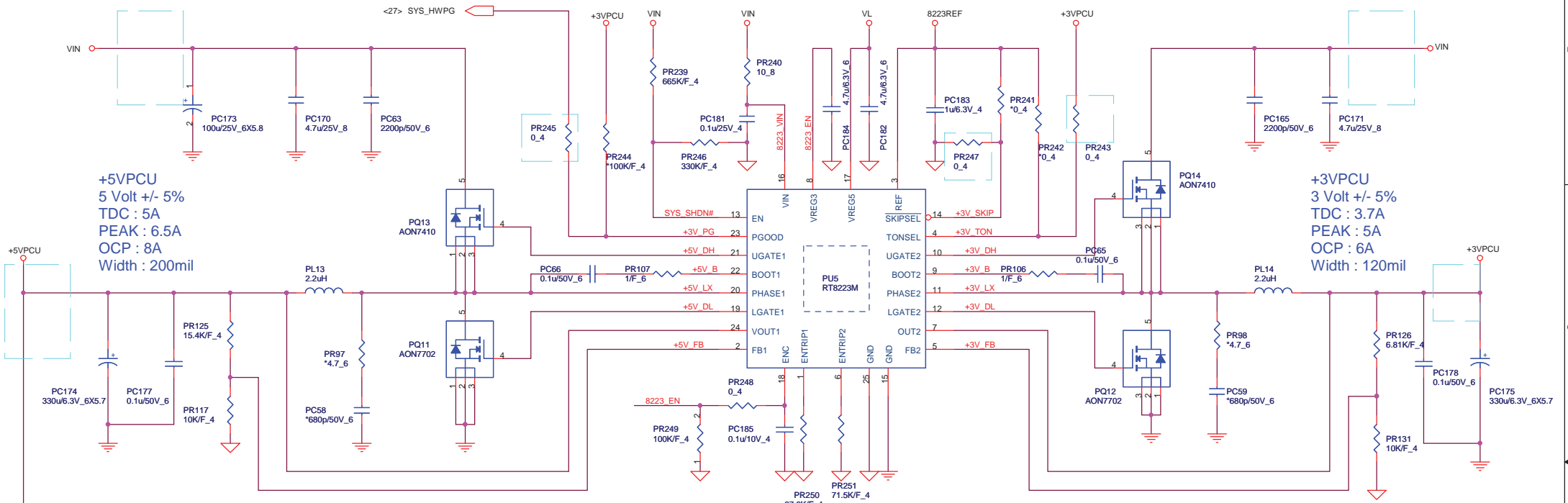




Quanta Computer Inc.
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Ven=7.23V

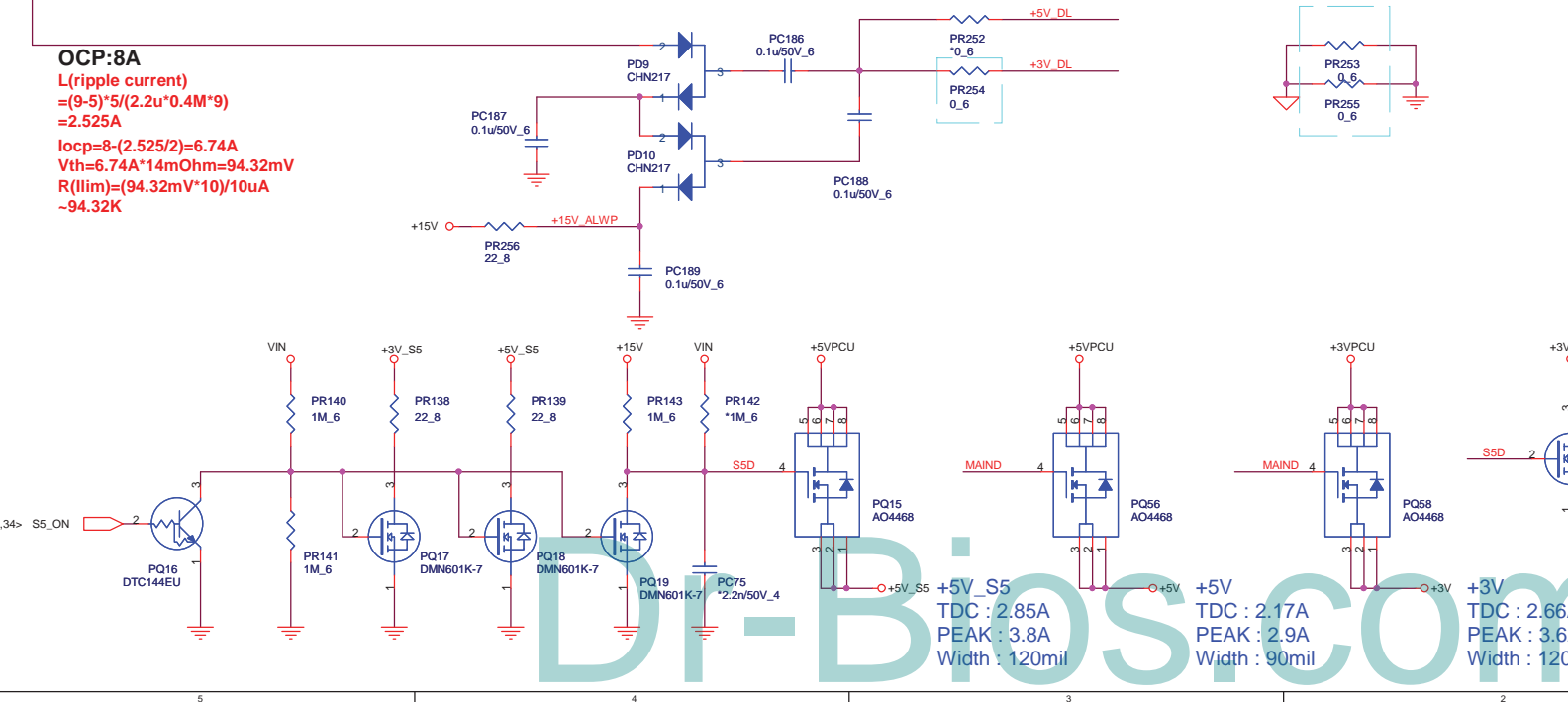


+5VPCU
 5 Volt +/- 5%
 TDC : 5A
 PEAK : 6.5A
 OCP : 8A
 Width : 200mil

+3VPCU
 3 Volt +/- 5%
 TDC : 3.7A
 PEAK : 5A
 OCP : 6A
 Width : 120mil

OCP:8A
 L(ripple current)
 $= (9-3) * 5 / (2.2u * 0.4M * 9)$
 $= 2.525A$
 $I_{ocp} = 8 - (2.525/2) = 6.74A$
 $V_{th} = 6.74A * 14mOhm = 94.32mV$
 $R(I_{lim}) = (94.32mV * 10) / 10uA$
 $= 94.32K$

OCP:6A
 L(ripple current)
 $= (9-3.3) * 3.3 / (2.2u * 0.5M * 9)$
 $\sim 1.9A$
 $I_{ocp} = 6 - (1.9/2) = 5.05A$
 $V_{th} = 5.05A * 14mOhm = 70.7mV$
 $R(I_{lim}) = (70.7mV * 10) / 10uA$
 $= 70.7K$



+5V_S5
 TDC : 2.85A
 PEAK : 3.8A
 Width : 120mil

+5V
 TDC : 2.17A
 PEAK : 2.9A
 Width : 90mil

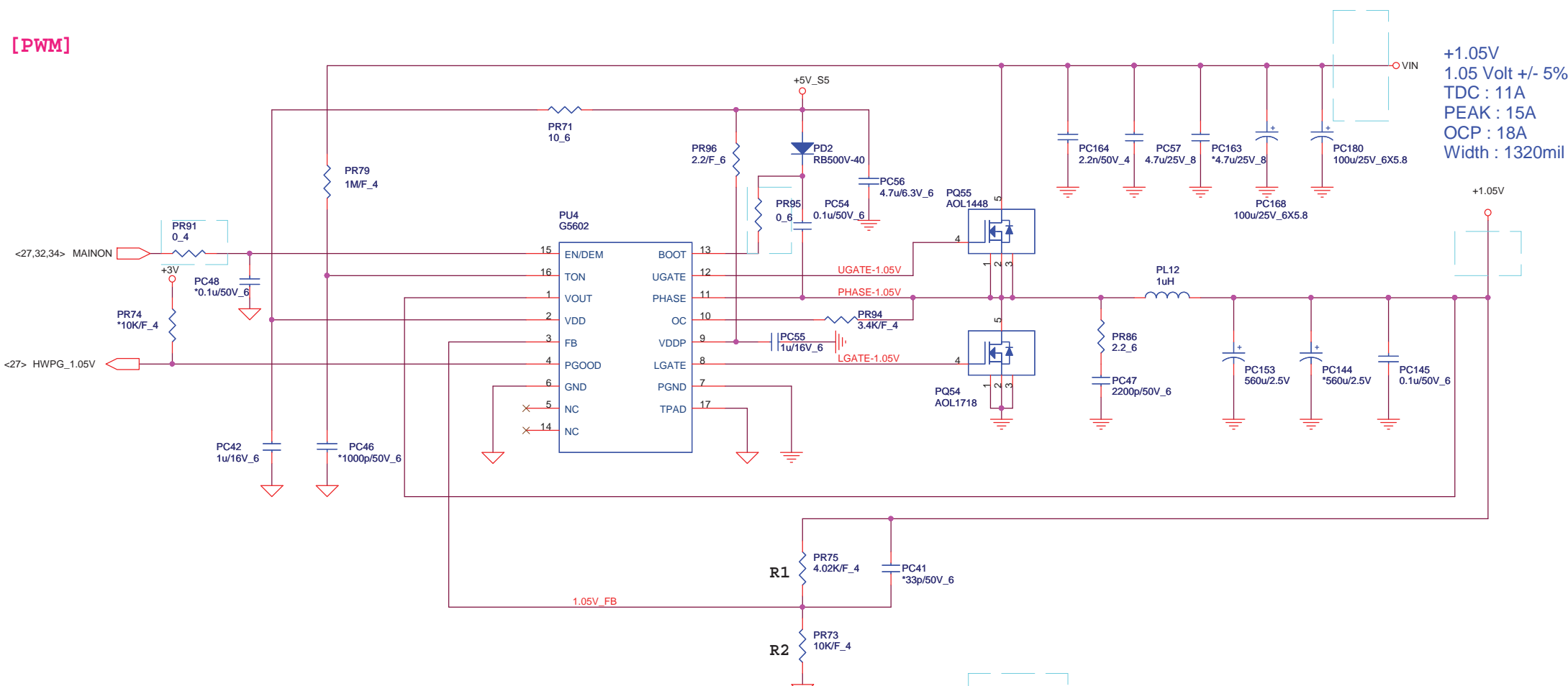
+3V
 TDC : 2.66A
 PEAK : 3.6A
 Width : 120mil

+3V_S5
 TDC : 0.23
 PEAK : 0.3A
 Width : 20mil

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	SYSTEM 5V/3V (RT8206)	1A
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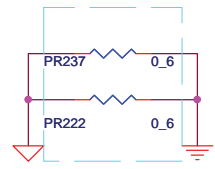
[PWM]




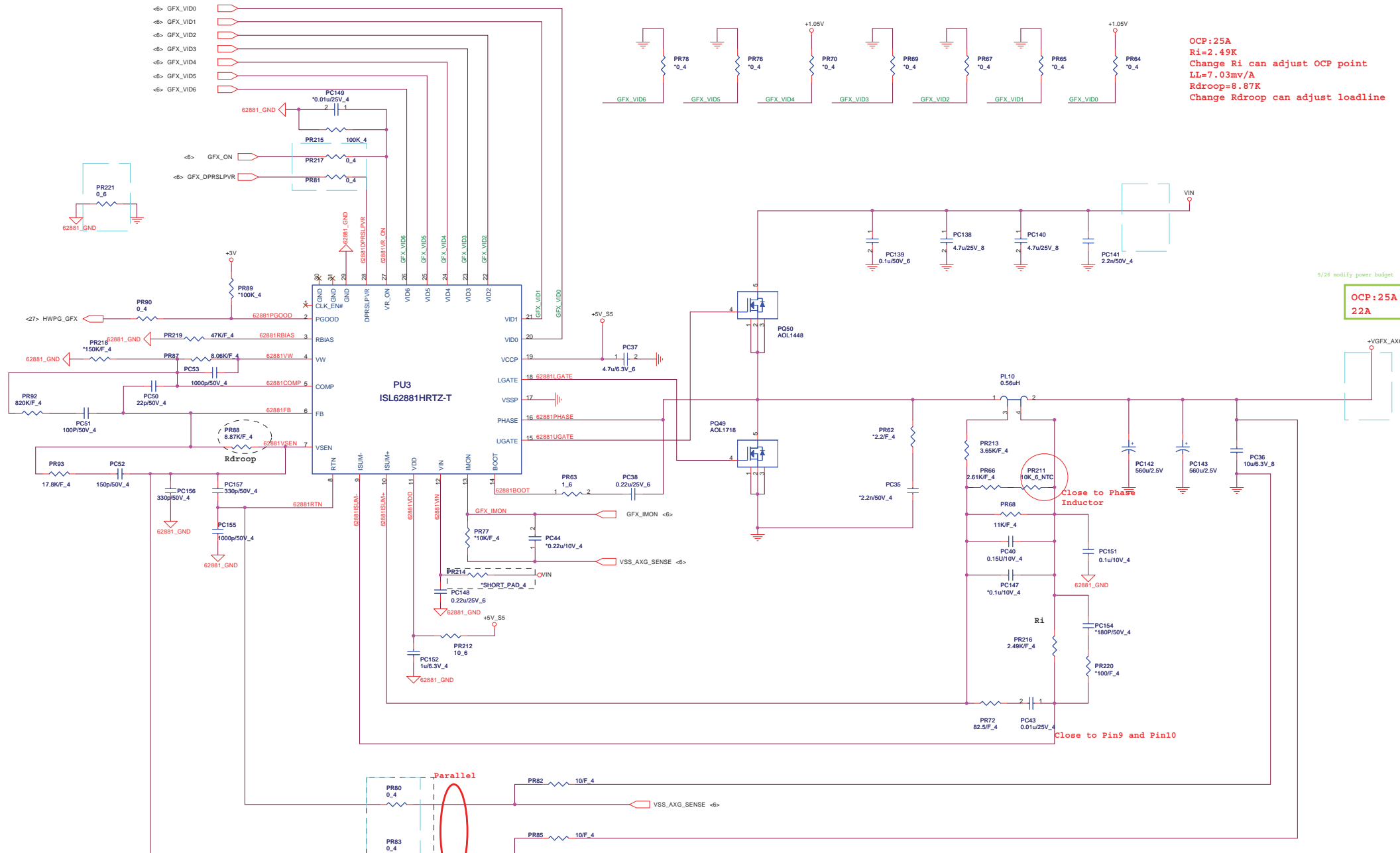
+1.05V
 1.05 Volt +/- 5%
 TDC : 11A
 PEAK : 15A
 OCP : 18A
 Width : 1320mil

$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO1718 $R_{dson} = 3 \sim 4.3m\Omega$
 $I (ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.647A$
 $RILIM = 4.3m\Omega * 18 - 1.823 / 20uA = 3.477K\Omega$
 $I (choke)\ peak = 21.647A$



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OCP:25A
 Ri=2.49K
 Change Ri can adjust OCP point
 LL=7.03mv/A
 Rdroop=8.87K
 Change Rdroop can adjust loadline

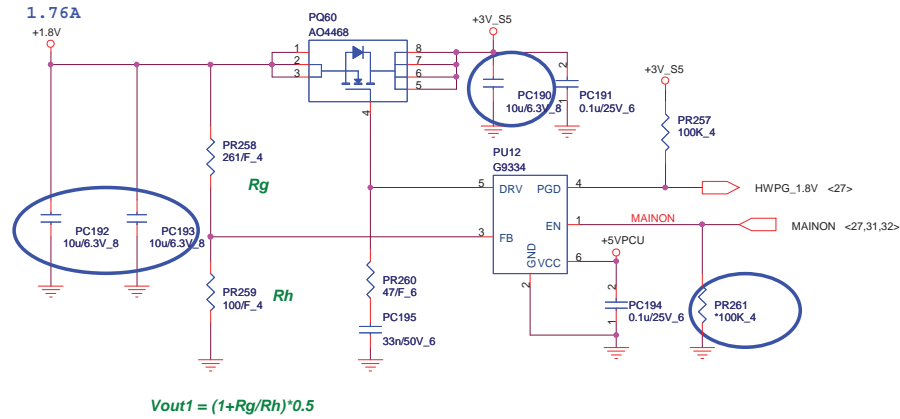
5/26 modify power budget.

OCP:25A
 22A

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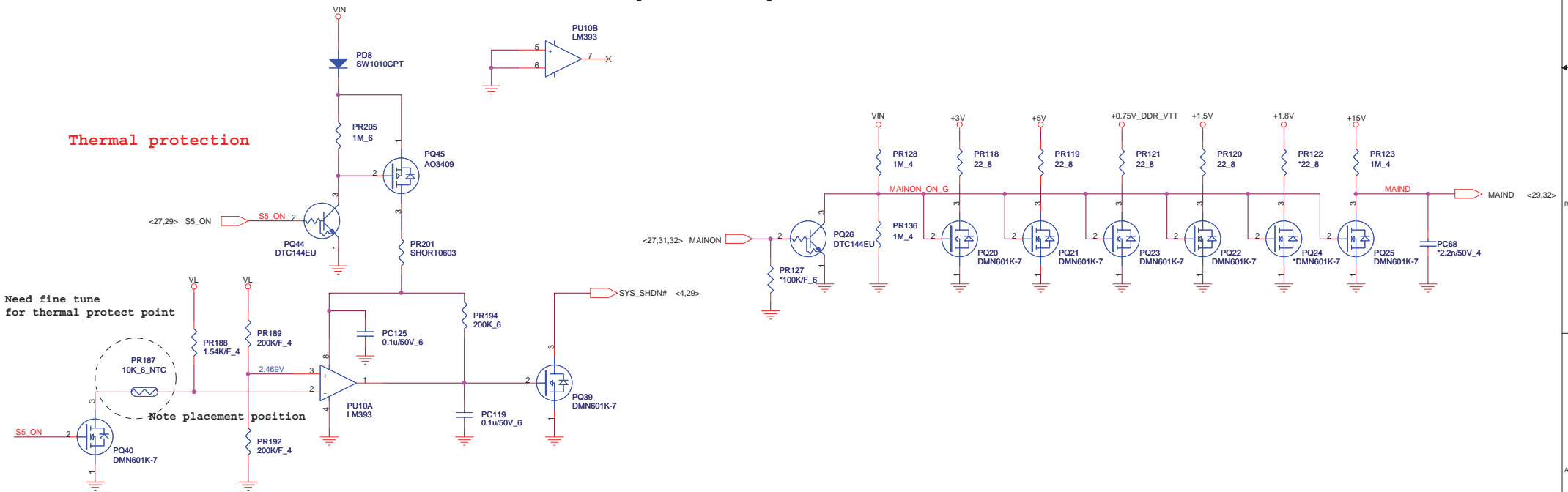
1.Level 1 Environment-related Substances should NEVER be Used.
 2.Purchase Ink, paints, wire rodday and Soldering resins only from the business Partners that Sony approves as Green Partners.

+1.8V
 1.8 Volt +/- 5%
 TDC : 0.76A
 PEAK : 1.01A
 Width : 40mil




For EC control thermal protection (output 3.3V)

Thermal protection



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		1 / 7 / 7 modify		

CHANGE LIST		DATE	DESCRIPTION
2024	1.1	2024-01-01	Initial release of the BIOS code.
2024	1.2	2024-01-15	Added support for SATA drives.
2024	1.3	2024-02-01	Fixed a bug in the boot sequence.
2024	1.4	2024-02-15	Added support for USB drives.
2024	1.5	2024-03-01	Improved the boot speed.
2024	1.6	2024-03-15	Added support for network booting.
2024	1.7	2024-04-01	Fixed a security vulnerability.
2024	1.8	2024-04-15	Added support for RAID configurations.
2024	1.9	2024-05-01	Improved the error handling.
2024	1.10	2024-05-15	Added support for virtual machines.
2024	1.11	2024-06-01	Fixed a bug in the memory management.
2024	1.12	2024-06-15	Added support for secure boot.
2024	1.13	2024-07-01	Improved the power management.
2024	1.14	2024-07-15	Added support for remote management.
2024	1.15	2024-08-01	Fixed a bug in the BIOS update process.
2024	1.16	2024-08-15	Added support for advanced BIOS settings.
2024	1.17	2024-09-01	Improved the overall system stability.
2024	1.18	2024-09-15	Added support for new hardware components.
2024	1.19	2024-10-01	Fixed a bug in the boot loader.
2024	1.20	2024-10-15	Added support for multi-boot configurations.
2024	1.21	2024-11-01	Improved the BIOS firmware security.
2024	1.22	2024-11-15	Added support for advanced networking options.
2024	1.23	2024-12-01	Fixed a bug in the BIOS initialization.
2024	1.24	2024-12-15	Added support for custom BIOS themes.
2024	1.25	2025-01-01	Final release of the BIOS code.

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