ZQ2B SOLE UMA SYSTEM DIAGRAM

AMD Smarter Choice
Danube Platform
(Main Stream)

VER : 1A

BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Sansung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

IV@ -----> iGPU
SP@ -----> Option Notice
SIDE@ -----> SidePort VRAM
GA@ ----> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

- CHARGER (ISL88731A) PAGE 26
- AMD CPU CORE (ISL6265) PAGE 28 — CPU
- NB_CORE (UP6111AQDD) PAGE 30 — NB
- 0.9V/DDR 1.5V(RT8207) PAGE 31
- SYSTEM 5V/3V (RT8206) PAGE 27
- 1.1V(UP6111AQDD) PAGE 29
- Discharge /Thermal protec PAGE 32

DDR3- SODIMM1 PAGE 5 — DDR3 channel A
DDR3- SODIMM2 PAGE 5 — DDR3 channel B

AMD Champlain
S1G4 Processor
35mm X 35mm
638P (PGA) 35W
PAGE 2,3,4

CPU THERMAL SENSOR (Reserve Only) PAGE 4
PWM FAN SCH. PAGE 24 — CPU (PROCHOT), E.C. (CPUFAN#)

CPU_CLK, NBGFX_CLK, NBGPP_CLK, SBLINK_CLK

From SB CLK GEN
SB820M PAGE 10
CLK_PCI_775, PCLK_DEBUG
25MHz, 32.768KHz

CPU SideBand TemperatureSense I2C

HT3
1.8GHz

NORTH BRIDGE
RS880M GFX Engine: 500MHz
A11
21mm X 21mm, 528pin BGA
TDP: 13W
0.95 ~ 1.1V
PAGE 6,7,8,9

PCI-Expresss
P0 — **LAN** Atheros PCIE-LAN AR8151 (10/100/1000) PAGE 17 — 25MHz
RJ45 PAGE 17
P2 — **Mini PCI-E Card** (Wireless LAN) PAGE 18

Side Port — **gDDR3 VRAM** DDR III-800MHz PAGE 6
HDMI — **HDMI** PAGE 16
CRT — **CRT** PAGE 15
LVDS — **LVDS** PAGE 23

A-LINK

SOUTH BRIDGE
SB820M
A12
23mm X 23mm, 605pin BGA
No PCI I/F
TDP: 4.9W
PAGE 10,11,12,13, 14

SATA - HDD PAGE 19 — SATA0 150MB 3 Gb/s
SATA - ODD PAGE 19 — SATA1 150MB 3 Gb/s

P0 — **USB2.0 Port** on board x1 PAGE 30
P9 — **Blue Tooth** PAGE 22
P13 — **Web-Camera** PAGE 15
P4 — **Mini Card** WLAN & Debug PAGE 18 — PCLK_DEBUG
P10 — **CardReader** AU6347 PAGE 21 — 12MHz

P8, 11, 12
USB BOARD USB2.0 Ports x3 PAGE 22
Power BOARD PAGE 22
Switch BOARD PAGE 22
There are three Daughter boards.

LPC, Azalia

CLK_PCI_775
Winbond KBC NPCE781L & Green Adapter PAGE 25
CPU SideBand TemperatureSense I2C

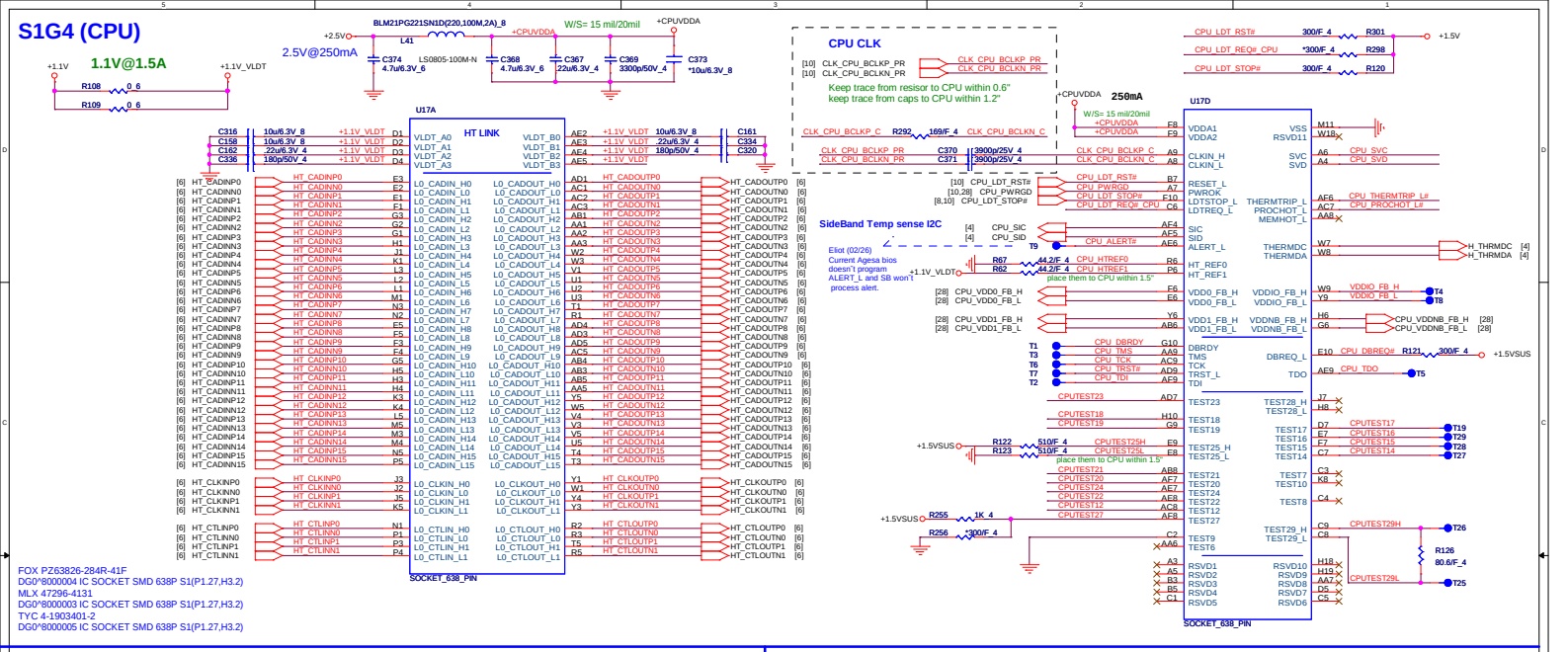
Audio CODEC RTL ALC271X PAGE 20

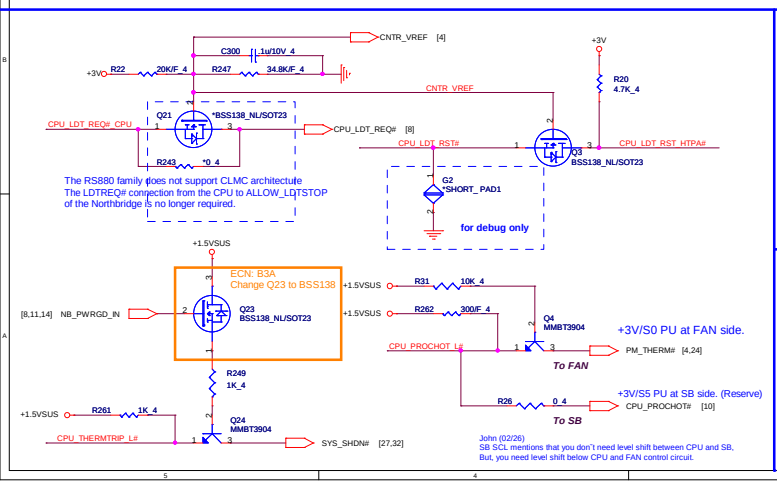
- Green ADP. PAGE 25
- Keyboard TouchPad PAGE 24
- SPI ROM PAGE 25
- Digital MIC PAGE 15 & 20
- AUDIO CONN (H.P./ MIC) PAGE 20
- Speaker CN PAGE 20

SSID: 035E
SVID: 1025

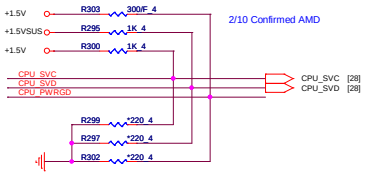
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Thursday, March 04, 2010	Sheet 1 of 36	





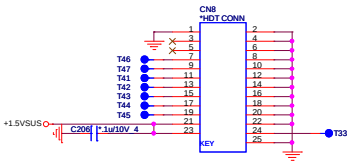
Serial VID

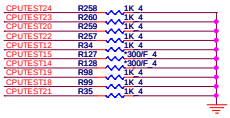


VFIX MODE — VID Override Circuit

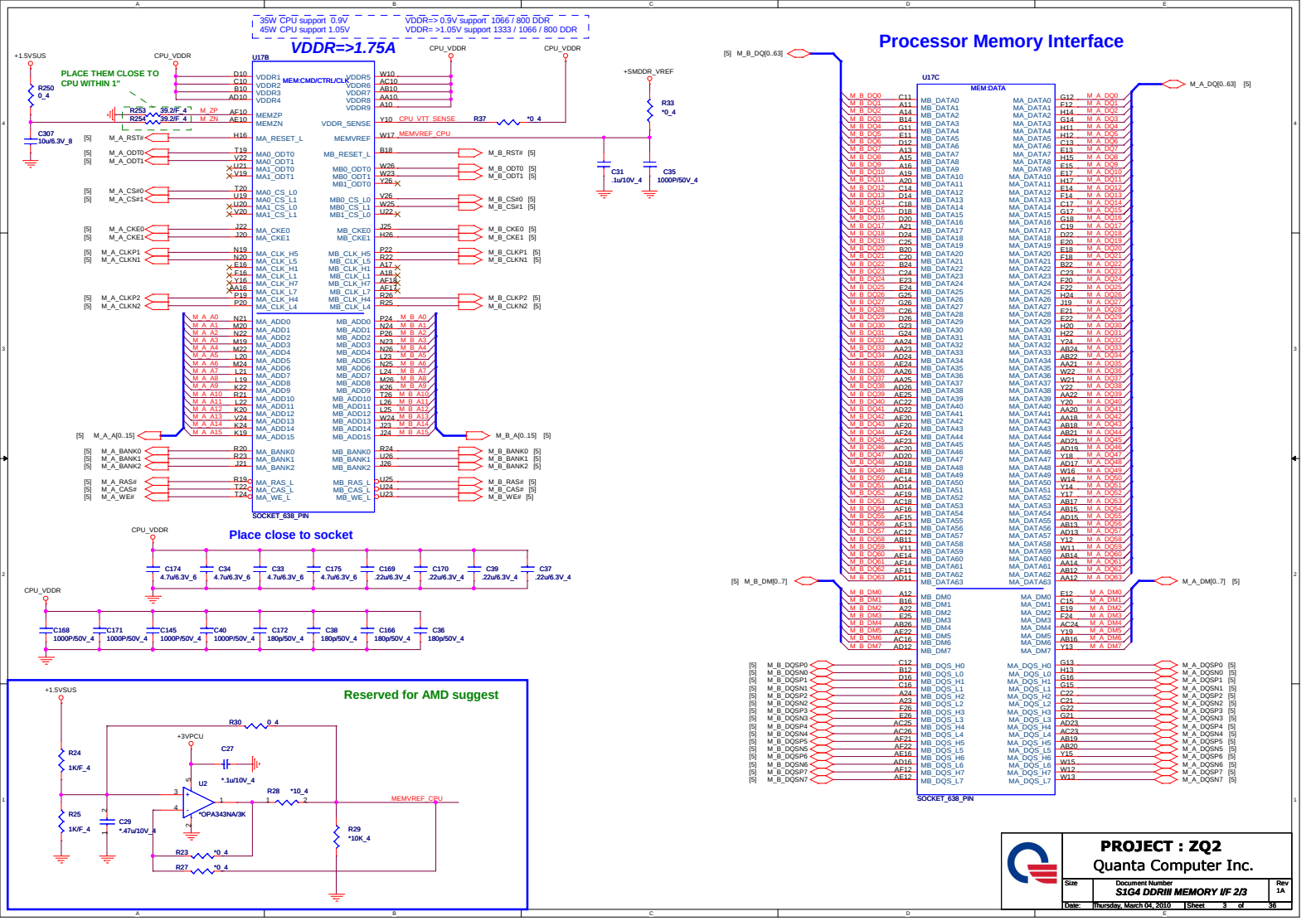
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

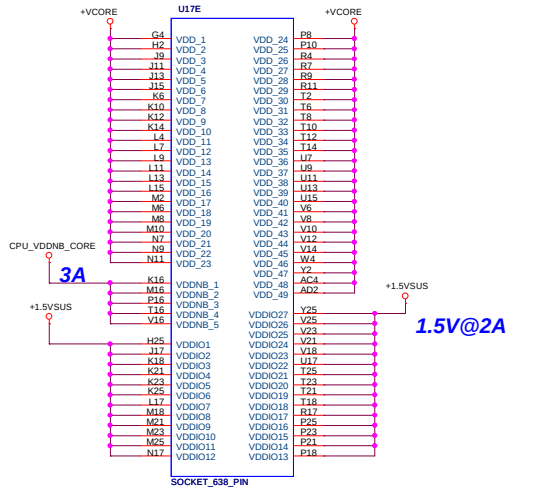
HDT Connector

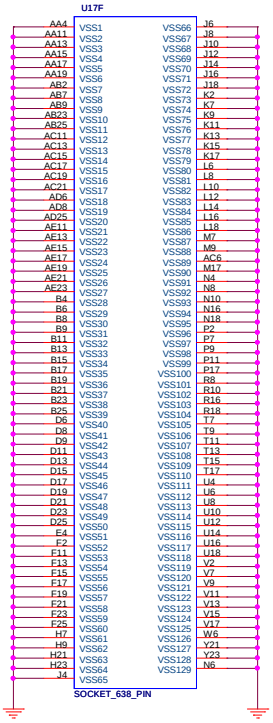


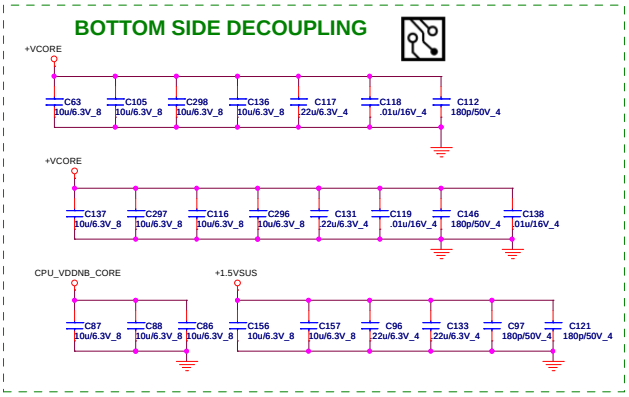


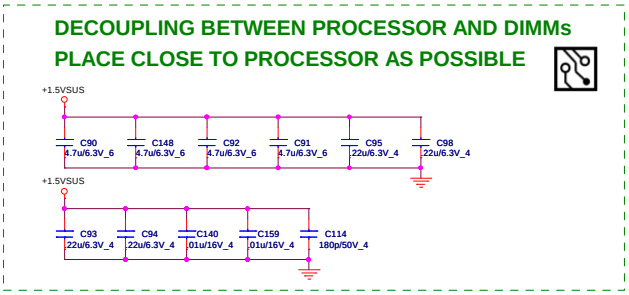
PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: S1G4 HT,CTL I/F 1/3 — Rev: 1A
Date: Thursday, March 04, 2010	Sheet 2 of 36

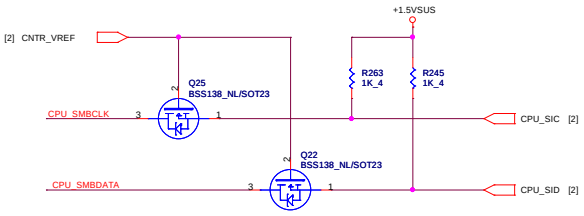

35W CPU support 0.9V
45W CPU support 1.05V
VDDR=> 0.9V support 1066 / 800 DDR
VDDR=> >1.05V support 1333 / 1066 / 800 DDR
VDDR=>1.75A
Processor Memory Interface
PLACE THEM CLOSE TO CPU WITHIN 1"
Place close to socket
Reserved for AMD suggest
SOCKET_638_PIN
PROJECT : ZQ2
Quanta Computer Inc.
S1G4 DDRIII MEMORY I/F 2/3
Thursday, March 04, 2010



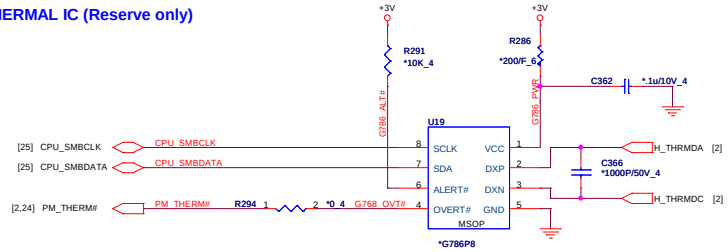






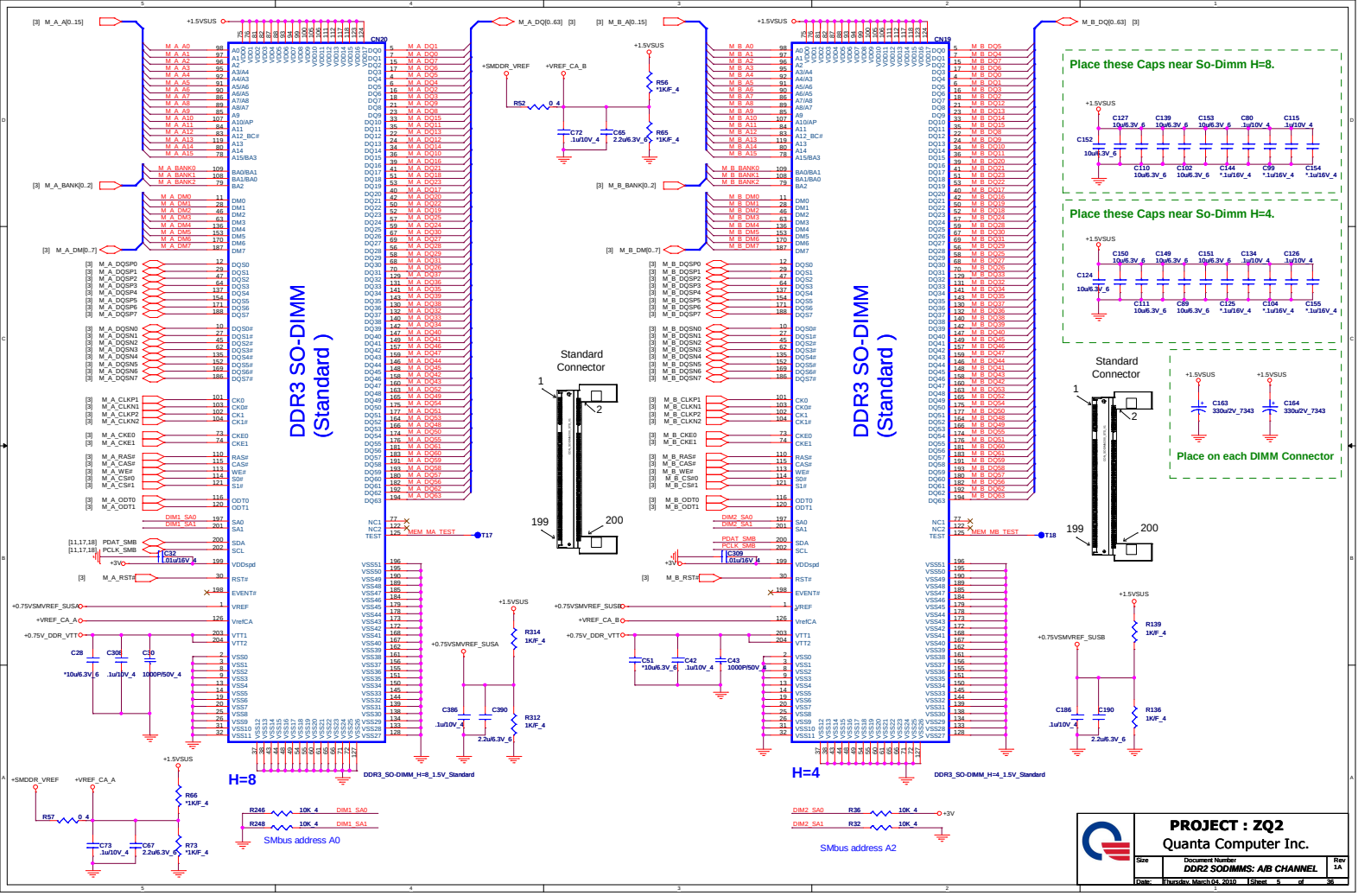


PROCESSOR POWER AND GROUND

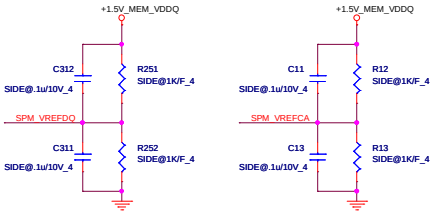


PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date: Thursday, March 04, 2010	Sheet 4 of 36	


DDR3 SO-DIMM (Standard)
H=8
H=4
Standard Connector
Place these Caps near So-Dimm H=8.
Place these Caps near So-Dimm H=4.
Place on each DIMM Connector
SMbus address A0
SMbus address A2
PROJECT : ZQ2
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Thursday, March 04, 2010

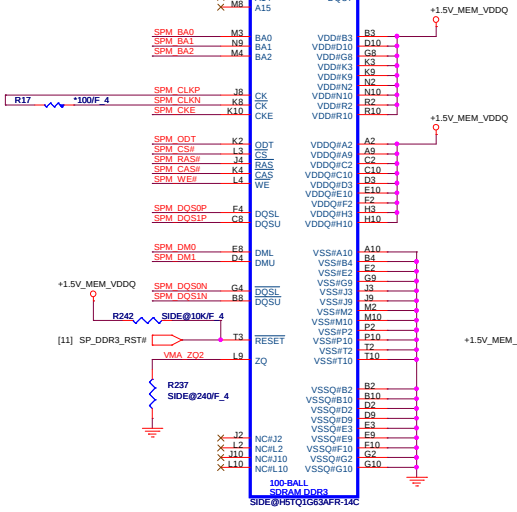
SIDE PORT

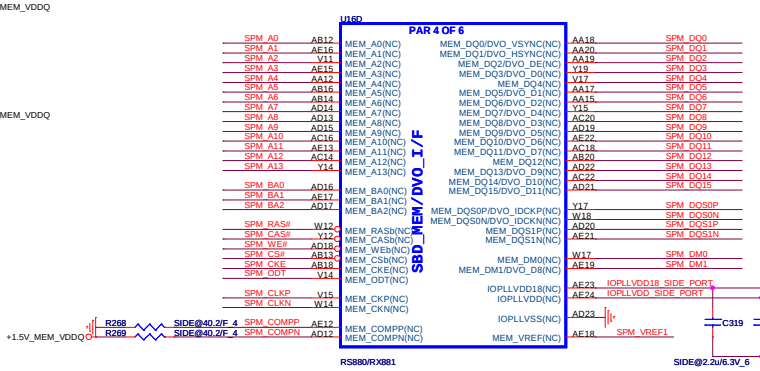


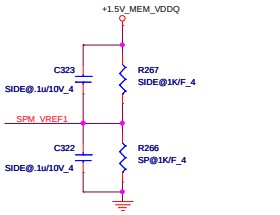
Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

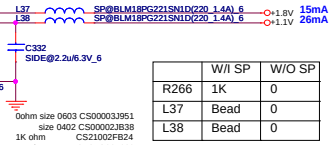
This block is for Side-Port only







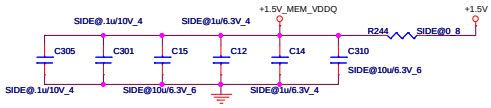
IOPLLVDD18 - memory PLL
not applicable to RX881



0ohm size 0603 CS00003J951
size 0402 CS00002JB38
1K ohm CS21002FB24
Bead CX8PG221003

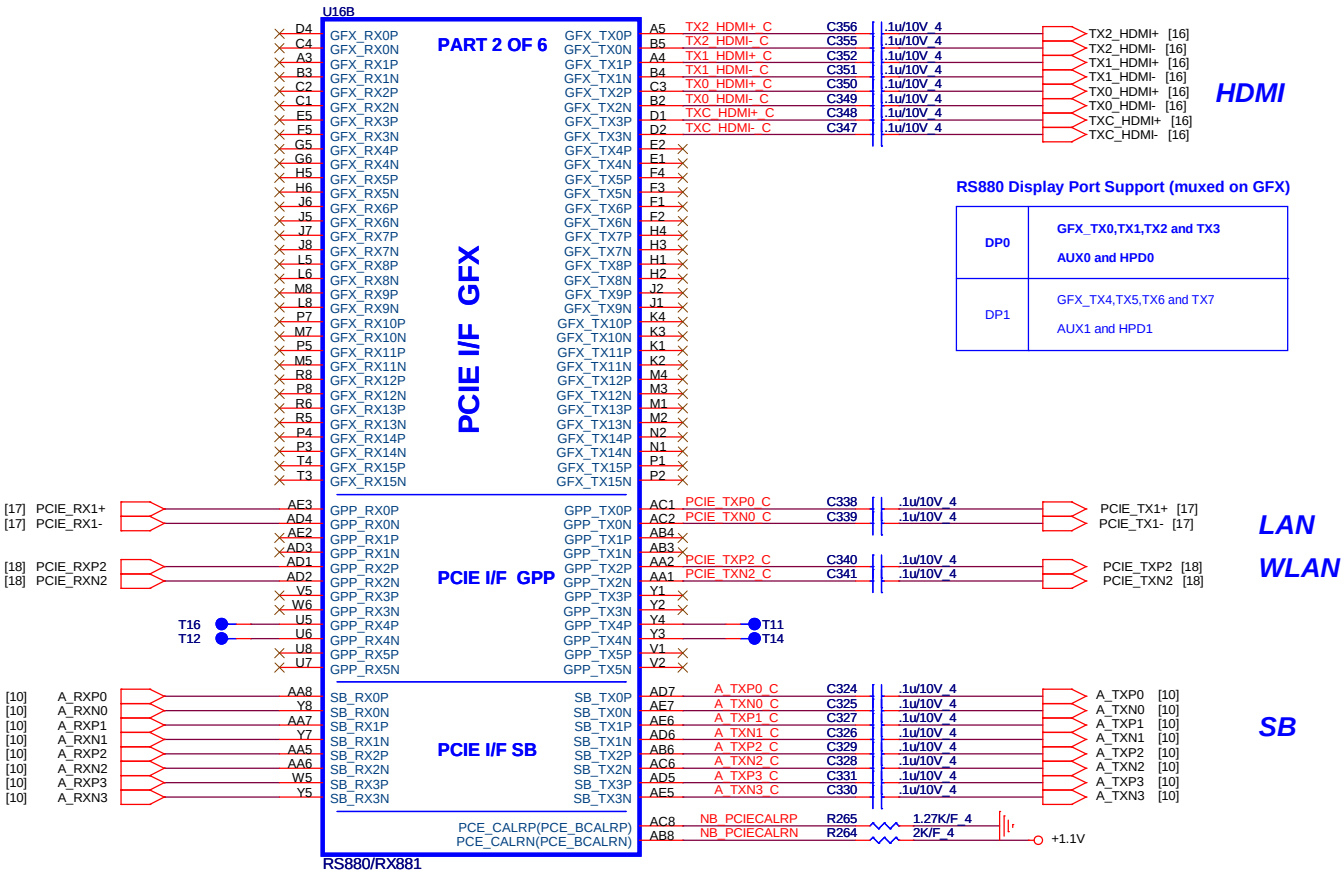
	W/I SP	W/O SP
R266	1K	0
L37	Bead	0
L38	Bead	0

40 mil~50 mil



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Thursday, March 04, 2010	Sheet 6 of 36	



PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number		Rev
	RS880M-PCIE I/F 2/4		1A
Date:	Thursday, March 04, 2010	Sheet 7 of	36

For Check list JTAG

R279 *4.7K_4 NB_PWRGD_IN
+3V
R88 *4.7K_4 INT_EDIDDATA
R96 *4.7K_4 INT_EDIDCLK
+3V
R94 *4.7K_4 HDMI_DDC_DATA

For A11 version

(02/10) Don`t need 49.9 ohm PD.

R47 *49.9/F_4 CLK_SBLINKP
R48 *49.9/F_4 CLK_SBLINKN

All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb

U18C
PART 3 OF 6
RS880/RX881

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
AVDD1(NC)
AVDD2(NC)
AVDDDI(NC)
AVSSDI(NC)
AVDDQ(NC)
AVSSQ(NC)
C_Pr(DFT_GPIO5)
Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)

VGA
[15] INT_CRT_RED
[15] INT_CRT_GRE
[15] INT_CRT_BLU
R102 140/F_4
R103 150/F_4
R104 150/F_4
RED(DFT_GPIO0)
REDb(NC)
GREEN(DFT_GPIO1)
GREENb(NC)
BLUE(DFT_GPIO3)
BLUEb(NC)
[15] INT_CRT_HSYNC
[15] INT_CRT_VSYNC
[15] INT_DDCDATA
[15] INT_DDCCLK
INT_CRT_HSYNC
INT_CRT_VSYNC
DAC_HSYNC(PWM_GPIO4)
DAC_VSYNC(PWM_GPIO6)
DAC_SDA(PCE_TCALRN)
DAC_SCL(PCE_RCALRN)
R79 715/F_6
DAC_RSET_NB
DAC_RSET(PWM_GPIO1)

+1.1V_PLLVDD
+1.8V_PLLVDD18
PLLVDD(NC)
PLLVDD18(NC)
PLLVSS(NC)
20mA +1.8V_VDDA18HTPLL
VDDA18HTPLL
120mA +1.8V_VDDA18PCIEPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2

[10,25] A_RST#_SB
[2,11,14] NB_PWRGD_IN
SYSRESETb
POWERGOOD
LDTSTOPb
ALLOW_LDTSTOP
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

[10] CLK_NB_HTREFP_PR
[10] CLK_NB_HTREFN_PR
HT_REFCLKP
HT_REFCLKN

[10] CLK_NB_REF_CLKP
[10] CLK_NB_REF_CLKN
CLK_NB_REF_CLKP
CLK_NB_REF_CLKN
REFCLK_P(OSCIN/OSCIN)
REFCLK_N(PWM_GPIO3)
R46 4.7K_4
R45 4.7K_4
NBGFX_CLKP
NBGFX_CLKN
GFX_REFCLKP
GFX_REFCLKN
T15
T13
GPP_REFCLKP
GPP_REFCLKN
GPP_REFCLKP
GPP_REFCLKN

[10] CLK_SBLINKP
[10] CLK_SBLINKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)

[15] INT_EDIDDATA
[15] INT_EDIDCLK
I2C_DATA
I2C_CLK
DDC_DATA/AUX0N(NC)
DDC_CLK/AUX0P(NC)
AUX1P(NC)
AUX1N(NC)
[16] HDMI_DDC_DATA
[16] HDMI_DDC_CLK
DDC_DATA & DDC_CLK Not applicable to RX881

[30] +NB_CORE_ON
+NB_CORE_ON
STRP_DATA
RSVD
T74
RS880_AUX_CAL
AUX_CAL(NC)

TXOUT_L0P(NC)
TXOUT_L0N(NC)
TXOUT_L1P(NC)
TXOUT_L1N(NC)
TXOUT_L2P(NC)
TXOUT_L2N(DBG_GPIO0)
TXOUT_L3P(NC)
TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC)
TXOUT_U0N(NC)
TXOUT_U1P(PCIE_RESET_GPIO3)
TXOUT_U1N(PCIE_RESET_GPIO2)
TXOUT_U2P(NC)
TXOUT_U2N(NC)
TXOUT_U3P(PCIE_RESET_GPIO5)
TXOUT_U3N(NC)
LA_DATAP0 [15]
LA_DATAN0 [15]
LA_DATAP1 [15]
LA_DATAN1 [15]
LA_DATAP2 [15]
LA_DATAN2 [15]

TXCLK_LP(DBG_GPIO1)
TXCLK_LN(DBG_GPIO3)
TXCLK_UP(PCIE_RESET_GPIO4)
TXCLK_UN(PCIE_RESET_GPIO1)
LA_CLK [15]
LA_CLK# [15]

VDDLTP18(NC)
VSSLTP18(NC)
+1.8V_VDDLTP18_NB
15mA
VDDLT18_1(NC)
VDDLT18_2(NC)
VDDLT33_1(NC)
VDDLT33_2(NC)
+1.8V_VDDLT_18_NB
300mA
VSSLT1(VSS)
VSSLT2(VSS)
VSSLT3(VSS)
VSSLT4(VSS)
VSSLT5(VSS)
VSSLT6(VSS)
VSSLT7(VSS)

LVDS_DIGON(PCE_TCALRP)
LVDS_BLON(PCE_RCALRP)
LVDS_ENA_BL(PWM_GPIO2)
INT_LVDS_DIGON [15]
INT_DPST_PWM [15]
INT_LVDS_BLON [15]

TMDS_HPD(NC)
HPD(NC)
INT_HDMI_HPD [16]
TVCLKIN(PWM_GPIO5)
SUS_STAT#_NB
R111 *0/short_4
SUS_STAT# [11]
THERMALDIODE_P
THERMALDIODE_N
R112 *3K_4
TESTMODE
TEST_EN
R87 1.8K/F_4

Made provision for external pull-down which is not installed by default. Pulled up externally for bypassing EEPROM strapping and using default values.

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	

INT_CRT_VSYNC R277 3K_4 +3V

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

INT_CRT_HSYNC R276 *SP@3K_4 +3V
R100 SIDE@3K_4

For extrnal EEPROM Debug only

RS780/RX780/RS880

+NB_CORE_ON R278 2K/F_4

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880_AUX_CAL R282 *150/F_4

RS880M --- ADD

+3V L11 BLM18PG221SN1D(220_1.4A)_6 +3V_AVDD_NB
C120 *10u/6.3V_8
C123 2.2U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V L39 BLM18PG221SN1D(220_1.4A)_6 +1.1V_PLLVDD
C359 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V L15 BLM18PG221SN1D(220_1.4A)_6 +1.8V_VDDLTP18_NB
C135 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

+1.8V R86 0_6 +1.8V_AVDDDI_NB
C113 .1u/10V_4
AVDDI-DAC Digital not applicable to RX780

+1.8V L13 BLM18PG221SN1D(220_1.4A)_6 +1.8V_PLLVDD18
C147 *10u/6.3V_8
C128 4.7u/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

L9 BLM18PG221SN1D(220_1.4A)_6 +1.8V_AVDDQ_NB
C108 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

L40 BLM21PG221SN1D(220,100M,2A)_8 +1.8V_VDDLT_18_NB
C360 4.7u/6.3V_6
C357 .1u/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

+1.8V
VDDA18PCIEPLL -PCIE PLL
20mils width
L10 BLM18PG221SN1D _6 +1.8V_VDDA18PCIEPLL
C122 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
20mils width
L14 BLM18PG221SN1D _6 +1.8V_VDDA18HTPLL
C106 2.2U/6.3V_6

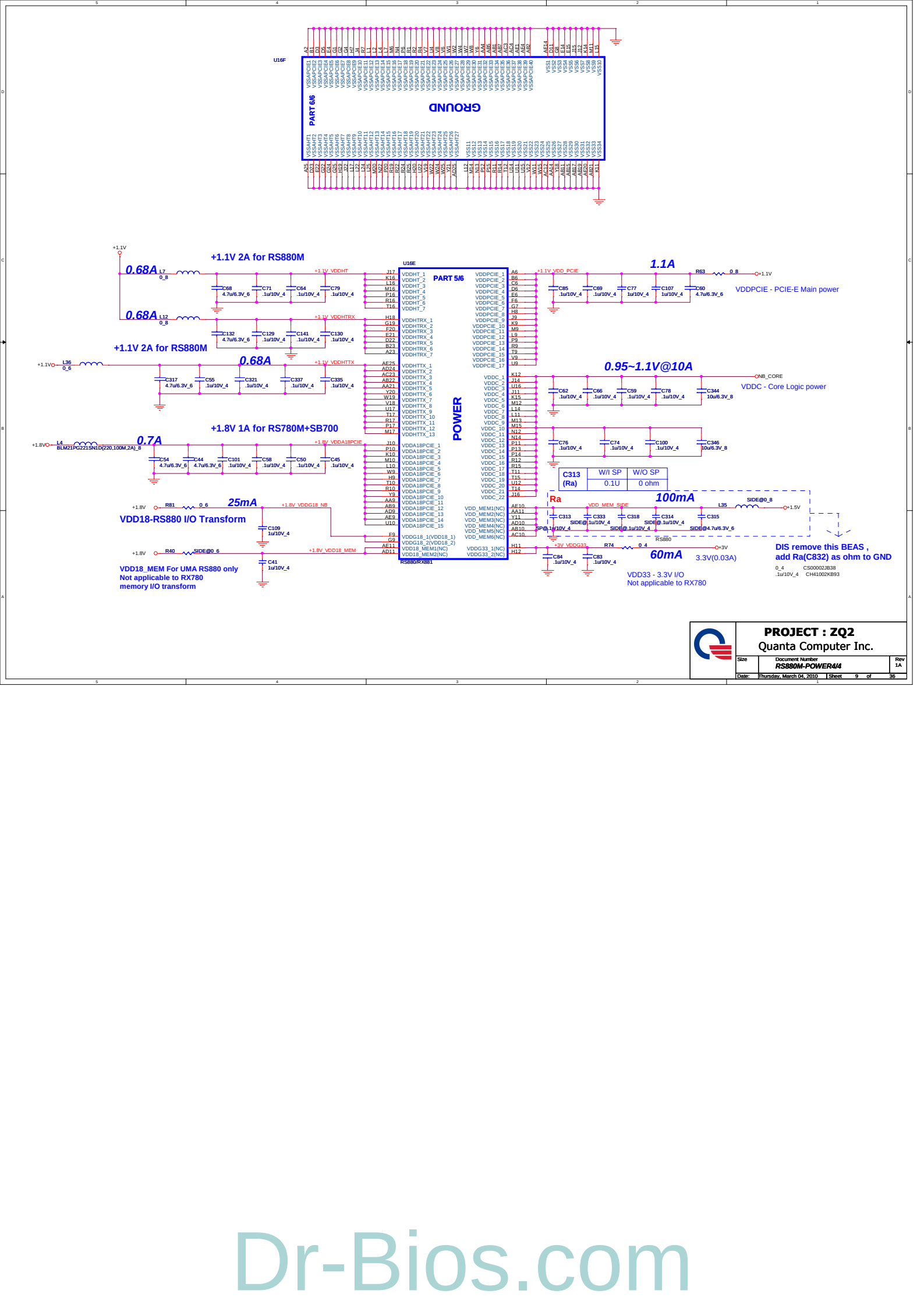
+1.8V
U16 Open Drain 74LVC07
[2,10] CPU_LDT_STOP#
NB_LDT_STOP#
R107 2.2K_4
9/16 need modify PN

DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

R285 1K_4 +1.8V
[2] CPU_LDT_REQ#
R284 *0_4
NB_ALLOW_LDTSTOP
[10] ALLOW_LDTSTOP
R283 0_4

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: RS880M-SYSTEM I/F 3/4	Rev 1A
Date: Thursday, March 04, 2010	Sheet 8 of 36	


U16F
PART 6/6
GROUND
U16E
PART 5/6
POWER
RS880/RX881
+1.1V 2A for RS880M
0.68A
+1.1V_VDDHT
+1.1V_VDDHTRX
+1.1V 2A for RS880M
0.68A
+1.1V_VDDHTTX
+1.8V 1A for RS780M+SB700
0.7A
+1.8V_VDDA18PCIE
25mA
+1.8V_VDDG18_NB
VDD18-RS880 I/O Transform
+1.8V_VDD18_MEM
VDD18_MEM For UMA RS880 only
Not applicable to RX780
memory I/O transform
1.1A
+1.1V_VDD_PCIE
VDDPCIE - PCIE-E Main power
0.95~1.1V@10A
NB_CORE
VDDC - Core Logic power
C313
W/I SP
W/O SP
(Ra)
0.1U
0 ohm
Ra
100mA
SIDE@0_8
+1.5V
RS880
60mA
3.3V(0.03A)
+3V_VDDG33
VDD33 - 3.3V I/O
Not applicable to RX780
DIS remove this BEAS ,
add Ra(C832) as ohm to GND
0_4 CS00002JB38
.1u/10V_4 CH41002KB93
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
RS880M-POWER4/4
Rev
1A
Date: Thursday, March 04, 2010
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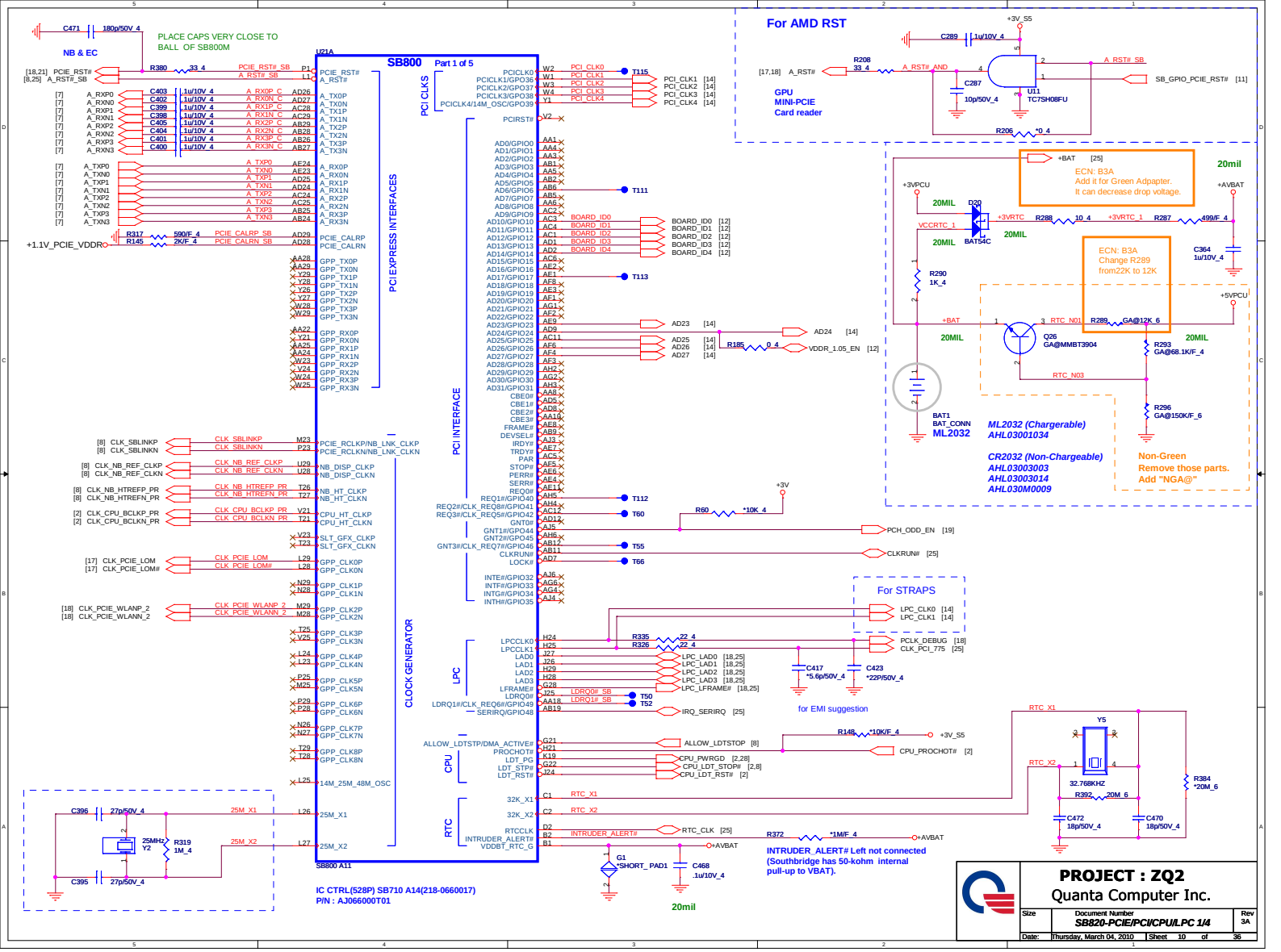

NB & EC
PLACE CAPS VERY CLOSE TO BALL OF SB800M
SB800
Part 1 of 5
PCI EXPRESS INTERFACES
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
For AMD RST
GPU MINI-PCIE Card reader
U11 TC7SH08FU
ECN: B3A Add it for Green Adpapter. It can decrease drop voltage.
ECN: B3A Change R289 from22K to 12K
BAT1 BAT_CONN ML2032
ML2032 (Chargerable) AHL03001034
CR2032 (Non-Chargeable) AHL03003003 AHL03003014 AHL030M0009
Non-Green Remove those parts. Add "NGA@"
For STRAPS
for EMI suggestion
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
PROJECT : ZQ2
Quanta Computer Inc.
SB820-PCIE/PCI/CPU/LPC 1/4
Thursday, March 04, 2010
Sheet 10 of 36

NC only ,Can't be install

+3V_S5
R368 *2.2K_4 SB_TEST0
R217 *2.2K_4 SB_TEST1
R210 *2.2K_4 SB_TEST2

SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer

+3V
R150 2.2K_4 PCLK_SMB
R147 2.2K_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

+3V_S5
R188 10K_4 SB_SMBCLK1
R215 10K_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it

+3V_S5
R153 10K_4 SB_SCLK2
R149 10K_4 SB_SDATA2

+3V
R195 4.7K_4 SUS_STAT#

+3V
R316 8.2K_4 CLK_PCIE_LAN_REQ#
R178 8.2K_4 CLK_PCIE_2_REQ#

JTAG DEBUG

+3V_S5
CN13
C279 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

To Azalia

ACZ_SDOUT R200 33_4 ACZ_SDOUT_AUDIO [20]
C283 *10P/50V_4
ACZ_SYNC R202 33_4 ACZ_SYNC_AUDIO [20]
C284 *10P/50V_4
ACZ_BCLK R203 33_4 ACZ_BITCLK_AUDIO [20]
C285 *10P/50V_4
ACZ_RST# R201 33_4 ACZ_RST#_AUDIO [20]
ACZ_SDIN0 ACZ_SDIN0 [20]

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U21D
SB800
Part 4 of 5

T71 SB_PCI_PME# J2
K1
D3
[25] SUSB# F1
[25] SUSC# SUSC# H1
[25] DNBSWON# F2
[14] SB_PWRGD_IN H5
[8] SUS_STAT# G6
SB_TEST0 B3
SB_TEST1 C4
SB_TEST2 F6
[25] SIO_A20GATE AD21
[25] SIO_RCIN# SIO_RCIN# AE21
T114 LANLINK_STATE# K2
[25] SIO_EXT_SMI# J29
[25] SIO_EXT_SCI# H2
T116 SYS_RST# J1
[17,18] PCIE_WAKE# H6
T117 IR_RX1 F3
T69 SB_THERMTRIP# J6
[2,8,14] NB_PWRGD_IN AC19
[25] ICH_RSMRST# G1

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

USBCLK/14M_25M_48M_OSC
USB_RCOMP
A10 USB_14_48M T110
G19 USB_RCOMP_SB R169 11.8K/F_6

USB_FSD1P/GPIO186 J10
USB_FSD1N H11
USB_FSD0P/GPIO185 H9 USB_FDS12P T63
USB_FSD0N J8 USB_FDS12N T58

USB_HSD13P B12 USBP13+ [15]
USB_HSD13N A12 USBP13- [15]
CAMERA
USB_HSD12P F11 USBP12+ [22]
USB_HSD12N E11 USBP12- [22]
USBX3 board
USB_HSD11P E14 USBP11+ [22]
USB_HSD11N E12 USBP11- [22]
USBX3 board
USB_HSD10P J12 USBP10+ [21]
USB_HSD10N J14 USBP10- [21]
Card reader
USB_HSD9P A13 USBP9+ [22]
USB_HSD9N B13 USBP9- [22]
BLUETOOTH
USB_HSD8P D13 USBP8+ [22]
USB_HSD8N C13 USBP8- [22]
USBX3 board
USB_HSD7P G12
USB_HSD7N G14
USB_HSD6P G16
USB_HSD6N G18
USB_HSD5P D16
USB_HSD5N C16
USB_HSD4P B14 USBP4+ [18]
USB_HSD4N A14 USBP4- [18]
WLAN Min-Card
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17 USBP1+ T54
USB_HSD1N A17 USBP1- T53
USB_HSD0P A16 USBP0+ [22]
USB_HSD0N B16 USBP0- [22]

EHCI3/ OHCI3
EHCI2/ OHCI2
EHCI1/ OHCI1

USB 2.0

On Board USB Connector
Only USB Port0 can be configured as debug port.

[10] SB_GPIO_PCIE_RST# SB_GPIO_PCIE_RST# AB21
[17] CLK_PCIE_LAN_REQ# CLK_PCIE_LAN_REQ# AC18
T51 SB_GPIO59 AE20
[20] SPKR AE19
[5,17,18] PCLK_SMB PCLK_SMB AD22
[5,17,18] PDAT_SMB PDAT_SMB AE22
SB_SMBCLK1 F5
SB_SMBDATA1 F4
[18] CLK_PCIE_2_REQ# AH21
AB18
E1
[6] SP_DDR3_RST# AJ21
H8
D5
D7
G5
K3
T109 E_SB_OSC AA20

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

GPIO

T59 Eliot (02/26) Current Agesa bios doesn't program ALERT_L and SB won't process alert.
[22] OC_7# H3
[22] OC_6# SB_PM_THERM# D1
[22] OC_4# E6
SB_JTAG_TDO D4
SB_JTAG_TCK E8
SB_JTAG_TDI F7
SB_JTAG_RST# F8

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

USB OC

HD audio interface is +3VS5 voltage

ACZ_BCLK M3
ACZ_SDOUT N1
ACZ_SDIN0 L2
M2
M1
M4
N2
ACZ_SYNC
ACZ_RST# P2
[14] ACZ_SDOUT

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_GPIO195
SDA3_LV/GPIO196 E26 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197 F25 T48
EC_PWM1/EC_TIMER1/GPIO198 F22
EC_PWM2/EC_TIMER2/GPIO199 F22 GPIO199 [14]
EC_PWM3/EC_TIMER3/GPIO200 E21 GPIO200 [14]

[02/22] AMD FAE and checklist request PL.

+3V_S5
R197 10K_4 GBE_COL
R191 10K_4 GBE_CRS
R182 10K_4 GBE_MDIO
R196 10K_4 GBE_RXERR
R190 10K_4 GBE_PHY_INTR

T1 GBE_COL
T4 GBE_CRS
L6 GBE_MDCK
L5 GBE_MDIO
T9 GBE_RXCLK
U1 GBE_RXD3
U3 GBE_RXD2
T2 GBE_RXD1
U2 GBE_RXD0
T5 GBE_RXCTL/RXDV
V5 GBE_RXERR
P5 GBE_TXCLK
M5 GBE_TXD3
P9 GBE_TXD2
T7 GBE_TXD1
P7 GBE_TXD0
M7 GBE_TXCTL/TXEN
H4 GBE_PHY_PD
M9 GBE_PHY_RST#
V7 GBE_PHY_INTR

GBE LAN

T49 ADP_PRES0 E23
E24
F21
G29
D27
F28
F29
E27

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

EMBEDDED CTRL

Check list
SB_GPIO195 R146 10K_4
SB_GPIO196 R144 10K_4

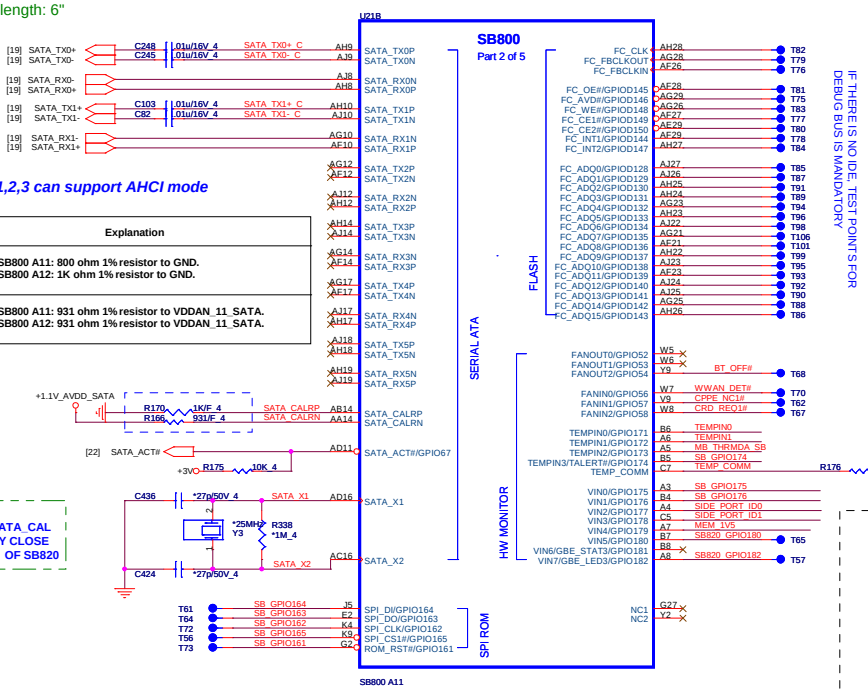
SB800 A11

PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number SB820-ACPI/GPIO/USB 2/4
Rev 1A
Date: Thursday, March 04, 2010 Sheet 11 of 36

Max trace length: 6"

SATA HDD

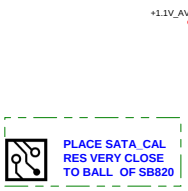
SATA ODD



SATA PORT 0,1,2,3 can support AHCI mode

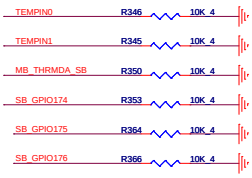
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

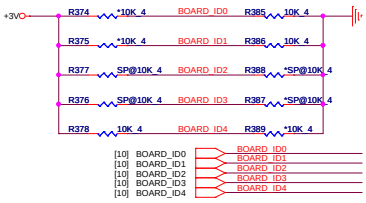


IF THERE IS NO IDE TEST POINTS FOR DEBUG BUS IS MANDATORY

Check list

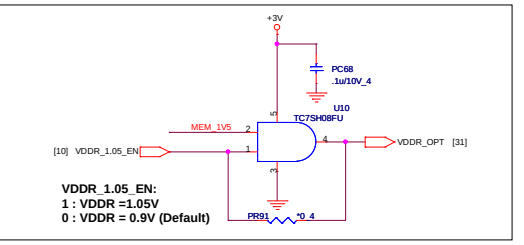


BOM check

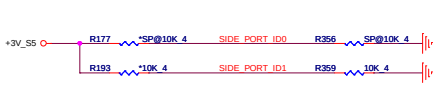


	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	W/I	W/O
ID3	JM	JV
ID4	6L	8L

Sideport



VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)



	1	0
ID0	SAM	HYU
ID1	RSV	RSV

DDR3 Sideport Memory Device

Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A

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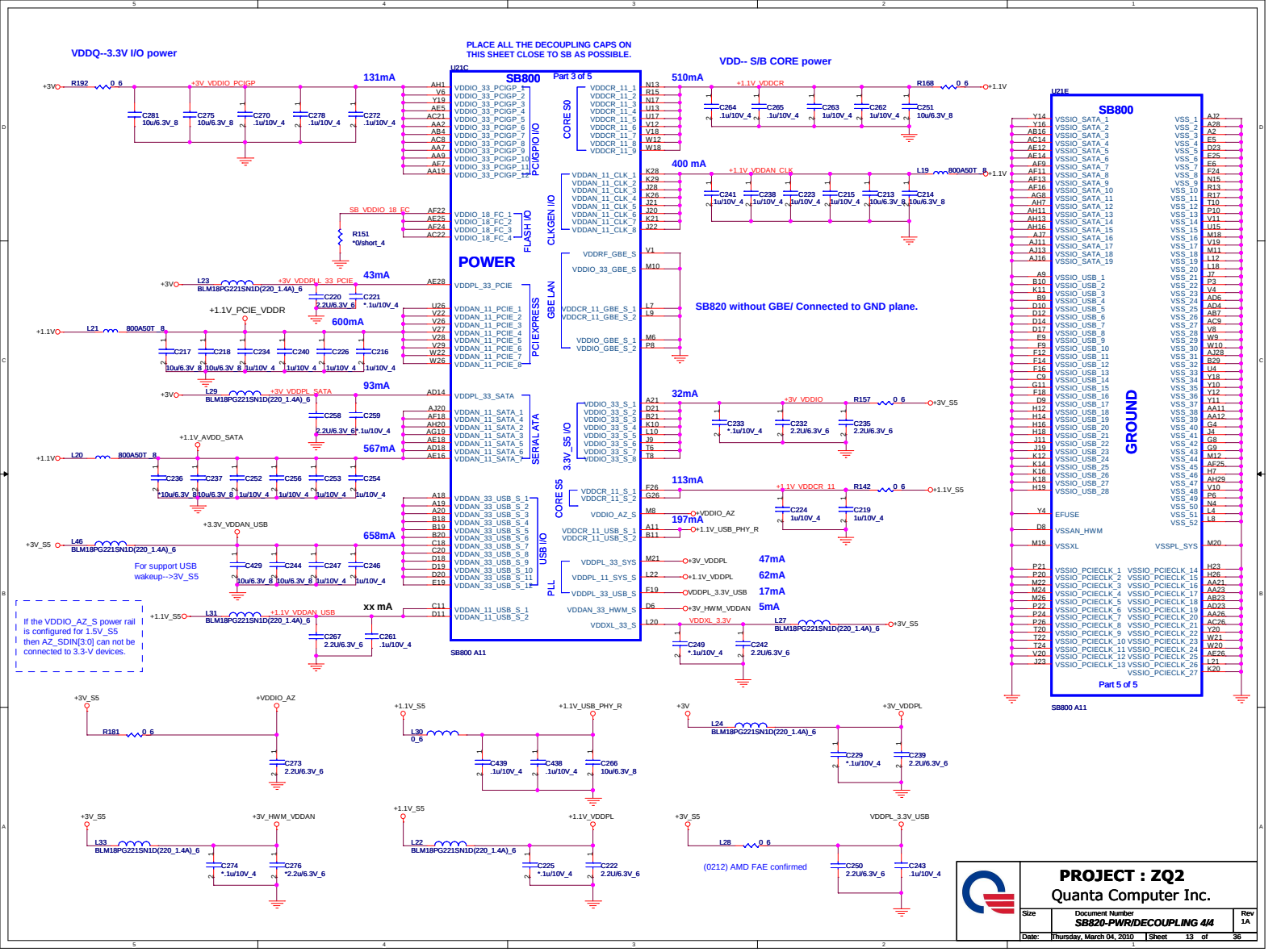
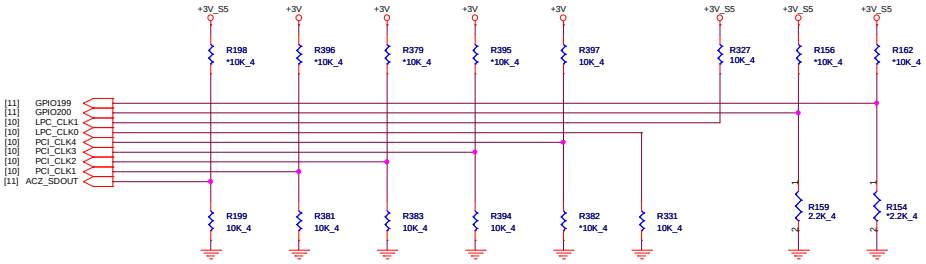

VDDQ--3.3V I/O power
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
VDD-- S/B CORE power
SB800
Part 3 of 5
POWER
131mA
43mA
+1.1V_PCIE_VDDR
600mA
93mA
567mA
+1.1V_AVDD_SATA
658mA
+3.3V_VDDAN_USB
For support USB wakeup-->3V_S5
xx mA
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.
510mA
400 mA
SB820 without GBE/ Connected to GND plane.
32mA
113mA
197mA
47mA
62mA
17mA
5mA
(0212) AMD FAE confirmed
SB800
Part 5 of 5
GROUND
PROJECT : ZQ2
Quanta Computer Inc.
SB820-PWR/DECOUPLING 4/4
Thursday, March 04, 2010
13 of 36

REQUIRED STRAPS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

SB820M is supported Gen.1 mode only.

For internal clock GEN.

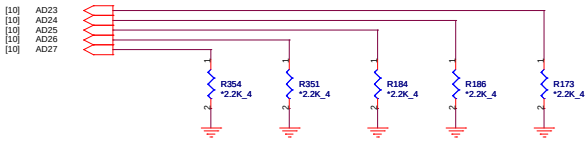


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

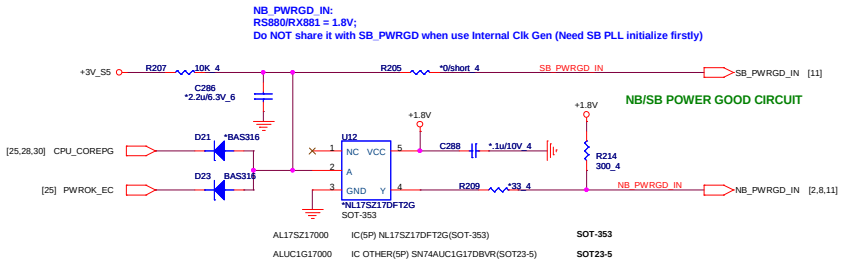
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A

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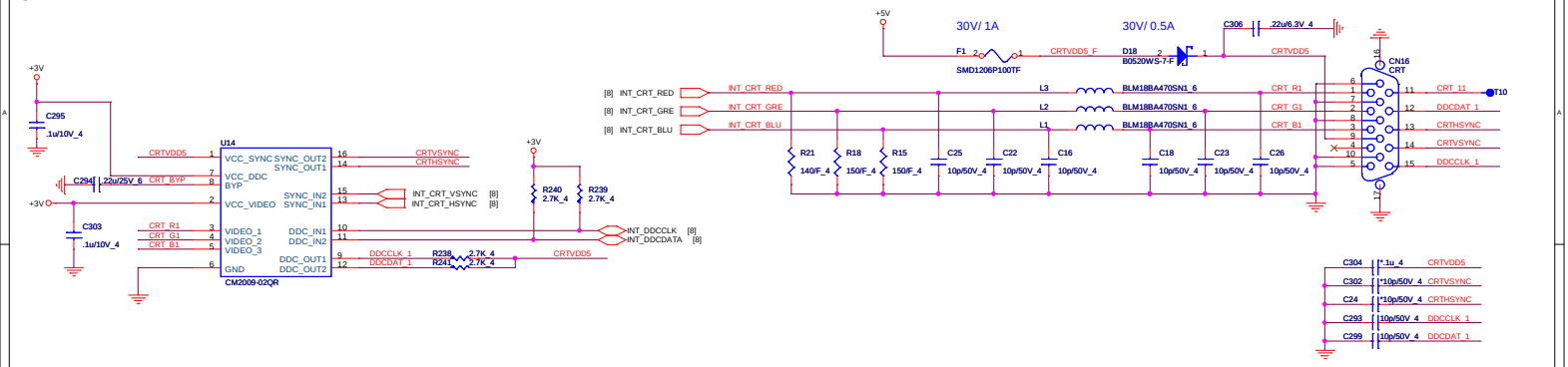
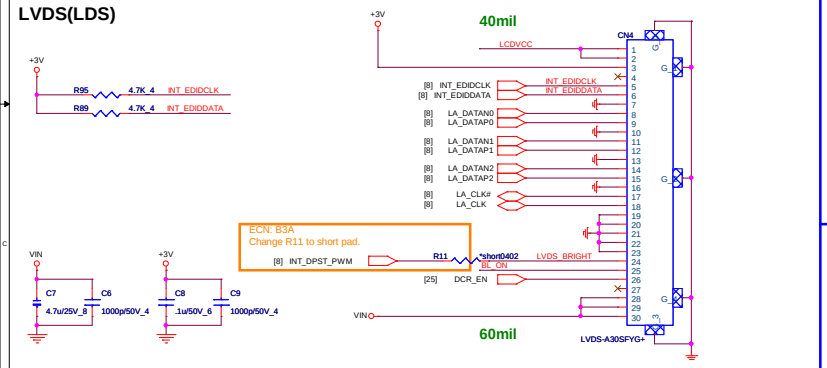
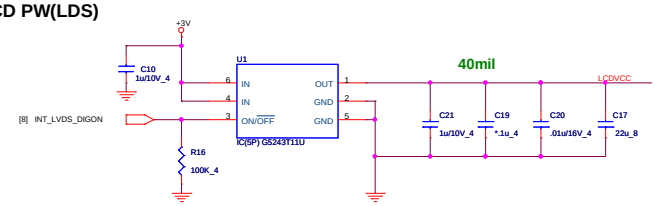
CRT



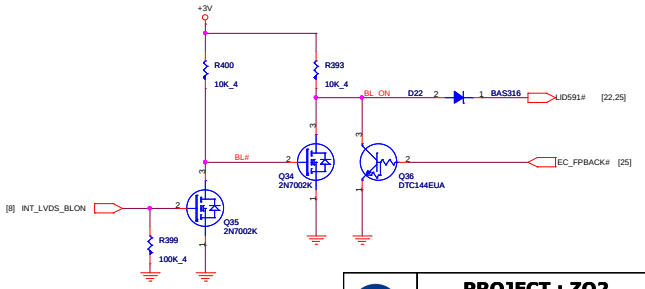
LVDS(LDS)



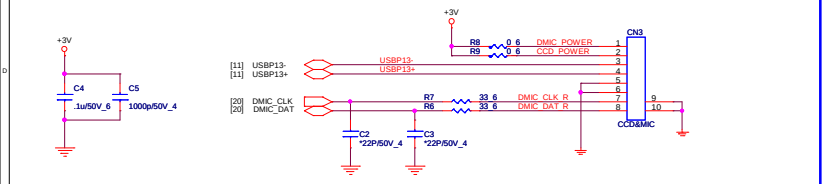
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	3A

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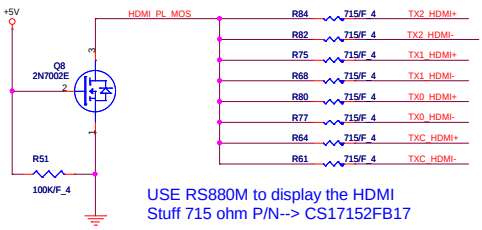
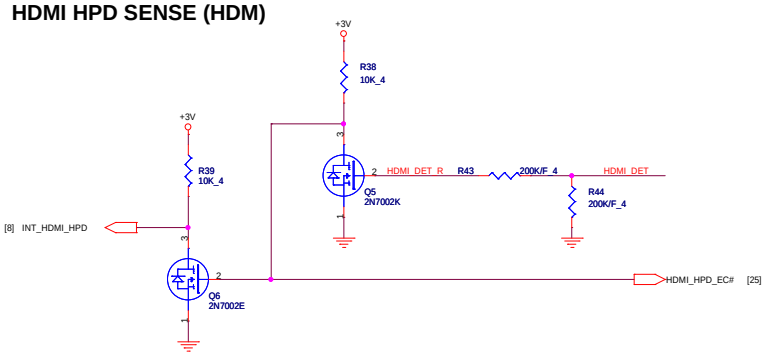
HDMI (HDM)

Close to HDMI Connector

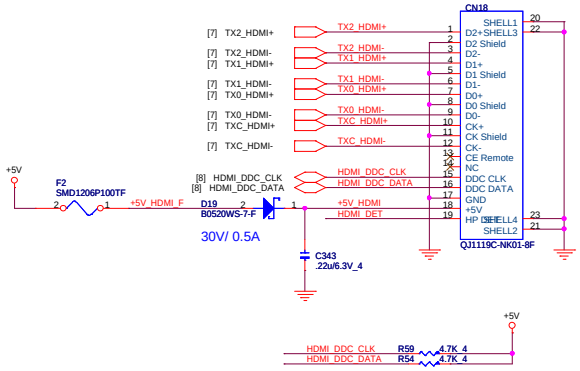


USE RS880M to display the HDMI
Stuff 715 ohm P/N--> CS17152FB17

HDMI HPD SENSE (HDM)

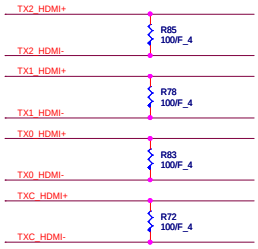


HDMI PORT (HDM)



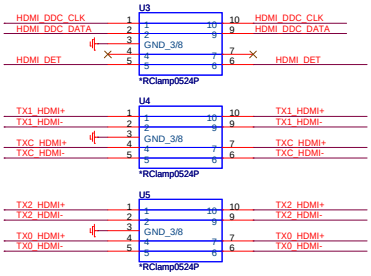
EMI reserve for HDMI(EMC)

Close connector



ESD Protect (EMC)

close to HDMI connector



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Quanta Computer Inc.

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	HDMI	1A
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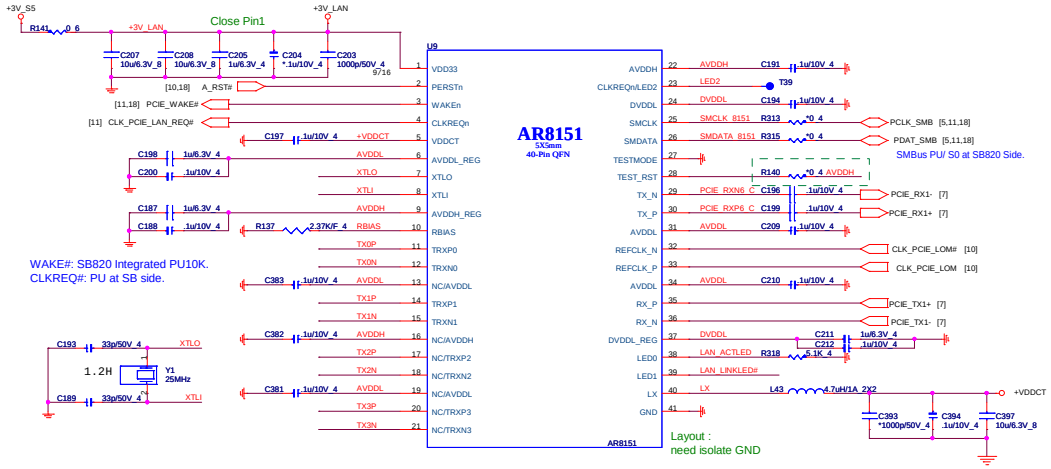
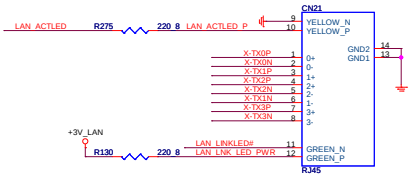
Giga-LAN AR8151

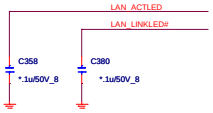


WAKE#: SB820 Integrated PU10K.
CLKREQ#: PU at SB side.

Layout :
need isolate GND

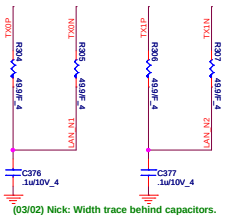
RJ45(LAN)



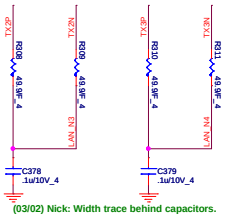


Sertek (03/01):
EMI capacitors, 470pF is enough.
Don't over 490 pF.

TRANSFORMER(LAN)

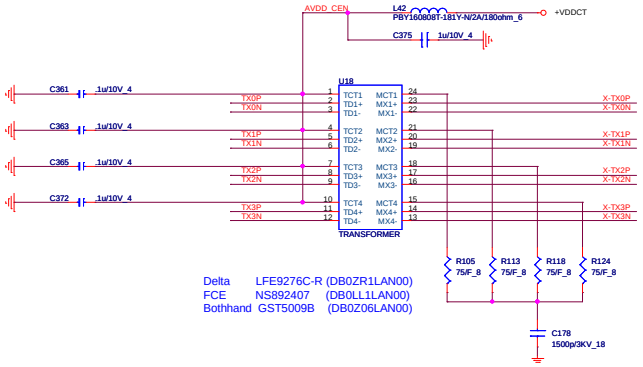


(03/02) Nick: Width trace behind capacitors.



(03/02) Nick: Width trace behind capacitors.

Close Transformer U28



Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)
Bothhand GST5009B (DB0Z06LAN00)

PROJECT : ZQ2
Quanta Computer Inc.

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	LAN (AR8151)	1A
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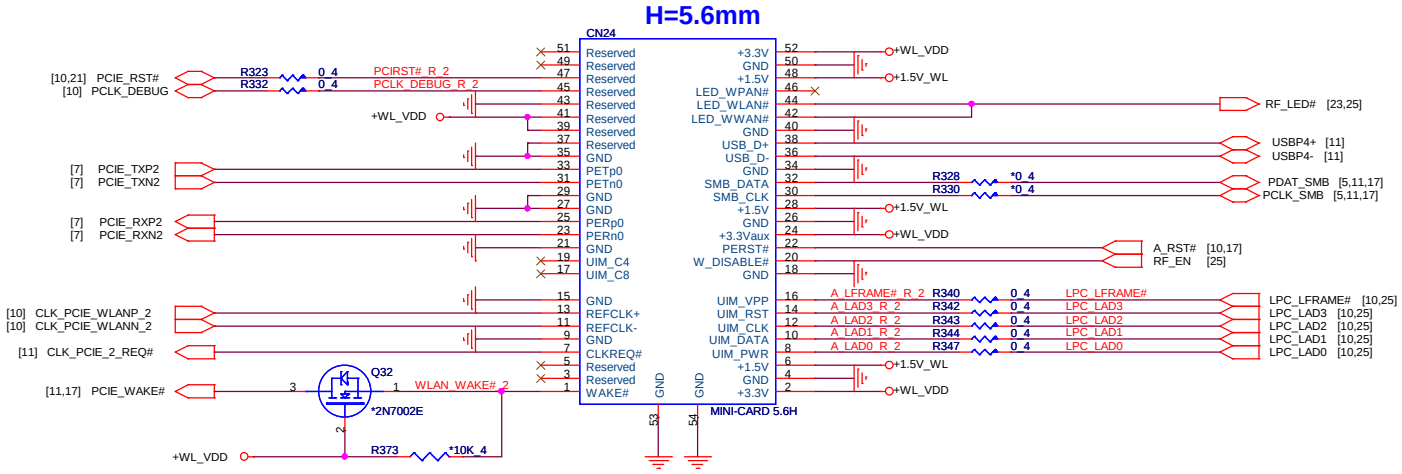
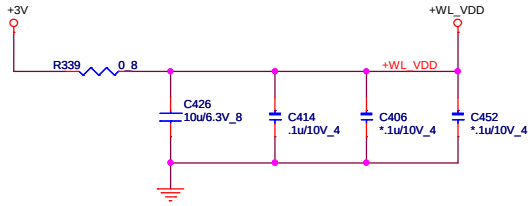
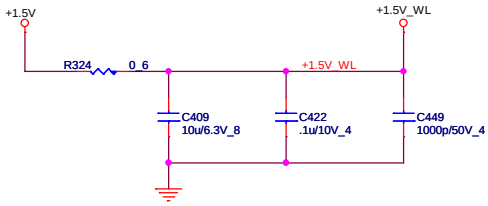
MINI-CARD WLAN(MNC)







PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
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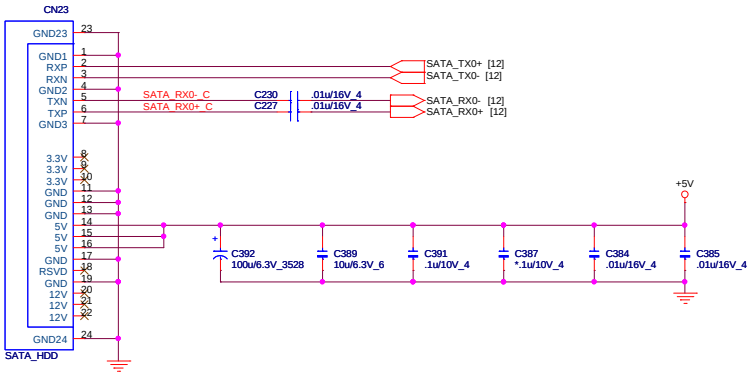
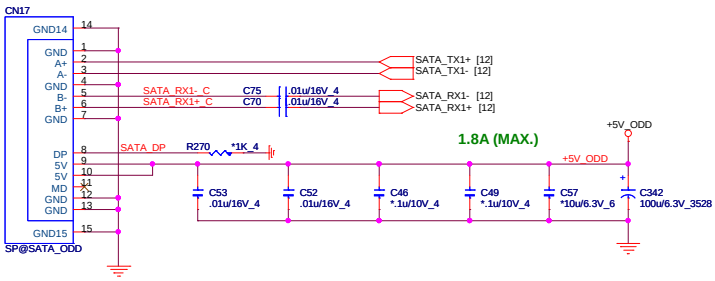
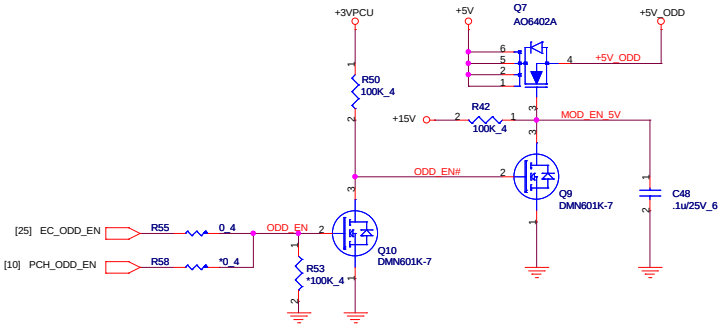
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



JM-9.5mm (H=2.4mm)/ Slim

Main	DFHS13FR078, DFHS13FR077
Second	DFHS13FR075

JV-12.7mm(H=5.5mm)/ Standard

Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005

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Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

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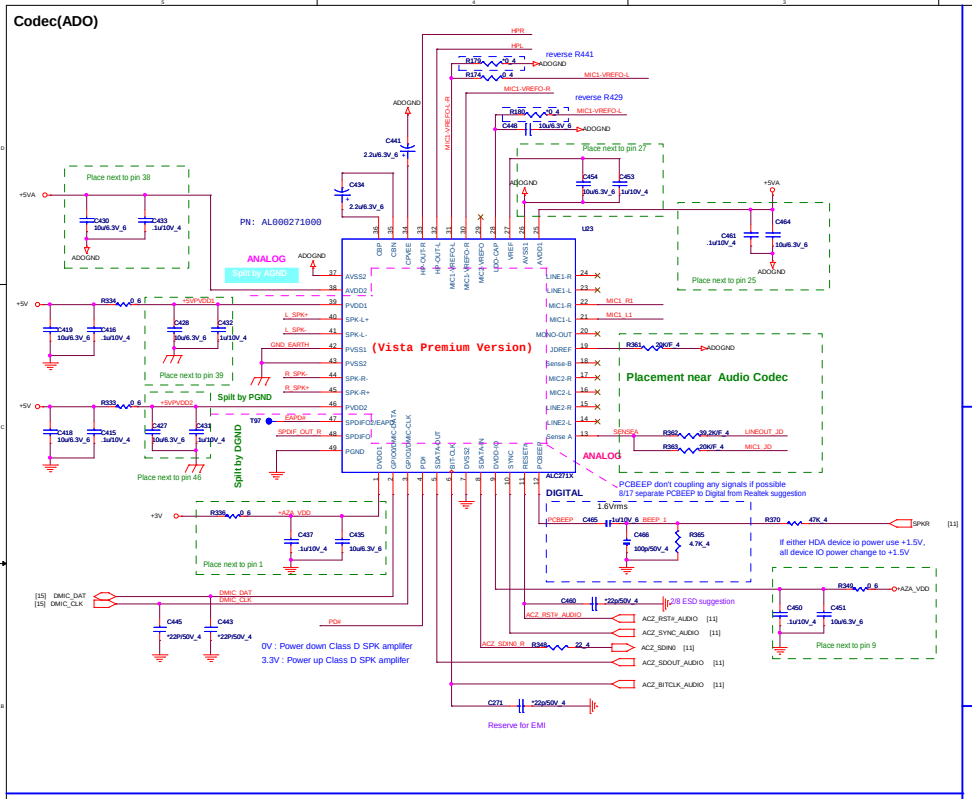
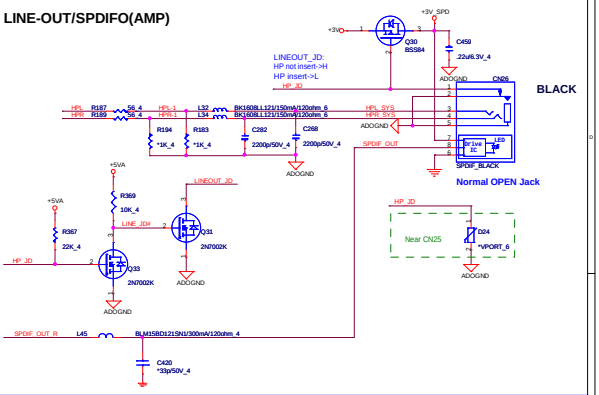
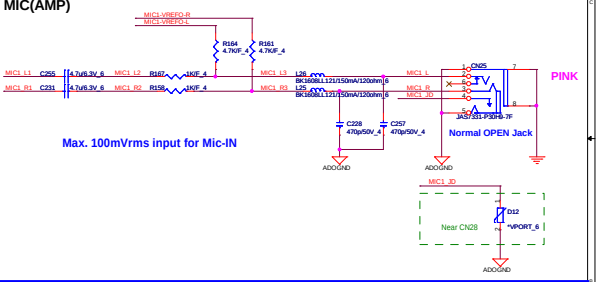
Codec(ADO)



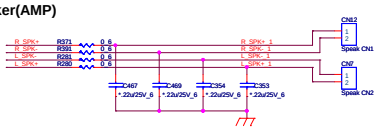
LINE-OUT/SPDIFO(AMP)



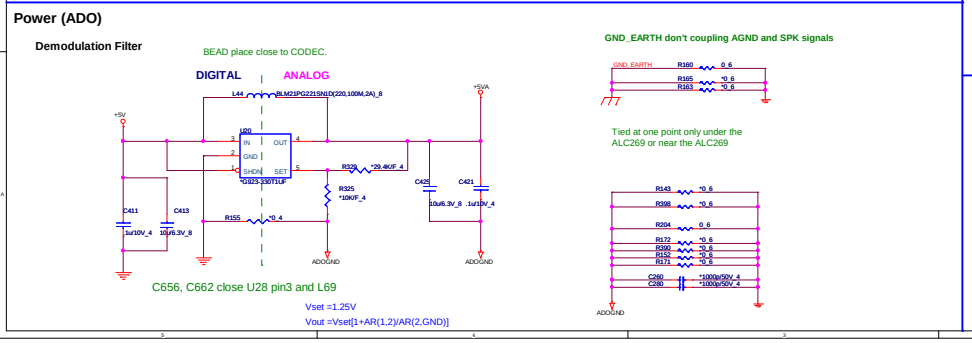
MIC(AMP)



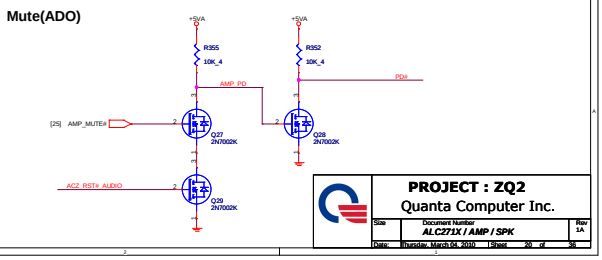
Internal Speaker(AMP)



Power (ADO)



Mute(ADO)



PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: ALC271X / AMP / SPK — Rev: 1A
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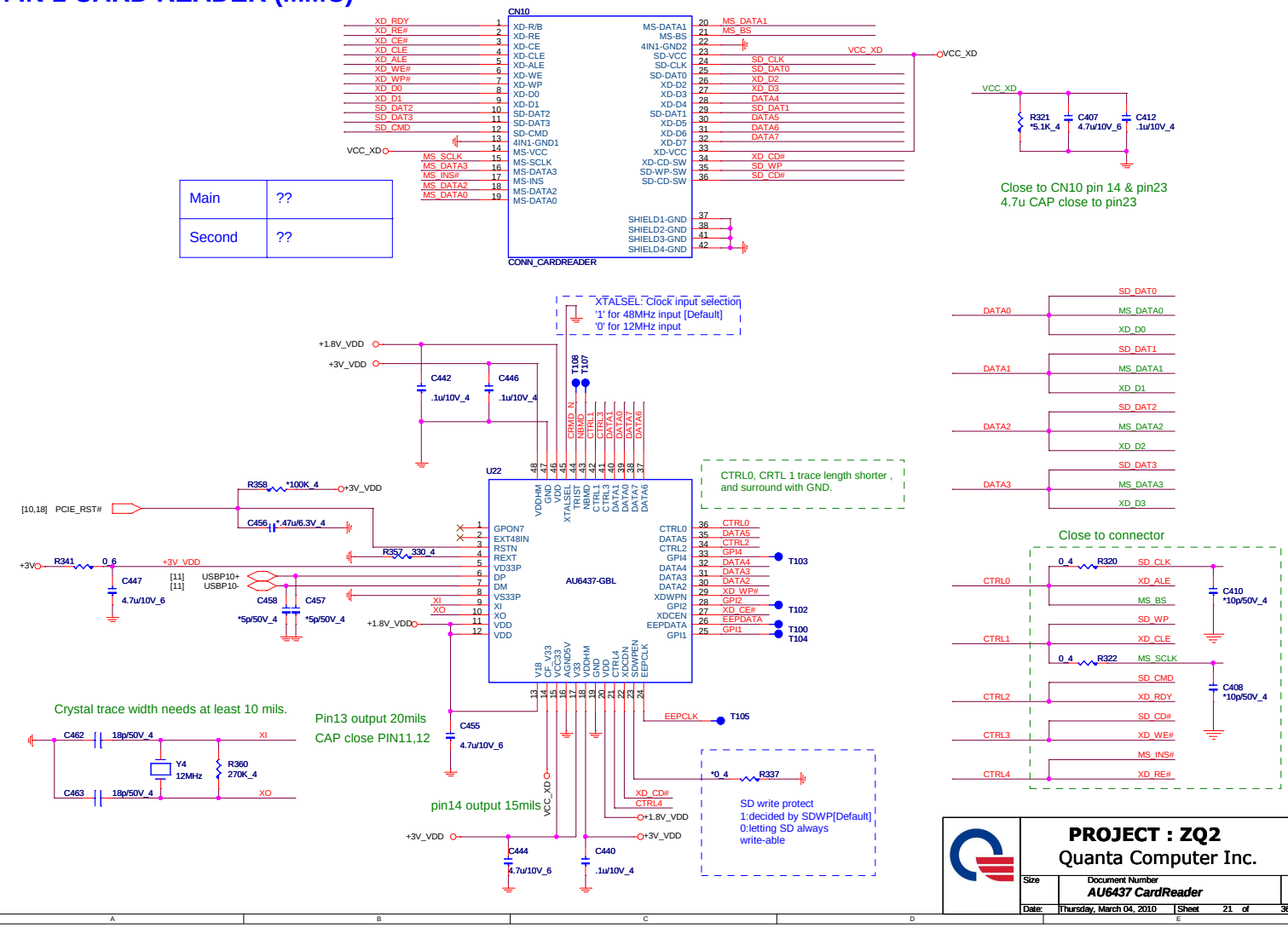
4 IN 1 CARD READER (MMC)



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Quanta Computer Inc.

Size	Document Number	Rev
	AU6437 CardReader	1A
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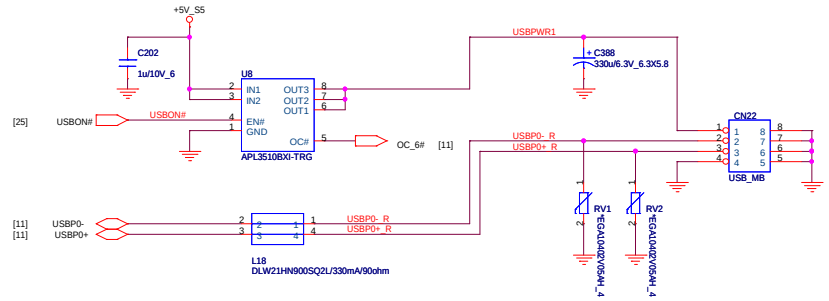
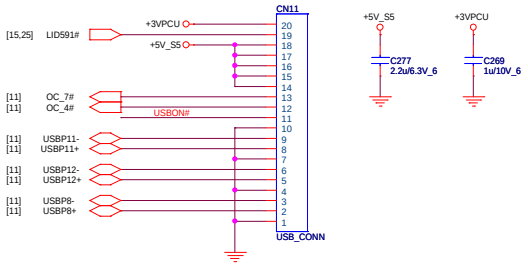
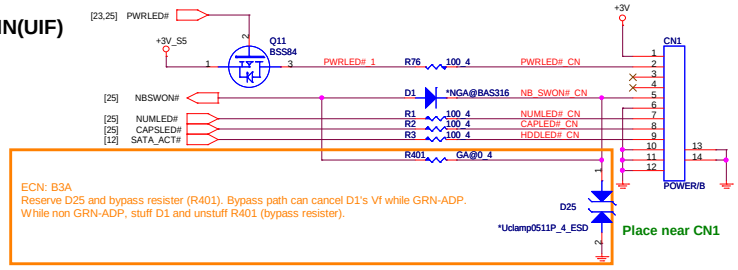
USB PORT(USB/MB)



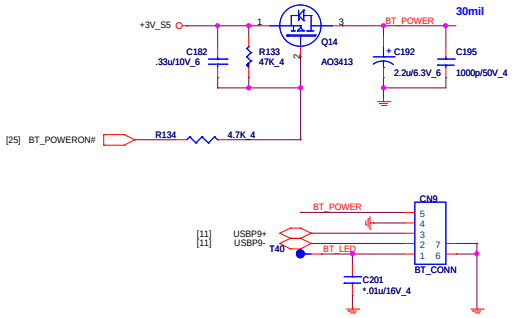
USB BOARD CONN(USB/SB)



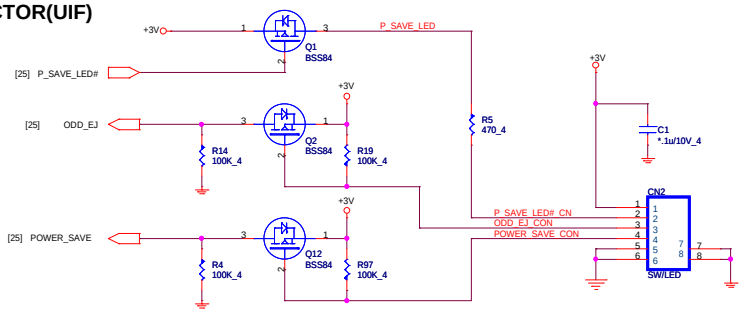
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



LED BOARD CONNECTOR(UIF)



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Quanta Computer Inc.

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	USB/BT/ITP	3A
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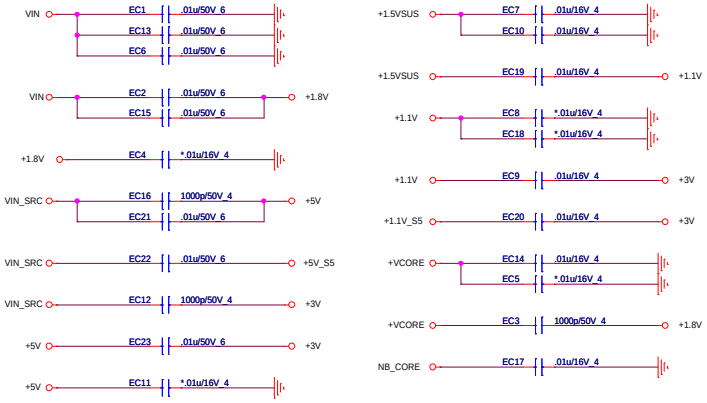
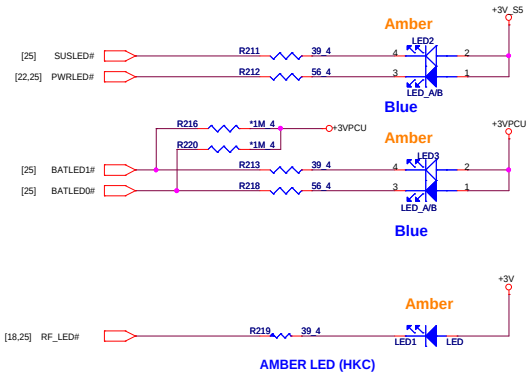
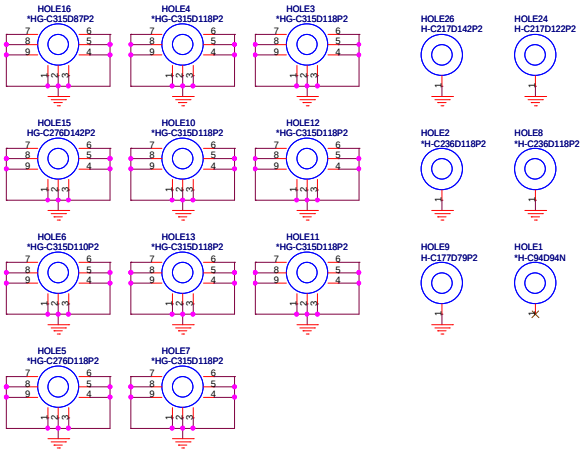
EE RETURN-PATH CAPACITORS(EMC)

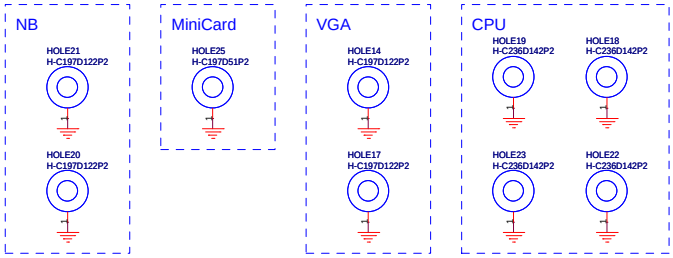


LED(UIF)



HOLE(OTH)





PROJECT : ZQ2
Quanta Computer Inc.

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	POWER/USB/BT/TP/MDC	1A
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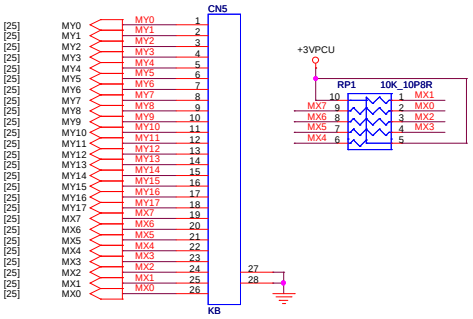
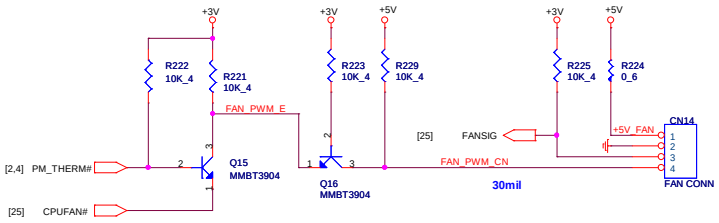
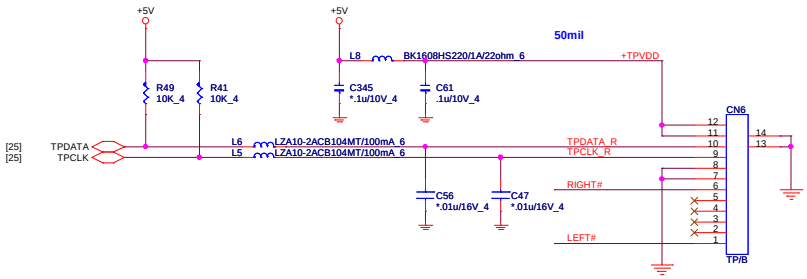
K/B(KBC)

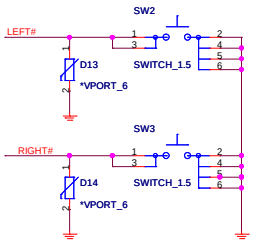


CPU FAN(THM)



TOUCHPAD BOARD CONN(TPD)





PROJECT : ZQ2

Quanta Computer Inc.

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	KB/FAN/EE RETURN CAP	1A
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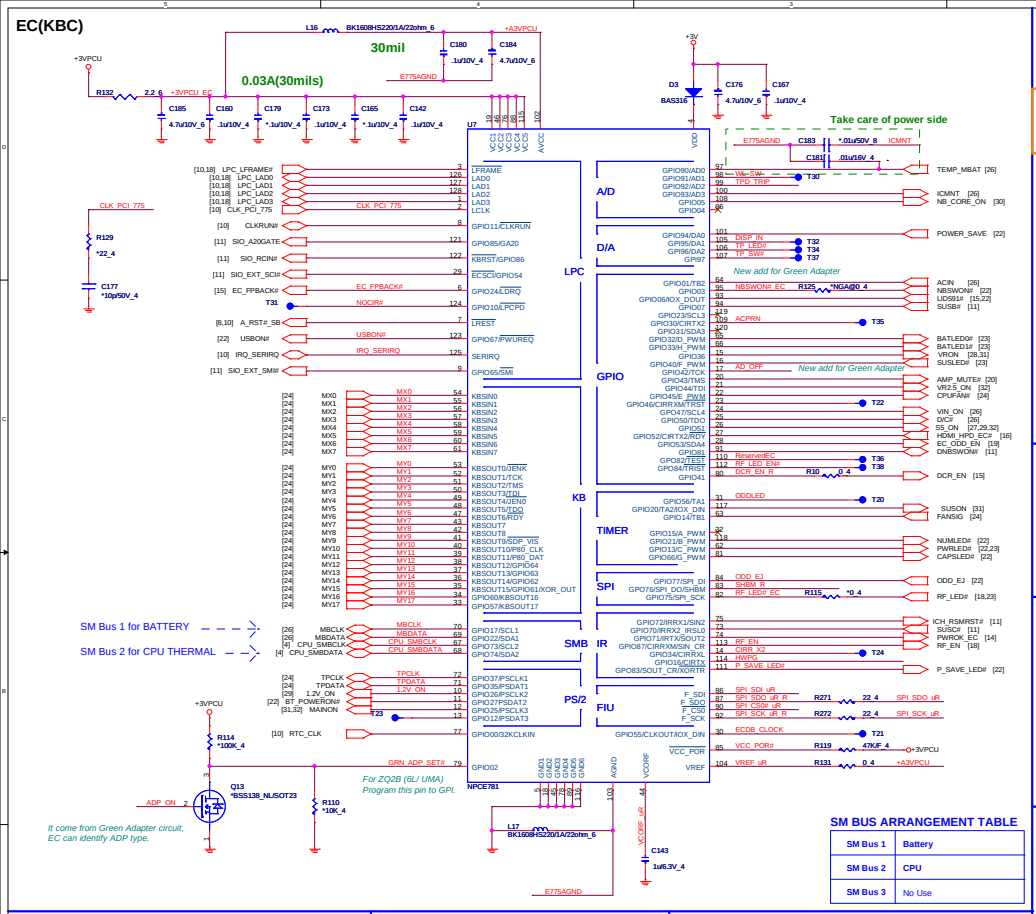
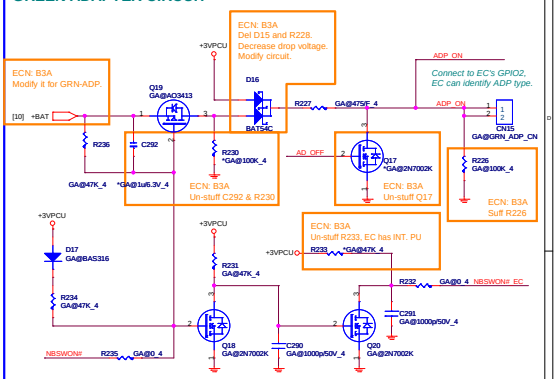
EC(KBC)



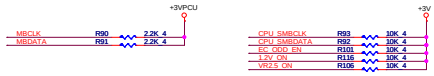
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU
SM Bus 3	No Use

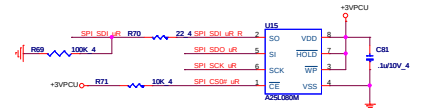
GREEN ADAPTER CIRCUIT



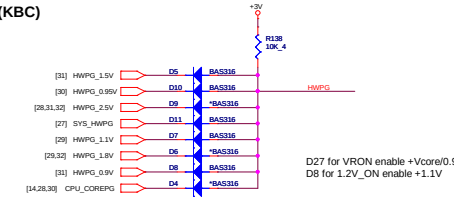
SM BUS PU(KBC)



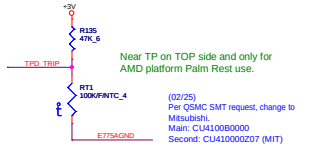
SPI FLASH(KBC)



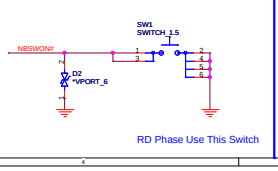
HWPG(KBC)



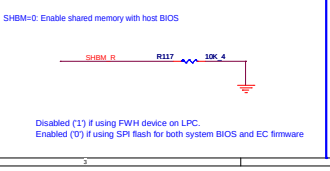
PALM REST THERMAL SENSOR (THM)



POWER-ON SWITCH (KBC)



POWER-ON SWITCH (KBC)



PROJECT : ZQ2
Quanta Computer Inc.
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PWCE775C_0DG & FLASH
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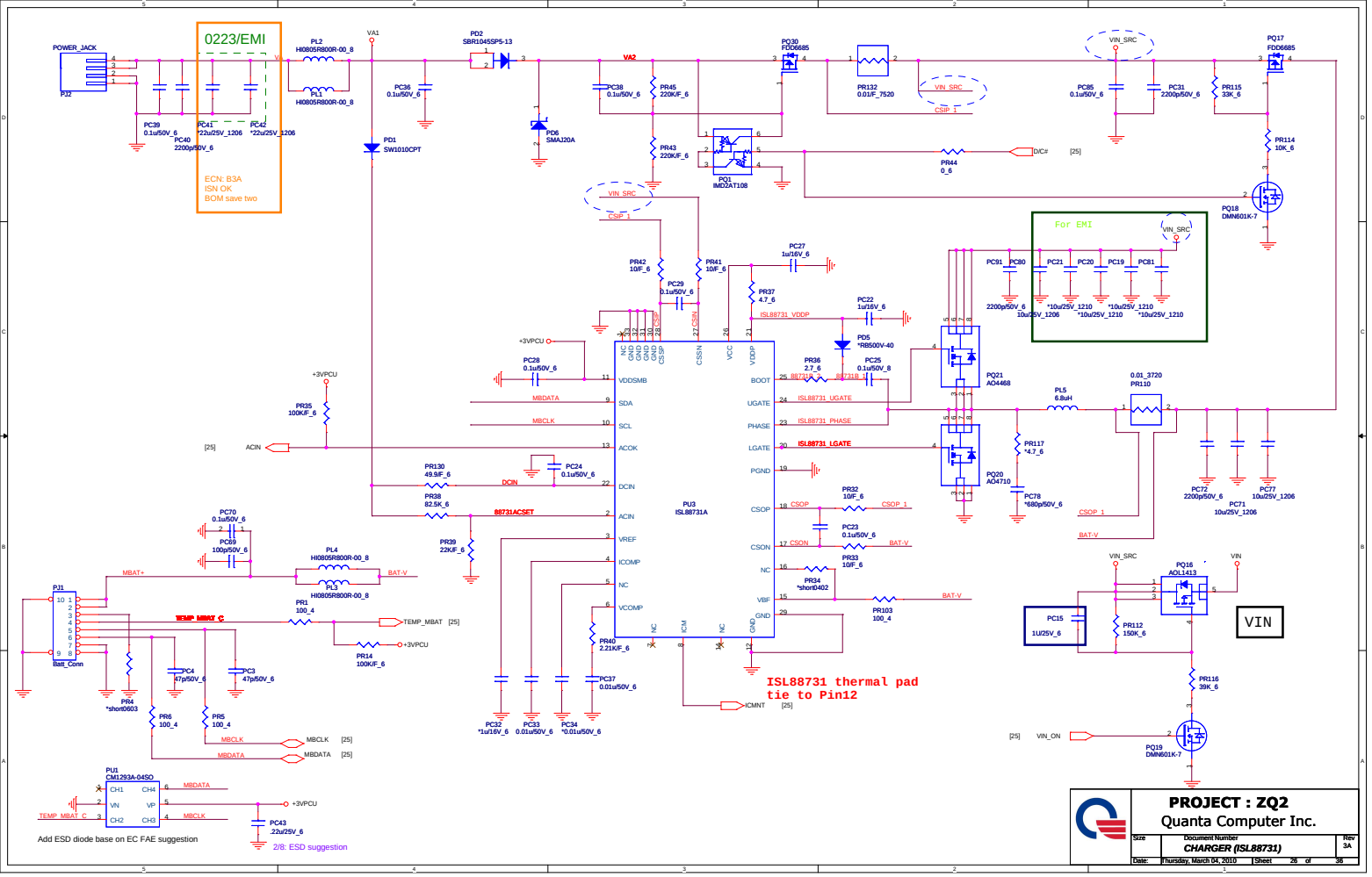
0223/EMI
ECN: B3A
ISN OK
BOM save two
For EMI
ISL88731 thermal pad
tie to Pin12
Add ESD diode base on EC FAE suggestion
2/8: ESD suggestion
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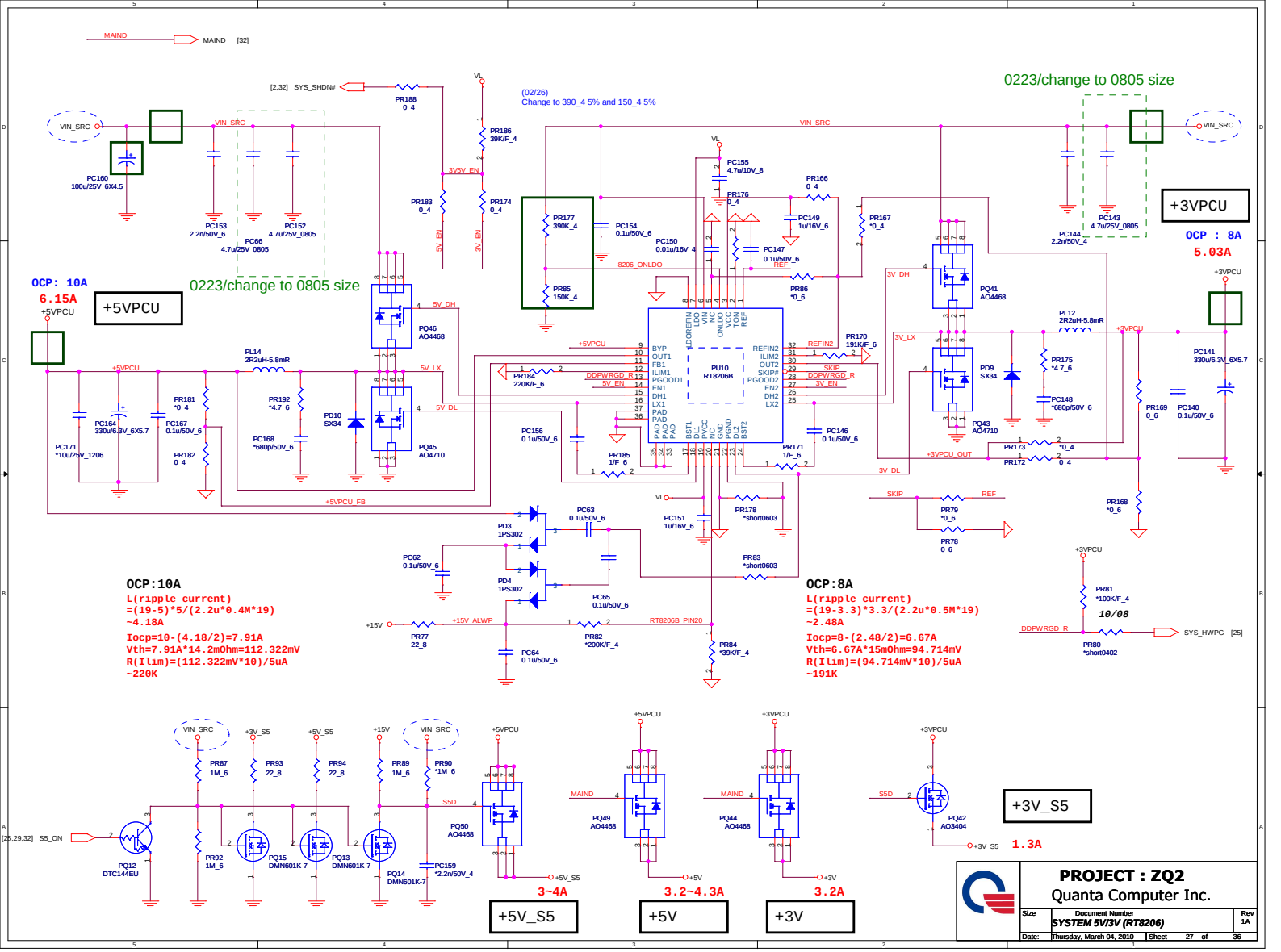
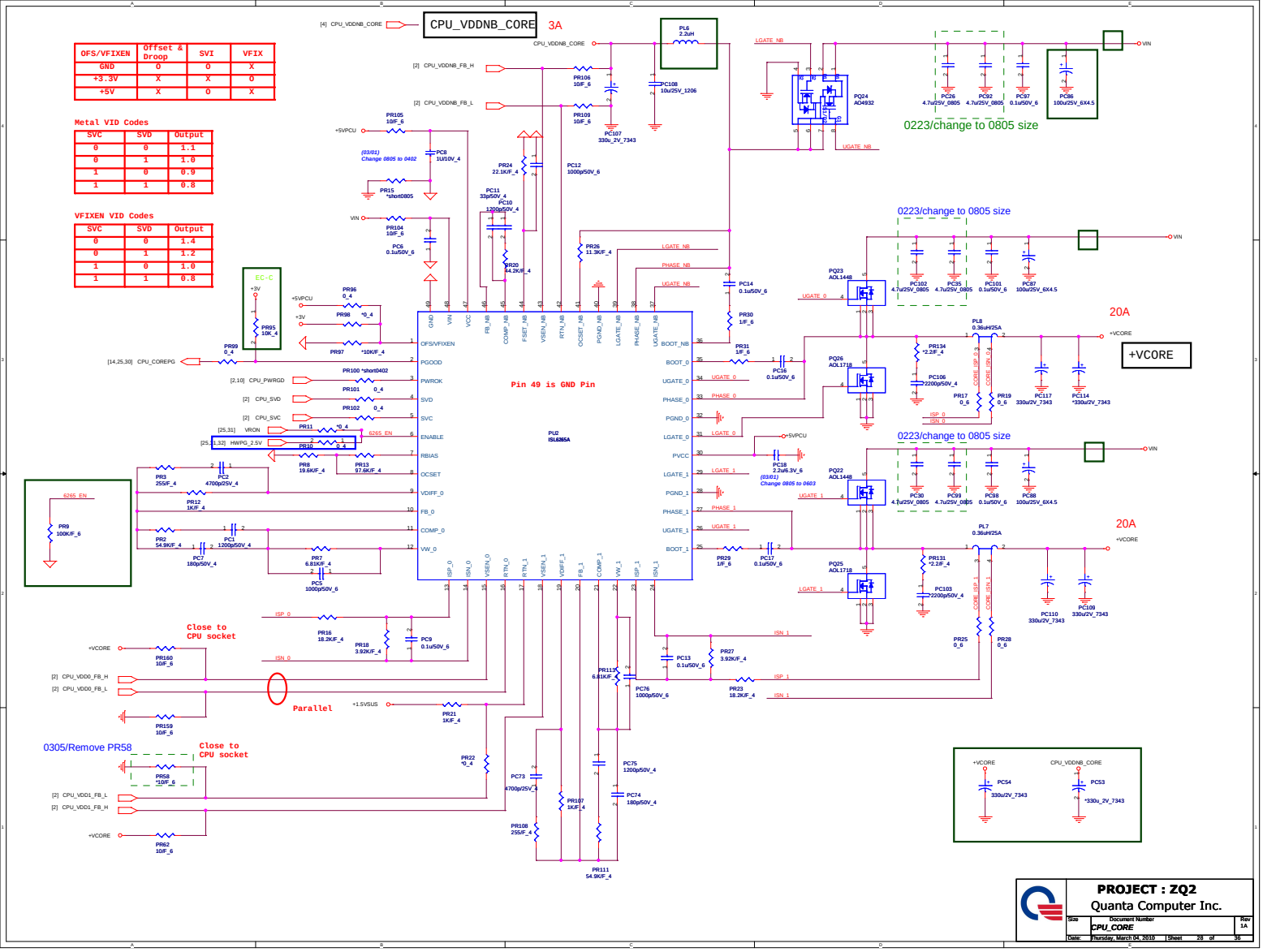
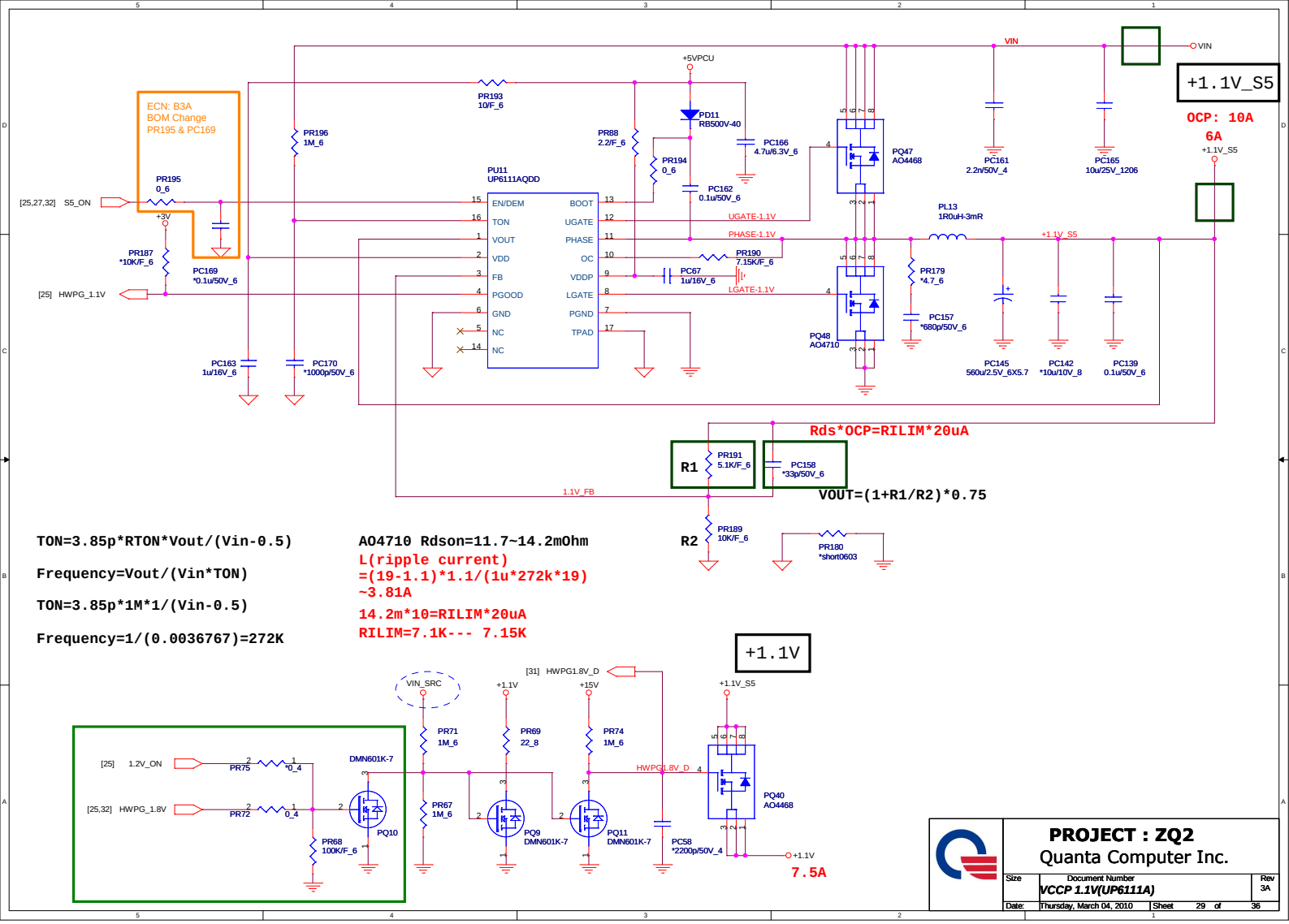
Quanta Computer Inc.
CHARGER (ISL88731)
Thursday, March 04, 2010


MAIND
MAIND [32]
[2,32] SYS_SHDN#
PR188 0_4
VL
PR186 39K/F_4
(02/26)
Change to 390_4 5% and 150_4 5%
0223/change to 0805 size
VIN_SRC
PC160 100u/25V_6X4.5
PC153 2.2n/50V_6
PC66 4.7u/25V_0805
PC152 4.7u/25V_0805
PR183 0_4
PR174 0_4
3V5V_EN
5V_EN
3V_EN
PR177 390K_4
PR85 150K_4
PC154 0.1u/50V_6
PC150 0.01u/16V_4
8206_ONLDO
PC155 4.7u/10V_8
PR176 0_4
PR166 0_4
PC149 1u/16V_6
PC147 0.1u/50V_6
REF
PR86 *0_6
PR167 *0_4
PC144 2.2n/50V_4
PC143 4.7u/25V_0805
+3VPCU
OCP : 8A
5.03A
OCP: 10A
6.15A
+5VPCU
+5VPCU
0223/change to 0805 size
5V_DH
PQ46 AO4468
PL14 2R2uH-5.8mR
5V_LX
PR181 *0_4
PR164 330u/6.3V_6X5.7
PC167 0.1u/50V_6
PC171 *10u/25V_1206
PR182 0_4
PR192 *4.7_6
PD10 SX34
PC168 *680p/50V_6
5V_DL
PQ45 AO4710
+5VPCU_FB
PR184 220K/F_6
DDPWRGD_R
5V_EN
PU10 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
DORFPN
LDO
VIN
NC
ONLDO
VCC
FDN
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
GND
PGND
DL2
SST2
PR185 1/F_6
PC156 0.1u/50V_6
PC146 0.1u/50V_6
PR171 1/F_6
PR170 191K/F_6
REFIN2
SKIP
DDPWRGD_R
3V_EN
3V_DH
PQ41 AO4468
3V_LX
PD9 SX34
PQ43 AO4710
3V_DL
PL12 2R2uH-5.8mR
PR175 *4.7_6
PC148 *680p/50V_6
PR173 *0_4
PR172 0_4
+3VPCU_OUT
PR169 0_6
PC140 0.1u/50V_6
PC141 330u/6.3V_6X5.7
PR168 *0_6
SKIP
REF
PR79 *0_6
PR78 0_6
PC151 1u/16V_6
PR178 *short0603
PR83 *short0603
PD3 1PS302
PD4 1PS302
PC63 0.1u/50V_6
PC62 0.1u/50V_6
PC65 0.1u/50V_6
PC64 0.1u/50V_6
+15V
PR77 22_8
+15V_ALWP
PR82 *200K/F_4
RT8206B_PIN20
PR84 *39K/F_4
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR81 *100K/F_4
10/08
DDPWRGD_R
PR80 *short0402
SYS_HWPG [25]
[25,29,32] S5_ON
PQ12 DTC144EU
PR87 1M_6
PR92 1M_6
PR93 22_8
PR94 22_8
PR89 1M_6
PR90 *1M_6
S5D
PQ15 DMN601K-7
PQ13 DMN601K-7
PQ14 DMN601K-7
PQ50 AO4468
PC159 *2.2n/50V_4
+5V_S5
3~4A
+5V_S5
MAIND
PQ49 AO4468
+5V
3.2~4.3A
+5V
PQ44 AO4468
+3V
3.2A
+3V
PQ42 AO3404
+3V_S5
1.3A
+3V_S5
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Thursday, March 04, 2010
Sheet 27 of 36


CPU_VDDNB_CORE
3A
OFS/VFIXEN
Offset & Droop
SVI
VFIX
GND
0
0
X
+3.3V
X
X
0
+5V
X
0
X
Metal VID Codes
SVC
SVD
Output
0
0
1.1
0
1
1.0
1
0
0.9
1
1
0.8
VFIXEN VID Codes
SVC
SVD
Output
0
0
1.4
0
1
1.2
1
0
1.0
1
1
0.8
Pin 49 is GND Pin
0223/change to 0805 size
20A
+VCORE
Close to CPU socket
Parallel
0305/Remove PR58
PROJECT : ZQ2
Quanta Computer Inc.
CPU_CORE
Thursday, March 04, 2010


ECN: B3A
BOM Change
PR195 & PC169
+1.1V_S5
OCP: 10A
6A
VIN
+5VPCU
PU11
UP6111AQDD
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-1.1V
PHASE-1.1V
LGATE-1.1V
PQ47
AO4468
PQ48
AO4710
PL13
1R0uH-3mR
[25,27,32] S5_ON
[25] HWPG_1.1V
1.1V_FB
Rds*OCP=RILIM*20uA
R1
R2
VOUT=(1+R1/R2)*0.75
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K
+1.1V
VIN_SRC
[31] HWPG1.8V_D
[25] 1.2V_ON
[25,32] HWPG_1.8V
DMN601K-7
PQ10
PQ9
DMN601K-7
PQ11
DMN601K-7
PQ40
AO4468
7.5A
PROJECT : ZQ2
Quanta Computer Inc.
VCCP 1.1V(UP6111A)
Thursday, March 04, 2010
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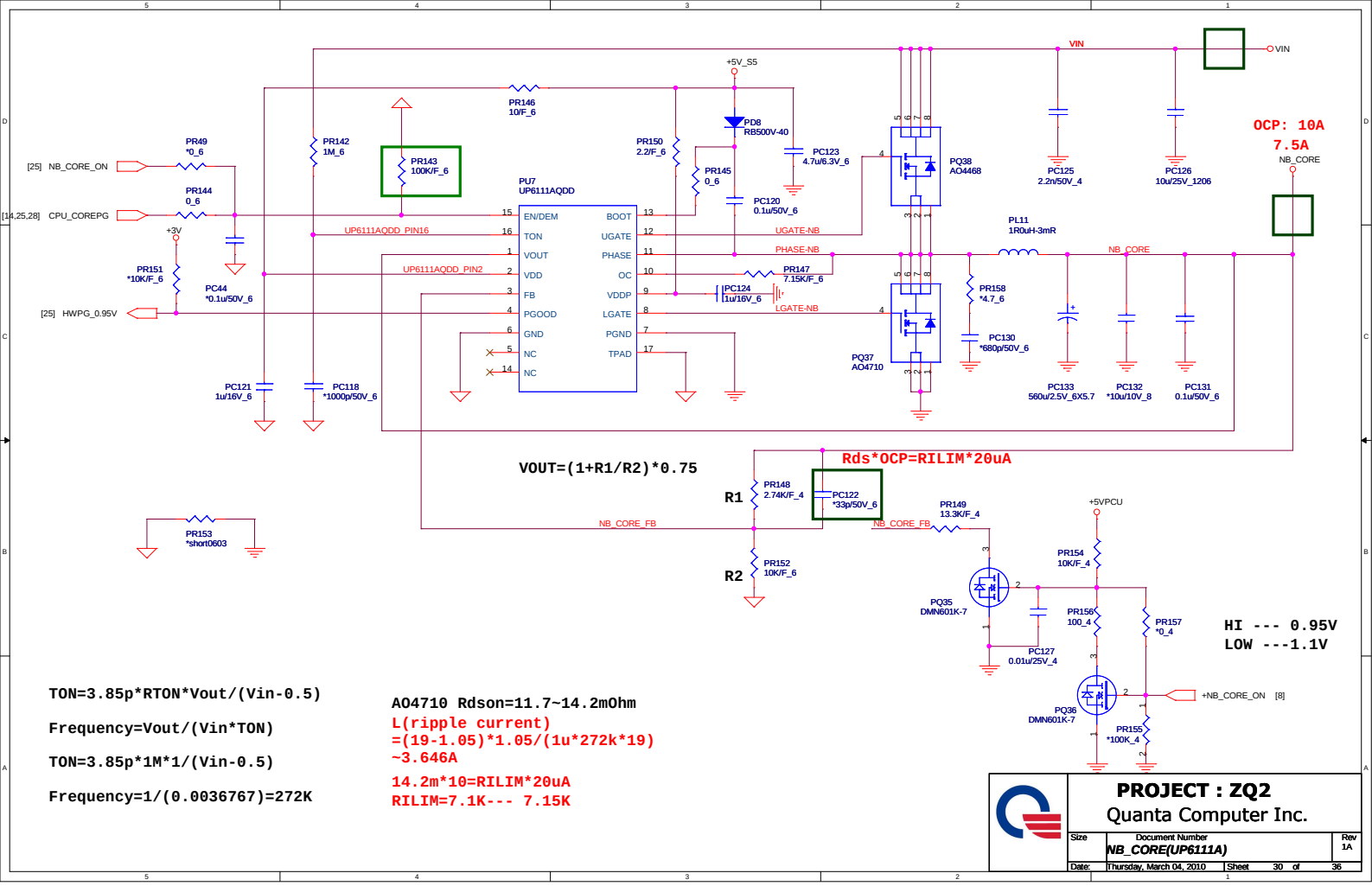


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

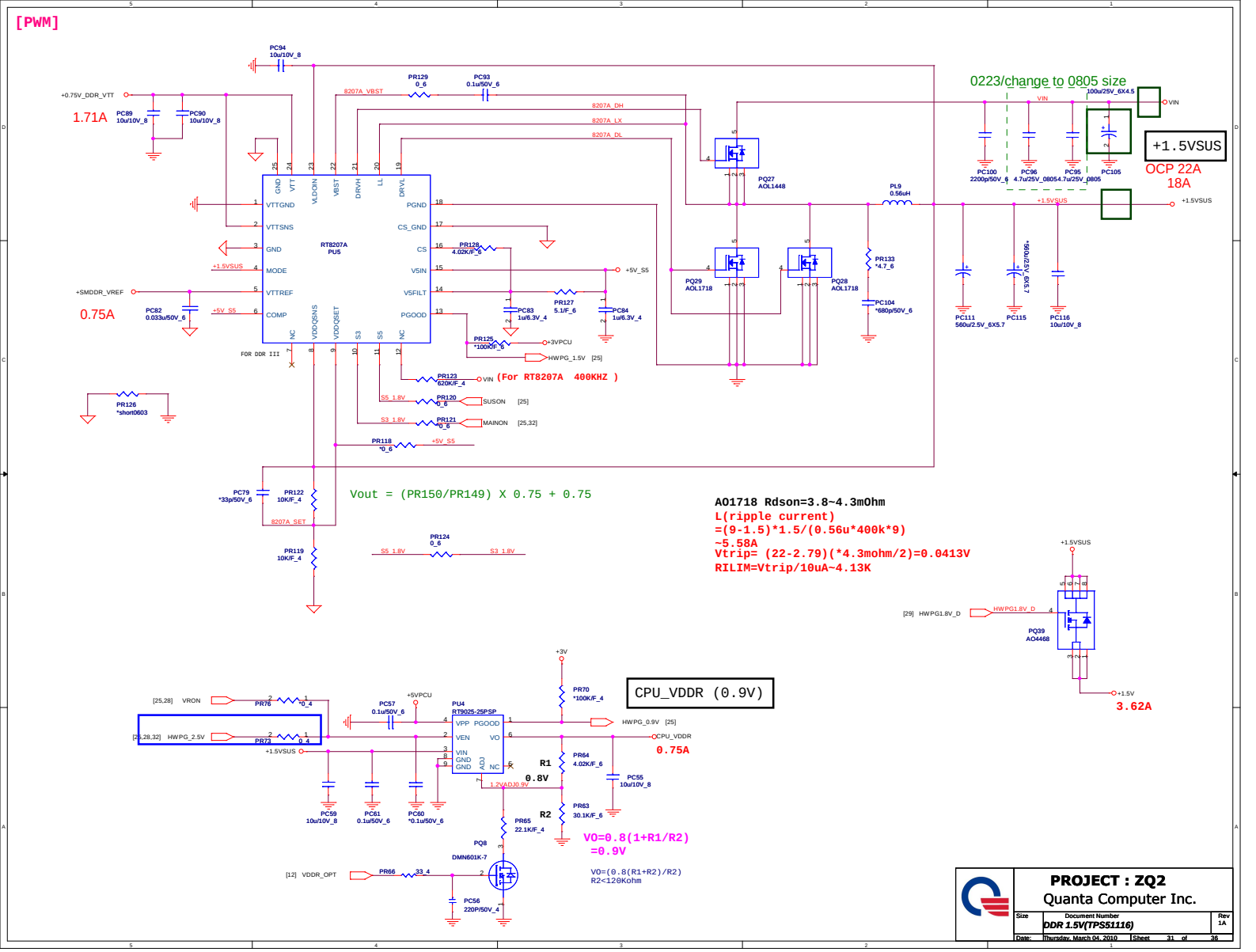
AO4710 Rdson=11.7~14.2mOhm

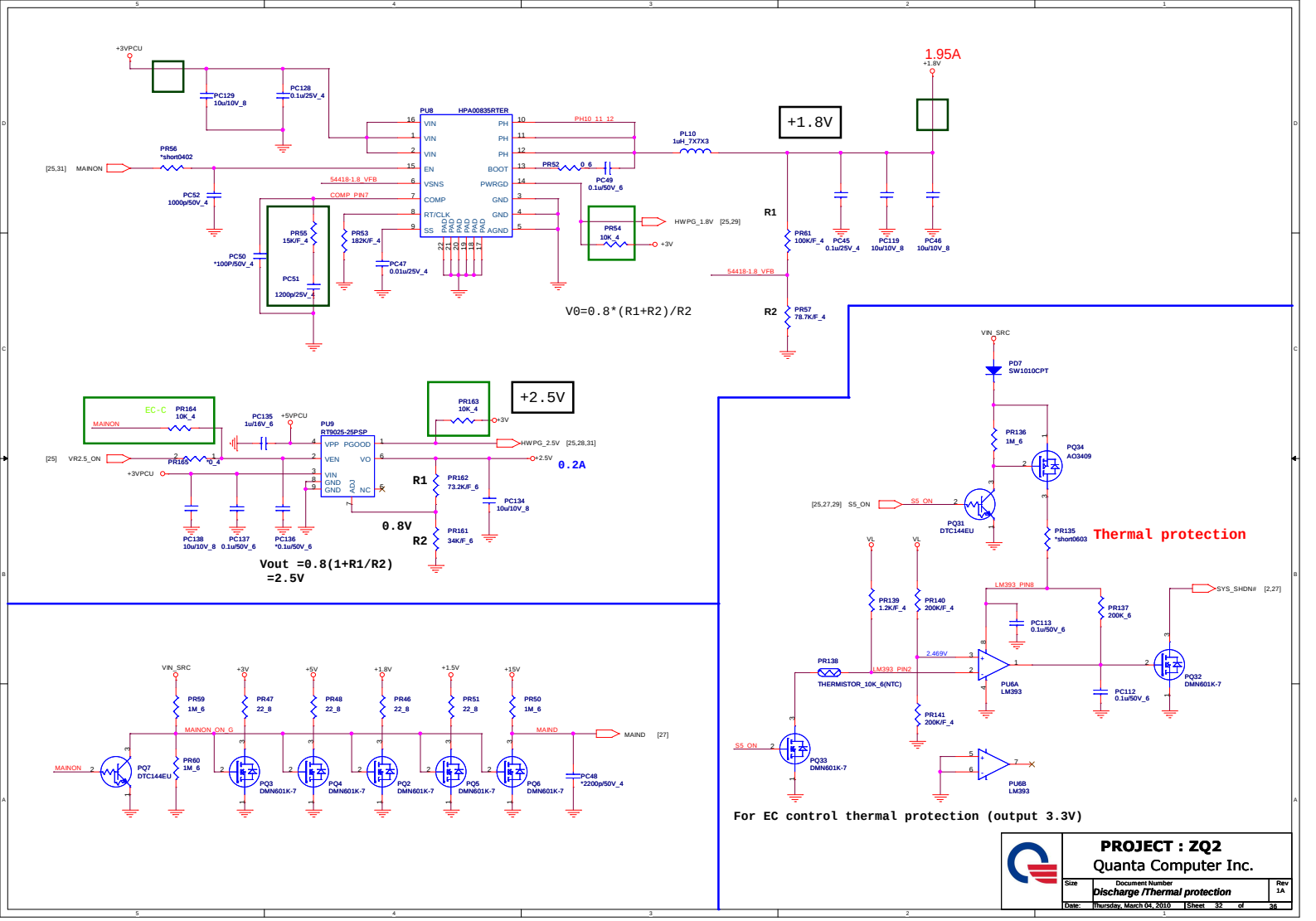
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	NB_CORE(UP6111A)	1A
Date: Thursday, March 04, 2010	Sheet 30 of 36	


[PWM]
0223/change to 0805 size
+1.5VSUS
OCP 22A
18A
1.71A
0.75A
RT8207A
PU5
(For RT8207A 400KHZ)
Vout = (PR150/PR149) X 0.75 + 0.75
AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K
CPU_VDDR (0.9V)
RT9025-25PSP
PU4
0.8V
VO=0.8(1+R1/R2)
=0.9V
VO=(0.8(R1+R2)/R2)
R2<120Kohm
3.62A
0.75A
PROJECT : ZQ2
Quanta Computer Inc.
DDR 1.5V(TPS51116)
Thursday, March 04, 2010


+3VPCU
PC129 10u/10V_8
PC128 0.1u/25V_4
PU8 HPA00835RTER
VIN
VIN
VIN
EN
VSNS
COMP
RT/CLK
SS
PH
PH
PH
BOOT
PWRGD
GND
GND
AGND
PAD
PH10_11_12
PL10 1uH_7X7X3
PR52 0_6
PC49 0.1u/50V_6
1.95A
+1.8V
+1.8V
PR56 *short0402
[25,31] MAINON
PC52 1000p/50V_4
54418-1.8_VFB
COMP_PIN7
PR55 15K/F_4
PC50 *100P/50V_4
PC51 1200p/25V_4
PR53 182K/F_4
PC47 0.01u/25V_4
PR54 10K_4
HWPG_1.8V [25,29]
+3V
R1
PR61 100K/F_4
PC45 0.1u/25V_4
PC119 10u/10V_8
PC46 10u/10V_8
54418-1.8_VFB
R2
PR57 78.7K/F_4
V0=0.8*(R1+R2)/R2
+2.5V
PR163 10K_4
+3V
EC-C
PR164 10K_4
MAINON
PC135 1u/16V_6
+5VPCU
PU9 RT9025-25PSP
VPP
VEN
VIN
GND
GND
PGOOD
VO
NC
ADJ
HWPG_2.5V [25,28,31]
+2.5V
0.2A
[25] VR2.5_ON
PR165 10_4
+3VPCU
R1
PR162 73.2K/F_6
PC134 10u/10V_8
0.8V
R2
PR161 34K/F_6
PC138 10u/10V_8
PC137 0.1u/50V_6
PC136 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=2.5V
VIN_SRC
PD7 SW1010CPT
PR136 1M_6
PQ34 AO3409
[25,27,29] S5_ON
S5_ON
PQ31 DTC144EU
PR135 *short0603
Thermal protection
VL
VL
PR139 1.2K/F_4
PR140 200K/F_4
LM393_PIN8
PC113 0.1u/50V_6
PR137 200K_6
SYS_SHDN# [2,27]
2.469V
PR138
THERMISTOR_10K_6(NTC)
LM393_PIN2
PU6A LM393
PQ32 DMN601K-7
PC112 0.1u/50V_6
PR141 200K/F_4
S5_ON
PQ33 DMN601K-7
PU6B LM393
VIN_SRC
+3V
+5V
+1.8V
+1.5V
+15V
PR59 1M_6
PR47 22_8
PR48 22_8
PR46 22_8
PR51 22_8
PR50 1M_6
MAINON_ON_G
MAIND
MAIND [27]
MAINON
PQ7 DTC144EU
PR60 1M_6
PQ3 DMN601K-7
PQ4 DMN601K-7
PQ2 DMN601K-7
PQ5 DMN601K-7
PQ6 DMN601K-7
PC48 *2200p/50V_4
For EC control thermal protection (output 3.3V)
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
Discharge /Thermal protection
Rev 1A
Date: Thursday, March 04, 2010
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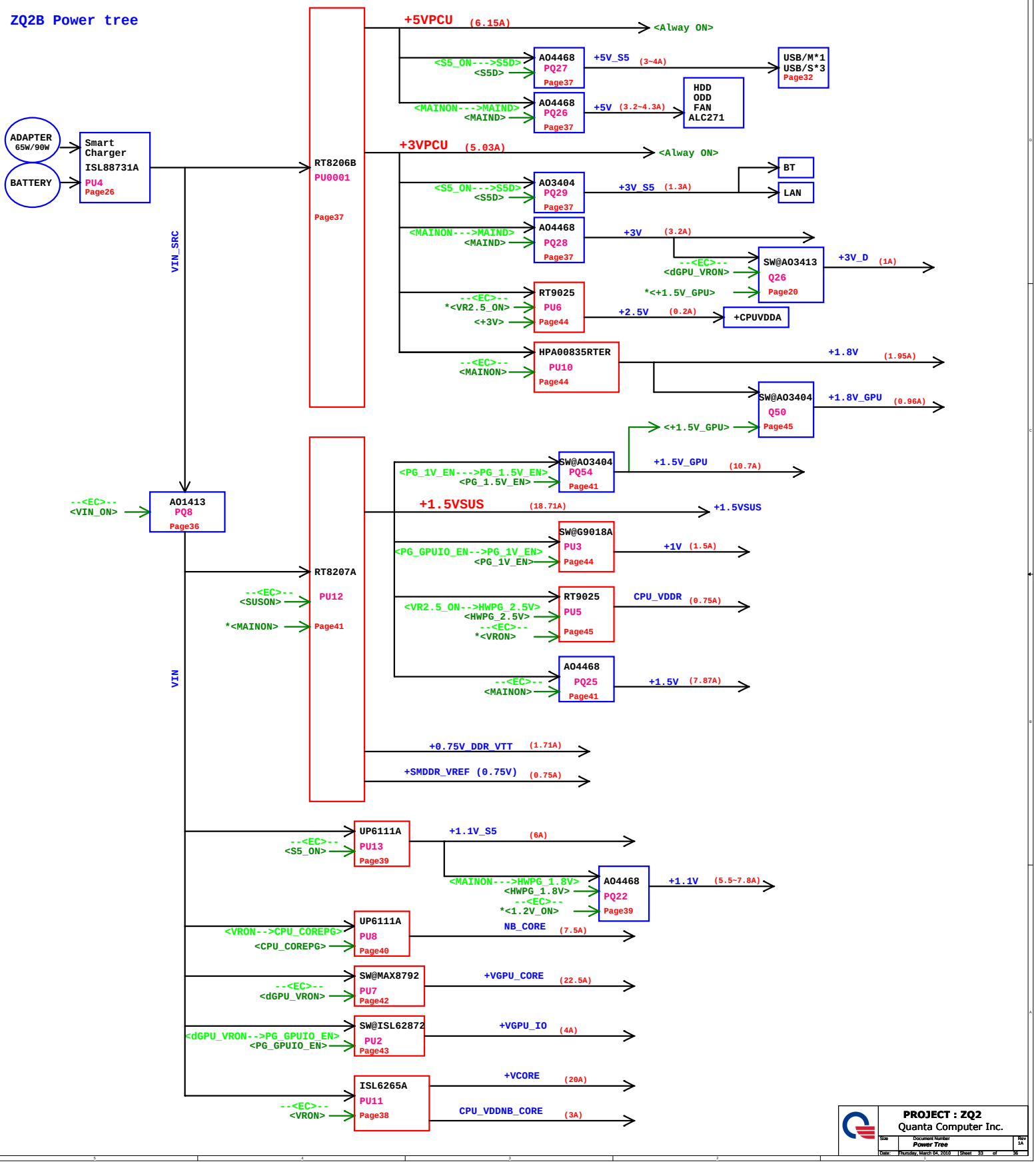
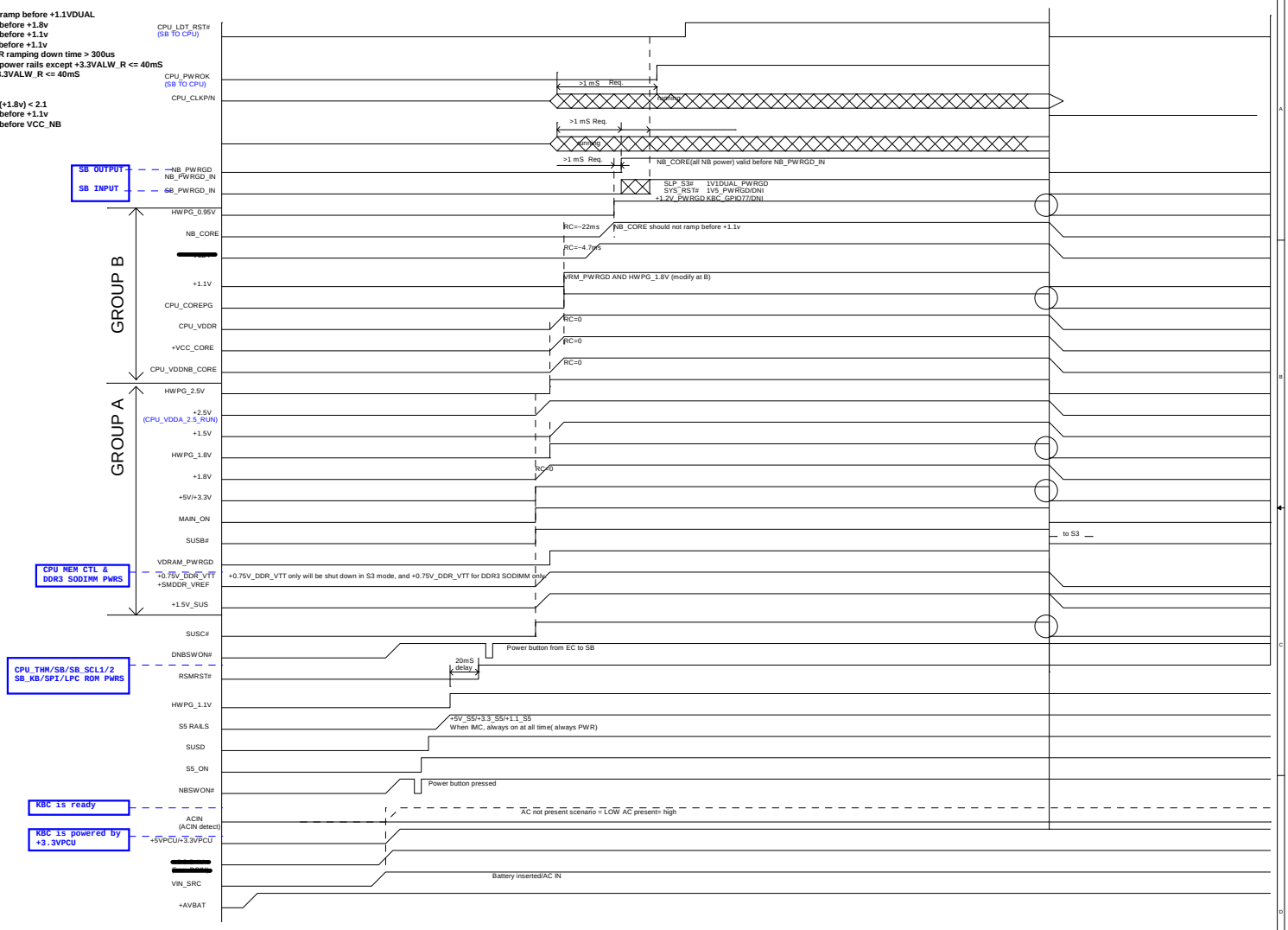

ZQ2B Power tree
ADAPTER
65W/90W
BATTERY
Smart Charger
ISL88731A
PU4
Page26
VIN_SRC
RT8206B
PU0001
Page37
+5VPCU (6.15A)
<Alway ON>
<S5_ON--->S5D>
<S5D>
AO4468
PQ27
Page37
+5V_S5 (3~4A)
USB/M*1
USB/S*3
Page32
<MAINON--->MAIND>
<MAIND>
AO4468
PQ26
Page37
+5V (3.2~4.3A)
HDD
ODD
FAN
ALC271
+3VPCU (5.03A)
<Alway ON>
<S5_ON--->S5D>
<S5D>
AO3404
PQ29
Page37
+3V_S5 (1.3A)
BT
LAN
<MAINON--->MAIND>
<MAIND>
AO4468
PQ28
Page37
+3V (3.2A)
--<EC>--
<dGPU_VRON>
SW@AO3413
Q26
Page20
+3V_D (1A)
*<+1.5V_GPU>
--<EC>--
*<VR2.5_ON>
<+3V>
RT9025
PU6
Page44
+2.5V (0.2A)
+CPUVDDA
--<EC>--
<MAINON>
HPA00835RTER
PU10
Page44
+1.8V (1.95A)
SW@AO3404
Q50
Page45
+1.8V_GPU (0.96A)
<+1.5V_GPU>
--<EC>--
<VIN_ON>
AO1413
PQ8
Page36
VIN
RT8207A
PU12
Page41
--<EC>--
<SUSON>
*<MAINON>
<PG_1V_EN--->PG_1.5V_EN>
<PG_1.5V_EN>
SW@AO3404
PQ54
Page41
+1.5V_GPU (10.7A)
+1.5VSUS (18.71A)
+1.5VSUS
<PG_GPUIO_EN-->PG_1V_EN>
<PG_1V_EN>
SW@G9018A
PU3
Page44
+1V (1.5A)
<VR2.5_ON-->HWPG_2.5V>
<HWPG_2.5V>
--<EC>--
*<VRON>
RT9025
PU5
Page45
CPU_VDDR (0.75A)
--<EC>--
<MAINON>
AO4468
PQ25
Page41
+1.5V (7.87A)
+0.75V_DDR_VTT (1.71A)
+SMDDR_VREF (0.75V) (0.75A)
--<EC>--
<S5_ON>
UP6111A
PU13
Page39
+1.1V_S5 (6A)
<MAINON--->HWPG_1.8V>
<HWPG_1.8V>
--<EC>--
*<1.2V_ON>
AO4468
PQ22
Page39
+1.1V (5.5~7.8A)
<VRON-->CPU_COREPG>
<CPU_COREPG>
UP6111A
PU8
Page40
NB_CORE (7.5A)
--<EC>--
<dGPU_VRON>
SW@MAX8792
PU7
Page42
+VGPU_CORE (22.5A)
<dGPU_VRON-->PG_GPUIO_EN>
<PG_GPUIO_EN>
SW@ISL62872
PU2
Page43
+VGPU_IO (4A)
--<EC>--
<VRON>
ISL6265A
PU11
Page38
+VCORE (20A)
CPU_VDDNB_CORE (3A)
PROJECT : ZQ2
Quanta Computer Inc.
Power Tree
Thursday, March 04, 2010

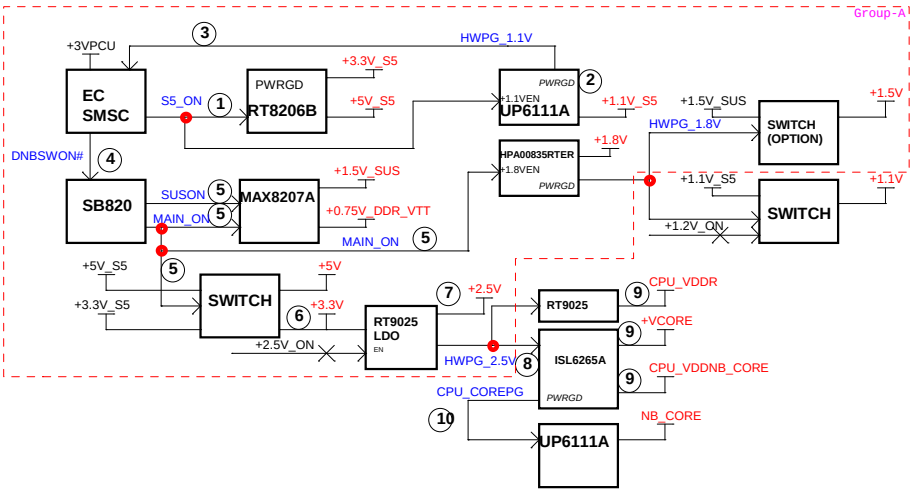
Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



	PROJECT : ZQ2 Quanta Computer Inc.	
Size	Document Number: *Power Squence Chart*	Rev 1A
Date: Thursday, March 04, 2010	Sheet 34 of 36	

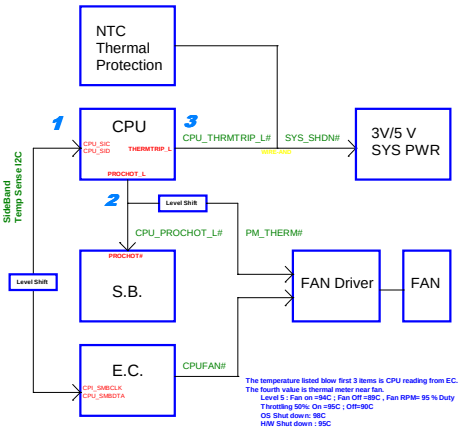


Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

H/W Thermal Follow Chart



POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: PWR ON SEQ and THERM POLICY | Rev 1A
Date: Thursday, March 04, 2010 | Sheet 35 of 36

Model	REV	CHANGE LIST
ZQ2B MB	1A	A1A The First Release.
	3A	B3A Page 02 Q23 cahnge from FDV301V to BSS138. Becasue FDV301V EOL. B3A Page 10 Add off-page net of +BAT for Green Adpapter. It can decrease drop voltage. R289 change value to 12K beucase charge current. B3A Page 15 Change R11's footprint to short pad. BOM cancel R11. B3A Page 22 Reserve D25 and add R401. It can cancel D1's Vf while GRN-ADP. B3A Page 25 Del D15 and R228. And change PWR source of ADP_ON. All for decrease drop voltage. And un-stuff Q17 in oreder to EC suggestion. B3A Page 25 BOM change for fine-tune. Stuff R226 and BOM unstuff C292, R230 and R233. B3A Page 26 BOM save PC41 and PC42. B3A Page 29 BOM change for Pr195 and PC169 in order to AMD power up timing requirement.

MODEL	ZQ2B	
	FROM	To
	X	1A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	

DOC NO.						
	PROJECT MODEL :	ZQ2B	APPROVED BY:		DATE:	2010/03/05
	PART NUMBER:		DRAWING BY:		REVISON:	1A

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A

Date: Thursday, March 04, 2010 Sheet 36 of 36