ZQP SYSTEM DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

HDMI@ -----> HDMI option
SP@ -----> Board ID/Strap pin
H@ -----> 家電下鄉

UMA **REV:B**

DDR3- SODIMM2 PAGE 7

DDR3- SODIMM1 PAGE 6

DDR3 Channel A

AMD Brazos
Zacate TDP~18W
19mmX19mm 413pin BGA
PAGE 3,4,5

CRT → CRT PAGE 13

LVDS → LVDS PAGE 13

TMDS → HDMI PAGE 14

CPU (PROCHOT)
E.C. (CPUFAN#)
32.768KHz 25MHz

PWM FAN SCH. PAGE 23

CPU THERMAL SENSOR *(Reserve Only)* PAGE 4

CPU SideBand TemperatureSense I2C

HT3 1.8GHz

AMD Hudson-M1
23mmX23mm, 605pin BGA
TDP~4.7W
PAGE 8,9,10,11,12

PCI-Express

P0 → **LAN** Atheros AR8158L rev.B (10/100) PAGE 15
25MHz
RJ45 PAGE 15

SATA - HDD PAGE 17 — SATA0 150MB 3 Gb/s

SATA - ODD PAGE 17 — SATA1 150MB 3 Gb/s

P0 → **USB2.0 Port** on board x1 PAGE 21

P9 → **Blue Tooth** PAGE 21

P13 → **Web-Camera** PAGE 13

FFC → **USB BOARD** USB2.0 Ports x2 PAGE 21

P4 → **Mini Card** (Wireless LAN) PAGE 16

P10 → **CardReader** AU6435 PAGE 18
12MHz

PCLK_DEBUG

LPC

Azalia

CLK_PCI_775

Winbond KBC NPCE791L PAGE 24

CPU SideBand TemperatureSense I2C

Audio CODEC Conexant CX20584-21Z PAGE 19

Keyboard TouchPad PAGE 23

SPI ROM PAGE 24

INT MIC PAGE 19

AUDIO CONN (H.P./ MIC) PAGE 20

Speaker CN PAGE 20

CHARGER (ISL88731A) PAGE 25

AMD CPU CORE (OZ8380) PAGE 27 — *CPU*

1V (G5602) PAGE 29 — *NB*

0.9V/DDR 1.5V(RT8207) PAGE 37

SYSTEM 5V/3V (RT8223M) PAGE 26

1.1V(G5602) PAGE 28

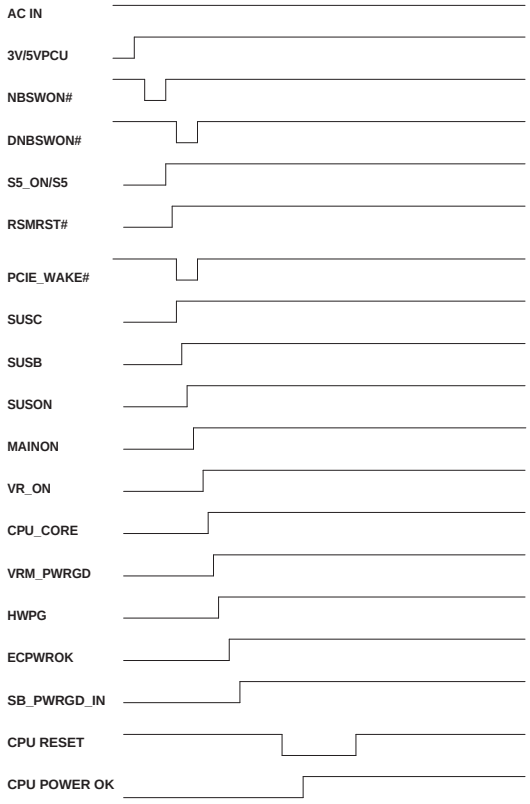
Discharge /Thermal protec PAGE 31

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Tuesday, March 15, 2011	Sheet 1 of 32	

INDEX

Power Sequence



Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

This page is different AMD Nile

U17E

ONTARIO (2.0)
PART 1 OF 5

MEMORY I/F

FT1_ONTARIO

U17A

ONTARIO (2.0)
PART 2 OF 5

PCIE I/F

UMI I/F

FT1_ONTARIO

Del PCIE TP 01/05

Del PCIE TP 01/05

Add R150/R153 for S3 issue
01/13

0902-- change value from 1uF to 1nF

Size	Document Number: ONTARIO MEM & PCIE I/F(1/3) — Rev 1A
Date: Tuesday, March 15, 2011	Sheet 3 of 32

PROJECT : ZQP
Quanta Computer Inc.

E350	AJ0E350VT01
C50	AJ00C50VT02

+1.8V 5,31
+3V 5,6,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

Add HDMI 01/18

ANALOG/DISPLAY/MISC

DIFFERENTIAL ROUTING

0831---follow AMD request for HDMI function

Can remove on MP------>LX

Modify 12/31

Modify 01/11

0830---add circuit

VID Override Circuit

for normal operation
open all switches

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	ONTATIO DISPLAY/CLK/MI(2/3)	1A
Date: Tuesday, March 15, 2011	Sheet 4 of 32	

This page is different AMD Nil

+1.5V_SUS 3,6,7,22,30
+1V 22,29
+1.8V 4,31
+3V 4,6,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+VCORE 22,27
+NBCORE 22,27
VDD_10 3

U17C

11A 440mil viax22

+VCORE

VDD_18 2A 80mil viax4

+1.8V

150mA 10mil viax1

VDDAN_18_DAC

+NBCORE

10A 400mil viax20

C18

C19

BLM18PG221SN1D(220_1.4A)_6

200mA 10mil viax1

T49

+1V

VDDPL_10

0901-- change R7037 P/N and footprint add R

5.5A 220mil viax11

+1.5V_SUS

2A 80mil viax4

500mA 20mil viax1

+3V

POWER

ONTARIO (2.0) PART 4 OF 5

FT1_ONTARIO

U17D

GROUND

ONTARIO (2.0) PART 5 OF 5

FT1_ONTARIO

EMC CAPS

place capacitors under BGA

PROJECT : ZQP
Quanta Computer Inc.

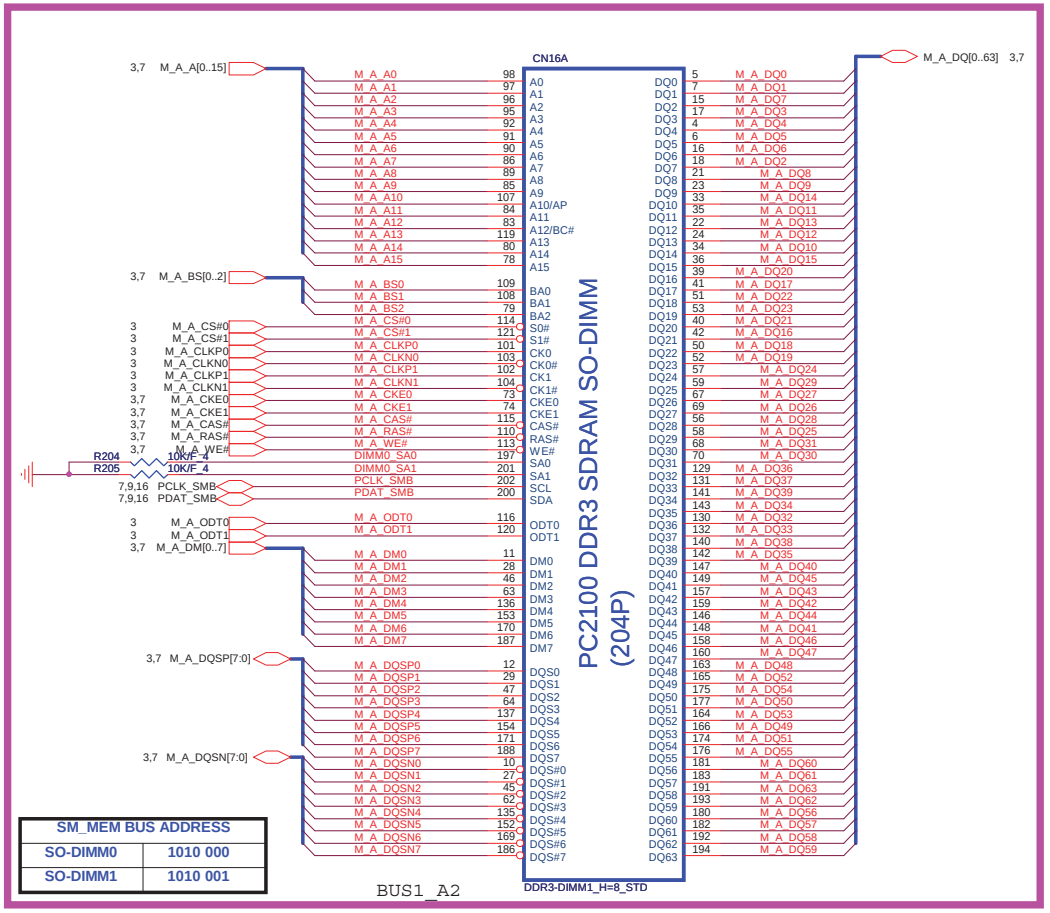
Size	Document Number	Rev
	ONTARIO POWER&DECOUP(3/3)	1A
Date: Tuesday, March 15, 2011	Sheet 5 of 32	

0830--P/N and footprint are follow ZR7B

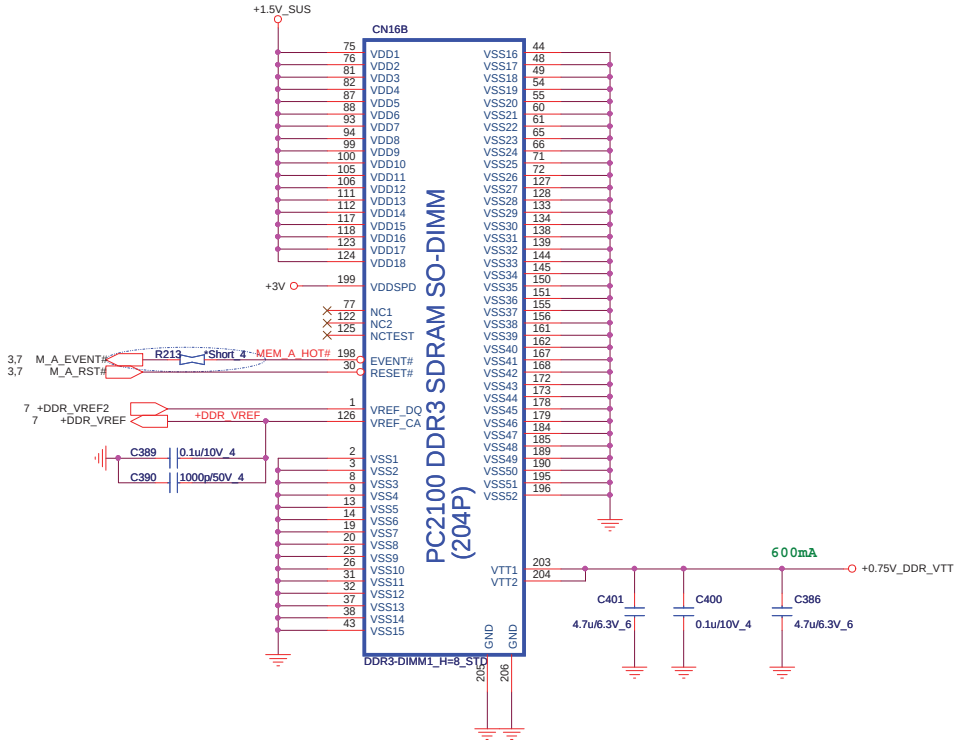
+1.5V_SUS 3,5,7,22,30

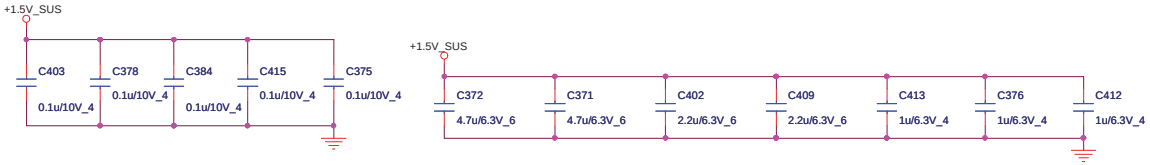
+0.75V_DDR_VTT 7,30

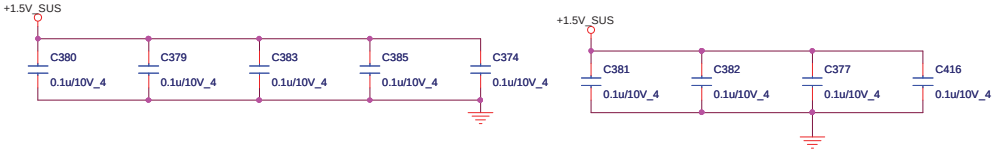
+3V 4,5,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

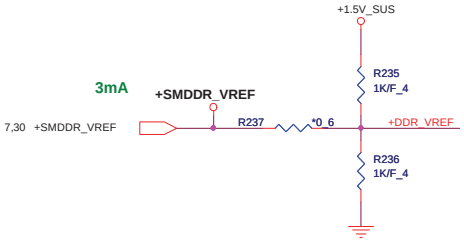


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001









PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number DDR3 SO-DIMM (STD)	Rev 1A
Date: Tuesday, March 15, 2011	Sheet 6 of 32	

0830--P/N and footprint are follow ZR7B

07

+1.5V_SUS 3,5,6,22,30
+0.75V_DDR_VTT 6,30
+3V 4,5,6,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

CN20A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_Standard

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

BUS1_A2

CN20B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_Standard

3mA

+SMDDR_VREF

R244 *0_6

R245 1K/F_4

R246 1K/F_4

C423 4.7u/6.3V_6
C434 4.7u/6.3V_6
C410 2.2u/6.3V_6
C439 2.2u/6.3V_6
C417 1u/6.3V_4
C435 1u/6.3V_4
C420 1u/6.3V_4

C433 0.1u/10V_4
C426 0.1u/10V_4
C428 0.1u/10V_4
C429 0.1u/10V_4

C411 0.1u/10V_4
C430 0.1u/10V_4
C424 0.1u/10V_4
C414 0.1u/10V_4
C418 0.1u/10V_4

C436 0.1u/10V_4
C427 0.1u/10V_4
C425 0.1u/10V_4
C438 0.1u/10V_4
C404 0.1u/10V_4

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 SO-DIMM (STD)	1A
Date: Tuesday, March 15, 2011	Sheet 7 of 32	

This page is different AMD Nile expect RTC circuit

PCIE_VDDR 11
+3V_S5 9,10,11,12,15,21,22,26
+3VPCU 13,22,23,24,25,26,31
+5VPCU 26,27,28,31

+3V_S5
C600 *0.1u/10V_4
U20 TC7SH08FU
15,16,18,24 PLTRST# R441 33_4 A_RST#_L R440 0_4 A_RST#_R
C609 150P/25V_4
24 EC_A_RST#_L R439 *0_4

+3V_S5
C601 *0.1u/10V_4
U21 *TC7SH08FU
A_RST#_L PCIE_RST#
R442 *0_4 SB_GPIO_RST# 9

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U41

U18A
Hudson M1 Part 1 of 5

PCIE_RST# P1
A_RST# L1
Modify 12/31

UMI_RXP0 C96 0.1u/10V_4 UMI_RXP0_C AD26
UMI_RXN0 C99 0.1u/10V_4 UMI_RXN0_C AD27
UMI_RXP1 C86 0.1u/10V_4 UMI_RXP1_C AC28
UMI_RXN1 C93 0.1u/10V_4 UMI_RXN1_C AC29
UMI_RXP2 C80 0.1u/10V_4 UMI_RXP2_C AB29
UMI_RXN2 C84 0.1u/10V_4 UMI_RXN2_C AB28
UMI_RXP3 C70 0.1u/10V_4 UMI_RXP3_C AB26
UMI_RXN3 C75 0.1u/10V_4 UMI_RXN3_C AB27

UMI_TXP0 AE24
UMI_TXN0 AE23
UMI_TXP1 AD25
UMI_TXN1 AD24
UMI_TXP2 AC24
UMI_TXN2 AC25
UMI_TXP3 AB25
UMI_TXN3 AB24

UMI_RX0P UMI_TX0P
UMI_RX0N UMI_TX0N
UMI_RX1P UMI_TX1P
UMI_RX1N UMI_TX1N
UMI_RX2P UMI_TX2P
UMI_RX2N UMI_TX2N
UMI_RX3P UMI_TX3P
UMI_RX3N UMI_TX3N

PCIE_VDDR R105 590/F_4 R108 2K_4 U600_CALRP AD29 U600_CALRN AD28
PCIE_CALRP PCIE_CALRN

LAN 15 PCIE_TXP0_LAN C515 0.1u/10V_4 PCIE_TXP0_C AA28
15 PCIE_TXN0_LAN C516 0.1u/10V_4 PCIE_TXN0_C AA29
WLAN 16 PCIE_TXP1 C514 0.1u/10V_4 PCIE_TXP1_C Y29
16 PCIE_TXN1 C513 0.1u/10V_4 PCIE_TXN1_C Y28
Modify 12/31

GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N
Y26 Y27 W28 W29

15 PCIE_RXP0_LAN AA22
15 PCIE_RXN0_LAN Y21
16 PCIE_RXP1 AA25
16 PCIE_RXN1 AA24
Modify 12/31

GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N
W23 V24 W24 W25

PCI EXPRESS INTERFACES

PCIE_RCLKP/NB_LNK_CLKP M23
PCIE_RCLKN/NB_LNK_CLKN P23

4 DISP_CLKP DISP_CLKP R342 0_4 DISP_CLKP_R U29
4 DISP_CLKN DISP_CLKN R341 0_4 DISP_CLKN_R U28
NB_DISP_CLKP NB_DISP_CLKN

T26 NB_HT_CLKP
T27 NB_HT_CLKN

CPU_CLK 4 APU_CLKP APU_CLKP R339 0_4 APU_CLKP_R V21
4 APU_CLKN APU_CLKN R340 0_4 APU_CLKN_R T21
CPU_HT_CLKP CPU_HT_CLKN

T174 SLT_GFX_CLKP V23
T175 SLT_GFX_CLKN T23
Modify 12/31
SLT_GFX_CLKP SLT_GFX_CLKN

To LAN Controller
15 CLK_PCIE_LANP L29
15 CLK_PCIE_LANN L28

To WLAN Controller
16 CLK_PCIE_WLAN1P N29
16 CLK_PCIE_WLAN1N N28
Modify 12/31

GPP_CLK0P GPP_CLK0N GPP_CLK1P GPP_CLK1N GPP_CLK2P GPP_CLK2N GPP_CLK3P GPP_CLK3N GPP_CLK4P GPP_CLK4N GPP_CLK5P GPP_CLK5N GPP_CLK6P GPP_CLK6N GPP_CLK7P GPP_CLK7N GPP_CLK8P GPP_CLK8N
M29 M28 T25 V25 L24 L23 P25 M25 P29 P28 N26 N27 T29 T28

CLOCK GENERATOR

Add cardreader clock 12/31
18 CardReader_48M R498 0_4 14M_25M_48M L25
14M_25M_48M_OSC
C518 27P/50V_4 25M_X1 L26
25M_X1
Y3 25MHz_30PPM R349 1M/F_4
25M_X2 L27
C519 27P/50V_4
25M_X2

CardReader_48M C606 15p/50V_4
APU_CLKP C614 4.7p/50V_4
APU_CLKN C619 4.7p/50V_4
Add C606,C614,C619 for strong clock
02/15 REV:B

PCI CLKS
PCICLK0 W2 PCI_CLK0 R419 22_4 T93
PCICLK1/GPO36 W1 PCI_CLK1 12
PCICLK2/GPO37 W3 PCI_CLK2 12
PCICLK3/GPO38 W4 PCI_CLK3 12
PCICLK4/14M_OSC/GPO39 Y1 PCI_CLK4 12
STRAP Function To EC

PCIRST# V2 T167

PCI INTERFACE
AD0/GPIO0 AA1
AD1/GPIO1 AA4
AD2/GPIO2 AA3
AD3/GPIO3 AB1
AD4/GPIO4 AA5
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1 dGPU_RST_GPIO T101
AD22/GPIO22 AF2
AD23/GPIO23 AE9 AD23 12
AD24/GPIO24 AD9 AD24 12
AD25/GPIO25 AC11 AD25 12
AD26/GPIO26 AF6 AD26 12
AD27/GPIO27 AF4 AD27 12
AD28/GPIO28 AF3 dGPU_PWROK T100
AD29/GPIO29 AH2
AD30/GPIO30 AG2
AD31/GPIO31 AH3
Modify 01/06
Modify 12/31
Debug STRAPs

All the PCI bus has build-in Pull-UP/Down resistors

CBE0# AA8 T75
CBE1# AD5 T161
CBE2# AD8 T88
CBE3# AA10 T71
FRAME# AE8 T87
DEVSEL# AB9 T80
IRDY# AJ3 T153
TRDY# AE7 T94
PAR AC5 T99
STOP# AF5 T151
PERR# AE6 T98
SERR# AE4 SERR# T158
REQ0# AE11 T73
REQ1#/GPIO40 AH5 T145
REQ2#/CLK_REQ8#/GPIO41 AH4 T146
REQ3#/CLK_REQ5#/GPIO42 AC12 SB_GPIO42 T66
GNT0# AD12 T67
GNT1#/GPO44 AJ5 T149
GNT2#/GPO45 AH6 dGPU_VRON T92
GNT3#/CLK_REQ7#/GPIO46 AB12 GNT3#CLK_REQ7# T72
CLKRUN# AB11 CLKRUN# 24
LOCK# AD7 LOCK# T95
Modify 12/31

INTE#/GPIO32 AJ6
INTF#/GPIO33 AG6 T147
INTG#/GPIO34 AG4 T148
INTH#/GPIO35 AJ4 INTG# T152
INTH# T150

LPC_CLK0 12
LPC_CLK1 12
To STRAPs Page

LPC
LPCCLK0 H24 LPC_CLK0 R101 22_4 CLK_PCI_775 24
LPCCLK1 H25 LPC_CLK1 R115 22_4 PCLK_DEBUG PCLK_DEBUG 16
LAD0 J27 LPC_LAD0 16,24
LAD1 J26 LPC_LAD1 16,24
LAD2 H29 LPC_LAD2 16,24
LAD3 H28 LPC_LAD3 16,24
LFRAME# G28 LPC_LFRAME# 16,24
LDRQ0# J25 LPC_DRQ#0 16
LDRQ1#/CLK_REQ6#/GPIO49 AA18 T63
SERIRQ/GPIO48 AB19 IRQ_SERIRQ 24

CPU
ALLOW_LDTSTP/DMA_ACTIVE# G21 ALLOW_LDTSTP 4
PROCHOT# H21 H_PROCHOT# 4,10,24
LDT_PG K19 APU_PWRGD 4
LDT_STP# G22 T56
LDT_RST# J24 LDT_RST# 4

RTC
32K_X1 C1 RTC_X1
32K_X2 C2 RTC_X2
RTCCLK D2 PCH_SUSCLK R409 *10K/F_4 +3V_S5
INTRUDER_ALERT# B2 INTRUDER_ALERT# T156
VDDBT_RTC_G B1 +AVBAT
RTC_CLK must ready refore RSMRST#

C603 22p/50V_4
R407 20M_6
Y5 32.768KHZ
C602 22p/50V_4

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

PCH_SUSCLK PCH_SUSCLK 24

RTC

20mils +3VPCU D22 RB500V-40 20mils +AVBAT
20mils +3VRTC_2 D23 RB500V-40 +3VRTC R406 510/F_6 20mils
C599 1u/6.3V_4
G1 *SHORT_PAD1
R423 1K_4
20mils

Del Q33,R434,R435,R444 from BOMs, ZQE no support RTC charge circuits.

20MIL VCCRTC_2 1 3 RTC_N01 R434 *16K_6 +5VPCU
20MIL Q33 *MMBT3904 2 RTC_N03
R435 *68.1K/F_4
R444 *150K/F_6

1VCCRTC_2 2 CN13 BAT_CONN

CR2032 (Non-Chargeable)
AHL03003014
AHL030M0009

BG625000486

PROJECT : ZQP Quanta Computer Inc.			
Size	Document Number HUDSON PCIE/LPC/CPU IF(1/5)		Rev 1A
Date: Tuesday, March 15, 2011	Sheet 8 of 32		

This page is different AMD Nile

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson/TV tuner /DDR3/DDR3 thermal/Accelerometer

+3V R125 2.2K_4 PCLK_SMB
+3V R131 2.2K_4 PDAT_SMB

+3V R179 *10K/F_4 SUS_STAT#
+3V R133 4.7K_4 NB_PWRGD

+3V_S5 R175 10K/F_4 CPU_THERMTRIP#

SB/ PWR_GOOD / VDDIO_33_S

+3V_S5 R437 *10K/F_4 SYS_RST#
+3V R120 *10K/F_4 SIO_A20GATE

By AMD confirm

+3V_S5 R436 *10K/F_4 DNBSWON#
R189 10K/F_4 PCIE_WAKE#
R352 10K/F_4 SB_SCLK3
R353 10K/F_4 SB_SDATA3
R193 10K/F_4 SB_PWRGD_IN
R116 2.2K_4 SB_SCLK4
R102 2.2K_4 SB_SDATA4

+3V, +3V_S5 4,5,6,7,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31 / 8,10,11,12,15,21,22,26

U18D

Hudson M1
Part 4 of 5

3 APU_MEMHOT# J2
T163 RI# K1
T157 SPI_CS3# D3
24 SUSB# F1
24 SUSC# H1
24 DNBSWON# F2
SB_PWRGD_IN H5
SUS_STAT# G6
SB_TEST0 B3
T155 SB_TEST1 C4
T97 SB_TEST2 F6
T82 SIO_A20GATE AD21
24 SIO_A20GATE AE21
24 SIO_RCIN# K2
24 SIO_EXT_SCI# J29
24 SIO_EXT_SMI# H2
T166 SYS_RST# J1
15,24 PCIE_WAKE# H6
T169 F3
4 CPU_THERMTRIP# J6
CPU_THERMTRIP# NB_PWRGD AC19
C346 100p/50V_4
24 ICH_RSMRST# G1

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC A10 T144
USB_RCOMP G19 USB_RCOMP_SB R139 11.8K/F_4

USB 1.1 USB MISC

USB_FSD1P/GPIO186 J10 T69
USB_FSD1N H11 T70
USB_FSD0P/GPIO185 H9 T76
USB_FSD0N J8 T85

USB_HSD13P B12 A12
USB_HSD13N
USB_HSD12P F11 E11 T192 T194
USB_HSD12N
Add TP 01/11
USB_HSD11P E14 E12
USB_HSD11N
USB_HSD10P J12 J14
USB_HSD10N

DEL MINI CARD 12/31

USB_HSD9P A13 B13 USBP9+ 16 / USBP9- 16 WL1
USB_HSD9N
USB_HSD8P D13 C13 USBP8+ 21 / USBP8- 21 EXT BLUETOOTH
USB_HSD8N
USB_HSD7P G12 G14 USBP7+ 21 / USBP7- 21 BLUETOOTH
USB_HSD7N
USB_HSD6P G16 G18 USBP6+ 18 / USBP6- 18 4 IN 1 CARD READER (MMC)
USB_HSD6N
USB_HSD5P D16 C16 USBP5+ 21 / USBP5- 21 USB3 Connector (Daughter)
USB_HSD5N
USB_HSD4P B14 A14
USB_HSD4N
USB_HSD3P E18 E16 T195 T196
USB_HSD3N
Add TP 01/11
USB_HSD2P J16 J18 USBP2+ 13 / USBP2- 13 CCD
USB_HSD2N
USB_HSD1P B17 A17 USBP1+ 21 / USBP1- 21 USB2 Connector (Daughter)
USB_HSD1N
USB_HSD0P A16 B16 USBP0+ 21 / USBP0- 21 USB1 Connector (MB Side)
USB_HSD0N

USB 2.0

T62 AD19
T64 CLK_REQ4#/SATA_IS0#/GPIO64 AA16
CLK_REQ3#/SATA_IS1#/GPIO63 AB21
SMARTVOLT1/SATA_IS2#/GPIO50 AC18
15 PCIE_REQ_LAN# R140 *Short_4 8 SB_GPIO_RST# CLK_REQ0#/SATA_IS3#/GPIO60 PCIE_REQ_LAN#_R AF20
Modify 12/31 T86 dGPU_PWR_EN AE19
SATA_IS4#/FANOUT3/GPIO55 T61 AF19
SATA_IS5#/FANIN3/GPIO59
19 SPKR SPKR/GPIO66 AD22
6,7,16 PCLK_SMB PCLK_SMB SCL0/GPIO43 AE22
6,7,16 PDAT_SMB PDAT_SMB SDA0/GPIO47
+3V_S5 R184 10K/F_4 R185 10K/F_4 SB_SMBCLK1 SCL1/GPIO227 F5
SB_SMBDATA1 SDA1/GPIO228 F4
Modify 12/31 T183 PCIE_REQ_WLAN2#_R CLK_REQ2#/FANIN4/GPIO62 AH21
16 PCIE_REQ_WLAN1# R142 Short_4 PCIE_REQ_WLAN1#_R CLK_REQ1#/FANOUT4/GPIO61 AB18
T168 ACCLED_EN IR_LED#/LLB#/GPIO184 E1
T142 SMARTVOLT2/SHUTDOWN#/GPIO51 AJ21
T159 DDR3_RST#/GEVENT7# H4
T90 GBE_LED0/GPIO183 D5
T81 GBE_LED1/GEVENT9# D7
T91 GBE_LED2/GEVENT10# G5
T165 GBE_STAT0/GEVENT11# K3
T59 CLK_REQG#/GPIO65/OSCIN AA20

GPIO

T164 CPU_MEMHOT#_IN H3
+3V_S5 R187 *10K/F_4 21 OC_6# BLINK/USB_OC7#/GEVENT18# D1
21 OC_4# USB_OC6#/IR_TX1/GEVENT6# E4
USB_OC5#/IR_TX0/GEVENT17# D4
USB_OC4#/IR_RX0/GEVENT16# E8
T77 USB_OC3#/AC_PRES/TDO/GEVENT15# F7
T84 USB_OC2#/TCK/GEVENT14# E7
T83 USB_OC1#/TDI/GEVENT13# F8
T78 USB_OC0#/TRST#/GEVENT12#

USB OC

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

SCL2/GPIO193 D25 SB_SCLK2 R360 10K/F_4 +3V_S5
SDA2/GPIO194 F23 SB_SDATA2 R362 10K/F_4
SCL3_LV/GPIO195 B26 SB_SCLK3 SB_SCLK3 4
SDA3_LV/GPIO196 E26 SB_SDATA3 SB_SDATA3 4
EC_PWM0/EC_TIMER0/GPIO197 T53 F25
EC_PWM1/EC_TIMER1/GPIO198 T125 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 SB_GPIO199 R132 *2.2K_4
EC_PWM3/EC_TIMER3/GPIO200 E21 SB_GPIO200 R134 2.2K_4

has checked with AMD FAE already--Allen

GPIO200	GPIO199
H,H = Reserved	
H,L = SPI ROM (DEFAULT)	
L,H = LPC ROM	
L,L = FWH ROM	

EMBEDDED CTRL

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28

KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

To Azalia
HD audio interface is 3.3S5 voltage

for EMI
19 ACZ_BITCLK_AUDIO C607 *10p/50V_4 R424 33_4 R412 *10K_4 ACZ_BITCLK_R M3
12 ACZ_SDOUT ACZ_SDOUT N1
19 ACZ_SDOUT_AUDIO R425 33_4 L2
C608 *10p/50V_4 M2
19 ACZ_SDIN0 C604 *10p/50V_4 R411 *10K_4 M1
M4
19 ACZ_SYNC_AUDIO R414 33_4 ACZ_SYNC_R N2
19 ACZ_RESET#_AUDIO R416 33_4 ACZ_RST#_R P2
C605 *10p/50V_4

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

R417 10K/F_4 R428 10K/F_4 GBE_COL T1
GBE_CRS T4
L6
+3V_S5 R171 10K/F_4 GBE_MDIO L5
T9
U1
U3
T2
U2
T5
R169 10K/F_4 GBE_RXERR V5
P5
M5
P9
T7
P7
M7
P4
M9
+3V_S5 R161 10K/F_4 GBE_PHY_INTR V7

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE LAN

Modify 12/31 T172 SB_SDATA4 E23
T171 SB_SCLK4 E24
T58 SB_GPIO166 F21
T114 SB_GPIO160 G29

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160

T116 AC_OK D27
T115 BAT_INT# F28
F29
E27

PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

HudsonM1

System PWR_OK(CLG)

+3V_S5 C349 *0.1u/10V_4
U8 TC7SH08FU
T193 SB_PWRGD_IN 4
Modify 12/31
2 CPU_COREPG 27
1 PWROK_EC PWROK_EC 24
R194 100K_4

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON ACPI/GPIO/USB(2/5)	1A
Date: Tuesday, March 15, 2011	Sheet 9 of 32	

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO Hudson M1

AVDD_SATA 11
+3V 4,5,6,7,9,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,11,12,15,21,22,26

This page is different AMD Nile

U18B

Hudson M1
Part 2 of 5

SATA HDD

17 SATA_TXP0 — C592 .01U/16V/X7R_4 — SATA_TXP0_C — AH9 SATA_TX0P
17 SATA_TXN0 — C590 .01U/16V/X7R_4 — SATA_TXN0_C — AJ9 SATA_TX0N
AJ8 SATA_RX0N
AH8 SATA_RX0P
17 SATA_RXN0
17 SATA_RXP0

SATA ODD

17 SATA_TXP1 — C588 .01U/16V/X7R_4 — SATA_TXP1_C — AH10 SATA_TX1P
17 SATA_TXN1 — C585 .01U/16V/X7R_4 — SATA_TXN1_C — AJ10 SATA_TX1N
AG10 SATA_RX1N
AF10 SATA_RX1P
17 SATA_RXN1
17 SATA_RXP1

AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

SERIAL ATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF Hudson M1

XTLVDD_SATA-- SATA crystal power

PLVDD_SATA-- SATA PLL POWER

AVDD_SATA — R147 1K/F_4 — R143 931/F_4 — SATA_CALRP AB14 — SATA_CALRN AA14 — SATA_CALRP SATA_CALRN

22 SATA_LED# — AD11 SATA_ACT#/GPIO67

C575 *22p/50V_4 — Y4 *25MHz_30PPM — R381 *1M/F_4 — C582 *22p/50V_4
SATA_X1 AD16 — SATA_X1
SATA_X2 AC16 — SATA_X2

T89 SPI_DI J5 — SPI_DI/GPIO164
T96 SPI_DO E2 — SPI_DO/GPIO163
T160 SPI_CLK K4 — SPI_CLK/GPIO162
T79 SPI_CS1# K9 — SPI_CS1#/GPIO165
T162 ROM_RST# G2 — ROM_RST#/GPIO161

SPI ROM

HudsonM1

FC_CLK AH28 T123
FC_FBCLKOUT AG28 T124
FC_FBCLKIN AF26 T47
FC_OE#/GPIOD145 AF28 T121
FC_AVD#/GPIOD146 AG29 T122
FC_WE#/GPIOD148 AG26 T128
FC_CE1#/GPIOD149 AF27 T119
FC_CE2#/GPIOD150 AE29 T118
FC_INT1/GPIOD144 AF29 T120
FC_INT2/GPIOD147 AH27 T129
FC_ADQ0/GPIOD128 AJ27 T126
FC_ADQ1/GPIOD129 AJ26 T133
FC_ADQ2/GPIOD130 AH25 T132
FC_ADQ3/GPIOD131 AH24 T137
FC_ADQ4/GPIOD132 AG23 T135
FC_ADQ5/GPIOD133 AH23 T134
FC_ADQ6/GPIOD134 AJ22 T138
FC_ADQ7/GPIOD135 AG21 T143
FC_ADQ8/GPIOD136 AF21 T139
FC_ADQ9/GPIOD137 AH22 T140
FC_ADQ10/GPIOD138 AJ23 T141
FC_ADQ11/GPIOD139 AF23 T131
FC_ADQ12/GPIOD140 AJ24 T136
FC_ADQ13/GPIOD141 AJ25 T130
FC_ADQ14/GPIOD142 AG25 T46
FC_ADQ15/GPIOD143 AH26 T127

FLASH

FANOUT0/GPIO52 W5 BOARD_ID0
FANOUT1/GPIO53 W6 BOARD_ID1
FANOUT2/GPIO54 Y9 SB_PROCHOT#
FANIN0/GPIO56 W7 BOARD_ID2
FANIN1/GPIO57 V9 BOARD_ID3
FANIN2/GPIO58 W8 BOARD_ID4

0831--modify location

TEMPIN0/GPIO171 B6 TEMPIN0
TEMPIN1/GPIO172 A6 TEMPIN1
TEMPIN2/GPIO173 A5 TEMPIN2
TEMPIN3/TALERT#/GPIO174 B5 SB_TALERT# — SB_TALERT# 4
TEMP_COMM C7

VIN0/GPIO175 A3 CPU_TYPE
VIN1/GPIO176 B4 SB_HOLE_TIME
VIN2/GPIO177 A4 CPU_SENSOR
VIN3/GPIO178 C5 VIN2 R390 10K_4
VIN4/GPIO179 A7 VIN3 R387 10K_4
VIN5/GPIO180 B7 VIN4 R386 10K_4
VIN6/GBE_STAT3/GPIO181 B8 VIN5 R383 10K_4
VIN7/GBE_LED3/GPIO182 A8 BOARD_ID5

HW MONITOR

NC1 G27
NC2 Y2

4,8,24 H_PROCHOT# — H_PROCHOT# — D6 RB500V-40 — SB_PROCHOT#

0831--add circuit

AMD recommand : TEMPIN0 / TEMPIN1 / TEMPIN2 can not maintain on floating stages when without usage. Do not care pull high or pull down.

TEMPIN2 — R388 10K_4
TEMPIN1 — R389 10K_4
TEMPIN0 — R391 10K_4

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0

	GPIO57
(Dis) SW	1
UMA	0

SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0

	GPIO58
With HDMI	1
Without HDMI	0

DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

	GPIO182
PX4.0	1
PX3.0	0

+3V

GPIO52: R182 10K_4 BOARD_ID0 R192 *10K_4
GPIO53: R181 10K_4 BOARD_ID1 R191 *10K_4
GPIO56: R180 10K_4 BOARD_ID2 R190 *10K_4
GPIO57: R158 10K_4 BOARD_ID3 R157 *SP@10K_4
GPIO58: R418 *SP@10K_4 BOARD_ID4 R429 SP@10K_4

GPIO 58 define to HDMI strap pin
02/11 REV:B

+3V_S5

GPIO182: R385 *SP@10K_4 BOARD_ID5 R384 10K_4
R400 *10K/F_4 CPU_TYPE R399 10K/F_4
R395 *10K/F_4 CPU_SENSOR R394 10K/F_4
R398 *10K/F_4 SB_HOLE_TIME R397 10K/F_4

Modify 01/14

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON SATA/BIDs(3/5)	1A
Date: Tuesday, March 15, 2011	Sheet 10 of 32	

+3V 4,5,6,7,9,10,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+1.1V 22,28,31
+3V_S5 8,9,10,12,15,21,22,26
+1.1V_S5 28
AVDD_SATA 10
VDDIO_AZ 12

This page is different AMD Nile

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

GPIOD Interface Not Implemented connected to GND through a 0-Ω resistor

U18C Hudson M1 Part 3 of 5

POWER

42mA
150mA 10mil viax1
22mA
1115mA 50mil viax3
15mA 5mil vaix1
1354mA 60mil viax3
534mA 25mil viax2
88mA
790mA 35mil viax2
382mA 20mil viax1
49mA
165mA 10mil viax1
15mA
58mA
46mA
65mA
16mA
12mA
5mA

U18E Hudson M1 Part 5 of 5

GROUND

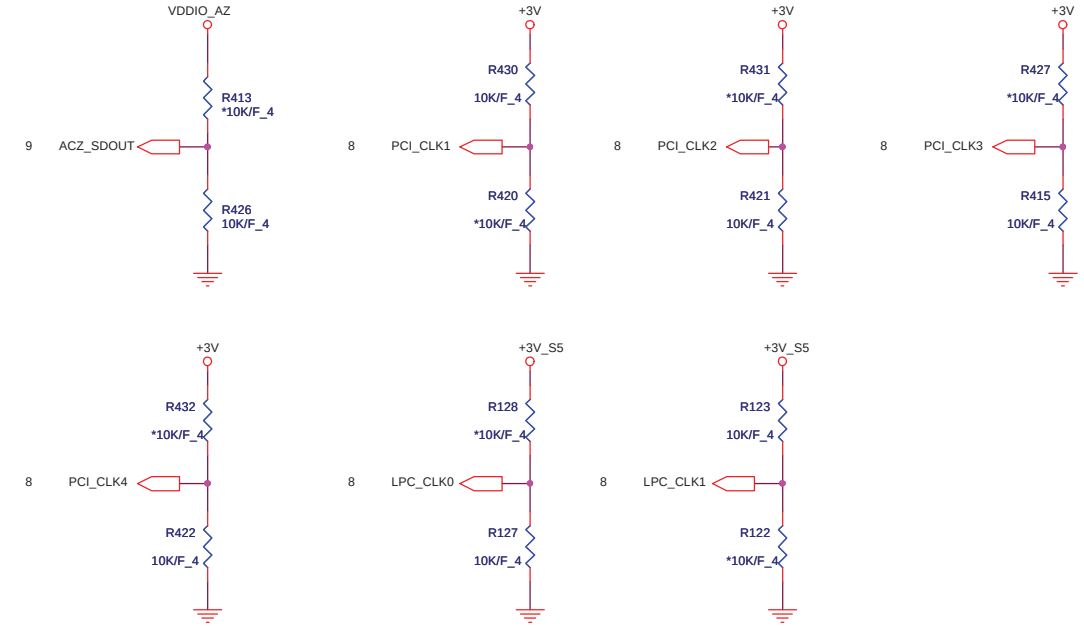
PROJECT : ZQP
Quanta Computer Inc.
Size | Document Number: HUDSON PWR/GND(4/5) | Rev 1A
Date: Tuesday, March 15, 2011 | Sheet 11 of 32

VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

REQUIRED STRAPS



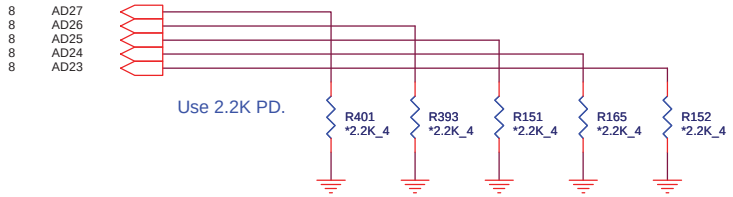
PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date: Tuesday, March 15, 2011	Sheet 12 of 32	

CRT

OPTION SIGNAL FROM NB to LVDS/CRT for UMA

13

4 INT_DDCCLK → INT_DDCCLK
4 INT_DDCDATA → INT_DDCDATA
4 INT_CRT_HSYNC → INT_CRT_HSYNC
4 INT_CRT_VSYNC → INT_CRT_VSYNC
4 INT_CRT_RED → INT_CRT_RED
4 INT_CRT_GRE → INT_CRT_GRE
4 INT_CRT_BLU → INT_CRT_BLU

+5V, F1 SMD1206P100TF, CRTVDD5_F, D21 B0520WS-7-F (30V/ 1A, 30V/ 0.5A), CRTVDD5, C560 .22u/6.3V_4

INT_CRT_RED, INT_CRT_GRE, INT_CRT_BLU
L28 BLM18BA470SN1_6, L27 BLM18BA470SN1_6, L26 BLM18BA470SN1_6
CRT_R1, CRT_G1, CRT_B1
R136 150/F_4, R141 150/F_4, R138 150/F_4
C240 10P/50V_4, C216 10P/50V_4, C242 10P/50V_4, C282 10P/50V_4, C279 10P/50V_4, C294 10P/50V_4

CN12 CRT: CRT_GND_1, CRT_11, DDCDAT_1, CRTHSYNC, CRTVSYNC, DDCCLK_1, CRT_GND_2; T68

CRT_GND_1 R33 0_6, CRT_GND_2 R34 0_6
Add R33,R34 for ESD
02/16 REV:B

+3V, C580 0.1u/10V_4, C239 .22u/6.3V_4, CRT_BYP, C223 0.1u/10V_4
U16 CM2009-02QR
VCC_SYNC, SYNC_OUT2, SYNC_OUT1, VCC_DDC, BYP, SYNC_IN2, SYNC_IN1, VCC_VIDEO, VIDEO_1, VIDEO_2, VIDEO_3, DDC_IN1, DDC_IN2, DDC_OUT1, DDC_OUT2, GND
CRTVDD5, CRTVSYNC, CRTHSYNC, INT_CRT_VSYNC, INT_CRT_HSYNC, INT_DDCCLK, INT_DDCDATA, DDCCLK_1, DDCDAT_1
R369 2.7K_4, R368 2.7K_4, R370 2.7K_4, R367 2.7K_4

C551 *.1u/10V_4 CRTVDD5
C125 *10P/50V_4 CRTVSYNC
C202 *10P/50V_4 CRTHSYNC
C108 *10P/50V_4 DDCCLK_1
C570 *10P/50V_4 DDCDAT_1

LVDS(LDS)

4 INT_EDIDCLK, 4 INT_EDIDDATA, 4 INT_TXLCLKN, 4 INT_TXLCLKP, 4 INT_TXLOUTN0, 4 INT_TXLOUTP0, 4 INT_TXLOUTN1, 4 INT_TXLOUTP1, 4 INT_TXLOUTN2, 4 INT_TXLOUTP2

24 CONTRAST, 4 INT_LVDS_PWM

+3V Pull up at APU
R6 *2.2K_4, R5 *2.2K_4, R3 *0_4, R4 0_4
INT_EDIDDATA, INT_EDIDCLK, LVDS_BRIGHT, BL_ON, INT_TXLCLKP, INT_TXLCLKN, INT_TXLOUTP0, INT_TXLOUTN0, INT_TXLOUTP1, INT_TXLOUTN1, INT_TXLOUTP2, INT_TXLOUTN2

CN6 LVDS_CONN

VIN, +3V
C12 4.7u/25V_8, C13 1000P/50V_4, C2 0.1u/10V_4, C7 1000P/50V_4

Del R26,R27 and add RP5
and Swap nets
02/16 REV:B

Add Pin23 to GND
01/11

RP5 0_4P2R_4: USBP2- / USBP2+ → USBP2- R / USBP2+ R
*DLW21HN900SQ2L/330mA/90ohm L50
CCD_POWER, LCDVCC_L, LCD_VIN

VIN, L5 *0_6, L4 0_6, LCD_VIN, C14 *10P/50V_4, C11 *10P/50V_4
+3V, L1 0_6, CCD_POWER, C10 *10P/50V_4, C40 *4.7u/6.3V_6, C15 *10P/50V_4
C38 *10P/50V_4, C39 *10P/50V_4

change Pin defined as ZRH 01/03

LCD PW(LDS)

+3V, C8 1U/6.3V_4
U1 IC(5P)G5243T11U: IN, IN, ON/OFF, OUT, GND, GND
4 INT_LVDS_DIGON
R2 100K_4

LCDVCC_L2 0_6 LCDVCC_L
C4 *10P/50V_4, C9 *10P/50V_4
40mil
LCDVCC
C5 1U/6.3V_4, C1 *.1u/10V_4, C6 .01u/16V_4, C3 22u/6.3V_8

Backlight Control(LDS)

+3V
R8 10K_4, R7 10K_4
BL_ON, D2 BAS316, LID591# 24
BL# 2
Q1 2N7002K, Q2 DTC144EUA, EC_FPBACK# 24
4 INT_LVDS_BLON
Q3 2N7002K
R9 100K_4

Lid Switch (HSR)

+3VPCU, C480 1U/6.3V_4
R269 *470K/F_4
LID591#
HE1 PT3661-BB SOT23_123-2_8-1_9

PT3661-BB (PLC) : AL003661003
ME268-002 (PCE) : AL000268000

PROJECT : ZQP
Quanta Computer Inc.

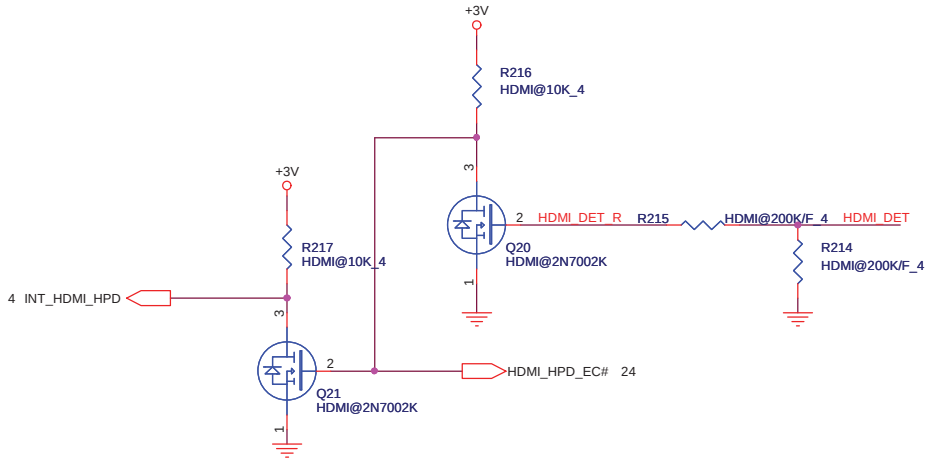
Size	Document Number	Rev
	CRT/LVDS/LID	1A
Date: Tuesday, March 15, 2011	Sheet 13 of 32	

HDMI SDVO I2C Control

4 HDMI_DDCDATA
4 HDMI_DDCCLK
HDMI_DDCDATA
HDMI_DDCCLK

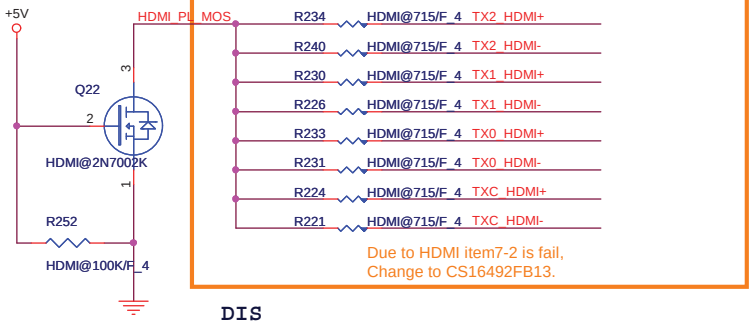
HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



HDMI (HDM)

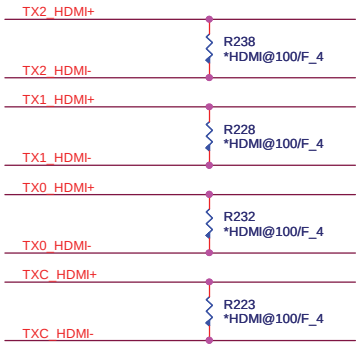
Close to HDMI Connector



DIS
Stuff 499 ohm CS14992FB24

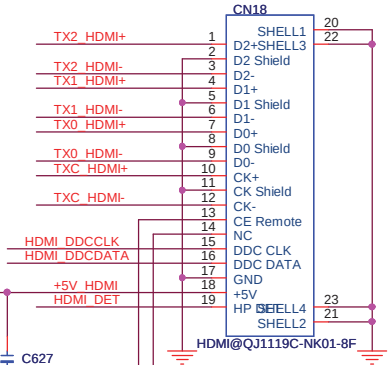
EMI reserve for HDMI(EMC)

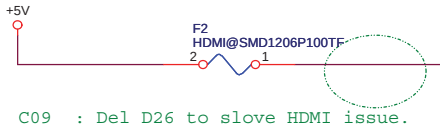
Close connector



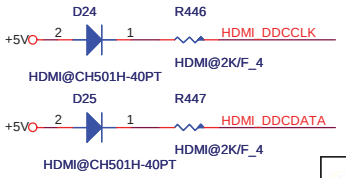
Added HDMI function
01/19 REV:B

HDMI PORT (HDM)





C09 : Del D26 to slove HDMI issue.



4 TX2_HDMI+
4 TX2_HDMI-
4 TX1_HDMI+
4 TX1_HDMI-
4 TX0_HDMI+
4 TX0_HDMI-
4 TXC_HDMI+
4 TXC_HDMI-
TX2_HDMI+
TX2_HDMI-
TX1_HDMI+
TX1_HDMI-
TX0_HDMI+
TX0_HDMI-
TXC_HDMI+
TXC_HDMI-

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date: Tuesday, March 15, 2011	Sheet 14 of 32	

LAN (LAN)

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<Layout note>
Close to Pin1

If use LDO mode L55 no stuff

L55 4.7uH/1A DCR:0.15ohm LX
C615 0.1U/16V_4
C616 10U/10V_8
Modify 01/06
VDDCT
VDDCT_REG R35 *52LDO@0/J_6
C37 0.1U/16V_4
C48 *52LDO@1U/10V_4

C365 33P/50V_4 XTLO_LAN
XTLI_LAN
Y2 25MHz-LAN
C364 33P/50V_4

BG625000486

Add R28/D4 for 家電下鄉
01/13

U4 U5
X-TX1N X-TX1P X-TX0N X-TX0P
TX1N TX1P TX0N TX0P
*H@UCLAMP2512T.TCT

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

76.1mA ; 30mil <Layout note> Close to Pin2
+3V_S5 +3V_LAN
R195 0/J_6
C353 10U/10V_8 C366 1U/10V_4 C361 0.1U/16V_4
* Int. PU in SB

U9
8,16,18,24 PLTRST#
9,24 PCIE_WAKE#
VDDCT_REG 20mil
VDDCT 20mil
AVDDL 20mil
AVDDH 20mil
C373 0.1U/16V_4
C618 1U/10V_4 C624 0.1U/16V_4
C368 1U/10V_4 C367 0.1U/16V_4
R203 2.37K/F_4 RBIAS
XTLO_LAN XTLI_LAN
TX0P TX0N TX1P TX1N
PCIE_REQ_LAN# R506 *0/J_4

AR8158
4X4mm
32Pin QFN
AR8158-BL1A-RL

PU in CLK Gen.
CLKREQn R485 0/J_4 R505 *0/J_4 DVDDL PCIE_REQ_LAN# 9
SMCLK SMBUS for debug only
SMDATA
TESTMODE
C406 0.1U/16V_4
NC
TX_N PCIE_RXN0 C407 .1U/10V_4 PCIE_RXN0_LAN 8
TX_P PCIE_RXP0 C408 .1U/10V_4 PCIE_RXP0_LAN 8
AVDDL
REFCLK_N CLK_PCIE_LANN 8
REFCLK_P CLK_PCIE_LANP 8
C621 0.1U/16V_4
RX_P PCIE_TXP0_LAN 8
RX_N PCIE_TXN0_LAN 8
C622 0.1U/16V_4
DVDDL_REG DVDDL 20mil
LED[0] LAN_ACTLED
LED[1] Del LED
C397 0.1U/16V_4 C393 1U/10V_4
GND1
GND10 GND9 GND8 GND7 GND6 GND5 GND4 GND3 GND2
42 41 40 39 38 37 36 35 34

<Layout note>
Close to LAN Chip
1nF reserved for EMI
RN2 49.9/F_4P2R
RN1 49.9/F_4P2R
C29 0.1U/16V_4 C33 *1000P/50V_4
C66 0.1U/16V_4 C35 *1000P/50V_4

Add R29
01/13
R29 5.1K/J_8 LAN_ACTLED
Active LED Pin:
Non-overclocking=>active high

+3V_S5 2 VDD33
+1.1V analog power 24/27 AVDDL
+1.7V analog power 6 VDDCT
ATHEROS AR8158
AVDDL_REG 7 +1.1V regulator output (For all the analog 1.1V supply pins)
AVDDH_REG 10 +2.7V regulator output
DVDDL_REG 30 +1.1V regulator output (For all the digital 1.1V supply pins)
VDDCT_REG 5 +1.8V regulator output (For VDDCT when LDO mode)
LX 1 +1.7V Switching regulator (For VDDCT when switching mode)

TRANSFORMER (LAN)

exchange pair 0/1
0110

VDDCT L54 0/J_6
CX8EG601000: 0.5A/600ohm_6
AVDD_CEN
C356 *1U/6.3V_4
C613 0.1U/16V_4
C363 *1000P/50V_4
C394 0.1U/16V_4
C357 *1000P/50V_4
1nF reserved for EMI

U22
TX1N TX1P TX0N TX0P
TD- TD+ CT NC NC CT RD- RD+
TX- TX+ CT NC NC CT RX- RX+
X-TX1N X-TX1P TERM0 TERM1 X-TX0N X-TX0P
NS0014LF_Bothhand

R199 75/F_8 R196 75/F_8
R28 *H@1M_8
*H@B88069X9231T2032 D4
C354 220P/3KV_1808 TERM9

Add R28/D4 for 家電下鄉
01/13

change C354 to CH122GK1I10 for EMI
02/16 REV:B

TX0P EC38 6.8p/50V_4
TX0N EC40 6.8p/50V_4
TX1P EC43 6.8p/50V_4
TX1N EC46 6.8p/50V_4
Add EC38,EC40,EC43,EC46 for EMI
02/16 REV:B

Del 0110

RJ45 Connector (LAN)

Del LAN LED 01/05

CN15
YELLOW_N YELLOW_P
X-TX0P X-TX0N X-TX1P TERM9 X-TX1N TERM9
GND2 GND1
LAN_GND_2 R31 V-PORT-0603-220K
LAN_GND_1 R32 V-PORT-0603-220K
chenge to ESD
01/18 REV:B
GREEN_N GREEN_P
RJ45

change RJ45 connector without LED
03/02

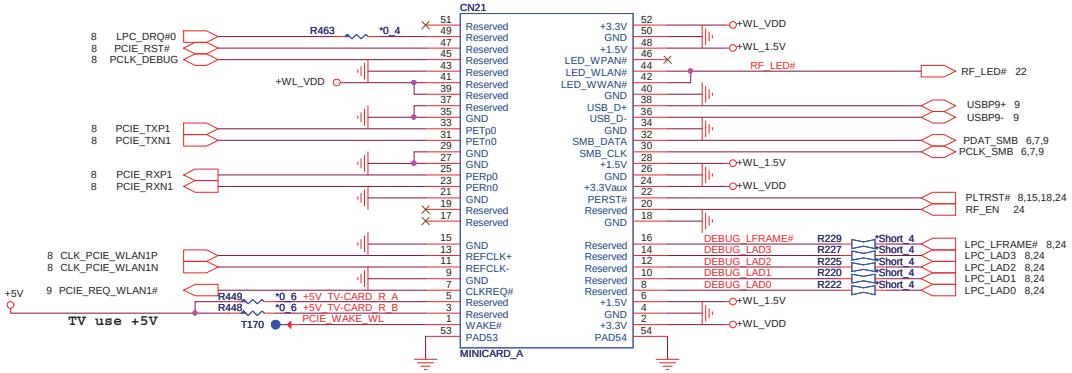
We will change RJ45 connector

PROJECT : ZQP
Quanta Computer Inc.
Size
Document Number
LAN AR8158L
Rev 1A
Date: Tuesday, March 15, 2011
Sheet 15 of 32

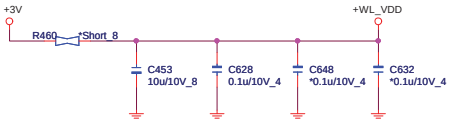
MINI-CARD WLAN(MPC)

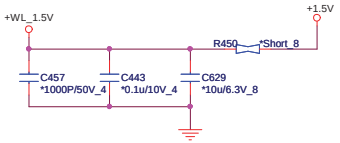
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug

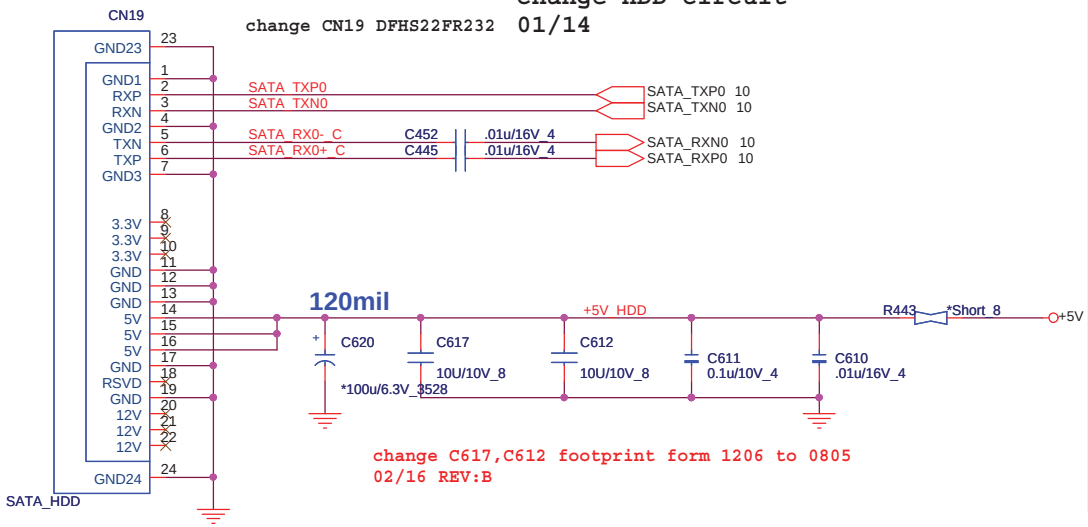




PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number MINI PCI-E card	Rev 1A
Date: Tuesday, March 15, 2011	Sheet 16 of 32	

SATA HDD

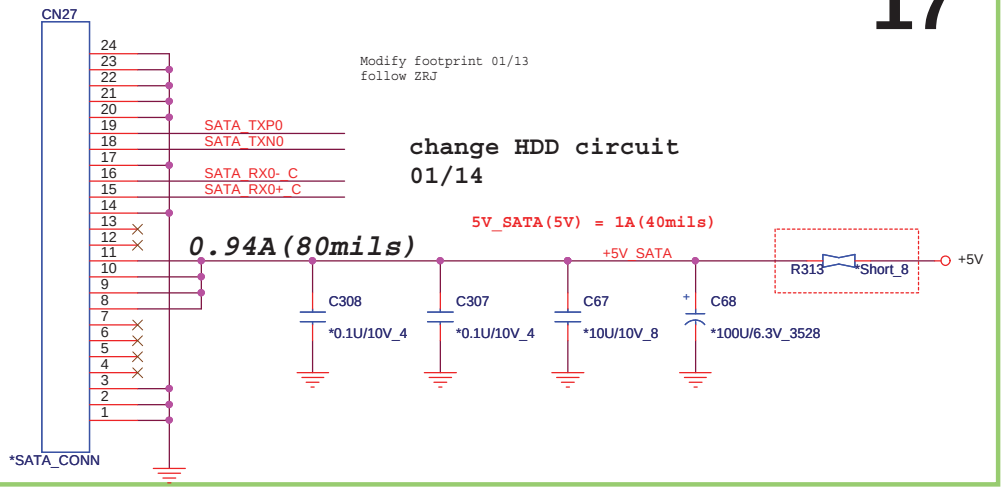
change HDD circuit
change CN19 DFHS22FR232 01/14



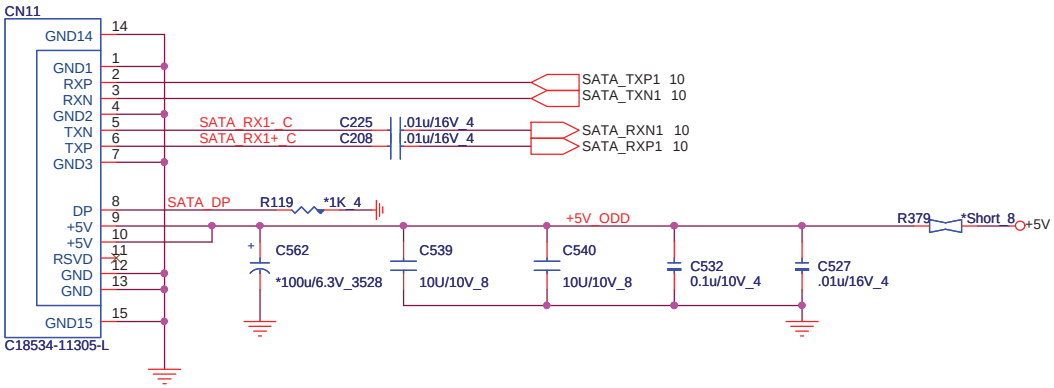
change C617,C612 footprint form 1206 to 0805
02/16 REV:B

SATA HDD(HDD)

17



SATA ODD



change C539,C540 footprint form 1206 to 0805
02/16 REV:B

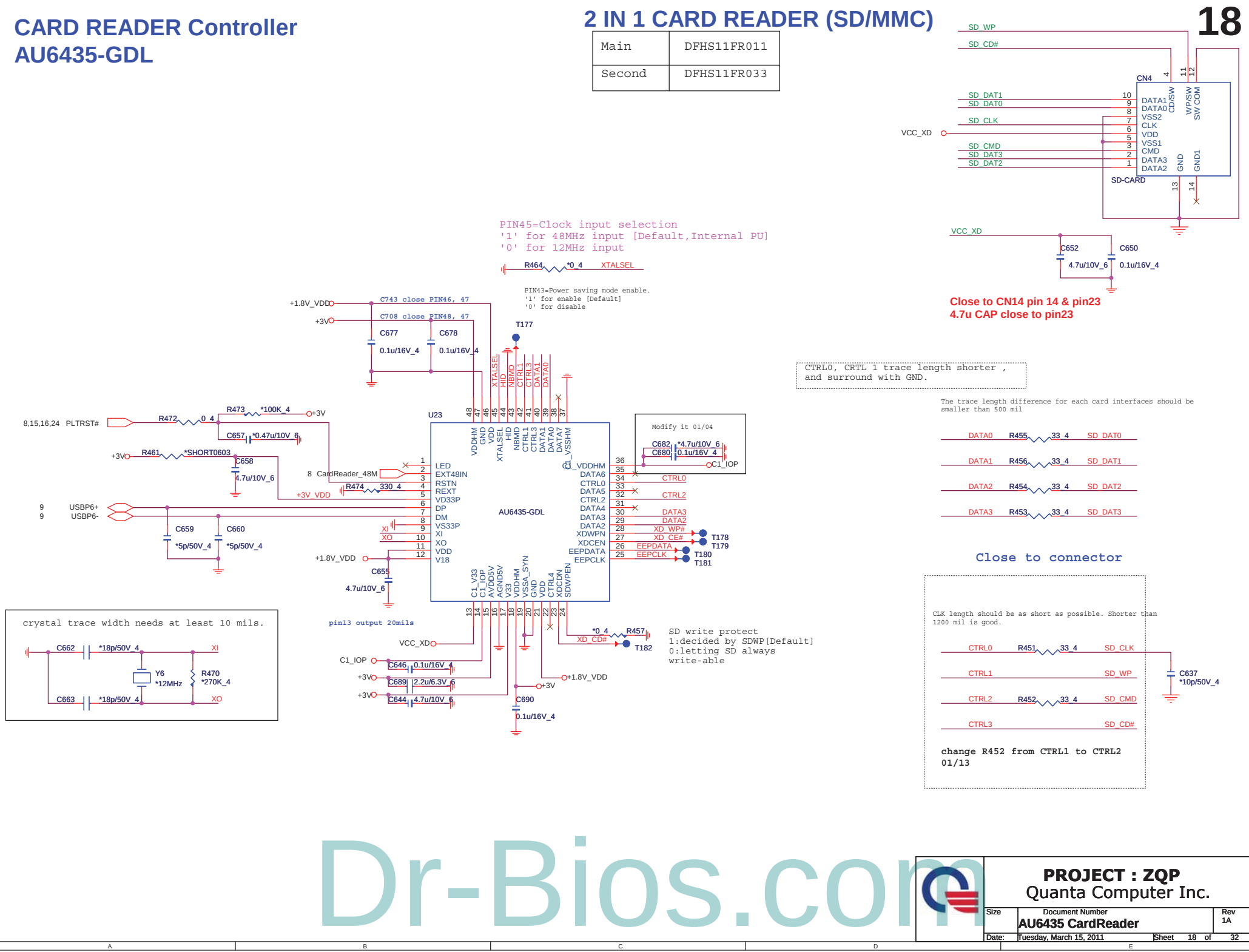
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
Date: Tuesday, March 15, 2011	Sheet 17 of 32	

CARD READER Controller
AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

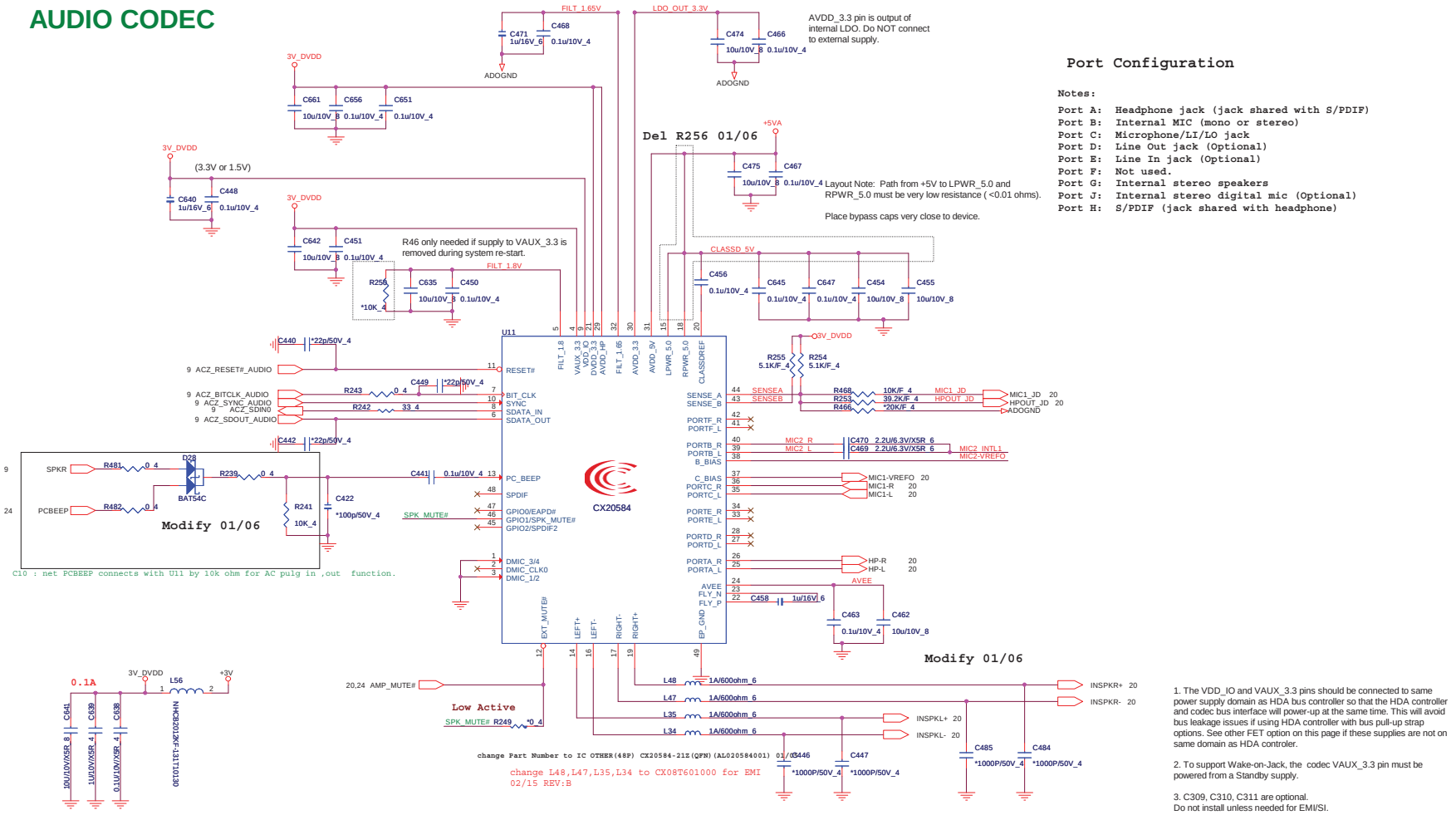
Main	DFHS11FR011
Second	DFHS11FR033



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AU6435 CardReader	1A
Date: Tuesday, March 15, 2011	Sheet 18 of 32	

AUDIO CODEC



Port Configuration

Notes:

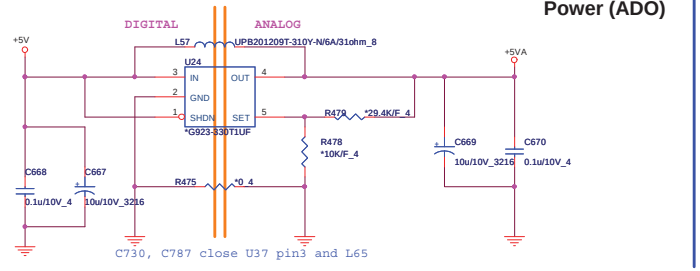
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

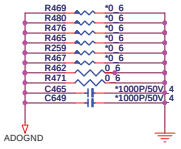
1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controler.

2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.

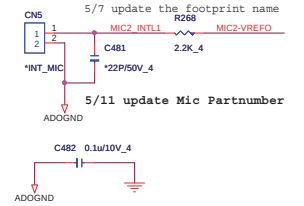
3. C309, C310, C311 are optional.
Do not install unless needed for EMI/SI.

Power (ADO)





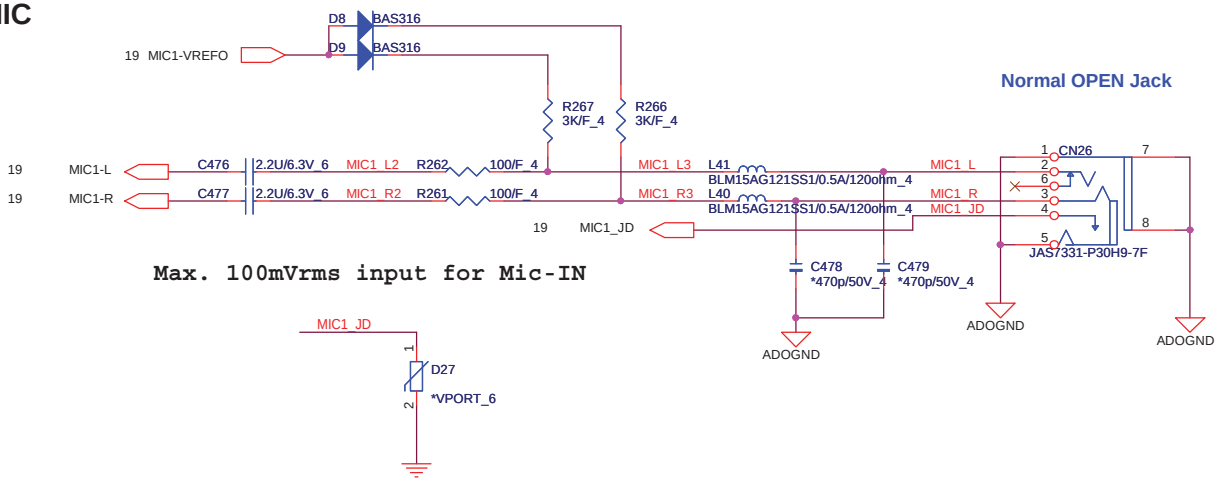
INT MIC array



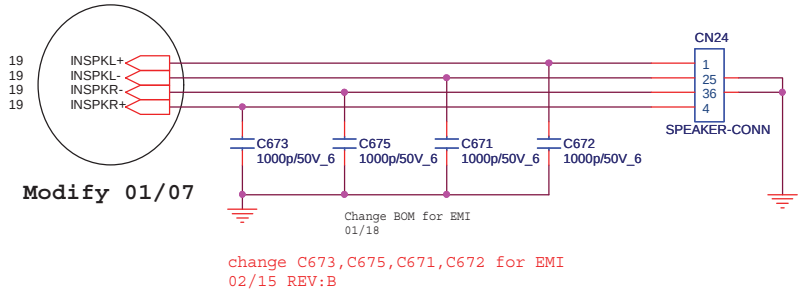
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	CONEXANT 20584	1A
Date: Tuesday, March 15, 2011	Sheet 19 of 32	

MIC

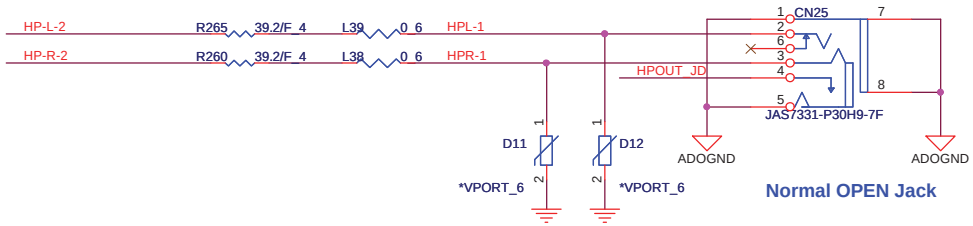


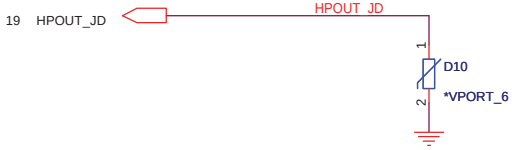
Internal Speaker

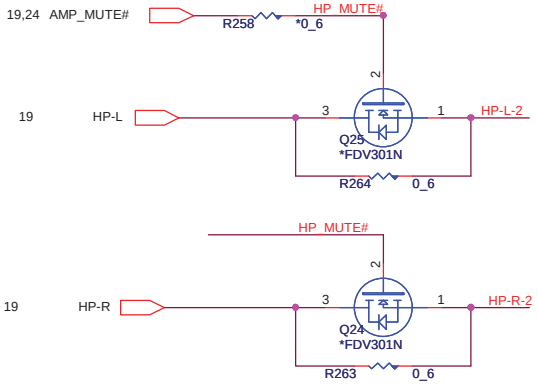


change C673,C675,C671,C672 for EMI
02/15 REV:B

HP



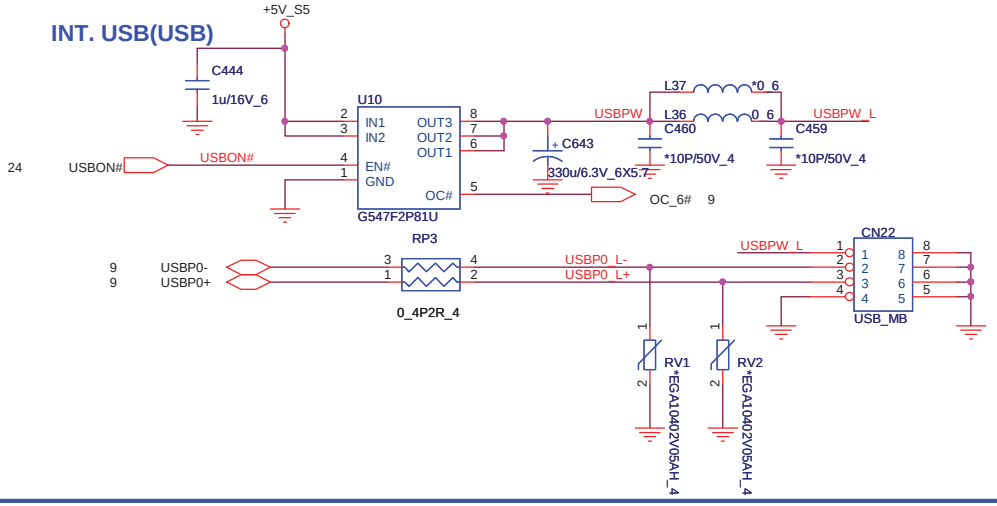




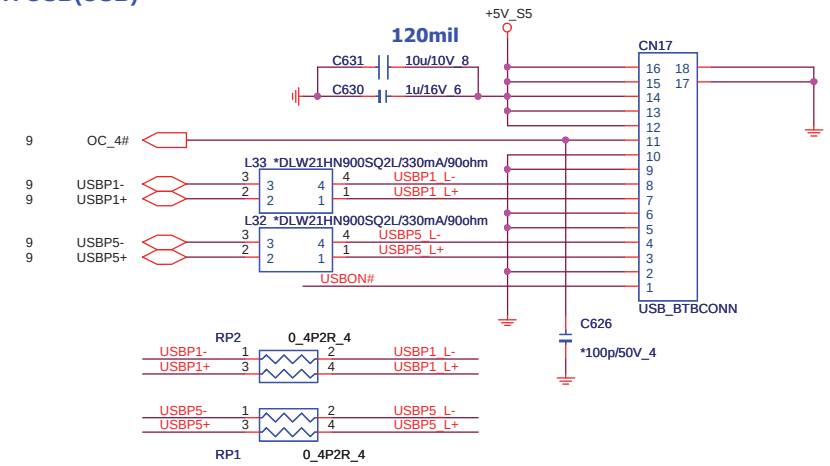
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO JACK CONN	1A
Date: Tuesday, March 15, 2011	Sheet 20 of 32	

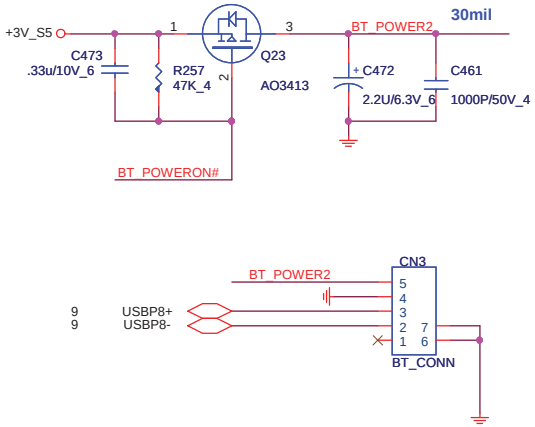
INT. USB(USB)



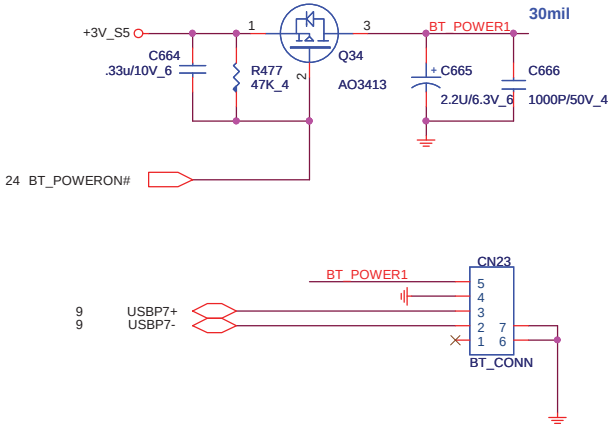
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



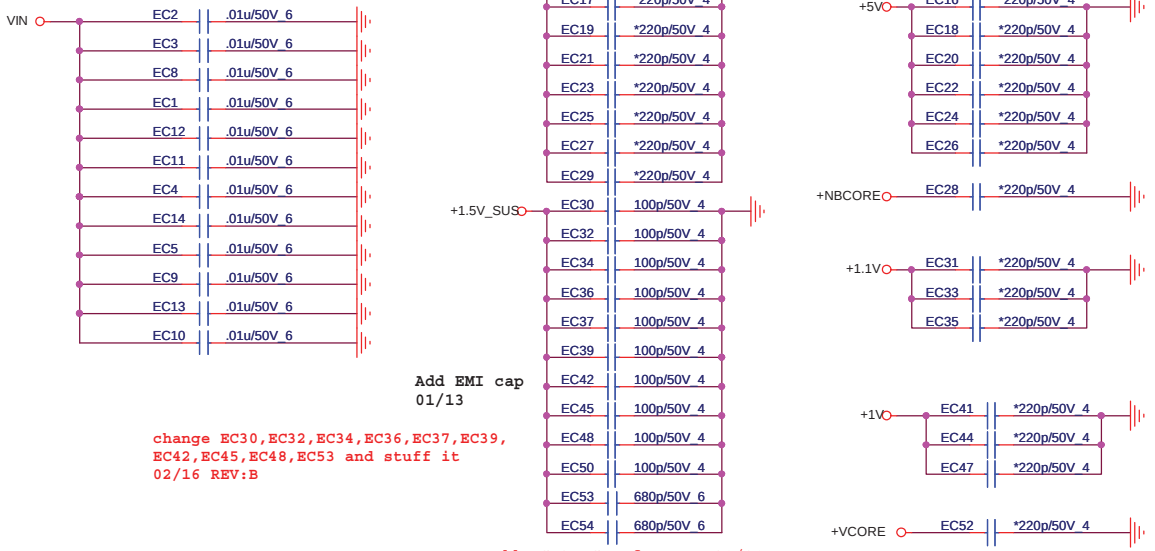
BLUETOOTH V3.0 CONN(BTM)



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT	1A
Date: Tuesday, March 15, 2011	Sheet 21 of 32	

EE RETURN-PATH CAPACITORS(EMC)



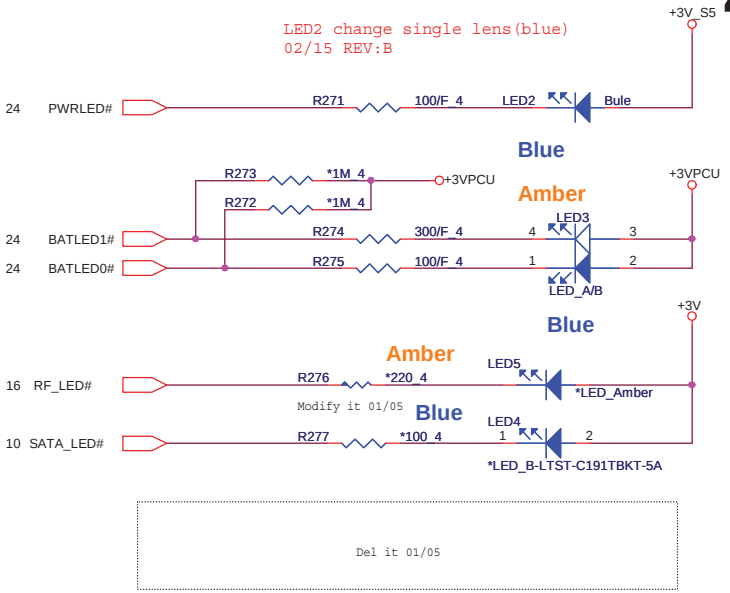
Add EMI cap
01/13

change EC30,EC32,EC34,EC36,EC37,EC39,
EC42,EC45,EC48,EC53 and stuff it
02/16 REV:B

Add EC53,EC54 for EMI 01/21
REV:B

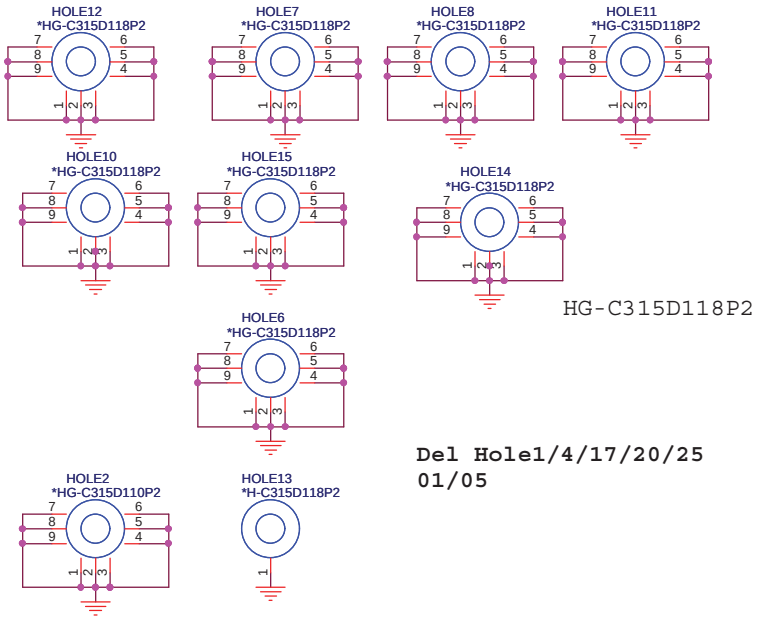
LED(UIF)

LED2 change single lens(blue)
02/15 REV:B



Del it 01/05

HOLE(OTH)

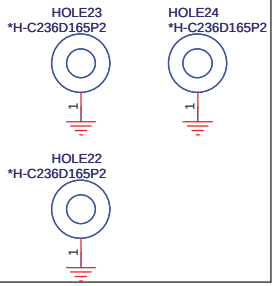


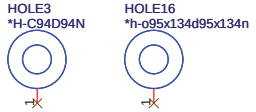
HG-C315D118P2

Del Hole1/4/17/20/25
01/05

mini PCI

cpu





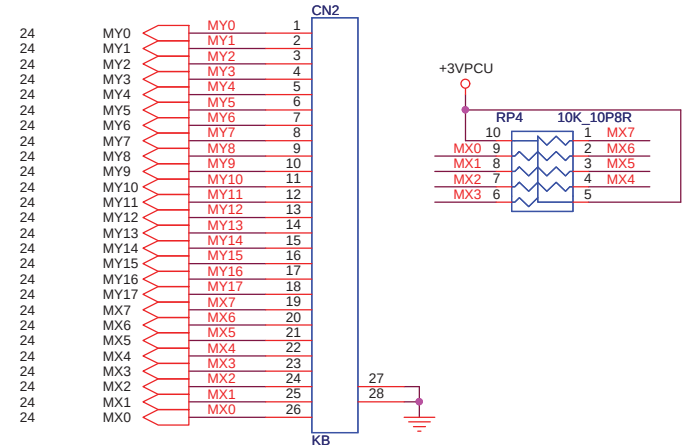
No stuff HOLE9
REV:B 02/17

CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

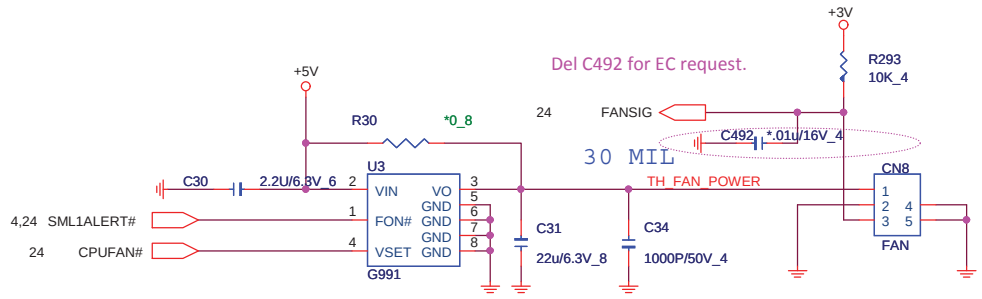
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	LED/ EMI/ Screw Hole& Nut	1A
Date: Tuesday, March 15, 2011	Sheet 22 of 32	

K/B(KBC)

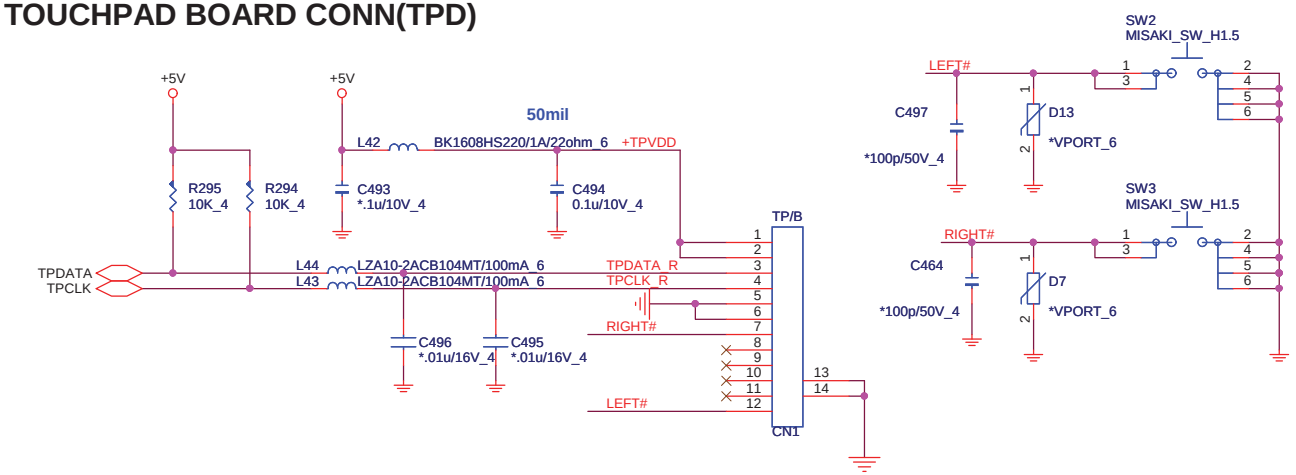


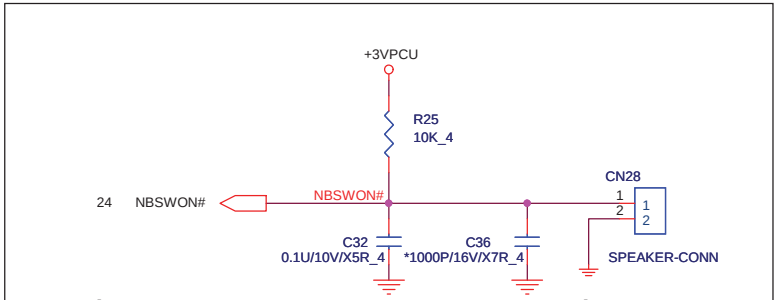
CPU FAN(THM)



change footpirnt as SA6
4/23

TOUCHPAD BOARD CONN(TPD)



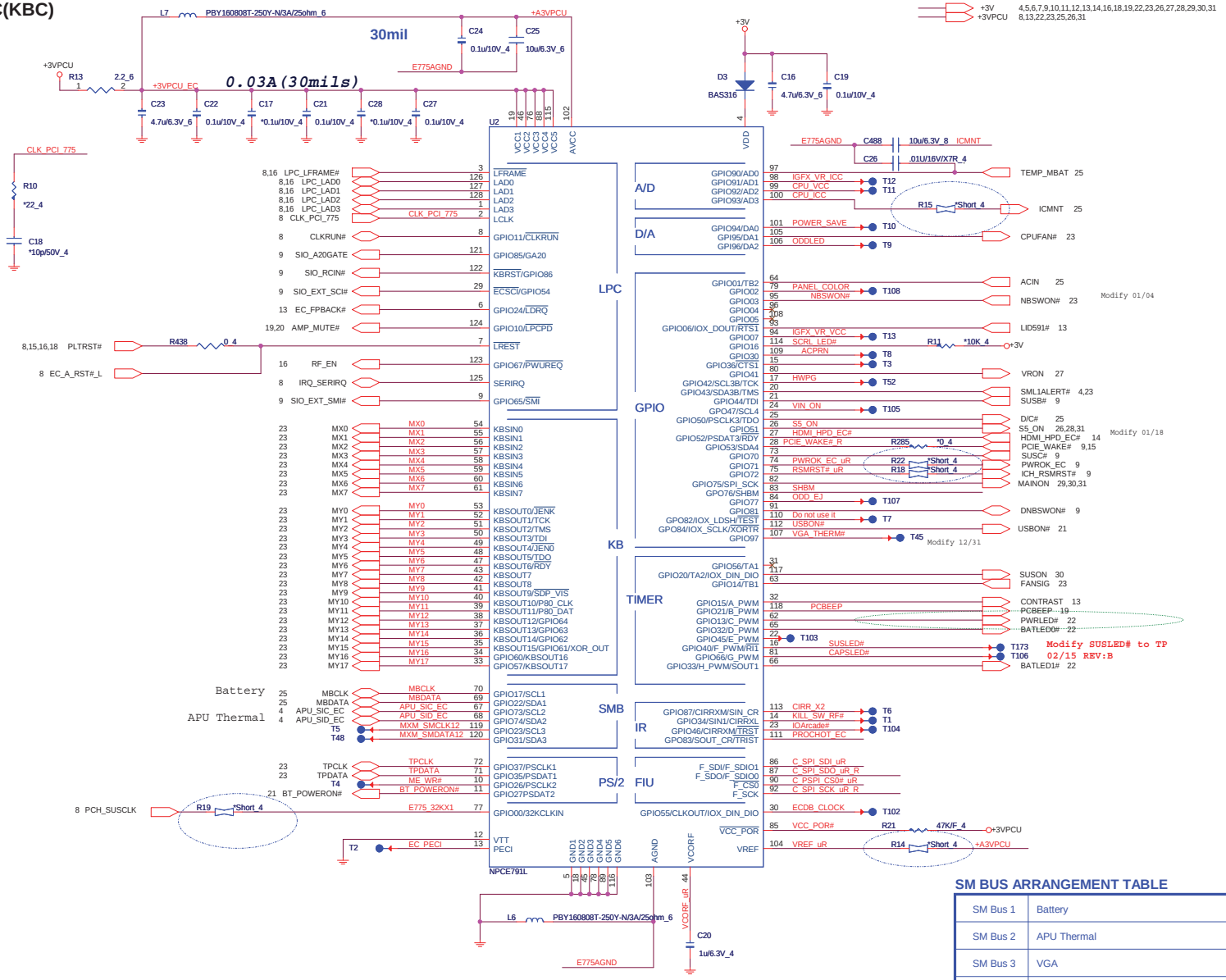


change P-SW connector as ZQ5 speark connector
01/10

DFFC12FR234 will be EOL by PDC , so change PN to DFFC12FR026

	PROJECT : ZQP Quanta Computer Inc.	
Size	Document Number **KB/TP/FAN**	Rev 1A
Date: Tuesday, March 15, 2011	Sheet 23 of 32	

EC(KBC)

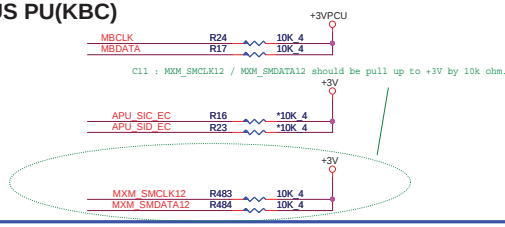


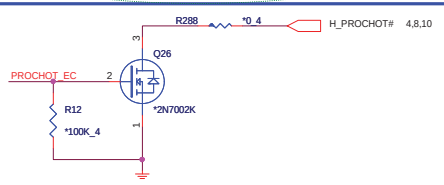
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

I/O ADDRESS SETTING(KBC)

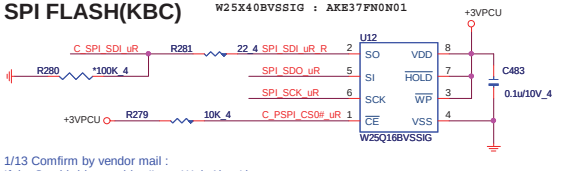
SM BUS PU(KBC)





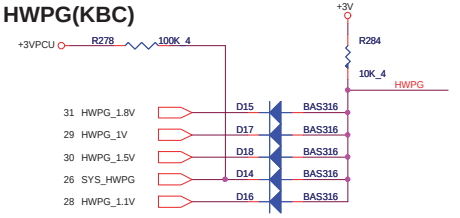
SPI FLASH(KBC)

socket : DG008000031
W25X40BVSSIG : AKE37FN0N01

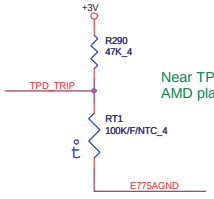


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



PALM REST THERMAL SENSOR (THM)



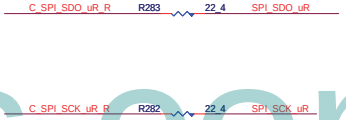
Near TP on TOP side and only for
AMD platform Palm Rest use.

(02/25)
Per QSMC SMT request, change to Mitsubishi.
Main: CU4100B0000
Second: CU410000Z07 (MIT)

POWER-ON SWITCH (KBC)

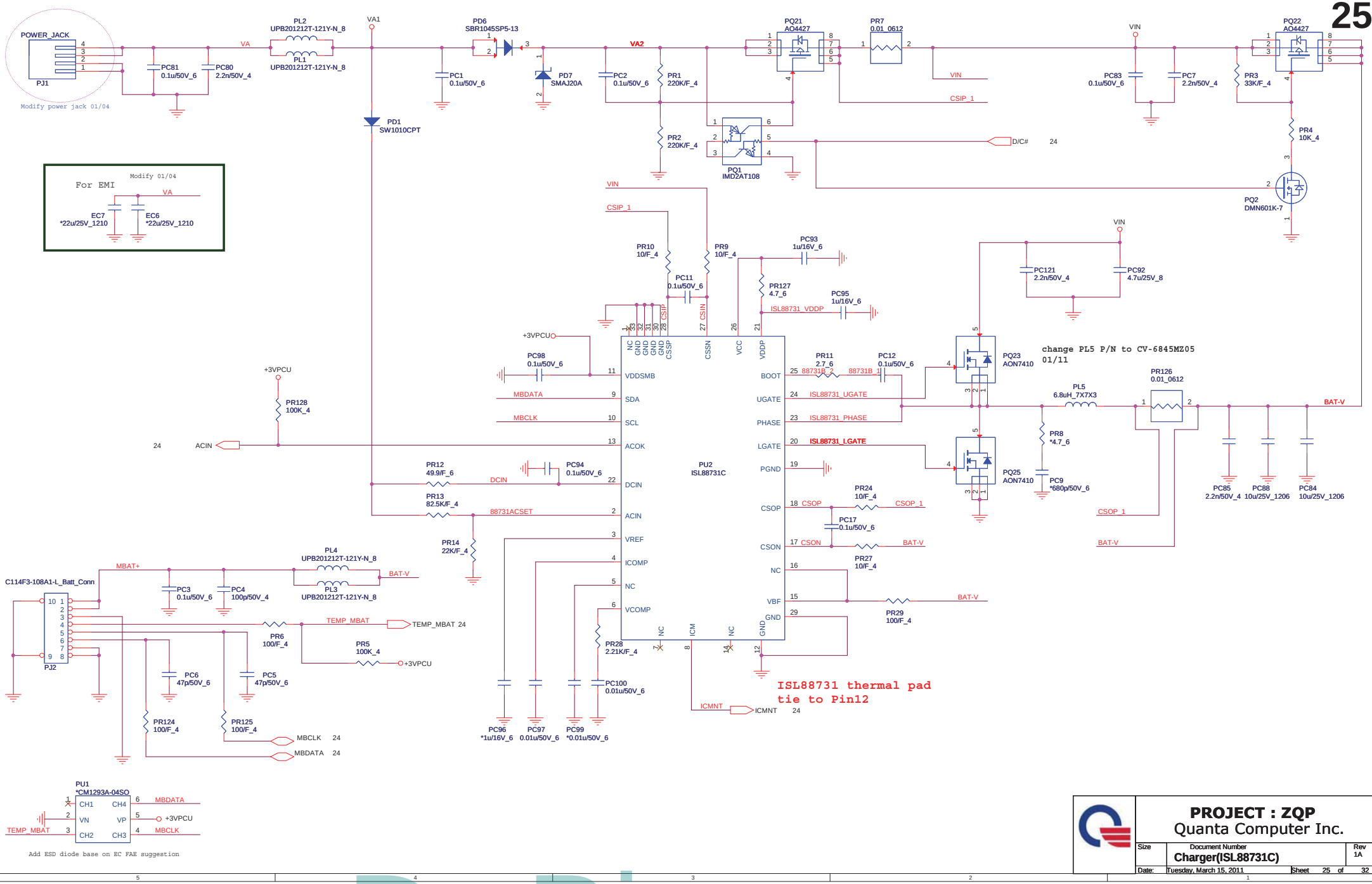
Del SW1,stuff D1
02/15 REV:B

Add D5 for ESD
02/15 REV:B



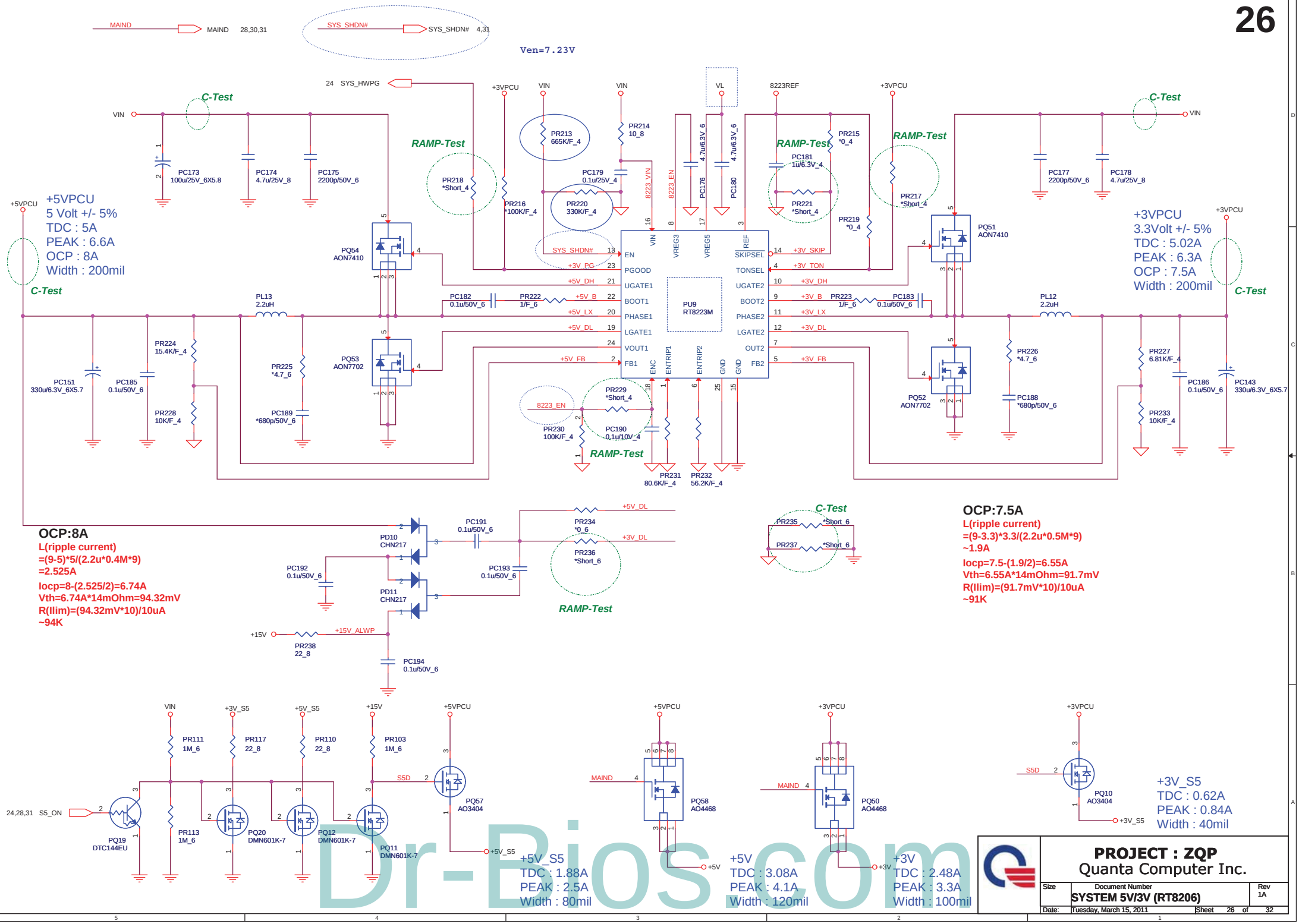
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE791 & FLASH	1A
Date: Tuesday, March 15, 2011	Sheet 24 of 32	

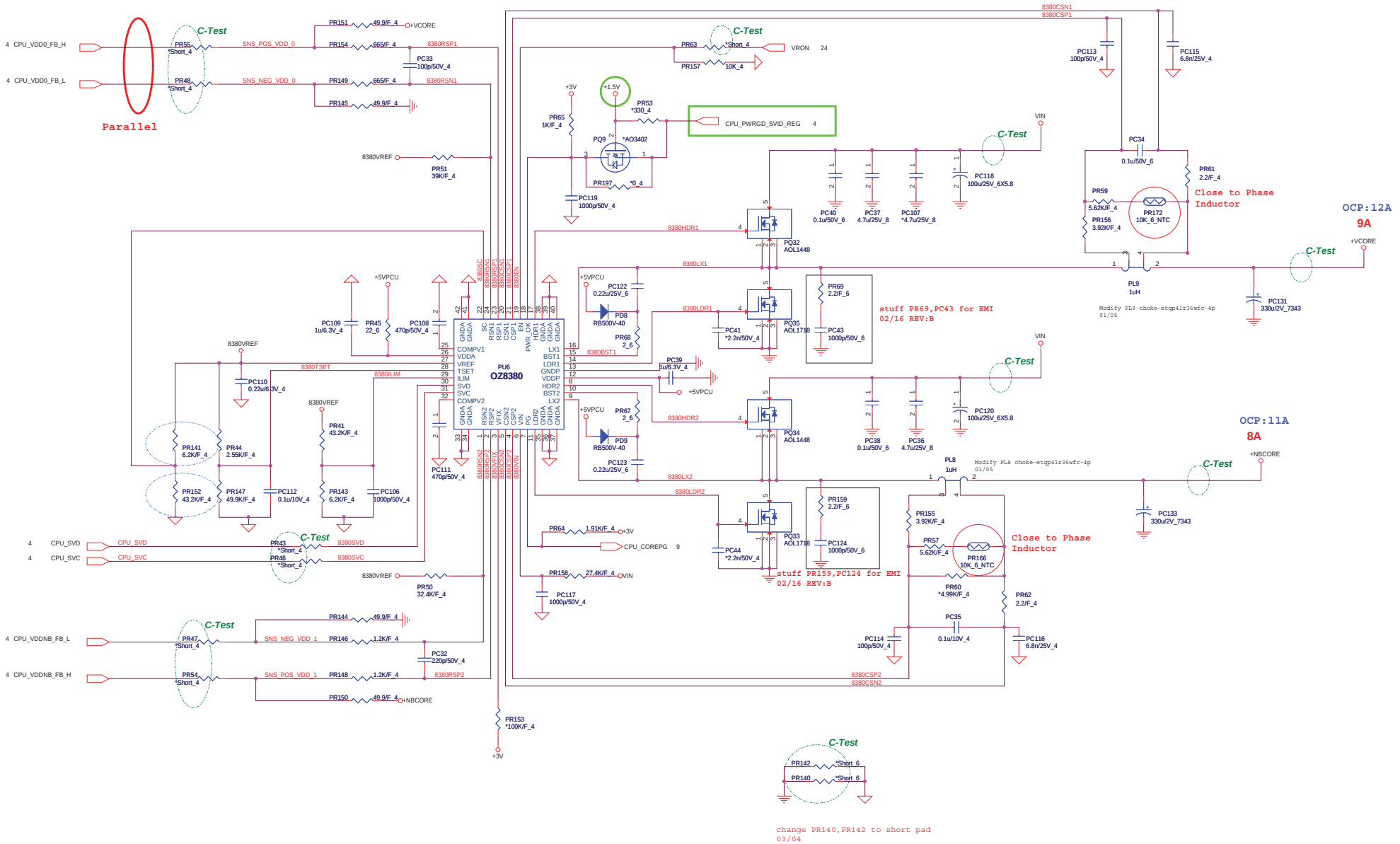


PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Charger(ISL88731C)	1A
Date: Tuesday, March 15, 2011	Sheet 25 of 32	

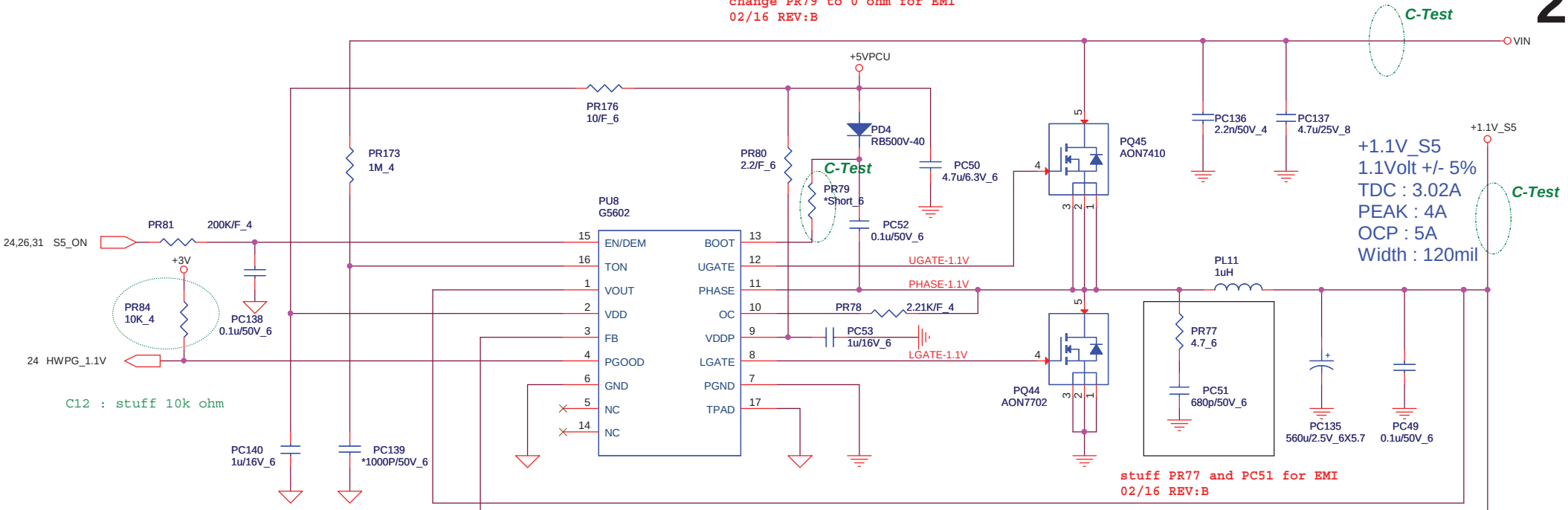


PROJECT : ZQP		
Quanta Computer Inc.		
Size	Document Number: SYSTEM 5V/3V (RT8206)	Rev 1A
Date: Tuesday, March 15, 2011	Sheet 26 of 32	



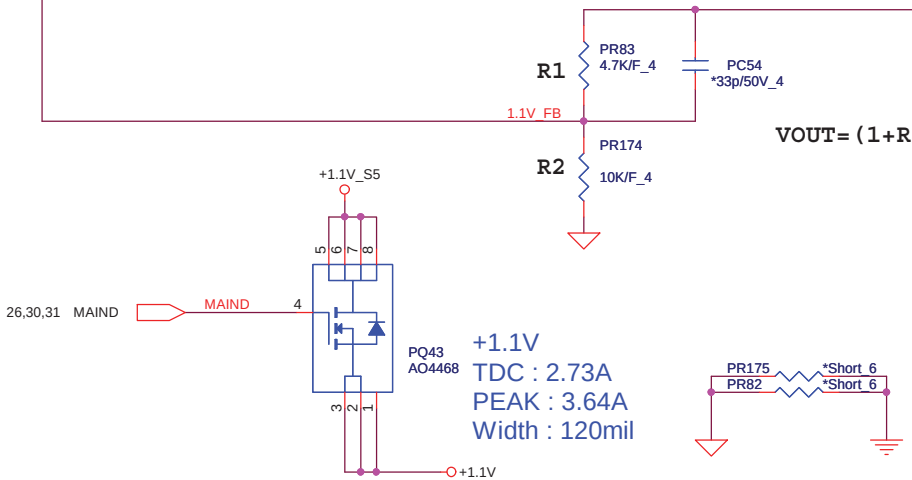
PROJECT : ZQP Quanta Computer Inc.			
Size	Document Number CPU Core (OZ8380)		Rev 1A
Date: Tuesday, March 15, 2011		Sheet 27 of 32	

change PR79 to 0 ohm for EMI
02/16 REV:B



TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
Rth = 14mohm*(5-1.905)/20uA
=2.166K



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date: Tuesday, March 15, 2011	Sheet 28 of 32	

change PR76 to 0 ohm for EMI
02/16 REV:B

C13

change PR169 PN from 0ohm to 430kohm for timing issue

C14 : stuff 10k ohm

C-Test

+1V
1Volt +/- 5%
TDC : 4.3A
PEAK : 5.7A
OCP : 7A
Width : 180mil

stuff PR164,PC126 for EMI
02/16 REV:B

VOUT=(1+R1/R2)*0.75

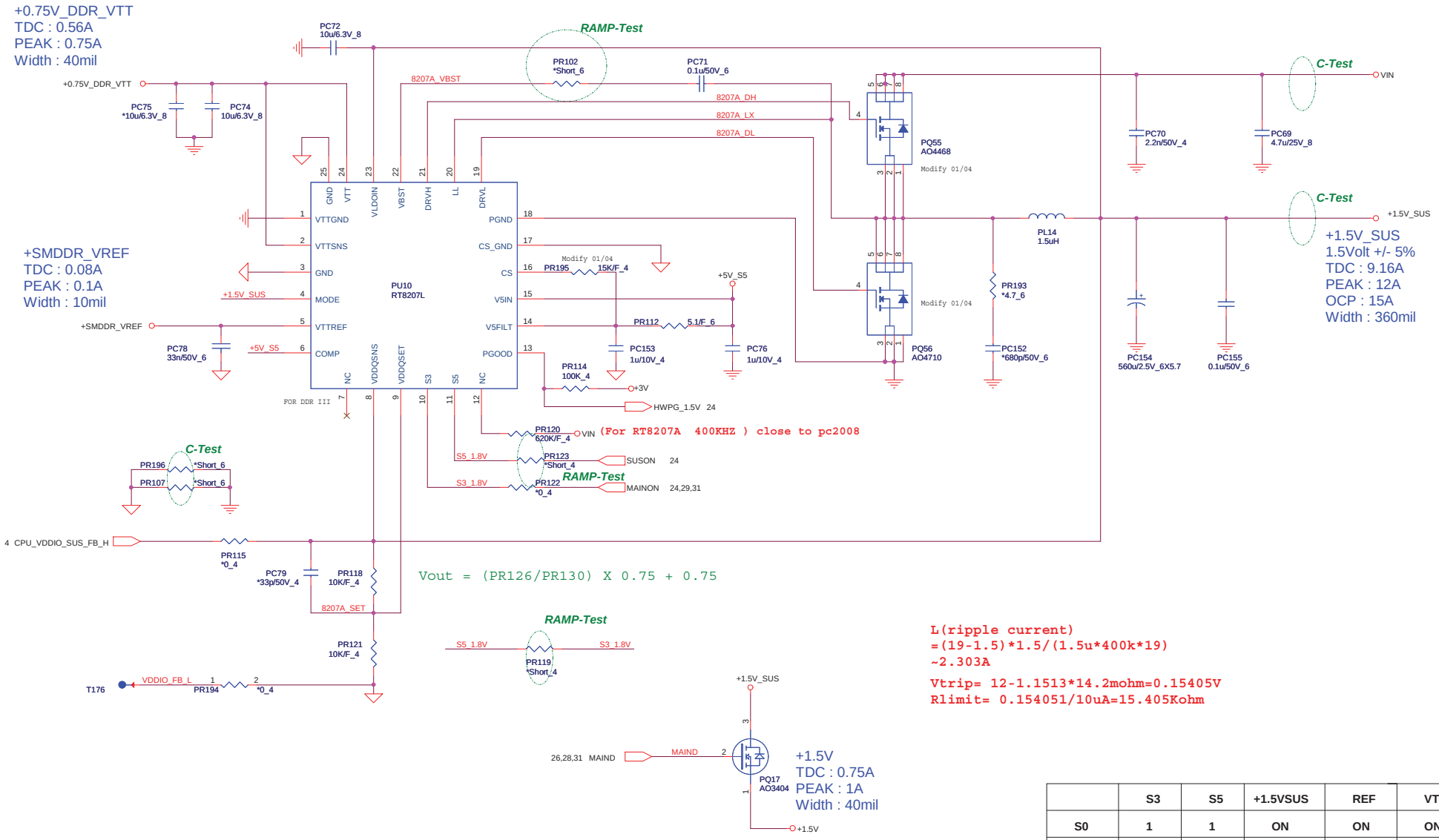
C15 : change PR75 value from 3.57k to 3.65k
PR75-->4.02K for
1333MHz,1.05V

TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1)*1/(1u*272k*19)
~3.483A
Rth=14mohm*(10-1.741)/20uA
=3.68Kohm

PROJECT : ZQP
Quanta Computer Inc.

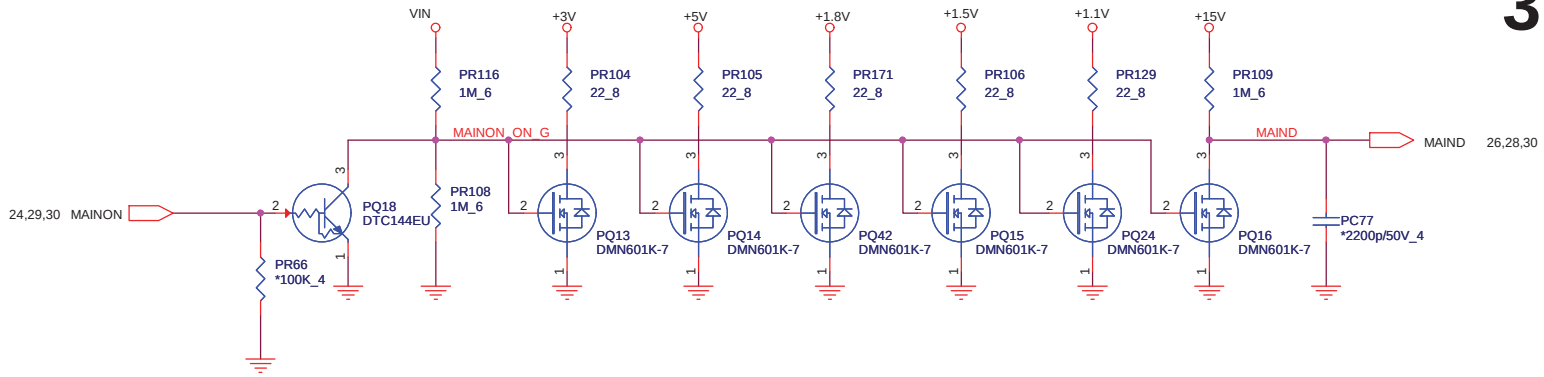
Size	Document Number	Rev
	+1V(G5602)	1A
Date: Tuesday, March 15, 2011	Sheet 29 of 32	



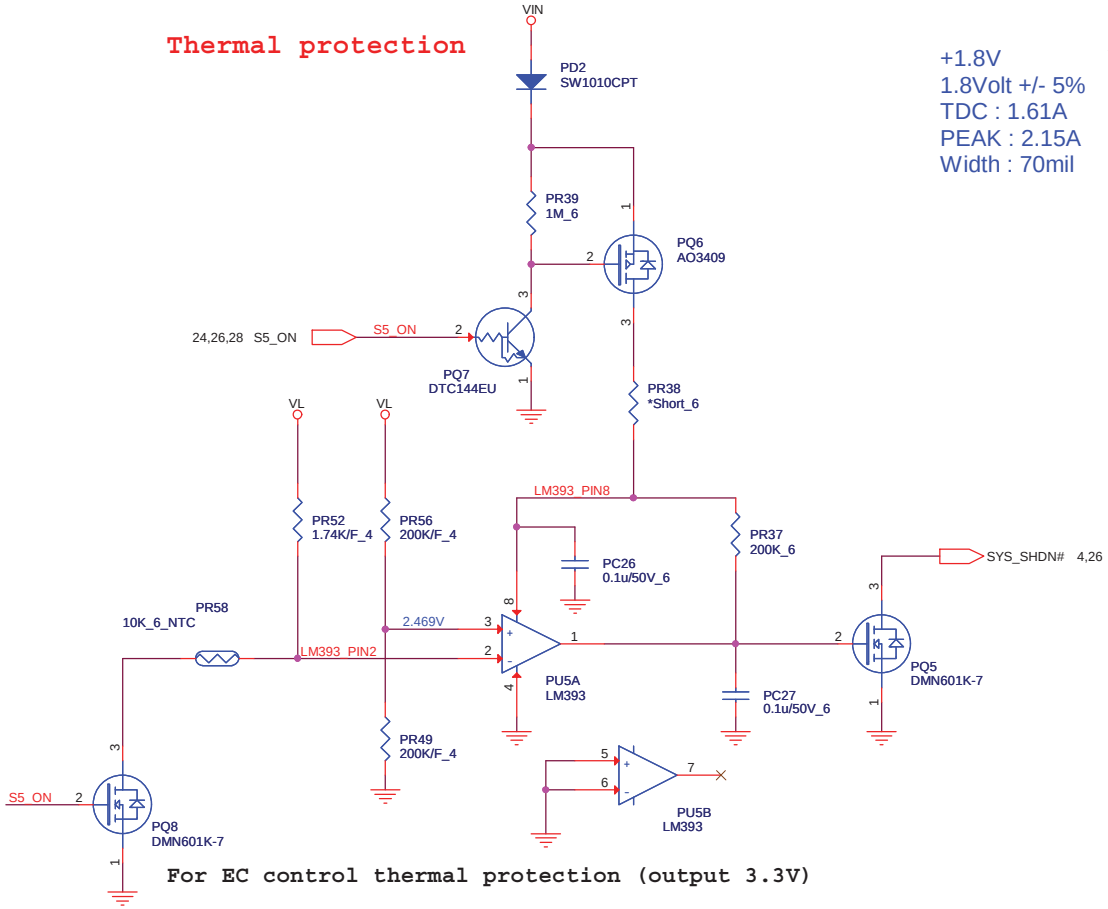
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Tuesday, March 15, 2011	Sheet 30 of 32	

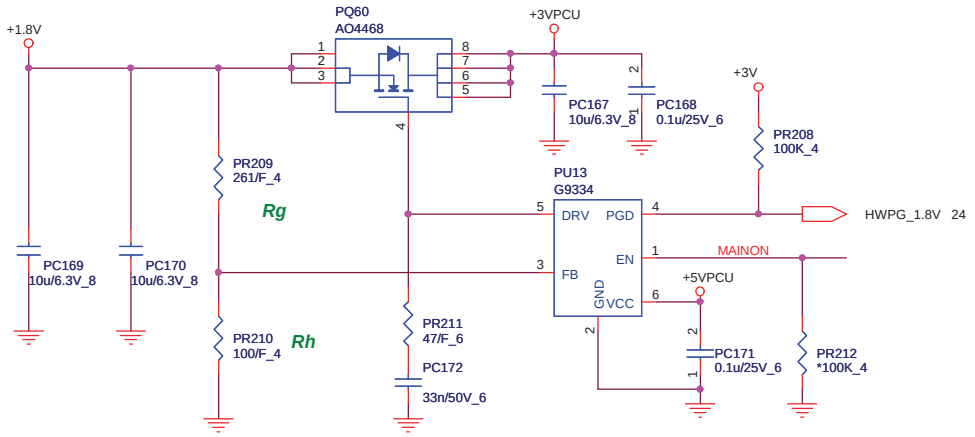


Thermal protection



For EC control thermal protection (output 3.3V)

+1.8V
1.8Volt +/- 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



*Vout1 = (1+Rg/Rh)*0.5*

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge /Thermal protection	1A
Date: Tuesday, March 15, 2011	Sheet 31 of 32	

MODEL	REV	CHANGE LIST
ZQP/Q M/B	A	First Release
	B	01.P14: Add HDMI function 02.P22: Add EC53,EC54 for EMI 03.P20: Stuff C673/C675/C671/C672 for EMI 04.P15: Stuff ESD protector at R31/R32 for EMI 05.P10: GPIO 58 define to HDMI strap pin 06.P08: Add C606,C614,C619 for strong clock 07.P20:change C673,C675,C671,C672 for EMI 08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI 09.P24:No stuff SW1,stuff D1 10.P24:Add D5 on S5_ON for ESD 11.P22:LED2 change single lens(blue) 12.P08:Del C623 13.P24:Del SW1 14.P13:Del R26,R27 and add RP5 for EMI 15.P15:Add EC38,EC40,EC43,EC46 for EMI 16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI 17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI 18.P27:stuff PR69,PC43 for EMI 19.P17:change C617,C612,C539,C540 footprint form 1206 to 0805 20.P13:Swap USB nets between L50 and PR5 21.P13:Add R33,R34 for ESD 22.P15:change C354 to CH122GK1I10 for EMI 23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI 24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237 25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140 26.P28:Remove JP24,JP25 27.P29:Remove JP16,JP17 and change to short pad PR70,PR72 28.P30:Remove JP18,JP19 and change to short pad PR196,PR107 29.P22:No stuff HOLE9
	C	01.P15:change RJ45 connector without LED 02.P27:change PR140,PR142 to short pad 03.P30:change PR119,PR123,PR102 to short pad 04.P26:change PR217,PR218,PR221,PR229,PR236 to short pad 05.P29:change PR76 to short pad 06.P28:change PR79 to short pad

Model	ZQE/G M/B BOARD	
Page	From	To
1	1A	3A
2	1A	3A
3	1A	3A
4	1A	3A
5	1A	3A
6	1A	3A
7	1A	3A
8	1A	3A
9	1A	3A
10	1A	3A
11	1A	3A
12	1A	3A
13	1A	3A
14	1A	3A
15	1A	3A
16	1A	3A
17	1A	3A
18	1A	3A
19	1A	3A
20	1A	3A
21	1A	3A
22	1A	3A
23	1A	3A
24	1A	3A
25	1A	3A
26	1A	3A
27	1A	3A
28	1A	3A
29	1A	3A
30	1A	3A
31	1A	3A
32	1A	3A
33	1A	3A
34	1A	3A
35	1A	3A
36	1A	3A
37	1A	3A
38	1A	3A
39	1A	3A
40	1A	3A
41	1A	3A

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	CHANGE LIST - 3A	1A
Date: Tuesday, March 15, 2011	Sheet 32 of 32	

Quanta Computer Inc. ZQP/Q	PROJECT: ZQP/Q	PCBA NO.	REV: 3A	DOC. NO :	
	APPROVED BY : Andy Lin	CHECK BY : JC Huang	DRAWING BY : Andy Chen	DATE :10/18/2010	SHEET 1