ZB3

CPU CORE
MAX8736
Page:31
VCC_CORE
+1.5V_RUN

+1.2V (SC1470) VCCP_+1.05V (MAX1992)
Page:32
+1.2V
VCCP_+1.05V

+1.8VSUS +0.9V_VTER (NCP5214)
Page:33
+1.8VSUS
+1.8V
+0.9V_VTER

+3VPCU/+5VPCU +3V_S5 +3V/+5V +3VSUS/+5VSUS 15V
MAX1999
Page:34
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5VSUS
+5V
15V

BATTERY CHARGER
MAX8724
Page:35
BATTERY

Power State Table

Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
VCCP_+1.05V	MAINON	S0
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0-S5
+3VSUS	SUSD	S0-S3
+3V	MAIND	S0
+5VPCU	N/A	ALWAYS
+5VSUS	SUSD	S0-S3
+5V	MAIND	S0
15V	N/A	S0
+1.2V	MAINON	S0
VGA_CORE	VGA_MAINON	S0
+2.5V	MAINON (Delay 1ms)	S0
+0.9V_VTER	MAINON	S0
+1.8V_S5 +1.8VSUS +1.8V	S5_ON SUSON MAIND	S0-S5 S0-S3 S0
+1.5V_RUN	MAINON	S0

X'TAL 14.31818MHz
Clock generator
ICS951413CGLFT
Page:5

Yonah/Yonah Celeron-M
INTEL Mobile_479 CPU SOCKET_M
Page:3, 4
HOST BUS 533/667MHZ

VGA option
+1.0V/+1.2V VGA Power
MAX1993
Page:30
VGA_CORE
VGA Memory 128MB/256MB (Channel-B)
Page:19

NB
ATi RC410ME
533MHz/667MHz
707-Pins FCBGA Package
Page: 6 , 7, 8, 9
PCI-E 16X
UMA(option)

VGA
ATi M52-P(M54-P)
Page: 15, 16, 17, 18, 19
RGB
LVDS

CRT Page: 20
LVDS Page: 20

DDR-II SODIMM1 Page: 10
DDR-II SODIMM2 Page: 10
DDR-II 533/667MHz

Manufacturing Option
SATA HDD Page: 21
PATA HDD Page: 21
IDE-ODD Page: 21
SATA
ATA 66/100

SB
ATi SB460
549-Pins BGA Package
Page: 11, 12, 13, 14
2X PCIE
X'TAL 32.768KHz
LPC 33MHZ
Azalia
PCI BUS 33MHZ
USB 2.0

RTC Page: 11

MINI-Card Wireless LAN Page: 22
2X PCIE
USB7

MARVEL 88E8038
64QFN-Pins Package
Page: 23
2X PCIE

BOTHHAND TRANSFORMER NS0013 Page: 23
RJ45 Page: 23

TI PCI7412 Cardbus controller
AD17
REQ3# / GNT3#
INTE#, INTH#,
INTG#(share)
Page: 24,25

PCMCIA SLOT Page: 24
5 IN1 CARD READER Page: 25

MINI-PCI Wireless LAN
AD20
REQ2# / GNT2#
INTF#,
INTG#(share)
Page: 22

Bluetooth USB interface Page:22
USB6

SYSTEM USB PORT*3 Page: 22
USB0,2,4

AUDIO CODEC
REALTEK- ALC883
48-pins Package
Page: 26
MIC-IN Page: 26
LINE-IN Page: 26

Audio AMP
MAX9755
Page: 27
SPEAKER Page: 27

MODEM Page: 26
RJ11 Page: 23

KBC
NS PC97551
176-Pins Package
Page: 28
BIOS Page: 28
Touchpad Page: 26
Keyboard Page: 29
Audio DJ Page: 27
FAN Page: 29

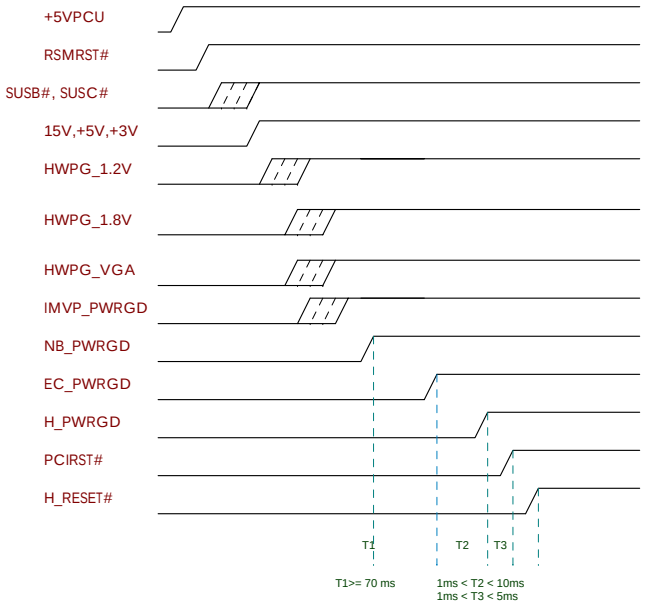
PROJECT : ZB3
Quanta Computer Inc.
Size | Document Number: BLOCK DIAGRAM | Rev: 1A
Date: Monday, April 03, 2006 | Sheet 1 of 37

TABLE OF CONTENTS

Page 01 : BLOCK DIAGRAM
Page 02 : TABLE OF CONTENTS
Page 03 : Yanah CPU(HOST Bus)-1
Page 04 : Yanah CPU(POWER/NC)-2
Page 05 : CLOCK GENERATOR
Page 06 : RC410ME-MEMORY_AGTL+ I/F
Page 07 : RC410ME-PCIE LINK EXTERNAL VGA
Page 08 : RC410ME-LVDS OUT & CLKGEN
Page 09 : RC410ME-POWER
Page 10 : DDR2 SO-DIMM X2 & TERMINA
Page 11 : SB460M-PCIE/PCI/CPU/LPC
Page 12 : SB460M ACPI/GPIO/USB/AC97
Page 13 : SB460M HDD/POWER/DECOUPLI
Page 14 : SB460M STRAPS
Page 15 : M52-P_MAIN_PCIE (1 of 4)
Page 16 : M52-P_MEM_GND (2 of 4)
Page 17 : M52-P_Power_LVDS(3 of 4)
Page 18 : M52-P_Straps (4 of 4)
Page 19 : VGA RAM (64BIT DDR2)
Page 20 : CRT & LVDS
Page 21 : HDD & CDROM ,HOLES
Page 22 : MINI PCI, USB Bluetooth PORT
Page 23 : LAN PCI-E EE88038
Page 24 : PCI7412-PCMCIA CONTROLLE
Page 25 : PCI7412-CARD READER
Page 26 : CODEC T/P MIC/LINE-IN/OUT-ALC883
Page 27 : AUDIO AMP&LINE OUT
Page 28 : PC97551 & FLASH
Page 29 : FAN,SWITCH,LED,KB
Page 30 : VGA CORE 1.0V/1.2V
Page 31 : CPU CORE-MAX8736ETL+
Page 32 : +VCCP(1.05V)& 1.2V(NB PWR
Page 33 : DDRII PWR_1.8VSUS-VTERM
Page 34 : SYSTEM +5V& +3V MAX1999A
Page 35 : BATTERY CHARGER

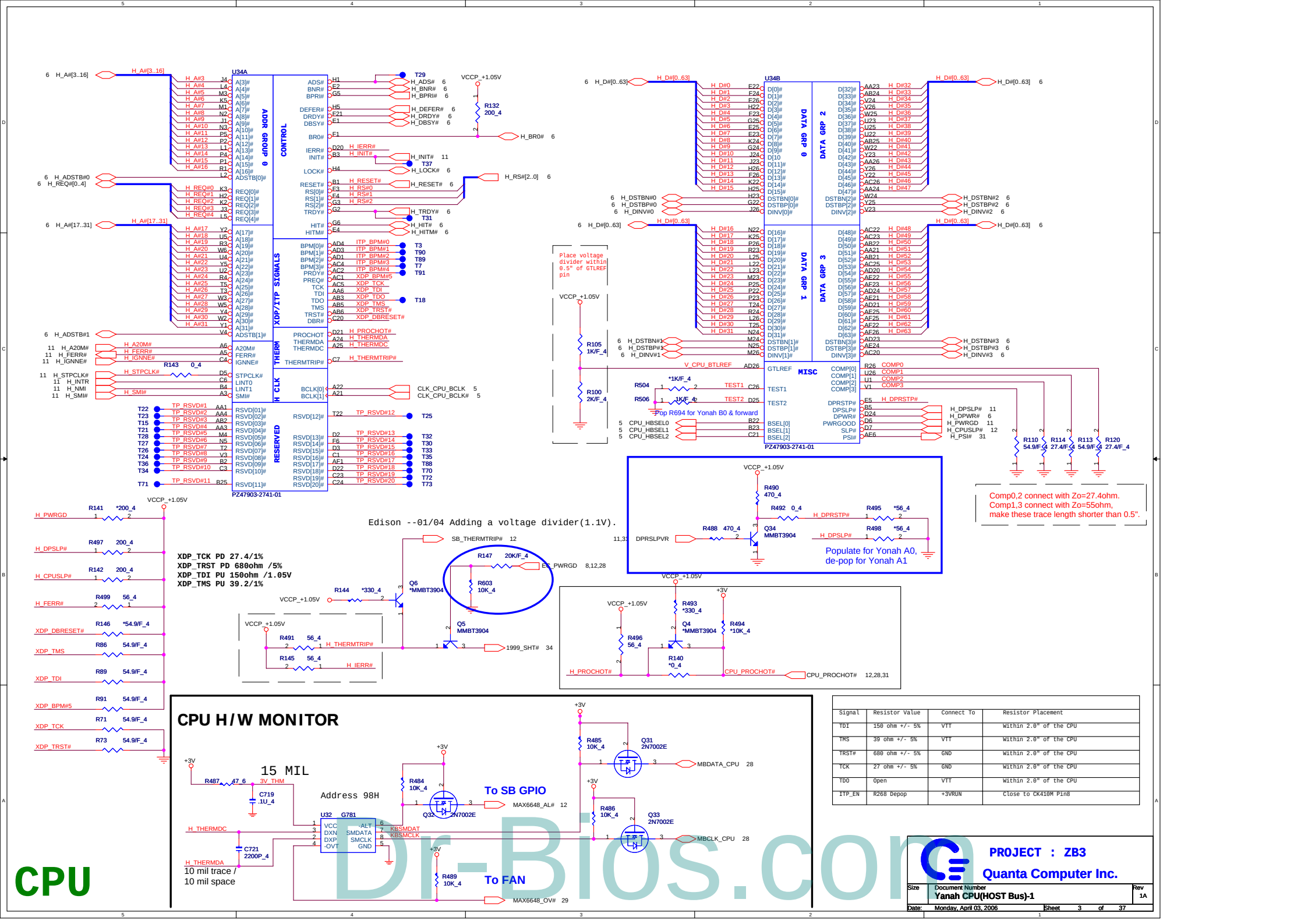
	POWER	VOLTAGE	ACTIVE SCOPE	PAGE
SYSTEM	15V	15V	S0	33
	+5V	+5V	S0	33
	+3V	+3.3V	S0	33
	+5VPCU	+5V	ALWAYS	33
	+3VPCU	+3.3V	ALWAYS	33
	+5VSUS	+5V	S0-S3	33
	+3VSUS	+3.3V	S0-S3	33
	+3V_S5	+3.3V	S0-S5	33
CPU	VCC_CORE	VID[0..6]	S0	31
	VCCP_+1.05V	+1.05V	S0	31
	+1.5V_RUN	+1.5V	S0	31
RC410ME NB	VCCP_+1.05V	+1.05V	S0	31
	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	33
	+1.2V	+1.2V	S0	32
	+3V	+3.3V	S0	33
	+1.2V_PCIE	+1.2V	S0	9
	+1.2V_CORE	+1.2V	S0	9
	VDD18	+1.8V	S0	9
	VDDA18	+1.8V	S0	9
	NB_VDDR	+3.3V	S0	8
	AVDD_NB	+3.3V	S0	8
	AVDDQ	+1.8V	S0	8
	PLVDD	+1.8V	S0	8
	NB_LPVDD	+1.8V	S0	8
	NB_LVDDR18A	+1.8V	S0	8
SB460 SB	+3V	+3.3V	S0	33
	+1.8V	+1.8V	S0	33
	+3V_S5	+3.3V	S0-S5	33
	+1.8V_S5	+1.8V	S0-S5	30
	VCCP_+1.05V	+1.05V	S0	31
	+1.8VUSB_PHY	+1.8V	S0-S5	13
	V5_REF	+5V	S0	13
	+1.8V_ATA	+1.8V	Reserve	13
	PLLVDD_ATA	+1.8V	Reserve	13
	XTLVDD_ATA	+1.8V	Reserve	13
	PCIE_PVDD	+1.8V	S0	11
	PCIE_VDDR	+1.8V	S0	11
	AVDD_USB	+3VSUS	S0-S3	12
	+3.3V_AVDDC	+3.3V	S0-S3	12
	VCCRTC	+3.0V	--	11
	VDDQ_3V	+3.3V	S0	13
	VDD_1.8V	+1.8V	S0	13
	SB_S5_3V	+3.3V	S0-S5	13
	SB_S5_1.8V	+1.8V	S0-S5	13
	AVDD_CK_1.8V	+1.8V	S0	13
DDR2	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	10
	+0.9V_VTER	+0.9V	S0	10

POWER UP SEQUENCE



PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Monday, April 03, 2006	Sheet 2 of 37	



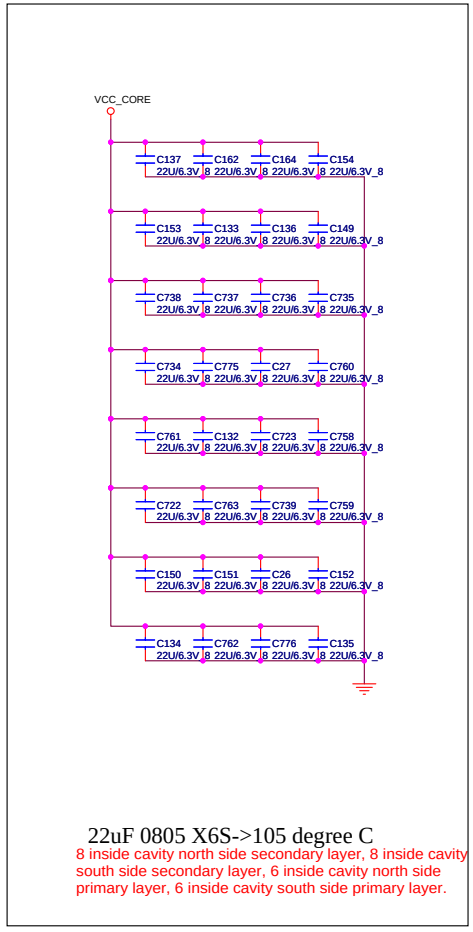
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

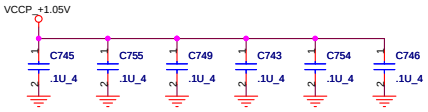
PROJECT : ZB3

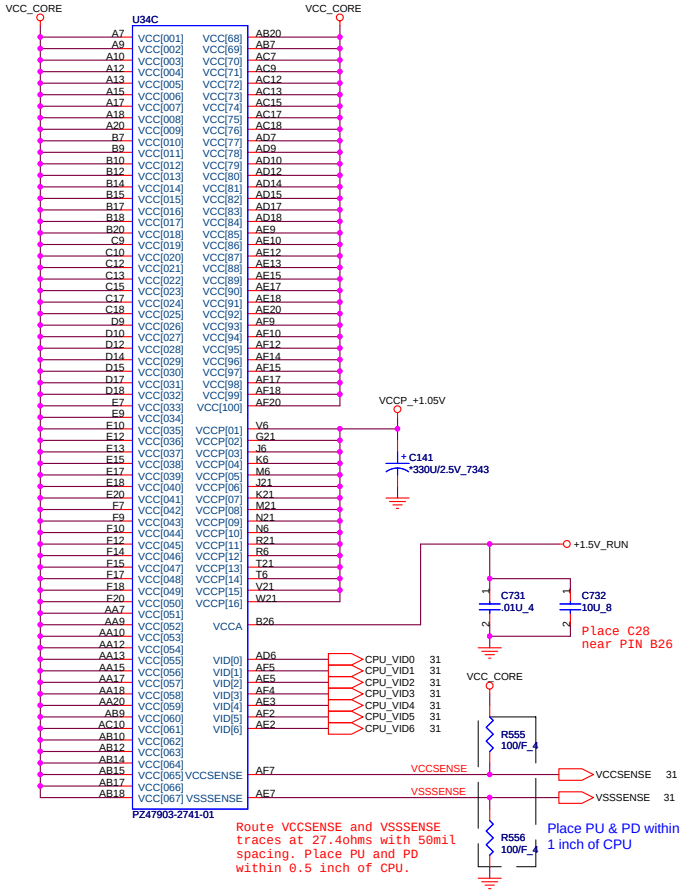
Quanta Computer Inc.

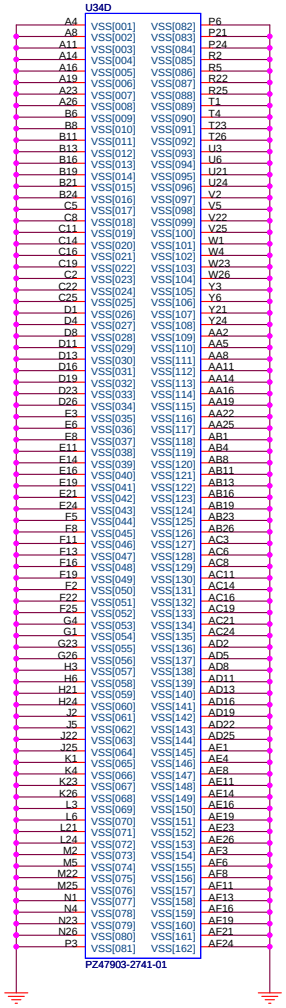
Size	Document Number	Rev
	Yanah CPU(HOST Bus)-1	1A

Date: Monday, April 03, 2006 Sheet 3 of 37



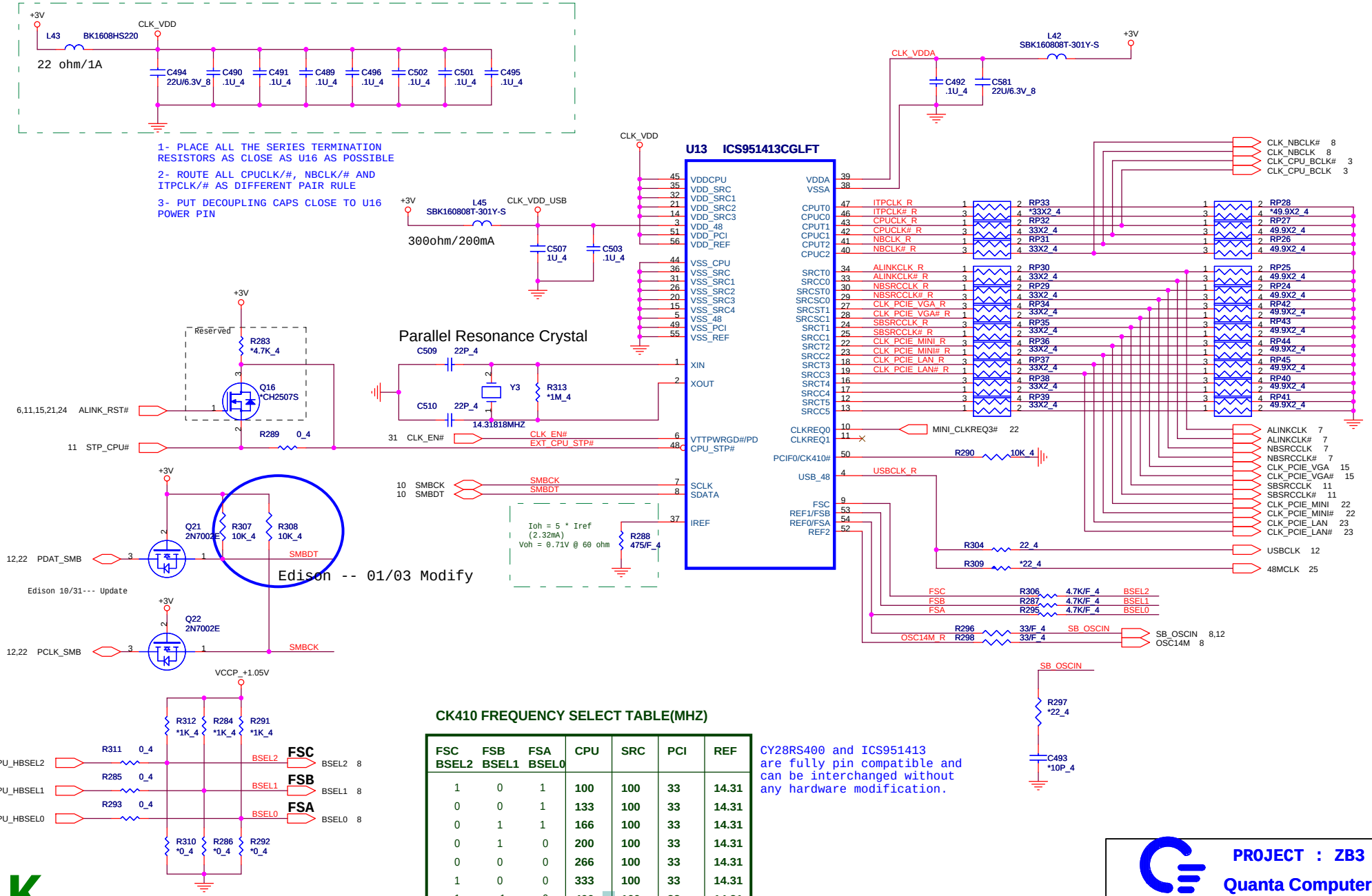






CPU

PROJECT : ZB3		
Quanta Computer Inc.		
Size	Document Number: Yanah CPU(Power/NC)-2	Rev: 1A
Date: Monday, April 03, 2006	Sheet 4 of 37	



CK410 FREQUENCY SELECT TABLE(MHZ)

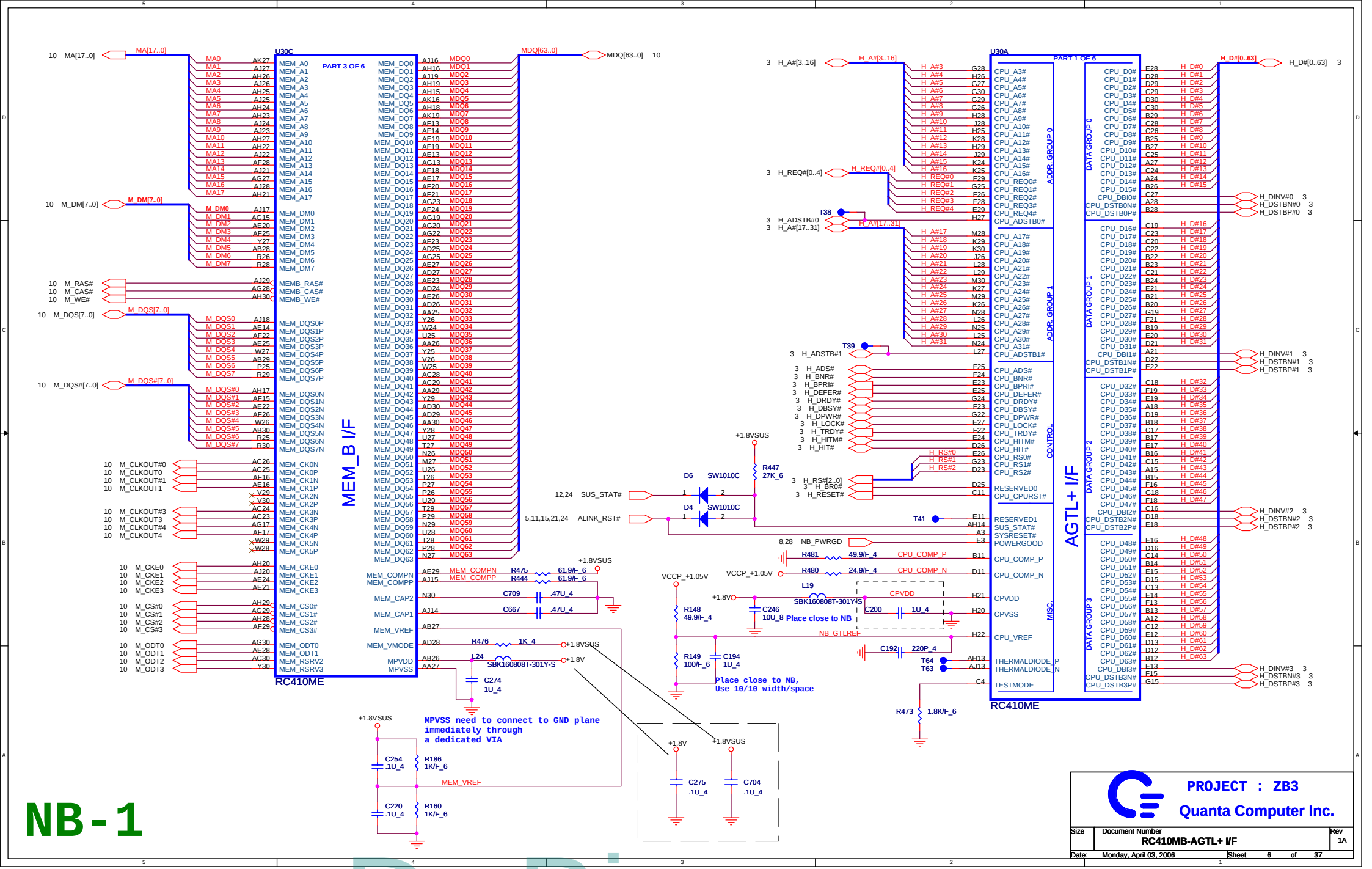
FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

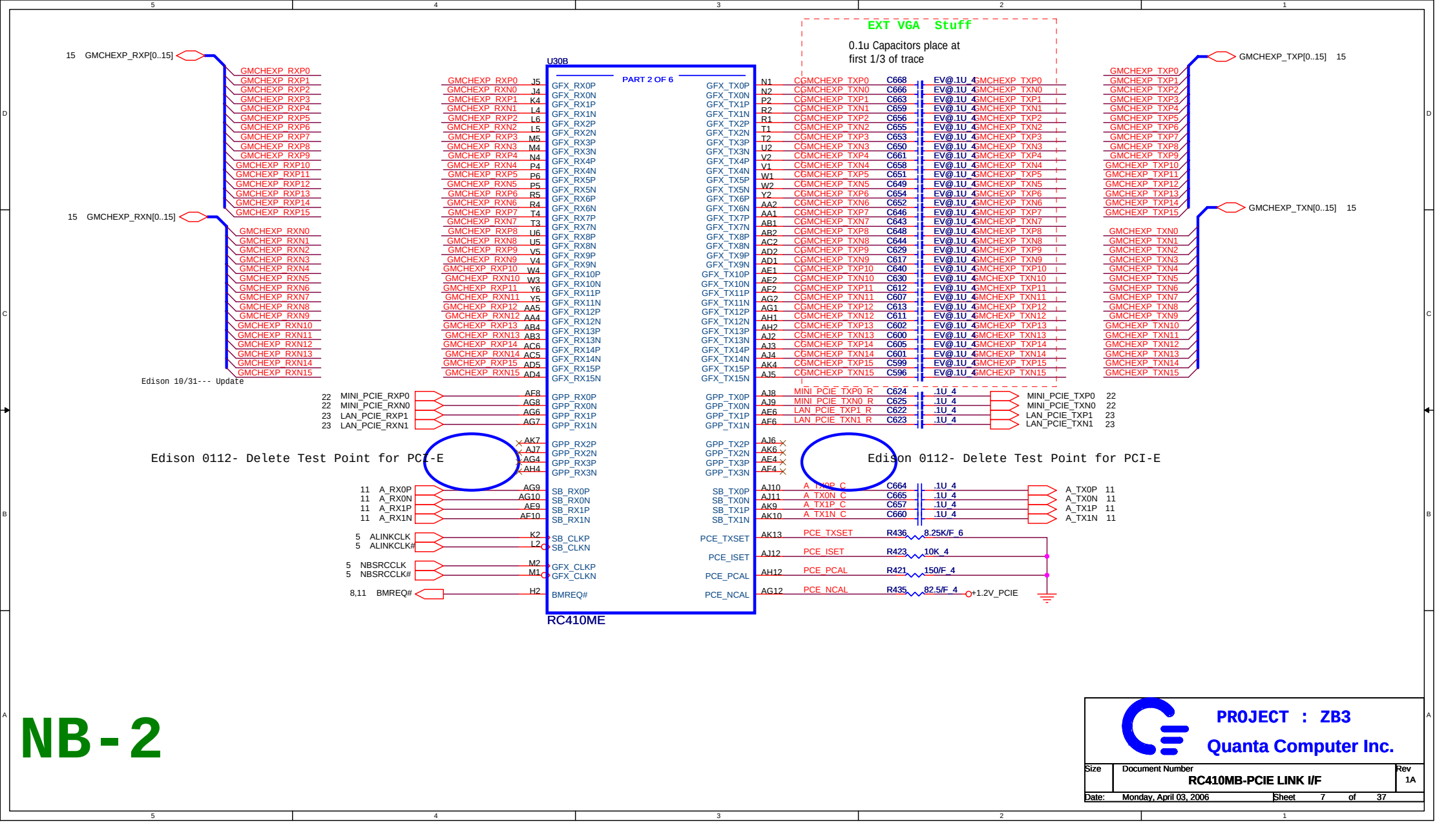
CY28RS400 and ICS951413 are fully pin compatible and can be interchanged without any hardware modification.

CLK

PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Monday, April 03, 2006	Sheet 5 of 37	


U30C
PART 3 OF 6
MEM_B I/F
RC410ME
U30A
PART 1 OF 6
AGTL+ I/F
RC410ME
MEMB_RAS#
MEMB_CAS#
MEMB_WE#
MPVSS need to connect to GND plane immediately through a dedicated VIA
Place close to NB, Use 10/10 width/space
Place close to NB
NB-1
PROJECT : ZB3
Quanta Computer Inc.
RC410MB-AGTL+ I/F
Monday, April 03, 2006
Sheet 6 of 37

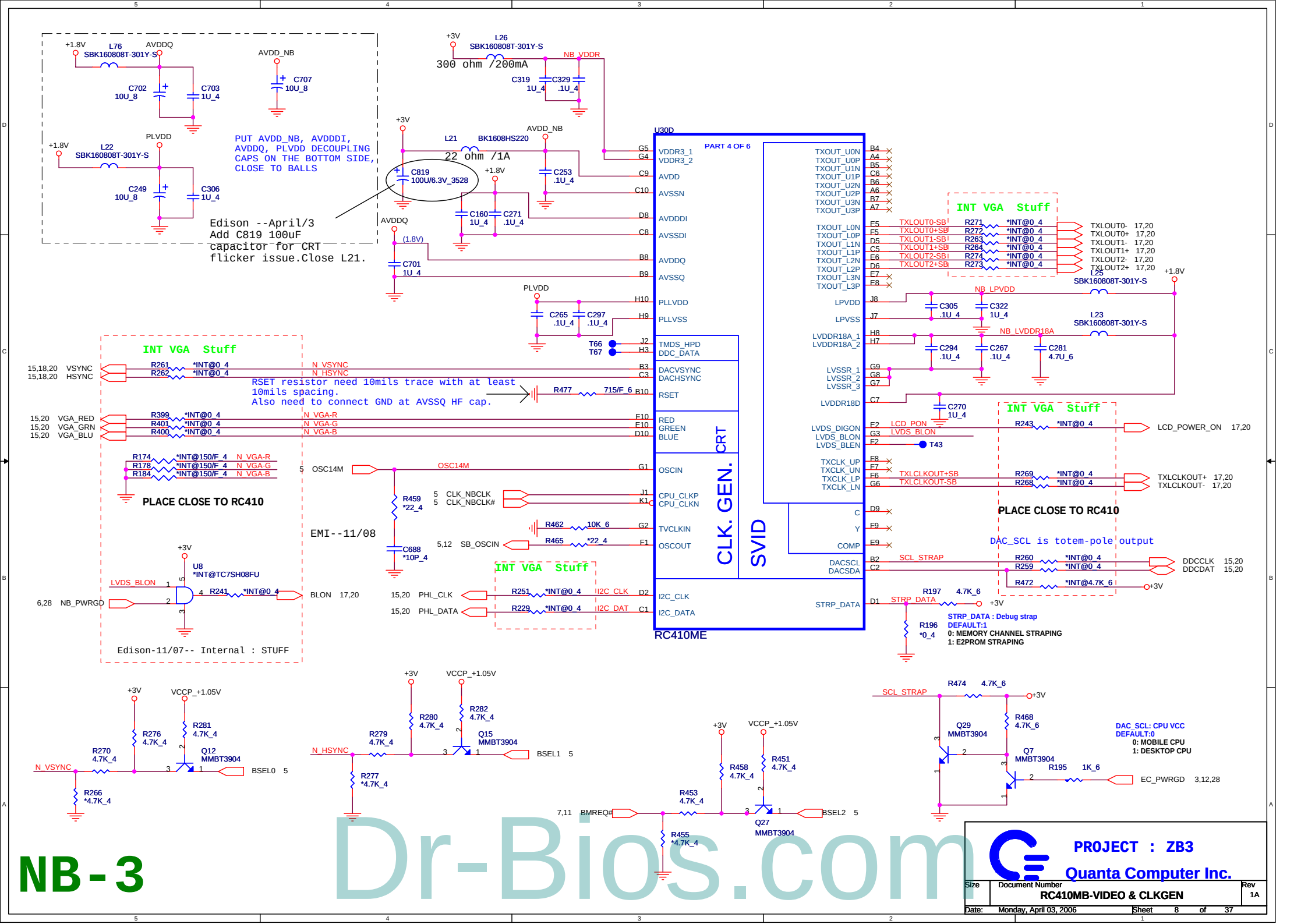


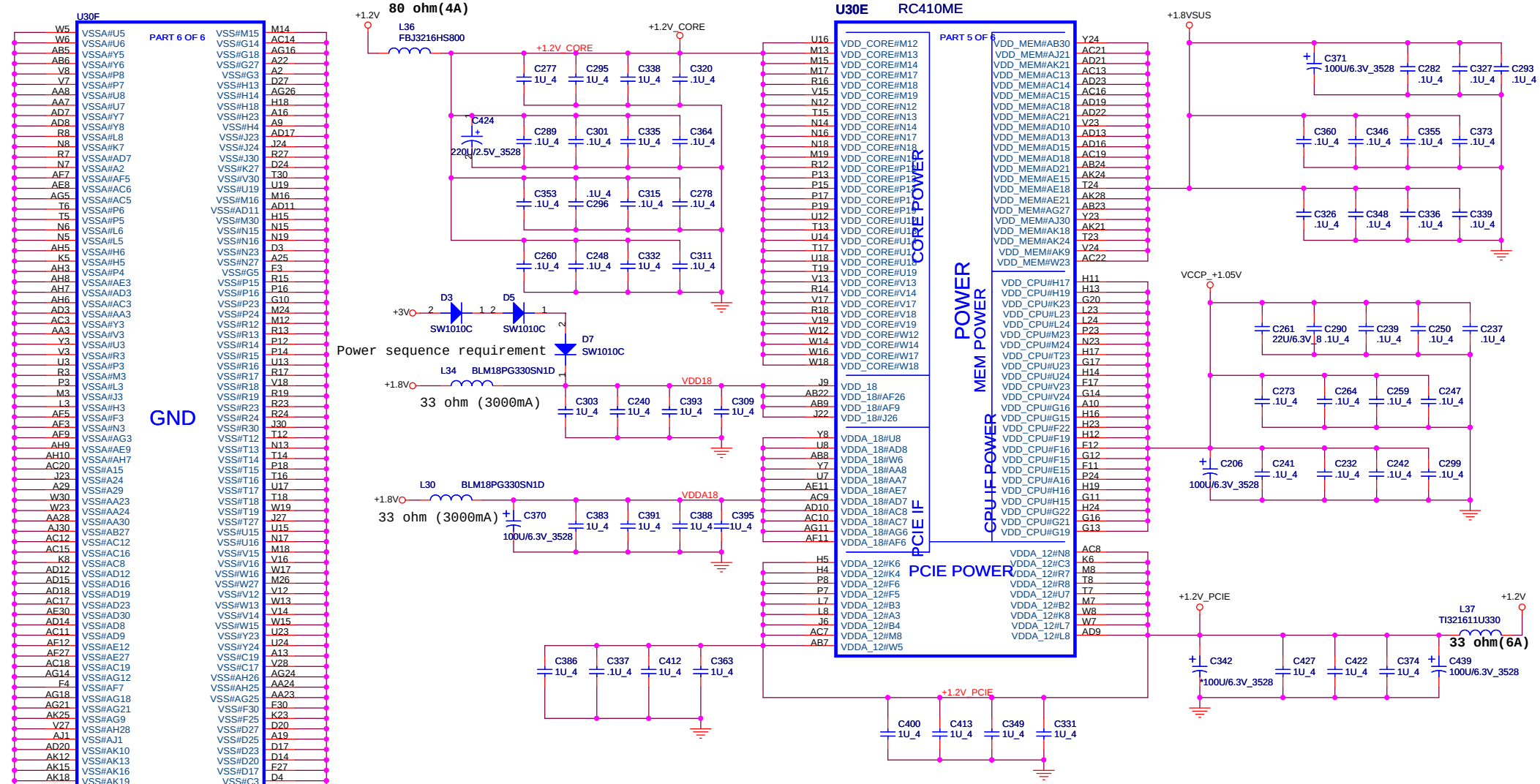
NB-2

PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-PCIE LINK I/F	1A
Date: Monday, April 03, 2006	Sheet 7 of 37	


PUT AVDD_NB, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS
Edison --April/3
Add C819 100uF
capacitor for CRT
flicker issue.Close L21.
300 ohm /200mA
22 ohm /1A
U30D
PART 4 OF 6
RC410ME
CLK. GEN.
SVID
CRT
INT VGA Stuff
RSET resistor need 10mils trace with at least 10mils spacing.
Also need to connect GND at AVSSQ HF cap.
PLACE CLOSE TO RC410
EMI--11/08
Edison-11/07-- Internal : STUFF
DAC_SCL is totem-pole output
STRP_DATA : Debug strap
DEFAULT:1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING
DAC_SCL: CPU VCC
DEFAULT:0
0: MOBILE CPU
1: DESKTOP CPU
NB-3
PROJECT : ZB3
Quanta Computer Inc.
RC410MB-VIDEO & CLKGEN
Monday, April 03, 2006
Sheet 8 of 37



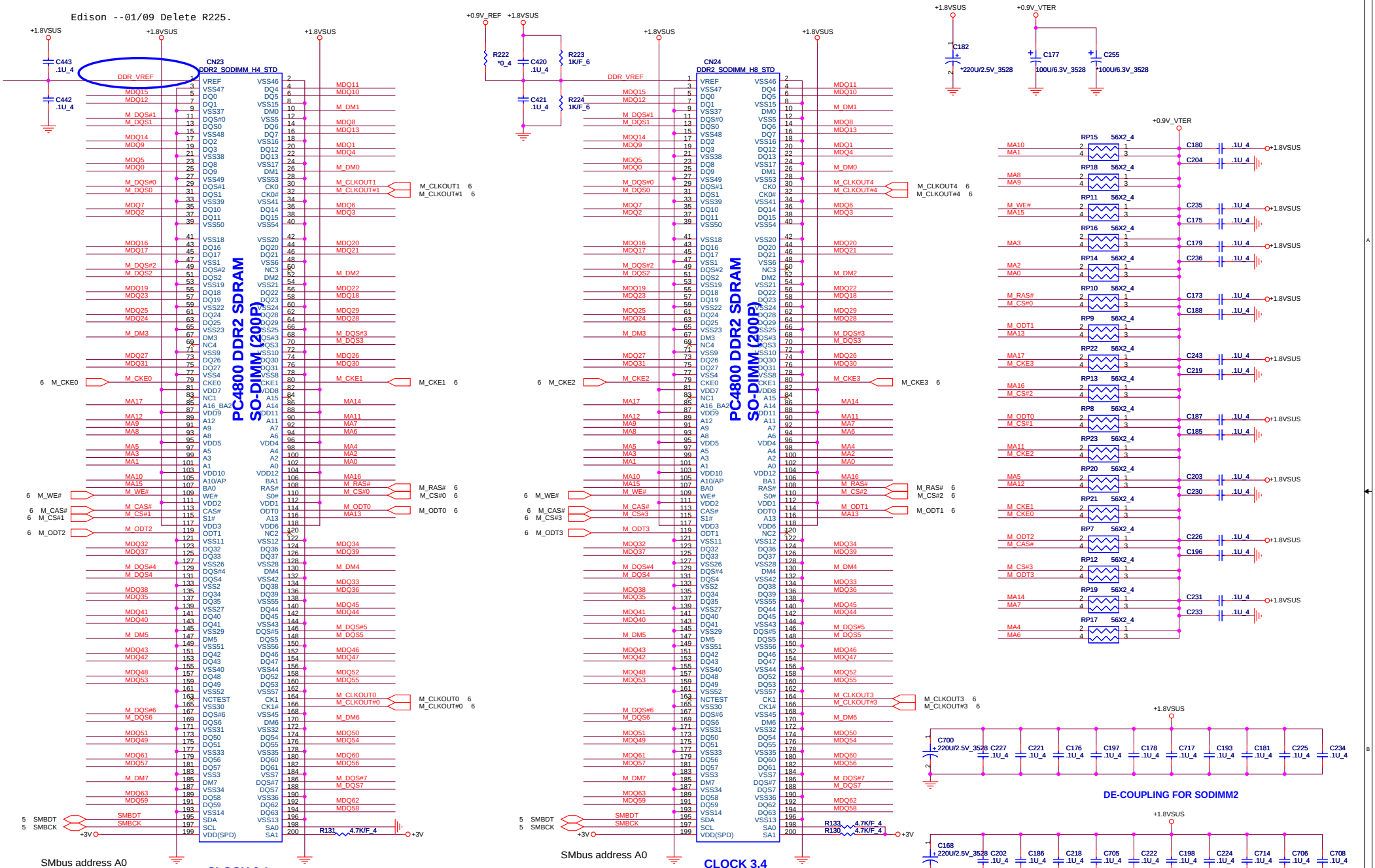
NB-4

PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-POWER	1A
Date: Monday, April 03, 2006	Sheet 9 of 37	

Edison --01/09 Delete R225.

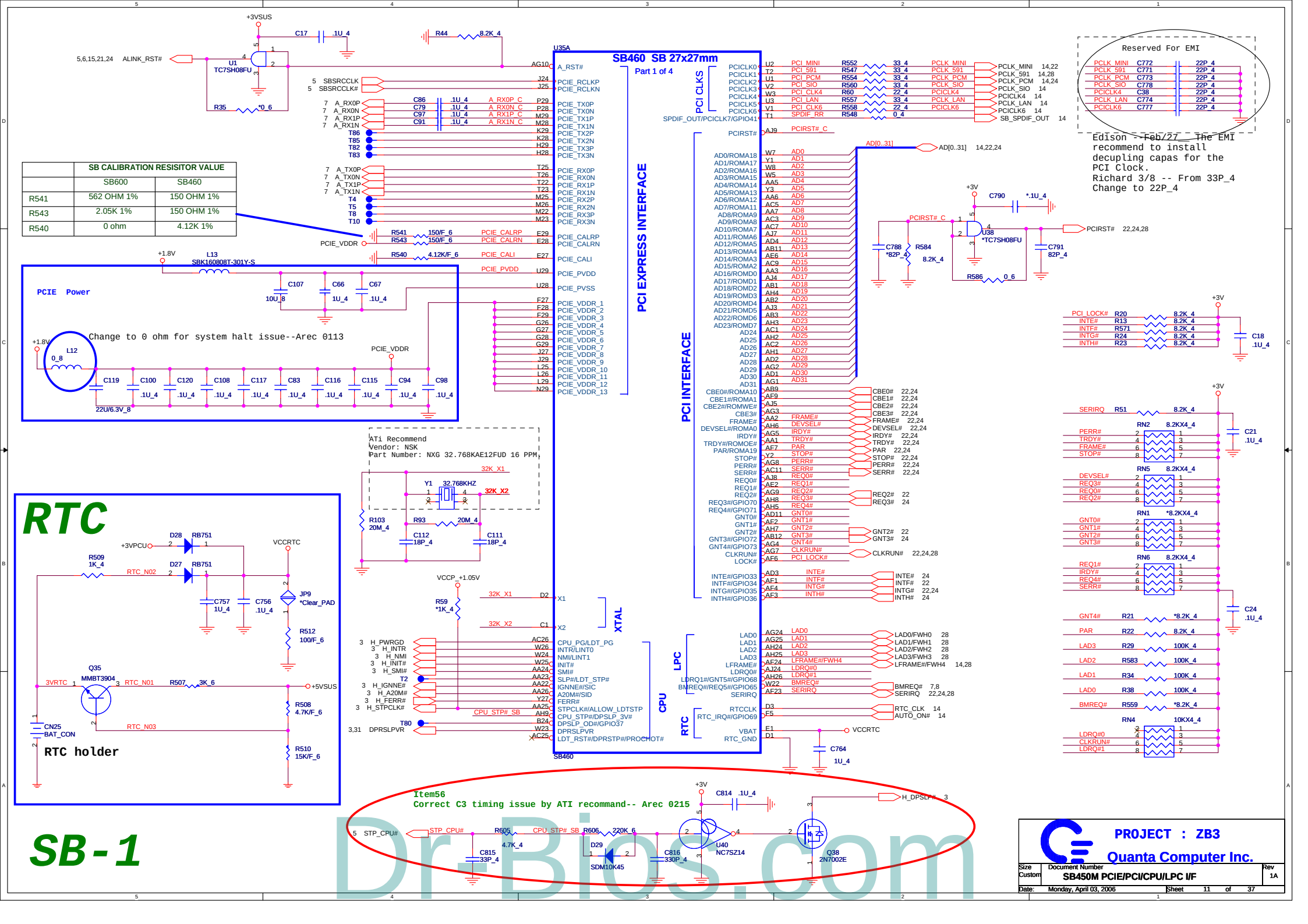


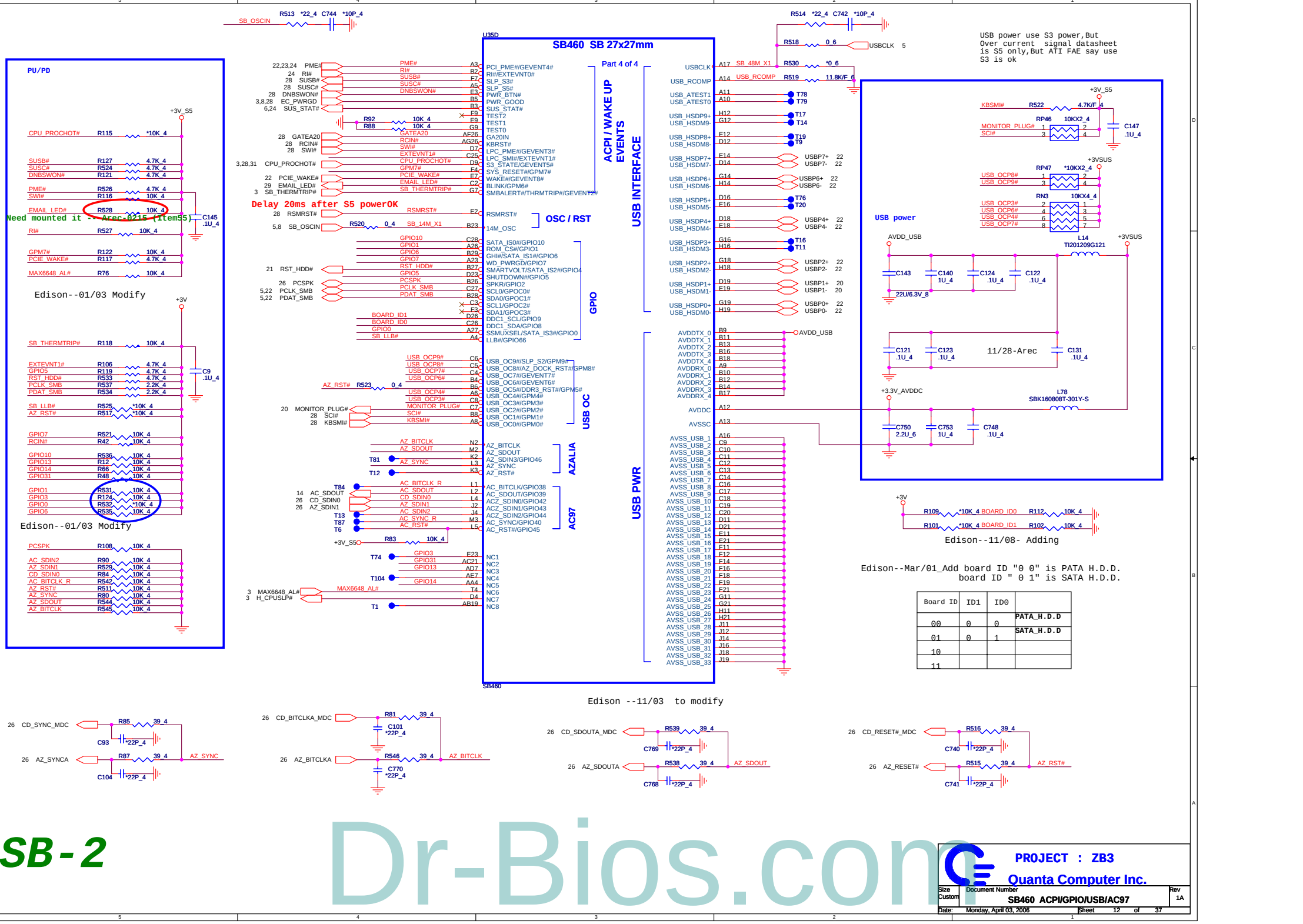
DDRII

PROJECT : ZB3

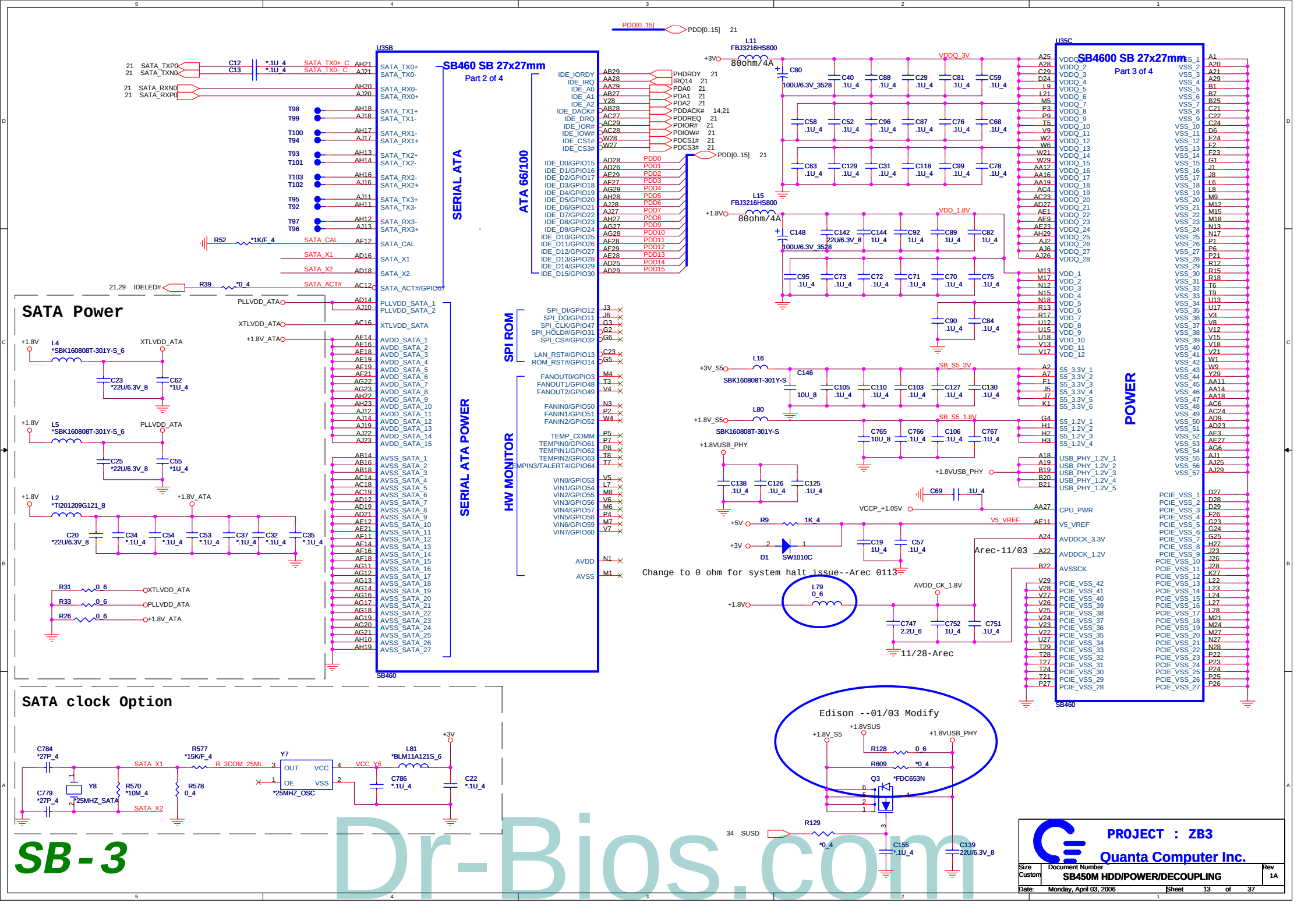
Quanta Computer Inc.

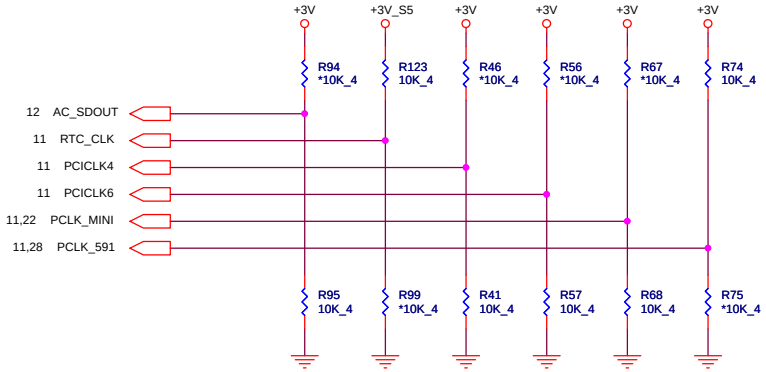
Size	Document Number	Rev
	DDR2 SO-DIMM	1A
Date: Monday, April 03, 2006	Sheet 10 of 37	

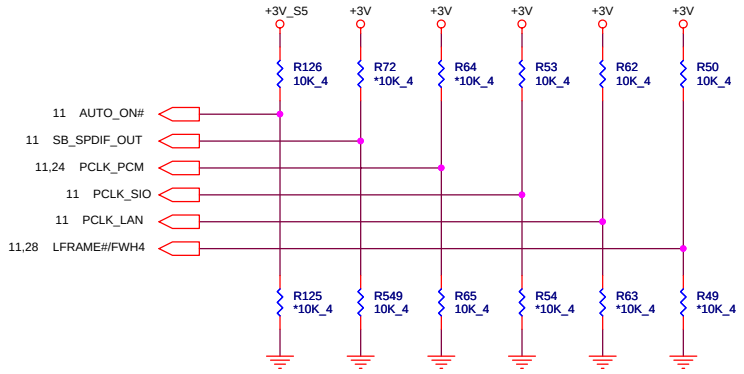

SB460 SB 27x27mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
SB460
SB CALIBRATION RESISITOR VALUE
SB600
SB460
R541 562 OHM 1% 150 OHM 1%
R543 2.05K 1% 150 OHM 1%
R540 0 ohm 4.12K 1%
PCIE Power
Change to 0 ohm for system halt issue--Arec 0113
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM
RTC
RTC holder
Reserved For EMI
Edison --Feb/27 -- The EMI recommend to install decupling capas for the PCI Clock.
Richard 3/8 -- From 33P_4 Change to 22P_4
Item56
Correct C3 timing issue by ATI recommand-- Arec 0215
SB-1
Dr.Bios.com
PROJECT : ZB3
Quanta Computer Inc.
SB450M PCIE/PCI/CPU/LPC I/F
Rev 1A
Date: Monday, April 03, 2006
Sheet 11 of 37



Board ID	ID1	ID0	
00	0	0	PATA_H.D.D
01	0	1	SATA_H.D.D
10			
11			


SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA Power
SATA clock Option
SB460 SB 27x27mm
Part 3 of 4
POWER
Change to 0 ohm for system halt issue--Arec 0113
Arec-11/03
11/28-Arec
Edison --01/03 Modify
SB-3
PROJECT : ZB3
Quanta Computer Inc.
SB450M HDD/POWER/DECOUPLING
Monday, April 03, 2006
Dr-Bios.com



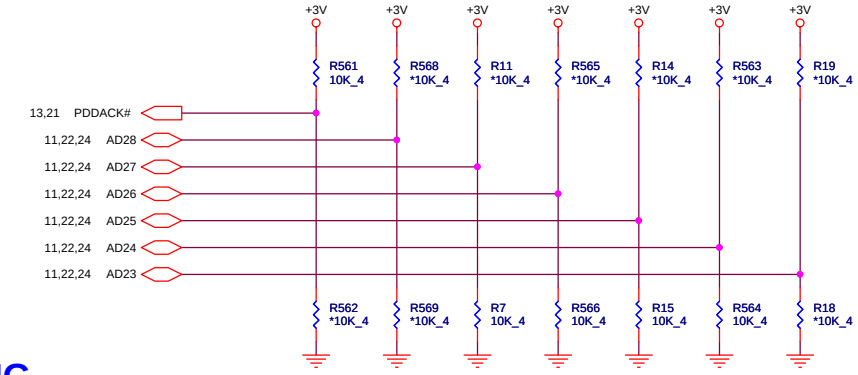


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

Edison-11/07-- Modify



DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

SB-4

PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB450M STRAPS	1A
Date: Monday, April 03, 2006	Sheet 14 of 37	

NOTE: some of the PCIE testpoints will be available trought via on traces.

MEMORY CLOCK SPREAD SPECTRUM

S0: H = -2.5%
S0: X = -0.6% (Default)
S0: L = -1.8%

PUT THEM CLOSE TO X'TAL

VGA H/W MONITOR

15 MIL

10 mil trace / 10 mil space

Close to pin ASIC

SLAVE ADDRESS: 9A

Edison -0111--
Detele resistor
R267,R278

VRAM TYPE STRAP PINS

POWERPLAY

HI: LOW CORE VOLTAGE FOR BATTERY MODE
LO: HIGH CORE VOLTAGE FOR PERFORMANCE MODE

PLACE CLOSE TO ASIC

PROJECT : ZB3
Quanta Computer Inc.
Size | Document Number: M52-P_MAIN_PCIE (1 of 4) | Rev: 00
Date: Thursday, April 06, 2006 | Sheet 15 of 37

RV410 MEMORY CHANNELS A and B

Channel B

19 MDA[0..63]

Z= 50 ohm

U29D — Part 4 of 7 — MEMORY INTERFACE B

MDA0 B12, MDA1 C12, MDA2 B11, MDA3 C11, MDA4 C8, MDA5 B7, MDA6 C7, MDA7 B6, MDA8 F12, MDA9 D12, MDA10 E11, MDA11 F11, MDA12 F9, MDA13 D8, MDA14 D7, MDA15 F7, MDA16 G12, MDA17 G11, MDA18 H12, MDA19 H11, MDA20 H9, MDA21 E7, MDA22 F8, MDA23 G8, MDA24 G6, MDA25 G7, MDA26 H8, MDA27 J8, MDA28 K8, MDA29 L8, MDA30 K9, MDA31 L9, MDA32 K5, MDA33 L4, MDA34 K4, MDA35 L5, MDA36 N5, MDA37 N6, MDA38 P4, MDA39 R4, MDA40 P2, MDA41 R2, MDA42 T3, MDA43 T2, MDA44 W3, MDA45 W2, MDA46 Y3, MDA47 Y2, MDA48 T4, MDA49 R5, MDA50 T5, MDA51 T6, MDA52 V5, MDA53 W5, MDA54 W6, MDA55 Y4, MDA56 R6, MDA57 T8, MDA58 R7, MDA59 T7, MDA60 V7, MDA61 W7, MDA62 W8, MDA63 W9

MAA[0..15] 19

MAIN TRUNK: Z= 35 ohm
BRACHES: Z= 55 ohm

MAA0 G4, MAA1 E6, MAA2 E4, MAA3 H4, MAA4 J5, MAA5 G5, MAA6 F4, MAA7 H6, MAA8 G3, MAA9 G2, MAA10 D4, MAA11 F2, MAA12 F5, MAA13 D5, MAA14 H2, MAA15 H3

-DQMA[0..7] 19

Z= 50 ohm

DQMBb_0 B8 -DQMA0, DQMBb_1 D9 -DQMA1, DQMBb_2 G9 -DQMA2, DQMBb_3 K7 -DQMA3, DQMBb_4 M5 -DQMA4, DQMBb_5 V2 -DQMA5, DQMBb_6 W4 -DQMA6, DQMBb_7 T9 -DQMA7

RDQSA[0..7] 19

Z= 50 ohm

QSB_0 B9 RDQSA0, QSB_1 D10 RDQSA1, QSB_2 H10 RDQSA2, QSB_3 K6 RDQSA3, QSB_4 N4 RDQSA4, QSB_5 U2 RDQSA5, QSB_6 U4 RDQSA6, QSB_7 V8 RDQSA7

WDQSA[0..7] 19

Z= 50 ohm

QSB_0B B10 WDQSA0, QSB_1B E10 WDQSA1, QSB_2B G10 WDQSA2, QSB_3B J7 WDQSA3, QSB_4B M4 WDQSA4, QSB_5B U3 WDQSA5, QSB_6B V4 WDQSA6, QSB_7B V9 WDQSA7

ODTB D6 ODTA0 19, ODTB1 J4 ODTA1 19

CLKB0 B4 M_CLKA0 19, CLKB0b B5 -M_CLKA0 19

Z= 100 ohm

CKEB0 C2 CKEA 19

RASB0b E2 -RASA 19

CASB0b D3 -CASA 19

WEB0b B2 -WEA 19

CSB0b_0 D2 -CSA0 19, CSB0b_1 E3

CLKB1 N2 M_CLKA1 19, CLKB1b P3 -M_CLKA1 19

CKEB1 L3 CKEA1 19

RASB1b J2 -RASA1 19

CASB1b L2 -CASA1 19

WEB1b M2 -WEA1 19

CSB1b_0 K2 -CSAb0 19, CSB1b_1 K3

Z= 55 ohm

EV@M52(M54)

+1.8V

R482 EV@100/F_4

VRAM_REF0

R483 EV@100/F_4

C715 EV@.1U_4

MVREFD_1 B3, MVREFS_1 C3

DRAM_RST AA3

TEST_MCLK AA5

TEST_YCLK AA2

MEMTEST AA7

+1.8V

R162 EV@100/F_4

VRAM_REF1

R176 EV@100/F_4

C223 EV@.1U_4

R208 EV@4.7K_4

R449 EV@4.7K_4

R205 EV@243/F_4

Channel A

U29C — Part 3 of 7 — MEMORY INTERFACE A

DQA_0 M31, DQA_1 M30, DQA_2 L31, DQA_3 L30, DQA_4 H30, DQA_5 G31, DQA_6 G30, DQA_7 F31, DQA_8 M27, DQA_9 M29, DQA_10 L28, DQA_11 L27, DQA_12 J27, DQA_13 H29, DQA_14 G29, DQA_15 G27, DQA_16 M26, DQA_17 L26, DQA_18 M25, DQA_19 L25, DQA_20 J25, DQA_21 G28, DQA_22 H27, DQA_23 H26, DQA_24 F26, DQA_25 G26, DQA_26 H25, DQA_27 H24, DQA_28 H23, DQA_29 H22, DQA_30 J23, DQA_31 J22, DQA_32 E23, DQA_33 D22, DQA_34 D23, DQA_35 E22, DQA_36 E20, DQA_37 F20, DQA_38 D19, DQA_39 D18, DQA_40 B19, DQA_41 B18, DQA_42 C17, DQA_43 B17, DQA_44 C14, DQA_45 B14, DQA_46 C13, DQA_47 B13, DQA_48 D17, DQA_49 E18, DQA_50 E17, DQA_51 F17, DQA_52 E15, DQA_53 E14, DQA_54 F14, DQA_55 D13, DQA_56 H18, DQA_57 H17, DQA_58 G18, DQA_59 G17, DQA_60 G15, DQA_61 G14, DQA_62 H14, DQA_63 J14

MVREFD_0 C31, MVREFS_0 C30

MAA_0 D26, MAA_1 F28, MAA_2 D28, MAA_3 D25, MAA_4 E24, MAA_5 F26, MAA_6 D27, MAA_7 F25, MAA_8 C26, MAA_9 B26, MAA_10 D29, MAA_11 B27, MAA_12 E27, MAA_13 E29, MAA_14 B25, MAA_15 C25

DQMAb_0 H31, DQMAb_1 J29, DQMAb_2 J26, DQMAb_3 G23, DQMAb_4 E21, DQMAb_5 B15, DQMAb_6 D14, DQMAb_7 J17

QSA_0 J31, QSA_1 K29, QSA_2 K25, QSA_3 F23, QSA_4 D20, QSA_5 B16, QSA_6 D16, QSA_7 H15

QSA_0B K31, QSA_1B K28, QSA_2B K26, QSA_3B G24, QSA_4B D21, QSA_5B C16, QSA_6B D15, QSA_7B J15

ODTA F29, ODTA1 D24

CLKA0 D31, CLKA0b E31

CKEA0 B30

RASA0b B28

CASA0b C29

WEA0b B31

CSA0b_0 B29, CSA0b_1 C28

CLKA1 B20, CLKA1b C19

CKEA1 C22

RASA1b B24

CASA1b B22

WEA1b B21

CSA1b_0 B23, CSA1b_1 C23

EV@M52(M54)

U29F — Part 6 of 7 — PCI-Express GND

PCIE_VSS_1 AH27, PCIE_VSS_2 AC23, PCIE_VSS_3 AL27, PCIE_VSS_4 R23, PCIE_VSS_5 P25, PCIE_VSS_6 R25, PCIE_VSS_7 T26, PCIE_VSS_8 U26, PCIE_VSS_9 W26, PCIE_VSS_10 Y26, PCIE_VSS_11 AB26, PCIE_VSS_12 AC26, PCIE_VSS_13 AD25, PCIE_VSS_14 AE26, PCIE_VSS_15 AF26, PCIE_VSS_16 AD26, PCIE_VSS_17 AG25, PCIE_VSS_18 AH26, PCIE_VSS_19 AC28, PCIE_VSS_20 Y28, PCIE_VSS_21 U28, PCIE_VSS_22 P28, PCIE_VSS_23 AH29, PCIE_VSS_24 AF28, PCIE_VSS_25 V29, PCIE_VSS_26 AC29, PCIE_VSS_27 W27, PCIE_VSS_28 AB27, PCIE_VSS_29 V26, PCIE_VSS_30 AJ26, PCIE_VSS_31 AJ32, PCIE_VSS_32 AK29, PCIE_VSS_33 P26, PCIE_VSS_34 P29, PCIE_VSS_35 R29, PCIE_VSS_36 T29, PCIE_VSS_37 U29, PCIE_VSS_38 W29, PCIE_VSS_39 Y29, PCIE_VSS_40 AA29, PCIE_VSS_41 AB29, PCIE_VSS_42 AD29, PCIE_VSS_43 AE29, PCIE_VSS_44 AF29, PCIE_VSS_45 AG29, PCIE_VSS_46 AJ29, PCIE_VSS_47 AK26, PCIE_VSS_48 AK30, PCIE_VSS_49 AG26, PCIE_VSS_50 N30, PCIE_VSS_51 R31, PCIE_VSS_52 AF30, PCIE_VSS_53 AC30, PCIE_VSS_54 V31, PCIE_VSS_55 P30, PCIE_VSS_56 AA31, PCIE_VSS_57 U30, PCIE_VSS_58 AD31, PCIE_VSS_59 AK32, PCIE_VSS_60 AJ28, PCIE_VSS_61 Y30, PCIE_VSS_62 AJ30, PCIE_VSS_63 AK31, PCIE_VSS_64 AA23, PCIE_VSS_65 AG31, PCIE_VSS_66 N24, PCIE_VSS_67 AB23, PCIE_VSS_68 P24, PCIE_VSS_69 R24, PCIE_VSS_70 T24, PCIE_VSS_71 U24, PCIE_VSS_72 Y24, PCIE_VSS_73 W24, PCIE_VSS_74 Y24, PCIE_VSS_75 AC24, PCIE_VSS_76 AH24, PCIE_VSS_77 V25, PCIE_VSS_78 AA25, PCIE_VSS_79 R26, PCIE_VSS_80 AA26, PCIE_VSS_81 T27, PCIE_VSS_82 AE27

L31 EV@BLM18PG181SN1D_6

PCIE_PVSS W23

VSS_1 B1, VSS_2 H1, VSS_3 L1, VSS_4 P1, VSS_5 U1, VSS_6 Y1, VSS_7 AD7, VSS_8 AE8, VSS_9 AL1, VSS_10 A2, VSS_11 AM2, VSS_12 AD10, VSS_13 E8, VSS_14 H5, VSS_15 K10, VSS_16 M8, VSS_17 T10, VSS_18 E12, VSS_19 AC9, VSS_20 AF14, VSS_21 AD8, VSS_22 C5, VSS_23 F10, VSS_24 J3, VSS_25 L6, VSS_26 M6, VSS_27 P6, VSS_28 AA4, VSS_29 AG11, VSS_30 V3, VSS_31 AG16, VSS_32 R3, VSS_33 C6, VSS_34 C9, VSS_35 F6, VSS_36 H7, VSS_37 J6

CORE GND

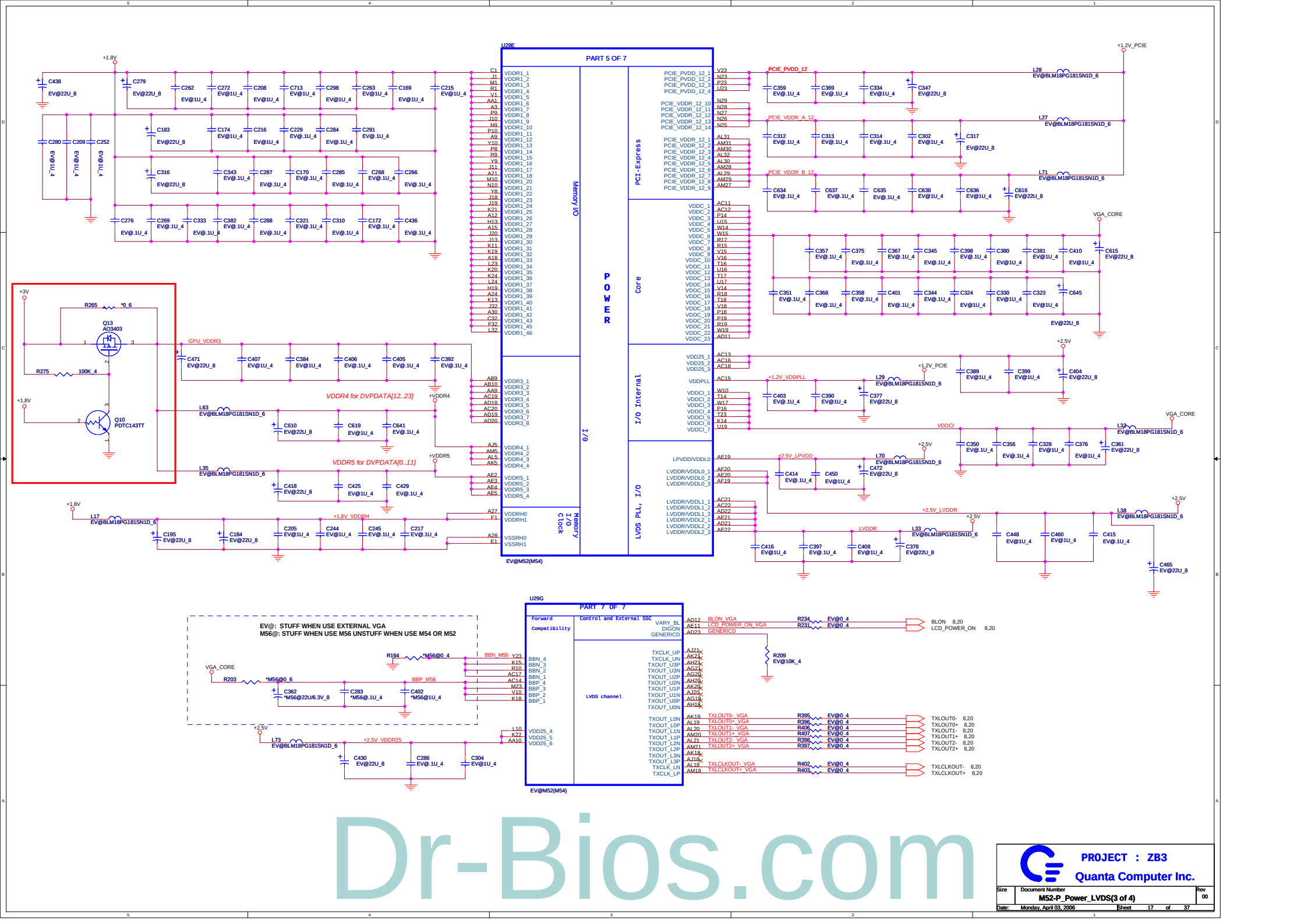
VSS_38 AD16, VSS_39 AA6, VSS_40 P7, VSS_41 P5, VSS_42 M3, VSS_43 M9, VSS_44 L7, VSS_45 M7, VSS_46 AD17, VSS_47 AH11, VSS_48 A8, VSS_49 U7, VSS_50 C10, VSS_51 E9, VSS_52 F3, VSS_53 J9, VSS_54 N7, VSS_55 N3, VSS_56 Y5, VSS_57 AM13, VSS_58 AC10, VSS_59 Y6, VSS_60 U6, VSS_61 E5, VSS_62 AL13, VSS_63 A11, VSS_64 U8, VSS_65 U9, VSS_66 U10, VSS_67 R6, VSS_68 AD6, VSS_69 V6, VSS_70 AD14, VSS_71 AD13, VSS_72 D11, VSS_73 J12, VSS_74 K12, VSS_75 A13, VSS_76 E13, VSS_77 E13, VSS_78 F15, VSS_79 K16, VSS_80 J21, VSS_81 H16, VSS_82 T15, VSS_83 V17, VSS_84 C15, VSS_85 C4, VSS_86 U14, VSS_87 P15, VSS_88 A16, VSS_89 E16, VSS_90 G13, VSS_91 G16, VSS_92 P17, VSS_93 R16, VSS_94 R14, VSS_95 W16, VSS_96 T15, VSS_97 C18, VSS_98 F16, VSS_99 W18, VSS_100 U18, VSS_101 AE16, VSS_102 AE17, VSS_103 A19, VSS_104 H32, VSS_105 F19, VSS_106 G19, VSS_107 N8, VSS_108 Y7, VSS_109 T19, VSS_110 V19, VSS_111 G21, VSS_112 C21, AE14 E21, AK16 AE14, U5 AK16, E22 U5, F18 E22, K30 F18, C24 K30, E24 C24, M24 E24, A25 M24, D30 A25, E25 D30, G25 E25, G20 G25, G22 G20, E27 G22, E28 E27, H21 E28, C27 H21, E32 C27, H28 E32, J30 H28, K17 J30, K27 K17, M32 K27, A22 M32, C20 A22, E19 C20, H20 E19, J24 H20, M28 J24, J28 M28, J16 J28, F30 J16, L29 F30, A31 L29, B32 A31, E30 B32, AE15 E30, AG23 AE15, AD9 AG23, AF16 AD9, AH10 AF16, AJ10 AH10, AD15 AJ10, AH16 AD15, K23 AH16, VSS_159 K23

EV@M52(M54)

PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	M52-P_MEM_GND (2 of 4)	00

Date: Monday, April 03, 2006 Sheet 16 of 37



PROJECT : ZB3		
Quanta Computer Inc.		
Size	Document Number	Rev
	M52-P_Power_LVDS(3 of 4)	00
Date: Monday, April 03, 2006	Sheet 17 of 37	

OPTION STRAPS

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground ↓ High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

Vendor P/N	QCI P/N	Size	GPU_GPIO13	GPU_GPIO12	MEMTYP_1	MEMTYP_0
HYB18T256161AFL25	AKD5JG-T^00	**16M*16 *4pcs (128MB)**	0	0	0	0
HY5PS561621AFP-25	AKD5JG-TW12					
K4N56163QG-ZC25	AKD5JG-T514					
HYB18T512161BF-25	AKD5FG-T^00	32M*16 *2pcs (128MB)	0	0	1	1
HY5PS121621BFP-25	AKD5FG-TW14	**32M*16 *4pcs (256MB)**	0	1	0	1
K4N51163QC-ZC25	AKD5FGBT501					

(Default setting)

Memory Aperture Size Select
When no ROM is attached, GPIO_9 is set to 0
GPIO_[13:12] is used to select the memory aperture size.
GPIO_[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO_[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO_[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO_[13:12] = 11: reserved, same as ROM strap 11

Default: 128M memory aperture.
GPIO_[13:12] = 01 (256M memory aperture) recommended
for designs with 256MB or 512MB of physical memory.

+3V

15 GPU_GPIO0 — GPU_GPIO0 — R433 — EV@10K_4
15 GPU_GPIO1 — GPU_GPIO1 — R432 — EV@10K_4
15 GPU_GPIO2 — GPU_GPIO2 — R422 — *EV@10K_4
15 GPU_GPIO3 — GPU_GPIO3 — R431 — *EV@10K_4
15 GPU_GPIO4 — GPU_GPIO4 — R434 — *EV@10K_4
15 GPU_GPIO5 — GPU_GPIO5 — R437 — EV@10K_4

GPIO5 MUST PULL UP

15 GPU_GPIO6 — GPU_GPIO6 — R441 — *EV@10K_4
15 GPU_GPIO8 — GPU_GPIO8 — R215 — *EV@10K_4

Memory Size strap

15 GPU_GPIO9 — GPU_GPIO9 — R219 — *EV@10K_4
15 GPU_GPIO11 — GPU_GPIO11 — R445 — *EV@10K_4
15 GPU_GPIO12 — GPU_GPIO12 — R217 — *EV@10K_4
15 GPU_GPIO13 — GPU_GPIO13 — R212 — *EV@10K_4

000x - No ROM, MEM_AP_SIZE=00 128MB
001x - No Rom, MEM_AP_SIZE=01 256M & 512MB
010x - No Rom, MEM_AP_SIZE=10 64MB
011x - No ROM,MEM_AP_SIZE=11 Reserved

8,15,20 VSYNC — R247 — *10K_4
8,15,20 HSYNC — R248 — *10K_4

Memory identification for BIOS
00 - DDR2 16X16X4pcs 128MB
01 - DDR2 32X16X4pcs 256MB
10 - DDR2 16X16X2pcs 64MB
11 - DDR2 32X16X2pcs 128MB

Memory Q'ty ID

15 MEMTYP_0 — R236 *10K_4 / R238 10K_4
15 MEMTYP_1 — R237 *10K_4 / R230 10K_4
15 MEMTYP_2 — R249 *10K_4 / R250 *10K_4

RESERVE FOR MEMORY ID

15 GENERICC — R210 EV@10K_4 / R206 EV@10K_4

ATI FAE: ALL N/A

+1.8V
R425 *EV@10K_4 R427 *EV@10K_4
DC_Strap4 15 DC_Strap2 15
R428 *EV@10K_4 R426 *EV@10K_4

+3V +1.8V
R429 *EV@10K_4 R216 *EV@10K_4
15 DC_Strap3 15 GPU_GPIO10
R211 *EV@10K_4 R430 *EV@10K_4

M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWRS_ENB	GPIO0 (Internal pull-down)	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	1
TX_DEEMPH_EN	GPIO1 (Internal pull-down)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO(3:2) (Internal pull-down)	RSVD	
DEBUG_ACCESS	GPIO4 (Internal pull-down)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5 (Internal pull-down)	RSVD	
	GPIO6 (Internal pull-down)	RSVD	
Force_ Compliance	GPIO8 (Internal pull-down)	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13,12,11) (Internal pull-down)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	000
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

00

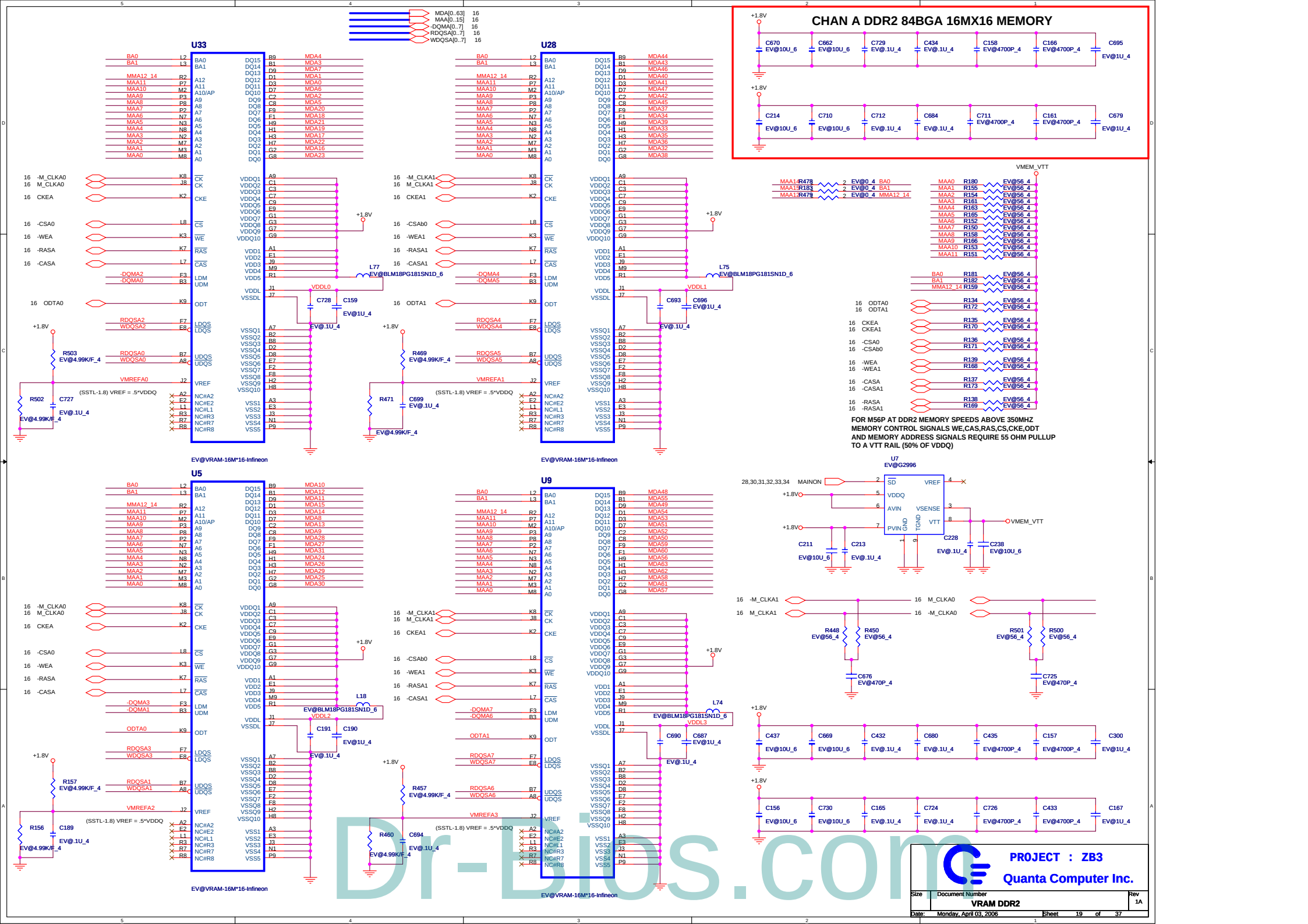
Board Straps REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVPDATA(1:0)	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	DVPDATA13	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	DVPDATA14	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	DVPDATA15	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

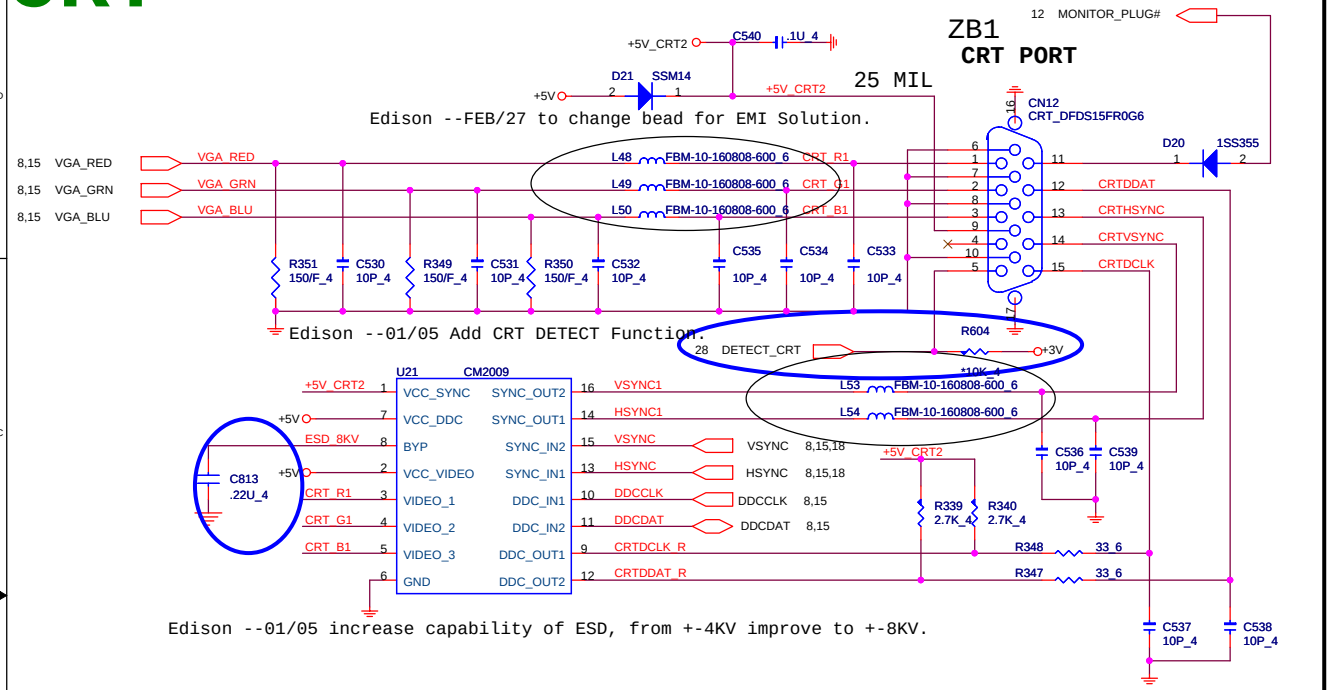
PROJECT : ZB3
Quanta Computer Inc.

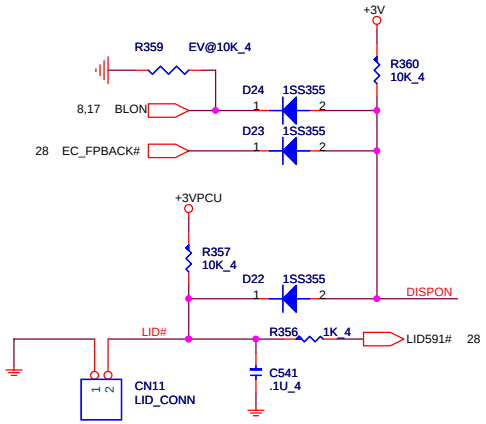
Size	Document Number	Rev
	M52-P_Straps (4 of 4)	00

Date: Monday, April 03, 2006 Sheet 18 of 37

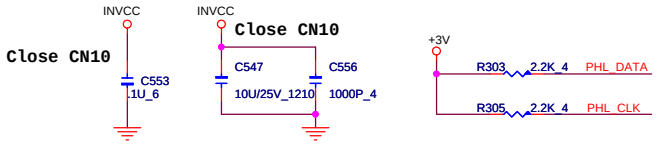

MDA[0..63] 16
MAA[0..15] 16
-DQMA[0..7] 16
RDQSA[0..7] 16
WDQSA[0..7] 16
CHAN A DDR2 84BGA 16MX16 MEMORY
U33
U28
U5
U9
U7
EV@G2996
EV@VRAM-16M*16-Infineon
VMEM_VTT
FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP
TO A VTT RAIL (50% OF VDDQ)
(SSTL-1.8) VREF = .5*VDDQ
PROJECT : ZB3
Quanta Computer Inc.
VRAM DDR2
Monday, April 03, 2006
Sheet 19 of 37
Dr-BIOS.com

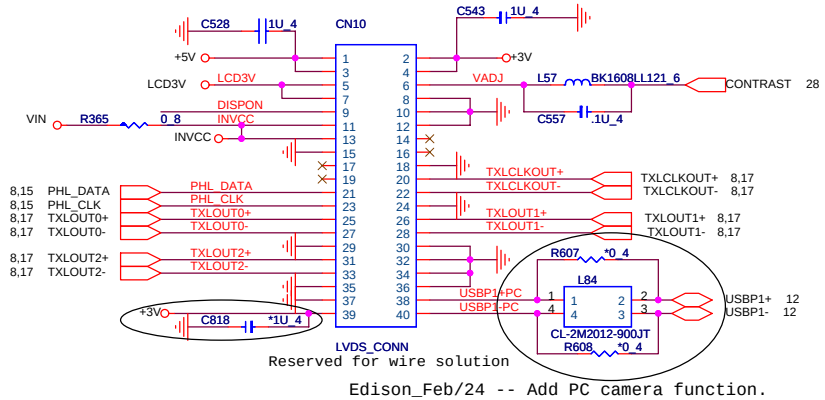
CRT

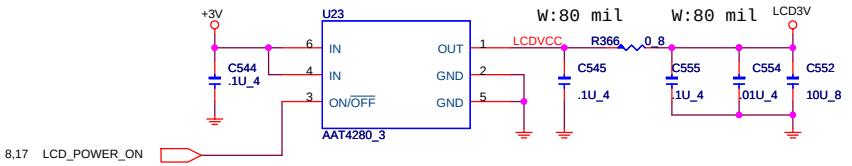




LVDS







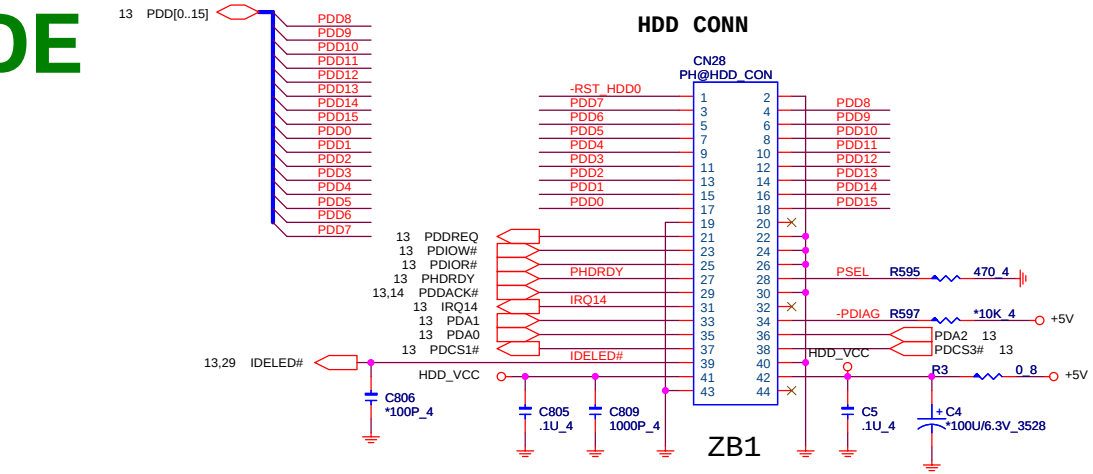
DSC Pinout : pin1 -- VCC(+3V)
pin2 -- USB-
pin3 -- USB+
pin4 -- GND
pin5 -- Shielding
the connector is JST SM05B-SSR-H-TB

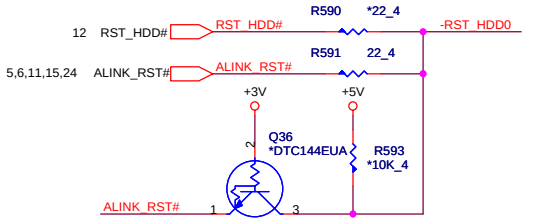
PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	VGA Ports, LID, & HOLES	1A
Date: Monday, April 03, 2006	Sheet 20 of 37	

IDE

HDD CONN

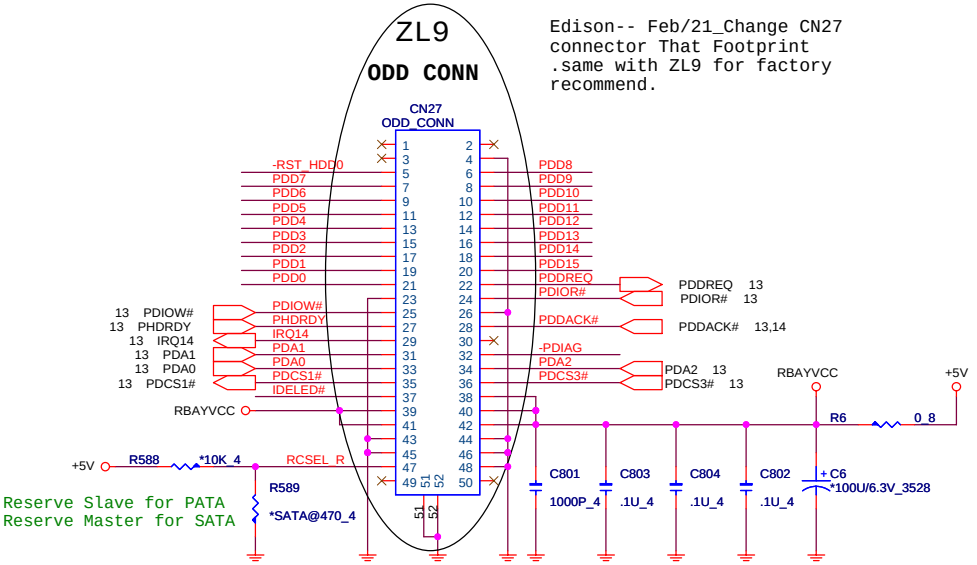


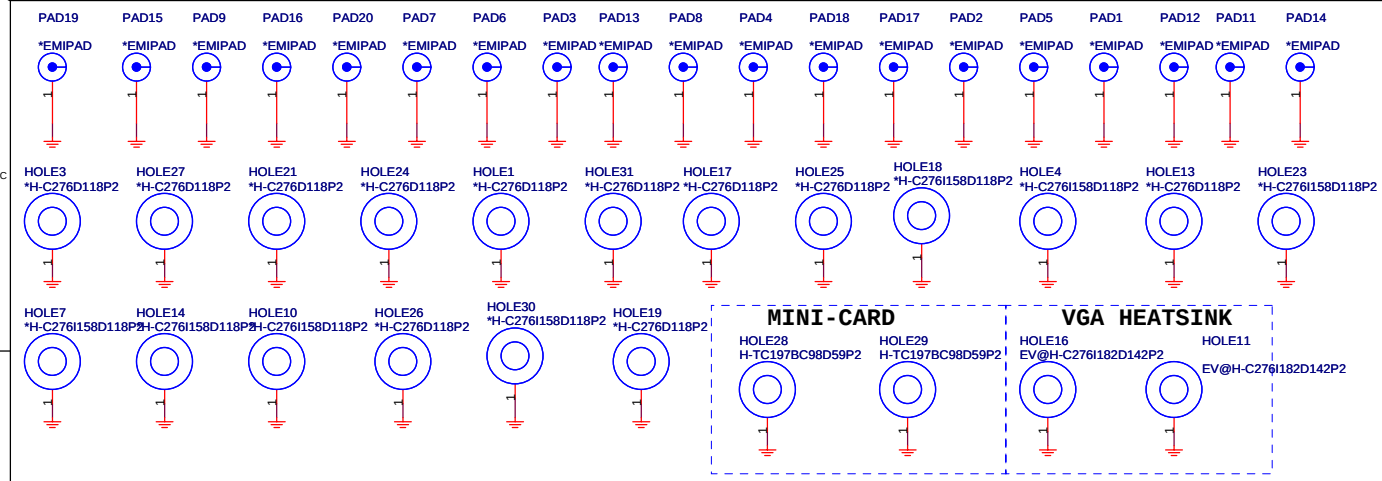


CLOSE IDE SIDE

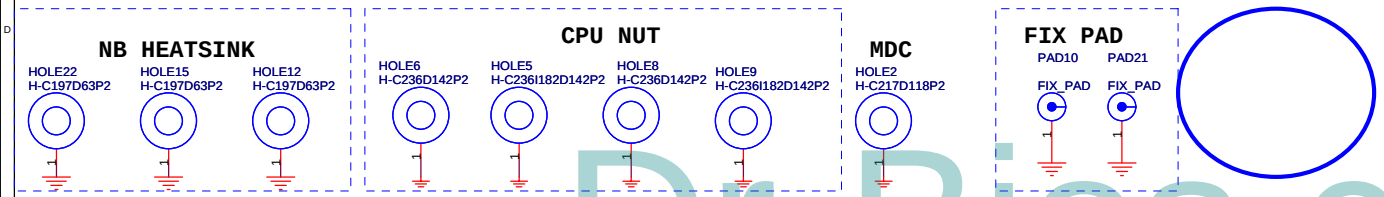
ZL9 ODD CONN

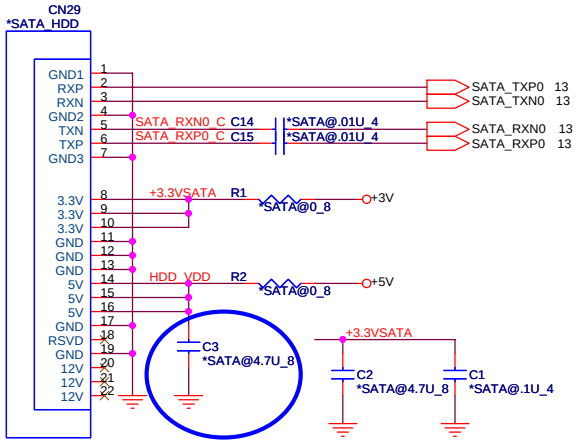
Edison-- Feb/21_Change CN27 connector That Footprint .same with ZL9 for factory recommend.

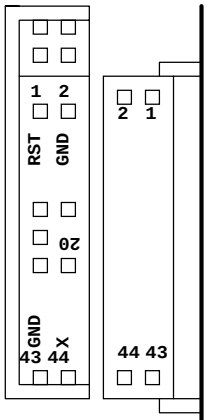




Edison 0106 - Delete PAD22 ~ PAD24.







Edison 0112 - To modify the C3 connect to HDD_VDD.

PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM , HOLES	1A
Date: Monday, April 03, 2006	Sheet 21 of 37	

ID Select : AD20
Interrupt Pin : INTF# , INTG#
Request Indicate : REQ2#
Grant Indicate : GNT2#

MINI-PCI

CN18 MINIPCI

Edison ---Feb/22_ Delete the C673, C674 capacitor for PCI-E of Minicard.

Edison -0104-- Modify

Edison -0111-- Delete Resistor R439,R440,R438

Close Minicard connector

Edison--Mar/02__Add EMI solution install L52, and also delete R354,R355.

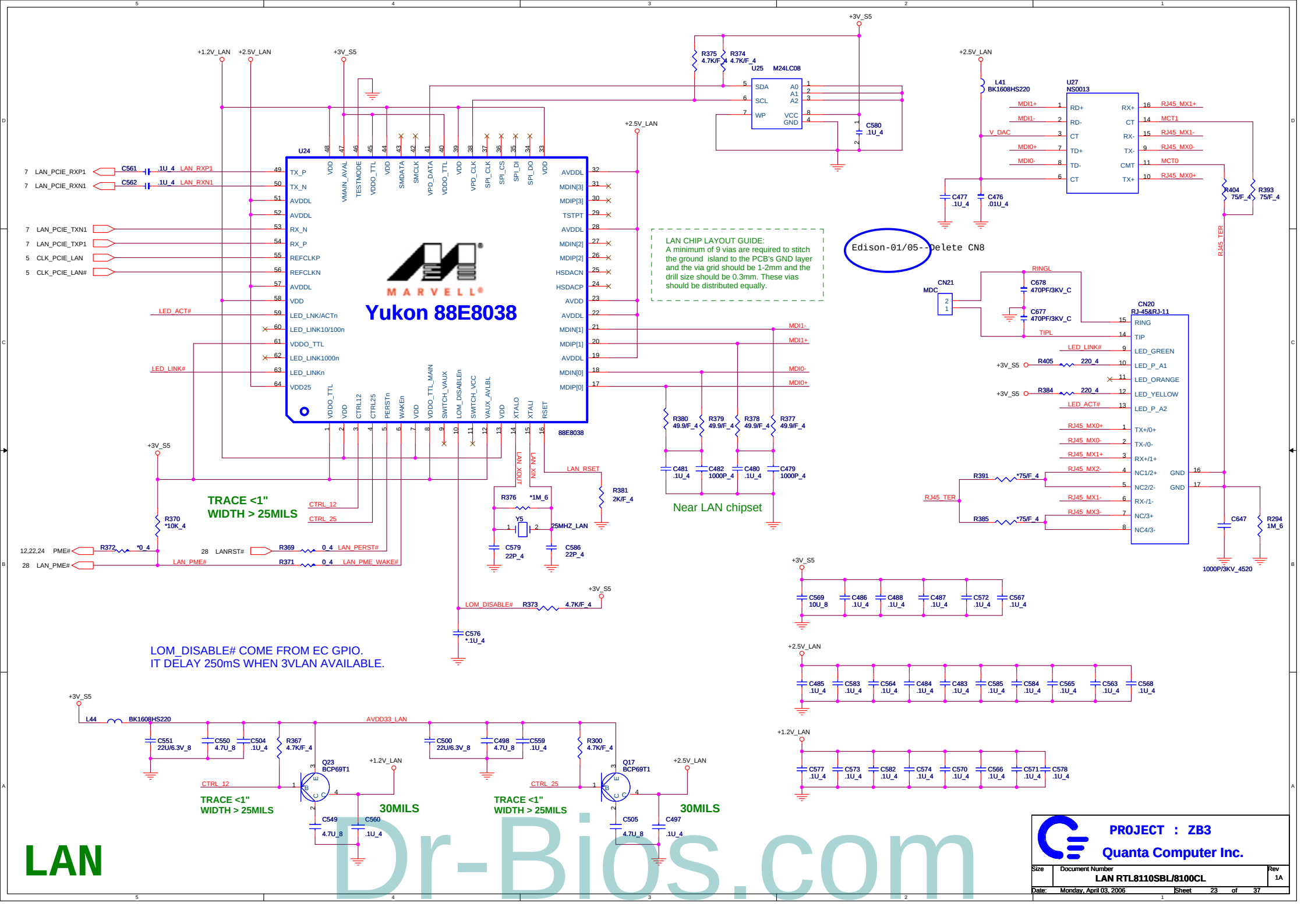
Edison--Mar/22__Add EMI solution install L51/L56, and also delete R352,R353,R362,R363.

MPC

USB

PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI&PCI-E,USB PORT	1A
Date: Monday, April 03, 2006	Sheet 22 of 37	


Yukon 88E8038
MARVELL
U24
88E8038
U25 M24LC08
U27 NS0013
L41 BK1608HS220
CN21 MDC
CN20 RJ-45&RJ-11
L44 BK1608HS220
Q23 BCP69T1
Q17 BCP69T1
Y5 25MHZ_LAN
+1.2V_LAN
+2.5V_LAN
+3V_S5
LAN_RXP1
LAN_RXN1
LAN_PCIE_TXN1
LAN_PCIE_TXP1
CLK_PCIE_LAN
CLK_PCIE_LAN#
LED_ACT#
LED_LINK#
LAN_RSET
CTRL_12
CTRL_25
LAN_PERST#
LAN_PME#
LAN_PME_WAKE#
LOM_DISABLE#
AVDD33_LAN
MDI1-
MDI1+
MDI0-
MDI0+
RJ45_MX1+
RJ45_MX1-
RJ45_MX0+
RJ45_MX0-
MCT1
MCT0
RJ45_TER
LAN CHIP LAYOUT GUIDE:
A minimum of 9 vias are required to stitch the ground island to the PCB's GND layer and the via grid should be 1-2mm and the drill size should be 0.3mm. These vias should be distributed equally.
Edison-01/05--Delete CN8
TRACE <1"
WIDTH > 25MILS
Near LAN chipset
30MILS
LOM_DISABLE# COME FROM EC GPIO.
IT DELAY 250mS WHEN 3VLAN AVAILABLE.
LAN
PROJECT : ZB3
Quanta Computer Inc.
LAN RTL8110SBL/8100CL
Monday, April 03, 2006
Sheet 23 of 37
Dr-Bios.com

ID Select : AD17
Interrupt Pin : INTE#/INTG#(share)/INTH#
Request Indicate : REQ3#
Grant Indicate : GNT3#

CARDBUS SLOT
ZB1

Near Slot

CN19

U10A PCI7412

PCI Interface

1394 Interface

Miscellaneous

U10B PCI7412

CardBus Interface

UPPER PIN

LOWER PIN

CARD_BUS

Near Chipset

+3V Plane

U10D Power/GND PCI7412

Cardbus EEPROM

U6 2K bit 24LC02BT

Cardbus power switch

U11 TPS2220APWP

Near TPS2210A

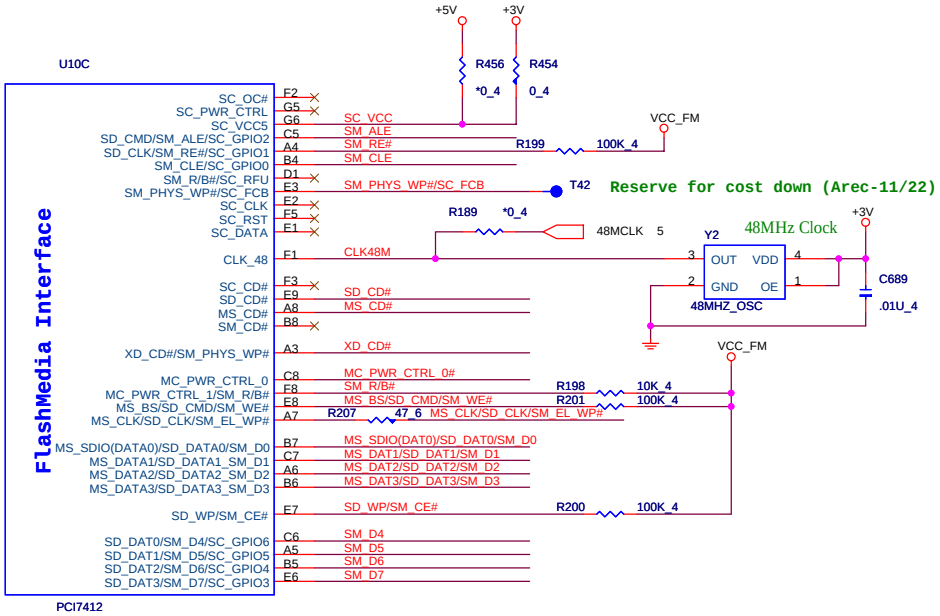
CARD Bus

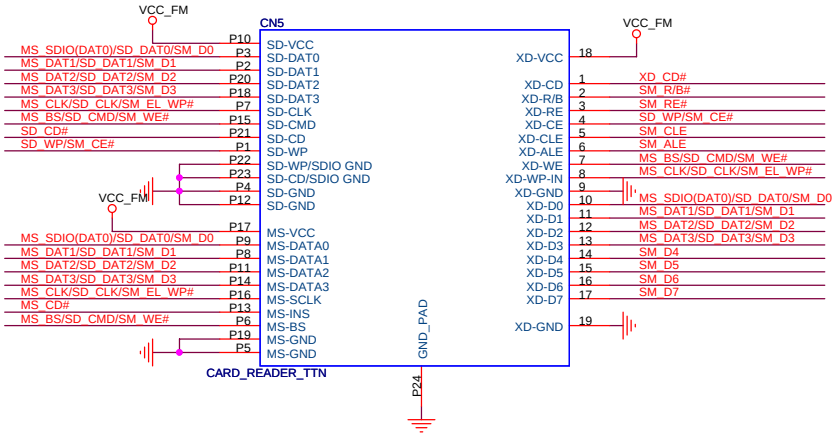
PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-PCMCIA CONTROLLE	1A
Date: Monday, April 03, 2006	Sheet 24 of 37	

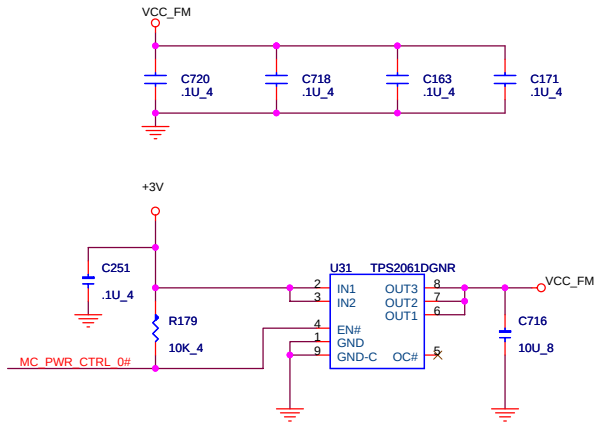
Reserve for XD identification (Arec-11/23)

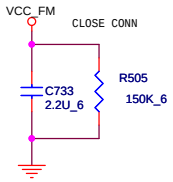
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

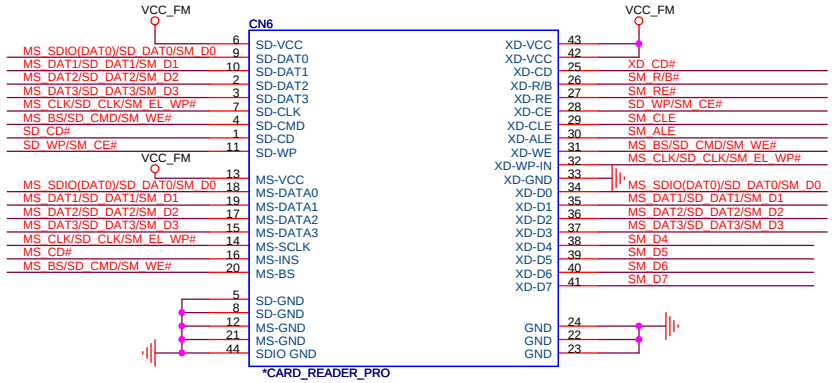




5 IN1 CARD READER





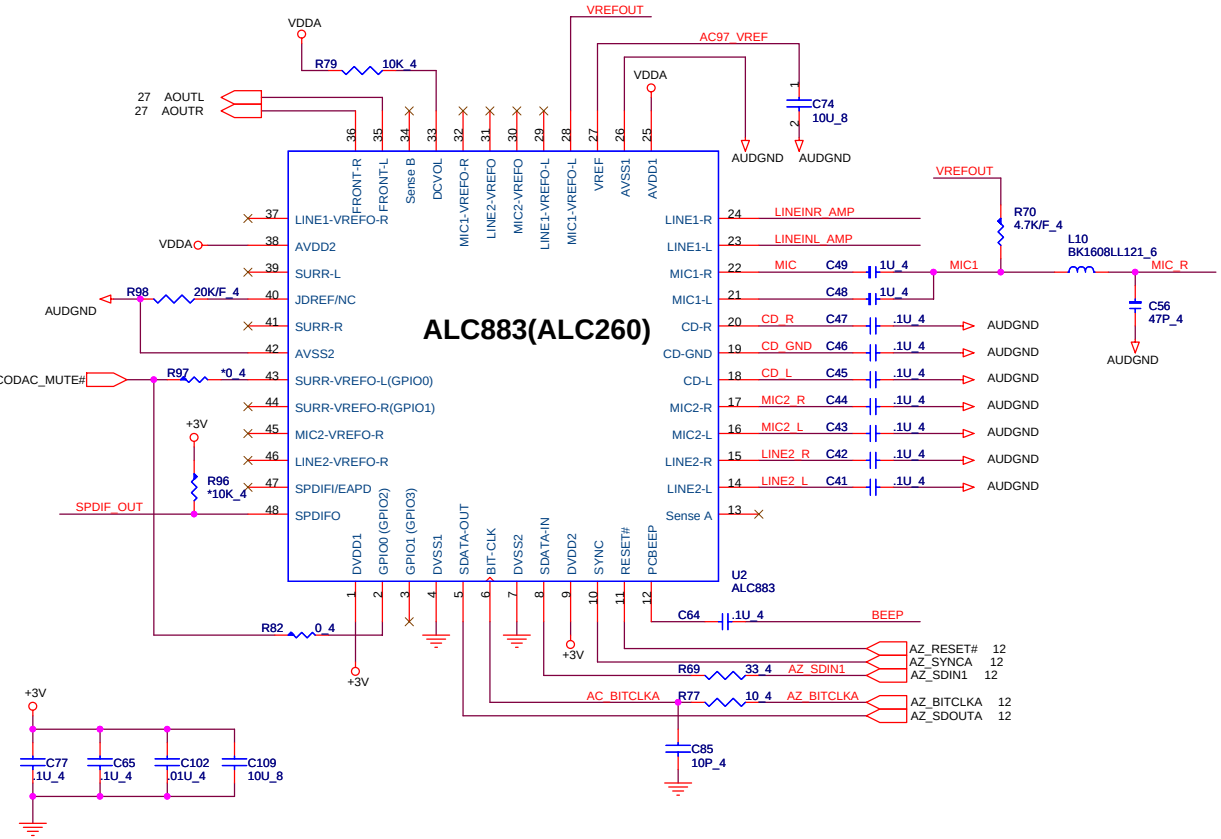


PROJECT : ZB2

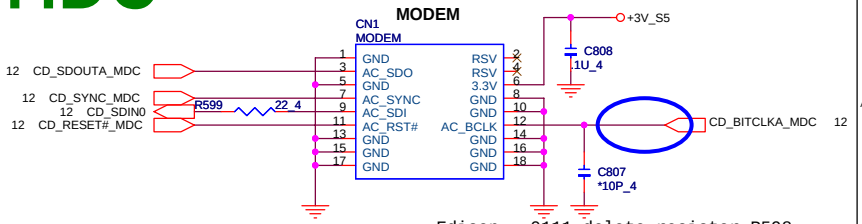
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-CARD READER	00
Date: Monday, April 03, 2006	Sheet 25 of 37	

ADO

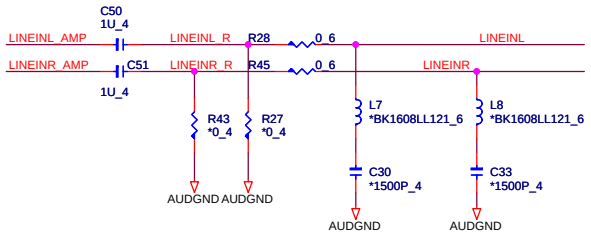


MDC



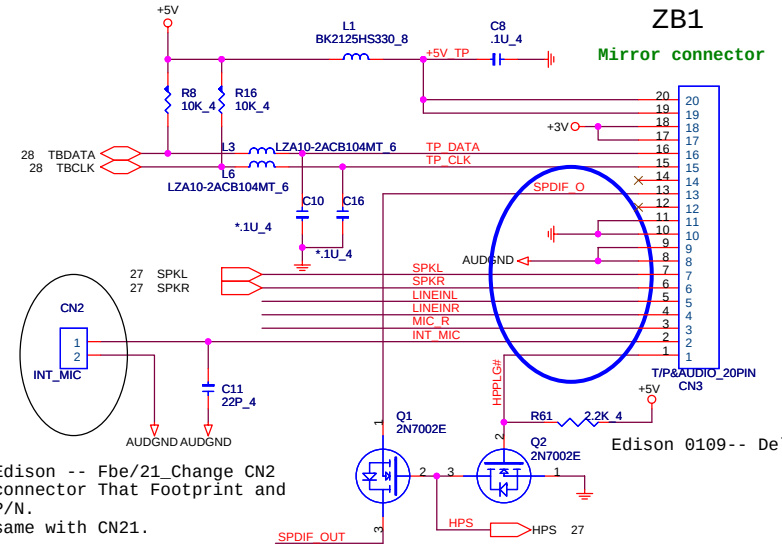
Edison --0111 delete resistor R598

LINE IN



ZB1

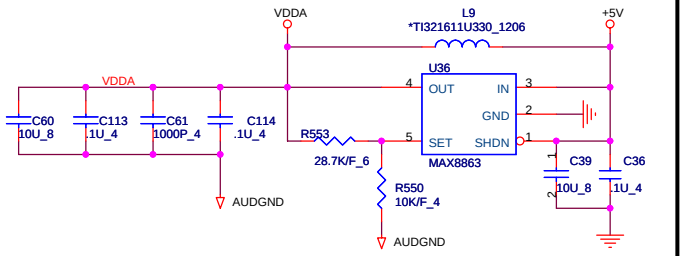
Mirror connector



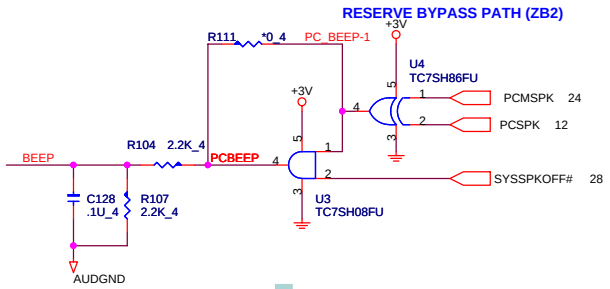
Edison -- Fbe/21_Change CN2 connector That Footprint and P/N.
same with CN21.

Edison 0109-- Delete

Audio Power



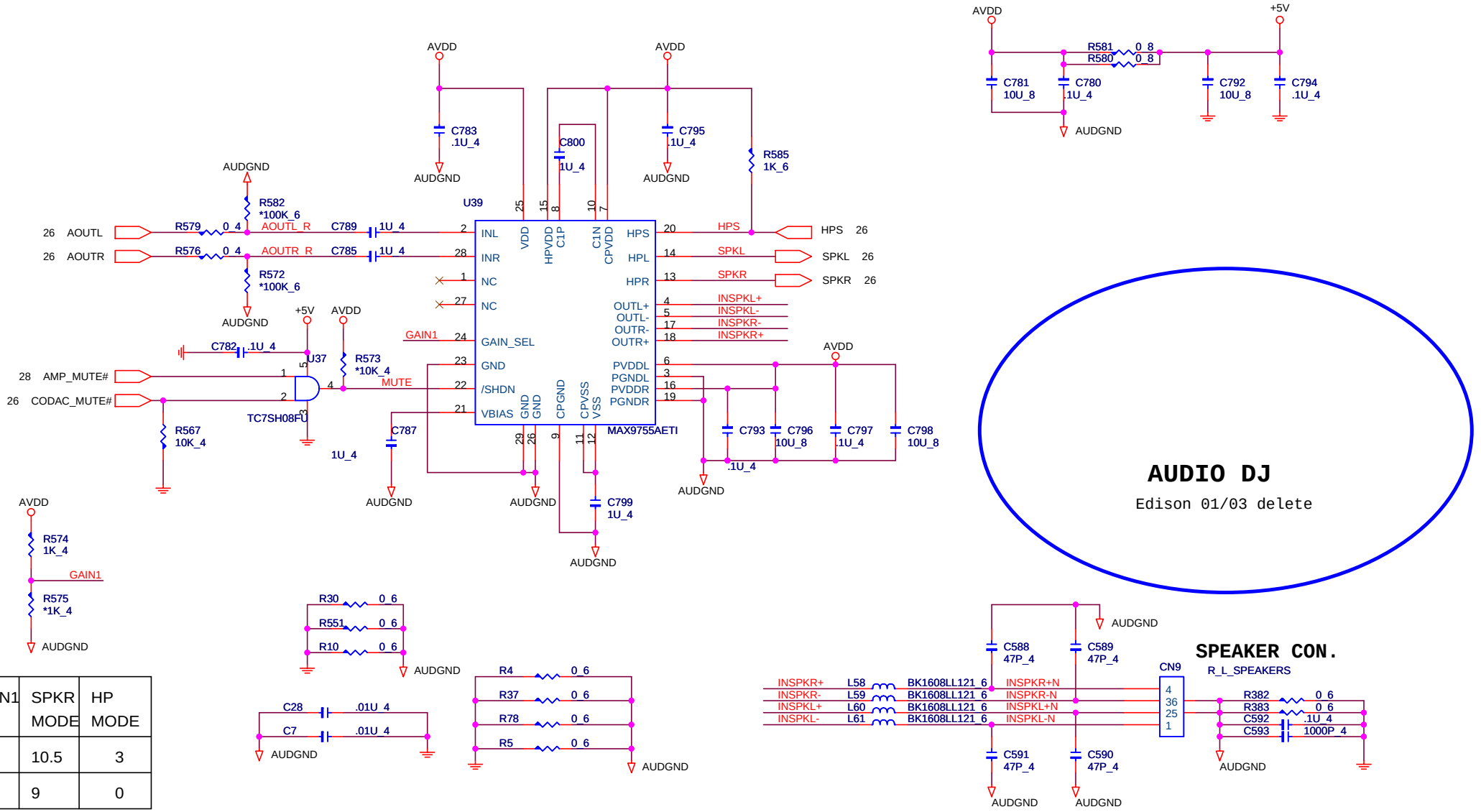
BEEP



PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	CODEC & LINE IN & MIC	1A
Date: Monday, April 03, 2006	Sheet 26 of 37	



AUDIO DJ

Edison 01/03 delete

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

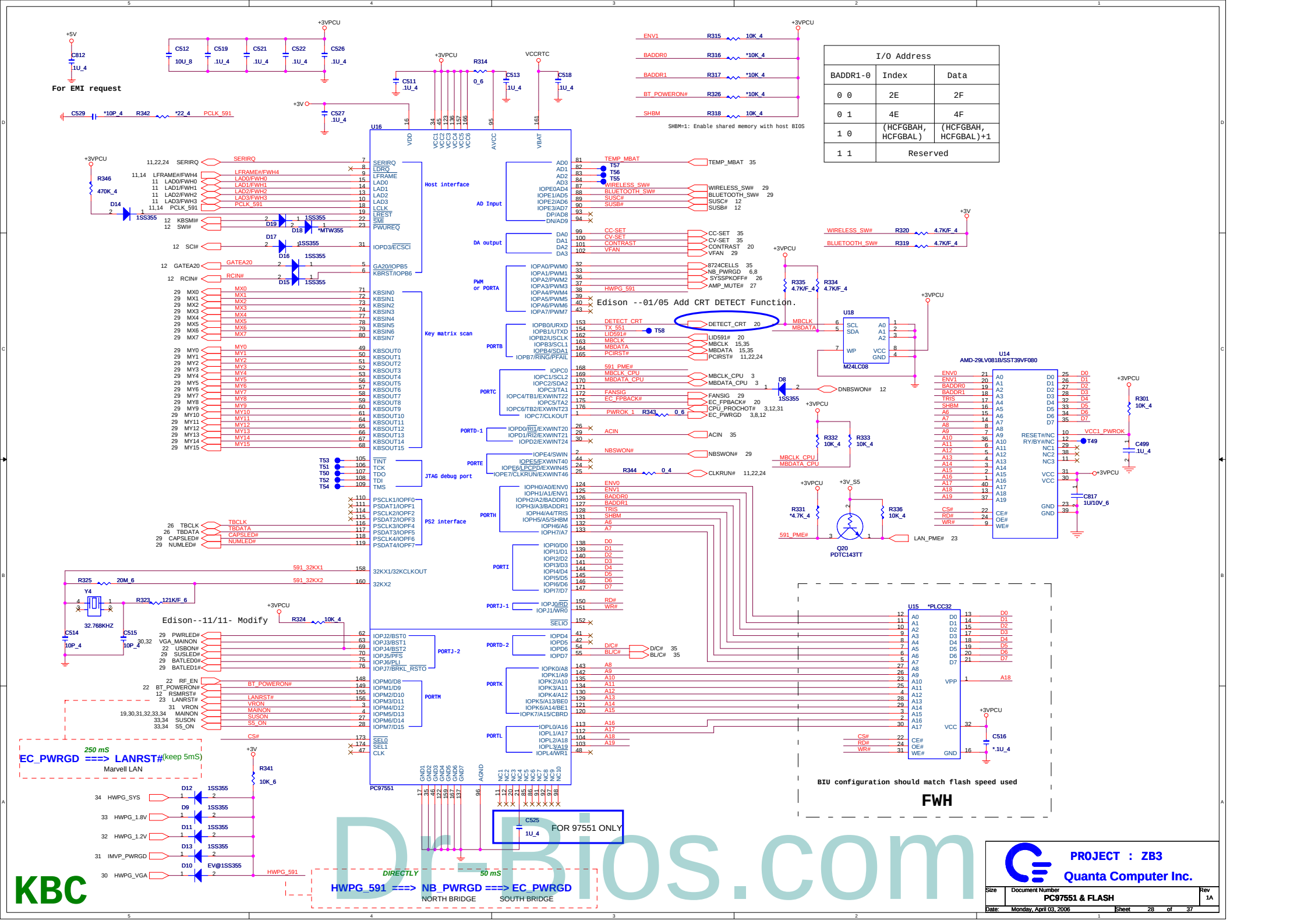
SPEAKER CON.

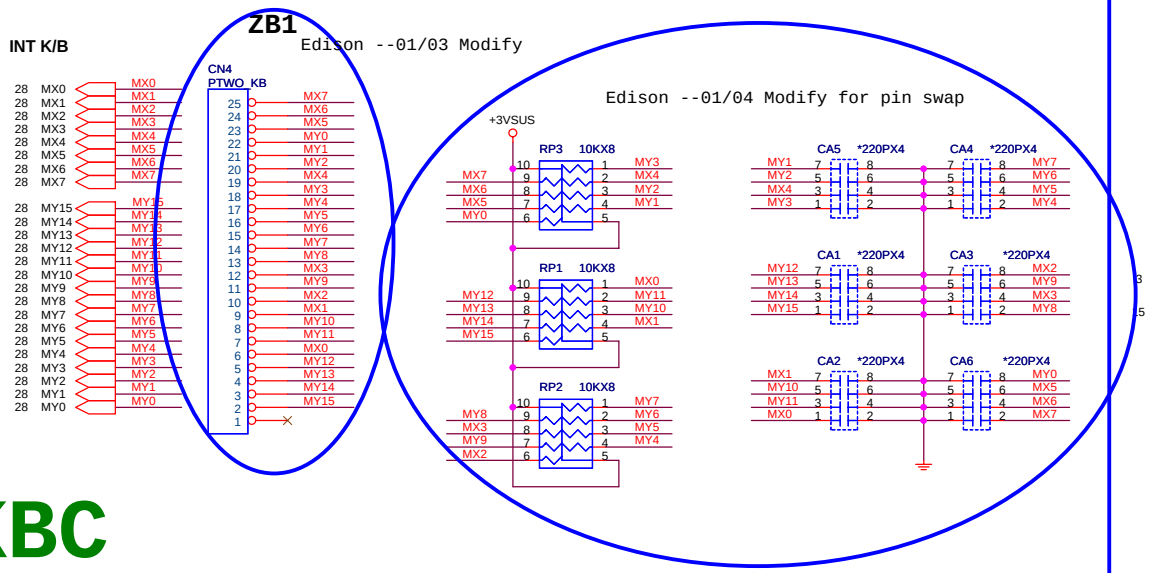
AMP

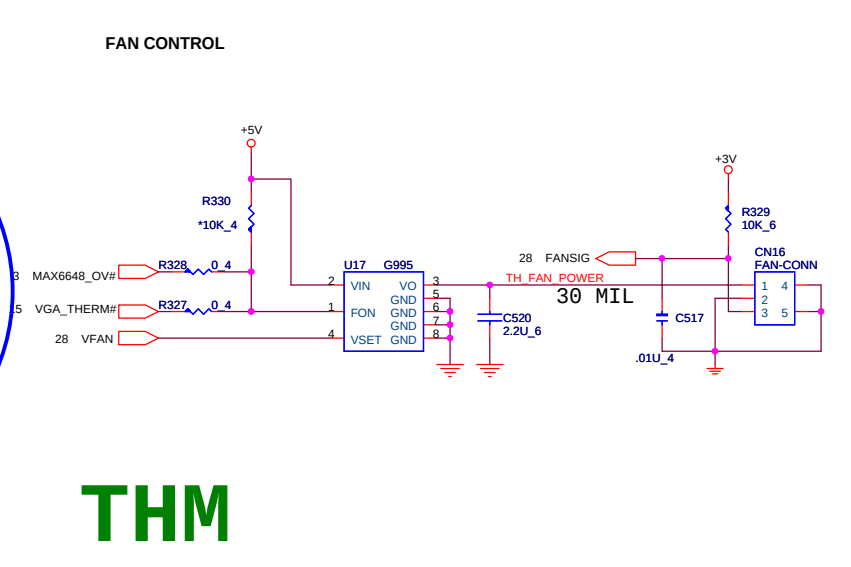
PROJECT : ZB3

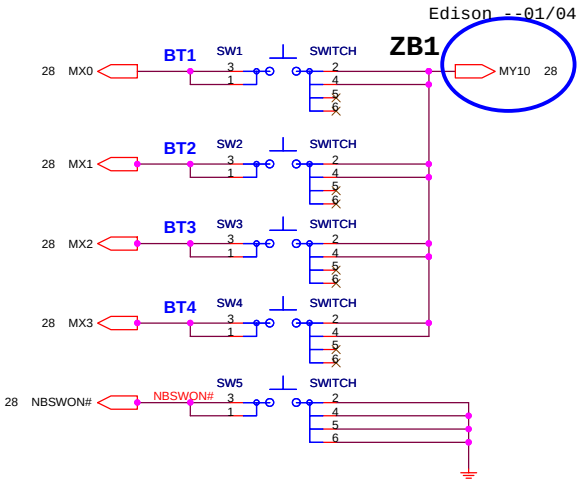
Quanta Computer Inc.

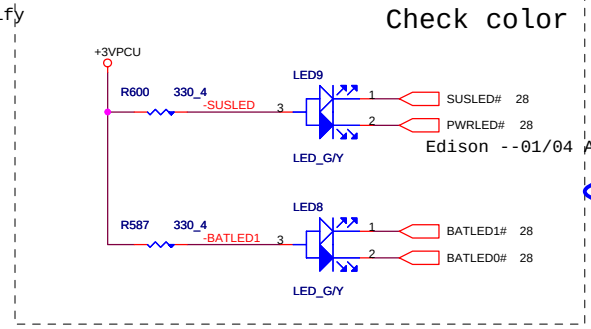
Size	Document Number	Rev
	AUDIO AMP	1A
Date: Monday, April 03, 2006	Sheet 27 of 37	

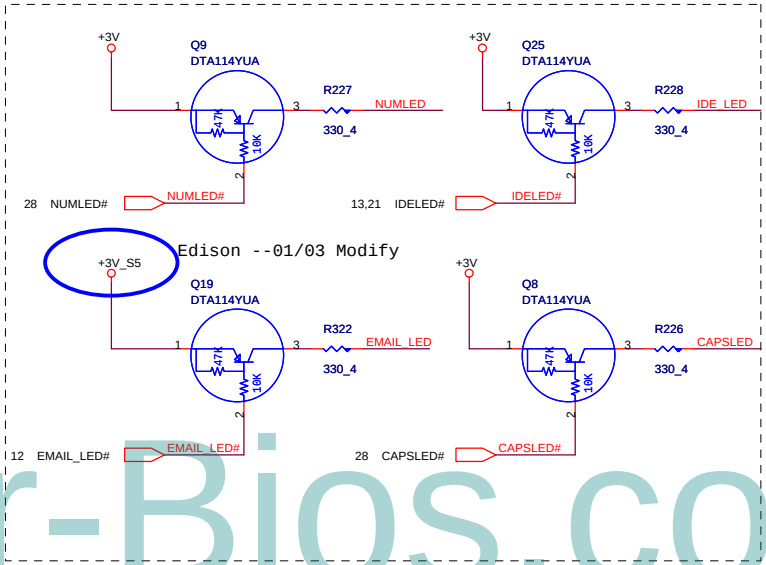

For EMI request
U16
PC97551
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
Edison --01/05 Add CRT DETECT Function.
Edison--11/11- Modify
U18
M24LC08
U14
AMD-29LV081B/SST39VF080
U15 *PLCC32
Q20
PDTC143TT
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
SHBM=1: Enable shared memory with host BIOS
BIU configuration should match flash speed used
FWH
FOR 97551 ONLY
EC_PWRGD ===> LANRST# (keep 5mS)
Marvell LAN
HWPG_591 ===> NB_PWRGD ===> EC_PWRGD
NORTH BRIDGE
SOUTH BRIDGE
KBC
PROJECT : ZB3
Quanta Computer Inc.
PC97551 & FLASH
Monday, April 03, 2006
Sheet 28 of 37

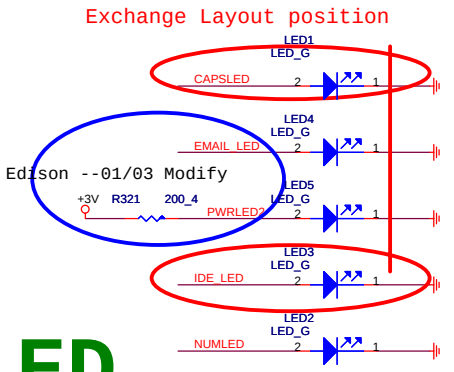


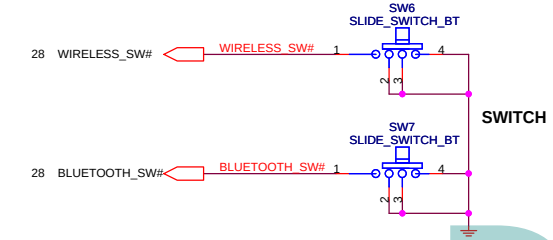






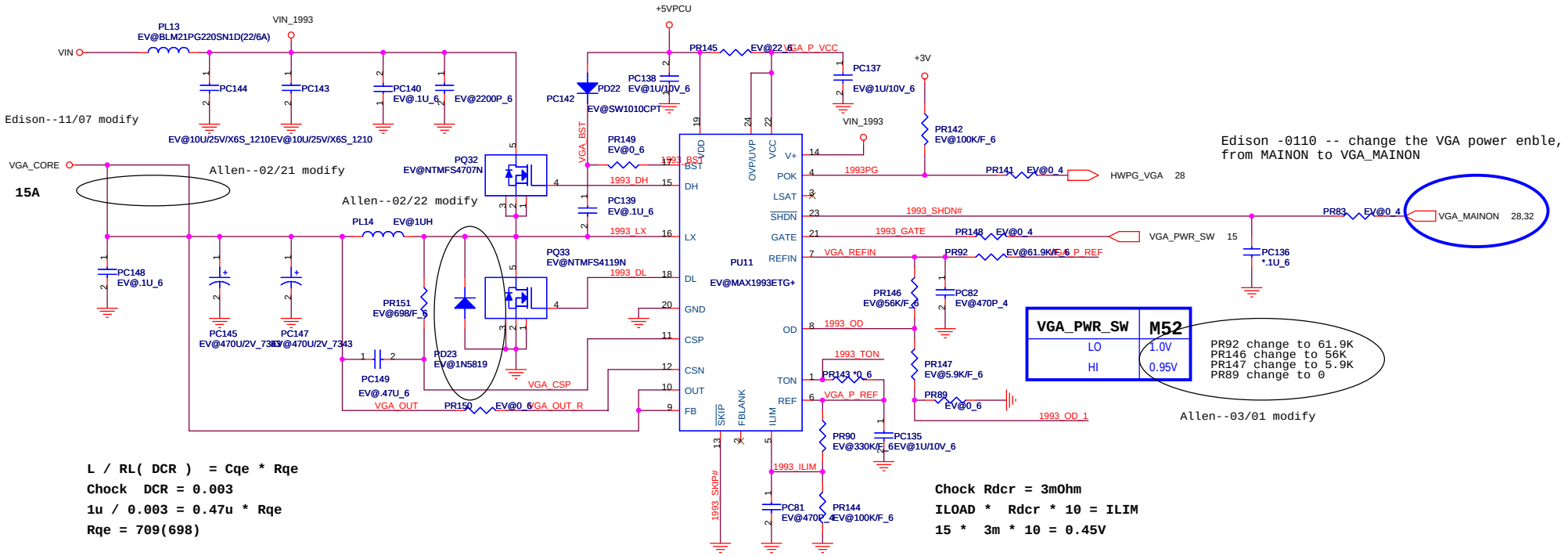






PROJECT : ZB3
Quanta Computer Inc.

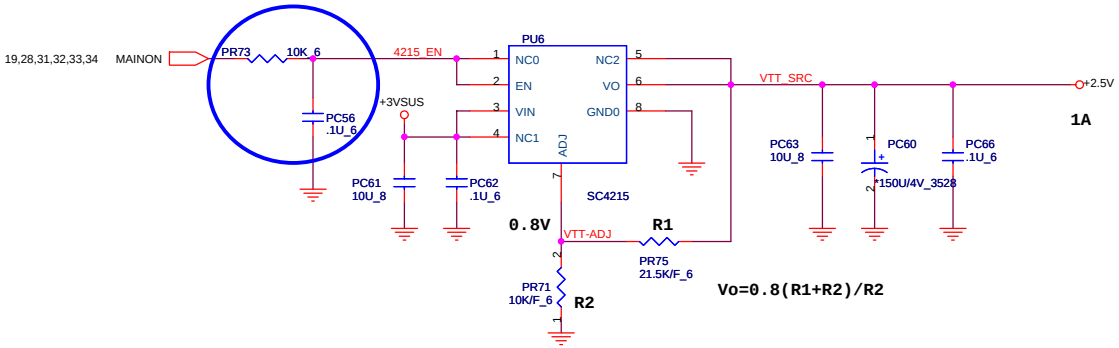
Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	1A
Date: Monday, April 03, 2006	Sheet 29 of 37	



L / RL(DCR) = Cqe * Rqe
Chock DCR = 0.003
1u / 0.003 = 0.47u * Rqe
Rqe = 709(698)

Chock Rdcr = 3mOhm
ILOAD * Rdcr * 10 = ILIM
15 * 3m * 10 = 0.45V

+2.5v delay 1ms for VGA power-up sequence --Arec 0113

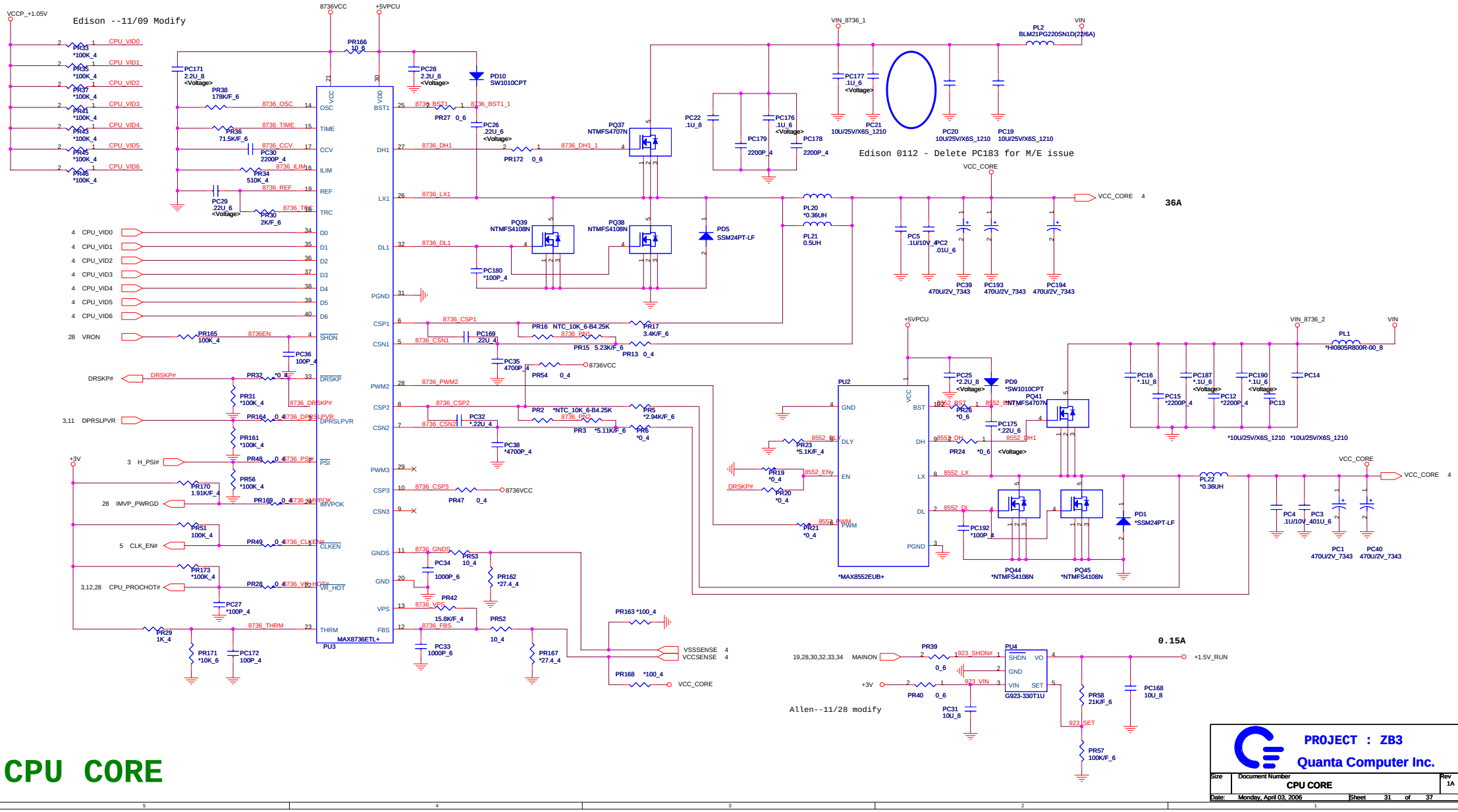


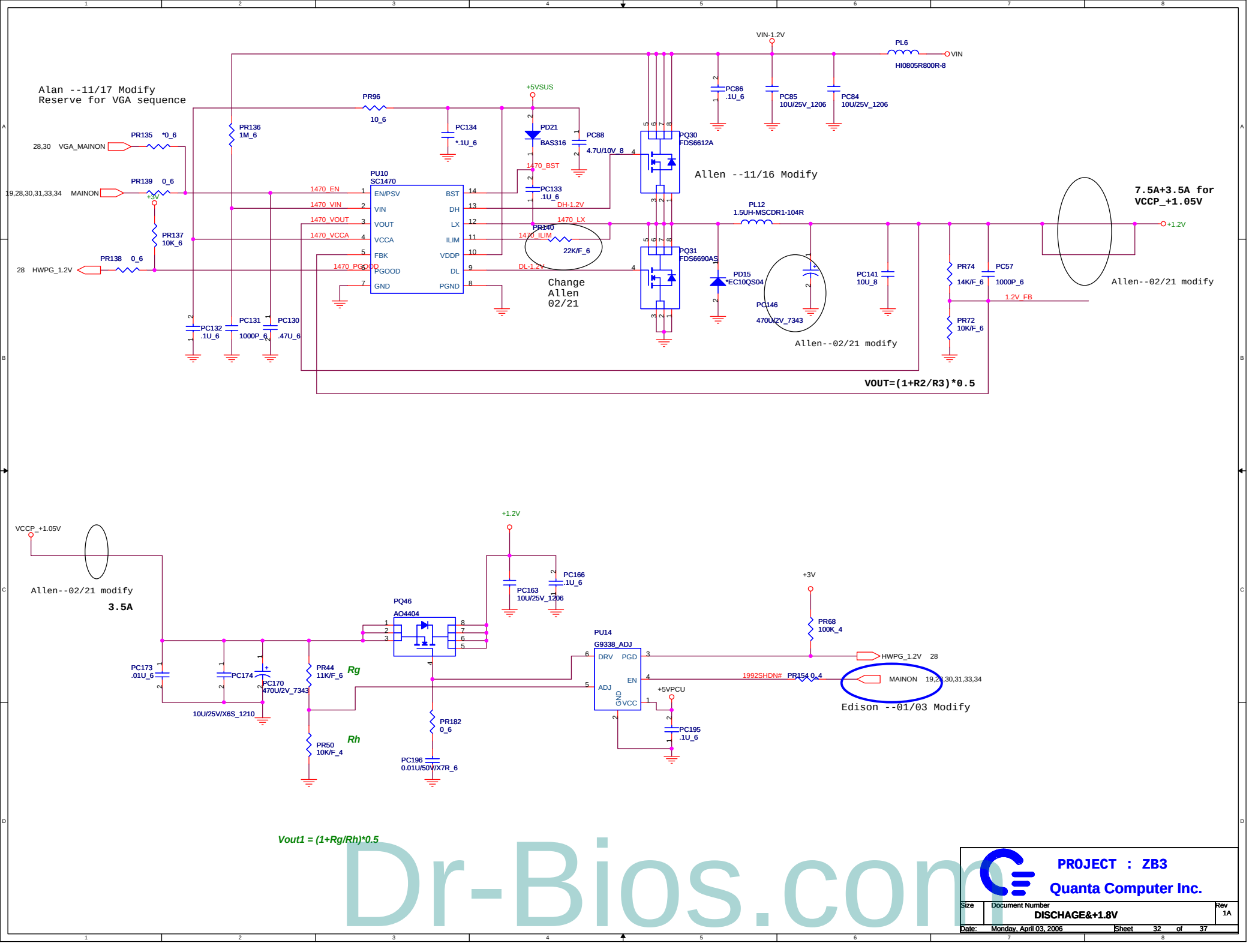
VGA CORE

PROJECT : ZB3
Quanta Computer Inc.

Size	Document Number	Rev
	VGA CORE	1A

Date: Monday, April 03, 2006 Sheet 30 of 37

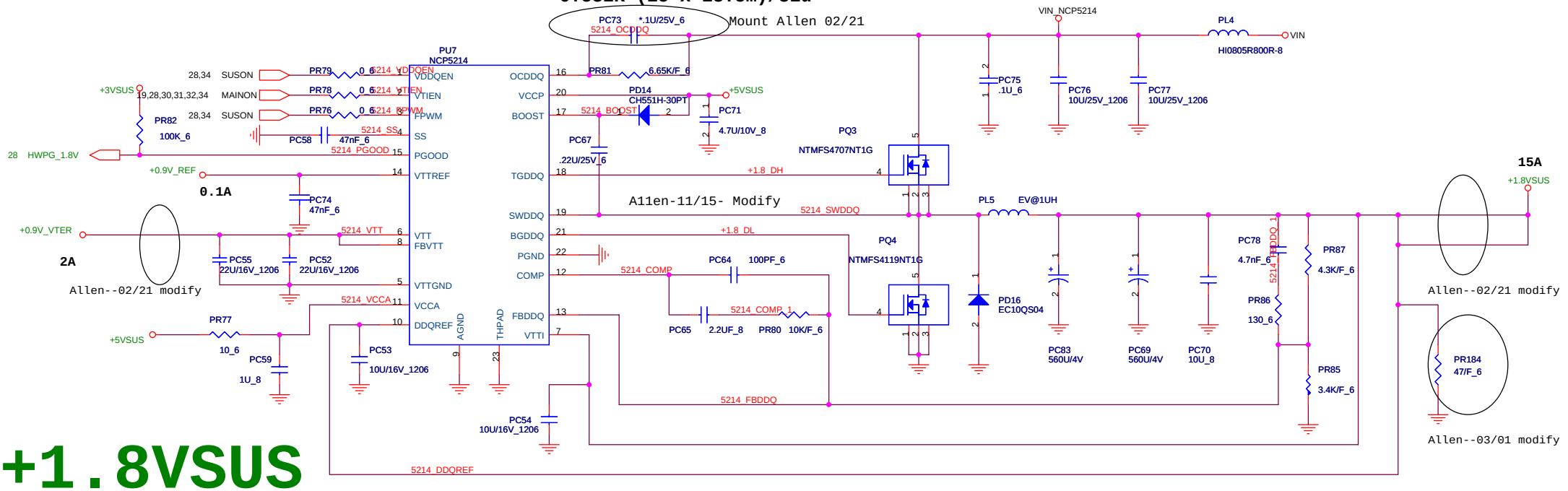

Edison --11/09 Modify
Edison 0112 - Delete PC183 for M/E issue
Allen--11/28 modify
36A
0.15A
MAX8736ETL+
*MAX8552EUB+
G923-330T1U
CPU CORE
PROJECT : ZB3
Quanta Computer Inc.
CPU CORE
Monday, April 03, 2006
Sheet 31 of 37



PROJECT : ZB3		
Quanta Computer Inc.		
Size	Document Number: DISCHAGE&+1.8V	Rev: 1A
Date: Monday, April 03, 2006	Sheet 32 of 37	

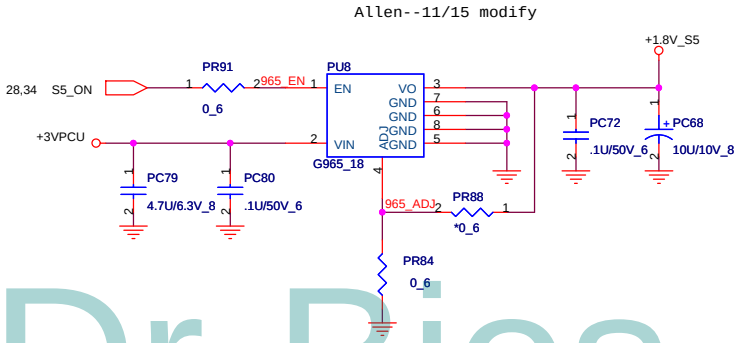
RL1=(Ilim x Rdson-h)/IOC(31uA)

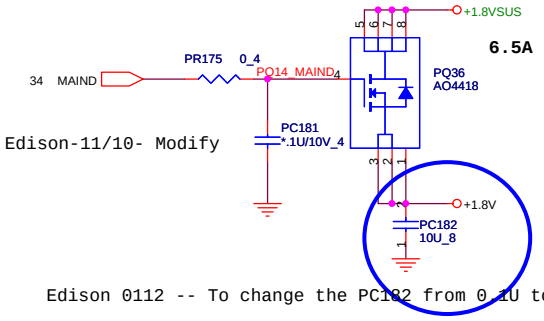
6.532K=(15 x 13.5m)/31u



+1.8VSUS

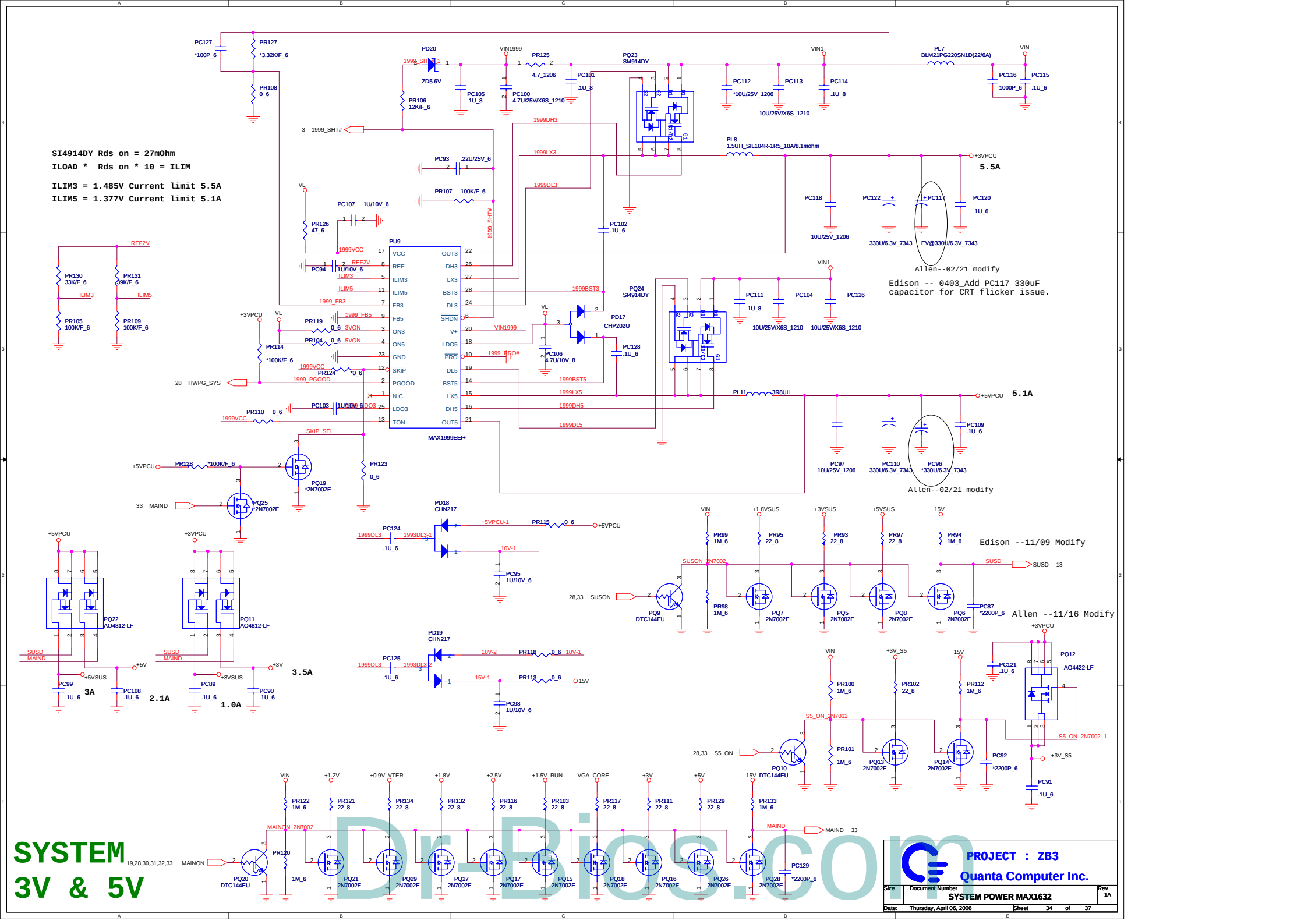
DDR Power & NB Power

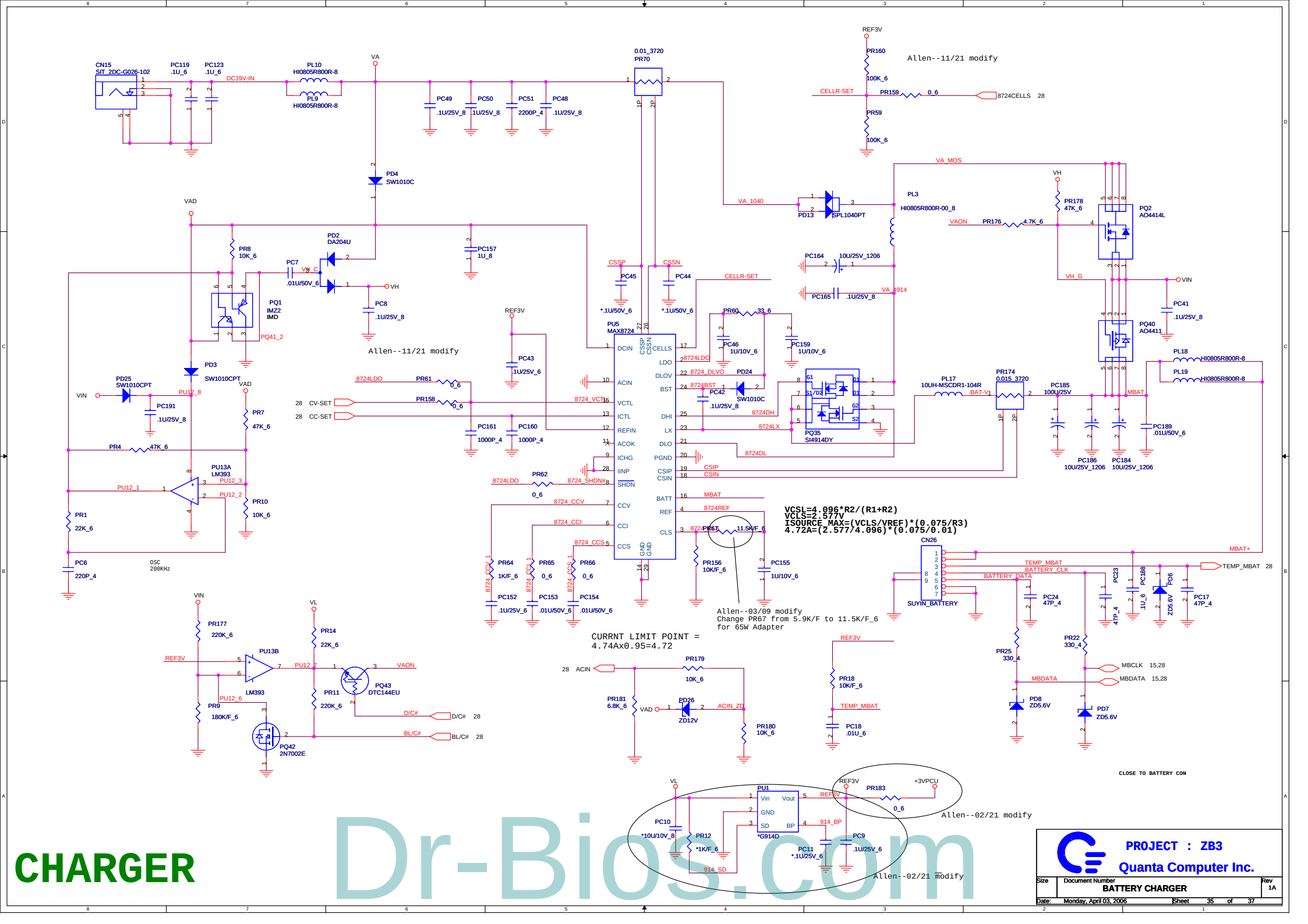




Edison 0112 -- To change the PC182 from 0.1U to 10uF_0805

PROJECT : ZB3		
Quanta Computer Inc.		
Size	Document Number: SMDDR_VTERM&+1.2V&+1.8VSUS	Rev: 1A
Date: Monday, April 03, 2006	Sheet 33 of 37	


SI4914DY Rds on = 27mOhm
ILOAD * Rds on * 10 = ILIM
ILIM3 = 1.485V Current limit 5.5A
ILIM5 = 1.377V Current limit 5.1A
PU9
MAX1999EEI+
PQ23 SI4914DY
PQ24 SI4914DY
PL8 1.5UH_SIL104R-1R5_10A/8.1mohm
PL11 3R8UH
PL7 BLM21PG220SN1D(22/6A)
5.5A
5.1A
Allen--02/21 modify
Edison -- 0403_Add PC117 330uF capacitor for CRT flicker issue.
Edison --11/09 Modify
Allen --11/16 Modify
3A
2.1A
1.0A
3.5A
SYSTEM
3V & 5V
PROJECT : ZB3
Quanta Computer Inc.
SYSTEM POWER MAX1632
Thursday, April 06, 2006
Dr-Bios.com


CHARGER
Allen--11/21 modify
Allen--11/21 modify
Allen--03/09 modify
Change PR67 from 5.9K/F to 11.5K/F_6
for 65W Adapter
CURRNT LIMIT POINT =
4.74Ax0.95=4.72
VCSL=4.096*R2/(R1+R2)
VCLS=2.577V
ISOURCE_MAX=(VCLS/VREF)*(0.075/R3)
4.72A=(2.577/4.096)*(0.075/0.01)
Allen--02/21 modify
Allen--02/21 modify
CLOSE TO BATTERY CON
PROJECT : ZB3
Quanta Computer Inc.
BATTERY CHARGER
Monday, April 03, 2006
Sheet 35 of 37
Dr-Bios.com