

Compal Confidential

Model Name : A5WAH/A5WAB

File Name : LA-B991P

Compal Confidential

EA50_HB M/B Schematics Document

Intel Broadwell ULT (Broadwell + Wildcat point)

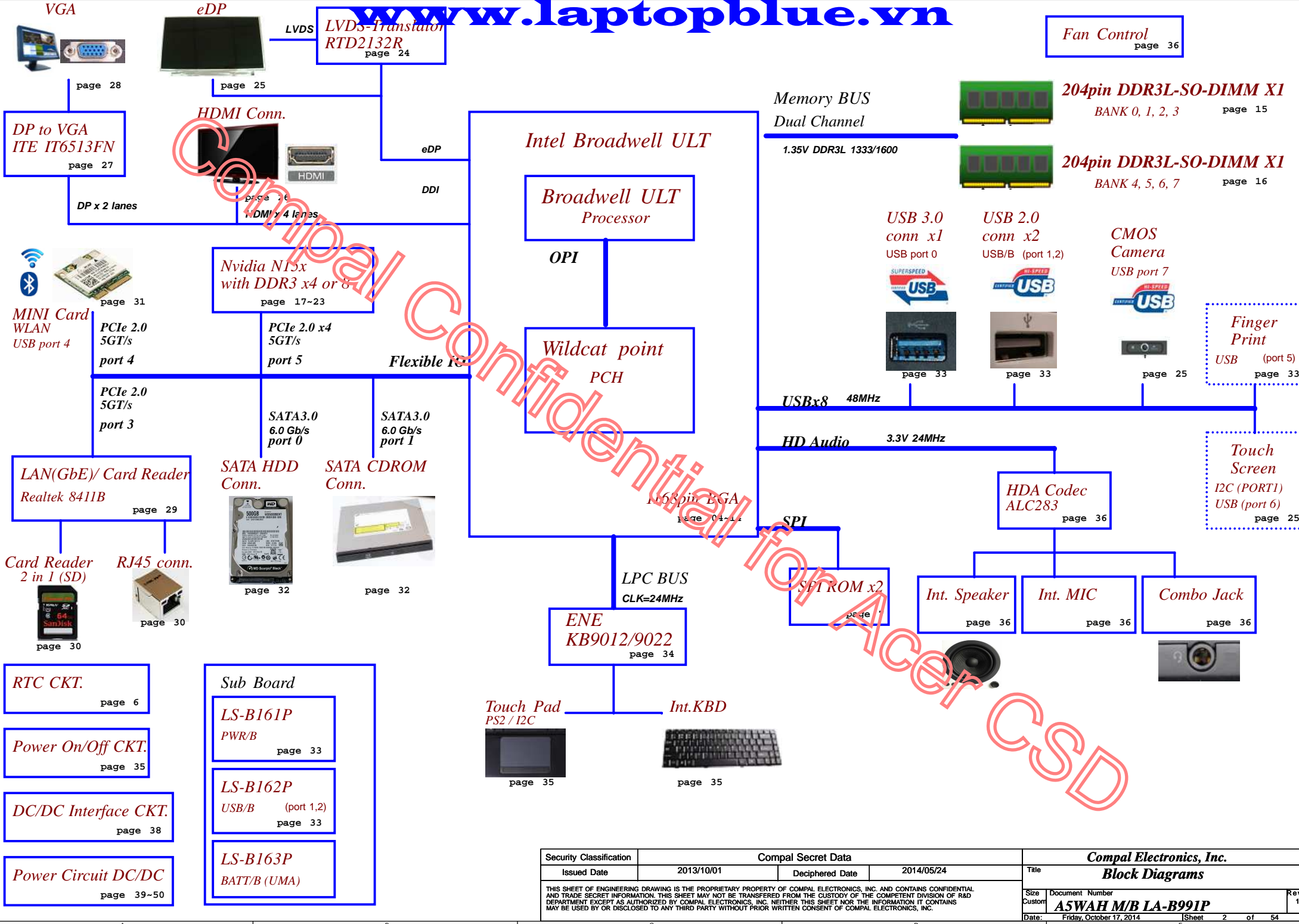
Nvidia N15S-GT / N15V-GM / N15V-GL

2014-08-27

REV:1.0

Compal Confidential for Acer CSD

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Title		Block Diagrams					
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for USB3	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power.	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

	S1	S3	S5	ALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0x16	On Board Thermal Sensor	0x96
		VGA Internal Thermal Sensor	0x9E

EC SM Bus2 address

PCH SM Bus address

Device	Address
ChannelA DIMM0	1010 0000 JDIMM1
ChannelB DIMM1	1010 0010 JDIMM2

USB Port Table

USB 2.0	Port	3 External USB Port
	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
EHCI1	3	
	4	Mini Card (WLAN+BT)
	5	Touch Screen
	6	Camera
	7	Finger Print
USB 3.0	Port	
	0	USB Port(Left 3.0)
XHCI	1	
	2	
	3	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMA@
GPU	VGA@
On Board HDD	HDD@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
TPM Module	TPM@
G-Sensor	BA@
Redriver HDD	BA@
Touch Screen	TS@
VRAM Selection	X76@
DGPU IDEN	VGL@, VGM@, SGT@
CPU IDEN	HW@, BW@
GC 2.0	GC6@
One GC6	NGC6@
One MIC	EA50@
Two MIC	2MIC@

BOARD ID Table

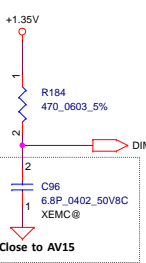
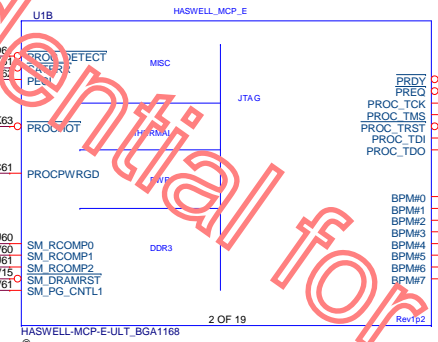
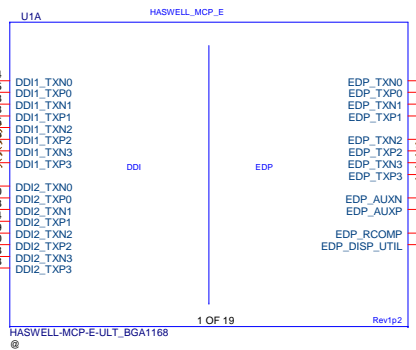
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

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DP to CRT

FDMI

eDP Panel



DDR3 Compensation on 5 grds
Trace width=12-15 mils, Spacing=20 mils
Max trace length= 500 mil

PVT2 ,Replace I3-4030 to I3-4020

U1 CPU_Haswell intel PMD3558U 1.7G 3558@ SA00007G260	U1 CPU_Haswell intel I3-4030 1.9G 4030@ SA00007TA60	U1 CPU Haswell Intel I5-4200U 1.6G 4200@ SA00006SMB0	U1 CPU Haswell Intel I3-4010U 1.7G 4010@ SA00006SX70
U1 CPU_Haswell intel I5-4210 1.7G 4210@ SA00007LO70	U1 CPU_Haswell intel I7-4510 2G 4510@ SA00007M760	U1 CPU Haswell Intel I7-4500U 1.8G 4500@ SA00006SLB0	U1 CPU_Haswell intel I3-4158U 2G 4158@ SA00006VW40
U1 CPU_Haswell intel I3-4020 1.9G 4020@ SA00007MG50	U1 CPU_Haswell intel PMD3556U 1.7G 3556@ SA00007Y70	U1 CPU_Haswell intel I7-4550U 1.5G 4550@ SA00006SJA0	U1 CPU_Haswell intel PDC2957 1.4G 2957@ SA00007G060
ZZZ	U1 CPU Boardwell intel QG21 1.2G QG21@ SA00007OS10	U1 CPU Boardwell intel QG22 1.2G QG22@ SA00007OT10	U1 CPU Boardwell intel QGH9 1.8G QGH9@ SA00007U920
			U1 CPU Boardwell intel QGHA 1.6G QGHA@ SA00007UG20

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U1C

HASWELL_MCP_E



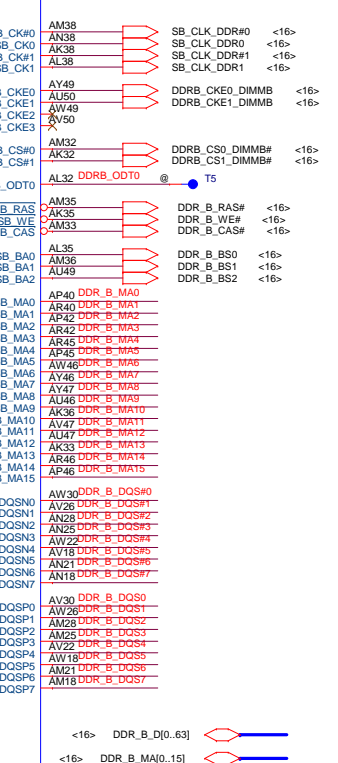
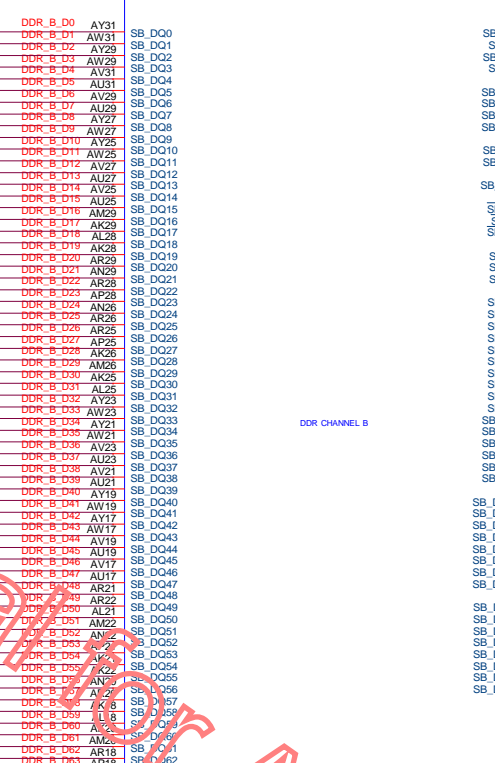
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HASWELL-MCP-E-ULT_BGA1168

U1D

HASWELL_MCP_E

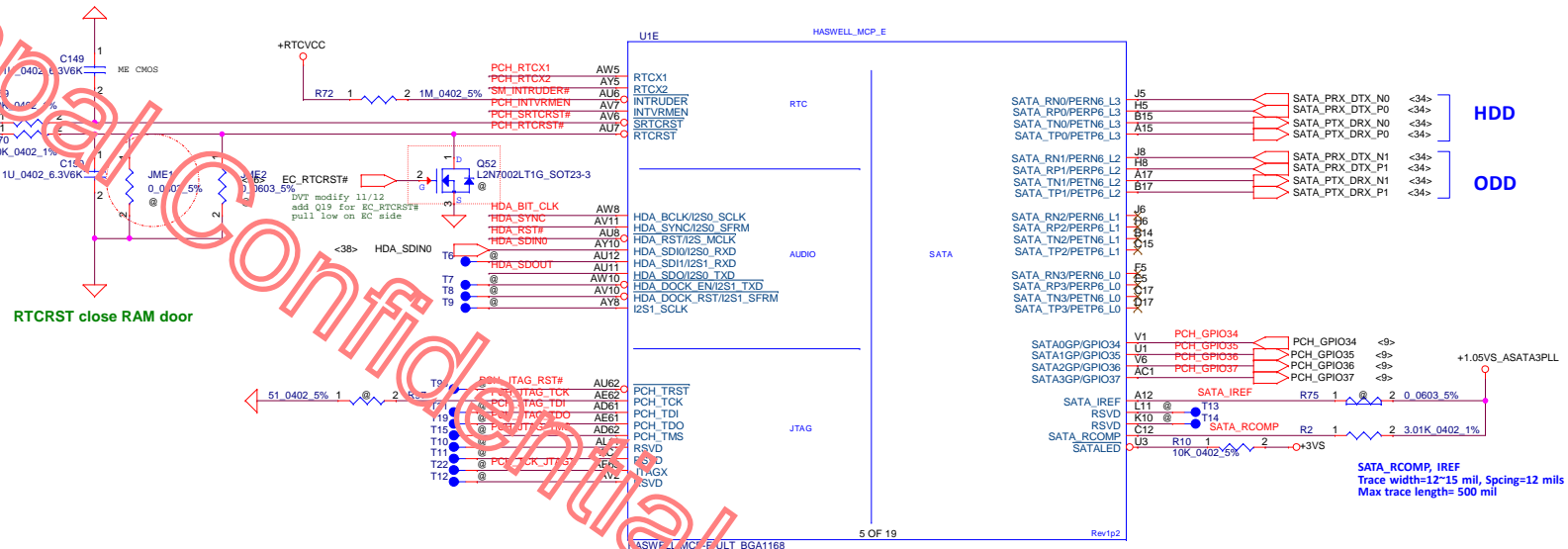
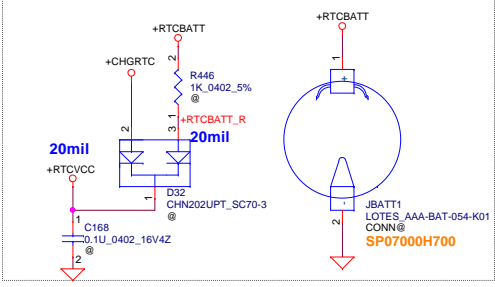
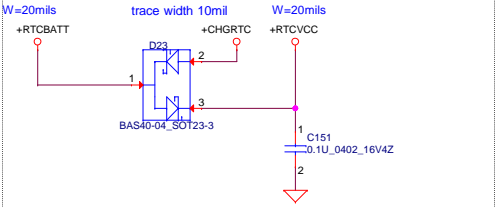
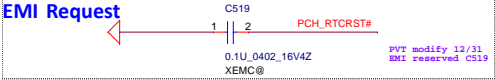
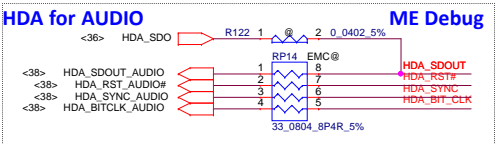
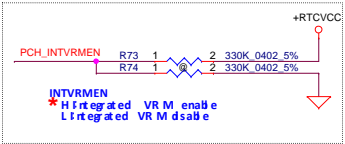
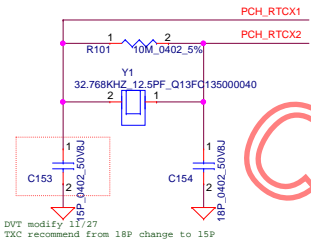


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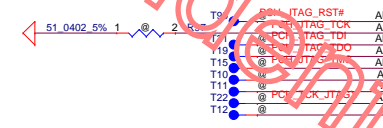
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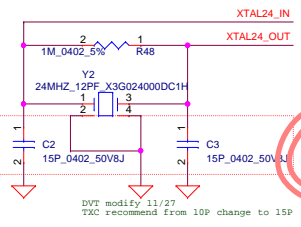
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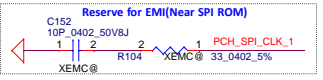
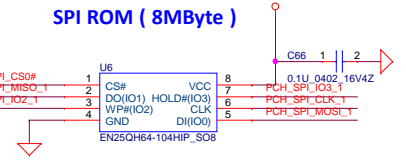
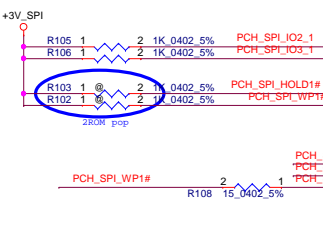
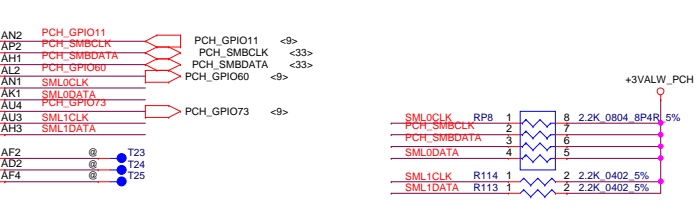
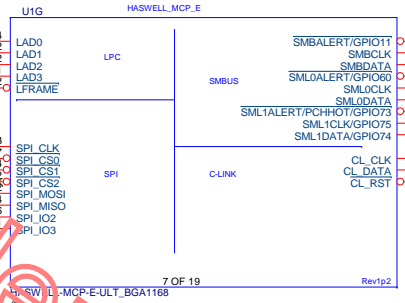
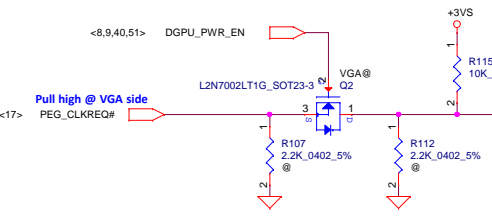
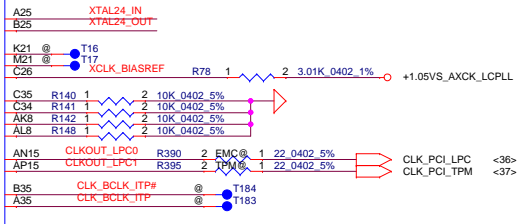
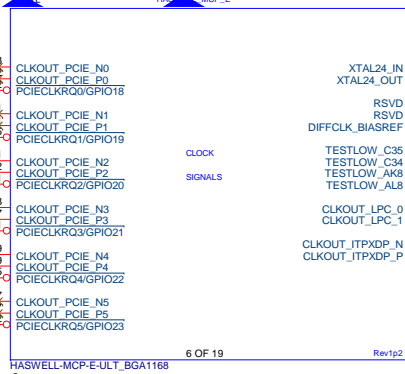
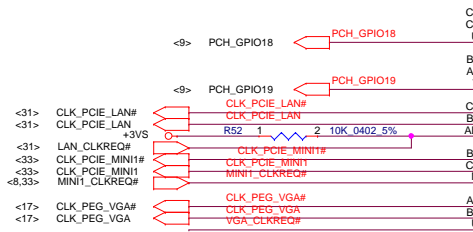
RTCRST close RAM door



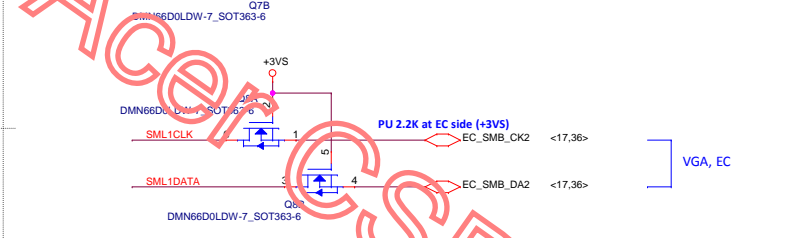
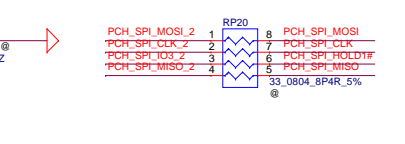
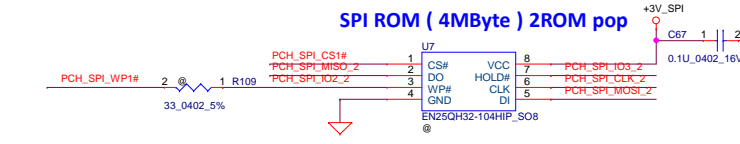
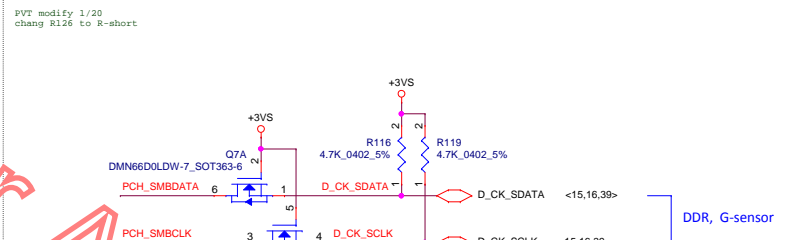
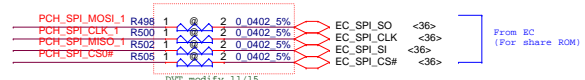
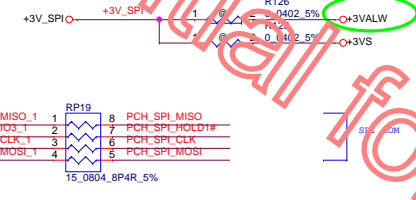
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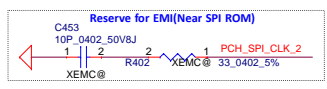
PCIE LAN
WLAN
VGA



for Share EC ROM, +3VS change to +3VALW

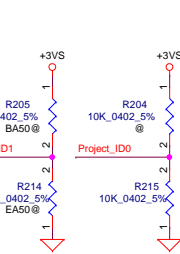
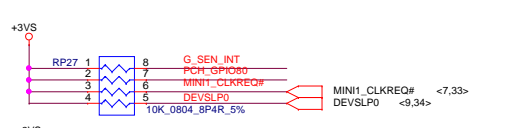
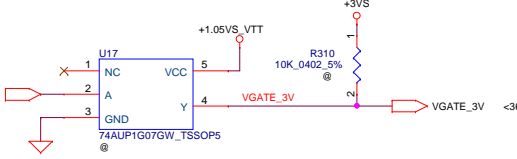
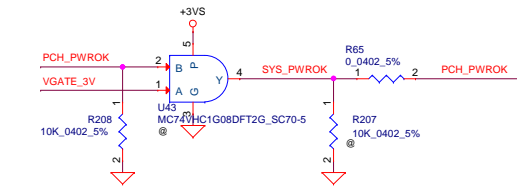
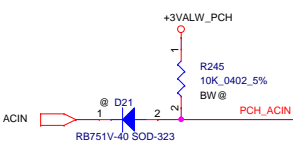
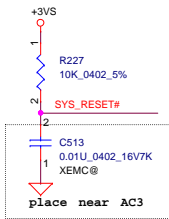


2ROM is SPI ROM 2M + 4M Byte
2ROM POP
U6 - EN25QH16-104HIP_S08 (SA00004UG00)
RP19 - 33_0804_8P4R_5% (SD309330A80)
R108 - 33_0402_5% (SD028330A80)

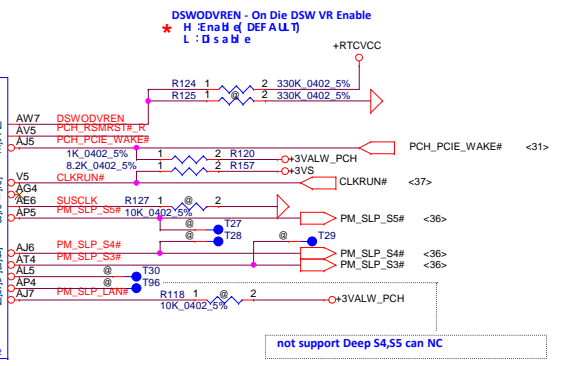
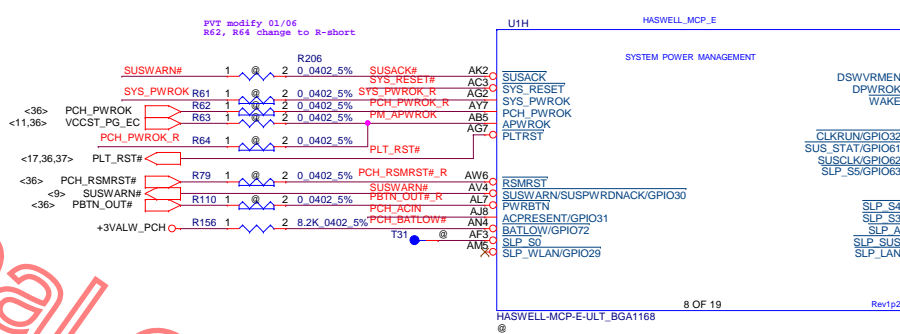


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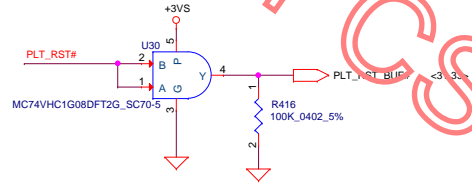
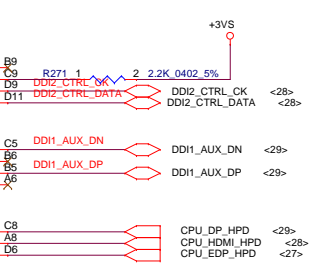
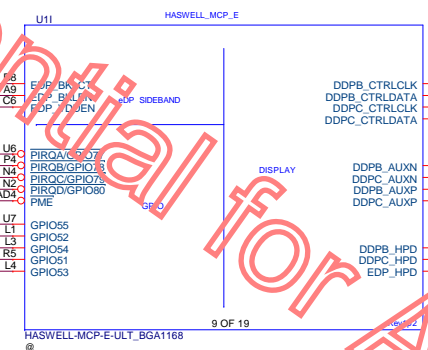


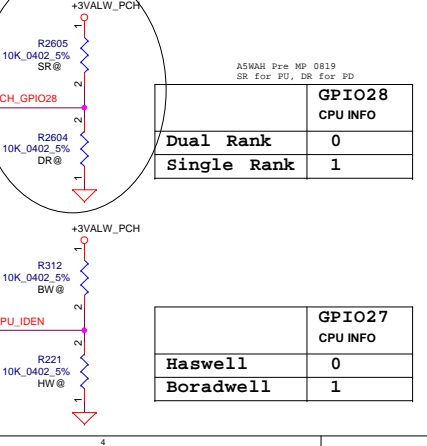
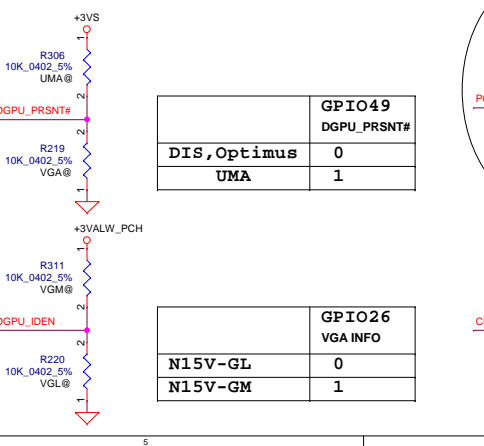
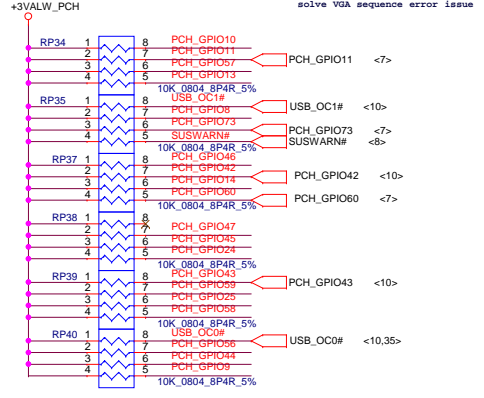
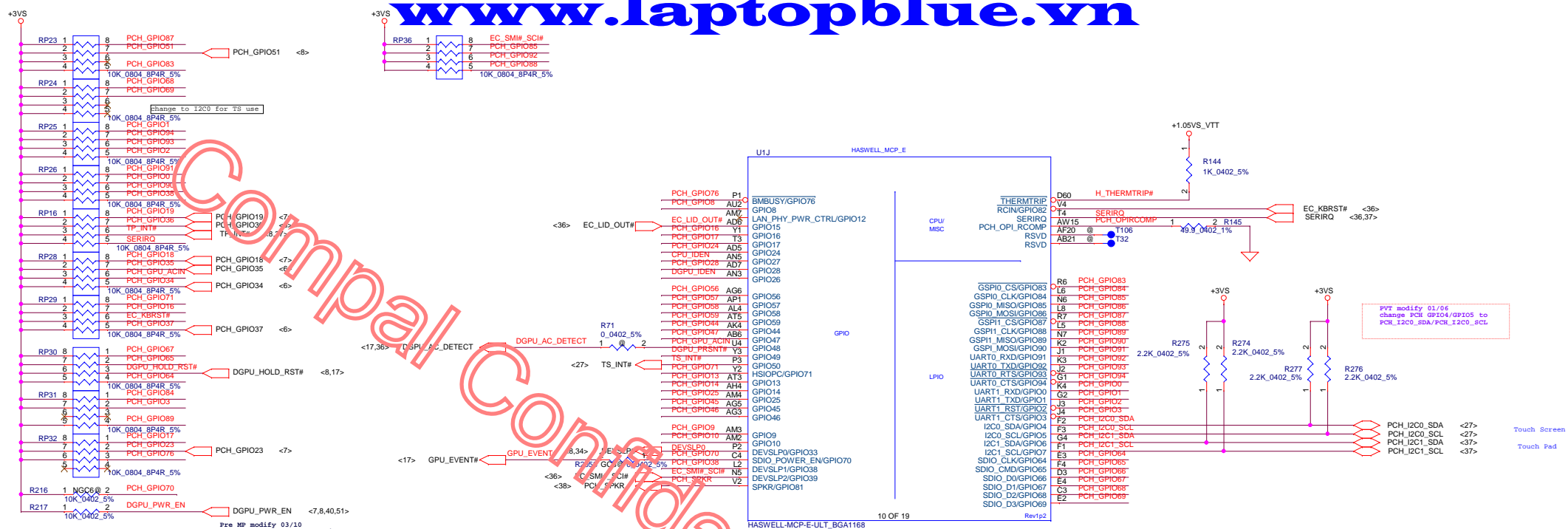
Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
*Z5WAH	0	0
Z5W1H	0	1
Z5WBH	1	0
Reserved	1	1



DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected

* 1: Port B or C is detected
0: Port B or C is not detected
(Have internal PD)





	GPIO49 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

	GPIO28 CPU INFO
Dual Rank	0
Single Rank	1

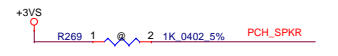
	GPIO26 VGA INFO
N15V-GL	0
N15V-GM	1

	GPIO27 CPU INFO
Haswell	0
Boradwell	1



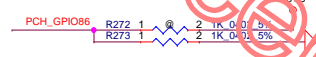
GPIO1 : TLS Confidential

1: ENABLED
* 0: DISABLED (Have internal PD)



SPKR / GPIO81 : NO REBOOT

1: ENABLED
* 0: DISABLED (Have internal PD)



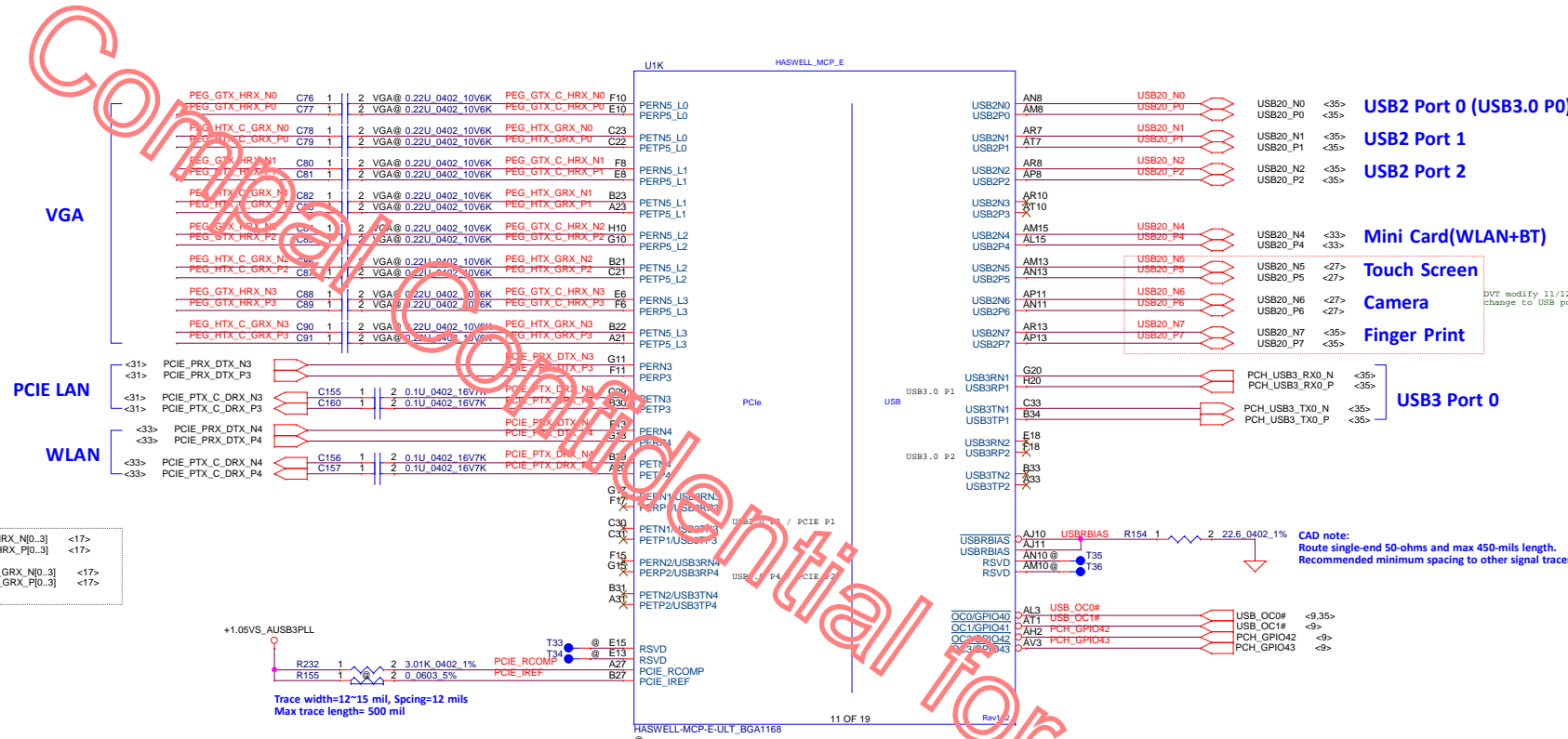
GPIO86 / GPIO86 : Boot BIOS Strap

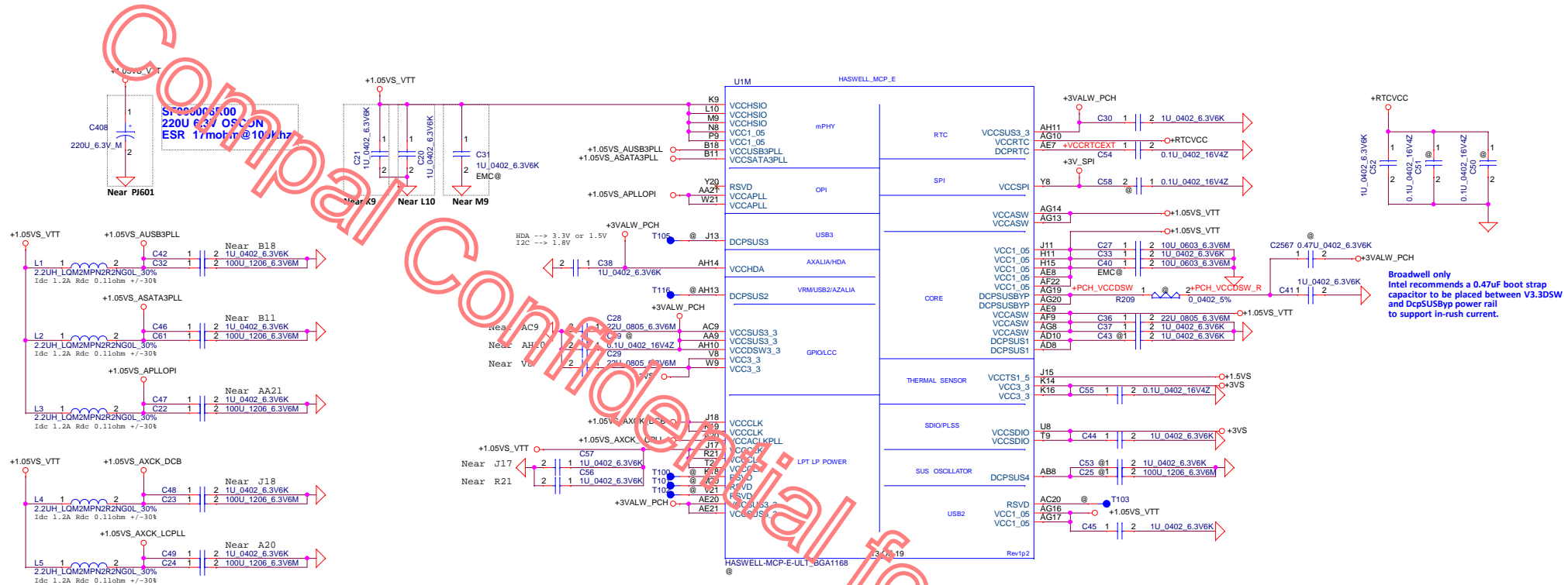
1: ENABLED
* 0: SPI ROM (Have internal PD)



SDIO_D0 / GPIO66 : Top-Block Swap Override

1: ENABLED
* 0: DISABLED (Have internal PD)





S-205J005F00
220U 6.3V OSCON
ESR 17mohm @10KHz

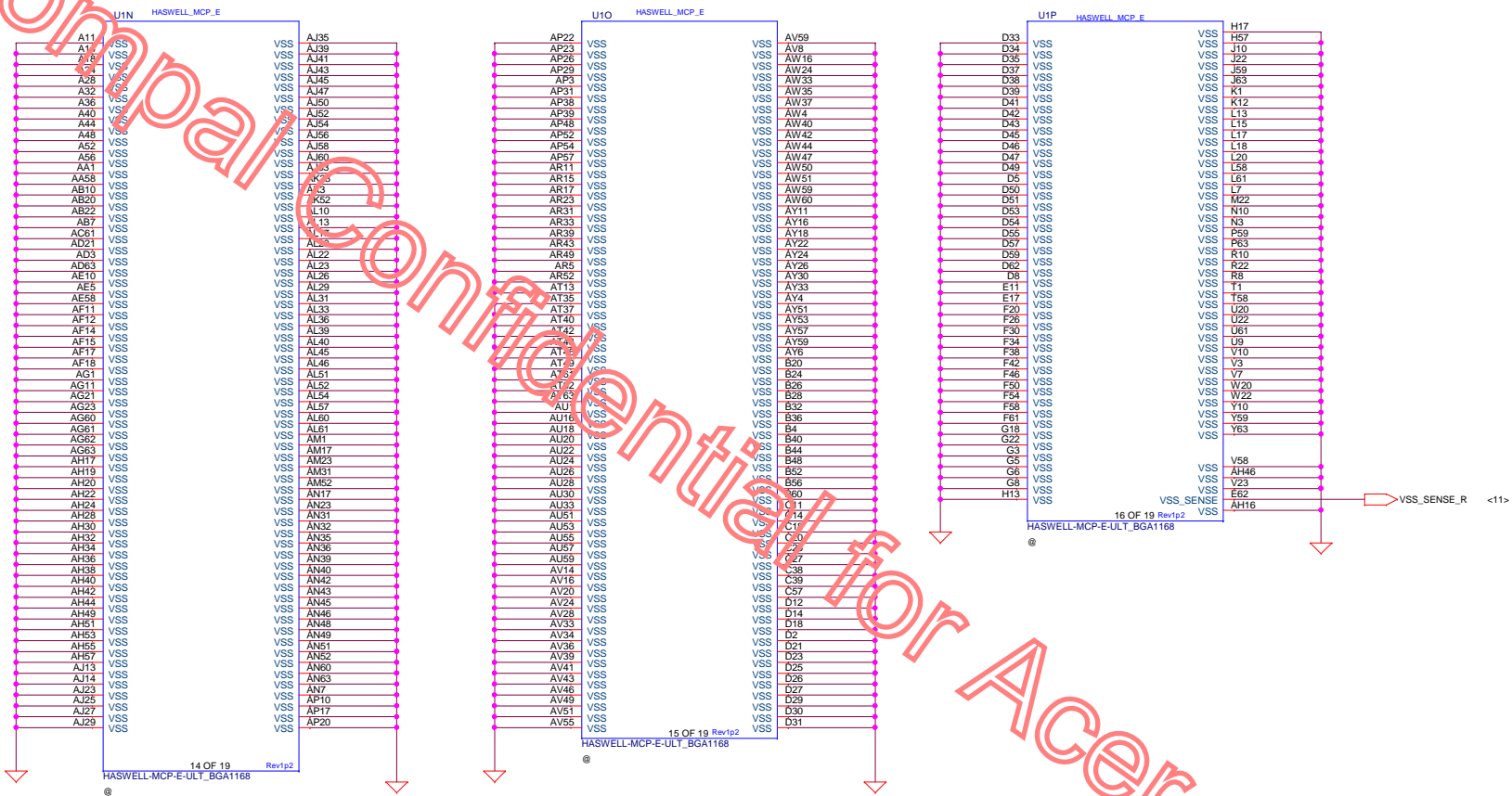
Broadwell only
Intel recommends a 0.47uF boot strap capacitor to be placed between V3.3DSW and DcpSUSByp power rail to support in-rush current.

**+3VALW TO +3VALW(PCH AUX Power)
Short J8 for PCH VCCSUS3.3**

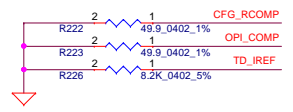
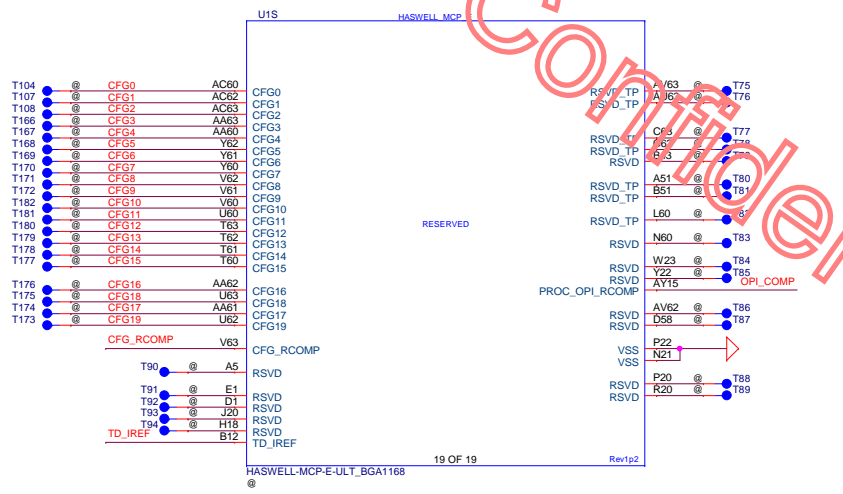
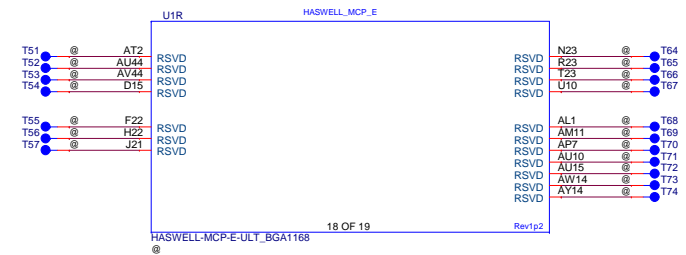
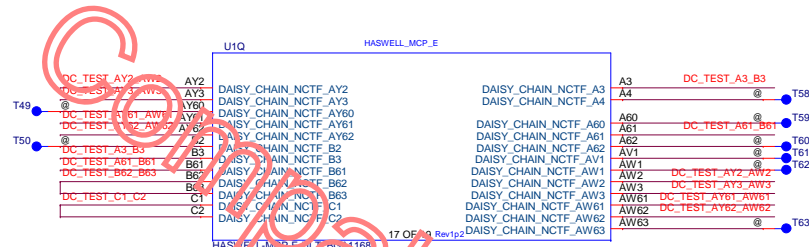


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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title BDW MCP(9/11) Power	
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Date:	Friday, October 17, 2014	Sheet	12	of	54
Rev	1.0				

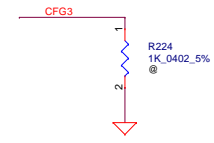
Confidential for Acer CSD



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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title
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Size	Document Number	Rev	1.0	
Custom	ASWAH M/B LA-B991P	Date:	Friday, October 17, 2014	Sheet 13 of 54

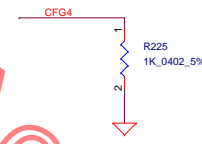


CFG Straps for Processor



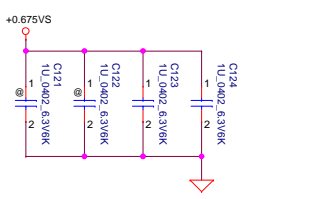
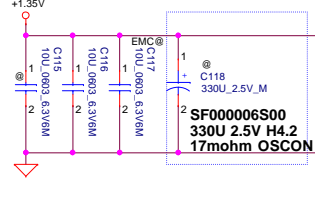
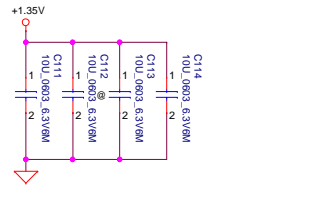
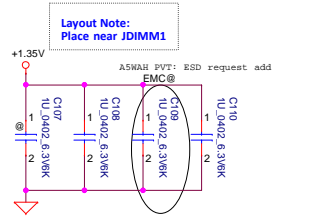
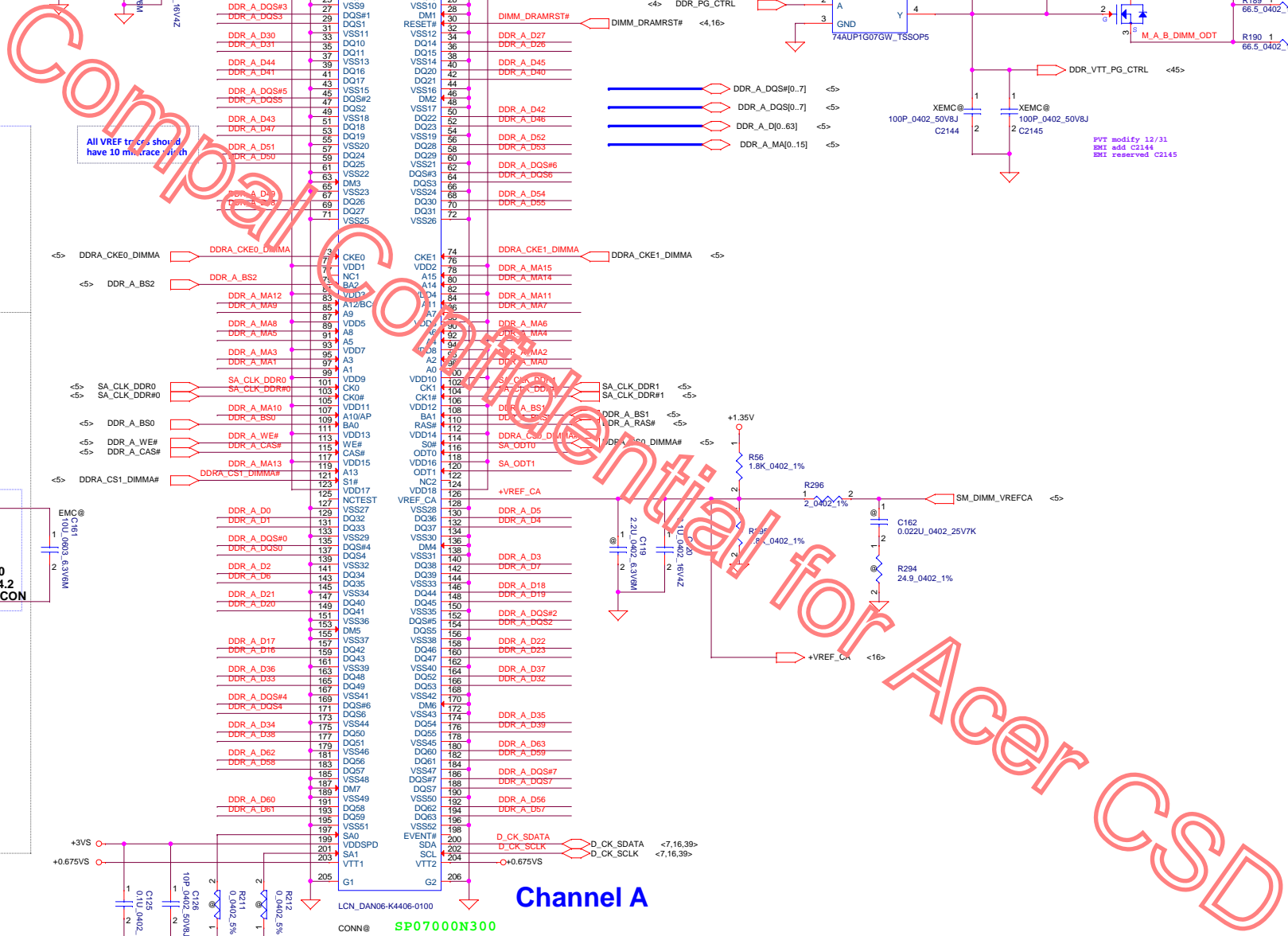
Physical Debug Enable (DFX Privacy)

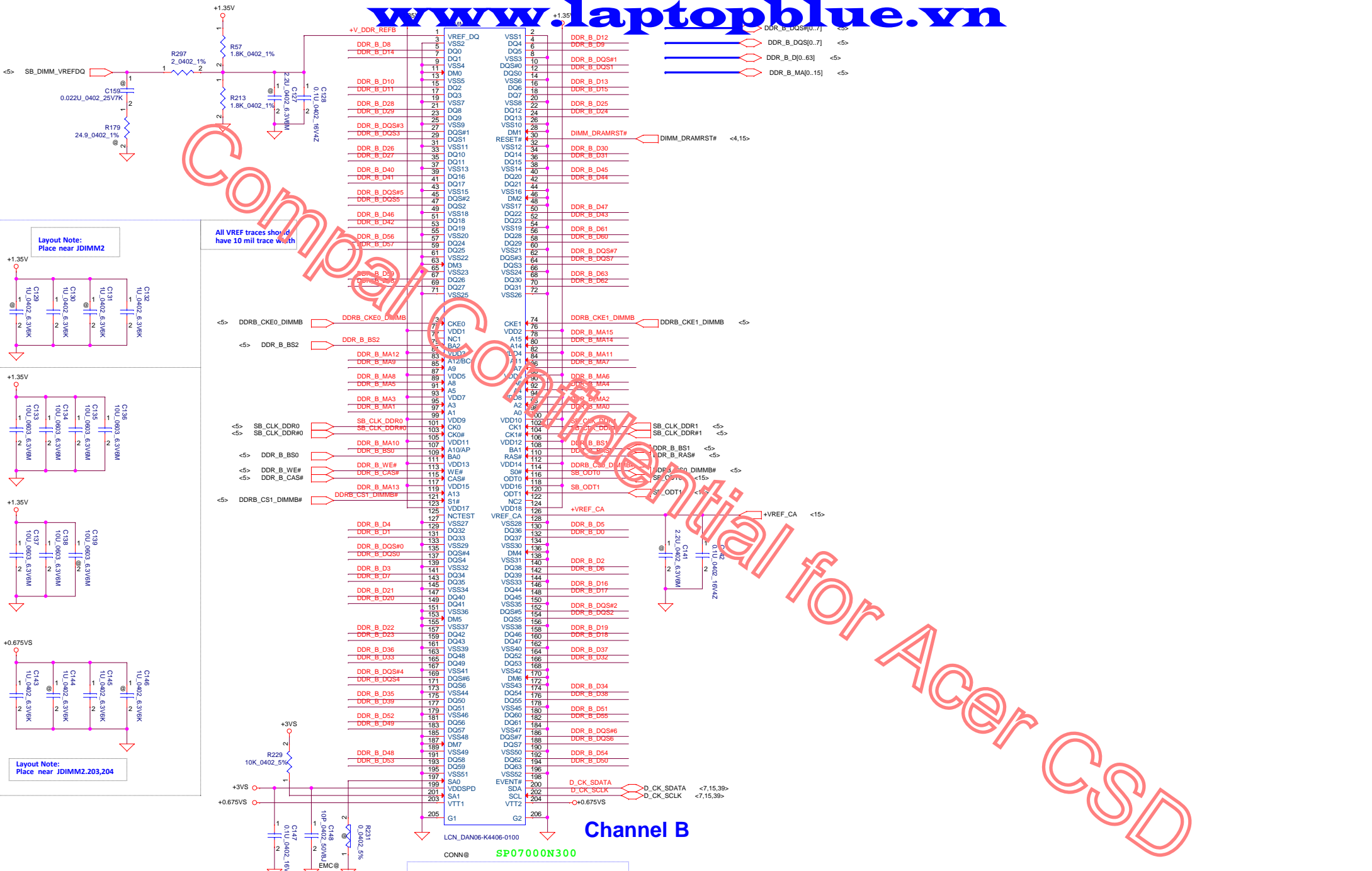
CFG3	1: DISABLED
	0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

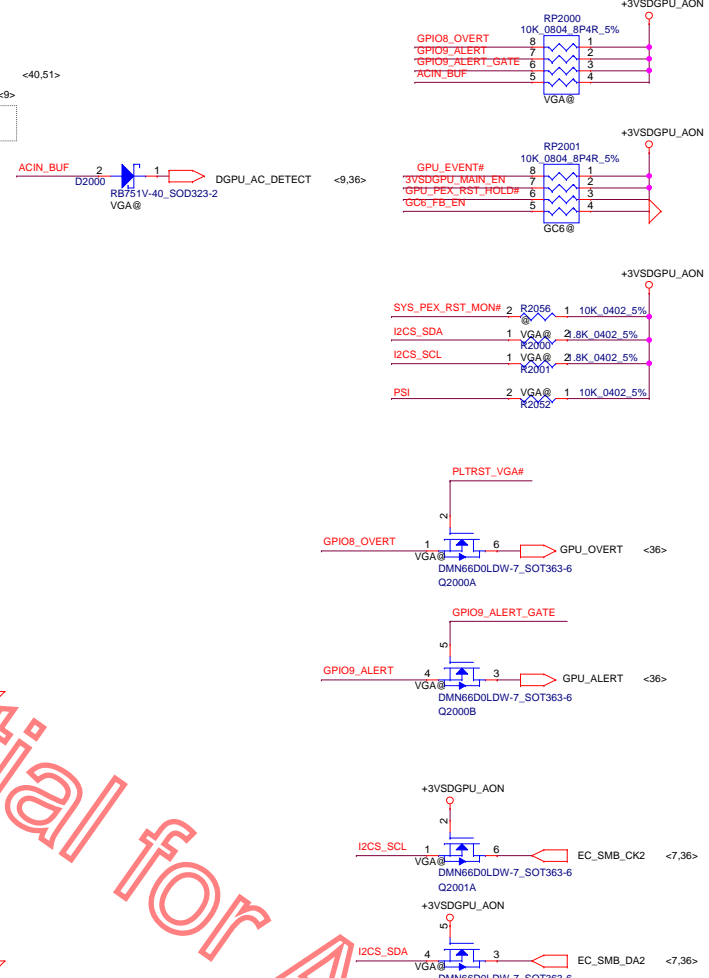
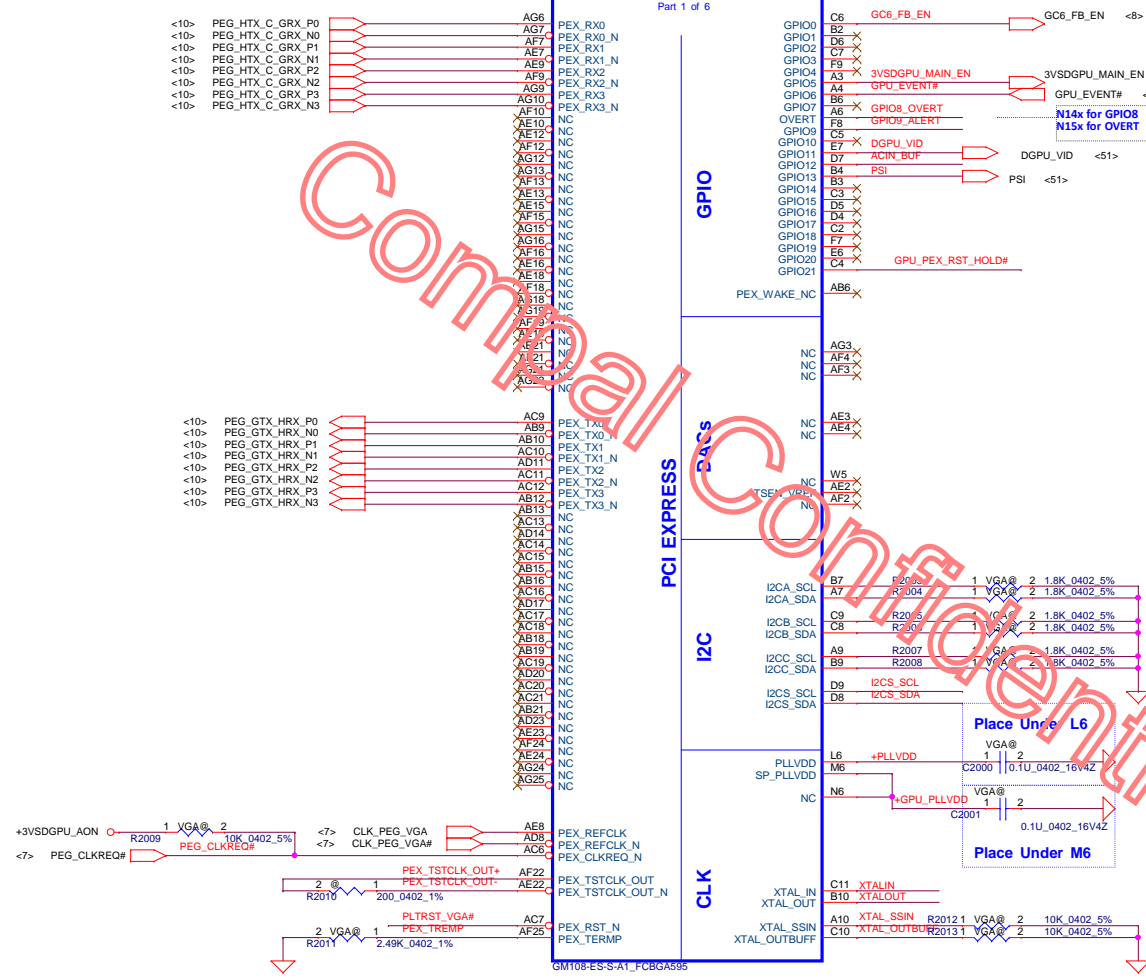


Display Port Presence Strap

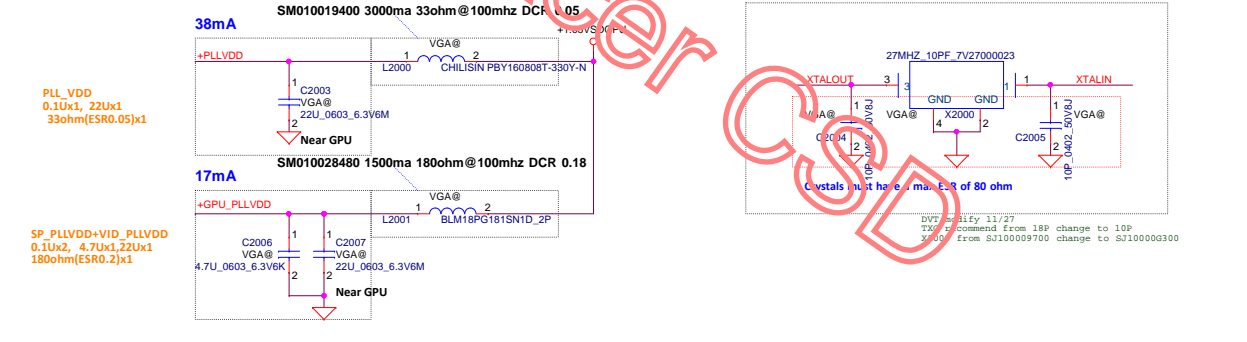
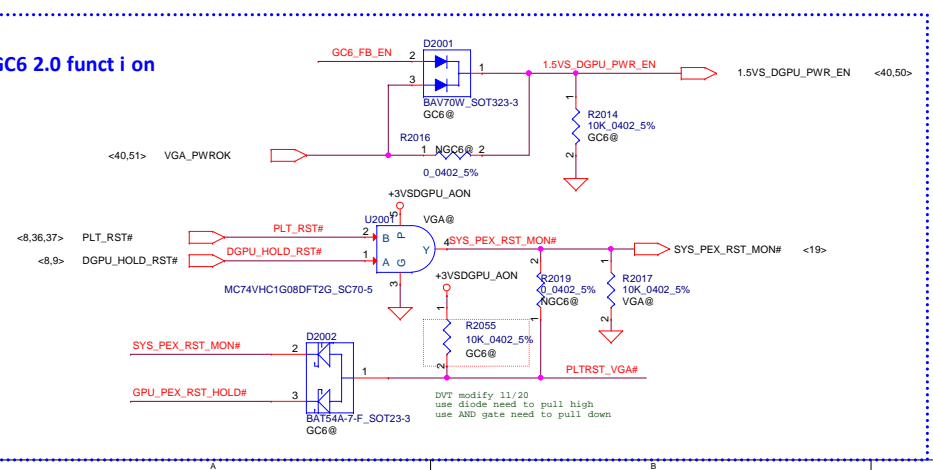
CFG4	1: Disabled, Physical Display Port at Embedded Display Port
	0: Enabled, no external Display Port, there is connected to the Embedded Display Port







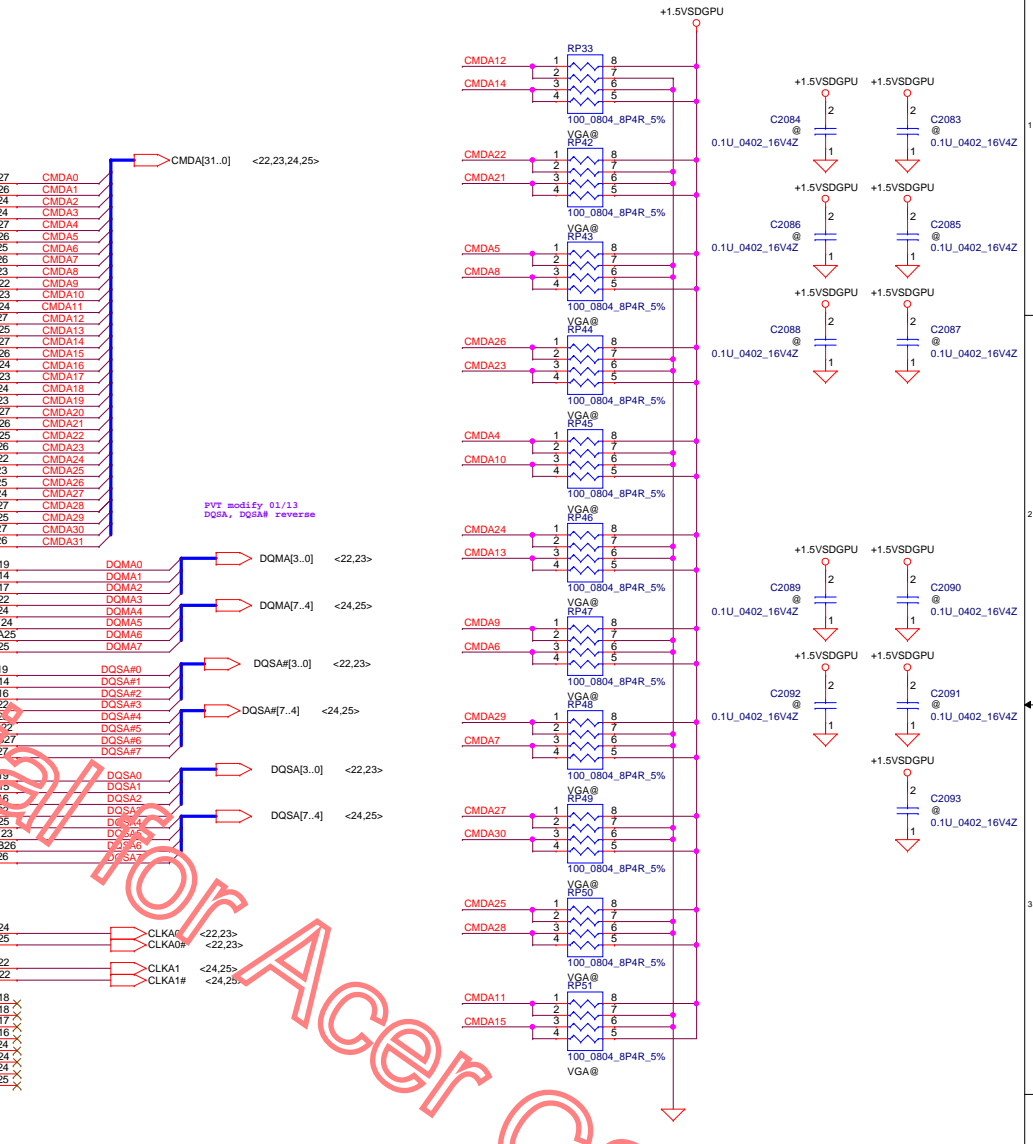
GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		



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Size	Custom	Document Number	ASWAH M/B LA-B991P	Rev	1.0
Date:	Friday, October 17, 2014	Sheet	17	of	54

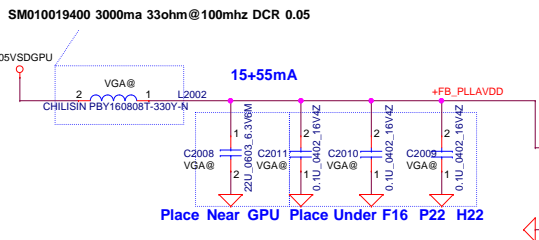
VRAM Interface

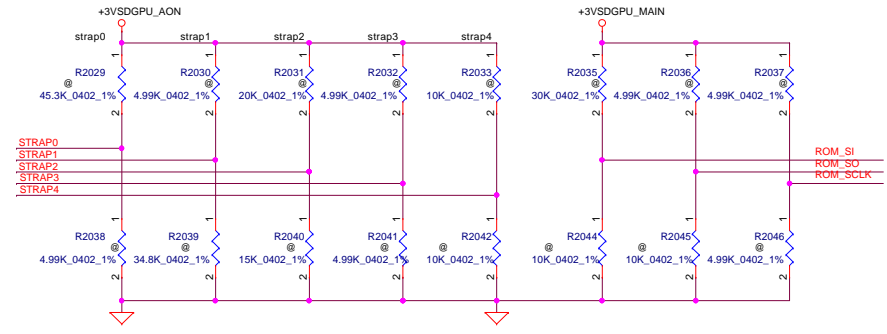
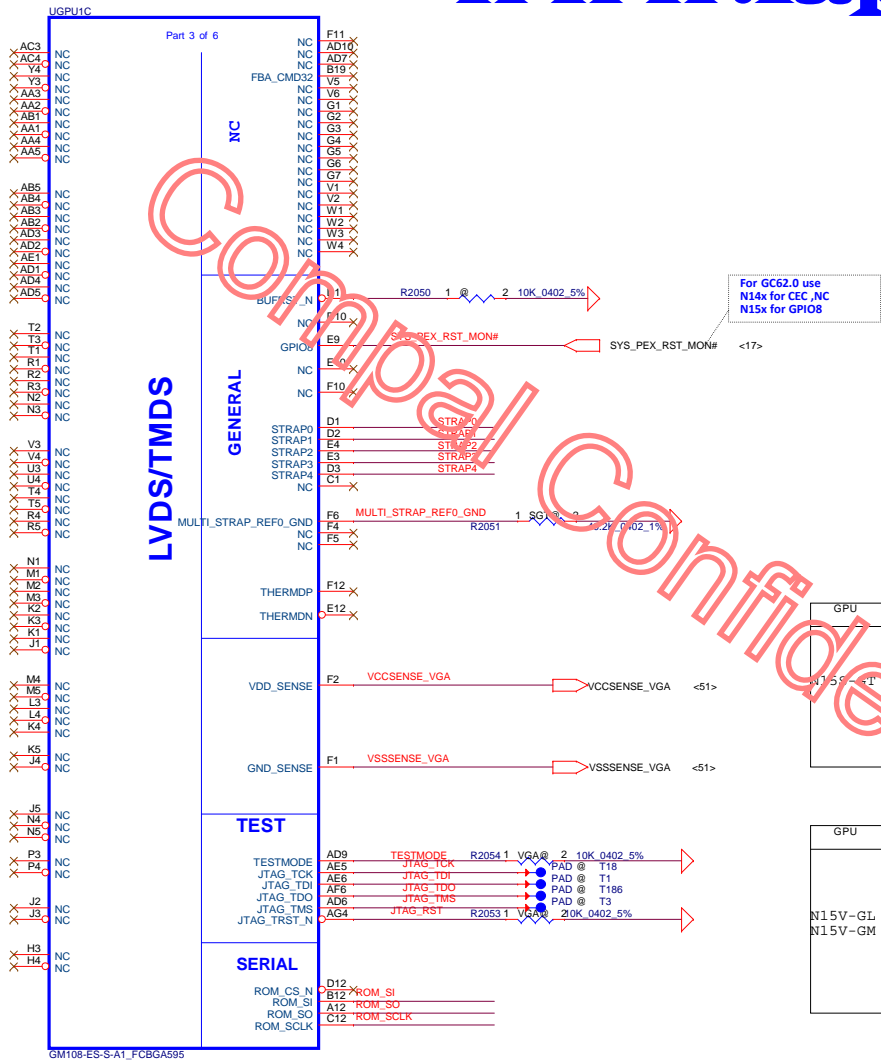
- UGPU1
N15V-GM
VGM@
SA00007BR20
- UGPU1
N15V-GT
SGT@
SA00007GJ10
- UGPU1
N15V-GL
VGL@
SA00007OO10



NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF X7R 22 µF X5R	0402 0805	2 1	Under GPU Near GPU
Bead Type		30 Ω (ESR=0.010 Ω)	0603	1	(Near GPU





For GC62.0 use N15x for CEC, NC N15x for GPIO8

02/19 PreMP modify strap resistor for 1.35V VRAM

For N15S-GT Binary strap table Decive ID : 0x1341

GPU	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15S-GT	X76550BOL05	1GHz	128Mx16x4	0xA (SA000067550) Micron MT41J128M16JT-093G-K	PU 50K	NC	NC	NC	NC	PU 15K	PD 4.99K	PD 4.99K
				0xB (SA000068U90) Samsung K4W2G1646Q-BC1A						PU 20K		
				0x9 (SA00006H430) Hynix H5TC2G63FFR-11C						PU 10K		
				0x4 (SA000077K20) Micron MT41J256M16HA-093G-E						PD 24.9K		
N15S-GM	X76550BOL10	2GHz	256Mx16x4	0x5 (SA000076P20) Samsung K4W4G1646D-BC1A	PU 10K	PD10K	PU 10K	PU 10K	PD 10K	PD 30.1K	PD 10K	PD 10K
				0x3 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 20K		
				0x4 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 20K		

For N15V-GL/GM Binary strap table Decive ID : 0x1140

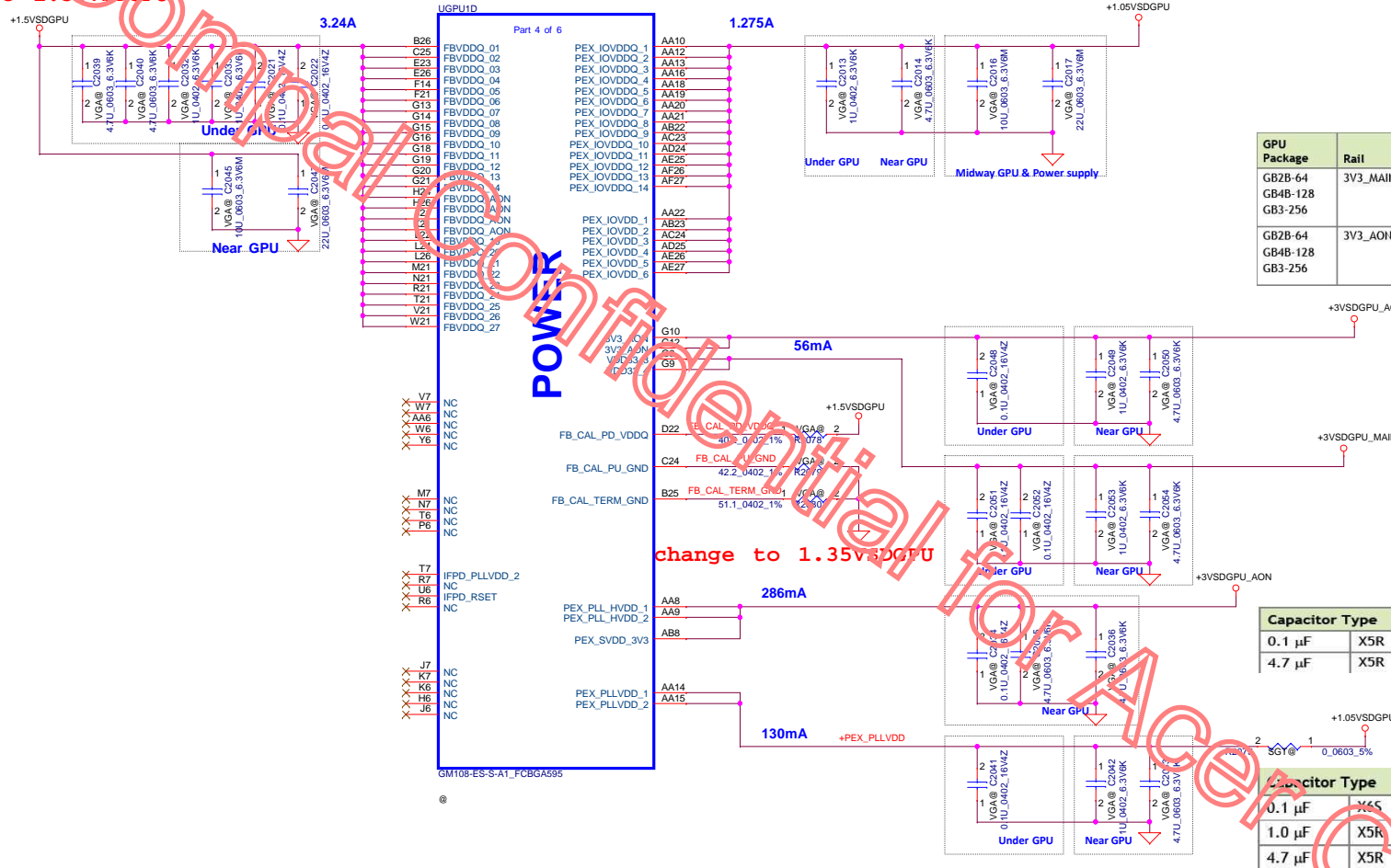
GPU	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GL	X76550BOL03	1GHz	128Mx16x4	0x1 (SA000067550) Micron MT41J128M16JT-093G-K	PU 10K	PD10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
				0x5 (SA000068U00) Samsung K4W2G1646E-BC1A	PU 10K	PD10K	PU 10K	PD 10K				
				0x9 (SA00006H430) Hynix H5TC2G63FFR-11C	PD 10K	PD10K	PU 10K	PU 10K				
N15V-GM	X76550BOL10	2GHz	256Mx16x4	0x5 (SA000068U90) Samsung K4W2G1646Q-BC1A	PD 10K	PU 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K
				0x4 (SA000076P20) Samsung K4W4G1646D-BC1A	PU 10K	PD10K	PD 10K	PU 10K				
				0x3 (SA00006E840) Hynix H5TC4G63AFR-11C	PU 10K	PD10K	PU 10K	PU 10K				
				0x4 (SA00006E840) Hynix H5TC4G63AFR-11C	PD 10K	PD10K	PU 10K	PD 10K				

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF X7R	0402	2	Under GPU
	1µF X7R	0603	2	Under GPU
	4.7µF X6S	0603	2	Under GPU
	10µF X5R	0805	1	Near GPU
	22µF X5R	0805	1	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0µF X6S	0402	1	Under GPU
	4.7µF X6S	0603	1	Near GPU
	10µF X5R	0805	1	Midway between GPU and Power Supply
	22µF X5R	0805	1	Midway between GPU and Power Supply

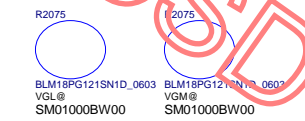
change to 1.35VSDGPU



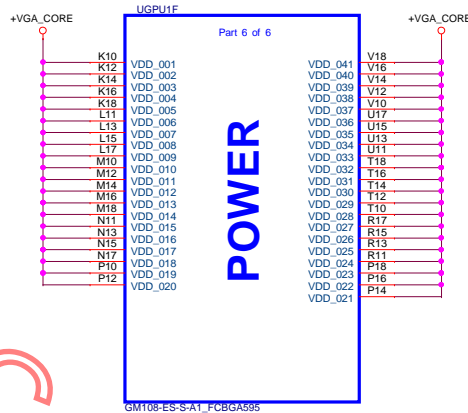
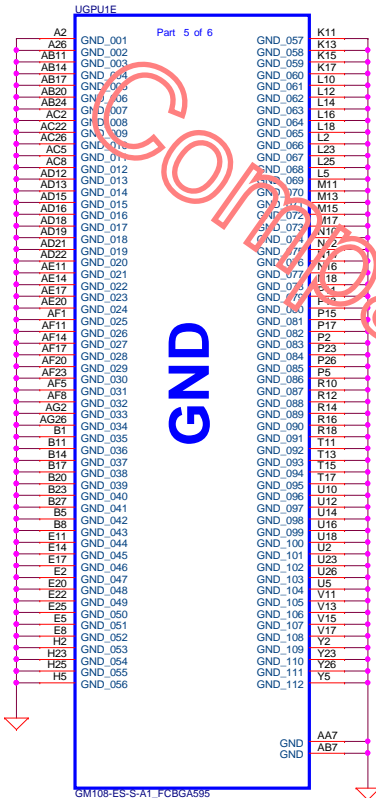
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1µF X6S	0402	2	Under GPU
GB4B-128		1µF X5R	0603	1	Near GPU
GB3-256		4.7µF X5R	0603	1	Near GPU
GB2B-64	3V3_AON	0.1µF X6S	0402	1	Under GPU
GB4B-128		1µF X5R	0603	1	Near GPU
GB3-256		4.7µF X5R	0603	1	Near GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X5R	0402	1
4.7µF	X5R	0603	2

Capacitor Type	Footprint	Population	Location
0.1µF	X6S	0402	1
1.0µF	X5R	0603	1
4.7µF	X5R	0805	1



SM010028800 2000ma 120ohm@100mhz DCR 0.1



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments	
GB2B-64	4.7 μ F	X65	0603	10	10	Under GPU
	1 μ F	X65	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		(A)	(A)	(A)
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102 °C

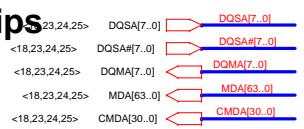
Power Supply Rail (V)	N15V-GM-S
	DDR3/L (A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

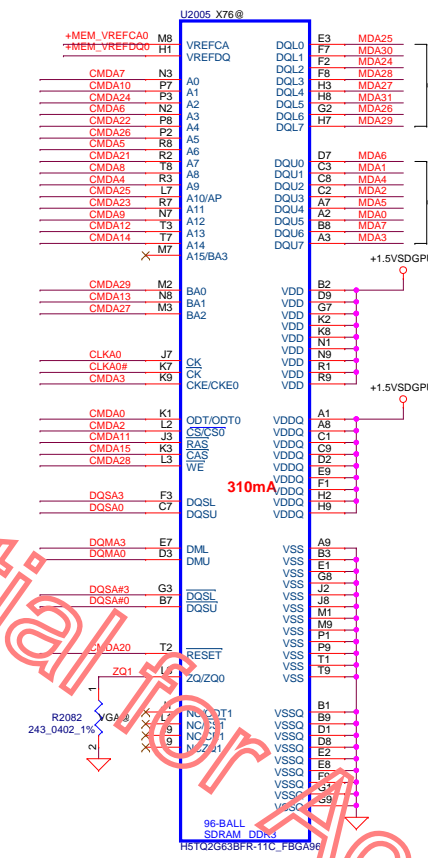
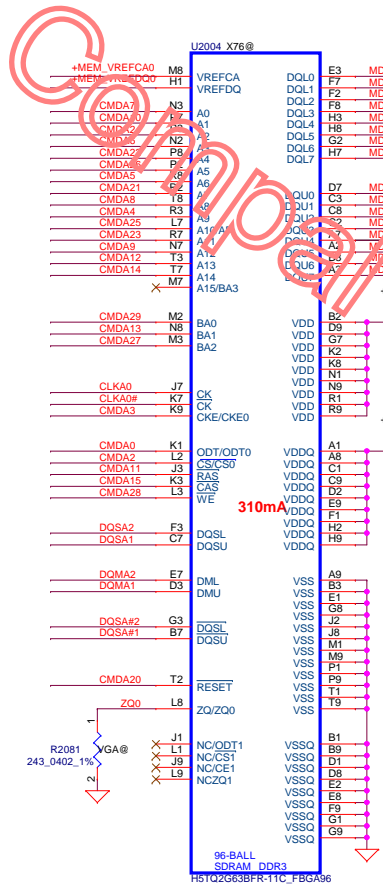
Table 7. EDP-Peak at T_J = 102 °C

Power Supply Rail (V)	N15V-GL
	DDR3 (A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips



Upper Rank 0 BOT SIDE

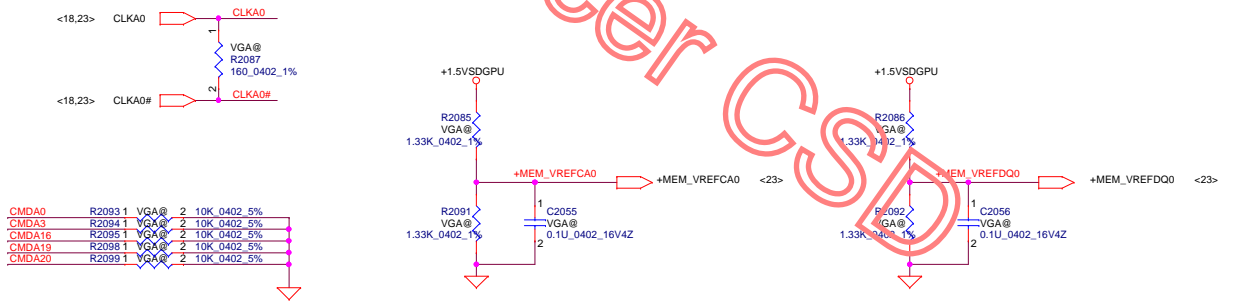
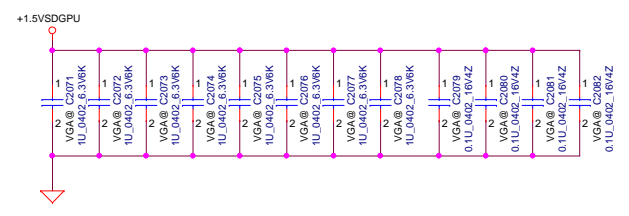


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			CKE
CMD3	CKE			CKE
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

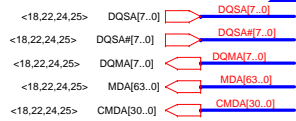
Command Bit	Default Full-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

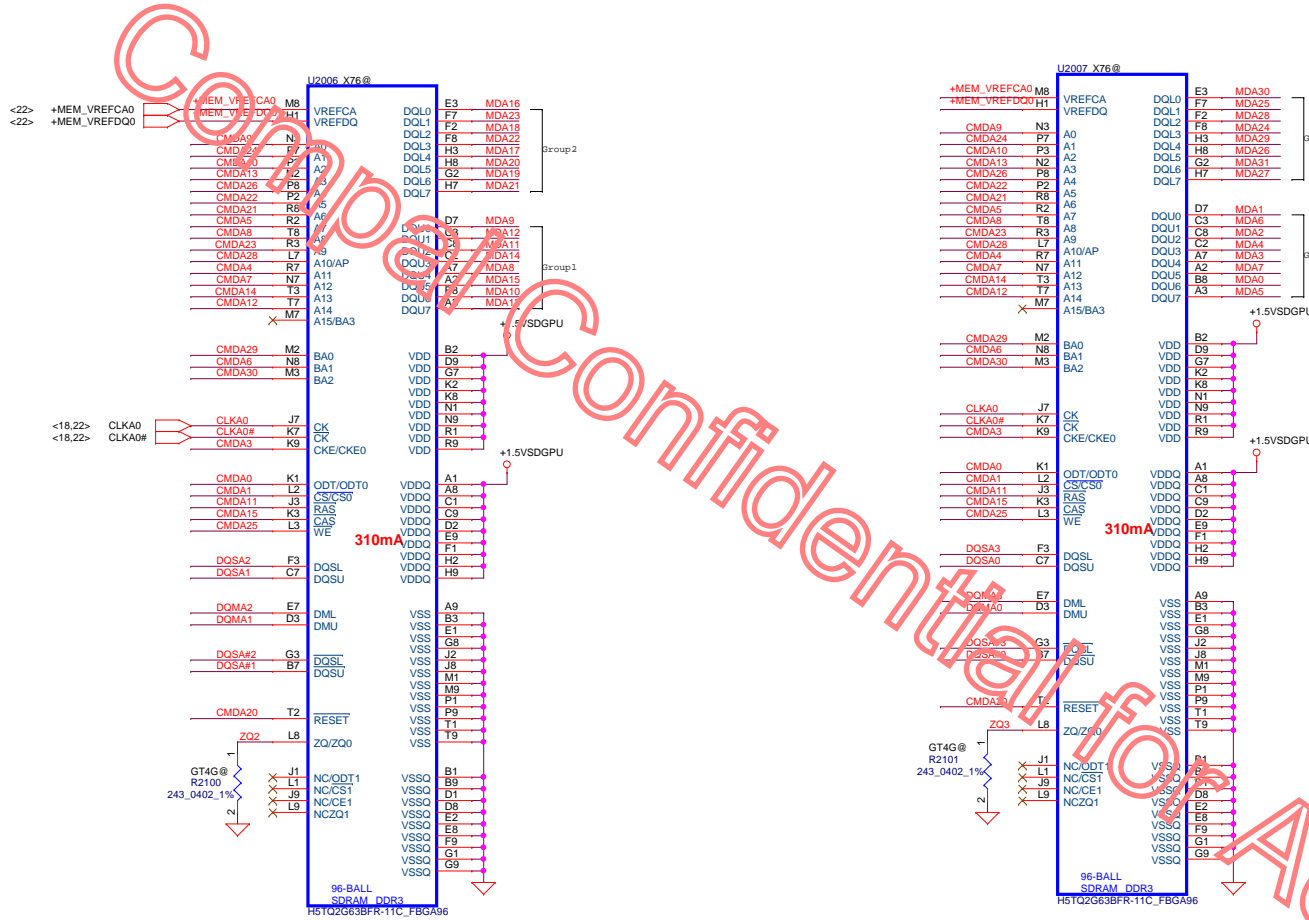
Capacitor Type	Population		Location
	FBVDDQ	FBVDD	
FBVDD/Q Combined			
0.1 μF	X7R	0402	Under DRAM
1.0 μF	X7R	0603	Under DRAM
10 μF	X5R	0805	Close to DRAM



VRAM DDR3 chips



Upper Rank 1 TOP SIDE

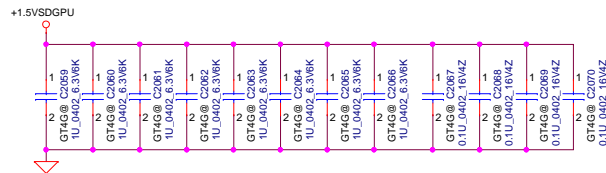


Mode & Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

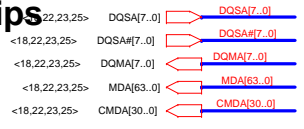
DDR3	Command Bit	Default	Pull-down
	ODTx		10k
	CKEx		10k
	RST		10k
	CS*		No Termination

Only for N15S-GT 4G

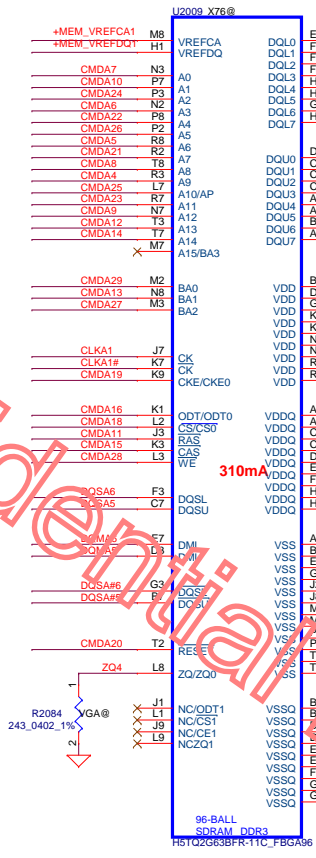
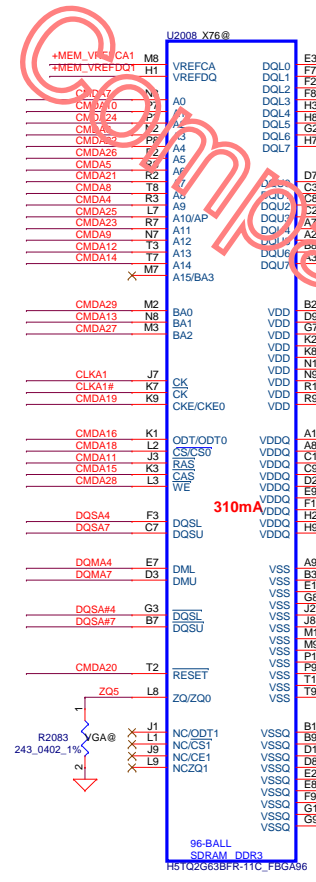
Only for N15S-GT 4G



VRAM DDR3 chips

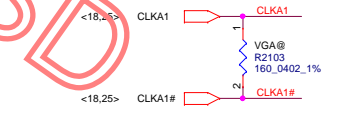
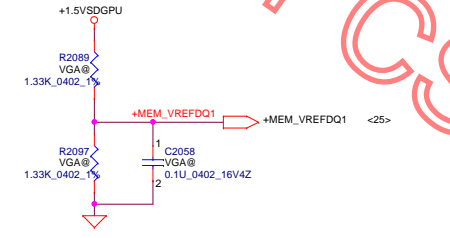
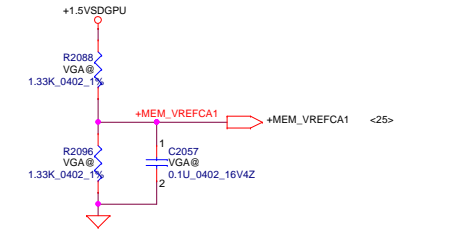
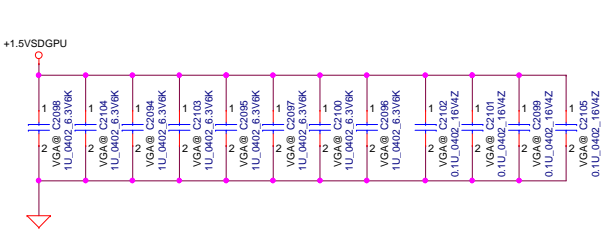


Lower Rank 0 BOT SIDE

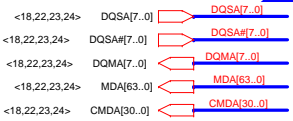


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
CMD31				
CMD32				
CMD33				
CMD34				
CMD35				
CMD36				
CMD37				
CMD38				
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CMD40				
CMD41				
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CMD95				
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CMD97				
CMD98				
CMD99				
CMD100				

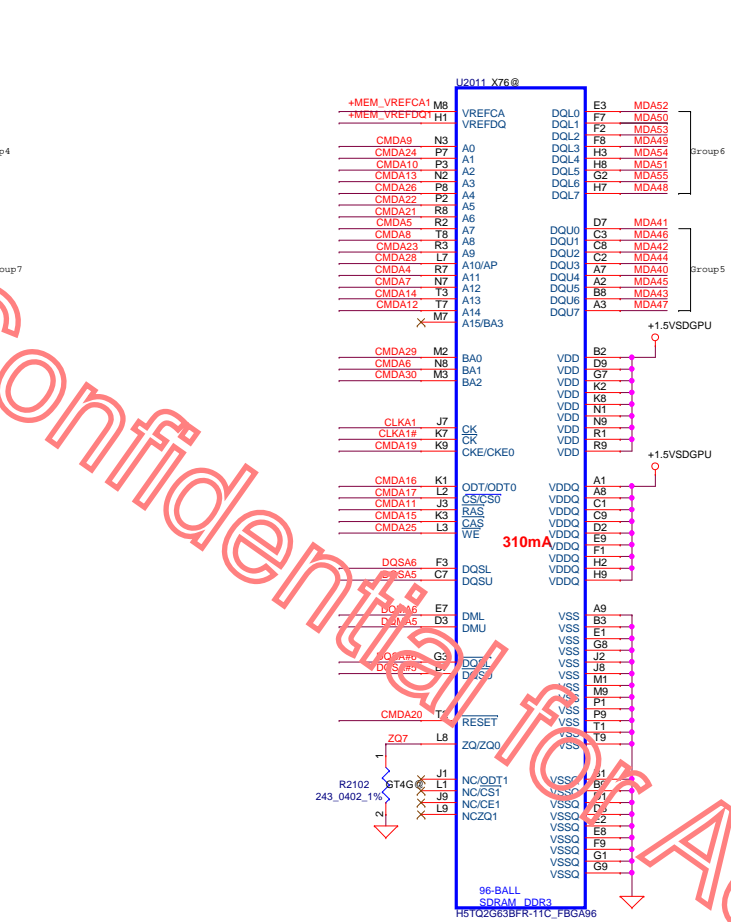
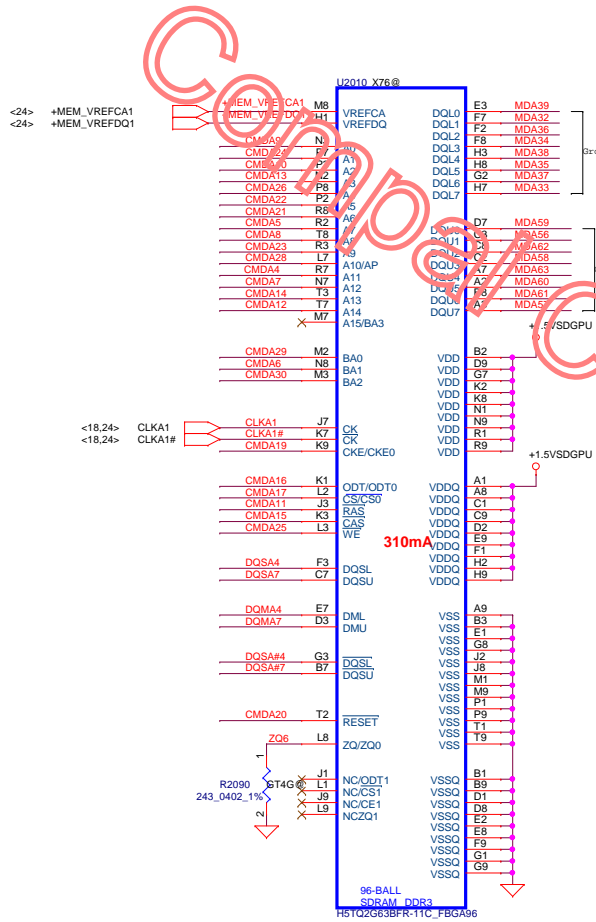
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



VRAM DDR3 chips



Lower Rank 1 TOP SIDE

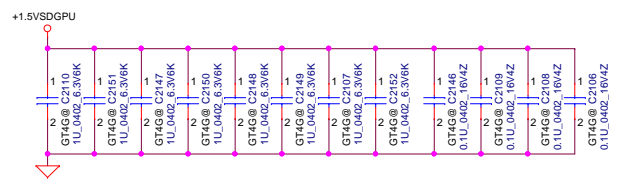


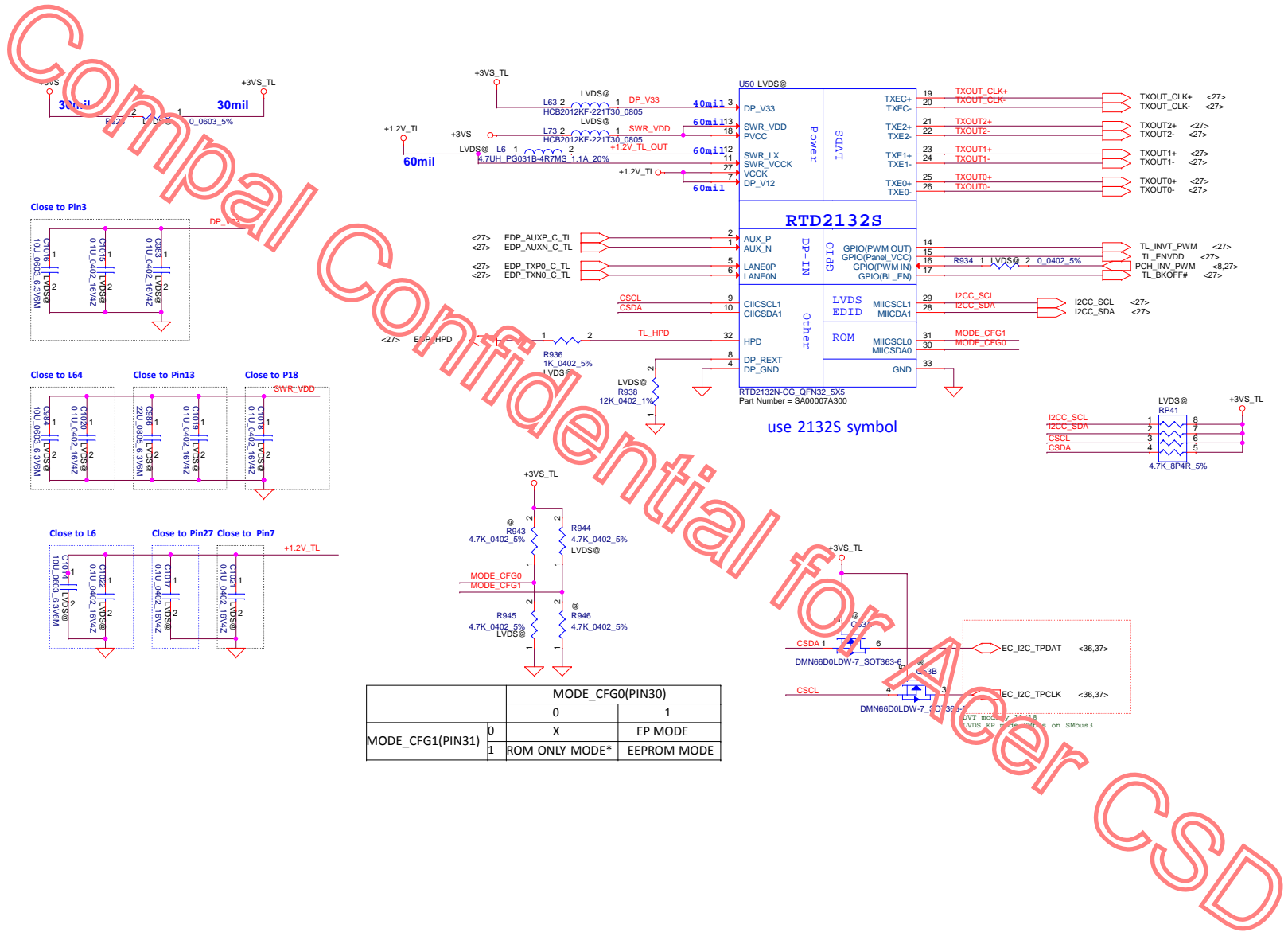
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Only for N15S-GT 4G

Only for N15S-GT 4G

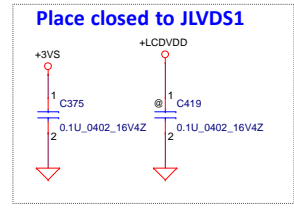
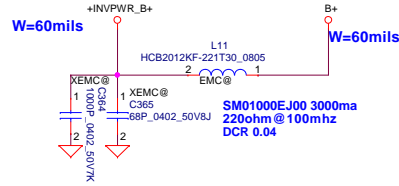
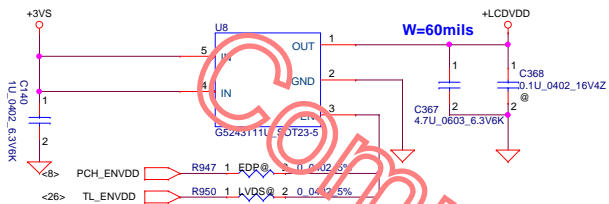




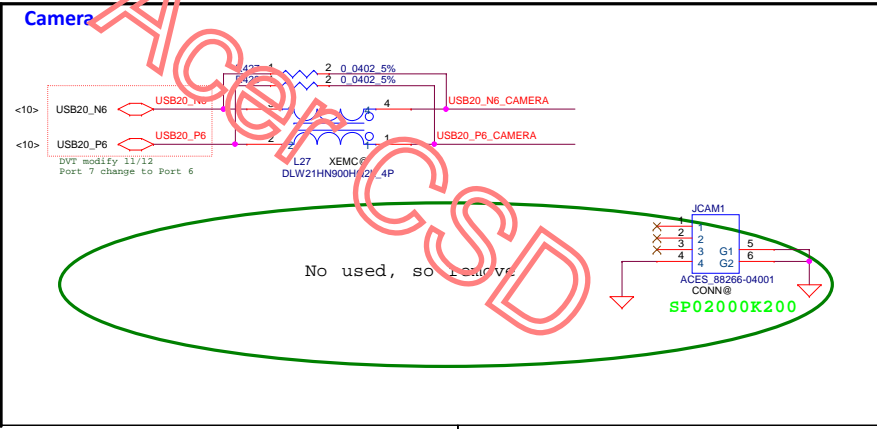
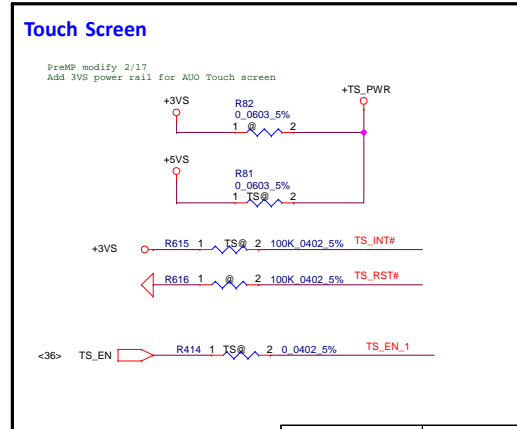
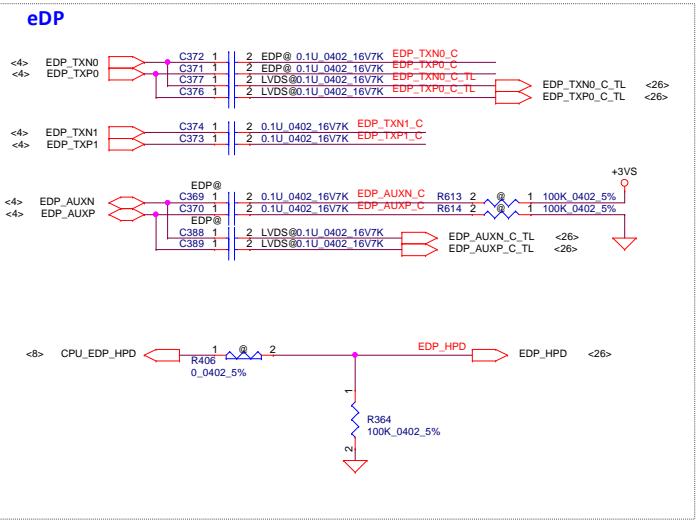
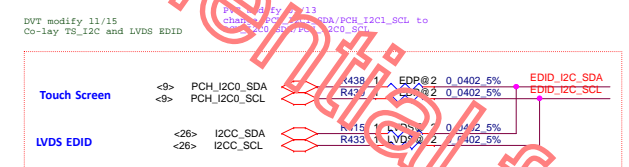
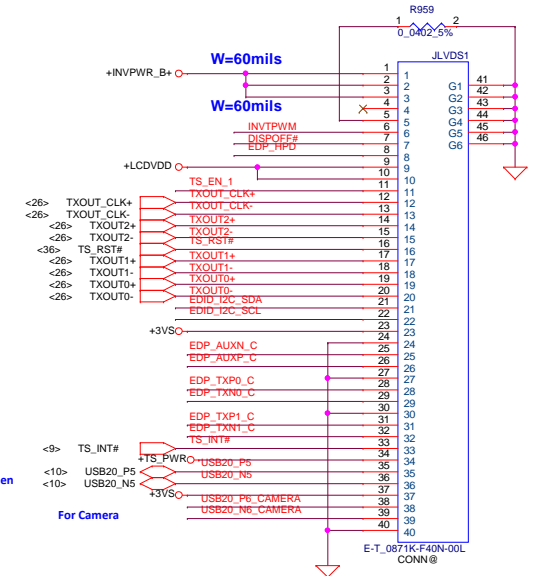
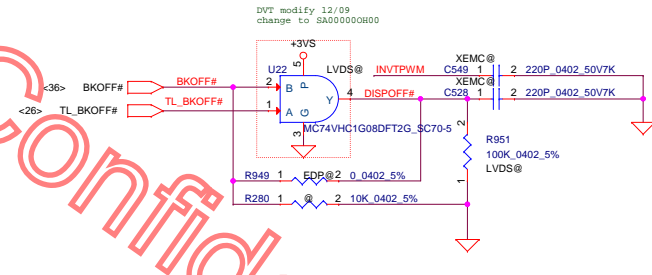
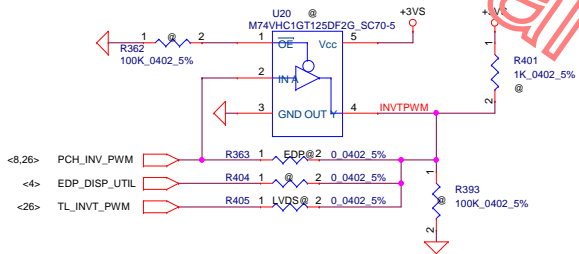
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE*	EEPROM MODE

EDP / LVDS conn.

LCD POWER CIRCUIT

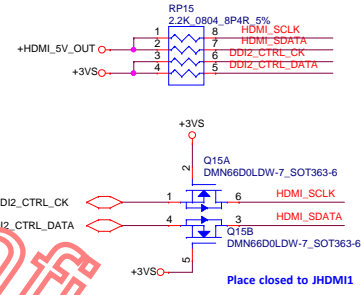
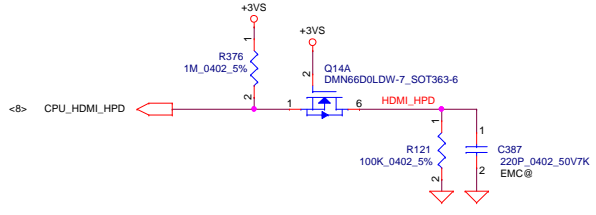
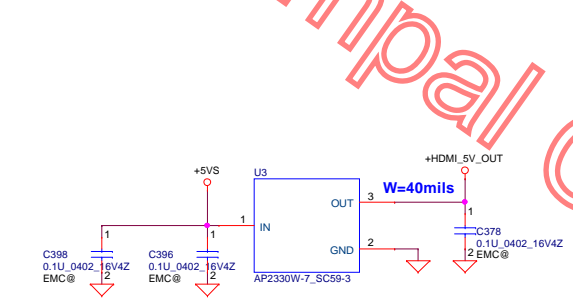


LCD/ LED PANEL Conn.



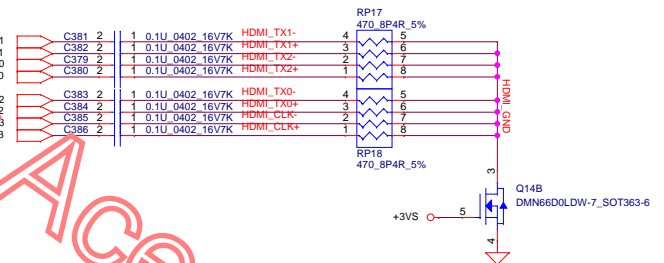
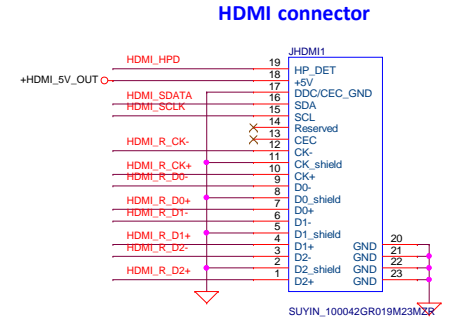
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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title	
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Size	Document Number	Customer		Rev	
A5	WAH M/B LA-B991P	A5WAH M/B LA-B991P		1.0	
Date:	Friday, October 17, 2014	Sheet	27	of 54	

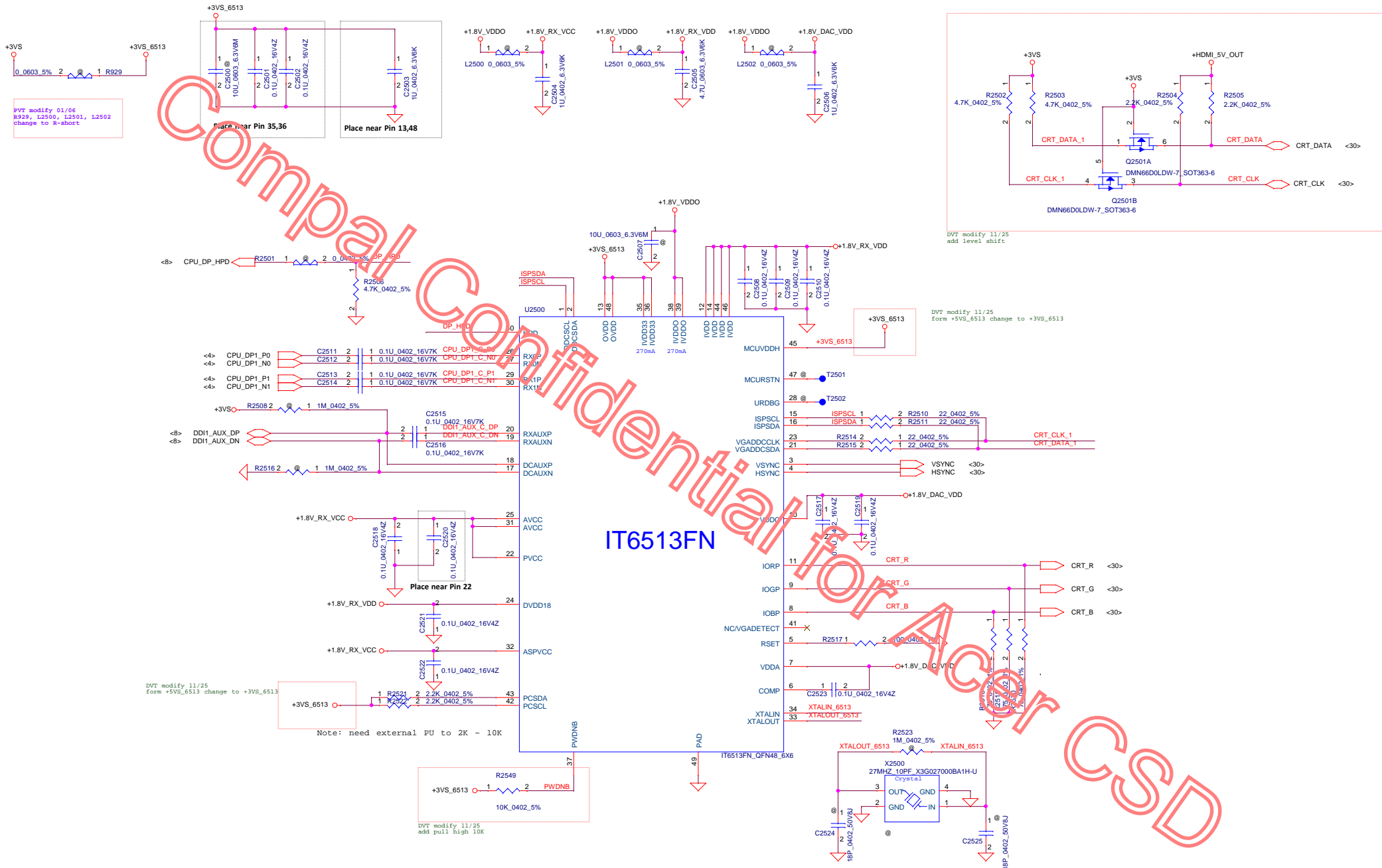
Compal Confidential for Acer CSD



SM070001310 400ma 300nm@1100nmhz 5% R 0.3

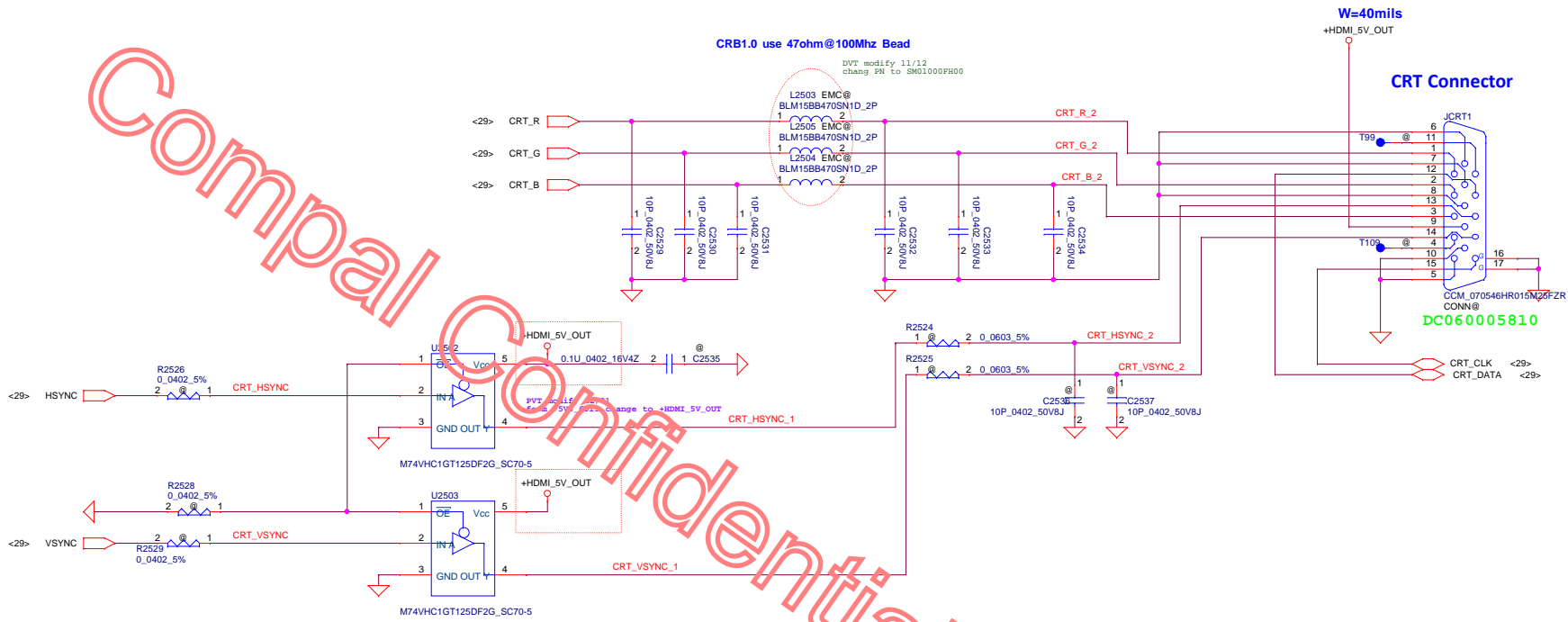
HDMI_CLK-	R368	1	XEMC@	2	0.0402_5%	HDMI_R_CLK-
HDMI_CLK+	R369	1	XEMC@	2	0.0402_5%	HDMI_R_CLK+
HDMI_TX0-	R370	1	XEMC@	2	0.0402_5%	HDMI_R_D0-
HDMI_TX0+	R371	1	XEMC@	2	0.0402_5%	HDMI_R_D0+
HDMI_TX1-	R372	1	XEMC@	2	0.0402_5%	HDMI_R_D1-
HDMI_TX1+	R373	1	XEMC@	2	0.0402_5%	HDMI_R_D1+
HDMI_TX2-	R374	1	XEMC@	2	0.0402_5%	HDMI_R_D2-
HDMI_TX2+	R375	1	XEMC@	2	0.0402_5%	HDMI_R_D2+





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Size	Document	Number	Rev	1.0	
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Date:	Friday, October 17, 2014	Sheet	29	of 54	

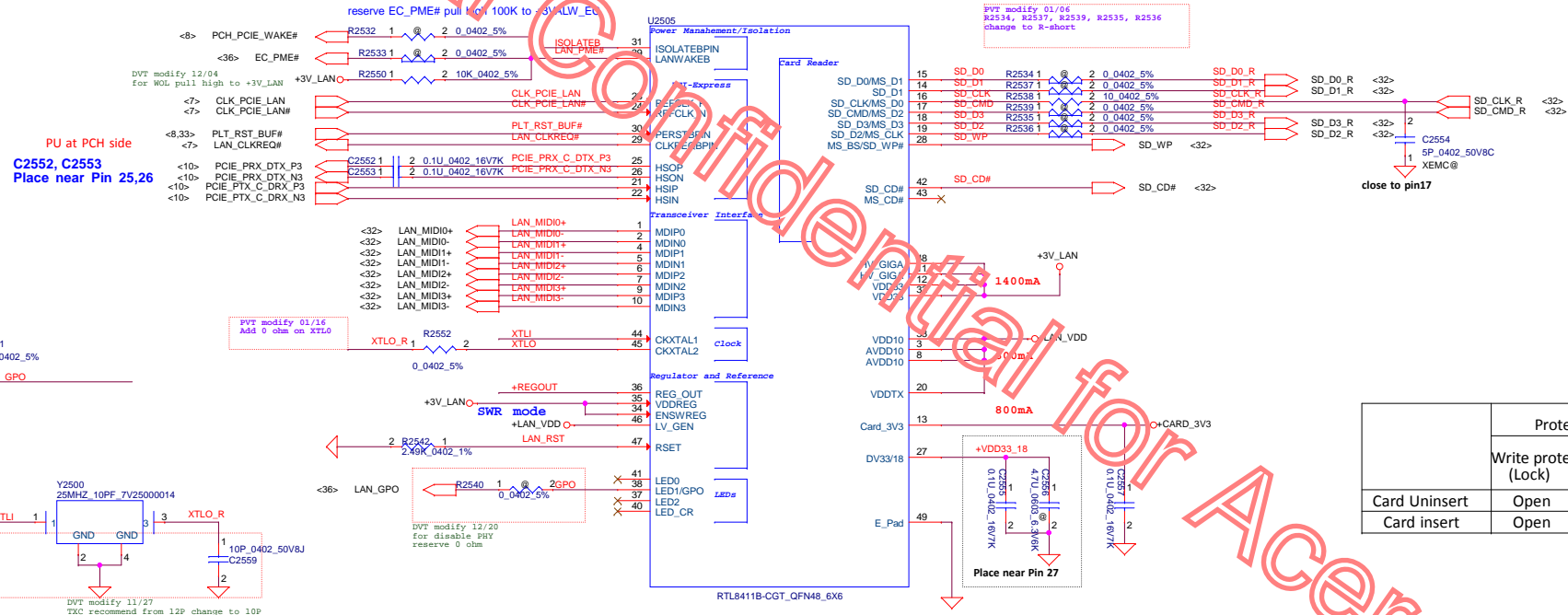
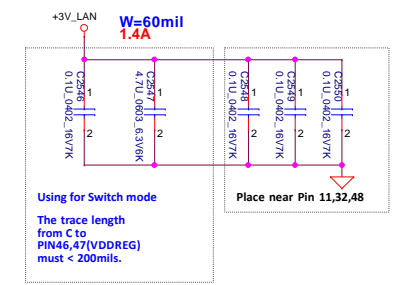
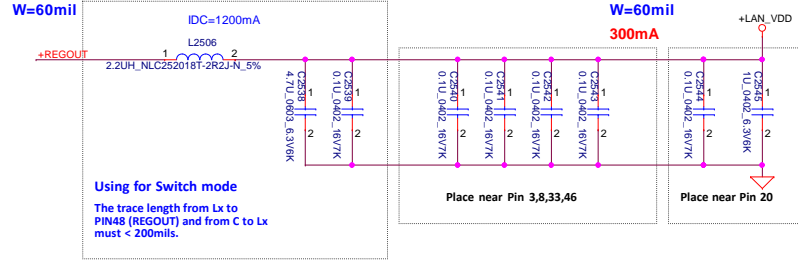
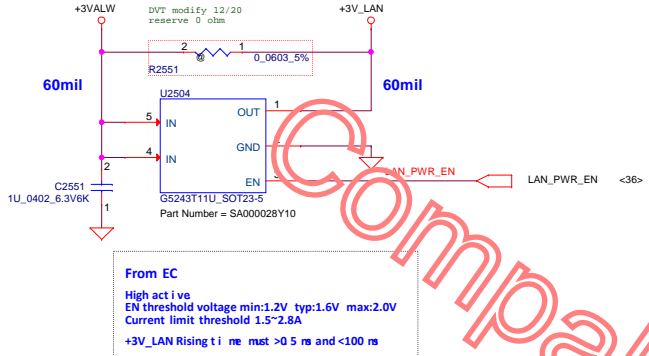
CRT conn.



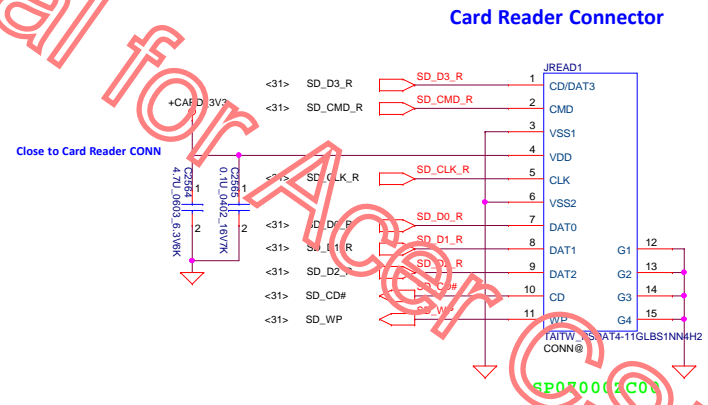
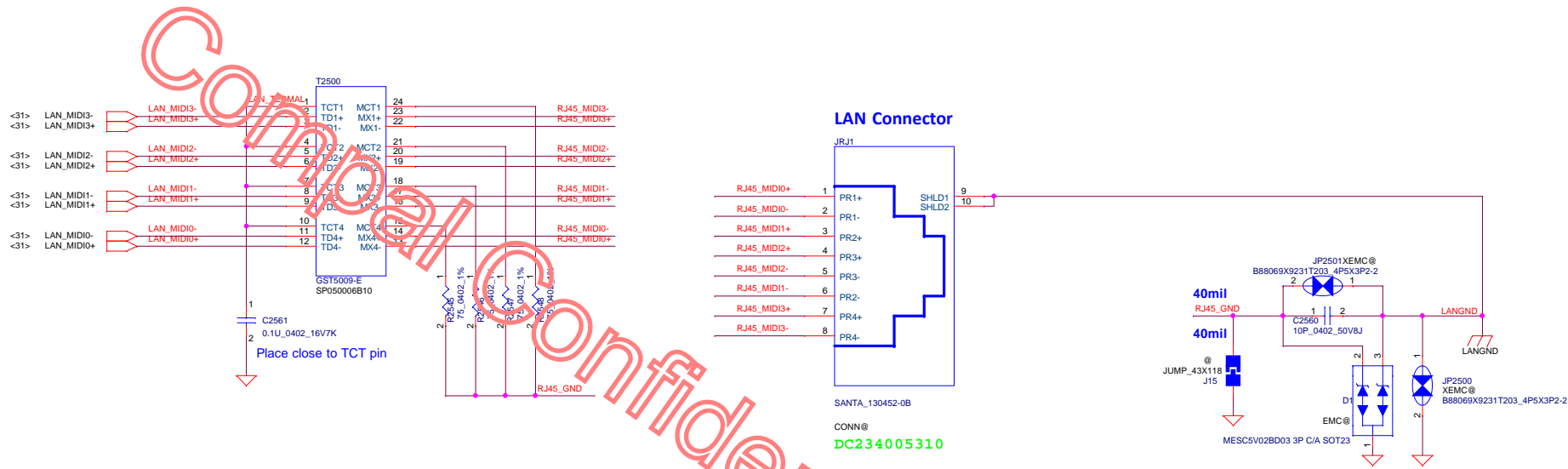
Confidential for Acer CSD

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LAN-RTL8411B

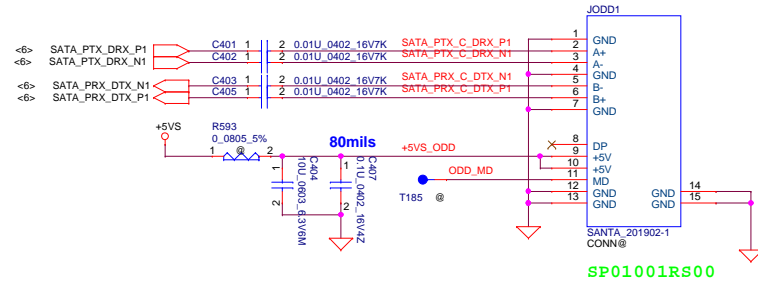
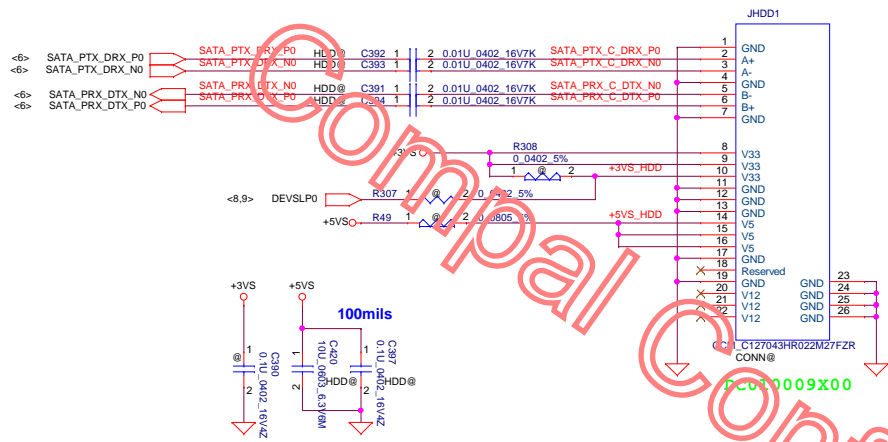


	Protect contact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

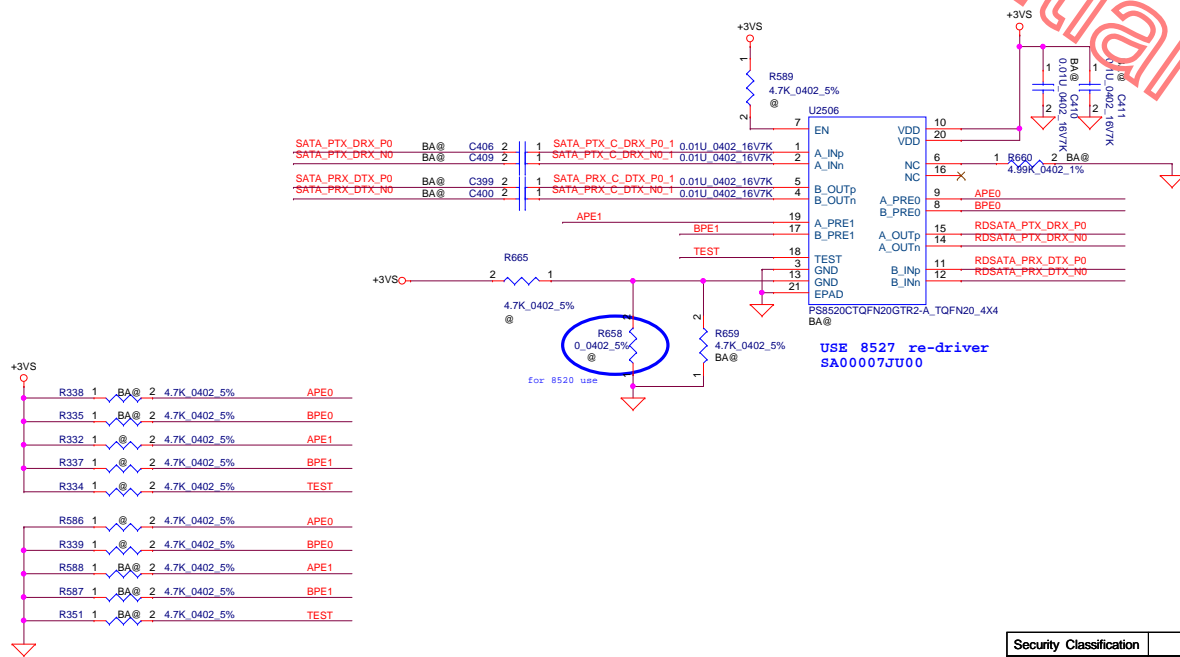


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Size	Document	Number	Rev	1.0
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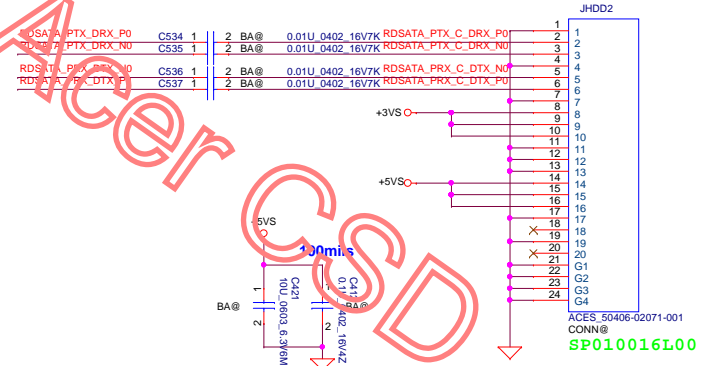
SATA HDD1 Conn.



SATA Re-Driver HDD Conn. for BA50

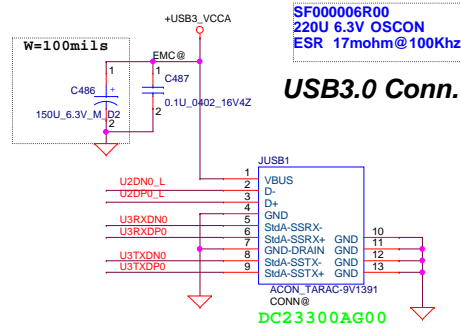
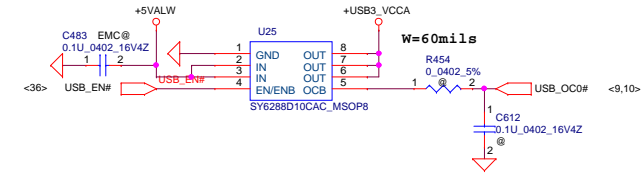
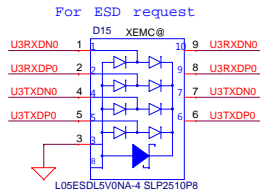
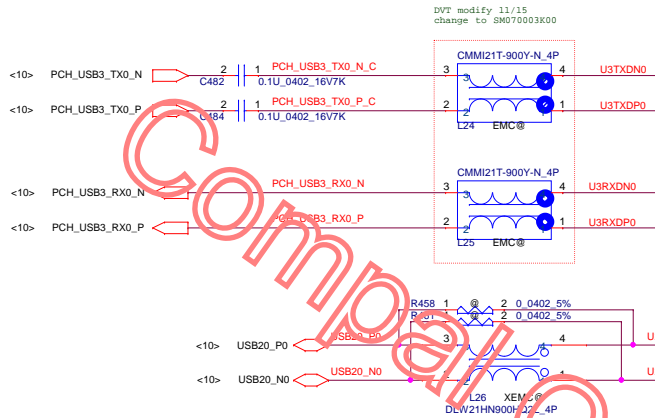


SATA HDD1 Conn. CL 4.0 mm

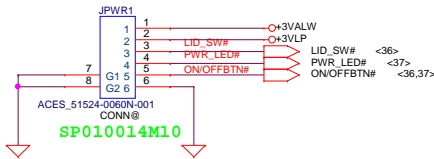


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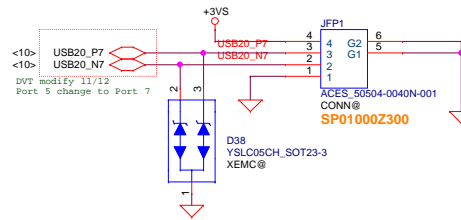
USB3.0 (Port 0)



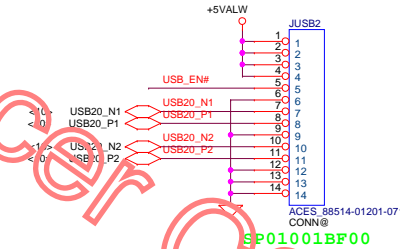
PWR/B



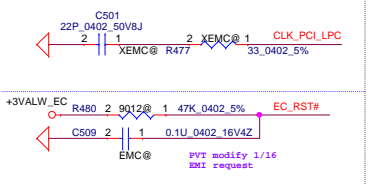
Finger Print /B for BA50



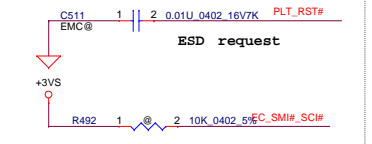
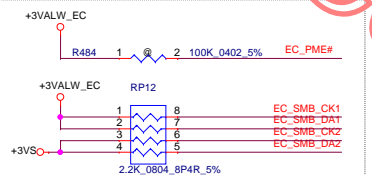
USB/B (USB Port 1, Port2)



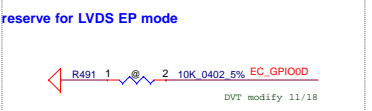
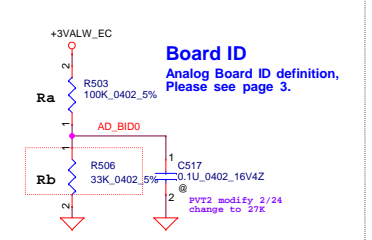
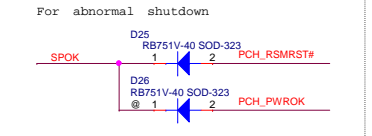
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Size	Document Number	Rev	1.0
Custom	A5WAH M/B LA-B991P	Date:	Friday, October 17, 2014
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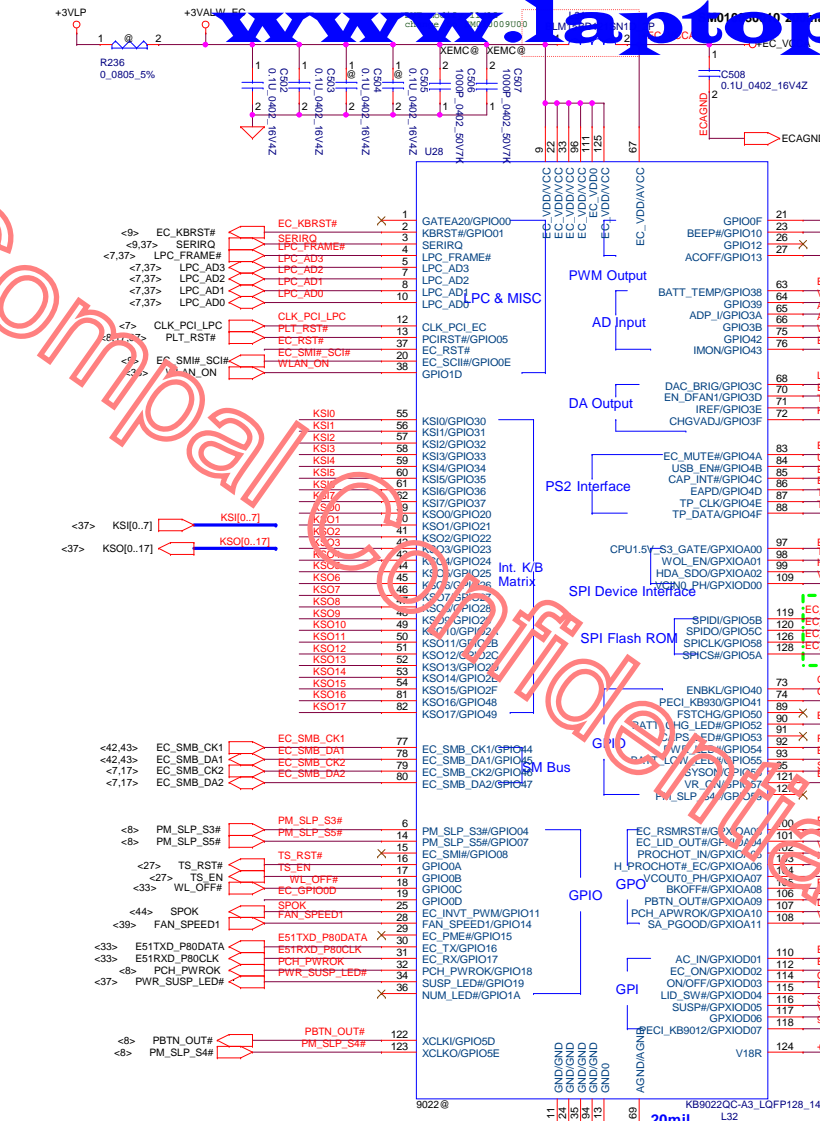
9022: ECRST# is internally pull-up to VCC via 40kOhm resistor so can remove external pull-up resistor and capacitor.



9022: Change control method from push-pull to open-drain, so EC_SCI# must be pull high. *PU on PCH side (pull high in PCH side)

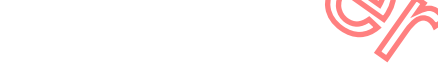
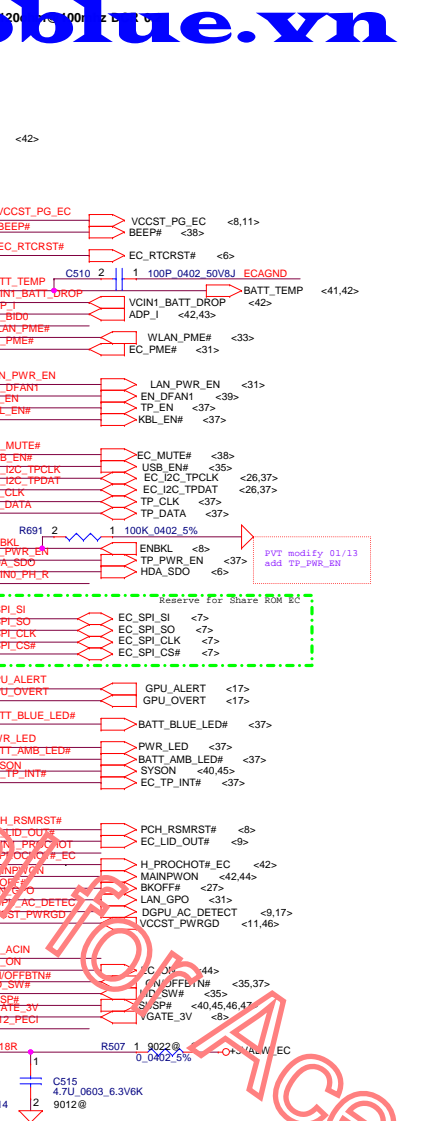


DVT modify 11/18

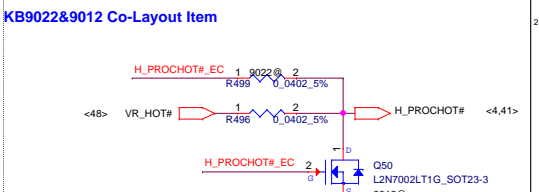
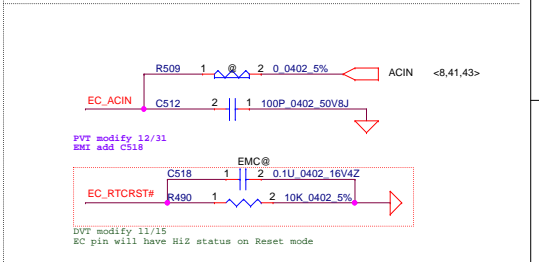
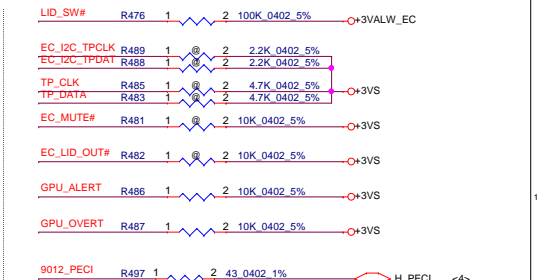


SM010030010 200ma 120ohm@100mhz DCR 0.2

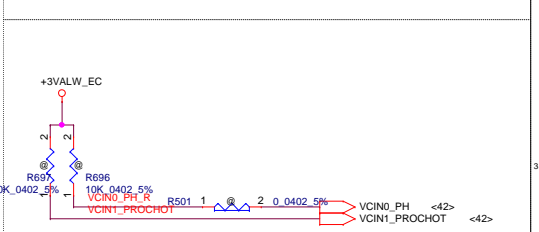
DVT modify 11/12 change to SM01009000



DVT modify 11/12 change to SM01009000



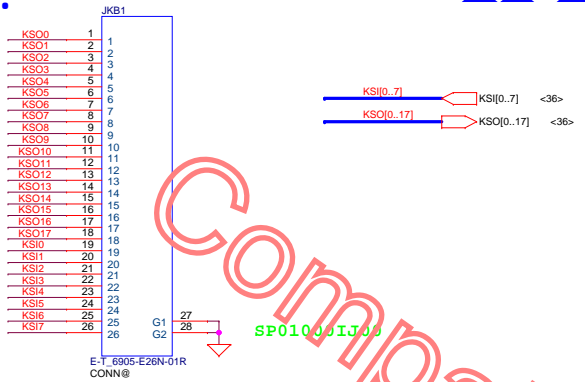
Latest design guide suggest change to 74LVC1G06.



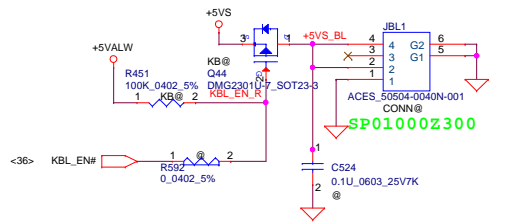
PU will disable PH function

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Size	Document Number	Rev		1.0	
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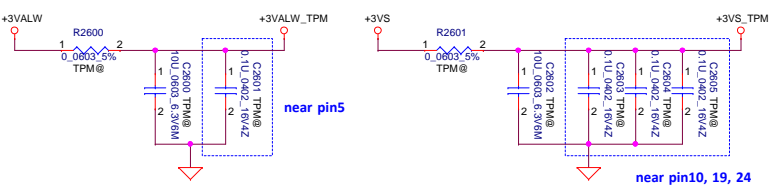
KB Conn.



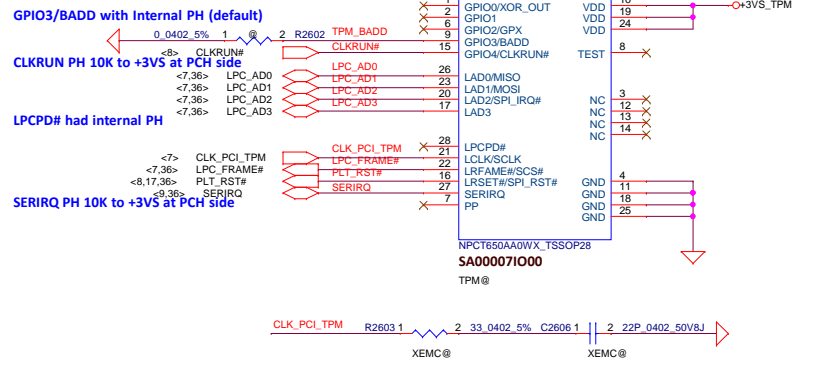
KB BackLight Conn. Reserve



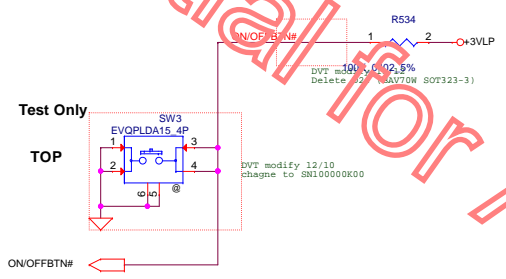
TPM Board for 2015



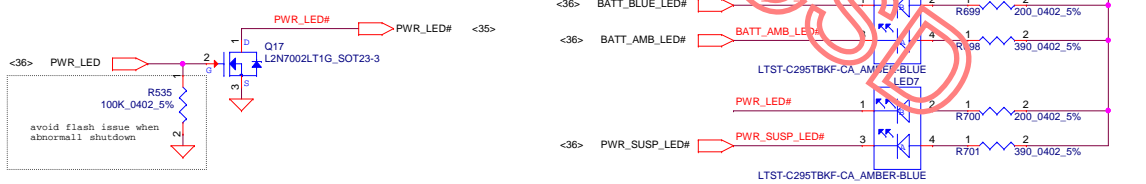
BADD	SELECTION
0	Eh - Efh
* 1	7eh - 7fh



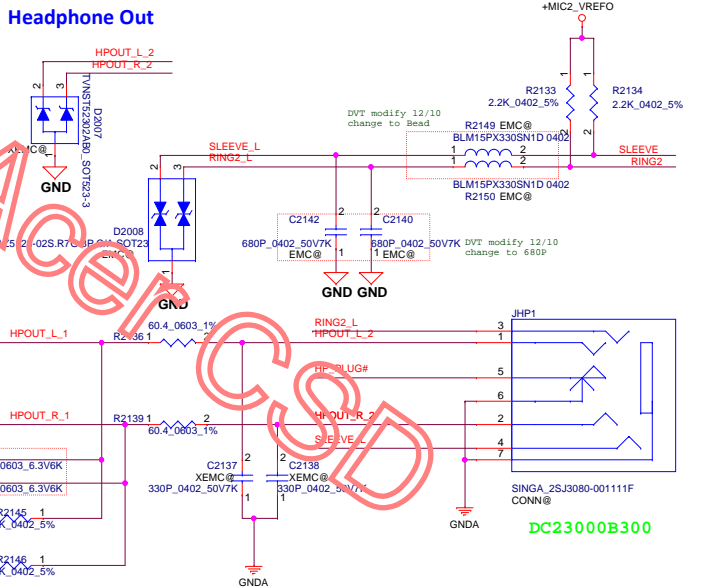
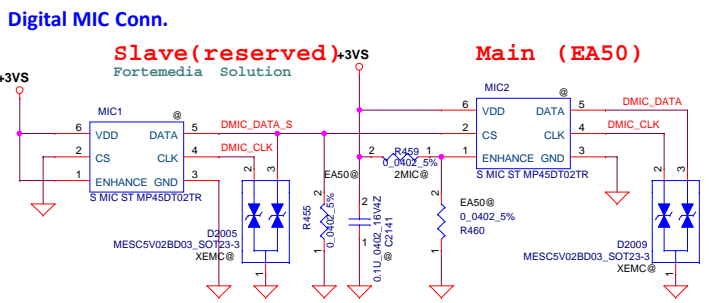
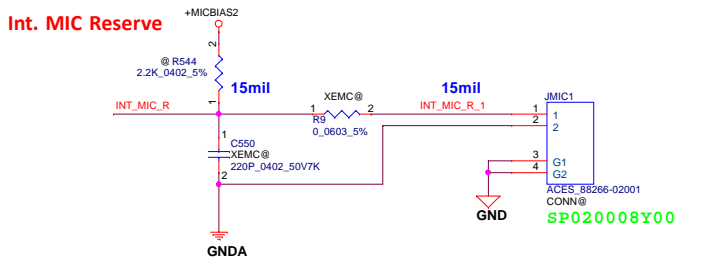
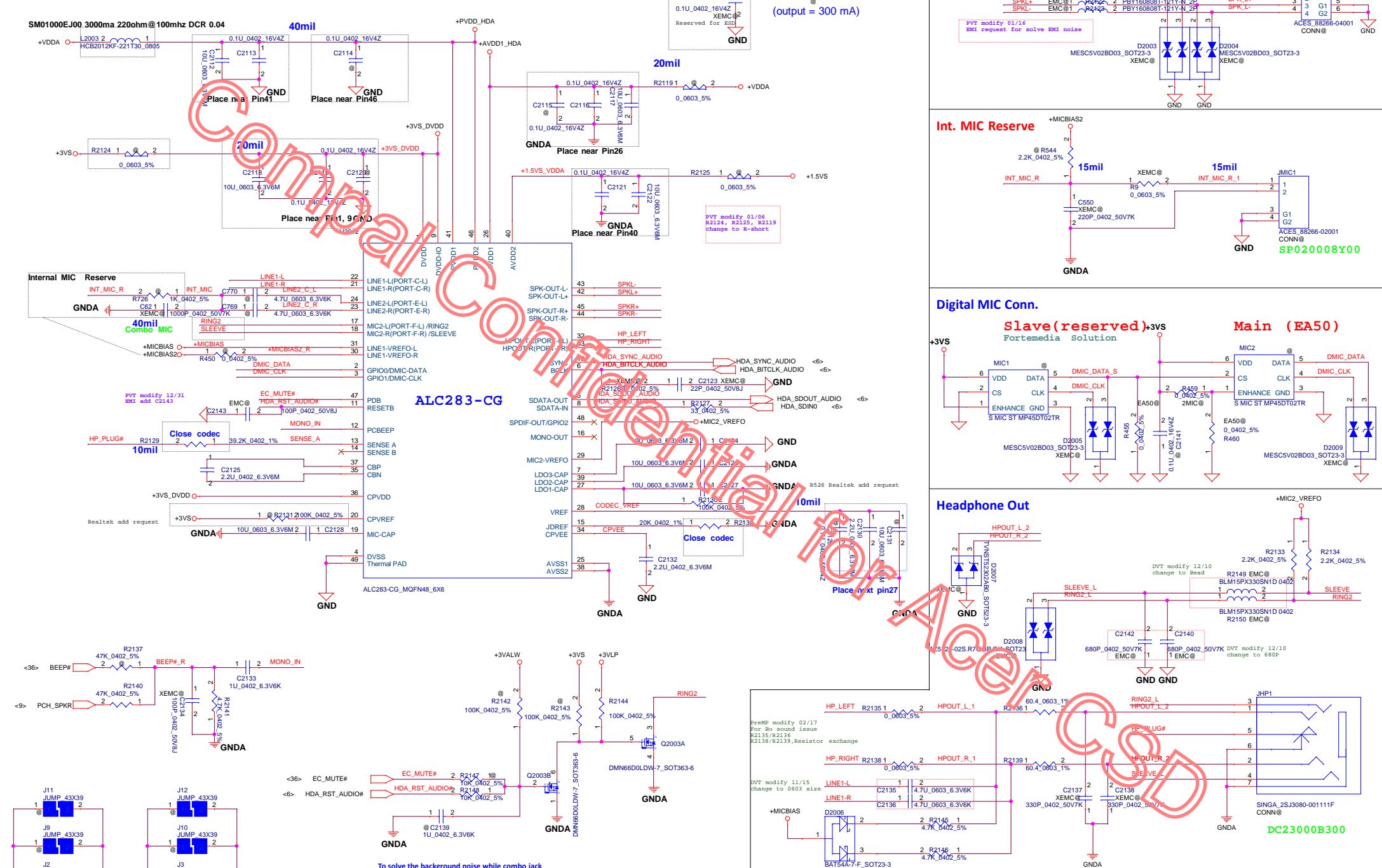
ON/OFF BTN



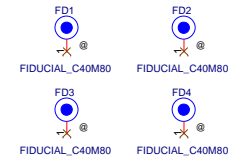
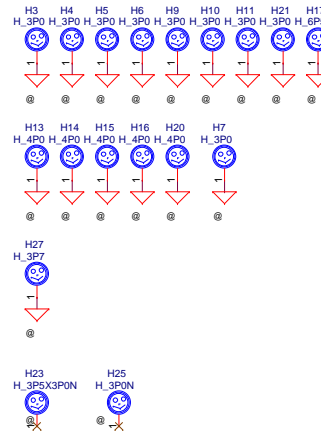
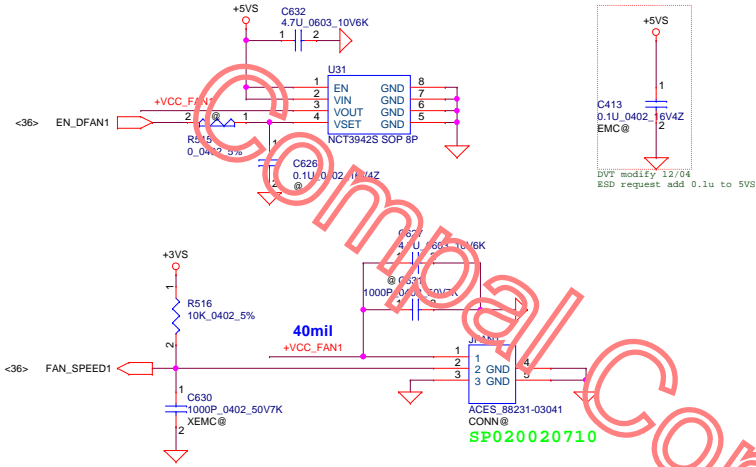
LED



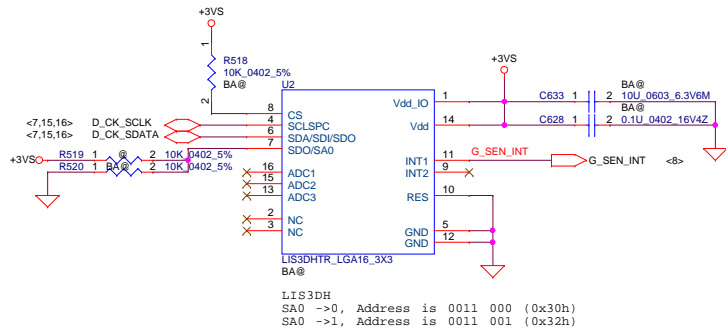
HD Audio Codec



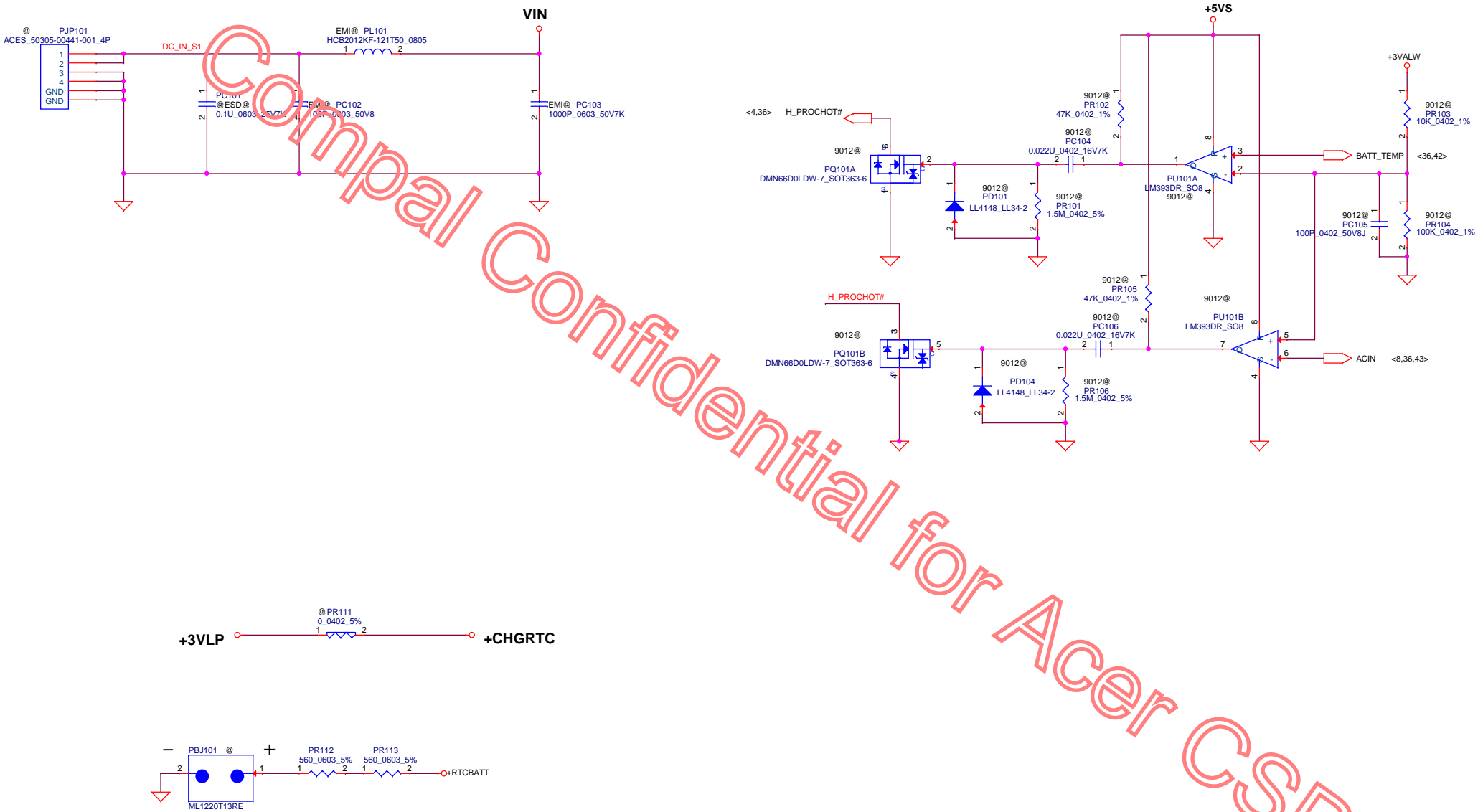
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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title	
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Size	Document Number	Customer		Rev	
A5WAH	M/B LA-B991P			1.0	
Date:	Friday, October 17, 2014	Sheet	38	of 54	



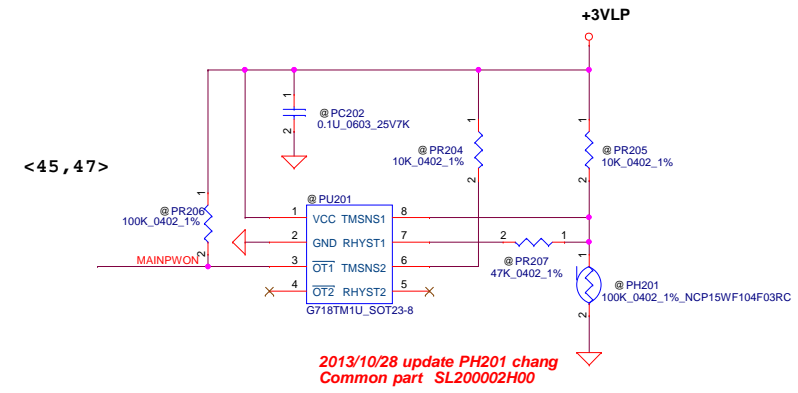
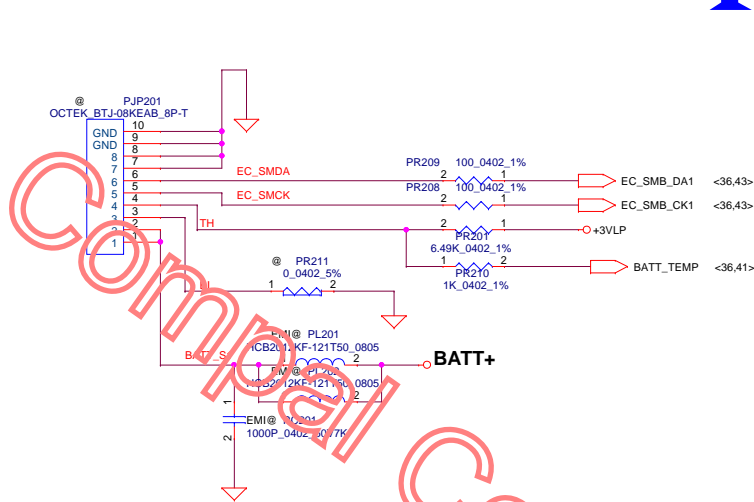
G-Sensor for BA50



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Title	FAN & Screw Hole & G-Sensor			
Size	Document	Number	Rev	
Custom	A5WAH M/B LA-B991P		1.0	
Date:	Friday, October 17, 2014	Sheet	39	of 54



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Size	Document Number	Rev		1.0
Custom				
Date:	Friday, October 17, 2014	Sheet	41 of 54	



```

---Battery_pin define---
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

---Battery Con_pin define---
PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+
    
```

2013/10/28 update PH201 chang
Common part SL200002H00

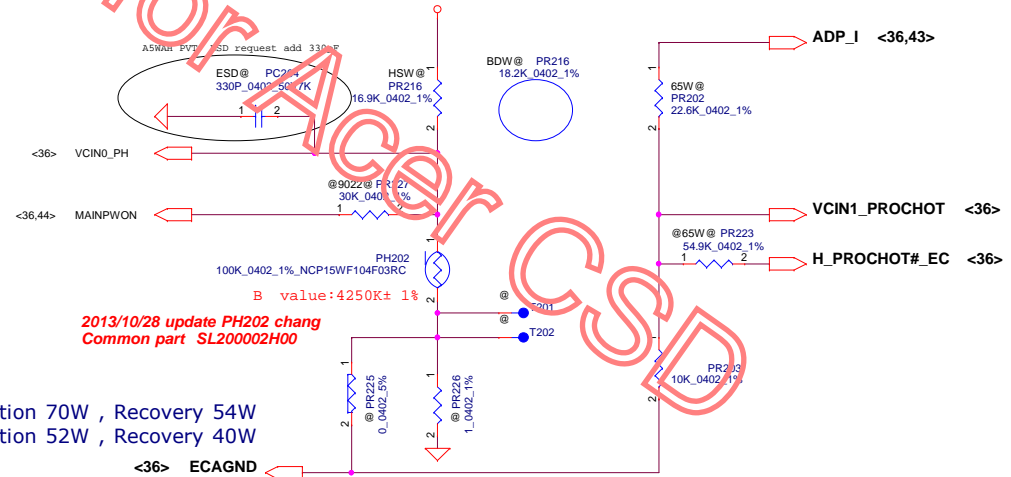
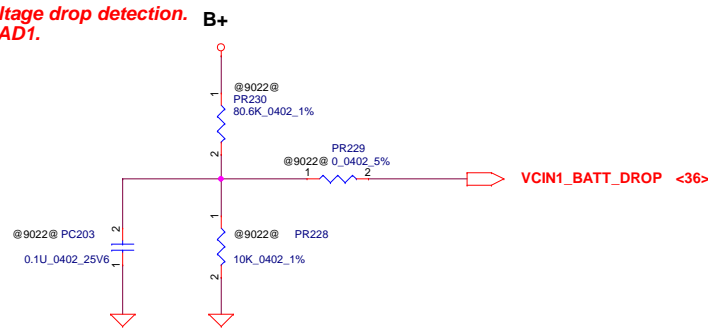
2013/10/14 update

For KB9022 sense 20mΩ	Active	Recovery
40W PR202 10K ohm	52W, 0.54V	40W, 0.42V
65W PR202 22.6K ohm	84.5W, 0.54V	65W, 0.42V

PH201 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C +EC_VCCA

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



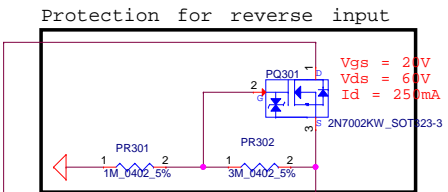
For 65W adapter==>action 70W , Recovery 54W
For 40W adapter==>action 52W , Recovery 40W

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				BATTERY CONN / OTP	
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Custom			1.0		
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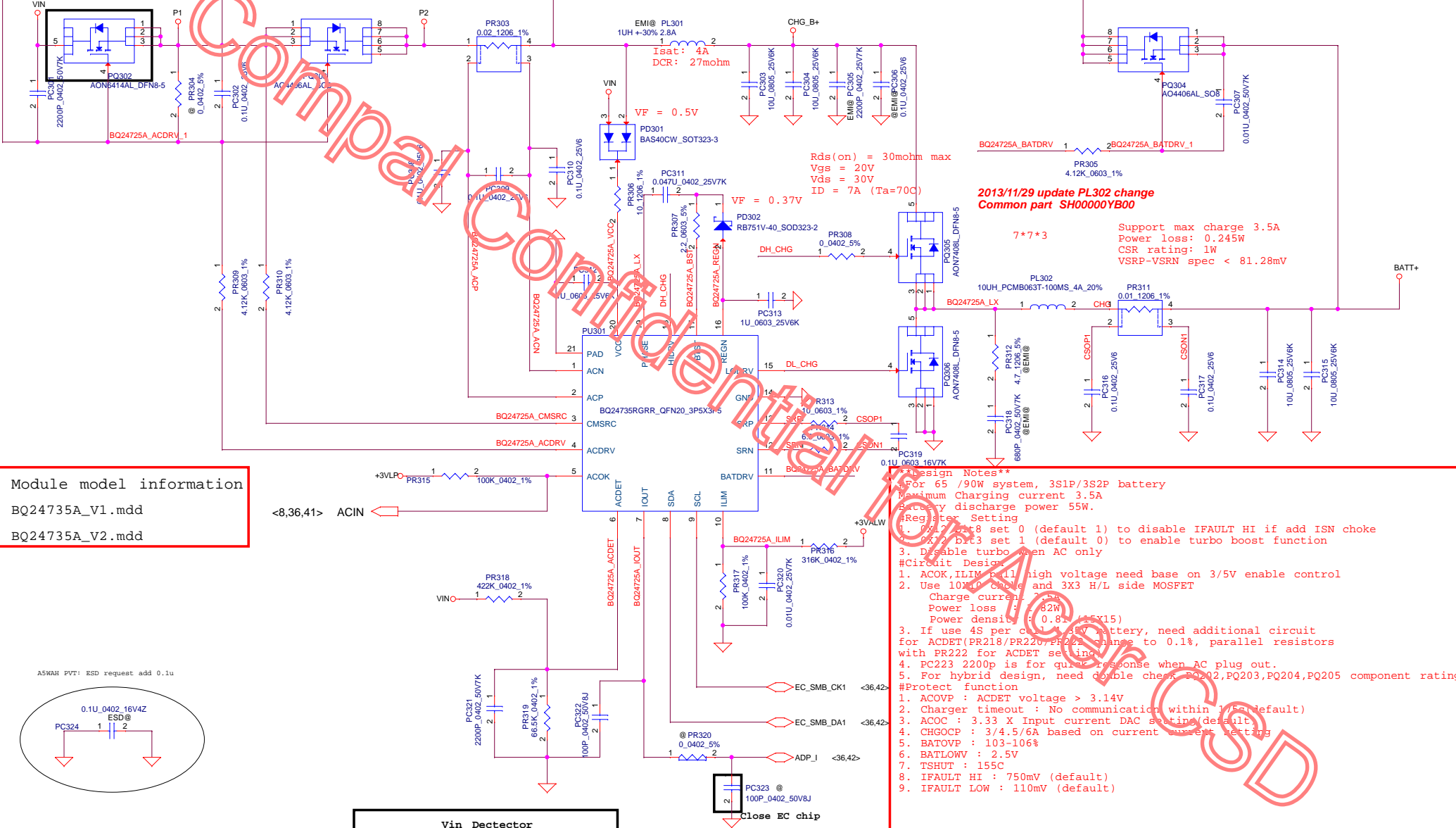
2013/10/14
PR303 10m ohm chang -->20m ohm
SD00000S120

2014/01/21 update PL301 change
Common part SH00000YG00

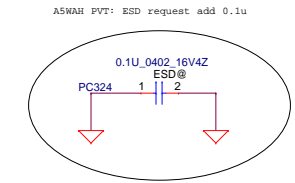
2013/11/29 update PL302 change
Common part SH00000YB00



Need check the SOA for inrush



Module model information
BQ24735A_V1.mdd
BQ24735A_V2.mdd



Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+107)/20/0.02
= 3.986 A

Design Notes**

For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.

Register Setting

- PR218 set 0 (default 1) to disable IFAULT HI if add ISN choke
- PR217 bit3 set 1 (default 0) to enable turbo boost function
- Disable turbo when AC only

#Circuit Design

- ACOK,ILIM,ILIM high voltage need base on 3/5V enable control
- Use 10MΩ cable and 3X3 H/L side MOSFET

Charge current

Power loss : 82W
Power density : 0.82W/(5X15)

- If use 4S per cell 3.6V battery, need additional circuit for ACDET (PR218/PR220, PR221 change to 0.1%, parallel resistors with PR222 for ACDET setting)
- PC223 2200p is for quick response when AC plug out.
- For hybrid design, need double check PQ202,PQ203,PQ204,PQ205 component rating

#Protect function

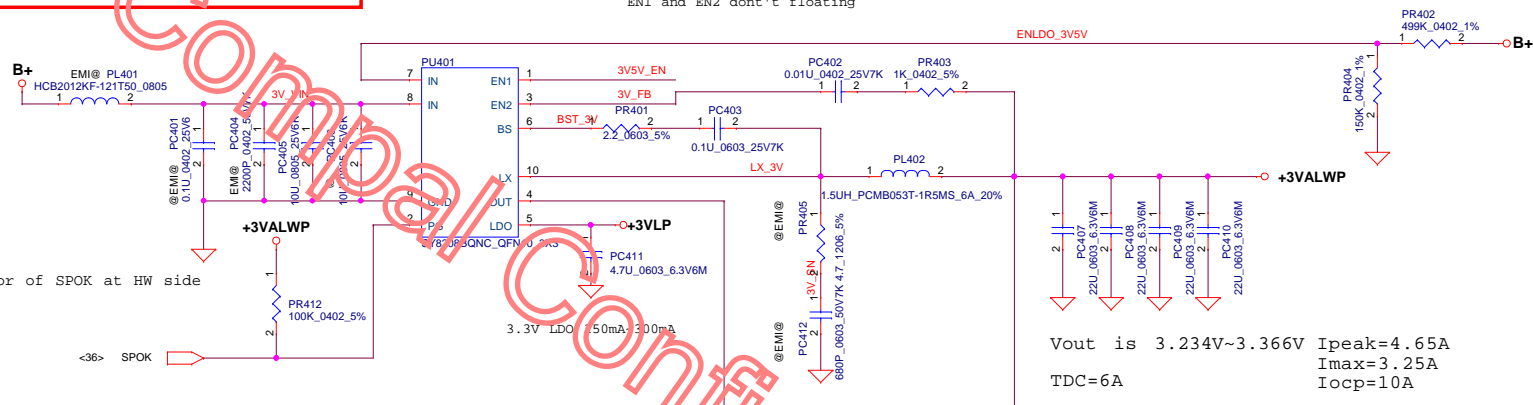
- ACOVIP : ACDET voltage > 3.14V
- Charger timeout : No communication within 1/5s(default)
- ACOC : 3.33 X Input current DAC setting(default)
- CHGCOIP : 3/4.5/6A based on current current setting
- BATOVIP : 103-106%
- BATLOWIP : 2.5V
- TSHTUT : 155C
- IFAULT HI : 750mV (default)
- IFAULT LOW : 110mV (default)

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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title		CHARGER		
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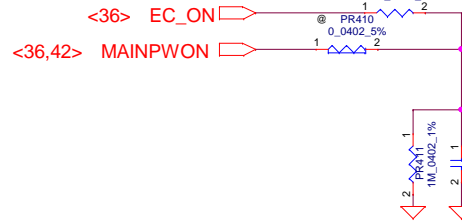
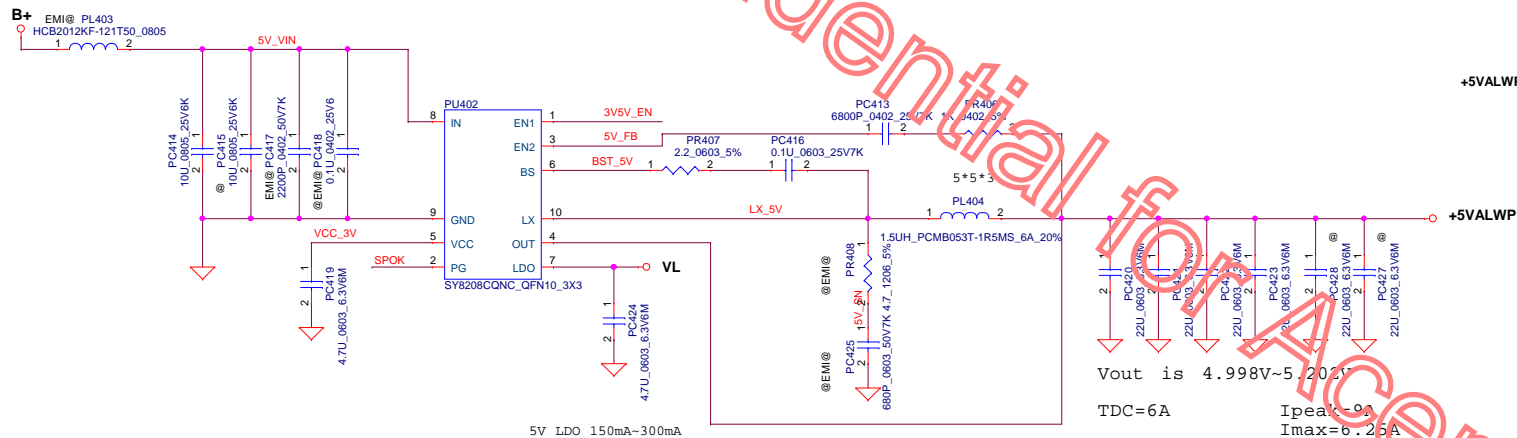
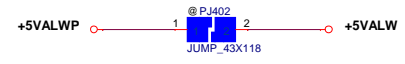
Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd

EN1 and EN2 dont't floating



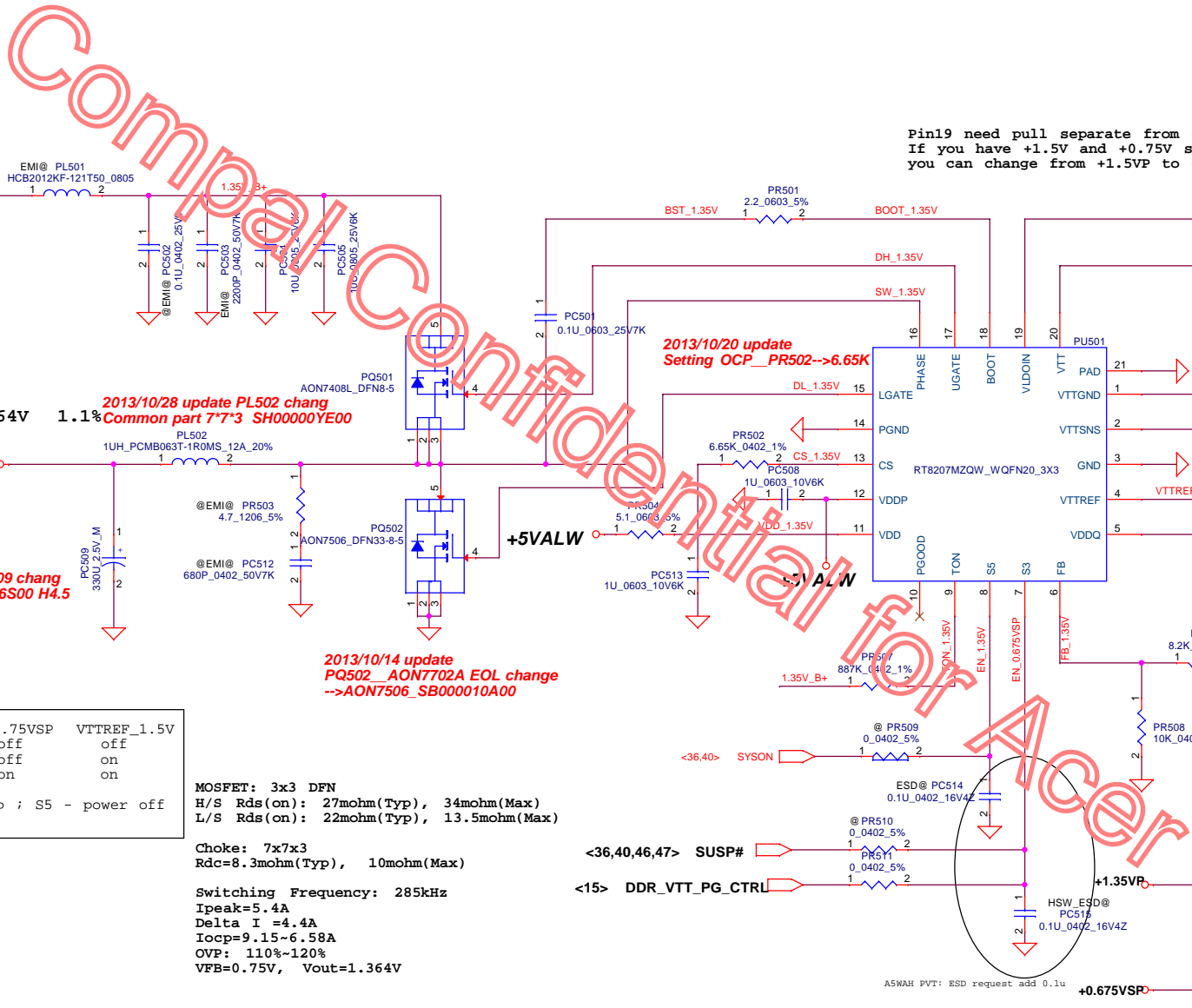
Check pull up resistor of SPOK at HW side



EC VDD0 is +3VL, PC426 UNPOP
EC VDD0 is +3VALW, PC426 POP

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				+3VALW/+5VALW	
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Module model information
 RT8207M_v1.mdd For Single layer
 RT8207M_V2.mdd For Dual layer



Pin19 need pull separate from +1.5VP.
 If you have +1.5V and +0.75V sequence question,
 you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
 TDC 0.7A
 Peak Current 1A

2013/10/28 update PL502 chang
 Common part 7*7*3 SH00000YE00

2013/10/20 update
 Setting OCP_PR502-->6.65K

2013/10/14 update
 PQ502_AON7702A EOL change
 -->AON7506_SB000010A00

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
 H/S Rds(on): 27mohm(Typ), 34mohm(Max)
 L/S Rds(on): 22mohm(Typ), 13.5mohm(Max)

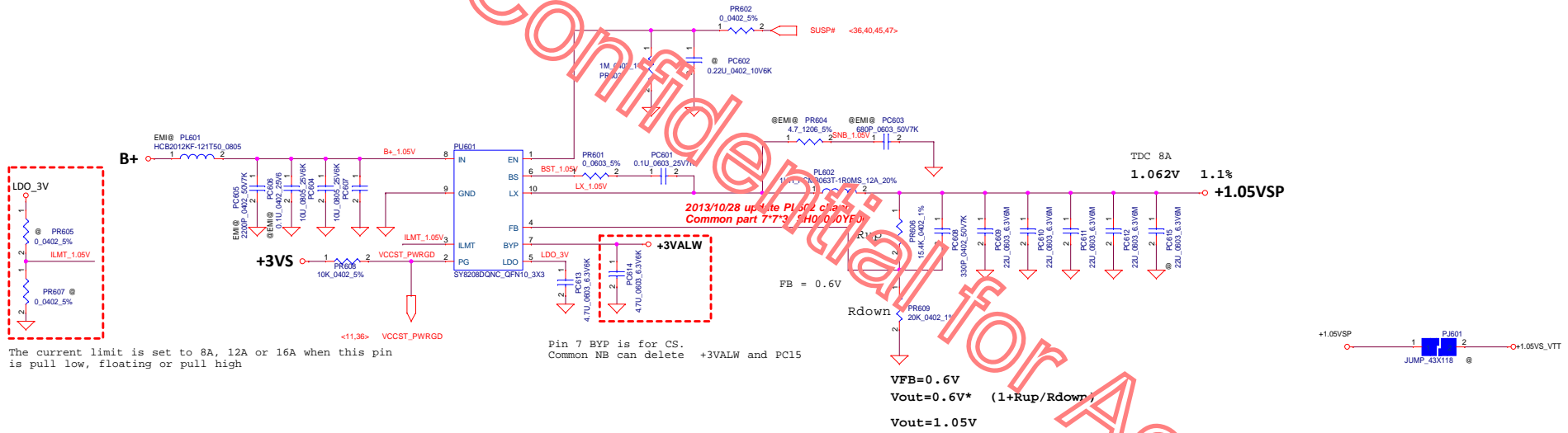
Choke: 7x7x3
 Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
 Ipeak=5.4A
 Delta I =4.4A
 Iocp=9.15-6.58A
 OVP= 110%-120%
 VFB=0.75V, Vout=1.364V

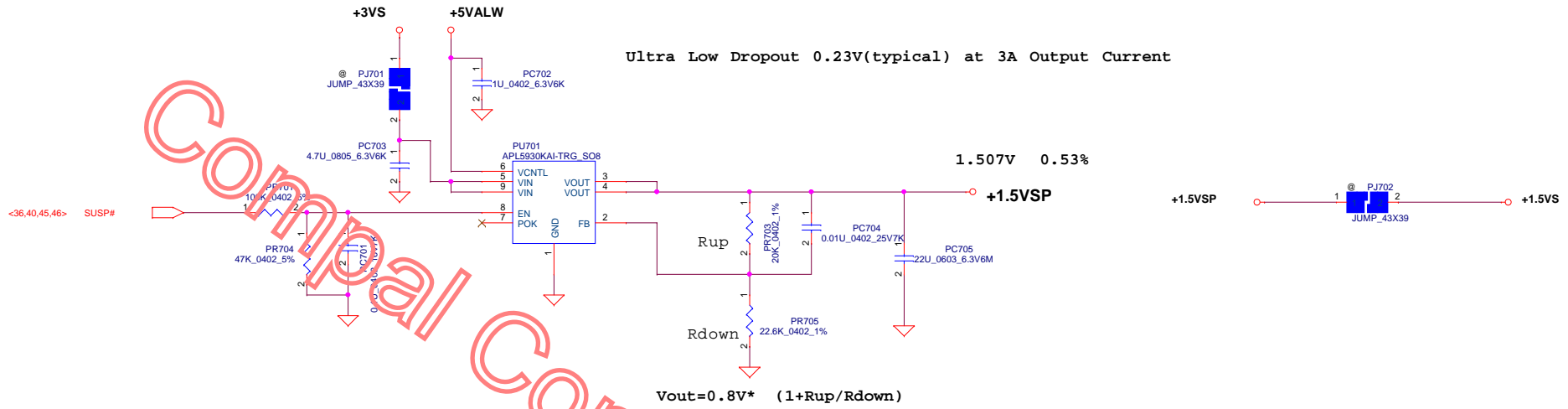
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Issued Date	2013/10/01	Deciphered Date	2014/05/24	Title	
				+1.35VP/+0.675VSP	
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Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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Ultra Low Dropout 0.23V(typical) at 3A Output Current

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				Document Number
				Rev
				1.0
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Module model information:
ISL95813 (for 15W & 28W CPU)

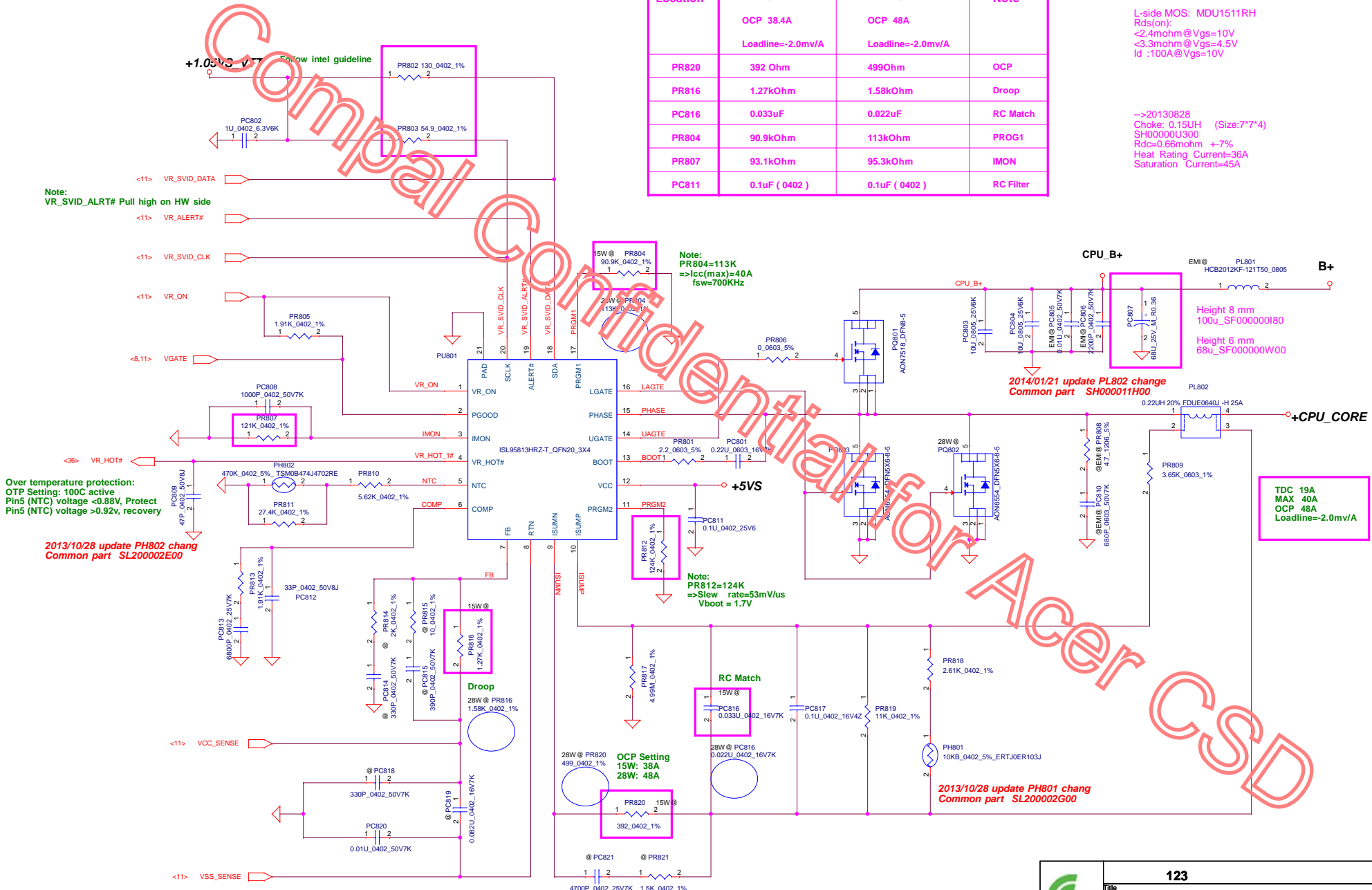
Base on BDW_PDDG_Rev_0_73

Location	15W	28W	Note
	TDC 14A MAX 32A OCP 38.4A Loadline=-2.0mV/A	TDC 19A MAX 40A OCP 48A Loadline=-2.0mV/A	
PR820	392 Ohm	499Ohm	OCP
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

-->20130828
Choke: 0.15uH (Size:77*4)
SH0000U300
Rdc=0.66mohm +7%
Heat Rating Current=36A
Saturation Current=45A



Note:
VR_SVID_ALERT# Pull high on HW side

Note:
PR804=113K
=>Icc(max)=40A
Isw=700KHz

Note:
PR812=124K
=>Slew rate=53mV/us
Vboot = 1.7V

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

2013/10/28 update PH802 chang
Common part SL200002E00

2014/01/21 update PL802 change
Common part SH000011H00

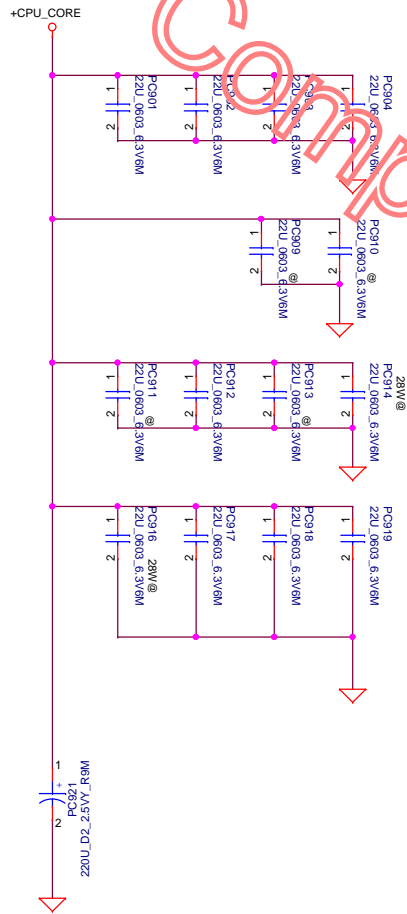
2013/10/28 update PH801 chang
Common part SL200002G00

Height 8 mm
100u_SF000000180
Height 6 mm
68u_SF000000W00

TDC 19A
MAX 40A
OCP 48A
Loadline=-2.0mV/A

Local sense put on HW site

PWR Rule
 需確認最新SPEC
 Modify 8/6.

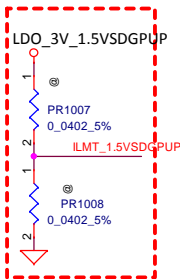
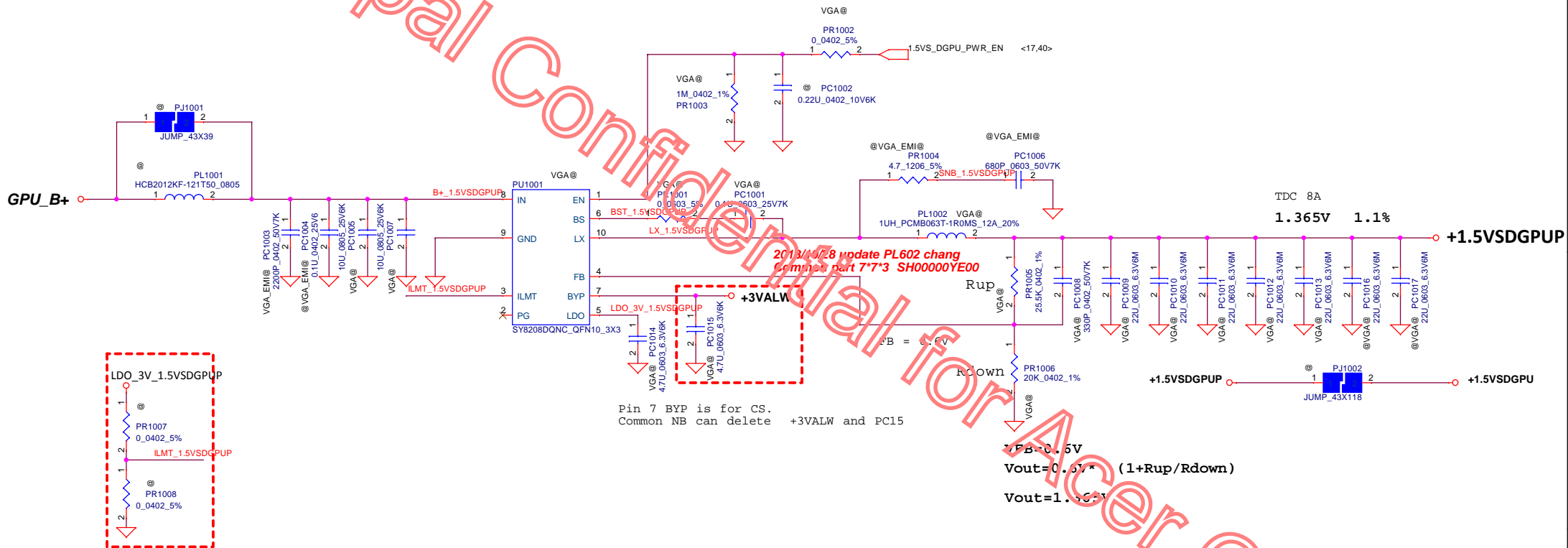


30 X 22uF 0805
 2012/10/23
 check the output cap Qty!!!
 2012/10/24
 23 pcs 22uF and reserve 7 pcs
 2013/01/14
 22uF*17 unpop:22uF*3

20130828
 15W: 22uF*14
 28W: 22uF*16

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				CPU CORE CAP	
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				Custom	1.0
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Compal Confidential for Acer CSD



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

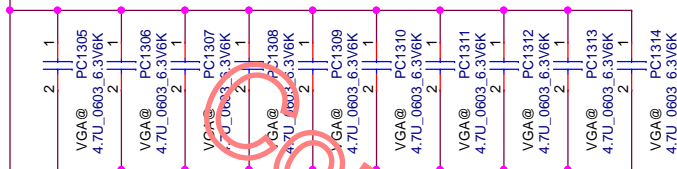
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

$$V_{out} = 0.5V \cdot (1 + R_{up}/R_{down})$$

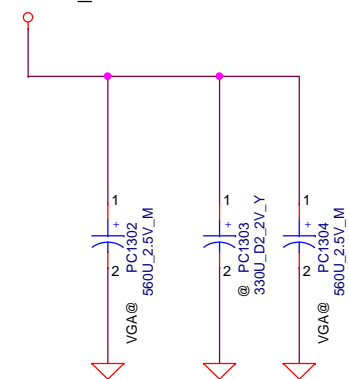
$$V_{out} = 1.5V$$

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+VGA_CORE Under VGA Core



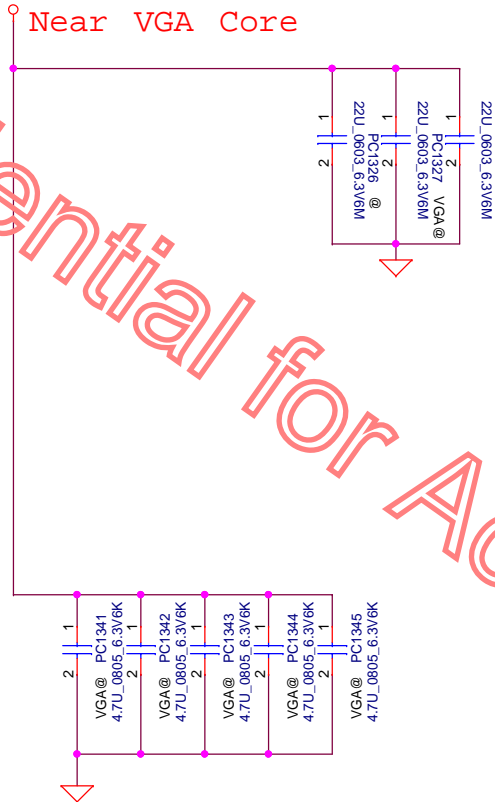
+VGA_CORE



N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

+VGA_CORE

Near VGA Core



N15x 2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x 2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x 2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Design Update	ESD request	P.42 P.43 P.45	Add PC204 330P_0402_50V7K SE074331K80 Add PC324 0.1U_0402_16V4Z SE070104Z80 Add PC514 PC515 0.1U_0402_16V4Z SE070104Z80	20140812	EVT
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